MS-7851

MIN ITX

Ver: 1.0(17x17)

Intel -SharkBay plamform Z87

CPU:

Haswell LGA1150

System Chipset:

Lynx Point Z87

Onboard Chip:

HD Audio Codec:ALC892
LAN-RTL8111G
SIO:Nuvoton 6779D
Flash ROM: SPI 64 MB

Main Memory:

*DDRIII (1066/1333/1600MHz) * 2 (Dual Channel)*

ACPI:

UPI

PWM:

UP1649 4 Phase

Expansion Slots:

*PCI Express (X16) Slot * 1*

Other:

SATA3.0 x4(PCH)
*REAL USB2.0 *2*
*FRONT USB2.0 *2*
*REAL USB3.0 *4*
*FRONT USB3.0 *2*

MICRO-STAR INT'L CO.,LTD

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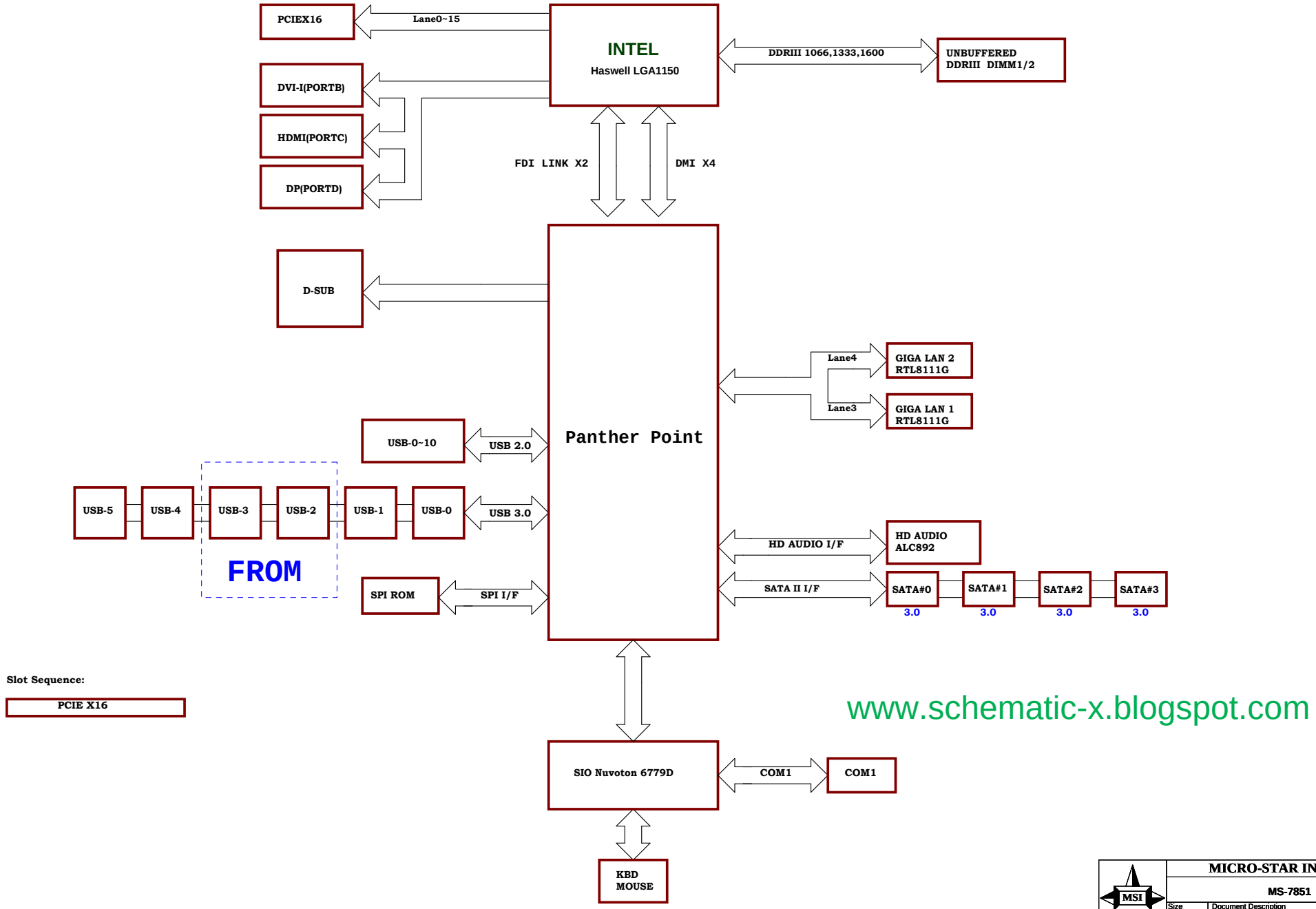
MS-7851 Block Diagram



MICRO-STAR INT'L CO.,LTD		
MS-7851		
Size: Custom	Document Description: Block Diagram	Rev: 10
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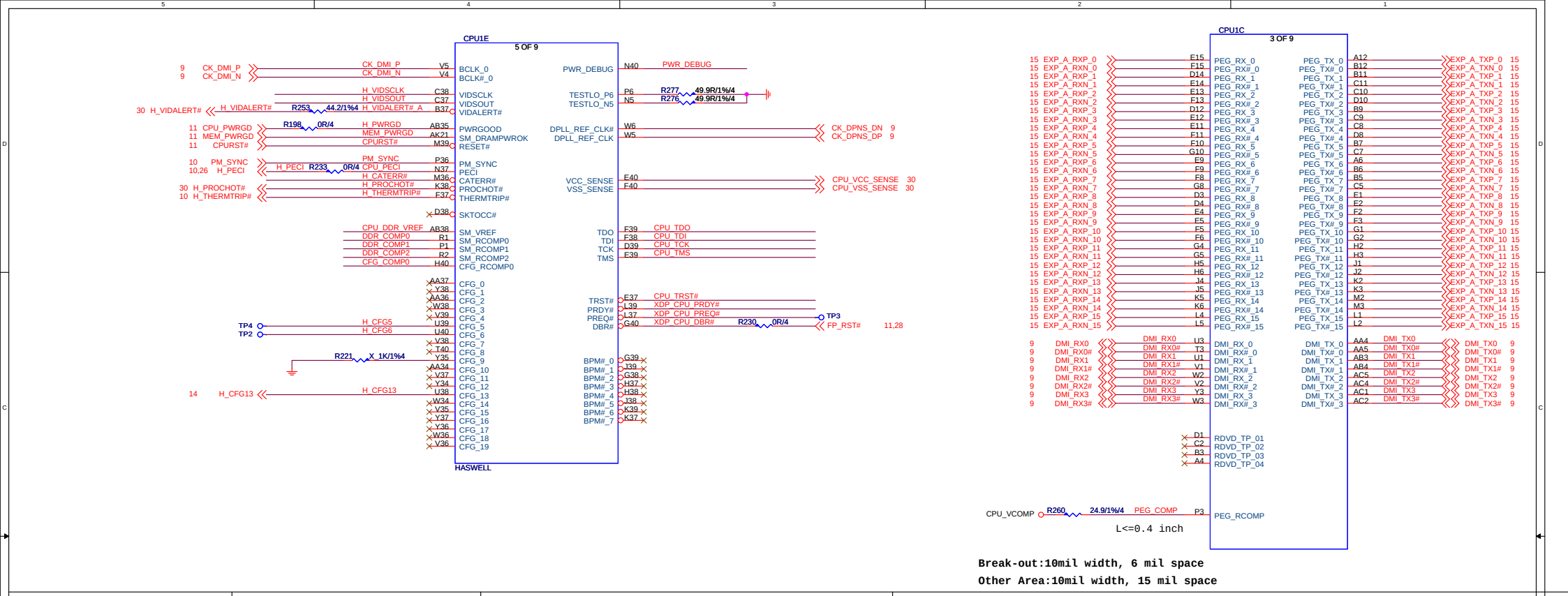
CPU1E
5 OF 9
HASWELL
CPU1C
3 OF 9
Break-out:10mil width, 6 mil space
Other Area:10mil width, 15 mil space
CPU_RESET#
CPURST# rise/fall time <6ns
0.98V?
CPU1D
4 OF 9
HASWELL
MICRO-STAR INT'L CO.,LTD
MS-7851
CPU-CNTL/CLK/MISC
Rev 10
Thursday, March 14, 2013
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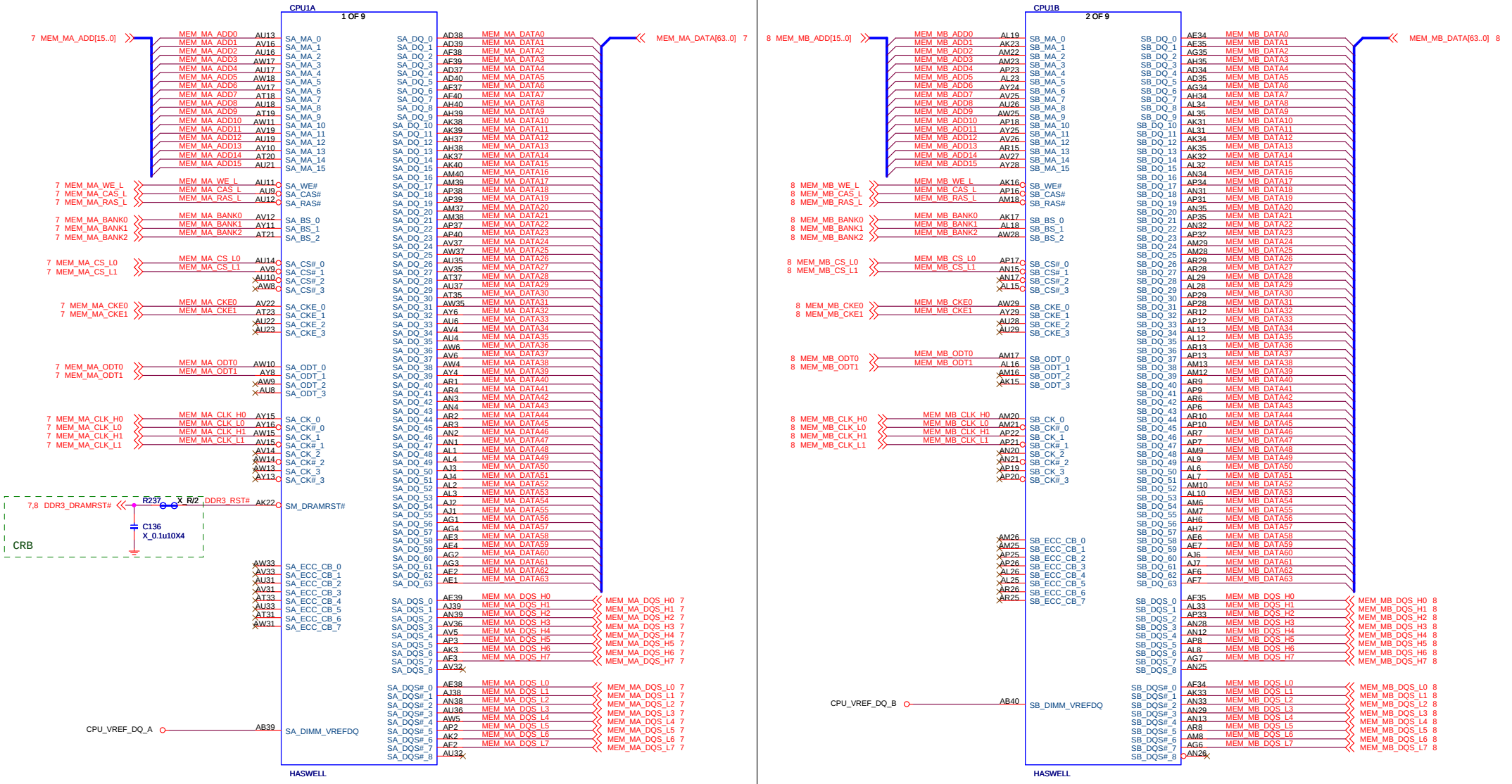

MICRO-STAR INT'L CO.,LTD	
MS-7851	
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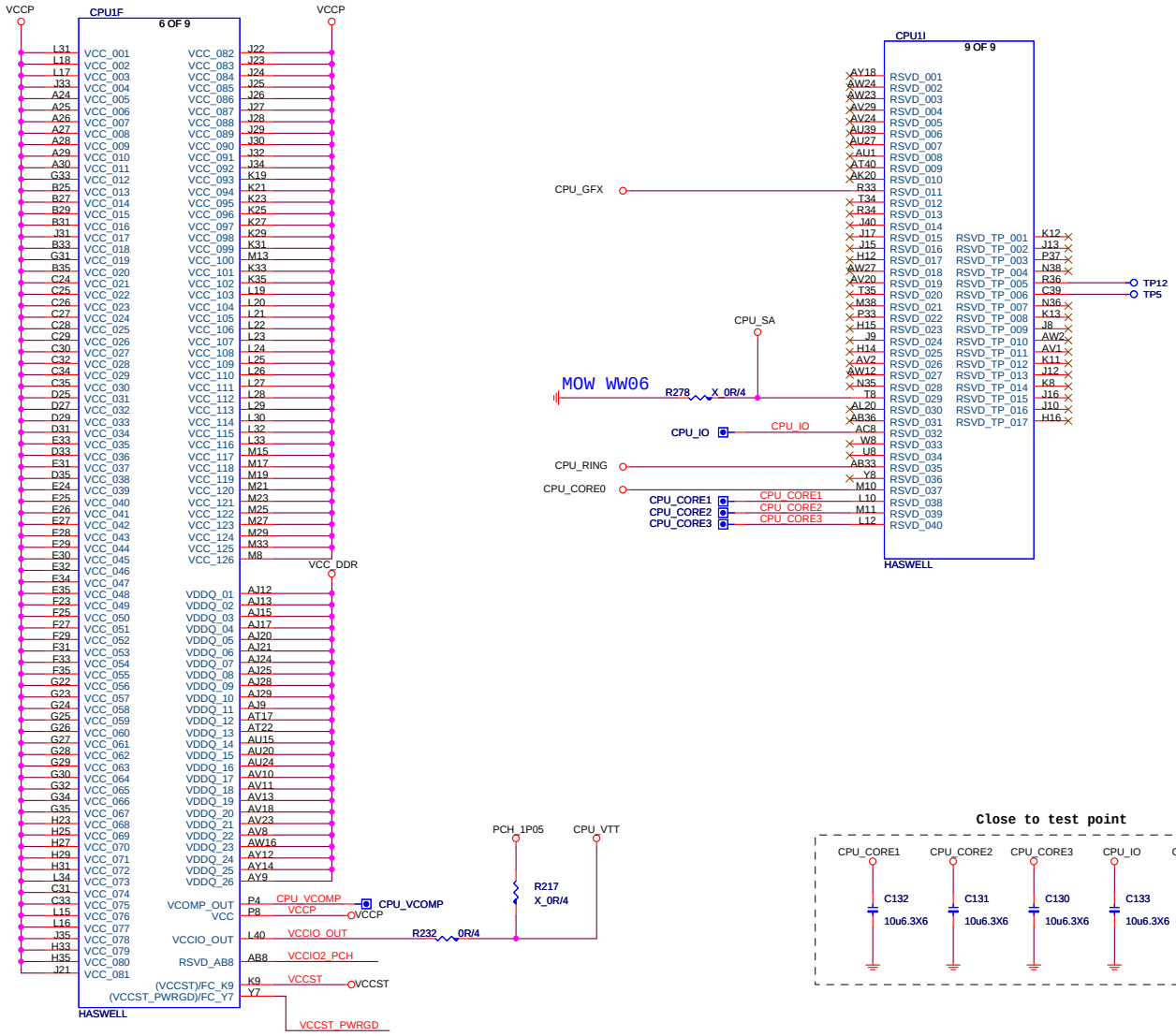
CPU1F
6 OF 9
HASWELL
VCCP
VCC_DDR
VCC_001
VCC_002
VCC_003
VCC_004
VCC_005
VCC_006
VCC_007
VCC_008
VCC_009
VCC_010
VCC_011
VCC_012
VCC_013
VCC_014
VCC_015
VCC_016
VCC_017
VCC_018
VCC_019
VCC_020
VCC_021
VCC_022
VCC_023
VCC_024
VCC_025
VCC_026
VCC_027
VCC_028
VCC_029
VCC_030
VCC_031
VCC_032
VCC_033
VCC_034
VCC_035
VCC_036
VCC_037
VCC_038
VCC_039
VCC_040
VCC_041
VCC_042
VCC_043
VCC_044
VCC_045
VCC_046
VCC_047
VCC_048
VCC_049
VCC_050
VCC_051
VCC_052
VCC_053
VCC_054
VCC_055
VCC_056
VCC_057
VCC_058
VCC_059
VCC_060
VCC_061
VCC_062
VCC_063
VCC_064
VCC_065
VCC_066
VCC_067
VCC_068
VCC_069
VCC_070
VCC_071
VCC_072
VCC_073
VCC_074
VCC_075
VCC_076
VCC_077
VCC_078
VCC_079
VCC_080
VCC_081
VCC_082
VCC_083
VCC_084
VCC_085
VCC_086
VCC_087
VCC_088
VCC_089
VCC_090
VCC_091
VCC_092
VCC_093
VCC_094
VCC_095
VCC_096
VCC_097
VCC_098
VCC_099
VCC_100
VCC_101
VCC_102
VCC_103
VCC_104
VCC_105
VCC_106
VCC_107
VCC_108
VCC_109
VCC_110
VCC_111
VCC_112
VCC_113
VCC_114
VCC_115
VCC_116
VCC_117
VCC_118
VCC_119
VCC_120
VCC_121
VCC_122
VCC_123
VCC_124
VCC_125
VCC_126
VDDQ_01
VDDQ_02
VDDQ_03
VDDQ_04
VDDQ_05
VDDQ_06
VDDQ_07
VDDQ_08
VDDQ_09
VDDQ_10
VDDQ_11
VDDQ_12
VDDQ_13
VDDQ_14
VDDQ_15
VDDQ_16
VDDQ_17
VDDQ_18
VDDQ_19
VDDQ_20
VDDQ_21
VDDQ_22
VDDQ_23
VDDQ_24
VDDQ_25
VDDQ_26
VCOMP_OUT
VCC
VCCIO_OUT
RSVD_AB8
(VCCST)/FC_K9
(VCCST_PWRGD)/FC_Y7
CPU_VCOMP
CPU_VCOMP
VCCP
VCCIO_OUT
VCCIO2_PCH
VCCST
VCCST
VCCST_PWRGD
R232 0R/4
PCH_1P05
CPU_VTT
R217
X_0R/4
CPU1I
9 OF 9
HASWELL
RSVD_001
RSVD_002
RSVD_003
RSVD_004
RSVD_005
RSVD_006
RSVD_007
RSVD_008
RSVD_009
RSVD_010
RSVD_011
RSVD_012
RSVD_013
RSVD_014
RSVD_015
RSVD_016
RSVD_017
RSVD_018
RSVD_019
RSVD_020
RSVD_021
RSVD_022
RSVD_023
RSVD_024
RSVD_025
RSVD_026
RSVD_027
RSVD_028
RSVD_029
RSVD_030
RSVD_031
RSVD_032
RSVD_033
RSVD_034
RSVD_035
RSVD_036
RSVD_037
RSVD_038
RSVD_039
RSVD_040
RSVD_TP_001
RSVD_TP_002
RSVD_TP_003
RSVD_TP_004
RSVD_TP_005
RSVD_TP_006
RSVD_TP_007
RSVD_TP_008
RSVD_TP_009
RSVD_TP_010
RSVD_TP_011
RSVD_TP_012
RSVD_TP_013
RSVD_TP_014
RSVD_TP_015
RSVD_TP_016
RSVD_TP_017
TP12
TP5
CPU_GFX
CPU_SA
MOW WW06
R278 X_0R/4
CPU_IO
CPU_IO
CPU_RING
CPU_CORE0
CPU_CORE1
CPU_CORE2
CPU_CORE3
CPU_CORE1
CPU_CORE2
CPU_CORE3
Close to test point
CPU_CORE1
CPU_CORE2
CPU_CORE3
CPU_IO
CPU_VCOMP
C132 10u6.3X6
C131 10u6.3X6
C130 10u6.3X6
C133 10u6.3X6
C205 10u6.3X6
+1.5V_DDR3-Decoupling
VCC_DDR
C195 22u6.3X8
C185 22u6.3X8
C160 22u6.3X8
C166 22u6.3X8
C169 22u6.3X8
C172 22u6.3X8
C175 22u6.3X8
C182 22u6.3X8
C189 22u6.3X8
CPU SOCKET CAVITY 0805CAPS
+CPU_VCCP-Decoupling
VCCP
C164 22u6.3X8
C176 22u6.3X8
C170 22u6.3X8
C158 22u6.3X8
C167 22u6.3X8
C159 22u6.3X8
C408 22u6.3X8
C407 22u6.3X8
C406 22u6.3X8
C405 22u6.3X8
C180 22u6.3X8
C183 22u6.3X8
C187 22u6.3X8
C193 22u6.3X8
C194 22u6.3X8
PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY
3VSB
R305 47K/4
VCCST
R290 47K/4
Q12
2N7002D
CP_PGD#
VCCST_PWRGD
10,11,26,30 CHIP_PWGD
R304 10K/4
C168 0.1u10X4
VCCIO2_PCH
R291 X_0R/4
V_PROC_IO
VCCST
R292 0R/4
PCH_1P05
R465 0R/4
VCCST
C213 0.1u16X4
C212 4.7u6.3X8
CRB 1.0
MICRO-STAR INT'L CO.,LTD
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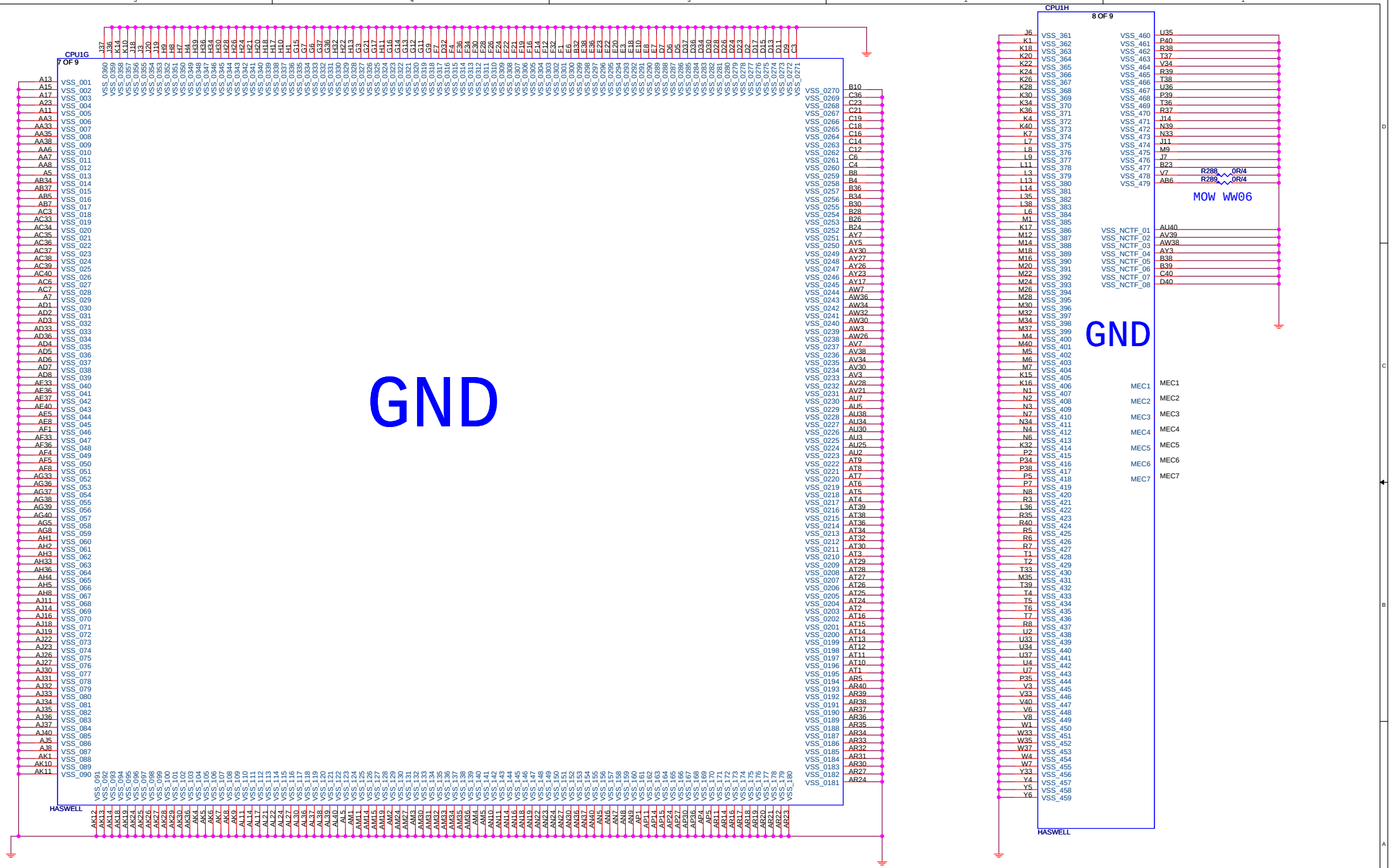

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MS-7851	
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Rev: 10	
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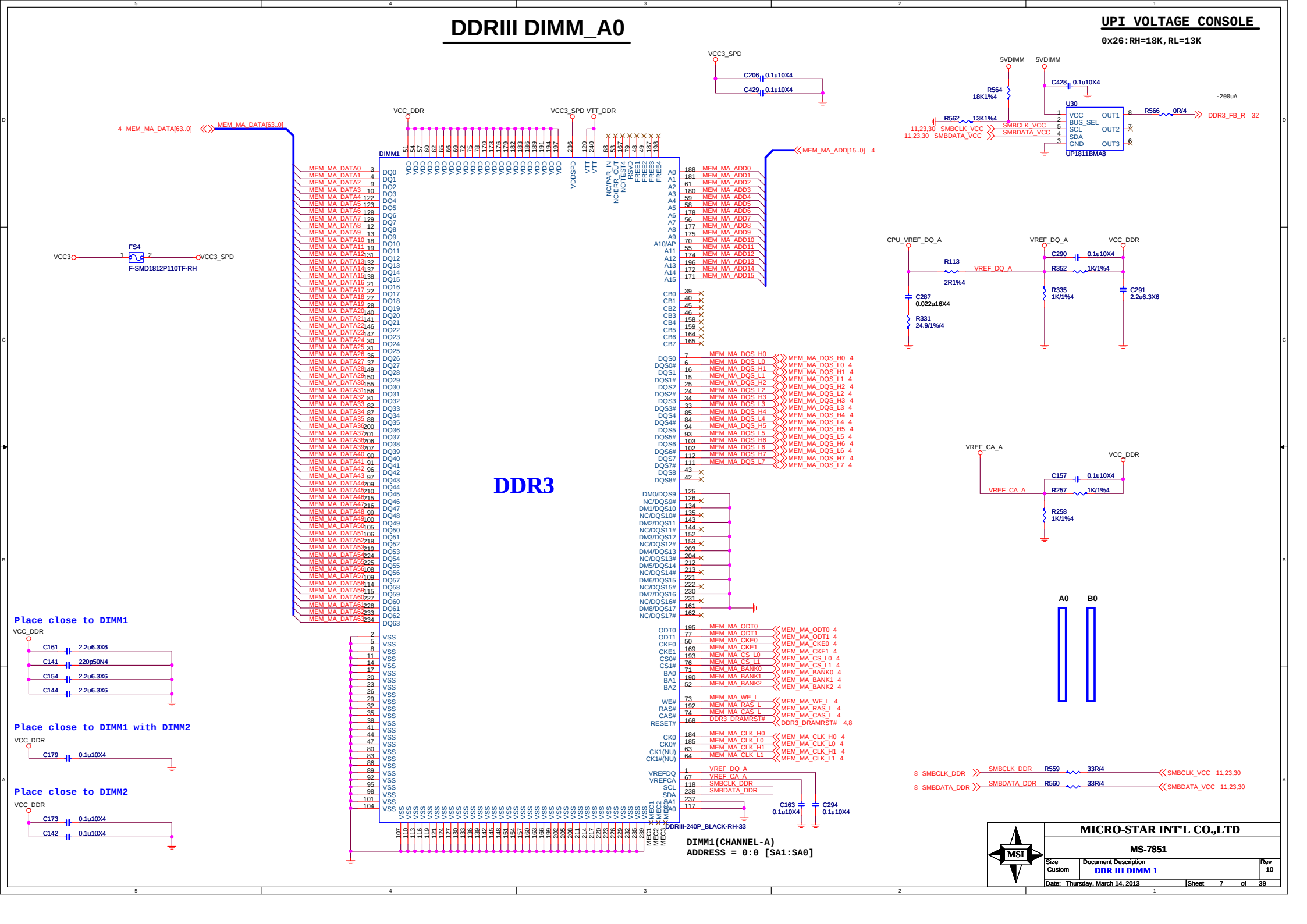
DDRIII DIMM_A0

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: DDR III DIMM 1
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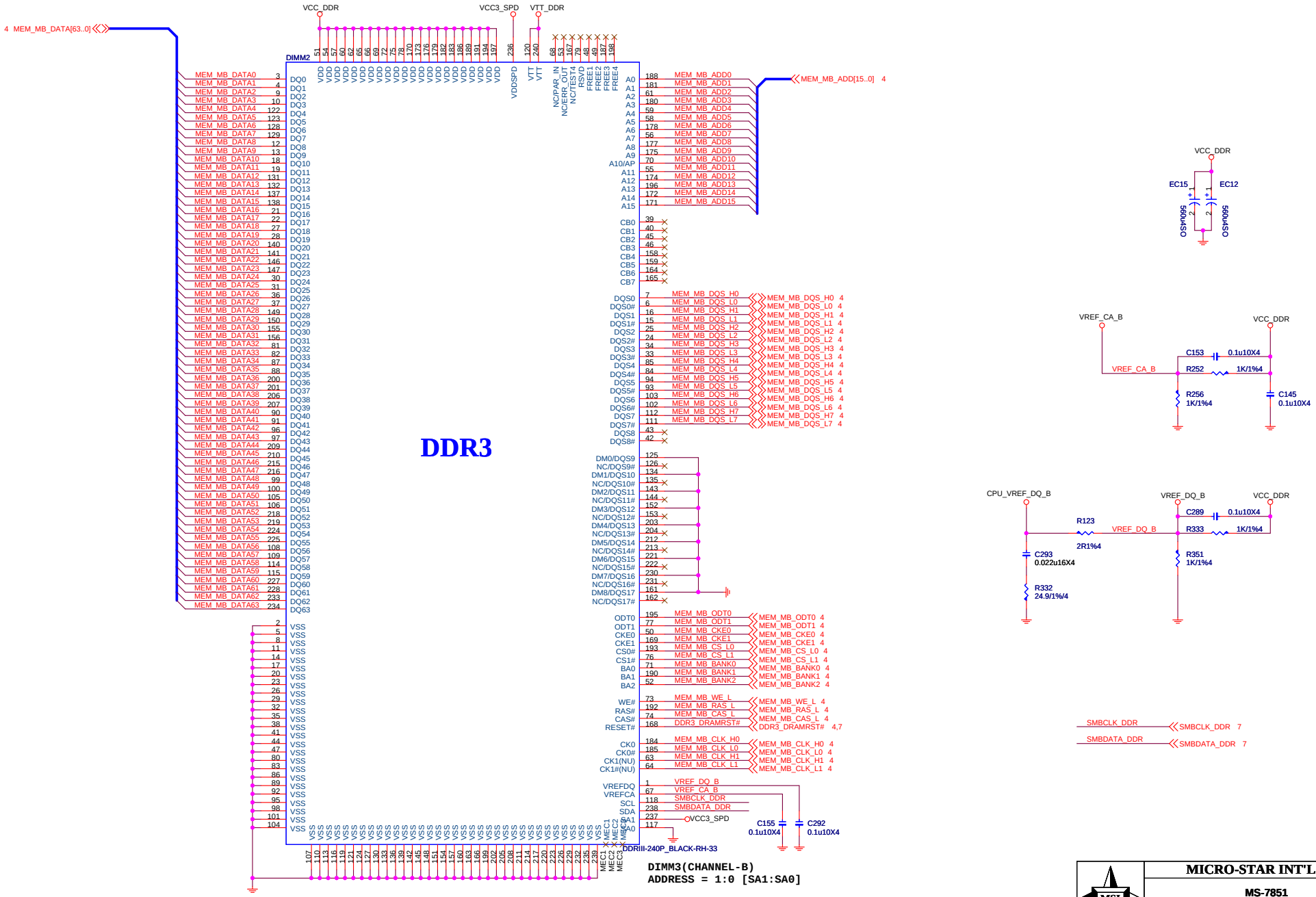
DDRIII DIMM_B0



MICRO-STAR INT'L CO.,LTD		
MS-7851		
Size: Custom	Document Description: DDR III DIMM 2	Rev: 10
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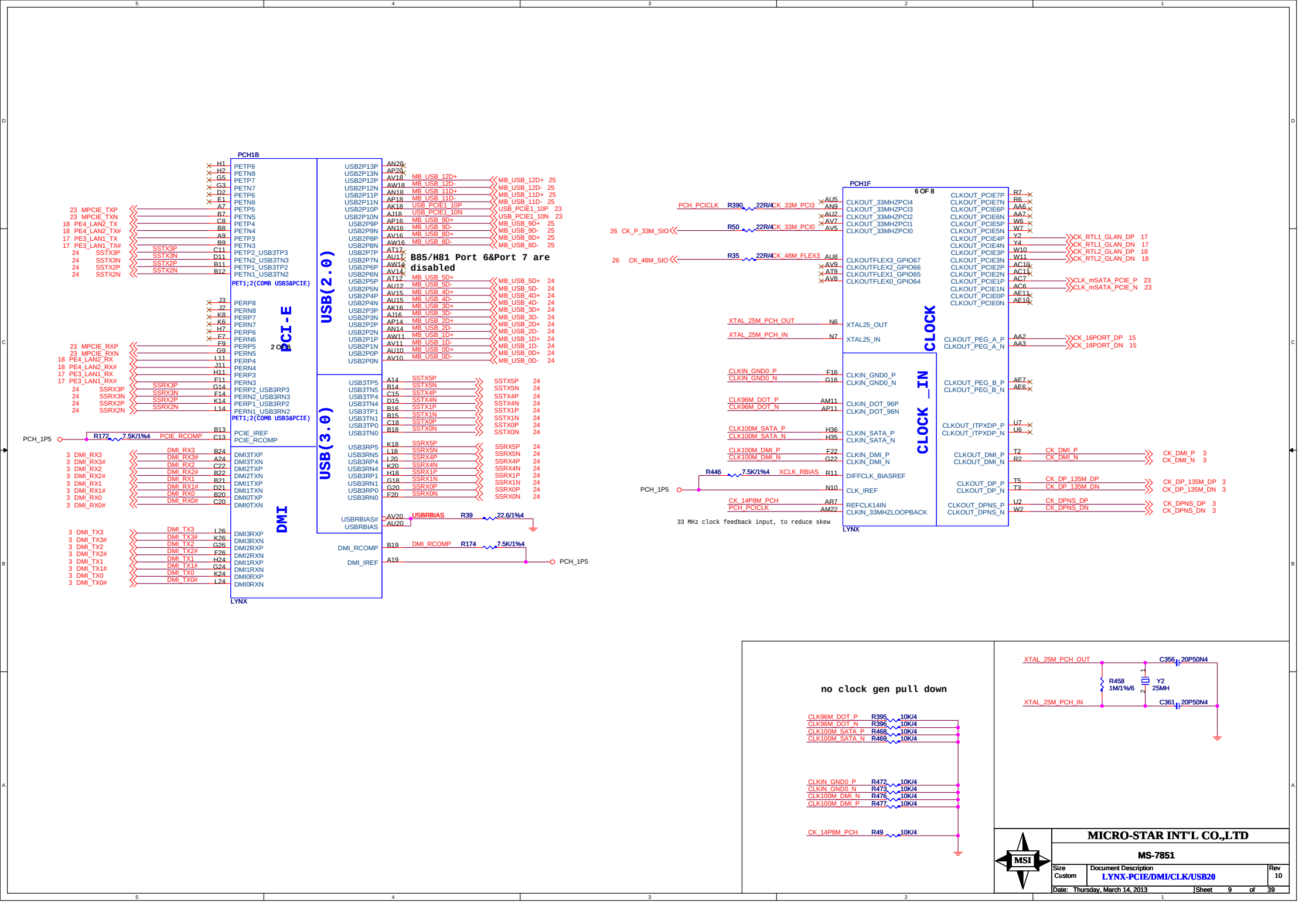
PCH1B
PCI-E
2 OF 8
USB(2.0)
USB(3.0)
DMI
LYNX
B85/H81 Port 6&Port 7 are disabled
PCH1F
6 OF 8
CLOCK
CLOCK_IN
33 MHz clock feedback input, to reduce skew
no clock gen pull down
MICRO-STAR INT'L CO.,LTD
MS-7851
LYNX-PCIE/DMI/CLK/USB20
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SATA port
Z87,H87:Port 0 ~ 5 are SATA 6G
B85: Port 0, 1, 2, 3 are SATA 6G
H81: Port 0, 1 are SATA 6G
B85,H81: Port 4,5 are SATA 3G

Z87->Stuff R376
H87、B85->Stuff R363

PCH1C

CLINK
FAN
GPIO
SATA
HOST

3 OF8
LYNX

SATA4;5(COMB SATA&PCIE)

PCH1E

VGA
FDILINK
DISPLAY
PORT B
PORT C
PORT D
eDP CONTROL

LYNX

PCH1A

PIRQ&GPIO

1 OF8
LYNX

Some condition control for BIOS use

output pin

Close to PCH within 250 mils.

Company	MICRO-STAR INT'L CO.,LTD
Model	MS-7851
Size	Custom
Document Description	LYNX-SATA/HOST/GPIO/VGA
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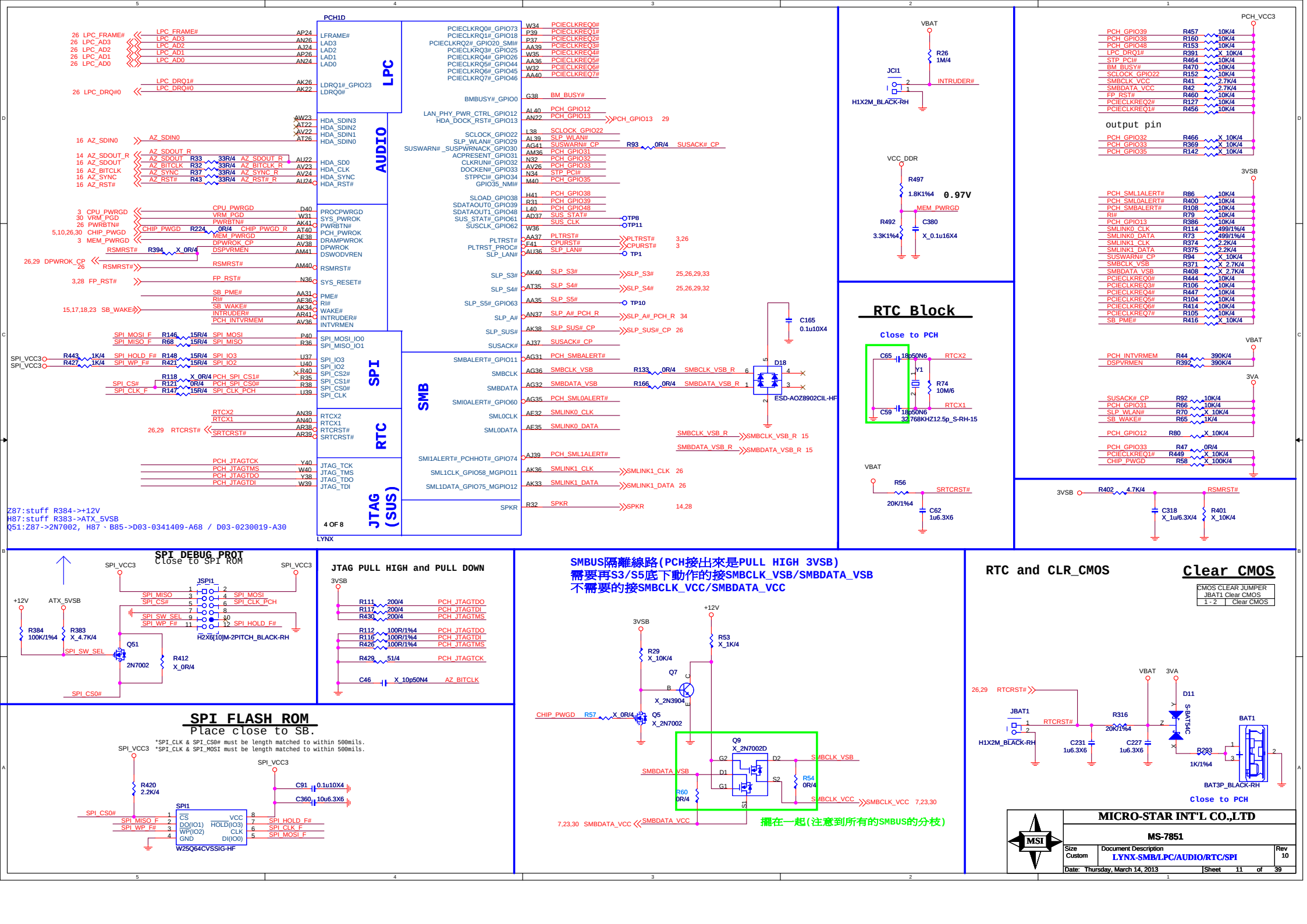
PCH1D
LPC
AUDIO
SPI
SMB
RTC
JTAG (SUS)
LYNX
4 OF 8
Z87:stuff R384->+12V
H87:stuff R383->ATX_5VSB
Q51:Z87->2N7002, H87、B85->D03-0341409-A68 / D03-0230019-A30
RTC Block
Close to PCH
output pin
SPI DEBUG PROT
Close to SPI ROM
JTAG PULL HIGH and PULL DOWN
SMBUS隔離線路(PCH接出來是PULL HIGH 3VSB)
需要再S3/S5底下動作的接SMBCLK_VSB/SMBDATA_VSB
不需要的接SMBCLK_VCC/SMBDATA_VCC
擺在一起(注意到所有的SMBUS的分枝)
SPI FLASH ROM
Place close to SB.
*SPI_CLK & SPI_CS0# must be length matched to within 500mils.
*SPI_CLK & SPI_MOSI must be length matched to within 500mils.
RTC and CLR_CMOS
Clear CMOS
CMOS CLEAR JUMPER
JBAT1 Clear CMOS
1 - 2 Clear CMOS
Close to PCH
MICRO-STAR INT'L CO.,LTD
MS-7851
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Document Description LYNX-SMB/LPC/AUDIO/RTC/SPI
Rev 10
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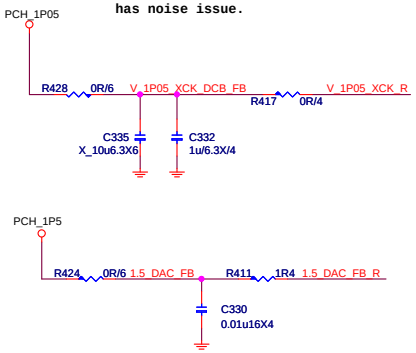
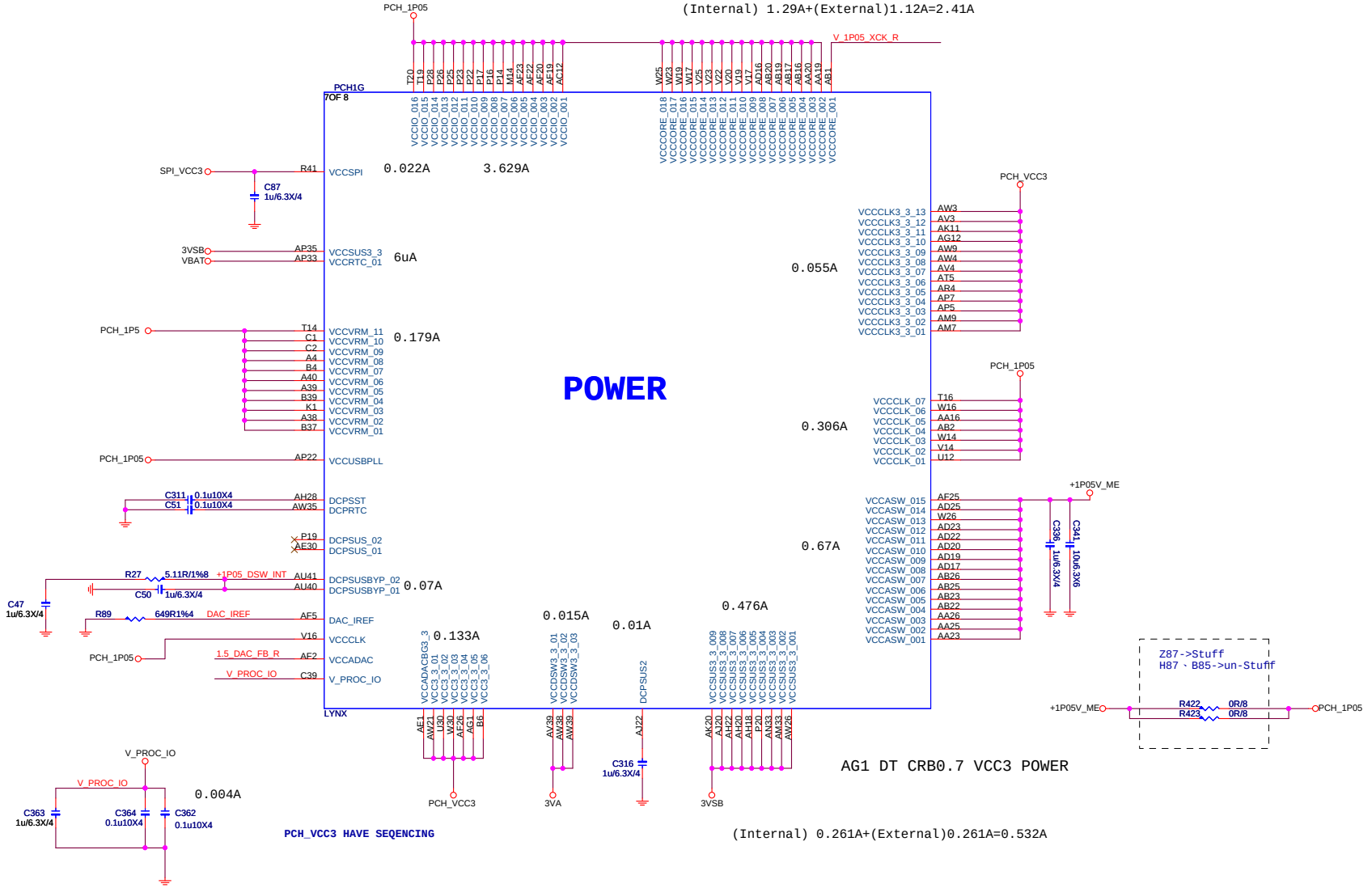
Change to 10UH if
VCCA_DPLLA/VCCA_DPLLB
has noise issue.



VCC3	0.21A
3VA	0.015A
VBAT	6uA
3VSB	0.261A
VCC1_5	0.249A
PCH_1P05	5.747A

AF25 ;AD25 DT CRB0.7 ASW POWER

(Internal) 1.29A+(External)1.12A=2.41A

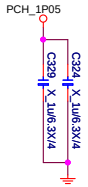


PCH_VCC3 HAVE SEQENCING

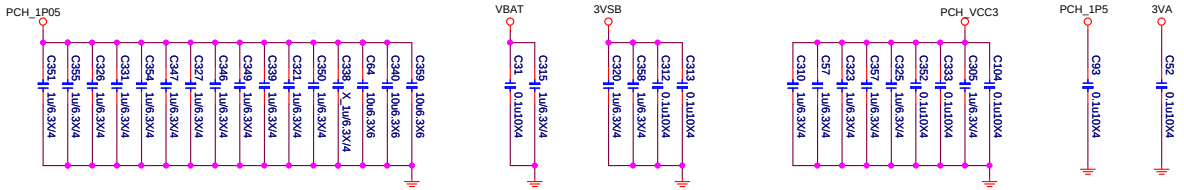
(Internal) 0.261A+(External)0.261A=0.532A

AG1 DT CRB0.7 VCC3 POWER

Backside for V14,U12,T16,V16
unstuff



PCH decoupling cap



MICRO-STAR INT'L CO.,LTD

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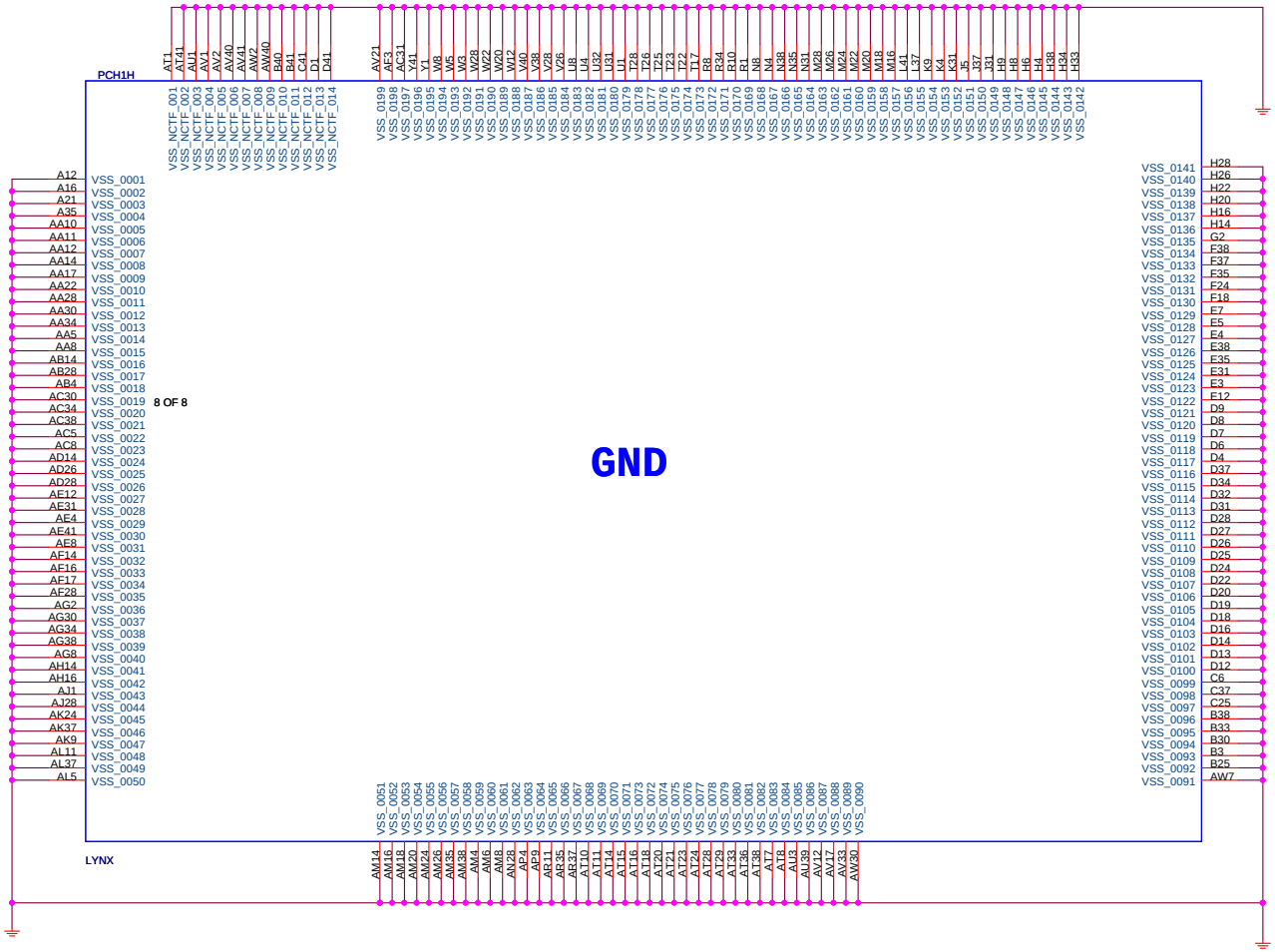

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Size: Custom	Document Description: LYNX-GND/NVRAM/USB30	Rev: 10
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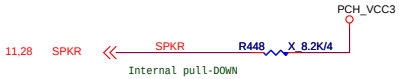
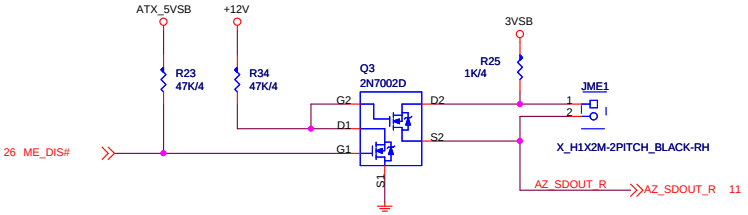
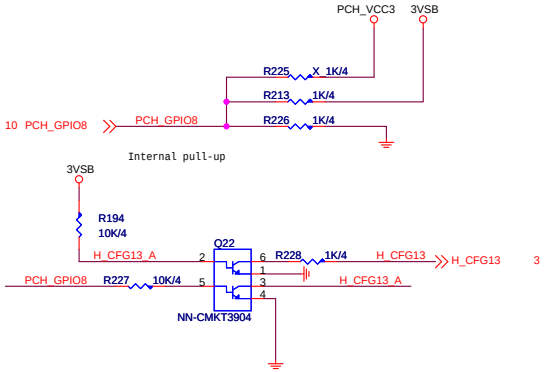


SPKR
Default Mode:
Internal weak Pull-down.

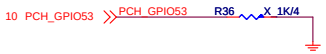
No Reboot Mode with TCO Disabled:
Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.



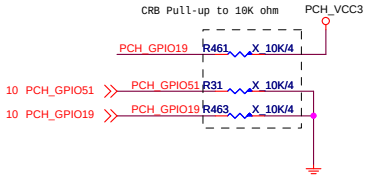


GPIO55
Default Mode:
Internal pull-up.

Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.



GPIO53
Connect to ground with 1k Ohm pull-down resistor.



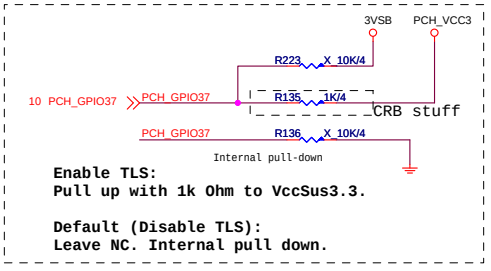
Default (SPI):
Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.

Boot from PCI:
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

Boot from LPC:
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

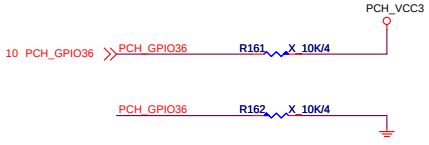
BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1

Default



Enable TLS:
Pull up with 1k Ohm to VccSus3.3.

Default (Disable TLS):
Leave NC. Internal pull down.



MICRO-STAR INT'L CO.,LTD

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Custom	LYNX-Strap	10

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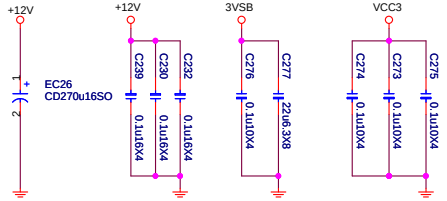

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Size: Custom	Document Description: PCIE1(X16) Slots	Rev: 10
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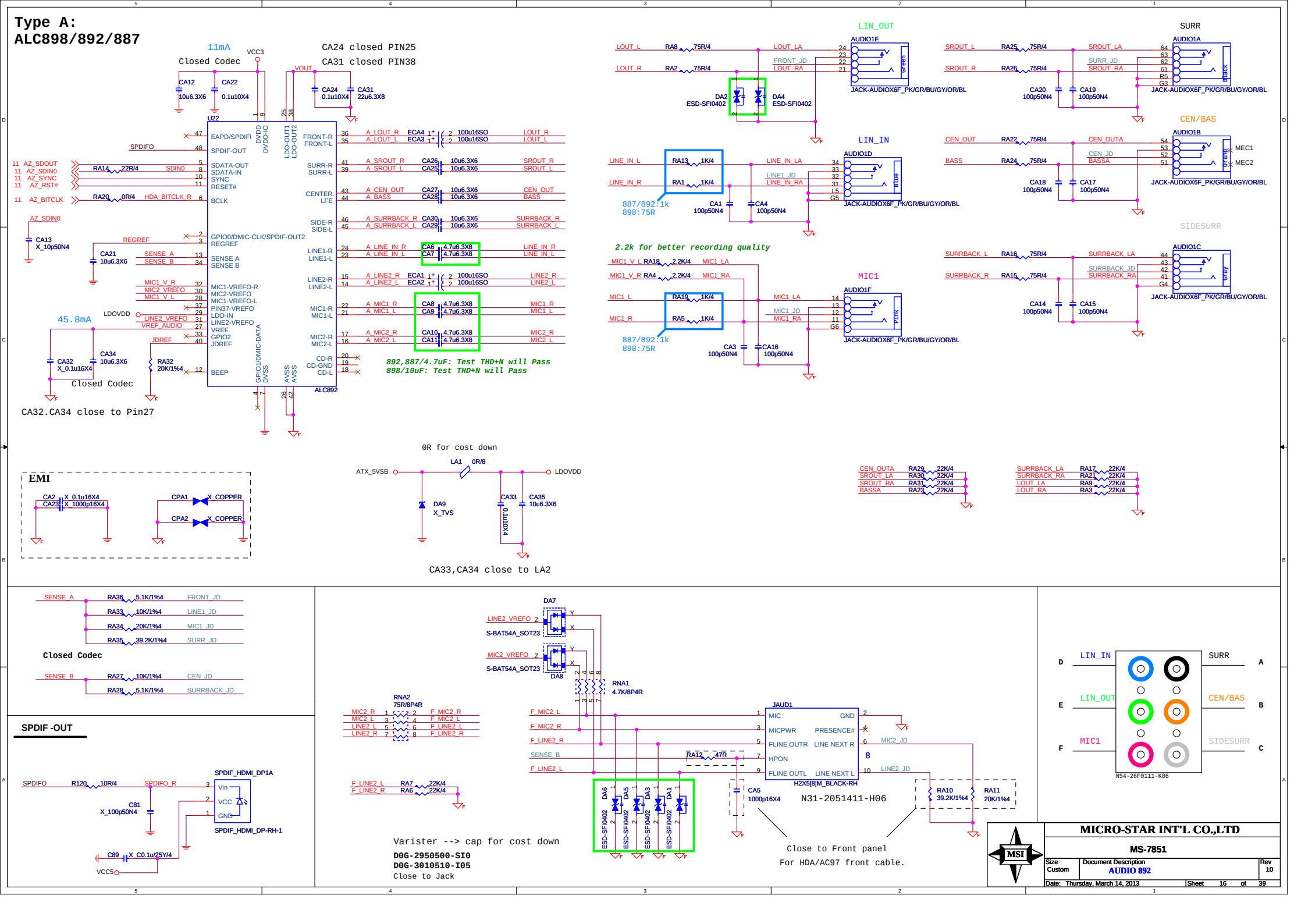
Type A:
ALC898/892/887

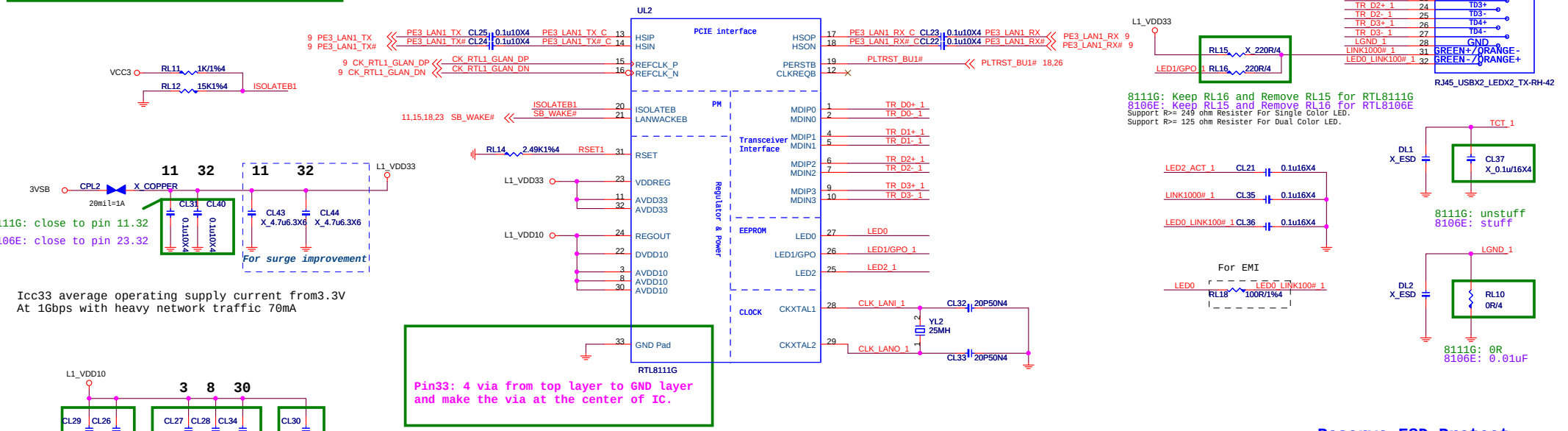


RTL8111G Giga LAN

RTL8106E 10/100M LAN

L1_VDD33 — RL13 X_10K/4 SB_WAKE#

Remove pull-up R if R existence on motherboard
(or SB has internal pull-up R).



VCC3 — RL11 1K/1%4 — RL12 15K1%4 — ISOLATEB1

RL14 2.49K1%4 — RSET1

3VSB — CPL2 X_COPPER 20mil=1A

11 32 — CL31 CL40 0.1u10X4

11 32 — CL43 X_4.7u6.3X6 — CL44 X_4.7u6.3X6

For surge improvement

8111G: close to pin 11.32
8106E: close to pin 23.32

Icc33 average operating supply current from3.3V
At 1Gbps with heavy network traffic 70mA

Pin33: 4 via from top layer to GND layer and make the via at the center of IC.

L1_VDD10 — 3 8 30 — CL29 CL26 1u10X4 — CL27 CL28 CL34 0.1u10X4 — CL30 0.1u10X4

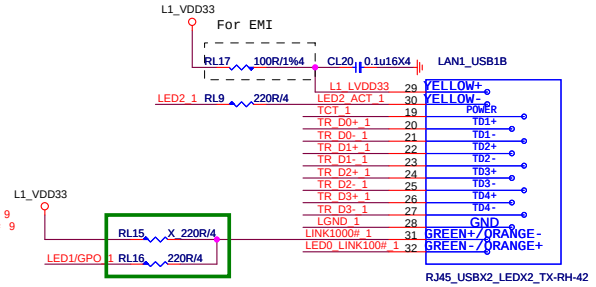
22

8111G: close to pin 22 8111G: close to pin 3.8.30 8111G: LDO mode close to pin 24
8106E: close to pin 30 8106E: close to pin 8.30 8106E: unstuff

30

Icc10 average operating supply current from1.0V
At 1Gbps with heavy network traffic 300mA

LAN Connector



L1_VDD33 — RL15 X_220R/4 — LED1/GPO_1 RL16 220R/4

8111G: Keep RL16 and Remove RL15 for RTL8111G
8106E: Keep RL15 and Remove RL16 for RTL8106E
Support R>= 249 ohm Resister For Single Color LED.
Support R>= 125 ohm Resister For Dual Color LED.

LED2_ACT_1 CL21 0.1u16X4
LINK1000#_1 CL35 0.1u16X4
LED0_LINK100#_1 CL36 0.1u16X4

For EMI
LED0 RL18 100R/1%4 LED0_LINK100#_1

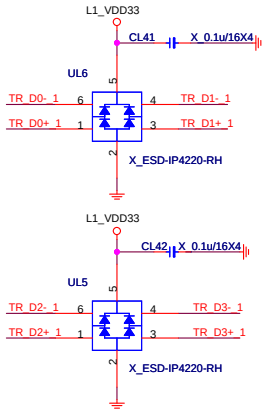
TCT_1 — DL1 X_ESD — CL37 X_0.1u/16X4

8111G: unstuff
8106E: stuff

LGND_1 — DL2 X_ESD — RL10 0R/4

8111G: 0R
8106E: 0.01uF

Reserve ESD Protect



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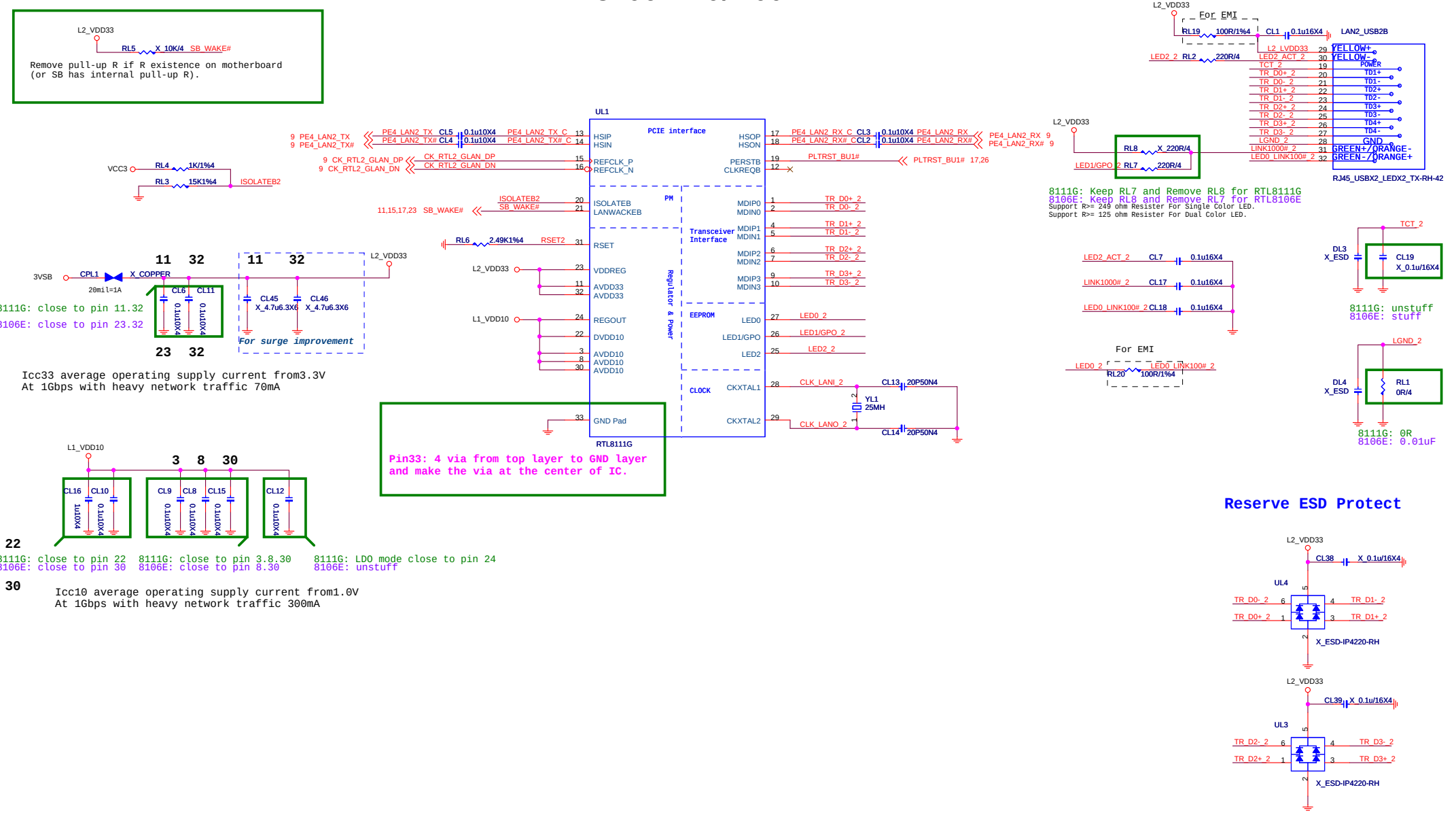
RTL8111G Giga LAN
RTL8106E 10/100M LAN

LAN Connector



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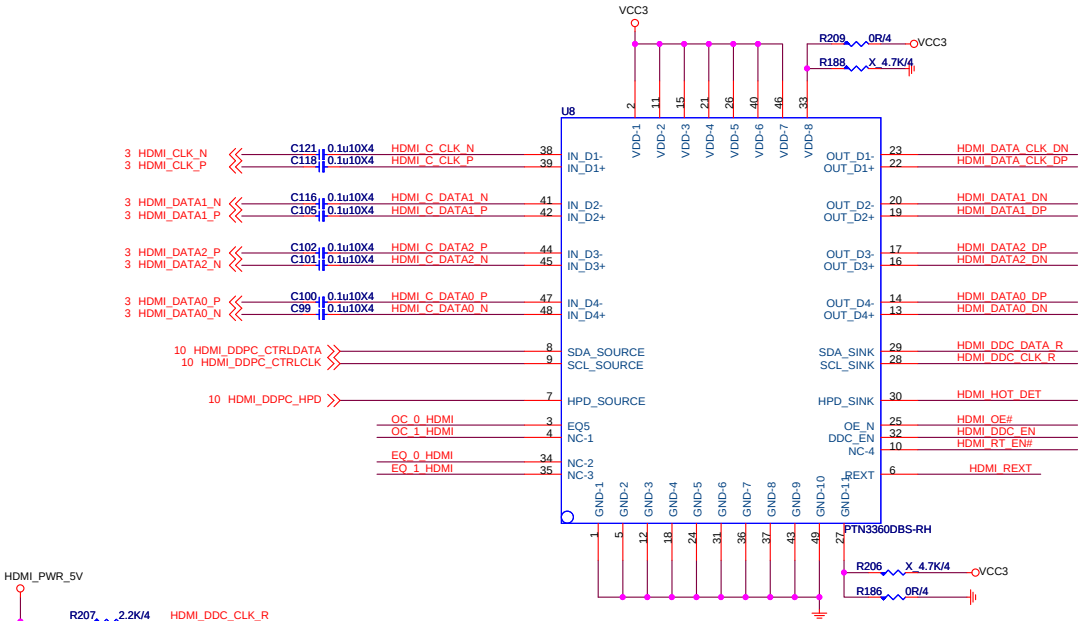
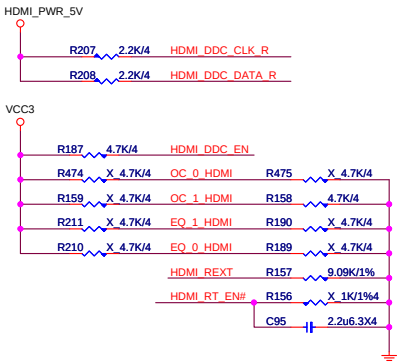
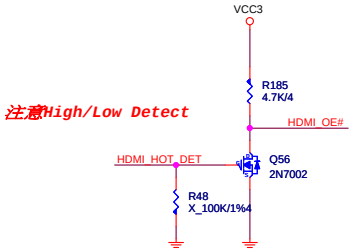
HDMI level shifter







	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

EMI

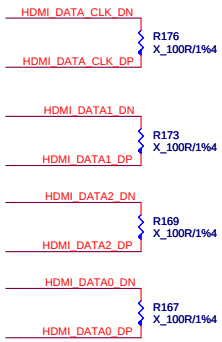
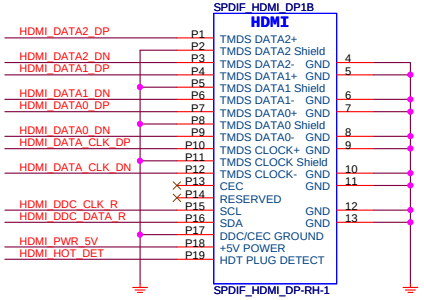
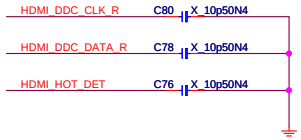


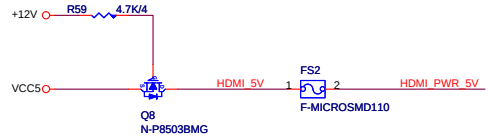
Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

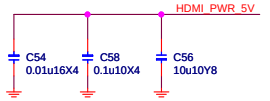
Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	

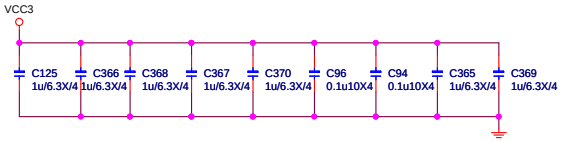


EMI cap.









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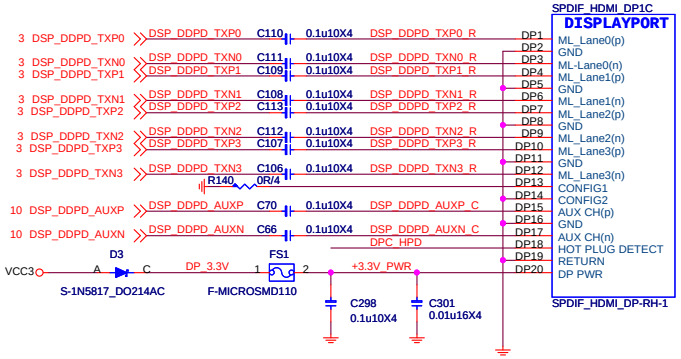
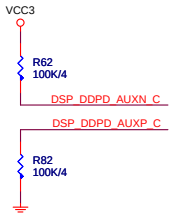
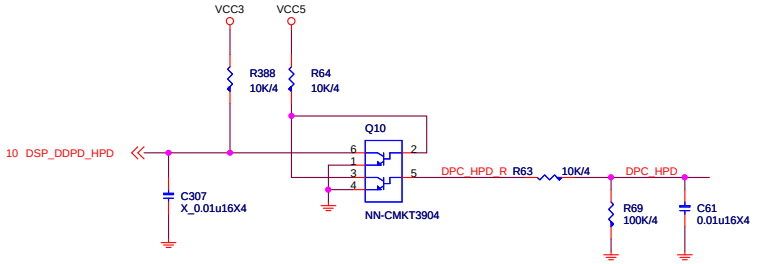
DP







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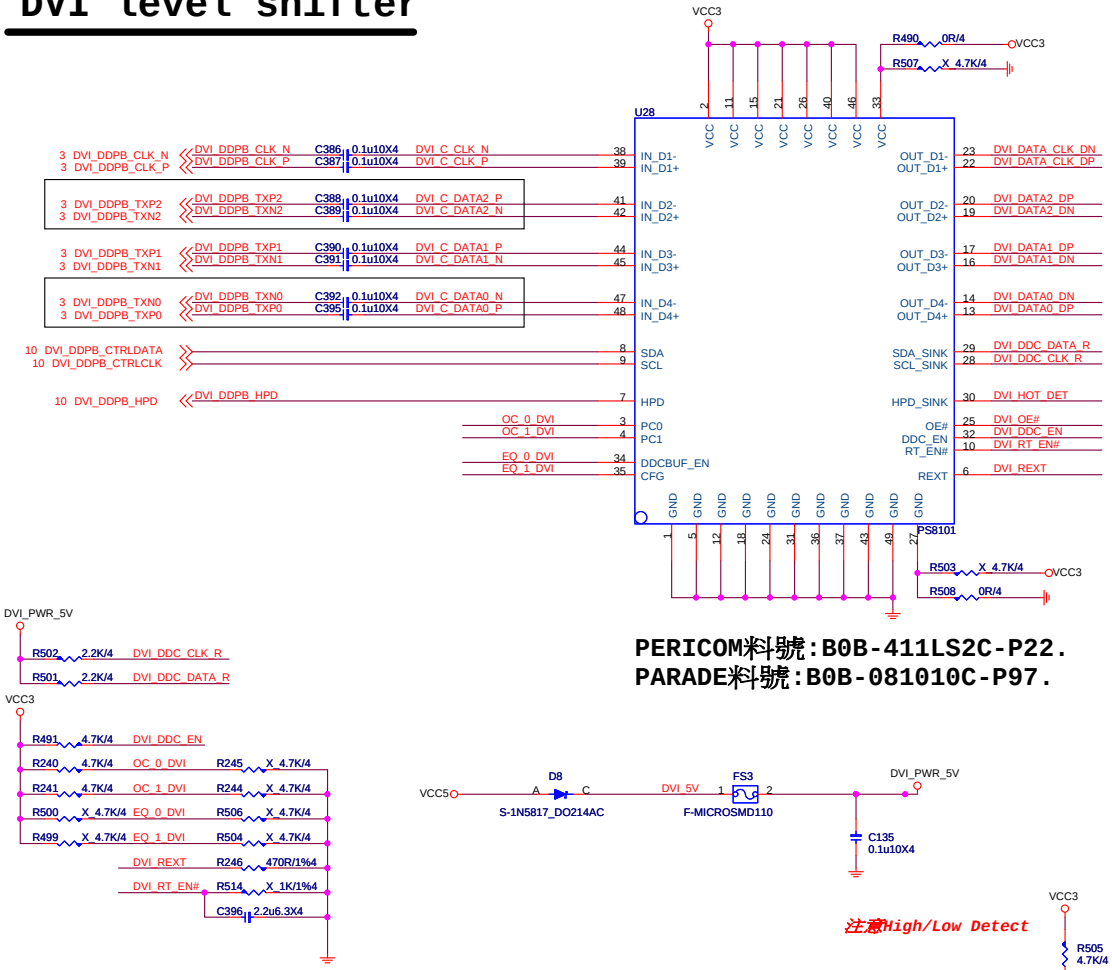
DVI level shifter



PERICOM料號:B0B-411LS2C-P22.
PARADE料號:B0B-081010C-P97.

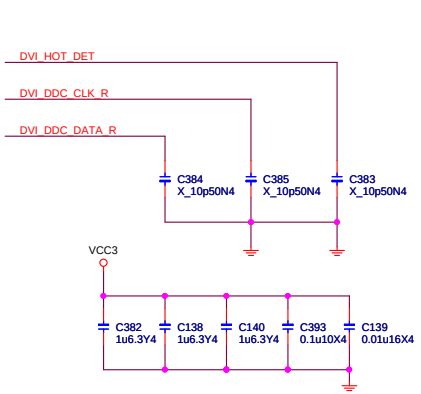
	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

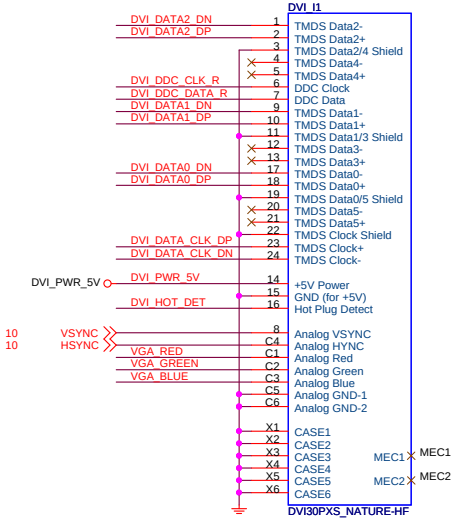
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

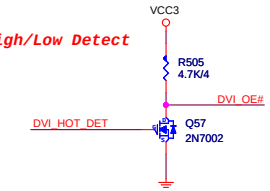
Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	

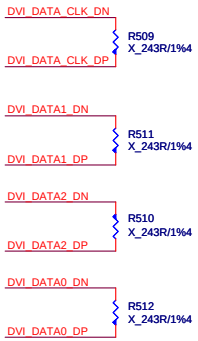




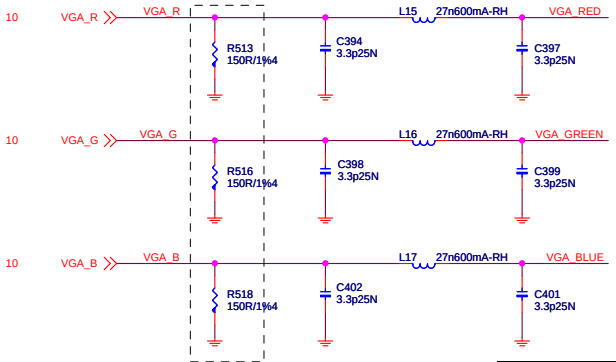
注意High/Low Detect



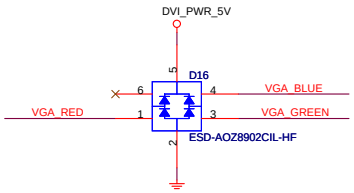
EMI



D-Sub



PLACE CLOSE TO VGA CONNECTOR, WITHIN 750 MIL OF PIN



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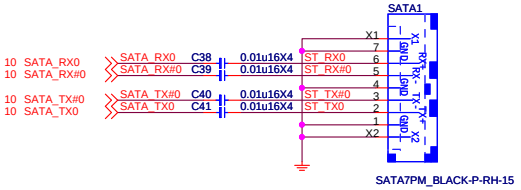
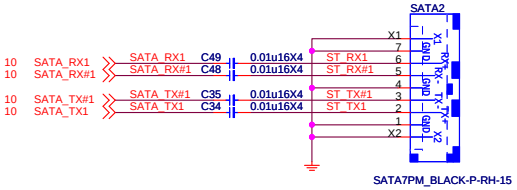
SATA port
Z87,H87:Port 0 ~ 5 are SATA 6G
B85: Port 0, 1, 2, 3 are SATA 6G
H81: Port 0, 1 are SATA 6G
B85,H81: Port 4,5 are SATA 3G

SATA 6G PORT 0,1

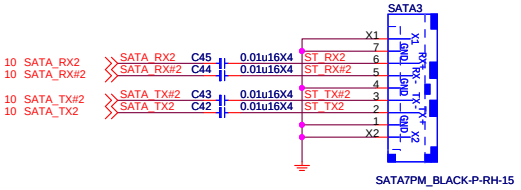
3.0 BLACK

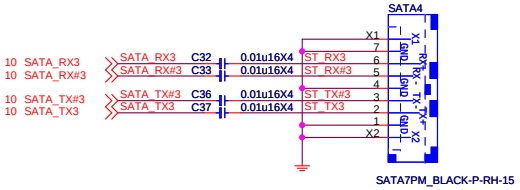




SATA 6G PORT 2,3

3.0 BLACK





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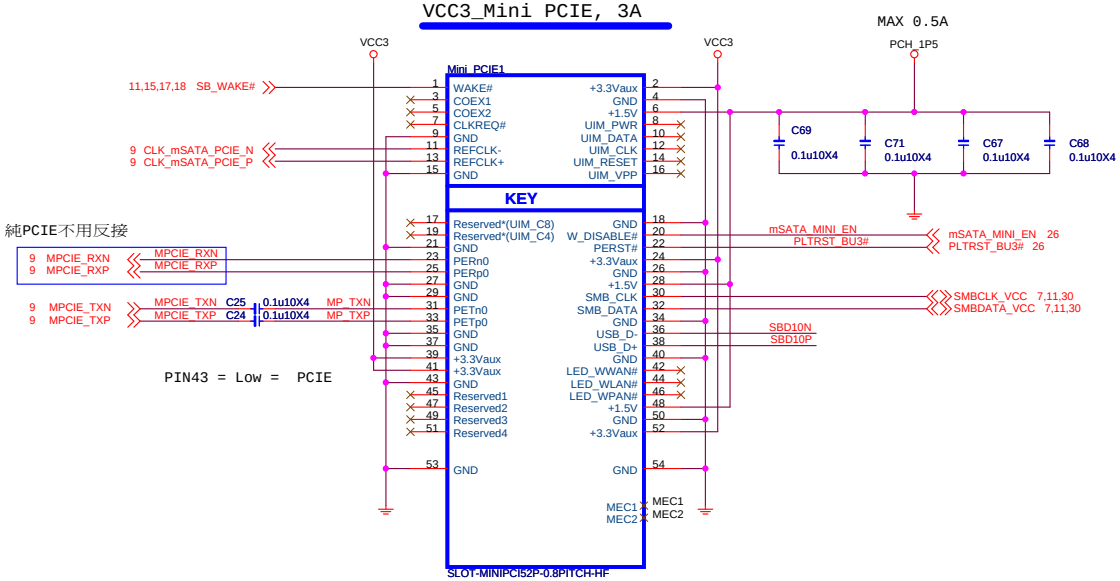
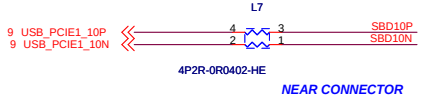
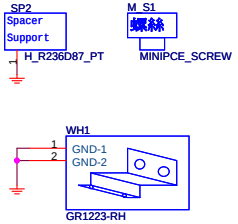
Mini PCIE SHORT CARD







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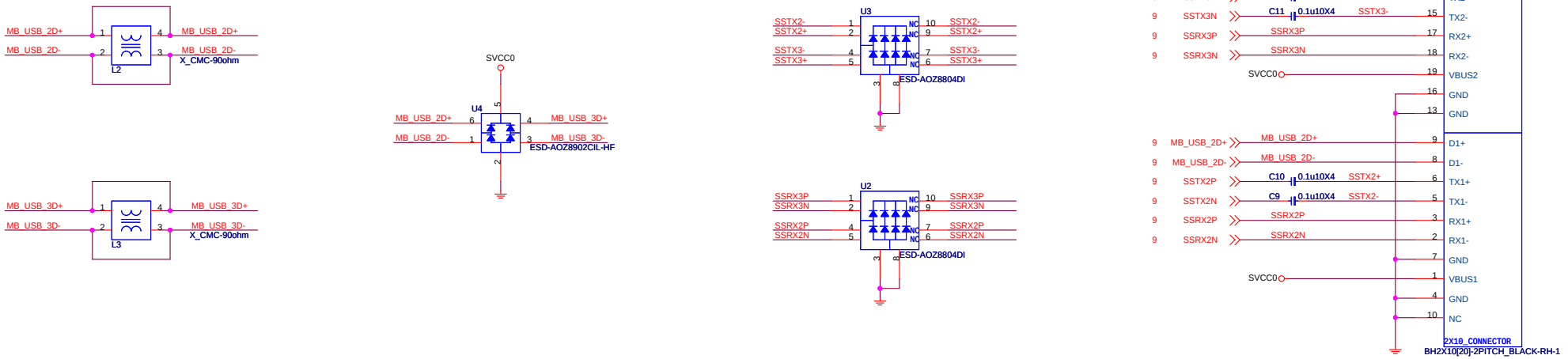
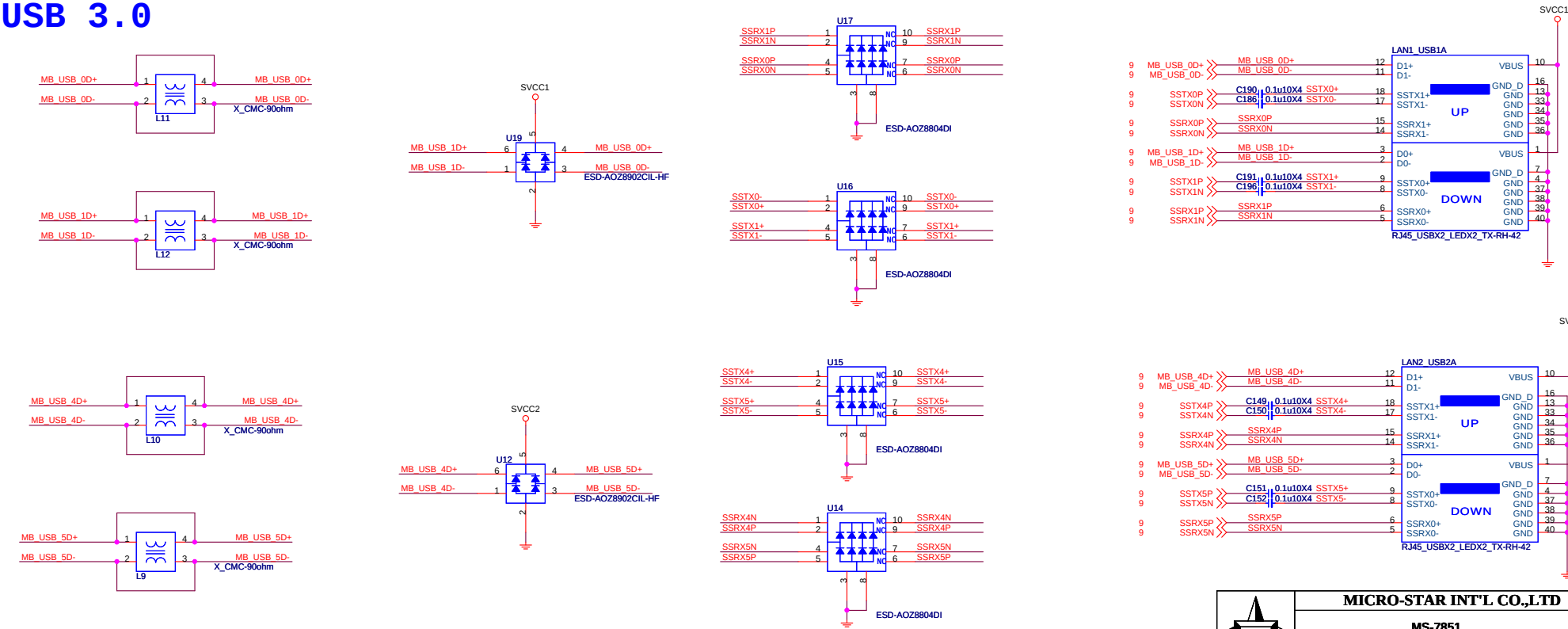
Front USB 3.0



Rear USB 3.0



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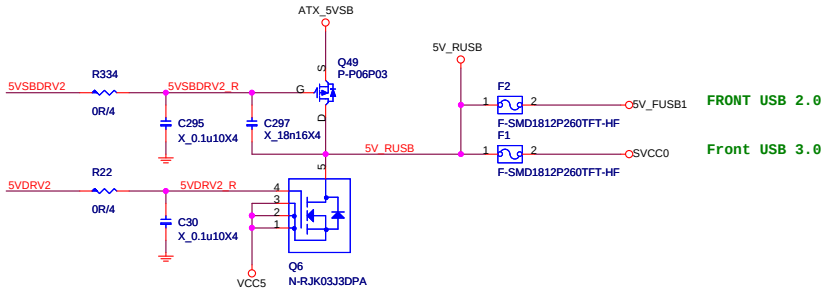
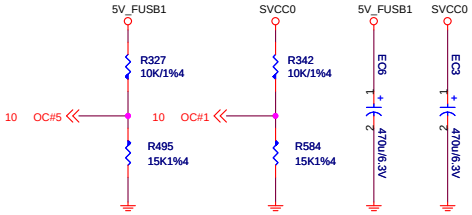
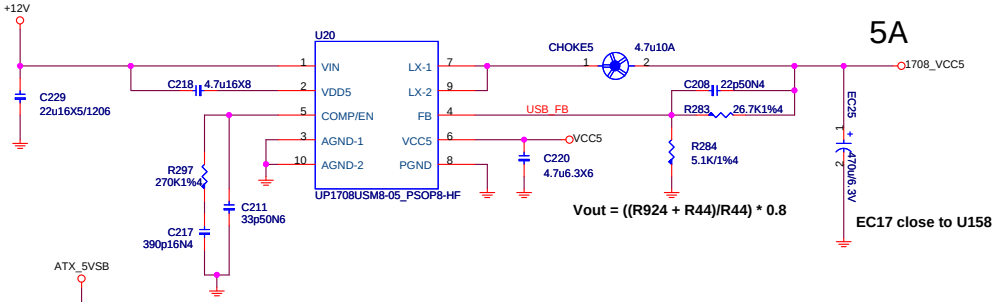
Front USB Power

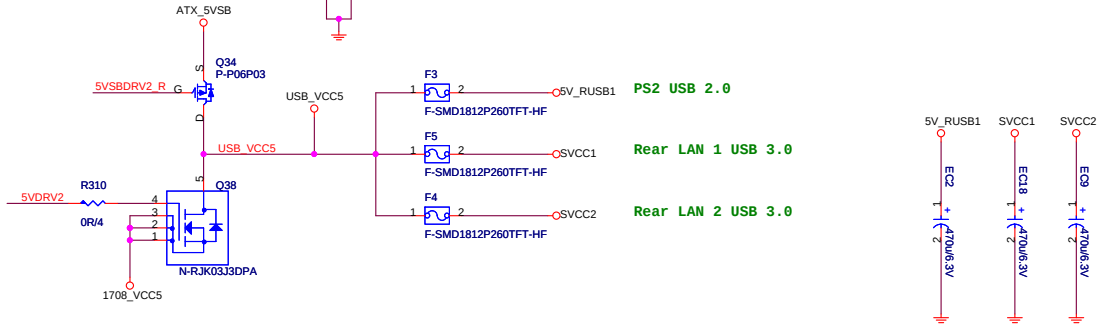


5VDRV2, 5VSBDRV2 width 12mil
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 2 USB ports

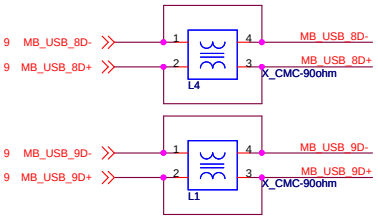


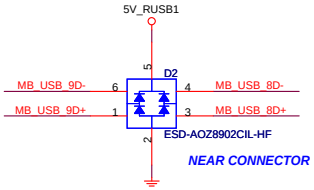
Real USB Power

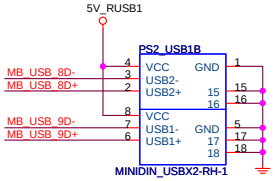




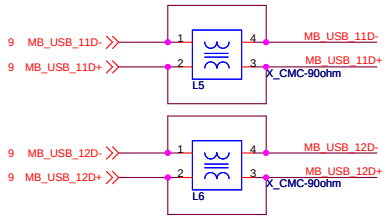
REAR USB PORT 08,09 (With PS2)

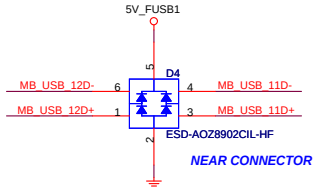


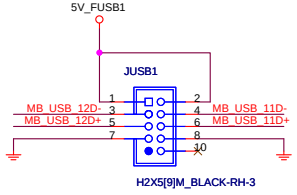




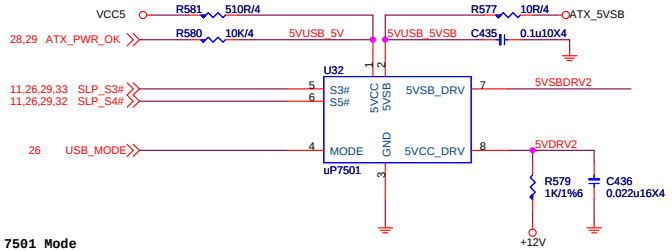
FRONT USB PORT 11,12





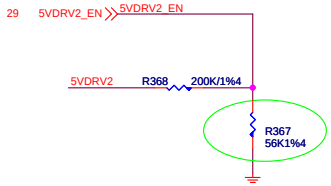


USB Power Select



7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

USB MODE



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都當GPIO
沒用的GPIO PIN 請PULL DOWN
FOR SIO POWER CONSUMPTION

GP73 BIOS要PO成WDT# FUNCTION

U25

LPC Interface
GPIO
Printer mode
Port80
LED Control
DSW Interface
GPIO
GPIO 41, 46, 31 and 32 that
Support Wake-Up Function
AMD used TSIC/D but intel used GPIO
UART SIR
FOR BIOS USED
Harddware Monitor
If un-used input pin please add pull down
KBC Function
FAN Control
ACPI Function
Power Pin
PLTRST_BUS1,2,3
connect to slot or device

NCT6779D-RH

PS2 KEYBOARD & MOUSE CONNECTOR

可以切換在
s5底下是不
是要有電

ESD-AOZ8902CIL-HF

For EMI solution 2008-12-03

SERIAL PORT 1

GD75232DBR_SSOP20-RH

NO USE UART PORT1

X_470p/50X/8P4C

H2X5[10]M_BLACK-RH

Fast boot & Clear CMOS Button

SW-TACTB2#_BLACK-RH-1

3V Analog Power

Closed PIN99

Closed PIN46,85

Closed PIN24,108

SIO Pin Strap

(PIN31)RTSA# 0=2E 1=4E
(PIN32)DTRA# 0=24MHz 1=48MHz
(PIN34)SOUTA 0=Port80 Enable 1=PRT Enable
(PIN69)DSW_EN 0=Disable 1=Enable
(PIN9))(RTSB#)ORT80_EN 0=Disable 1=Enable
(PIN96)AMDPWR_EN 0=Disable 1=Enable
(PIN62)(SLP_S5_LCH#)TEST_MODE_EN 0=Disable 1=Enable

HW Monitor - Voltage

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Size: Custom
Document Description: SIO-NTC6779D/PS2
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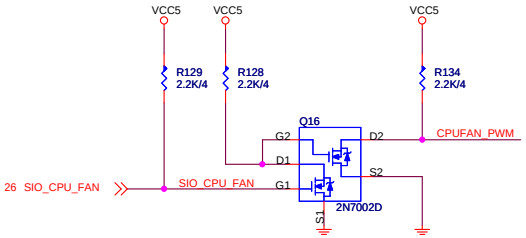
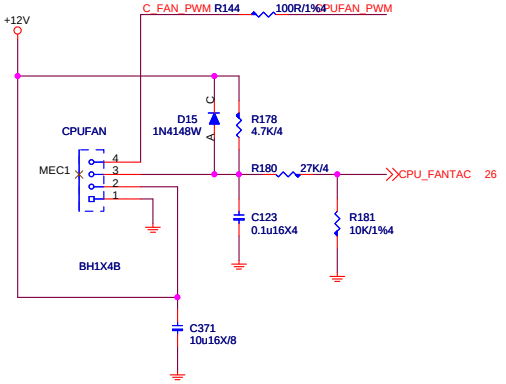
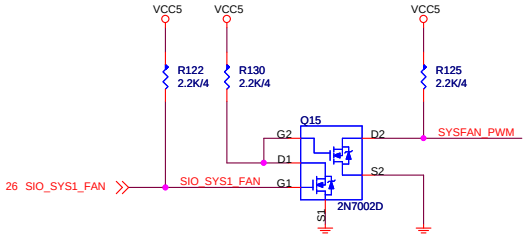
FAN-COUNTROL CIRCUIT

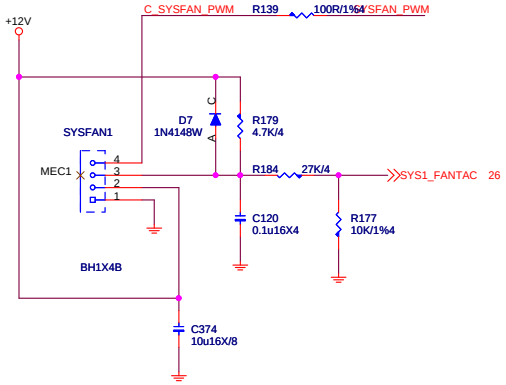
CPUFAN TYPE E





SYSTEM FAN1(PWM MODE)





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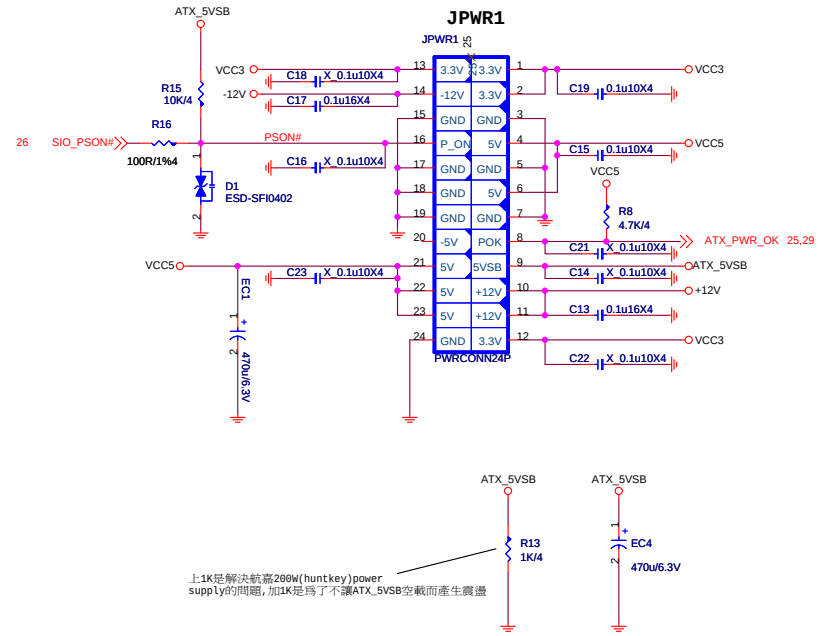
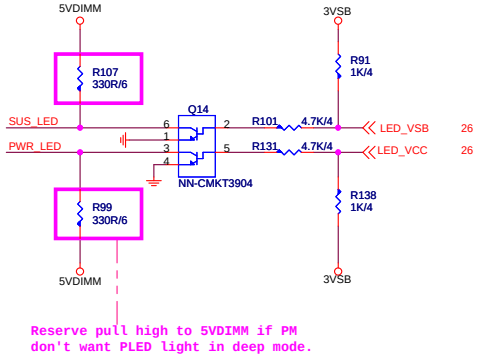
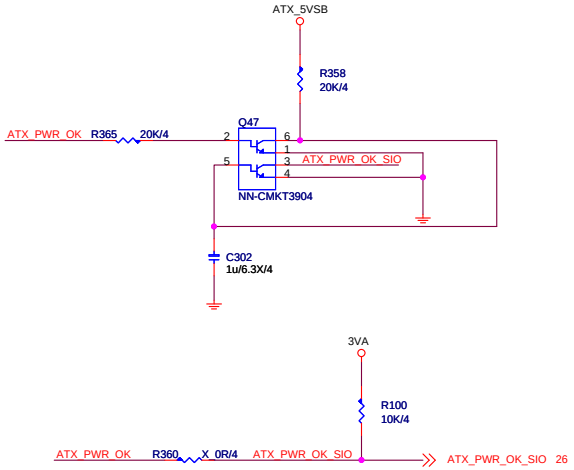
ATX POWER CONNECTOR



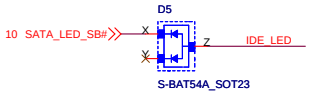
LED (for Fintek NTC6779D)

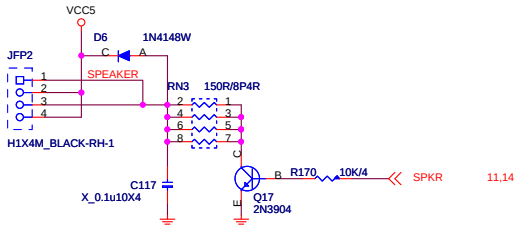


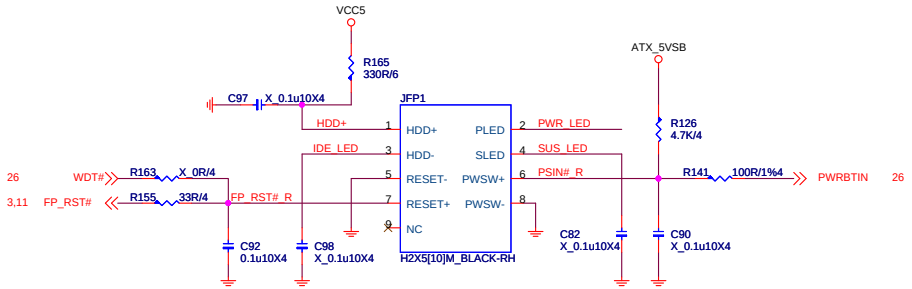
5VCC leakage from ATXPGD



FRONT PANNEL







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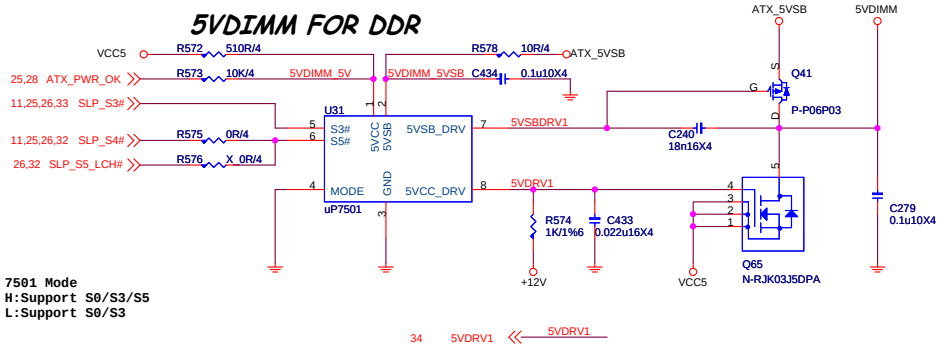
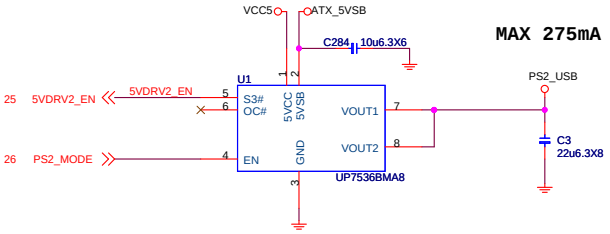
5VDIMM FOR DDR



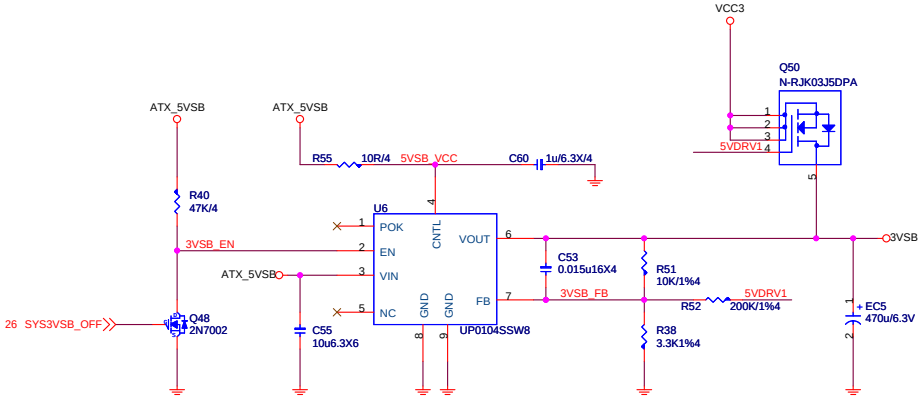
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

PS2 Power



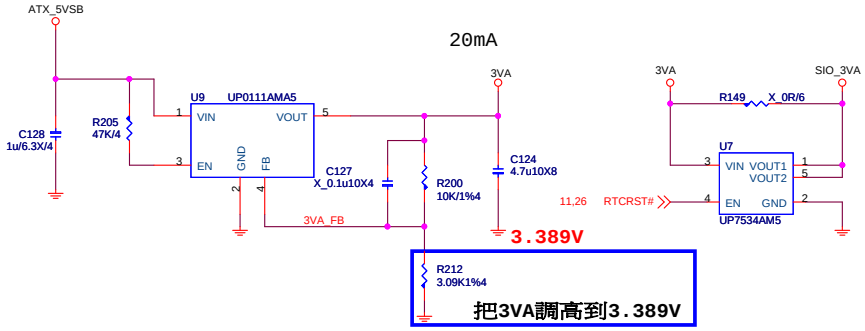
3VSB

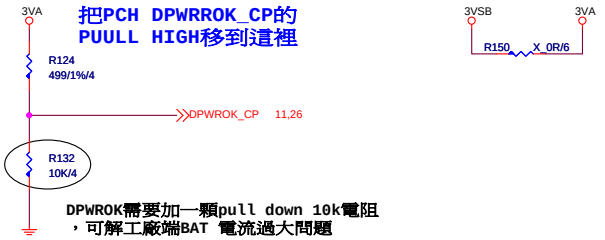
3.041A



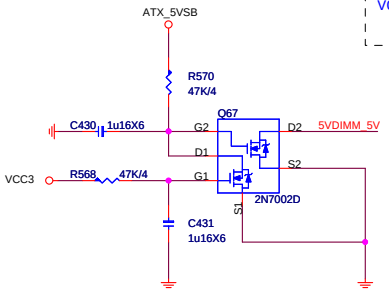
3VA

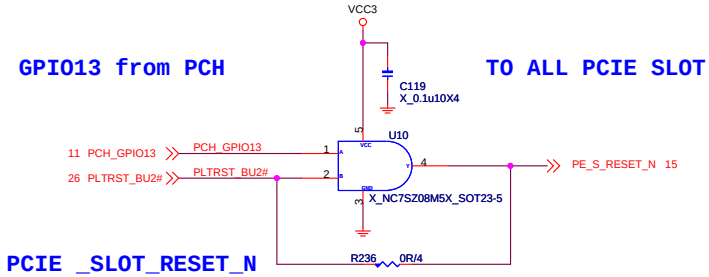
20mA





For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.





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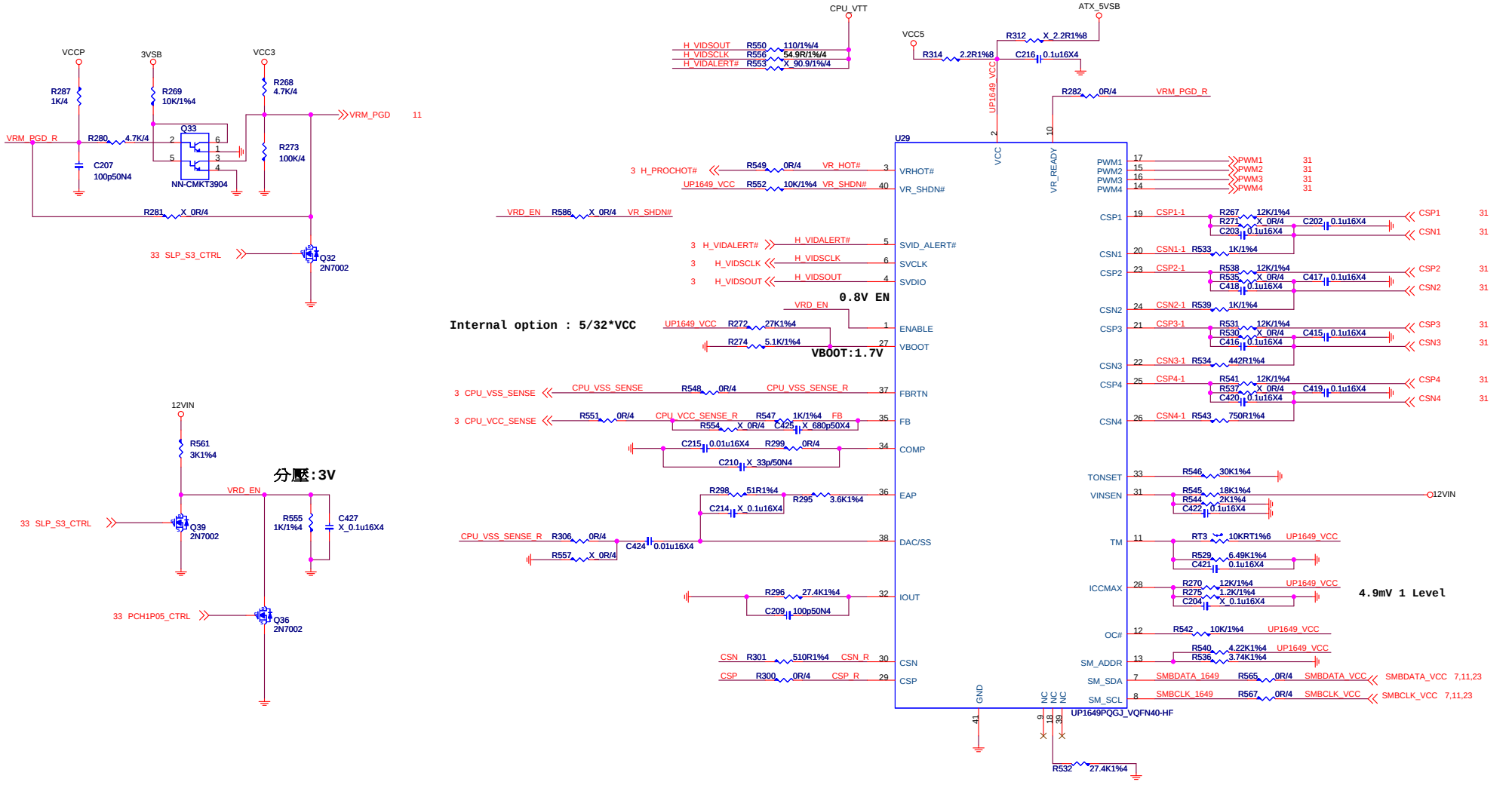
VCCP
3VSB
VCC3
R287 1K/4
R269 10K/1%4
R268 4.7K/4
VRM_PGD 11
VRM_PGD_R
R280 4.7K/4
Q33
NN-CMKT3904
R273 100K/4
C207 100p50N4
R281 X_0R/4
33 SLP_S3_CTRL
Q32 2N7002
CPU_VTT
ATX_5VSB
H_VIDSOUT R550 110/1%/4
H_VIDSCLK R556 54.9R/1%/4
H_VIDALERT# R553 X_90.9/1%/4
VCC5
R312 X_2.2R1%8
R314 2.2R1%8
C216 0.1u16X4
UP1649_VCC
R282 0R/4
VRM_PGD_R
U29
3 H_PROCHOT#
R549 0R/4
VR_HOT#
UP1649_VCC R552 10K/1%4
VR_SHDN#
VRD_EN R586 X_0R/4 VR_SHDN#
3 H_VIDALERT#
3 H_VIDSCLK
3 H_VIDSOUT
VRHOT#
VR_SHDN#
SVID_ALERT#
SVCLK
SVDIO
VCC
VR_READY
0.8V EN
VRD_EN
Internal option : 5/32*VCC
UP1649_VCC R272 27K1%4
R274 5.1K/1%4
VBOOT:1.7V
ENABLE
VBOOT
PWM1
PWM2
PWM3
PWM4
CSP1
CSN1
CSP2
CSN2
CSP3
CSN3
CSP4
CSN4
CSP1-1 R267 12K/1%4 R271 X_0R/4 C203 0.1u16X4 C202 0.1u16X4
CSN1-1 R533 1K/1%4
CSP2-1 R538 12K/1%4 R535 X_0R/4 C418 0.1u16X4 C417 0.1u16X4
CSN2-1 R539 1K/1%4
CSP3-1 R531 12K/1%4 R530 X_0R/4 C416 0.1u16X4 C415 0.1u16X4
CSN3-1 R534 442R1%4
CSP4-1 R541 12K/1%4 R537 X_0R/4 C420 0.1u16X4 C419 0.1u16X4
CSN4-1 R543 750R1%4
3 CPU_VSS_SENSE
CPU_VSS_SENSE R548 0R/4 CPU_VSS_SENSE_R
FBRTN
3 CPU_VCC_SENSE
R551 0R/4 CPU_VCC_SENSE_R R547 1K/1%4 FB
R554 X_0R/4 C425 X_680p50X4
FB
C215 0.01u16X4 R299 0R/4
C210 X_33p/50N4
COMP
R298 51R1%4 R295 3.6K1%4
C214 X_0.1u16X4
EAP
CPU_VSS_SENSE_R R306 0R/4
R557 X_0R/4
C424 0.01u16X4
DAC/SS
R296 27.4K1%4
C209 100p50N4
IOUT
CSN R301 510R1%4 CSN_R
CSP R300 0R/4 CSP_R
CSN
CSP
GND
NC
UP1649PQGJ_VQFN40-HF
R532 27.4K1%4
TONSET
VINSEN
TM
ICCMAX
OC#
SM_ADDR
SM_SDA
SM_SCL
R546 30K1%4
R545 18K1%4
R544 2K1%4
C422 0.1u16X4
12VIN
RT3 10KRT1%6 UP1649_VCC
R529 6.49K1%4
C421 0.1u16X4
R270 12K/1%4 UP1649_VCC
R275 1.2K/1%4
C204 X_0.1u16X4
4.9mV 1 Level
R542 10K/1%4 UP1649_VCC
R540 4.22K1%4 UP1649_VCC
R536 3.74K1%4
SMBDATA_1649 R565 0R/4 SMBDATA_VCC
SMBCLK_1649 R567 0R/4 SMBCLK_VCC
SMBDATA_VCC 7,11,23
SMBCLK_VCC 7,11,23
12VIN
R561 3K1%4
分壓:3V
VRD_EN
33 SLP_S3_CTRL
Q39 2N7002
R555 1K/1%4
C427 X_0.1u16X4
33 PCH1P05_CTRL
Q36 2N7002
UPI VOLTAGE CONSOLE
0x20:RH=10K,RL=OPEN
ADDRESS 0x2A 0X28 0x26 0x24 0x22 0x20
RH (KOhm) OPEN 3.9 3 2.2 1.3 10
RL (KOhm) 10 1.3 2.3 3 3.9 OPEN
BUS_SEL 0% 25% 40% 60% 75% 100%
J1
H1X2M-2PITCH
CHIP_PWGD 5,10,11,26
R313 2.7K1%4 CSP1
R303 2.7K1%4 CSP2
R309 2.7K1%4 CSP3
R307 2.7K1%4 CSP4
CSP
R308 1.3K1%4
C223 1u/6.3X/4
C219 X_0.1u16X4
R315 16K1%4
RT2 10KRT1%6
CSN
C226 0.1u16X4
R279 1R1%4 CSN1
R285 1R1%4 CSN2
R286 1R1%4 CSN3
R294 1R1%4 CSN4
CPU_VSS_SENSE_R
R302 100R/1%4
C423 X_0.1u16X4
C221 X_0.1u16X4
CPU_VCC_SENSE_R
VCCP
R558 100R/1%4
C426 X_0.1u16X4
VCC5
R239 10K/1%4
C137 0.1u16X4
R243 X_9.1K1%4
7,11,23 SMBCLK_VCC
7,11,23 SMBDATA_VCC
SMBCLK_VCC
SMBDATA_VCC
U11
VCC
BUS_SEL
SCL
SDA
GND
OUT1
OUT2
OUT3
UP1811BMA8
R238 0R/4
R242 0R/4
PCH_1P05_REF 33 -200uA
PCH_1P5_FB 33 -10uA
MICRO-STAR INT'L CO.,LTD
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Size Custom
Document Description VRM12 .5 - UP1649
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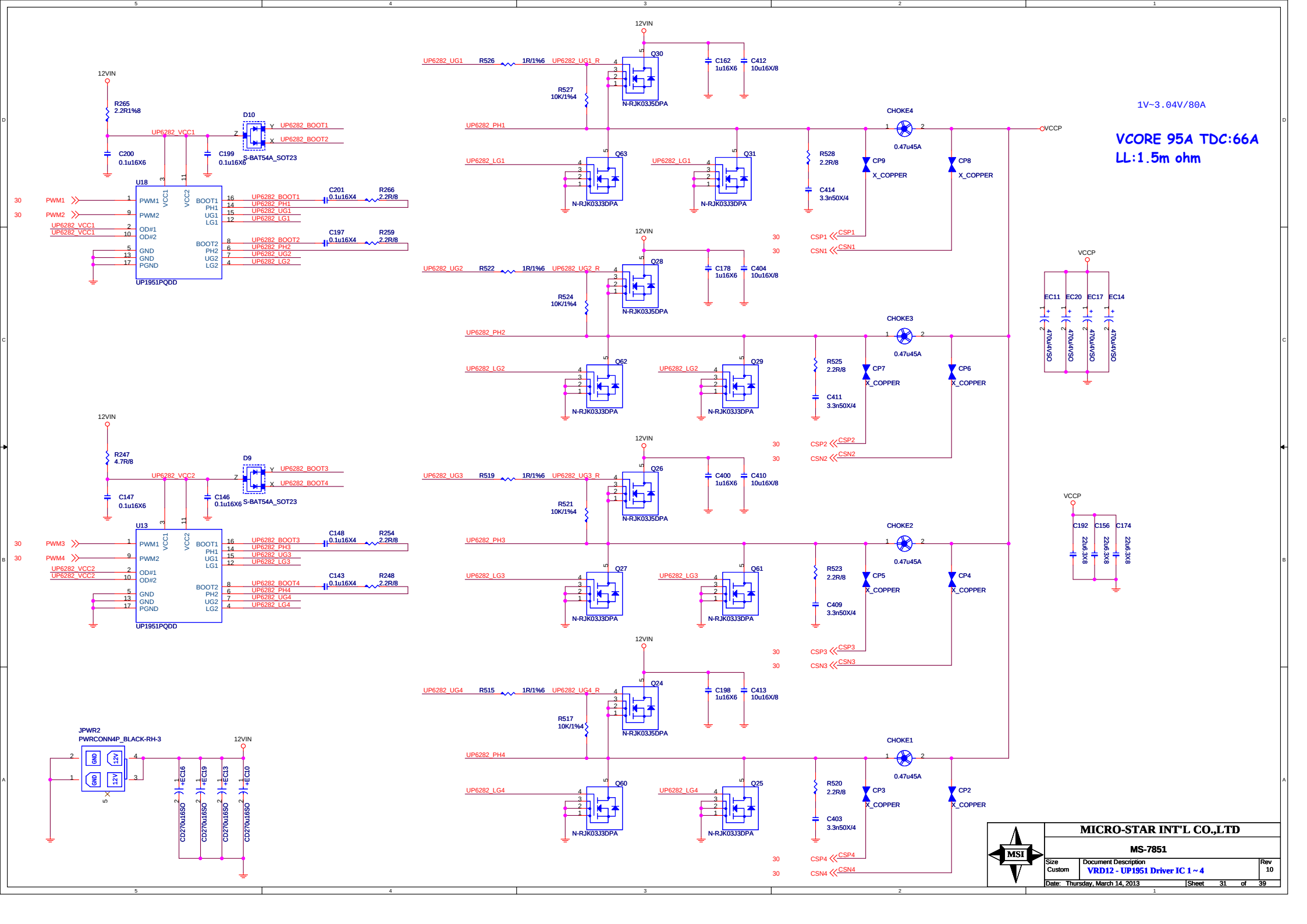
1V~3.04V/80A
VCORE 95A TDC:66A
LL:1.5m ohm
12VIN
R265 2.2R1%8
C200 0.1u16X6
C199 0.1u16X6
D10
S-BAT54A_SOT23
U18
UP1951PQDD
C201 0.1u16X4
R266 2.2R/8
C197 0.1u16X4
R259 2.2R/8
R247 4.7R/8
C147 0.1u16X6
C146 0.1u16X6
D9
U13
C148 0.1u16X4
R254 2.2R/8
C143 0.1u16X4
R248 2.2R/8
JPWR2
PWRCONN4P_BLACK-RH-3
CD270u16SO
R526 1R/1%6
R527 10K/1%4
Q30
C162 1u16X6
C412 10u16X/8
Q63
Q31
R528 2.2R/8
C414 3.3n50X/4
CHOKE4
0.47u45A
CP9 X_COPPER
CP8 X_COPPER
VCCP
R522 1R/1%6
R524 10K/1%4
Q28
C178 1u16X6
C404 10u16X/8
Q62
Q29
R525 2.2R/8
C411 3.3n50X/4
CHOKE3
CP7 X_COPPER
CP6 X_COPPER
EC11 EC20 EC17 EC14
470u4VSO
R519 1R/1%6
R521 10K/1%4
Q26
C400 1u16X6
C410 10u16X/8
Q27
Q61
R523 2.2R/8
C409 3.3n50X/4
CHOKE2
CP5 X_COPPER
CP4 X_COPPER
C192 C156 C174
22u6.3X8
R515 1R/1%6
R517 10K/1%4
Q24
C198 1u16X6
C413 10u16X/8
Q60
Q25
R520 2.2R/8
C403 3.3n50X/4
CHOKE1
CP3 X_COPPER
CP2 X_COPPER
N-RJK03J5DPA
N-RJK03J3DPA
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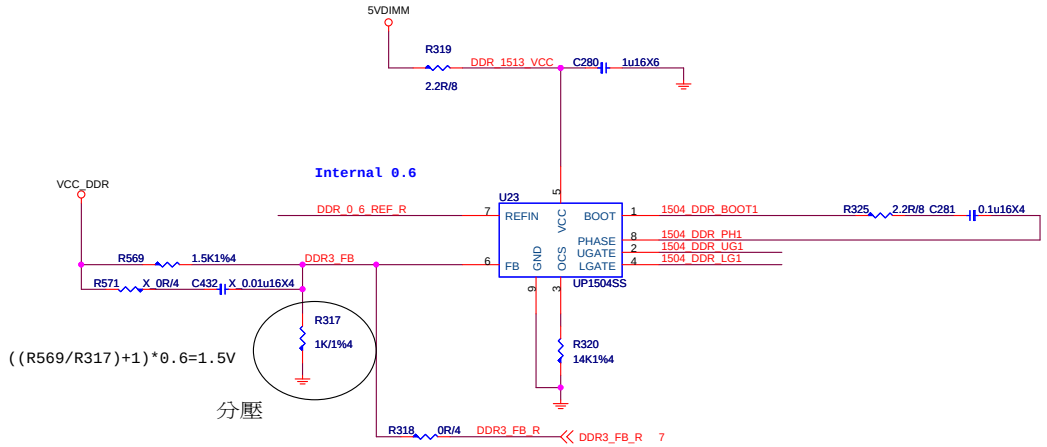
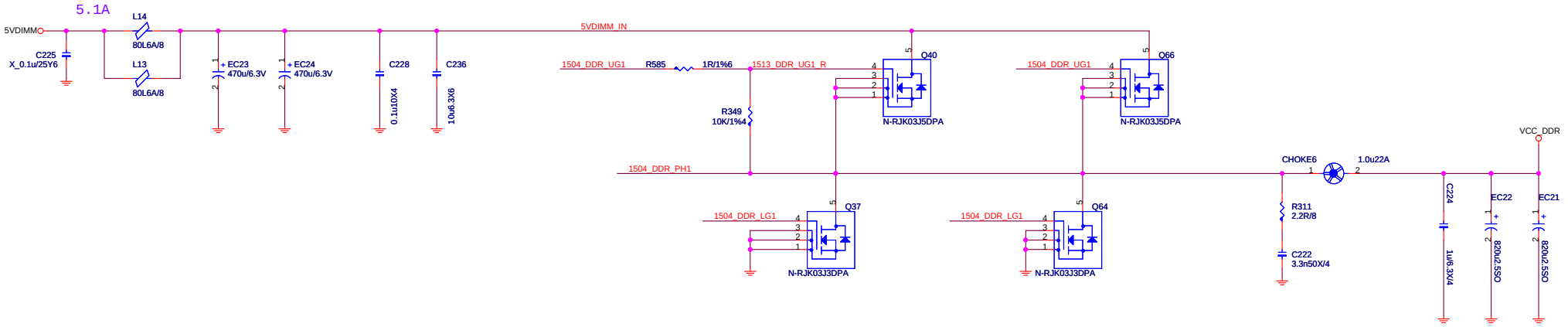
DDR Power:1.5V

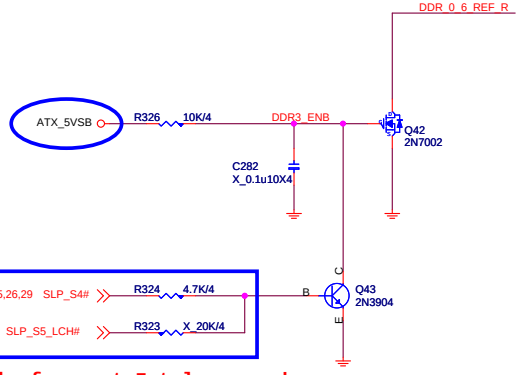
DDR3_1.5V 4.2A+6A+0.557A+6A=16.757A

4.2A FOR CPU
6A FOR 2DIMM
0.557A FOR VTT_DDR
PCH Core 6A

*OCP 16.757*1.5=25.1355A*
*OCP=[20uA*Rocs(R320)]/4*Rdson(Low side for NXP)2.75mohm*
R320=14K ohm



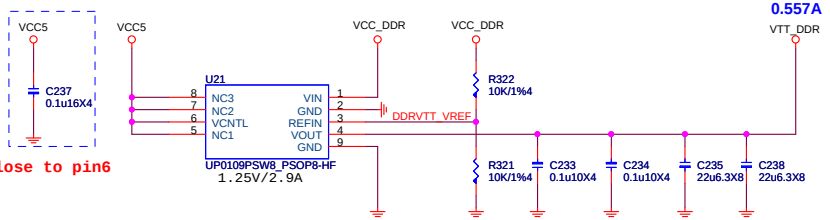




P.S. Only for meet Intel power down sequence.

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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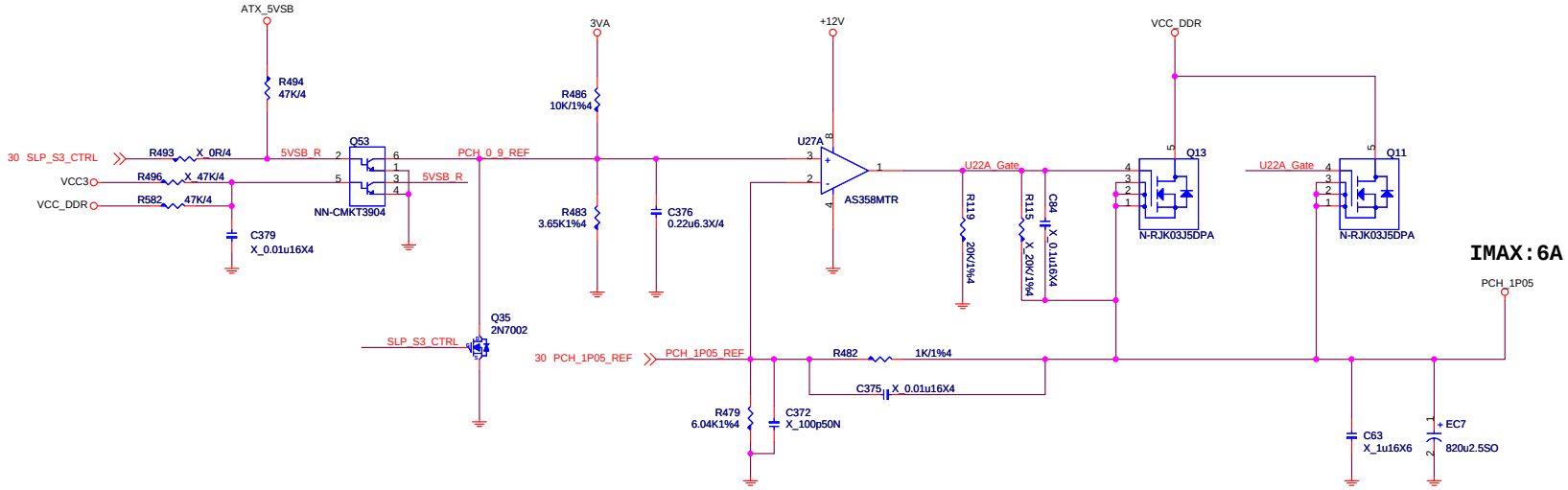
PCH Power:1.05V

PCH Core 6A

Iripple=1.80A
5*1=5A>1.80A

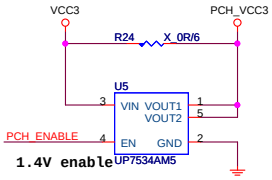
Imax: 6A

Iout ripple = 5A

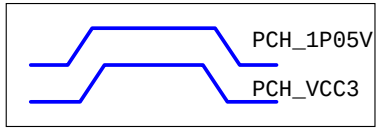


PCH Power:3.3V

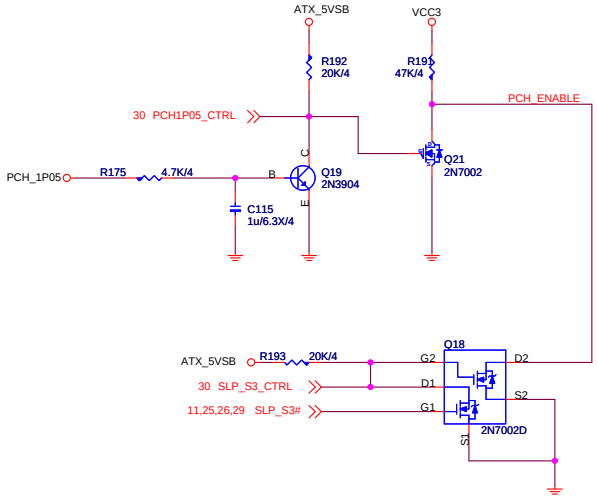
0.133A



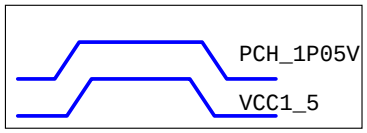
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



Waitting PCH_1P05 Ready



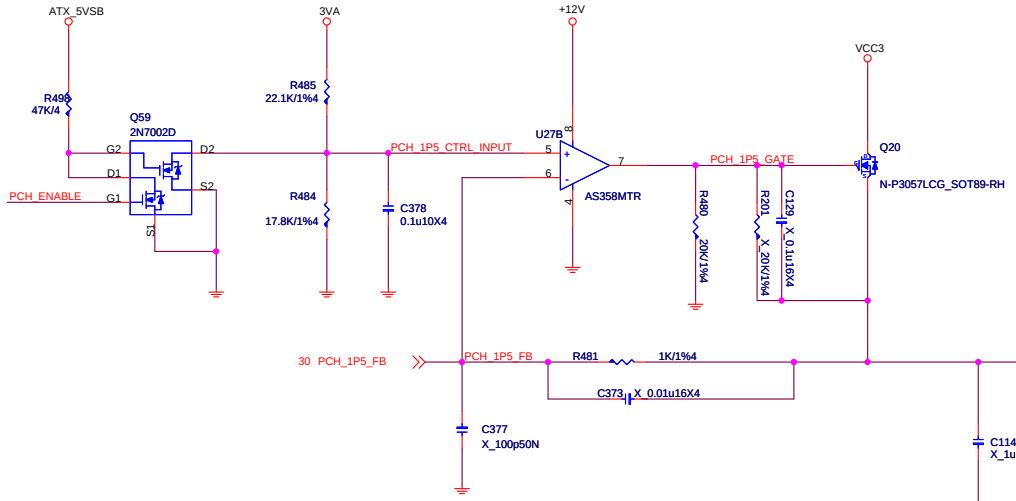
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



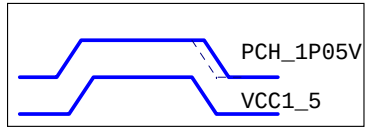
PCH Power:1.5V

PCH: 0.35A

PCH_1P5
Imax: 0.35A



VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



0.35A

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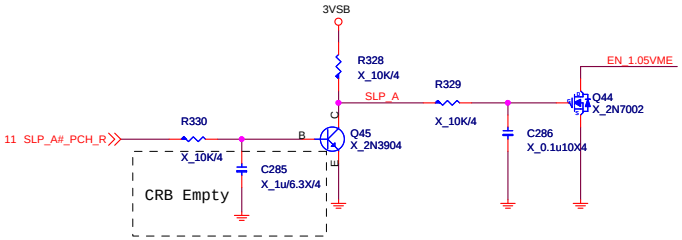
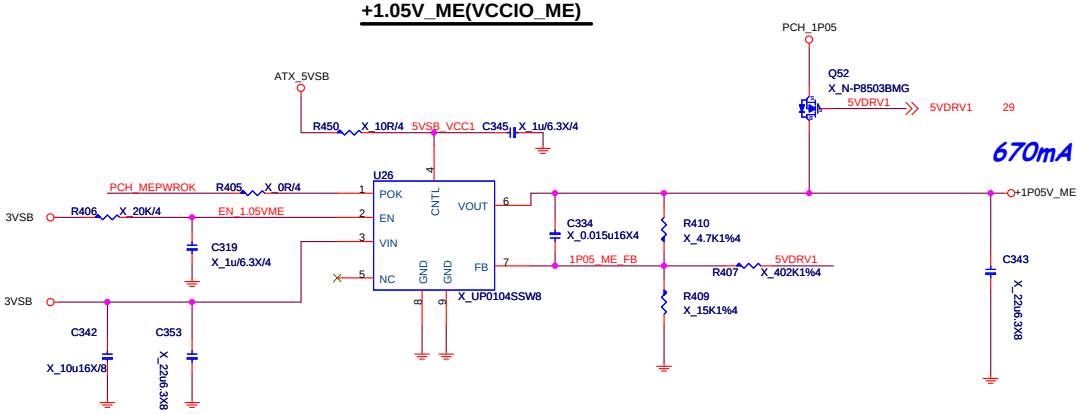
C318,C323,R378,C313,C314,C333,R366 for H87 un stuff
Z87 only stuff R354

SLP_A

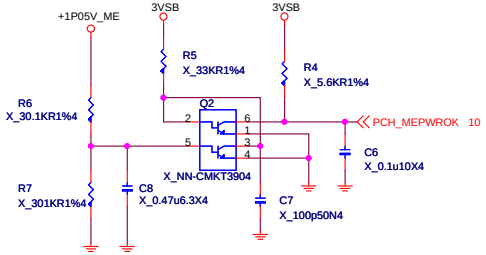
ME Power Control

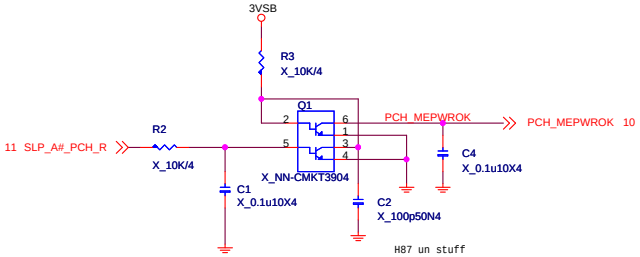


+1.05V_ME(VCCIO_ME)

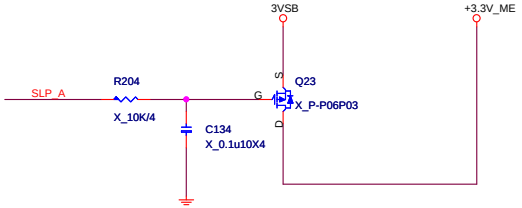


PCH_MEPWROK



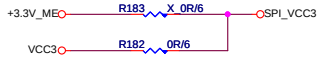


+3.3V_ME



For INTEL ME BUG

Z87->Stuff R654
H87、B85->Stuff R653



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PCB1

7851_10

PD0-078510A-E48,競華,23,寶安恩斯邁廠(MSIS)

WIFI

WIFI
CADR

WIFI_CARD

LABEL2

MKT

BUY

HDMI_LA1

Label
HDMI

HDMI LABEL

CPU_H1

CPU
鐵座

CPU_H1

LA3

AMI_BIOS
LABLE

BIOS_LABLE

BAT1_X1

BAT-BCR2032P-RH

HEATSINK

HS_PCH1

MEC2

MEC2

MEC1

MEC1

HS-0406530-RH

HS_MOS

MEC2

MEC1

HS-0502440-RH

SPI OPT.

SPI10

SPI
8M

X_W25Q128FVSIQ-HF

D1000

MOS

X_N-AO3414

H87 OPT.

U100

LPT
H87

X_Lynx PointH87

LA20

MKT
H87

X_Lynx PointH87

B85 OPT.

U1000

LPT
B85

X_Lynx PointB85

LA200

MKT
B85

X_Lynx PointH85

AUDIO1

AUDIO
B85

X_Lynx PointH85

C5000

270u/16V
B85

X_Lynx PointH85

C1000

470u/6.3V
B85

X_Lynx PointH85

C2000

820u/2.5V
B85

X_Lynx PointH85

C3000

560u/6.3V
B85

X_Lynx PointH85

C4000

100u/16V
B85

X_Lynx PointH85

Mounting Holes

MH2

X_MH001

MH3

X_MH001

MH1

X_MH001

MH4

X_MH001

Simulation

SIM2

SIM2

X_PIN1*2

SIM1

SIM1

X_PIN1*2

SIM4

SIM4

X_PIN1*2

SIM3

SIM3

X_PIN1*2

Optical Fiducial Marks-120

FM4

X_FM

FM2

X_FM

FM1

X_FM

FM3

X_FM

FM7

X_FM

FM6

X_FM

FM5

X_FM

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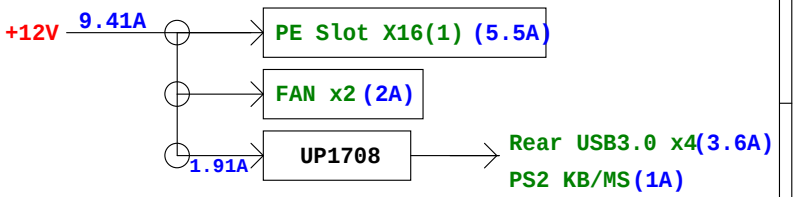
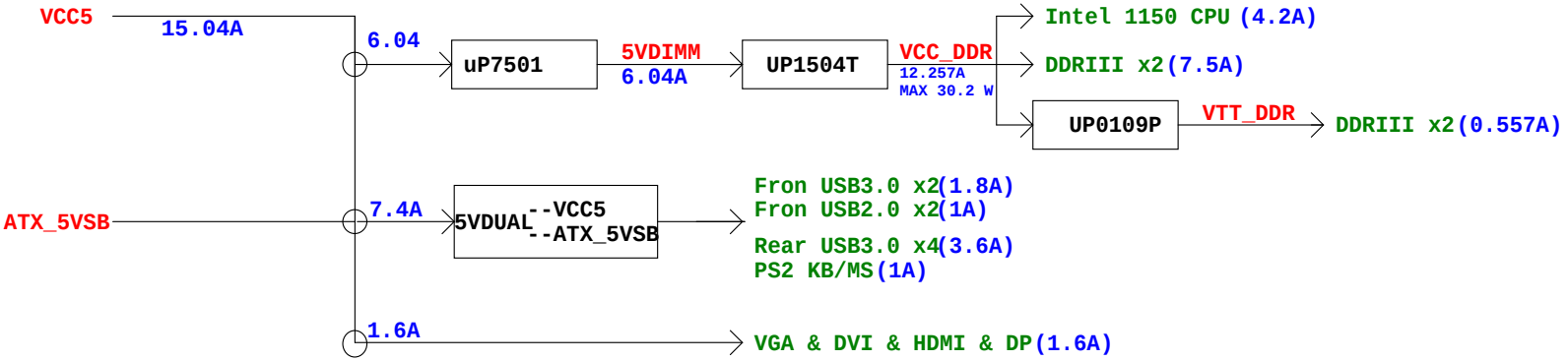
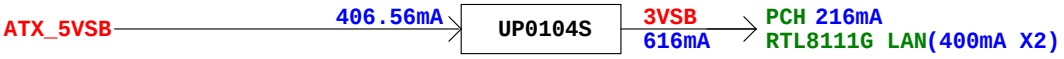
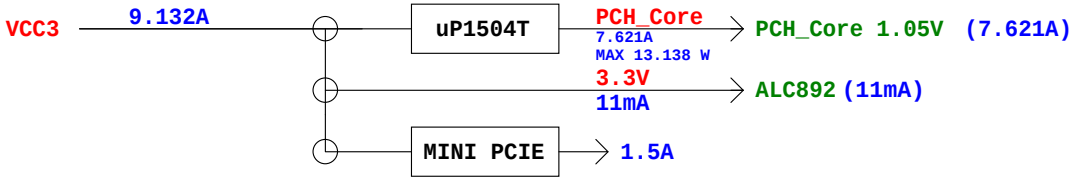
Power Delivery

Slot









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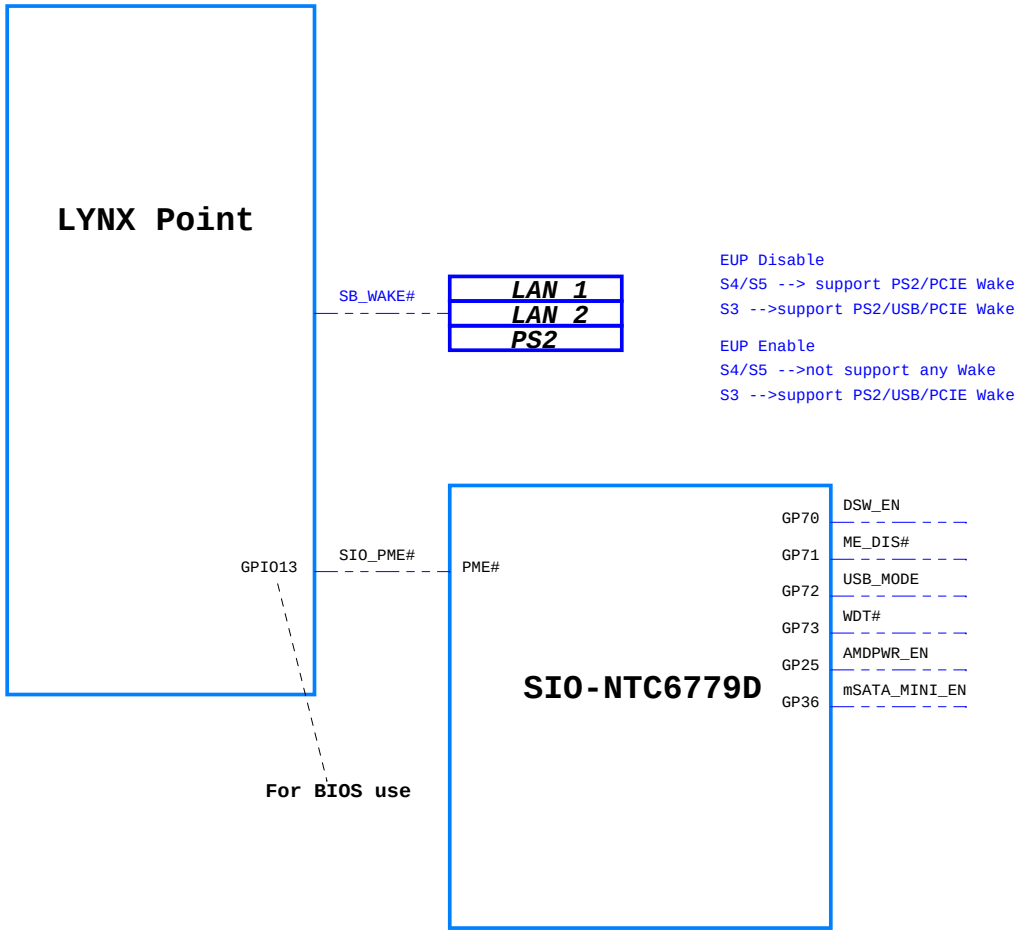

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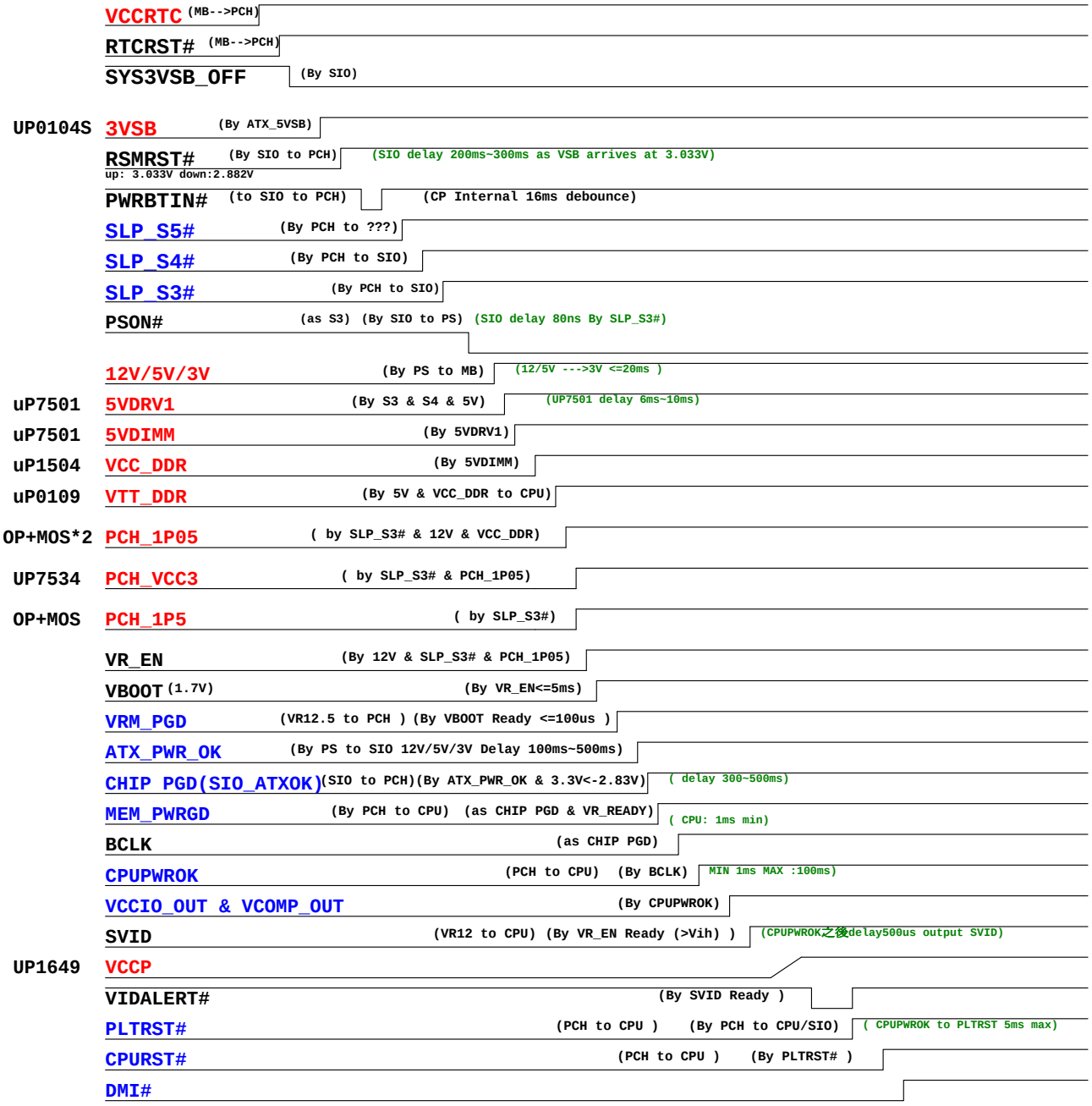
(G3)DS5 ---> S0



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MS-7851-0A to 1.0 Modify history

1. Remove TPM connect .
2. Add COM port .
3. Remove C85,C88,R113,R133,R123,Q12,Q53 .
4. LAN1_USB 3.0 TX0 TX1 change .
5. Change Q20 to "D03-3057L19-N03" for PCH power 1.5V .
6. Add R224 for PCH_PWRGD .
7. Q12 change to 2N7002 for CHIP_PWRGD .
8. Remove C171,168,165,177,181,184,188,EC8 for power solution .
9. Add R113,123 to DDR function.
10. Change D18 for SMBUS EMI solution .
11. Add R223 for GPIO37 .
12. HDMI levlshift change to NXP3360 .
13. Q53 change to 3904 .
14. Add OC#1 & OC#5 to from USB.
15. Remove +1P05_ME one 22u output cap .
16. Add 4.7u CL43~46 for surge improvement .

Model	Sample BOM	chipset	Market Name
MS-7851 0A OPT:A	601-7851-A10	H87 chipset	H87-G51
MS-7851 0A OPT:B	601-7851-A20	Z87 chipset	Z87-G51

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