Intel Sky Lake Platform

SLK-S CPU / SLK PCH-H

Marking	Description
I	Installed
NI	Not Installed
MP	Production Part ONLY
PROTO	Not For Production Part
CCL	Critical Components List

PCA P/N, Scorpion/Spitfire/Toledo	
SCH P/N, Scorpion/Spitfire/Toledo	
PCB P/N, Scorpion/Spitfire/Toledo	

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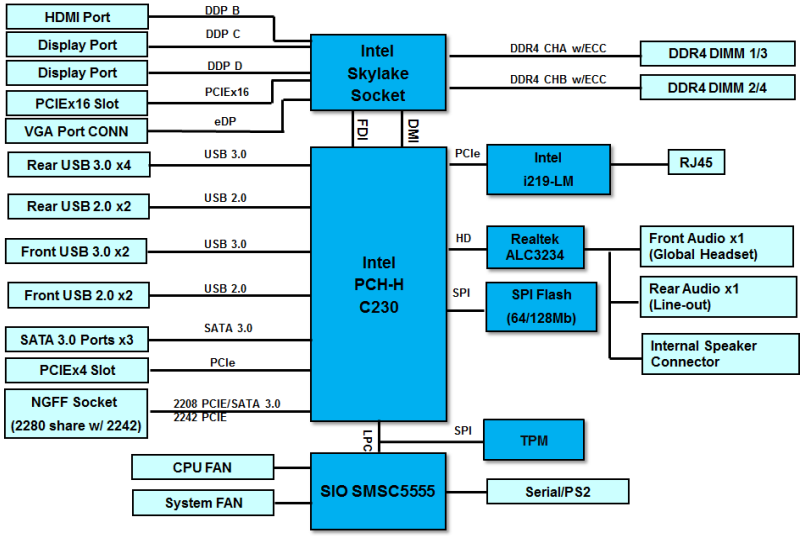
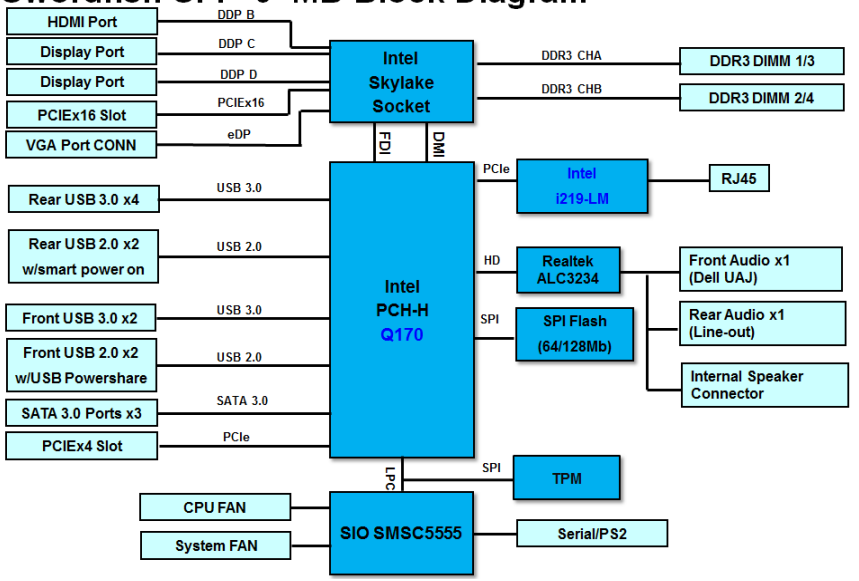
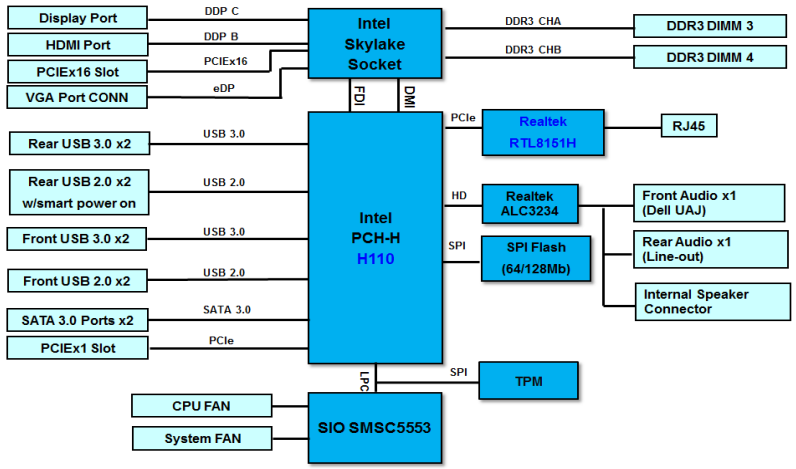
Farallon SFF MB Block Diagram



Swordfish SFF 9 MB Block Diagram



Swordfish SFF 3 MB Block Diagram



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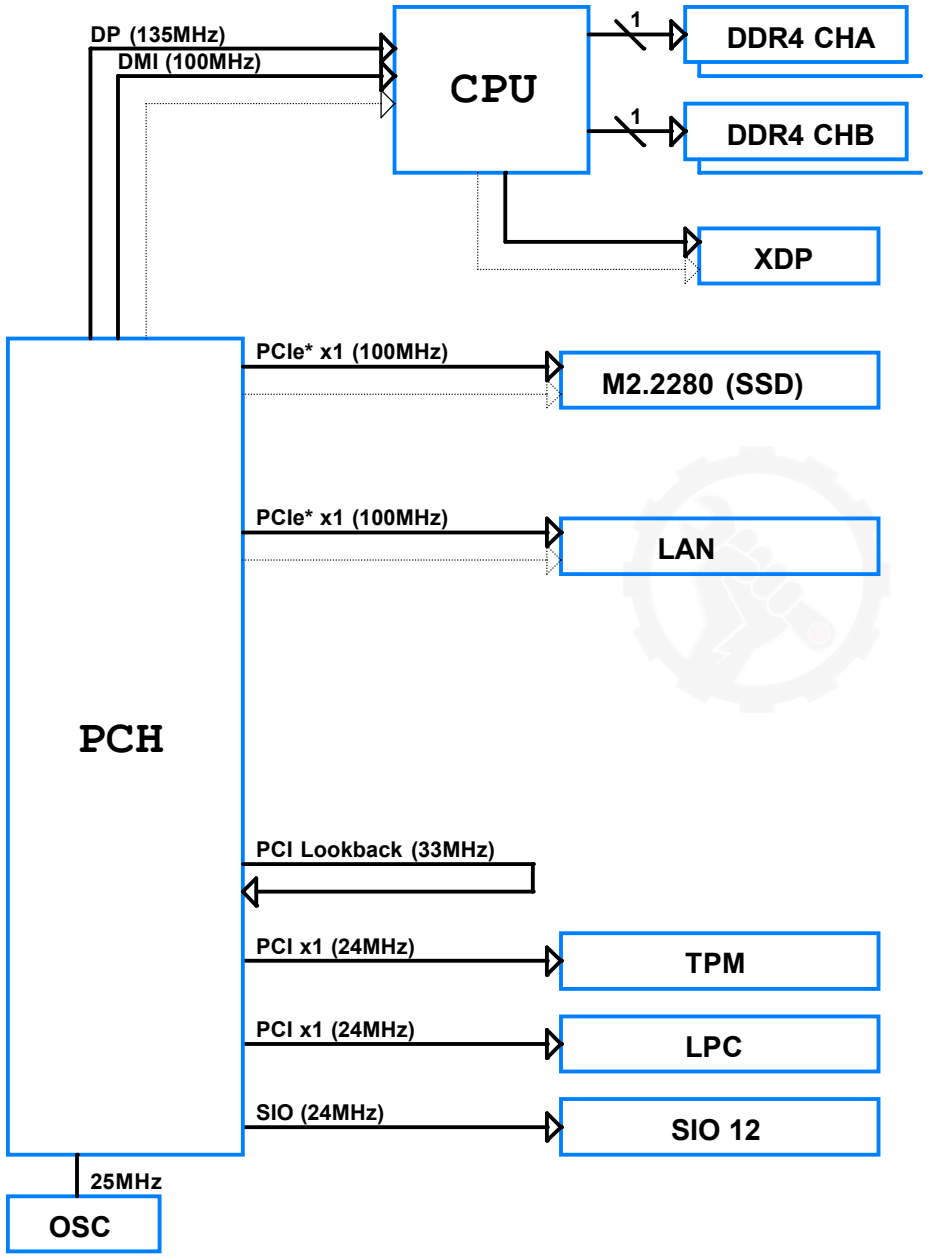
Clock Diagram



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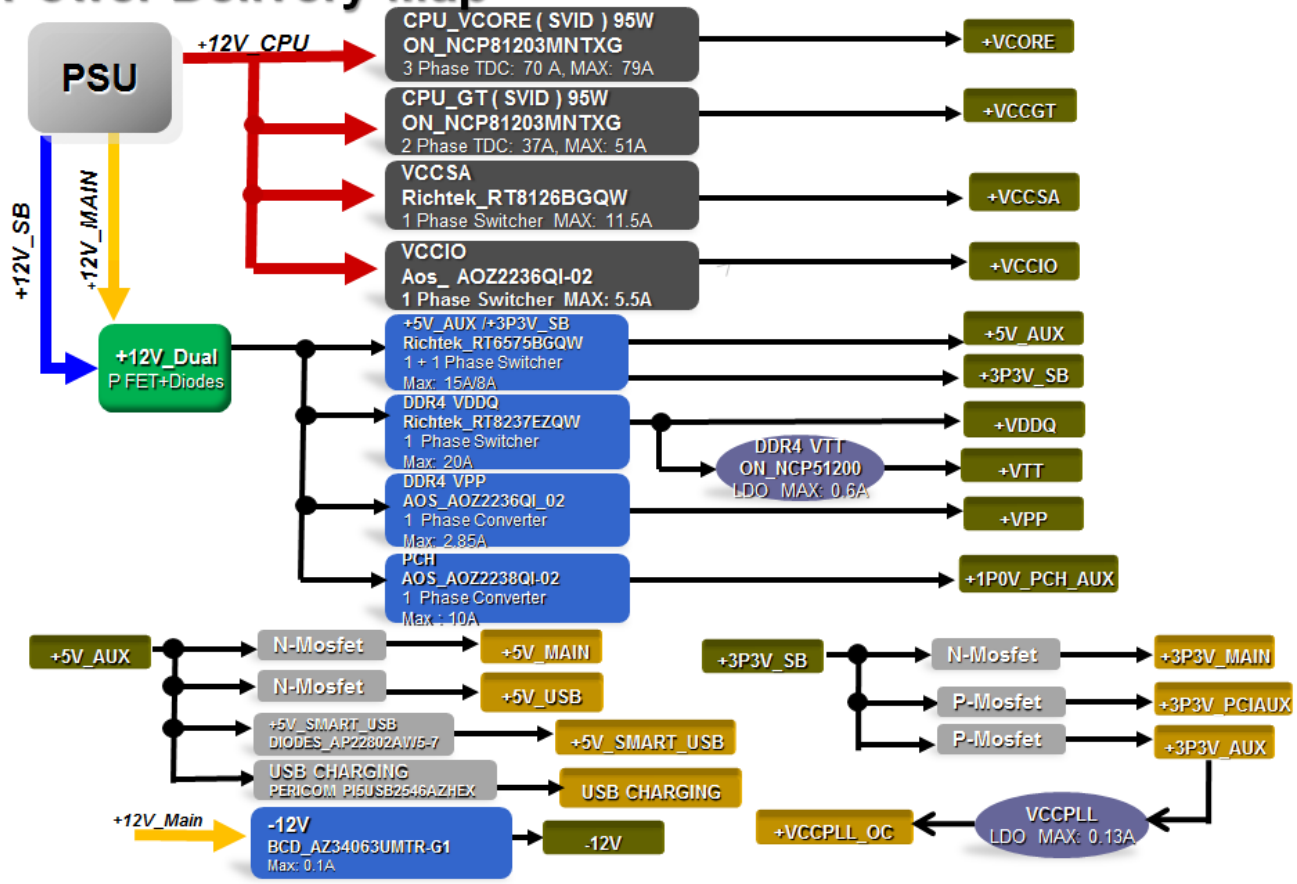
Power Delivery Map



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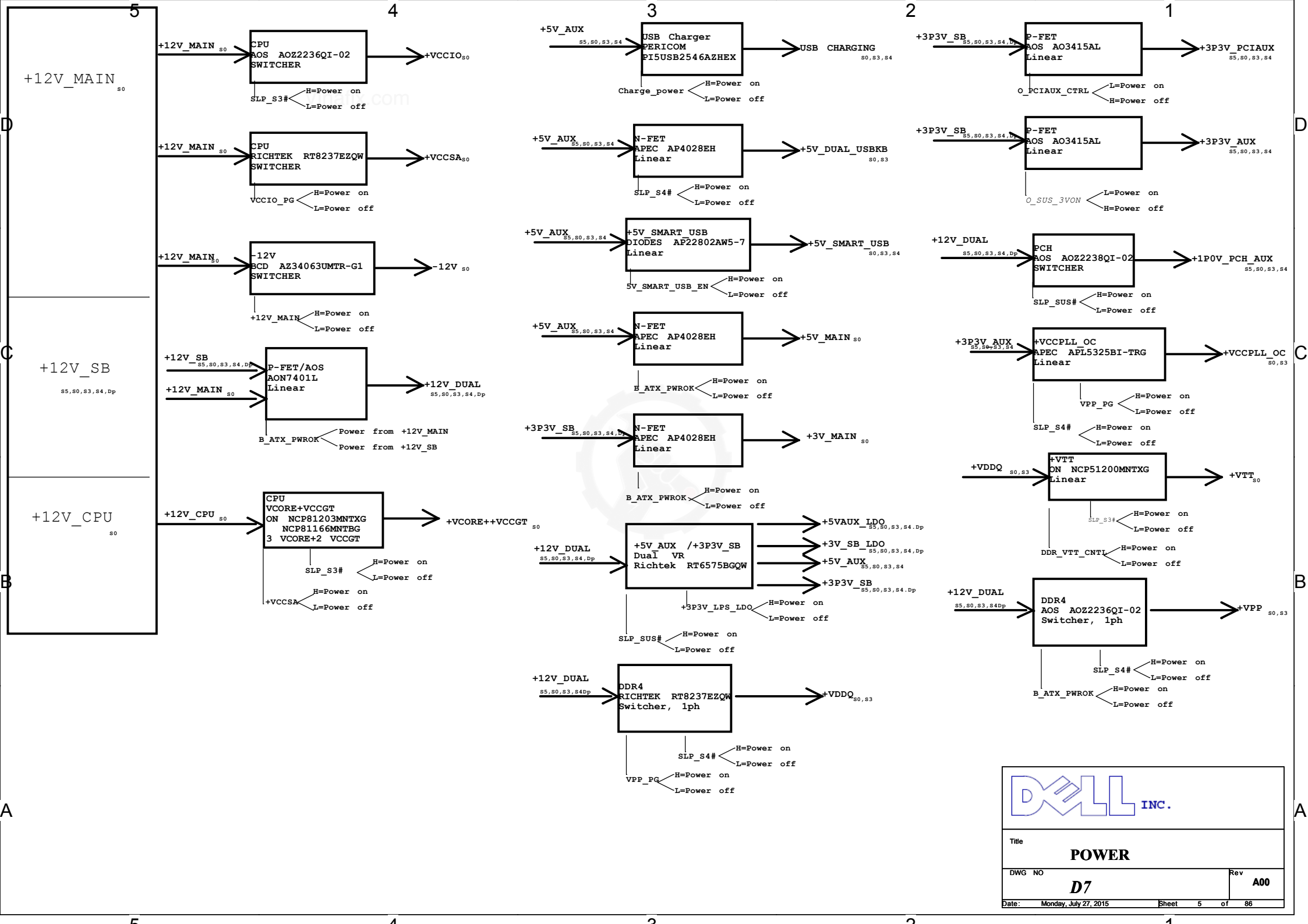
+12V_MAIN S0
+12V_SB S5,S0,S3,S4,Dp
+12V_CPU S0
+12V_MAIN S0 → CPU AOS AOZ2236QI-02 SWITCHER → +VCCIO S0
SLP_S3# H=Power on L=Power off
+12V_MAIN S0 → CPU RICHTEK RT8237EZQW SWITCHER → +VCCSA S0
VCCIO_PG H=Power on L=Power off
+12V_MAIN S0 → -12V BCD AZ34063UMTR-G1 SWITCHER → -12V S0
+12V_MAIN H=Power on L=Power off
+12V_SB S5,S0,S3,S4,Dp
+12V_MAIN S0 → P-FET/AOS AON7401L Linear → +12V_DUAL S5,S0,S3,S4,Dp
B_ATX_PWROK Power from +12V_MAIN Power from +12V_SB
+12V_CPU S0 → CPU VCORE+VCCGT ON NCP81203MNTXG NCP81166MNTBG 3 VCORE+2 VCCGT → +VCORE++VCCGT S0
SLP_S3# H=Power on L=Power off
+VCCSA H=Power on L=Power off
+5V_AUX S5,S0,S3,S4 → USB Charger PERICOM PI5USB2546AZHEX → USB CHARGING S0,S3,S4
Charge_power H=Power on L=Power off
+5V_AUX S5,S0,S3,S4 → N-FET APEC AP4028EH Linear → +5V_DUAL_USBKB S0,S3
SLP_S4# H=Power on L=Power off
+5V_AUX S5,S0,S3,S4 → +5V_SMART_USB DIODES AP22802AW5-7 Linear → +5V_SMART_USB S0,S3,S4
5V_SMART_USB_EN H=Power on L=Power off
+5V_AUX S5,S0,S3,S4 → N-FET APEC AP4028EH Linear → +5V_MAIN S0
B_ATX_PWROK H=Power on L=Power off
+3P3V_SB S5,S0,S3,S4,Dp → N-FET APEC AP4028EH Linear → +3V_MAIN S0
B_ATX_PWROK H=Power on L=Power off
+12V_DUAL S5,S0,S3,S4,Dp
+5V_AUX /+3P3V_SB Dual VR Richtek RT6575BGQW
+5VAUX_LDO S5,S0,S3,S4.Dp
+3V_SB_LDO S5,S0,S3,S4,Dp
+5V_AUX S5,S0,S3,S4
+3P3V_SB S5,S0,S3,S4.Dp
+3P3V_LPS_LDO H=Power on L=Power off
SLP_SUS# H=Power on L=Power off
+12V_DUAL S5,S0,S3,S4Dp → DDR4 RICHTEK RT8237EZQW Switcher, 1ph → +VDDQ S0,S3
SLP_S4# H=Power on L=Power off
VPP_PG H=Power on L=Power off
+3P3V_SB S5,S0,S3,S4,Dp → P-FET AOS AO3415AL Linear → +3P3V_PCIAUX S5,S0,S3,S4
O_PCIAUX_CTRL L=Power on H=Power off
+3P3V_SB S5,S0,S3,S4,Dp → P-FET AOS AO3415AL Linear → +3P3V_AUX S5,S0,S3,S4
O_SUS_3VON L=Power on H=Power off
+12V_DUAL S5,S0,S3,S4,Dp → PCH AOS AOZ2238QI-02 SWITCHER → +1P0V_PCH_AUX S5,S0,S3,S4
SLP_SUS# H=Power on L=Power off
+3P3V_AUX S5,S0,S3,S4 → +VCCPLL_OC APEC APL5325BI-TRG Linear → +VCCPLL_OC S0,S3
VPP_PG H=Power on L=Power off
SLP_S4# H=Power on L=Power off
+VDDQ S0,S3 → +VTT ON NCP51200MNTXG Linear → +VTT S0
SLP_S3# H=Power on L=Power off
DDR_VTT_CNTL H=Power on L=Power off
+12V_DUAL S5,S0,S3,S4Dp → DDR4 AOS AOZ2236QI-02 Switcher, 1ph → +VPP S0,S3
SLP_S4# H=Power on L=Power off
B_ATX_PWROK H=Power on L=Power off
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GPIO	Native Function (M: Mobile Only); (D: Desktop Only); (S: Server Only)	Strap Function	PU/PD	I/O	Voltage Tolerance (V)	Power Well	GIO or Native	Buffer Type	Reset Output Value	S0 Output	S3 Output	S4/S5 Output	Function	Native or GP I/O	Output Level on Server Board	Required
75	SML1DATA			I/O	3.3	Sus	N	I	Z	Z	Df	Df	SML1DATA	N	I	-
74	SML1ALERT#/ TEMP_ALERT#/NFC			I/O	3.3	Sus	N	I	Z	Z	Df	Df	Rsvd	G	I	-
73	PCICLKRQ0#			I/O	3.3	Sus	N	I	Z	Z	Df	Df	BRD_REV1	G	I	-
72	M: BATLOW#			I/O	3.3	Sus	N	I	Z	Z	Df	Df	BATLOW#	N	I	-
71	S: TACH7		20k PU[2]	I/O	3.3	Core	N	I	Z	Z	Df	-	BRD_ID0	G	I	-
70	S: TACH6		20k PU[2]	I/O	3.3	Core	N	I	Z	Z	Df	-	BOOT_BLK_REC#	G	I	-
69	S: TACH5		20k PU[2]	I/O	3.3	Core	G	I	Z	Z	Df	-	COMM_B_DET#	G	I	-
68	S: TACH4		20k PU[2]	I/O	3.3	Core	G	I	Z	Z	Df	-	FR_USB_DET1#	G	I	-
67	CLKOUTFLEX3		20k PD[3]	I/O	3.3	Core	N	O	0	Df	Df	-	CLKOUTFLEX3	N	O	x
66	CLKOUTFLEX2		20k PD[3]	I/O	3.3	Core	N	O	0	Df	Df	-	CLKOUTFLEX2	N	O	x
65	CLKOUTFLEX1		20k PD[3]	I/O	3.3	Core	N	O	0	Df	Df	-	CLKOUTFLEX1	N	O	x
64	CLKOUTFLEX0		20k PD[3]	I/O	3.3	Core	N	O	0	Df	Df	-	CLKOUTFLEX0	N	O	x
63	SLP_S5#			I/O	3.3	Sus	N	O	0	1	1	1	SLP_S5#	N	O	x
62	SUSCLK	PLL VR EN	20k PU[6]	I/O	3.3	Sus	N	O	0	Df	Df	Df	SUSCLK	N	O	x
61	SUS_STAT#			I/O	3.3	Sus	N	O	0	1	1	0	PRNTR_DET#	G	I	Y
60	SML0ALERT#			I/O	3.3	Sus	N	OD	Z	Z	Df	Df	MXM_PWR_LEVEL	G	O	1
59	OC0#			I/O	3.3	Sus	N	I	Z	Z	Df	Df	OC0#	N	I	-
58	SML1CLK			I/O	3.3	Sus	N	I	Z	Z	Df	Df	SML1CLK	N	I	-
57	NFC			I/O	3.3	Sus	G	I	Z	Z	Df	Df	Rsvd	G	I	-
56	M: PEG_B_CLKRQ#[9]			I/O	3.3	Sus	N	I	Z	Z	Df	Df	N/A	N	I	-
55	-	Top-block Swap Override	20k PU[4,5]	I/O	3.3	Core	G	O	1	1	1	-	Rsvd	G	O	1
54	-			I/O	3.3	Core	G	I	Z	Z	Df	-	BOOT_BLK_EN#	G	I	-
53	-	ESI Strap[9]	20k PU[4,5]	I/O	3.3	Core	G	O	1	1	1	-	PWR_COMA_CFG1	G	O	1
52	-			I/O	3.3	Core	G	I	Z	Z	Df	-	CVTR_PRESENT#	G	I	-
51	-	BBS1	20k PU[4,5]	I/O	3.3	Core	G	O	1	1	1	-	Rsvd	G	O	1
50	-			I/O	3.3	Core	G	I	Z	Z	Df	-	TPNL_PRESENT#	G	I	-
49	SATAGP5			I/O	3.3	Core	G	I	Z	Z	Df	-	Rsvd	G	I	-
48	SDATAOUT1			I/O	3.3	Core	G	I	Z	Z	Z	-	CHASSIS_ID1	G	I	-
47	M: PEG_A_CLKRQ#[9]			I/O	3.3	Sus	N	I	Z	Z	Df	Df	N/A	N	I	-
46	PCIECLKRQ7#		20k PU[6]	I/O	3.3	Sus	N	I	Z	Z	Df	Df	PCI_EXT_DET#/MXM_DET#/PCI_RISER_DET#	G	I	-
45	PCIECLKRQ6#			I/O	3.3	Sus	N	I	Z	Z	Df	Df	STD_PS_DET#	G	I	-
44	PCIECLKRQ5#		20k PU[6]	I/O	3.3	Sus	N	I	Z	Z	Df	Df	PCIE_RISER_DET#	G	I	-
43	OC4#			I/O	3.3	Sus	N	I	Z	Z	Df	Df	PASSWORD_EN	G	I	-
42	OC3#			I/O	3.3	Sus	N	I	Z	Z	Df	Df	OC3#	N	I	-
41	OC2#			I/O	3.3	Sus	N	I	Z	Z	Df	Df	OC2#	N	I	-
40	OC1#			I/O	3.3	Sus	N	I	Z	Z	Df	Df	OC1#	N	I	-
39	SDATAOUT0			I/O	3.3	Core	G	I	Z	Z	Z	-	BRD_ID1	G	I	-
38	SLOAD			I/O	3.3	Core	G	I	Z	Z	Df	-	CHASSIS_ID0	G	I	-
37	SATA3GP	TLS Conf.	20k PU[7]	I/O	3.3	Core	G	I	0	Z	Df	-	Rsvd	G	I	-
36	SATA2GP	Rsvd	20k PU[7]	I/O	3.3	Core	G	I	0	Z	Df	-	Rsvd	G	I	-
35	S: NMI#			I/O	3.3	Core	G	O	1	1	1	-	BRD_REV0	G	I	-
34	-			I/O	3.3	Core	G	I	Z	Z	Df	-	HOOD_LOCK_DET	G	I	-
33	M: HAD_DOCK_EN#	Rsvd		I/O	3.3	Core	G	O	0	0	1	-	Rsvd	G	I	-
32	-			I/O	3.3	Core	G	O	1	1	Df	-	PWR_COMB_CFG1	G	O	1
31	M: ACPRESENT		20k PD[8]	I/O	3.3	DSW	G	I	Z	Z	Df	Df	Rsvd	G	I	-
30	SUSWARN#/ SUSPWRDNACK			I/O	3.3	Sus	N	O	0	1	Df	Df	SUSWARN#	N	O	x
29	SLP_WLAN#			I/O	3.3	DSW	G[1]	O	0	0	1	Df	SLP_WLAN#	N	O	x
28	-			I/O	3.3	Sus	G	O	0	0	0	0	PWR_COMA_CFG0	G	O	0
27	-		20k PD[8]	I/O	3.3	DSW	G	I	Z	Z	Z	Z	DSW_WOL_WAKE	G	I	-
26	PCIECLKRQ4#			I/O	3.3	Sus	N	I	Z	Z	Df	Df	PWR_SER_DET#	G	I	-
25	PCIECLKRQ3#			I/O	3.3	Sus	N	I	Z	Z	Df	Df	BRD_ID2	G	I	-
24	-			I/O	3.3	Sus	G[1]	O	0	0	Df	Df	PWR_COMB_CFG0	G	O	0
23	LDRQ1#		20k PU	I/O	3.3	Core	N	I	Z	Z	Df	-	LDRQ1#	N	I	-
22	SCLOCK			I/O	3.3	Core	G	I	Z	Z	Df	-	INT_USB_DET1#	G	I	-
21	SATA0GP			I/O	3.3	Core	G	I	Z	Z	Df	-	FRNT_AUD_DET#	G	I	-
20	PCIECLKRQ2 S: SMI#			I/O	3.3	Core	N	I	Z	Z	Df	-	PCIECLKRQ2#	N	I	-
19	SATA1GP	BBS0	20k PU[7]	I/O	3.3	Core	G	I	1	Z	Df	-	Rsvd	G	I	-
18	PCIECLKRQ1#			I/O	3.3	Core	N	I	Z	Z	Df	-	MXM_PWR_GD	G	I	-
17	S: TACH0		20k PU[2]	I/O	3.3	Core	G	I	Z	Z	Df	-	HOOD_SW_DET#	G	I	-
16	SATA4GP			I/O	3.3	Core	G	I	Z	Z	Df	-	Rsvd	G	I	-
15	-			I/O	3.3	Sus	G	O	0	0	Df	Df	WRITE_EDID_ROM	G	O	0
14	OC7#			I/O	3.3	Sus	N	I	Z	Z	Df	Df	OC7#	N	I	-
13	M: HAD_DOCK_RST#			I/O	3.3	Sus	G	I	Z	Z	Z	Z	INT_USB_DET2#	G	I	-
12	LAN_PHY_PWR_CTRL			I/O	3.3	Sus	N[4]	O	0	0	Df	Df	LAN_DISABLE#	N	O	x
11	SMBALERT#			I/O	3.3	Sus	N	I	Z	Z	Df	Df	CBB_PRESENT#	G	I	-
10	OC6#			I/O	3.3	Sus	N	I	Z	Z	Df	Df	OC6#	N	I	-
9	OC5#			I/O	3.3	Sus	N	I	Z	Z	Df	Df	OC5#	N	I	-
8	-	Rsvd	20k PU[6]	I/O	3.3	Sus	G	O	1	1	Df	Df	Rsvd	G	I	-
7	S: TACH3		20k PU[2]	I/O	3.3	Core	G	I	Z	Z	Df	-	MXM_TH_ALERT#	G	I	-
6	S: TACH2		20k PU[2]	I/O	3.3	Core	G	I	Z	Z	Df	-	SMI# from SIO	G	I	-
5	PIRQH#			I/OD	5	Core	G	I	Z	Z	Df	-	GS_INT2#	G	I	-
4	PIRQG#			I/OD	5	Core	G	I	Z	Z	Df	-	Rsvd	G	I	-
3	PIRQF#			I/OD	5	Core	G	I	Z	Z	Df	-	MXM_RESET#	G	O	OD
2	PIRQE#			I/OD	5	Core	G	I	Z	Z	Df	-	MXM_PWR_EN#	G	O	OD
1	S: TACH1		20k PU[2]	I/O	3.3	Core	G	I	Z	Z	Df	-	MXM_TH_OVERT#	G	I	-
0	BMBUSY#			I/O	3.3	Core	G	I	Z	Z	Df	-	FR_USB_DET0#	G	I	-

Signal	Usage	When Sampled	Comment
SATA1GP / GPIO19	Boot BIOS Strap bit 0 (BBS0)	Rising edge of PWROK	This signal has a weak internal pull-up. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. **Bit11 / Bit 10 — Boot BIOS Destination** 0 1 — Reserved 1 0 — Reserved 1 1 — SPI (default) 0 0 — LPC **NOTES:** 1. The internal pull-up is disabled after PLTRST# deasserts. 2. If option 00 (LPC) is selected, BIOS may still be placed on LPC, but the platform is required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GbE LAN. 4. See Chapter 10, "GCS—General Control and Status Register" for additional information.

Signal	Usage	When Sampled	Comment
GPIO51	Boot BIOS Strap bit 1 (BBS1)	Rising edge of PWROK	This signal has a weak internal pull-up. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. **Bit11 / Bit 10 — Boot BIOS Destination** 0 1 — Reserved 1 0 — Reserved 1 1 — SPI (default) 0 0 — LPC **NOTES:** 1. The internal pull-up is disabled after PLTRST# deasserts. 2. If option 00 (LPC) is selected, BIOS may still be placed on LPC, but the platform is required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GbE LAN. 4. See Chapter 10, "GCS—General Control and Status Register" for additional information.
SATA2GP / GPIO36	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. **NOTES:** 1. The internal pull-down is disabled after PLTRST# deasserts. 2. This signal should not be pulled high when strap is sampled.
SATA3GP / GPIO37	TLS Confidentiality	Rising edge of PWROK	This signal has a weak internal pull-down. **0 = Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality) **1 = Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality) **NOTES:** 1. The internal pull-down is disabled after PLTRST# deasserts. 2. A strong pull-up may be needed for GPIO functionality 3. This signal must be pulled up to support Intel AMT with TLS. Intel ME configuration parameters also need to be set correctly to enable TLS. 4. This signal is in the Core well.

Signal	Usage	When Sampled	Comment
HDA_SDO	Flash Descriptor Security Override	Rising edge of PWROK	This signal has a weak internal pull-down. **0 = Enable** security measures defined in the Flash Descriptor. **1 = Disable** Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. **NOTES:** 1. The weak internal pull-down is disabled after PLTRST# deasserts. 2. Asserting the HDA_SDO high on the rising edge of PWROK will also halt Intel® Management Engine after chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug. 3. This signal is in the Suspend well.
HDA_DOCK_EN# / GPIO33	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. **NOTES:** 1. The internal pull-down is disabled after PLTRST# deasserts. 2. This signal should not be pulled high when strap is sampled.
INTVRMEN	Integrated VRM Enable	Always	This signal does not have an internal resistor; an **external** resistor is **required**. **0 = DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source (should be connected to an external VRM). External VR powering option is for Mobile Only. Other systems should not pull the strap low.** **1 = Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left floating.** **NOTES:** 1. This signal is always sampled. 2. This signal is in the RTC well.
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	Rising edge of RSMRST#	This signal has a weak internal pull-up. **0 = Disable** PLL On-Die voltage regulator. **1 = Enable** PLL On-Die voltage regulator. **NOTES:** 1. The internal pull-up is disabled after RSMRST# deasserts. 2. This signal is in the Suspend well.

Signal	Usage	When Sampled	Comment
DSWVRMEN	DeepSx Well On-Die Voltage Regulator Enable	Always	This signal does not have an internal resistor; an **external** resistor is **required**. **0 = Disable** Integrated DeepSx Well (DSW) On-Die Voltage Regulator. **1 = Enable** DSW 3.3V-to-1.05V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards; the external mode is only used for testing environments. **NOTES:** 1. This signal is always sampled. 2. This signal is in the RTC well.
GPIO8	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull-up but **requires an external pull down**. **NOTES:** 1. The internal pull-up is disabled after RSMRST# deasserts. 2. This signal **must be pulled low** when strap is sampled. 3. This signal is in the Suspend well.
SPKR	No Reboot	Rising edge of PWROK	The signal has a weak internal pull-down. **0 = Disable** "No Reboot" mode. **1 = Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). **NOTES:** 1. The internal pull-down is disabled after PLTRST# deasserts. 2. The status of this strap is readable using the NO REBOOT bit (Chipset Config Registers: RCBA + Offset 3410h:Bit 5). 3. See Chapter 10, "GCS—General Control and Status Register" for additional information. 4. This signal is in the Core well.
GPIO53	Reserved	Rising edge of PWROK	This signal has a weak internal pull-up. **NOTES:** 1. The internal pull-up is disabled after PLTRST# deasserts. 2. This signal should not be pulled low when strap is sampled.

Signal	Usage	When Sampled	Comment
GPIO55	Top-Block Swap Override	Rising edge of PWROK	The signal has a weak internal pull-up. **0 = Enable** "Top-Block Swap" mode - PCH will invert A16 for cycles going to the upper two 64 KB blocks in the FWH or appropriate address lines (A16, A17, A18, A19 or A20) as selected in BIOS Boot-Block size soft strap for SPI. **1 = Disable** "Top-Block Swap" mode. **NOTES:** 1. The internal pull-up is disabled after PLTRST# deasserts. 2. Software will not be able to clear the Top-Block Swap bit until the system is rebooted. 3. This signal is in the Core well. 4. The status of this strap is readable using the Top-Block Swap bit (Chipset Config Registers: RCBA + Offset 3414h:Bit 0).
DDPB_CTRLDATA	Port B Detected	Rising edge of PWROK	This signal has a weak internal pull-down. **0** = Port B is not detected. **1** = Port B is detected. **NOTES:** 1. The internal pull-down is disabled after PLTRST# deasserts.
DDPC_CTRLDATA	Port C Detected	Rising edge of PWROK	This signal has a weak internal pull-down. **0** = Port C is not detected. **1** = Port C is detected. **NOTES:** 1. The internal pull-down is disabled after PLTRST# deasserts.
DDPD_CTRLDATA	Port D Detected	Rising edge of PWROK	This signal has a weak internal pull-down. **0** = Port D is not detected. **1** = Port D is detected. **NOTES:** 1. The internal pull-down is disabled after PLTRST# deasserts.

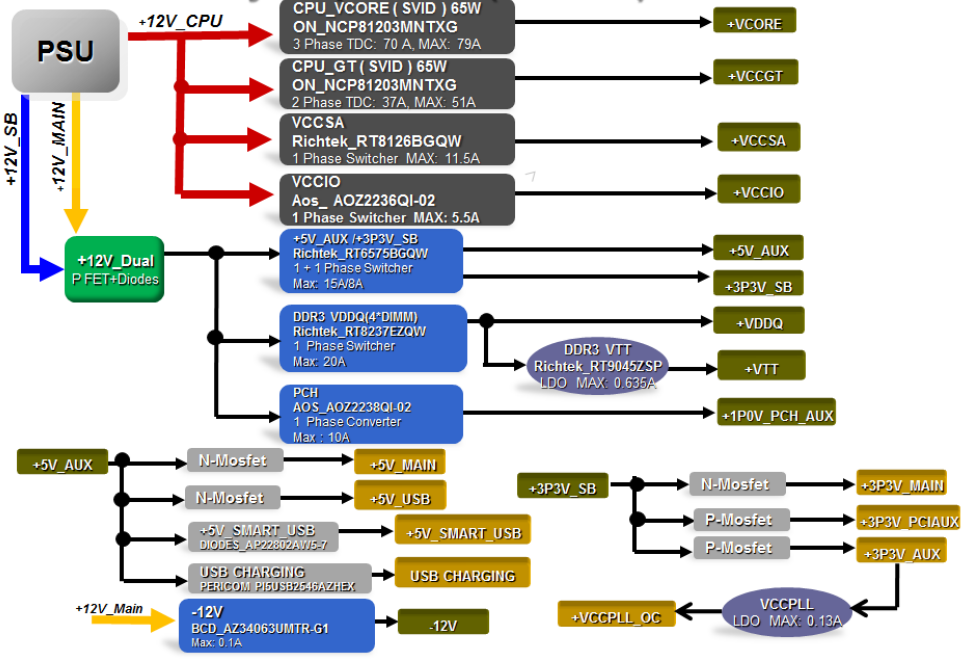
DELL INC.

Title: **STRAP and GPIO**

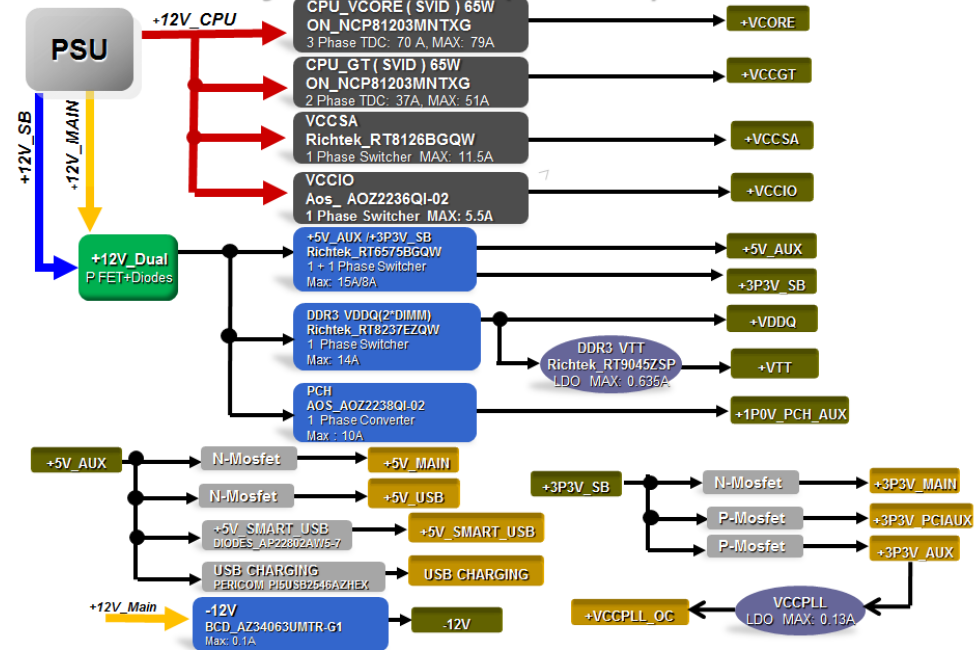
DWG NO: *D7* Rev: A00

Date: Monday, July 27, 2015 Sheet 6 of 86

Power Delivery Map_DDR3(4*DIMM)



Power Delivery Map_DDR3(2*DIMM)



DELL INC.

Title: TBD

DWG NO: D7

Rev: A00

Date: Monday, July 27, 2015 Sheet 7 of 86

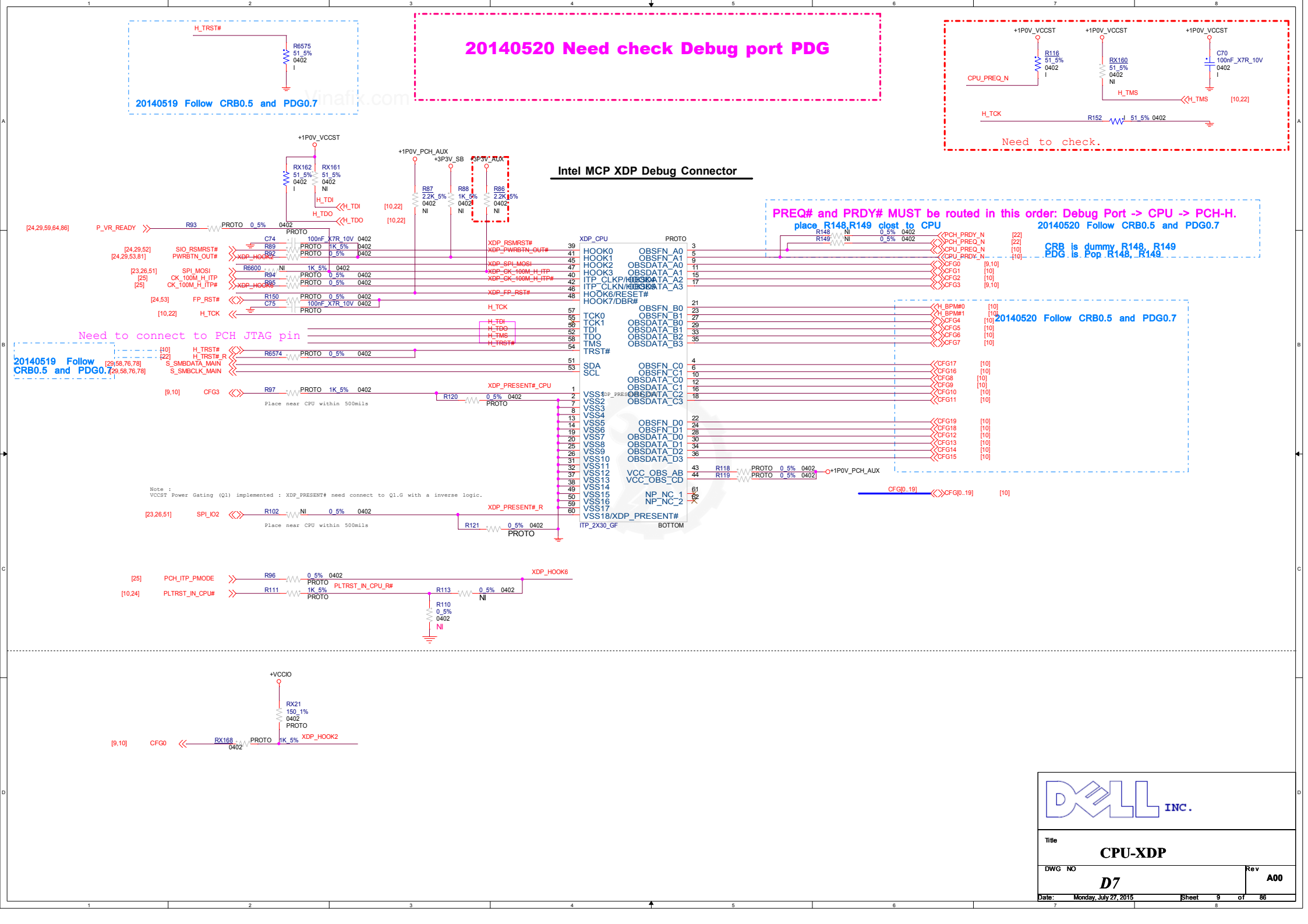
DELL INC.

Title

Interrupt & PME

DWG NO	Rev
D7	A00

Date: Monday, July 27, 2015 Sheet 8 of 86


20140520 Need check Debug port PDG
20140519 Follow CRB0.5 and PDG0.7
Need to check.
Intel MCP XDP Debug Connector
PREQ# and PRDY# MUST be routed in this order: Debug Port -> CPU -> PCH-H.
place R148,R149 clost to CPU
20140520 Follow CRB0.5 and PDG0.7
CRB is dummy R148, R149
PDG is Pop R148, R149
Need to connect to PCH JTAG pin
Note :
VCCST Power Gating (Q1) implemented : XDP_PRESENT# need connect to Q1.G with a inverse logic.
Place near CPU within 500mils
XDP_CPU
ITP_2X30_GF
BOTTOM
DELL INC.
Title
CPU-XDP
DWG NO
D7
Rev
A00
Date: Monday, July 27, 2015
Sheet 9 of 86

APU - VID,CTRL, MSIC

20140508 The resistors value of SVID follow CRB0.5 and PDG0.7

Need to check VR control power level. Level Shift?

20140516 CRB0.5 add RS 33 ohm , but PDG0.7 is 20 ohm , need check Intel

20140519 Need check with Intel about RS value . CRB is 0 ohm , PDG0.7 is 500 ohm

20140519 Change net name to H_SKTOCC#

20140516 SKL-S EDS0.75:It should be connected to VCCIO with pull-up resistor of xx

20140520 PU EDS0.75 "Stuff R47 for Enable eDP ,unstuff R38, R1 for PCIe X16

20140520 EDS0.75 CFG[19:8]: Reserved configuration lanes.

SKL S has adequate internal bias resistance on JTAG, PROC_PRDY# to keep the devices in an idel state without the external pull resistors.

PEI-E CONFIG TABLE		
CFG5	CFG6	PCI-E CONFIG
0	0	X8 X4 X4
0	1	RESERVED
1	0	X8 X8
1	1	X16

CFG	High	Low	Strap Description
0	NORMAL	STALL	EAR
1	NORMAL	PCHLESS	PCHLESS MODE
2	NORMAL	REVERSE	PEG_LANE_REVERSAL
3	ENABLE	DISABLE	PHYSICAL_DEBUG_ENABLE
4	DISABLE	ENABLE	eDP en/dis
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET_N	BIOS REQ	PEG_DEFER_TRAINING
8	DISABLE	ENABLE	CFG UNLOCK
9	PRESENT	NOT PRESENT	SVID NOT PRESENT
10	ACTIVE	DEACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DMI_AC_COUPLED
12	PMSYNC 2.0	LEGACY	PMSYNC LEGACY
13	SYNC	ASYNC	PMSYNC ASYNC MODE
14	RESERVED		
15	RESERVED		

ALL PINS HAVE INTERNAL PULL-UPS

CPUE

Socket_LGA 1151_15u_Black

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CL_LGA1151_FARALLON_SHF

XU1_2

DELL INC.

Title: CPU

DWG NO: D7

Rev: A00

Date: Monday, July 27, 2015 Sheet 10 of 86

DDR3 CH-A

CPUA

20140423 correted M_A_MA[13..0] to M_A_MA[15..0]

20140423 SKYLAKE-S PIN NAME 0.7DDR3 MAA14/15 should be here

20140423 DDR3 Design need check CRB

20140423 SKYLAKE-S PIN NAME 0.7 DDR3 RAS/CAS/WE

1 OF 10

Socket_LGA 1151_15u_Black

DDR3 CH-B

CPUB

20140423 corret M_B_MA[13..0] to M_B_MA[15..0]

20140423 SKYLAKE-S PIN NAME 0.7 DDR3 MAB14/15 should be here

20140423 SKYLAKE-S PIN NAME 0.7 DDR3 RAS/CAS/WE

20140423 DDR3 Design need check CRB

2 OF 10

Socket_LGA 1151_15u_Black

DDR3 DRAMRST# BUFFER CIRCUIT

Place close to DIMMs

R6587 NI SHORT-PAD-4 0402_4Mil +VDDDQ

R6588 470_1% 0402

U139

M_AB_RESET_N

SLP_S4#

R6589 NI SHORT-PAD-4 0402_4Mil DDR3_DRAMRST#

R6586 10K_5%

C1735 100nF_X5R_10V 0402

M_B_DQ_VREF

M_A_DQ_VREF

CD44 220nF_X7R_16V 0603

CD11 220nF_X7R_16V 0603

RD24 24.9_1%

RD17 24.9_1%

DELL INC.

Title: DDR3 CHANEL A/B

DWG NO: D7

Rev: A00

Date: Monday, July 27, 2015 Sheet 11 of 86

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title

CPU

DWG NO

D7

Rev

X02

Date: Monday, July 27, 2015 Sheet 12 of 86

MCP - PCIE,DMI,FDI,DDI

PEG AC Cap Value	
Gen1/Gen2	75nf~265nf
Gen3	180nf~265nf

PEG x16 & DMI - Refer to PDG page45
Breakout
MS = 10/4/4/4/10
DSL = 10/3/3.5/3/10

Main
12/3.5/4.5/3.5/12 (Group)
15/3.5/4.5/3.5/15 (Other)

+VCCSA
CX80 100nF_X7R_16V 0402
+VCCSA
CX82 100nF_X7R_16V 0402

PEG_RCOMP:
Trace Width = 12 mils
Spacing = 15 mils
Length = 400mils

CPUC

[37]	EXP_A_RXP_0	B8	PEG_RX[0]	PEG_TX[0]	A5	EXP_A_TXP_0_C [37]
[37]	EXP_A_RXN_0	B7	PEG_RX#[0]	PEG_TX#[0]	A6	EXP_A_TXN_0_C [37]
[37]	EXP_A_RXP_1	C7	PEG_RX[1]	PEG_TX[1]	B4	EXP_A_TXP_1_C [37]
[37]	EXP_A_RXN_1	C6	PEG_RX#[1]	PEG_TX#[1]	B5	EXP_A_TXN_1_C [37]
[37]	EXP_A_RXP_2	D6	PEG_RX[2]	PEG_TX[2]	C3	EXP_A_TXP_2_C [37]
[37]	EXP_A_RXN_2	D5	PEG_RX#[2]	PEG_TX#[2]	C4	EXP_A_TXN_2_C [37]
[37]	EXP_A_RXP_3	E5	PEG_RX[3]	PEG_TX[3]	D2	EXP_A_TXP_3_C [37]
[37]	EXP_A_RXN_3	E4	PEG_RX#[3]	PEG_TX#[3]	D3	EXP_A_TXN_3_C [37]
[37]	EXP_A_RXP_4	F6	PEG_RX[4]	PEG_TX[4]	E1	EXP_A_TXP_4_C [37]
[37]	EXP_A_RXN_4	F5	PEG_RX#[4]	PEG_TX#[4]	E2	EXP_A_TXN_4_C [37]
[37]	EXP_A_RXP_5	G5	PEG_RX[5]	PEG_TX[5]	F2	EXP_A_TXP_5_C [37]
[37]	EXP_A_RXN_5	G4	PEG_RX#[5]	PEG_TX#[5]	F3	EXP_A_TXN_5_C [37]
[37]	EXP_A_RXP_6	H6	PEG_RX[6]	PEG_TX[6]	G1	EXP_A_TXP_6_C [37]
[37]	EXP_A_RXN_6	H5	PEG_RX#[6]	PEG_TX#[6]	G2	EXP_A_TXN_6_C [37]
[37]	EXP_A_RXP_7	J5	PEG_RX[7]	PEG_TX[7]	H2	EXP_A_TXP_7_C [37]
[37]	EXP_A_RXN_7	J4	PEG_RX#[7]	PEG_TX#[7]	H3	EXP_A_TXN_7_C [37]
[37]	EXP_A_RXP_8	K6	PEG_RX[8]	PEG_TX[8]	J1	EXP_A_TXP_8_C [37]
[37]	EXP_A_RXN_8	K5	PEG_RX#[8]	PEG_TX#[8]	J2	EXP_A_TXN_8_C [37]
[37]	EXP_A_RXP_9	L5	PEG_RX[9]	PEG_TX[9]	K2	EXP_A_TXP_9_C [37]
[37]	EXP_A_RXN_9	L4	PEG_RX#[9]	PEG_TX#[9]	K3	EXP_A_TXN_9_C [37]
[37]	EXP_A_RXP_10	M6	PEG_RX[10]	PEG_TX[10]	L1	EXP_A_TXP_10_C [37]
[37]	EXP_A_RXN_10	M5	PEG_RX#[10]	PEG_TX#[10]	L2	EXP_A_TXN_10_C [37]
[37]	EXP_A_RXP_11	N5	PEG_RX[11]	PEG_TX[11]	M2	EXP_A_TXP_11_C [37]
[37]	EXP_A_RXN_11	N4	PEG_RX#[11]	PEG_TX#[11]	M3	EXP_A_TXN_11_C [37]
[37]	EXP_A_RXP_12	P6	PEG_RX[12]	PEG_TX[12]	N1	EXP_A_TXP_12_C [37]
[37]	EXP_A_RXN_12	P5	PEG_RX#[12]	PEG_TX#[12]	N2	EXP_A_TXN_12_C [37]
[37]	EXP_A_RXP_13	R5	PEG_RX[13]	PEG_TX[13]	P2	EXP_A_TXP_13_C [37]
[37]	EXP_A_RXN_13	R4	PEG_RX#[13]	PEG_TX#[13]	P3	EXP_A_TXN_13_C [37]
[37]	EXP_A_RXP_14	T6	PEG_RX[14]	PEG_TX[14]	R2	EXP_A_TXP_14_C [37]
[37]	EXP_A_RXN_14	T5	PEG_RX#[14]	PEG_TX#[14]	R1	EXP_A_TXN_14_C [37]
[37]	EXP_A_RXP_15	U5	PEG_RX[15]	PEG_TX[15]	T2	EXP_A_TXP_15_C [37]
[37]	EXP_A_RXN_15	U4	PEG_RX#[15]	PEG_TX#[15]	T3	EXP_A_TXN_15_C [37]

[21]	DMI_PCH_CPU_RXP0	Y3	DMI_RX[0]	DMI_TX[0]	AC2	DMI_CPU_PCH_RXP0 [21]
[21]	DMI_PCH_CPU_RXN0	Y4	DMI_RX#[0]	DMI_TX#[0]	AC1	DMI_CPU_PCH_RXN0 [21]
[21]	DMI_PCH_CPU_RXP1	AA4	DMI_RX[1]	DMI_TX[1]	AD3	DMI_CPU_PCH_RXP1 [21]
[21]	DMI_PCH_CPU_RXN1	AA5	DMI_RX#[1]	DMI_TX#[1]	AD2	DMI_CPU_PCH_RXN1 [21]
[21]	DMI_PCH_CPU_RXP2	AB4	DMI_RX[2]	DMI_TX[2]	AE2	DMI_CPU_PCH_RXP2 [21]
[21]	DMI_PCH_CPU_RXN2	AB3	DMI_RX#[2]	DMI_TX#[2]	AE1	DMI_CPU_PCH_RXN2 [21]
[21]	DMI_PCH_CPU_RXP3	AC4	DMI_RX[3]	DMI_TX[3]	AF2	DMI_CPU_PCH_RXP3 [21]
[21]	DMI_PCH_CPU_RXN3	AC5	DMI_RX#[3]	DMI_TX#[3]	AF3	DMI_CPU_PCH_RXN3 [21]

+VCCIO R6280 24.9_1% 0402 PEGICOMP_MCP L7 PEG_RCOMP

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Socket_LGA 1151_15u_Black

CPUD

		B13	DDIB_AUX	DDIB_TXB[0]	C21	DPB_LANE_DP0_C [39]
		C13	DDIB_AUX#	DDIB_TXB#[0]	D21	DPB_LANE_DN0_C [39]
				DDIB_TXB[1]	D22	DPB_LANE_DP1_C [39]
				DDIB_TXB#[1]	E22	DPB_LANE_DN1_C [39]
[82]	DPC_AUX_DP_C	A12	DDIC_AUX	DDIB_TXB[2]	B23	DPB_LANE_DP2_C [39]
[82]	DPC_AUX_DN_C	B12	DDIC_AUX#	DDIB_TXB#[2]	A23	DPB_LANE_DN2_C [39]
		B11	DDID_AUX	DDIB_TXB[3]	C23	DPB_LANE_DP3_C [39]
		C11	DDID_AUX#	DDIB_TXB#[3]	D23	DPB_LANE_DN3_C [39]
NOBOM	TPVIA291	E10	EDP_TX[0]	DDIC_TXC[0]	B18	DPC_LANE_DP0_C [82]
NOBOM	TPVIA386	D10	EDP_TX#[0]	DDIC_TXC#[0]	A18	DPC_LANE_DN0_C [82]
NOBOM	TPVIA387	D9	EDP_TX[1]	DDIC_TXC[1]	D18	DPC_LANE_DP1_C [82]
NOBOM	TPVIA388	C9	EDP_TX#[1]	DDIC_TXC#[1]	E18	DPC_LANE_DN1_C [82]
[58]	DP2VGA_LANE_DP2	G10	EDP_TX[2]	DDIC_TXC[2]	C19	DPC_LANE_DP2_C [82]
[58]	DP2VGA_LANE_DN2	H10	EDP_TX#[2]	DDIC_TXC#[2]	D19	DPC_LANE_DN2_C [82]
[58]	DP2VGA_LANE_DP3	F9	EDP_TX[3]	DDIC_TXC[3]	D20	DPC_LANE_DP3_C [82]
[58]	DP2VGA_LANE_DN3	G9	EDP_TX#[3]	DDIC_TXC#[3]	E20	DPC_LANE_DN3_C [82]
[58]	DP2VGA_AUX	D12	EDP_AUX	DDID_TXD[0]	B14	
[58]	DP2VGA_AUX#	E12	EDP_AUX#	DDID_TXD#[0]	A14	
				DDID_TXD[1]	C15	
				DDID_TXD#[1]	B15	
				DDID_TXD[2]	B16	
				DDID_TXD#[2]	A16	
				DDID_TXD[3]	C17	
				DDID_TXD#[3]	B17	

DP2VGA_AUX_
DP2VGA_AUX#

20140515 remove duplicated AC caps

+VCCIO R6290 24.9_1% 0402 EDP_RCOMP M9 EDP_RCOMP

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Socket_LGA 1151_15u_Black

Processor PCI Express* Compensation Signal Routing Guidelines					
Parameter	Units	Trace width	Trace spacing to other signals	Routing Length	Resistance
PEG_RCOMP	mils	12	15	400	
Resistor	ohm				24.9+-1%

2014-03-07-J

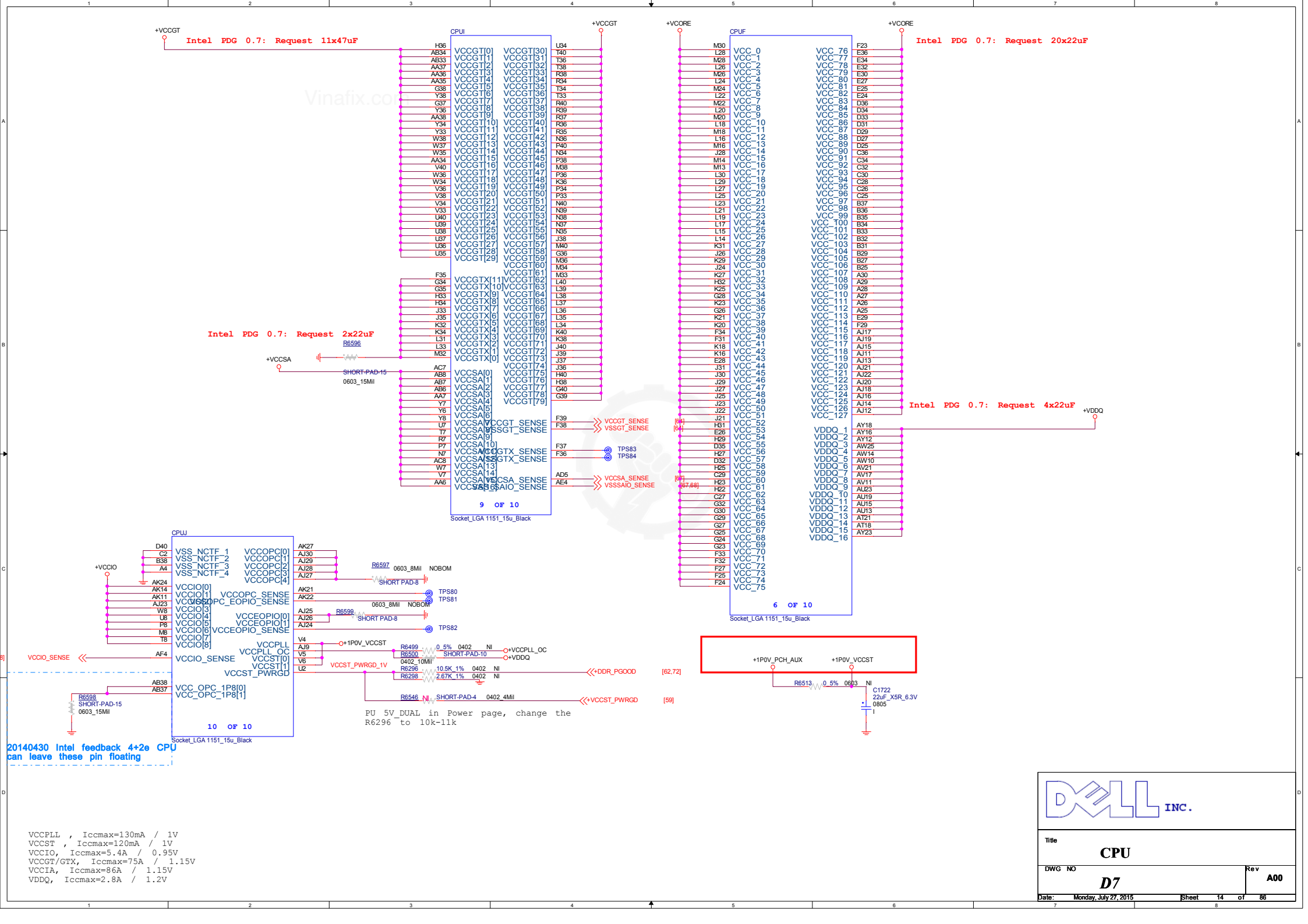
DELL INC.

Title: CPU

DWG NO: D7

Rev: A00

Date: Monday, July 27, 2015 Sheet 13 of 86


Intel PDG 0.7: Request 11x47uF
Intel PDG 0.7: Request 2x22uF
Intel PDG 0.7: Request 20x22uF
Intel PDG 0.7: Request 4x22uF
CPUI
9 OF 10
Socket_LGA 1151_15u_Black
CPUF
6 OF 10
Socket_LGA 1151_15u_Black
CPUJ
10 OF 10
Socket_LGA 1151_15u_Black
+VCCGT
+VCCSA
+VCORE
+VCCIO
+VDDQ
+1P0V_VCCST
+1P0V_PCH_AUX
VCCIO_SENSE
VCCST_PWRGD_1V
+DDR_PGOOD
+VCCST_PWRGD
+VCCPLL_OC
+VDDQ
PU 5V_DUAL in Power page, change the R6296 to 10k-11k
20140430 Intel feedback 4+2e CPU can leave these pin floating
VCCPLL , Iccmax=130mA / 1V
VCCST , Iccmax=120mA / 1V
VCCIO, Iccmax=5.4A / 0.95V
VCCGT/GTX, Iccmax=75A / 1.15V
VCCIA, Iccmax=86A / 1.15V
VDDQ, Iccmax=2.8A / 1.2V
DELL INC.
Title
CPU
DWG NO
D7
Rev
A00
Date: Monday, July 27, 2015
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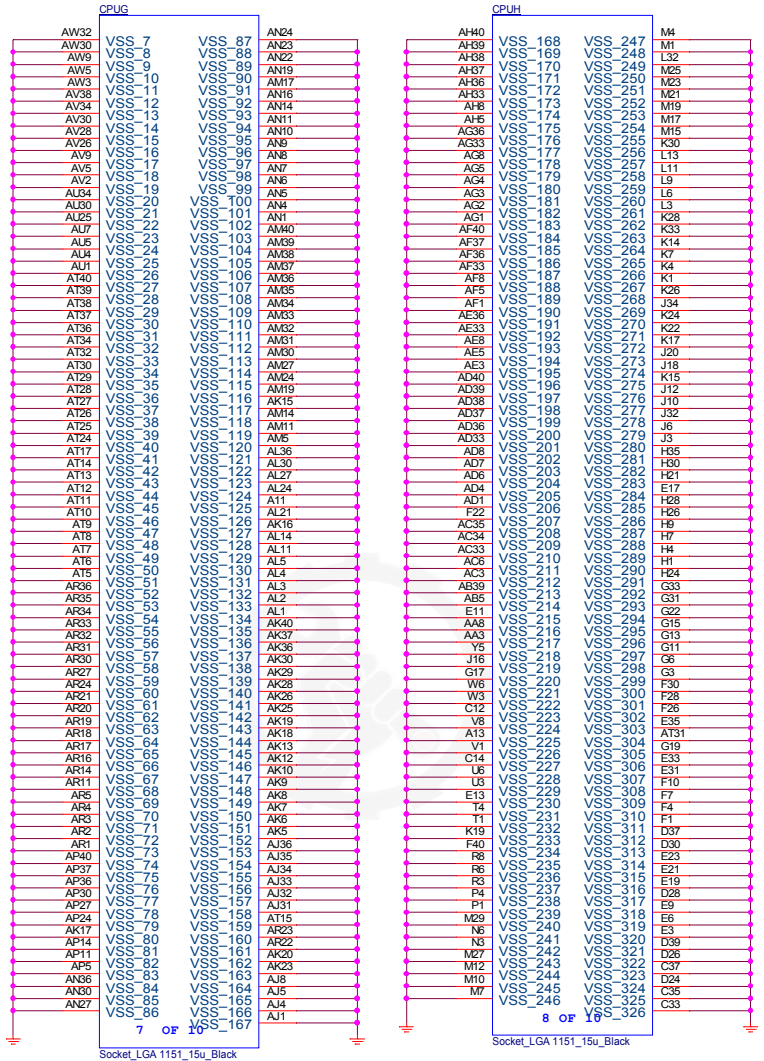


DELL INC.

Title: CPU

DWG NO: D7

Rev: A00

Date: Monday, July 27, 2015 Sheet 15 of 86

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title: **CPU**

DWG NO: ***D7***

Rev: **A00**

Date: Monday, July 27, 2015 Sheet 16 of 86

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title

CPU

DWG NO	Rev
D7	A00

Date: Monday, July 27, 2015 Sheet 17 of 86

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title: **CPU**

DWG NO: ***D7***

Rev: **A00**

Date: Monday, July 27, 2015 Sheet 18 of 86

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title

CPU

DWG NO

D7

Rev

A00

Date: Monday, July 27, 2015 Sheet 19 of 86

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

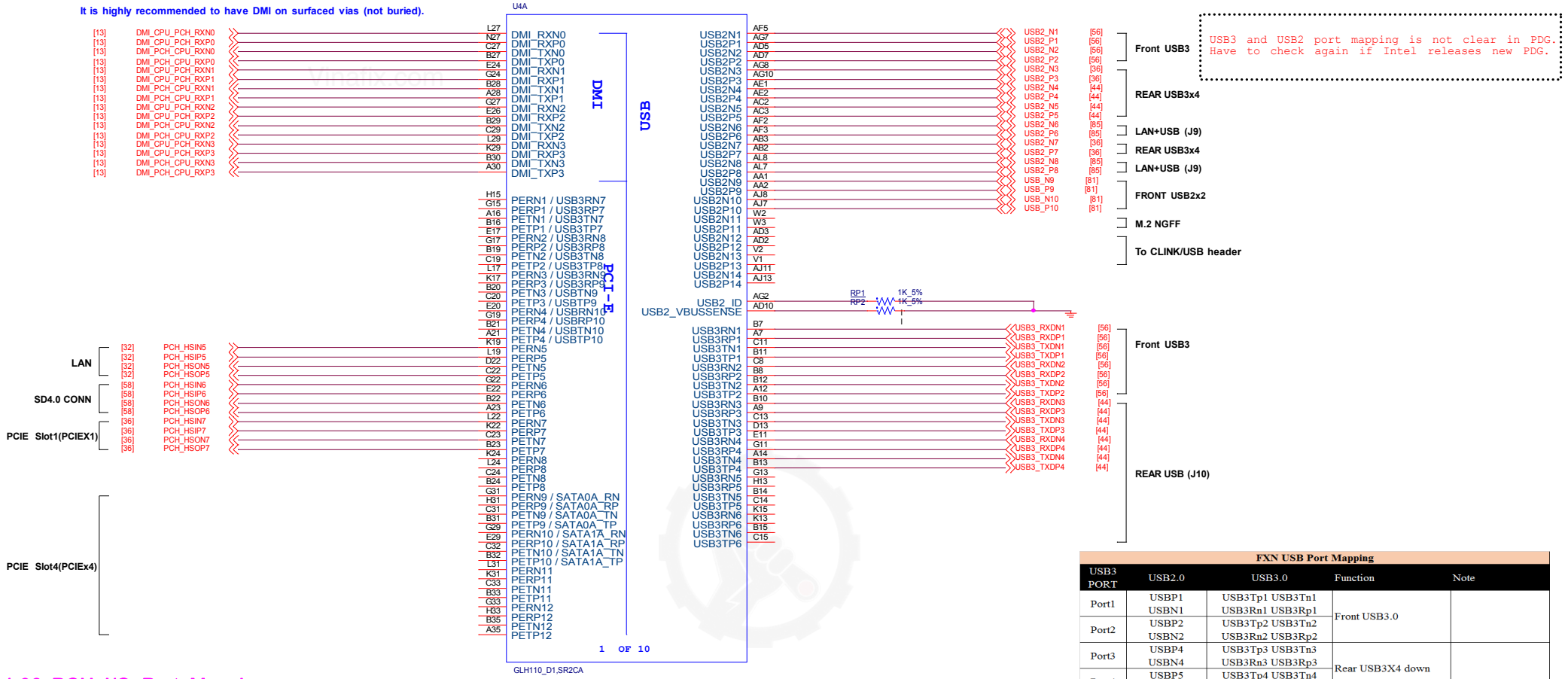
Title: **CPU**

DWG NO: ***D7***

Rev: **A00**

Date: Monday, July 27, 2015 Sheet 20 of 86

It is highly recommended to have DMI on surfaced vias (not buried).



USB3 and USB2 port mapping is not clear in PDG. Have to check again if Intel releases new PDG.

FXN USB Port Mapping

USB3 PORT	USB2.0	USB3.0	Function	Note
Port1	USBP1 USBN1	USB3Tp1 USB3Tn1 USB3Rn1 USB3Rp1	Front USB3.0	
Port2	USBP2 USBN2	USB3Tp2 USB3Tn2 USB3Rn2 USB3Rp2		
Port3	USBP4 USBN4	USB3Tp3 USB3Tn3 USB3Rn3 USB3Rp3	Rear USB3X4 down	
Port4	USBP5 USBN5	USB3Tp4 USB3Tn4 USB3Rn4 USB3Rp4		
Port5	USBP7 USBN7	USB3Tp5 USB3Tn5 USB3Rn5 USB3Rp5	Rear USB3X4 up	SFF3: CLINK/BT
Port6	USBP3 USBN3	USB3Tp6 USB3Tn6 USB3Rn6 USB3Rp6		

ARD1.06 PCH I/O Port Mapping

	Intel	3 Series PCB, H110		7/9 Series PCB, Q170	
Port#	Sunrise-Point	Interface	Device	Interface	Device
1	USB3#1	USB3	Front USB3 conn.	USB3	Front USB3 conn.
2	USB3#2	USB3	Front USB3 conn.	USB3	Front USB3 conn.
3	USB3#3	USB3	Rear USB3 conn.	USB3	Rear USB3 conn.
4	USB3#4	USB3	Rear USB3 conn.	USB3	Rear USB3 conn.
5	USB3#5			USB3	Rear USB3 conn.
6	USB3#6			USB3	Rear USB3 conn.
7	USB3#7/PCIE#1				
8	USB3#8/PCIE#2				
9	USB3#9/PCIE#3				
10	USB3#10/PCIE#4/GbE				
11	PCIE#5/GbE	PCIe	NIC	GbE	Intel NIC
12	PCIE#6	PCIe	SD 4.0 CR	PCIe	SD 4.0 CR
13	PCIE#7	PCIe	PCIe slot 1 (x1)		
14	PCIE#8	PCIe	M.2 WLAN*	PCIe	M.2 WLAN*
15	PCIE#9/SATA#0/GbE			PCIe	PCIe slot 1 (x4)
16	PCIE#10/SATA#1			PCIe	PCIe slot 1 (x4)
17	PCIE#11			PCIe	PCIe slot 1 (x4)
18	PCIE#12/GbE			PCIe	PCIe slot 1 (x4)
19	PCIE#13/SATA#0/GbE	SATA	HDD1	SATA	HDD1
20	PCIE#14/SATA#1	SATA	HDD2/ODD	SATA	HDD2/ODD
21	PCIE#15/SATA#2			SATA	HDD3
22	PCIE#16/SATA#3	SATA	M.2 SSD*		
23	PCIE#17/SATA#4			SATA/PCIe	M.2, SSD SATA/PCIe lane 1
24	PCIE#18/SATA#5			SATA/PCIe	M.2, SSD PCIe lane 2
25	PCIE#19			PCIe	M.2, SSD PCIe lane 3
26	PCIE#20			PCIe	M.2, SSD PCIe lane 4

USB Pin Assignment

USB2 Port	Pin Name	Pin Type	USB OC Port	Y/N	Note	Loction
1	USB2N1/P1	IN/OUT	USB_OC0_R_N	Y	Front USB3.0	USB3F2 port1
2	USB2N2/P2	IN/OUT		Y	Front USB3.0	USB3F2 port2
3	USB2N4/P4	IN/OUT	USB_OC1_R_N	Y	Rear USB 3.0x4 Down	USB3R1 port 1
4	USB2N5/P5	IN/OUT		Y	Rear USB 3.0x4 Down	USB3R1 port 2
5	USB2N7/P7	IN/OUT	USB_OC2_R_N	Y	Rear USB 3.0x4 up	USB3R1 port 3
6	USB2N3/P3	IN/OUT		Y	Rear USB 3.0x4 up	USB3R1 port 4
7	USB2N8/P8	IN/OUT	USB_OC3_R_N	Y	RJ45+Rear USB2.0 W Smart pwr on	RJ45 USB port1
8	USB2N6/P6	IN/OUT		Y	RJ45+Rear USB2.0 W Smart pwr on	RJ45 USB port2
9	USB2N9/P9	IN/OUT	USB_OC4_R_N	Y	Front USB2.0 W/O CHRGER	USB2F1 port1
10	USB2N10/P10	IN/OUT	USB_OC6_R_N	Y	Front USB2.0 W CHRGER	USB2F1 port2
11	USB2N11/P11	IN/OUT	N/A	N	N/A	N/A
12	USB2N12/P12	IN/OUT	USB_OC5_R_N	Y	CLINK/USB HEADER	CLINK1 port1
13	USB2N13/P13	IN/OUT		Y	CLINK/USB HEADER	CLINK1 port2
14	USB2N14/P14	IN/OUT	N/A	N	N/A	N/A

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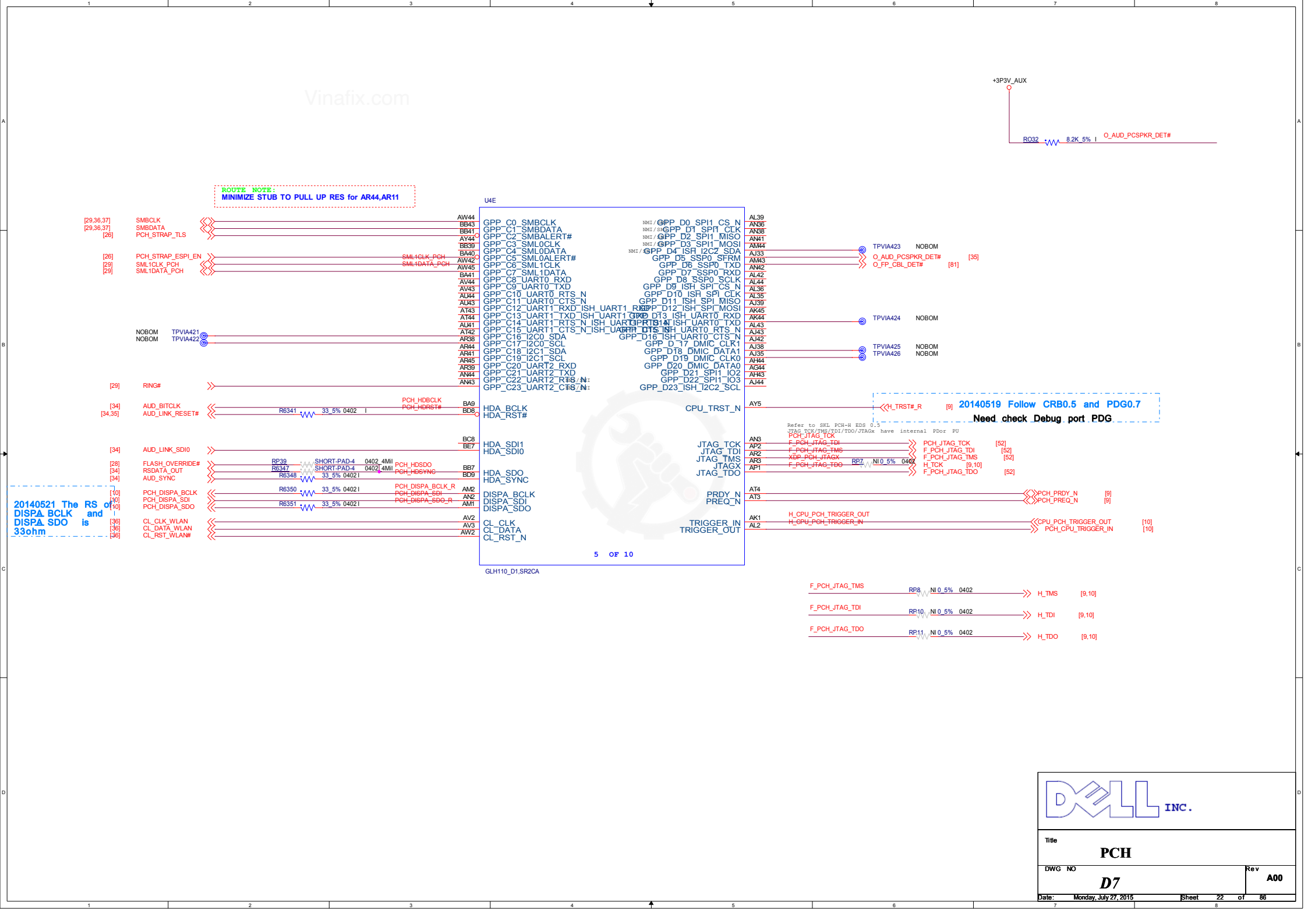
ROUTE NOTE:
MINIMIZE STUB TO PULL UP RES for AR44,AR11
U4E
GPP_C0_SMBCLK
GPP_C1_SMBDATA
GPP_C2_SMBALERT#
GPP_C3_SML0CLK
GPP_C4_SML0DATA
GPP_C5_SML0ALERT#
GPP_C6_SML1CLK
GPP_C7_SML1DATA
GPP_C8_UART0_RXD
GPP_C9_UART0_TXD
GPP_C10_UART0_RTS_N
GPP_C11_UART0_CTS_N
GPP_C12_UART1_RXD_ISH_UART1_RXD
GPP_C13_UART1_TXD_ISH_UART1_TXD
GPP_C14_UART1_RTS_N_ISH_UART1_RTS_N
GPP_C15_UART1_CTS_N_ISH_UART1_CTS_N
GPP_C16_I2C0_SDA
GPP_C17_I2C0_SCL
GPP_C18_I2C1_SDA
GPP_C19_I2C1_SCL
GPP_C20_UART2_RXD
GPP_C21_UART2_TXD
GPP_C22_UART2_RTS_N
GPP_C23_UART2_CTS_N
GPP_D0_SPI1_CS_N
GPP_D1_SPI1_CLK
GPP_D2_SPI1_MISO
GPP_D3_SPI1_MOSI
GPP_D4_ISH_I2C2_SDA
GPP_D5_SSP0_SFRM
GPP_D6_SSP0_TXD
GPP_D7_SSP0_RXD
GPP_D8_SSP0_SCLK
GPP_D9_ISH_SPI_CS_N
GPP_D10_ISH_SPI_CLK
GPP_D11_ISH_SPI_MISO
GPP_D12_ISH_SPI_MOSI
GPP_D13_ISH_UART0_RXD
GPP_D14_ISH_UART0_TXD
GPP_D15_ISH_UART0_RTS_N
GPP_D16_ISH_UART0_CTS_N
GPP_D_17_DMIC_CLK1
GPP_D18_DMIC_DATA1
GPP_D19_DMIC_CLK0
GPP_D20_DMIC_DATA0
GPP_D21_SPI1_IO2
GPP_D22_SPI1_IO3
GPP_D23_ISH_I2C2_SCL
HDA_BCLK
HDA_RST#
HDA_SDI1
HDA_SDI0
HDA_SDO
HDA_SYNC
DISPA_BCLK
DISPA_SDI
DISPA_SDO
CL_CLK
CL_DATA
CL_RST_N
CPU_TRST_N
JTAG_TCK
JTAG_TDI
JTAG_TMS
JTAGX
JTAG_TDO
PRDY_N
PREQ_N
TRIGGER_IN
TRIGGER_OUT
5 OF 10
GLH110_D1,SR2CA
+3P3V_AUX
RQ32 8.2K_5% I O_AUD_PCSPKR_DET#
TPVIA423 NOBOM
O_AUD_PCSPKR_DET# [35]
O_FP_CBL_DET# [81]
TPVIA424 NOBOM
TPVIA425 NOBOM
TPVIA426 NOBOM
H_TRST#_R [9]
20140519 Follow CRB0.5 and PDG0.7
Need check Debug port PDG
Refer to SKL PCH-H EDS 0.5
JTAG TCK/TMS/TDI/TDO/JTAGx have internal PDor PU
PCH_JTAG_TCK
F_PCH_JTAG_TDI
F_PCH_JTAG_TMS
XDP_PCH_JTAGX
F_PCH_JTAG_TDO
RP7 NI 0_5% 0402
PCH_JTAG_TCK [52]
F_PCH_JTAG_TDI [52]
F_PCH_JTAG_TMS [52]
H_TCK [9,10]
F_PCH_JTAG_TDO [52]
PCH_PRDY_N [9]
PCH_PREQ_N [9]
H_CPU_PCH_TRIGGER_OUT
H_CPU_PCH_TRIGGER_IN
CPU_PCH_TRIGGER_OUT [10]
PCH_CPU_TRIGGER_IN [10]
F_PCH_JTAG_TMS RP8 NI 0_5% 0402 H_TMS [9,10]
F_PCH_JTAG_TDI RP10 NI 0_5% 0402 H_TDI [9,10]
F_PCH_JTAG_TDO RP11 NI 0_5% 0402 H_TDO [9,10]
[29,36,37] SMBCLK
[29,36,37] SMBDATA
[26] PCH_STRAP_TLS
[26] PCH_STRAP_ESPI_EN
[29] SML1CLK_PCH
[29] SML1DATA_PCH
SML1CLK_PCH
SML1DATA_PCH
NOBOM TPVIA421
NOBOM TPVIA422
[29] RING#
[34] AUD_BITCLK
[34,35] AUD_LINK_RESET#
R6341 33_5% 0402 I
PCH_HDBCLK
PCH_HDRST#
[34] AUD_LINK_SDI0
[28] FLASH_OVERRIDE#
[34] RSDATA_OUT
[34] AUD_SYNC
RP39 SHORT-PAD-4 0402_4Mil
R6347 SHORT-PAD-4 0402_4Mil
R6348 33_5% 0402 I
PCH_HDSDO
PCH_HDSYNC
[10] PCH_DISPA_BCLK
[10] PCH_DISPA_SDI
[10] PCH_DISPA_SDO
R6350 33_5% 0402 I
R6351 33_5% 0402 I
PCH_DISPA_BCLK_R
PCH_DISPA_SDI
PCH_DISPA_SDO_R
[36] CL_CLK_WLAN
[36] CL_DATA_WLAN
[36] CL_RST_WLAN#
20140521 The RS of DISPA BCLK and DISPA SDO is 33ohm
DELL INC.
Title
PCH
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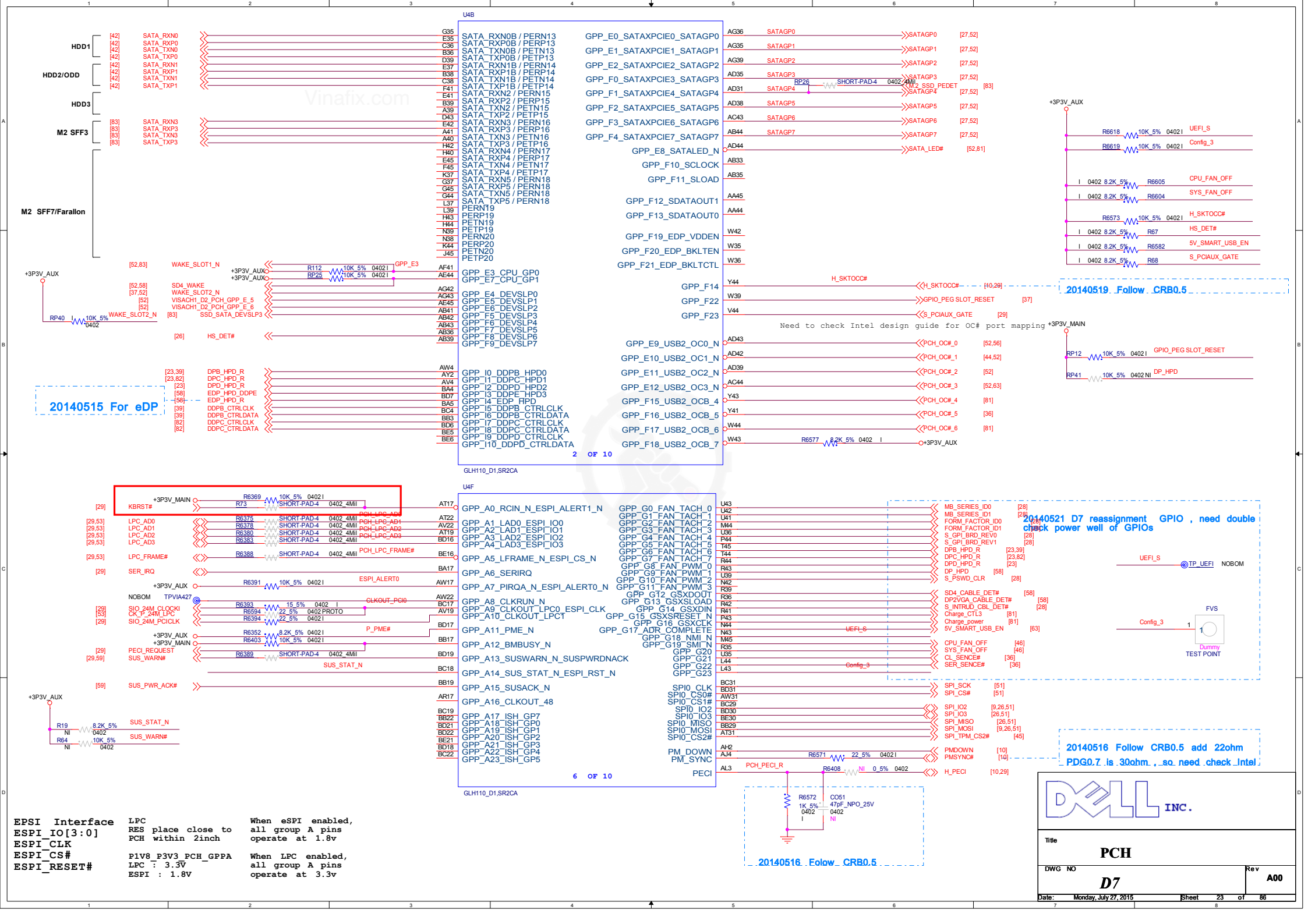
U4B
HDD1
HDD2/ODD
HDD3
M2 SFF3
M2 SFF7/Farallon
SATA_RXN0B / PERN13
SATA_RXP0B / PERP13
SATA_TXN0B / PETN13
SATA_TXP0B / PETP13
SATA_RXN1B / PERN14
SATA_RXP1B / PERP14
SATA_TXN1B / PETN14
SATA_TXP1B / PETP14
SATA_RXN2 / PERN15
SATA_RXP2 / PERP15
SATA_TXN2 / PETN15
SATA_TXP2 / PETP15
SATA_RXN3 / PERN16
SATA_RXP3 / PERP16
SATA_TXN3 / PETN16
SATA_TXP3 / PETP16
SATA_RXN4 / PERN17
SATA_RXP4 / PERP17
SATA_TXN4 / PETN17
SATA_TXP4 / PETP17
SATA_RXN5 / PERN18
SATA_RXP5 / PERN18
SATA_TXN5 / PERN18
SATA_TXP5 / PERN18
PERN19
PERP19
PETN19
PETP19
PERN20
PERP20
PETN20
PETP20
GPP_E0_SATAXPCIE0_SATAGP0
GPP_E1_SATAXPCIE1_SATAGP1
GPP_E2_SATAXPCIE2_SATAGP2
GPP_F0_SATAXPCIE3_SATAGP3
GPP_F1_SATAXPCIE4_SATAGP4
GPP_F2_SATAXPCIE5_SATAGP5
GPP_F3_SATAXPCIE6_SATAGP6
GPP_F4_SATAXPCIE7_SATAGP7
GPP_E8_SATALED_N
GPP_F10_SCLOCK
GPP_F11_SLOAD
GPP_F12_SDATAOUT1
GPP_F13_SDATAOUT0
GPP_F19_EDP_VDDEN
GPP_F20_EDP_BKLTEN
GPP_F21_EDP_BKLTCTL
GPP_E3_CPU_GP0
GPP_E7_CPU_GP1
GPP_E4_DEVSLP0
GPP_E5_DEVSLP1
GPP_E6_DEVSLP2
GPP_F5_DEVSLP3
GPP_F6_DEVSLP4
GPP_F7_DEVSLP5
GPP_F8_DEVSLP6
GPP_F9_DEVSLP7
GPP_I0_DDPB_HPD0
GPP_I1_DDPC_HPD1
GPP_I2_DDPD_HPD2
GPP_I3_DDPE_HPD3
GPP_I4_EDP_HPD
GPP_I5_DDPB_CTRLCLK
GPP_I6_DDPB_CTRLDATA
GPP_I7_DDPC_CTRLCLK
GPP_I8_DDPC_CTRLDATA
GPP_I9_DDPD_CTRLCLK
GPP_I10_DDPD_CTRLDATA
GPP_F14
GPP_F22
GPP_F23
GPP_E9_USB2_OC0_N
GPP_E10_USB2_OC1_N
GPP_E11_USB2_OC2_N
GPP_E12_USB2_OC3_N
GPP_F15_USB2_OCB_4
GPP_F16_USB2_OCB_5
GPP_F17_USB2_OCB_6
GPP_F18_USB2_OCB_7
2 OF 10
GLH110_D1,SR2CA
SATAGP0
SATAGP1
SATAGP2
SATAGP3
SATAGP4
SATAGP5
SATAGP6
SATAGP7
SATA_LED#
M.2_SSD_PEDET
SHORT-PAD-4
H_SKTOCC#
GPIO_PEG SLOT_RESET
S_PCIAUX_GATE
Need to check Intel design guide for OC# port mapping
PCH_OC#_0
PCH_OC#_1
PCH_OC#_2
PCH_OC#_3
PCH_OC#_4
PCH_OC#_5
PCH_OC#_6
+3V_AUX
+3V_MAIN
UEFI_S
Config_3
CPU_FAN_OFF
SYS_FAN_OFF
H_SKTOCC#
HS_DET#
5V_SMART_USB_EN
S_PCIAUX_GATE
DP_HPD
20140519 Follow CRB0.5
20140515 For eDP
WAKE_SLOT1_N
WAKE_SLOT2_N
SD4_WAKE
VISACH1_D2_PCH_GPP_E_5
VISACH1_D2_PCH_GPP_E_6
SSD_SATA_DEVSLP3
HS_DET#
DPB_HPD_R
DPC_HPD_R
DPD_HPD_R
EDP_HPD_DDPE
EDP_HPD_R
DDPB_CTRLCLK
DDPB_CTRLDATA
DDPC_CTRLCLK
DDPC_CTRLDATA
U4F
GPP_A0_RCIN_N_ESPI_ALERT1_N
GPP_A1_LAD0_ESPI_IO0
GPP_A2_LAD1_ESPI_IO1
GPP_A3_LAD2_ESPI_IO2
GPP_A4_LAD3_ESPI_IO3
GPP_A5_LFRAME_N_ESPI_CS_N
GPP_A6_SERIRQ
GPP_A7_PIRQA_N_ESPI_ALERT0_N
GPP_A8_CLKRUN_N
GPP_A9_CLKOUT_LPC0_ESPI_CLK
GPP_A10_CLKOUT_LPCT
GPP_A11_PME_N
GPP_A12_BMBUSY_N
GPP_A13_SUSWARN_N_SUSPWRDNACK
GPP_A14_SUS_STAT_N_ESPI_RST_N
GPP_A15_SUSACK_N
GPP_A16_CLKOUT_48
GPP_A17_ISH_GP7
GPP_A18_ISH_GP0
GPP_A19_ISH_GP1
GPP_A20_ISH_GP2
GPP_A21_ISH_GP3
GPP_A22_ISH_GP4
GPP_A23_ISH_GP5
GPP_G0_FAN_TACH_0
GPP_G1_FAN_TACH_1
GPP_G2_FAN_TACH_2
GPP_G3_FAN_TACH_3
GPP_G4_FAN_TACH_4
GPP_G5_FAN_TACH_5
GPP_G6_FAN_TACH_6
GPP_G7_FAN_TACH_7
GPP_G8_FAN_PWM_0
GPP_G9_FAN_PWM_1
GPP_G10_FAN_PWM_2
GPP_G11_FAN_PWM_3
GPP_G12_GSXDOUT
GPP_G13_GSXSLOAD
GPP_G14_GSXDIN
GPP_G15_GSXSRESET_N
GPP_G16_GSXCLK
GPP_G17_ADR_COMPLETE
GPP_G18_NMI_N
GPP_G19_SMI_N
GPP_G20
GPP_G21
GPP_G22
GPP_G23
SPI0_CLK
SPI0_CS0#
SPI0_CS1#
SPI0_IO2
SPI0_IO3
SPI0_MISO
SPI0_MOSI
SPI0_CS2#
PM_DOWN
PM_SYNC
PECI
6 OF 10
GLH110_D1,SR2CA
KBRST#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
SER_IRQ
TPVIA427
SIO_24M_CLOCKI
CK_P_24M_LPC
SIO_24M_PCICLK
PECI_REQUEST
SUS_WARN#
SUS_PWR_ACK#
SUS_STAT_N
PCH_LPC_AD0
PCH_LPC_AD1
PCH_LPC_AD2
PCH_LPC_AD3
PCH_LPC_FRAME#
ESPI_ALERT0
CLKOUT_PCI0
P_PME#
SPI_SCK
SPI_CS#
SPI_IO2
SPI_IO3
SPI_MISO
SPI_MOSI
SPI_TPM_CS2#
PMDOWN
PMSYNC#
H_PECI
PCH_PECI_R
MB_SERIES_ID0
MB_SERIES_ID1
FORM_FACTOR_ID0
FORM_FACTOR_ID1
S_GPI_BRD_REV0
S_GPI_BRD_REV1
DPB_HPD_R
DPC_HPD_R
DPD_HPD_R
DP_HPD
S_PSWD_CLR
SD4_CABLE_DET#
DP2VGA_CABLE_DET#
S_INTRUD_CBL_DET#
Charge_CTL3
Charge_power
5V_SMART_USB_EN
CPU_FAN_OFF
SYS_FAN_OFF
CL_SENCE#
SER_SENCE#
20140521 D7 reassignment GPIO , need double check power well of GPIOs
TP_UEFI
NOBOM
FVS
Dummy
TEST POINT
20140516 Follow CRB0.5 add 22ohm
PDG0.7 is 30ohm , so need check Intel
20140516 Follow CRB0.5
EPSI Interface
ESPI_IO[3:0]
ESPI_CLK
ESPI_CS#
ESPI_RESET#
LPC
RES place close to
PCH within 2inch
P1V8_P3V3_PCH_GPPA
LPC : 3.3V
ESPI : 1.8V
When eSPI enabled,
all group A pins
operate at 1.8v
When LPC enabled,
all group A pins
operate at 3.3v
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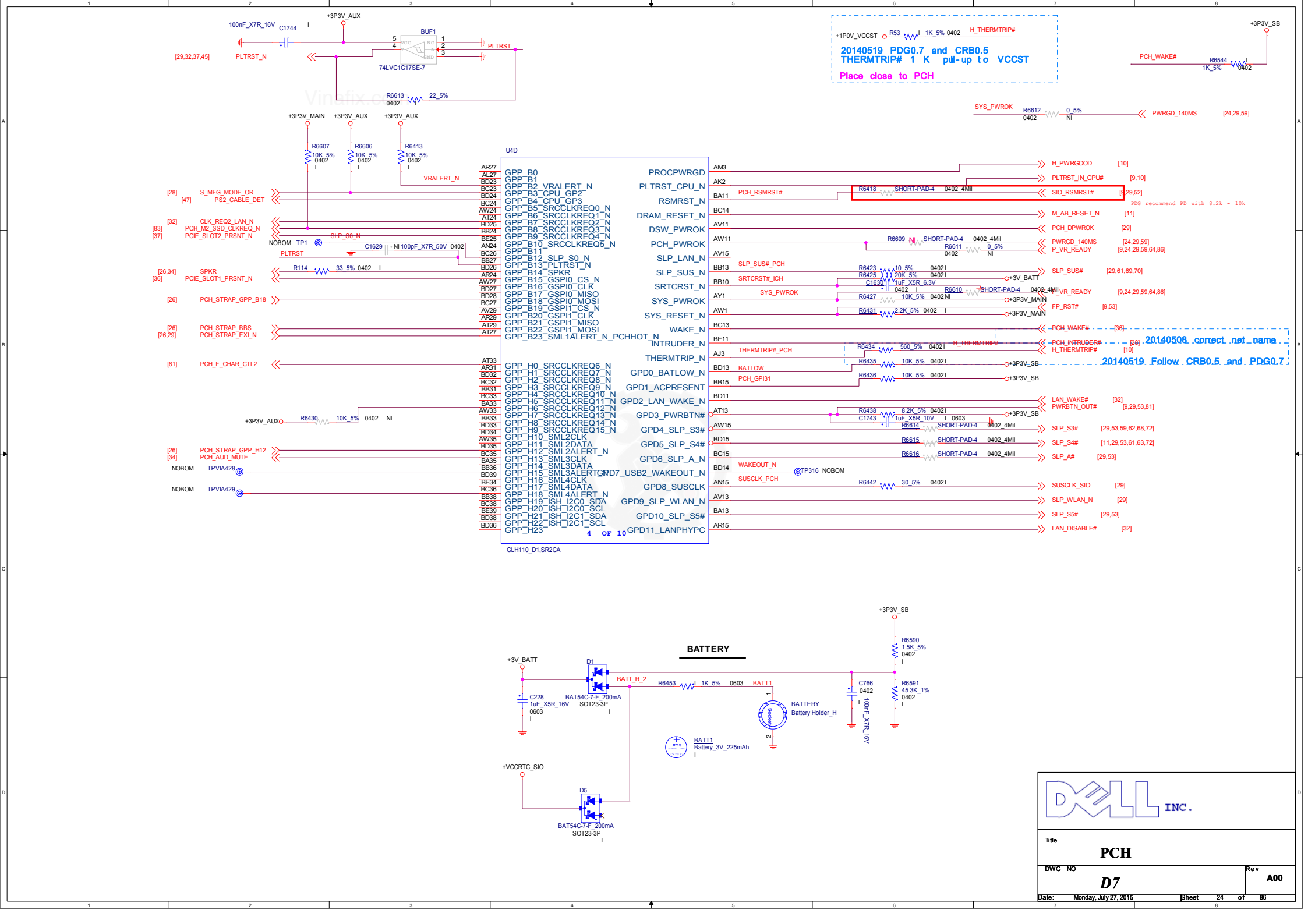
20140519 PDG0.7 and CRB0.5
THERMTRIP# 1 K pull-up to VCCST
Place close to PCH
20140508 correct net name
20140519 Follow CRB0.5 and PDG0.7
BATTERY
U4D
GLH110_D1,SR2CA
4 OF 10
PCH
DWG NO
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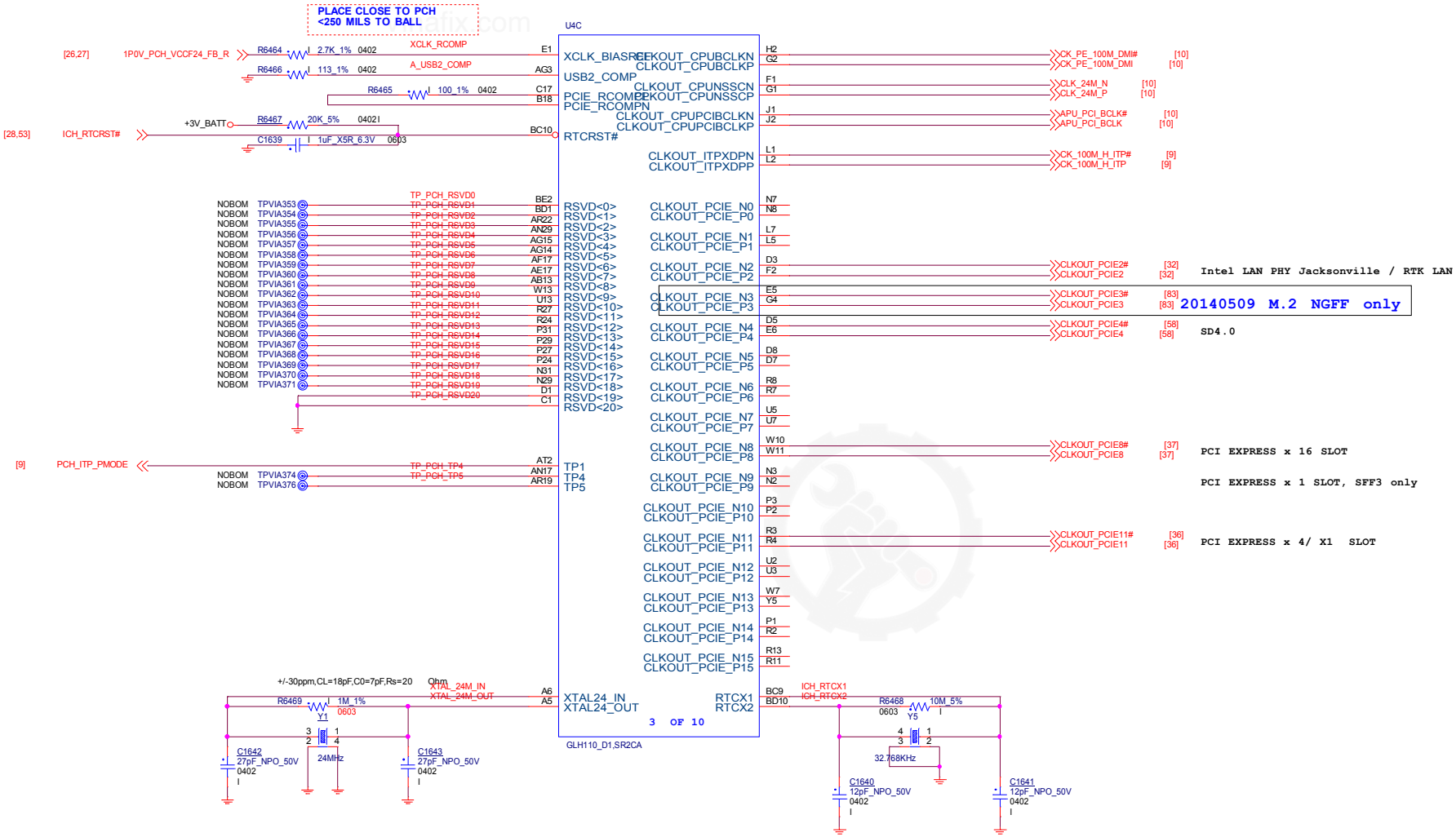
PCH - CLOCK DISTRIBUTION



DELL INC.

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DWG NO: D7

Rev: A00

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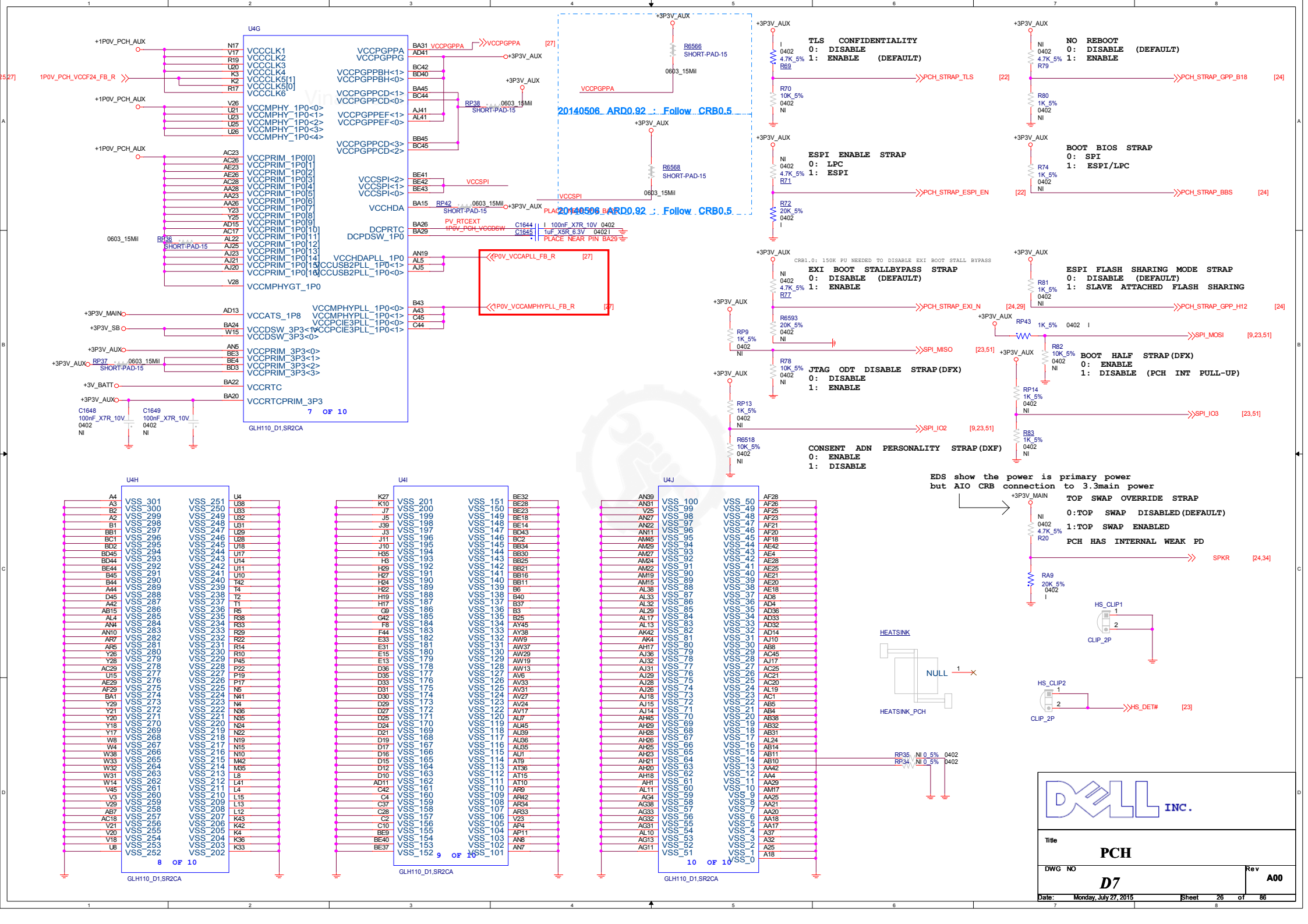
U4G
VCCCLK1
VCCCLK2
VCCCLK3
VCCCLK4
VCCCLK5[1]
VCCCLK5[0]
VCCCLK6
VCCMPHY_1P0<0>
VCCMPHY_1P0<1>
VCCMPHY_1P0<2>
VCCMPHY_1P0<3>
VCCMPHY_1P0<4>
VCCPRIM_1P0[0]
VCCPRIM_1P0[1]
VCCPRIM_1P0[2]
VCCPRIM_1P0[3]
VCCPRIM_1P0[4]
VCCPRIM_1P0[5]
VCCPRIM_1P0[6]
VCCPRIM_1P0[7]
VCCPRIM_1P0[8]
VCCPRIM_1P0[9]
VCCPRIM_1P0[10]
VCCPRIM_1P0[11]
VCCPRIM_1P0[12]
VCCPRIM_1P0[13]
VCCPRIM_1P0[14]
VCCPRIM_1P0[15]
VCCPRIM_1P0[16]
VCCMPHYGT_1P0
VCCATS_1P8
VCCDSW_3P3<1>
VCCDSW_3P3<0>
VCCPRIM_3P3<0>
VCCPRIM_3P3<1>
VCCPRIM_3P3<2>
VCCPRIM_3P3<3>
VCCRTC
VCCRTCPRIM_3P3
7 OF 10
GLH110_D1,SR2CA
VCCPGPPA
VCCPGPPG
VCCPGPPBH<1>
VCCPGPPBH<0>
VCCPGPPCD<1>
VCCPGPPCD<0>
VCCPGPPEF<1>
VCCPGPPEF<0>
VCCPGPPCD<3>
VCCPGPPCD<2>
VCCSPI<2>
VCCSPI<1>
VCCSPI<0>
VCCHDA
DCPRTC
DCPDSW_1P0
VCCHDAPLL_1P0
VCCUSB2PLL_1P0<1>
VCCUSB2PLL_1P0<0>
VCCMPHYPLL_1P0<0>
VCCMPHYPLL_1P0<1>
VCCPCIE3PLL_1P0<0>
VCCPCIE3PLL_1P0<1>
+1P0V_PCH_AUX
+3P3V_MAIN
+3P3V_SB
+3P3V_AUX
+3V_BATT
1P0V_PCH_VCCF24_FB_R
VCCSPI
PV_RTCEXT
1P0V_PCH_VCCDSW
1P0V_VCCAPLL_FB_R
1P0V_VCCAMPHYPLL_FB_R
RP36
RP37
RP38
RP42
SHORT-PAD-15
0603_15Mil
C1644
C1645
100nF_X7R_10V
1uF_X5R_6.3V
PLACE_NEAR_PIN_BA29
C1648
C1649
20140506_ARD0.92_:_Follow_CRB0.5
R6566
R6568
U4H
VSS_301
VSS_300
VSS_299
VSS_298
VSS_297
VSS_296
VSS_295
VSS_294
VSS_293
VSS_292
VSS_291
VSS_290
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VSS_210
VSS_209
VSS_208
VSS_207
VSS_206
VSS_205
VSS_204
VSS_203
VSS_202
8 OF 10
GLH110_D1,SR2CA
U4I
VSS_201
VSS_200
VSS_199
VSS_198
VSS_197
VSS_196
VSS_195
VSS_194
VSS_193
VSS_192
VSS_191
VSS_190
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VSS_144
VSS_143
VSS_142
VSS_141
VSS_140
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VSS_138
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VSS_135
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VSS_132
VSS_131
VSS_130
VSS_129
VSS_128
VSS_127
VSS_126
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VSS_108
VSS_107
VSS_106
VSS_105
VSS_104
VSS_103
VSS_102
VSS_101
9 OF 10
GLH110_D1,SR2CA
U4J
VSS_100
VSS_99
VSS_98
VSS_97
VSS_96
VSS_95
VSS_94
VSS_93
VSS_92
VSS_91
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VSS_15
VSS_14
VSS_13
VSS_12
VSS_11
VSS_10
VSS_9
VSS_8
VSS_7
VSS_6
VSS_5
VSS_4
VSS_3
VSS_2
VSS_1
VSS_0
10 OF 10
GLH110_D1,SR2CA
RP35
RP34
TLS CONFIDENTIALITY
0: DISABLE
1: ENABLE (DEFAULT)
PCH_STRAP_TLS
NO REBOOT
0: DISABLE (DEFAULT)
1: ENABLE
PCH_STRAP_GPP_B18
ESPI ENABLE STRAP
0: LPC
1: ESPI
PCH_STRAP_ESPI_EN
BOOT BIOS STRAP
0: SPI
1: ESPI/LPC
PCH_STRAP_BBS
CRB1.0: 150K PU NEEDED TO DISABLE EXI BOOT STALL BYPASS
EXI BOOT STALLBYPASS STRAP
0: DISABLE (DEFAULT)
1: ENABLE
PCH_STRAP_EXI_N
ESPI FLASH SHARING MODE STRAP
0: DISABLE (DEFAULT)
1: SLAVE ATTACHED FLASH SHARING
PCH_STRAP_GPP_H12
SPI_MISO
SPI_MOSI
JTAG ODT DISABLE STRAP(DFX)
0: DISABLE
1: ENABLE
BOOT HALF STRAP(DFX)
0: ENABLE
1: DISABLE (PCH INT PULL-UP)
SPI_IO2
SPI_IO3
CONSENT ADN PERSONALITY STRAP(DXF)
0: ENABLE
1: DISABLE
EDS show the power is primary power
but AIO CRB connection to 3.3main power
TOP SWAP OVERRIDE STRAP
0:TOP SWAP DISABLED(DEFAULT)
1:TOP SWAP ENABLED
PCH HAS INTERNAL WEAK PD
SPKR
HEATSINK
HEATSINK_PCH
NULL
HS_CLIP1
HS_CLIP2
CLIP_2P
HS_DET#
DELL INC.
Title
PCH
DWG NO
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A00
Date: Monday, July 27, 2015
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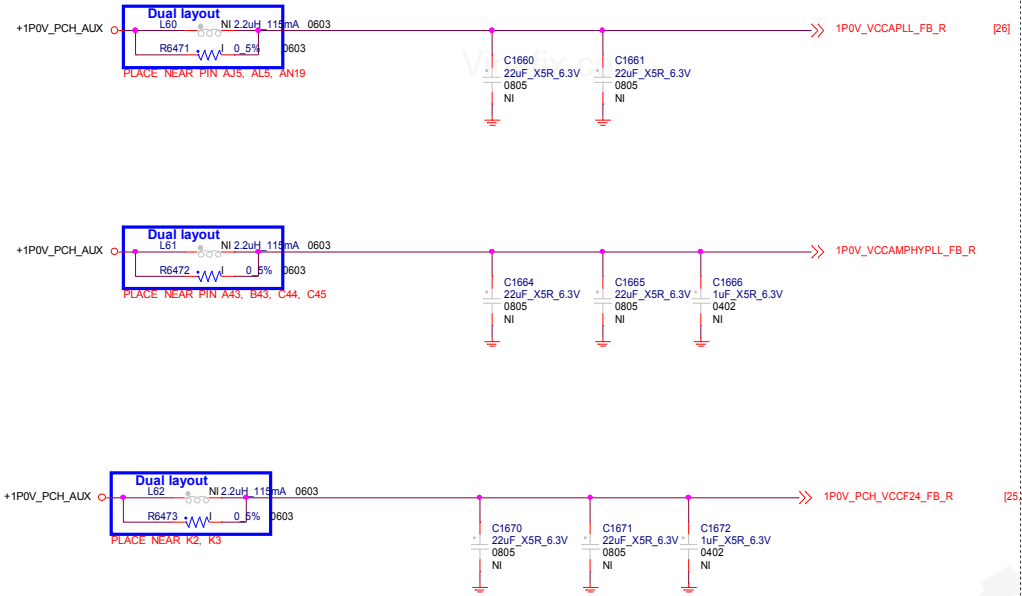
FILTER

SKYLAKE Decoupling & filter

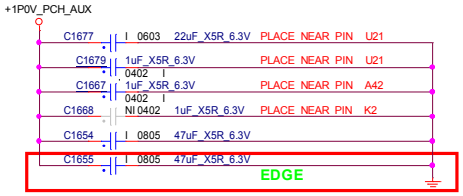


Power Plane Isolation

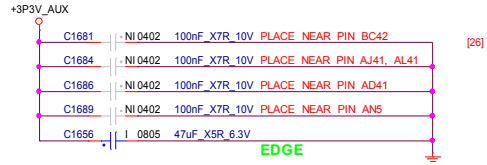
Need to update for SLK

Voltage	Interface	PCH Pins sharing power rail
VCC_PCH 1.05V	Core	U26, U25, U23, U21, V26,
	PCIe/SATA/ USB3	T19, T20, P22, P23, P25, P26, P28, P14, P16, P17
	GPIO/LPC	AC12
	FDI	M14
	DIFFCLK	U12, V14
		W14
		AB2
	SSC	T16, V16
		AA16, W16
	USB2	AF19, AF20, AF22, AF23, AP22
PCH 3.3V Standby	SUS	AM33, AN33
	USB2	AH18, AH20, AH22, AJ20, AK20
	AZALIA	AW26
	USB3	P20
	RTC	AP35
PCH 3.3V	CLK	AM7, AM9, AP5, AP7, AR4, AT5, AV4, AW4, AW9, AG12, AK11,
	HVCMOS	AG1
	PCIe	AV3, AW3
	Core	U30, W30
	Fuse	AF26

V1.0A



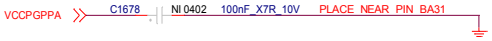
V1.8A / V3.3A



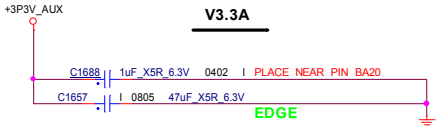
V1.8A / V1.8S / V3.3S

V3.3 DSW

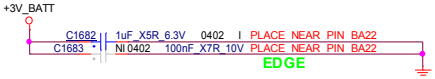
VccPGPPA

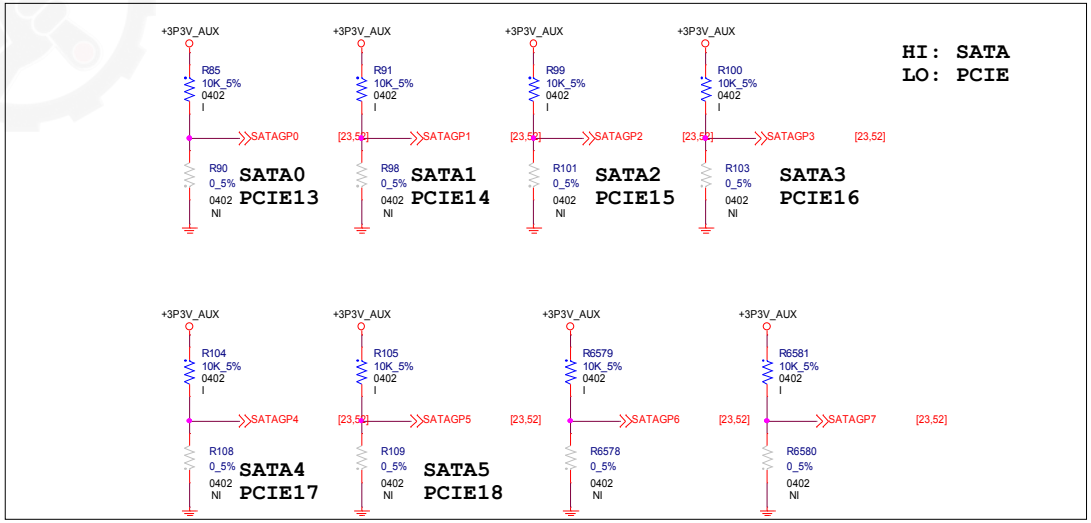


V3.3A



VCCRTC





DELL INC.

Title: PCH

DWG NO: D7

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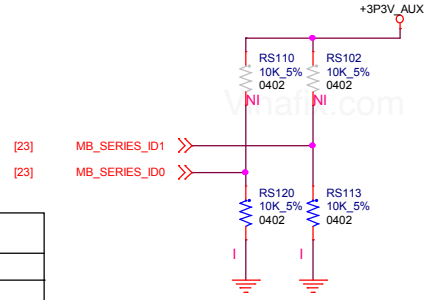
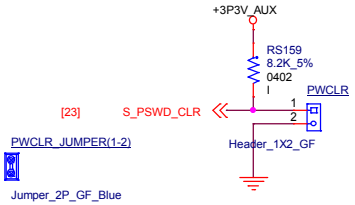
MB series ID



ID1	ID0	Type
0	0	SFF3
0	1	SFF5
1	0	SFF7
1	1	Farallon

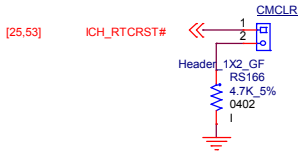
Clear Password

PASSWORD	SHORT : DEFAULT
	OPEN : CLEAR PASSWORD

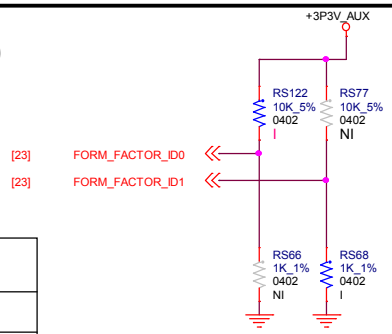


CLR_CMOS

CMOS	SHORT : CLEAR CMOS
	OPEN : DEFAULT

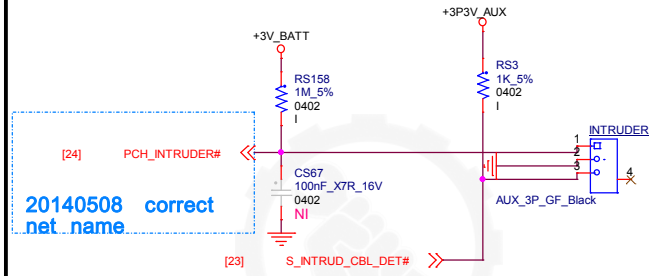


Form Factor ID

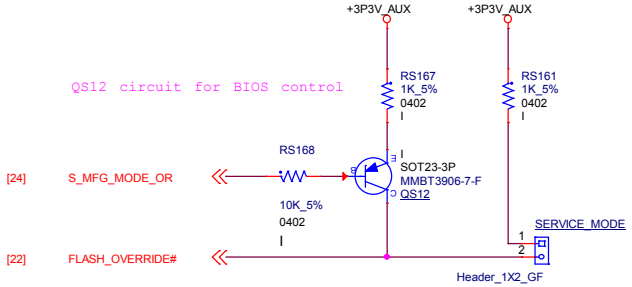


ID1	ID0	Type
1	1	MT
1	0	CT
0	1	SFF
0	0	Micro

Chassis Intruder

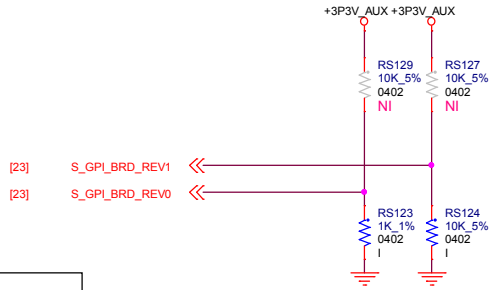


ME Disable (Flash overide)



SERVICE_MODE	SHORT : ME DISABLE
	OPEN : DEFAULT

BOARD ID



ID1	ID0	Type
1	1	X02
1	0	X01
0	1	X00
0	0	B00/A00

BEEP

DELL INC.

Title: PCH

DWG NO: D7

Rev: A00

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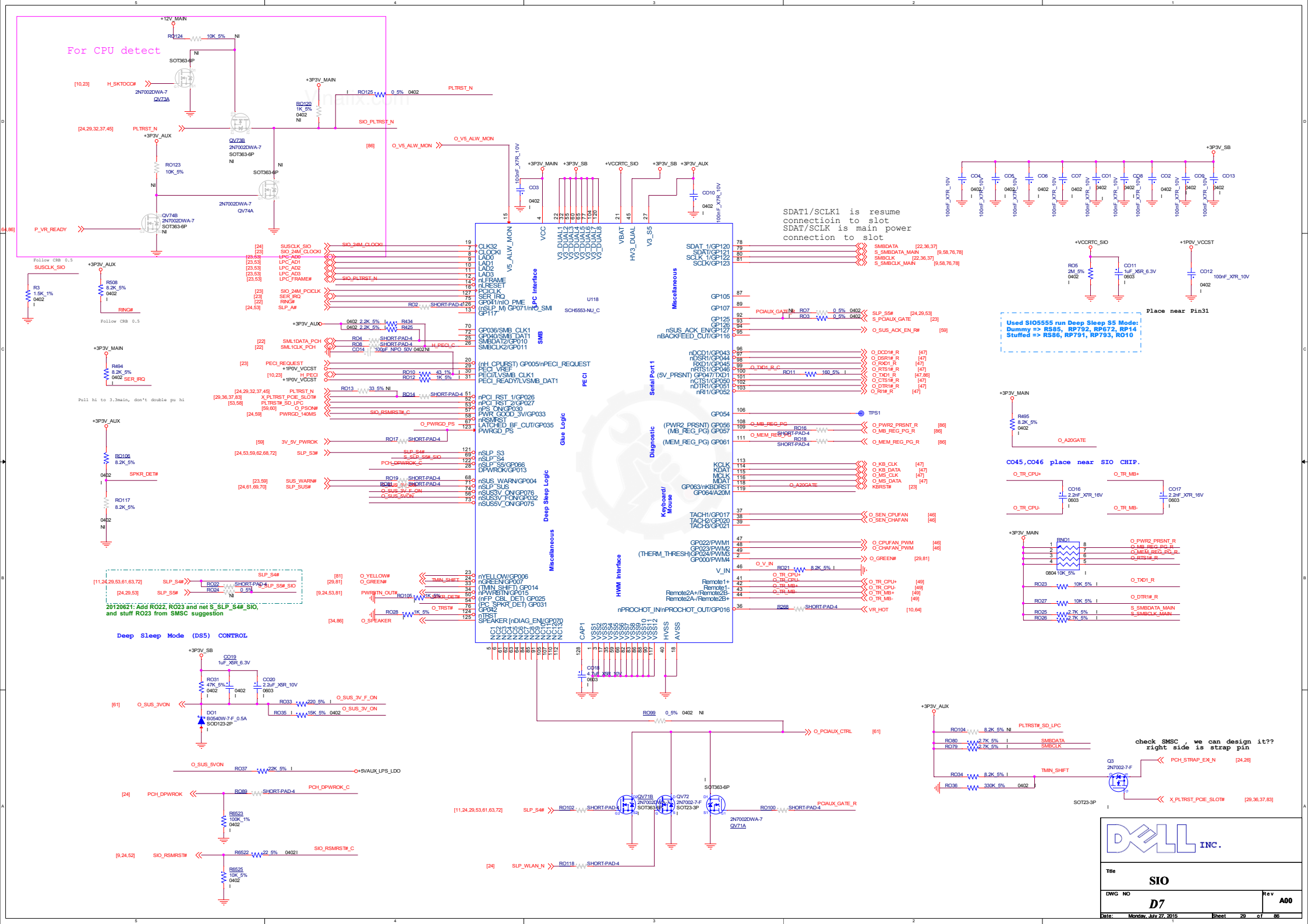
For CPU detect
SDAT1/SCLK1 is resume connectioin to slot
SDAT/SCLK is main power connection to slot
Used SIO5555 run Deep Sleep S5 Mode:
Dummy => RS85, RP792, RP672, RP14
Stuffed => RS86, RP791, RP793, RO10
Place near Pin31
C045,C046 place near SIO CHIP.
Deep Sleep Mode (DS5) CONTROL
20120621: Add RO22, RO23 and net S_SLP_S4#_SIO, and stuff RO23 from SMSC suggestion
check SMSC , we can design it?? right side is strap pin
SIO
D7
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Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title

CPU

DWG NO	Rev
D7	A00

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Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title: **CPU**

DWG NO: ***D7***

Rev: **A00**

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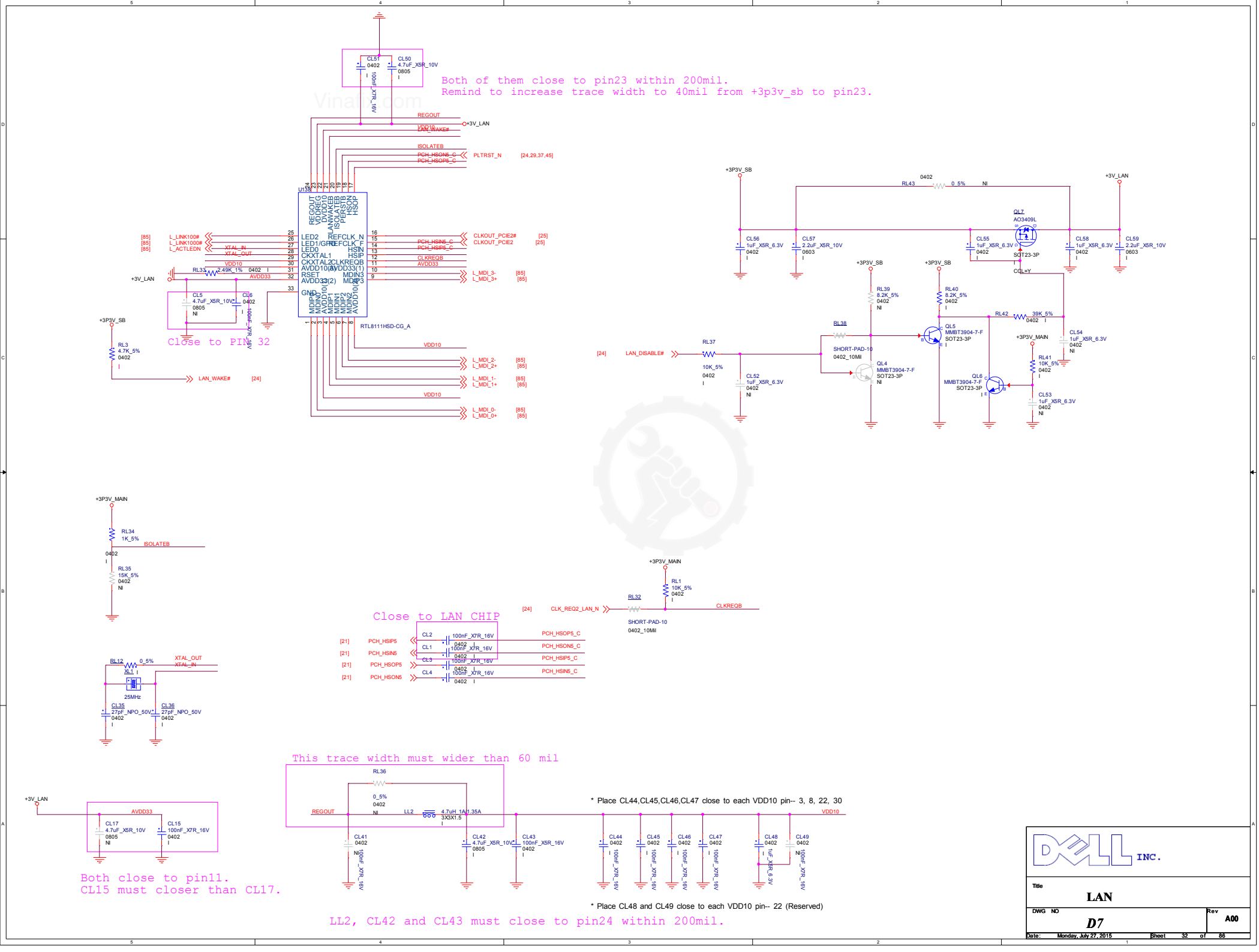
Both of them close to pin23 within 200mil.
Remind to increase trace width to 40mil from +3p3v_sb to pin23.
Close to PIN 32
Close to LAN CHIP
This trace width must wider than 60 mil
Both close to pin11.
CL15 must closer than CL17.
* Place CL44,CL45,CL46,CL47 close to each VDD10 pin-- 3, 8, 22, 30
* Place CL48 and CL49 close to each VDD10 pin-- 22 (Reserved)
LL2, CL42 and CL43 must close to pin24 within 200mil.
RTL8111HSD-CG_A
Title
LAN
DWG NO
D7
Rev
A00
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Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title

CPU

DWG NO

D7

Rev

A00

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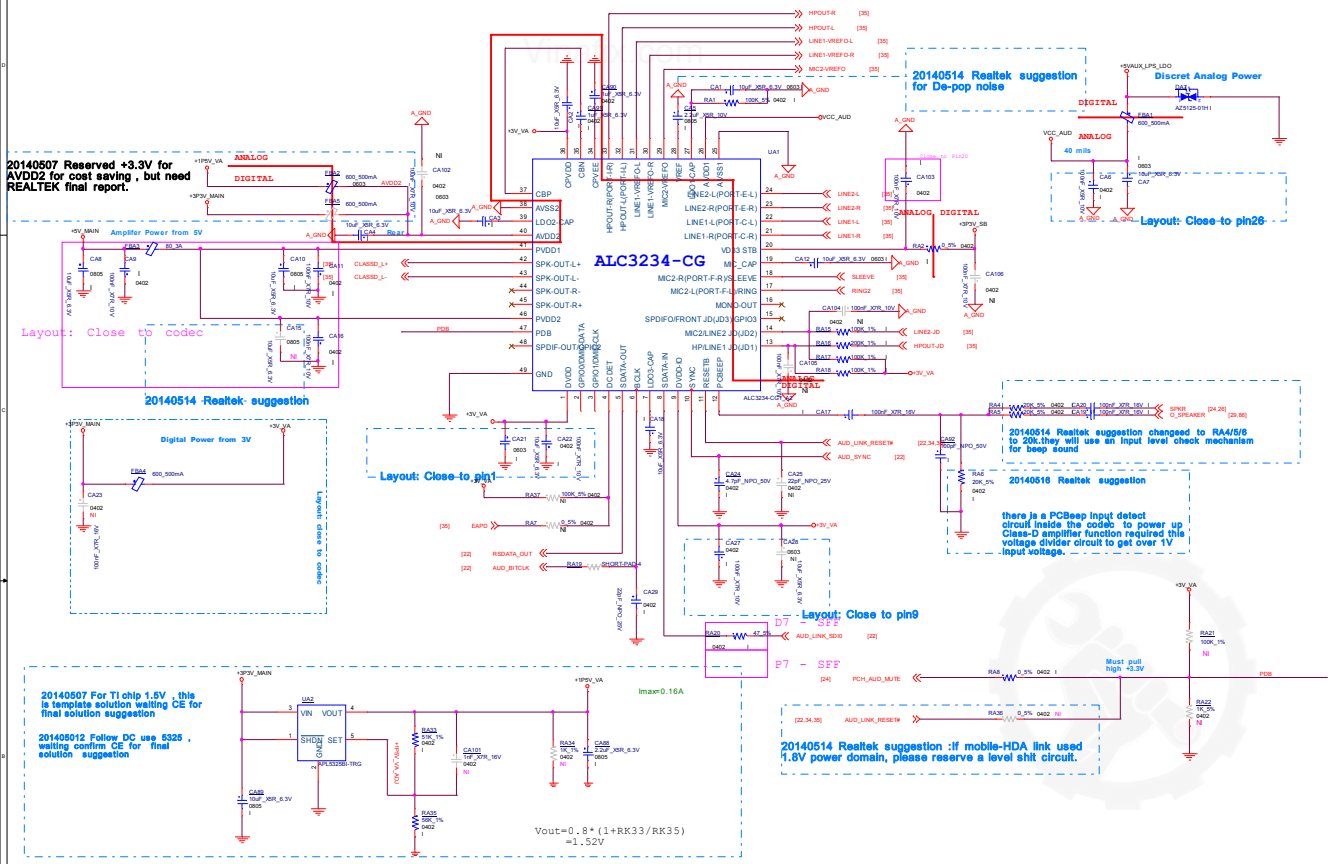

DELL INC.

Title: AUDIO

DWG NO: D7

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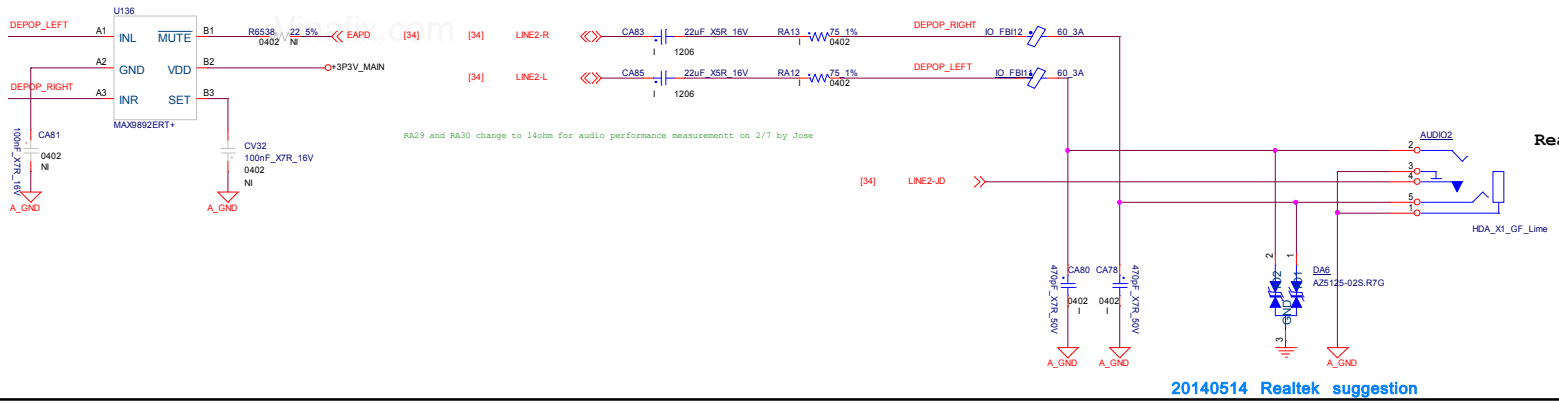
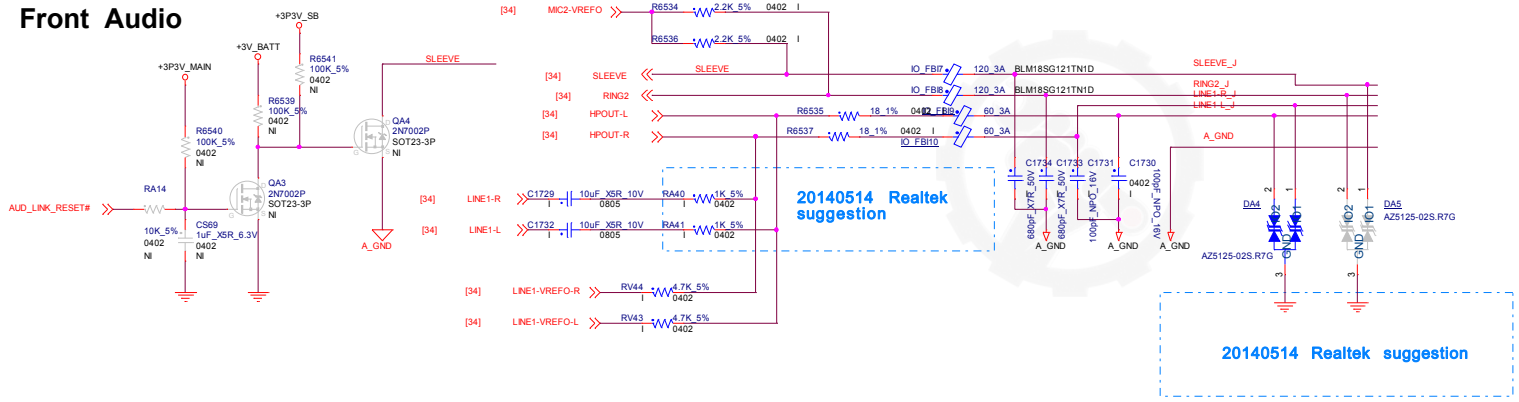
Rear Audio Jack



Rear Audio

20140514 Realtek suggestion

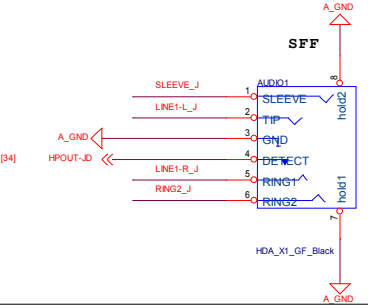
Front Audio



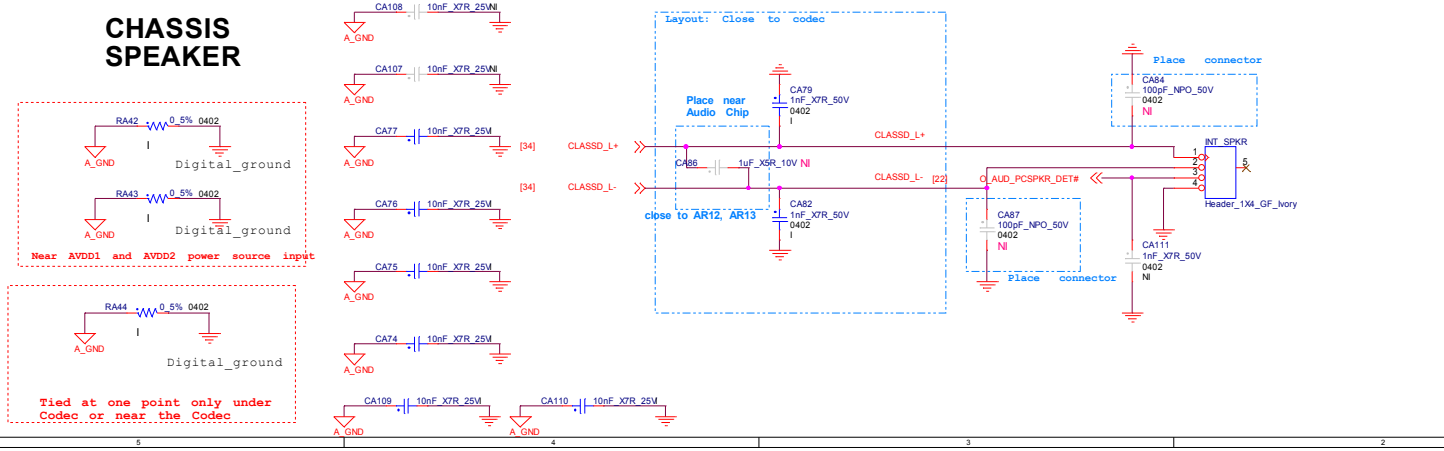
20140514 Realtek suggestion

20140514 Realtek suggestion

Front Panel



CHASSIS SPEAKER



DELL INC.

Title: AUDIO

DWG NO: D7

Rev: A00

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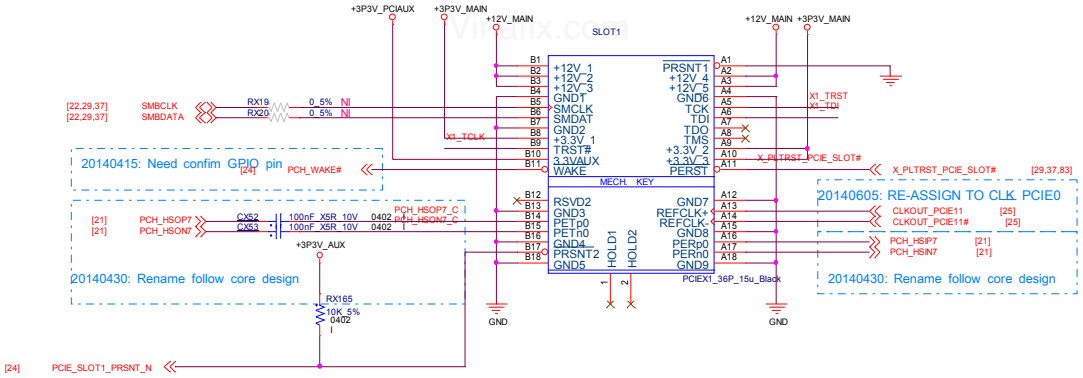
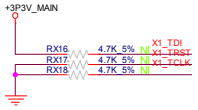
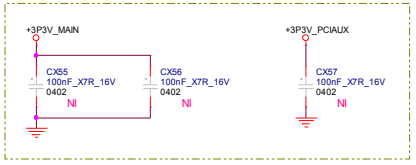
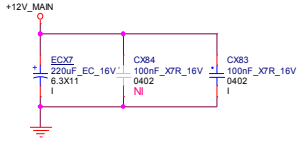




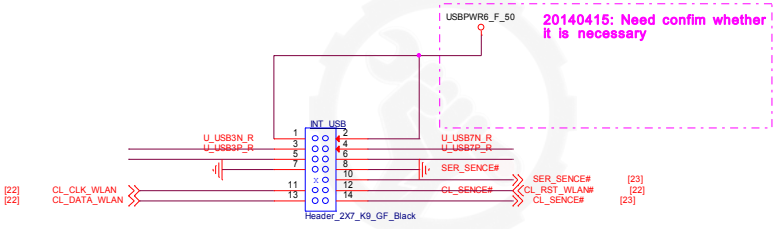


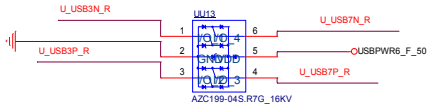


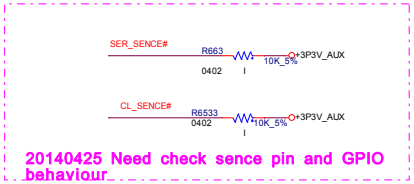
ARD 0.9 :Header populated on 7/9 series only
Provides vPro and BT support from Intel wireless Add-in-Card
USB and CLINK signals passed on cable from motherboard to Add-in-Card
Compatible with standard USB 2.0 headers and cables

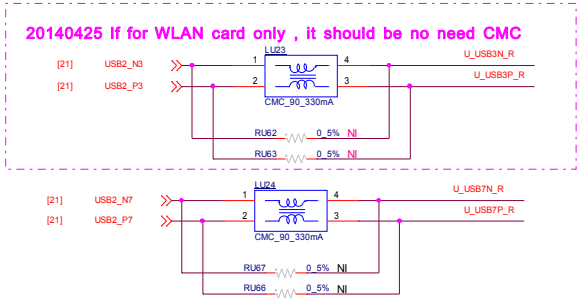
14 pin non shrouded header 0.1 pin spacing,
Pin 14 allows sense of the CLINK/BT cable ,
Add-in-Card does not use +5V_USB or USB2* (second port) signals

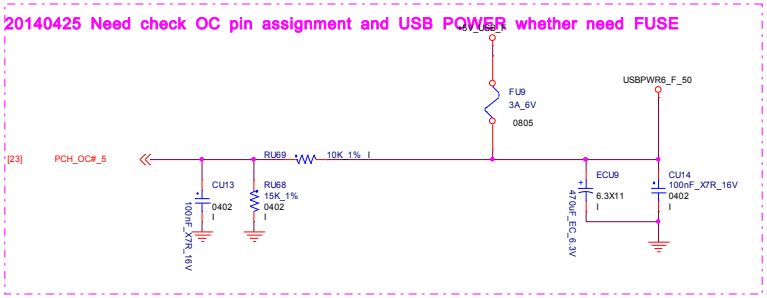
14 pin USB/CLINK Header			
+ 5V_USB	1	2	+ 5V_USB
USB1N	3	4	USB2N
USB1P	5	6	USB2P
GND	7	8	GND
Key (no pin)	9	10	SER_SENSE
CLINK_CLK	11	12	CLINK_RST
CLINK_DAT	13	14	CL_SENSE











DELL INC.

Title: **PCIe 1x**

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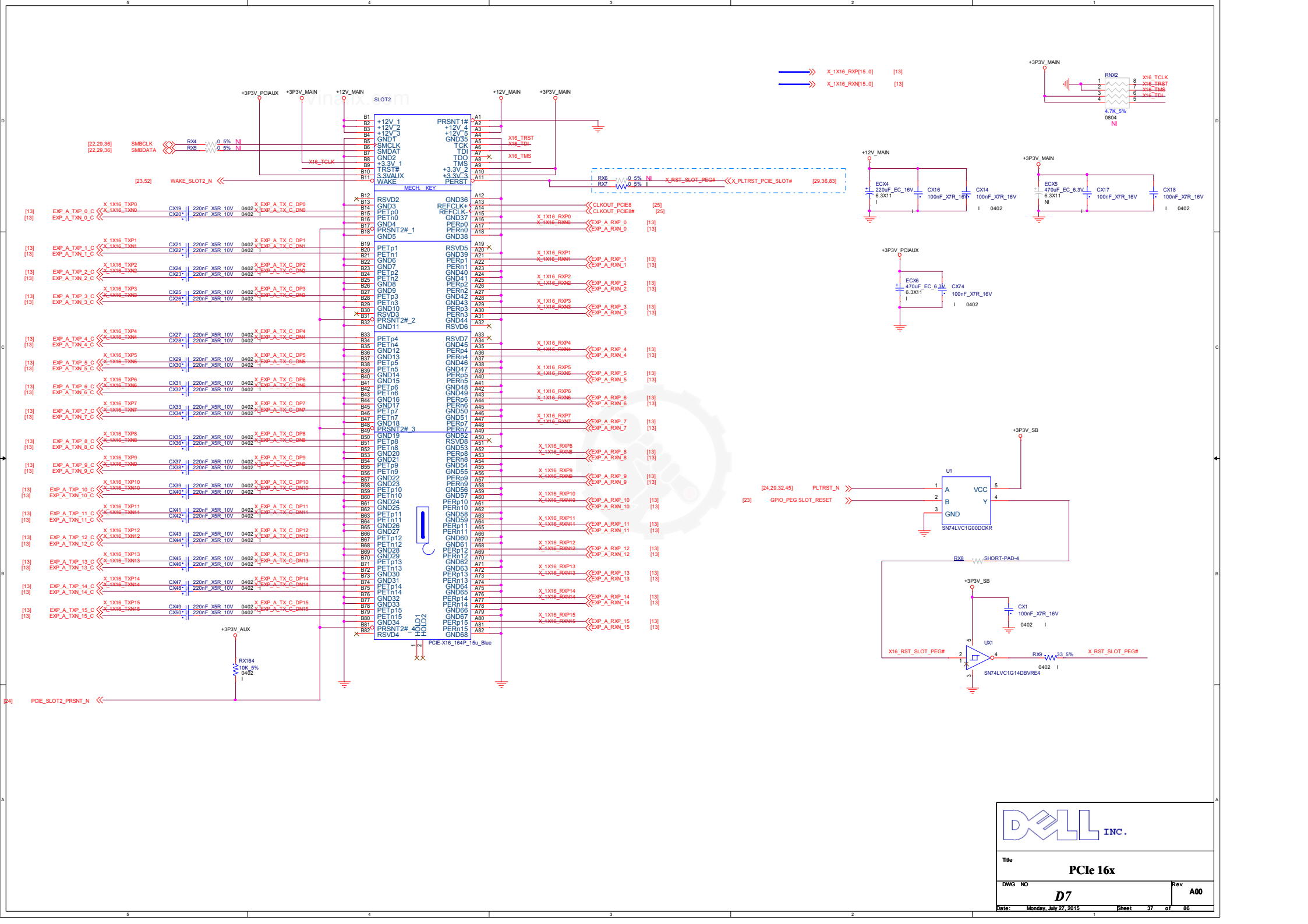
SLOT2
MECH_KEY
PCIE-X16_164P_15u_Blue
+3P3V_PCIAUX
+3P3V_MAIN
+12V_MAIN
+3P3V_AUX
+3P3V_SB
SMBCLK
SMBDATA
WAKE_SLOT2_N
PCIE_SLOT2_PRSNT_N
X_1X16_RXP[15..0]
X_1X16_RXN[15..0]
X16_TCLK
X16_TRST
X16_TDI
X16_TMS
X_RST_SLOT_PEG#
X_PLTRST_PCIE_SLOT#
CLKOUT_PCIE8
CLKOUT_PCIE8#
PLTRST_N
GPIO_PEG SLOT_RESET
SHORT-PAD-4
SN74LVC1G00DCKR
SN74LVC1G14DBVRE4
PCIe 16x
D7
A00
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Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

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Title

CPU

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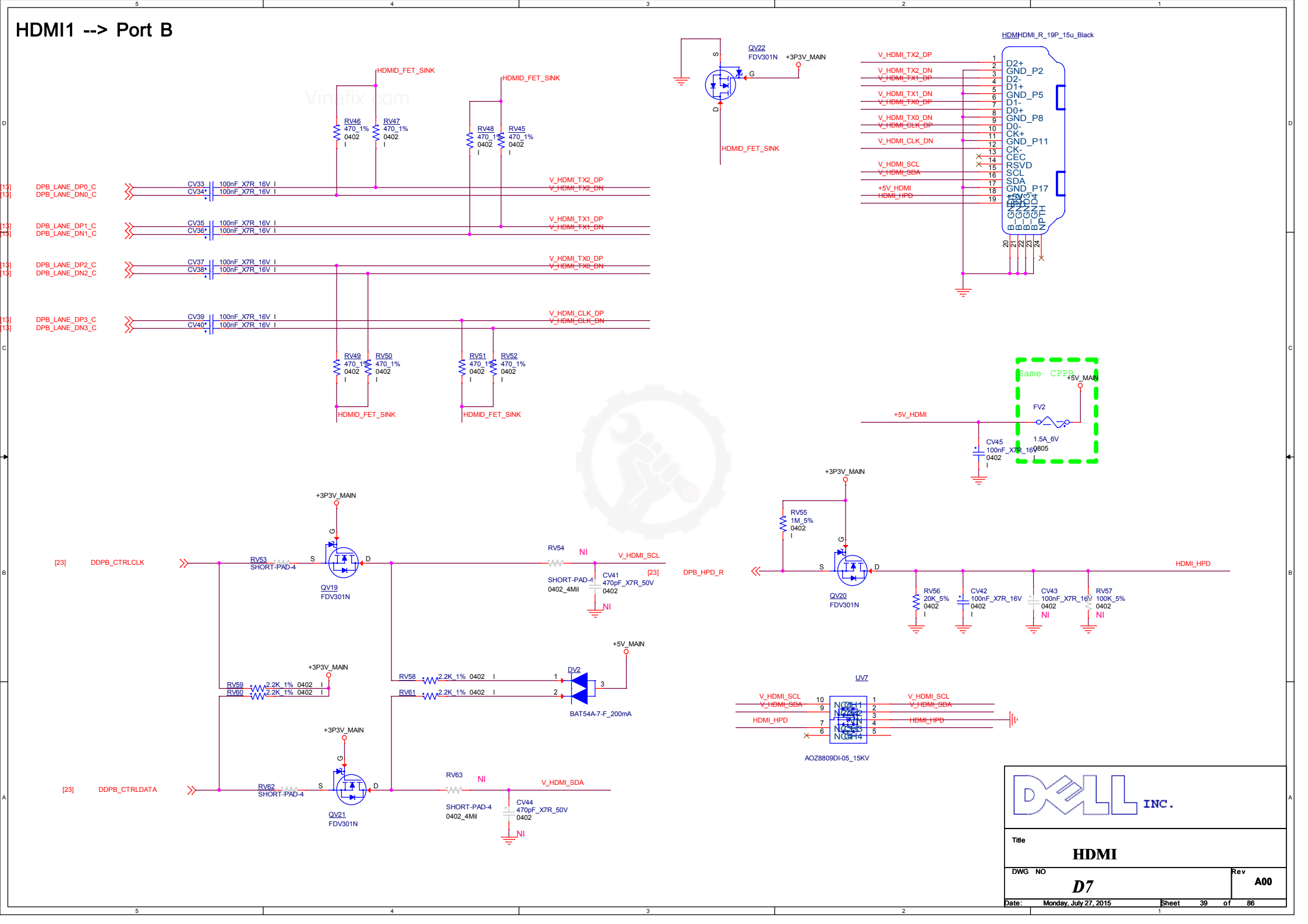
HDMI1 --> Port B



DELL INC.

Title	HDMI
DWG NO	D7
Rev	A00
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Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title

CPU

DWG NO	Rev
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Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title

CPU

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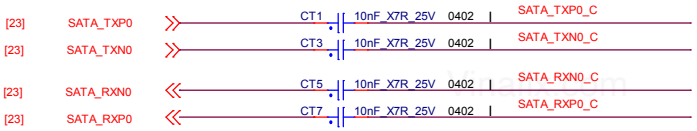
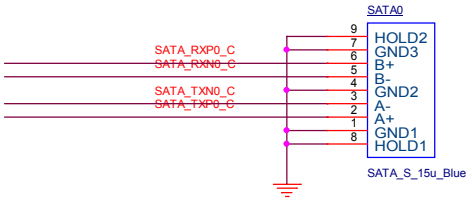
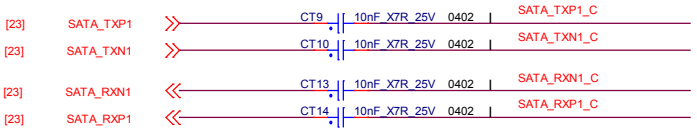
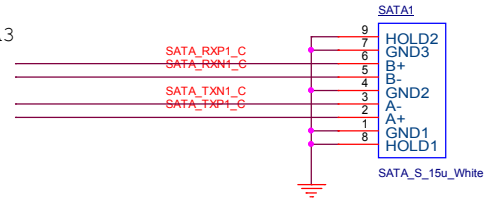


Blue SATA3





white ODD SATA3



DELL INC.

Title: **SATA Conn**

DWG NO: *D7*

Rev: **A00**

Date: Monday, July 27, 2015 Sheet 42 of 86

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

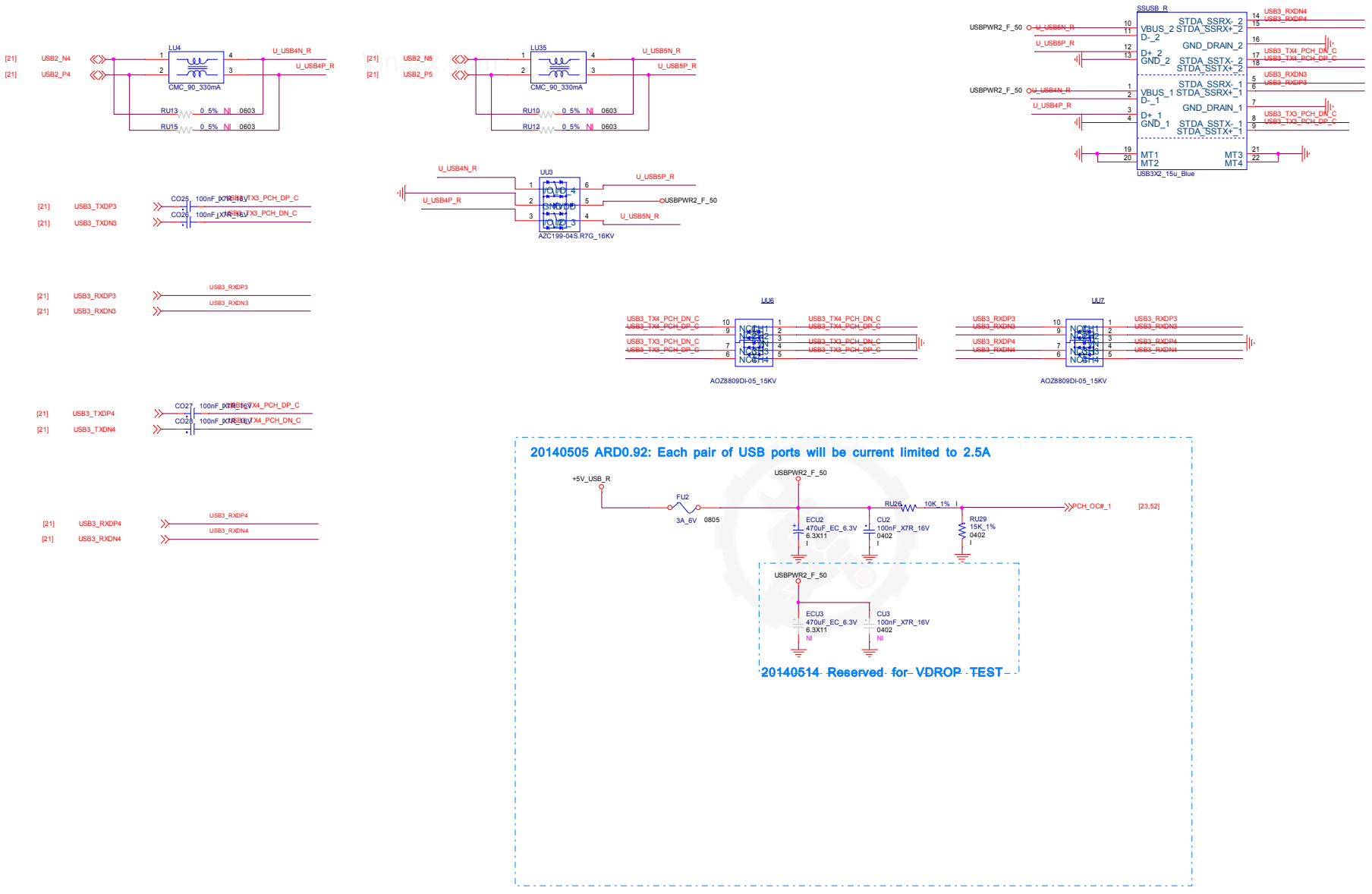
DELL INC.

Title

CPU

DWG NO	Rev
D7	A00

Date: Monday, July 27, 2015 Sheet 43 of 86



DELL INC.

Title: **Rear USB**

DWG NO: *D7*

Rev: A00

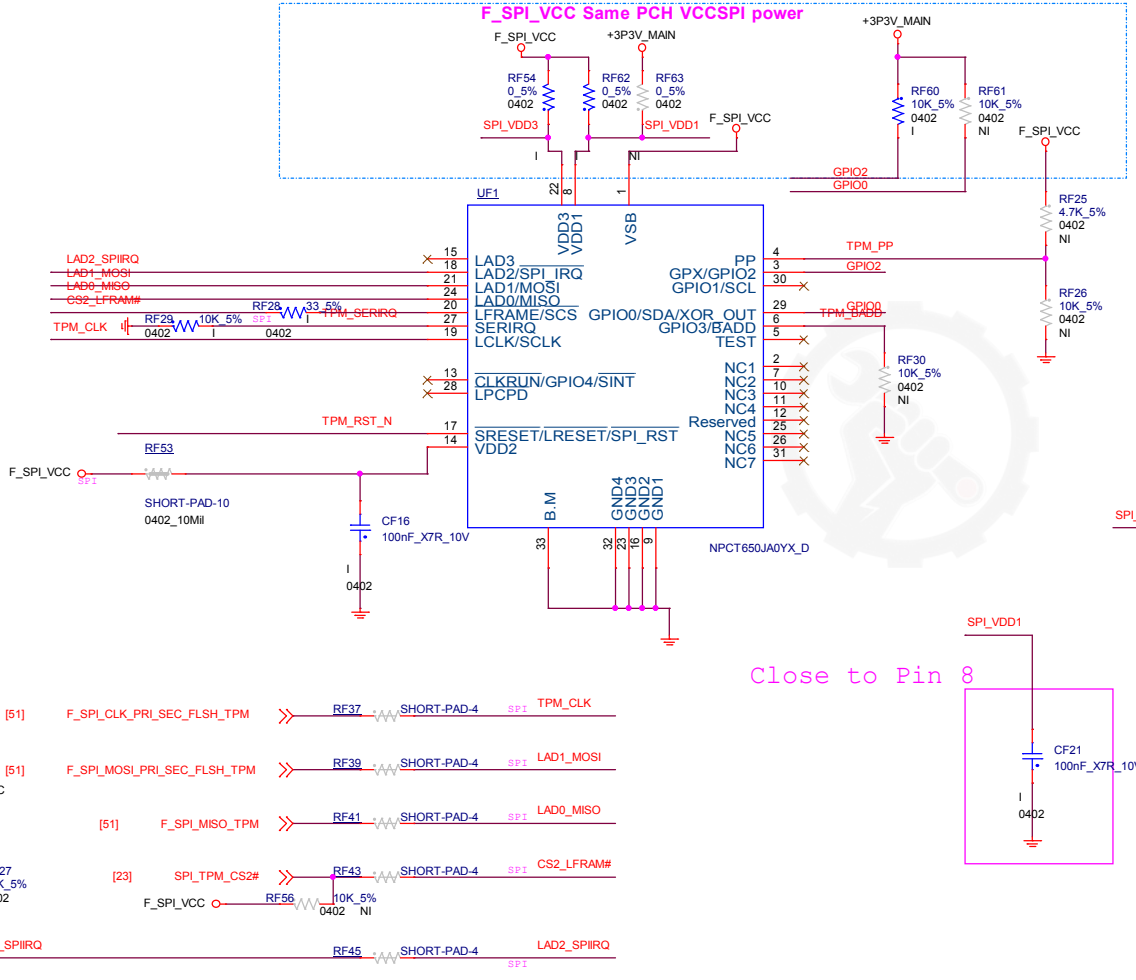
Date: Monday, July 27, 2015 Sheet 44 of 86

Trusted Computing Support

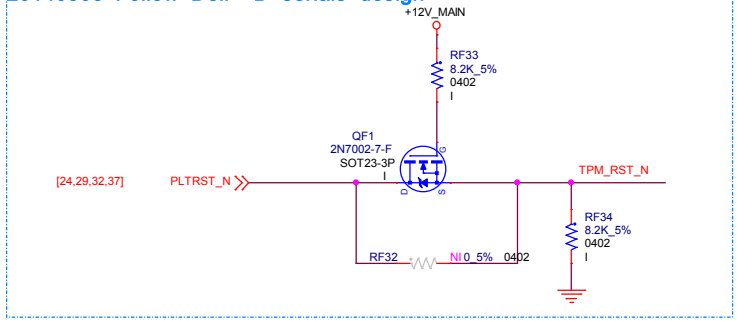
HW Low Power Mode	RF62	RF63	RF60
Support	Un-stuff	Stuff	Stuff
Not support	Stuff	Un-stuff	Un-stuff

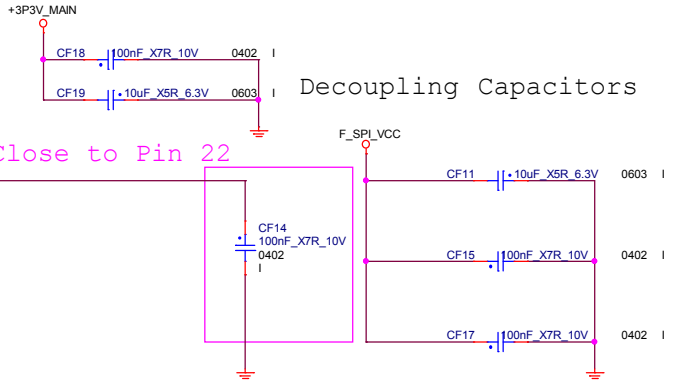
Nuvoton NPCT650JAAYX - 2.0
NPCT650JA0YX - 1.2

F_SPI_VCC Same PCH VCCSPI power



20140508 Follow Dell D serials design





NOTE:
- Place 0.1 uF capacitors as close as possible to the device power pins.
- CF17 is required only for the NPCT620/650.

DELL INC.

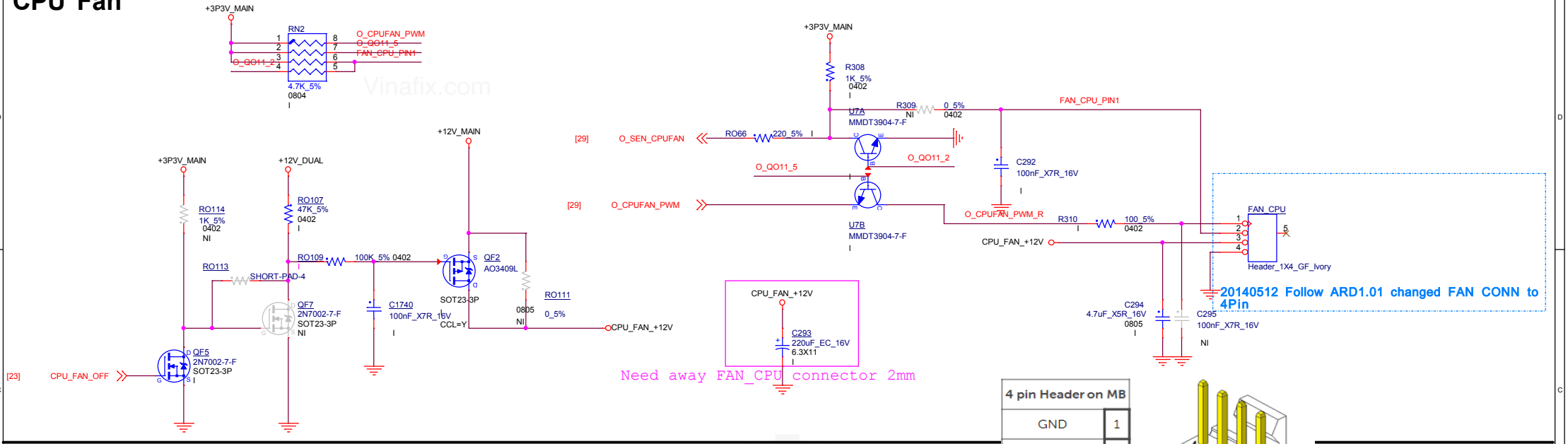
Title: **TPM**

DWG NO: ***D7***

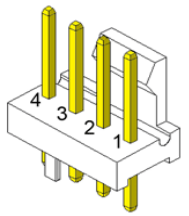
Rev: **A00**

Date: Monday, July 27, 2015 Sheet 45 of 86

CPU Fan

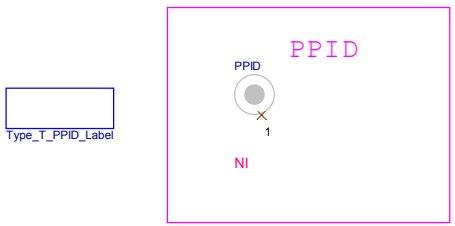


4 pin Header on MB	
GND	1
+12V	2
TACH_IN	3
PWM_OUT	4



SYS Fan

LABEL



Type_T_PPID_Label

SFF7

SFF5 DDR4

SFF5 DDR3L

PCB1 SFF3

Printed Circuit Board

PCB_D6 KINGCOBRA
<CRITICAL>

DELL INC.

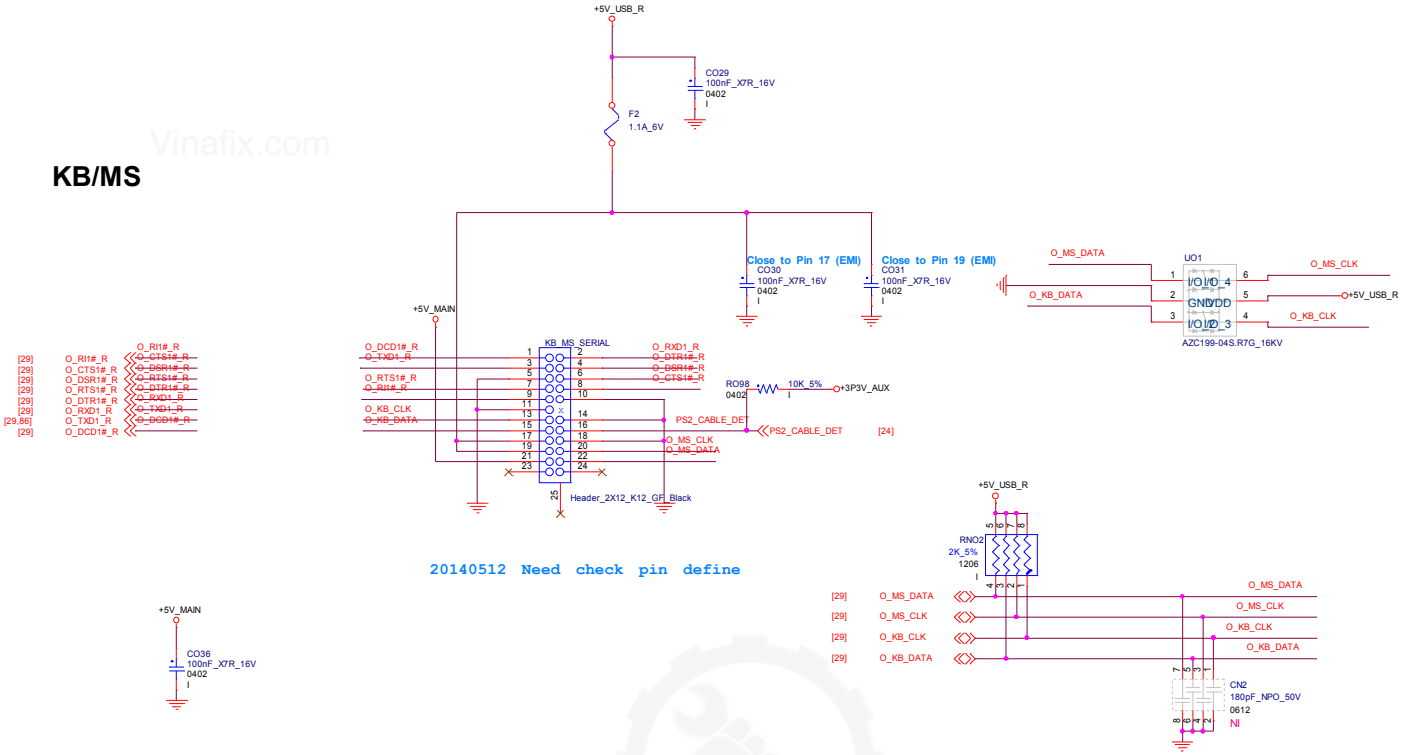
Title

FAN & LABEL

DWG NO	Rev
D7	A00

Date: Monday, July 27, 2015 Sheet 46 of 86

Serial Port 1 KB/MS



Title	PS2 Conn
DWG NO	D7
Rev	A00
Date:	Monday, July 27, 2015
Sheet	47 of 86

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title

CPU

DWG NO

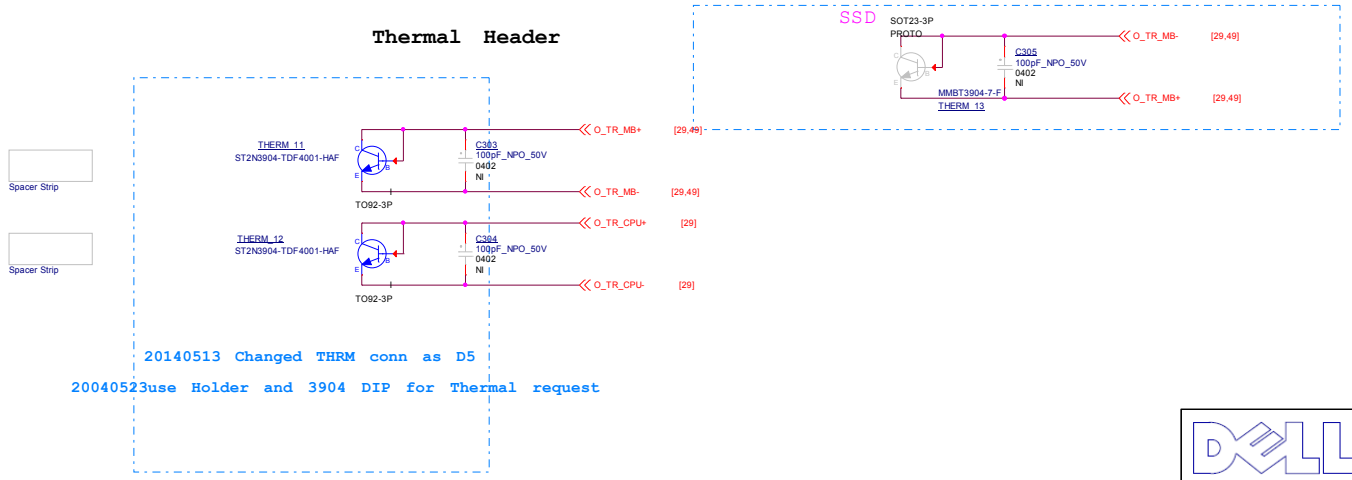
D7

Rev

A00

Date: Monday, July 27, 2015 Sheet 48 of 86

Thermal Header



DELL INC.

Title: **Thermal Sensor**

DWG NO: *D7*

Rev: A00

Date: Monday, July 27, 2015

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title

CPU

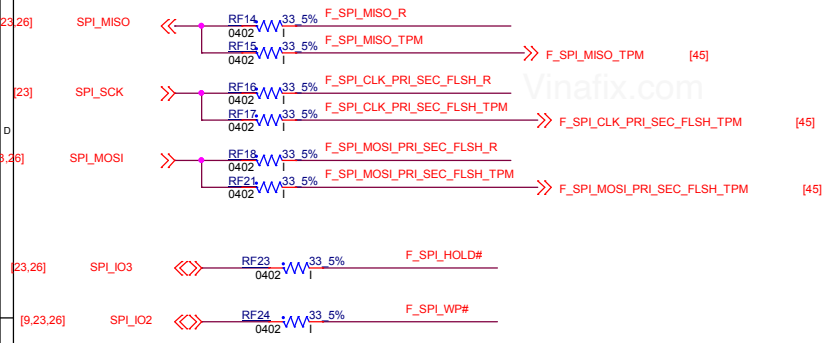
DWG NO

D7

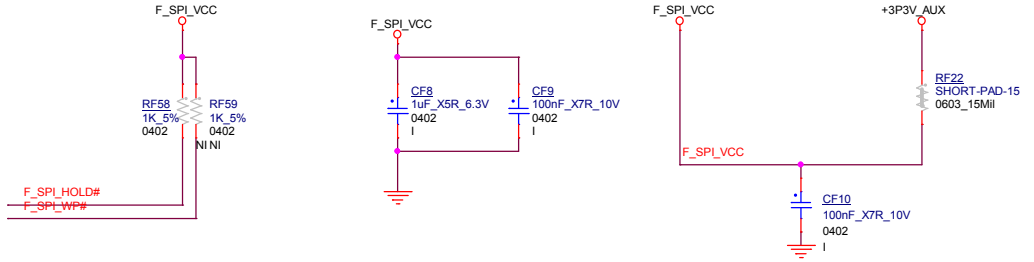
Rev

A00

Date: Monday, July 27, 2015 Sheet 50 of 86



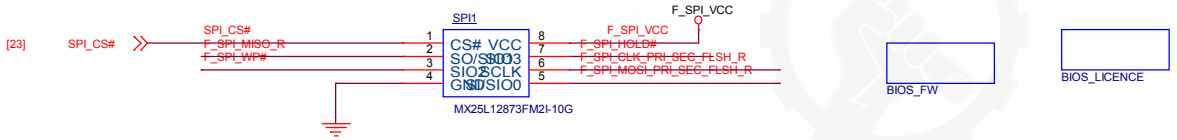
20140506 Follow CRB0.5 and PDG0.7 use +3P3V_AUX (enabled by SLP_SUS# for SPI VCC

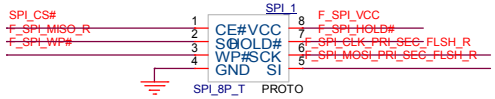


SPI_16MB

20140506 ARD0.92 : One SPI FLASH device site on PCB

Before RTS, please use DIP





DELL INC.

Title: SPI

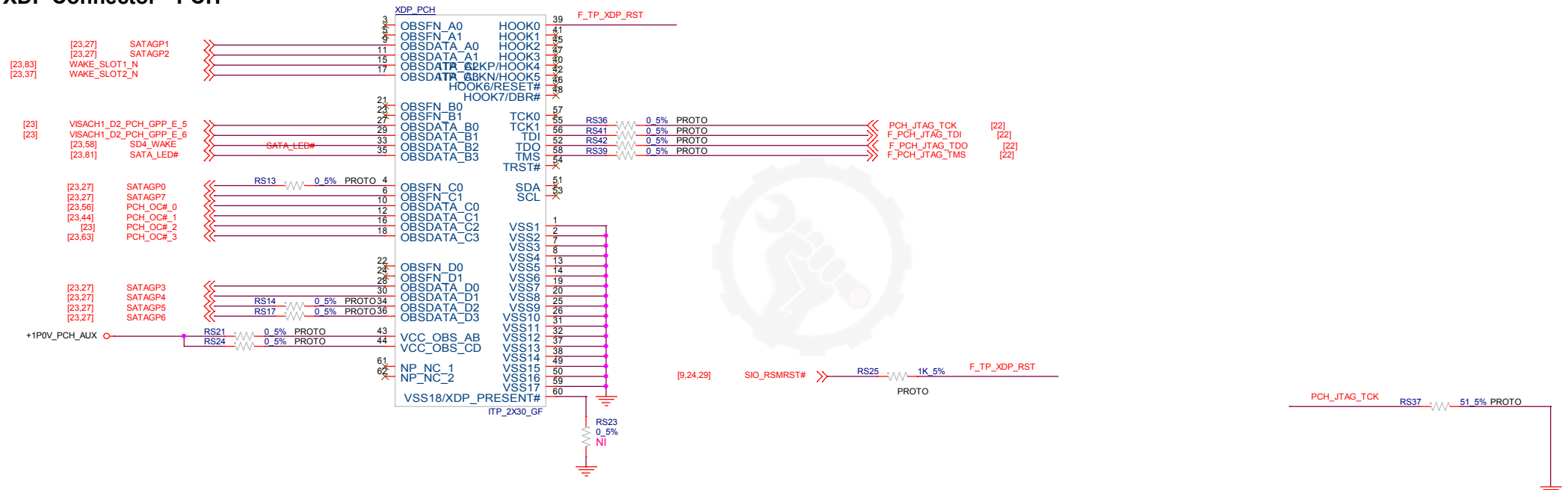
DWG NO: D7

Rev: A00

Date: Monday, July 27, 2015 Sheet 51 of 86

20140505 Remove Duplicated XDP

XDP Connector - PCH



DELL INC.

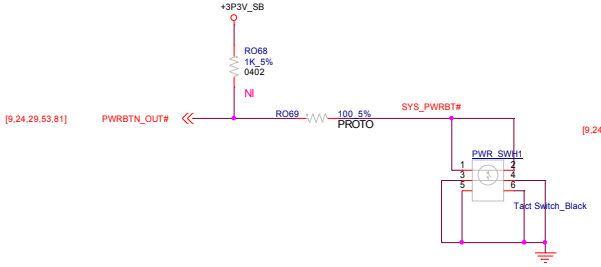
Title: XDP

DWG NO: D7

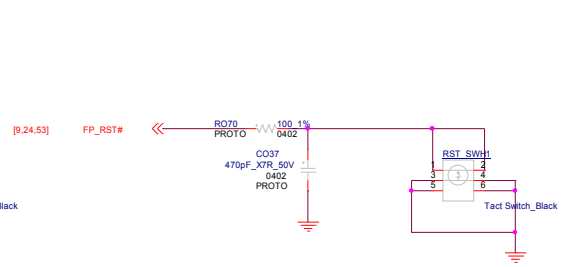
Rev: A00

Date: Monday, July 27, 2015 Sheet 52 of 86

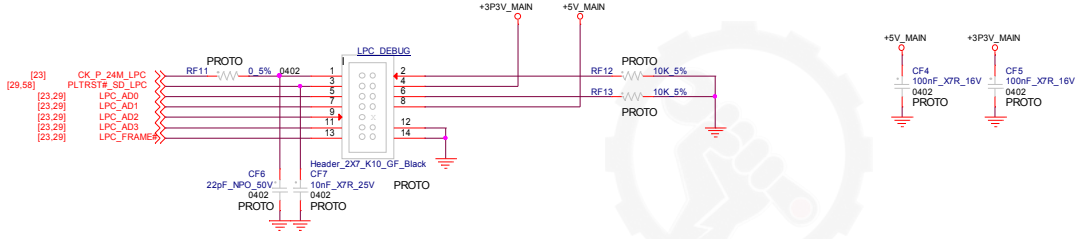
Power Bottom



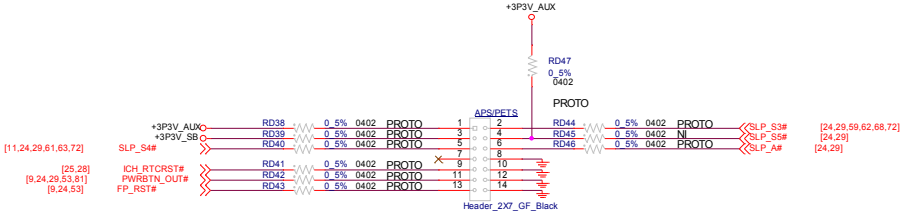
Reset Bottom



LPC DEBUG



APS Debug



Desktop		
APS Connector	Pin	Meaning
Pin 1	VccSus3_3	3.3 V Suspend Power Well
Pin 2	SLP_S3#	When asserted (0) system is in S3
Pin 3	VccDSW3_3	Used to determine if system is in Deep Sx
Pin 4	VccSus3_3	When off (0) system is in S5
Pin 5	SLP_S4#	When asserted (0) system is in S4
Pin 6	SLP_A#	When asserted (0) ME is in Moff
Pin 7	Unused	
Pin 8	GND	Ground
Pin 9	RTCRST#	When asserted (0) CMOS is cleared
Pin 10	GND	Ground for RTCRST#
Pin 11	PWRBTN#	When asserted (0) Power Button Pushed
Pin 12	GND	Ground for PWRBTN#
Pin 13	SYS_RESET#	When asserted (0) Reset Button Pushed
Pin 14	GND	Ground for SYS_RESET#

DELL INC.

Title: **Pilot Run Conn**

DWG NO: *D7* | Rev: A00

Date: Monday, July 27, 2015 | Sheet 53 of 86

FD2 OPTICS NI
FD1 OPTICS NI
FD3 OPTICS NI
FD4 OPTICS NI
FD5 OPTICS NI
FD6 OPTICS NI

Thermal Need

MH1 Mounting Hole MH40X80_10_DELL_L4
MH20 Mounting Hole NP236_RK354
MH3 Mounting Hole MH40X80_10_DELL_L4
MH5 Mounting Hole MH40X80_10_DELL_L4
MH6 Mounting Hole MH40X80_10_DELL_L4
MH7 Mounting Hole MH40X80_10_DELL_L4
MH8 Mounting Hole MH40X80_10_DELL_L4
MH10 Mounting Hole NP79_RK118
MH9 Mounting Hole NP79_RK118
NOBOM TPVIA372 A_GND

20140521 Change MH footprint to mh40x80_8 dell(Follow D.5

20140429 Need double confirm EMC caps location.

for H_ITPCLK.
for Front USB3.0

SFF3 SFF7

Title	EMI
DWG NO	D7
Rev	A00
Date:	Monday, July 27, 2015
Sheet	54 of 86

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title

CPU

DWG NO	Rev
D7	A00

Date: Monday, July 27, 2015 Sheet 55 of 86

Front USB/LED Header

SFF

+5V_USB_F
USBPWR1_F_50
FU6
3A_6V
0805
ECU6 470uF_EC_6.3V 6.3X11
CU10 100nF_X7R_16V 0402
RU46 10K_1%
RU47 15K_1% 0402
PCH_OC#_0 [23,52]

20140505 Need check OC arrangement

USBPWR1_F_50
+5V_USB_F
CO42 100nF_X7R_16V 0402
ECU7 470uF_EC_6.3V 6.3X11
CU11 100nF_X7R_16V 0402

20140505 Reserved

USBPWR1_F_50
U_USB2N_R
U_USB2P_R
USBPWR1_F_50
U_USB1N_R
U_USB1P_R

SSUSB_F
STDA_SSRX-_2
VBUS_2 STDA_SSRX+_2
D-_2
GND_DRAIN_2
D+_2
GND_2 STDA_SSTX-_2
STDA_SSTX+_2
STDA_SSRX-_1
VBUS_1 STDA_SSRX+_1
D-_1
GND_DRAIN_1
D+_1
GND_1 STDA_SSTX-_1
STDA_SSTX+_1
MT1 MT2 MT3 MT4
USB3X2_15u_Blue

USB3_RXDN2
USB3_RXDP2
USB3_TX2_PCH_DN_C
USB3_TX2_PCH_DP_C
USB3_RXDN1
USB3_RXDP1
USB3_TX1_PCH_DN_C
USB3_TX1_PCH_DP_C

20140505 ARD0.92: Each pair of USB ports will be current limited to 2.5A

LU36
USB2_N1
USB2_P1
U_USB1N_R
U_USB1P_R
CMC_90_330mA
RU54 0_5% NI
RU55 0_5% NI

LU37
USB2_N2
USB2_P2
U_USB2N_R
U_USB2P_R
CMC_90_330mA
RU58 0_5% NI
RU59 0_5% NI

[21] USB3_TXDP1
[21] USB3_TXDN1
CO43 100nF_X7R_16V
CO44 100nF_X7R_16V
USB3_TX1_PCH_DP_C
USB3_TX1_PCH_DN_C

[21] USB3_RXDP1
[21] USB3_RXDN1
USB3_RXDP1
USB3_RXDN1

U_USB2N_R
U_USB2P_R
UU9
U_USB1P_R
USBPWR1_F_50
U_USB1N_R
AZC199-04S.R7G_16KV

Pin 1 Pin 2 Pin 3 Pin 4 Pin 5
Pin 9 Pin 8 Pin 7 Pin 6
a) Pin configuration

Pin 1 Pin 2 Pin 4 Pin 5
I/O I/O I/O I/O
GND
Pin 3
b) Schematic diagram

[21] USB3_TXDN2
[21] USB3_TXDP2
CO45 100nF_X7R_16V
CO46 100nF_X7R_16V
USB3_TX2_PCH_DN_C
USB3_TX2_PCH_DP_C

[21] USB3_RXDN2
[21] USB3_RXDP2
USB3_RXDN2
USB3_RXDP2

UU10
USB3_TX1_PCH_DP_C
USB3_TX1_PCH_DN_C
USB3_TX2_PCH_DN_C
USB3_TX2_PCH_DP_C
AOZ8809DI-05_15KV

UU11
USB3_RXDP1
USB3_RXDN1
USB3_RXDP2
USB3_RXDN2
AOZ8809DI-05_15KV

DELL INC.

Title: FRONT_USB3.0

DWG NO: D7

Rev: A00

Date: Monday, July 27, 2015 Sheet 56 of 86

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title: **CPU**

DWG NO: ***D7***

Rev: **A00**

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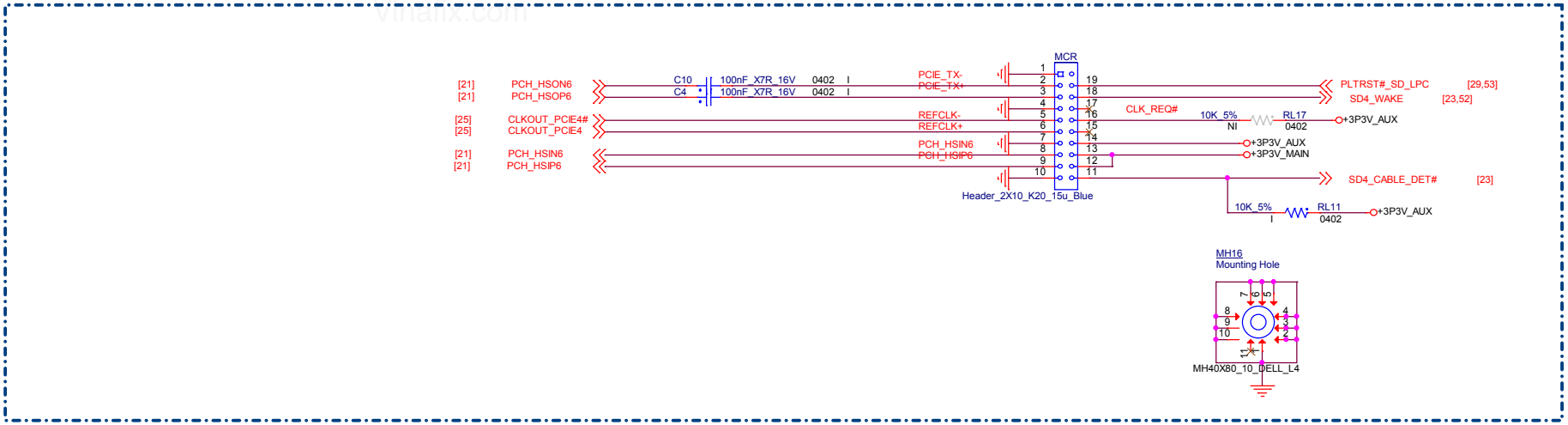
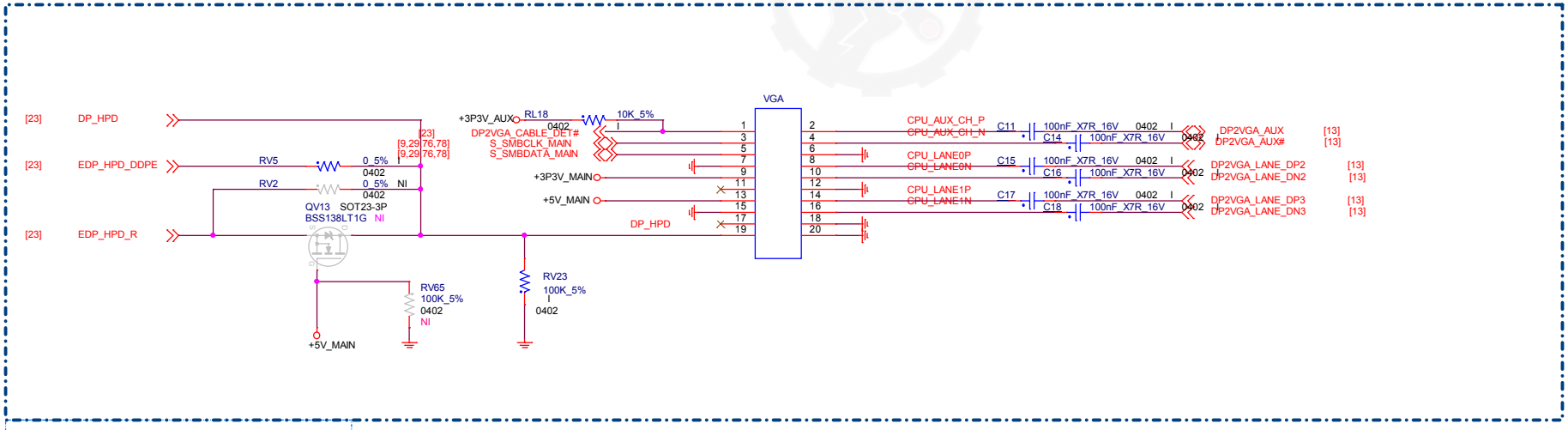
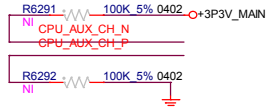
SD4.0 CONN



eDP to VGA CONN

M/B part already OK





20140515 reserved for AUX

DELL INC.

Title: SD4.0 CON/ DP TO VGA CON

DWG NO: D7

Rev: A00

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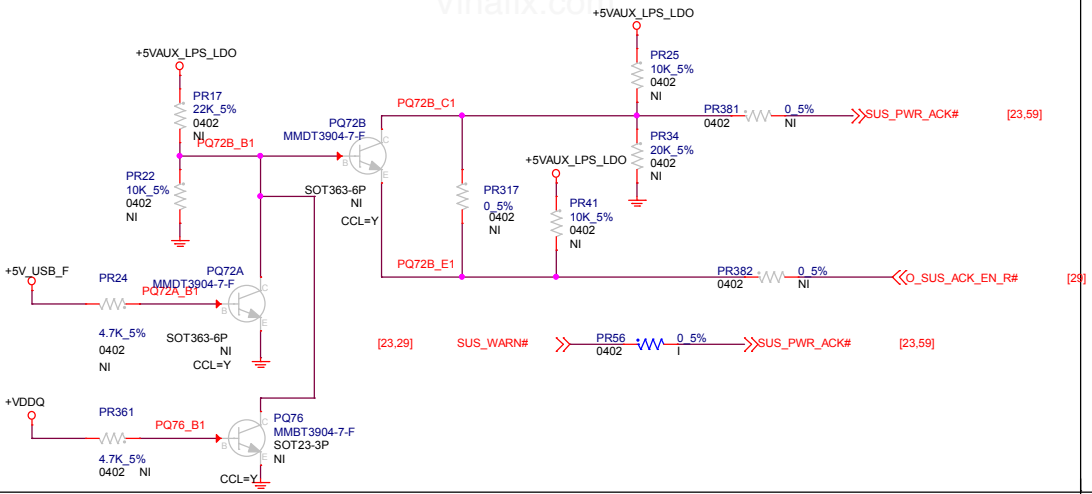
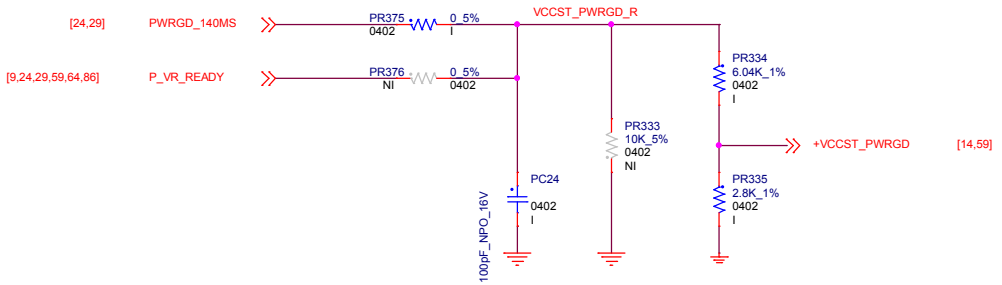
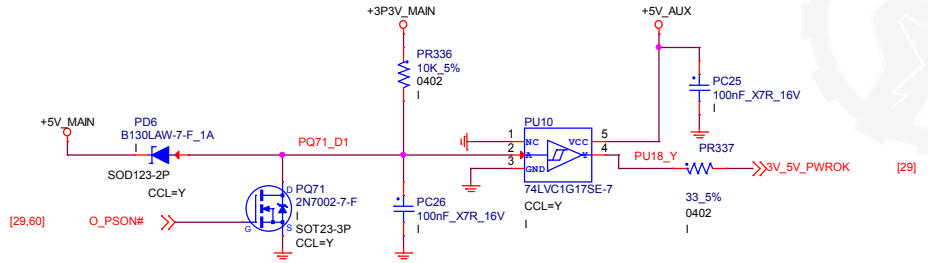
Power Sequence



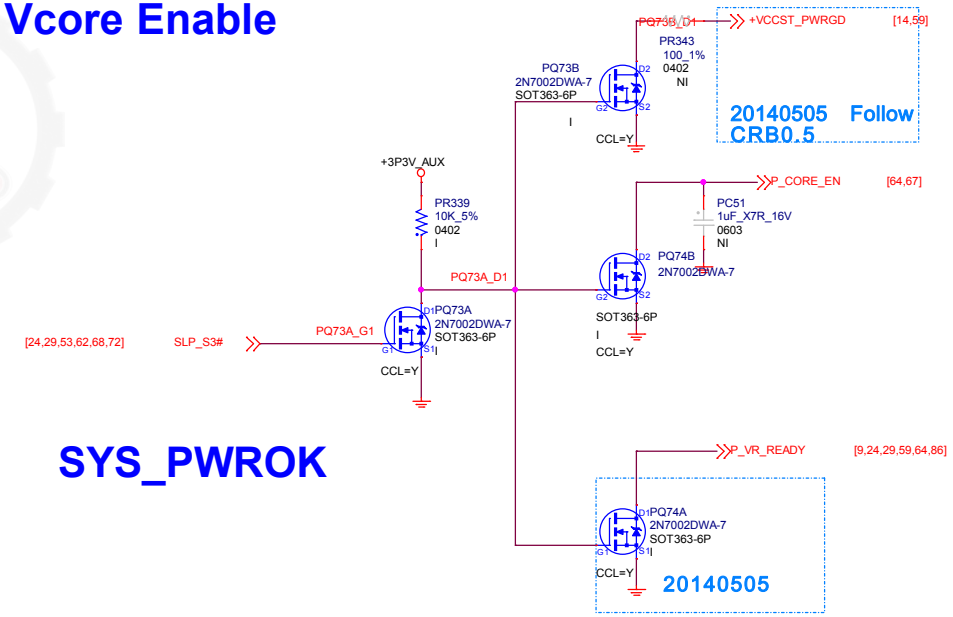
VCCST_PWRGD/PCH_PWROK



Power Sequence



Vcore Enable



SYS_PWROK

DELL INC.

Title

Power Sequence

DWG NO	Rev
D7	A00

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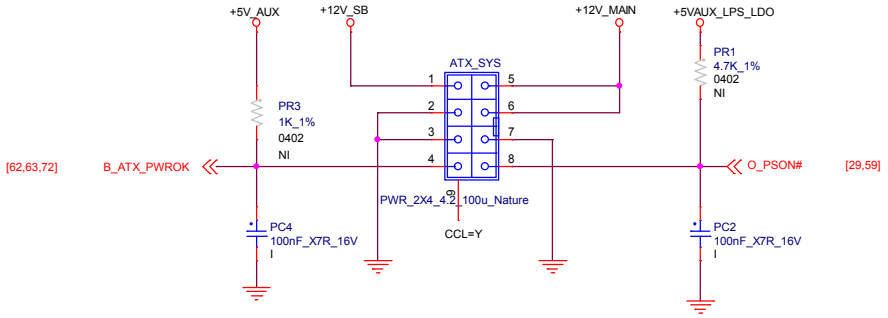
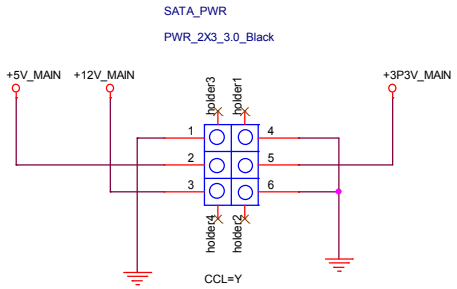
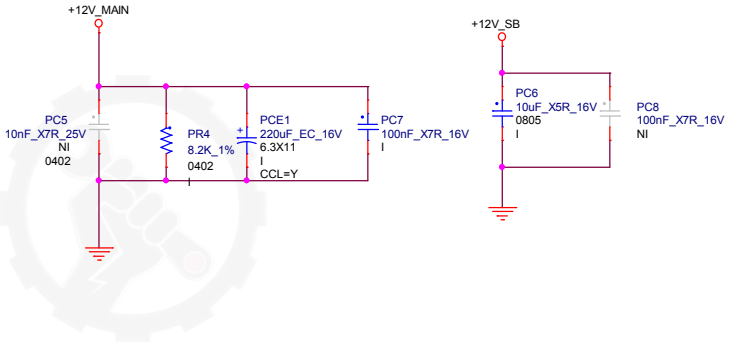
ATX POWER CONNECTOR



For ODD and HDD For SFF





DELL INC.

Title: **Power CONN**

DWG NO: *D7*

Rev: A00

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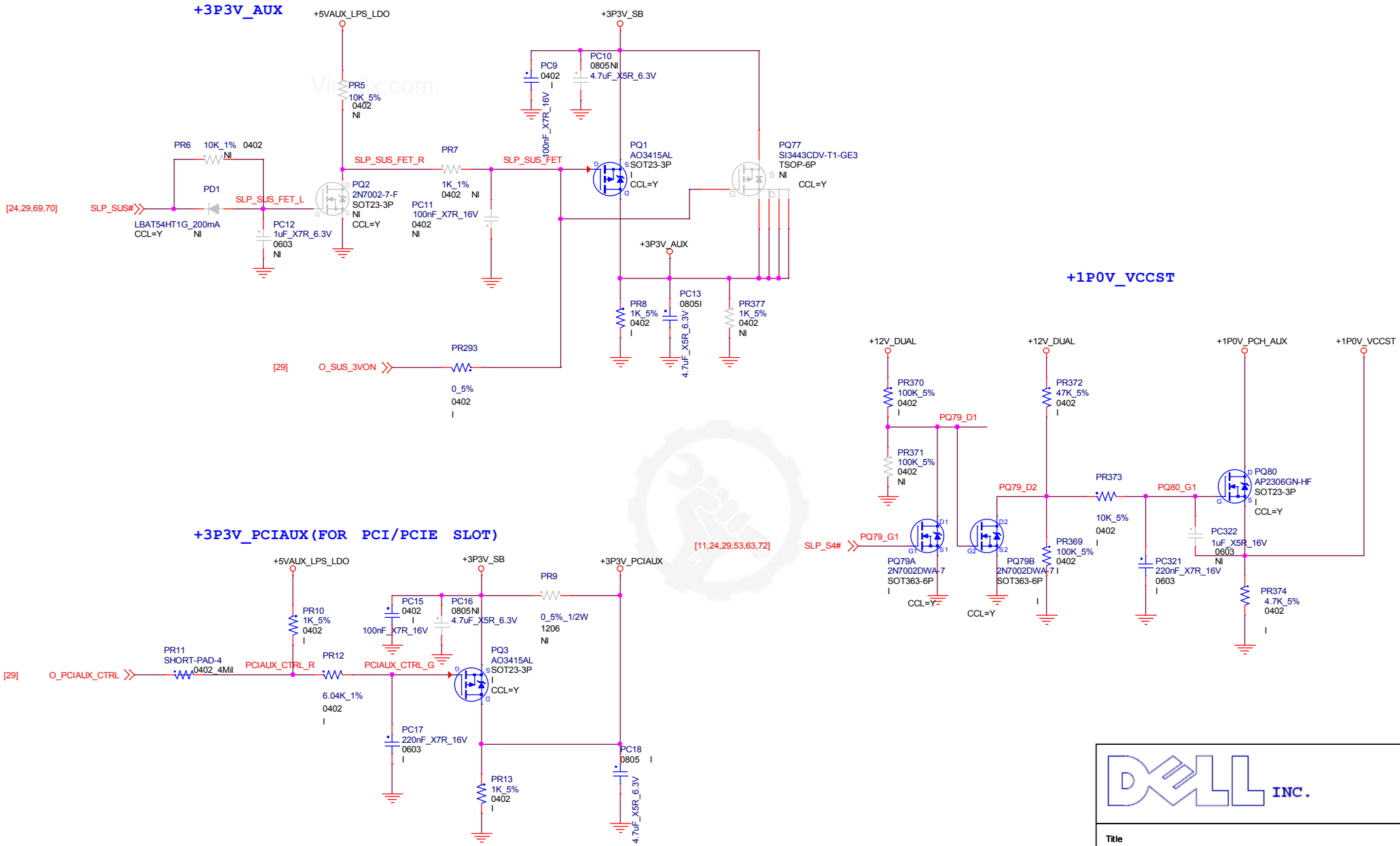


DELL INC.

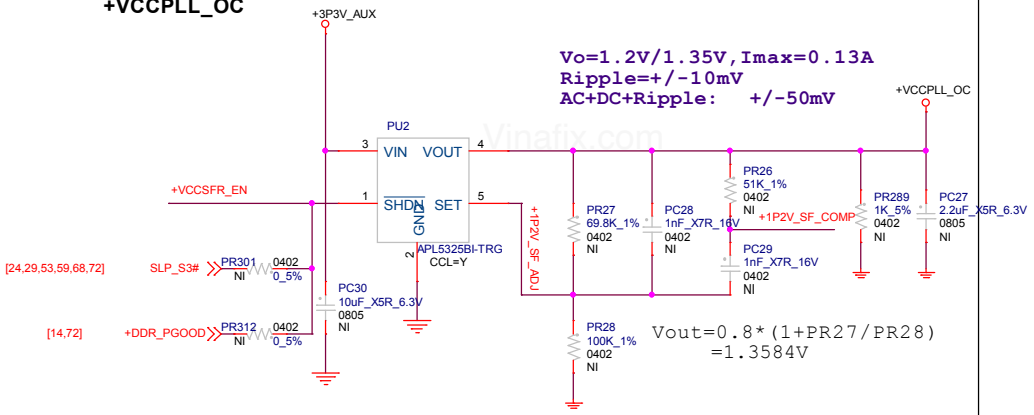
Title

Power-1: Linear Power-1

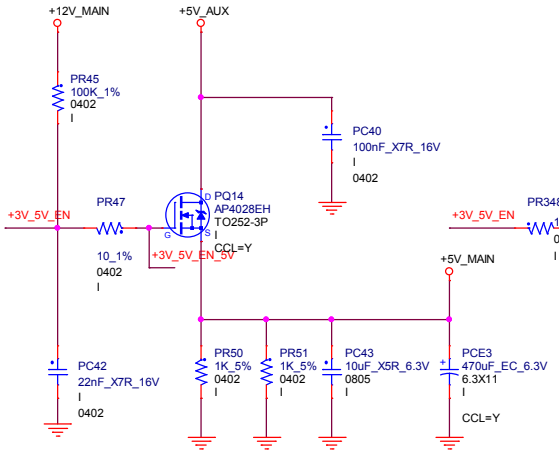
DWG NO	Rev
D7	A00

Date: Monday, July 27, 2015 Sheet 61 of 86

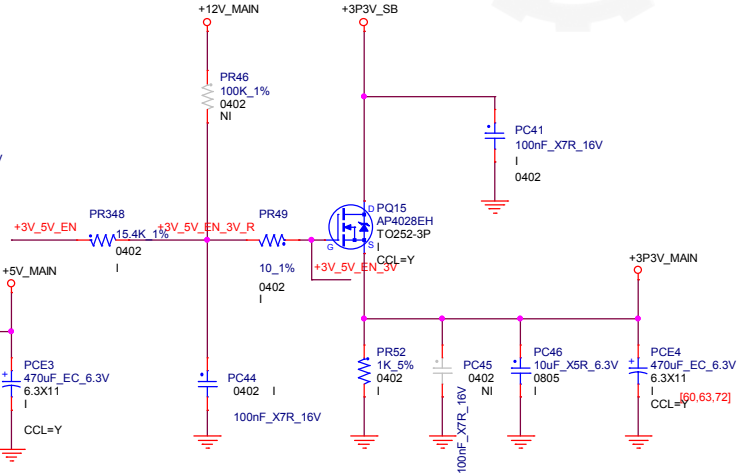
+VCCPLL_OC

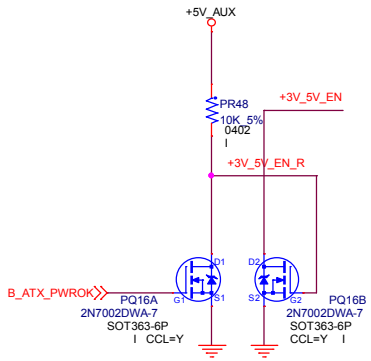


+5V MAIN



+3P3V_MAIN





DELL INC.

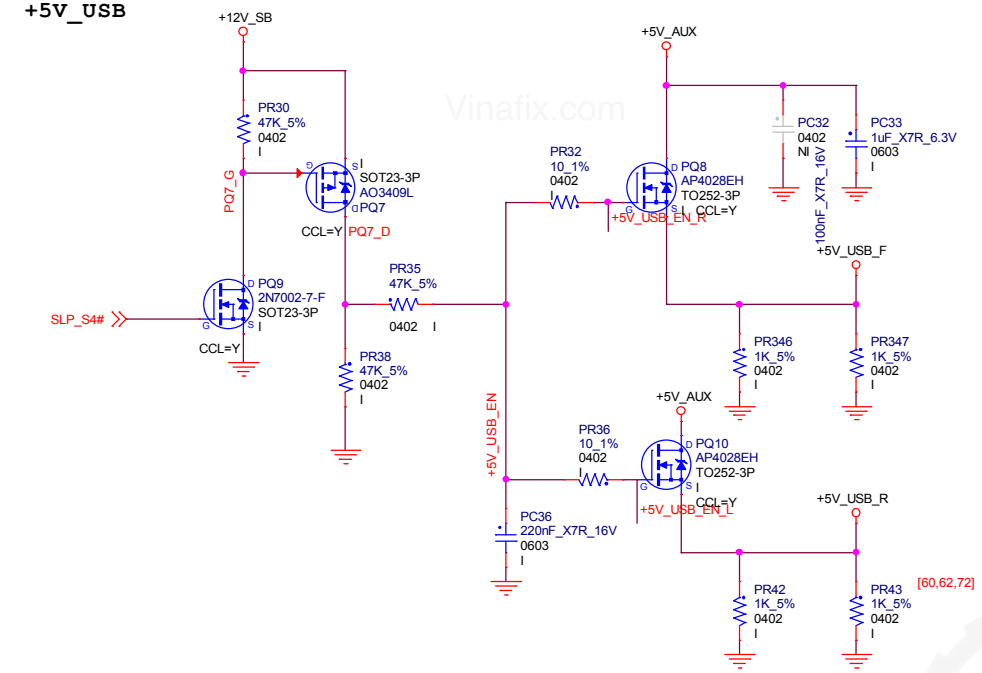
Title

Power-2: Linear Power-2

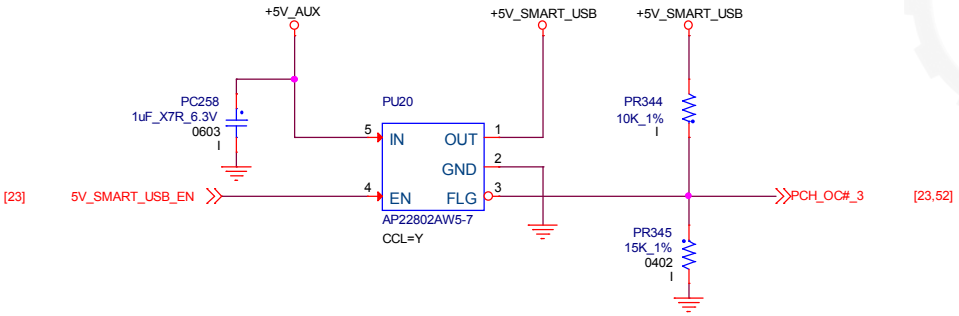
DWG NO	Rev
D7	A00

Date: Monday, July 27, 2015 Sheet 62 of 86

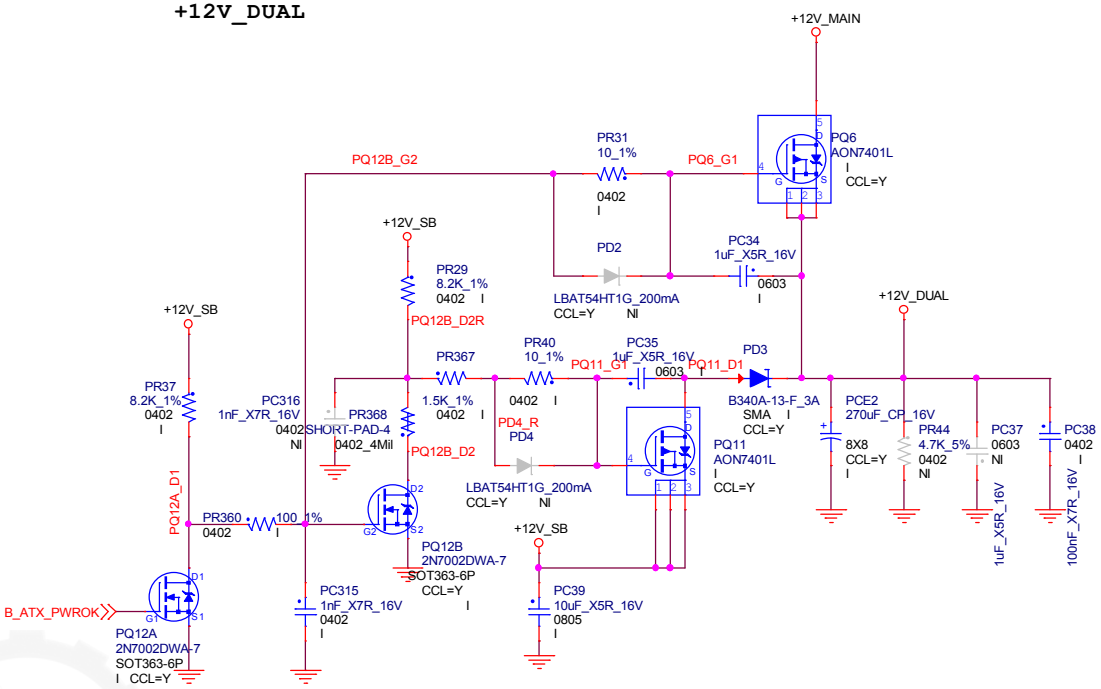
+5V_USB



+5V_SMART_USB



+12V_DUAL



DELL INC.

Title

Power-3: Linear Power-3

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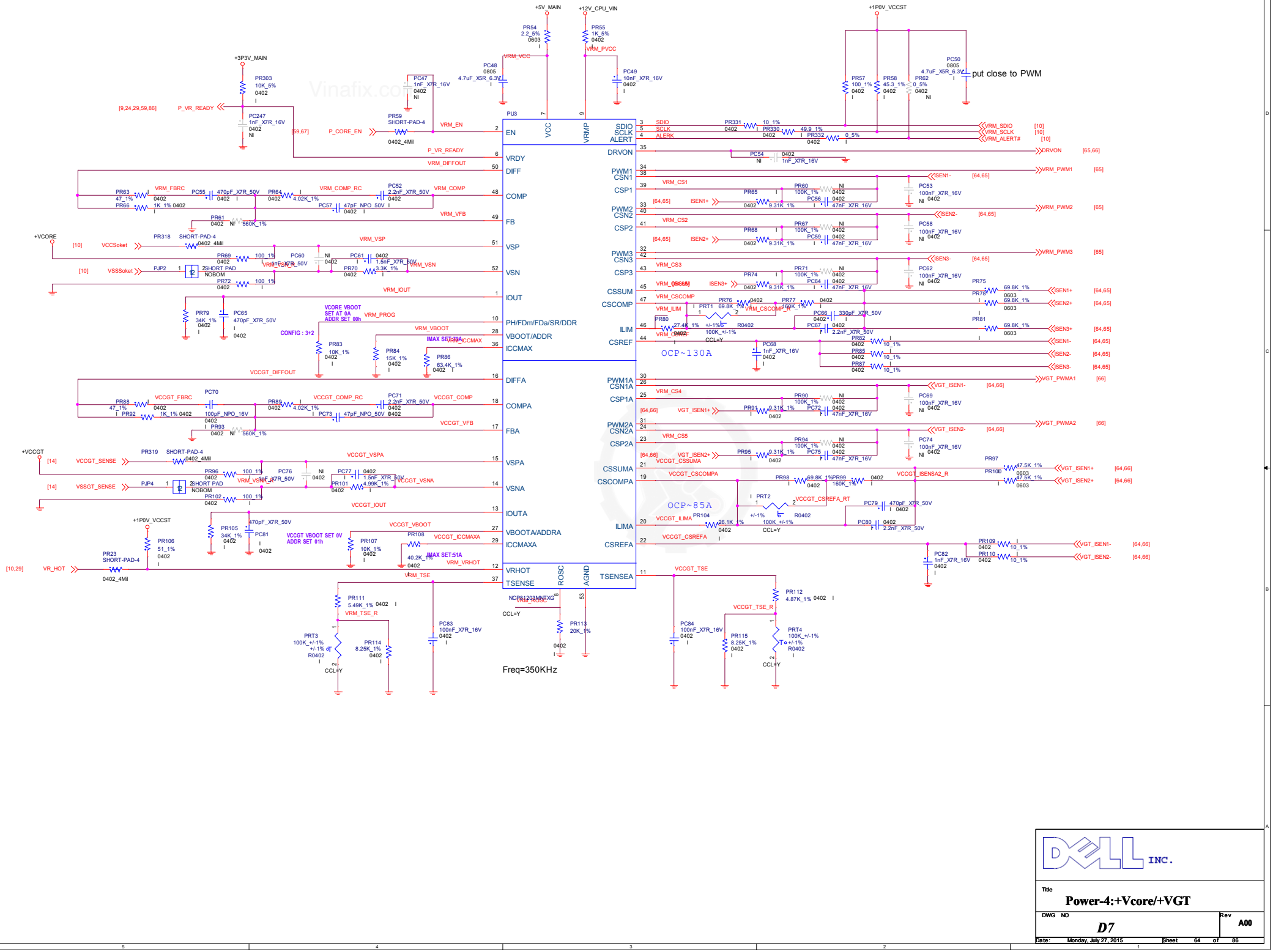
+5V_MAIN
+12V_CPU_VIN
+1P0V_VCCST
+3P3V_MAIN
PR54 2.2_5% 0603
PR55 1K_5% 0402
VRM_VCC
VRM_PVCC
PC48 0805 4.7uF_X5R_6.3V
PC49 10nF_X7R_16V 0402
PC50 0805 4.7uF_X5R_6.3V
put close to PWM
PR57 100_1% 0402
PR58 45.3_1% 0402
PR62 0_5% 0402 NI
PR303 10K_5% 0402
PC47 1nF_X7R_16V 0402 NI
PC247 1nF_X7R_16V 0402 NI
[9,24,29,59,86] P_VR_READY
[59,67] P_CORE_EN
PR59 SHORT-PAD-4 0402_4Mil
VRM_EN
P_VR_READY
VRM_DIFFOUT
PU3
EN
VCC
VRMP
VRDY
DIFF
COMP
FB
VSP
VSN
IOUT
PH/FDm/FDa/SR/DDR
VBOOT/ADDR
ICCMAX
DIFFA
COMPA
FBA
VSPA
VSNA
IOUTA
VBOOTA/ADDRA
ICCMAXA
VRHOT
TSENSE
ROSC
AGND
TSENSEA
SDIO
SCLK
ALERT
DRVON
PWM1
CSN1
CSP1
PWM2
CSN2
CSP2
PWM3
CSN3
CSP3
CSSUM
CSCOMP
ILIM
CSREF
PWM1A
CSN1A
CSP1A
PWM2A
CSN2A
CSP2A
CSSUMA
CSCOMPA
ILIMA
CSREFA
PR331 10_1%
PR330 49.9_1%
PR332 0_5%
VRM_SDIO [10]
VRM_SCLK [10]
VRM_ALERT# [10]
DRVON [65,66]
PC54 NI 0402 1nF_X7R_16V
VRM_PWM1 [65]
VRM_PWM2 [65]
VRM_PWM3 [65]
ISEN1- [64,65]
ISEN2- [64,65]
ISEN3- [64,65]
ISEN1+ [64,65]
ISEN2+ [64,65]
ISEN3+ [64,65]
VRM_CS1
VRM_CS2
VRM_CS3
VRM_CS4
VRM_CS5
PR65 PR67 PR68 PR74 PR90 PR94 PR95
PR60 PR71 PR76 PR77 PR82 PR85 PR87
PR56 PR64 PR75 PR78 PR81
PC53 PC58 PC62 PC69 PC74
100nF_X7R_16V NI 0402
47nF_X7R_16V 0402
9.31K_1%
100K_1%
69.8K_1%
0603
VRM_CSCOMP
VRM_ILIM
PR80 27.4K_1% 100K_+/-1%
PR79 PR84 PR86
PC65 470pF_X7R_50V
PC66 330pF_X7R_50V
PC67 2.2nF_X7R_50V
PC68 1nF_X7R_16V
PR81 69.8K_1%
PR83 10K_1%
PR84 15K_1%
PR86 63.4K_1%
PR82 PR85 PR87 10_1%
OCP~130A
VCORE VBOOT SET AT 0A ADDR SET 00h
CONFIG : 3+2
VRM_PROG
VRM_VBOOT
IMAX SET:79A
VRM_ICCMAX
VCCGT_DIFFOUT
VGT_ISEN1- [64,66]
VGT_ISEN1+ [64,66]
VGT_ISEN2- [64,66]
VGT_ISEN2+ [64,66]
VGT_PWMA1 [66]
VGT_PWMA2 [66]
PR88 PR92 PR89 PR93
PC70 100pF_NPO_16V
PC71 2.2nF_X7R_50V
PC69 PC72 PC73 PC74
100nF_X7R_16V NI 0402
47nF_X7R_16V 0402
47pF_NPO_50V
4.02K_1%
1K_1%
560K_1%
VCCGT_FBRC
VCCGT_COMP_RC
VCCGT_COMP
VCCGT_VFB
VCCGT_CSSUMA
VCCGT_CSCOMPA
VCCGT_ISENSA2_R
VCCGT_CSREFA_RT
PR97 47.5K_1%
PR100 47.5K_1%
PR98 69.8K_1%
PR99 160K_1%
PR104 26.1K_1%
PR102 100_1%
PR79 470pF_X7R_50V
PC80 2.2nF_X7R_50V
PRT2 100K_+/-1% +/-1% R0402
+VCCGT
[14] VCCGT_SENSE
[14] VSSGT_SENSE
PR319 SHORT-PAD-4 0402_4Mil
PR96 PR101
PJP4 2SHORT PAD NOBOM
VCCGT_VSPA
VCCGT_VSNA
VCCGT_IOUT
VCCGT_VBOOT
VCCGT_ICCMAXA
VCCGT_ILIMA
VCCGT_CSREFA
VCCGT VBOOT SET 0V ADDR SET 01h
IMAX SET:51A
VRM_VRHOT
VRM_TSE
VRM_TSE_R
VRM_ROSC
NCP81203MNTXG
CCL=Y
PR109 PR110 10_1%
PC82 1nF_X7R_16V 0402
PR23 SHORT-PAD-4 0402_4Mil
[10,29] VR_HOT
PR106 51_1% 0402
+1P0V_VCCST
PR105 34K_1% 0402
PC81 470pF_X7R_50V 0402
PR107 10K_1% 0402
PR108 40.2K_1% 0402
PR111 5.49K_1% 0402
PR113 20K_1% 0402
PR114 8.25K_1% 0402
PRT3 100K_+/-1% +/-1% R0402
PC83 100nF_X7R_16V 0402
PR112 4.87K_1% 0402
PC84 100nF_X7R_16V 0402
PR115 8.25K_1% 0402
PRT4 100K_+/-1% +/-1% R0402
Freq=350KHz
+VCORE
[10] VCCSoket
[10] VSSSoket
PR318 SHORT-PAD-4 0402_4Mil
PJP2 2SHORT PAD NOBOM
PR69 PR72
PC60 PC61
1.5nF_X7R_50V
PR70 3.3K_1%
VRM_VSP
VRM_VSN
VRM_IOUT
PR61 560K_1%
PR63 47_1%
PR66 1K_1%
PC55 470pF_X7R_50V
PR64 4.02K_1%
PC52 2.2nF_X7R_50V
PC57 47pF_NPO_50V
VRM_FBRC
VRM_COMP_RC
VRM_COMP
VRM_VFB
Vinafix.com
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Power-4:+Vcore/+VGT
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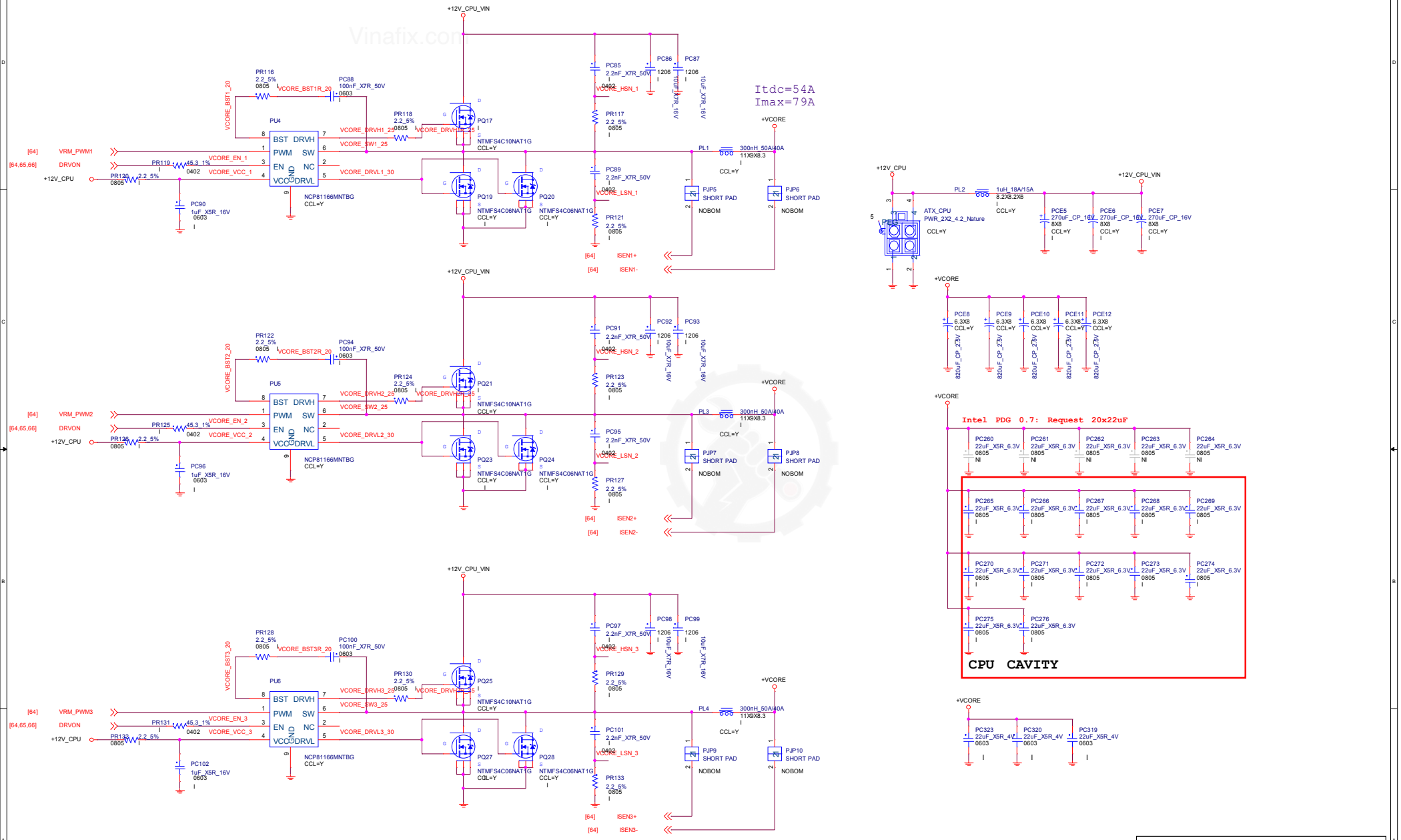
VCORE PHASE1~3



DELL INC.

Title

Power-5:+Vcore Driver

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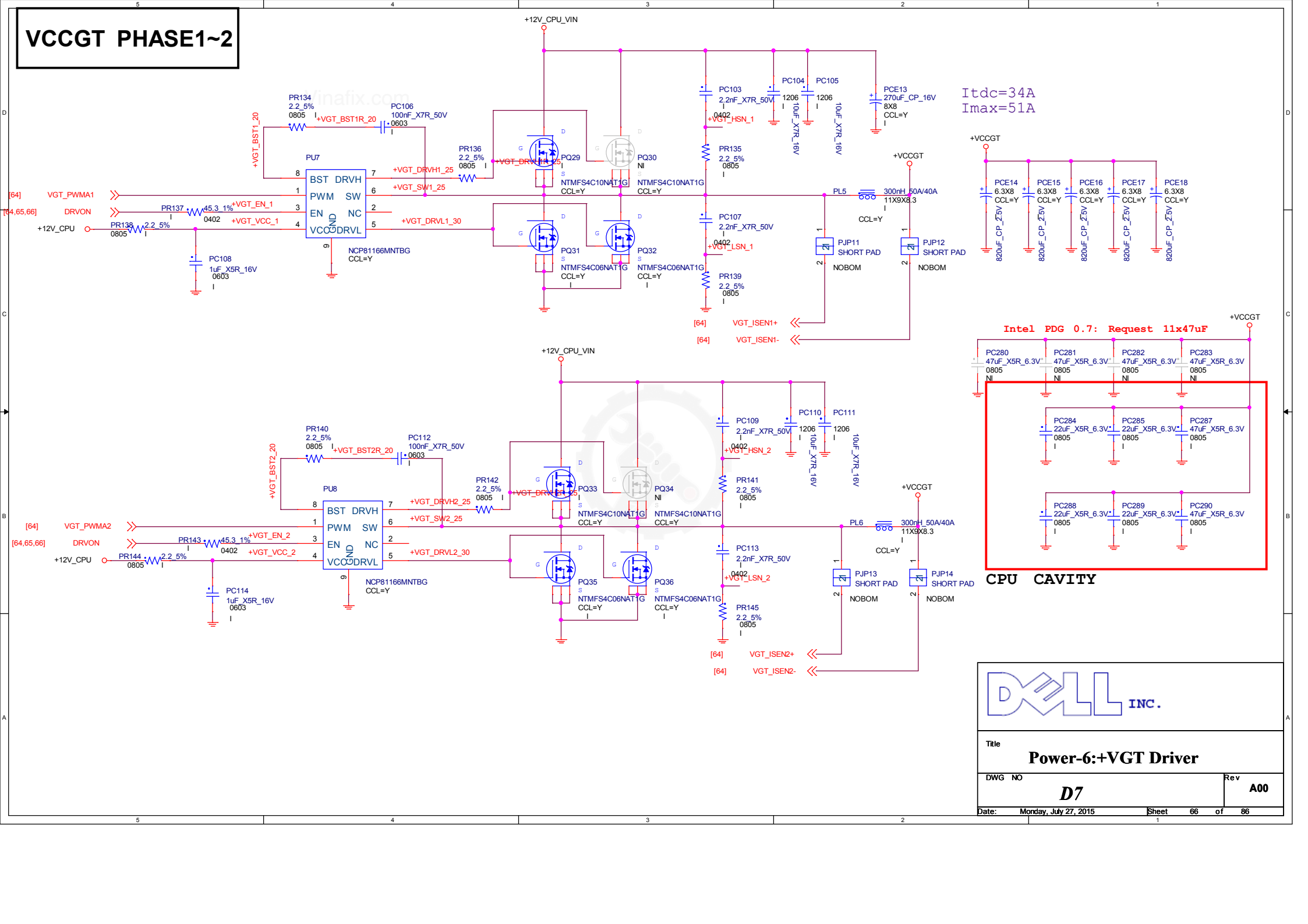
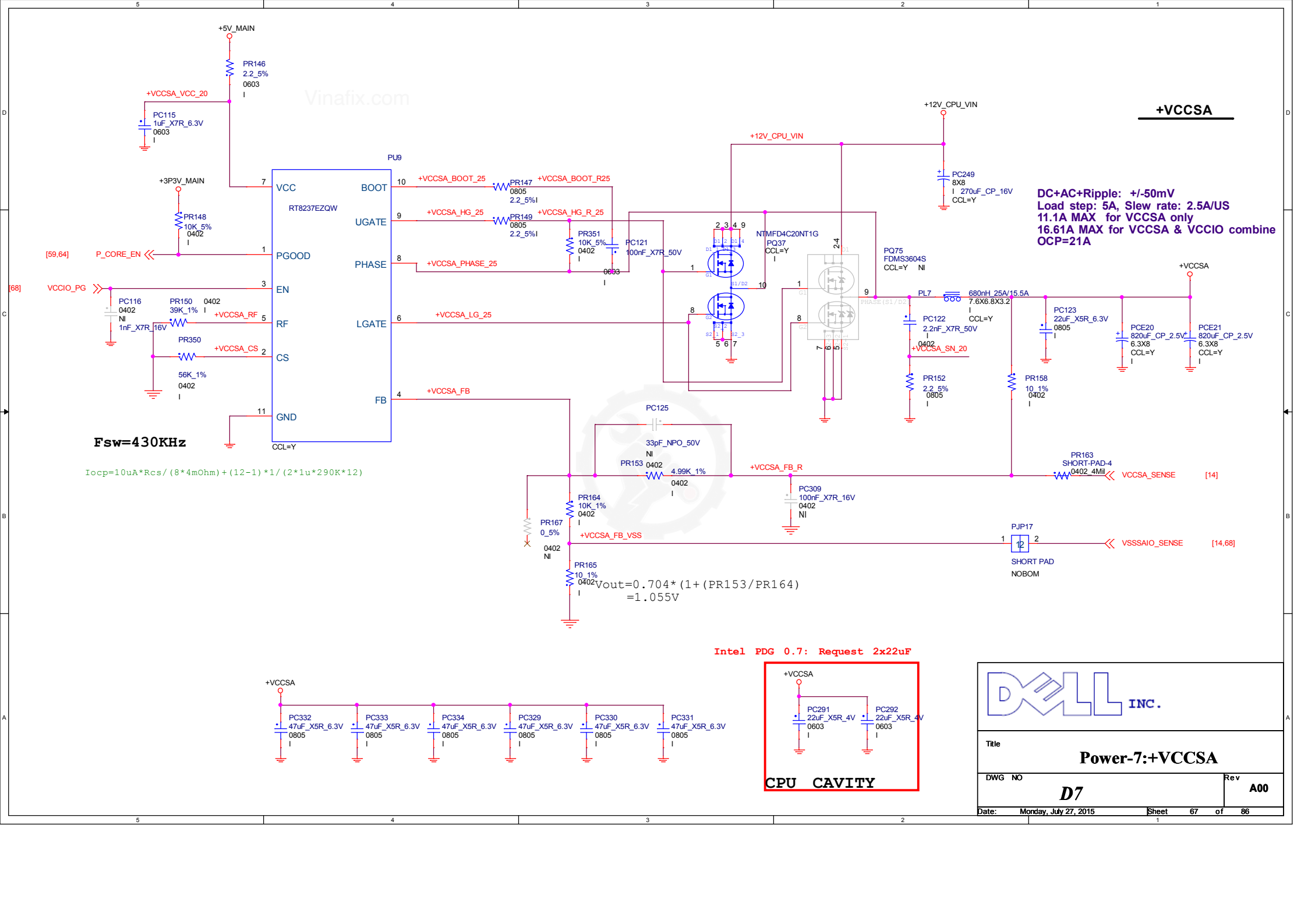
VCCGT PHASE1~2




+VCCSA
+5V_MAIN
PR146 2.2_5% 0603 I
+VCCSA_VCC_20
PC115 1uF_X7R_6.3V 0603 I
+3P3V_MAIN
PR148 10K_5% 0402 I
[59,64] P_CORE_EN
[68] VCCIO_PG
PC116 0402 NI 1nF_X7R_16V
PR150 39K_1% 0402 I
+VCCSA_RF
PR350 56K_1% 0402 I
+VCCSA_CS
PU9
RT8237EZQW
VCC
PGOOD
EN
RF
CS
GND
BOOT
UGATE
PHASE
LGATE
FB
CCL=Y
+VCCSA_BOOT_25
PR147 0805 2.2_5%I
+VCCSA_BOOT_R25
+VCCSA_HG_25
PR149 0805 2.2_5%I
+VCCSA_HG_R_25
PR351 10K_5% 0402 I
PC121 100nF_X7R_50V 0603 I
+VCCSA_PHASE_25
+VCCSA_LG_25
+VCCSA_FB
Fsw=430KHz
Iocp=10uA*Rcs/(8*4mOhm)+(12-1)*1/(2*1u*290K*12)
+12V_CPU_VIN
PC249 8X8 I 270uF_CP_16V CCL=Y
NTMFD4C20NT1G
PQ37 CCL=Y I
PQ75 FDMS3604S CCL=Y NI
PL7 680nH_25A/15.5A 7.6X6.8X3.2 I CCL=Y
PC122 2.2nF_X7R_50V I 0402
+VCCSA_SN_20
PR152 2.2_5% 0805 I
PR158 10_1% 0402 I
PC123 22uF_X5R_6.3V 0805 I
PCE20 820uF_CP_2.5V 6.3X8 CCL=Y I
PCE21 820uF_CP_2.5V 6.3X8 CCL=Y I
DC+AC+Ripple: +/-50mV
Load step: 5A, Slew rate: 2.5A/US
11.1A MAX for VCCSA only
16.61A MAX for VCCSA & VCCIO combine
OCP=21A
PC125 33pF_NPO_50V NI
PR153 0402 4.99K_1%
+VCCSA_FB_R
PR163 SHORT-PAD-4 0402_4Mil
VCCSA_SENSE [14]
PC309 100nF_X7R_16V 0402 NI
PR164 10K_1% 0402 I
PR167 0_5% 0402 NI
+VCCSA_FB_VSS
PR165 10_1% 0402 I
Vout=0.704*(1+(PR153/PR164)
=1.055V
PJP17
SHORT PAD
NOBOM
VSSSAIO_SENSE [14,68]
Intel PDG 0.7: Request 2x22uF
PC332 47uF_X5R_6.3V 0805 I
PC333 47uF_X5R_6.3V 0805 I
PC334 47uF_X5R_6.3V 0805 I
PC329 47uF_X5R_6.3V 0805 I
PC330 47uF_X5R_6.3V 0805 I
PC331 47uF_X5R_6.3V 0805 I
PC291 22uF_X5R_4V 0603 I
PC292 22uF_X5R_4V 0603 I
CPU CAVITY
DELL INC.
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Power-7:+VCCSA
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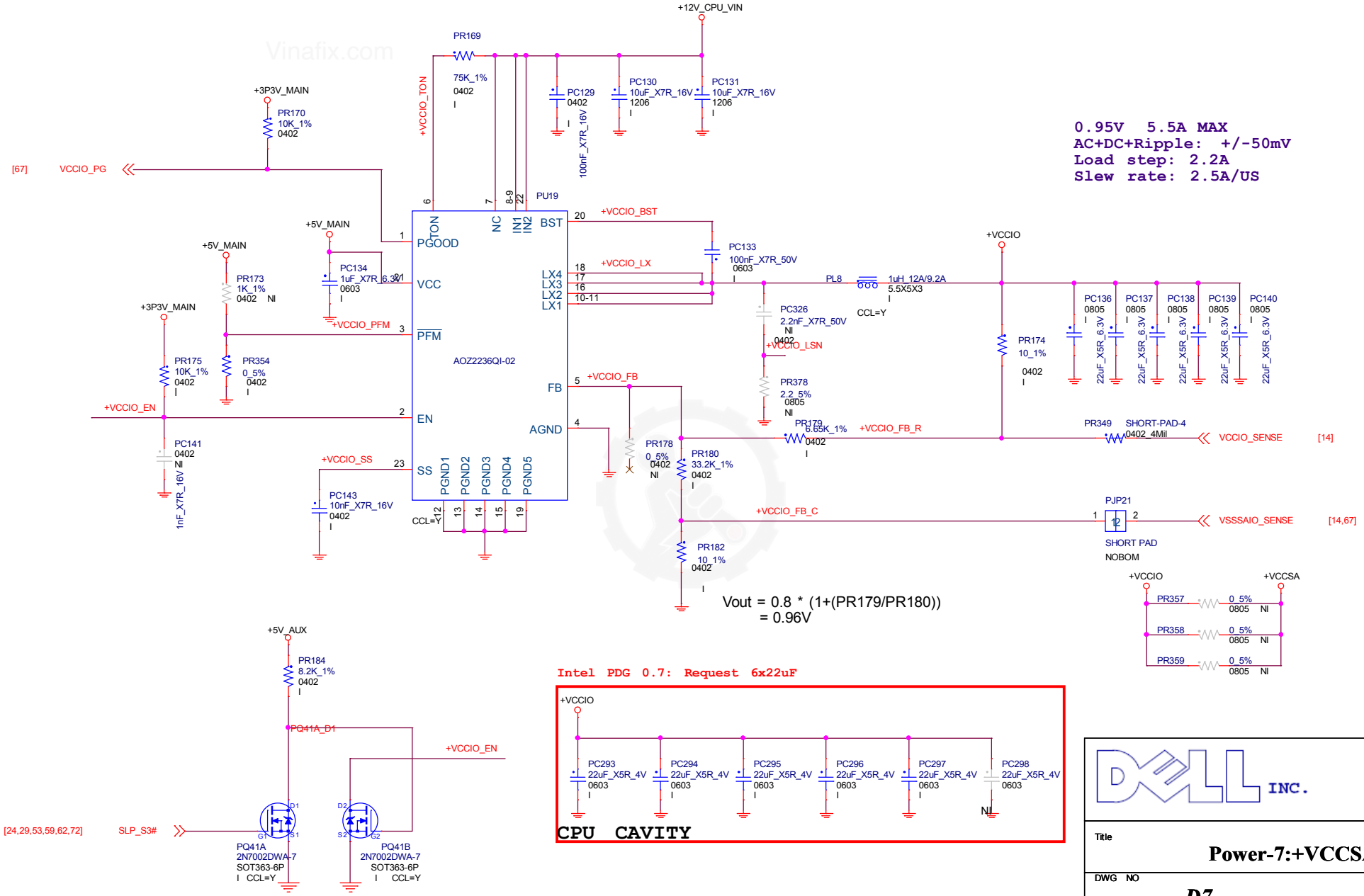
+VCCIO

Fsw(KHz)=38000*Vout/Rton(Kohm)=450KHz



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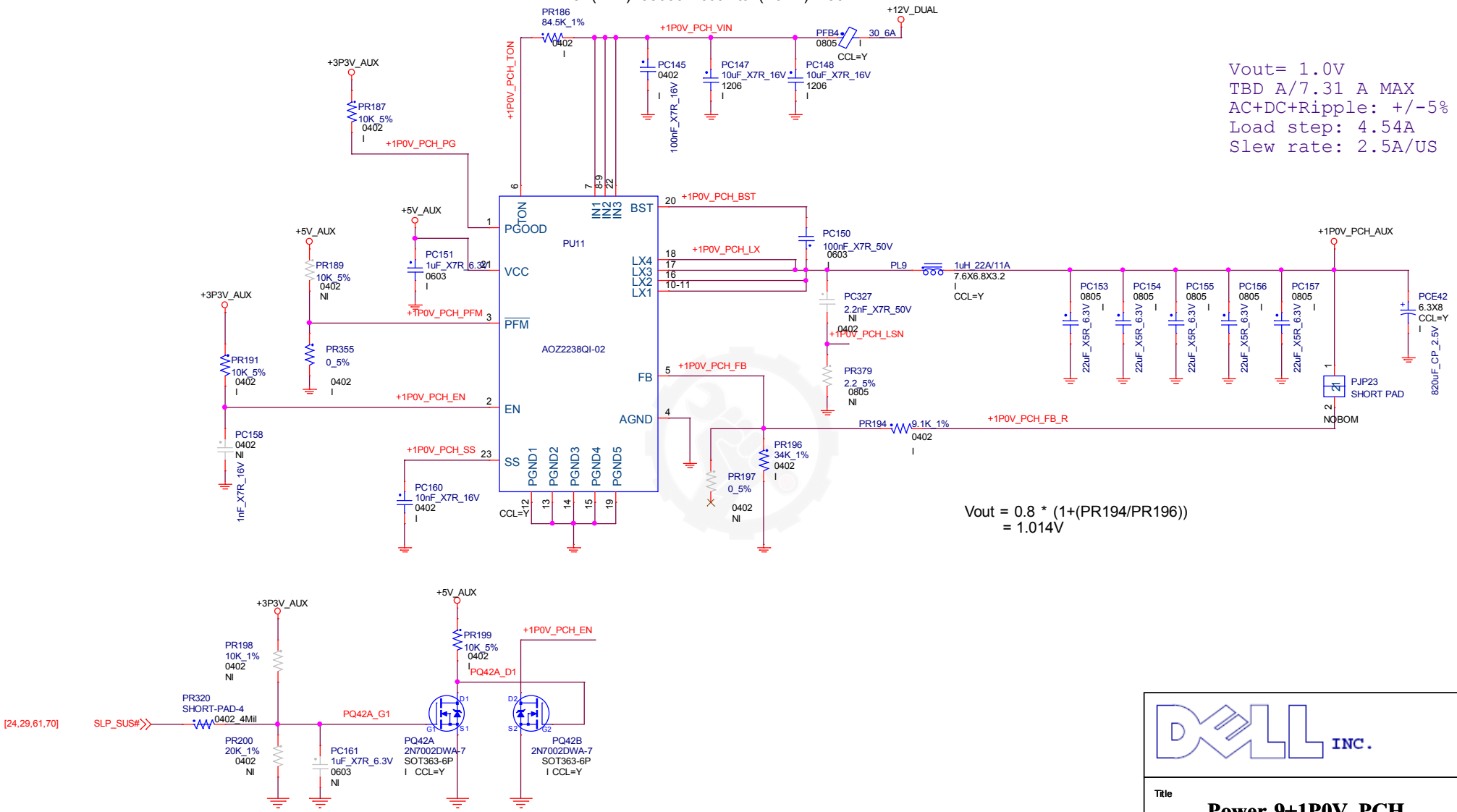
+1P0V_PCH_AUX

Fsw(KHz)=38000*Vout/Rton(Kohm)=450KHz



Vout= 1.0V
TBD A/7.31 A MAX
AC+DC+Ripple: +/-5%
Load step: 4.54A
Slew rate: 2.5A/US

DELL INC.

Title: **Power-9+1P0V_PCH**

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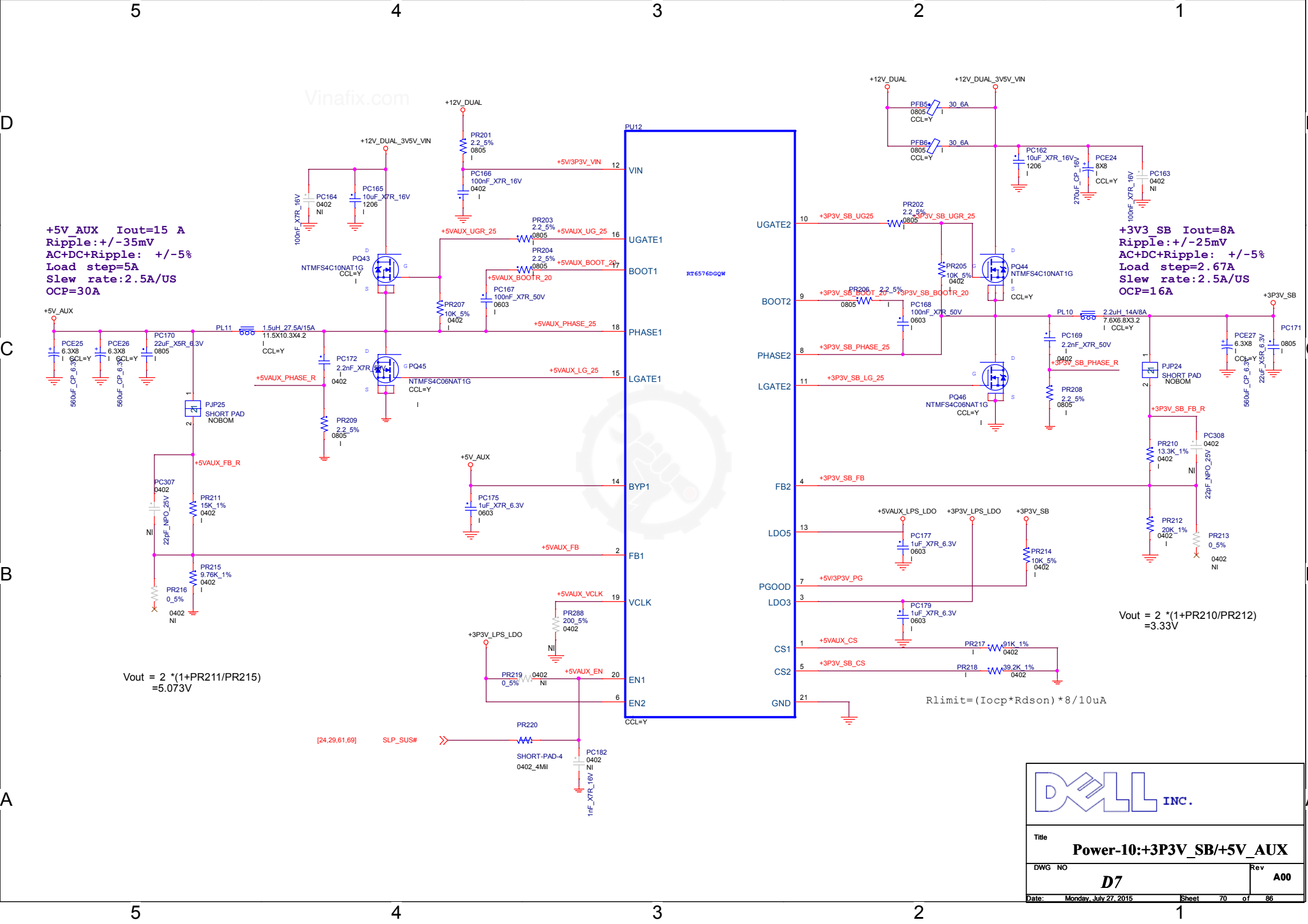
+5V_AUX Iout=15 A
Ripple:+/-35mV
AC+DC+Ripple: +/-5%
Load step=5A
Slew rate:2.5A/US
OCP=30A
Vout = 2 *(1+PR211/PR215)
=5.073V
+3V3_SB Iout=8A
Ripple:+/-25mV
AC+DC+Ripple: +/-5%
Load step=2.67A
Slew rate:2.5A/US
OCP=16A
Vout = 2 *(1+PR210/PR212)
=3.33V
Rlimit=(Iocp*Rdson)*8/10uA
PU12
RT6576DGQW
VIN
UGATE1
BOOT1
PHASE1
LGATE1
BYP1
FB1
VCLK
EN1
EN2
UGATE2
BOOT2
PHASE2
LGATE2
FB2
LDO5
PGOOD
LDO3
CS1
CS2
GND
PQ43 NTMFS4C10NAT1G
PQ44 NTMFS4C10NAT1G
PQ45 NTMFS4C06NAT1G
PQ46 NTMFS4C06NAT1G
PL11 1.5uH_27.5A/15A 11.5X10.3X4.2
PL10 2.2uH_14A/8A 7.6X6.8X3.2
PJP25 SHORT PAD NOBOM
PJP24 SHORT PAD NOBOM
SHORT-PAD-4 0402_4Mil
[24,29,61,69] SLP_SUS#
+12V_DUAL
+12V_DUAL_3V5V_VIN
+5V_AUX
+5V/3P3V_VIN
+5VAUX_UGR_25
+5VAUX_UG_25
+5VAUX_BOOT_20
+5VAUX_BOOTR_20
+5VAUX_PHASE_25
+5VAUX_PHASE_R
+5VAUX_LG_25
+5VAUX_FB_R
+5VAUX_FB
+5VAUX_VCLK
+5VAUX_EN
+3P3V_LPS_LDO
+3P3V_SB
+3P3V_SB_UG25
+3P3V_SB_UGR_25
+3P3V_SB_BOOT_20
+3P3V_SB_BOOTR_20
+3P3V_SB_PHASE_25
+3P3V_SB_PHASE_R
+3P3V_SB_LG_25
+3P3V_SB_FB
+3P3V_SB_FB_R
+5V/3P3V_PG
+5VAUX_CS
+3P3V_SB_CS
PR201 2.2_5% 0805
PR202 2.2_5% 0805
PR203 2.2_5% 0805
PR204 2.2_5% 0805
PR205 10K_5% 0402
PR206 2.2_5% 0805
PR207 10K_5% 0402
PR208 2.2_5% 0805
PR209 2.2_5% 0805
PR210 13.3K_1% 0402
PR211 15K_1% 0402
PR212 20K_1% 0402
PR213 0_5% 0402 NI
PR214 10K_5% 0402
PR215 9.76K_1% 0402
PR216 0_5% 0402 NI
PR217 91K_1% 0402
PR218 39.2K_1% 0402
PR219 0_5% 0402 NI
PR220
PR288 200_5% 0402 NI
PFB5 0805 CCL=Y 30_6A
PFB6 0805 CCL=Y 30_6A
PC162 10uF_X7R_16V 1206
PC163 0402 NI
PCE24 8X8 CCL=Y 270uF_CP_16V
PC164 0402 NI 100nF_X7R_16V
PC165 10uF_X7R_16V 1206
PC166 100nF_X7R_16V 0402
PC167 100nF_X7R_50V 0603
PC168 100nF_X7R_50V 0603
PC169 2.2nF_X7R_50V 0402
PC170 22uF_X5R_6.3V 0805
PC171 0805 22uF_X5R_6.3V
PC172 2.2nF_X7R_50V 0402
PC175 1uF_X7R_6.3V 0603
PC177 1uF_X7R_6.3V 0603
PC179 1uF_X7R_6.3V 0603
PC182 0402 NI 1nF_X7R_16V
PC307 0402 NI 22pF_NPO_25V
PC308 0402 NI 22pF_NPO_25V
PCE25 6.3X8 CCL=Y 560uF_CP_6.3V
PCE26 6.3X8 CCL=Y 560uF_CP_6.3V
PCE27 6.3X8 CCL=Y 560uF_CP_6.3V
Title
Power-10:+3P3V_SB/+5V_AUX
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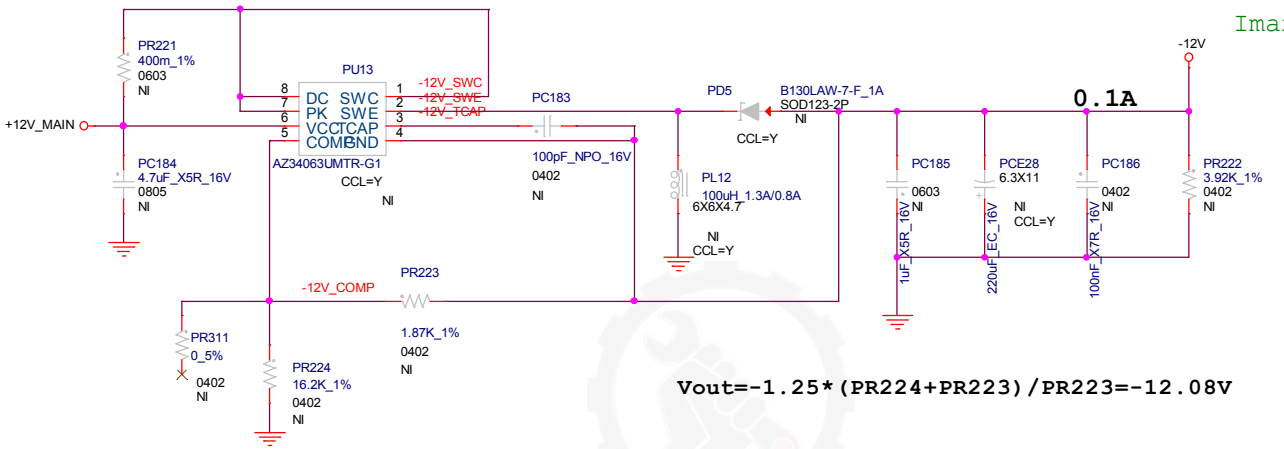

DELL INC.

Title

Power-11:-12V

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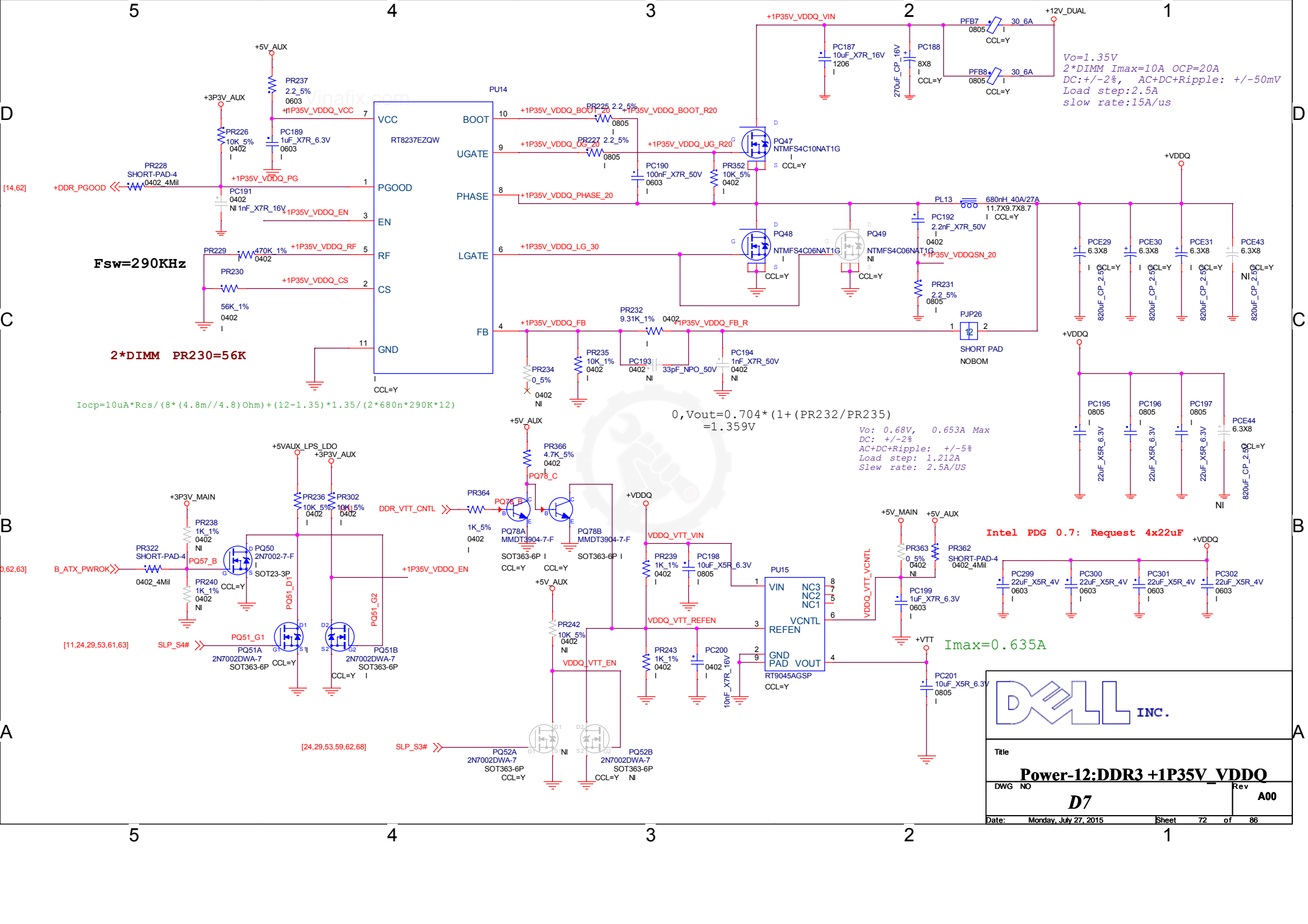
+5V_AUX
+3P3V_AUX
PR237 2.2_5% 0603
PR226 10K_5% 0402
PC189 1uF_X7R_6.3V 0603
+1P35V_VDDQ_VCC
PU14
RT8237EZQW
VCC
BOOT
UGATE
PHASE
LGATE
PGOOD
EN
RF
CS
FB
GND
PR228 SHORT-PAD-4 0402_4Mil
+DDR_PGOOD
[14,62]
+1P35V_VDDQ_PG
PC191 0402 NI 1nF_X7R_16V
+1P35V_VDDQ_EN
PR229 470K_1% 0402
PR230 56K_1% 0402
+1P35V_VDDQ_RF
+1P35V_VDDQ_CS
Fsw=290KHz
2*DIMM PR230=56K
Iocp=10uA*Rcs/(8*(4.8m//4.8)Ohm)+(12-1.35)*1.35/(2*680n*290K*12)
+1P35V_VDDQ_VIN
PC187 10uF_X7R_16V 1206
PC188 270uF_CP_16V 8X8 CCL=Y
PFB7 0805 30_6A CCL=Y
PFB8 0805 30_6A CCL=Y
+12V_DUAL
Vo=1.35V
2*DIMM Imax=10A OCP=20A
DC:+/-2%, AC+DC+Ripple: +/-50mV
Load step:2.5A
slow rate:15A/us
PR225 2.2_5% 0805
PR227 2.2_5% 0805
+1P35V_VDDQ_BOOT_20
+1P35V_VDDQ_BOOT_R20
+1P35V_VDDQ_UG_20
+1P35V_VDDQ_UG_R20
PQ47 NTMFS4C10NAT1G CCL=Y
PC190 100nF_X7R_50V 0603
PR352 10K_5% 0402
+1P35V_VDDQ_PHASE_20
PQ48 NTMFS4C06NAT1G NI CCL=Y
PQ49 NTMFS4C06NAT1G NI CCL=Y
+1P35V_VDDQ_LG_30
PL13 680nH_40A/27A 11.7X9.7X8.7 CCL=Y
PC192 2.2nF_X7R_50V 0402
+1P35V_VDDQSN_20
PR231 2.2_5% 0805
PJP26 SHORT PAD NOBOM
+VDDQ
PCE29 6.3X8 820uF_CP_2.5
PCE30 6.3X8 820uF_CP_2.5
PCE31 6.3X8 820uF_CP_2.5
PCE43 6.3X8 NI 820uF_CP_2.5
PR232 9.31K_1% 0402
PR234 0_5% 0402 NI
PR235 10K_1% 0402
PC193 0402 NI 33pF_NPO_50V
PC194 1nF_X7R_50V 0402 NI
+1P35V_VDDQ_FB
+1P35V_VDDQ_FB_R
0,Vout=0.704*(1+(PR232/PR235)
=1.359V
Vo: 0.68V, 0.653A Max
DC: +/-2%
AC+DC+Ripple: +/-5%
Load step: 1.212A
Slew rate: 2.5A/US
PC195 0805 22uF_X5R_6.3V
PC196 0805 22uF_X5R_6.3V
PC197 0805 22uF_X5R_6.3V
PCE44 6.3X8 NI 820uF_CP_2.5
+5VAUX_LPS_LDO
+3P3V_MAIN
PR236 10K_5% 0402
PR302 10K_5% 0402
PR238 1K_1% 0402 NI
PR322 SHORT-PAD-4
PR240 1K_1% 0402 NI
PQ50 2N7002-7-F SOT23-3P
PQ57_B
B_ATX_PWROK
[10,62,63]
0402_4Mil
CCL=Y
PQ51_D1
PQ51_G2
PQ51_G1
SLP_S4#
[11,24,29,53,61,63]
PQ51A 2N7002DWA-7 SOT363-6P
PQ51B 2N7002DWA-7 SOT363-6P
+1P35V_VDDQ_EN
PR364 1K_5% 0402
DDR_VTT_CNTL
PR366 4.7K_5% 0402
PQ78_C
PQ78A MMDT3904-7-F SOT363-6P
PQ78B MMDT3904-7-F SOT363-6P
+VDDQ
VDDQ_VTT_VIN
PR239 1K_1% 0402
PC198 10uF_X5R_6.3V 0805
PR242 10K_5% 0402 NI
VDDQ_VTT_REFEN
VDDQ_VTT_EN
PR243 1K_1% 0402
PC200 0402 10nF_X7R_16V
PU15
RT9045AGSP
VIN
NC3
NC2
NC1
VCNTL
REFEN
GND PAD
VOUT
VDDQ_VTT_VCNTL
PR363 0_5% 0402 NI
PR362 SHORT-PAD-4 0402_4Mil
PC199 1uF_X7R_6.3V 0603
+VTT
Imax=0.635A
PC201 10uF_X5R_6.3V 0805
Intel PDG 0.7: Request 4x22uF
PC299 22uF_X5R_4V 0603
PC300 22uF_X5R_4V 0603
PC301 22uF_X5R_4V 0603
PC302 22uF_X5R_4V 0603
[24,29,53,59,62,68]
SLP_S3#
PQ52A 2N7002DWA-7 SOT363-6P
PQ52B 2N7002DWA-7 SOT363-6P
DELL INC.
Title
Power-12:DDR3 +1P35V_VDDQ
DWG NO
D7
Rev
A00
Date: Monday, July 27, 2015
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Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title

CPU

DWG NO	Rev
D7	A00

Date: Monday, July 27, 2015 Sheet 73 of 86

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title: **CPU**

DWG NO: ***D7***

Rev: **A00**

Date: Monday, July 27, 2015 Sheet 74 of 86

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title: **CPU**

DWG NO: ***D7***

Rev: **A00**

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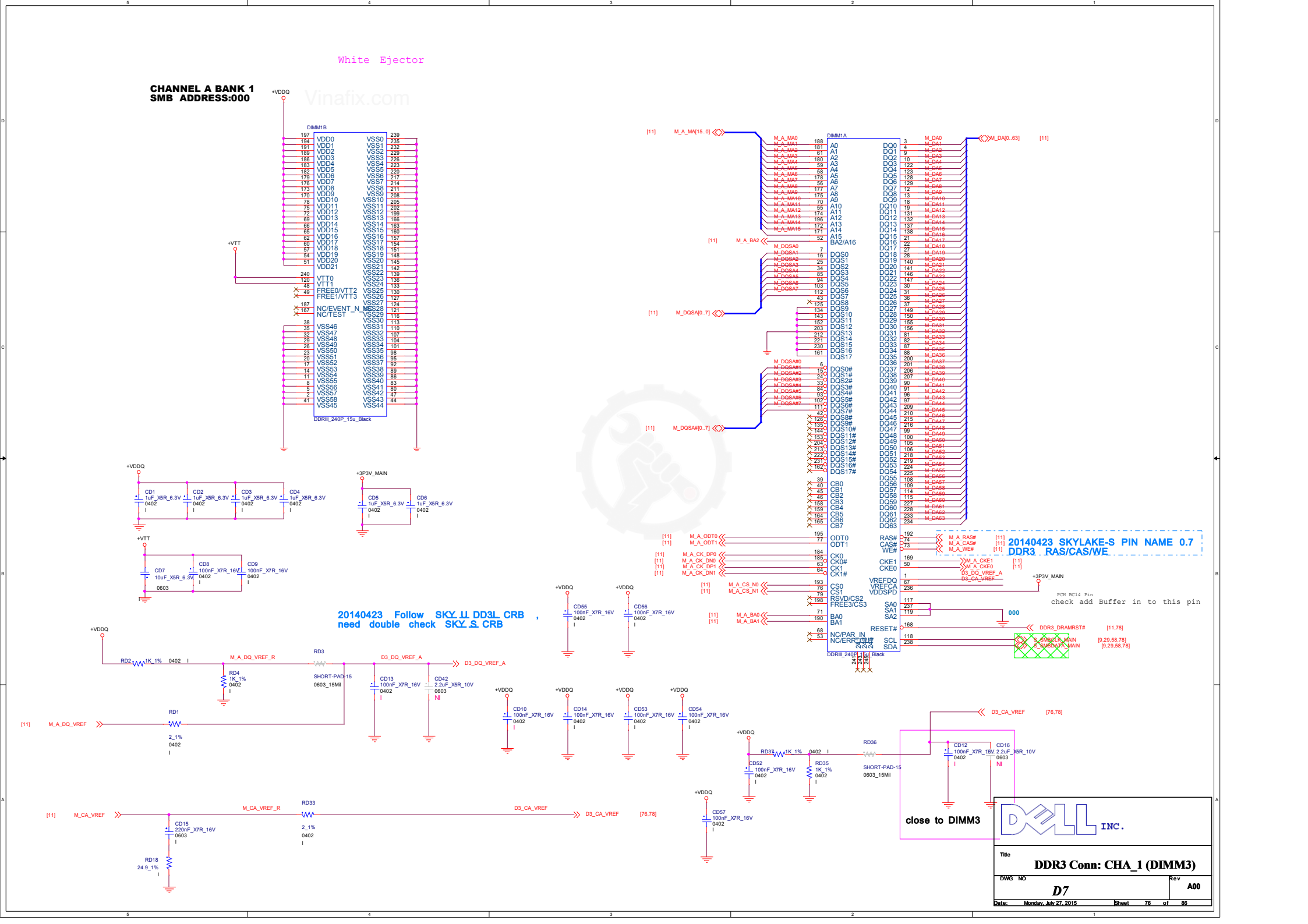
White Ejector

CHANNEL A BANK 1
SMB ADDRESS:000



Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title

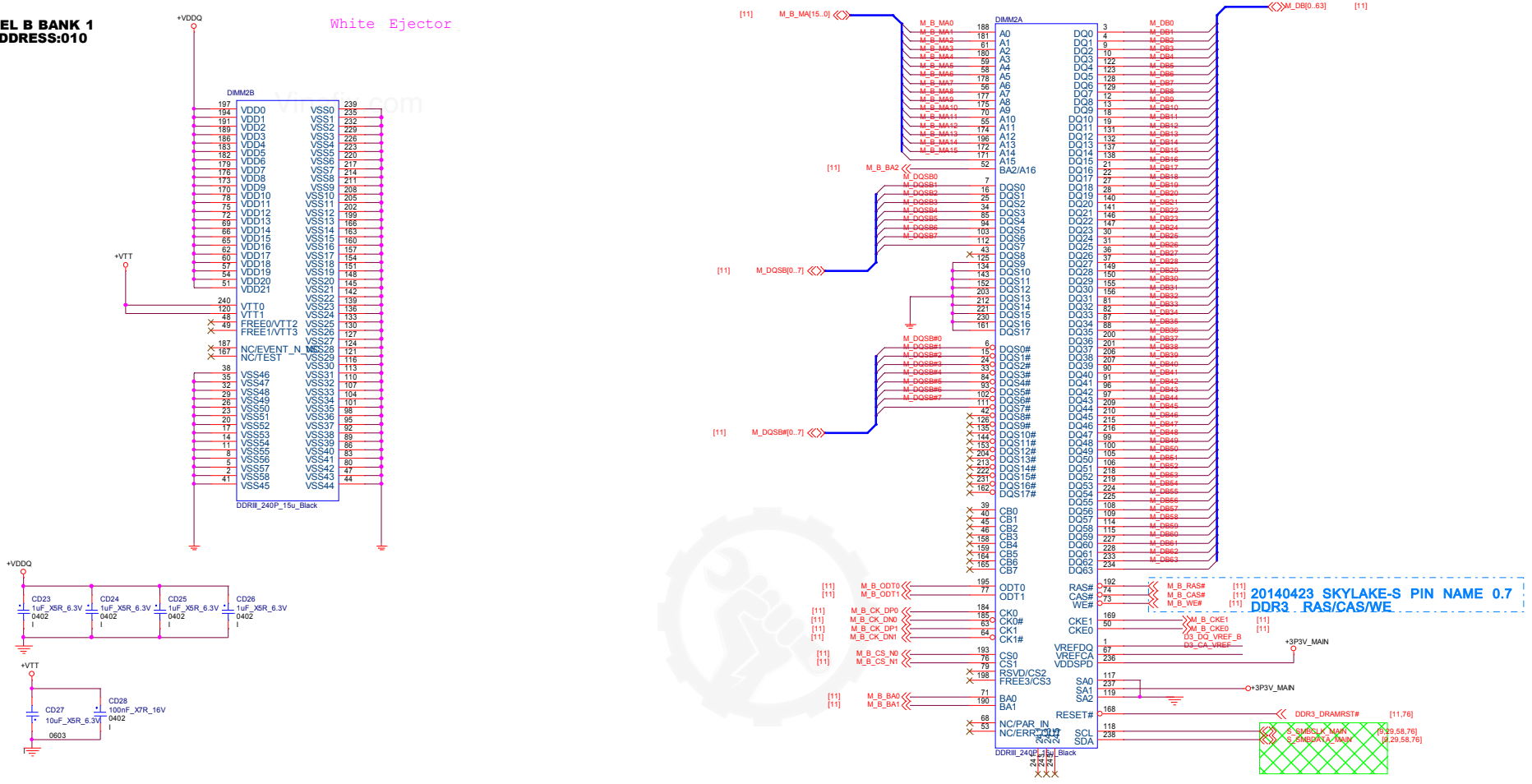
CPU

DWG NO	Rev
D7	A00

Date: Monday, July 27, 2015 Sheet 77 of 86

CHANNEL B BANK 1
SMB ADDRESS:010

White Ejector



Title	DDR3 Conn: CHB_1 (DIMM4)
DWG NO	D7
Rev	A00
Date:	Monday, July 27, 2015
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Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title

CPU

DWG NO

D7

Rev

A00

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Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

DELL INC.

Title

CPU

DWG NO

D7

Rev

A00

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SFF

USBPWR4_F_50

USB_F

U_USB10N_R 5 6 VBUS_2 D-_2

U_USB10P_R 7 8 D+_2 GND_2

USBPWR4_F_50

U_USB9N_R 1 2 VBUS_1 D-_1

U_USB9P_R 3 4 D+_1 GND_1

9 10 MT1 MT2 MT3 MT4 11 12

USBX2_15u_Black

+3P3V_AUX

RU2 10K_5% 0402 NI

IC on/off
Hi Lo
[23] Charge_power

+3P3V_AUX

RU1 10K_5% 0402 NI

GPIO
Hi : SDP, CDP
Lo :DCP, apple
[23] Charge_CTL3

PCH_OC#_6 R6576 8.2K_5% 0402 NI +3P3V_AUX

PCH_OC#_4 R6592 8.2K_5% 0402 I +3P3V_AUX

+5V_USB_F

FU6 3A_6V

USBPWR4_F_50

[23] PCH_OC#_6 RU97 0_5% I

[23] PCH_OC#_4 RU96 0_5% NI

RU91 10K_1% I

0805

CU17 100nF_X7R_16V 0402 I

RU90 15K_1% 0402 I

ECU16 470uF_FC_6.3V 6.3X11 I

CU18 100nF_X7R_16V 0402 I

20140505 ARD0.92: Each pair of USB ports will be current limited to 2.5A

[24] PCH_F_CHAR_CTL2 RU126 0_5% NI 0402

R28 10K_5% 0402 NI +3P3V_AUX

0402_4Mil

[21] USB_N10 [21] USB_P10 RU131 RU132 SHORT-PAD-4 0402_4Mil

U_USB10N_C U_USB10P_C

[21] USB_N9 [21] USB_P9

LU29 CMC_90_330mA

U_USB9N_R U_USB9P_R

RU88 0_5% NI

RU89 0_5% NI

U_USB10N_R U_USB10P_R

UU14 AZC199-04S.R7G_16KV

U_USB9P_R U_USB9N_R USBPWR4_F_50

U_USB10P_R U_USB10N_R

LU30 CMC_90_330mA

U_USB10P_C U_USB10N_C

NI 0_5% RU93

NI 0_5% RU92

SATA LED

O_FIO_SATA_LED#

CO47 0402 NI 470pF_X7R_50V

+3P3V_MAIN

RNO5 8.2K_5% 0804 I

O_FIO_SATA_LED#

SATA_LED#

OQ14_C

[23,52] SATA_LED#

QO9A MMDT3904-7-F

O_FIO_SATA_LED#

OQ14_C

MMDT3904-7-F QO9B

HDD_LED LED_White 4.3X8.35X15 I

+3P3V_MAIN

RO103 1K_1% 0603 I

HDD_LED_COVER

[83] O_FIO_SATA_LED#

O_FIO_SATA_LED#

POWER SWITCH Header

20120521: Add QO12, QO14, RN04, RO84, RO86 for Power LED control

If stuffed RO84, RO86 ; Dummy QO12, QO14, RNO4

[29,81] O_GREEN# O_GREEN#

O_GREEN# O_GREEN#_R

QO10A MMDT3904-7-F

MMDT3904-7-F QO10B

O_GREEN#_CTL

[29,81] O_YELLOW# O_YELLOW#

O_YELLOW# O_YELLOW#_R

QO11A MMDT3904-7-F

MMDT3904-7-F QO11B

O_YELLOW#_CTL

+5V_AUX

RNO6 1K_5% 1206 I

O_GREEN# O_GREEN#_CTL O_YELLOW# O_YELLOW#_CTL

[9,24,29,53] PWRBTN_OUT# [29,81] O_GREEN#

RO93 RO94 100_5% 0_5% NI

O_GREEN#_R

+5V_AUX RO95 1K_1% 0603 I

+5V_AUX RO96 1K_1% 0603 I

PWR_SW Header_2X3_K5_GF_Black

O_YELLOW#_R

RO97 0_5% NI

O_FP_CBL_DET# O_YELLOW# [22] [29,81]

+3P3V_AUX RO92 8.2K_5% 0402 I

O_FP_CBL_DET# O_GREEN# O_YELLOW# PWRBTN_OUT#

CO48 CO49 CO50 470pF_X7R_50V 0402

NI NI

DELL INC.

Title: Front_Panel

DWG NO: D7

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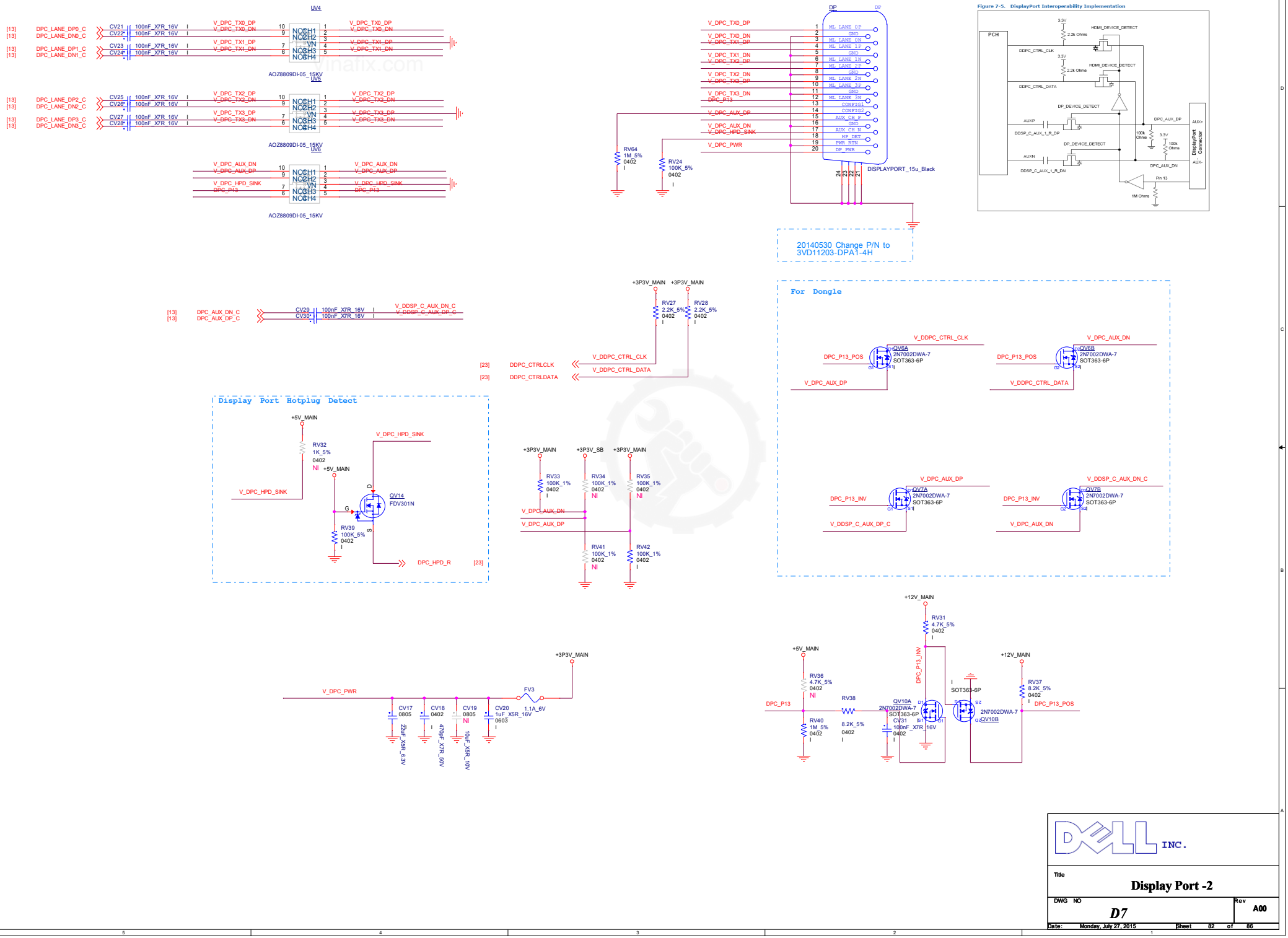
DP2 --> Port C



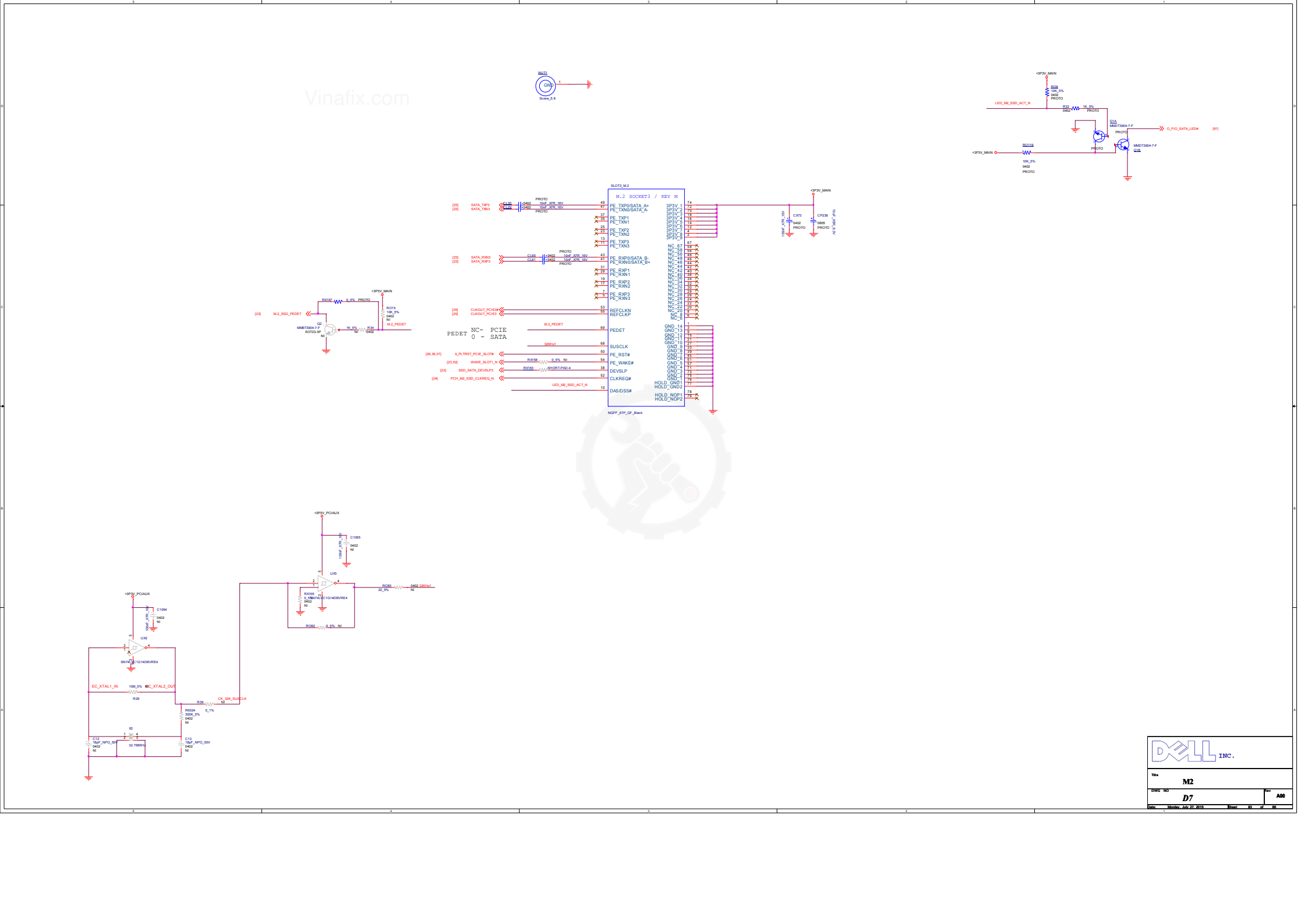
DELL INC.

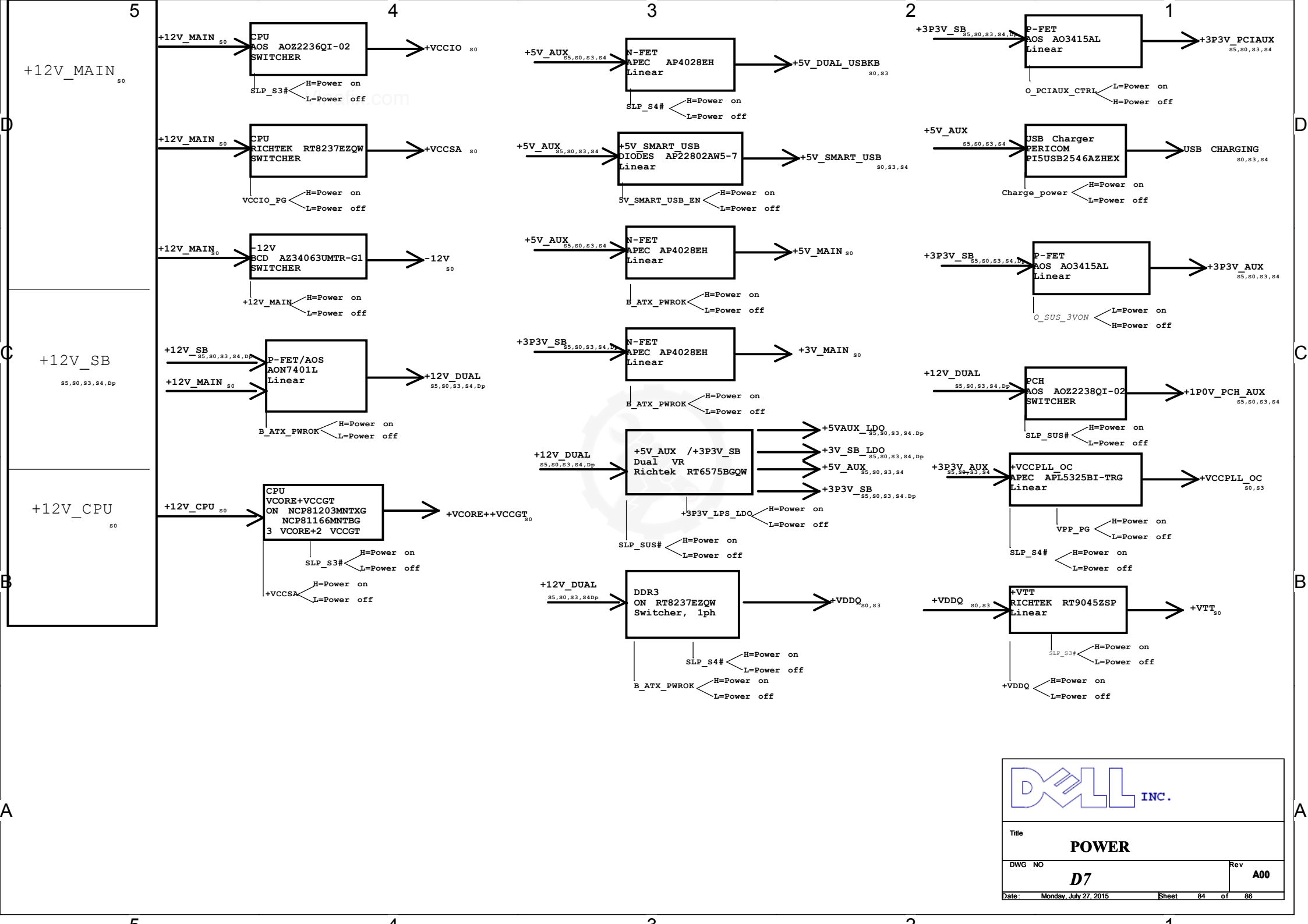
Title: **Display Port -2**

DWG NO: *D7*

Rev: A00

Date: Monday, July 27, 2015 Sheet 82 of 86


Vinafix.com
NUT1
GND
Screw_5.8
SLOT3_M.2
M.2 SOCKET3 / KEY M
NGFF_67P_GF_Black
PEDET NC- PCIE
0 - SATA
+3P3V_MAIN
+3P3V_PCIAUX
LED_M2_SSD_ACT_N
Q_FIO_SATA_LED#
MMDT3904-7-F
SN74LVC1G14DBVRE4
EC_XTAL1_IN
EC_XTAL2_OUT
CK_32K_SUSCLK
32.768KHz
INC.
M2
D7
A00
Monday, July 27, 2015


+12V_MAIN S0
+12V_SB S5,S0,S3,S4,Dp
+12V_CPU S0
+12V_MAIN S0
CPU
AOS AOZ2236QI-02
SWITCHER
+VCCIO S0
SLP_S3#
H=Power on
L=Power off
+12V_MAIN S0
CPU
RICHTEK RT8237EZQW
SWITCHER
+VCCSA S0
VCCIO_PG
H=Power on
L=Power off
+12V_MAIN S0
-12V
BCD AZ34063UMTR-G1
SWITCHER
-12V S0
+12V_MAIN
H=Power on
L=Power off
+12V_SB S5,S0,S3,S4,Dp
+12V_MAIN S0
P-FET/AOS
AON7401L
Linear
+12V_DUAL S5,S0,S3,S4,Dp
B_ATX_PWROK
H=Power on
L=Power off
+12V_CPU S0
CPU
VCORE+VCCGT
ON NCP81203MNTXG
NCP81166MNTBG
3 VCORE+2 VCCGT
+VCORE++VCCGT S0
SLP_S3#
H=Power on
L=Power off
+VCCSA
H=Power on
L=Power off
+5V_AUX S5,S0,S3,S4
N-FET
APEC AP4028EH
Linear
+5V_DUAL_USBKB S0,S3
SLP_S4#
H=Power on
L=Power off
+5V_AUX S5,S0,S3,S4
+5V_SMART_USB
DIODES AP22802AW5-7
Linear
+5V_SMART_USB S0,S3,S4
5V_SMART_USB_EN
H=Power on
L=Power off
+5V_AUX S5,S0,S3,S4
N-FET
APEC AP4028EH
Linear
+5V_MAIN S0
B_ATX_PWROK
H=Power on
L=Power off
+3P3V_SB S5,S0,S3,S4,Dp
N-FET
APEC AP4028EH
Linear
+3V_MAIN S0
B_ATX_PWROK
H=Power on
L=Power off
+12V_DUAL S5,S0,S3,S4,Dp
+5V_AUX /+3P3V_SB
Dual VR
Richtek RT6575BGQW
+5VAUX_LDO S5,S0,S3,S4.Dp
+3V_SB_LDO S5,S0,S3,S4,Dp
+5V_AUX S5,S0,S3,S4
+3P3V_SB S5,S0,S3,S4.Dp
+3P3V_LPS_LDO
H=Power on
L=Power off
SLP_SUS#
H=Power on
L=Power off
+12V_DUAL S5,S0,S3,S4Dp
DDR3
ON RT8237EZQW
Switcher, 1ph
+VDDQ S0,S3
SLP_S4#
H=Power on
L=Power off
B_ATX_PWROK
H=Power on
L=Power off
+3P3V_SB S5,S0,S3,S4,Dp
P-FET
AOS AO3415AL
Linear
+3P3V_PCIAUX S5,S0,S3,S4
O_PCIAUX_CTRL
L=Power on
H=Power off
+5V_AUX S5,S0,S3,S4
USB Charger
PERICOM
PI5USB2546AZHEX
USB CHARGING S0,S3,S4
Charge_power
H=Power on
L=Power off
+3P3V_SB S5,S0,S3,S4,Dp
P-FET
AOS AO3415AL
Linear
+3P3V_AUX S5,S0,S3,S4
O_SUS_3VON
L=Power on
H=Power off
+12V_DUAL S5,S0,S3,S4,Dp
PCH
AOS AOZ2238QI-02
SWITCHER
+1P0V_PCH_AUX S5,S0,S3,S4
SLP_SUS#
H=Power on
L=Power off
+3P3V_AUX S5,S0,S3,S4
+VCCPLL_OC
APEC APL5325BI-TRG
Linear
+VCCPLL_OC S0,S3
VPP_PG
H=Power on
L=Power off
SLP_S4#
H=Power on
L=Power off
+VDDQ S0,S3
+VTT
RICHTEK RT9045ZSP
Linear
+VTT S0
SLP_S3#
H=Power on
L=Power off
+VDDQ
H=Power on
L=Power off
DELL INC.
Title
POWER
DWG NO
D7
Rev
A00
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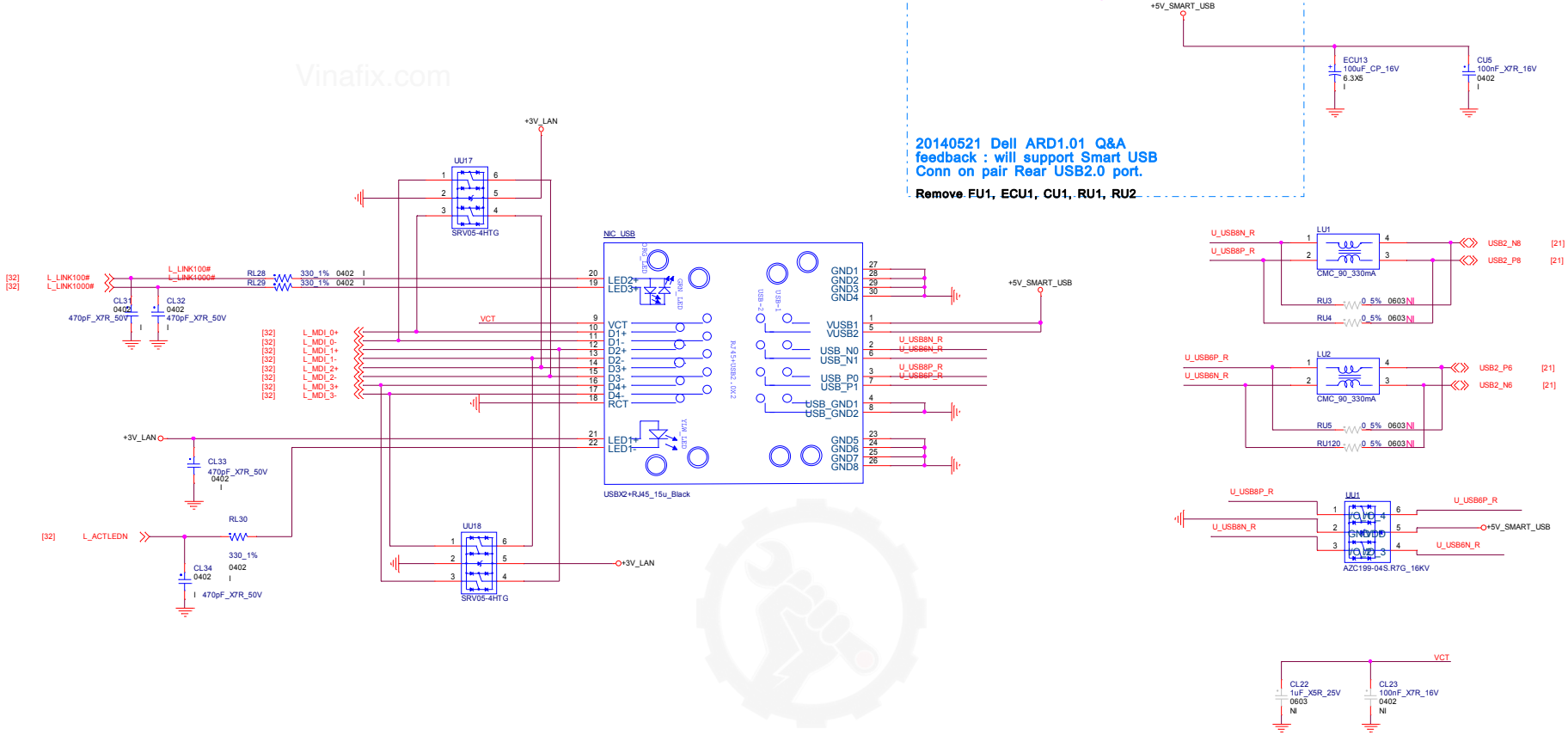
LAN CONNECTOR

20140509 ARD1.01: Support Smart Power On Conn
20140514 FU1 need change to 1.1A

20140521 Dell ARD1.01 Q&A feedback : will support Smart USB Conn on pair Rear USB2.0 port.

Remove FU1, ECU1, CU1, RU1, RU2



Title	LAN
DWG NO	D7
Rev	A00
Date:	Monday, July 27, 2015
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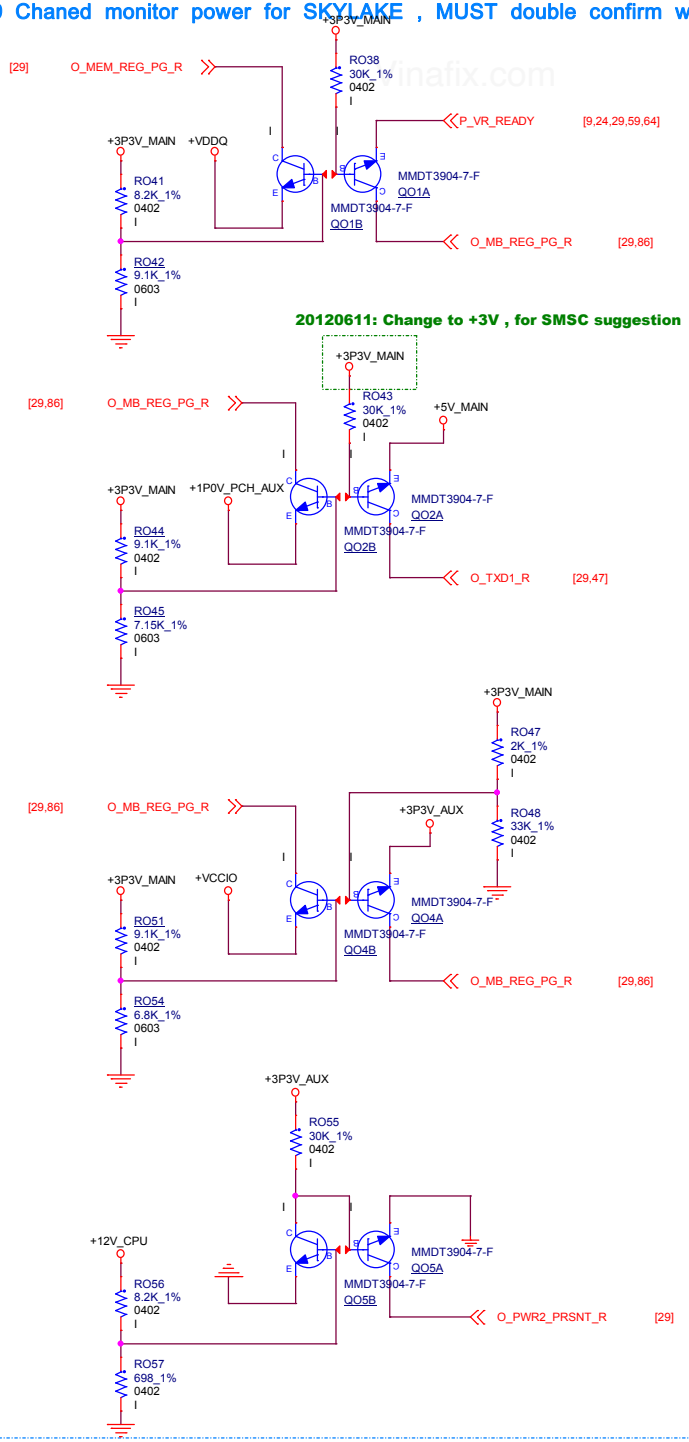
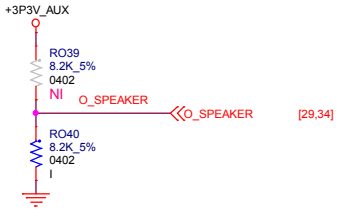
5555 PRE-POST DIAG Monitor

20140429 Chaned monitor power for SKYLAKE , MUST double confirm with SMSC



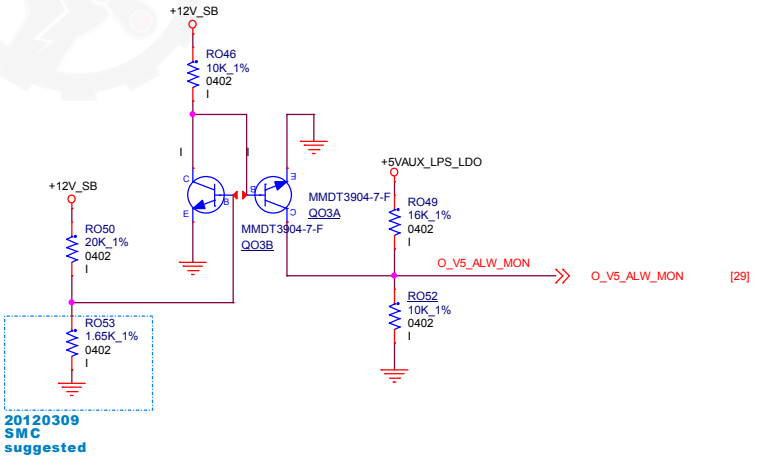
SIO STRAPING



SIO STRAPING

	SPEAKER	
	Diag_En	
PULL HIGH	**Disable**	
PULL LOW	**Enable**	

SIO5555 V5_ALW Monitor



DELL INC.

Title: **SIO**

DWG NO: ***D7***

Rev: **A00**

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