MS-14531 Ver : 0A

2009/07/07

Calpella Platform

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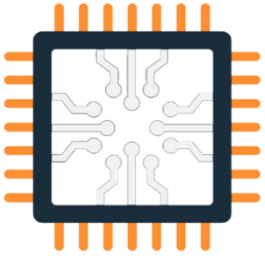

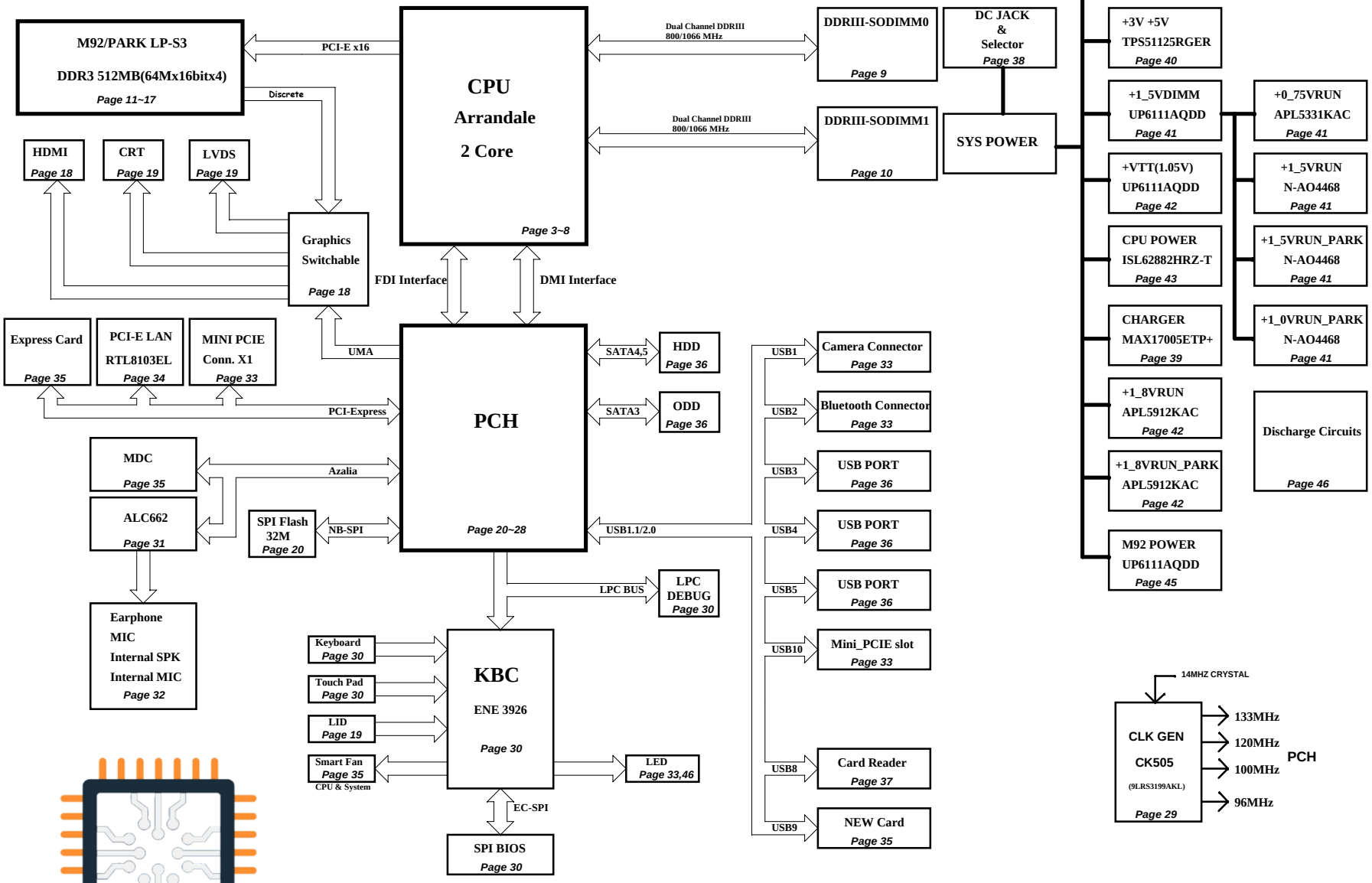

MICRO-STAR INT'L CO.,LTD.

Title: BLOCK DIAGRAM

Size: Custom | Document Number: MS-145X | Rev: 0A

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	LAN
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	DDRIII core
+1_5VRUN	1.5V	S0,S3	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDRIII command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC_GFXCORE	1.1V	S0	Graphics core rail (Dual Core only)
		S0	
M92S_VDD_CORE	0.95V	S0	GPU core power
+1_8VRUN_PARK	1.8V	S0	GPU PCIE power
+1_5VRUN_PARK	1.5V	S0	GPU DDR3 power
+1_0VRUN_PARK	1.0V	S0	GPU PCIE power
VDDR3	3.3V	S0	GPU I/O and DAC power

Net Naming Conventions

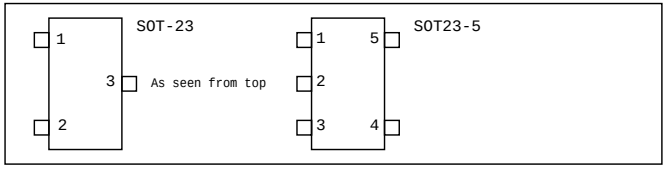
Suffix

\# = Active Low Signal

Prefix

H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

MICRO-STAR INT'L CO.,LTD.

Title: PLATFORM

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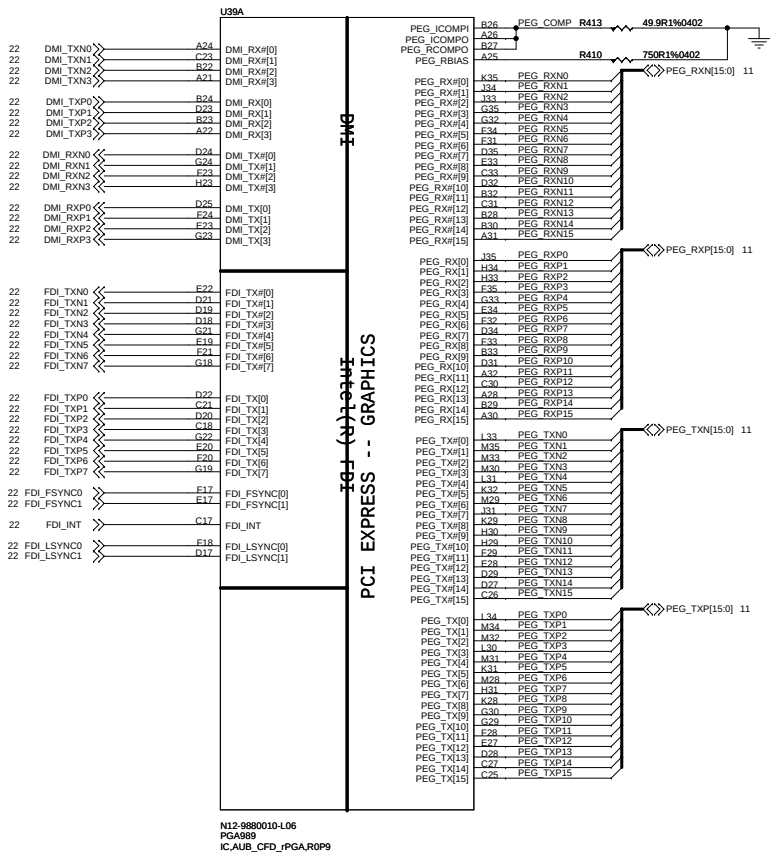
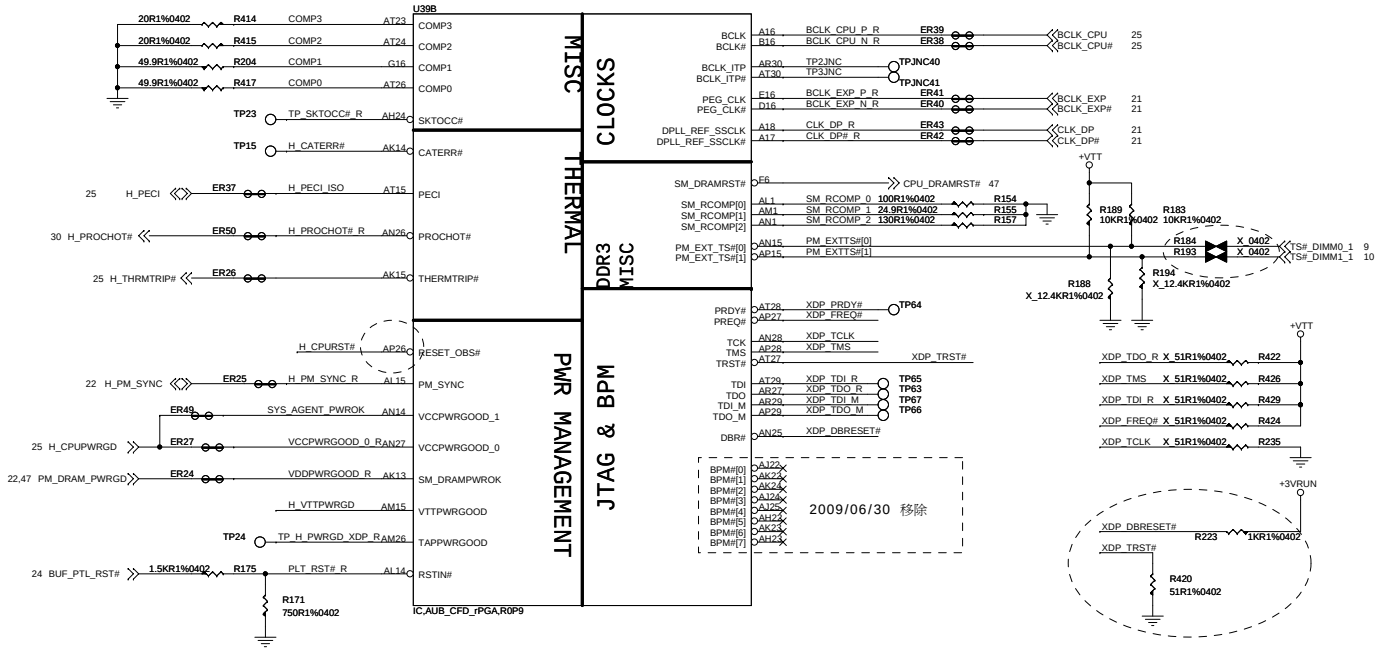
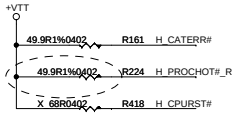
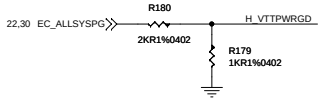
ARRANDALE PROCESSOR (CLK,MISC,JTAG)







2009/06/16 R224改50ohm



MICRO-STAR INT'L CO.,LTD.			
Title: PROCESSOR			
Size: Custom	Document Number: MS-145X		Rev: 0A
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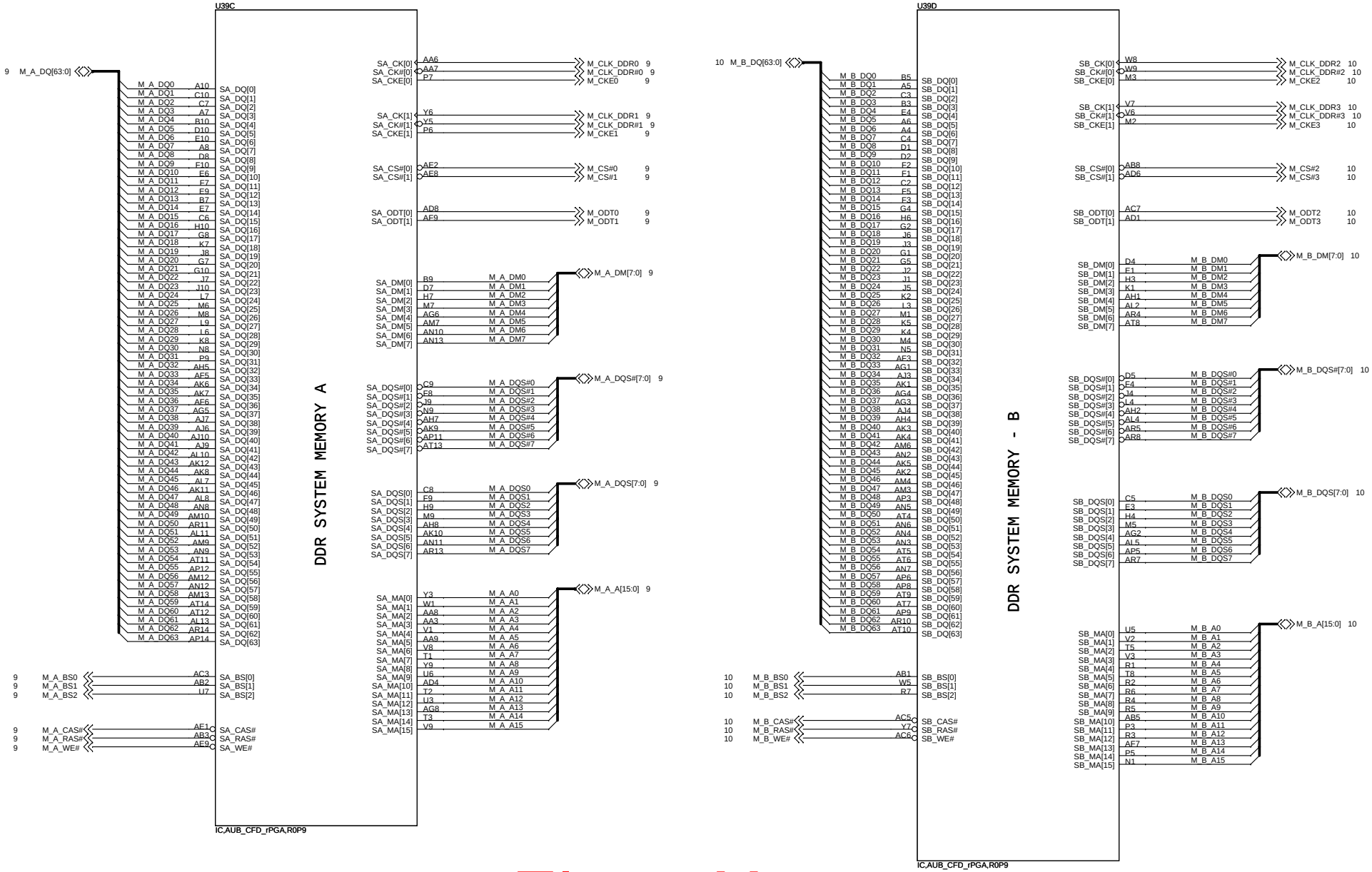
ARRANDALE PROCESSOR (DDR3)



MICRO-STAR INT'L CO.,LTD.

Title: DDR3

Size: Custom | Document Number: MS-145X | Rev: 0A

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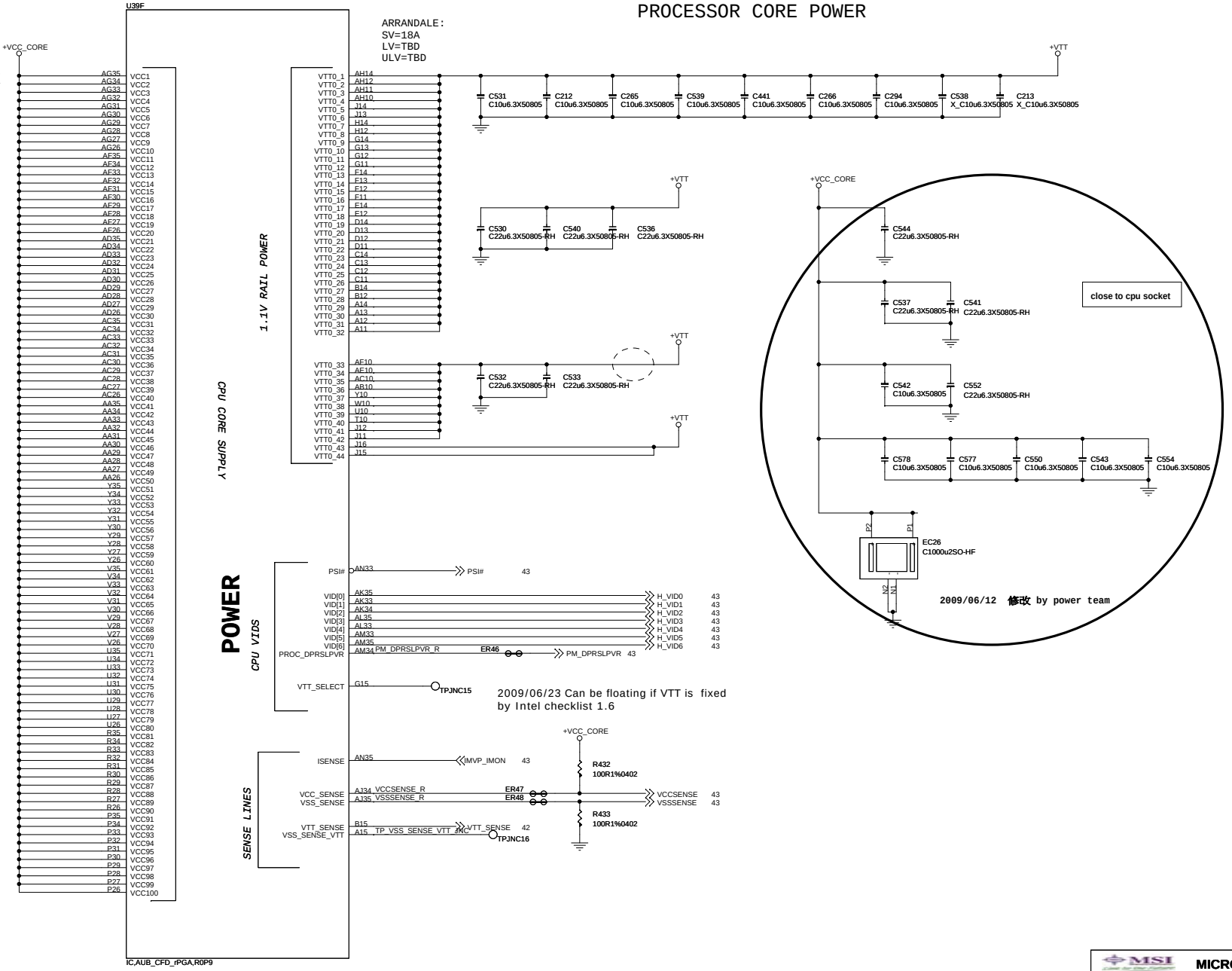
ARRANDALE PROCESSOR (POWER)

ARRANDALE:
SV=48A
LV=35A
ULV=27A

PROCESSOR CORE POWER

ARRANDALE:
SV=18A
LV=TBD
ULV=TBD

PROCESSOR CORE POWER



MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR POWER

Size: Custom | Document Number: MS-145X | Rev: 0A

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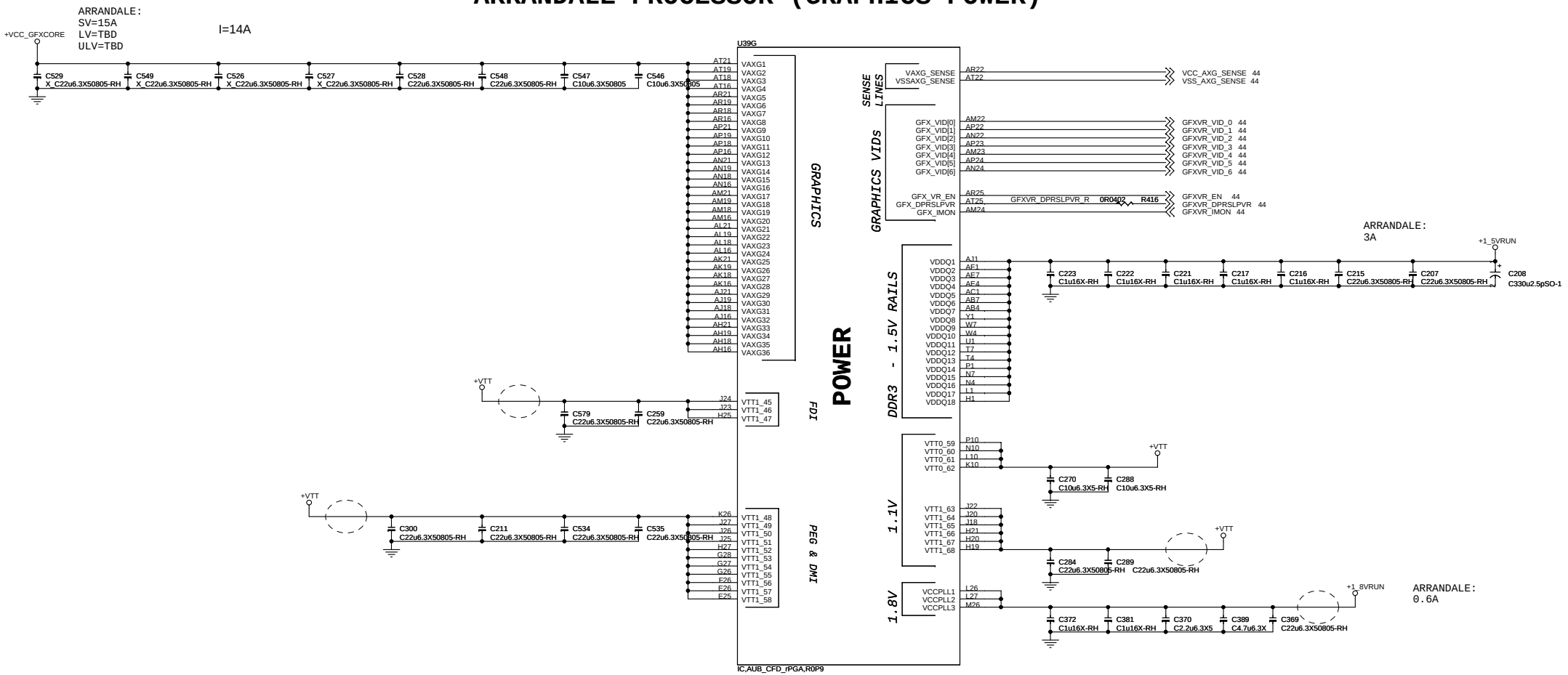
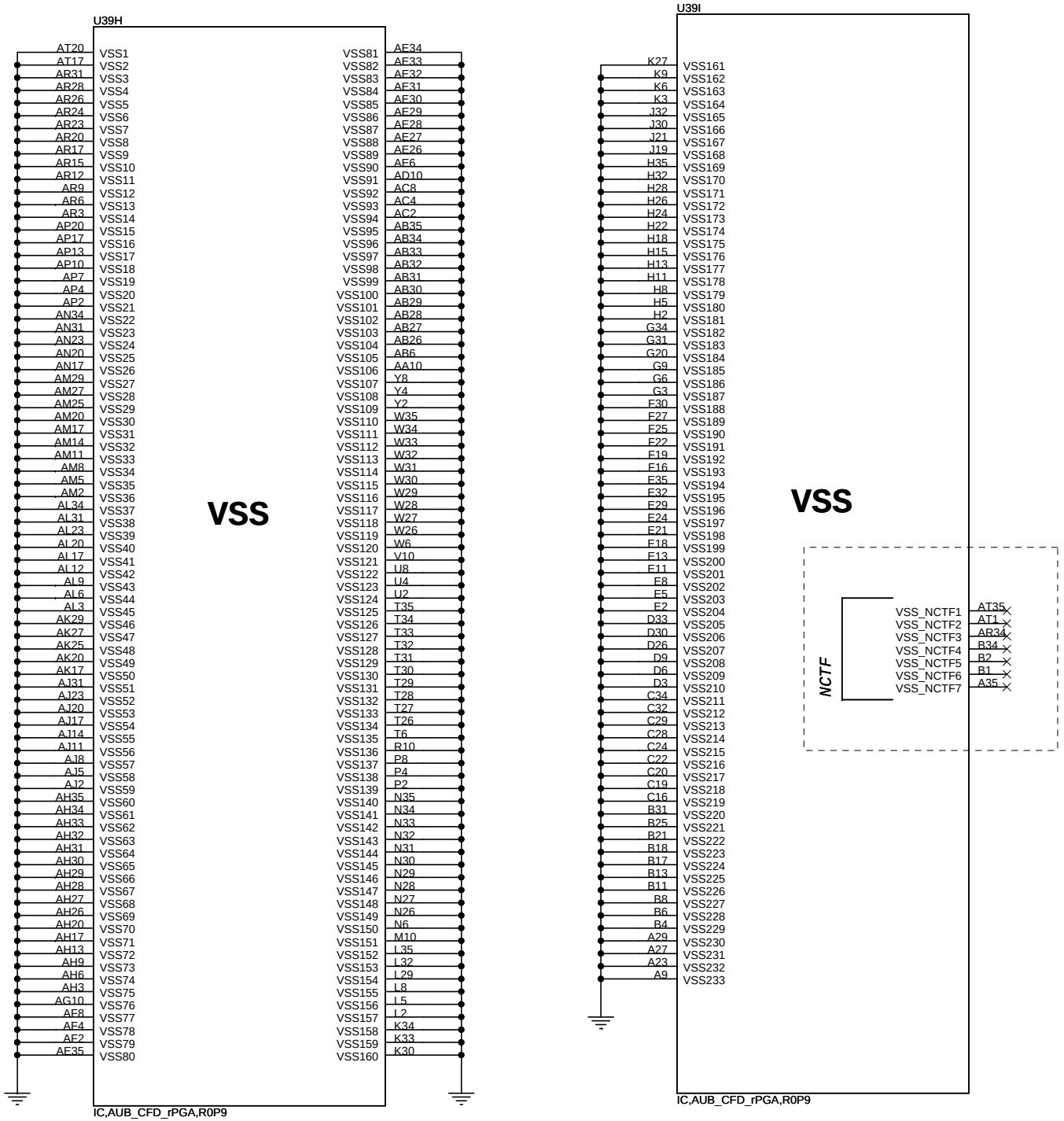
ARRANDALE PROCESSOR (GRAPHICS POWER)



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	GRAPHICS POWER	
Size: Custom	Document Number: MS-145X	Rev: 0A
Date: Wednesday, August 05, 2009	Sheet 6 of 56	

ARRANDALE PROCESSOR (GND)



MICRO-STAR INT'L CO.,LTD.	
Title	PROCESSOR GND
Size: Custom	Document Number: MS-145X
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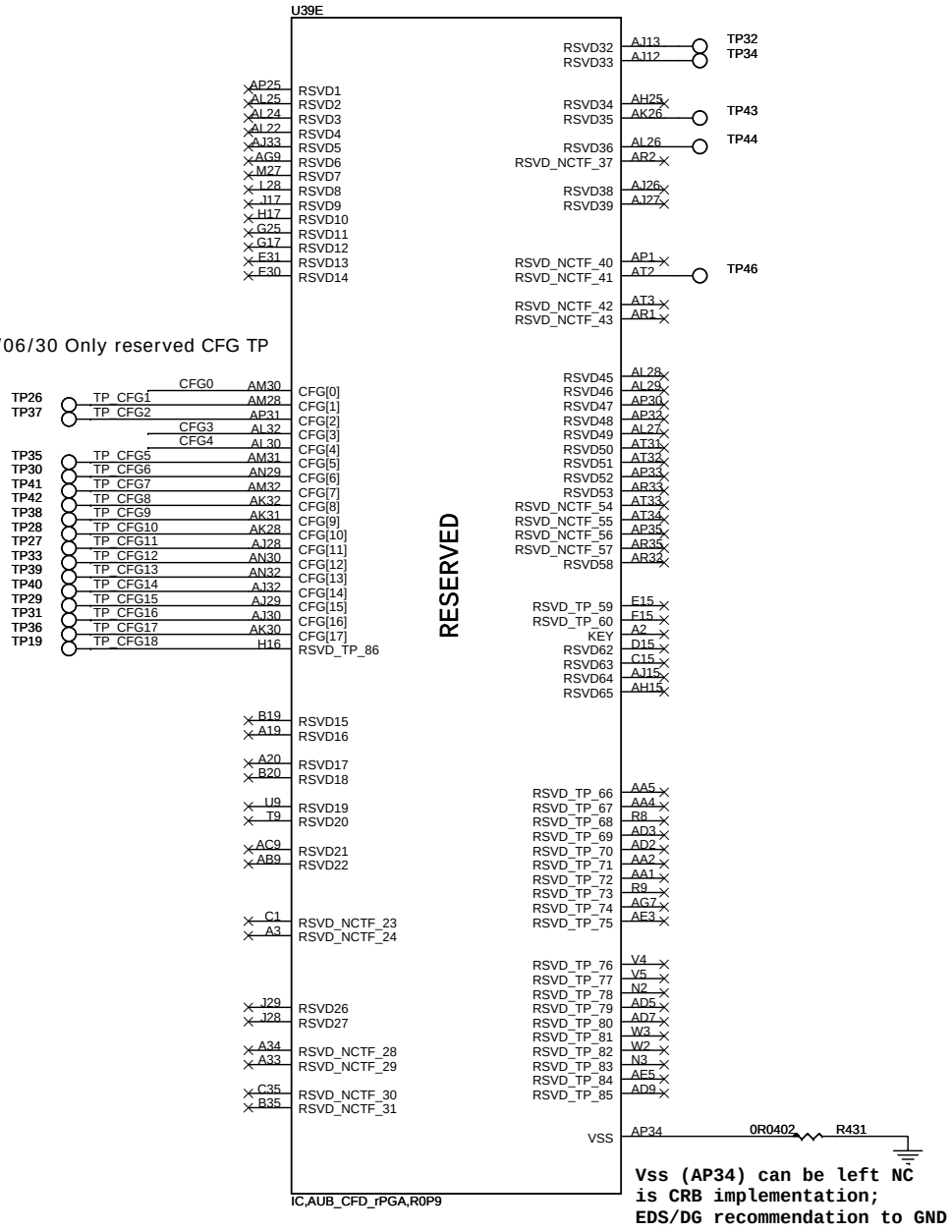
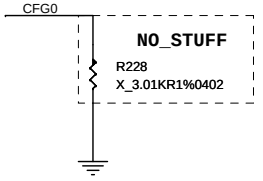
ARRANDALE PROCESSOR (RESERVED)



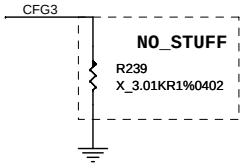
2009/06/30 Only reserved CFG TP

Vss (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND

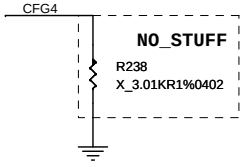
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



Layout Note:
Location of all CFG strap resistors needs to be close to trace to minimize stub

MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR RESERVED

Size: Custom | Document Number: MS-145X | Rev: 0A

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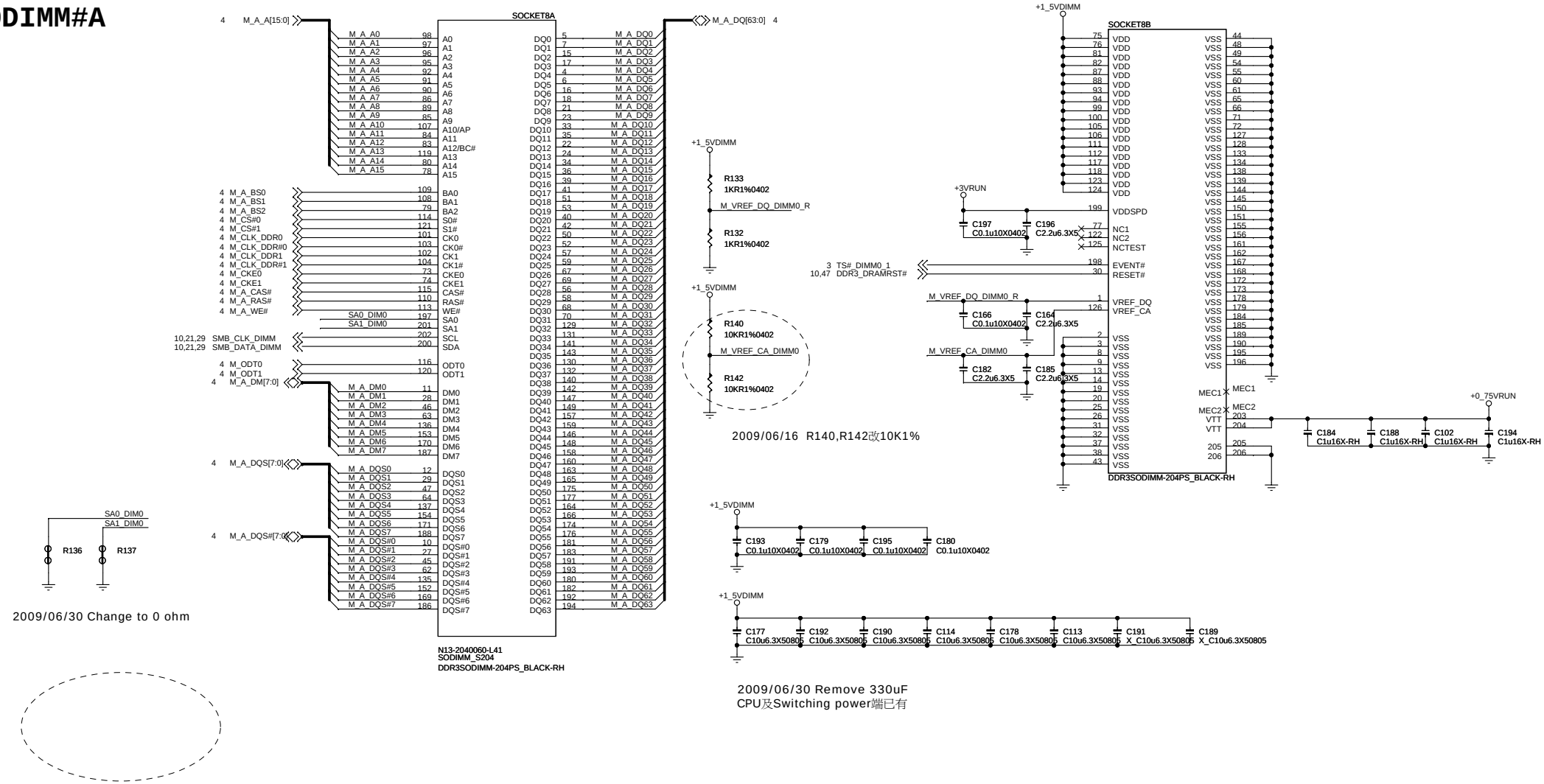
SODIMM#A



2009/06/30 Change to 0 ohm

2009/06/30 Remove 330uF
CPU及Switching power端已有

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	DDR3 SODIMM0	
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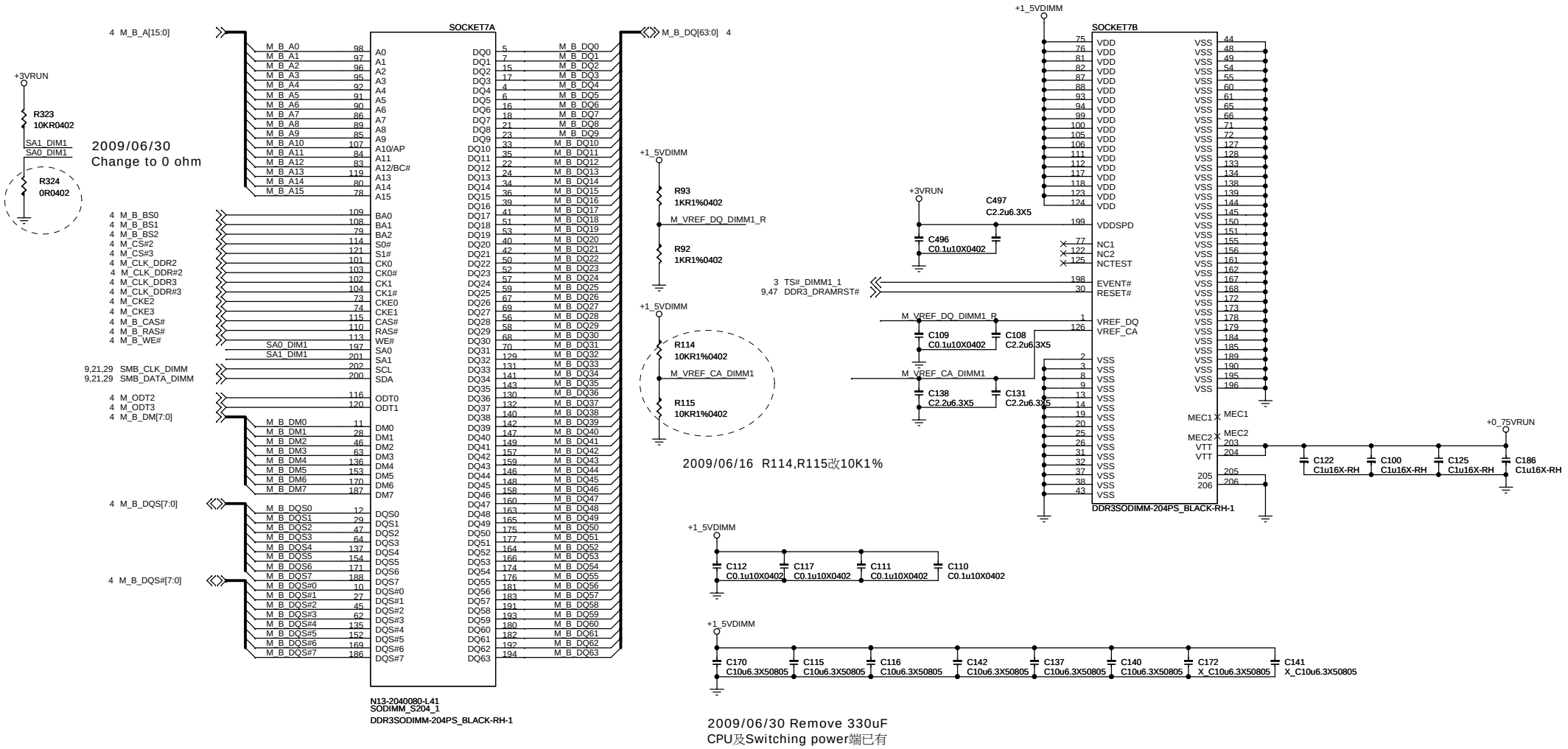
SODIMM#B



Eletro-X

MSI MICRO-STAR INT'L CO.,LTD.

Title	DDR3 SODIMM1	
Size: Custom	Document Number: MS-145X	Rev: 0A
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2009/06/30 靠近CPU(TX)

CheckResetSequence

For Park-S3: PWRGOOD pin must need to pull low

For M92-S2/S3: PWRGOOD pin should be NC

	M92-S2	PARK-S3
R215	X	-

MICRO-STAR INT'L CO.,LTD.

Title: M92/Pak-Sx (PCIE_Interface)

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	M92-S2	PARK-S3
R210	X	-
R195	X	-
R208	X	-
C659	X	-
C658	X	-
C512	X	-
C662	X	-
C661	X	-
C660	X	-
R197	X	-
R356	X	-
C665	X	-
C664	X	-
C663	X	-
R406	X	-
R404	X	-
R402	X	-

For PARK-S3: Install All components in this Box INCLUDING Decoupling caps and Bead connecting to DPC_VDD18#

For M92-S2: DO NOT Install any Component in this Box.

U40B

M93-S3/M92-S2

DVCNTL_0/ DVPDATA_18
DVCNTL_1 / NC
DVCNTL_2 / NC
DVDATA_12 / DVPDATA_16
DVDATA_11 / DVPDATA_20
DVDATA_10 / DVPDATA_22
DVDATA_9 / DVPDATA_12
DVDATA_8 / DVPDATA_14
DVDATA_7 / DVPCNTL_0
DVDATA_6 / DVPDATA_8
DVDATA_5 / DVPDATA_6
DVDATA_4 DVPDATA_4
DVDATA_3 / DVPDATA_19
DVDATA_2 / DVPDATA_21
DVDATA_1 / DVPDATA_2
DVDATA_0 / DVPDATA_0

DV0

DPA: TXCAP_DPA3P, TXCAM_DPA3N, TX0P_DPA2P, TX0M_DPA2N, TX1P_DPA1P, TX1M_DPA1N, TX2P_DPA0P, TX2M_DPA0N

DPB: TXCBP_DPB3P, TXCBM_DPB3N, TX3P_DPB2P, TX3M_DPB2N, TX4P_DPB1P, TX4M_DPB1N, TX5P_DPB0P, TX5M_DPB0N

M93-S3/M92-S2

DPC_PVDD / DVPDATA_11
DPC_PVSS / GND

DPC_VDD18#1/DVPDAT10
DPC_VDD18#2/DVPDAT23

DPC_VDD10#1/DVPDAT15
DPC_VDD10#2/DVPDAT17

DPC_VSSR#1 / DVPCLK
DPC_VSSR#2 / DVPDAT5
DPC_VSSR#3 / GND
DPC_VSSR#4 / GND
DPC_VSSR#5/ DVPCNTL_MV0

M92-S2/M93-S3

DVPDATA_3/TXCCP_DPC3P
DVPCNTL_2/TXCCM_DPC3N
DVPDATA_7 / TX0P_DPC2P
DVPDATA_1 / TX0M_DPC2N
DVPCNTL_MV1 / TX1P_DPC1P
DVPDATA_9 / TX1M_DPC1N
DVPDATA_13 / TX2P_DPC0P
DVPCNTL_1 / TX2M_DPC0N
VDDR4 / DPCD_CALR

DPC

For M92-S2: Use 0R to VDDR4
For Park-S3: DNI (NC)

	M92-S2	PARK-S3
R206	X	-

M93-S3/M92-S2

SCL
SDA

I2C

GENERAL PURPOSE I/O

GPIO_0
GPIO_1
GPIO_2
GPIO_3_SMBDATA
GPIO_4_SMBCLK
GPIO_5_AC_BATT
GPIO_6
GPIO_7_BLON
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15_PWRCNTL_0
GPIO_16_SSIN
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20_PWRCNTL_1
GPIO_21_BB_EN
GPIO_22_ROMCSB
GPIO_23_CLKREQB

JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
TESTEN

GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4

HPD1

VREFG

M92-S2/M93-S3

DAC1: R, RB, G, GB, B, BB, HSYNC, VSYNC, RSET, AVDD, AVSSQ, VDD1DI, VSS1DI

DAC2: R2 / NC, R2B / NC, G2 / NC, G2B / NC, B2 / NC, B2B / NC, C / NC, Y / NC, COMP / NC, H2SYNC, V2SYNC, VDD2DI / NC, VSS2DI / NC, A2VDD / NC, A2VDDQ / NC, A2VSSQ, R2SET / NC

M92-S2/M93-S3

PLL/CLOCK

DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
XTALIN
XTALOUT
NC#2/XO_IN
NC#1/XO_IN2

M92-S2/M93-S3

DDC/AUX: DDC1CLK, DDC1DATA, AUX1P, AUX1N, DDC2CLK, DDC2DATA, AUX2P, AUX2N, DDCCLK_AUX5P, DDCDATA_AUX5N, DDC6CLK, DDC6DATA, NC/DDCCLK_AUX3P, NC/DDCDATA_AUX3N

THERMAL

DPLUS
DMINUS
TS_FDO
TSVDD
TSVSS

216-0728020-00-A12-RH

AVSSQ have to be away from noisy ground
A2VSSQ have to be away from noisy ground
it is for layout recommendation

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

+1_8VRUN_PARK

B7 120L200mA-200 — (1.8V@70mA AVDD) — AVDD — C238 X_C10u6.3X50805 — C249 C0.1u10X0402-1 — C262 C1u6.3Y0402-RH

JNC9 X_0603 — (1.8V@45mA VDD1DI) — VDD1DI — C218 X_C10u6.3X50805 — C228 C1u6.3Y0402-RH — C277 C0.1u10X0402-1

B10 120L200mA-200 — (1.8V@2mA A2VDDQ) — A2VDDQ — C235 X_C10u6.3X50805 — C256 C0.1u10X0402-1 — C242 C1u6.3Y0402-RH

JNC10 X_0603 — (1.8V@40mA VDD2DI) — VDD2DI — C219 X_C10u6.3X50805 — C282 C0.1u10X0402-1 — C229 C1u6.3Y0402-RH

VDDR3 — JNC12 X_0603 — (3.3V@65mA A2VDD) — A2VDD — C236 X_C10u6.3X50805 — C257 C1u6.3Y0402-RH — C243 C0.1u10X0402-1

+3VRUN — HPD1 — R158 10KR0402 — U28 S08P5X_SC70 — DVI_A_HPD 18 — DGPU_PWROK 25 — ER20 — DGPU_HPD_INTR# 25

VDDR3 +3VRUN — 25,45 DGPU_PWR_EN — R443 0R0402 — Q28 P-NDS352AP — R453 100KR0402 — +1_8VRUN_PARK — R451 X_47KR0402 — C623 C0.1u16Y0402 — Q29 N-BSS138_SOT23

OPTIONAL RC NETWORK TO FINE TUNE POWER SEQUENCING

Check 1.8VRUN and VDDR3 Sequence
For Park-S3 : Stuff R443
For M92-S2 : Stuff R451

R386 150R1%0402
R382 150R1%0402
R387 150R1%0402

1.0 change P/N

VDDR3 +3VRUN — R478 X_0R0402 — R479 0R0402 — M92_THERMDA — C560 C100p16N0402 — M92_THERMDC — U41 SNSR-G780P81U-RH (VCC, DXP, DXN, THERM#, SMBCLK, SMBDATA, ALERT#, GND) — SMB_THRM_CLK 30 — SMB_THRM_DATA 30 — C615 C0.1u16Y0402

Sequence

RN26 8P4R-10KR0402 — VDDR3 — T_CRIT_M92# — M92_THRM_ALERT- — RN0402_MSI

ATI suggestion

TP22 TP59 TP60 TP62 TP61 35mil — GPIO24_TRSTB — GPIO25_TDI — GPIO26_TCK — GPIO27_TMS — GPIO28_TDO

R190 10KR0402

JTAG DEBUG PORT — 21 PEG_CLKREQ# — R220 X_0R0402

17 GENERICC — 13 TEST_EN

+1_8VRUN_PARK — HPD1 — R165 499R1%0402 — R166 249R1%0402 — C230 C0.1u10X0402-1

R191 715R1%0402

0R1

(1.8V@75mA DPLL_PVDD) — B9 470L1.5A-150-RH — C241 C10u6.3X50805 — C261 C1u6.3Y0402-RH — C247 C0.1u10X0402-1

(1.0V@125mA DPLL_VDDC)
(1.1V@150mA DPLL_VDDC)

+1_0VRUN_PARK — B14 470L1.5A-150-RH — C275 C10u6.3X50805 — C274 C1u6.3Y0402-RH — C273 C0.1u10X0402-1

2009/07/09 Default use clock GEN. 27MHz(SS)

29 CLK_XTAL_27M_IN — R385 0R0402 — M92_XTAL_IN — C521 X_C22p50N0402 — C522 X_C22p50N0402 — Y11 X_27MHZ — R384 X_1MR0402 — M92_XTAL_IN — M92_XTAL_OUT

Note:1
For M9x-S2/S3 XO_IN and XO_IN2 Pins are NC, can be gronded

For Park-S3: XO_IN and XO_IN2 can be use as 3.3V CLK Input. These poins can be grounded if not in use.

R187 0R0402 — R186 0R0402

M92_THERMDA — M92_THERMDC

(1.8V@20mA TSVDD) — +1_8VRUN_PARK

VDDR3

I2C_DATA	R392	10KR0402
I2C_CLK	R393	10KR0402
DAC_SDAT	R397	10KR0402
DAC_SCL	R398	10KR0402
DVI_DATA_MXM	R396	10KR0402
DVI_CLK_MXM	R395	10KR0402

HDMI 5V
LVDS 3.3V
CRT 5V

LVDS Interface

U40F

LVDS CONTROL: VARY_BL, DIGON — BLON_PWM 18 — LVDS_DIGON 18

R202 10KR0402 — R201 X_10KR0402

TXCLK_UP_DPF3P / TXCLK_UN_DPF3N
TXOUT_U0P_DPF2P / TXOUT_U0N_DPF2N
TXOUT_U1P_DPF1P / TXOUT_U1N_DPF1N
TXOUT_U2P_DPF0P / TXOUT_U2N_DPF0N
TXOUT_U3P / TXOUT_U3N

LVTMDP

TXCLK_LP_DPE3P / TXCLK_LN_DPE3N — LVDS_TX_CLKLP 18 — LVDS_TX_CLKLN 18
TXOUT_L0P_DPE2P / TXOUT_L0N_DPE2N — LVDS_TX_L0P 18 — LVDS_TX_L0N 18
TXOUT_L1P_DPE1P / TXOUT_L1N_DPE1N — LVDS_TX_L1P 18 — LVDS_TX_L1N 18
TXOUT_L2P_DPE0P / TXOUT_L2N_DPE0N — LVDS_TX_L2P 18 — LVDS_TX_L2N 18
TXOUT_L3P / TXOUT_L3N

216-0728020-00-A12-RH

MSI MICRO-STAR INT'L CO.,LTD.

Title: M92/Pak-Sx (Main IO)

Size: Custom — Document Number: MS-145X — Rev: 0A

Date: Wednesday, August 05, 2009 — Sheet 12 of 56

MVDDQ = 1.5V FOR DDR3 Memory

DDR3 Memory Interface

MDA[63..0] 16
MAA[13..0] 16
A_BA0 16
A_BA1 16
A_BA2 16
DQMA#[7..0] 16
QSA#[7..0] 16
QSA[7..0] 16
CLKA1 16
CLKA1# 16
CLKA0 16
CLKA0# 16
RASA0# 16
RASA1# 16
CASA0# 16
CASA1# 16
CSA0#_0 16
CSA1#_0 16
CKEA0 16
CKEA1 16
WEA0# 16
WEA1# 16

U40C

MEMORY INTERFACE

MDA0	K27	DQA_0	MAA_0	K17	MAA0
MDA1	J29	DQA_1	MAA_1	J20	MAA1
MDA2	H30	DQA_2	MAA_2	H23	MAA2
MDA3	H32	DQA_3	MAA_3	G23	MAA3
MDA4	G29	DQA_4	MAA_4	G24	MAA4
MDA5	F28	DQA_5	MAA_5	H24	MAA5
MDA6	F32	DQA_6	MAA_6	J19	MAA6
MDA7	E30	DQA_7	MAA_7	K19	MAA7
MDA8	C30	DQA_8	MAA_8	J14	MAA8
MDA9	F27	DQA_9	MAA_9	K14	MAA9
MDA10	A28	DQA_10	MAA_10	J11	MAA10
MDA11	C28	DQA_11	MAA_11	J13	MAA11
MDA12	E27	DQA_12	MAA_12	H11	MAA12
MDA13	G26	DQA_13	MAA_13/BA2	G11	A_BA2
MDA14	D26	DQA_14	MAA_14/BA0	J16	A_BA0
MDA15	F25	DQA_15	MAA_15/BA1	L15	A_BA1
MDA16	A25	DQA_16			
MDA17	C25	DQA_17	DQMA_0	E32	DQMA#0
MDA18	E25	DQA_18	DQMA_1	E30	DQMA#1
MDA19	D24	DQA_19	DQMA_2	A21	DQMA#2
MDA20	E23	DQA_20	DQMA_3	C21	DQMA#3
MDA21	F23	DQA_21	DQMA_4	E13	DQMA#4
MDA22	D22	DQA_22	DQMA_5	D12	DQMA#5
MDA23	E21	DQA_23	DQMA_6	E3	DQMA#6
MDA24	F21	DQA_24	DQMA_7	F4	DQMA#7
MDA25	D20	DQA_25			
MDA26	E19	DQA_26	RDQSA_0	H28	QSA0
MDA27	A19	DQA_27	RDQSA_1	C27	QSA1
MDA28	D18	DQA_28	RDQSA_2	A23	QSA2
MDA29	F17	DQA_29	RDQSA_3	E19	QSA3
MDA30	A17	DQA_30	RDQSA_4	F15	QSA4
MDA31	C17	DQA_31	RDQSA_5	D10	QSA5
MDA32	E17	DQA_32	RDQSA_6	D6	QSA6
MDA33	D16	DQA_33	RDQSA_7	G5	QSA7
MDA34	F15	DQA_34			
MDA35	A15	DQA_35	WDQSA_0	H27	QSA#0
MDA36	D14	DQA_36	WDQSA_1	A27	QSA#1
MDA37	F13	DQA_37	WDQSA_2	C23	QSA#2
MDA38	A13	DQA_38	WDQSA_3	C19	QSA#3
MDA39	C13	DQA_39	WDQSA_4	C15	QSA#4
MDA40	E11	DQA_40	WDQSA_5	F9	QSA#5
MDA41	A11	DQA_41	WDQSA_6	C5	QSA#6
MDA42	C11	DQA_42	WDQSA_7	H4	QSA#7
MDA43	E11	DQA_43			
MDA44	A9	DQA_44	ODTA0	L18	ODTA0
MDA45	C9	DQA_45	ODTA1	K16	ODTA1
MDA46	F9	DQA_46			
MDA47	D8	DQA_47	CLKA0	H26	CLKA0
MDA48	E7	DQA_48	CLKA0B	H25	CLKA0#
MDA49	A7	DQA_49			
MDA50	C7	DQA_50	CLKA1	G9	CLKA1
MDA51	E7	DQA_51	CLKA1B	H9	CLKA1#
MDA52	A5	DQA_52			
MDA53	E5	DQA_53	RASA0B	G22	RASA0#
MDA54	C3	DQA_54	RASA1B	G17	RASA1#
MDA55	E1	DQA_55			
MDA56	G7	DQA_56	CASA0B	G19	CASA0#
MDA57	G6	DQA_57	CASA1B	G16	CASA1#
MDA58	G1	DQA_58			
MDA59	G3	DQA_59	CSA0B_0	H22	CSA0# 0
MDA60	J6	DQA_60	CSA0B_1	J22	
MDA61	J1	DQA_61			
MDA62	J3	DQA_62	CSA1B_0	G13	CSA1# 0
MDA63	J5	DQA_63	CSA1B_1	K13	
MVREF	K26	MVREFDA	CKEA0	K20	CKEA0
	J26	MVREFSA	CKEA1	J17	CKEA1
	J25	MEM_CALRN0	WEA0B	G25	WEA0#
TEST_EN 12	K7	NC/TESTEN#2	WEA1B	H10	WEA1#
DPC_CALR	J8	MEM_CALRP1/DPC_CALR	PX_EN	AB16	TPJNC34
	K25	MEM_CALRP0			
DRAM_RST	L10	DRAM_RST			
CLKTESTA	K8	CLKTESTA	RSVD#2	G14	
CLKTESTB	L7	CLKTESTB	RSVD#3	G20	MAA13

216-0728020-00-A12-RH

For PARK-S3 only
For M9X-S2/S3 with DDR3: this pin is not in use.

	M92-S2	PARK-S3
R419	X	-
R421	-	X

Note:2

R419 X_150R1%0402 DPC_CALR
R421 240R1%0402

QSA#[7..0] QSA#[7..0] 16
QSA[7..0] QSA[7..0] 16
QSA#[7..0] QSA#[7..0] 16
QSA[7..0] QSA[7..0] 16
ODTA0 ODTA0 16
ODTA1 ODTA1 16

	M92-S2	PARK-S3
R419	X	-
R421	X	-

Option for DDR3/GDDR3/DDR2 with Park

CKEA1
CKEA0
R247 10KR0402
R246 10KR0402

Do not Install for M9X-S2/S3
INSTALL for Park-S3 to save power in auto refresh mode

These can be placed close to ASIC side or Memory side.

Note 1 : Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.

Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR

Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24

DRAM_RST
** R427 680R0402-RH
MEM_RST 16
R425 10KR0402
** C571 C68p50N0402-RH
** R430 X_2.2KR0402
+1_5VRUN_PARK

** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor vvalues are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Designator	For M9X-S2 and M93-S3	For Park-S3
R425	DNI	10K
R427	0R/Short	680R
R430	2.2K	DNI
C571	2.2nF	68pF

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

	M92-S2	PARK-S3
R234	X	-
R181	X	-
R230	X	-

+1_5VRUN_PARK
Ra R237 100R1%0402
Rb R236 100R1%0402
C358 C0.1u10X0402-1
MVREF
Note: 1 R234 X_240R1%0402
R181 X_0R0402 Note:3
Note: 1 R230 X_240R1%0402
Ra R232 100R1%0402
Rb R233 100R1%0402
C354 C0.1u10X0402-1
R428 4.7KR0402 R0402
R226 4.7KR0402 R0402
C568 X_C0.1u10X0402-1
C341 X_C0.1u10X0402-1
R423 X_51.1R1%0402
R227 X_51.1R1%0402

	M92-S2	PARK-S3
R428	-	X
R226	-	X

Use this option ONLY for M9x-S2/S3vFamily

route 50ohms single-ended/100ohms diff and keep short

Use this option ONLY for Park-S3

	M92-S2	PARK-S3
C568	X	-
C341	X	-
R423	X	-
R227	X	-

DIVIDER RESISTORS	DDR3	GDDR3
MVREF TO 1.5V (Ra)	100R	40.2R
MVREF TO GND (Rb)	100R	100R

MICRO-STAR INT'L CO.,LTD.

Title: M92/Pak-Sx (MEM Interface)
Size: Custom
Document Number: MS-145X
Rev: 0A
Date: Wednesday, August 05, 2009
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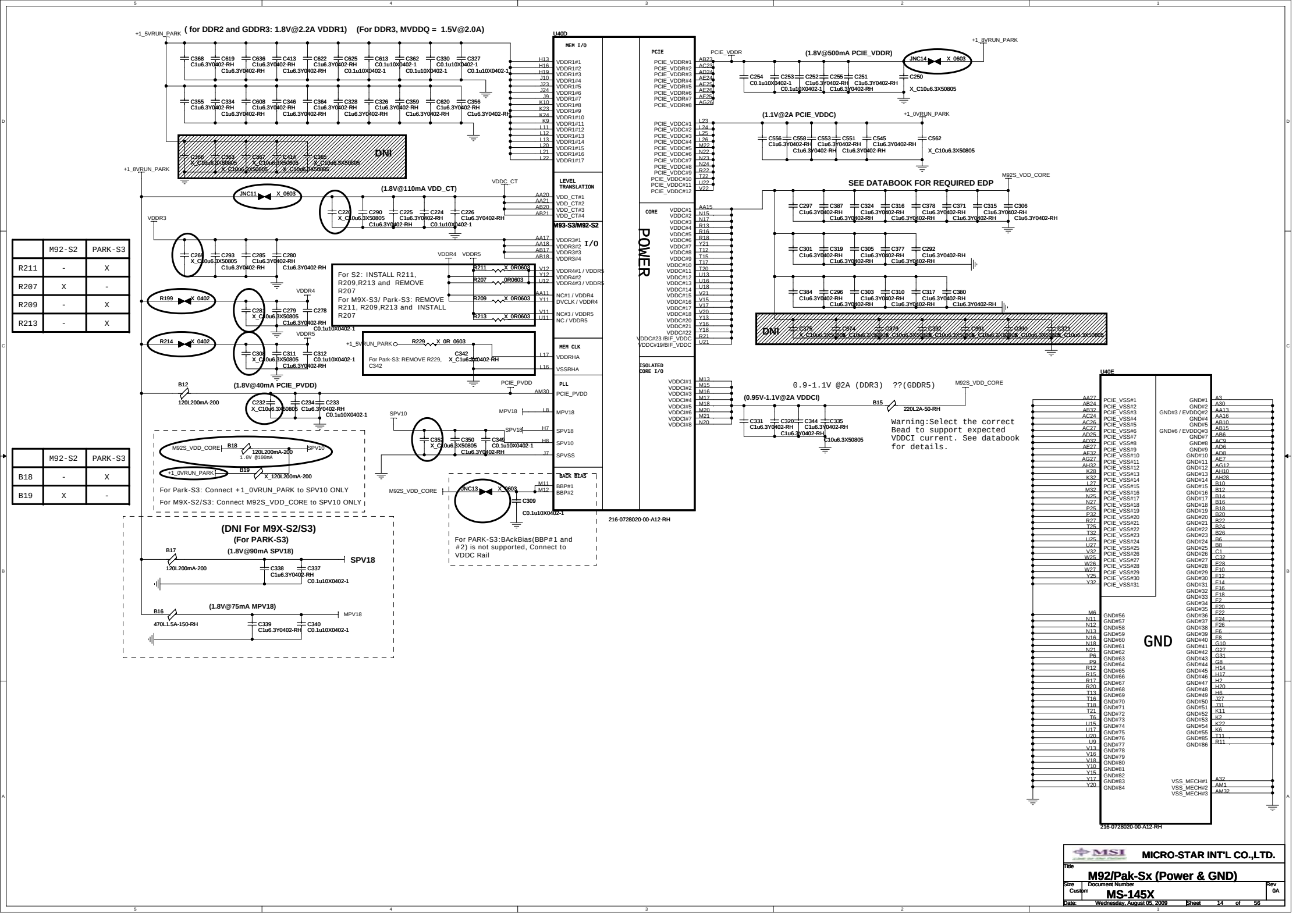


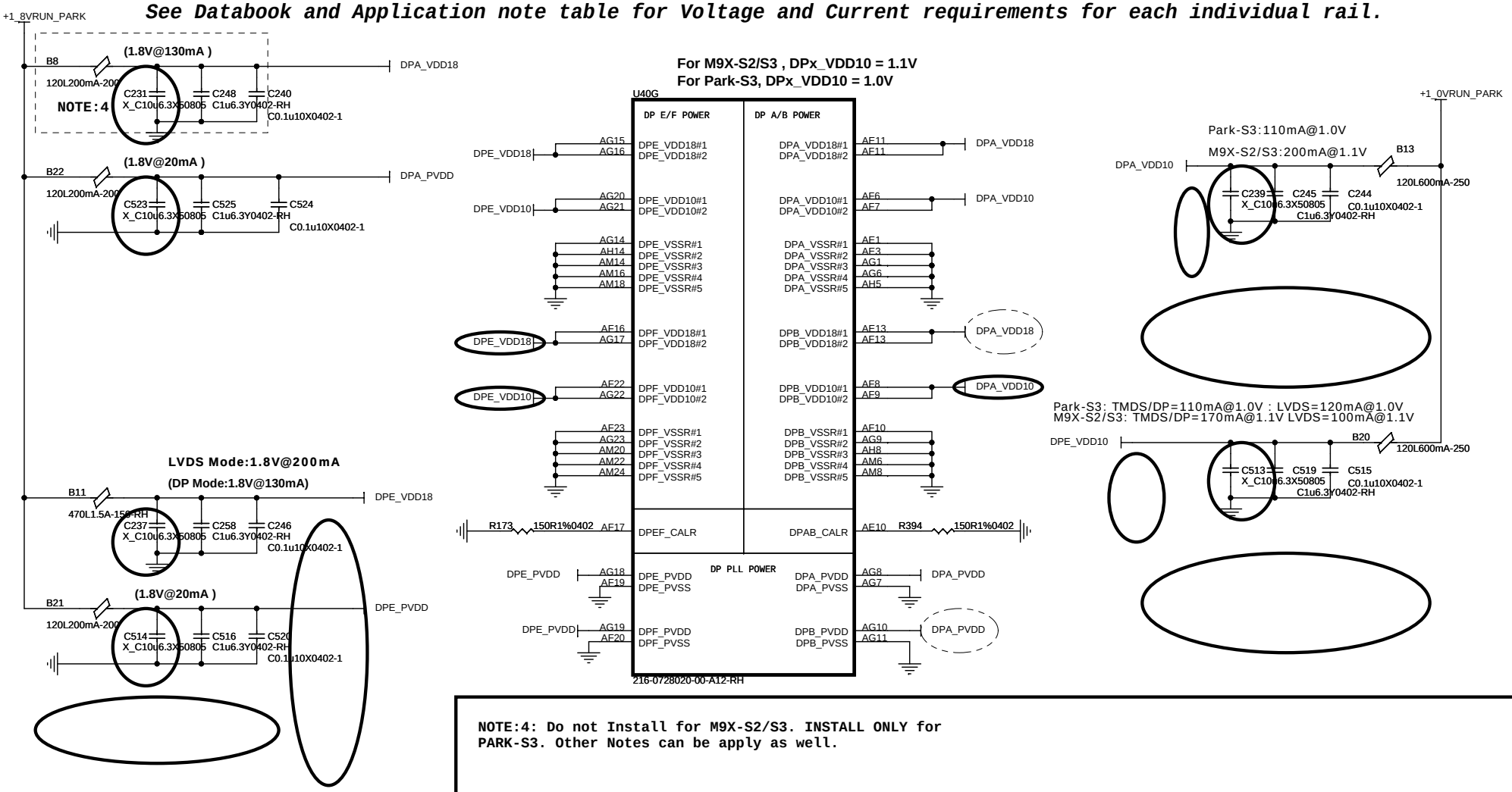
MICRO-STAR INT'L CO.,LTD.

Title: M92/Pak-Sx (Power & GND)

Size: Custom | Document Number: MS-145X | Rev: 0A

Date: Wednesday, August 05, 2009 | Sheet 14 of 56

See Databook and Application note table for Voltage and Current requirements for each individual rail.



NOTE:4: Do not Install for M9X-S2/S3. INSTALL ONLY for PARK-S3. Other Notes can be apply as well.

MICRO-STAR INT'L CO.,LTD.		
Title: M92/Pak-Sx (DP_Power)		
Size: Custom	Document Number: MS-145X	Rev: 0A
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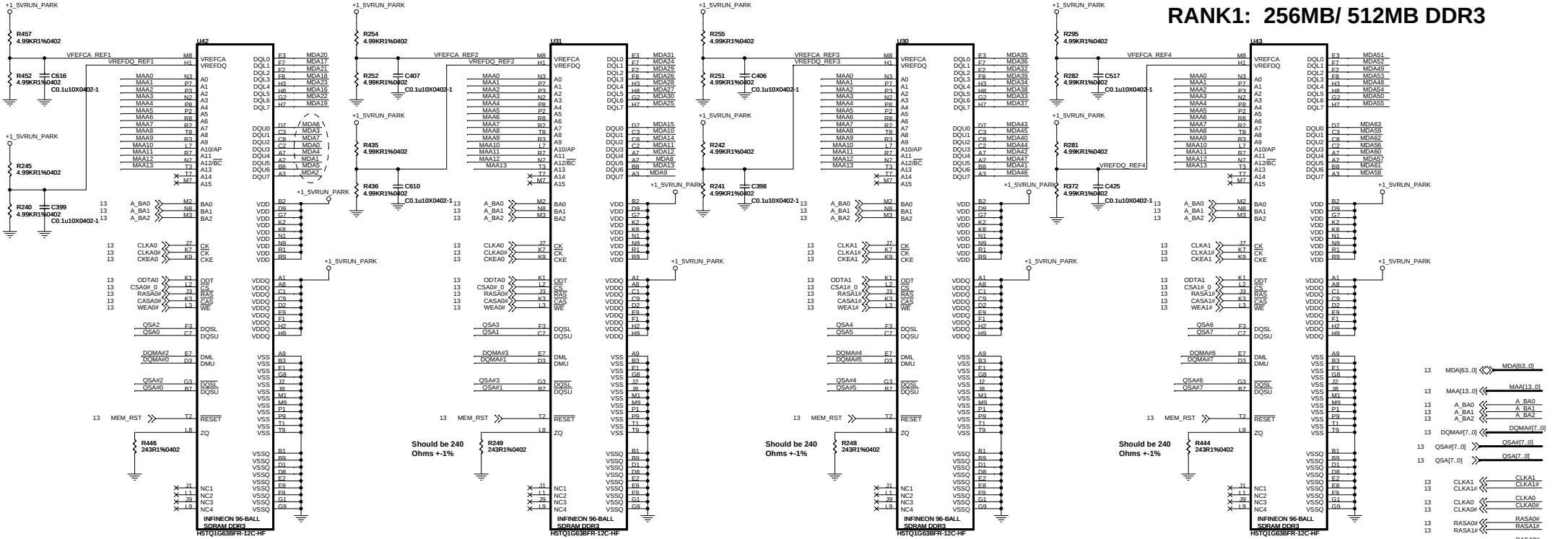
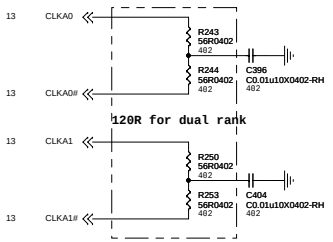
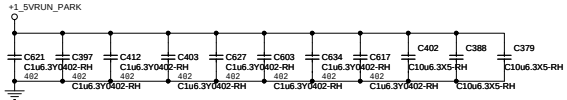
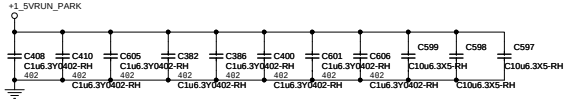
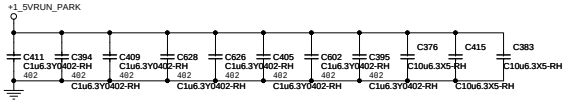
RANK1: 256MB/ 512MB DDR3

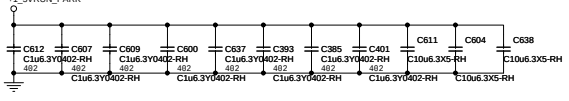


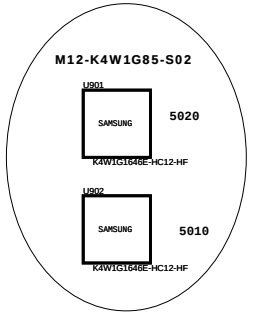












For M9X-S2/S3 with DDR3: Support MAA12-MAA0 Address or 64MX16 DDR3. MAA13 is NC

For PARK-S3 with DDR3: Support MAA13-MAA0 Address or 128MX16 DDR3.

MICRO-STAR INT'L CO.,LTD.

Title: DDR2 (64Mx16bit)

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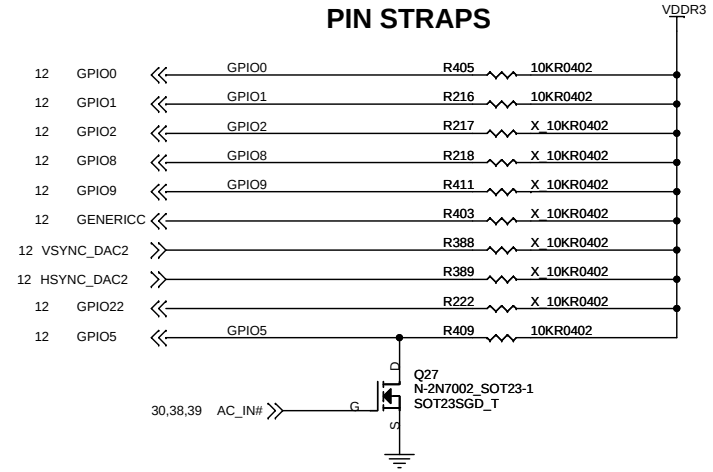
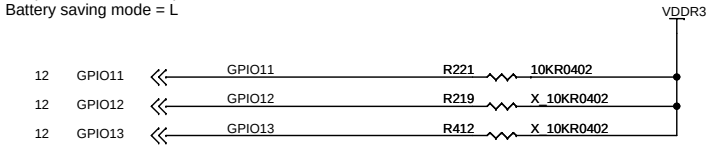
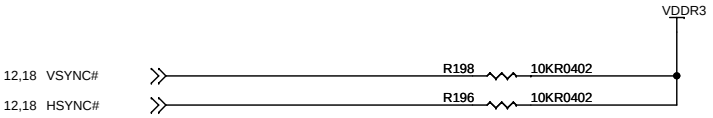
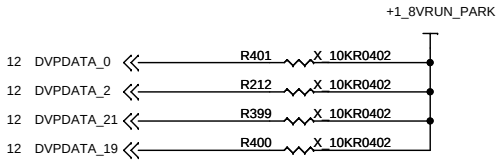
PIN STRAPS



GPIO_5_AC_BATT is an optional input which allows the system to request (AC) performance mode or battery mode operation.
AC (Performance mode) = H
Battery saving mode = L







CONFIGURATION STRAPS

PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
GPIO0	1		GPIO=0 50% TX output swing GPIO=1 Full TX output swing
GPIO1	1		GPIO=0 TX de-emphasis disabled GPIO=1 TX de-emphasis enabled
GPIO2	1		GPIO=0 Advertises the PCIE device as 2.5 GT/S capable at power -on GPIO=1 Advertises the PCIE device as 5 GT/S capable at power -on
GPIO9	0		GPIO=0 VGA controller capacity enabled. GPIO=1 The device will not be recognized as the system's VGA controler.
VSYNC_DAC2	0		GPIO=0 Driver would ignore the value sampled on DVPDATA_20 during reset.
GPIO22	0		GPIO=0 not used external BIOS ROM GPIO=1 if used

PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
GPIO 13 GPIO 12 GPIO 11			0 0 0=128 MB
	0 0 1		0 0 1=256 MB
			0 1 0=64 MB

PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
VGA_HSYNC# VGA_VSYNC#			0 0=No audio function
			0 1=Audio for display port only
			1 0=Audio for display port and HDMI if dongle is detected
	1 1		1 1=Audio for both displayport and HDMI

DVPDATA19	DVPDATA21	DVPDATA2	DVPDATA0	MEM_TYPE
0	0	0	0	Hynix 64Mx16 DDR3 (M12-5TQ1G25-H23)
0	0	0	1	Samsung 64Mx16 DDR3 (M12-K4W1G85-S02)
0	0	1	0	
0	0	1	1	

MICRO-STAR INT'L CO.,LTD.

Title: **M92/Pak-Sx (Straps & Thermal)**

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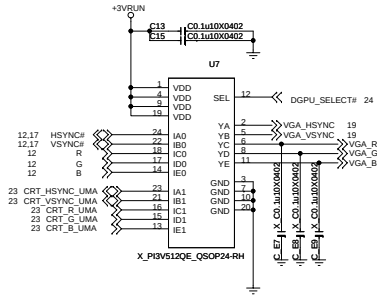
CRT Switch

2009/07/14 Change RGB SW



Logic Input	Function
0	S2 PORT
1	S1 PORT

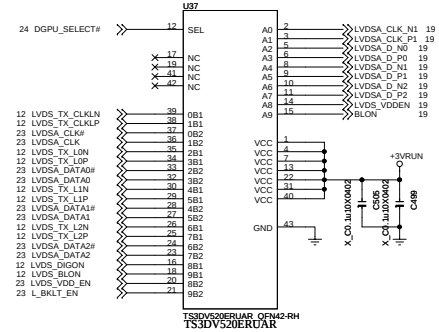
BR-ADJ

MXM only	1. MXM 2. EC
Switchable	1. MXM 2. iGPU 3. EC

UMA (MS-1454) USE ONLY

CRT_B_UMA	R14	X 0R0402	VGA_BLUE
CRT_G_UMA	R13	X 0R0402	VGA_GREEN
CRT_R_UMA	R11	X 0R0402	VGA_RED_
CRT_HSYNC_UMA	R12	X 0R0402	VGA_HSYNC
CRT_VSYNC_UMA	R15	X 0R0402	VGA_VSYNC

LVDS Switch



UMA (MS-1454) USE ONLY

RN4

LVDSA_CLK#	1	2		LVDSA_CLK_N1
LVDSA_CLK	3	4		LVDSA_CLK_P1
LVDSA_DATA0#	5	6		LVDSA_D_N0
LVDSA_DATA0	7	8		LVDSA_D_P0

X_8P4R-0R0402

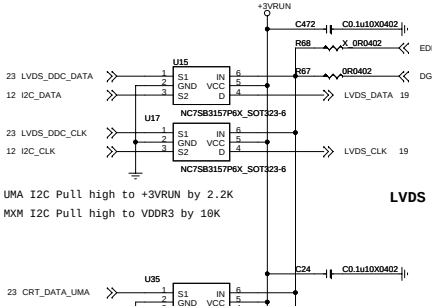
RN5

LVDSA_DATA1#	1	2		LVDSA_D_N1
LVDSA_DATA1	3	4		LVDSA_D_P1
LVDSA_DATA2#	5	6		LVDSA_D_N2
LVDSA_DATA2	7	8		LVDSA_D_P2

X_8P4R-0R0402

LVDS_VDD_EN	R71	X 0R0402	LVDS_VDDEN
L_BKLT_EN	R359	X 0R0402	BLON

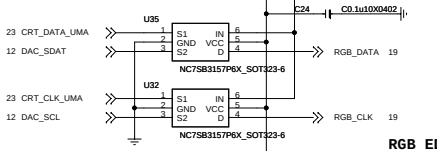
EDID Switch (CRT,LVDS)



UMA I2C Pull high to +3VRUN by 2.2K

MXM I2C Pull high to VDDR3 by 10K

LVDS EDID

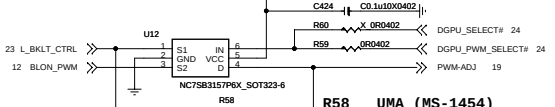


UMA I2C Pull high to +3VRUN by 2.2K

MXM I2C Pull high to VDDR3 by 10K

RGB EDID

2009/07/14 DEL HDMI I2C SW (U26,U27)



R58 UMA (MS-1454) USE ONLY

Logic Input	Function
0	PORT 1
1	PORT 2

UMA (MS-1454) USE ONLY

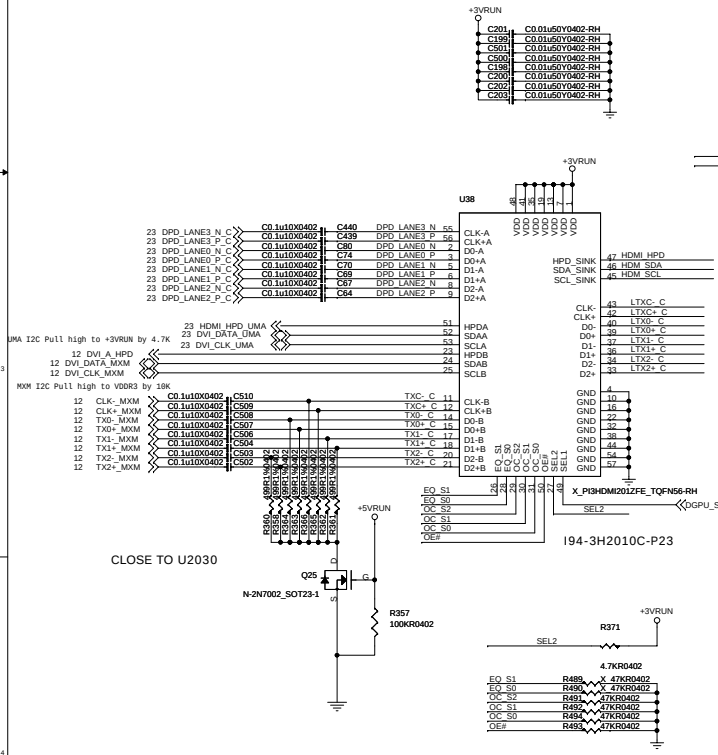
LVDS_DDC_CLK	R84	X 0R0402	LVDS_CLK
LVDS_DDC_DATA	R82	X 0R0402	LVDS_DATA
CRT_DATA_UMA	R265	X 0R0402	RGB_DATA
CRT_CLK_UMA	R266	X 0R0402	RGB_CLK

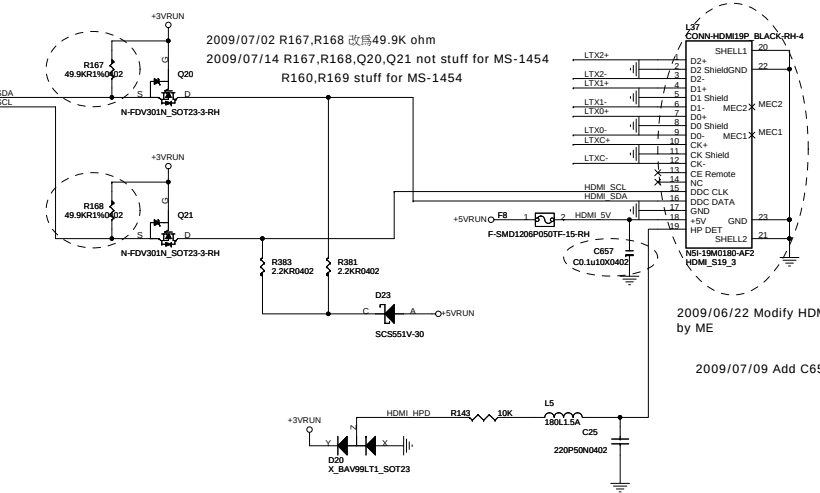
2009/07/14 DEL HDMI I2C RES (R372,R374)

HDMI Switch

2009/07/14 Change HDMI SW

Logic Input	Function
0	B PORT
1	A PORT





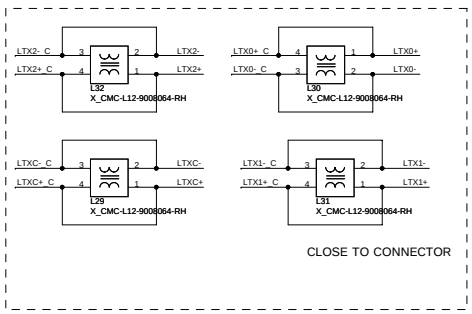
2009/07/02 R167,R168 改爲49.9K ohm

2009/07/14 R167,R168,Q20,Q21 not stuff for MS-1454

R160,R169 stuff for MS-1454

2009/06/22 Modify HDMI conn PN by ME

2009/07/09 Add C657



CLOSE TO CONNECTOR

MICRO-STAR INT'L CO.,LTD.

Title: SWITCH&HDMI

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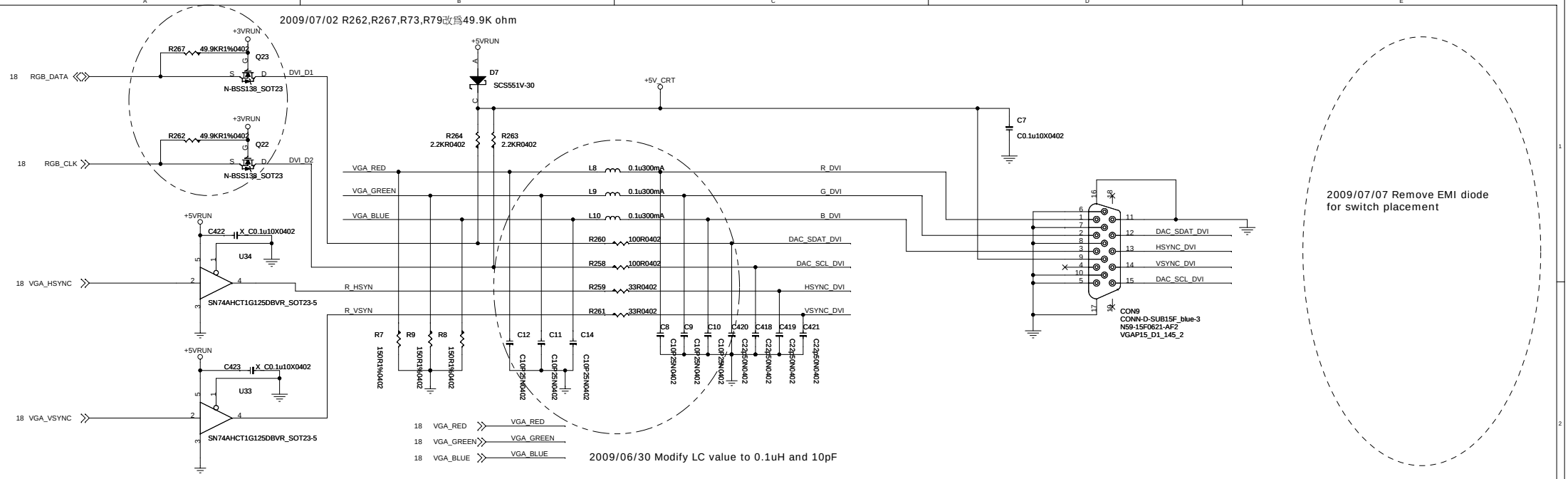
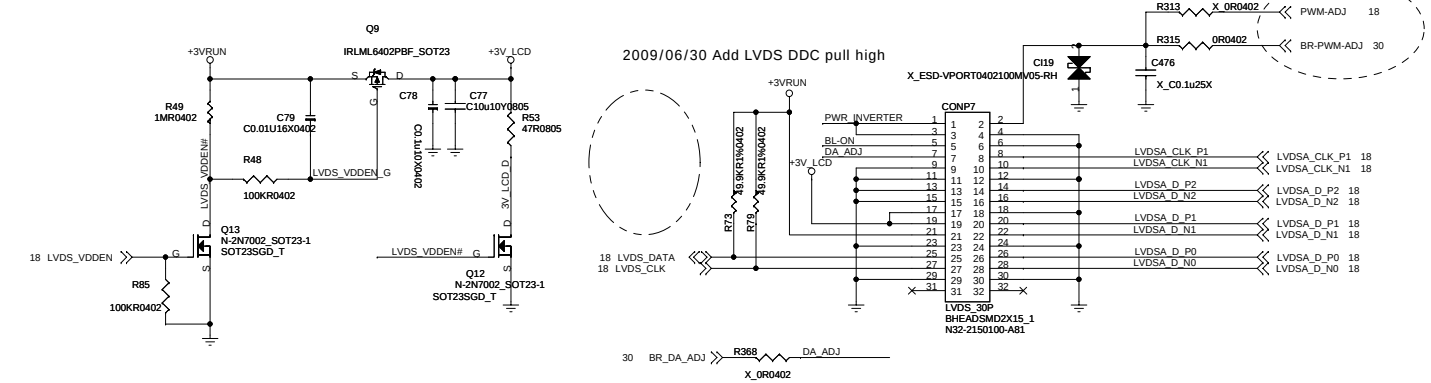
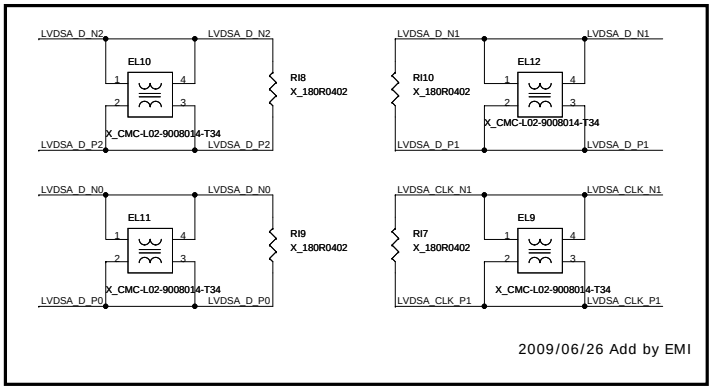
2009/07/02 R262,R267,R73,R79改爲49.9K ohm

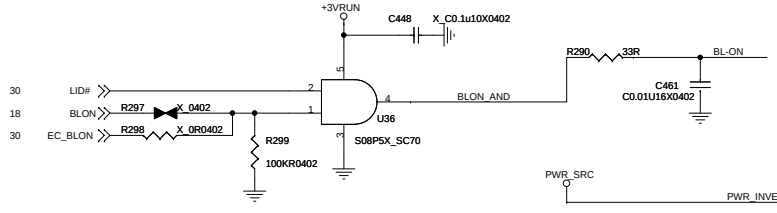


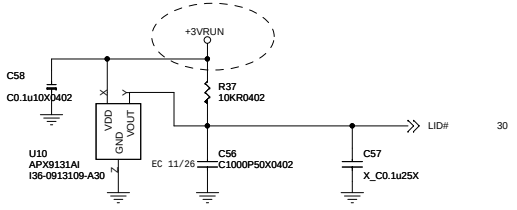
2009/06/30 Modify LC value to 0.1uH and 10pF

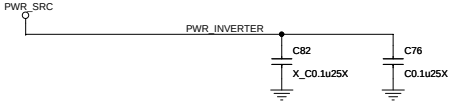
2009/07/07 Remove EMI diode for switch placement





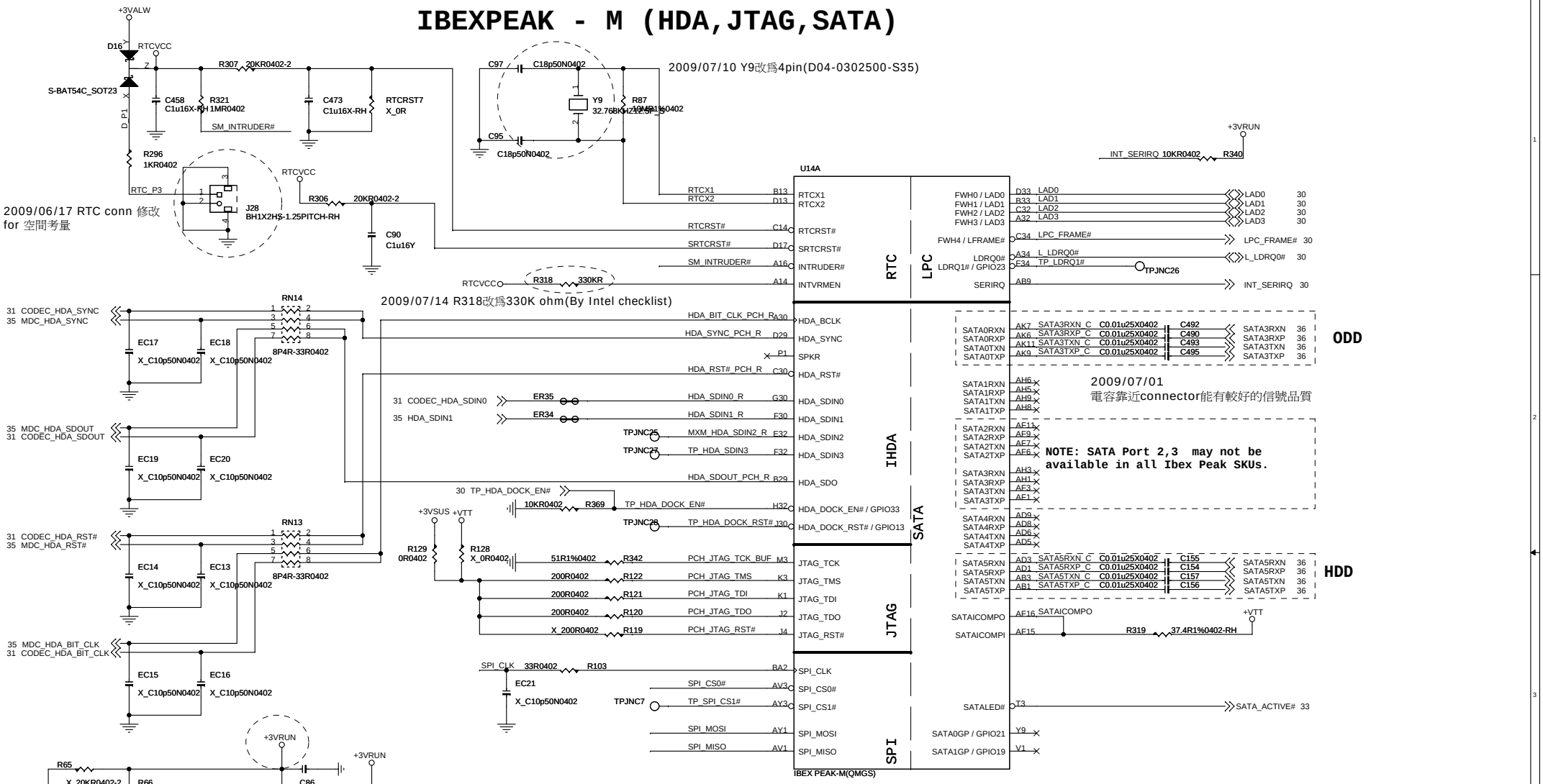






MICRO-STAR INT'L CO.,LTD.			
Title: CRT & LVDS			
Size: Custom	Document Number: MS-145X		Rev: 0A
Date: Wednesday, August 05, 2009	Sheet 19 of 56		

IBEXPEAK - M (HDA,JTAG,SATA)



		Pre-Production Systems		Production Systems
PCH Pin	RefDes	ES1	ES2	
TDO	R1	No Stff	200 Ohms	No Stuff
	R2	No Stff	100 Ohms	No Stuff
TMS	R3	200 Ohms	200 Ohms	No Stuff
	R4	100 Ohms	100 Ohms	No Stuff
TDI	R5	200 Ohms	200 Ohms	No Stuff
	R6	100 Ohms	100 Ohms	No Stuff
TCK	R7	51 Ohms	51 Ohms	51 Ohms
TRST#	R8	20K Ohms	Not Applicable[1]	Not Applicable[1]
	R9	10K Ohms	Not Applicable[1]	Not Applicable[1]

Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes

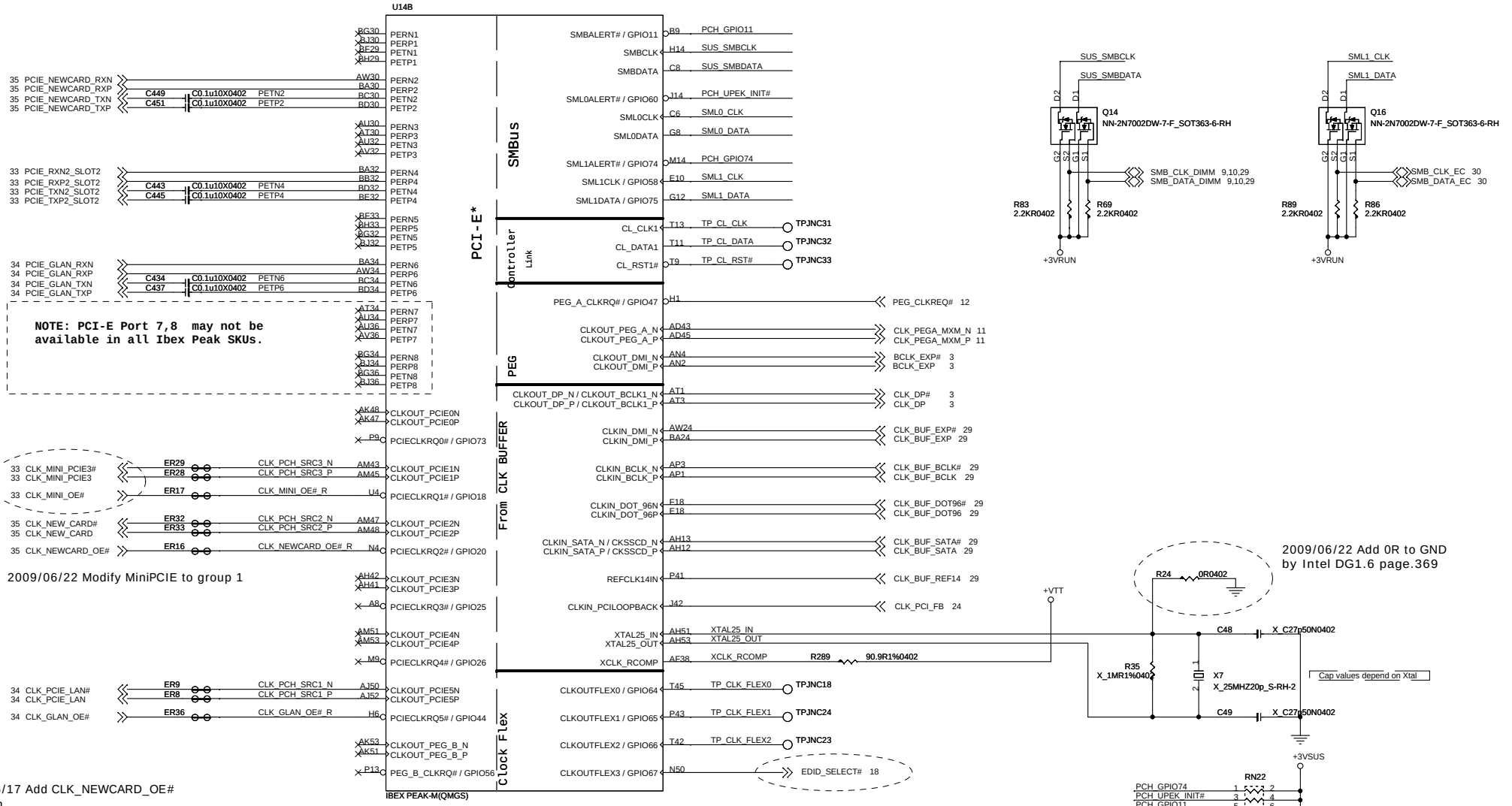
MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK - M (HDA,JTAG,SATA)

Size: Custom | Document Number: MS-145X | Rev: 0A

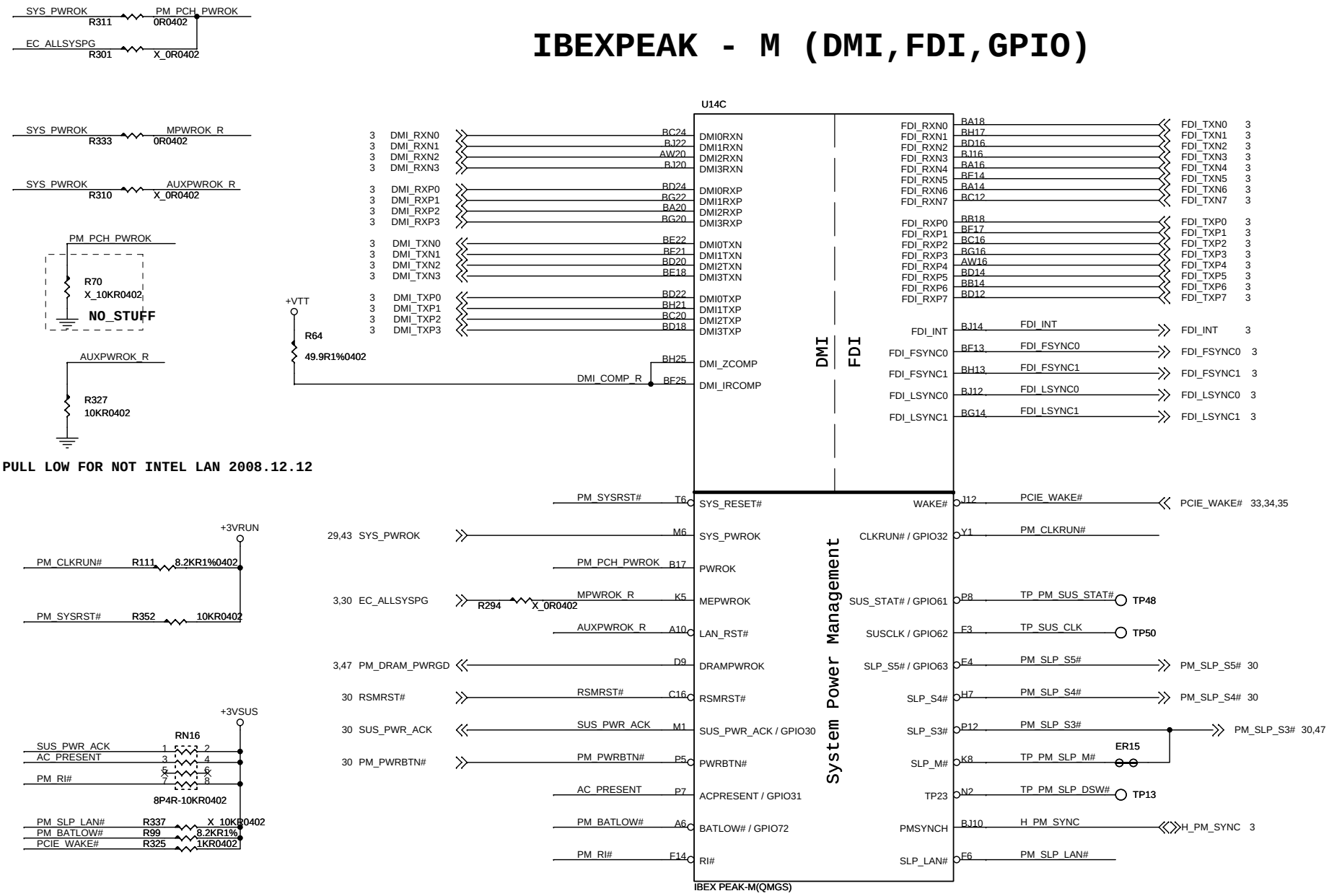
Date: Wednesday, August 05, 2009 | Sheet 20 of 56

IBEXPEAK - M (PCI-E,SMBUS,CLK)



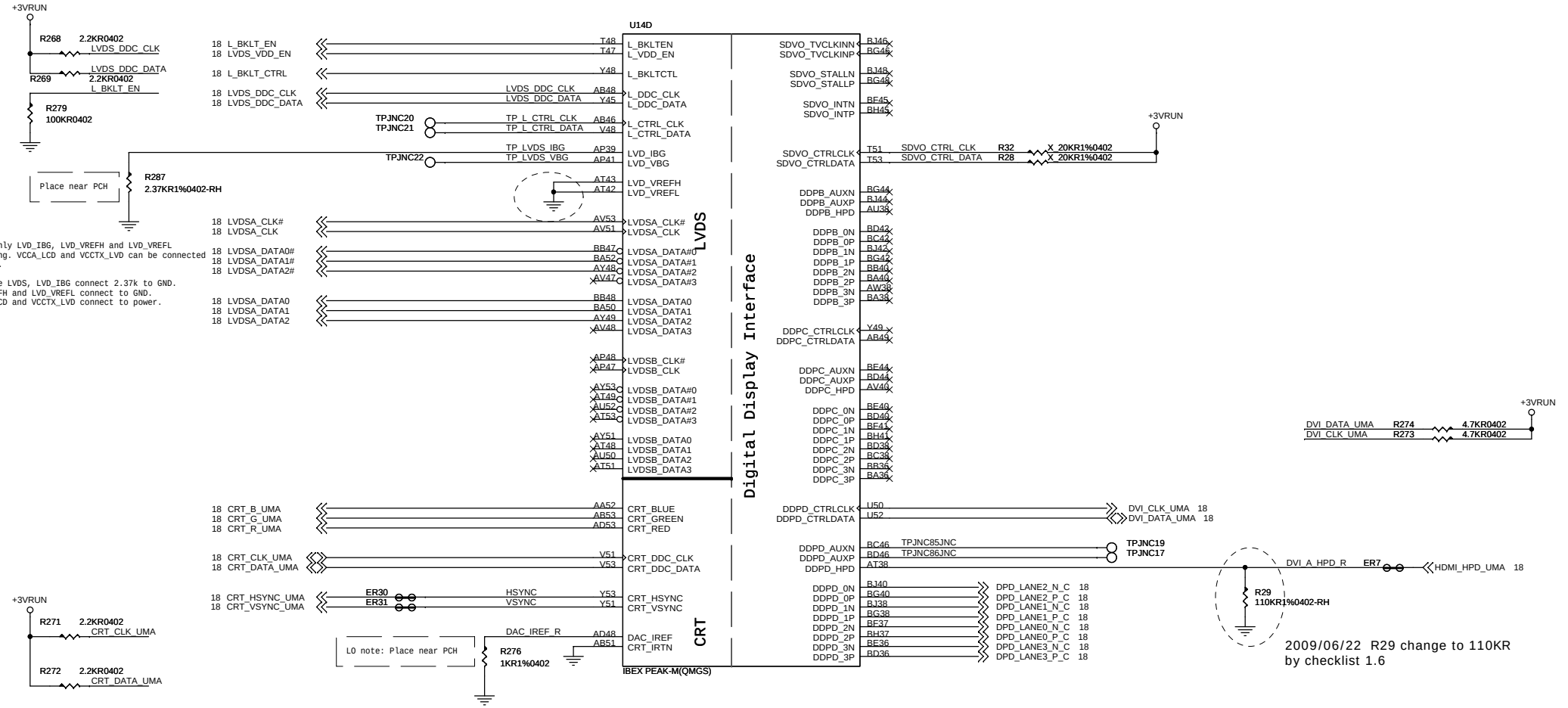
MICRO-STAR INT'L CO.,LTD.
Title: IBEXPEAK - M (PCI-E,SMBUS,CLK)
Size: Custom | Document Number: MS-145X | Rev: 0A
Date: Wednesday, August 05, 2009 | Sheet 21 of 56

IBEXPEAK - M (DMI,FDI,GPIO)



MICRO-STAR INT'L CO.,LTD.	
Title	IBEXPEAK - M (DMI,FDI,GPIO)
Size: Custom	Document Number: MS-145X
Rev: 0A	
Date: Wednesday, August 05, 2009	Sheet 22 of 56

IBEXPEAK - M (LVDS,DDI)



DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_L3#	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK - M (LVDS,DDI)

Size: Custom | Document Number: MS-145X | Rev: 0A

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IBEXPEAK - M (PCI,USB,NVRAM)

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

2009/06/26 For DGPU_SELECT# driving reserved
(No need for MS-1454)
R367 not stuff for MS-1454

PCI_GNT#0
PCI_GNT#1
R280 X_1KR0402
R277 X_1KR0402
PCI_GNT#3
DGPU_PWM_SELECT#
R275 X_1KR0402
R291 X_1KR0402
R367 0R0402
+3VRUN
R31 X_10KR0402
R36 X_10KR0402
18 DGPU_SELECT#
Q7 X_NN-2N7002DW-7-F_SOT363-6-RH
18 DGPU_PWM_SELECT#
TP51 TP_PCI_PME#
21 CLK_PCI_FB
30 CLK_PCI_KBC
30 CLK_PCIE_PORT80
EC8 X_C10p50N0402
EC27 X_C10p50N0402
EC7 X_C10p50N0402

U14E

PCI: AD0–AD31, C/BE0#–C/BE3#, PIRQA#–PIRQD#, REQ0#–REQ3# / GPIO50–GPIO54, GNT0#–GNT3# / GPIO51–GPIO55, PCIRST#, SERR#, PERR#, IRDY#, PAR, DEVSEL#, FRAME#, PLOCK#, STOP#, TRDY#, PME#, PLTRST#, CLKOUT_PCI0–CLKOUT_PCI4

NVRAM: NV_CE#0–NV_CE#3, NV_DQS0, NV_DQS1, NV_DQ0 / NV_IO0 – NV_DQ15 / NV_IO15, NV_ALE, NV_CLE, NV_RCOMP, NV_RB#, NV_WR#0_RE#, NV_WR#1_RE#, NV_WE#_CK0, NV_WE#_CK1

USB: USBP0N/P – USBP13N/P, USBRBIAS#, USBRBIAS, OC0# / GPIO59 – OC7# / GPIO14

IBEX PEAK-M(QMGS)

R107 X_32.4R1%0402-RH
R303 22.6R1%0402
R314 10KR0402

NOTE: USB Port 6,7 may not be available in all Ibex Peak SKUs.

USB_PN1 33, USB_PP1 33, USB_PN2 33, USB_PP2 33, USB_PN3 36, USB_PP3 36, USB_PN4 36, USB_PP4 36, USB_PN5 36, USB_PP5 36, USB_PN8 37, USB_PP8 37, USB_PN9 35, USB_PP9 35, USB_PN6 33, USB_PP6 33

CLK_PCI_FB R34 22R0402 CLKOUT_PCI1
CLK_PCI_KBC R283 22R0402 CLKOUT_PCI2
CLK_PCIF_PORT80 R33 22R0402 CLKOUT_PCI3

+3VRUN
RN10 8P4R-8.2KR0402-1: PCI_REQ#1, PCI_FRAME#, PCI_TRDY#, INT_PIRQH#
RN9 8P4R-8.2KR0402-1: PCI_REQ#0, INT_PIRQB#, INT_PIRQF#, PCI_REQ#3
RN12 8P4R-8.2KR0402-1: INT_PIRQG#, INT_PIRQC#, INT_PIRQE#, PCI_STOP#
RN21 8P4R-8.2KR0402-1: PCI_LOCK#, PCI_PERR#, PCI_DEVSEL#, INT_PIRQA#
RN11 8P4R-8.2KR0402-1: PCI_IRDY#, PCI_SERR#, INT_PIRQD#, PCI_REQ#2
DGPU_PWM_SELECT# R288 10KR0402

Not stuff for MS-1454
+3VSUS
C151 C0.1u10X0402
U21 S08P5X_SC70
PLT_RST#
25 DGPU_HOLD_RST#
PCIE_RST# 11

+3VSUS
C128 C0.1u10X0402
U19 S08P5X_SC70
RN18 8P4R-33R0402
LAN_RST# 34
LPC_RST# 30
NEWCARD_RST# 35
WLAN_RST# 33
R98 X_0402
BUF_PTL_RST# 3

MSI MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK - M (PCI,USB,NVRAM)

Size: Custom | Document Number: MS-145X | Rev: 0A

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IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)

2009/07/01 Combine Park 1.8V and 1.0V to DGPU_PWROK

Not stuff for MS-1454(UMA only)

R278 X_0R0402
DGPU_HPD_INTR_R#
12 DGPU_HPD_INTR#
Q24 X_N-2N7002_SOT23

Not stuff for MS-1454(UMA only)

+3VRUN
R284 10KR0402
R257 0R0402 +1_8VRUN_PARK_PWRGD 45
R256 0R0402 +1_0VRUN_PARK_PWRGD 45
12 DGPU_PWROK

U14F

MISC
S_GPIO0 Y3 BMBUSY# / GPIO0
30 KBSMI# C38 TACH1 / GPIO1
DGPU_HPD_INTR_R# D37 TACH2 / GPIO6
30 KBSCI# J32 TACH3 / GPIO7
HOST_ALERT#2 F10 GPIO8
TP45 PM_LANPHY_EN K9 LAN_PHY_PWR_CTRL / GPIO12
HOST_ALERT#1 T7 GPIO15
24 DGPU_HOLD_RST# DGPU_HOLD_RST# AA2 SATA4GP / GPIO16
DGPU_PWROK F38 TACH0 / GPIO17
BIOS_REC Y7 SCLOCK / GPIO22
TP49 TP_UPEK_PWR_EN H10 MEM_LED / GPIO24
SATA_PWR_EN#0 AB12 GPIO27
SPI_CS#2 V13 GPIO28
STP_PCI# M11 STP_PCI# / GPIO34
SATA_PWR_EN#1 V6 SATACLKREQ# / GPIO35
DGPU_PWR_EN# AB7 SATA2GP / GPIO36
DGPUPRSNT# AB13 SATA3GP / GPIO37
MFG_MODE V3 SLOAD / GPIO38
CRB_SV_DET P3 SDATAOUT0 / GPIO39
SPI2_SO H3 PCIECLKRQ6# / GPIO45
47 RS_GATE# SPI2_SI F1 PCIECLKRQ7# / GPIO46
SV_SET_UP AB6 SDATAOUT1 / GPIO48
30 CRIT_TEMP_REP#_R CRIT_TEMP_REP#_R AA4 SATA5GP / GPIO49
GPIO57 F8 GPIO57

GPIO

CPU
CLKOUT_PCIE6N AH45
CLKOUT_PCIE6P AH46
CLKOUT_PCIE7N AF48
CLKOUT_PCIE7P AF47
A20GATE U2 H_A20GATE 30
CLKOUT_BCLK0_N / CLKOUT_PCIE8N AM3 BCLK_CPU# 3
CLKOUT_BCLK0_P / CLKOUT_PCIE8P AM1 BCLK_CPU 3
PECI BG10 H_PECI_R ER14 H_PECI 3
RCIN# T1 KBRST# 30
PROCPWRGD BE10 H_CPUPWRGD 3
THRMTRIP# BD10 PCH_THRMTRIP#_R R329 56R1%0402 R330 56R0402 H_THRMTRIP# 3

+3VRUN
R353 10KR0402

+3VSUS
R346 10KR0402
R117 10KR0402

+3VSUS
R345 X_10KR0402
SATA_PWR_EN#0
R332 X_10KR0402
SATA_PWR_EN#1
R343 10KR0402

+3VSUS
HOST_ALERT#1 R344 X_1KR0402
HOST_ALERT#2 R335 10KR0402
SPI_CS#2 R341 10KR0402
GPIO57 R336 X_10KR0402
R334 10KR0402
DGPU_HOLD_RST# R110 X_10KR0402
HOST_ALERT#2 R328 X_1KR0402

Retain 25-MHz crystal footprint on your platform.
---Though FCIM will not be available, retaining the footprint will allow Intel and customer to test and evaluate FCIM for future platforms.
---25-MHz crystal and associated capacitor footprints only are requested - components do not need to be populated.
---Keep 1K Ohm resistor un-stuffed to GND on Ibex Peak GPIO8.

+3VRUN
DGPU_PWR_EN# R339 1KR0402
RN25
CRIT_TEMP_REP#_R
DGPU_HPD_INTR#
STP_PCI#
8P4R-10KR0402
DGPU_HOLD_RST# R338 X_10KR0402
RN17
SV_SET_UP
S_GPIO0
MFG_MODE
8P4R-10KR0402
CRB_SV_DET R123 X_10KR0402
R109 10KR0402
DGPU_PWROK R286 X_10KR0402
DGPUPRSNT# R322 10KR0402

2009/07/02 Stuff R316 and not stuff R322 for MS-1454

+3VRUN
DGPUPRSNT# R316 X_10KR0402

NCTF
VSS_NCTF_1 A4
VSS_NCTF_2 A49
VSS_NCTF_3 A5
VSS_NCTF_4 A50
VSS_NCTF_5 A52
VSS_NCTF_6 A53
VSS_NCTF_7 B2
VSS_NCTF_8 B4
VSS_NCTF_9 B52
VSS_NCTF_10 B53
VSS_NCTF_11 BE1
VSS_NCTF_12 BF53
VSS_NCTF_13 BF1
VSS_NCTF_14 BF53
VSS_NCTF_15 BH1
VSS_NCTF_16 BH2
VSS_NCTF_17 BH52
VSS_NCTF_18 BH53
VSS_NCTF_19 BJ1
VSS_NCTF_20 BJ2
VSS_NCTF_21 BJ4
VSS_NCTF_22 BJ49
VSS_NCTF_23 BJ5
VSS_NCTF_24 BJ50
VSS_NCTF_25 BJ52
VSS_NCTF_26 BJ53
VSS_NCTF_27 D1
VSS_NCTF_28 D2
VSS_NCTF_29 D53
VSS_NCTF_30 E1
VSS_NCTF_31 E53

RSVD
TP1 BA23
TP2 AW22
TP3 BB23
TP4 AY45
TP5 AY46
TP6 AV43
TP7 AV45
TP8 AE13
TP9 M18
TP10 N18
TP11 AJ24
TP12 AK41
TP13 AK42
TP14 M32
TP15 N32
TP16 M30
TP17 N30
TP18 H12
TP19 AA23
NC_1 AB45
NC_2 AB38
NC_3 AB43
NC_4 AB41
NC_5 T39
INIT3_3V# P6
TP24 C10

IBEX PEAK-M(QMGS)

+3VRUN
U24
DGPU_PWR_EN# 2
DGPU_PWR_EN 12,45
SN74LVC1G04DBV_SOT23-5-RH

Not stuff for MS-1454(UMA only)

MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK-M(GPIO,VSS_NCTF,RSVD)

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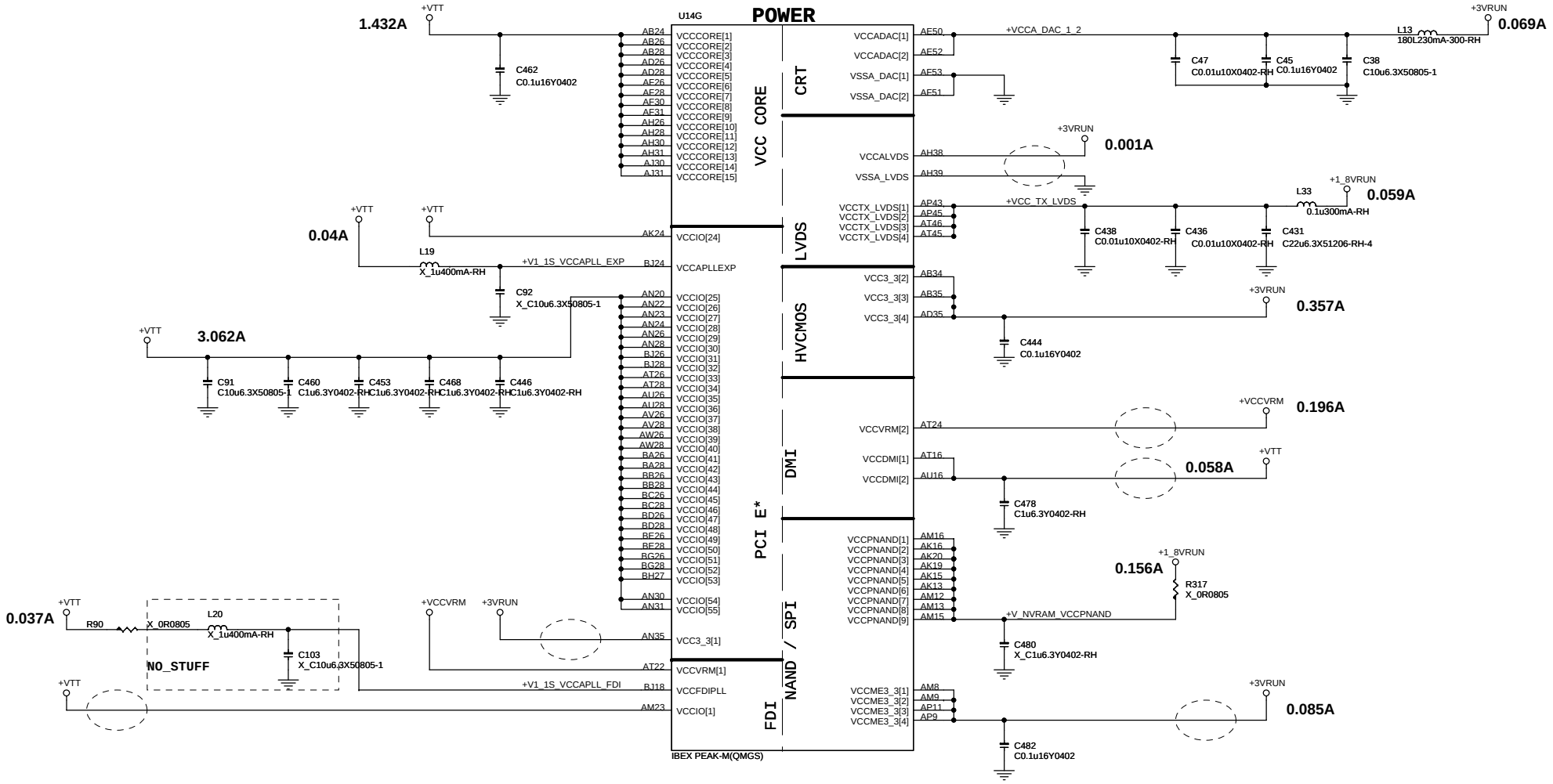
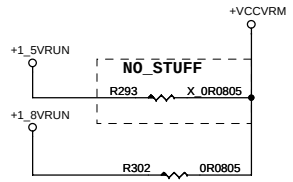
IBEXPEAK - M (POWER)



The VCCVRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAClk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.



MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK - M (POWER)

Size: Custom | Document Number: MS-145X | Rev: 0A

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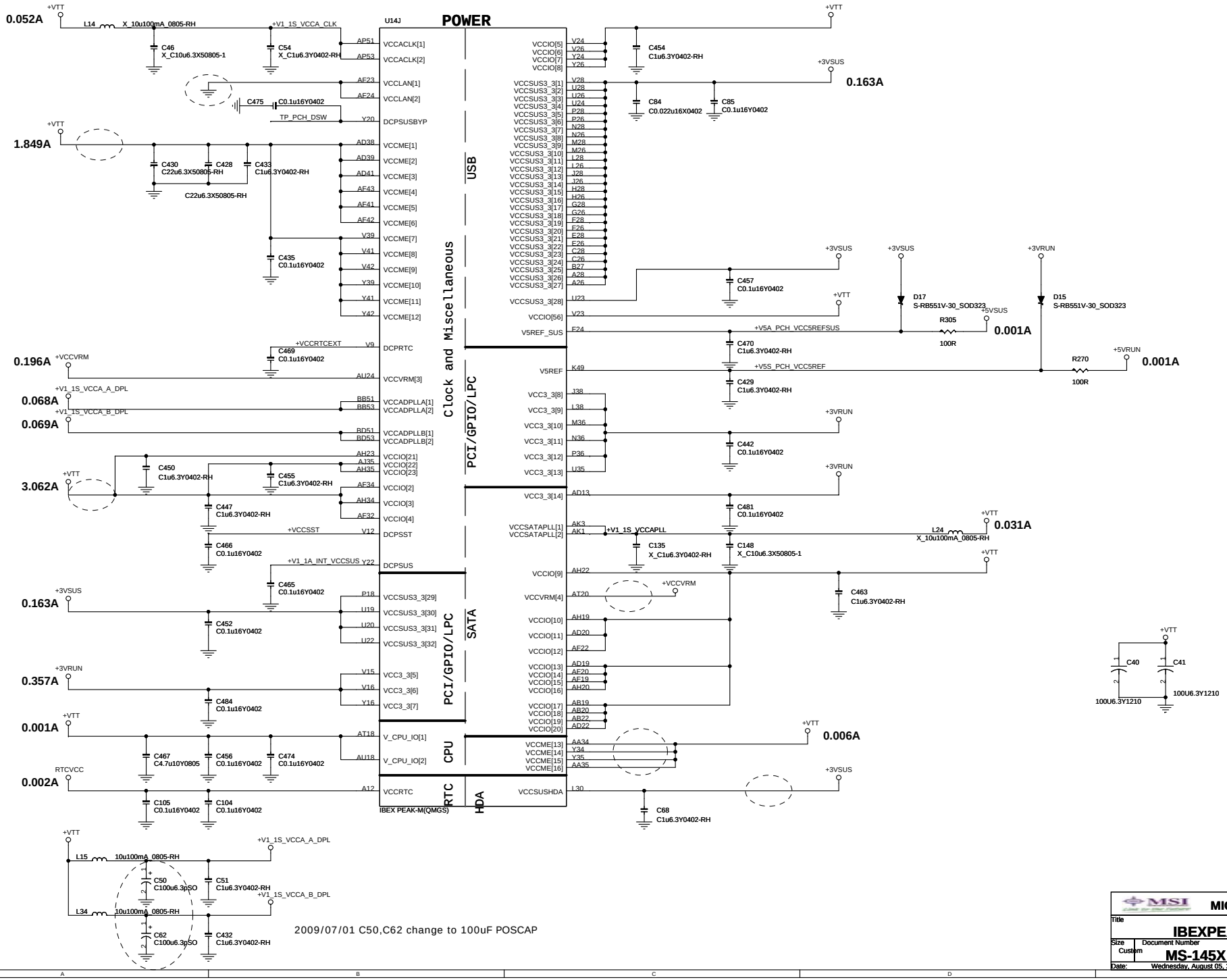
IBEXPEAK - M (POWER)



2009/07/01 C50,C62 change to 100uF POSCAP

MSI	MICRO-STAR INT'L CO.,LTD.		
Title	IBEXPEAK - M (POWER)		
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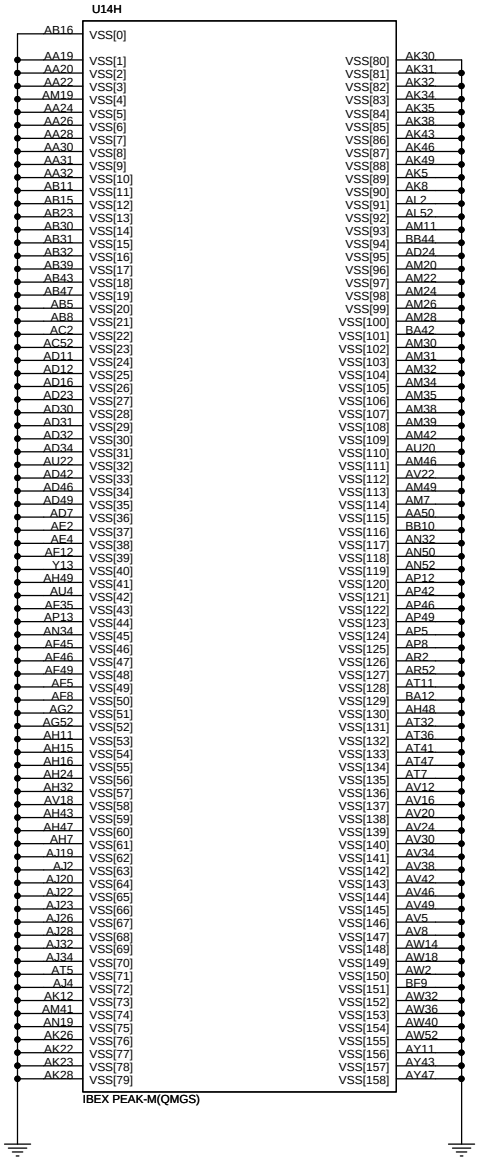
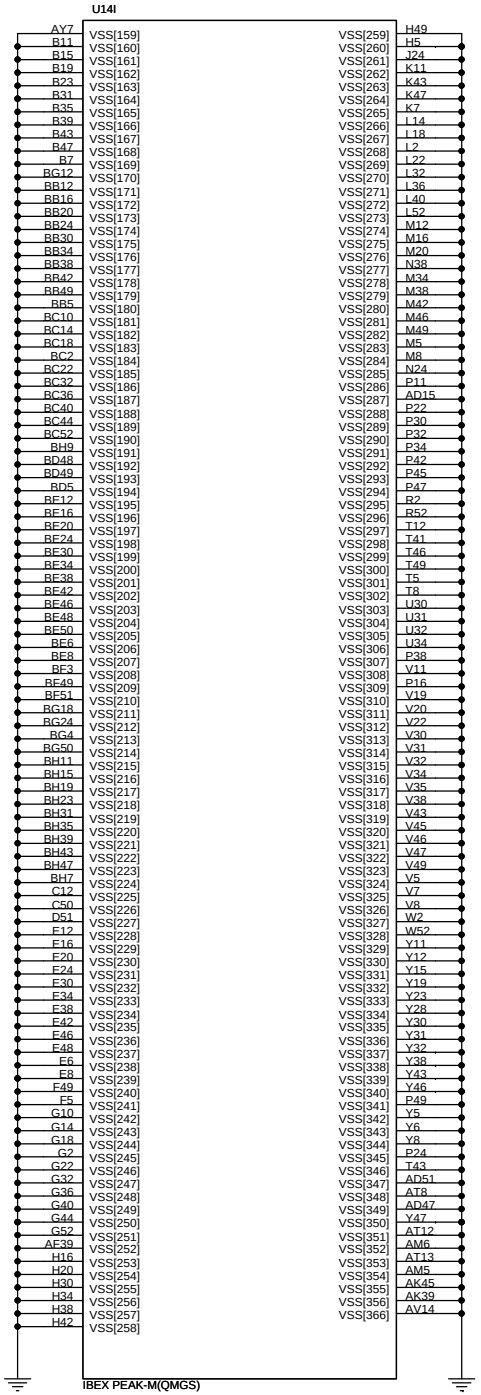
IBEXPEAK - M (GND)





MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK - M (GND)

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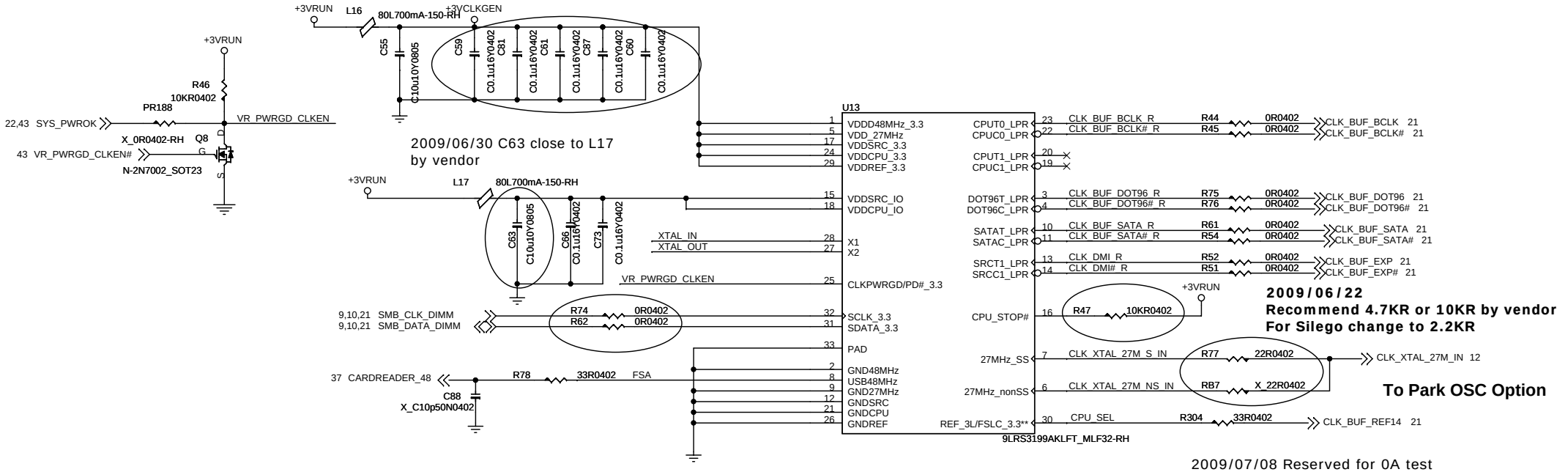
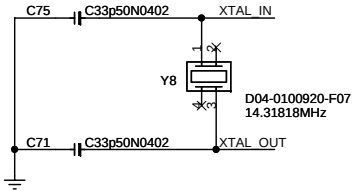
C59 Close to L16 ; C60,C61,C81,C87 Close to power pin



2009/07/08 Reserved for 0A test
R3211 is for Spread clock(Default use)
RB8 is for non-Spread clock

2009/07/08
Y4換成49S type(cost down as MS-1122)

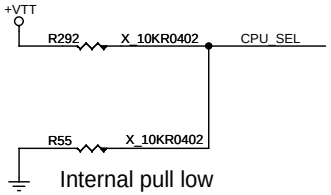


Capacity select

If Cload=20pf C71/C75=33pf

If Cload=32pf C71/C75=56pf

2009/06/30 R292 not stuff



Internal pull low

For CPU frequency select (133MHz)

CPU_SEL	CPU0	CPU1
0(Default)	133MHz	133MHz
1(1.05~1.5V)	100MHz	100MHz

Clock GEN. Vendor Table

	9LRS3199	SLG8SP587V
VDDIO spec	0.9975~3.465	1.05~3.466
BOM	R39 stuff	R40 stuff

MICRO-STAR INT'L CO.,LTD.

Title: Clock Generator (9LRS3199AKLFT)

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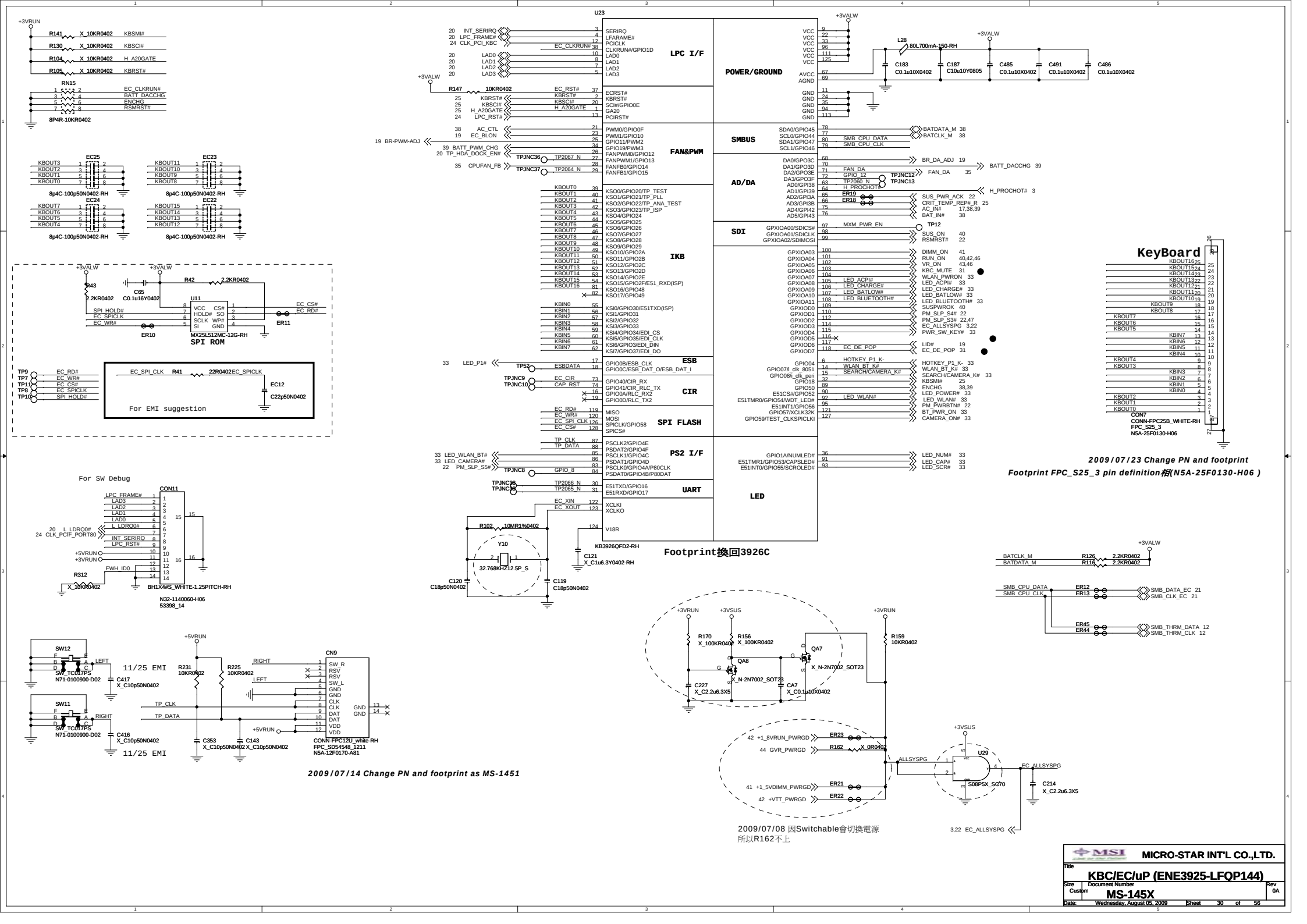
U23
LPC I/F
FAN&PWM
IKB
ESB
CIR
SPI FLASH
PS2 I/F
UART
POWER/GROUND
SMBUS
AD/DA
SDI
LED
KB3926QFD2-RH
Footprint換回3926C
SPI ROM
MX25L512MC-12G-RH
KeyBoard
CON7
CONN-FPC25B_WHITE-RH
FPC_S25_3
N5A-25F0130-H06
2009/07/23 Change PN and footprint
Footprint FPC_S25_3 pin definition按(N5A-25F0130-H06)
For SW Debug
CON11
BH1X4#S_WHITE-1.25PITCH-RH
N32-1140060-H06
53398_14
For EMI suggestion
11/25 EMI
CN9
CONN-FPC12U_white-RH
FPC_SD54548_1211
N5A-12F0170-A81
2009/07/14 Change PN and footprint as MS-1451
2009/07/08 因Switchable會切換電源
所以R162不上
MICRO-STAR INT'L CO.,LTD.
KBC/EC/uP (ENE3925-LFQP144)
MS-145X
Wednesday, August 05, 2009
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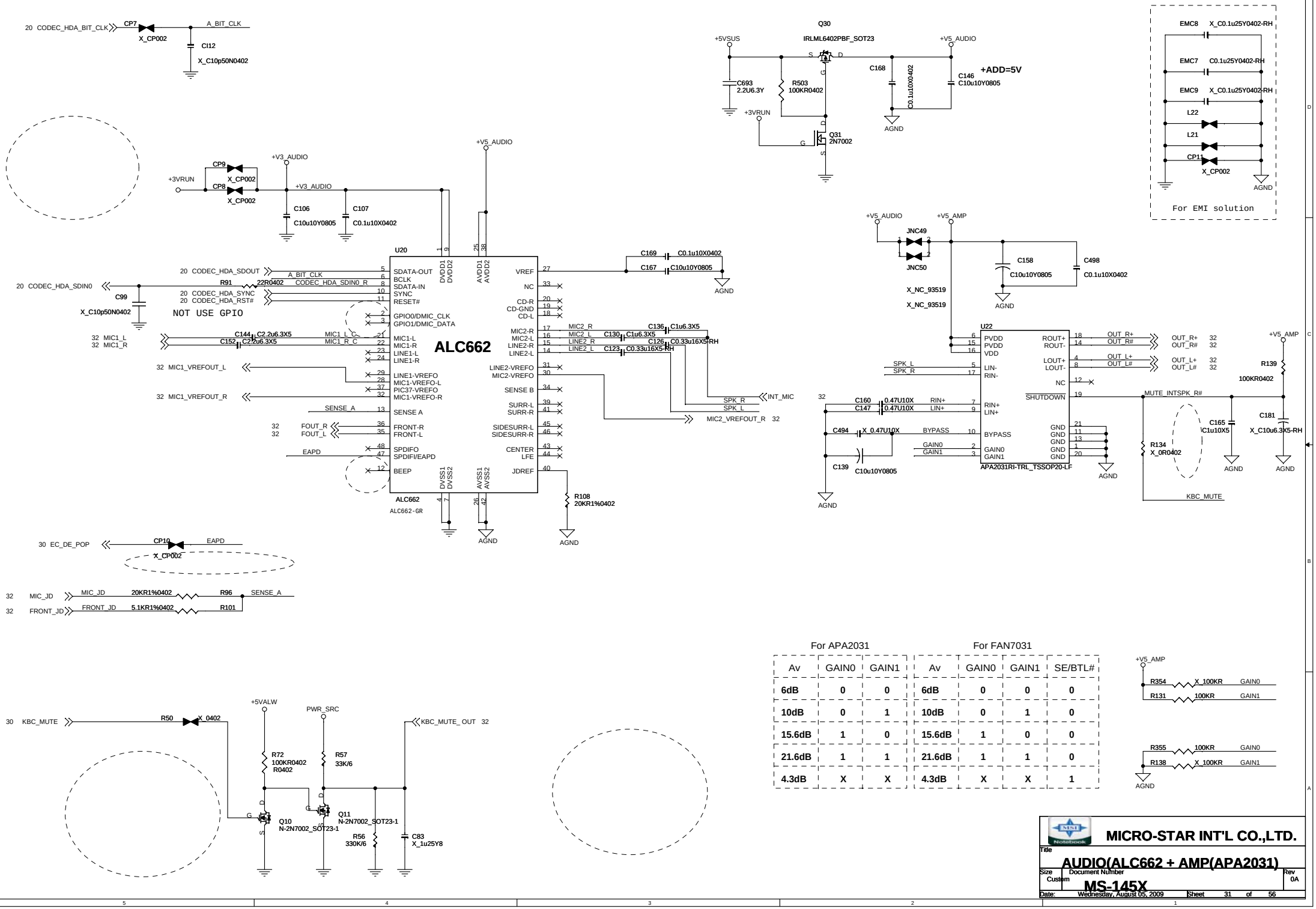

For APA2031

Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

For FAN7031

Av	GAIN0	GAIN1	SE/BTL#
6dB	0	0	0
10dB	0	1	0
15.6dB	1	0	0
21.6dB	1	1	0
4.3dB	X	X	1

MICRO-STAR INT'L CO.,LTD.

Title: AUDIO(ALC662 + AMP(APA2031)

Size: Custom | Document Number: MS-145X | Rev: 0A

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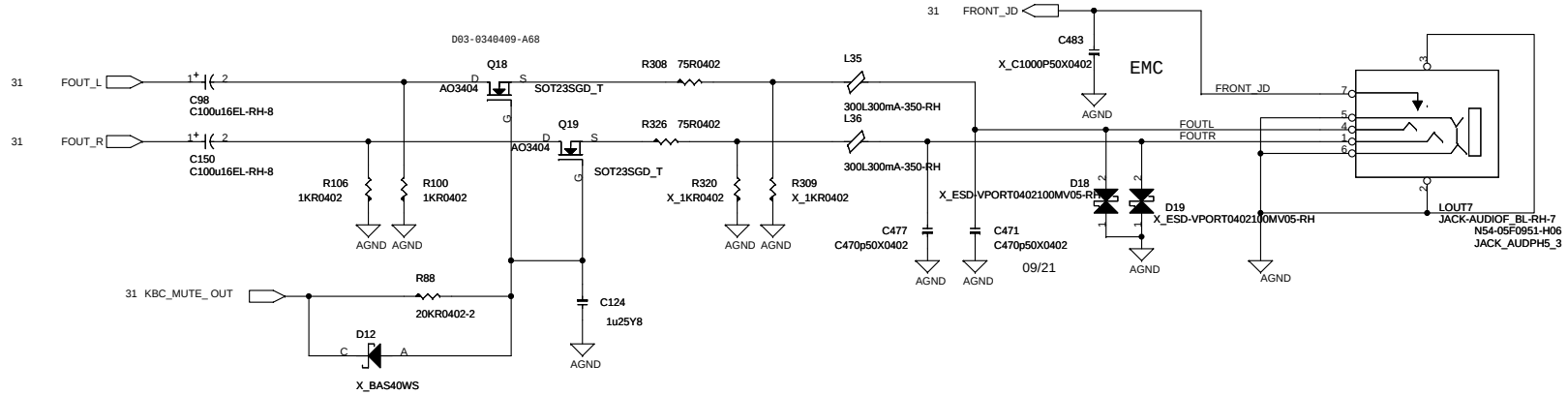
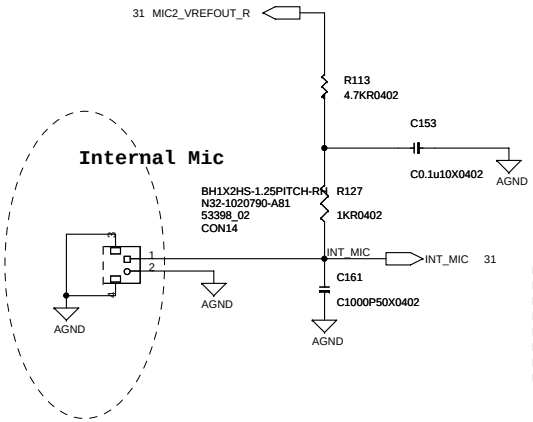
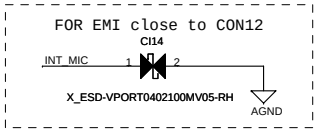
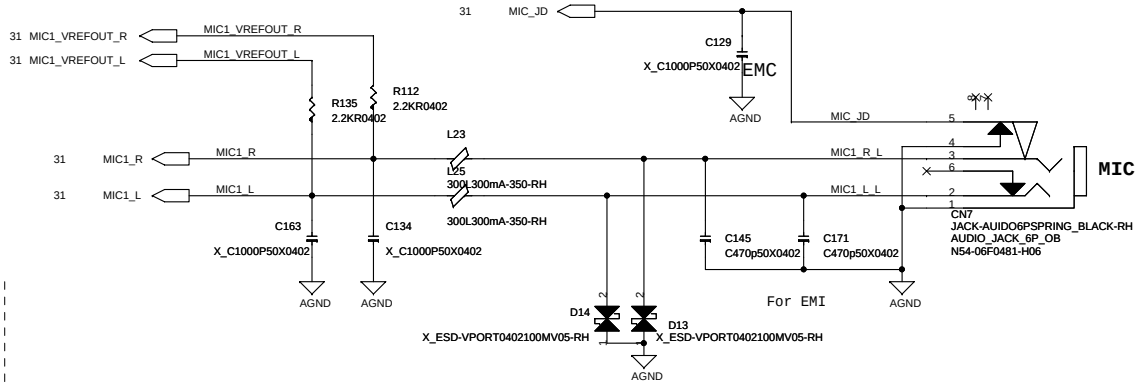
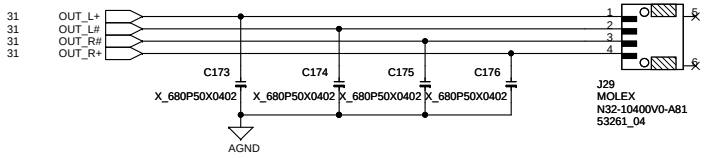








2009/06/29 Modify internal MIC PN to N32-1020790-A81



MICRO-STAR INT'L CO.,LTD.

Title: SPK / HP / MIC

Size: Custom | Document Number: MS-145X | Rev: 0A

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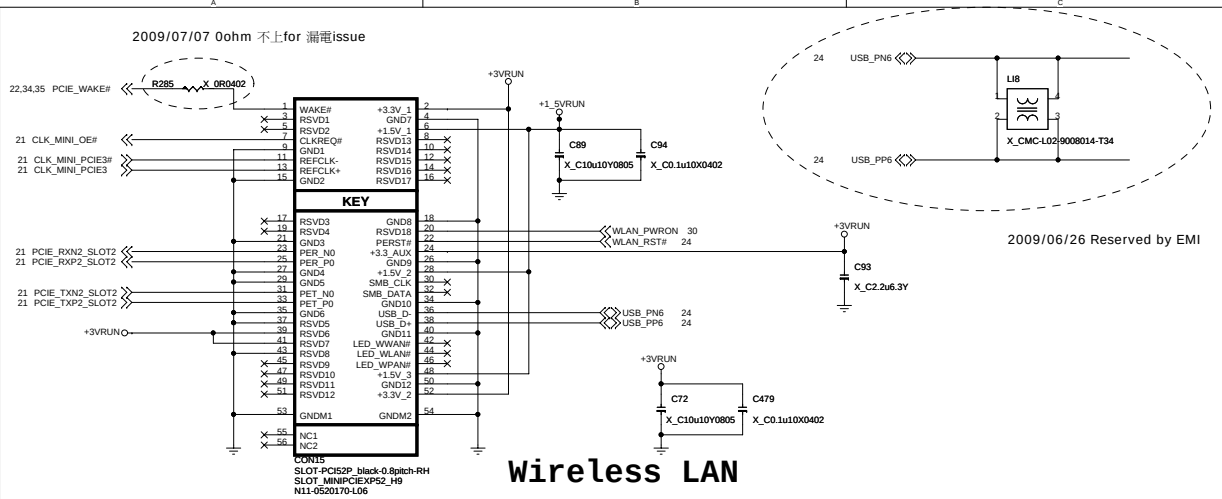
2009/07/07 0ohm 不上for 漏電issue

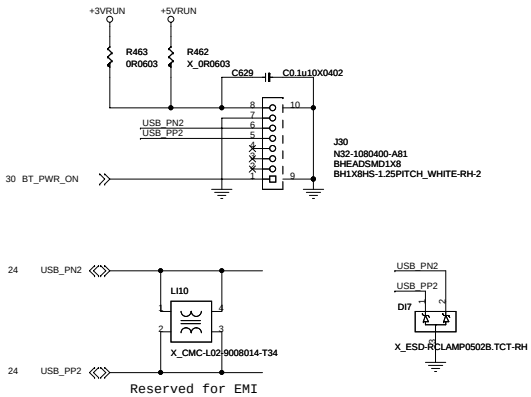


2009/06/26 Reserved by EMI

Wireless LAN

BLUETOOTH

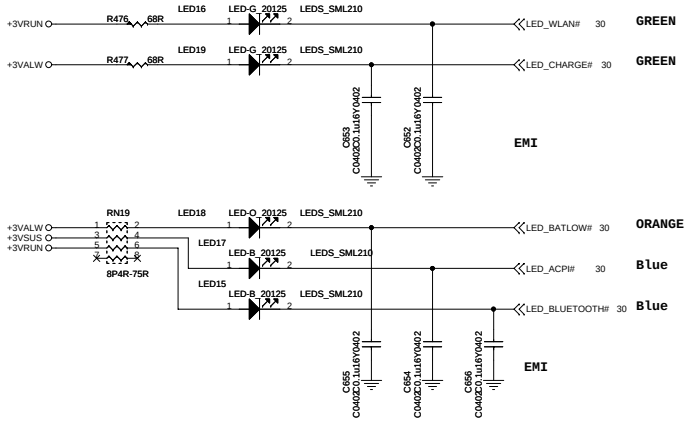
2009/05/11 修改 for new MS-3801



Reserved for EMI

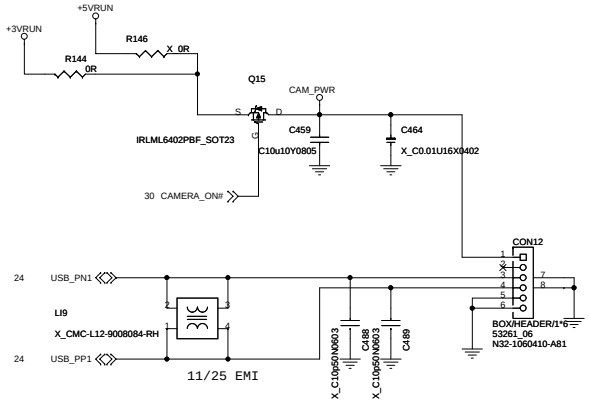
LED light

del CN8 0716



CAMERA

2009/06/29 Reserved 0 ohm pad by EMI

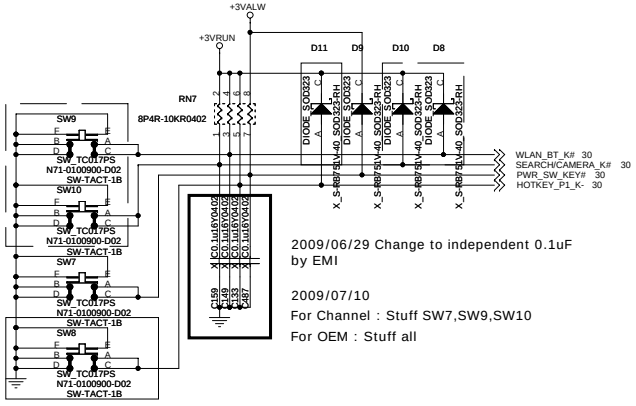


11/25 EMI

	LED7 SW7	LED8 SW8	LED9 SW9	LED10 SW10
1453	Stuff	Nostuff	Discreate	UMA
1454	Stuff	Nostuff	P1	IE
OEM	Stuff	P1	Wireless	Camera

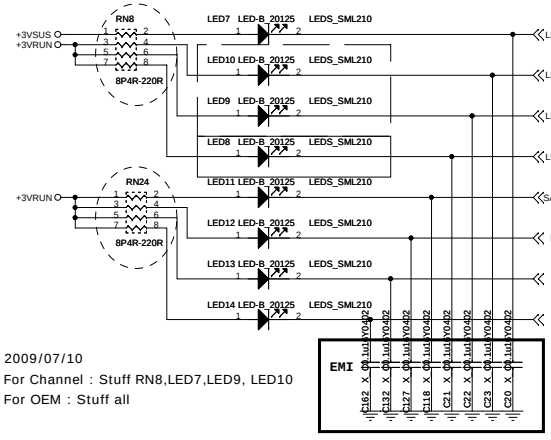
Stuff for CHANNEL ——— ———

Stuff for OEM ———



2009/06/29 Change to independent 0.1uF by EMI

2009/07/10
For Channel：Stuff SW7,SW9,SW10
For OEM：Stuff all



2009/07/10
For Channel：Stuff RN8,LED7,LED9, LED10
For OEM：Stuff all

Title	MSI CORPORATION
	MINIPCIE,CAMERA,BLUETOOTH,SW
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+3VSUS J38 IDD33 VDD33

X_NC_93519

C677
C22u6.3X50805-RH
C0805_67

IDD33 = Icc33 + ICC12
= 58mA + 289mA
= 347mA

R495 is only required by RTL8102EL

R495
X_1KR0402
R0402

U47
EECS_LAN
LED1/EESK
LED2/EEDI
LED3/EEDO
CS VCC
SK NC
DI ORG
DO GND
X_AT93C46DN-SH-T-RH

R498
3.6K
R0402
+3VSUS

C678 is only RTL8111DL

C678
C22u6.3X50805-RH
C0805_67

C679
C0.1u10X0402
C0402

R496 is only RTL8111DL

R496
0R0402
R0402

Close to LAN

R497
2.49KR1%0402
R0402

C17
C27p50N
C0402
C18
C27p50N
C0402
Y7
25MHZ20p
TXC7A
XTAL2
XTAL1

L12
CH-4.7u1.24A
CHK_S2_2_9

R500
X_0R
R0603

C683
C22u6.3X50805-RH
C0805_67

C684
C0.1u10X0402
C0402

C685
C22u6.3X50805-RH
C0805_67

R499
0R
R0603

C686
1U 0402
C0402
LAN_GND

EVDD12

Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.

For RTL8111DL,use this block

R501
0R0402
R0402
CTRL12/VDD

For RTL8102EL/8103EL,use this block

R502
X_0R0402
R0402
CTRL12/VDD

U9

RTL8111DL

RTL8111DL-GR-RH

Close to LAN

C687 C0.1u10X0402
C688 C0.1u10X0402
C691 C0.1u10X0402
C692 C0.1u10X0402
C0402

C42
1U 0402
C0402

R22
1KR0402

R21
15KR1%0402

+3VRUN

LAN_RST# 24
PCIE_WAKE# 22,33,35
CLK_GLAN_OE# 21

21 PCIE_GLAN_TXP
21 PCIE_GLAN_TXN

PCIE_GLAN_RXN_C C44 C0.1u10X0402
PCIE_GLAN_RXP_C C43 C0.1u10X0402

PCIE_GLAN_RXN 21
PCIE_GLAN_RXP 21

CLK_PCIE_LAN# 21
CLK_PCIE_LAN 21

MDC CONN

CN12
TS
RING
CN_TS
CN_RING
L11
1000L400m_450_0805
L7
1000L400m_450_0805

BH1X2S_white-1.25pitch
N32-1020650-H06
SD_53780_0210

CN11
RJ11
RJ45

LTK_RJ4511ROS_RJ4511
N55-12F0110-AF2
RJ45_RJ11_SMT_14P

RN20
MCT1
MCT2
MCT3
MCT4
8P4R-75R
RN0402_MSI
EC2
C1000p50N
C0805_67

LAN MAGNETICS

Close to Transfomer

T7
C674 C0.1u10X
C675 C0.1u10X
C676 C0.1u10X
C673 C0.1u10X
V_DAC
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
TCT1
TD1+
TD1-
TCT2
TD2+
TD2-
TCT3
TD3+
TD3-
TCT4
TD4+
TD4-
MCT1
MX1+
MX1-
MCT2
MX2+
MX2-
MCT3
MX3+
MX3-
MCT4
MX4+
MX4-
GST5009 LF-RH

R20
X_NC_93519
LAN_GND

2009/06/24 Modify as 1451

MSI MICRO-STAR INT'L CO.,LTD.

Title: PCIE 1G LAN (RTL8111DL)

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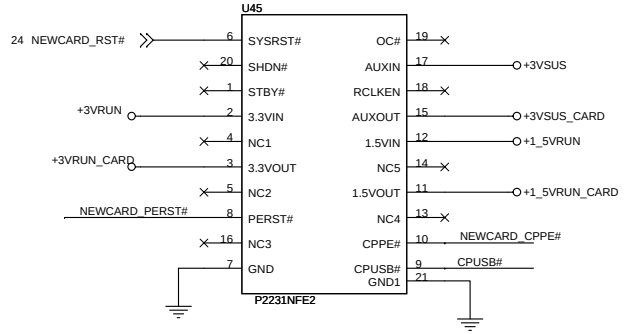
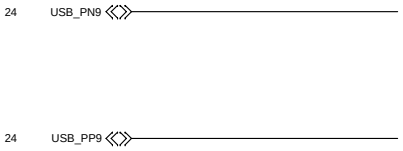
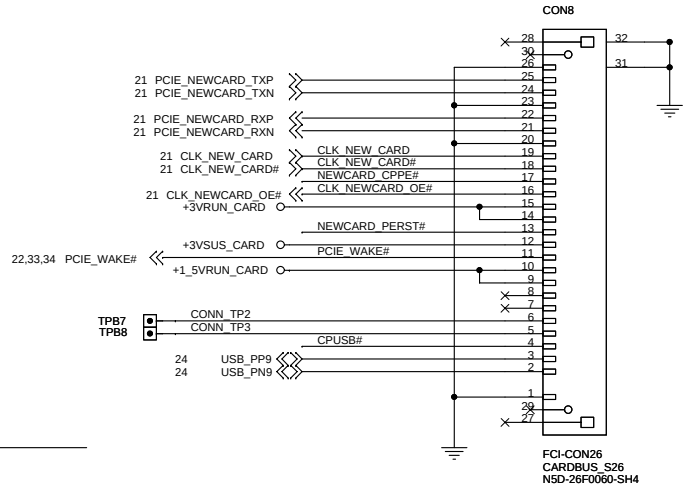
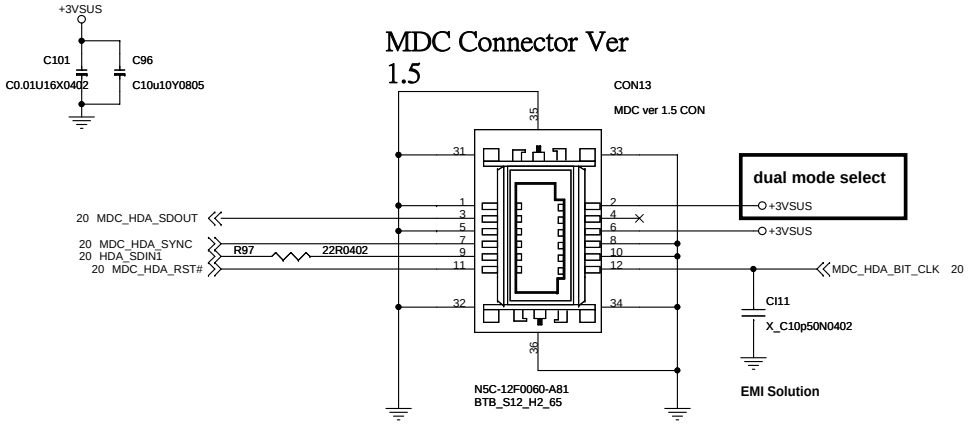
NEW CARD





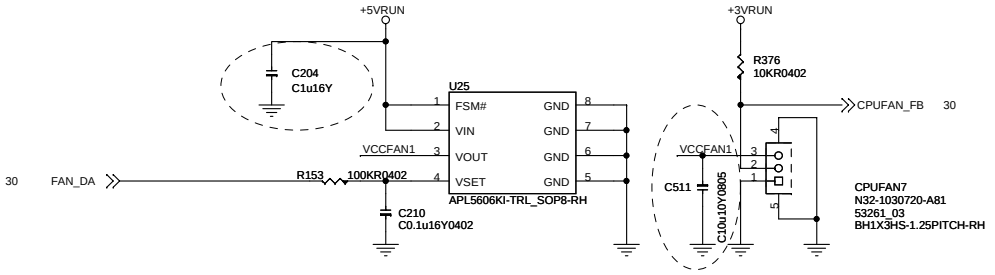


MDC Connector



2009/07/14 因限高問題,改回1451用料N5C-12F0060-A81

CPU FAN



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	NEWCARD,FAN	
Size: Custom	Document Number: MS-145X	Rev: 0A
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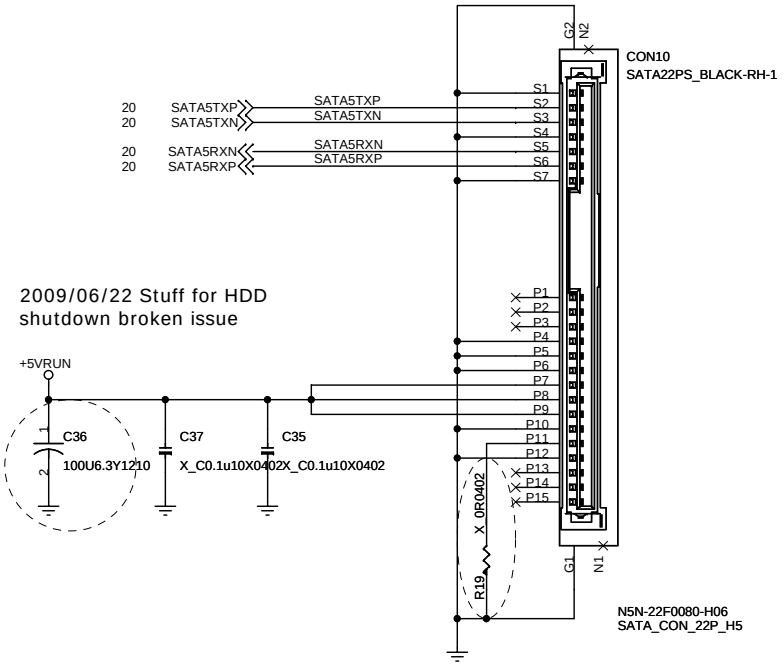
SATA HDD

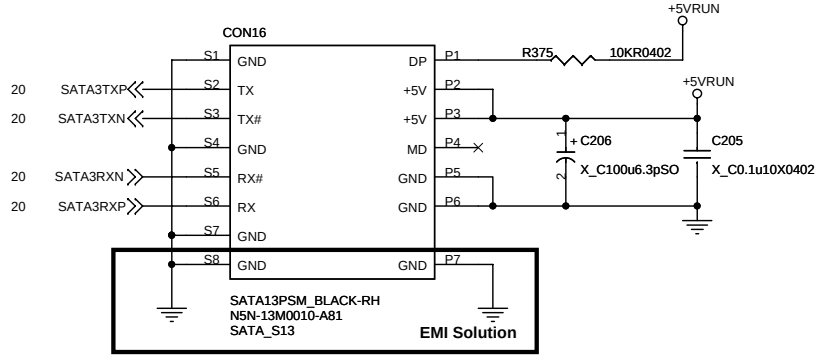


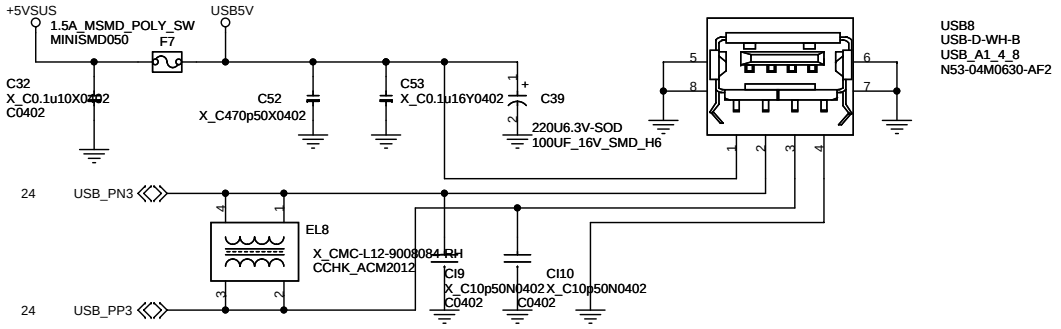
2009/06/22 SATA HDD P11 is Staggered Spinup function

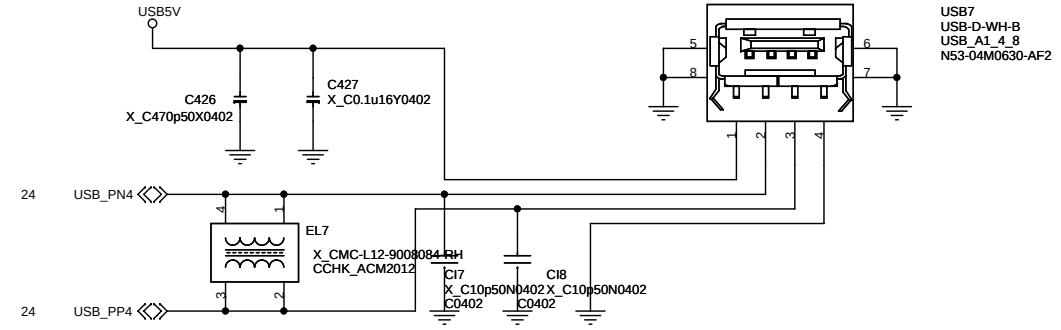
Staggered Spinup :

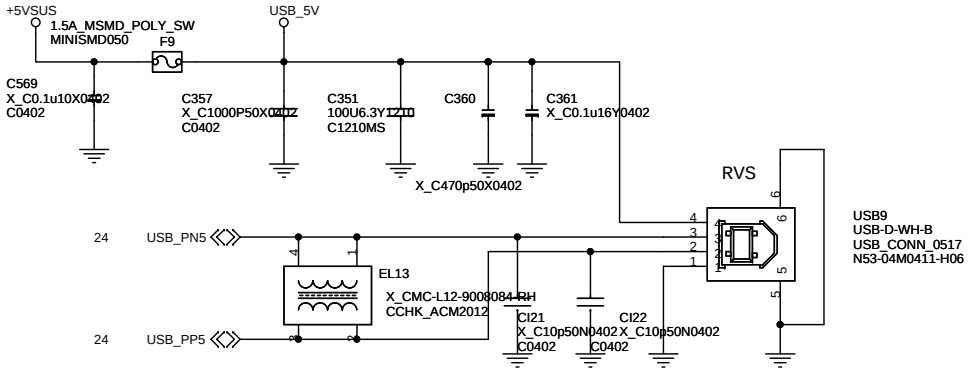
如果system 支援這個功能,開機時 HDD 的馬達是不轉的,
BIOS 必須下command 把 HDD wake up,才能做偵測HDD的動作
如果不支援Staggered Spinup 這個function 這隻腳必須接地

SATA ODD









2009/07/07 USB common choke先不上

MSI MICRO-STAR INT'L CO.,LTD.

Title: **HDD,CDROM,USB**

Size	Document Number	Rev
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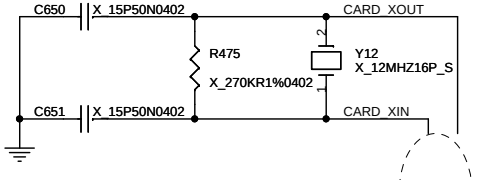
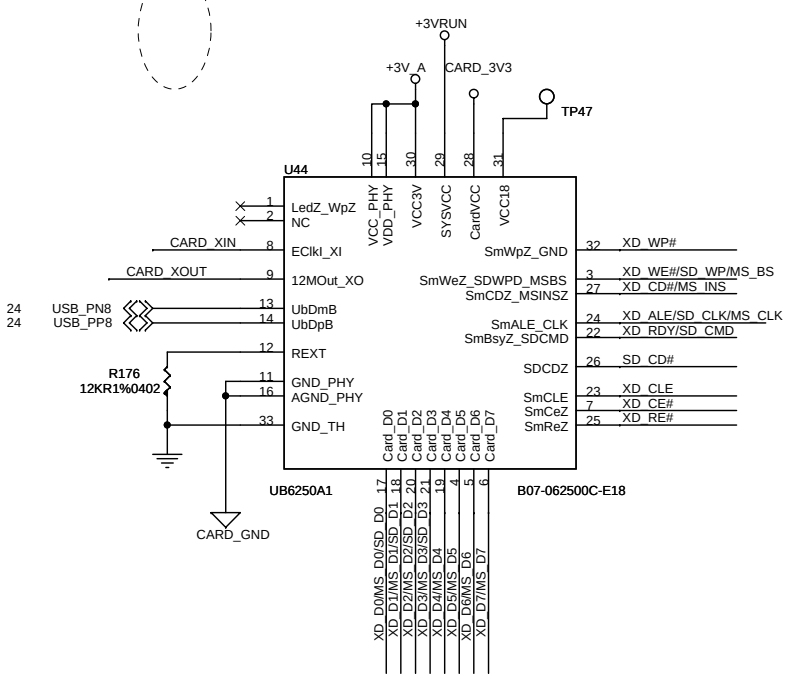
ENE UB6250 USB20 Flash Card Reader Controller
Pins for SD, MMC, MS, and xD memory cards

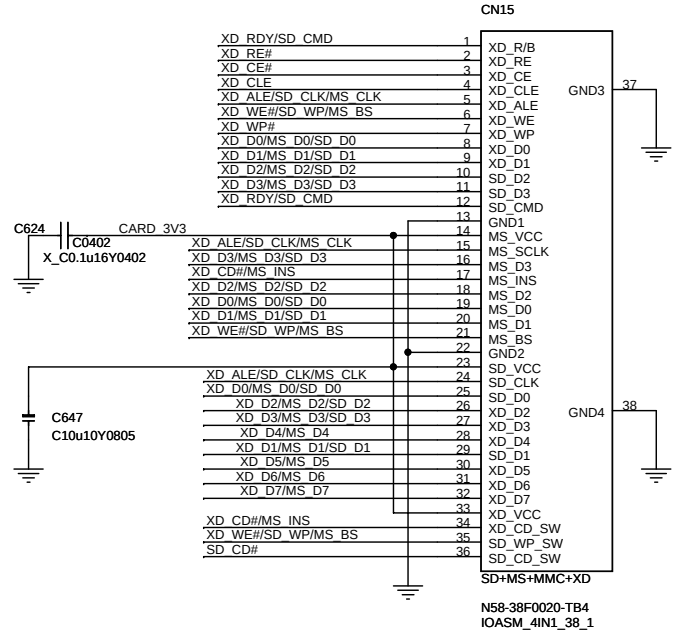
Name	No	I/O	xD	SD	MMC	MS
xDCeZ	7	O	xD card EN			
xDCle	23	O	xD CMD latch EN			
xDAle	24	O	xD ADDR latch EN	SD clock	MMC clock	MS serial clock
xDBsyZ	22	B	xD Ready/busy	SD CMD/response	MMC CMD/response	
xDData0	17	B	xD D0	SD D0	MMC D0	MS D0
xDData1	18	B	xD D1	SD D1	MMC D1	MS D1
xDData2	20	B	xD D2	SD D2	MMC D2	MS D2
xDData3	21	B	xD D3	SD D3	MMC D3	MS D3
xDData4	19	B	xD D4		MMC D4	MS D4
xDData5	4	B	xD D5		MMC D5	MS D5
xDData6	5	B	xD D6		MMC D6	MS D6
xDData7	6	B	xD D7		MMC D7	MS D7
xDWeZ	3	B	xD W EN	SD WP		MS Busy
xDReZ	25	O	xD R EN			
xDWpZ	32	O	xD WP			
SdCdZ	26	I		SD CD	MMC CD	
xDCdZ	27	I	xD CD			MS CD

29 CARDREADER_48 — 0R0402 — R473 — CARD_XIN

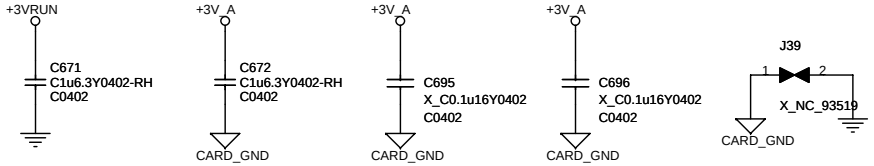
2009/07/01 48MHz from Clock GEN.







CLOCK frequency can vary
lie on strap pin config(pin7&pin25)



Configurations for Clock Source Selection:

4.7K Pull-high Resistor on		Frequency of external clock source to EClkin pin
xDReZ	xDCeZ	
NC	NC	48MHz
NC	O	24MHz
O	NC	12MHz

MICRO-STAR INT'L CO.,LTD.

Title: CARD_READER (RTS5159)

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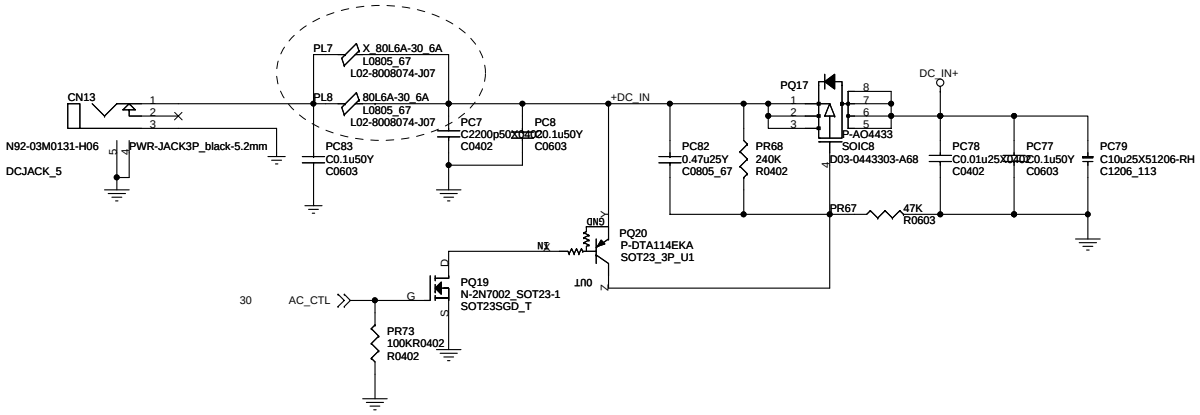
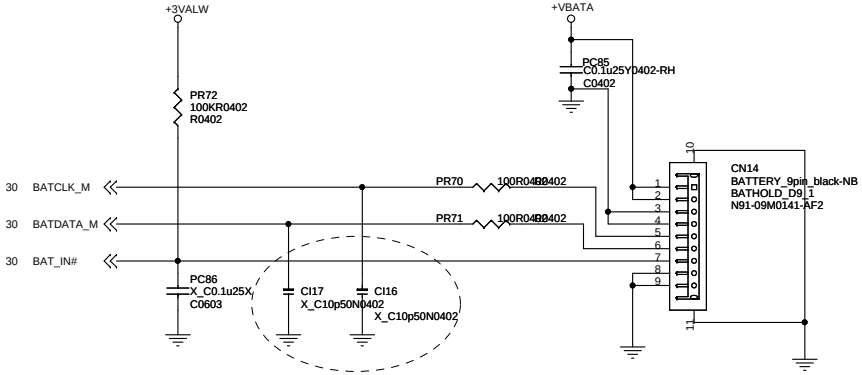
2009/07/10 65W adaptor只需要上一個BEAD

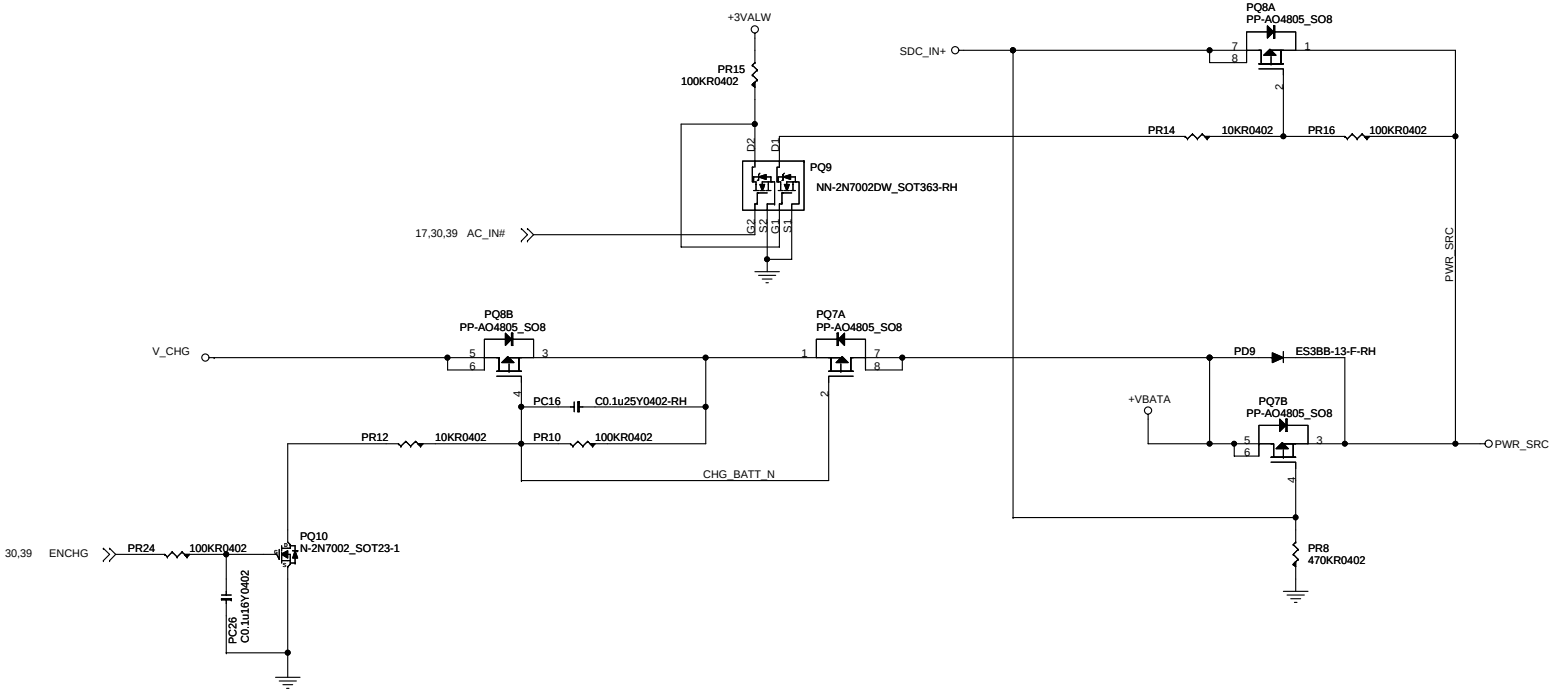




2009/06/26 Reserve 10p to GND
by EMI

JBAT1 Pin Definition

1: VBATA+
2: VBATA+
3: NC
4: NC
5: SMBCLK
6: SMBDATA
7: BAT_IN#
8: GND
9: GND



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	Battery Select		
Size: Custom	Document Number: MS-145X		Rev: 0A
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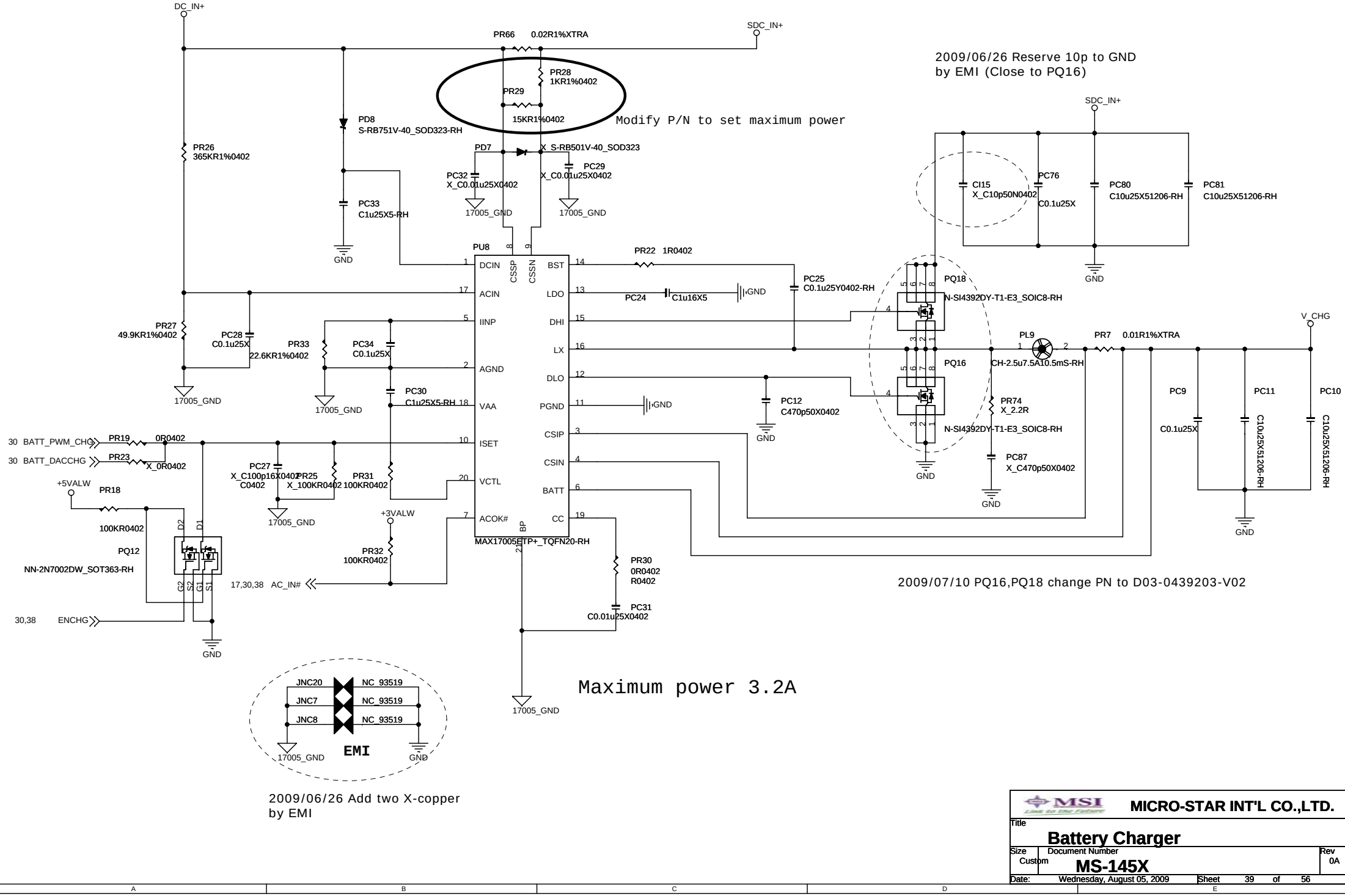
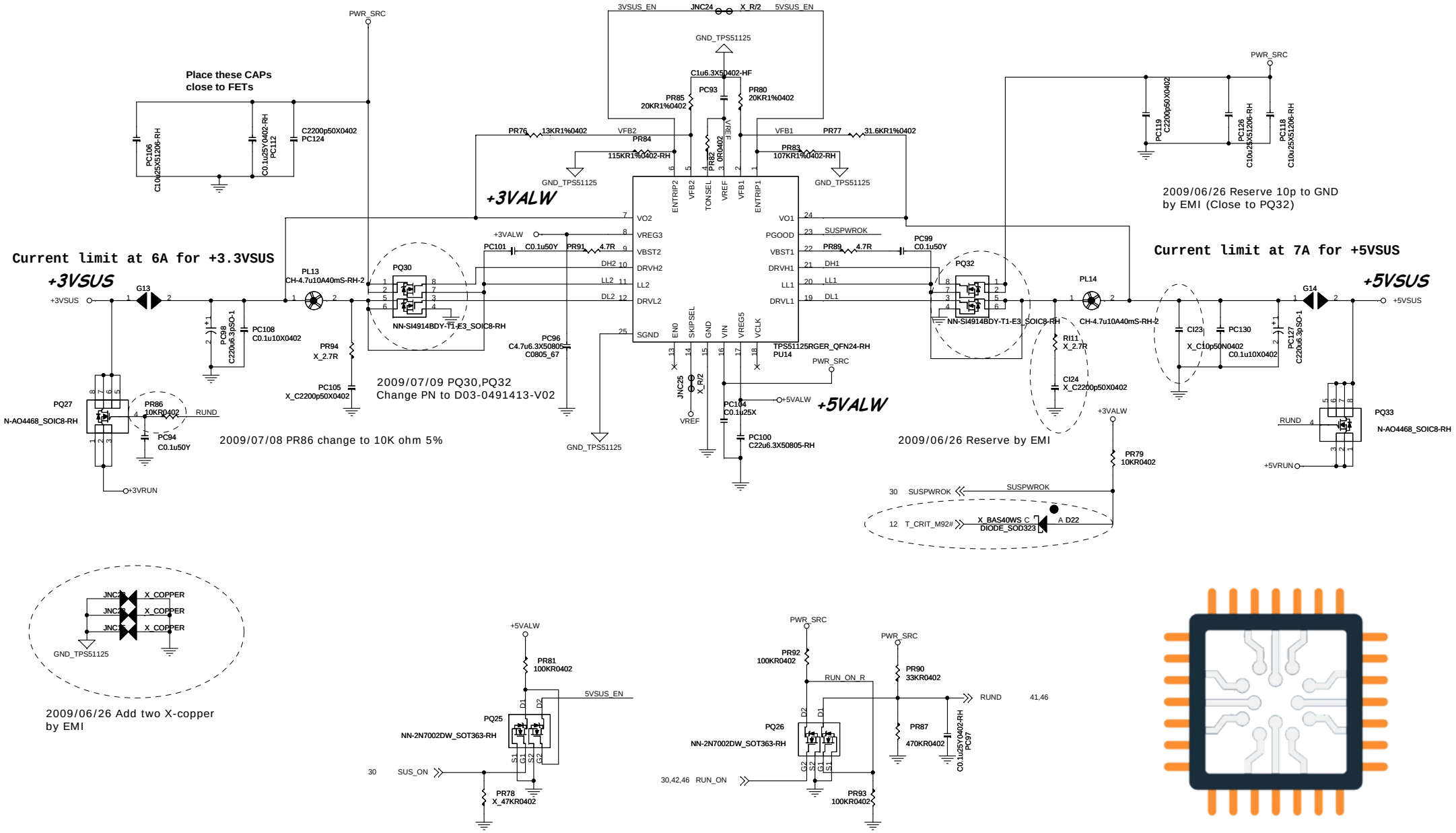


MSI Link to the Future	MICRO-STAR INT'L CO.,LTD.		
Title	Battery Charger		
Size: Custom	Document Number: MS-145X		Rev: 0A
Date: Wednesday, August 05, 2009	Sheet 39 of 56		



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	System power	
Size: Custom	Document Number: MS-145X	Rev: 0A
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2009/06/26 Reserve 10p to GND
by EMI (Close to PQ21)

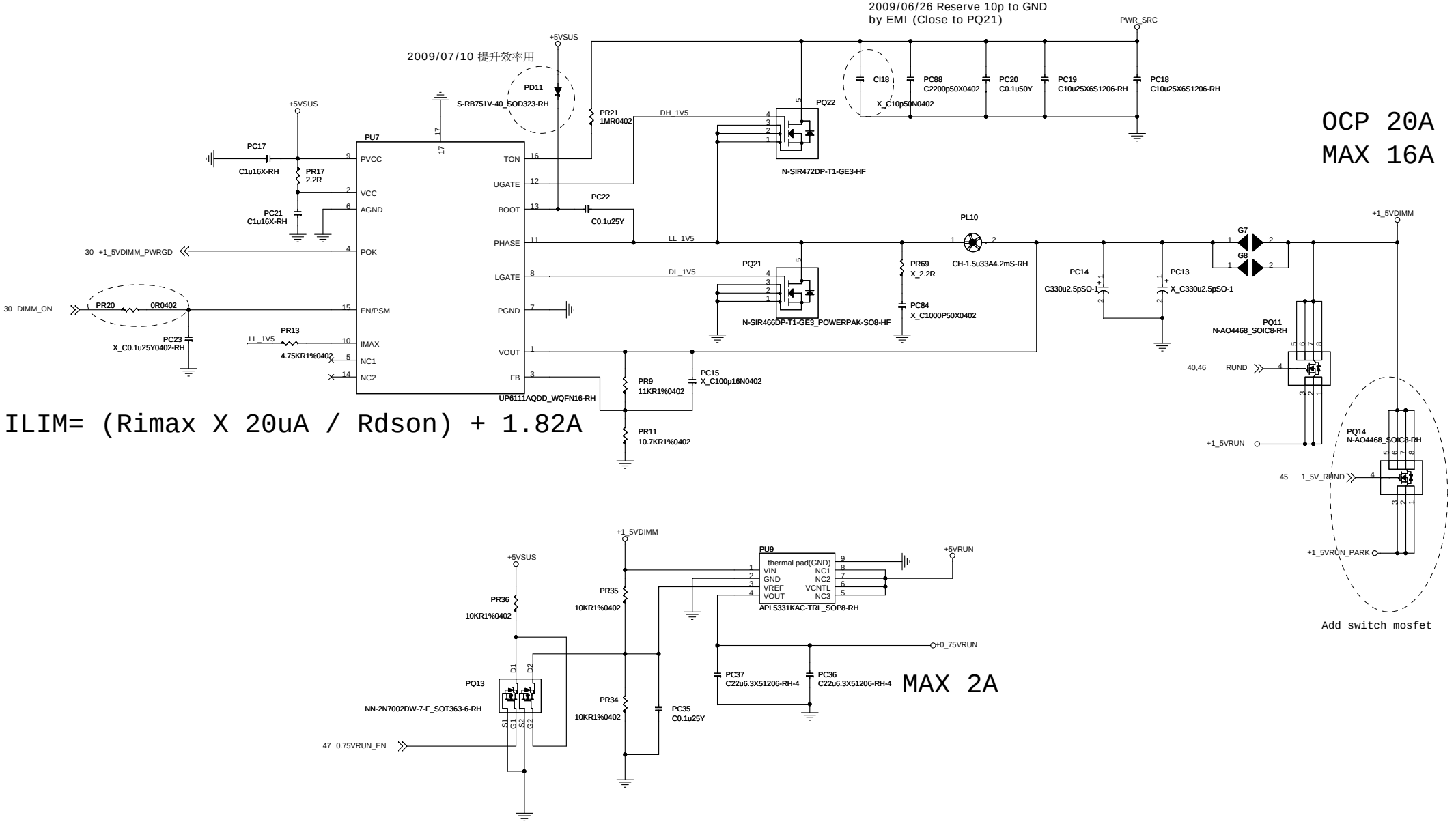
2009/07/10 提升效率用

OCP 20A
MAX 16A

ILIM= (Rimax X 20uA / Rdson) + 1.82A

MAX 2A

Add switch mosfet



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	SMDDR_VTERM /1_5VRUN	
Size: Custom	Document Number: MS-145X	Rev: 0A
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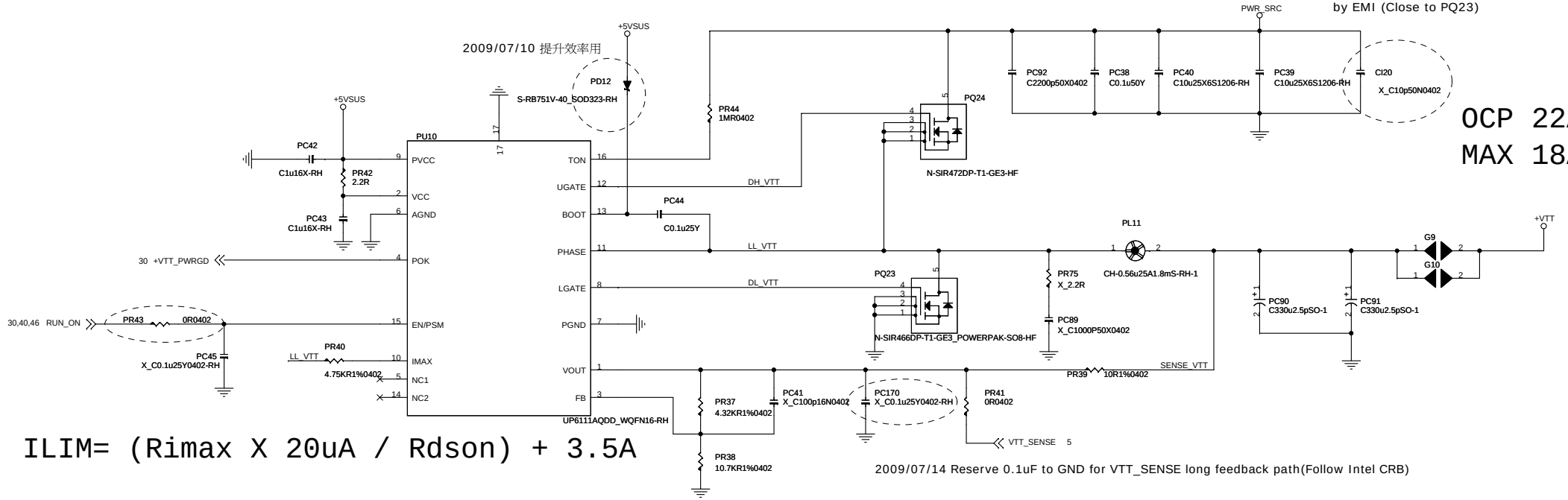
2009/06/26 Reserve 10p to GND
by EMI (Close to PQ23)

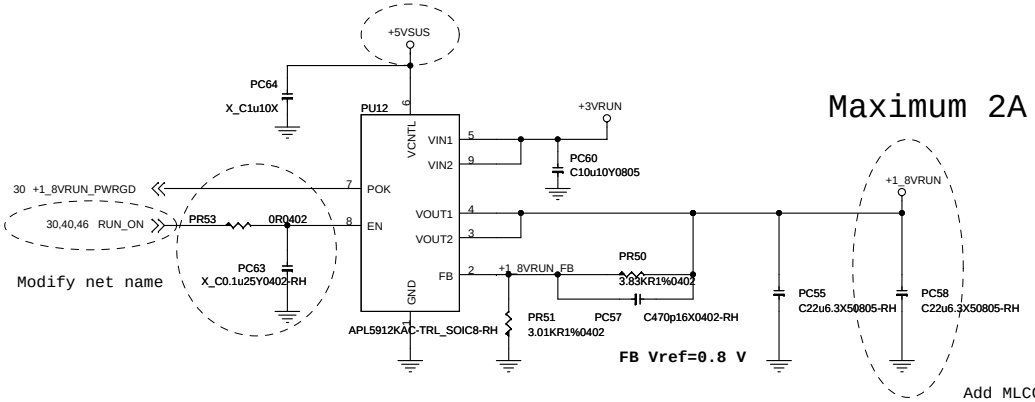
2009/07/10 提升效率用



OCP 22A
MAX 18A

ILIM= (Rimax X 20uA / Rdson) + 3.5A

2009/07/14 Reserve 0.1uF to GND for VTT_SENSE long feedback path(Follow Intel CRB)



Maximum 2A

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	VTT Power,+1.8VRUN	
Size: Custom	Document Number: MS-145X	Rev: 0A
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2009/06/26 Reserve 10p to GND
by EMI (Close to PQ47 or PQ48)

2009/06/26 Reserve 10p to GND
by EMI (Close to PQ45 or PQ46)

2009/07/14 PR170,PR171 not stuff
(在CPU端已有pull up及pull down電阻)
跟CPU拉載的位置有關

2009/07/01 Add three X-copper

Close to Phase 1 Inductor

Parallel

Parallel

Title	CPU Power
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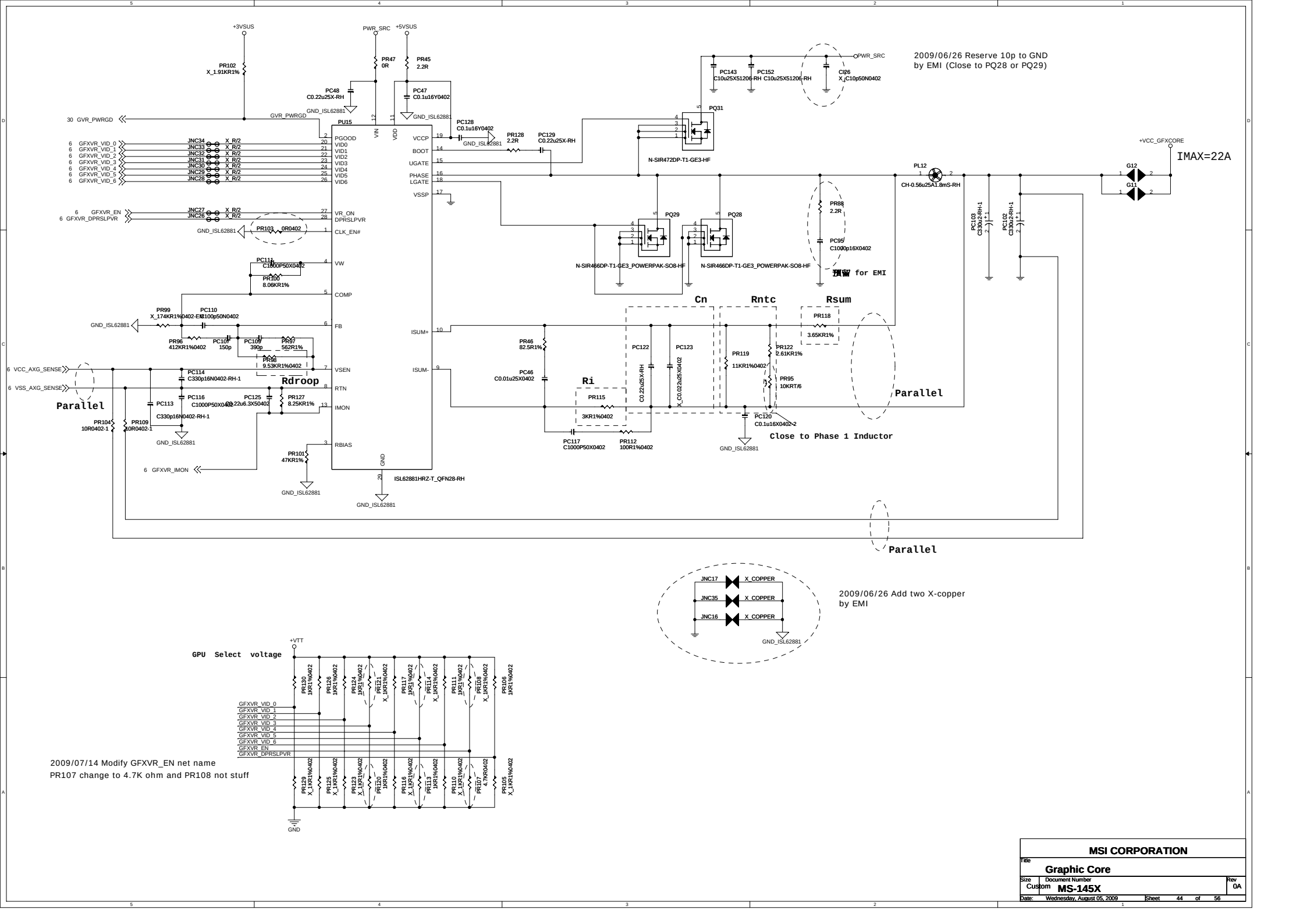
MSI CORPORATION



MSI CORPORATION		
Title: Graphic Core		
Size: Custom	Document Number: MS-145X	Rev: 0A
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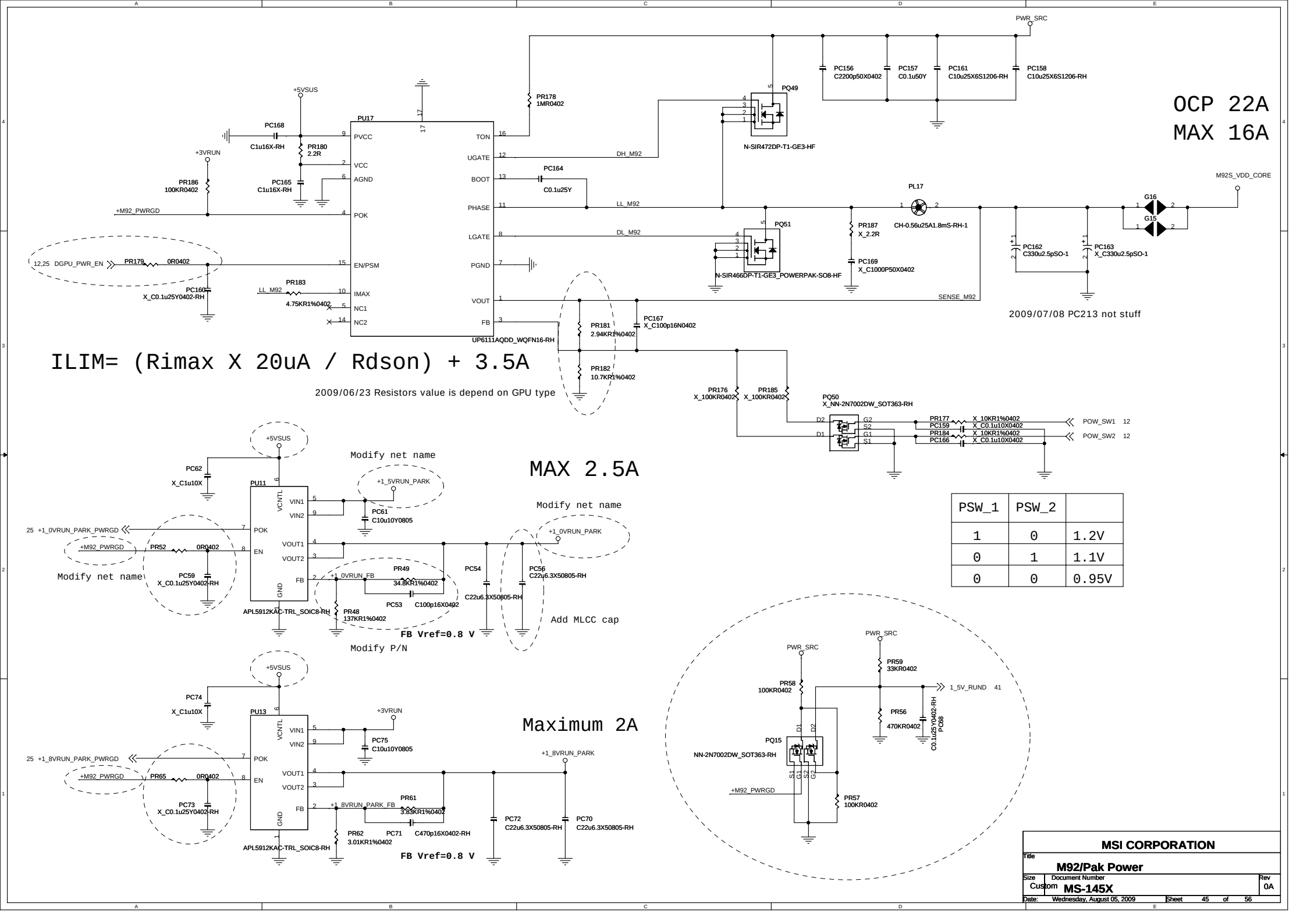
OCP 22A
MAX 16A
ILIM= (Rimax X 20uA / Rdson) + 3.5A
2009/06/23 Resistors value is depend on GPU type
2009/07/08 PC213 not stuff
MAX 2.5A
Maximum 2A
Modify net name
Modify P/N
Add MLCC cap
FB Vref=0.8 V
PWR_SRC
PU17
UP6111AQDD_WQFN16-RH
N-SIR472DP-T1-GE3-HF
N-SIR466DP-T1-GE3_POWERPAK-SO8-HF
PU11
APL5912KAC-TRL_SOIC8-RH
PU13
PQ50
X_NN-2N7002DW_SOT363-RH
PQ15
NN-2N7002DW_SOT363-RH
M92S_VDD_CORE
POW_SW1
POW_SW2
PSW_1 PSW_2
1 0 1.2V
0 1 1.1V
0 0 0.95V
MSI CORPORATION
M92/Pak Power
Custom MS-145X
Rev 0A
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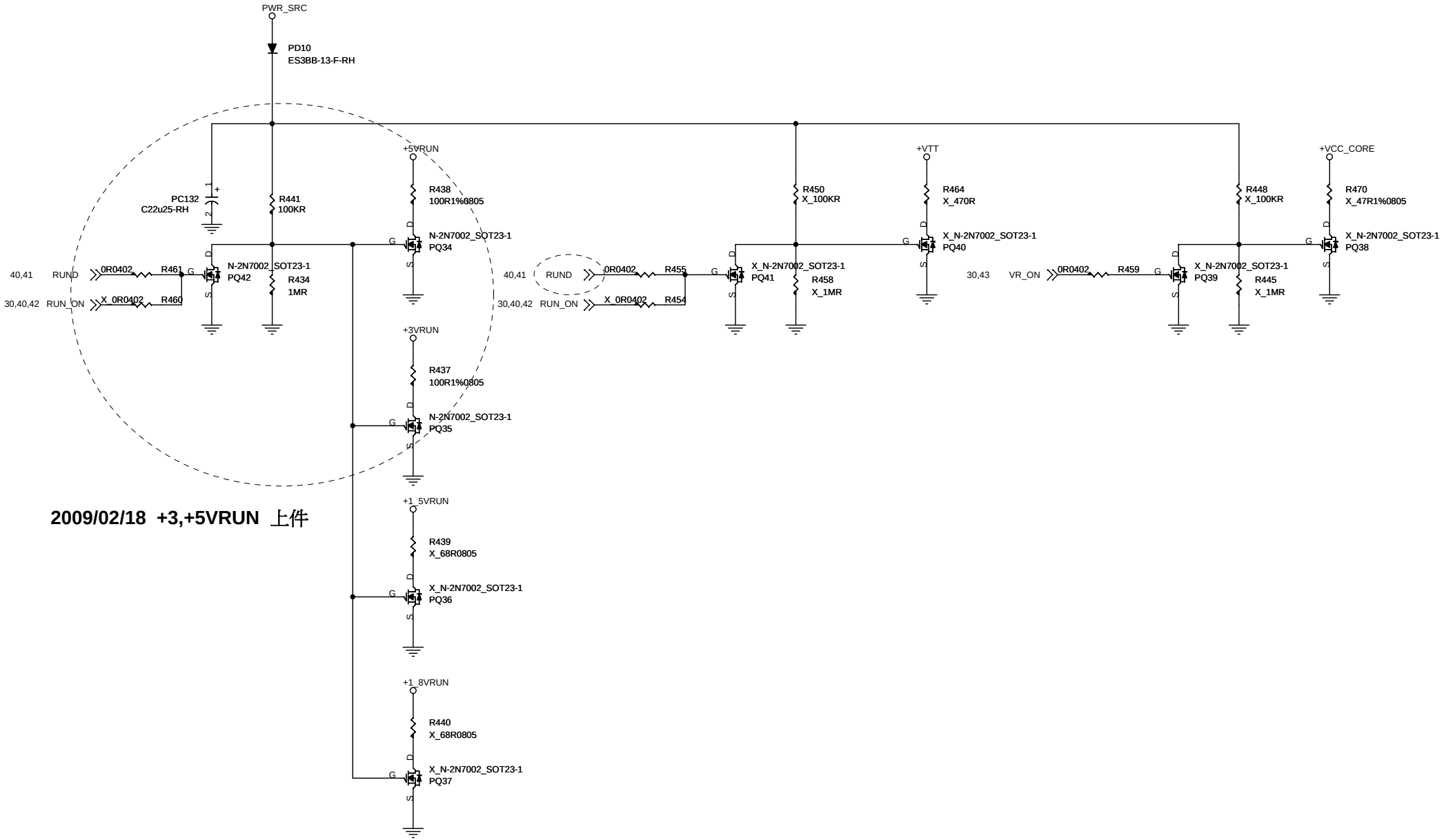

2009/02/18 +3,+5VRUN 上件

MSI	MICRO-STAR INT'L CO.,LTD.		
Title	Discharge Circuits		
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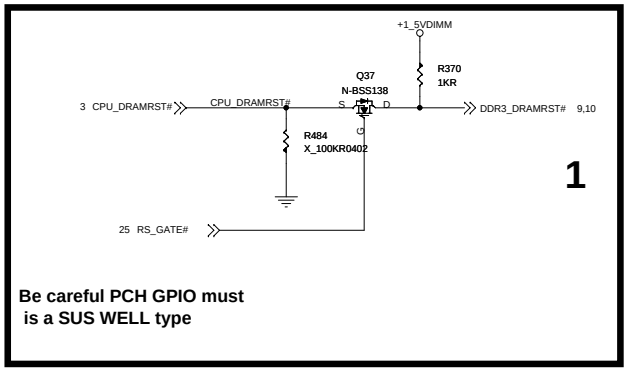

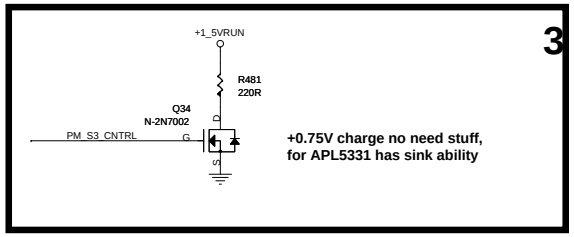

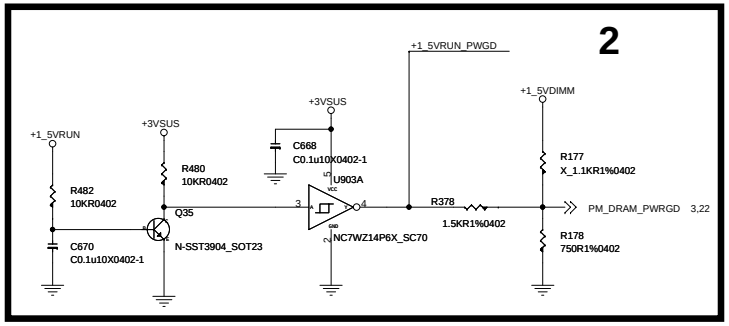

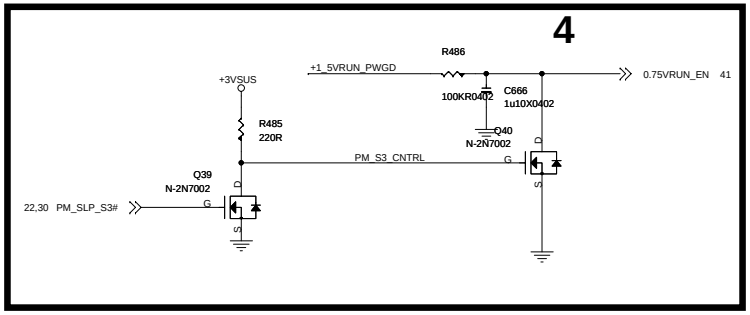

MSI	MICRO-STAR INT'L CO.,LTD.		
Title: INTEL S3 POWER			
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C-case & D-case

MH17 HOLES_8X8_D3MM_VIA8
MH14 HOLES_8X8_D3MM_VIA5
MH18 HOLES_8X8_D3MM_VIA8
MH19 HOLES_8X8_D3MM_VIA8
MH15 HOLES_8X8_D3MM_VIA8
MH10 HOLES_8X8_D3MM_VIA8
MH8 HOLES_8X8_D3MM_VIA8
MH7 HOLES_8X8_D3MM_VIA8
MH13 HOLES_8X8_D3MM_VIA5
MH12 HOLES_8X8_D3MM_VIA5
MH9 HOLES_8X8_D3MM_VIA8
MH11 HOLES_8X8_D3MM_VIA5

12/1 EMI

UME8
HOLES_R177D91
E2B-1634020-L63
MDC Stand off

CN10
FRAME_62_55X44_7
New Card Socket
E2M-4410111-SH4
SCREW5
SCREW6
E43-1204004-H29
E43-1204004-H29
ExpressCard

UME1
HDMI LABEL
HDMI_LABEL

PCB PN

PCB4
PCB
P30-1451111-H73

MH16
HOLES_8X8_D3MM_VIA5

PCH

H7 Holes_R276D185P_PT HOLES_R288D142
H8 Holes_R276D185P_PT HOLES_R288D142

CPU

H10 Holes_R276D185P_PT E2B-1676010-RH
H9 Holes_R276D185P_PT E2B-1676010-RH
H11 Holes_R276D185P_PT E2B-1676010-RH

GPU

H12 HOLES_R177D91 E2B-1022010-RH

Thermal_Module_Stand-off 螺絲孔

阻抗測試線確認

J19 L3_DIFF_8/5/8_70_Ohm+ X_H1X2_black-RH
J10 L3_DIFF_8/5/8_70_Ohm- X_H1X2_black-RH
J24 L4_DIFF_8/5/8_70_Ohm+ X_H1X2_black-RH
J18 L4_DIFF_8/5/8_70_Ohm- X_H1X2_black-RH
J17 L1_5mil_55_Ohm X_H1X2_black-RH
J13 L6_5mil_55_Ohm X_H1X2_black-RH
J12 L3_4.5mil_55_ohm X_H1X2_black-RH
J25 L4_4.5mil_55_ohm X_H1X2_black-RH
J11 L4_DIFF_4.5/5.5/4.5_90_Ohm+ X_H1X2_black-RH
J22 L4_DIFF_4.5/5.5/4.5_90_Ohm- X_H1X2_black-RH
J20 L6_DIFF_4.5/5.5/4.5_90_Ohm+ X_H1X2_black-RH
J23 L6_DIFF_4.5/5.5/4.5_90_Ohm- X_H1X2_black-RH
J16 L4_5.5mil_50_Ohm X_H1X2_black-RH
J27 L1_DIFF_4/7/4_100_Ohm+ X_H1X2_black-RH
J26 L1_DIFF_4/7/4_100_Ohm- X_H1X2_black-RH
J7 L3_DIFF_4/7/4_100_Ohm+ X_H1X2_black-RH
J15 L3_DIFF_4/7/4_100_Ohm- X_H1X2_black-RH
J9 L4_DIFF_4/7/4_100_Ohm+ X_H1X2_black-RH
J14 L4_DIFF_4/7/4_100_Ohm- X_H1X2_black-RH
J8 L6_DIFF_4/7/4_100_Ohm+ X_H1X2_black-RH
J21 L6_DIFF_4/7/4_100_Ohm- X_H1X2_black-RH

PAD12 E23-1029050-RH
PAD10 X_E23-1029050-RH
PAD7 GND PAD in TOP side
PAD11 X_E23-1029050-RH
PAD9 E23-1029050-RH

FM1 F_PAD_X
FM2 F_PAD_X
FM3 F_PAD_X
FM4 F_PAD_X
FM5 F_PAD_X
FM6 F_PAD_X
FM7 F_PAD_X
FM8 F_PAD_X
FM9 F_PAD_X
FM10 F_PAD_X
FM11 F_PAD_X
FM12 F_PAD_X
FM13 F_PAD_X
FM14 F_PAD_X
FM15 F_PAD_X
FM16 F_PAD_X
FM17 F_PAD_X
FM18 F_PAD_X
FM19 F_PAD_X
FM20 F_PAD_X

+1_5VDIMM
+0_75VRUN
+VTT
+VCC_CORE
+5VSUS
+3VSUS
+1_8VRUN
+VCC_GFXCORE
+5VRUN
+3VRUN
+3VALW
PWR_SRC
SDC_IN+

PAD18 10X6.7X3.1
PAD19 10X6.7X3.1
PAD20 X_MS-55101-RH
PAD21 X_MS-55101-RH
PAD22 X_MS-55101-RH

MICRO-STAR INT'L CO.,LTD.

Title: Screw/EMI
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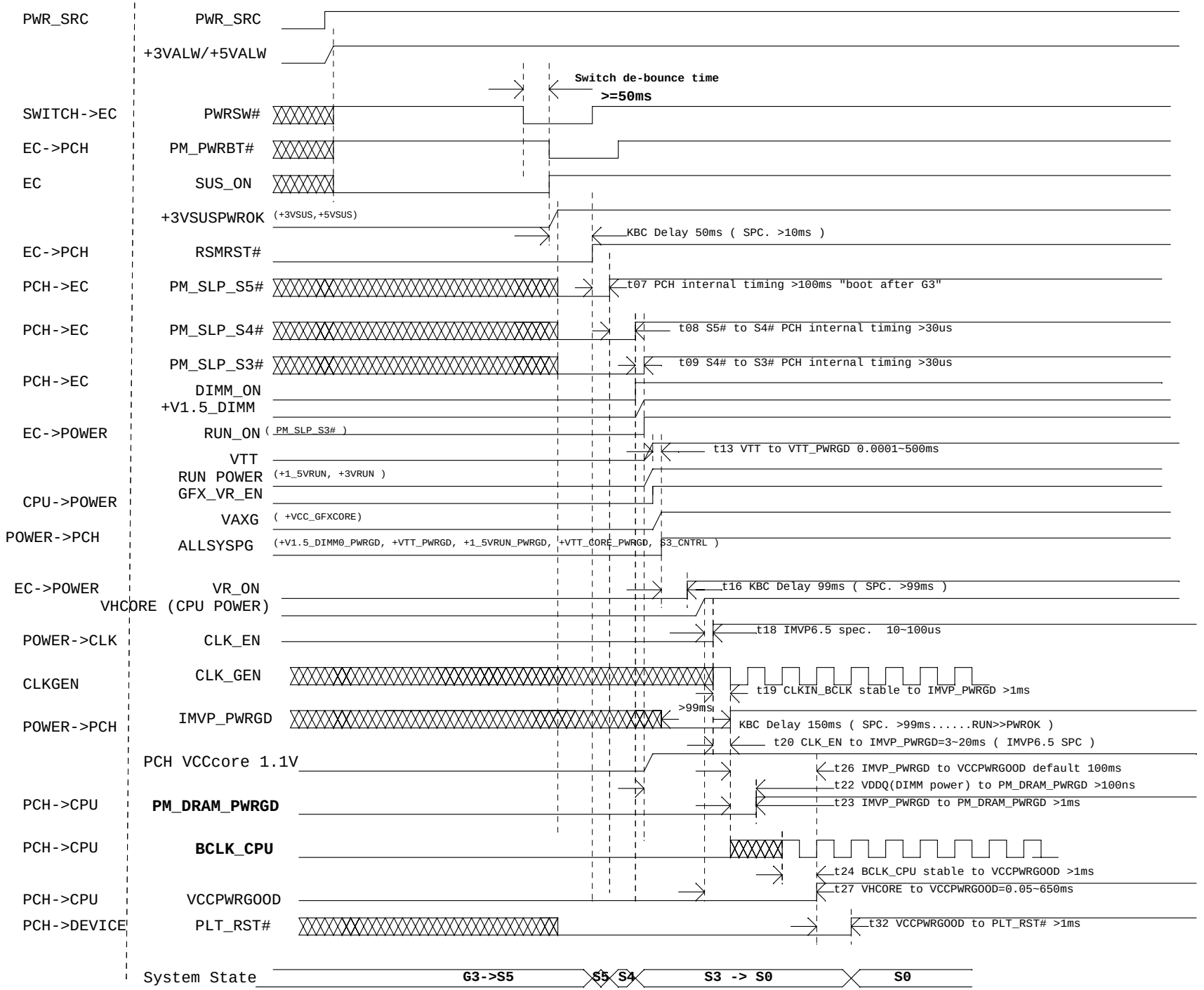
Calpella System Power on Sequence DC mode



MSI	MICRO-STAR INT'L CO.,LTD.
Title	Power on Sequency
Size: Custom	Document Number: MS-145X
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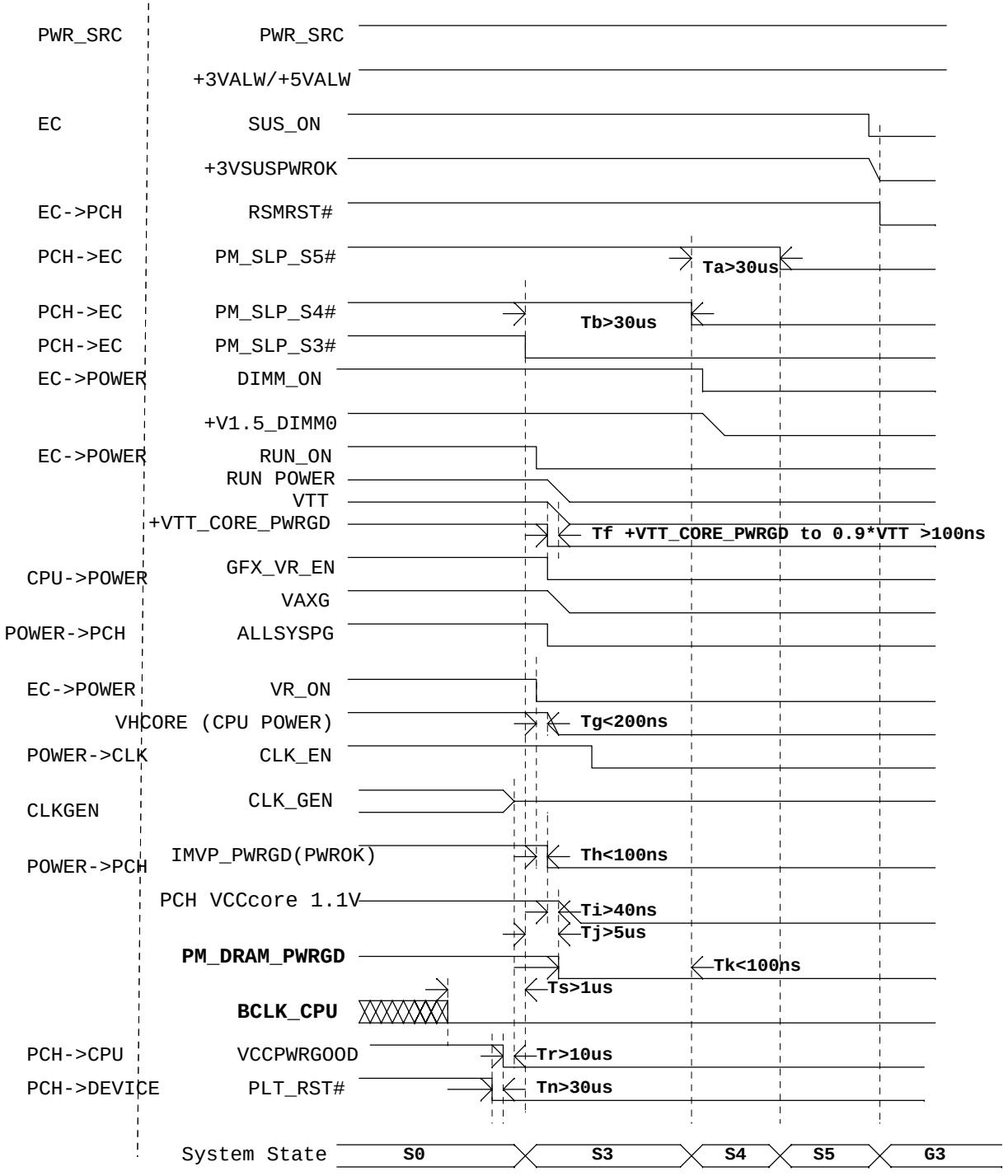
Power down Sequence DC mode S0 to G3



MSI	MICRO-STAR INT'L CO.,LTD.	
Title: Power on Sequency		
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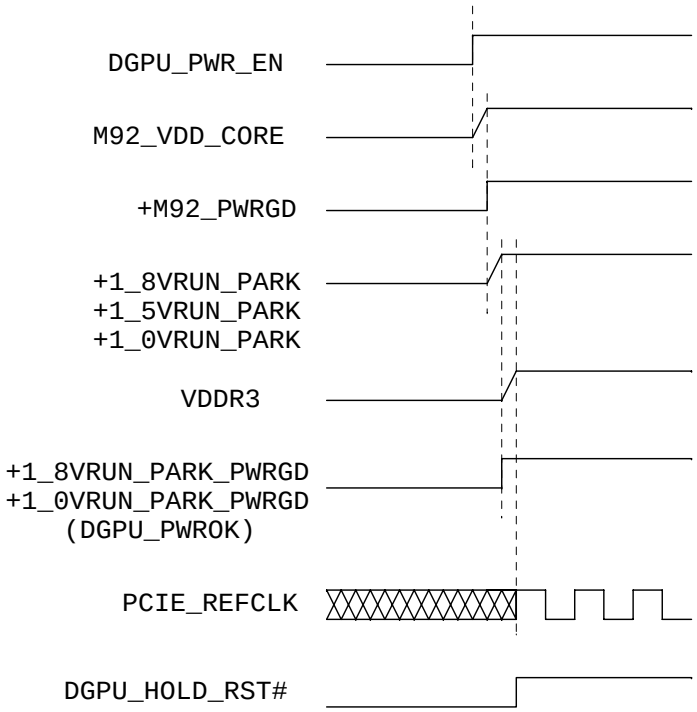
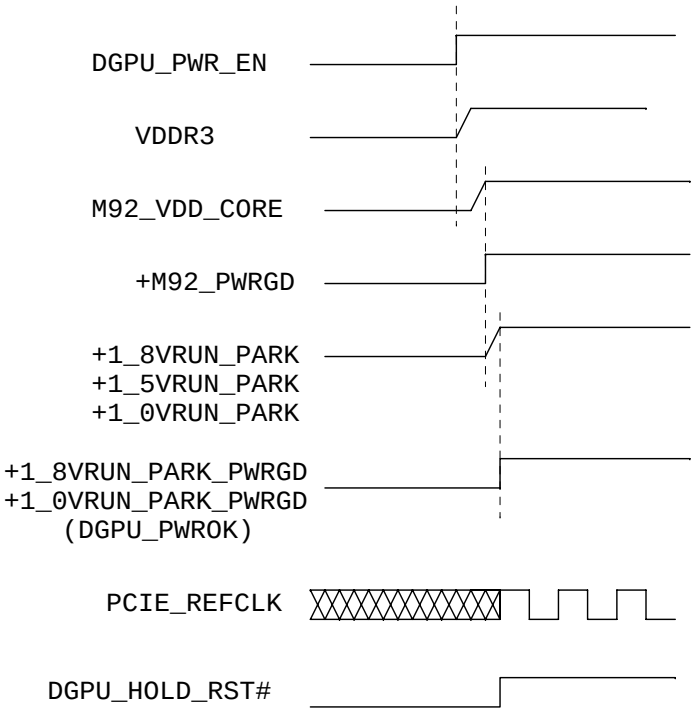
M92 Power on Sequence



PARK Power on Sequence



MICRO-STAR INT'L CO.,LTD.

Title: M92/PARK Power on Sequence

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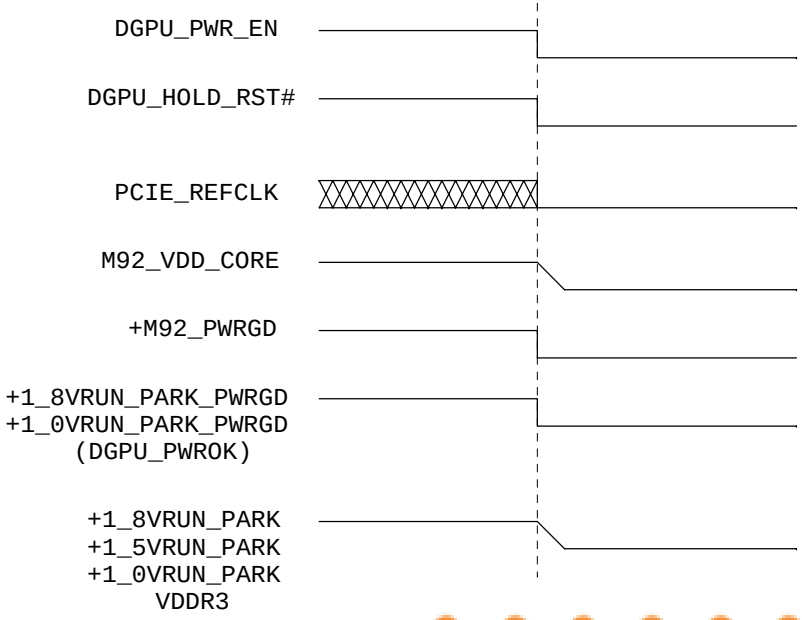
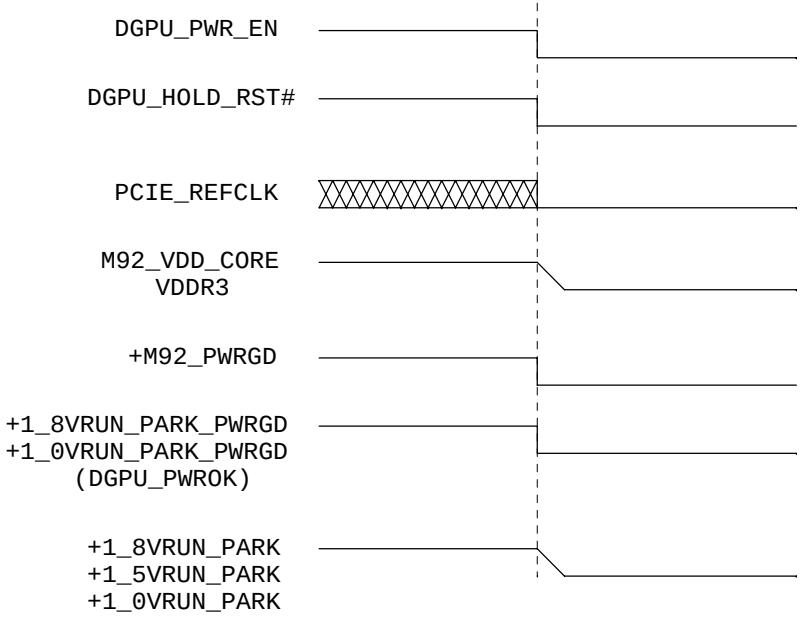
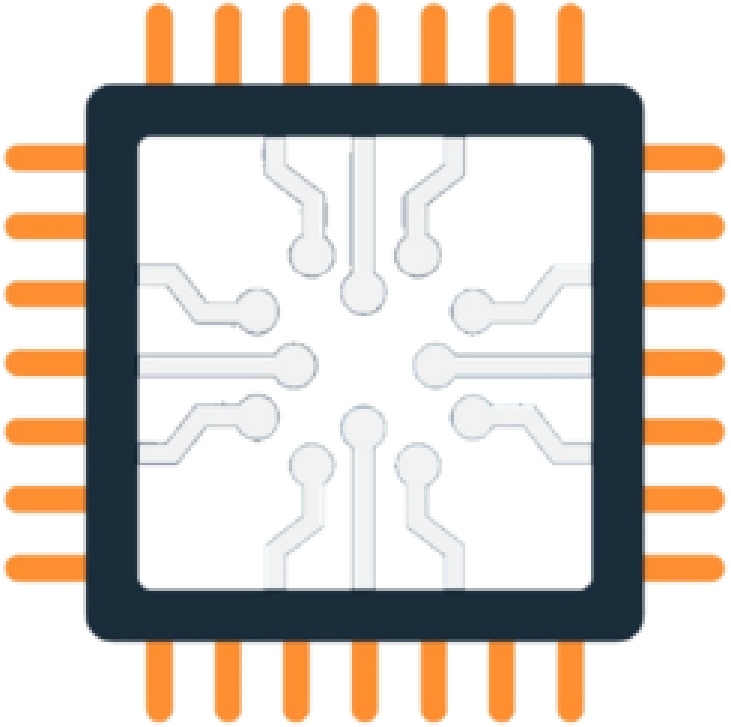
M92 Power down Sequence



PARK Power down Sequence





Eletro-X

MSI Link to the Future	MICRO-STAR INT'L CO.,LTD.	
Title	M92/PARK Power down Sequence	
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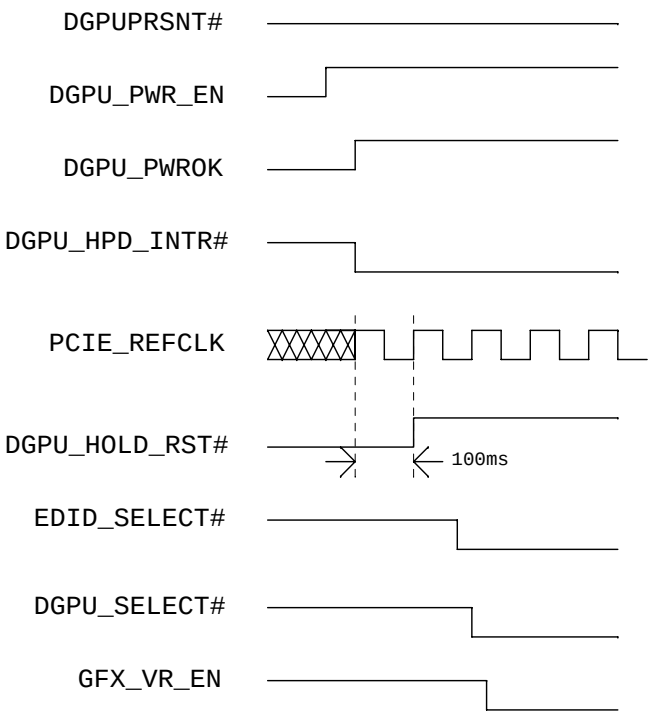
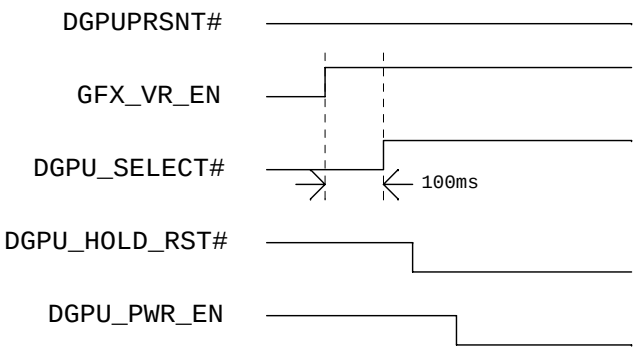
Switchable DGPU Power on Sequence
Discrete Mode



Switchable DGPU Power off Sequence
UMA Mode



MICRO-STAR INT'L CO.,LTD.		
Title: Switchable Power Sequence		
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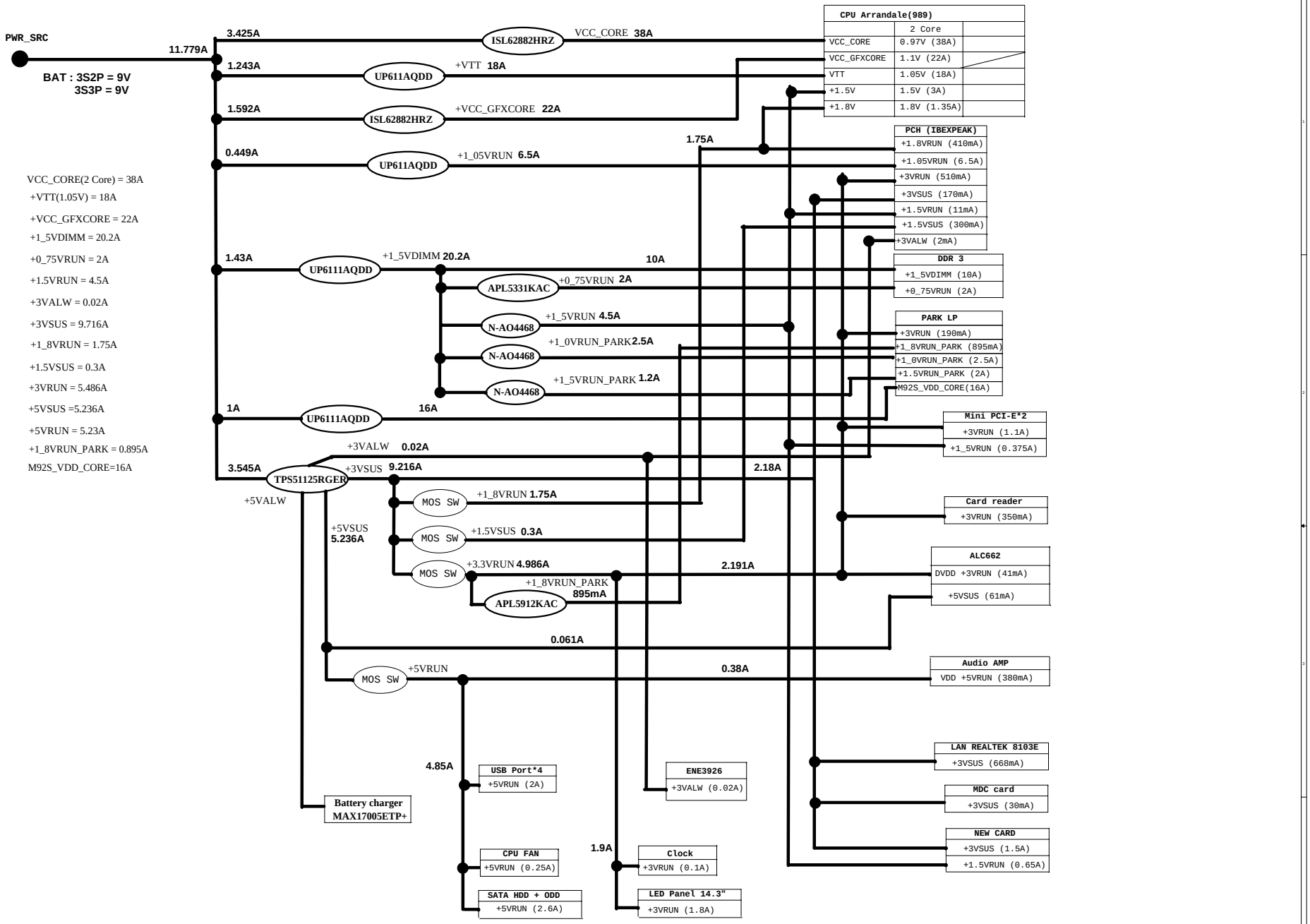

MICRO-STAR INT'L CO.,LTD.

Title: Power MAP

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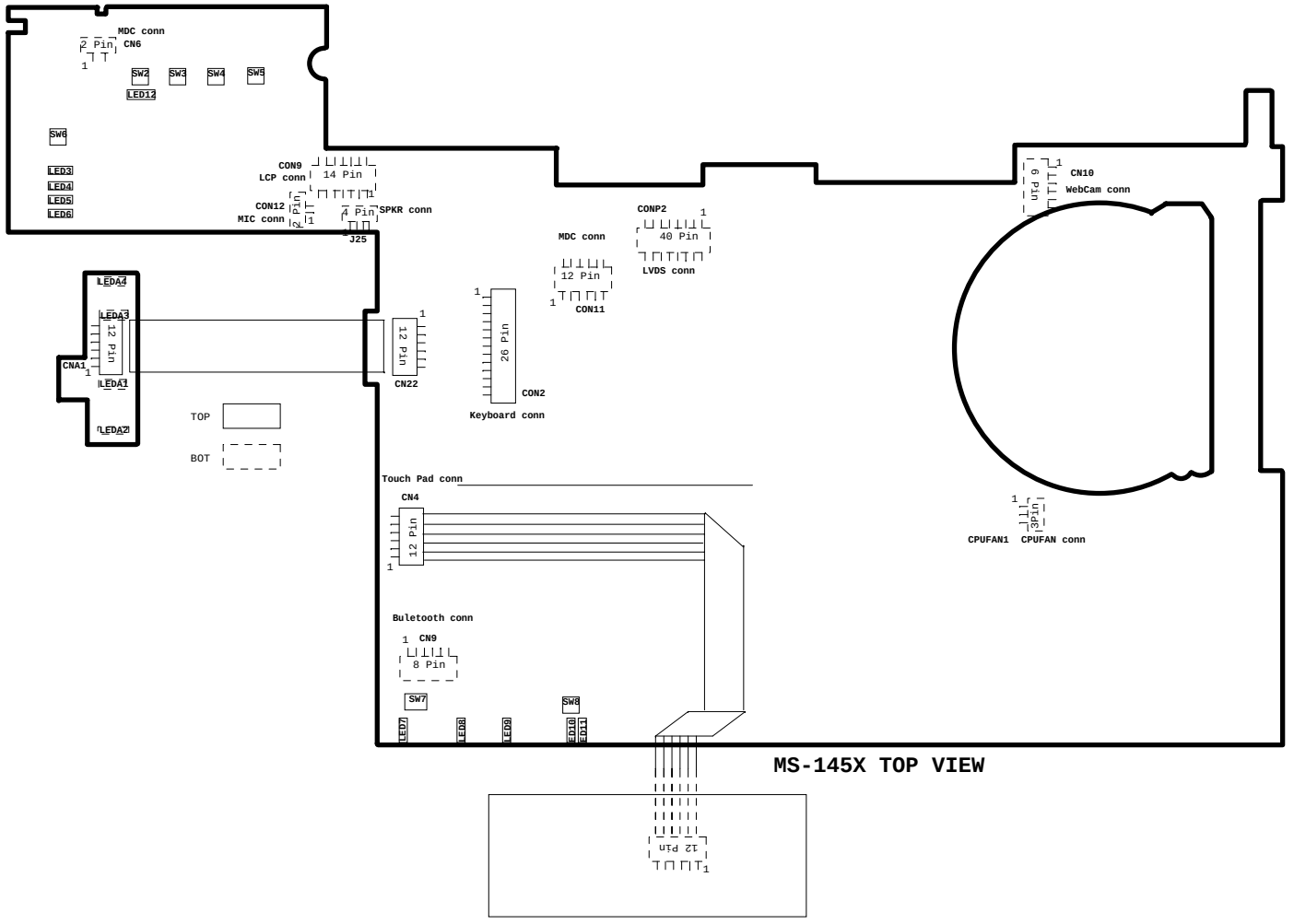
MS-145X	
SW2	Power_button(FOR OEM)
SW3	HotKeyP1_button(FOR OEM)
SW4	WLAN/BT_button(FOR OEM)
SW5	Search/Webcam_button (FOR OEM)
SW6	Power_button(FOR Channel)
SW7	Right_button
SW8	Left_button

MS-145X	
LED3	HDD LED(FOR OEM)
LED4	NUM_LED(FOR OEM)
LED5	CAP_LED(FOR OEM)
LED6	SCR_LED (FOR OEM)
LED7	BT_LED
LED8	WLAN_LED
LED9	ACPI_LED
LED10	CHARGE_LED
LED11	BATTERY_LOW_LED
LED12	POWER_LED

MS-145XA	
LEDA1	NUM_LED(FOR OEM)
LEDA2	HDD_LED(FOR OEM)
LEDA3	CAP_LED(FOR OEM)
LEDA4	SCR_LED (FOR OEM)

MS-145X : Main Board
MS-145XA : LED board



MS-145X TOP VIEW

MICRO-STAR INT'L CO.,LTD.		
Title: Topology		
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2009/06/25 [Page33] Add LED and switch function for OEM reserved

[Page30] Delete KBOUT16,KBOUT17 for MS-1451 keyboard matrix

[Page41/42] Modify APL5912 VCNTL to +5VSUS

[Page43/44] Modify some RC footprint and value

2009/06/26 Modify circuit to Switchable

[Page19] Add LVDS common choke by EMI

[Page12] Reserve RGB 10p to GND

[Page38] Reserve BAT CLK and DATA 10p to GND

[Page39] Reserve 10p SDC_IN+ to GND and close to PQ57

Add two X-Copper

[Page40] Reserve 10p +5VSUS to GND and close to PQ60

Reserve 2.2R+2200p

[Page41] Reserve 10p PWR_SRC to GND and close to PQ68

[Page42] Reserve 10p PWR_SRC to GND and close to PQ72

[Page43] Reserve 10p PWR_SRC to GND and close to PQ75 or PQ76

Reserve 10p PWR_SRC to GND and close to PQ78 or PQ79

[Page43] Reserve 10p PWR_SRC to GND and close to PQ81 or PQ82

Add two X-Copper

2009/06/29 [Page35] Modify CPU FAN.Add C121 and C304 by datasheet.Add one more RC for FAN speed calculation(as MS-1122)

Modify PARK circuit

Modify PCH PN to OB1-1675001 for Mobile IntelR 5 Series Chipset Full Feature

Modify Audio jack PN to N54-05F0951-H06

Modify internal MIC PN to N32-1020790-A81

Modify power sequence map

2009/07/01 [Page3] R234,R412等0A實驗結果再決定是否移除

BPM#[0~7] remove

BCLK只保留from PCH,移除from CLOCK GEN.

[Page5] Short bead

[Page6] Short bead

[Page7] VSS_NCTF1~7 remove

[Page8] 只保留CFG的測點,其餘移除

[Page9] SA0_DIM0及SA1_DIM0改爲0 ohm對地

移除330uF,因在CPU以及switching power端已有

[Page10] SA0_DIM1改爲0 ohm對地

移除330uF,因在CPU以及switching power端已有

[Page12] 補上HPD線路

[Page16] MDA0~MDA7 swap

[Page18] CRT及LVDS的預留電阻(for MS-1454)均改爲單顆的0 ohm

EDID switch的電源pin加上0.1uF

R3238,R3239改爲10K ohm

移除BR-AD-ADJ,BR-PWM-ADJ名稱改爲PWM-ADJ,HDMI DDC名稱改爲HDM_SDA及HDM_SCL

[Page19] 兀型濾波LC值改爲0.1uH+10pF

新增LVDS DDC pull high,backlight adj預留net PWM-ADJ

[Page25] DGPUPRSNT#改接pull down

[Page30] 修改+1_8VRUN_PARK_PWRGD及+1_0VRUN_PARK_PWRGD結合爲DGPU_PWROK

[Page34] C47,C49改爲0.1uF

[Page43] Add three X-copper

MICRO-STAR INT'L CO.,LTD.

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