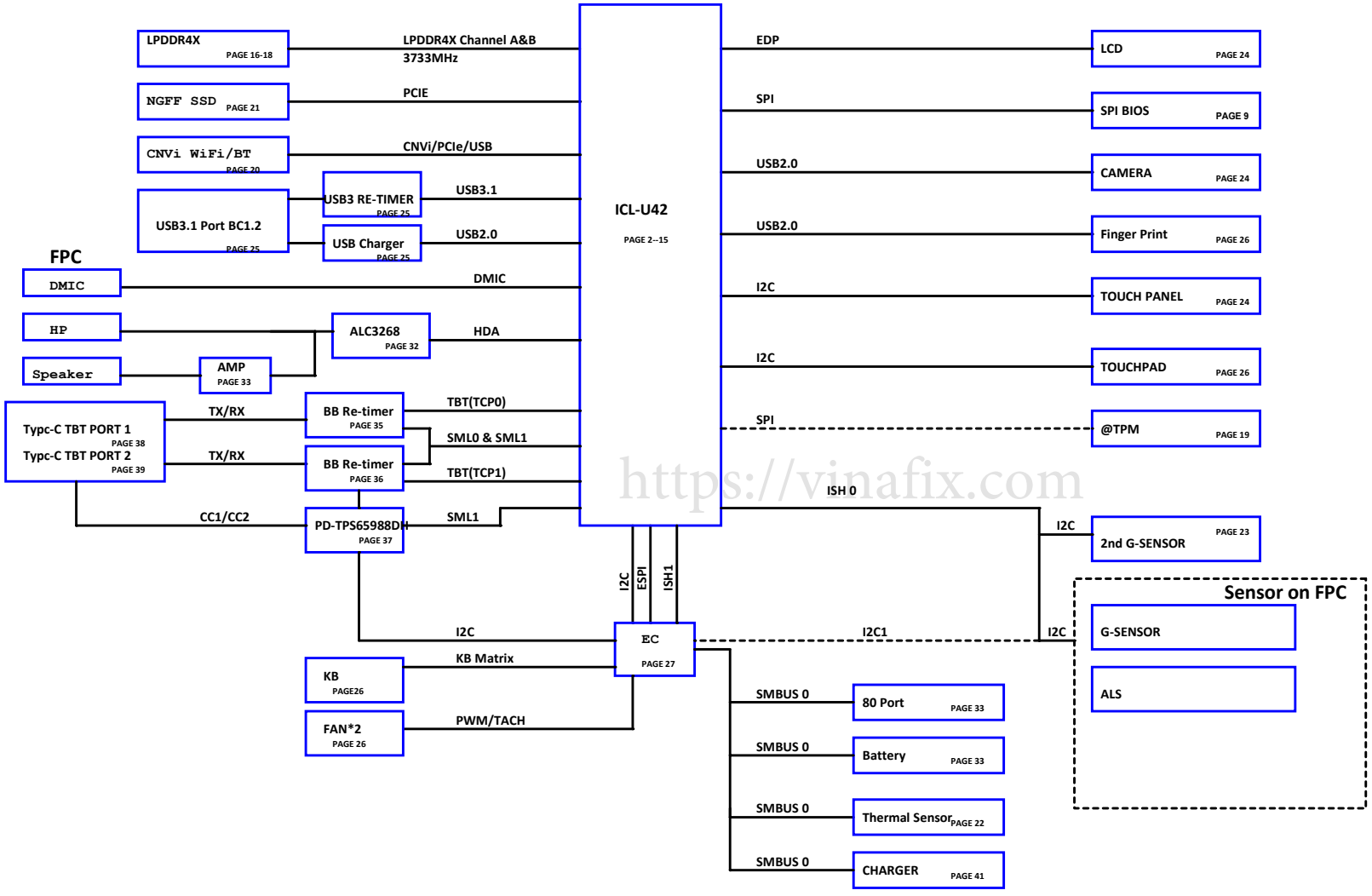
YogaC940 ICL-U42/U43e SIT Schematic Block Diagram

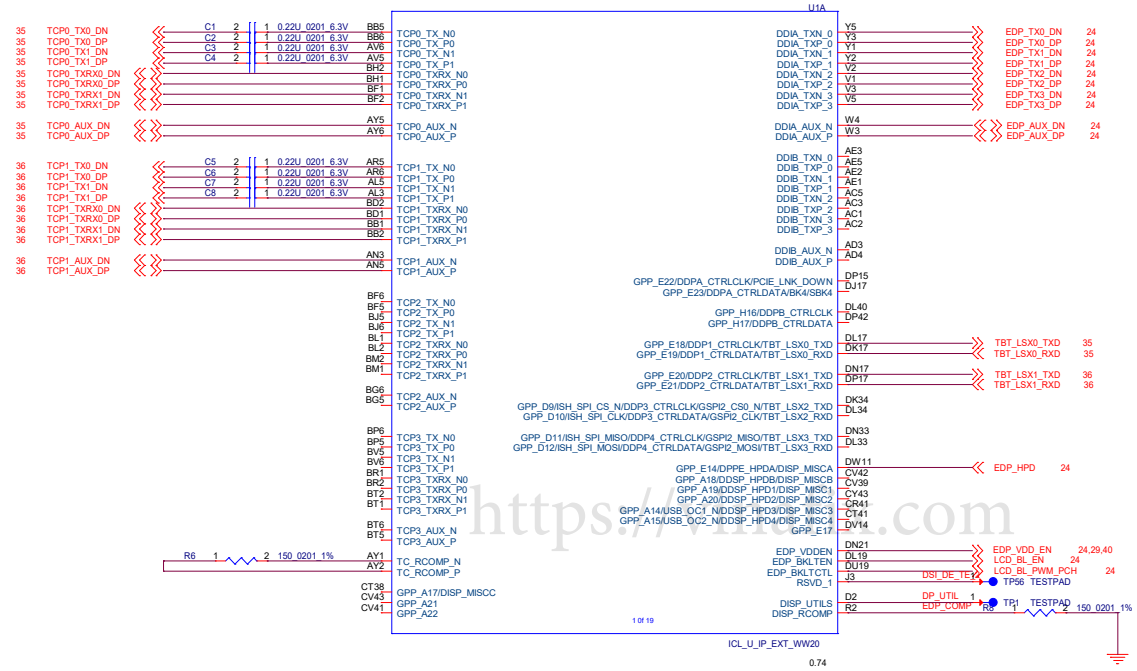


lenovo 联想 LENOVO.CRDN

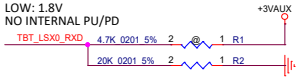
Title: Ice Lake Block Diagram

Size: C | Document Number: YOGAC940 | Rev: V0.5

Date: Thursday, June 13, 2019 | Sheet 1 of 50



TBT LSX #0 PINS VCCIO CONFIGURATION
HIGH: 3.3V
LOW: 1.8V
NO INTERNAL PU/PD



TBT LSX #1 PINS VCCIO CONFIGURATION
HIGH: 3.3V
LOW: 1.8V
NO INTERNAL 20K PD

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Title: Ice Lake MCP (TBT,EDP)

Size: C | Document Number: YOGAC940 | Rev: V0.5

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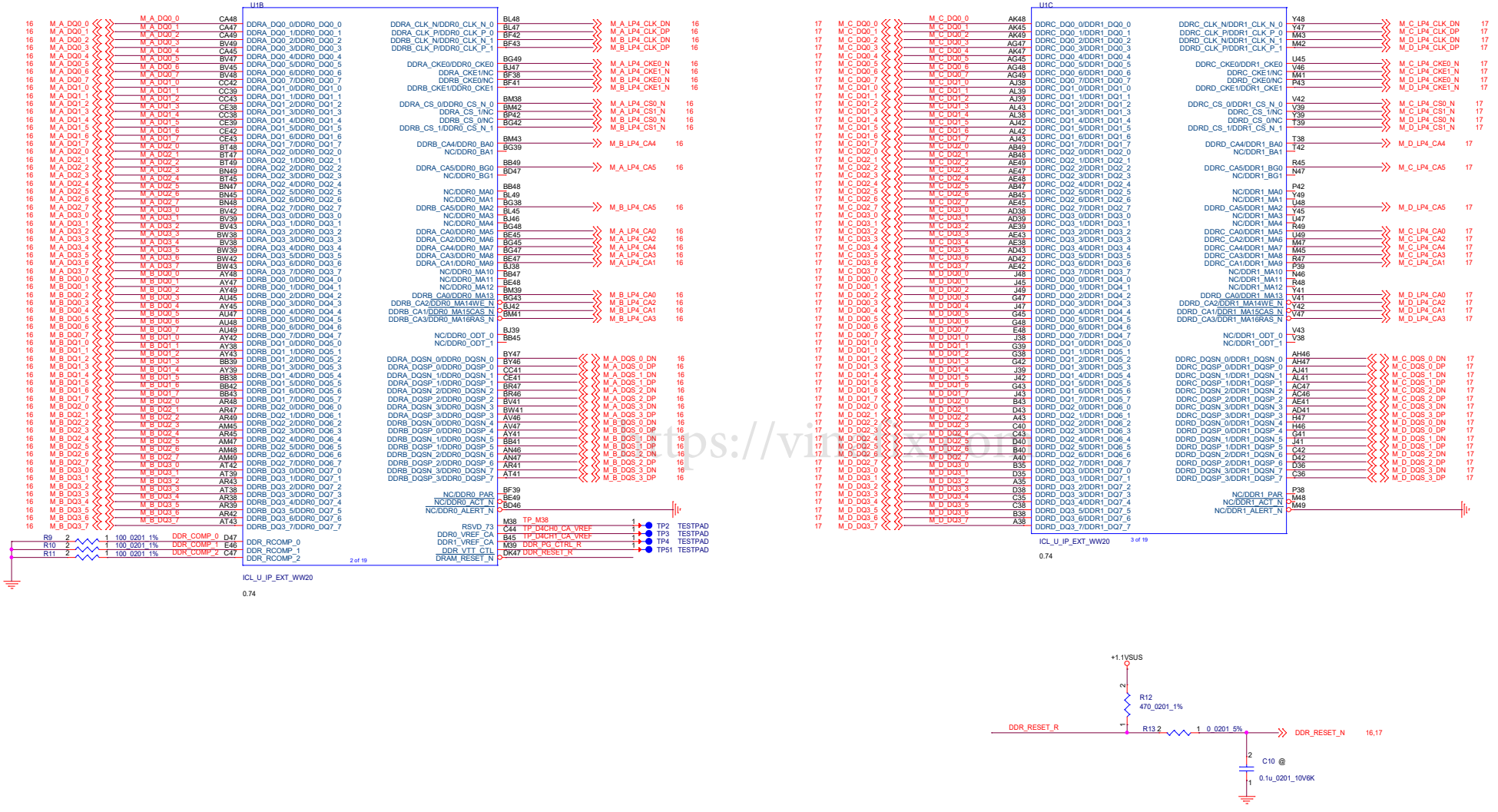

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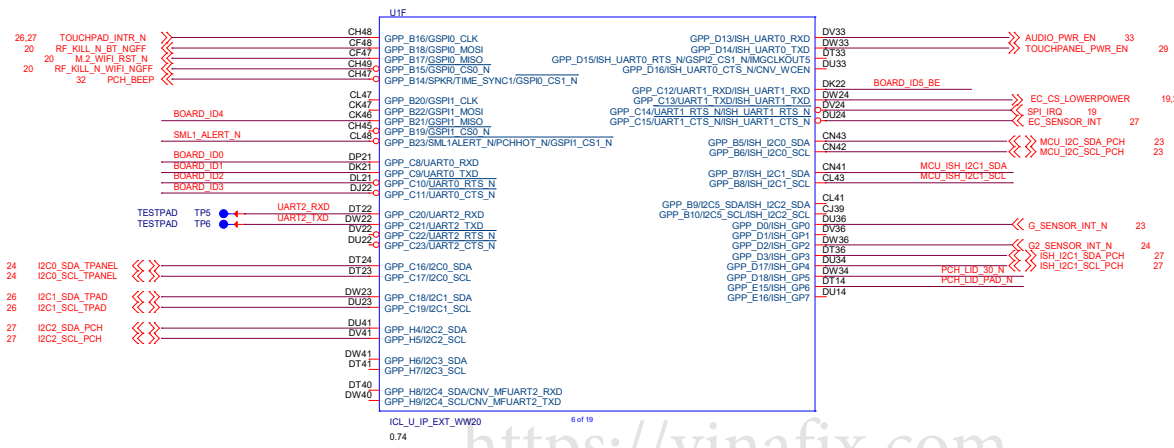
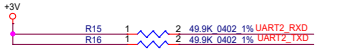
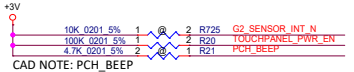
Title: Ice Lake MCP (PROCESSOR LPDDR4)

Size	Document Number	Rev
C	YOGAC940	V0.5

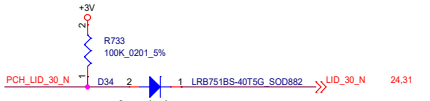
Date: Thursday, June 13, 2019 Sheet 3 of 50

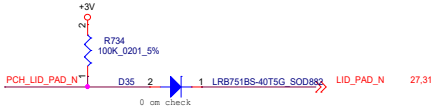


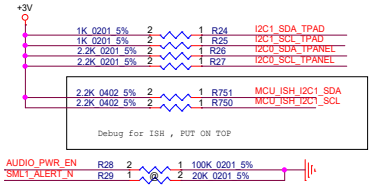




CAD NOTE: PCH_BEEP
0=DISABLE "TOP SWAP MODE".(DEFAULT)
1=ENABLE "TOP SWAP MODE"
INTERNAL 20K PD.

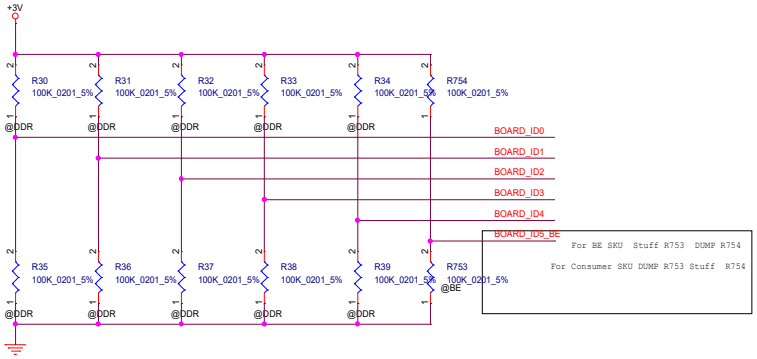






CAD NOTE: SML1_ALERT_N
0=38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)
1=19.2MHZ CLOCK FROM DIVIDER
INTERNAL 20K PD.

BOARD ID



lenovo联想 LENOVO.CRDN

Title: Ice Lake MCP (I2C ISH UART GPIO)

Size	Document Number	Rev
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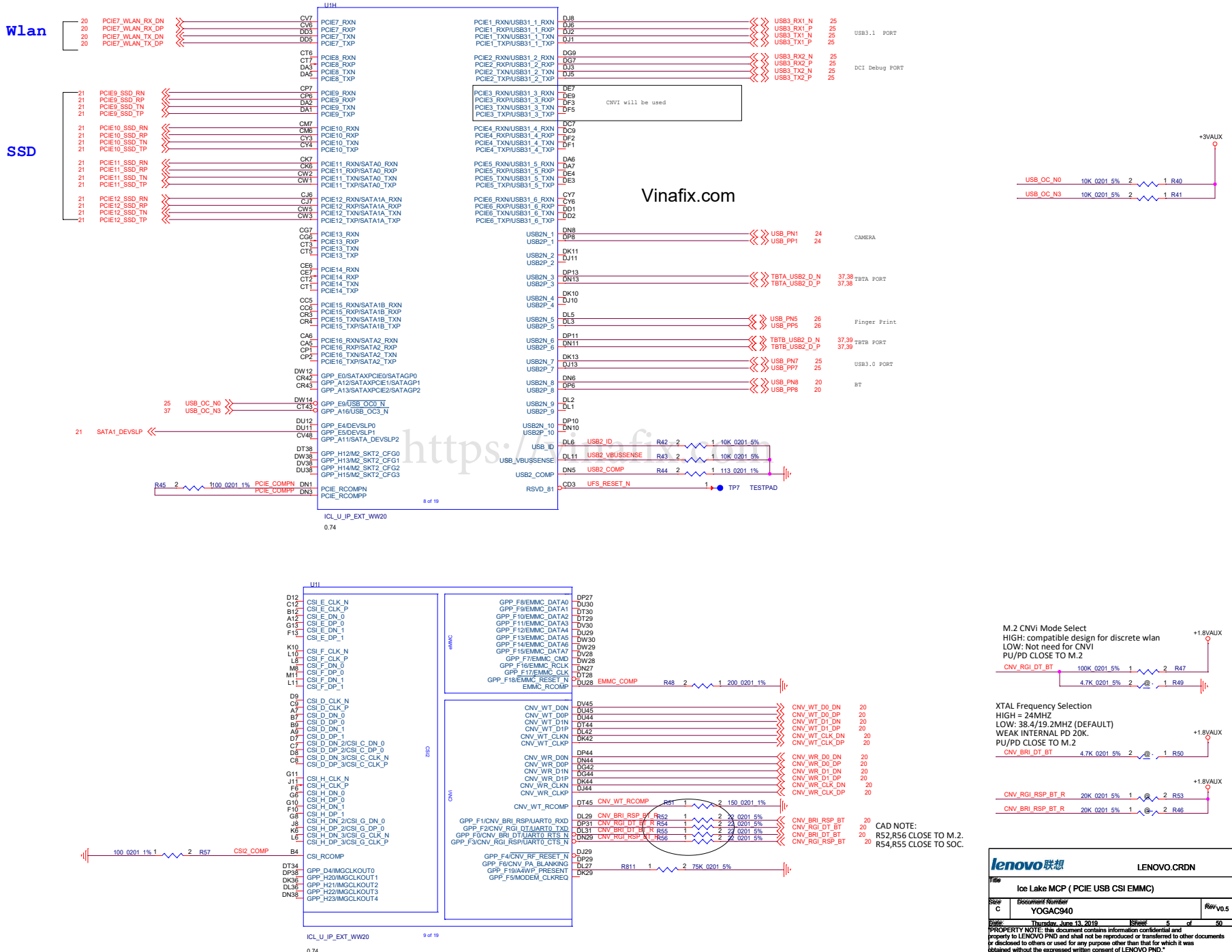

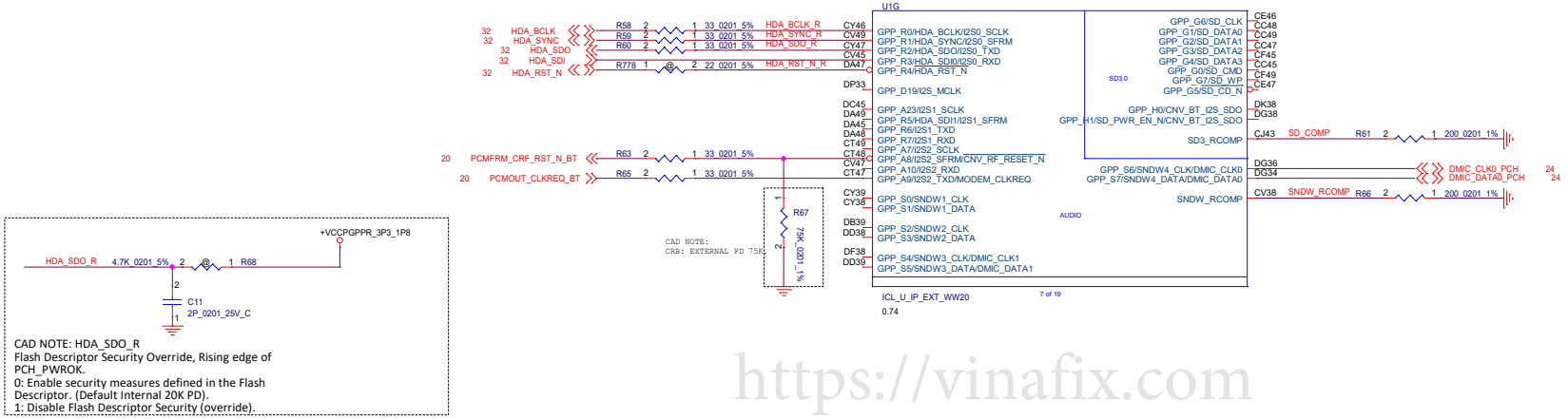

CAD NOTE: HDA_SDO_R
Flash Descriptor Security Override, Rising edge of PCH_PWROK.
0: Enable security measures defined in the Flash Descriptor. (Default Internal 20K PD).
1: Disable Flash Descriptor Security (override).

lenovo联想	LENOVO.CRDN	
Title: Ice Lake MCP (HDA/I2S/SDIO/DMIC)		
Size: C	Document Number: YOGAC940	Rev: V0.5
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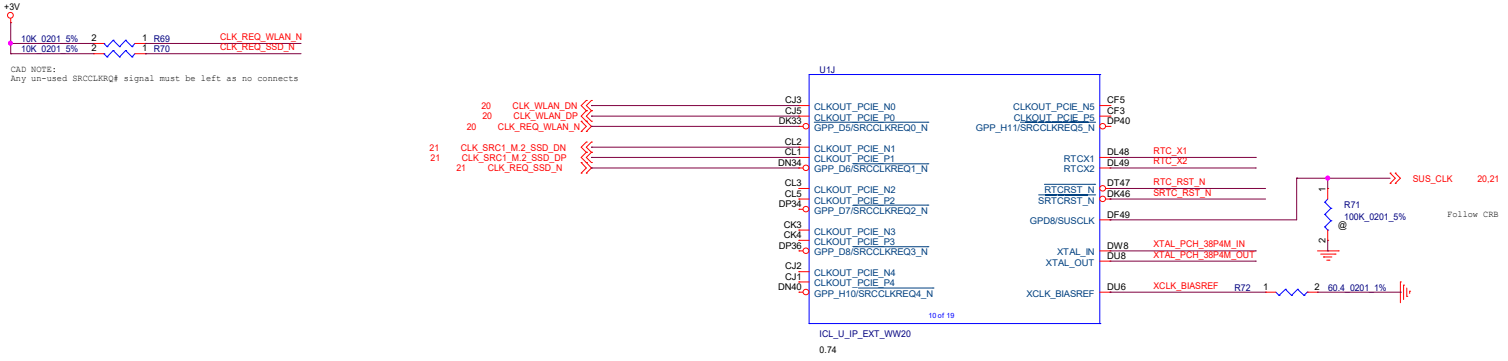
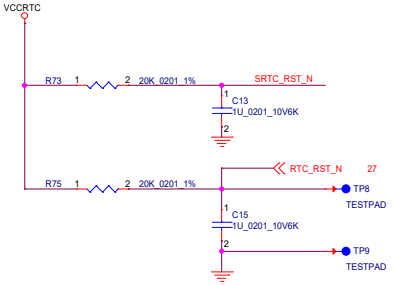
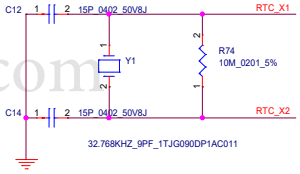


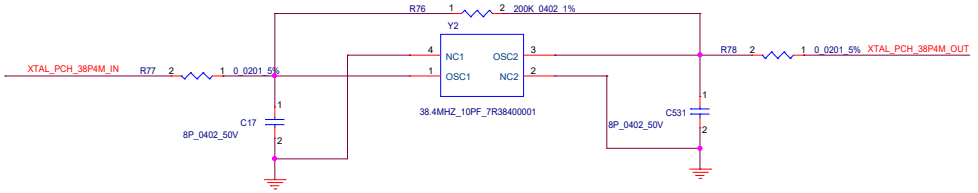


ME RESET
SAVE ME = PU (Default)
CLEAR ME = PD

CMOS RESET
SAVE CMOS = PU (Default)
CLEAR CMOS = PD

TP8 TP9 Need to put on the TOP



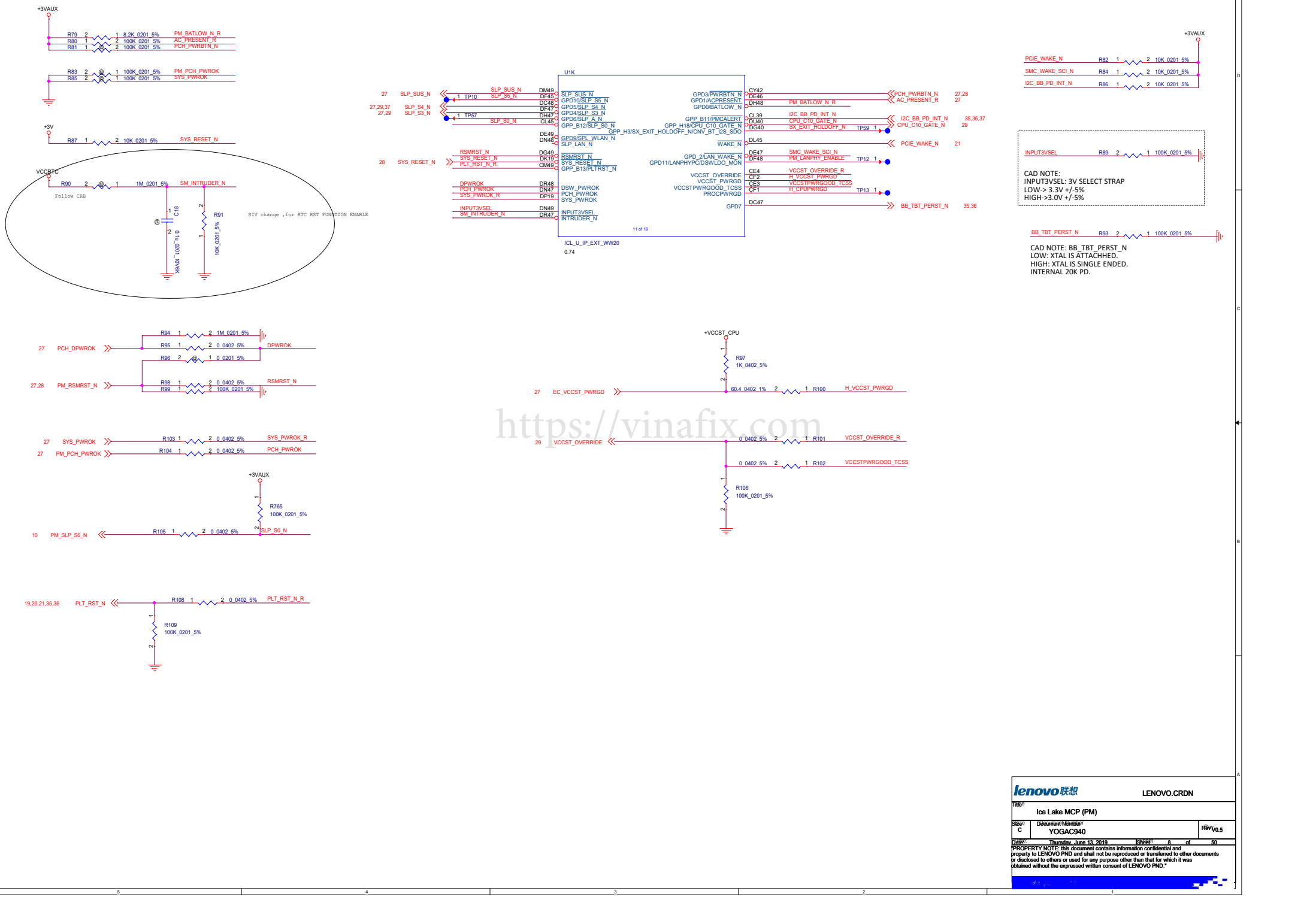


lenovo联想 LENOVO.CRDN

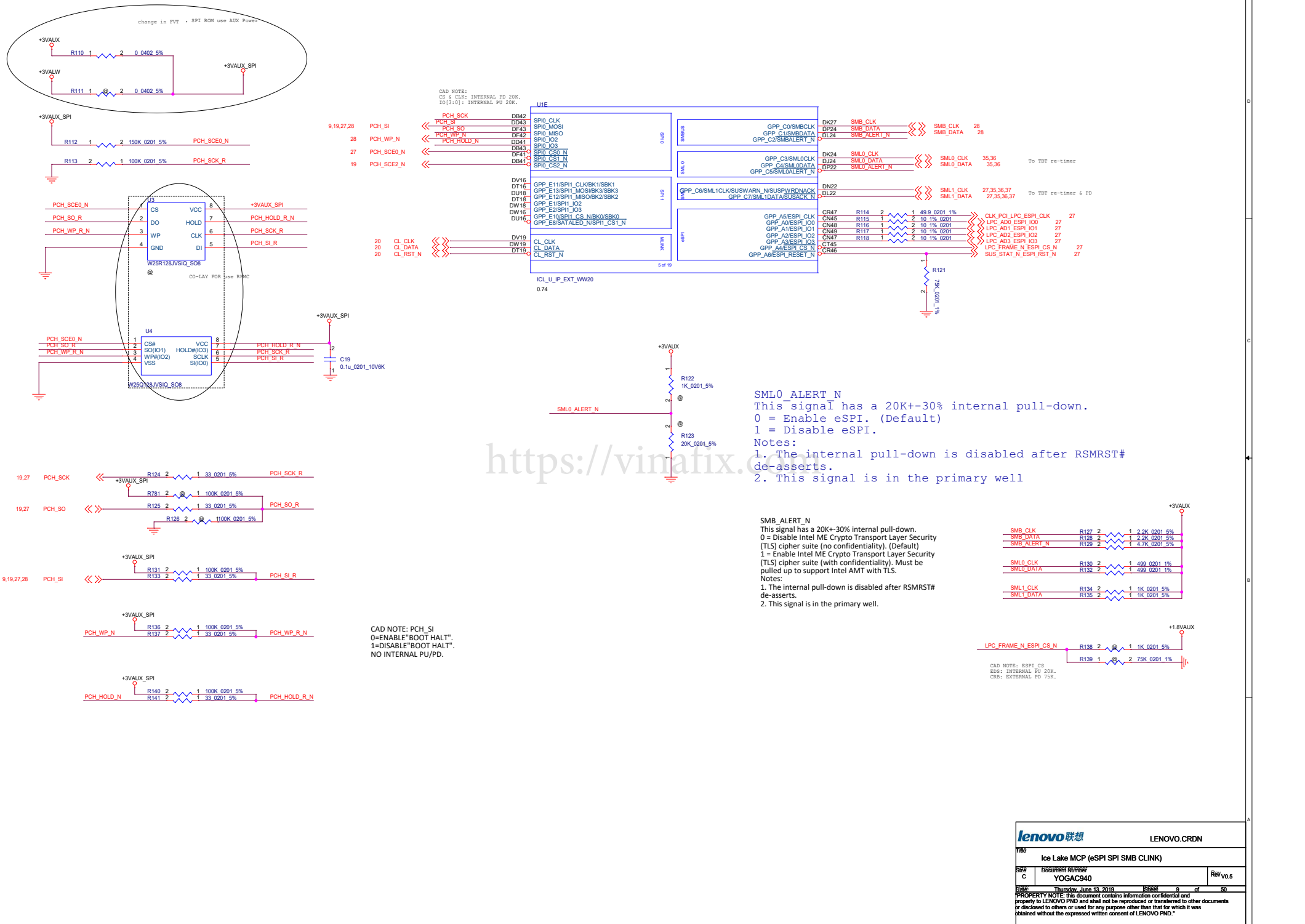
Title: Ice Lake MCP (CLK)

Size: C | Document Number: YOGAC940 | Rev: V0.5

Date: Thursday, June 13, 2019 | Sheet 7 of 50



lenovo联想	LENOVO.CRDN
Title	Ice Lake MCP (PM)
Size: C	Document Number: YOGAC940
Rev	V0.5
Date: Thursday, June 13, 2019	Sheet 8 of 50



lenovo联想 LENOVO.CRDN

Title: Ice Lake MCP (eSPI SPI SMB CLINK)

Size	Document Number	Rev
C	YOGAC940	V0.5

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CAD NOTE: PM_SLP_S0IX_R_N
0=JTAG ODT DISABLED
1=JTAG ODT ENABLED

+3VAUX
100K 0201 5% R142 PM_SLP_S0IX_R_N
2.2K 0201 5% @ R143 M.2_WLAN_WIFI_WAKE_R_N

This signal has a 20 K+- 30% internal pull-down.
0 = Master Attached Flash Sharing (MAFS) is enabled.
(Default)
1 = Slave Attached Flash Sharing (SAFS) is enabled.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

+VCCST_CPU
1K 0201 5% R144 PCH_THRMTRIP_N
49.9 0201 1% R145 H_CATERR_N

+3V
10K 0201 5% R146 SCI_N
10K 0201 5% R147 KBSMI_N
100K 0201 5% R148 TOUCH_PANEL_INTR_N

+VCCSTG_TERM
51 0201 5% R756 PCH_JTAG_TDO_CPU
51 0201 5% R151 PCH_JTAG_TDI_CPU
51 0201 5% R152 PCH_JTAG_TMS_CPU

+VCCSTG_TERM
12,27,41,42 H_PROCHOT_N
R153 1K 0201 5%
R154 499 0402 1% H_PROCHOT_R_N

CAD NOTE:
RCOMP NEEDED ONLY FOR ICL U43E SOC ON A14 & B14 PINS

R155 51 0201 5% PCH_TCK_JTAGX_CPU
R158 49.9 0201 1% CPU_POPIRCOMP
R159 49.9 0201 1% PCH_POPIRCOMP

U1D
27 PECI_EC
H_CATERR_N J4 CATERR_N
H_PROCHOT_R_N C3 PROCHOT_N
PCH_THRMTRIP_N E3 THRMTRIP_N
CPU_POPIRCOMP CJ41 PROC_POPIRCOMP
PCH_POPIRCOMP DU3 PCH_OPIRCOMP
A14 RSVD_25
B14 RSVD_26
28 DBG_PMODE DL15 DBG_PMODE
27 SCI_N DV11 GPP_E3/CPU_GP0
27 KBSMI_N DT11 GPP_E7/CPU_GP1
24 TOUCH_PANEL_INTR_N CR38 GPP_B3/CPU_GP2
35,36,37 BB_TBT_FORCE_PWR CR39 GPP_B4/CPU_GP3
8 PM_SLP_S0_N R149 @ 10 0201 5% PM_SLP_S0IX_R_N DT12 GPP_E6
20 M.2_WLAN_WIFI_WAKE_R_N DJ38 GPP_H2/CNV_BT_I2S_SDO
20 UART_BT_WAKE_N DL38 GPP_H19/TIME_SYNC0
4 of 19
ICL_U_IP_EXT_WW20
0.74

PROC_TCK P3 PCH_TCK_JTAGX_CPU
PROC_TDI K5 PCH_JTAG_TDI_CPU
PROC_TDO K3 PCH_JTAG_TDO_CPU
PROC_TMS P4 PCH_JTAG_TMS_CPU
PROC_TRST_N N1 XDP_TRST_CPU_N
PCH_TRST_N N5 XDP_TRST_CPU_N 28
PCH_TCK R5 PCH_JTAG_TCK 28
PCH_TDI K1 PCH_JTAG_TDI_CPU 28
PCH_TDO K2 PCH_JTAG_TDO_CPU 28
PCH_TMS N3 PCH_JTAG_TMS_CPU 28
PCH_JTAGX N2 PCH_TCK_JTAGX_CPU 28
PROC_PRDY_N P6 PROC_PRDY_N PROC_PRDY_N 28
PROC_PREQ_N M6 PROC_PREQ_N PROC_PREQ_N 28

lenovo联想 LENOVO.CRDN
Title: Ice Lake MCP (MISC THERM CPU JTAG)
Size: C | Document Number: YOGAC940 | Rev: V0.5
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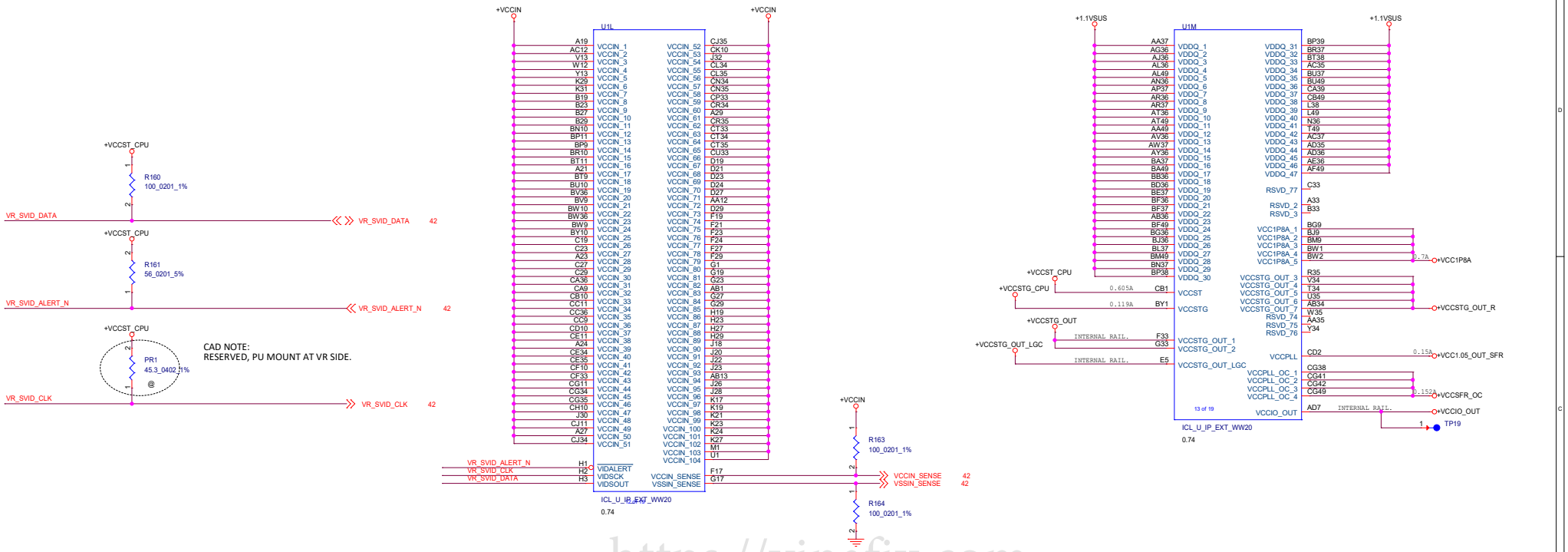
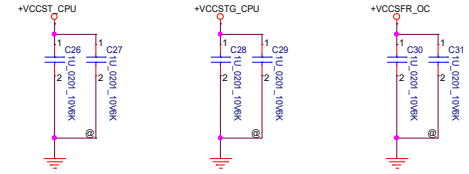


VCCST, VCCSTG, VCCSFR_OC DE-COUPLING

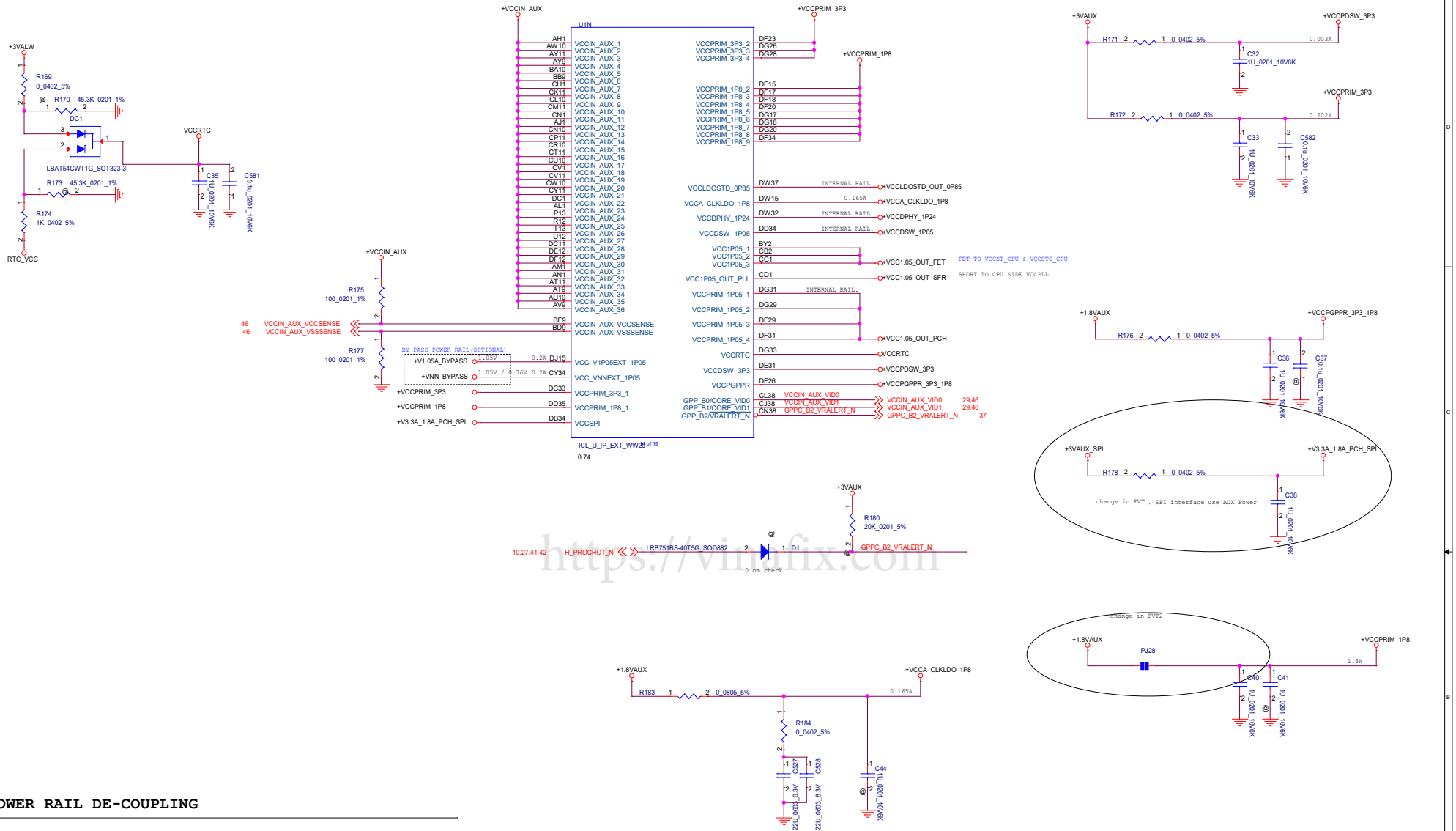


lenovo联想 LENOVO.CRDN

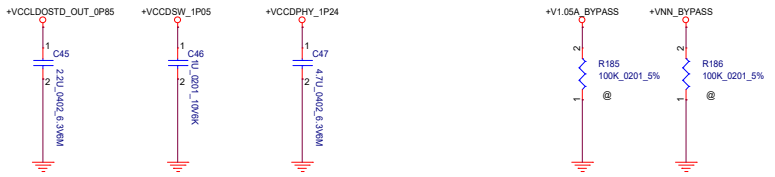
Title: Ice Lake MCP (PROCESSOR POWER)

Size: C | Document Number: YOGAC940 | Rev: V0.5

Date: Thursday, June 13, 2019 | Sheet 11 of 50

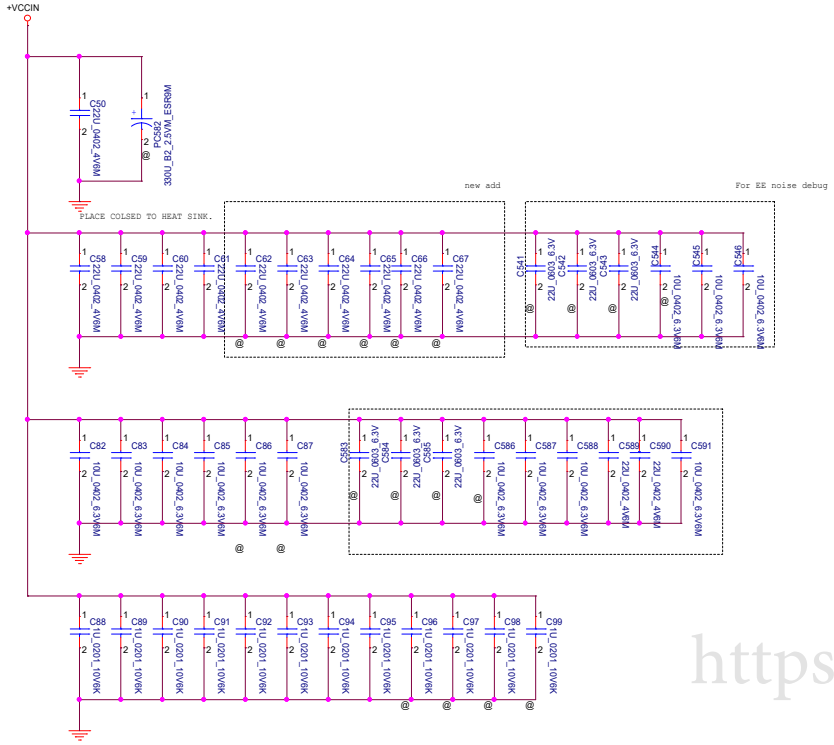


PCH POWER RAIL DE-COUPLING

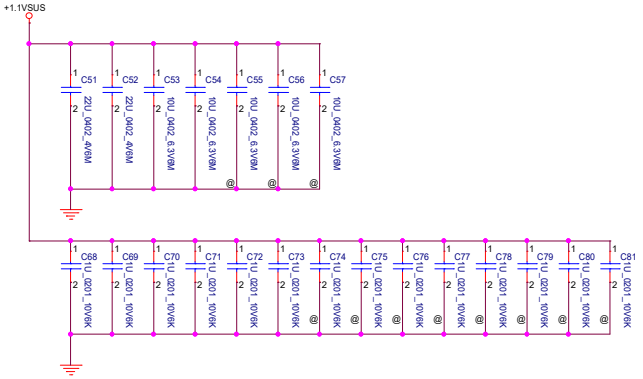


lenovo联想	LENOVO.CRDN	
Title: Ice Lake MCP (PCH POWER)		
Size: C	Document Number: YOGAC940	Rev: V0.5
Date: Thursday, June 13, 2019	Sheet 12 of 50	

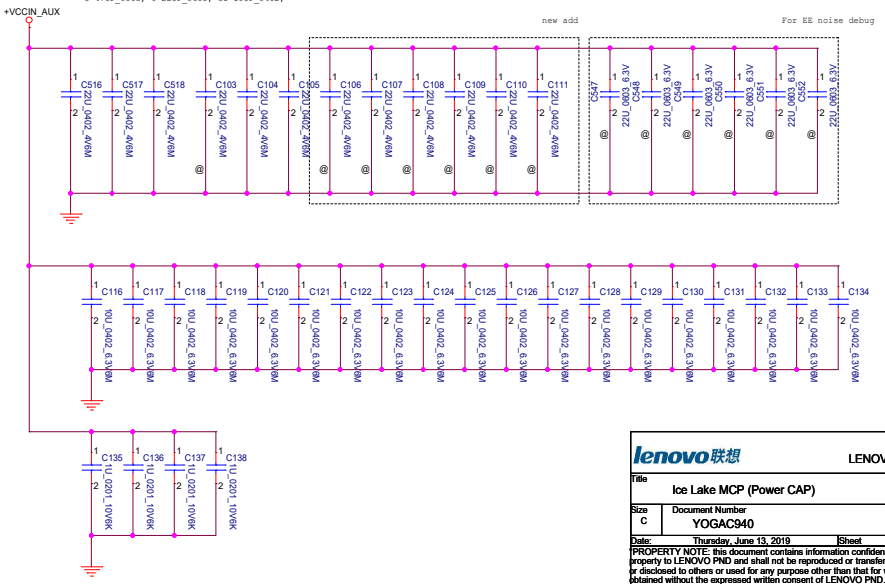
+VCCIN:
11*330UF, 16*47UF_0805, 21*22UF_0603, 36*10UF_0402



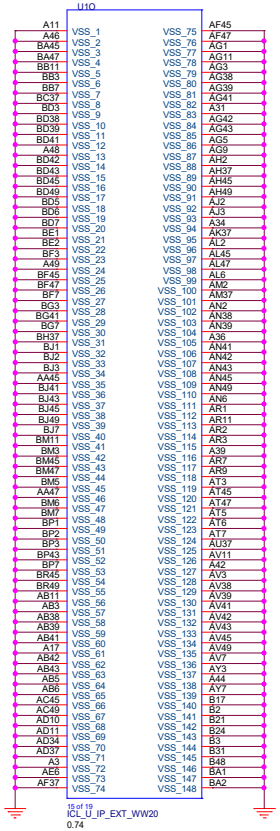
+VCCIN(CRB):
3*22UF_0603, 3*10UF_0402, 30*1UF_0402, 3*2.2pf_0402, 3*12pf_0402

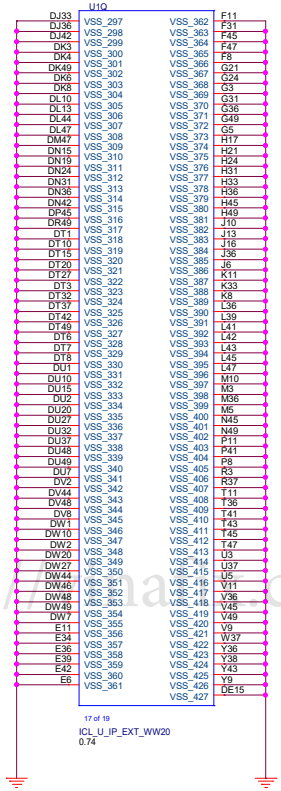


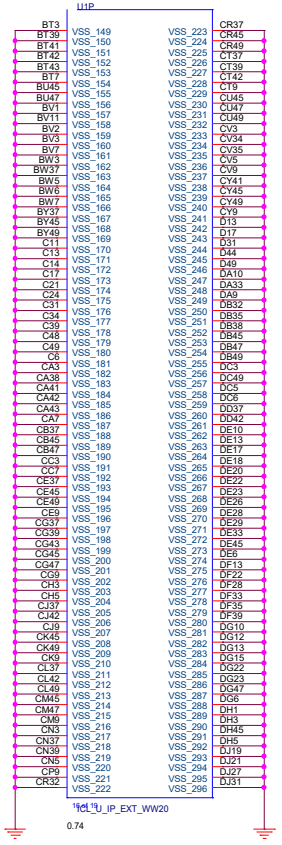
+VCCIN_AUX(CRB):
8*47UF_0805, 6*22UF_0603, 31*10UF_0402,



lenovo联想	LENOVO.CRDN	
Title: Ice Lake MCP (Power CAP)		
Size: C	Document Number: YOGAC940	Rev: V0.5
Date: Thursday, June 13, 2019	Sheet 13 of 50	







lenovo联想 LENOVO.CRDN

Title: Ice Lake MCP (GND)

Size: C | Document Number: YOGAC940 | Rev: V0.5

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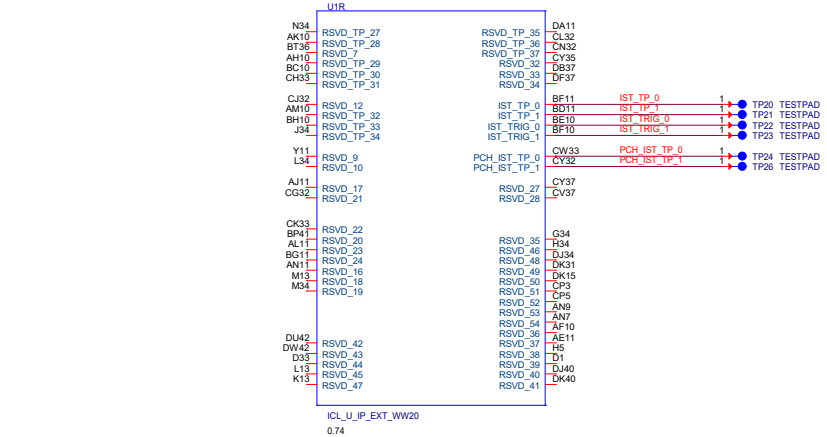
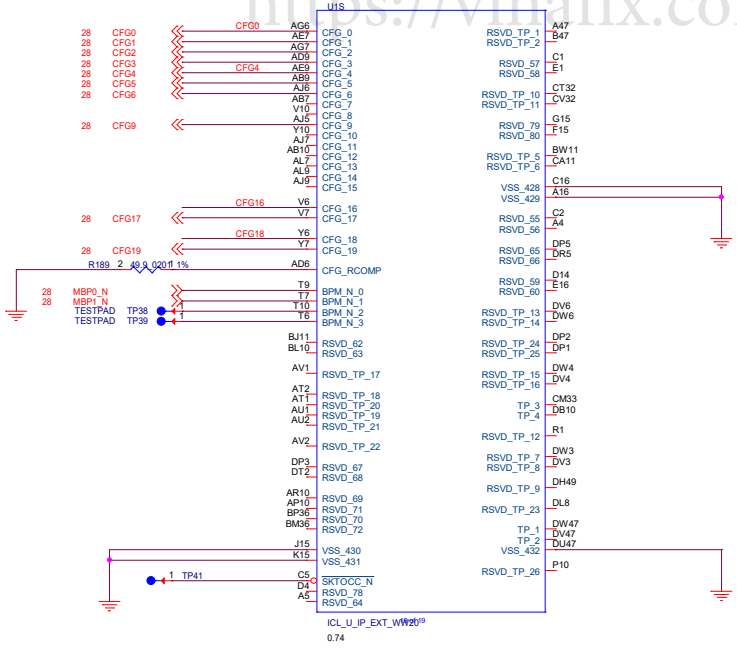




PROCESSOR CFG STRAPS

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	1:Normal(Default) *
	0:Stall

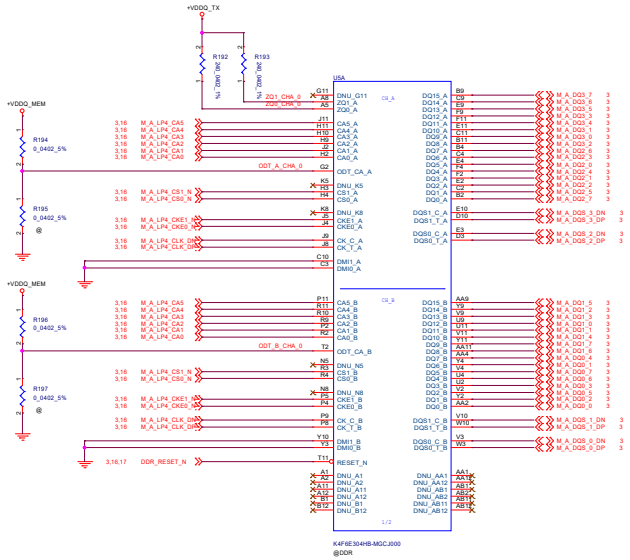
Embedded Display Port Presence Strap	
CFG4	1:Disable
	0:Enable(Default) *

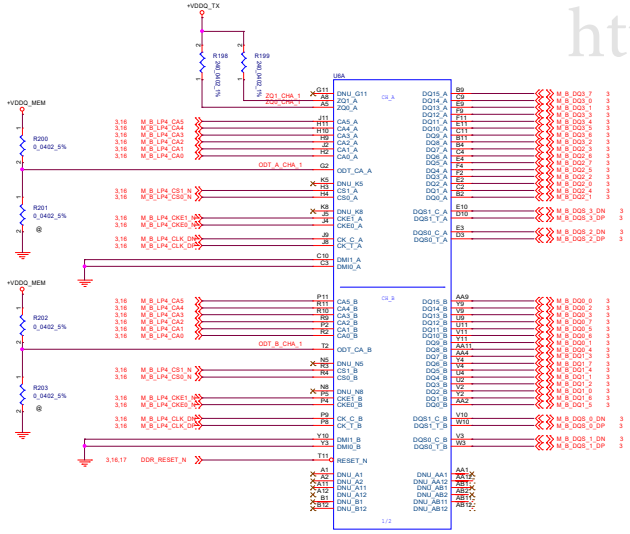
lenovo联想 LENOVO.CRDN

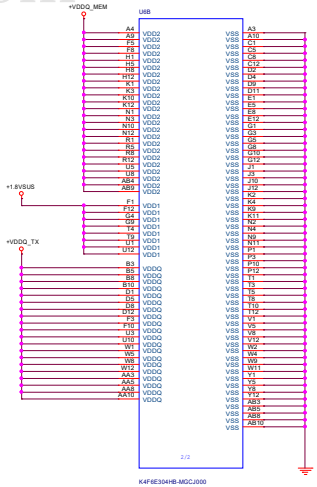
Title: Ice Lake MCP (RSVD)

Size: C | Document Number: YOGAC940 | Rev: V0.5

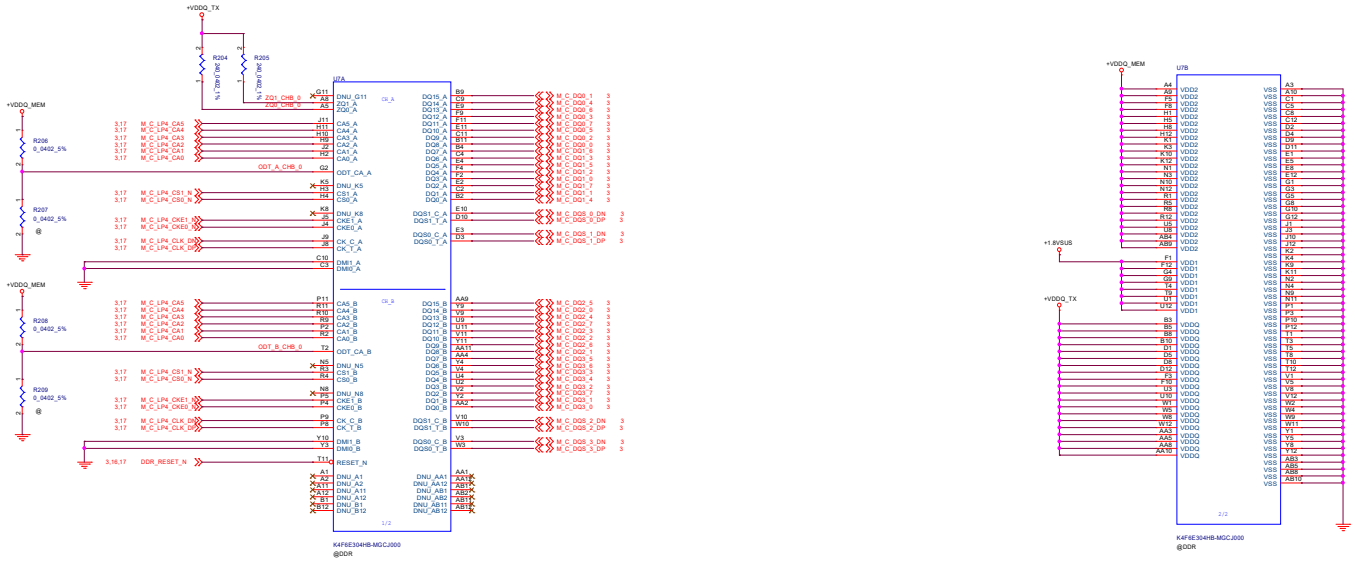
Date: Thursday, June 13, 2019 | Sheet 15 of 50

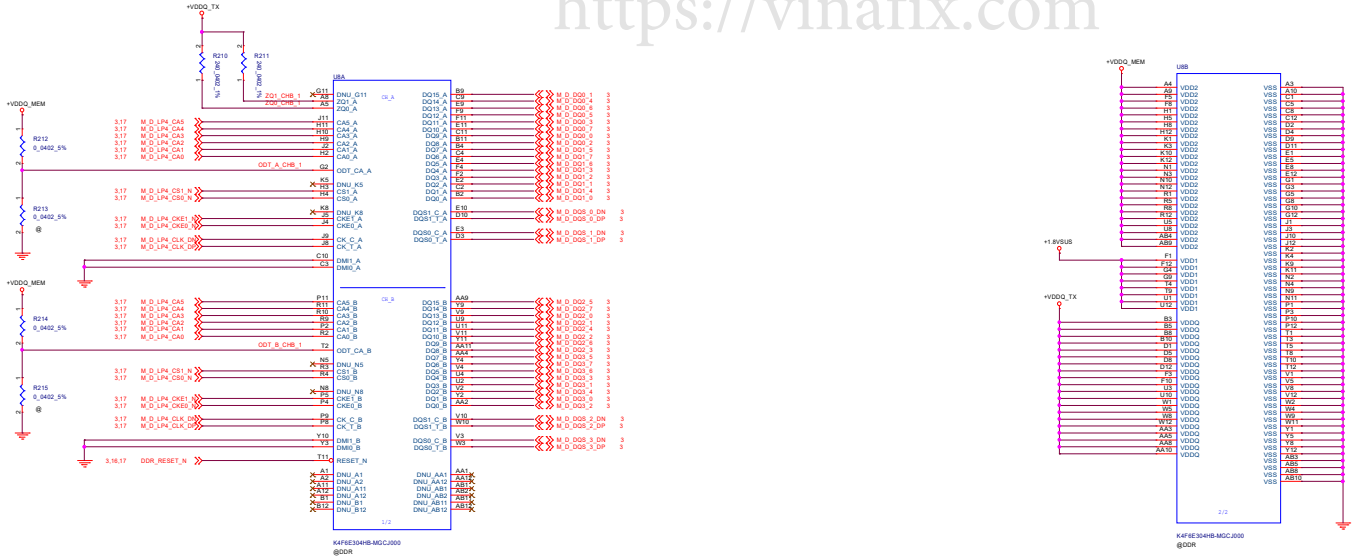




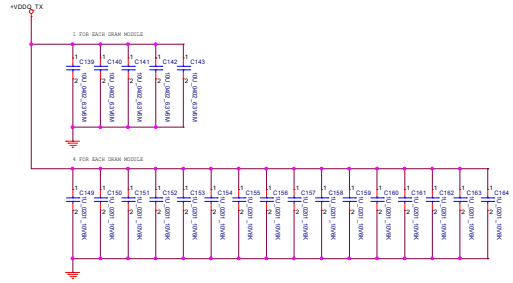


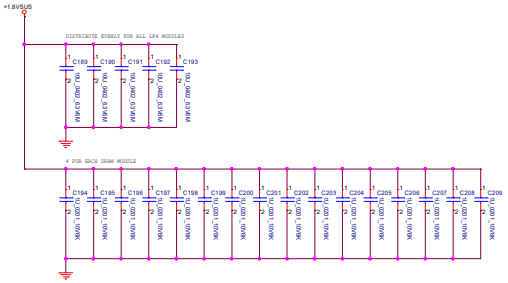
lenovo 联想	LENOVO.CRDN		
Title	LP4X-CHA ONBD		
Size D	Document Number YOGAC940		Rev V0.5
Date: Thursday, June 13, 2019	Sheet 16 of 50		

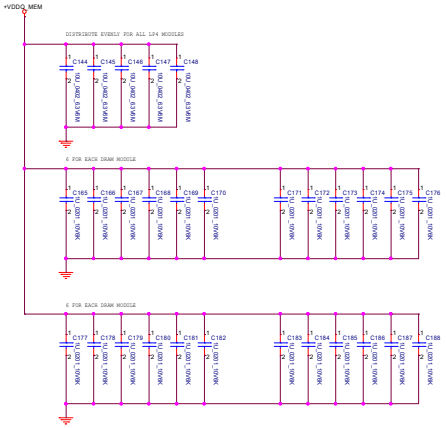




lenovo联想		LENOVO.CRDN	
Title	LP4X-CHB ONBD		
Size	Document Number		Rev
D	YOGA C940		V0.5
Date:	Thursday, June 13, 2019	Sheet 17 of 50	





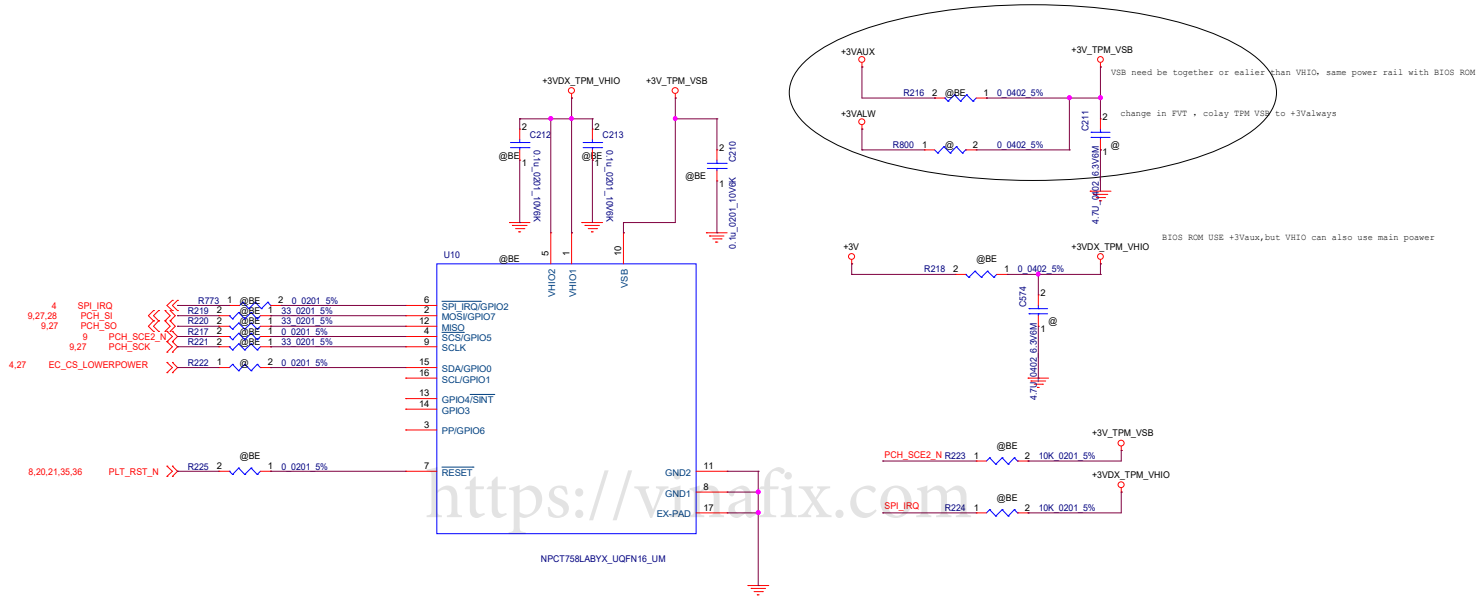


lenovo联想 LENOVO.CRDN

Title: LP4X-DECOUPLING

Size: D | Document Number: YOGA940 | Rev: V0.4

Date: Thursday, June 13, 2019 | Sheet 18 of 50

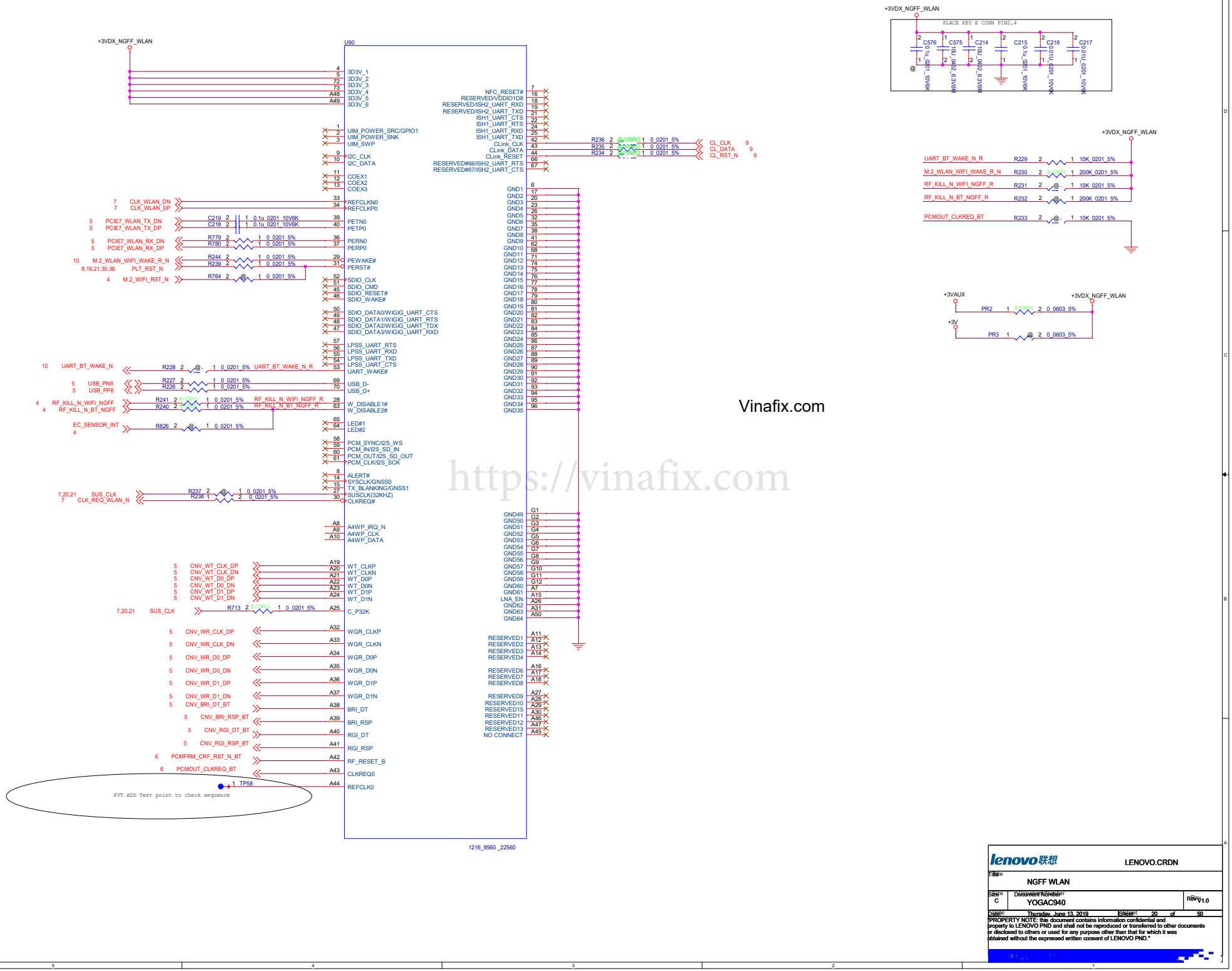


lenovo联想 LENOVO.CRDN

Title: TPM

Size: C | Document Number: YOGAC940 | Rev: V1.0

Date: Thursday, June 13, 2019 | Sheet 19 of 50


+3VDX_NGFF_WLAN
U90
3D3V_1
3D3V_2
3D3V_3
3D3V_4
3D3V_5
3D3V_6
UIM_POWER_SRC/GPIO1
UIM_POWER_SNK
UIM_SWP
I2C_CLK
I2C_DATA
COEX1
COEX2
COEX3
REFCLKN0
REFCLKP0
PETN0
PETP0
PERN0
PERP0
PEWAKE#
PERST#
SDIO_CLK
SDIO_CMD
SDIO_RESET#
SDIO_WAKE#
SDIO_DATA0/WIGIG_UART_CTS
SDIO_DATA1/WIGIG_UART_RTS
SDIO_DATA2/WIGIG_UART_TDX
SDIO_DATA3/WIGIG_UART_RXD
LPSS_UART_RTS
LPSS_UART_RXD
LPSS_UART_TXD
LPSS_UART_CTS
UART_WAKE#
USB_D-
USB_D+
W_DISABLE1#
W_DISABLE2#
LED#1
LED#2
PCM_SYNC/I2S_WS
PCM_IN/I2S_SD_IN
PCM_OUT/I2S_SD_OUT
PCM_CLK/I2S_SCK
ALERT#
SYSCLK/GNSS0
TX_BLANKING/GNSS1
SUSCLK(32KHZ)
CLKREQ#
A4WP_IRQ_N
A4WP_CLK
A4WP_DATA
WT_CLKP
WT_CLKN
WT_D0P
WT_D0N
WT_D1P
WT_D1N
C_P32K
WGR_CLKP
WGR_CLKN
WGR_D0P
WGR_D0N
WGR_D1P
WGR_D1N
BRI_DT
BRI_RSP
RGI_DT
RGI_RSP
RF_RESET_B
CLKREQ0
REFCLK0
TP58
FVT ADD Test point to check sequence
NFC_RESET#
RESERVED/VDDIO1D8
RESERVED/ISH2_UART_RXD
RESERVED/ISH2_UART_TXD
ISH1_UART_CTS
ISH1_UART_RTS
ISH1_UART_RXD
ISH1_UART_TXD
CLink_CLK
CLink_DATA
CLink_RESET
RESERVED#66/ISH2_UART_RTS
RESERVED#67/ISH2_UART_CTS
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
GND16
GND17
GND18
GND19
GND20
GND21
GND22
GND23
GND24
GND25
GND26
GND27
GND28
GND29
GND30
GND31
GND32
GND33
GND34
GND35
GND49
GND50
GND51
GND52
GND53
GND54
GND55
GND56
GND57
GND58
GND59
GND60
GND61
LNA_EN
GND62
GND63
GND64
RESERVED1
RESERVED2
RESERVED3
RESERVED4
RESERVED6
RESERVED7
RESERVED8
RESERVED9
RESERVED10
RESERVED15
RESERVED11
RESERVED12
RESERVED13
NO CONNECT
1216_9560 _22560
CL_CLK
CL_DATA
CL_RST_N
CLK_WLAN_DN
CLK_WLAN_DP
PCIE7_WLAN_TX_DN
PCIE7_WLAN_TX_DP
PCIE7_WLAN_RX_DN
PCIE7_WLAN_RX_DP
M.2_WLAN_WIFI_WAKE_R_N
PLT_RST_N
M.2_WIFI_RST_N
UART_BT_WAKE_N
USB_PN8
USB_PP8
RF_KILL_N_WIFI_NGFF
RF_KILL_N_BT_NGFF
EC_SENSOR_INT
SUS_CLK
CLK_REQ_WLAN_N
CNV_WT_CLK_DP
CNV_WT_CLK_DN
CNV_WT_D0_DP
CNV_WT_D0_DN
CNV_WT_D1_DP
CNV_WT_D1_DN
CNV_WR_CLK_DP
CNV_WR_CLK_DN
CNV_WR_D0_DP
CNV_WR_D0_DN
CNV_WR_D1_DP
CNV_WR_D1_DN
CNV_BRI_DT_BT
CNV_BRI_RSP_BT
CNV_RGI_DT_BT
CNV_RGI_RSP_BT
PCMFRM_CRF_RST_N_BT
PCMOUT_CLKREQ_BT
Vinafix.com
https://vinafix.com
+3VDX_NGFF_WLAN
PLACE KEY E CONN PIN2,4
C576
C575
C214
C215
C216
C217
+3VDX_NGFF_WLAN
UART_BT_WAKE_N_R
M.2_WLAN_WIFI_WAKE_R_N
RF_KILL_N_WIFI_NGFF_R
RF_KILL_N_BT_NGFF_R
PCMOUT_CLKREQ_BT
+3VAUX
+3V
+3VDX_NGFF_WLAN
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NGFF WLAN
YOGAC940
Thursday, June 13, 2019
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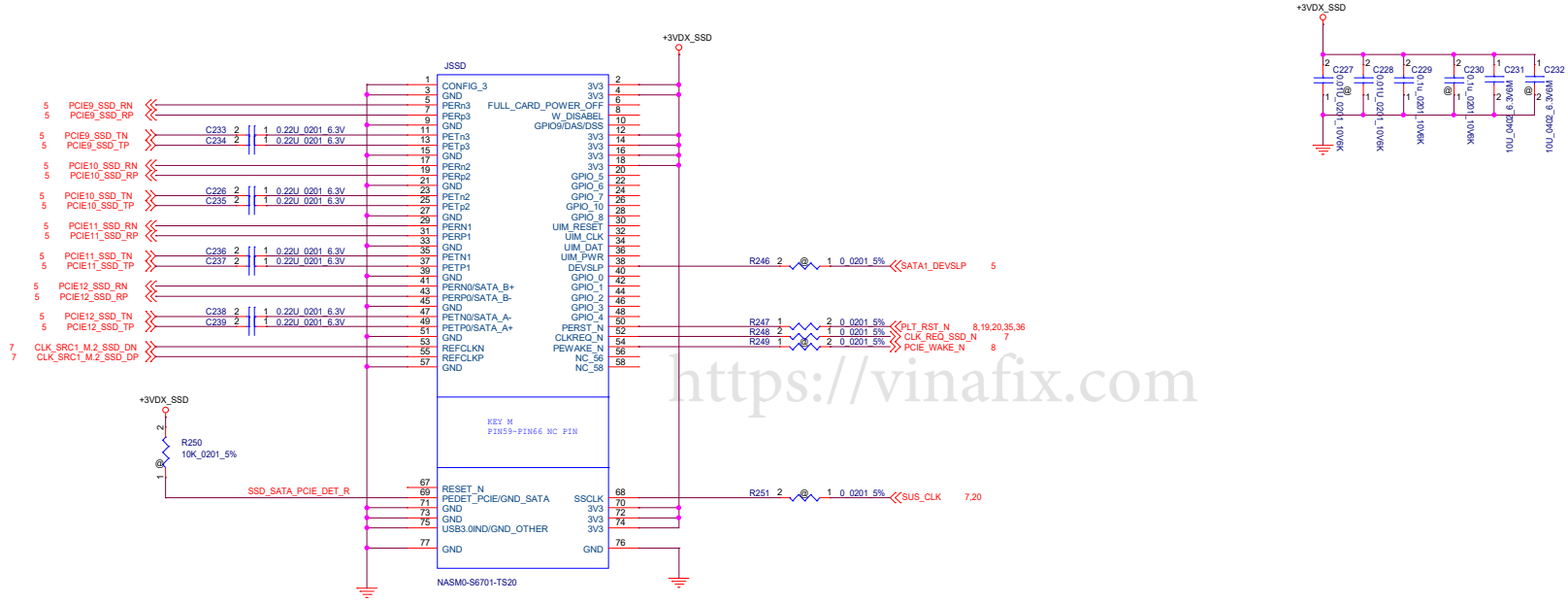

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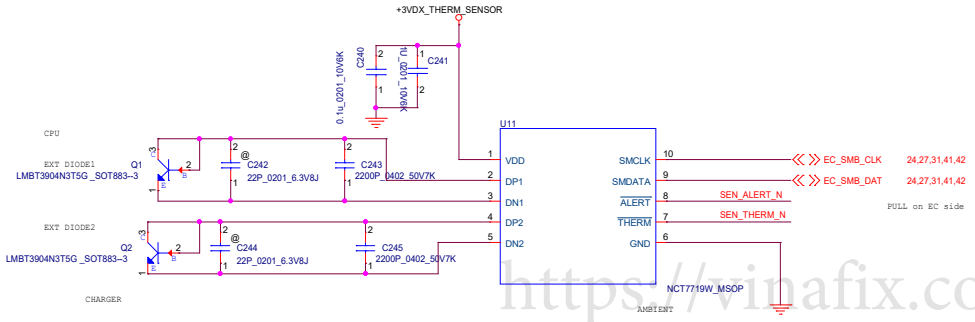
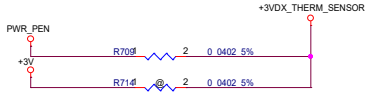
Title: NGFF SSD

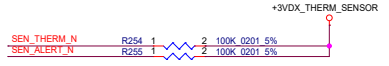
Size: C | Document Number: YOGAC940 | Rev: V1.0

Date: Thursday, June 13, 2019 | Sheet 21 of 50



SMBus ADDRESS:0x9A





Vinafix.com

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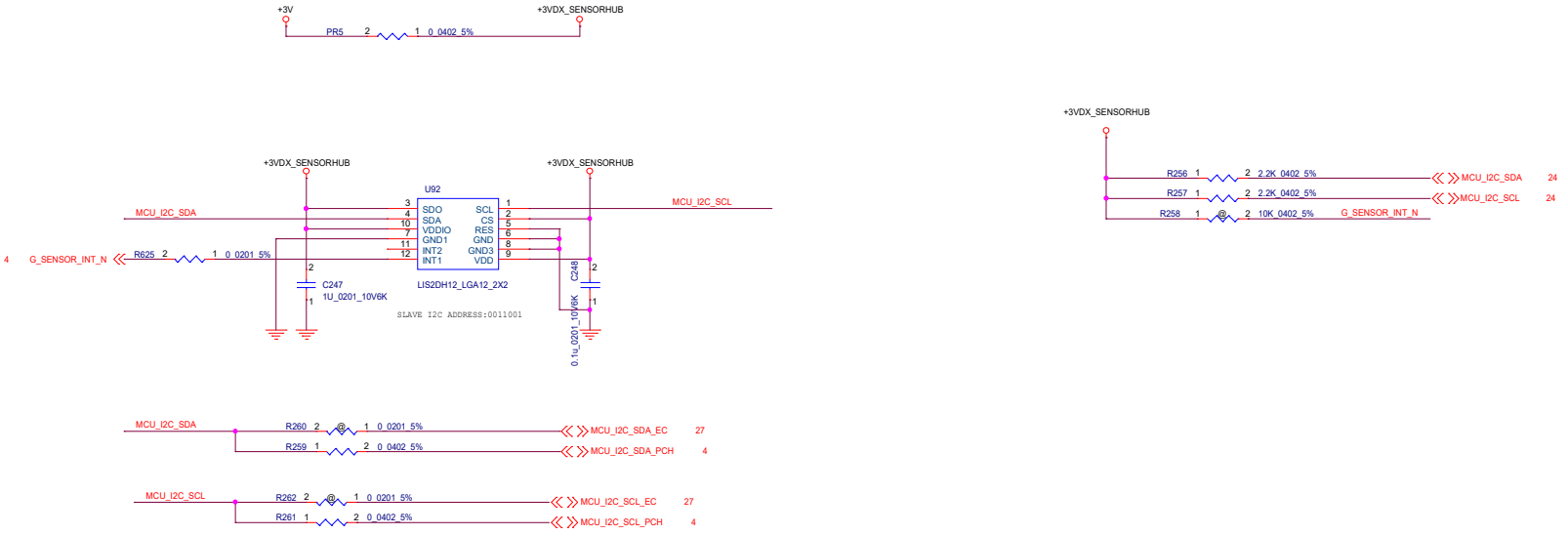
Title: ThermalSensor		
Size: C	Document Number: YOGAC940	Rev: V1.0
Date: Thursday, June 13, 2019	Sheet 22 of 50	



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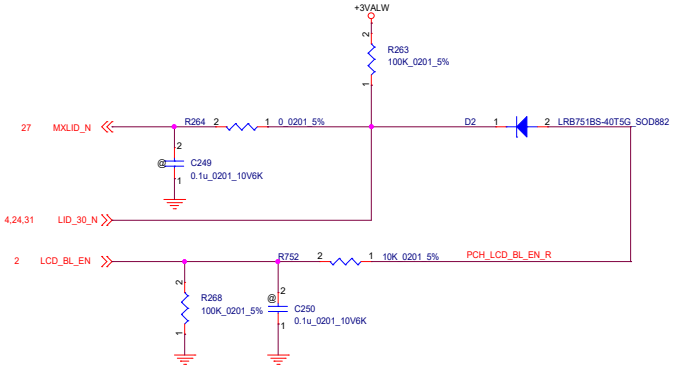
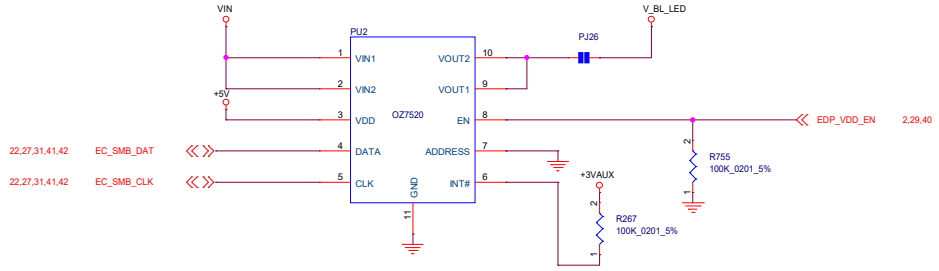
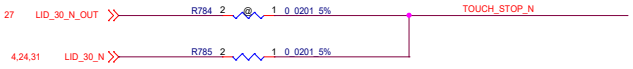
Title: SENSOR

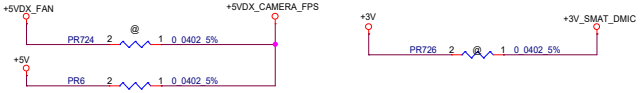
Size: C | Document Number: YOGAC940 | Rev: V1.0

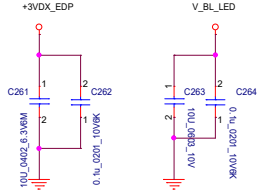
Date: Thursday, June 13, 2019 | Sheet 23 of 50

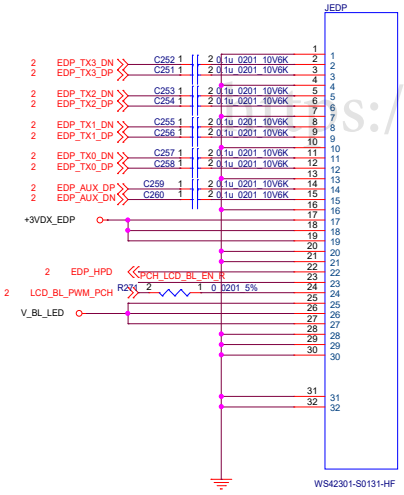


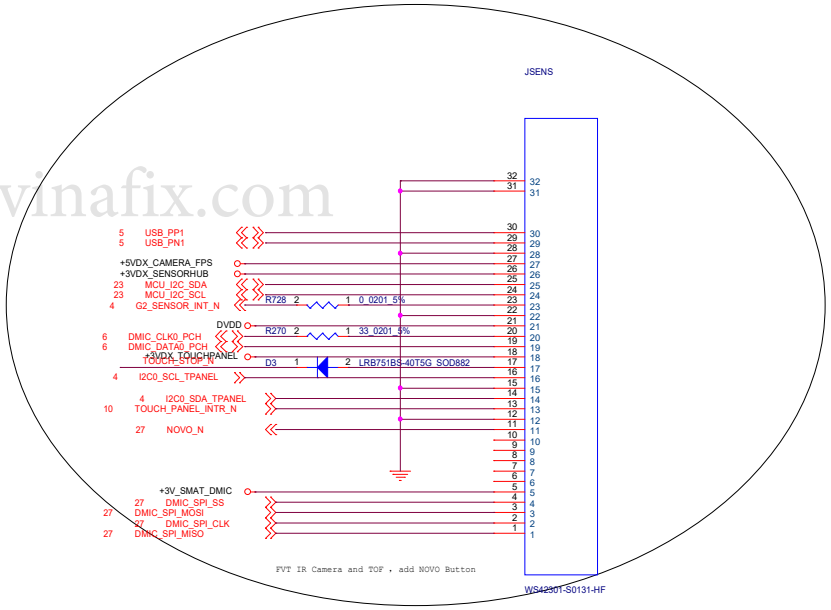












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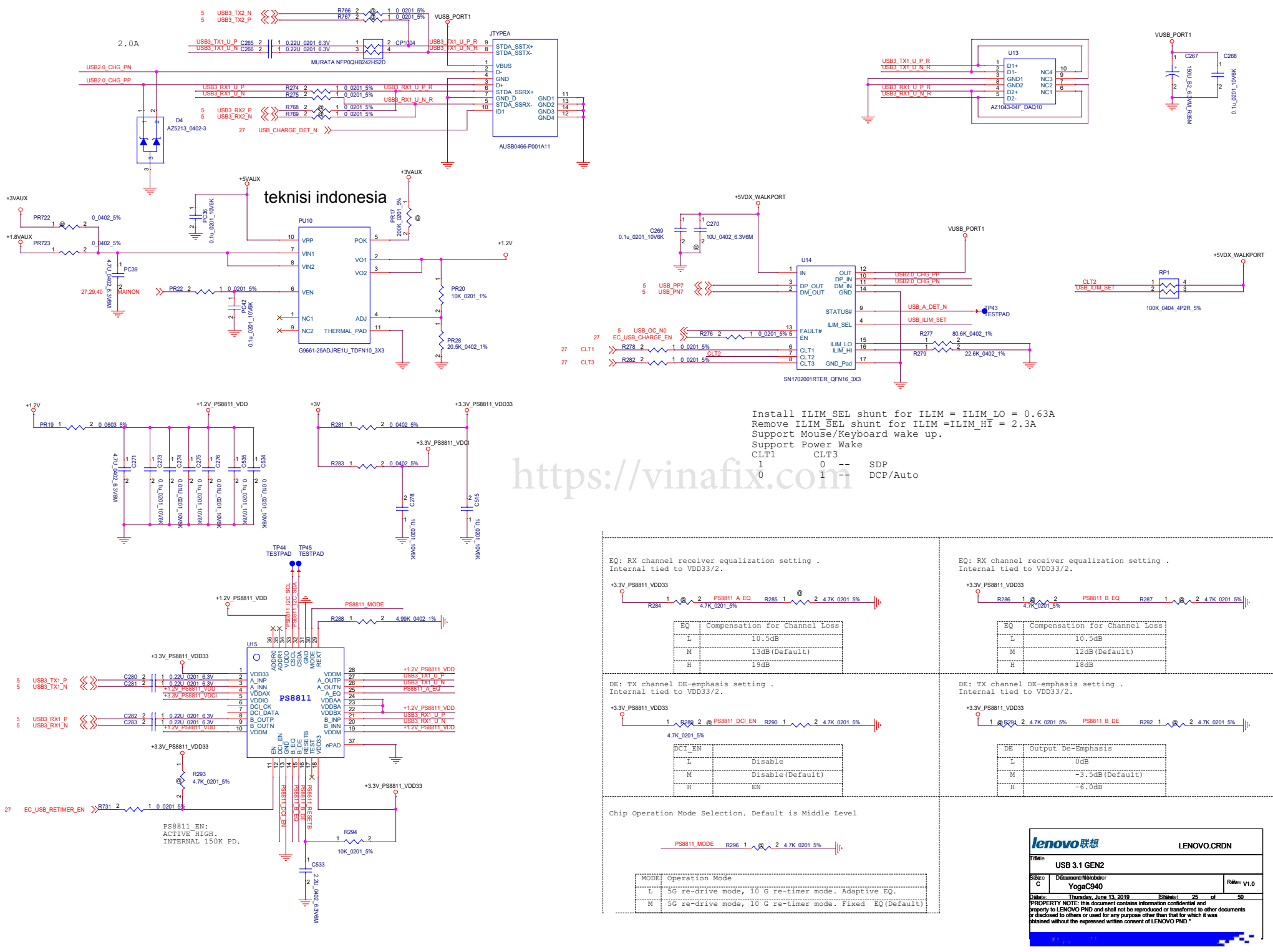
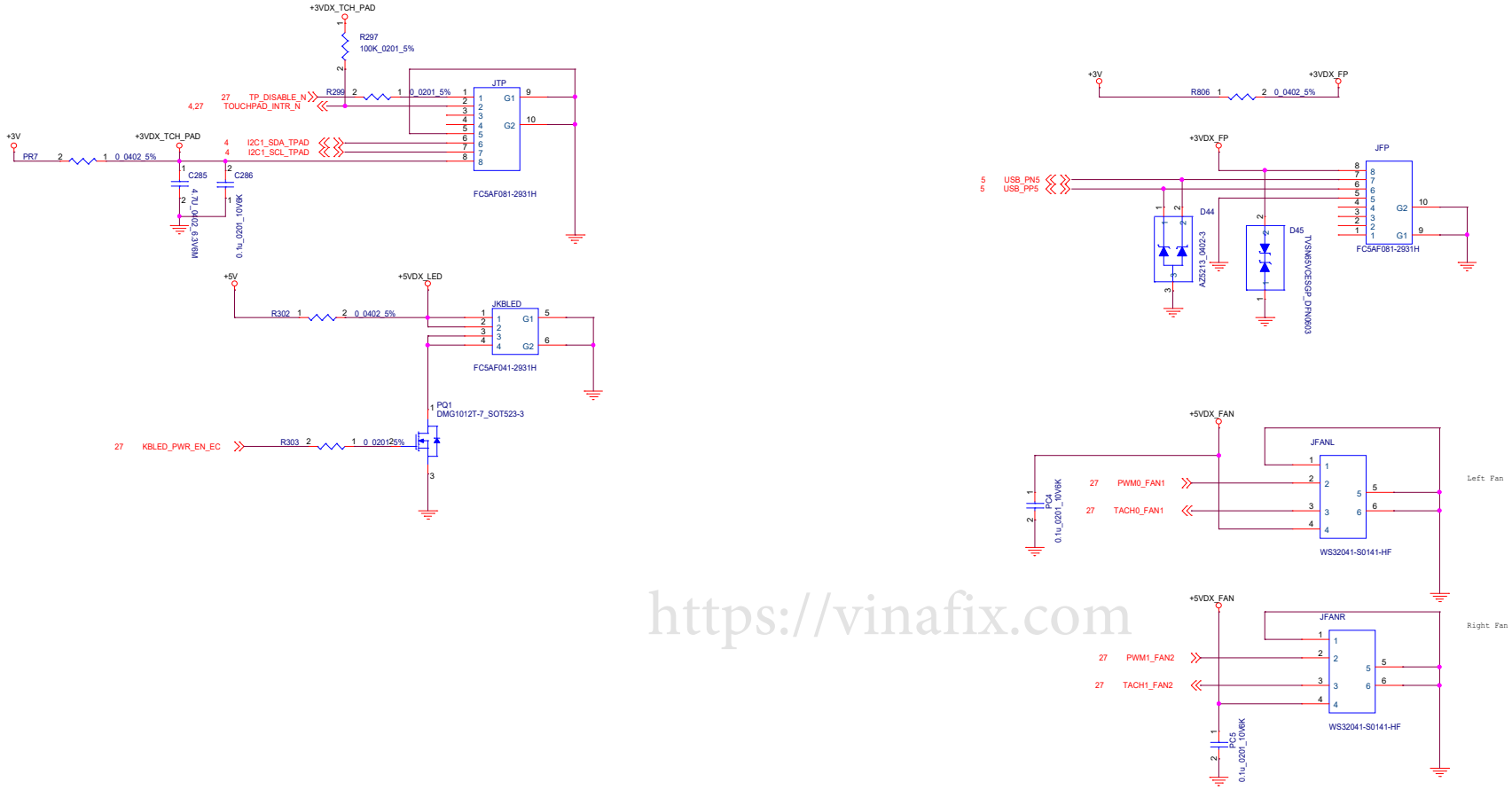
Title: EDP/CAMERA

Size: C | Document Number: YOGAC940 | Rev: V1.0

Date: Thursday, June 13, 2019 | Sheet 24 of 50





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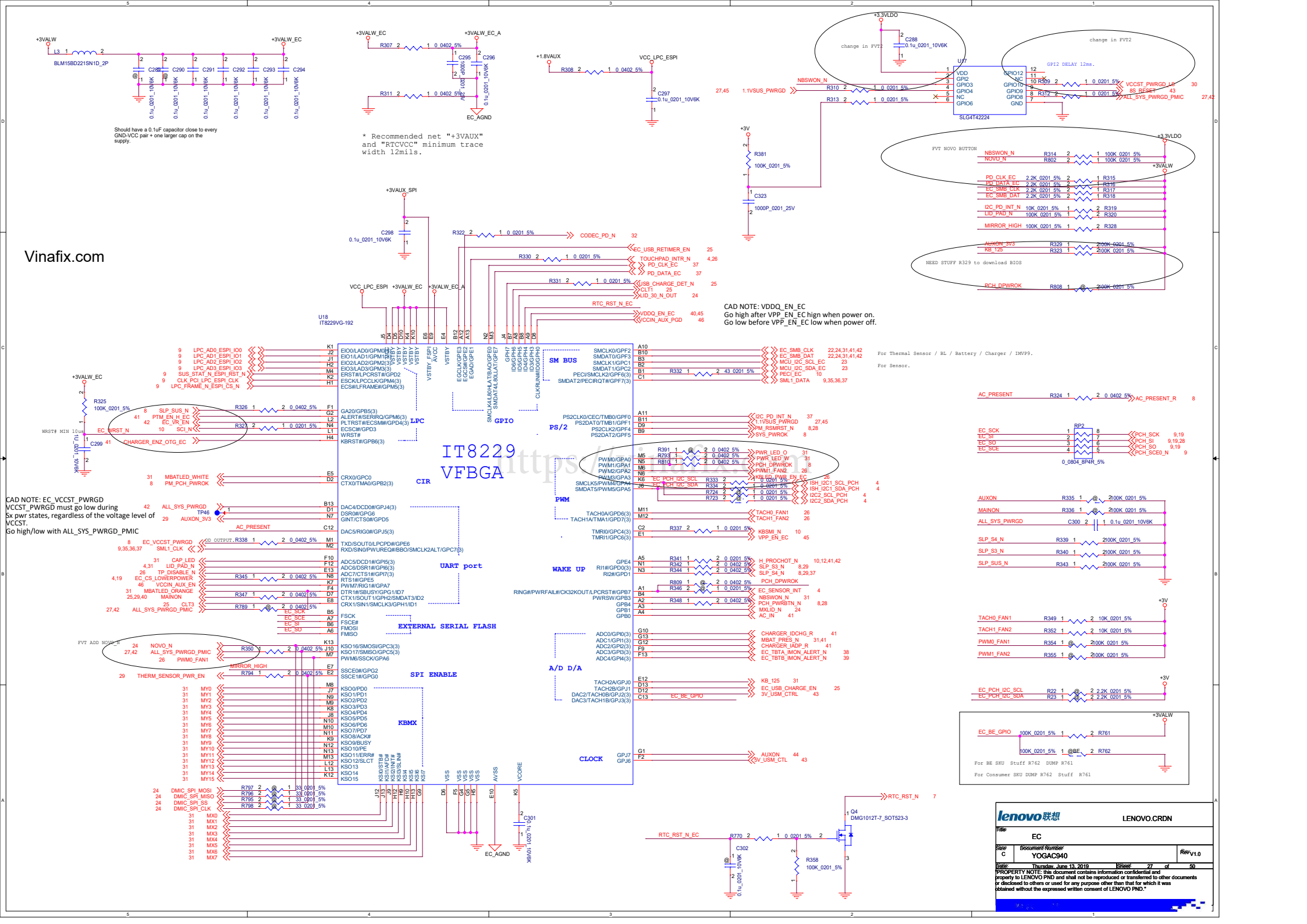
Title: TP/FP/KB LED

Size: C | Document Number: YOGAC940 | Rev: V1.0

Date: Thursday, June 13, 2019 | Sheet 26 of 50


Vinafix.com
IT8229
VFBGA
https://vinafix.com
U18
IT8229VG-192
SM BUS
GPIO
PS/2
LPC
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
A/D D/A
SPI ENABLE
KBMX
CLOCK
Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.
* Recommended net "+3VAUX" and "RTCVCC" minimum trace width 12mils.
CAD NOTE: VDDQ_EN_EC
Go high after VPP_EN_EC hign when power on.
Go low before VPP_EN_EC low when power off.
CAD NOTE: EC_VCCST_PWRGD
VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST.
Go high/low with ALL_SYS_PWRGD_PMIC
change in FVT2
GPI2 DELAY 12ms.
FVT NOVO BUTTON
NEED STUFF R329 to download BIOS
For Thermal Sensor / BL / Battery / Charger / IMVP9.
For Sensor.
For BE SKU Stuff R762 DUMP R761
For Consumer SKU DUMP R762 Stuff R761
SLG4T42224
Q4 DMG1012T-7_SOT523-3
LENOVO.CRDN
EC
YOGAC940
V1.0
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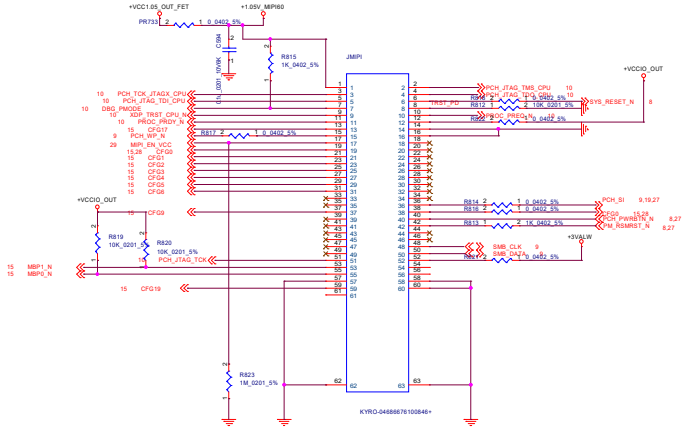

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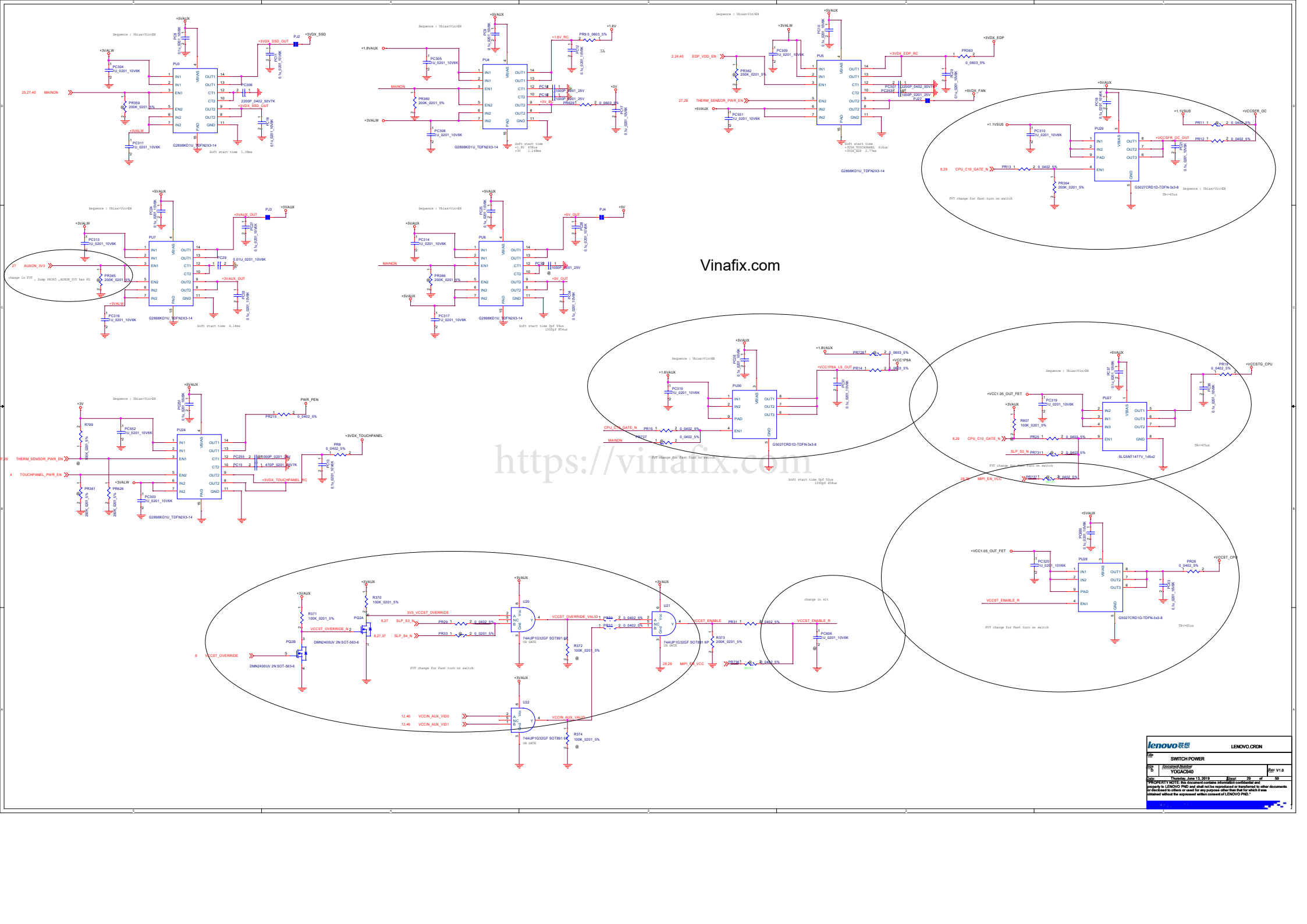
Title: MIPI60

Size: D | Document Number: YOGA C940 | Rev: V1.0

Date: Thursday, June 13, 2019 | Sheet 26 of 50


Vinafix.com
https://vinafix.com
SWITCH POWER
LENOVO.CRDN
YOGAC940
Thursday, June 13, 2019
29
50
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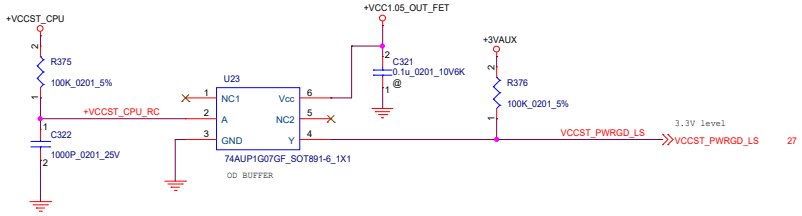
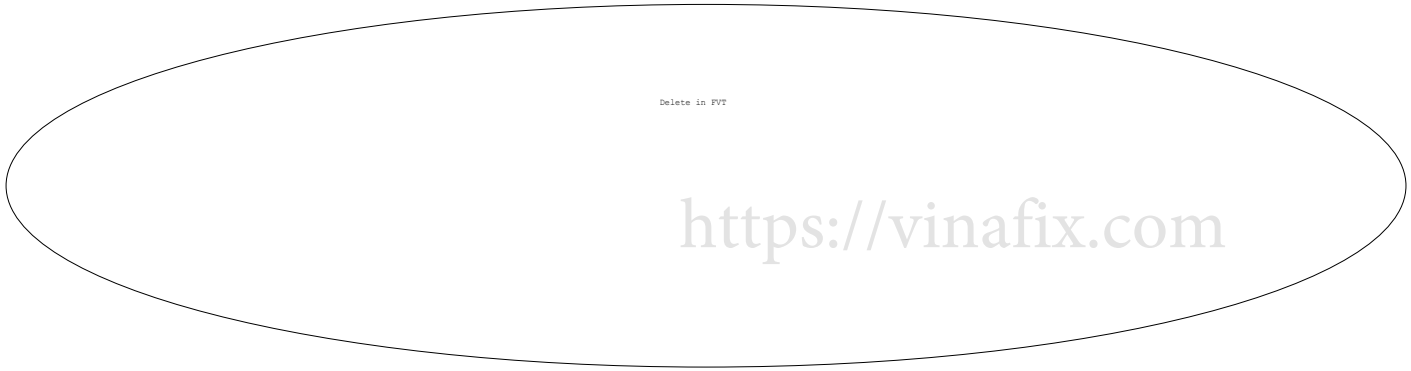
VCCST_PWRGD_LS



ALL_SYS_PWRGD_PMIC



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Title: PWRGD CONTROL

Size: C | Document Number: YOGAC940 | Rev: V1.0

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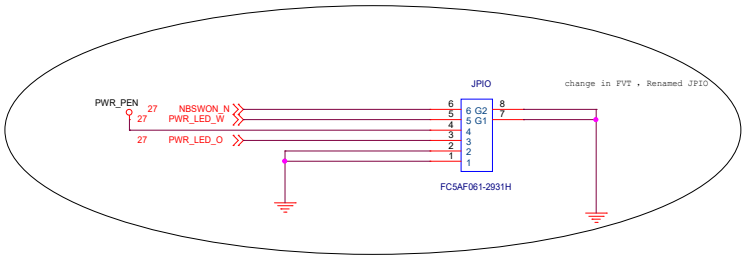

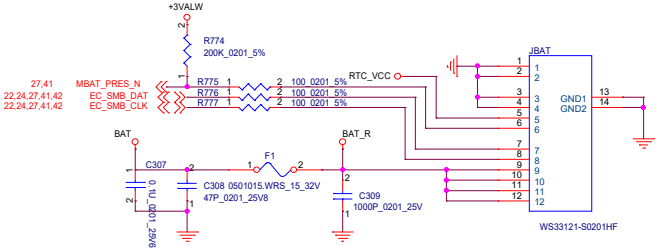

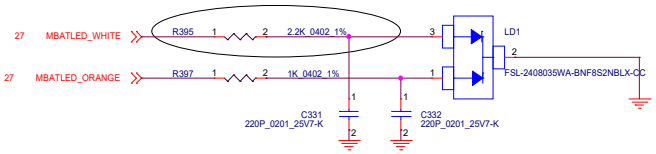

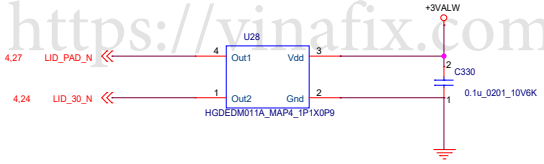

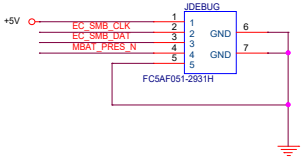

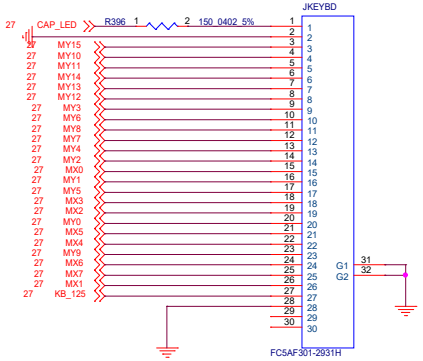

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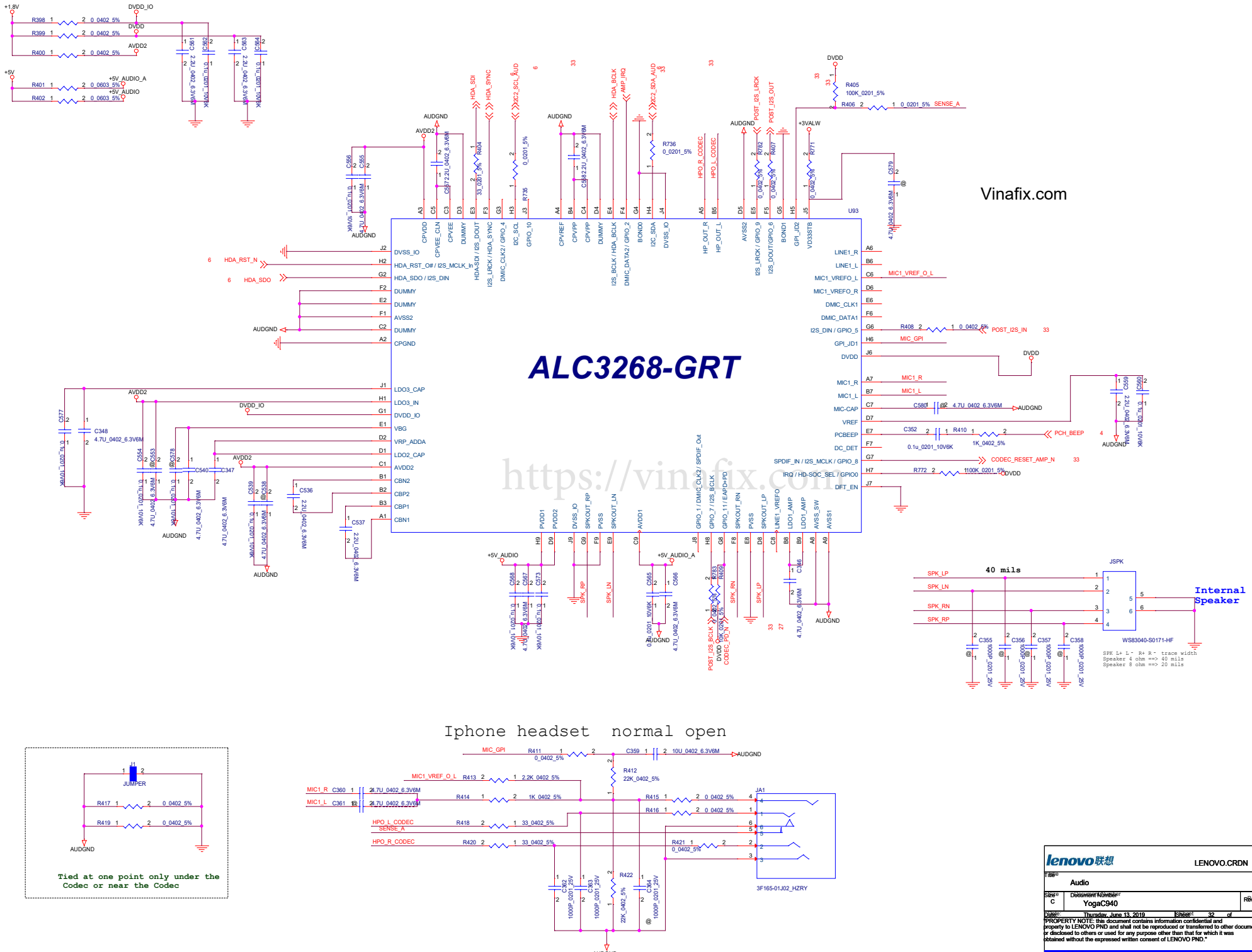
Title: CONNECTOR

Size: C | Document Number: YOGAC940 | Rev: V1.0

Date: Thursday, June 13, 2019 | Sheet 31 of 50


ALC3268-GRT
Vinafix.com
https://vinafix.com
Iphone headset normal open
Internal Speaker
Tied at one point only under the Codec or near the Codec
LENOVO.CRDN
Audio
YogaC940
V1.0
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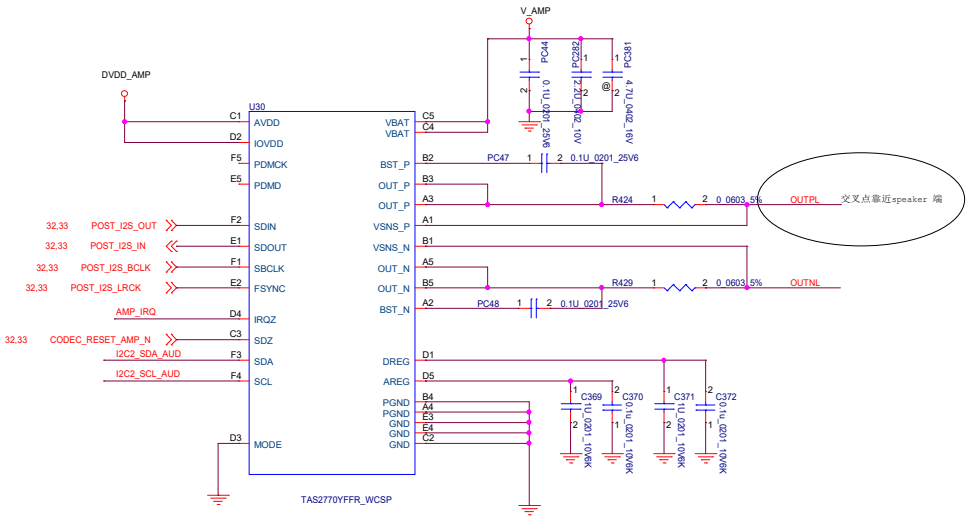
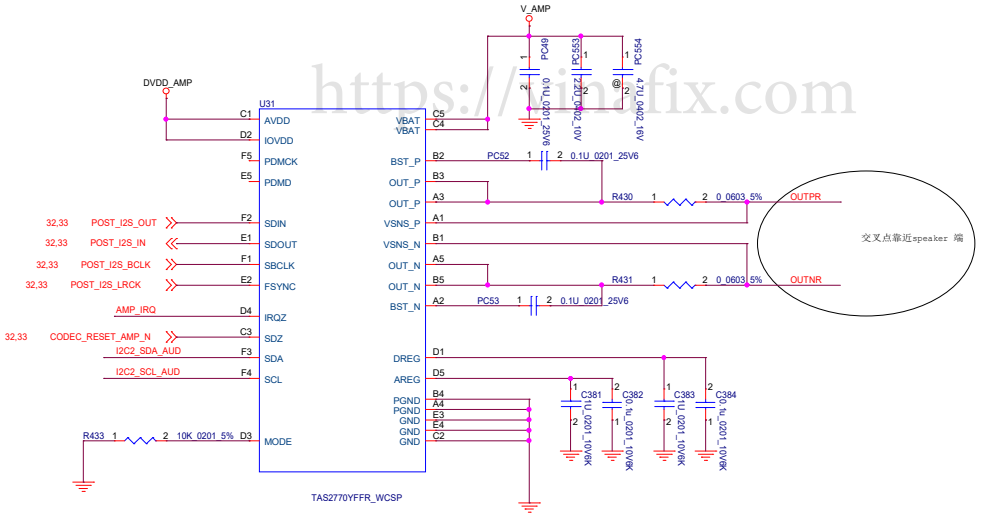
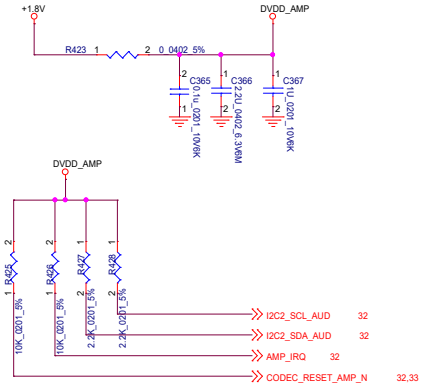
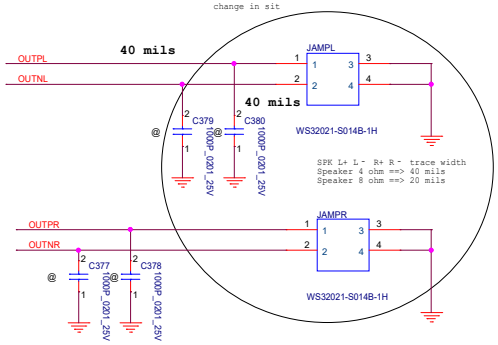


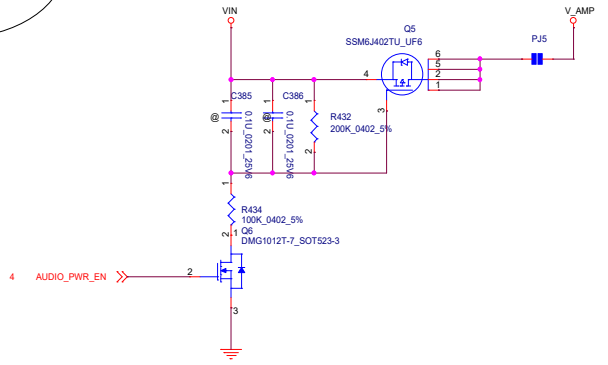
ADDRESS 0x82



ADDRESS 0x8C







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Title: SMART-AMP

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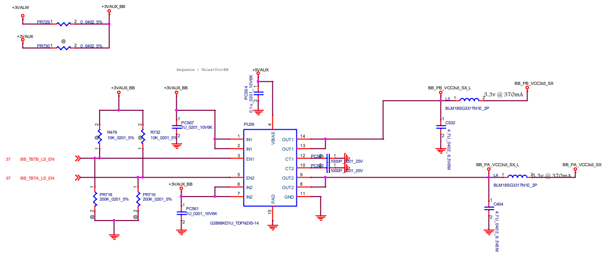

BB_PA_VCC3v3_SX Tolerance (+ 5%/-7.5%):
Burnside Bridge power pins which connected to BB_PA_VCC3v3_SX should be 3.465v maximum and 3.07v minimum for normal operation.
BB_PA_VCC3v3_SX ripple: 40mVp-p

BB_PB_VCC3v3_SX Tolerance (+ 5%/-7.5%):
Burnside Bridge power pins which connected to BB_PB_VCC3v3_SX should be 3.465v maximum and 3.07v minimum for normal operation.
BB_PB_VCC3v3_SX ripple: 40mVp-p

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Title	BBPOWSWITCH		
Size E	Document Number YOGAC940		Rev V1.0
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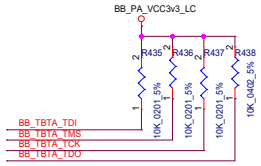
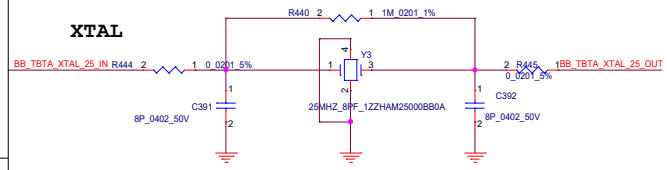
Burnside Bridge for TBT Port A

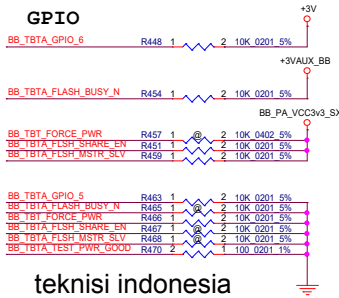
JTAG



XTAL



GPIO



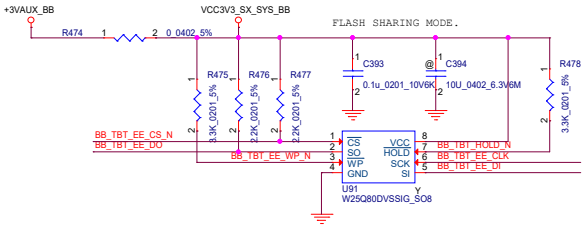
BB_FORCE_PWR:
Connect to EC/PCH for FW update
'0' - by default
'1' - for debug only

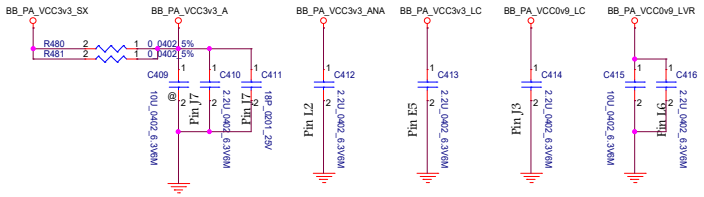
FLASH_BUSY#:
If Flash sharing is being used, PU should be used.
If Flash sharing isn't being used, PD should be used.

FLSH_SHARE_EN:
'0' - Flash isn't shared. 1 Flash per Re-timer
'1' - Flash is shared between 2 Re-timers

FLSH_MSTR_SLV:
'0' - Set Re-timer to be Slave on shared flash SPI I/F.
'1' - Set Re-timer to be Master on shared flash SPI I/F
If shared, BB1 PU as master, BB2 PD as slave.

ROM



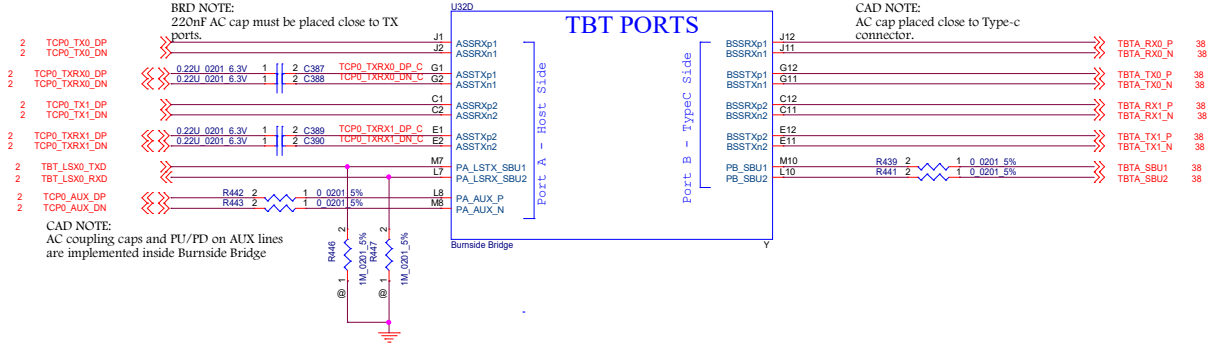


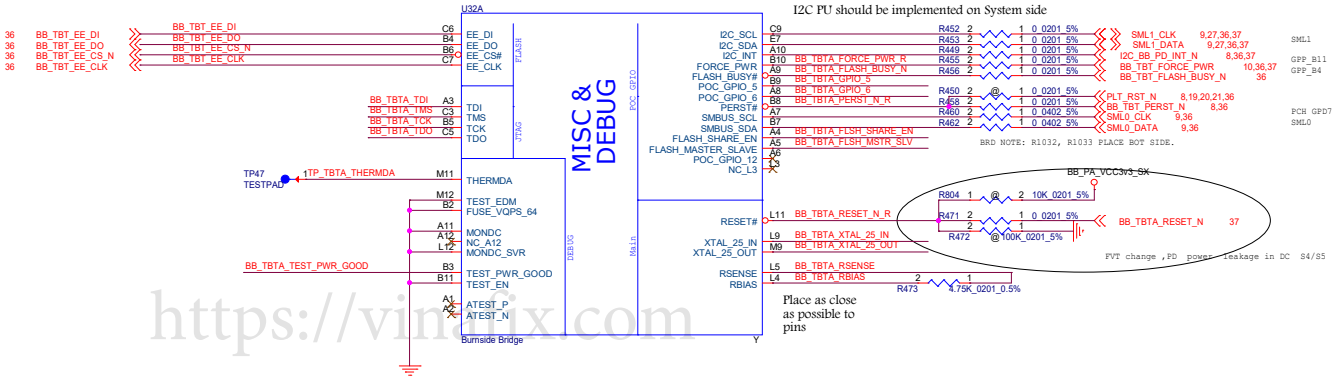
TBT PORTS

BRD NOTE:
220nF AC cap must be placed close to TX ports.

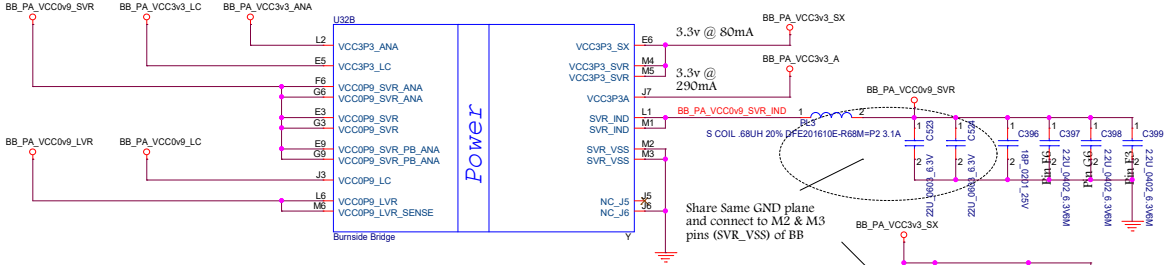
CAD NOTE:
AC coupling caps and PU/PD on AUX lines are implemented inside Burnside Bridge

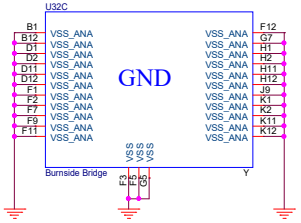
CAD NOTE:
AC cap placed close to Type-c connector.





I2C PU should be implemented on System side





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Title	TBT_BB_PORT A
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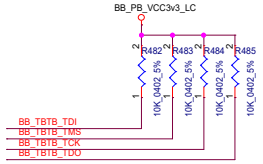
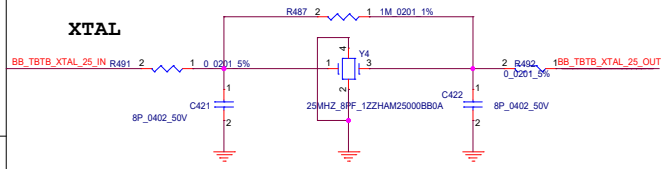
Burnside Bridge for TBT Port B

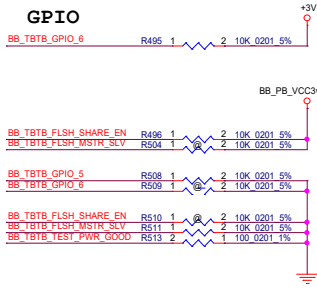
JTAG



XTAL



GPIO

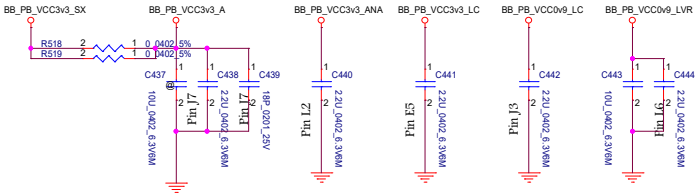


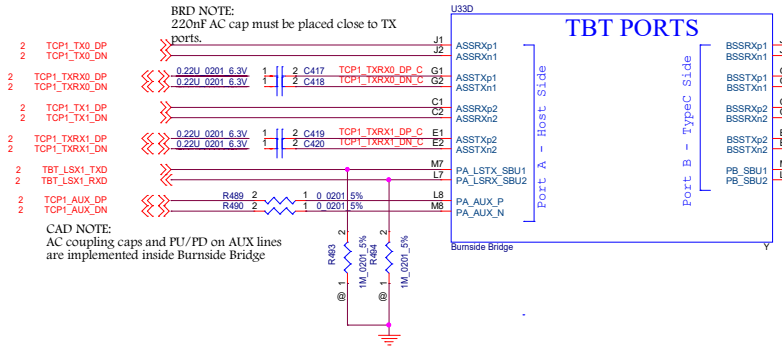
BB_FORCE_PWR:
Connect to EC/PCH for FW update
'0' - by default
'1' - for debug only

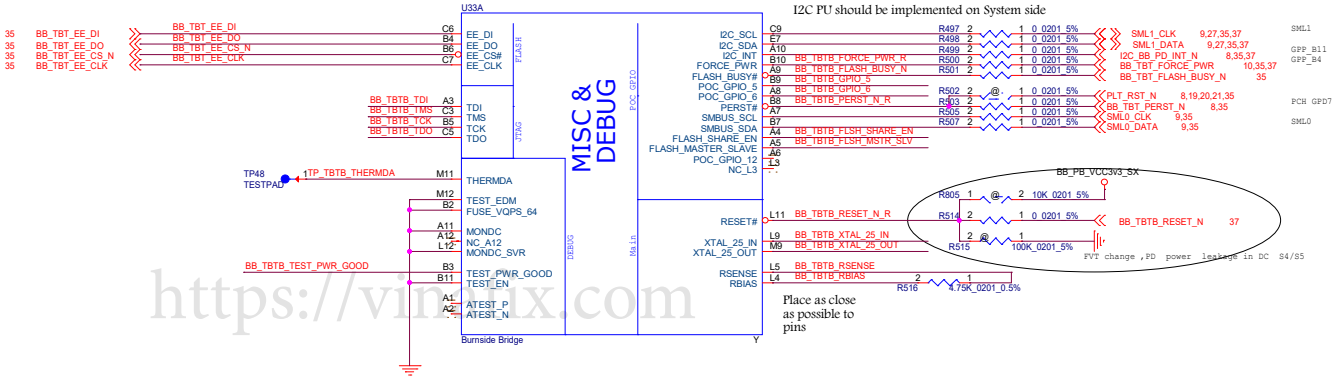
FLASH_BUSY#:
If Flash sharing is being used, PU should be used.
If Flash sharing isn't being used, PD should be used.
FLSH_SHARE_EN:
'0' - Flash isn't shared. 1 Flash per Re-timer
'1' - Flash is shared between 2 Re-timers

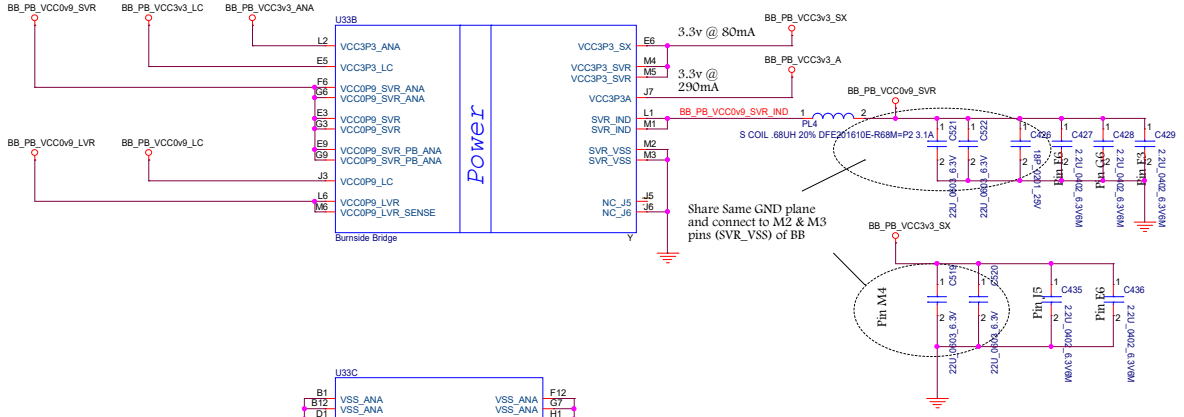
FLSH_MSTR_SLV:
'0' - Set Re-timer to be Slave on shared flash SPI I/F.
'1' - Set Re-timer to be Master on shared flash SPI I/F
If shared, BB1 PU as master, BB2 PD as slave.

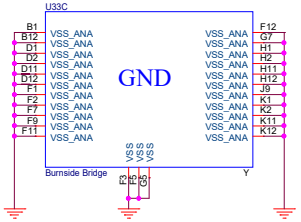
ROM











lenovo联想	LENOVO.CRDN	
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TABLE I2C Addressing

I2C1(to EC)	TBTA PORT	0x23
	TBTB PORT	0x27
I2C2(to AR)	TBTA PORT	0x23
	TBTB PORT	0x27

NEAR PIN11&12 NEAR PIN1&2 NEAR PIN46 NEAR PIN25

PLACE NEAR U192

ROM

Change in SIV FW load from EC, Stuff R542 R543 R544 R551

R551 NC if design to boot PD controller from SPI
If PD boot load was from EC, mount R551 and NC R548

Title	TBT_PD_TPS65988
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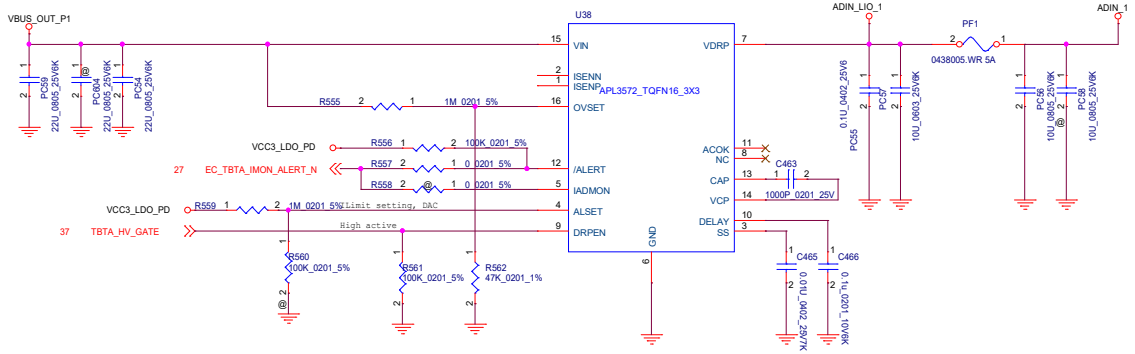
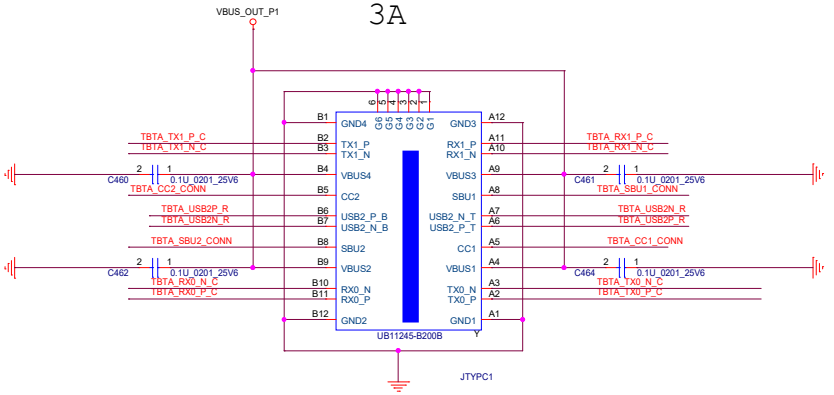
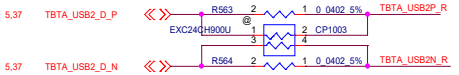
TBT A PORT VBUS SWITCH

Over Voltage Lock Out Trip Threshold = 1* (1 + R3400 / R3401)

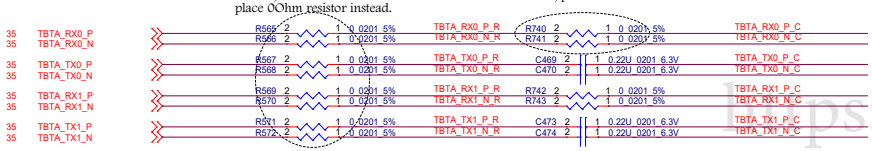




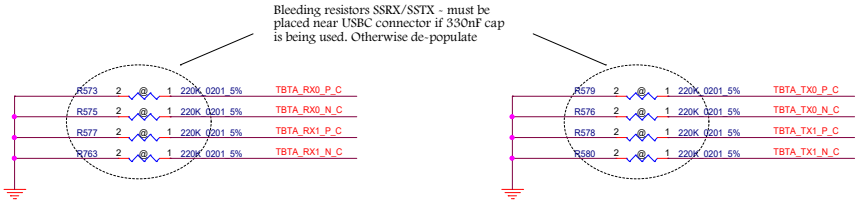


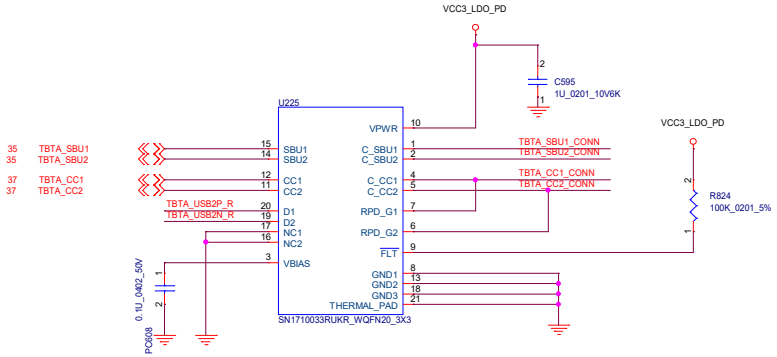
Reduce current surge in a VBUS-short event. If not needed, place 0Ohm resistor instead.

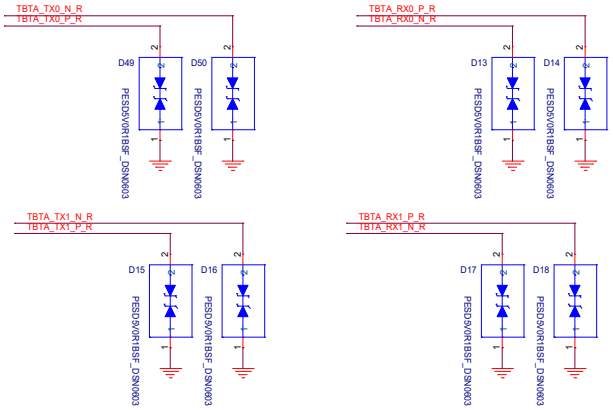
AC coupling is recommended for VBUS-short protection on SSRX lines. If not needed, place 0Ohm resistor instead.



Bleeding resistors SSRX/SSTX - must be placed near USBC connector if 330nF cap is being used. Otherwise de-populate







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Title: TYPEC_PORTA

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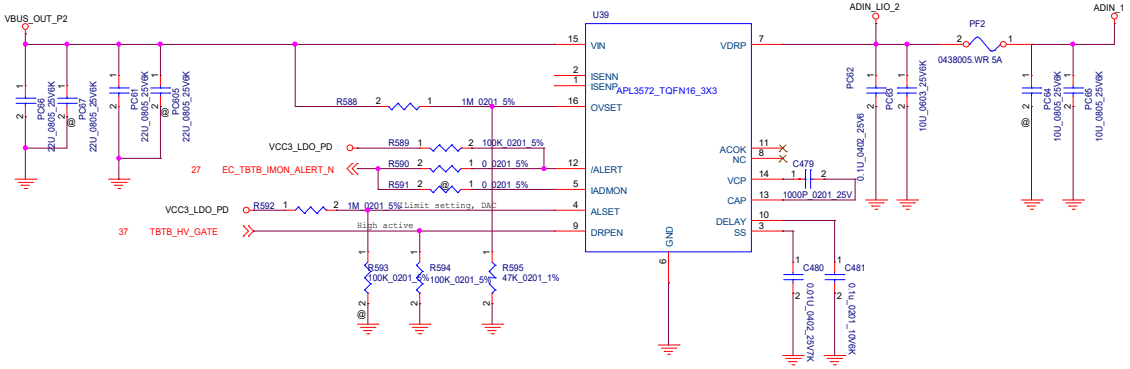
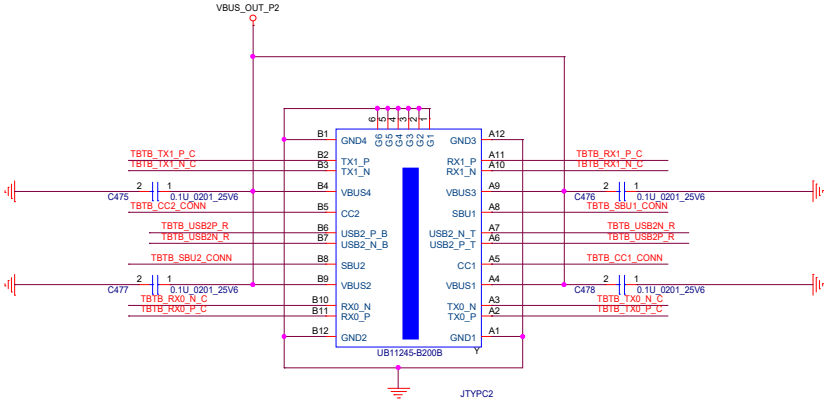
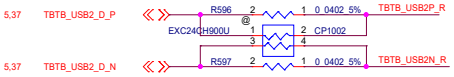
TBT B PORT VBUS SWITCH

Over Voltage Lock Out Trip Threshold = 1* (1 + R3397 / R485)

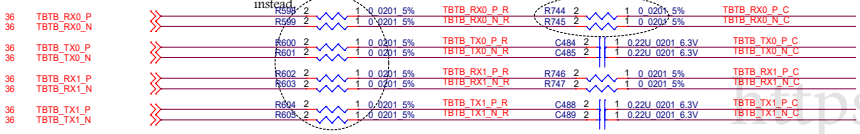




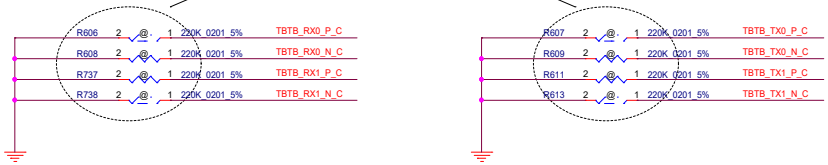


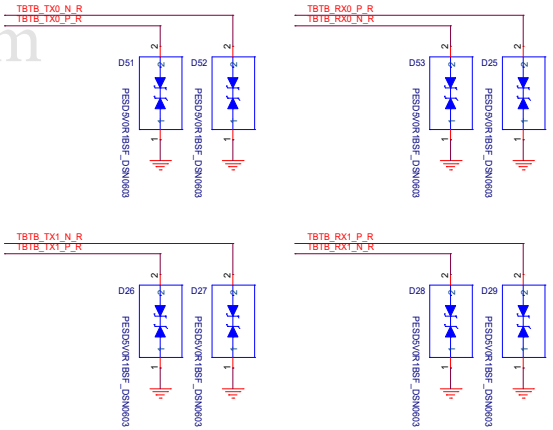
Reduce current surge in a VBUS-short event. If not needed, place 0Ohm resistor instead.

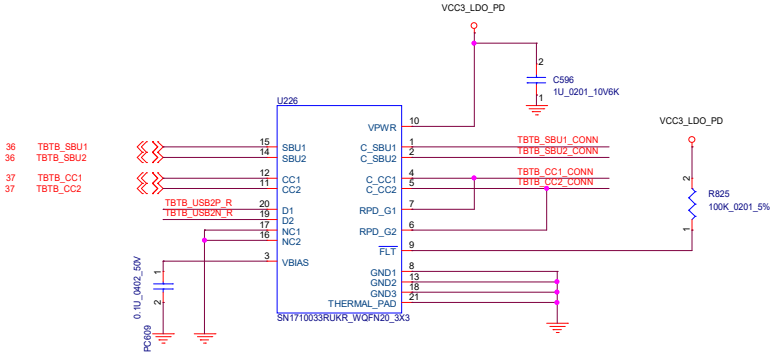
AC coupling is recommended for VBUS-short protection on SSRX lines. If not needed, place 0Ohm resistor instead.



Bleeding resistors SSRX/SSTX - must be placed near USBC connector if 330nF cap is being used. Otherwise de-populate







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Title	TYPEC_PORTB
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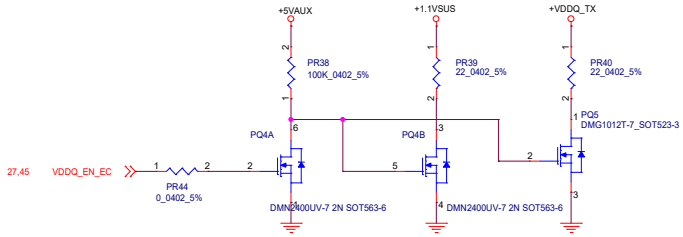

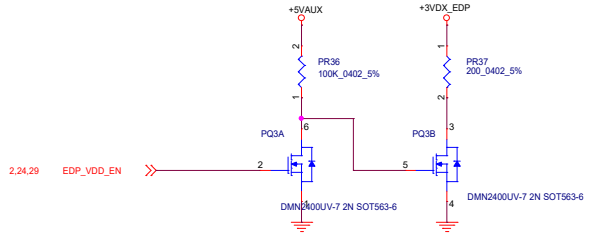

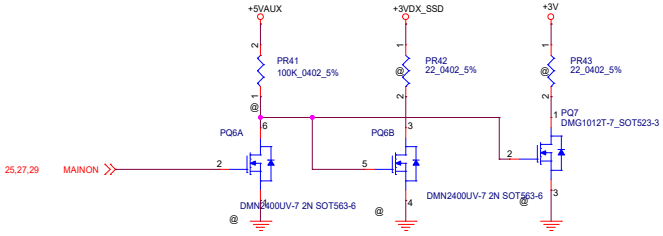

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Title: DISCHARGE

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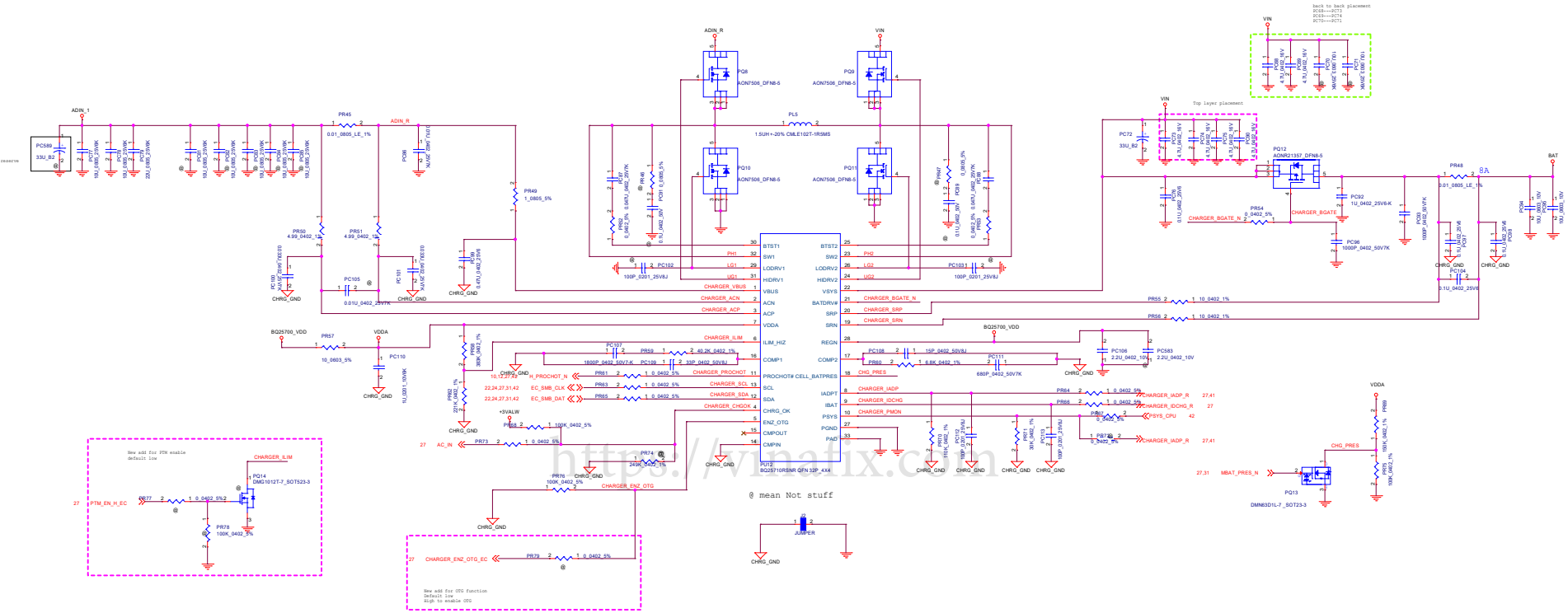

Title	NVDC CHARGER
Size	D
Document Number	YOGAC940
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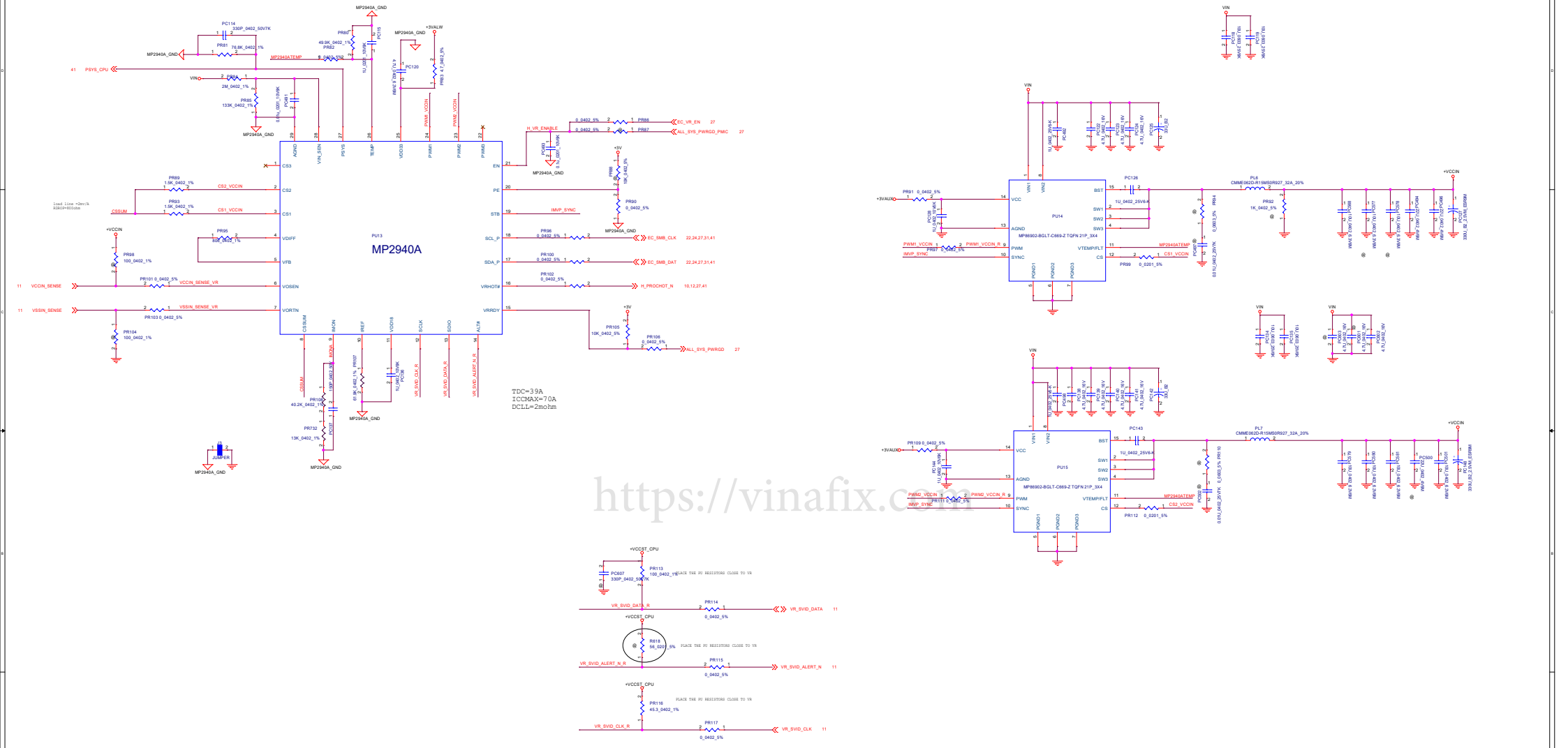

Title	IMVP9
Size	D
Document Number	YOGAC940
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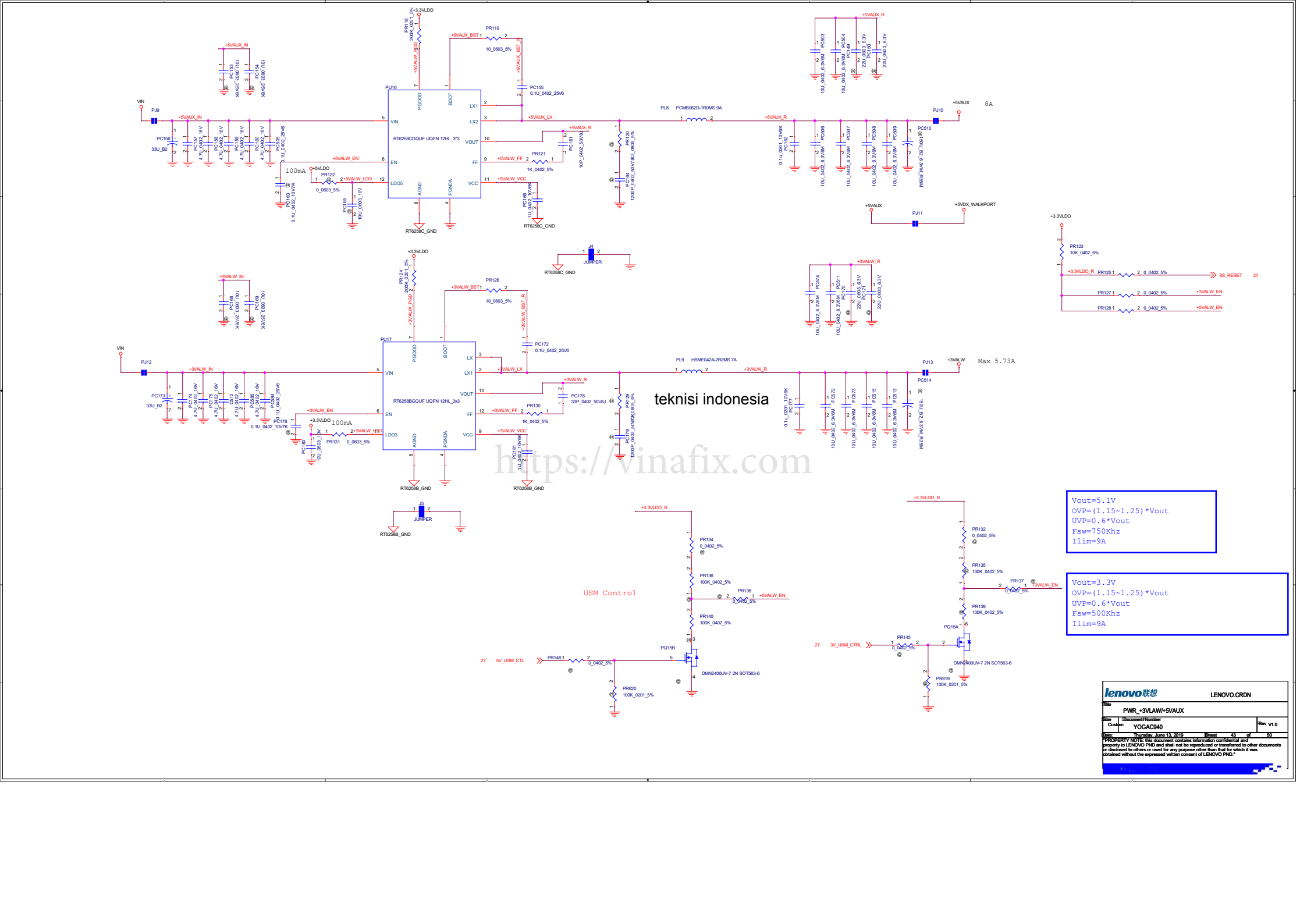
RT6258CGQUF UQFN 12HL_3*3
RT6258BGQUF UQFN 12HL_3x3
PU16
PU17
PJ9
PJ10
PJ11
PJ12
PJ13
PL8 PCMB062D-1R0MS 9A
PL9 HBME042A-2R2MS 7A
+5VAUX 8A
+3VALW Max 5.73A
+5VALDX
+5VDX_WALKPORT
+3.3VLDO
+5VAUX_IN
+3VALW_IN
+5VAUX_R
+3VALW_R
+5VAUX_LX
+3VALW_LX
+5VAUX_BST_R
+3VALW_BST_R
+5VAUX_PGD
+3VALW_PGD
+5VALW_EN
+3VALW_EN
+5VALW_FF
+3VALW_FF
+5VALW_VCC
+3VALW_VCC
+5VALW_LDO
+3VALW_LDO
100mA
RT6258C_GND
RT6258B_GND
J4 JUMPER
J5 JUMPER
USM Control
5V_USM_CTL
3V_USM_CTRL
DMN2400UV-7 2N SOT563-6
8S_RESET
teknisi indonesia
https://Vinafix.com
Vout=5.1V
OVP=(1.15~1.25)*Vout
UVP=0.6*Vout
Fsw=750Khz
Ilim=9A
Vout=3.3V
OVP=(1.15~1.25)*Vout
UVP=0.6*Vout
Fsw=500Khz
Ilim=9A
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LENOVO.CRDN
PWR_+3VLAW/+5VAUX
Custom
YOGAC940
V1.0
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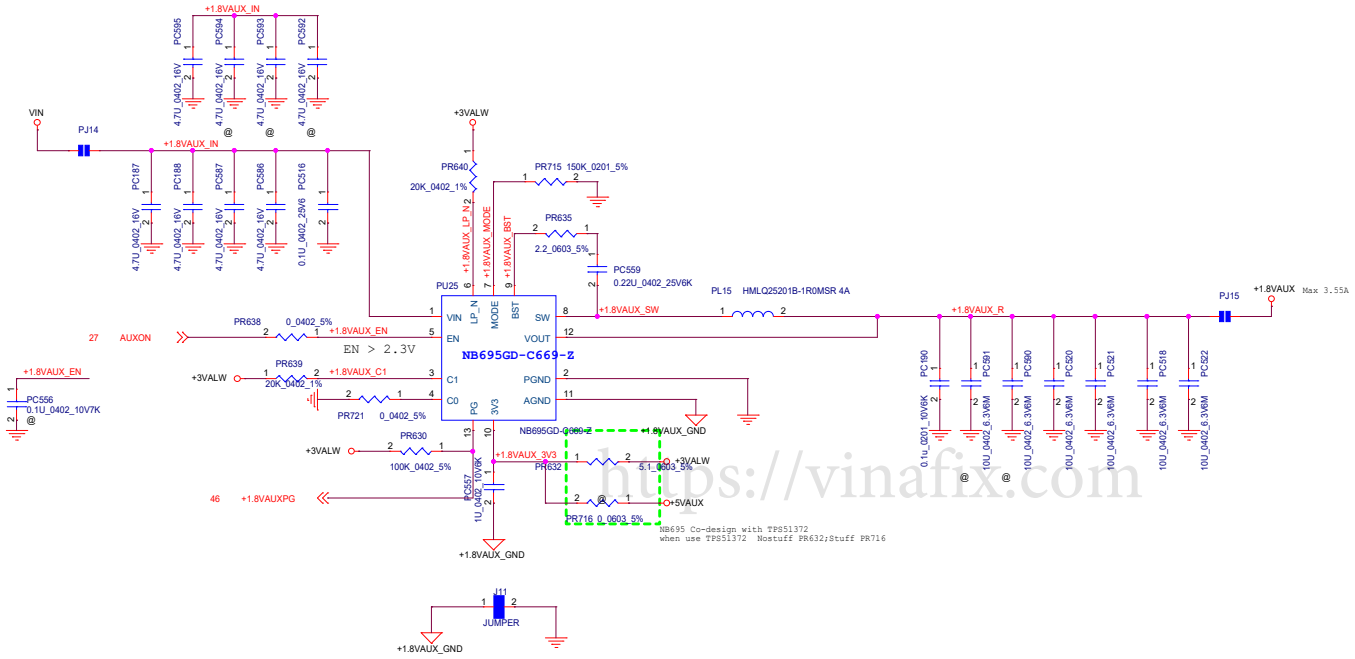

LP#	C1	C0	Vout(V)
1	1	0	1.8V

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Title: PWR_+1.8VALW

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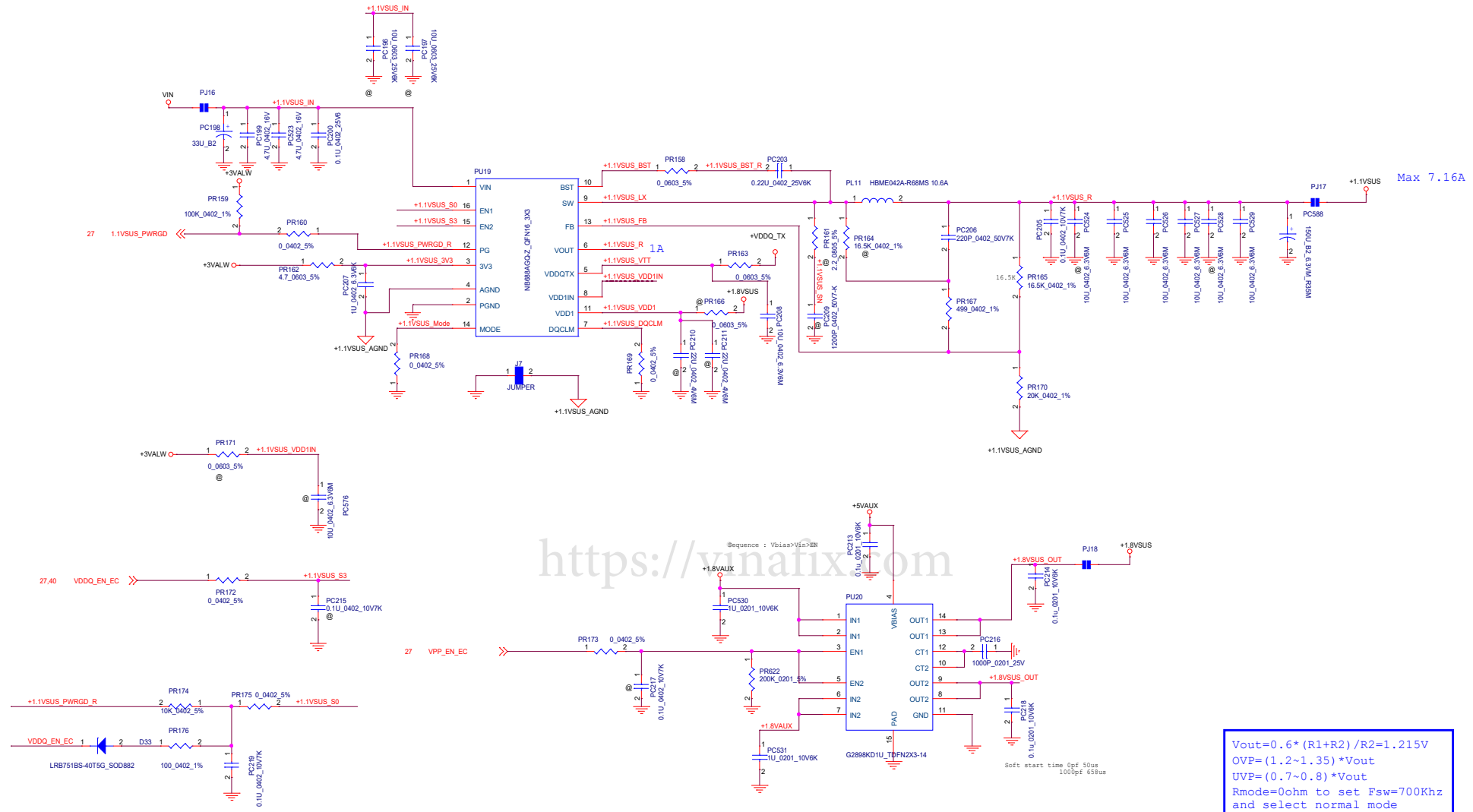

confirm with EE 0.6V enable

Vout=0.6*(R1+R2)/R2=1.215V
OVP=(1.2~1.35)*Vout
UVP=(0.7~0.8)*Vout
Rmode=0ohm to set Fsw=700Khz
and select normal mode

STATE	EN1	EN2	+1.1VSUS	+1.8VSUS	+0.6V
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

Vinafix.com

Title	+1.1VSUS/+1.8VSUS
Size	C
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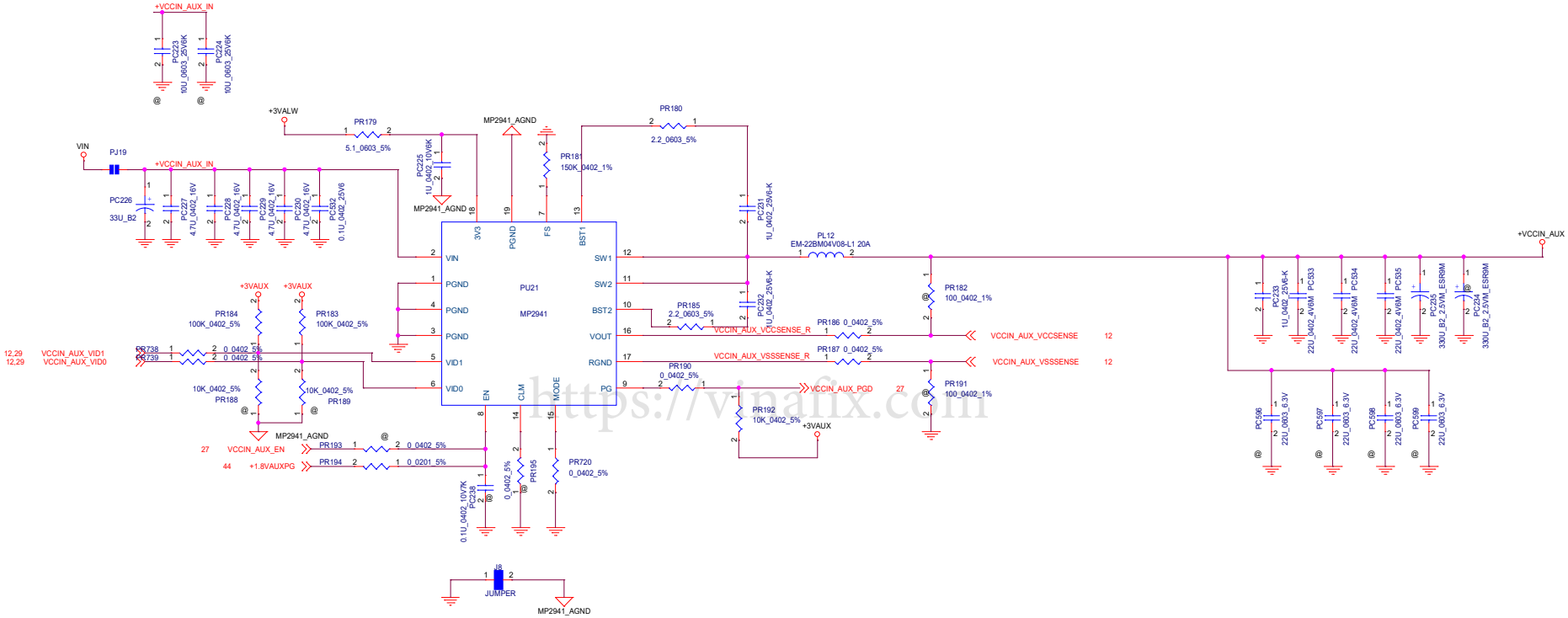

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Title: VCCINAUX		
Size: C	Document Number: YOGAC940	Rev: V1.0
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Title: BLANK

Size	Document Number	Rev
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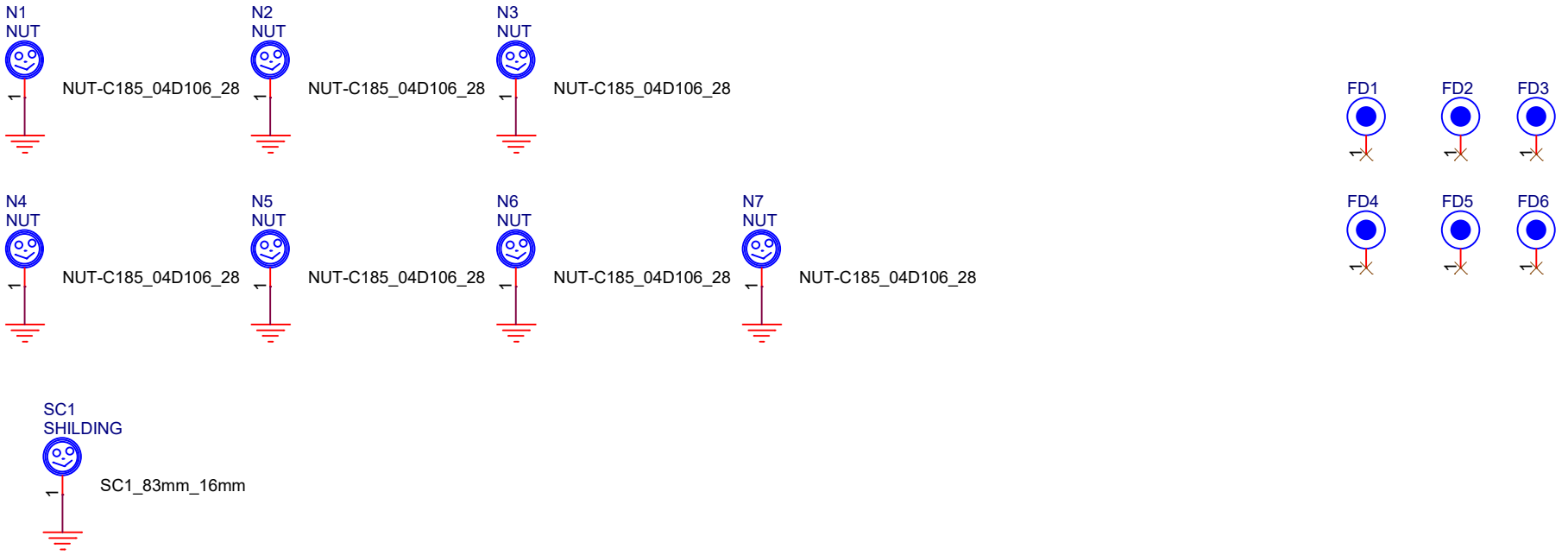

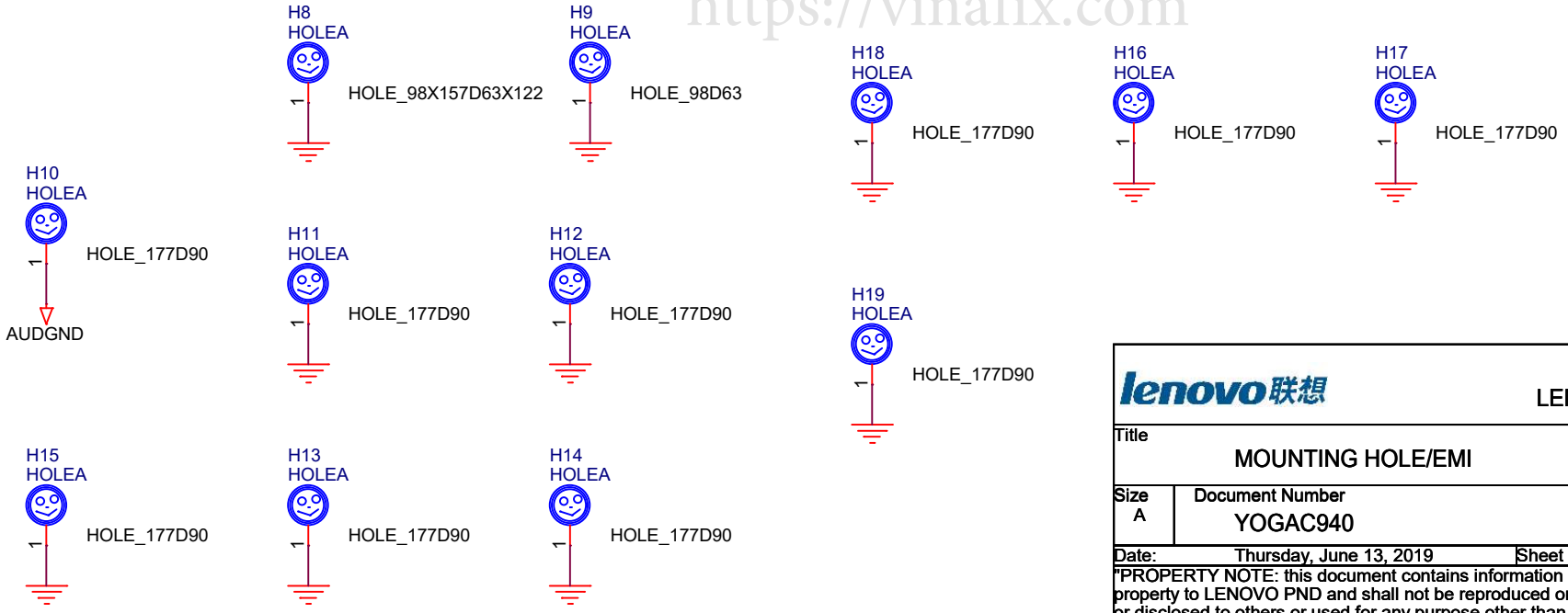

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Title

MOUNTING HOLE/EMI

Size	Document Number	Rev
A	YOGAC940	V1.0

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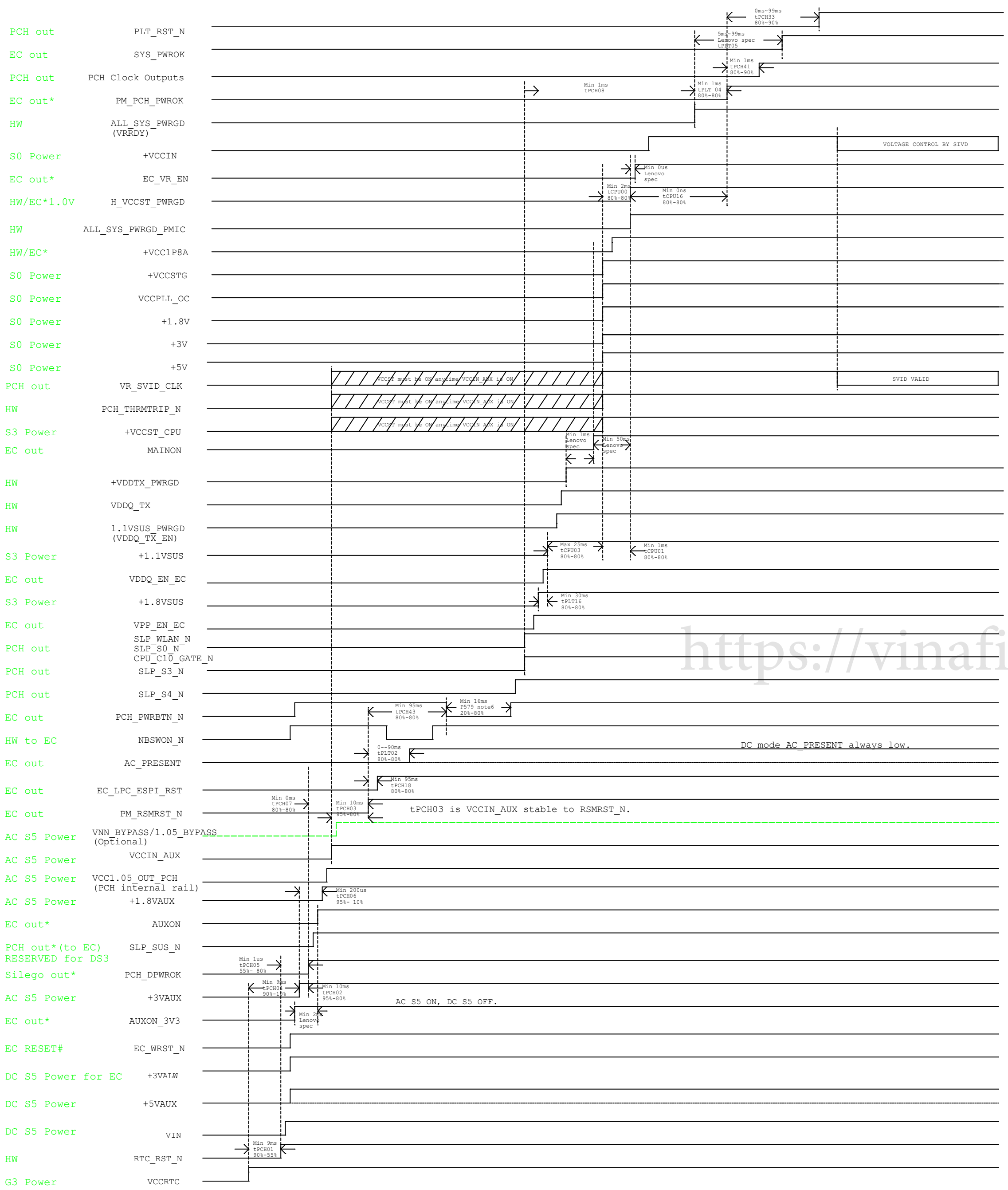
G3 AC/DC mode S5/S4 to S0 (Non Deep Sx)



G3 AC/DC mode S5/S4 to S0 (Non Deep Sx platform)

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Title	ICL Power Sequence
Size	Custom
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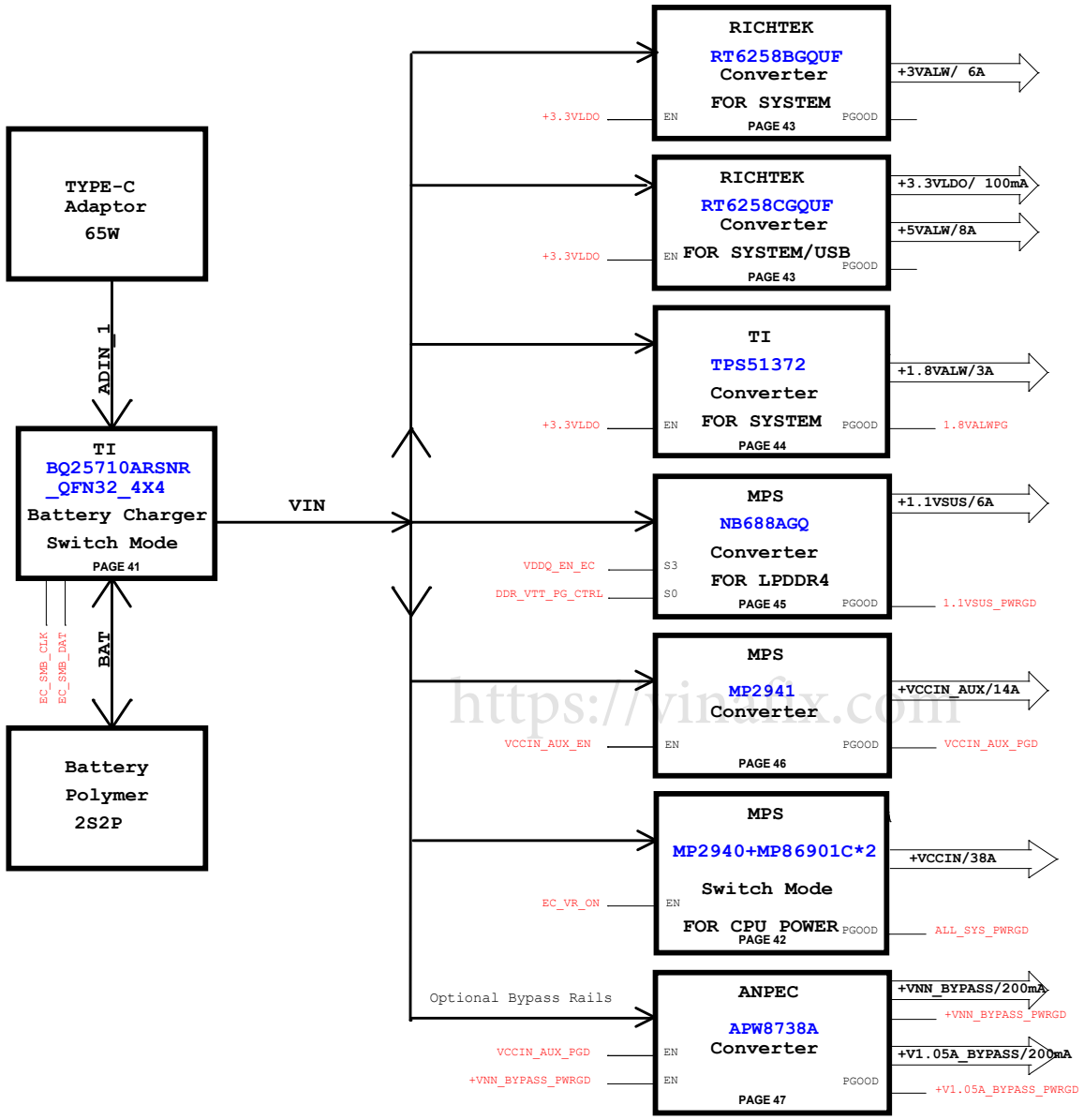

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Title: PWR-Power Diagram

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