Compal Confidential

DIUYA/YB/SA/SB/SD (KBL-R)

DIS M/B Schematics Document

Intel KabyLake U/KabyLake R Processor with DDR4

N16S-GTR(940) (23x23mm)
N16V-GMR1(920) (23x23mm)

2017-06-05

LA-E541P

REV：2.A

FAB: JB501

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Issued Date	2017/06/05	Deciphered Date	2018/06/05

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Title	*Cover Page*	
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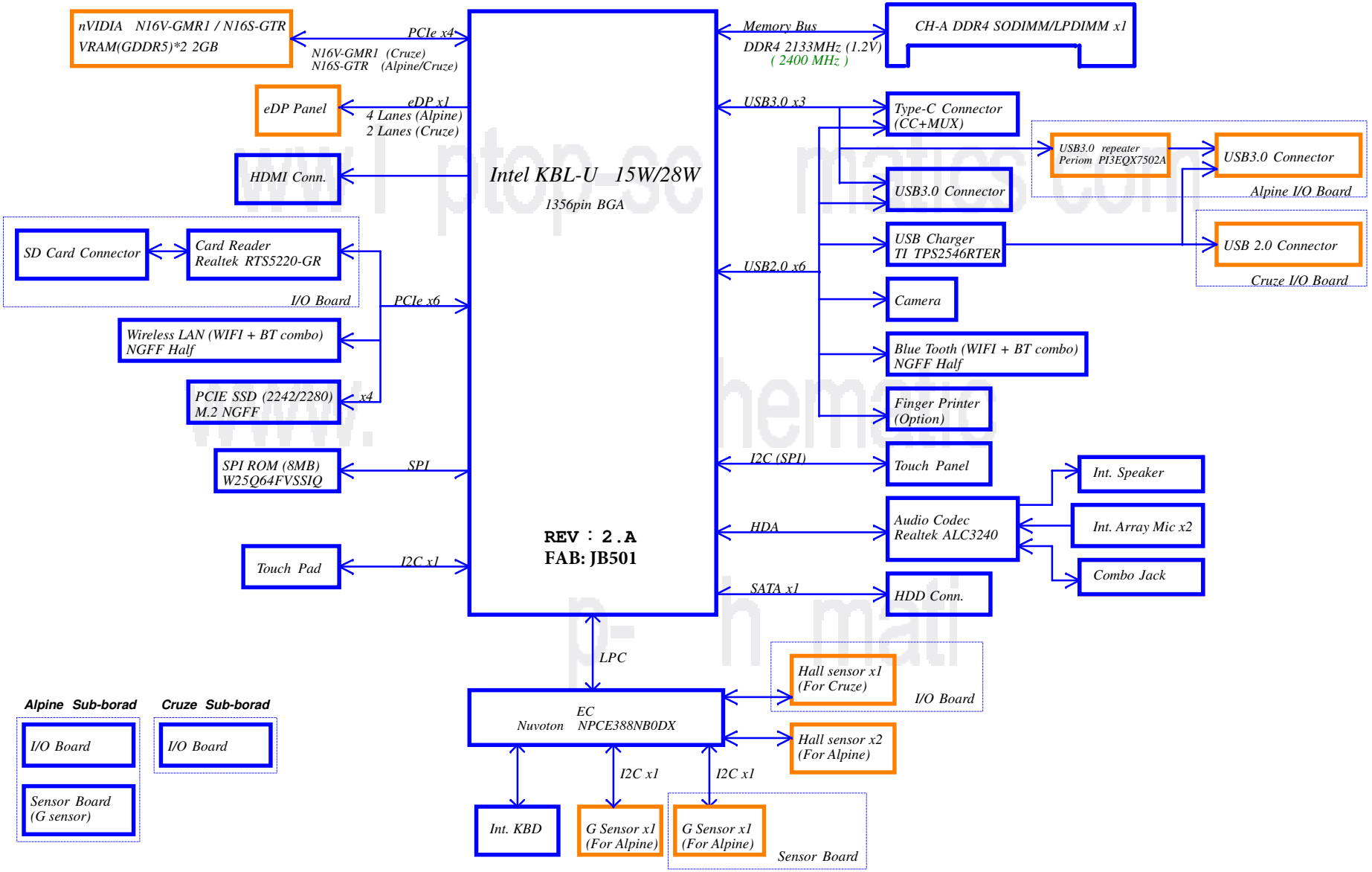

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Voltage Rails

power plane / State	B+	+5VALW +3VALW	+1.2V	+5VS +3VS +1.35VS +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.6VS +1.0VALW
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM Structure Table

Item	BOM Structure
For DIS	DIS@
For UMA	UMA@
For Touch Panel with SPI	TS_SPI@
For Touch Panel with I2C	~~TS_I2C@~~
For Keyboard backlight	KBL@
No Keyboard backlight	NOKBL@
For Samsung VRAM	S2G@
For Micron VRAM	M2G@
For Hynix VRAM	H2G@
For UHD Panel	UHD@
For Finger Printer	~~FP@~~
For SSD	SSD@
For EMI	EMI@
For ESD	ESD@
For RF	RF@
No EMI	@EMI@
No ESD	@ESD@
No RF	@RF@
Connector	ME@
For VARM X76	~~X76@~~
For Test Point	TP@
For Debug	@DCI@
For S series only	S_AL@
For S IMR series only	S_IMR@
For YOGA series only	YOGA@
For CPU Type	i7_7500U_R1@
	i5_7200U_R1@
	i3_7100U_R1@
	i7_7500U_R3@
	i5_7200U_R3@
	i3_7100U_R3@
	pt_4415U_R1@
	pt_4415U_R3@
	i3_6006U_R3@

Item	BOM Structure
For KBL U22 CPU	U22@
For KBL U42 CPU	U42@
For GPU Type	N16S_R1@
	N16S_R3@
	N16V_R1@
	N16V_R3@
For EMI	U22_EMI@
	U42_EMI@
For Thermal sensor	EX_THM@
For ESD	FP_ESD@

USB 2.0 Port Table

Port	External USB Port
1	USB3 Type-C Port
2	USB2/3 Port (MB)
3	USB2/3 Port (IO/B)
4	USB3 Type-C Port
5	Camera
6	Finger Printer (Option)
7	NGFF WLAN+BT

USB 3.0 Port Table

Port	
1	USB3 Type-C (MUX)
2	USB2/3 Port (MB)
3	USB2/3 Port (IO/B)
4	
5	
6	

SATA Port Table

Port	
0	HDD
1	

PCIE Port Table

Lane	Port	
1	1	GPU
2		
3		
4		
5		Card Reader
6		NGFF WLAN+BT
7		
8		
9	3	SSD
10		
11		
12		

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x 16h

EC SM Bus2 address

Device	Address
NCT7718W	1001 100x 98h

EC SM Bus4 address

Device	Address
BMA250E	0001 100X 18h

PCH SM Bus address

Device	Address
DDR_JDIMM1 Touch Pad	1010 000x A0h

GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111x 9Eh

SMBUS Control Table

	SOURCE	VGA	BATT	CHARGER	NECP388	SODIMM	Thermal Sensor	DGPU			TP	PCH	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	NECP388 +3VALW	X	V +3VALW	V +19V_VIN	X	X	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	NECP388 +3VS	V +3VGS	X	X	V +3VS	X	V +3VS	X	X	X	X	V +3VS	X
SMB_EC_CK4 SMB_EC_DA4	NECP388 +3VALW	X	X	X	X	X	X	X	X	X	X	X	V +3VS
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW	X	X	X	X	V +3VS	X	X	X	X	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X	V +3VS	X	X	X
SML1CLK SML1DATA	PCH +3VALW	X	X	X	V +3VS	X	X	V +3VS	X	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

X4E

Yoga Series

ZZZ4 X4E_YA@ — X4E Y Series — X4EA5R38LA1
ZZZ3 X4E_YA_FP@ — X4E Y Series FP SKU — X4EA5R38LA2
ZZZ5 X4E_YB@ — X4E Y Series UHD SKU — X4EA5R38LE2
ZZZ6 X4E_YB_FP@ — X4E Y Series UHD&FP SKU — X4EA5R38LE1

S Series

ZZZ8 X4E_S@ — X4E S Series — X4EA5R38L01
ZZZ7 X4E_S_FP@ — X4E S Series FP SKU — X4EA5R38L02

Yoga Series (U42)

ZZZ X4E_U42_YA@ — X4E Y Series — X4EA5R38LL2
ZZZ X4E_U42_YA_FP@ — X4E Y Series FP SKU — X4EA5R38LL1
ZZZ1 X4E_U42_YB@ — X4E Y Series UHD SKU — X4EA5R38LO2
ZZZ2 X4E_U42_YB_FP@ — X4E Y Series UHD&FP SKU — X4EA5R38LO1

S Series (U42)

ZZZ X4E_U42_S@ — X4E S Series — X4EA5R38LR1
ZZZ X4E_U42_S_FP@ — X4E S Series FP SKU — X4EA5R38LR2

GDDR5 VRAM * 2

X7671138L03

UV6 S2G@ — K4G80325FB-HC03 — SA000094R20
UV7 S2G@ — K4G80325FB-HC03 — SA000094R20
RV65 SD034499180 4.99K_0402_1% S2G@

X7671138L02

UV6 M2G@ — MT51J256M32HF — SA000096K20
UV7 M2G@ — MT51J256M32HF — SA000096K20
RV65 SD034100280 10K_0402_1% M2G@

X7671138L01

UV6 H2G@ — H5GC8H24MJR-T2C — SA000092G10
UV7 H2G@ — H5GC8H24MJR-T2C — SA000092G10
RV65 SD034301280 30.1K_0402_1% H2G@

HDMI Logo

ZZZ 45@ — HDMI Logo — RO0000003HM

PCB part

ZZZ YOGA@ — PCB Y Series — DA80019S02A
ZZZ S_AL@ — PCB S Series — DA80019S12A
ZZZ S_IMR@ — PCB S Series — DA80019S12A

GPU part

UV1 N16S_R1@ — N16S-GTR-S-A2 BGA 595P — SA00009FP00
UV1 N16V_R1@ — N16V-GMR1-S-A2 BGA 595P — SA00009IT00
UV1 N16S_R3@ — N16S-GTR-S-A2 BGA 595P — SA00009FP30
UV1 N16V_R3@ — N16V-GMR1-S-A2 BGA 595P — SA00009IT30

CPU part

KBL U22 (= U22@)

UC1 i3_7100U_R1@ — QLYK H0 2.4G — SA0000A38A0
UC1 i5_7200U_R1@ — QLYJ H0 2.5G — SA0000A37A0
UC1 i7_7500U_R1@ — QLYH H0 2.7G — SA0000A3490
UC1 pt_4415U_R1@ — QLYM H0 2.3G — SA0000ADV00
UC1 i3_7100U_R3@ — SR343 H0 2.4G — SA0000A38B0
UC1 i5_7200U_R3@ — SR342 H0 2.5G — SA0000A37B0
UC1 i7_7500U_R3@ — SR341 H0 2.7G — SA0000A34A0
UC1 pt_4415U_R3@ — SR348 H0 2.3G — SA0000ADV20

SKL U22 (= U22@)

UC1 i3_6006U_R3@ — SR2JG K1 i3-6006U 2.0G C38! — SA0000ACN10

KBL U42 (= U42@)

UC1 i5_QNEF_R1@ — QNEF Y0 1.6G FCBGA — SA0000AWB00
UC1 i7_QNBF_R1@ — QNBF Y0 1.8G FCBGA — SA0000AWC00
UC1 i5_QNEF_R3@ — QNEF Y0 1.6G FCBGA — SA0000AWB50
UC1 i7_QNBF_R3@ — QNBF Y0 1.8G FCBGA — SA0000AWC50

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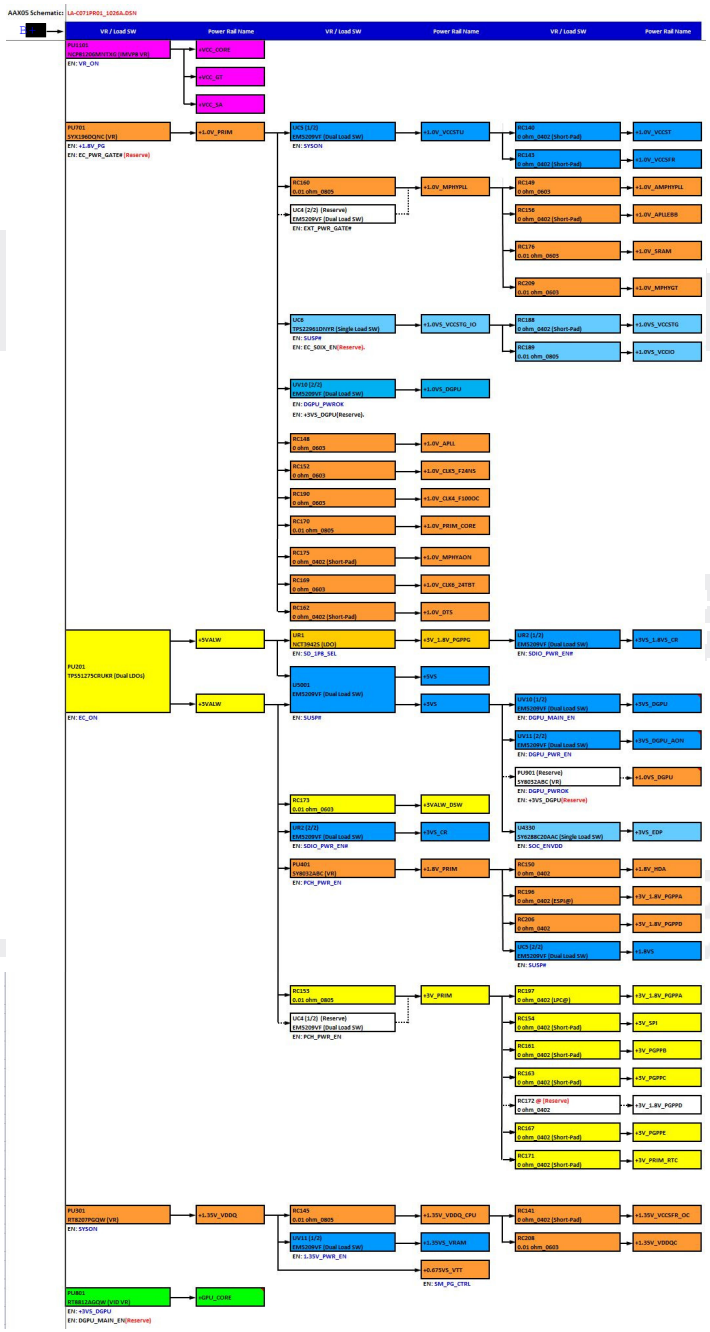
-PowerMap_KBL_DDR4_Volume_NON CS]



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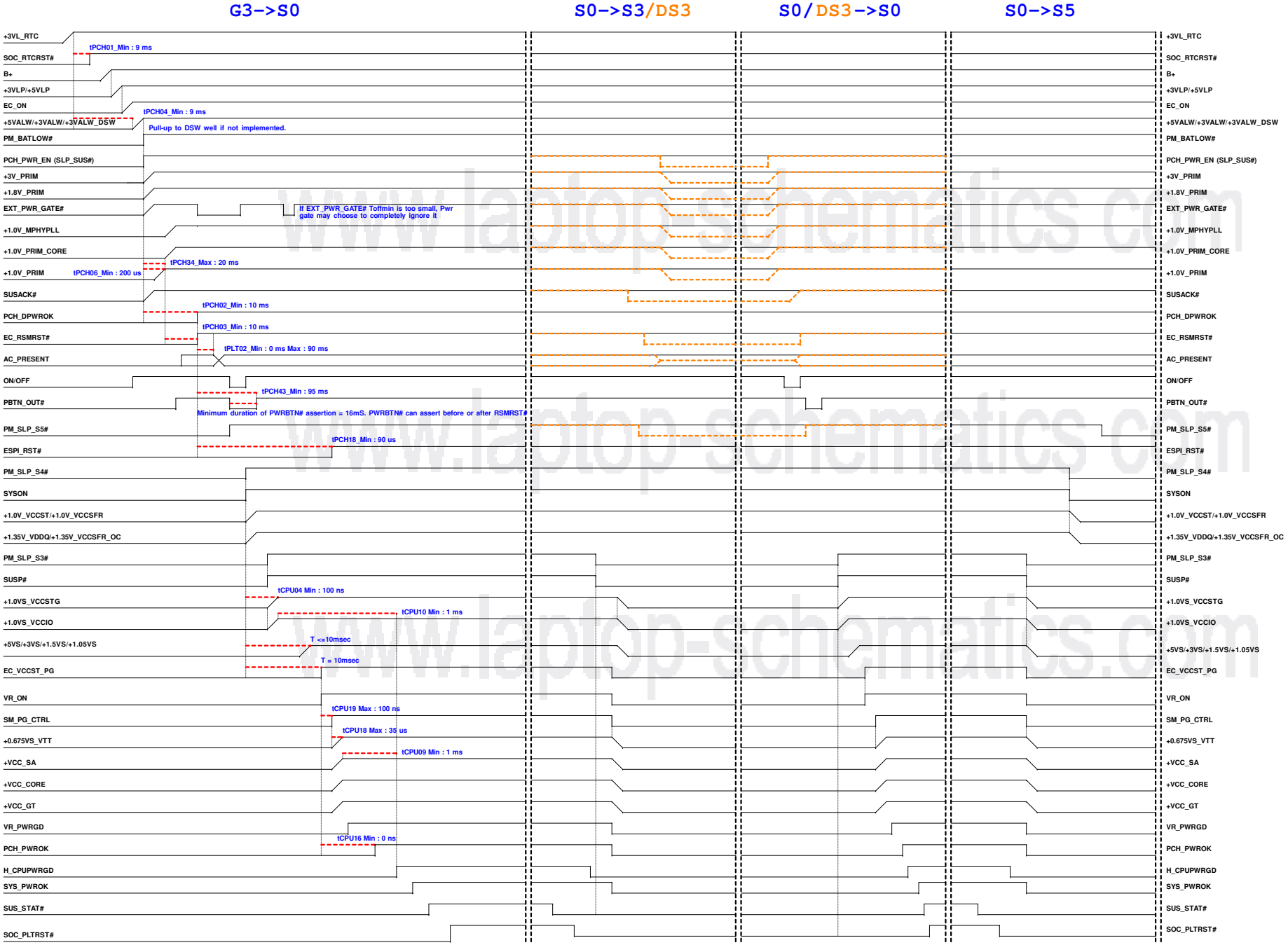

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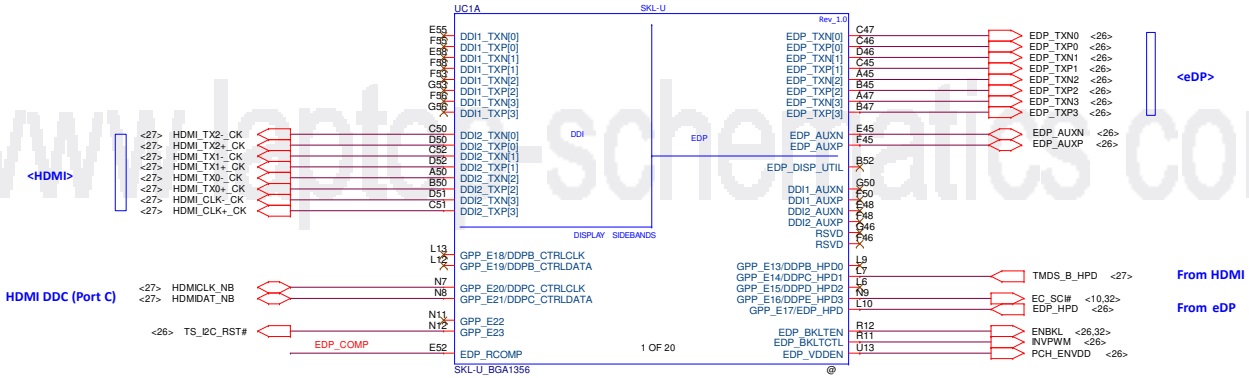


< Compensation PU For eDP >

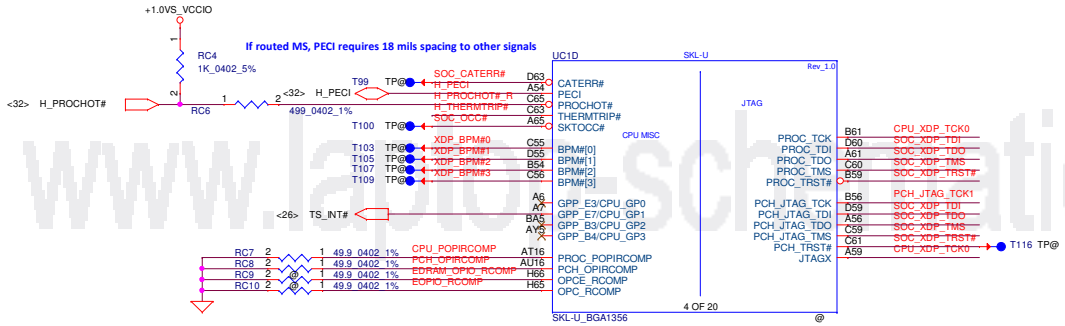
+1.0VS_VCCIO

RC3 1 2 EDP_COMP 24.9_0402_1%

Trace width=20 mils, Spacing=25mil, Max length=100mils

+1.0V_VCCST

RC5 1 2 H_THERMTRIP# 1K_0402_5%



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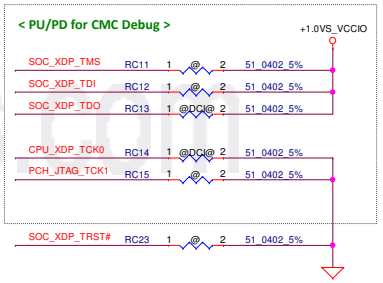

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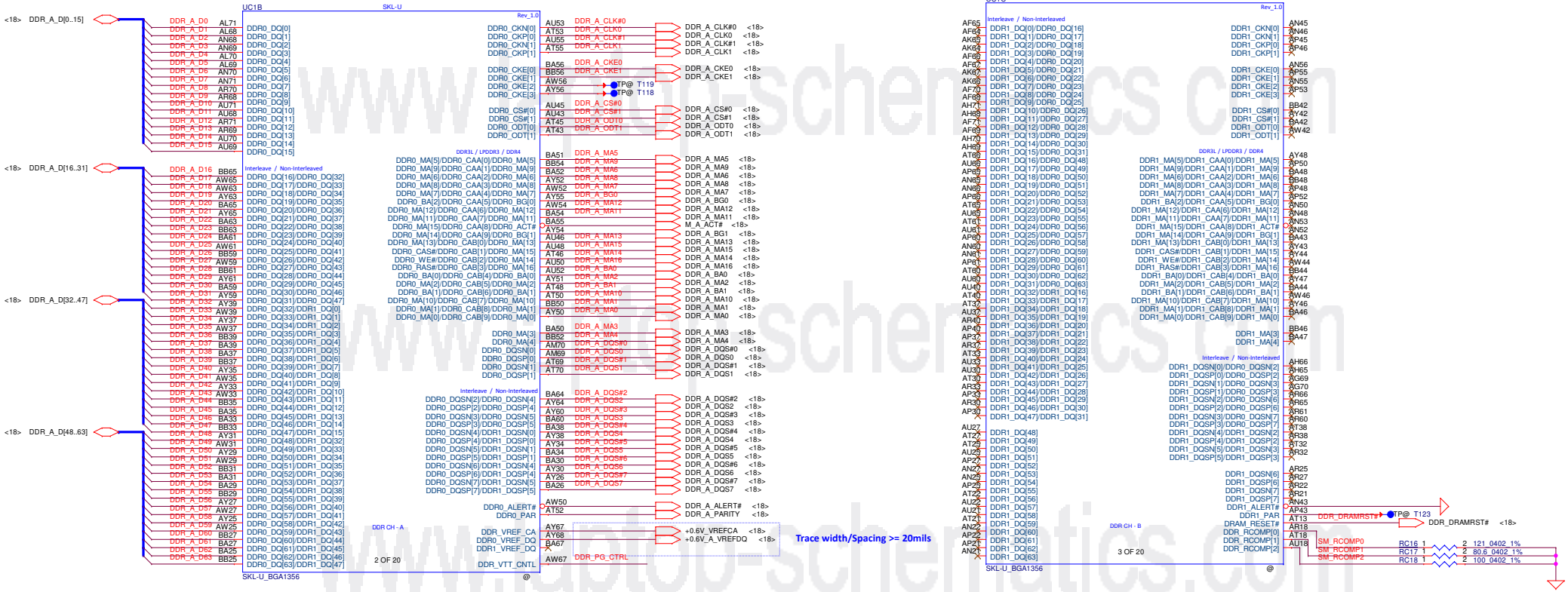
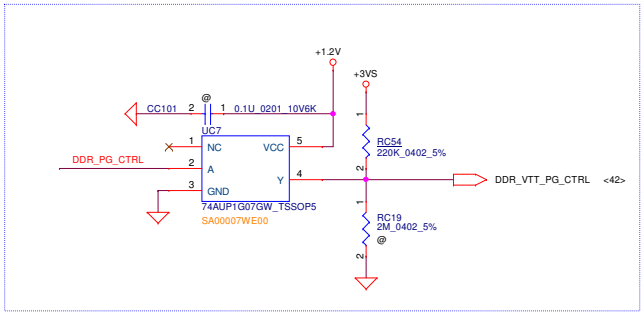
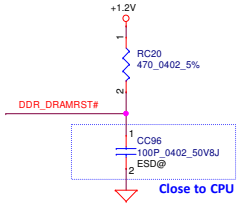
Interleaved Memory







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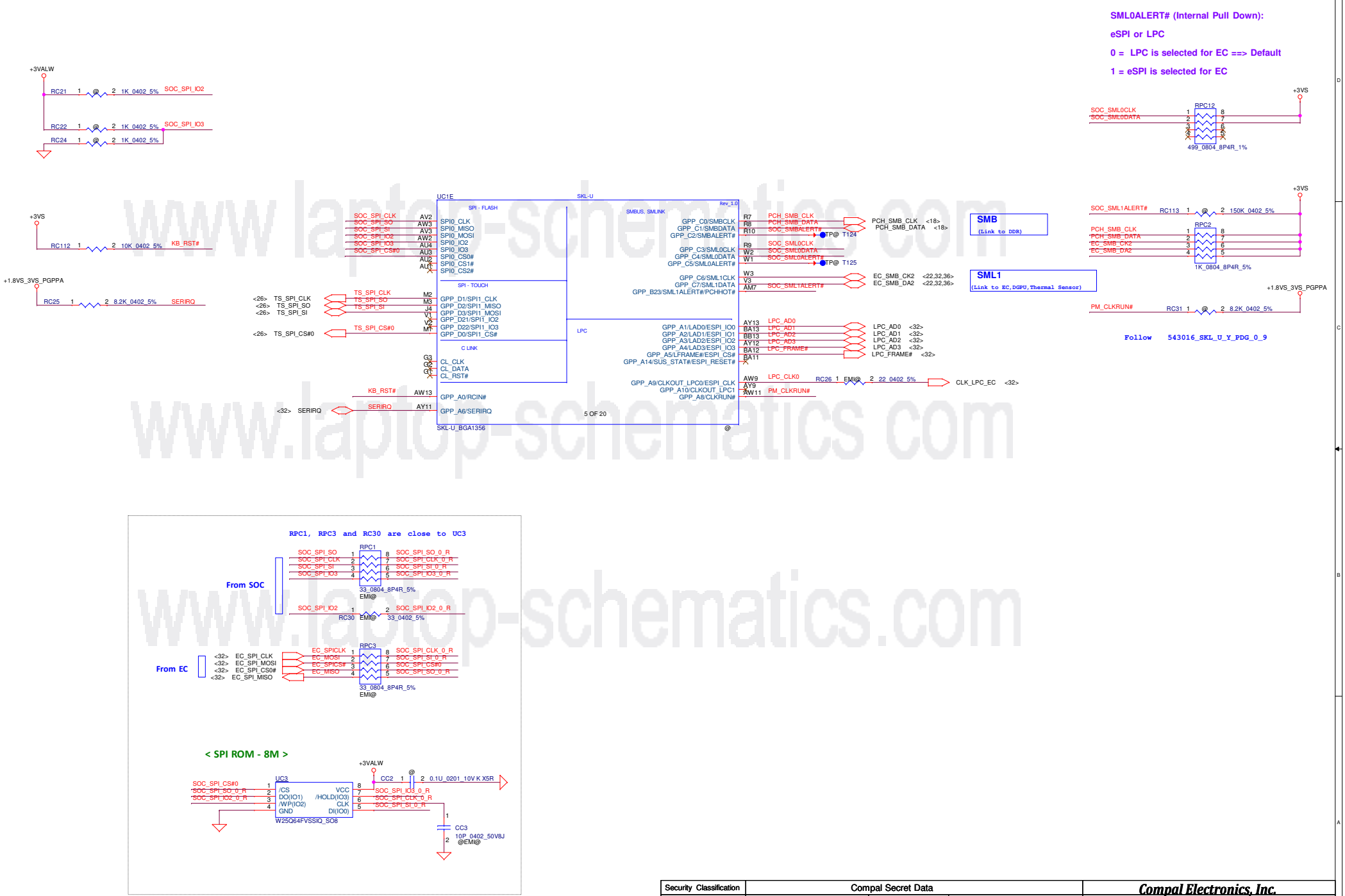

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Title	SKL-U(3/12)SPI,SMB,LPC,ESPI		
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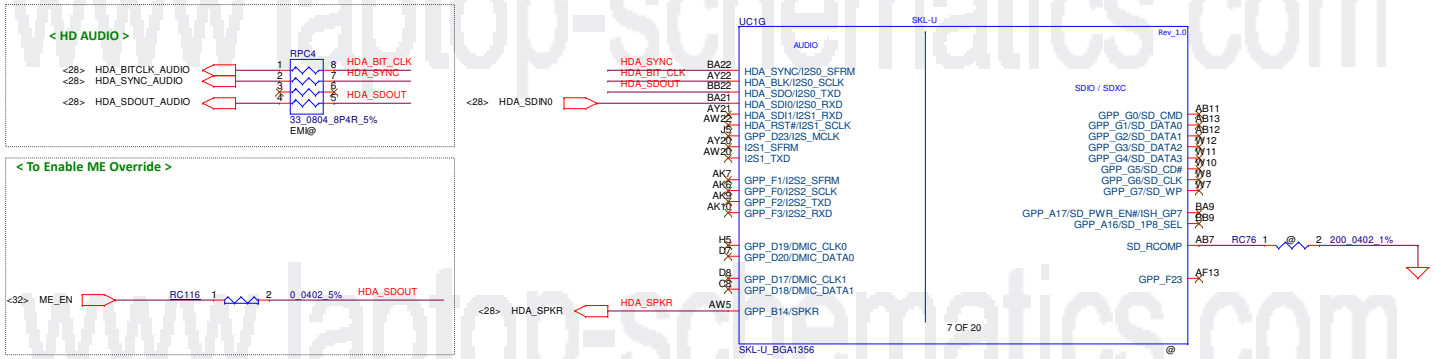

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Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2		
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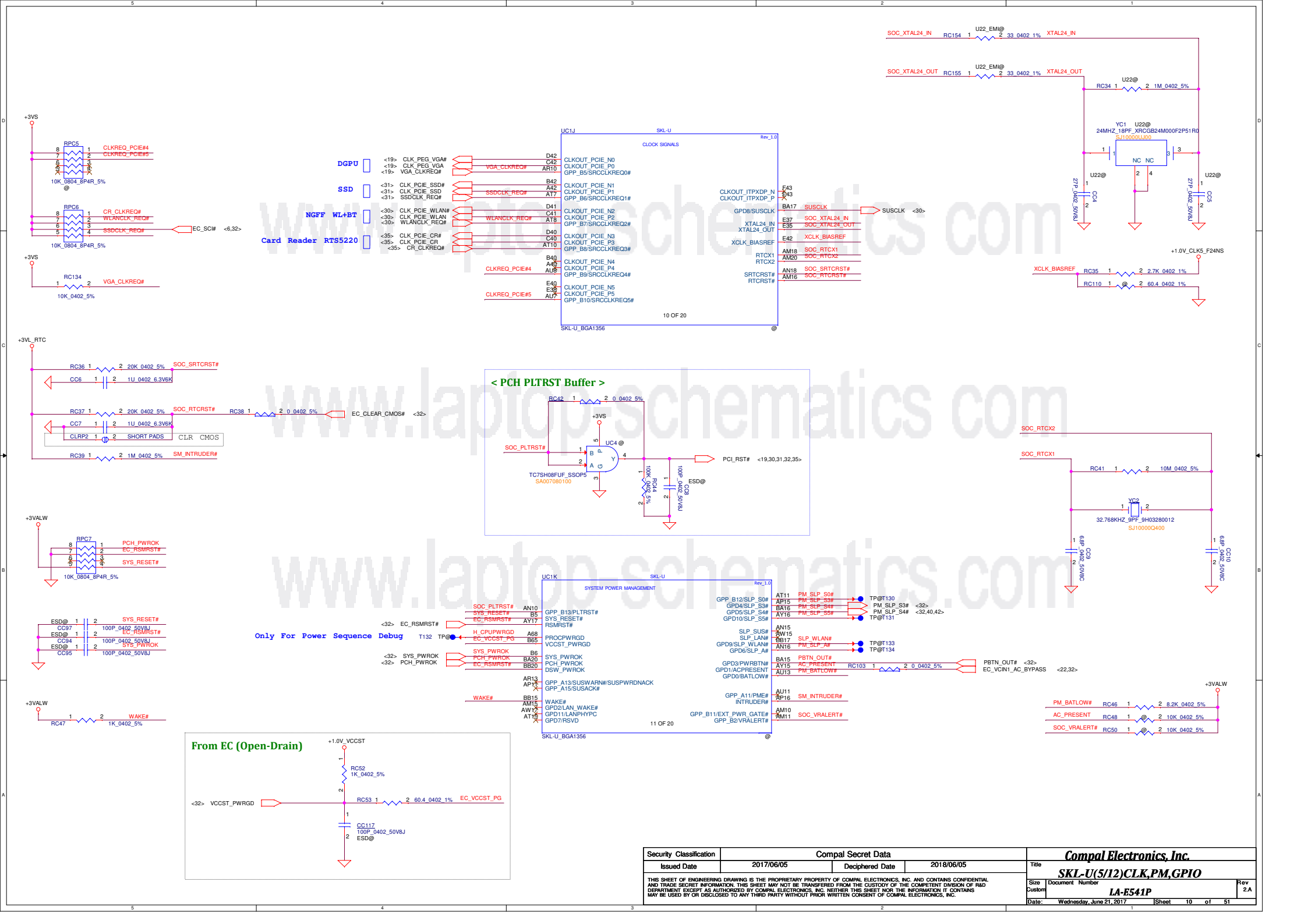

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GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

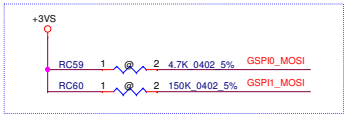
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This funct i oni s usef ul when running ITP/XDP.

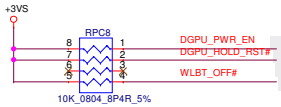
GSPI1_MOSI (Internal Pull Down):

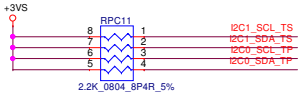
Boot BIOS Strap Bit

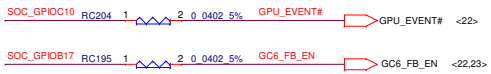
0 = SPI Mode ==> Default

1 = LPC Mode

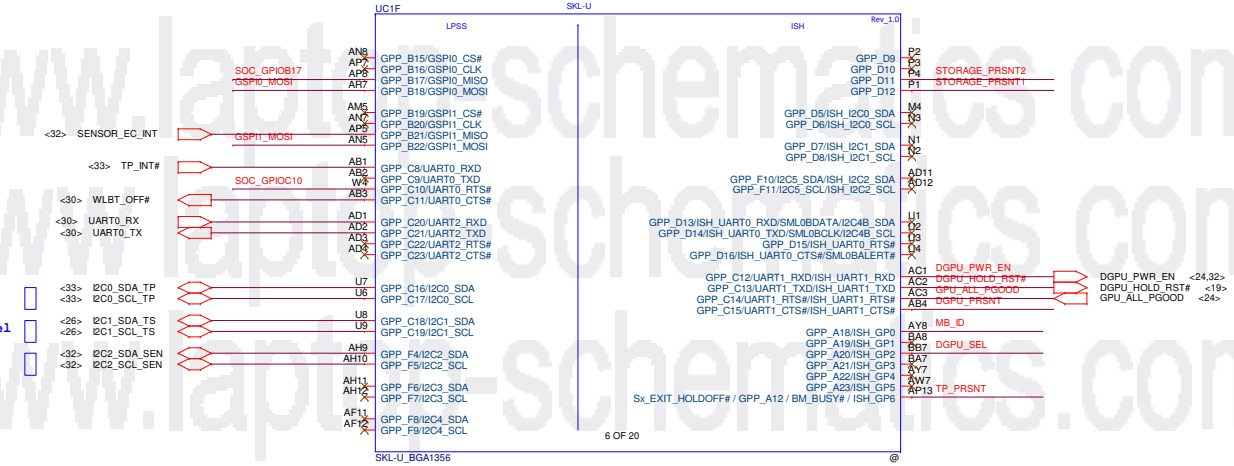


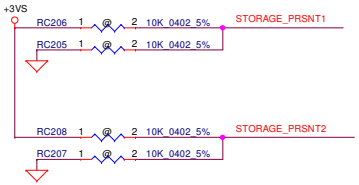




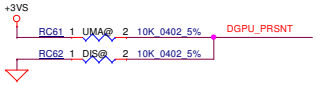


TO DGPU



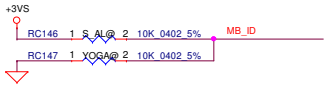


Funct i on	DGPU_PRSNT (GPP_C15)
DIS	0
UMA Only	1



Funct i on	MB_ID
YOGA series	0
S series	1

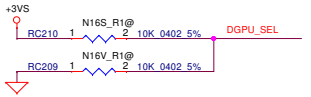
RC146 S_IMR@ 10K_0402_5%

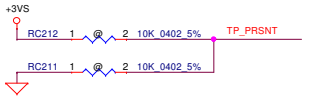


Funct i on	DGPU_SEL
N16V-GRM1(920)	0
N16S-GTR-S(940)	1

RC210 N16S_R3@ 10K_0402_5%

RC209 N16V_R3@ 10K_0402_5%





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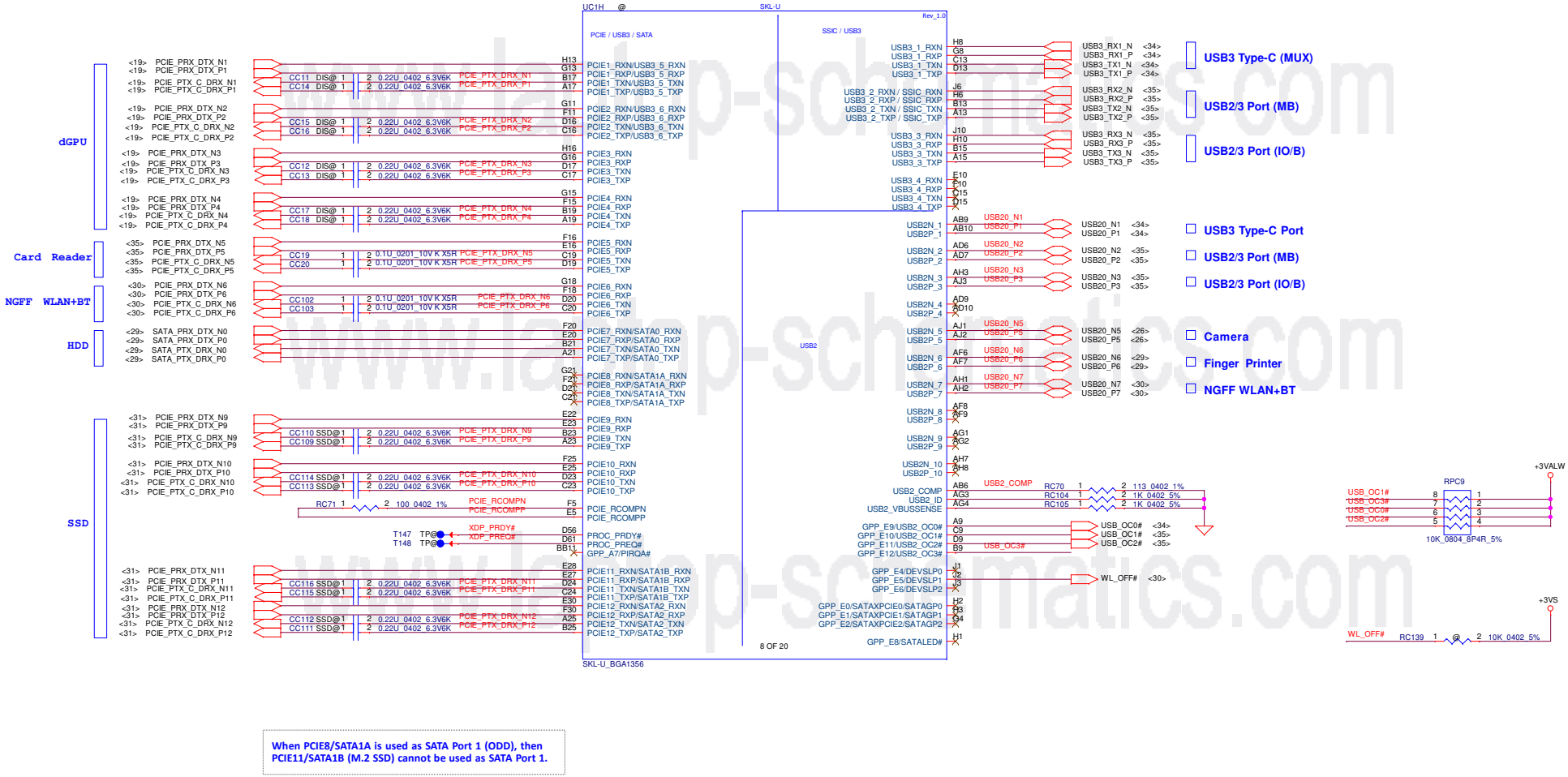
Compal Electronics, Inc.

Title: SKL-U(6/12)GPIO,I2C,GSPI

Size	Document Number	Rev
Custom	LA-E541P	2.A

Date: Wednesday, June 21, 2017 Sheet 11 of 51



When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

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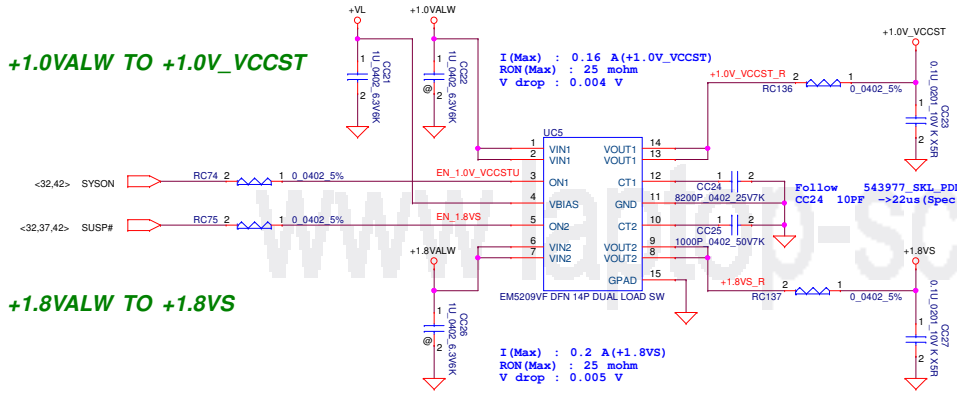
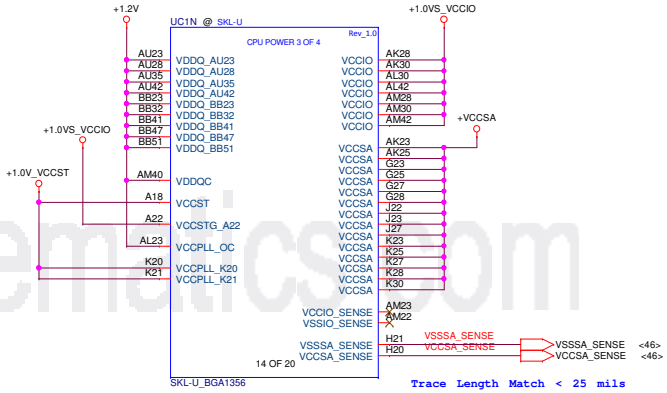
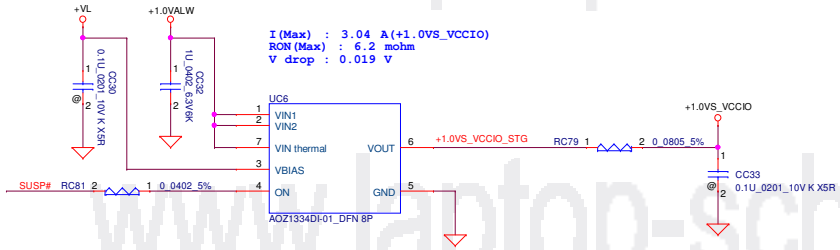
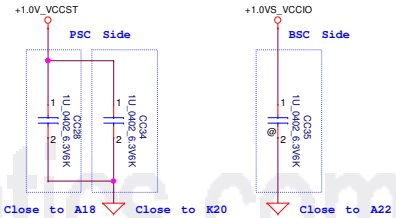
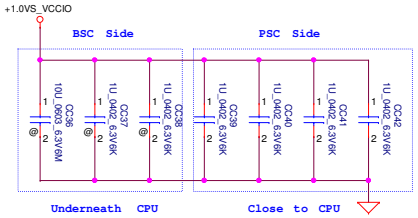
Compal Electronics, Inc.			
Title	SKL-U(7/12)PCIE,USB,SATA		
Size: Custom	Document Number: LA-E541P		Rev: 2.A
Date: Wednesday, June 21, 2017	Sheet 12 of 51		

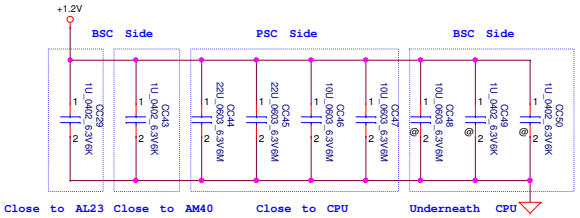












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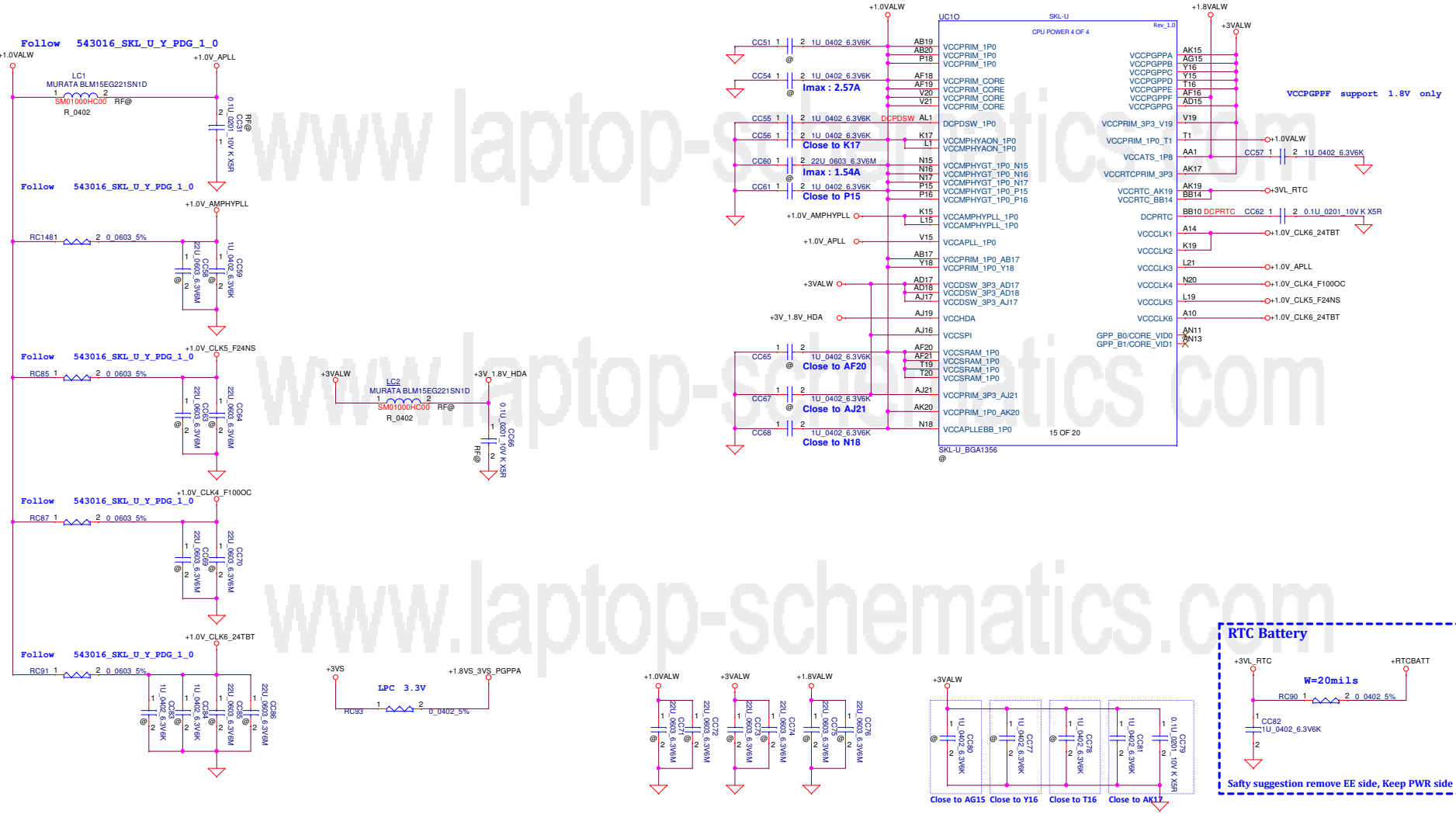
Compal Electronics, Inc.			
Title	SKL-U(8/12)Power		
Size: Custom	Document Number: LA-E541P		Rev: 2.A
Date: Wednesday, June 21, 2017	Sheet 13 of 51		



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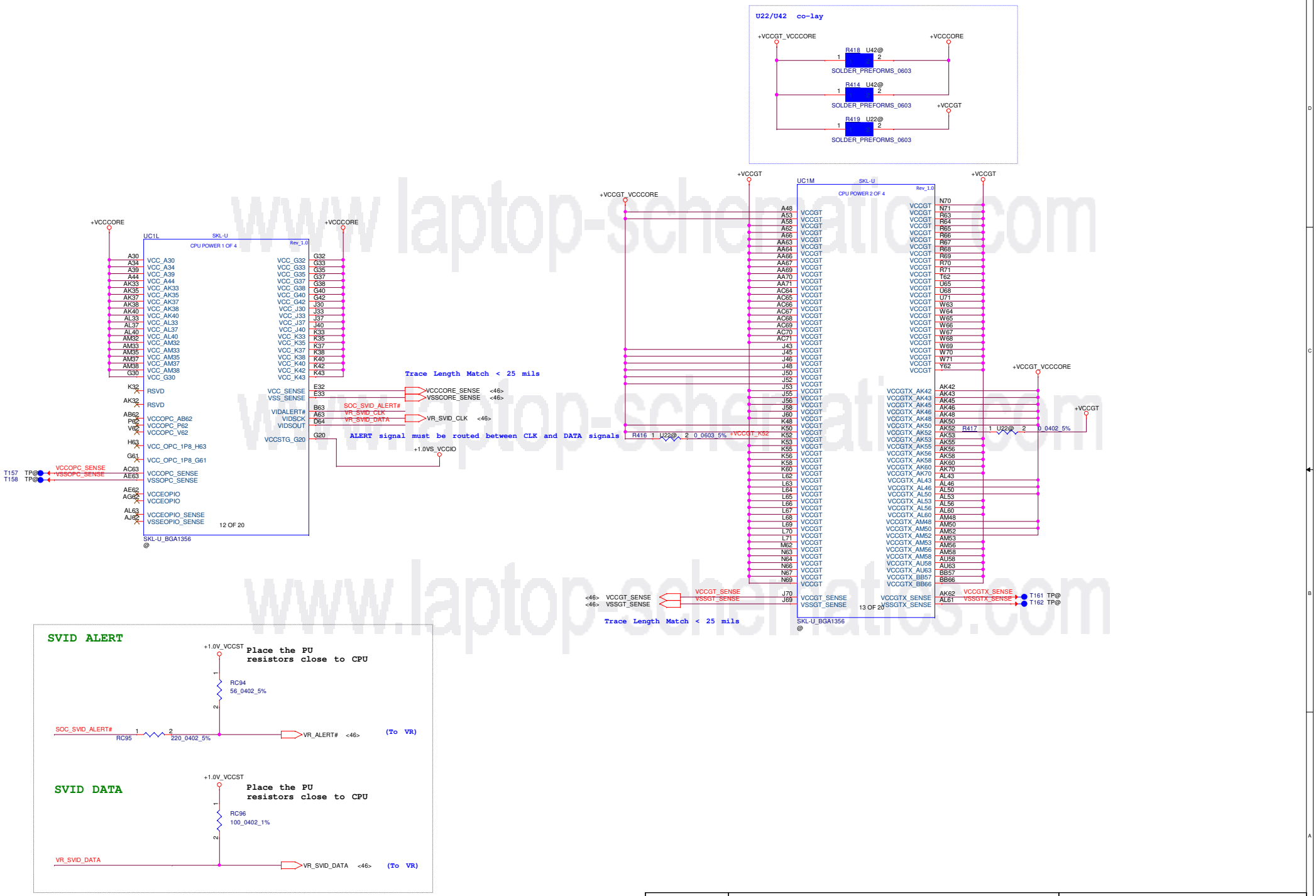
Compal Electronics, Inc.			
Title: SKL-U(9/12)Power			
Size: Custom	Document Number: LA-E541P		Rev: 2.A
Date: Wednesday, June 21, 2017	Sheet 14 of 51		



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Issued Date	2017/06/05	Deciphered Date	2018/06/05

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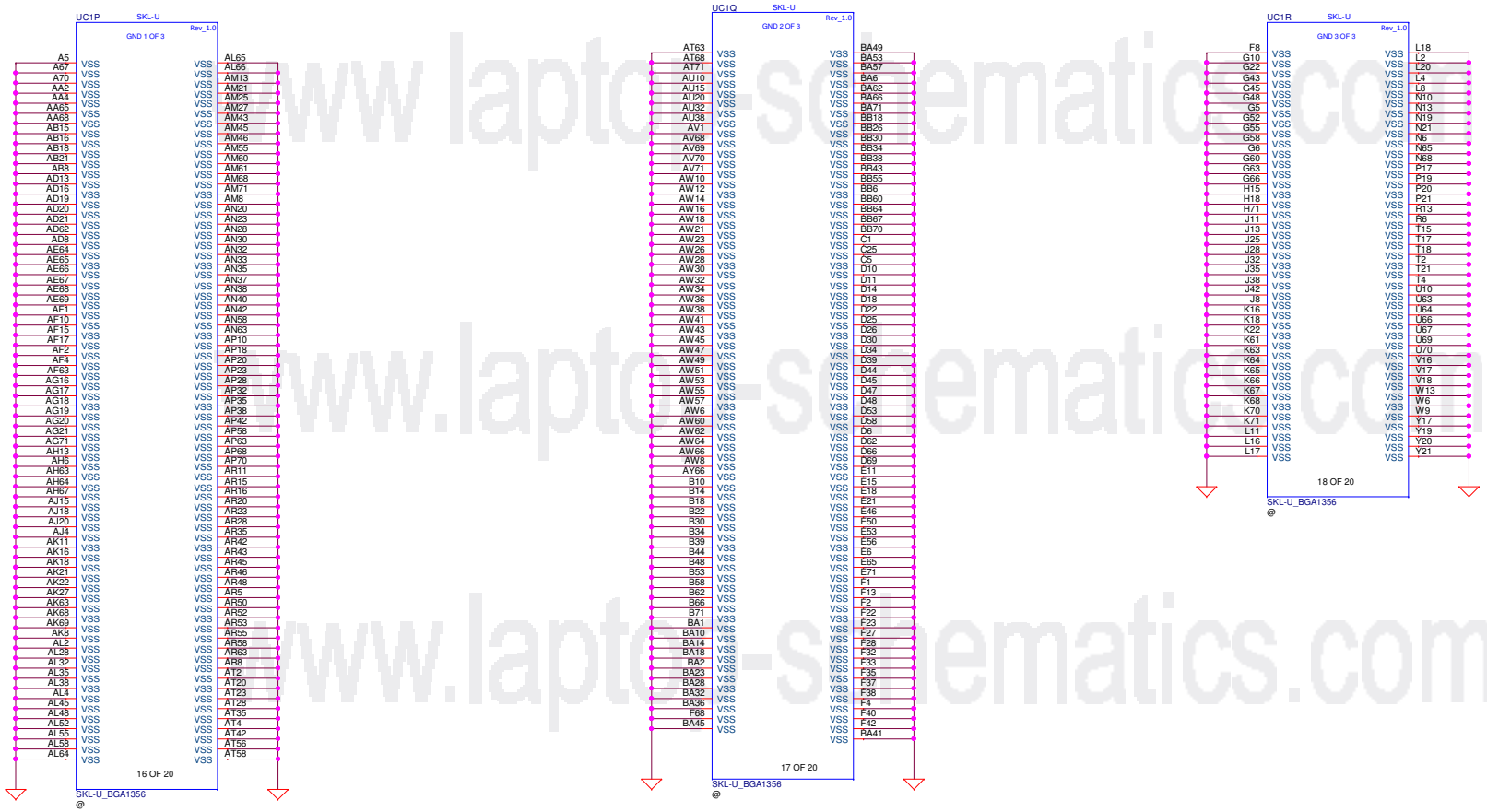
Compal Electronics, Inc.			
Title	SKL-U(10/12)Power,SVID		
Size Custom	Document Number LA-E541P		Rev 2.A
Date: Wednesday, June 21, 2017	Sheet 15 of 51		



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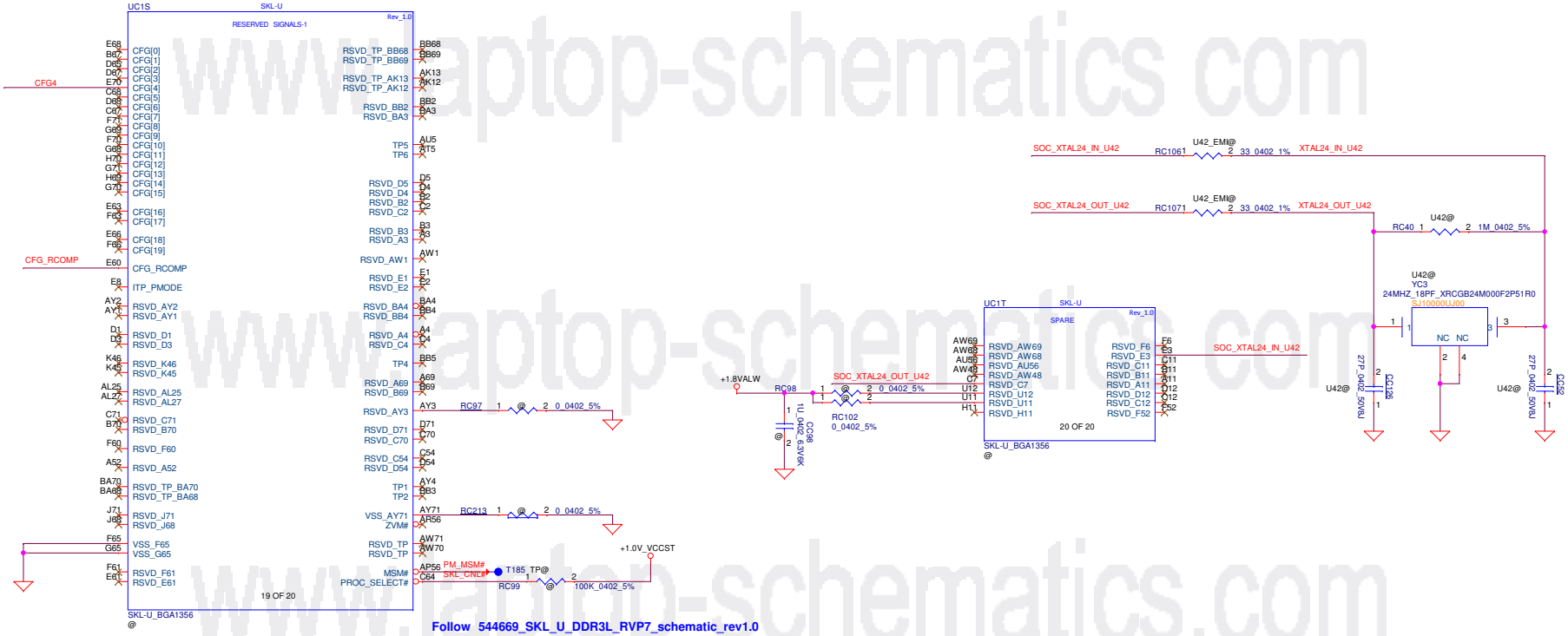
Compal Electronics, Inc.			
Title	SKL-U(11/12)GND		
Size: Custom	Document Number: LA-E541P		Rev: 2.A
Date: Wednesday, June 21, 2017	Sheet 16 of 51		



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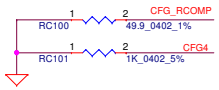
Follow 544669_SKL_U_DDR3L_RVP7_schematic_rev1.0

Stuff 100k(RC99) for CannonLake-U

Un-stuff 100k(RC99) for SkyLake-U



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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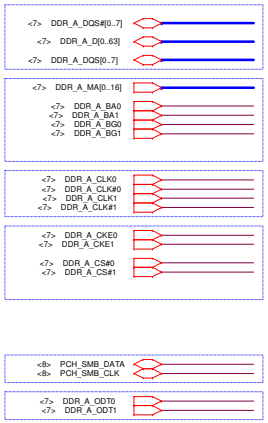
Compal Electronics, Inc.			
Title: SKL-U(12/12)CFG,RSVD			
Size: Custom	Document Number: LA-E541P		Rev: 2.A
Date: Wednesday, June 21, 2017	Sheet 17 of 51		

Interleaved Memory

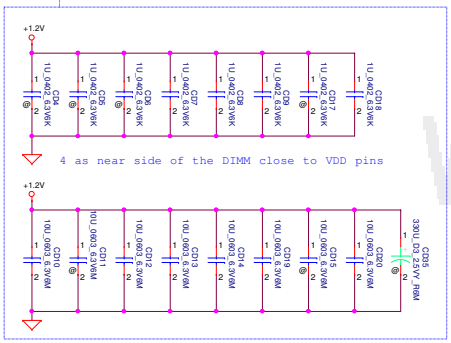
Reverse Type

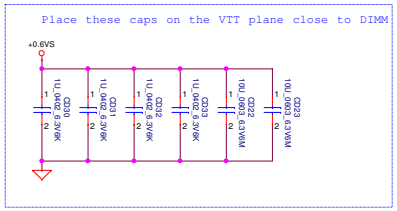
2-3A to 1 DIMMs/channel

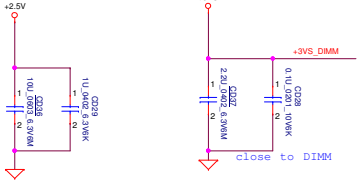


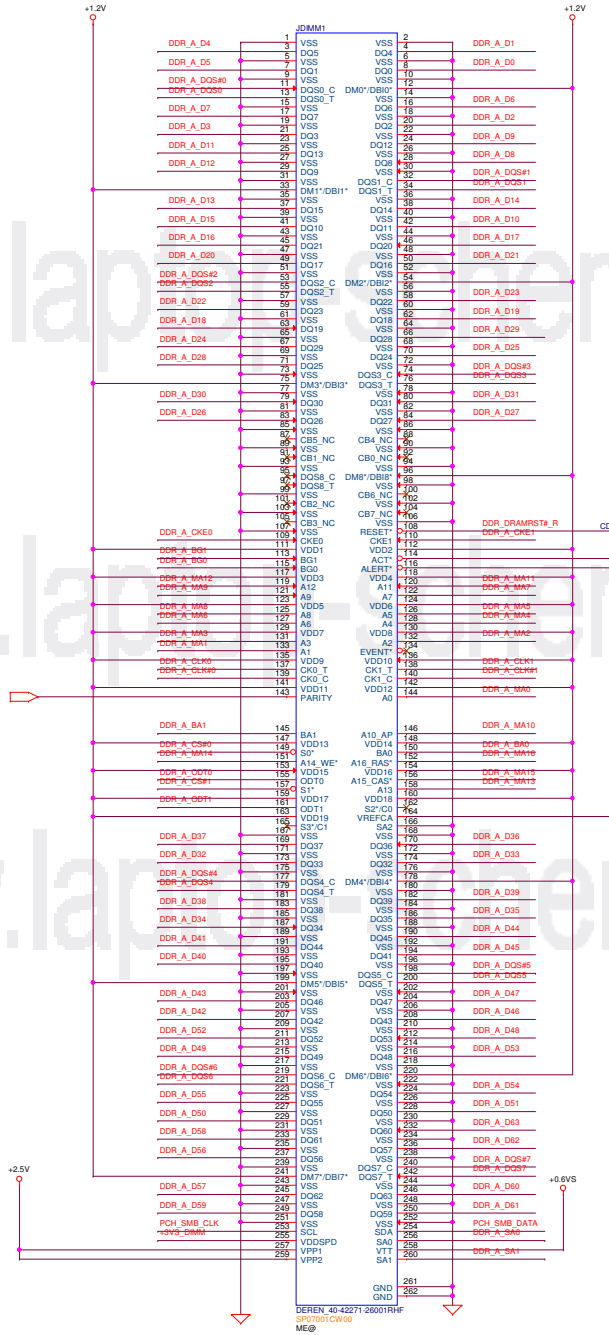
Layout Note:
Place near JDIMM1

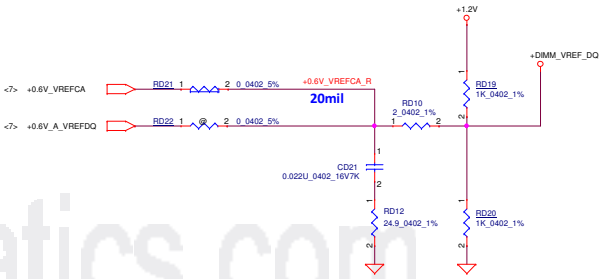
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

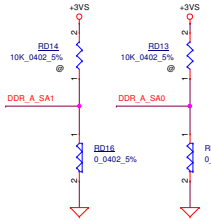












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Compal Electronics, Inc.			
Title: DDR4 DIMM			
Size: Custom	Document Number: LA-E541P		Rev: 2.A
Date: Wednesday, June 21, 2017	Sheet 18 of 51		

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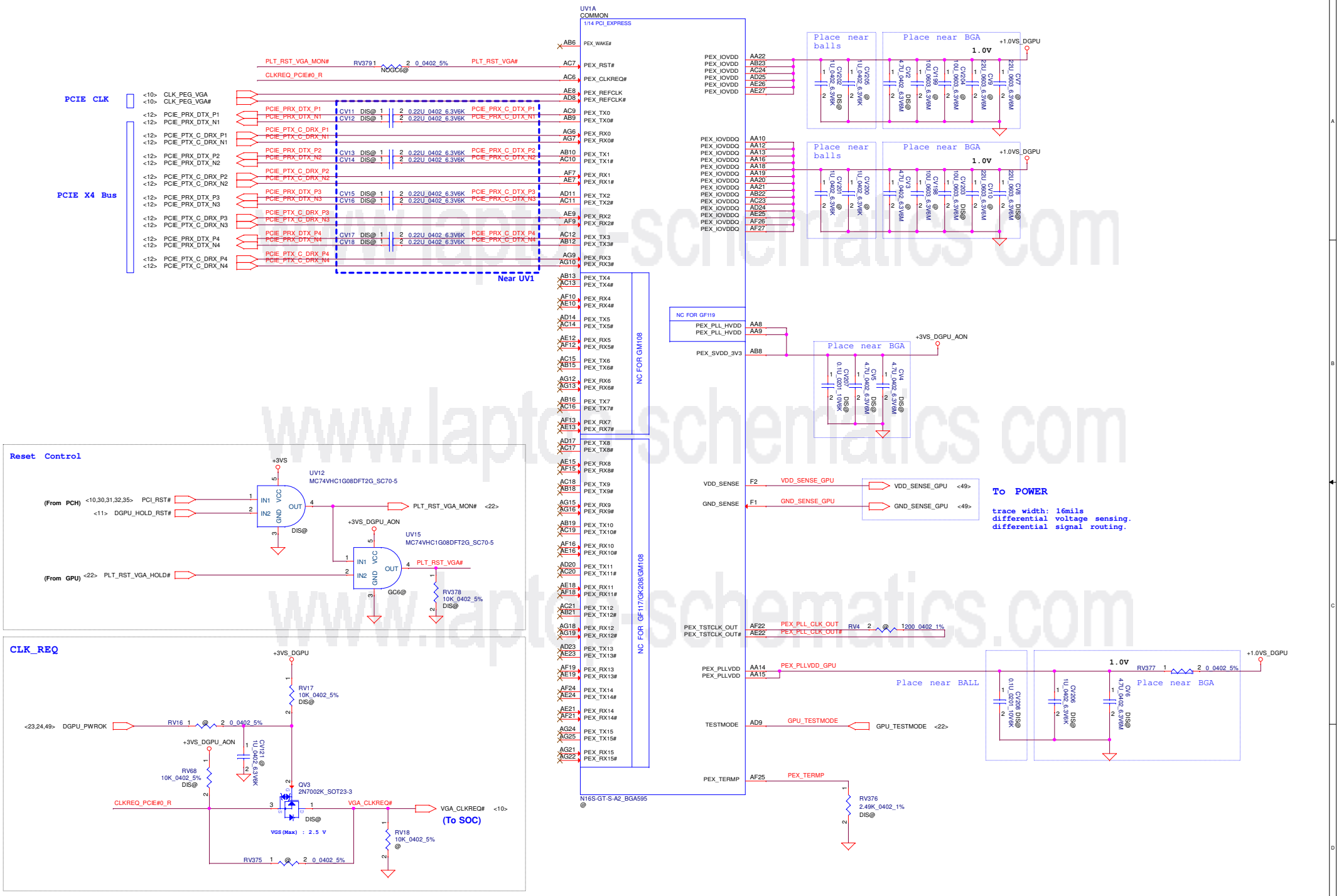

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Compal Electronics, Inc.

Title: **NV(1/5)-PCIE**

Size	Document Number	Rev
	LA-E541P	2.A

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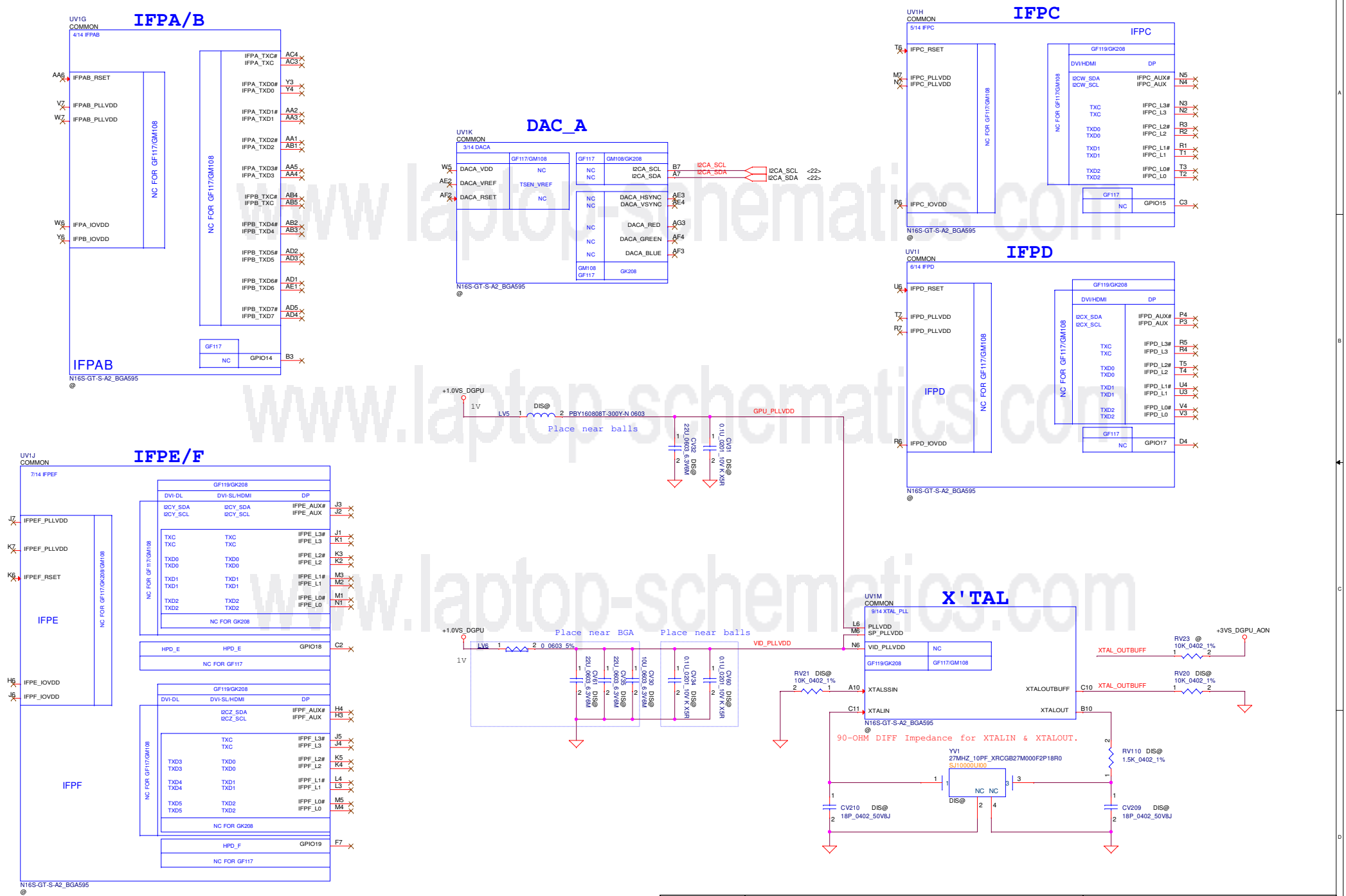

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Compal Electronics, Inc.	
Title	NV(2/5)-IFP_ABCDEF_DAC_XTAL
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Date:	Wednesday, June 21, 2017
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GPU_Decoupling CAPs @ Power Page

+1.35VS_VRAM

Place under GPU

CV217 4.7U_0402_6.3V6M DIS@
CV216 4.7U_0402_6.3V6M DIS@
CV218 1U_0402_6.3V6K DIS@
CV221 1U_0402_6.3V6K DIS@
CV222 0.1U_0201_10V6K DIS@
CV215 0.1U_0201_10V6K DIS@

Place near GPU

CV45 22U_0603_6.3V6M DIS@
CV44 10U_0603_6.3V6M DIS@

CIZ00 22uF x1 change to 10uF x2

UV1D COMMON 12/14 FBVDDQ

B26 C25 E23 E26 F14 F21 G13 G14 G15 G16 G18 G19 G20 G21 L22 L24 L26 M21 N21 R21 T21 V21 W21 — FBVDDQ

H24 H26 J21 K21 — FBVDDQ_AON

GF117 GF119 GK208 — FBVDDQ

N16S-GT-S-A2_BGA595 @

+VGA_CORE

Voltage by GPU SKU

UV1E COMMON 11/14 NVVDD

K10 K12 K14 K16 K18 L11 L13 L15 L17 M10 M12 M14 M16 M18 N11 N13 N15 N17 P10 P12 P14 P16 P18 R11 R13 R15 R17 T10 T12 T14 T16 T18 U11 U13 U15 U17 V10 V12 V14 V16 V18 — VDD

N16S-GT-S-A2_BGA595 @

Near Ball

+1.35VS_VRAM

FB_CAL_PD_VDDQ — D22 — RV41 1 DIS@ 2 40.2_0402_1%

FB_CAL_PU_GND — C24 — RV42 2 DIS@ 1 40.2_0402_1%

FB_CALTERM_GND — B25 — RV43 2 DIS@ 1 60.4_0402_1%

UV1F COMMON 13/14 GND

A2 AB17 AB20 AB24 AC2 AC22 AC26 AC5 AC8 AD12 AD13 A26 AD15 AD16 AD18 AD19 AD21 AD22 AE11 AE14 AE17 AE20 AB11 AF1 AF11 AF14 AF17 AF20 AF23 AF5 AF8 AG2 AG26 AB14 B1 B11 B14 B17 B20 B23 B27 B5 B8 E11 E14 E17 E2 E20 E22 E25 E5 E8 H2 H23 H25 H5 K11 K13 K15 K17 L10 L12 L14 L16 L18 L2 L23 L25 L5 M11 M13 M15 M17 N10 N12 N14 N16 N18 P11 P13 P15 P17 P2 P23 P26 P5 R10 R12 R14 R16 R18 T11 T13 T15 T17 U10 U12 U14 U16 U18 U2 U23 U26 U5 V11 V13 V15 V17 Y2 Y23 Y26 Y5 AA7 AB7 — GND

N16S-GT-S-A2_BGA595 @

UV1C COMMON 14/14 XVDD/VDD33

AD10 AD7 — NC

3V3_AON — GM108

G8 G9 G10 G12 — VDD33

F11 — 3V3AUX_NC

V5 V6 — FERMI_RSVD1_NC FERMI_RSVD2_NC

Under GPU / Near GPU

CV220 0.1U_0201_10V6K DIS@
CV211 0.1U_0201_10V6K DIS@
CV219 1U_0402_6.3V6K DIS@
CV218 4.7U_0402_6.3V6M DIS@

+3VS_DGPU

CONFIGURABLE POWER CHANNELS

* nc on substrate

G1 G2 G3 G4 G5 G6 G7 — XPWR_G1 XPWR_G2 XPWR_G3 XPWR_G4 XPWR_G5 XPWR_G6 XPWR_G7

V1 V2 — XPWR_V1 XPWR_V2

W1 W2 W3 W4 — XPWR_W1 XPWR_W2 XPWR_W3 XPWR_W4

Under GPU / Near GPU

CV214 0.1U_0201_10V6K DIS@
CV212 1U_0402_6.3V6K DIS@
CV213 4.7U_0402_6.3V6M DIS@

+3VS_DGPU_AON

N16S-GT-S-A2_BGA595 @

** XPWR pins are configurable.

These pins are not connected on the substrate.

Therefore, XPWR pins can be assigned as needed, to improve Top layer routing, power delivery.

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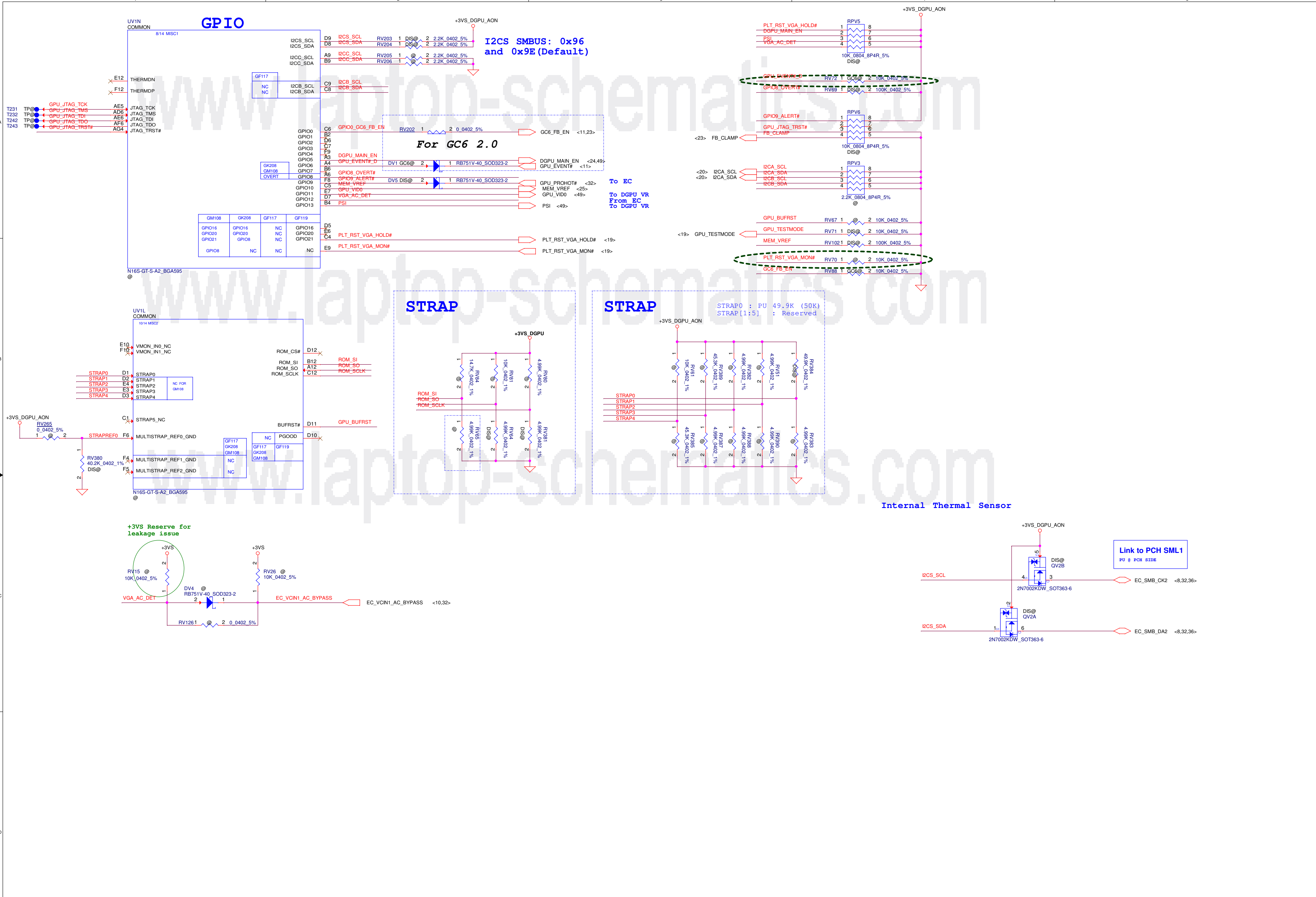
Title: NV(3/5)-POWER

Size: | Document Number: LA-E541P | Rev: 2.A

Date: Wednesday, June 21, 2017 | Sheet 21 of 51



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Issued Date	2017/06/05	Deciphered Date 2018/06/05	Title NV(4/5)-GPIO/Strap
			Size Document Number LA-E541P Rev 2.A
			Date: Wednesday, June 21, 2017 Sheet 22 of 51

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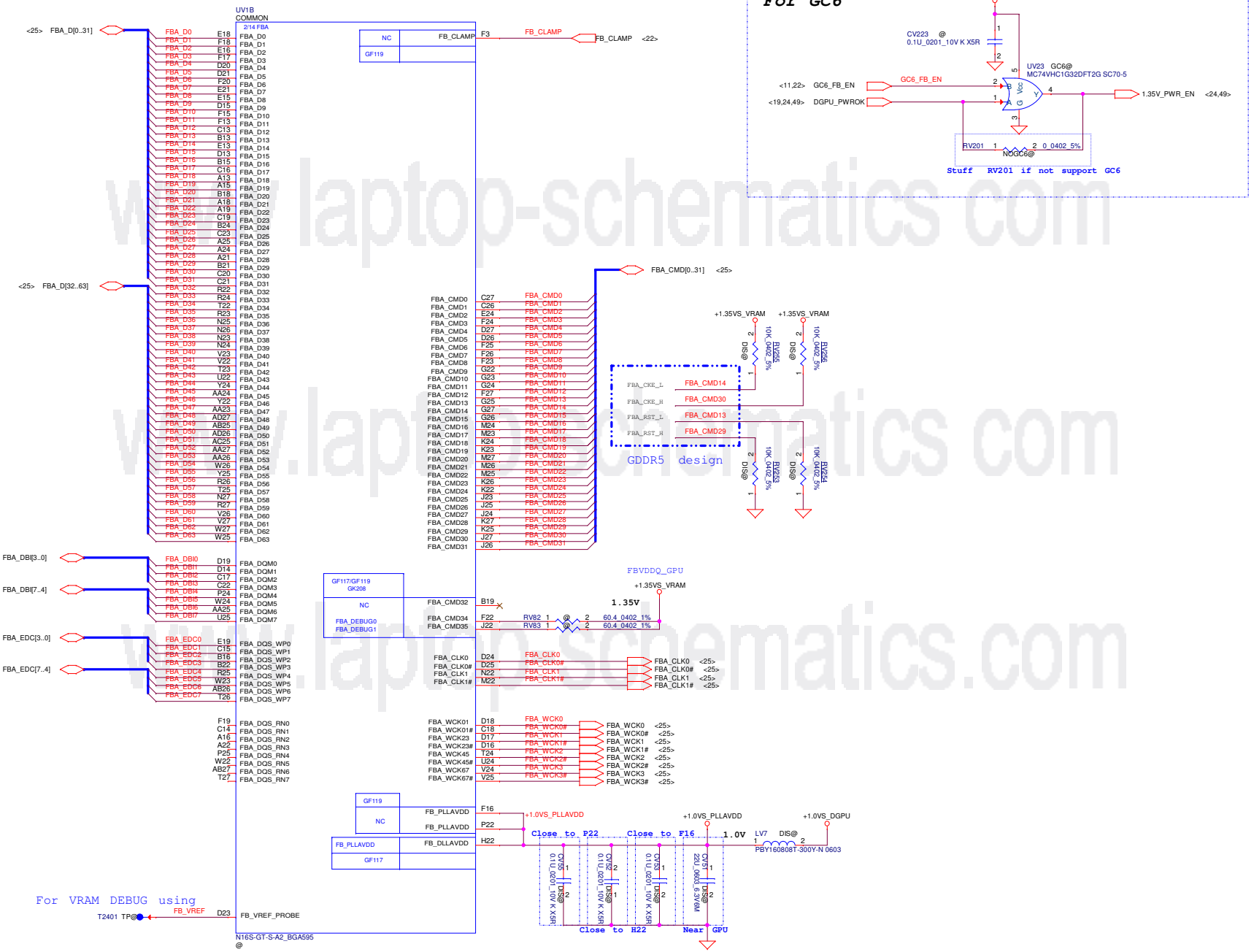

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Issued Date	2017/06/05	Deciphered Date	2018/06/05

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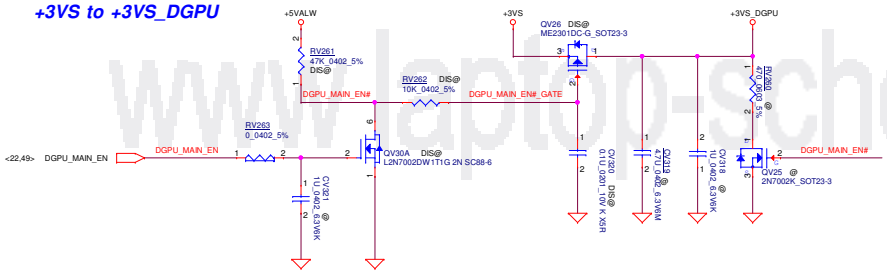
Compal Electronics, Inc.

Title: **NV(5/5)-MEMORY FBA**

Size	Document Number	Rev
	LA-E541P	2.A

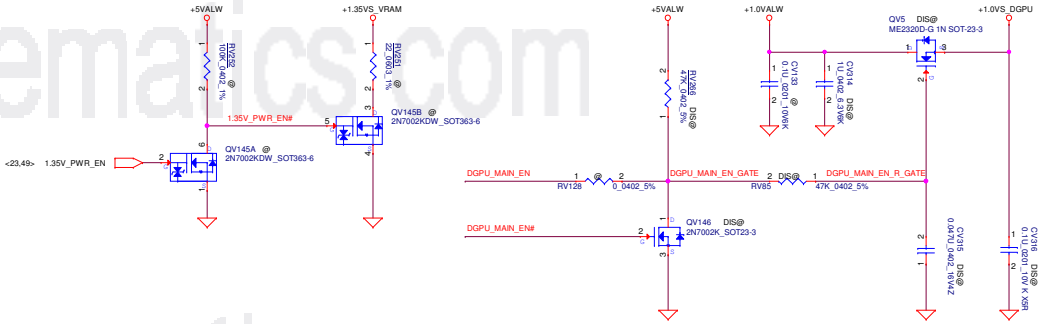
Date: Wednesday, June 21, 2017 | Sheet 23 of 51

+3VS to +3VS_DGPU

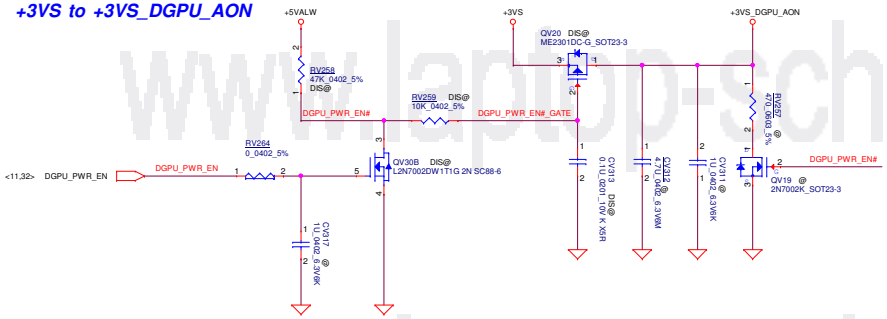


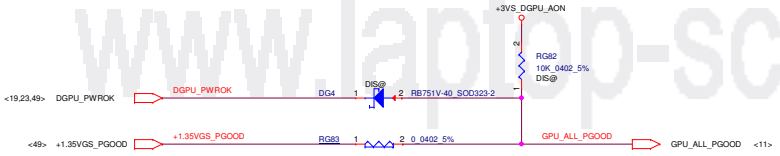
+1.0V_PRIM to +1.0VS_DGPU

I_Continuous(Max) : 0.79 A(+1.0VS_DGPU)
RON(Max) : 22 mohm
V drop : 0.0175 V
Rising : ~ 208us



+3VS to +3VS_DGPU_AON





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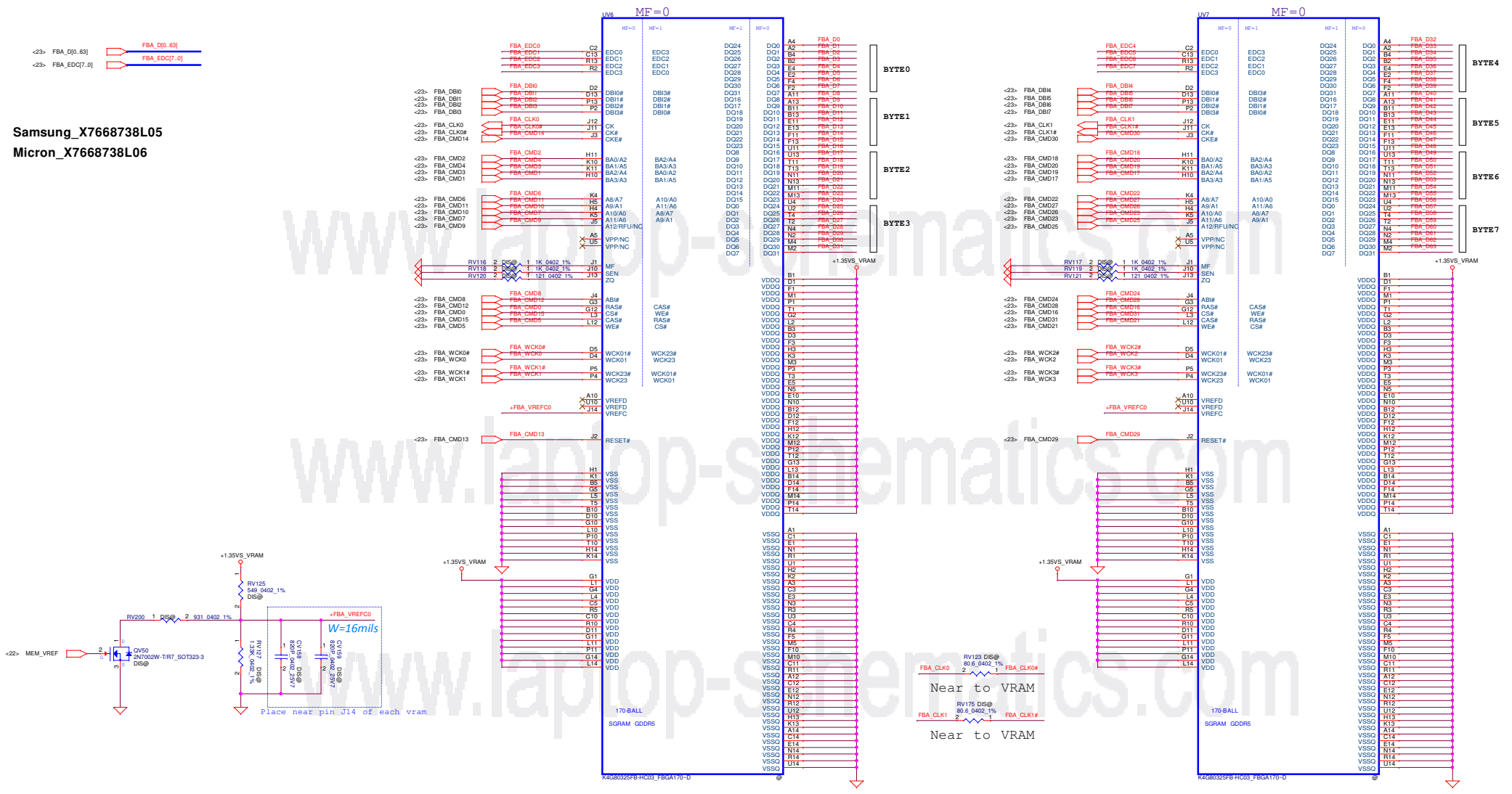
Compal Electronics, Inc.			
Title: DGPU_DC/DC Interface			
Size	Document Number: LA-E541P		Rev: 2.A
Date: Wednesday, June 21, 2017	Sheet 24 of 51		

Memory Partition A

Samsung_X7668738L05

Micron_X7668738L06



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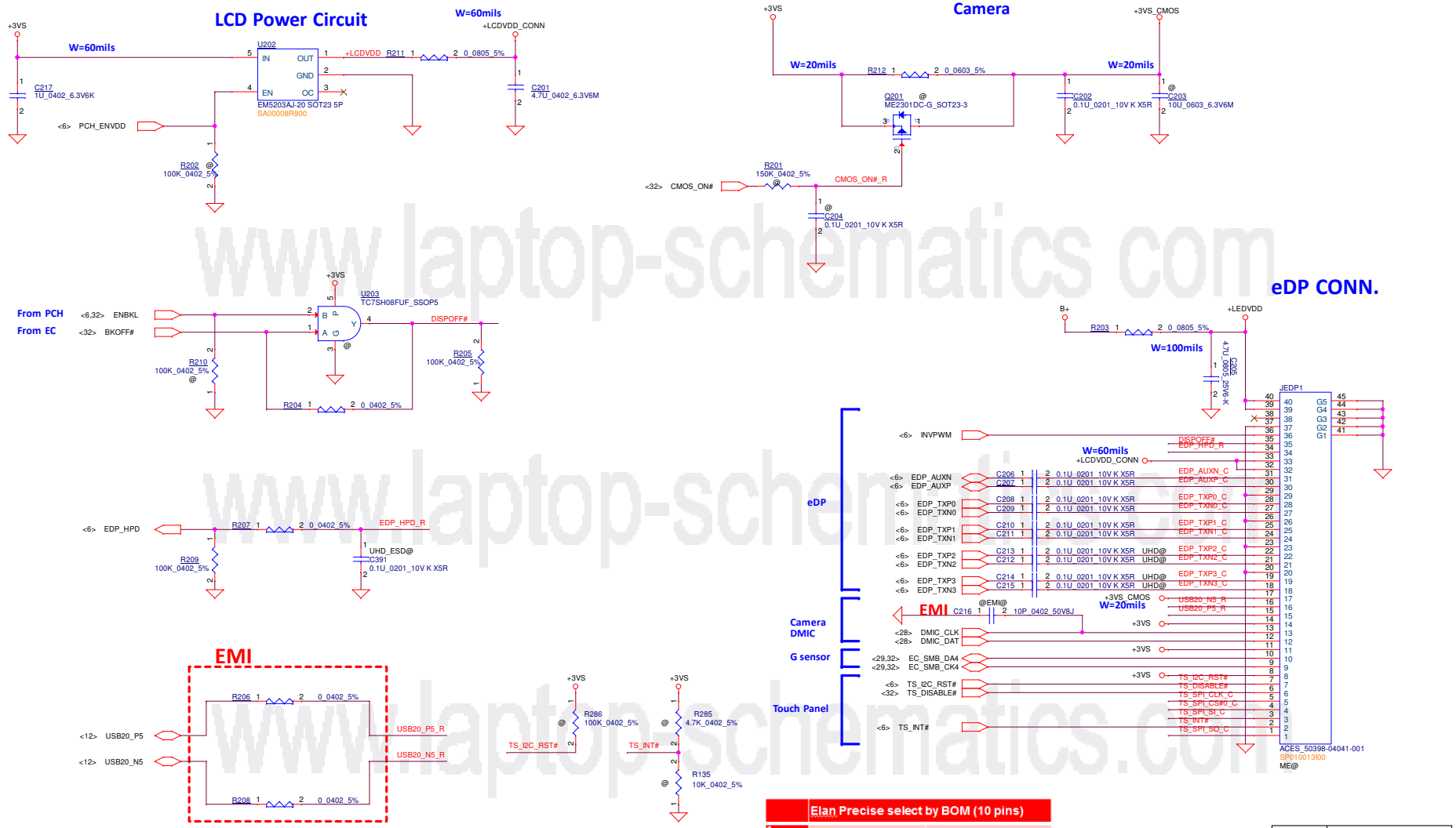
Compal Electronics, Inc.	
Title	N16P_GDDR5_A
Size	Document Number: LA-E541P
Rev	2.A
Date:	Wednesday, June 21, 2017
Sheet	25 of 51



	Elan Precise select by BOM (10 pins)	
1	PWR	PWR
2	CS	SCL
3	SCK	SDA
4	MOSI	Report switch
5	MISO	INT
6	Report switch	Reset
7	INT	Hsync
8	Reset	GND
9	Hsync	
10	GND	
Total	SPI (10 pins)	I2C (8 pins)

	SPI & I2C PIN define
1	PWR
2	SPI_Reset/I2C_Reset
3	Report_switch
4	GND
5	SPI_SCK/I2C_SCL
6	SPI_CS/I2C_SDA
7	SPI_MOSI
8	SPI_INT/I2C_INT
9	SPI_MISO
10	GND

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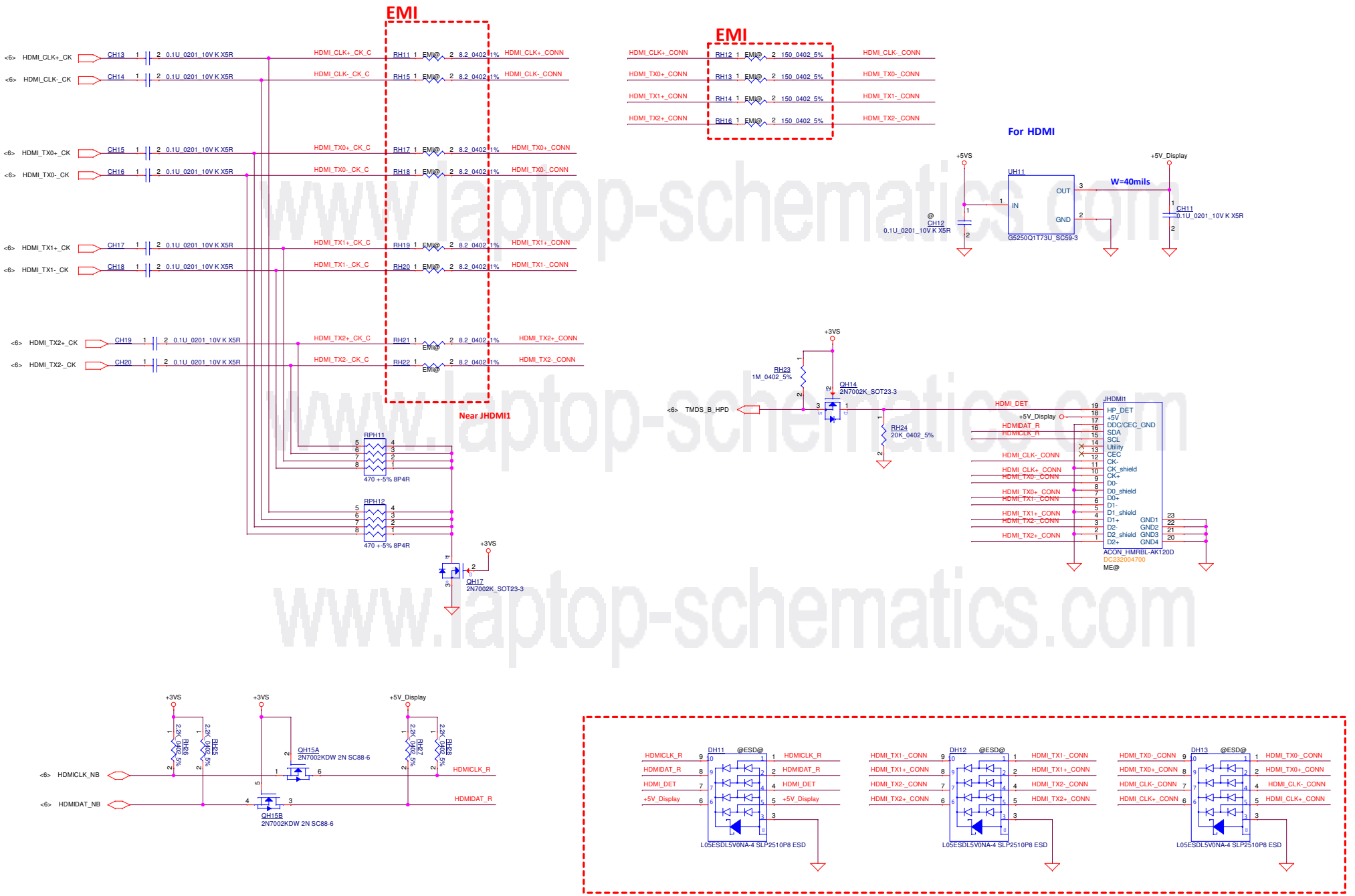
Compal Electronics, Inc.			
Title	eDP / Camera		
Size	Document Number	LA-E541P	Rev 2.A
Custom			
Date: Wednesday, June 21, 2017	Sheet 26 of 51		



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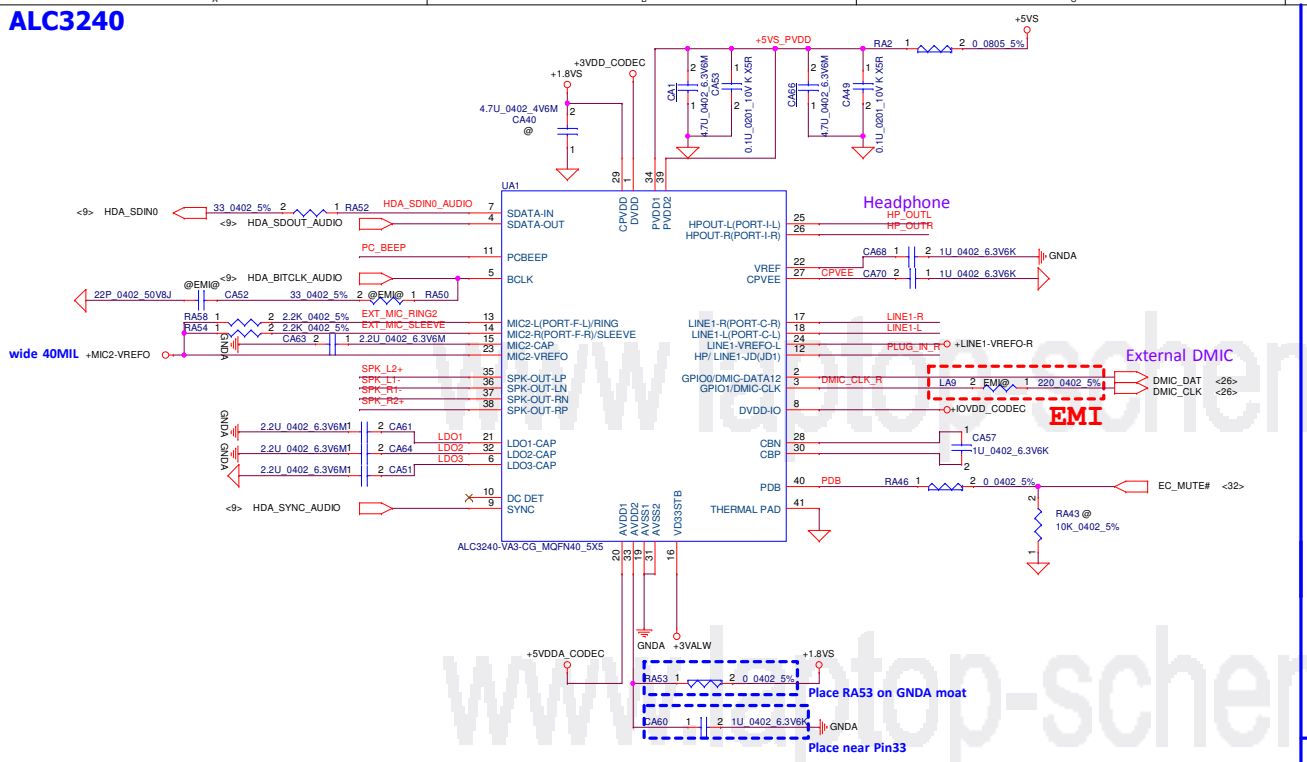
Compal Electronics, Inc.

Title: **HDMI**

Size	Document Number	Rev
Custom	LA-E541P	2.A

Date: Wednesday, June 21, 2017 | Sheet 27 of 51

ALC3240



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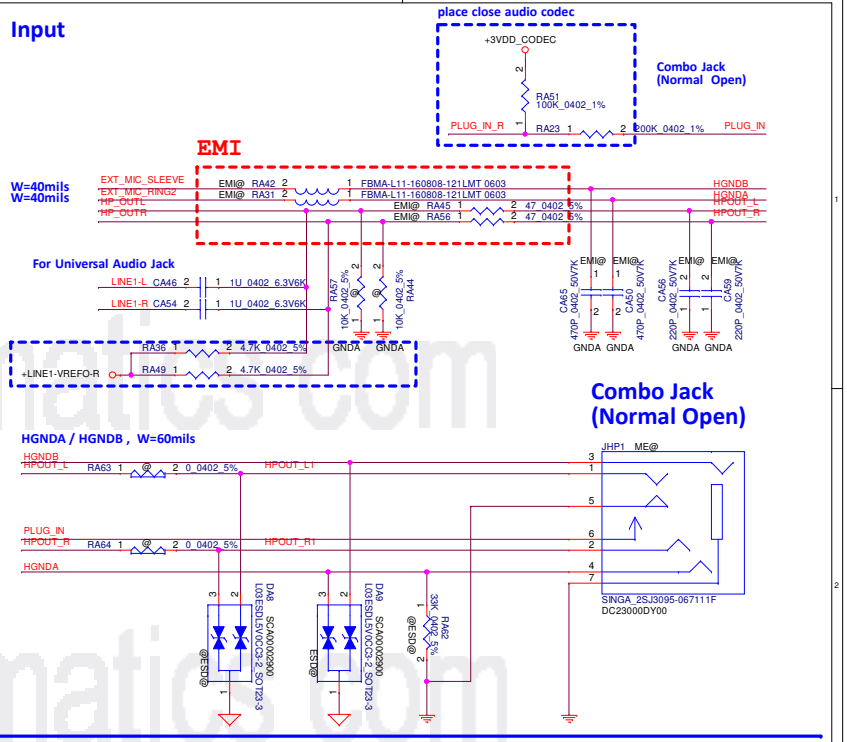

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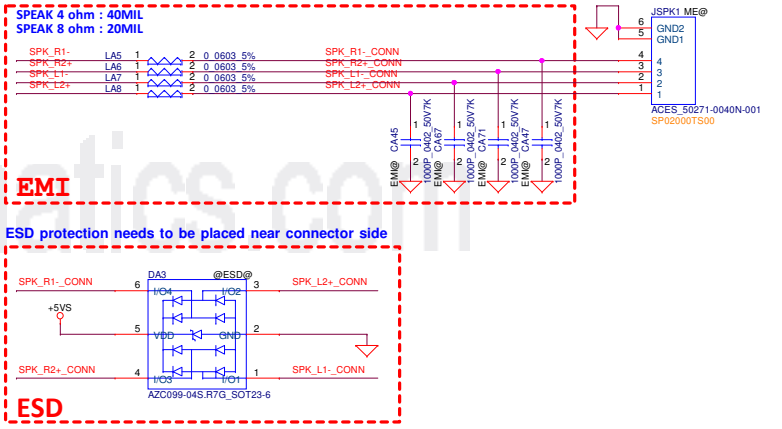
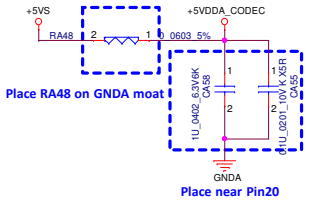


+5VS to +5VDDA_CODEC



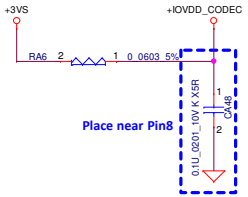
Each Platform Power Net Support List :

	+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
	1.5V(S0)	1.8V(S0)	3.3V(S0)	5V(S0)	3.3V(S0~S5)
Intel Broadwell	V	X	V	V	V
Intel Skylake	X	V	V	V	V

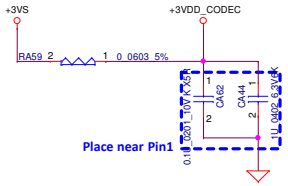
Each Platform HDA Link Voltage Support (Pin 8) :

	3.3V	1.5V
Intel Broadwell	V (default)	V
Intel Skylake	V (default)	V

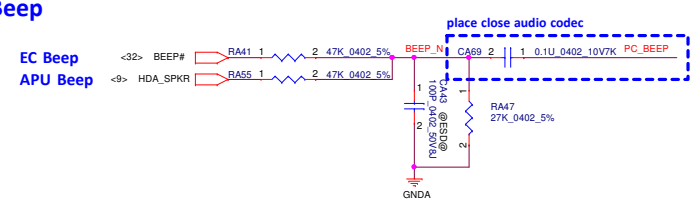
+3VS to +IOVDD_CODEC



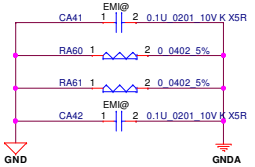
+3VS to +3VDD_CODEC



PC Beep



EMI



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Compal Electronics, Inc.		
Title	HD Audio Codec_ ALC3240	
Size Custom	Document Number LA-E541P	Rev 2.A
Date: Wednesday, June 21, 2017	Sheet 28 of 51	

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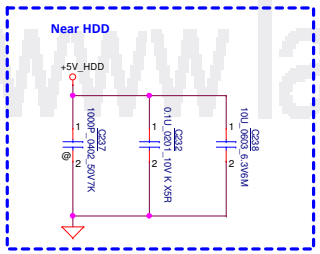
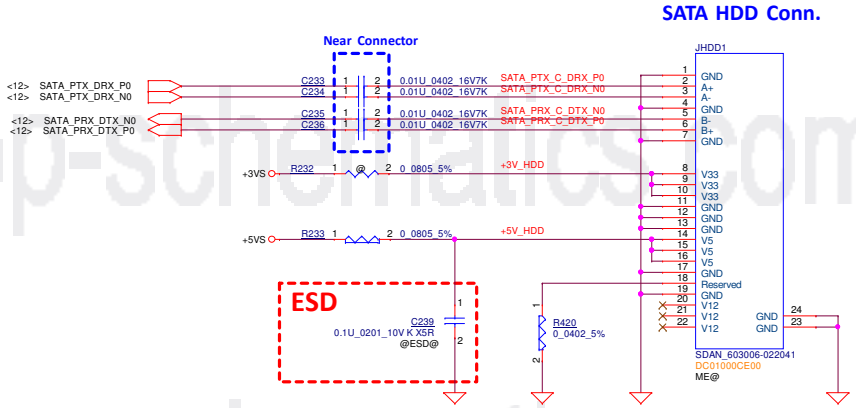
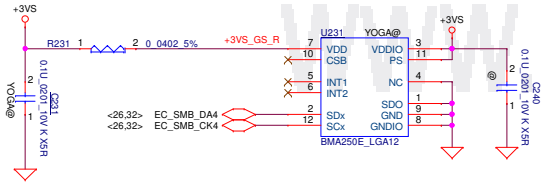
HDD





(G-Sensor for 360-degree reverse)



SMB Address: 0001 1000

Finger Printer

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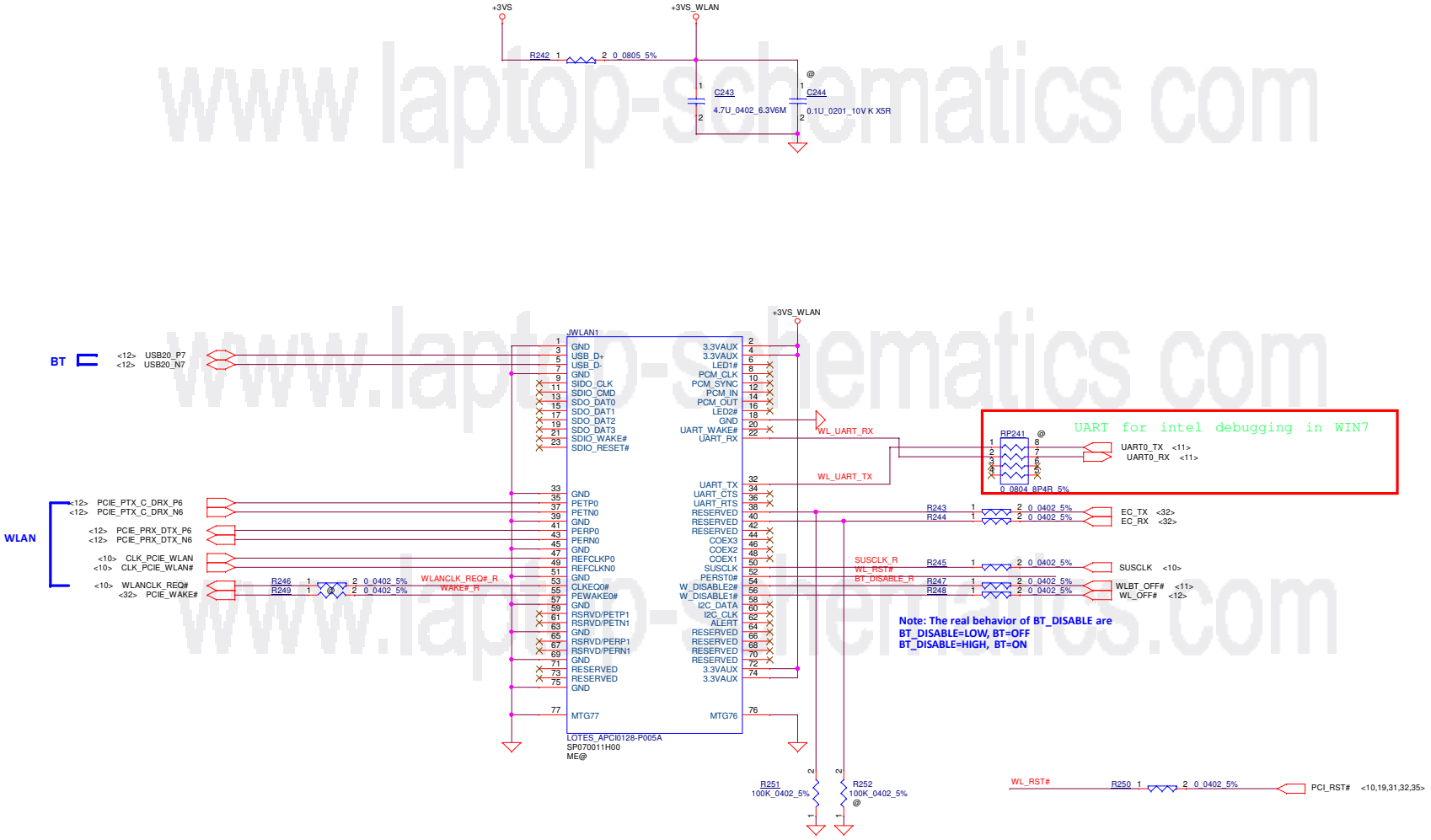
Compal Electronics, Inc.			
Title: HDD/FP/G-Sensor			
Size: Custom	Document Number: LA-E541P		Rev: 2.A
Date: Wednesday, June 21, 2017	Sheet 29 of 51		

NGFF for WLAN / BT (E- KEY)



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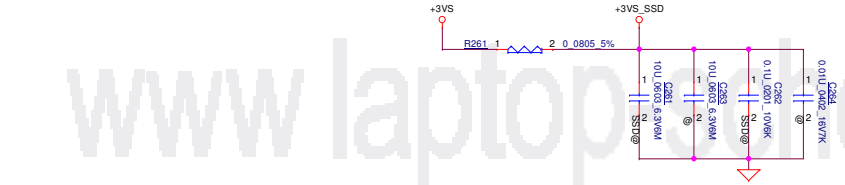
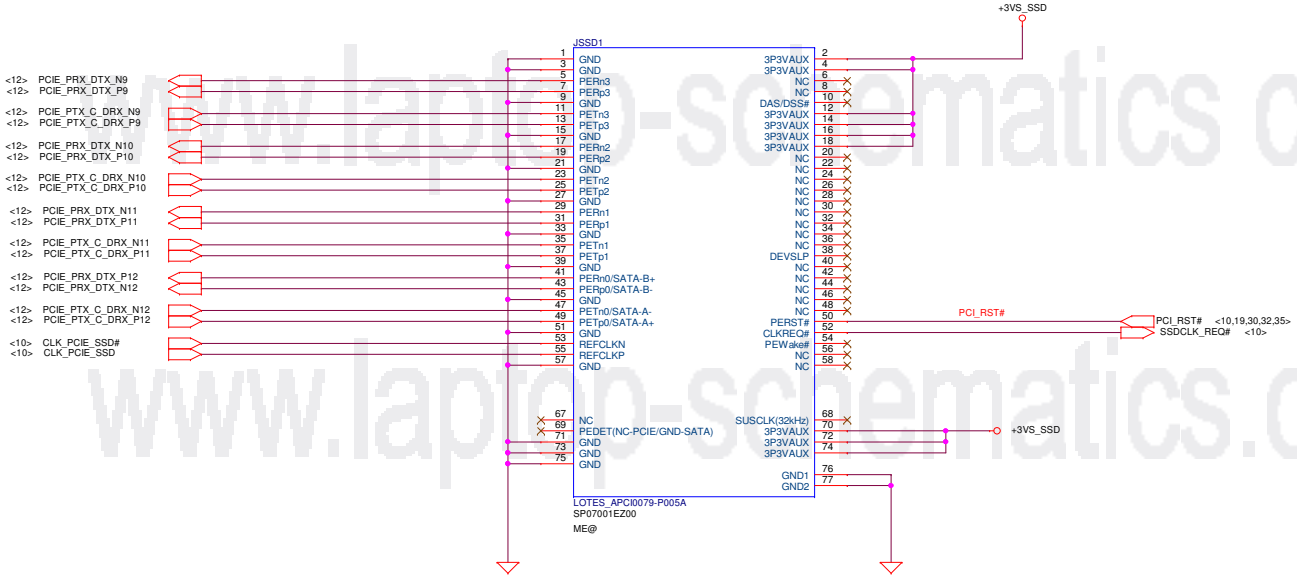
Compal Electronics, Inc.		
Title	NGFF WLAN / BT	
Size	Document Number	Rev
	LA-E541P	2.A
Date: Wednesday, June 21, 2017	Sheet 30 of 51	

NGFF for SSD (M-KEY)





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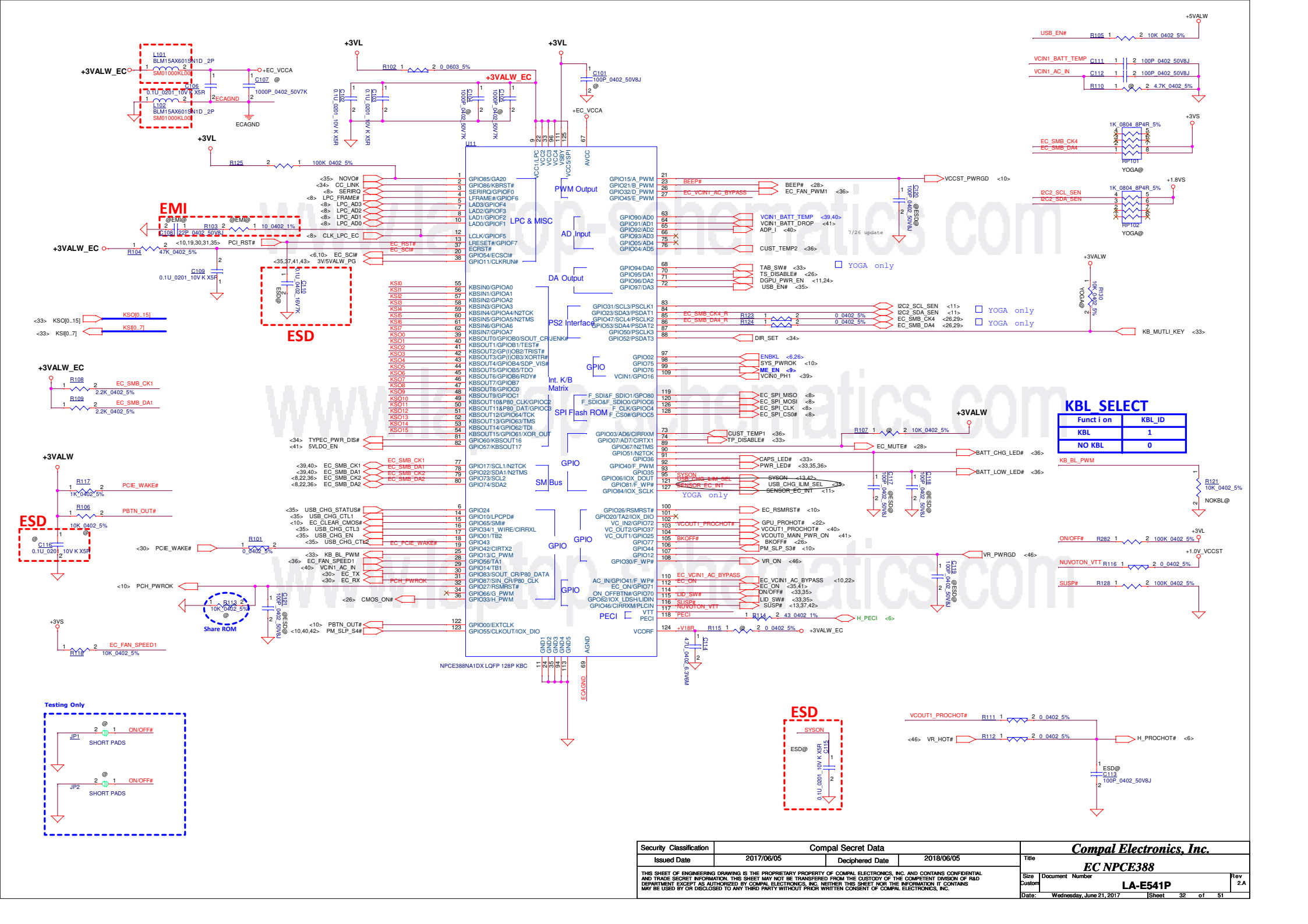
Compal Electronics, Inc.			
Title	NGFF SSD		
Size	Document Number	LA-E541P	Rev 2.A
Date: Wednesday, June 21, 2017	Sheet 31 of 51		


U11
NPCE388NA1DX LQFP 128P KBC
+3VALW_EC
+3VL
+3VALW
+5VALW
+1.8VS
+3VS
+EC_VCCA
ECAGND
EMI
ESD
Share ROM
Testing Only
PWM Output
LPC & MISC
AD_Input
DA Output
PS2 Interface
GPIO
Int. K/B Matrix
SPI Flash ROM
SM Bus
PECI
KBL_SELECT
Funct i on
KBL_ID
KBL
1
NO KBL
0
SHORT PADS
JP1
JP2
ON/OFF#
Compal Secret Data
Issued Date
2017/06/05
Deciphered Date
2018/06/05
Compal Electronics, Inc.
EC NPCE388
LA-E541P
Wednesday, June 21, 2017
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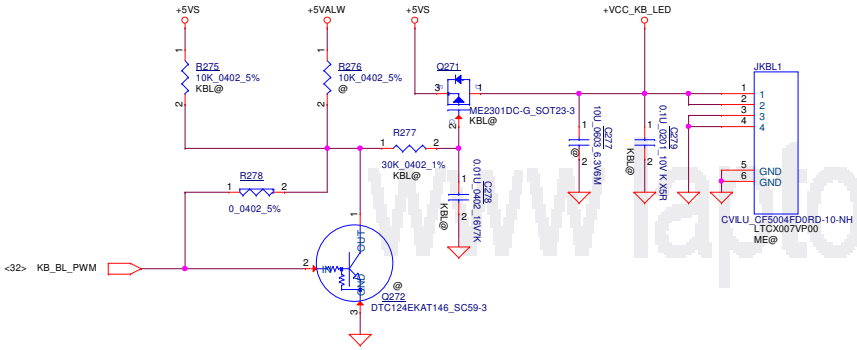
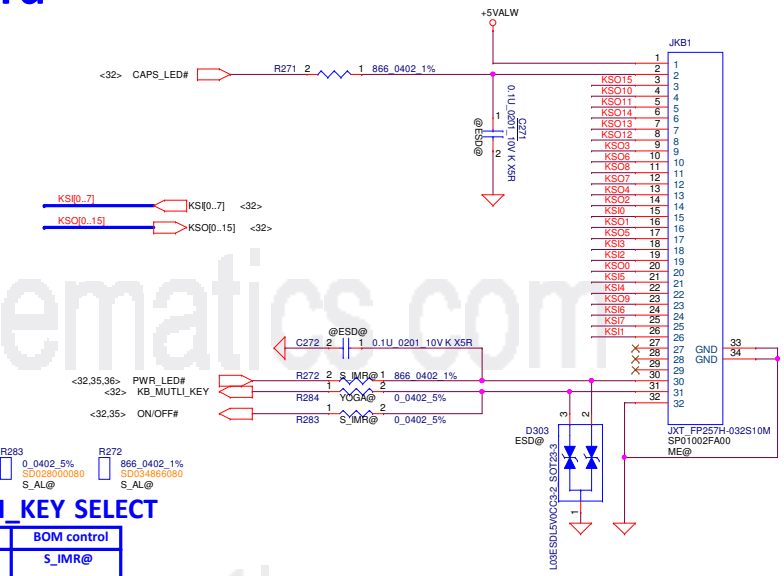
Keyboard Backlight



Keyboard

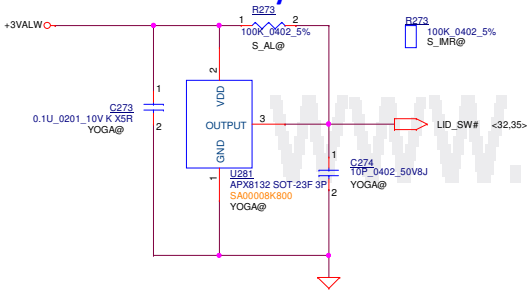


KB_MUTLI_KEY SELECT

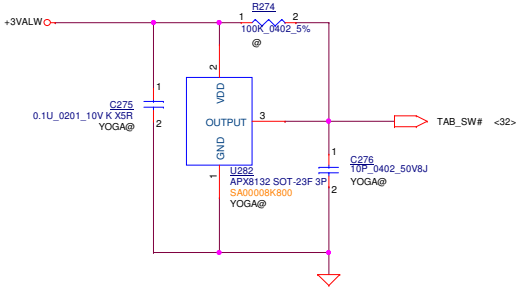
Funct i on	BOM control
Power Key (Cruze)	S_IMR@ S_AL@
Funct i on Key (Alpine)	YOGA@

Hall -Sensor for 0-deg reverse (TOP)

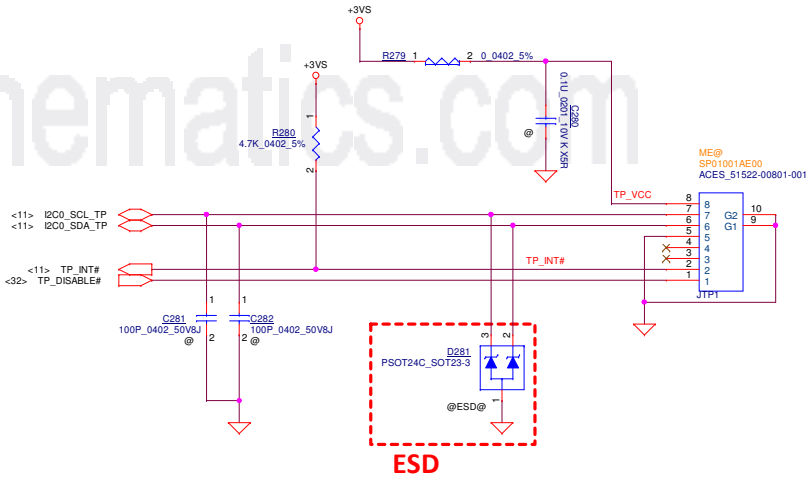
R273 only for 520S



Hall -Sensor for 360-deg reverse (BOT)



Touch Pad



ESD

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Compal Electronics, Inc.

Title: KBL/KBD/Hall Sensor/TP

Size: Custom | Document Number: LA-E541P | Rev: 2.A

Date: Wednesday, June 21, 2017 | Sheet 33 of 51

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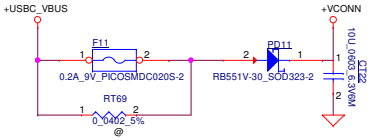
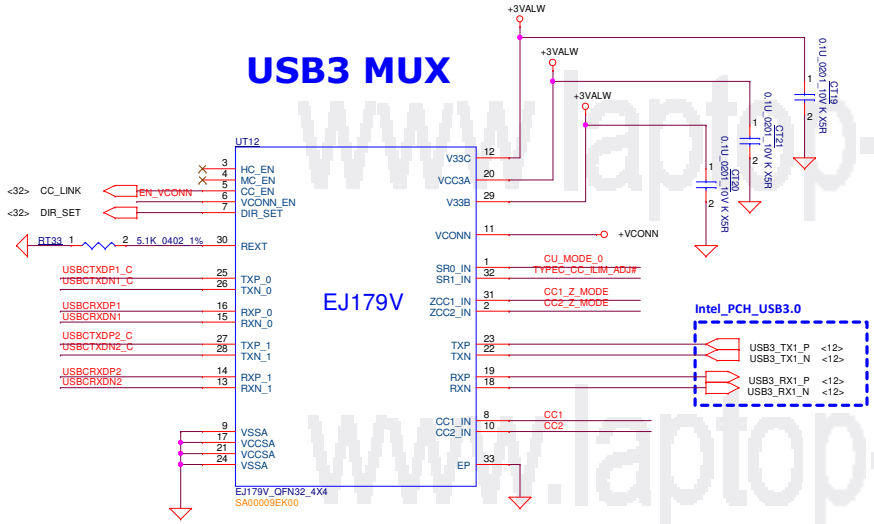
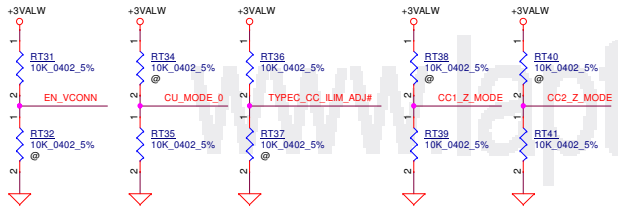
USB Type-C Port



USB3 MUX

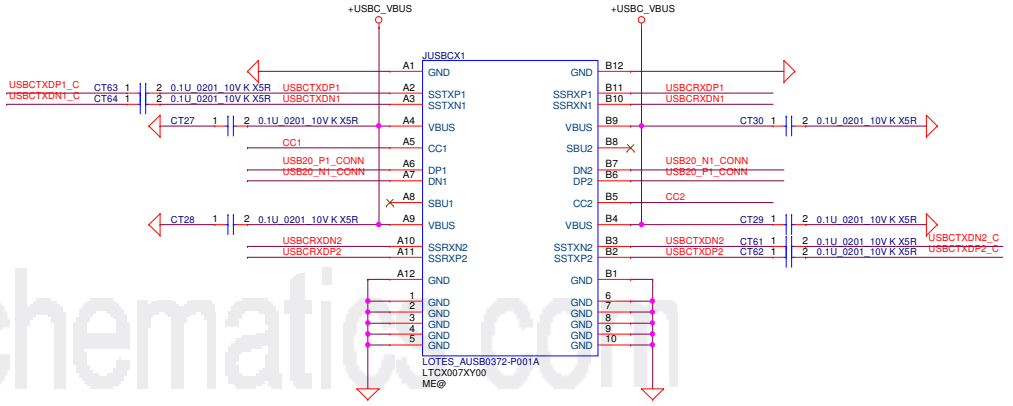




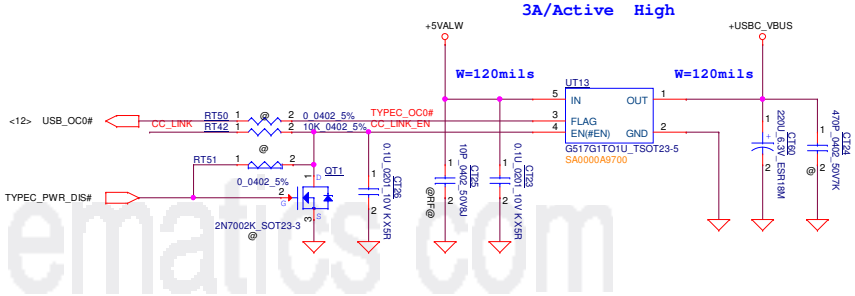
Profile Selection

EN_VCONN	CU_MODE_0	TYPEC_CC_ILIM_ADJ#	CC[1:2]_Z_MODE	CURRNET SELECT
1	0	0	00	DFP 900mA
1	1	0	00	DFP 1.5A
1	0	1	00	DFP 3A
0	1	1	00	UFP
0	X	X	01 10 11	EXTERNAL RESISTER

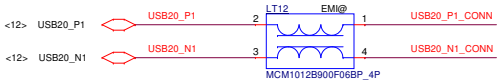
Currently setting



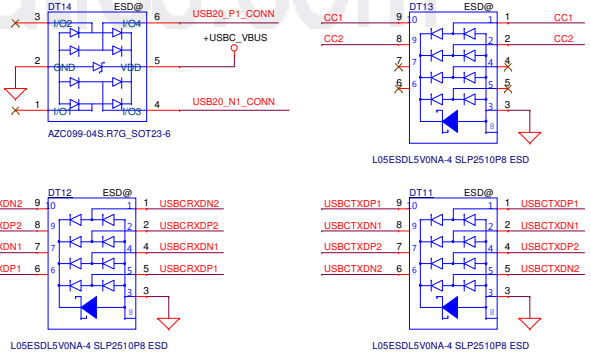
3A/Active High



EMI



ESD



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Compal Electronics, Inc.			
Title: Type-C			
Size: Custom	Document Number: LA-E541P		Rev: 2.A
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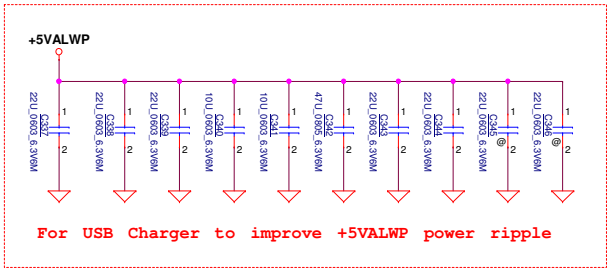
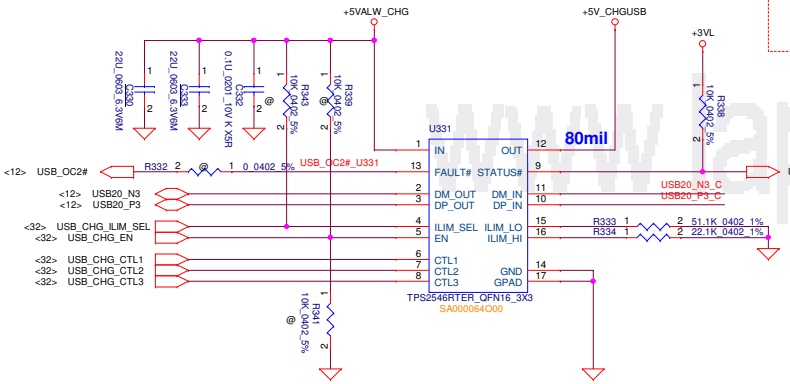
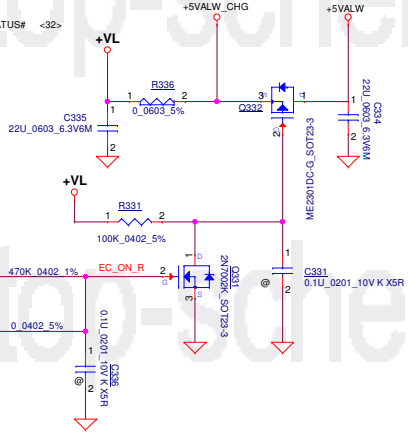
USB Charge

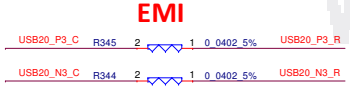


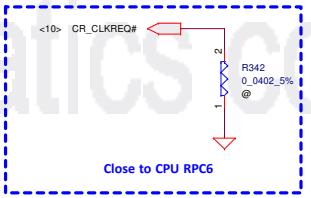




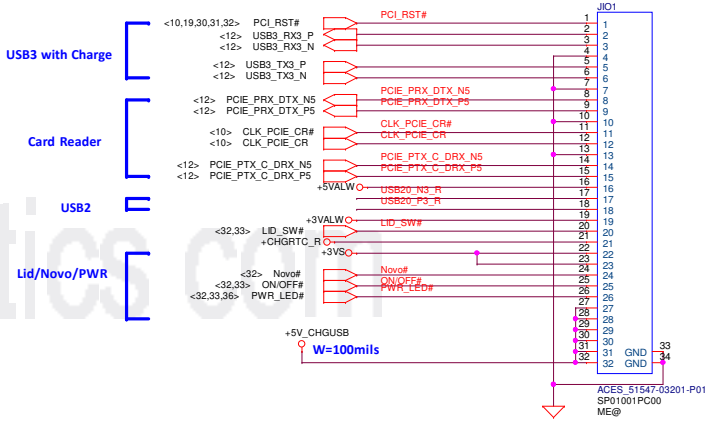
USB Charge switch

EMI



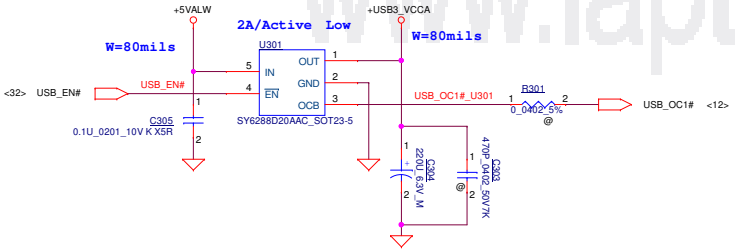


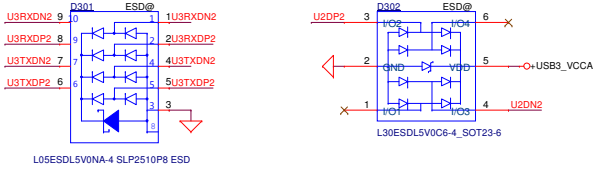
IO CONN

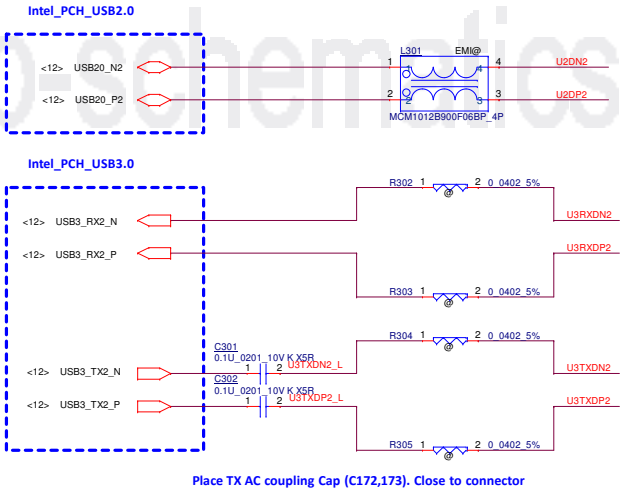


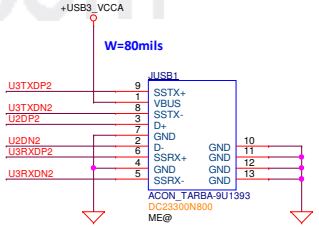
IO/B Function	Alpine	Cruze
USB3.0 w/charge	v	
USB2.0 w/charge		v
Card Reader	v	v
LID SW		v
RTC	v	v
PWR PTN	v	
NOVO BTN	v	v
PWR LED	v	

USB3.0_Port









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Title	USB2 / USB3 / FP / IO Board		
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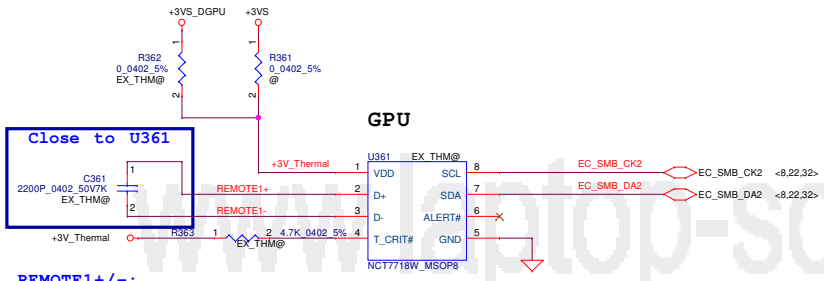
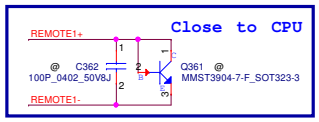
Thermal Sensor

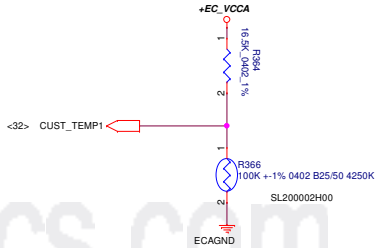


REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"

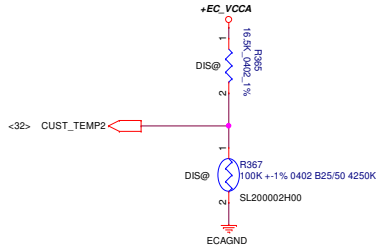
SMB Address: 1001100x



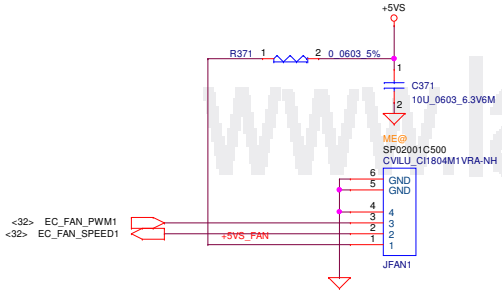
DDR



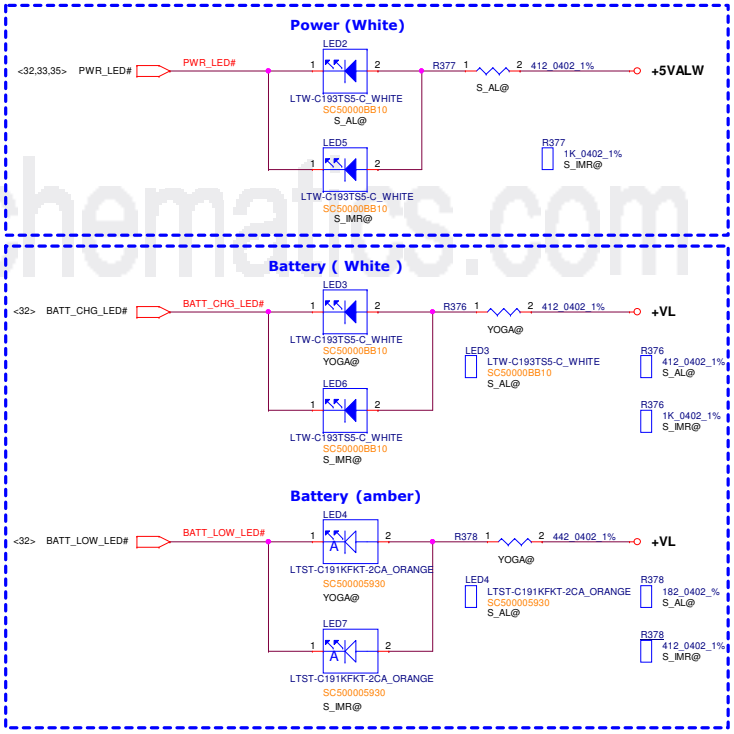
VRAM



FAN



Power LED & Battery LED



		Power (White) LED / Res.		Battery(White) LED / Res.		Battery(amber) LED / Res.	
TOP	YOGA (YOGA@)	IO Board		LED3	R376 412 Ω	LED4	R378 442 Ω
TOP	S series (S_AL@)	LED2	R377 412 Ω	LED3	R376 412 Ω	LED4	R378 182 Ω
BOT	S IMR (S_IMR@)	LED5	R377 1K Ω	LED6	R376 1K Ω	LED7	R378 412 Ω

Security Classification	Compal Secret Data		
Issued Date	2017/06/05	Deciphered Date	2018/06/05

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Compal Electronics, Inc.

Title: FAN / LED / Thermal Senser

Size	Document Number	Rev
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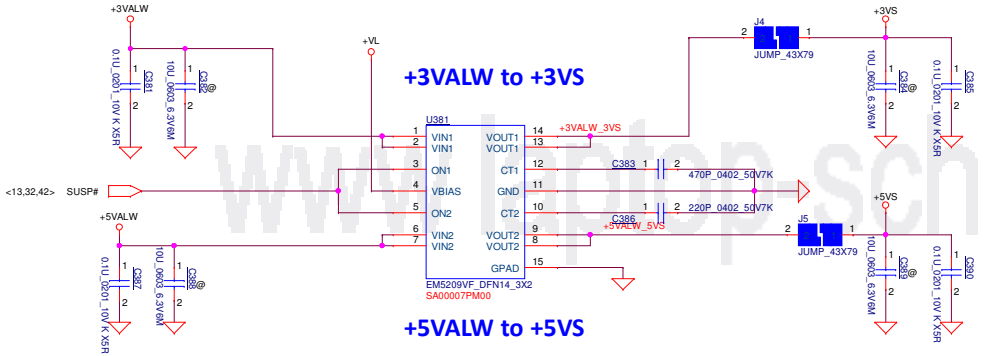
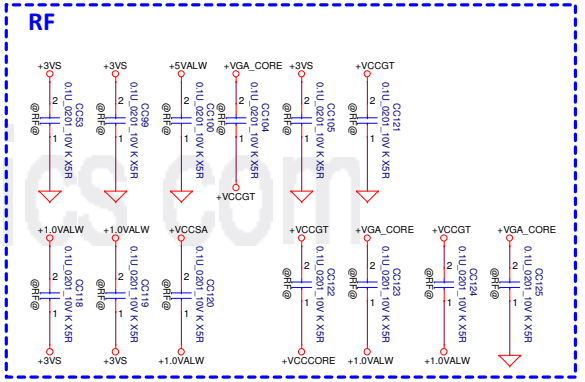
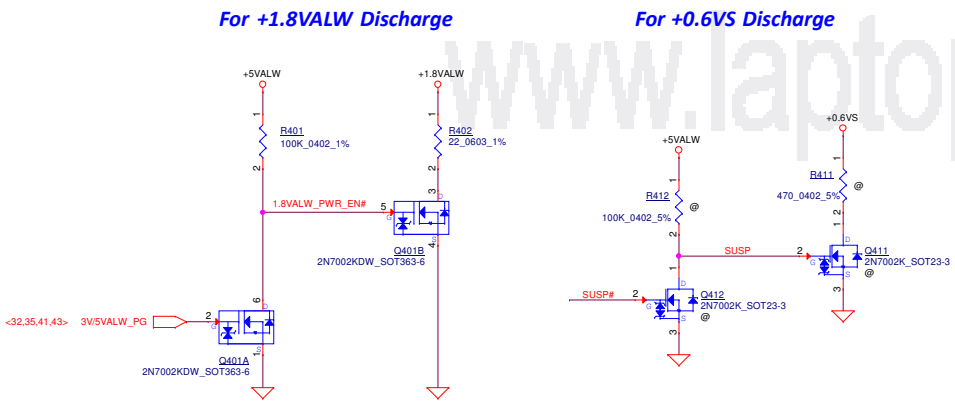
DC to DC

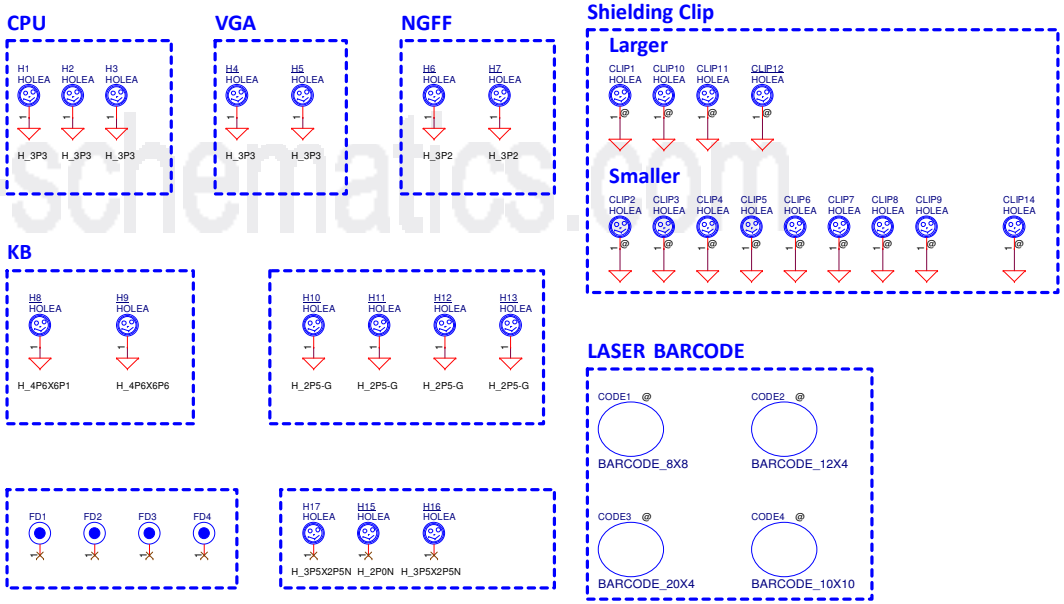




Discharge



Screw Hold



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Issued Date	2017/06/05	Deciphered Date 2018/06/05	Title: DC to DC
			Size: Custom; Document Number: LA-E541P; Rev: 2.A
			Date: Wednesday, June 21, 2017; Sheet 37 of 51

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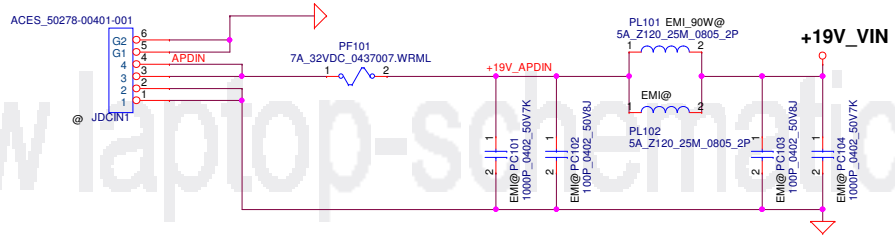

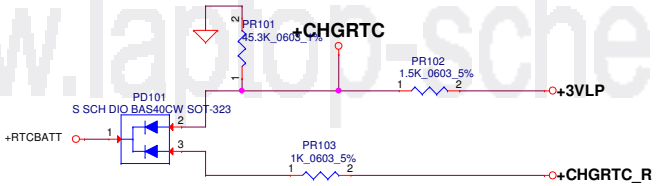

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Compal Electronics, Inc.

Title: **PWR- DCIN / Vin Detector**

Size	Document Number	
Custom	KBL	
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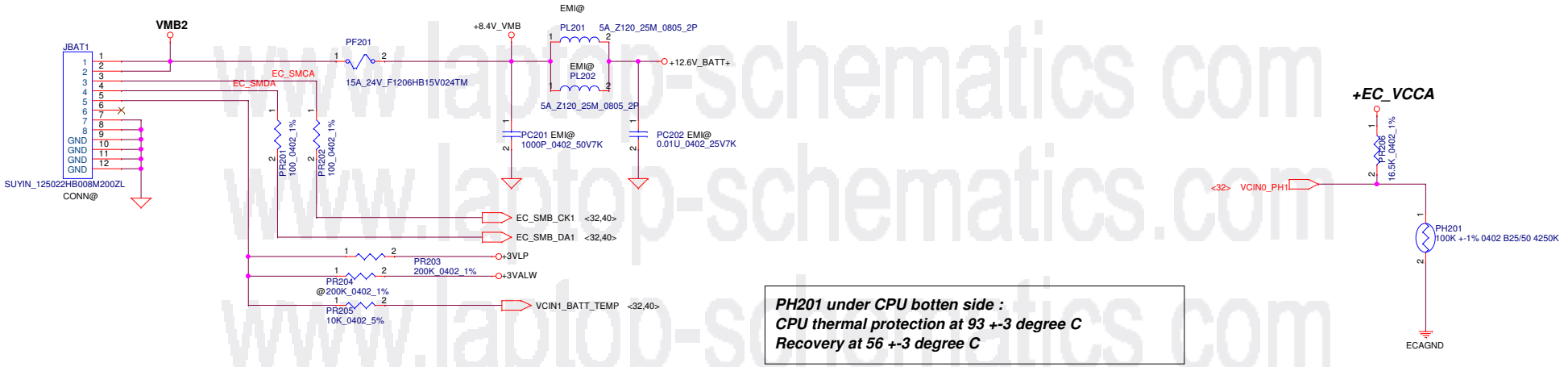

PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

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Compal Electronics, Inc.

Title: **PWR- BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	KBL	2.A

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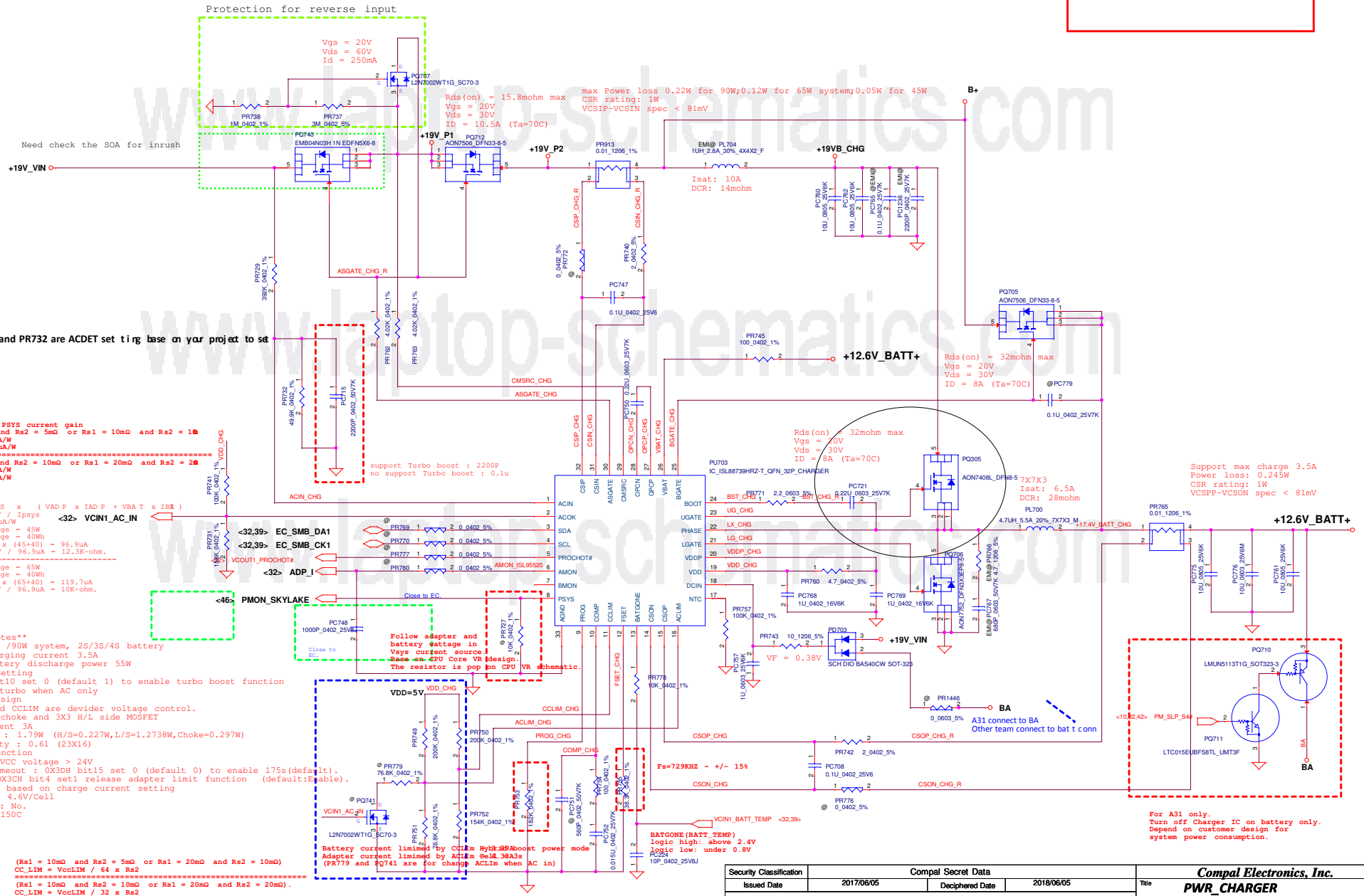
Module model information

ISL95520_Hybrid_Boost_V2.mdd



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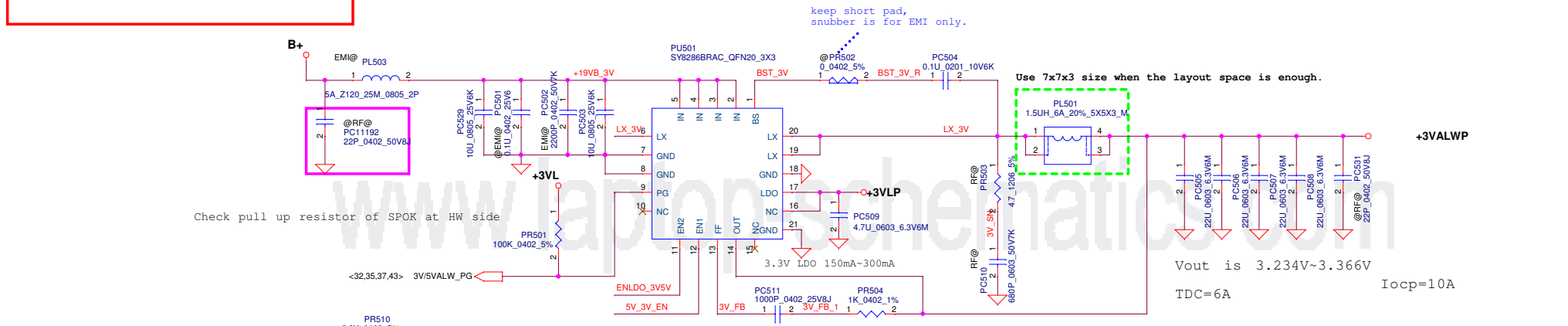
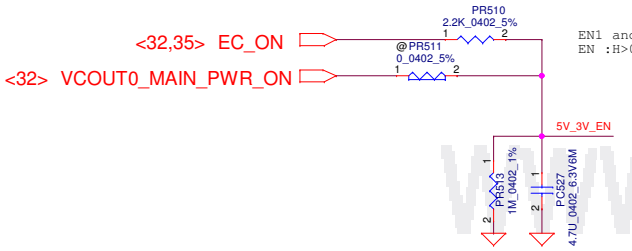
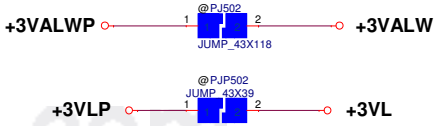
Compal Electronics, Inc.	
Title	PWR_CHARGER
Size	Document Number: KBL
Rev	2.A
Date:	Wednesday, June 21, 2017
Sheet	40 of 51

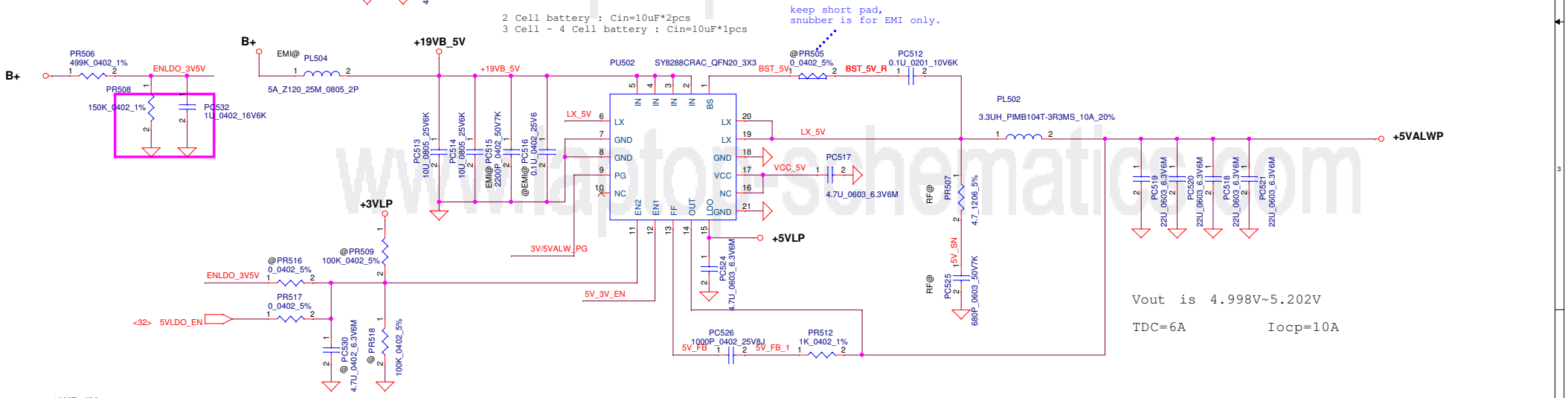
Module model information

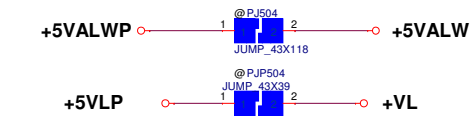
SY8286B_V3_single.mdd
SY8286B_V3_dual.mdd

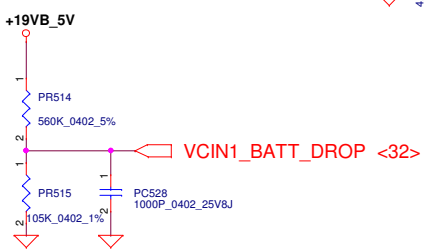












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Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size	Document Number	Rev
Custom	KBL	2.A

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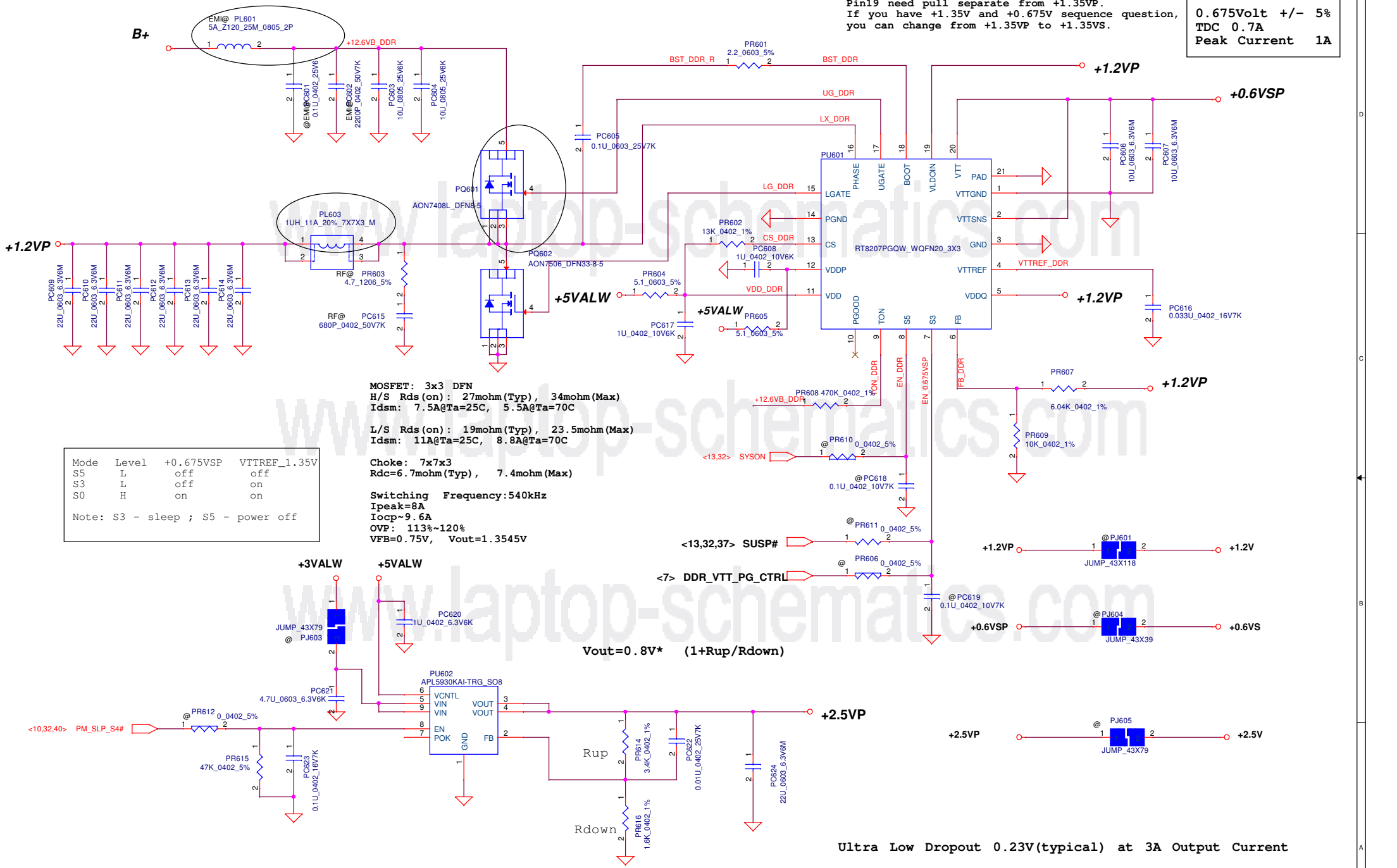

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Issued Date	2017/06/05	Deciphered Date	2018/06/05

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Compal Electronics, Inc.

Title: RT8207P

Size: Custom | Document Number: KBL | Rev: 2.A

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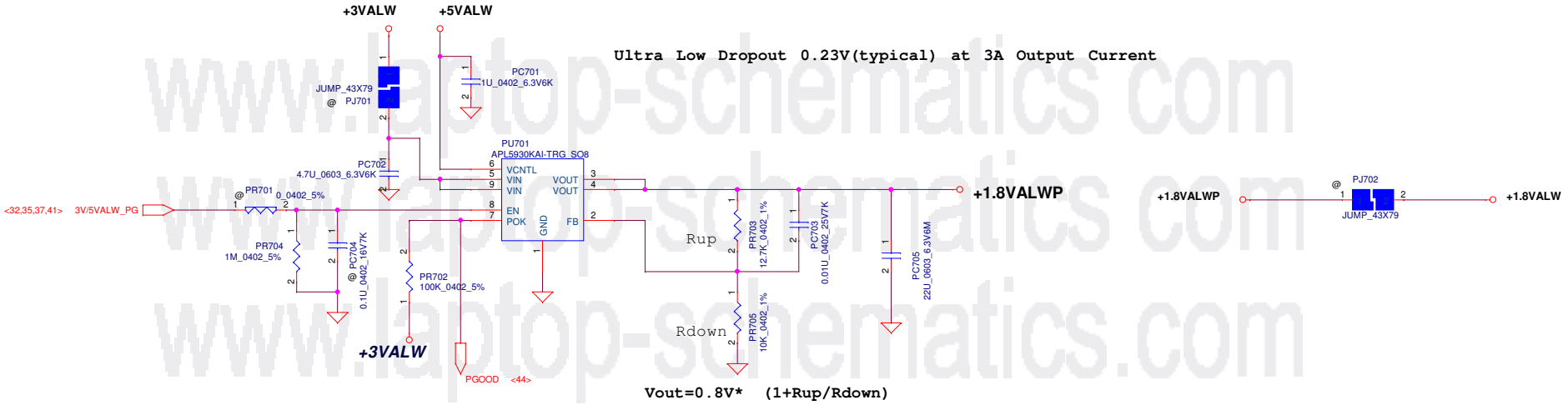
Module model information

APL5930_V2.mdd



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Compal Electronics, Inc.

Title: APL5930

Size	Document Number	Rev
Custom	KBL	2.A

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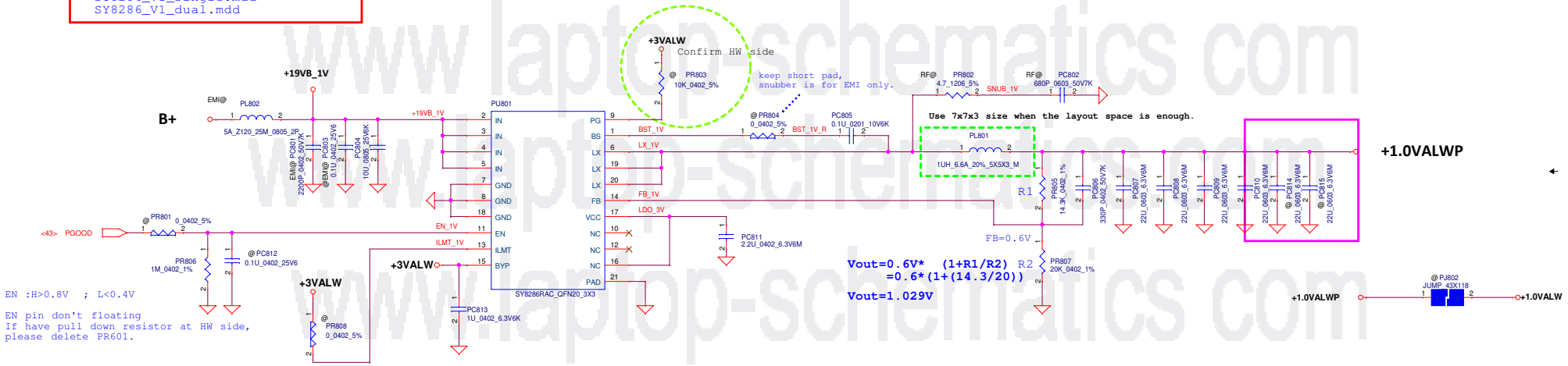
Module model information

SY8286_V1_single.mdd
SY8286_V1_dual.mdd



EN :H>0.8V ; L<0.4V

EN pin don't floating
If have pull down resistor at HW side,
please delete PR601.

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

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Issued Date	2017/06/05	Deciphered Date	2018/06/05

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Compal Electronics, Inc.

Title: SY8286

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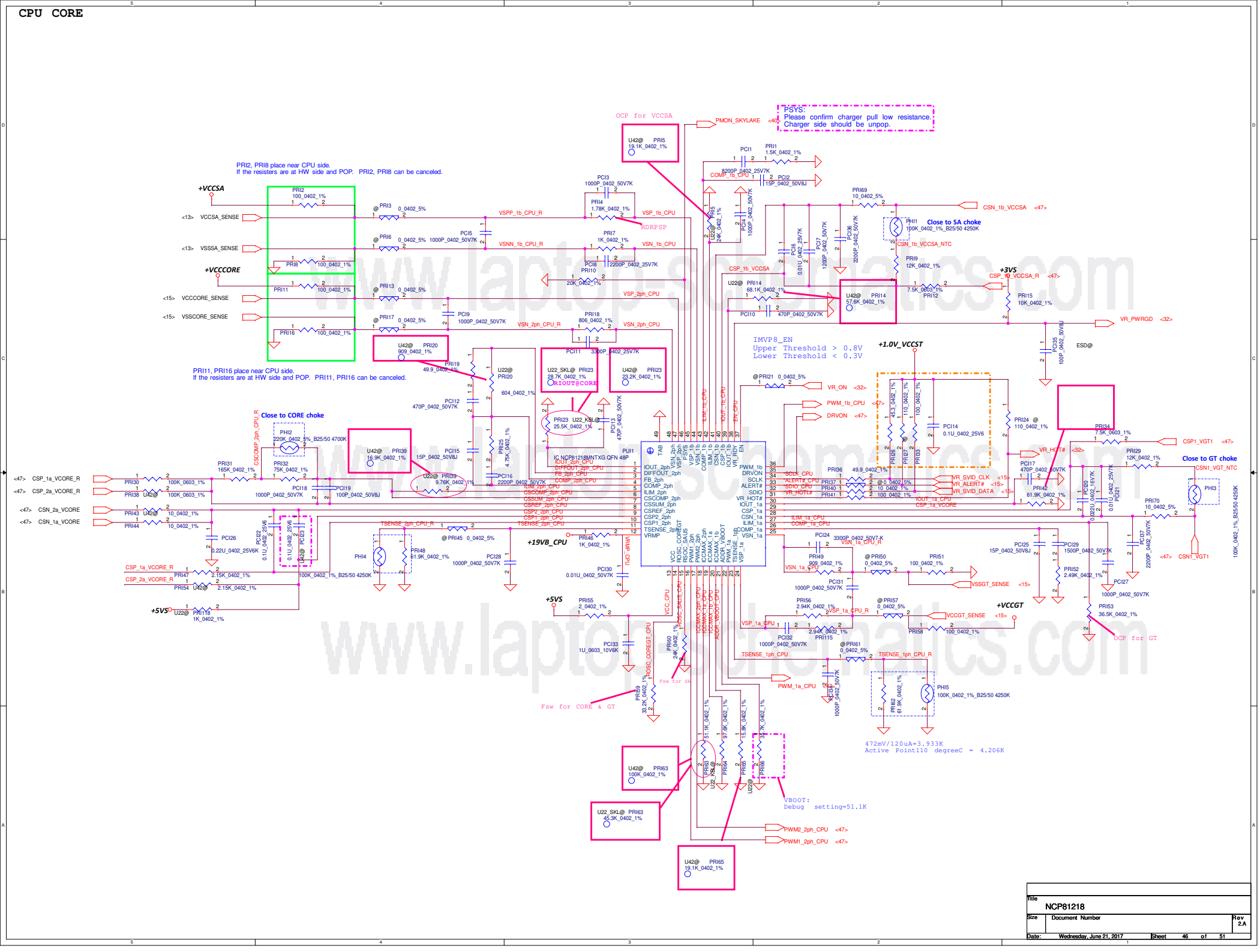
CPU CORE


PSYS:
Please confirm charger pull low resistance.
Charger side should be unpop.
PRI2, PRI8 place near CPU side.
If the resisters are at HW side and POP. PRI2, PRI8 can be canceled.
PRI11, PRI16 place near CPU side.
If the resisters are at HW side and POP. PRI11, PRI16 can be canceled.
IMVP8_EN
Upper Threshold > 0.8V
Lower Threshold < 0.3V
472mV/120uA=3.933K
Active Point110 degreeC = 4.206K
VBOOT:
Debug setting=51.1K
Close to SA choke
Close to CORE choke
Close to GT choke
OCP for VCCSA
OCP for GT
Fsw for CORE & GT
Fsw for SA
+VCCSA
+VCCCORE
+1.0V_VCCST
+3VS
+5VS
+19VB_CPU
+VCCGT
NCP81218
Title
Size
Document Number
Rev 2.A
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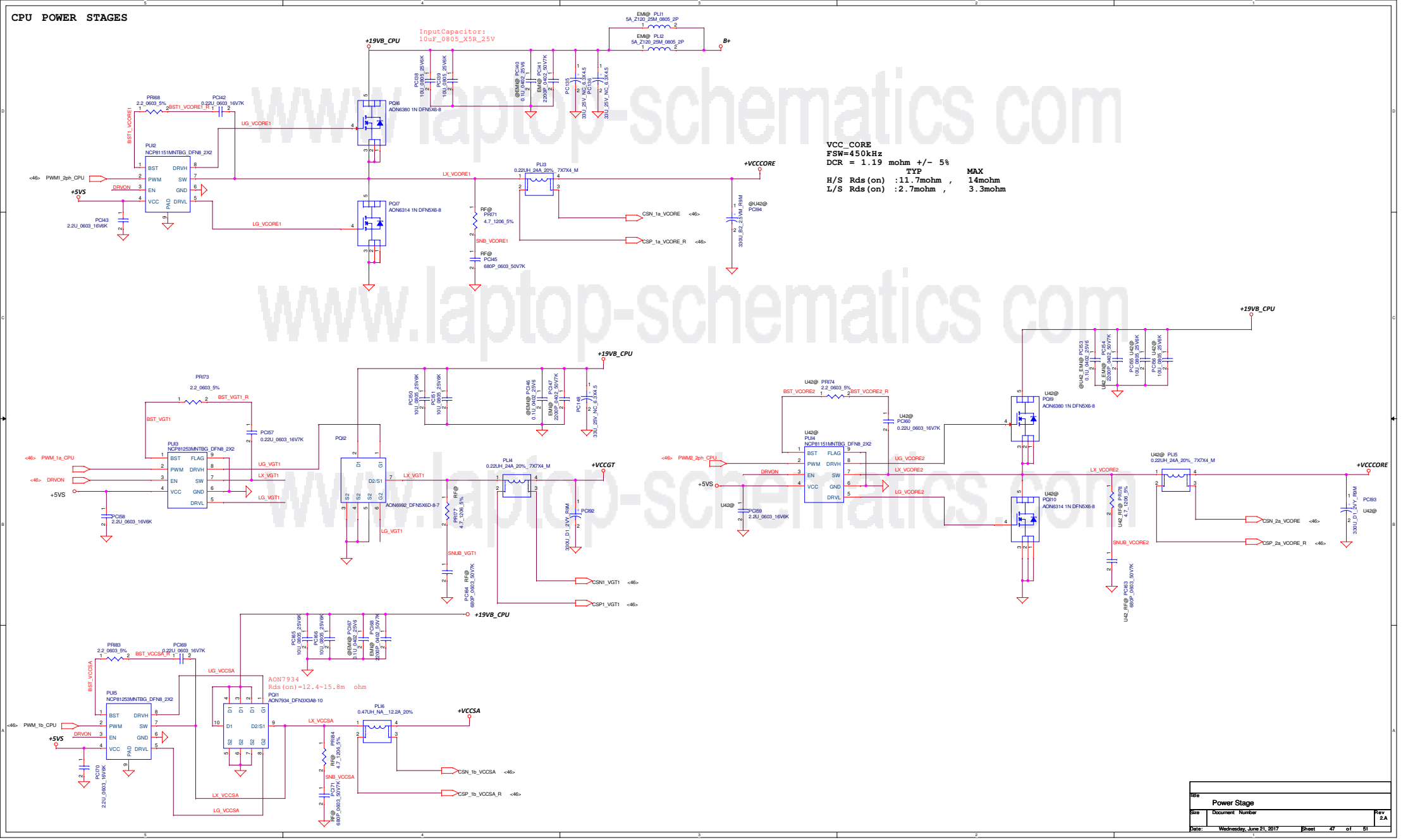
CPU POWER STAGES



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Title	Power Stage
Size	Document Number: Rev 2A
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VCC_CORE Place on CPU Back Side @ V09
22U_0603 * 36pcs +1U_0201*35 pcs

VCC_GT Place on CPU Back Side @ V09
22U_0603 * 32 pcs +1U_0201*12 pcs

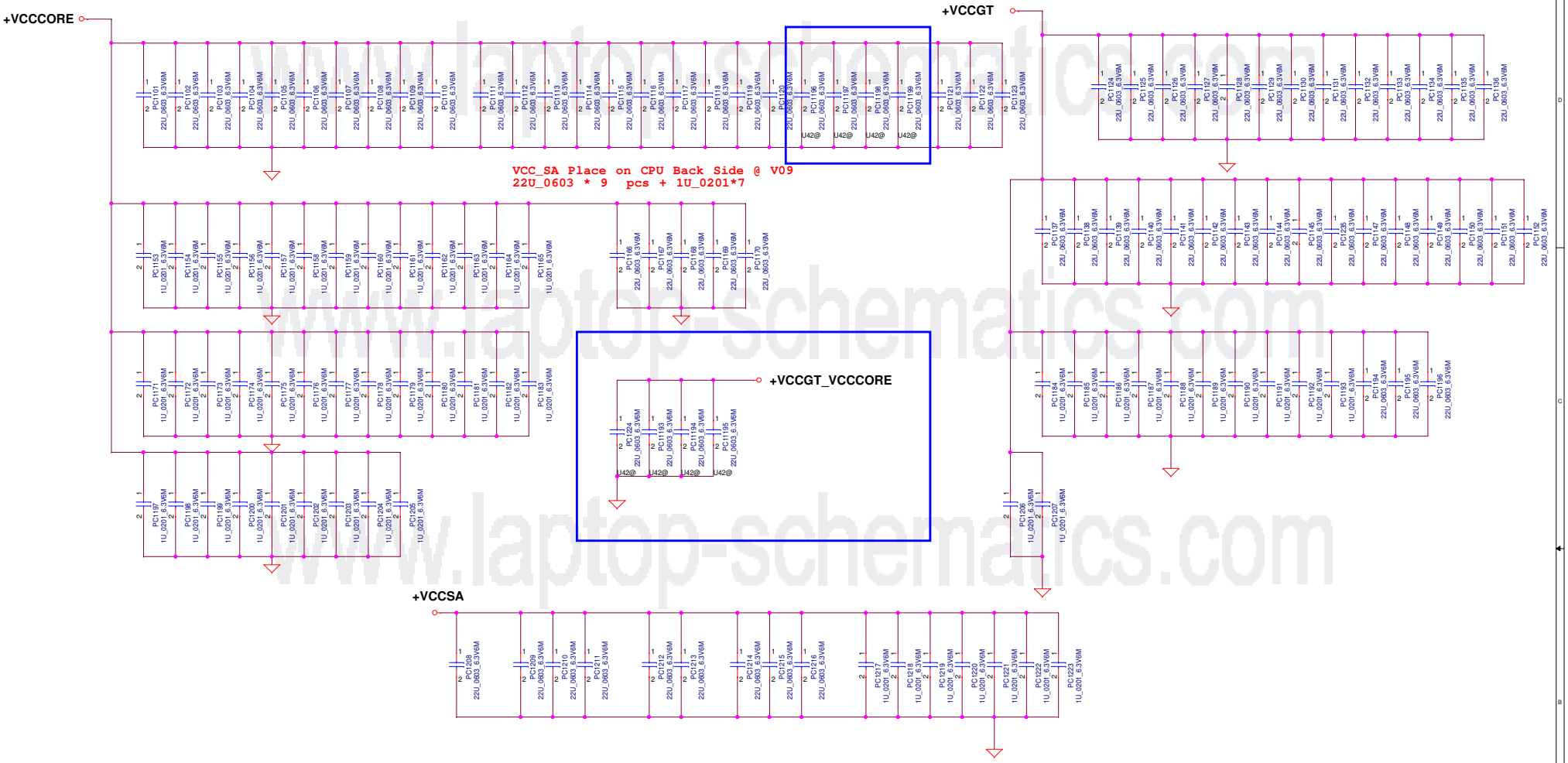
VCC_SA Place on CPU Back Side @ V09
22U_0603 * 9 pcs + 1U_0201*7

+VCCCORE

+VCCGT

+VCCGT_VCCCORE

+VCCSA



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Title: PWR-PROCESSOR_DECOUPLING

Size	Document Number	Rev
C	KBL	2.A

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3.PWM-VID Spec and component Values

PWM-VID Spec		Config A	Config B	Config C
Vmin		0.6V	0.6V	0.65V
Vmax		1.2V	1.2V	1.15V
Vboot		0.875V	0.9V	0.9V
Voltage step		6.25mV	6.25mV	25mV
N of Voltage level		96	96	20
Rrefadj	PR8	39K	20K	39K
Rref1	PR7	39K	20K	30K
Rboot	PR10	1.5K	2K	3K
Rref2=PR20+PR21	PR20	30K	18K	24K
	PR21	1.5K	0	3K
C	PC9	1.5nf	2.7nf	1.8nf

Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

Module model information:
RT8812A-2P_V1A.mdd for IC portion
RT8812A-2P_V1B.mdd for SW portion

PSI Pull high on HW side
Pull high on HW side
EN High Threshold = 1.6V
Rref1
Rboot
Rrefadj
Rref2
C
Rset
Rton
RT8812AGQW_WQFN20_3X3
+VGA_CORE
+5VS
+3VS
+3VALW
B+
B+_1.35V
+1.35VGSP
+1.35VS_VRAM
SY8286RAC_QFN20_3X3
AON6992_DFN5X6D-8-7
Confirm HW side
keep short pad, snubber is for EMI only.
Use 7x7x3 size when the layout space is enough.
Vout=0.6V* (1+R1/R2) R2
=0.6*(1+(12.4/10))
Vout=1.344V
FB=0.6V
+VGA_CORE
EDP-Continuous 26.5A
EDP-Peak 53A
OCP min 66.4A
Near GPU Core
Under GPU Core
GB4-128 package
LDO_3V_1.35V
EN :H>0.8V ; L<0.4V
EN pin don't floating
If have pull down resistor at HW side, please delete PR601.
The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

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Title: PWR-CPU_GFX

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