# Compal confidential
# BAP00 schematic document

## Sky Lake-H paltform with nVIDIA N17E-G1
## Kaby Lake-H paltform with nVIDIA N17E-G1
## Kaby Lake-H paltform with nVIDIA N17P-G0-B/N17P-G1-B
## Rev: 1.0(A00) PVT
## 2016/09/05(BOM 2016/09/06)

**@ : Nopop component**
**EMI@ / @EMI@ : EMI pop / unpop part**
**ESD@ / @ESD@ : ESD pop / unpop part**
**RF@ / @RF@ : RF pop / unpop part**
**CONN@ : Connector component**
**CMC@ : CMC debug**
**TBT@ : Thunderbolt**
**PD@ : Thunderbolt PD**
**SKL@ : Sky lake CPU**
**KBL@ : Kaby lake CPU**
**N17E@ : N17E-G1**
**N17P@ : N17P-G1-B / N17P-G0-B**

PR8211 34.8K_0402_1% SAMSUNG@
PR8211 30K_0402_1% MICRON@

PR8215 52.3K_0402_1% SAMSUNG@
PR8215 68.1K_0402_1% MICRON@

DAX PCB DAZ18F00100 PCB 18F LA-B752P REV0 M/B 8 R1@
DAX PCB DAZ18F00101 PCB 18F LA-B752P REV0 M/B 8 R3@



| | | | |
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Title: *Cover sheet*

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| Custom | *LA-D581P* | 0.4 |

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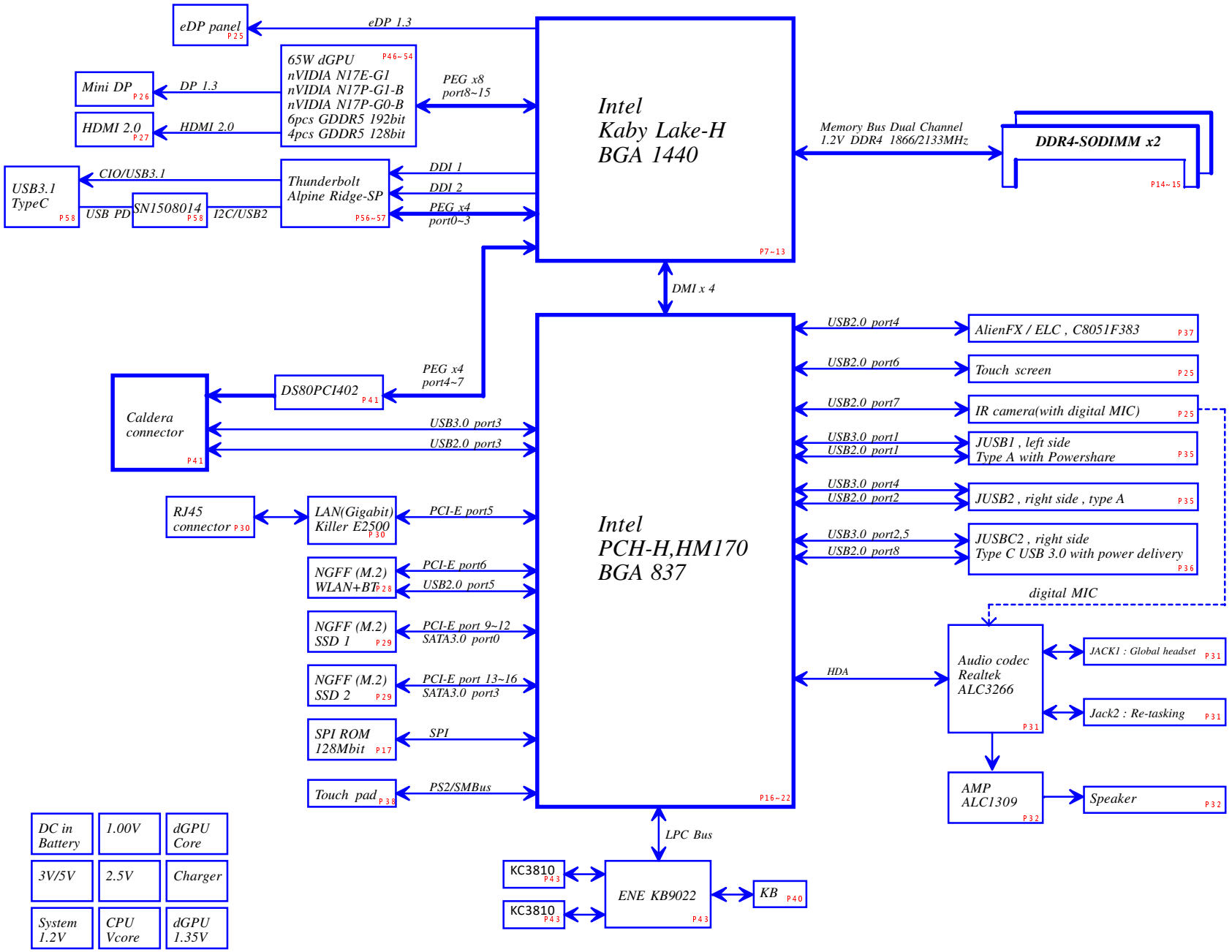
# Block Diagram

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Title: **Block diagram**

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## Board ID Table for AD channel

| Vcc | 3.3V +/- 1% |
|---|---|
| Ra | 100K +/- 1% |

| Board ID | Rb | $V_{AD\_BID}$ min | $V_{AD\_BID}$ typ | $V_{AD\_BID}$ max | EC AD3 |
|---|---|---|---|---|---|
| 0 | 0 | 0.000V | 0.000V | 0.300V | 0x00 - 0x13 |
| 1 | 12K +/- 1% | 0.347V | 0.354V | 0.360V | 0x14 - 0x1E |
| 2 | 15K +/- 1% | 0.423V | 0.430V | 0.438V | 0x1F - 0x25 |
| 3 | 20K +/- 1% | 0.541V | 0.550V | 0.559V | 0x26 - 0x30 |
| 4 | 27K +/- 1% | 0.691V | 0.702V | 0.713V | 0x31 - 0x3A |
| 5 | 33K +/- 1% | 0.807V | 0.819V | 0.831V | 0x3B - 0x45 |
| 6 | 43K +/- 1% | 0.978V | 0.992V | 1.006V | 0x46 - 0x54 |
| 7 | 56K +/- 1% | 1.169V | 1.185V | 1.200V | 0x55 - 0x64 |
| 8 | 75K +/- 1% | 1.398V | 1.414V | 1.430V | 0x65 - 0x76 |
| 9 | 100K +/- 1% | 1.634V | 1.650V | 1.667V | 0x77 - 0x87 |
| 10 | 130K +/- 1% | 1.849V | 1.865V | 1.881V | 0x88 - 0x96 |
| 11 | 160K +/- 1% | 2.015V | 2.031V | 2.046V | 0x97 - 0xA4 |
| 12 | 200K +/- 1% | 2.185V | 2.200V | 2.215V | 0xA45- 0xAF |
| 13 | 240K +/- 1% | 2.316V | 2.329V | 2.343V | 0xB0 - 0xB7 |
| 14 | 270K +/- 1% | 2.395V | 2.408V | 2.421V | 0xB8 - 0xBF |
| 15 | 330K +/- 1% | 2.521V | 2.533V | 2.544V | 0xC0 - 0xC9 |
| 16 | 430K +/- 1% | 2.667V | 2.677V | 2.687V | 0xCA - 0xD4 |
| 17 | 560K +/- 1% | 2.791V | 2.800V | 2.808V | 0xD5 - 0xDD |
| 18 | 750K +/- 1% | 2.905V | 2.912V | 2.919V | 0xDE - 0xF0 |
| 19 | NC | 3.000V | 3.300V | 3.300V | 0xF1 - 0xFF |

## Voltage Rails

| Power Plane | Description | S0 | S3 | S4 / S5 |
|---|---|---|---|---|
| VIN | Adapter power supply | N/A | N/A | N/A |
| BATT+ | Battery power supply | N/A | N/A | N/A |
| B+ | AC or battery power rail for power circuit | N/A | N/A | N/A |
| +VCC_CORE | Core voltage for CPU | ON | OFF | OFF |
| +VCCGT | Sliced graphics power rail | ON | OFF | OFF |
| +0.6VS | DDR4 +0.6VS power rail for DDR terminator | ON | OFF | OFF |
| +1VALW | System +1VALW power rail | ON | ON | ON* |
| +1V_PCH_PRIM | System +1VALW power rail | ON | ON | ON* |
| +VCCIO | +1.0VS IO power rail | ON | OFF | OFF |
| +PEX_VDD | +1.0VS power rail for GPU | ON | OFF | OFF |
| +1.35VS_VGA | +1.35~1.55VS power rail for GPU | ON | OFF | OFF |
| +1.2V_DDR | DDR4 +1.2V power rail | ON | ON | OFF |
| +VCCST | +1.0V power rail for CPU | ON | ON | OFF |
| +VCCSTG | +1.0VS power rail for CPU | ON | OFF | OFF |
| +3VALW | System +3VALW always on power rail | ON | ON | ON* |
| +3VLP | +19VB to +3VLP power rail for suspend power | ON | ON | ON |
| +3V_PCH | +3VALW power for PCH DSW rails | ON | ON | ON* |
| +LAN_IO | +3VALW power for LAN power rails | ON | ON | ON* |
| +3VS | System +3VS power rail | ON | OFF | OFF |
| +1V8_AON | +1.8VS power rail for GPU | ON | OFF | OFF |
| +3V3_SYS | +3VS power rail for GPU | ON | OFF | OFF |
| +5VALW | System +5VALW power rail | ON | ON | ON* |
| +5VS | System +5VS power rail | ON | OFF | OFF |
| +RTC_CELL | RTC power | ON | ON | ON |
| +VCCSA | System Agent power rail | ON | OFF | OFF |
| Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF | | | | |

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## PCH-H , HM170

| HSIO | USB3 | PCIe | SATA3 | Function |
|---|---|---|---|---|
| 1 | 1 | | | JUSB1,type A |
| 2 | 2 | | | JUSB3,type C |
| 3 | 3 | | | Caldera |
| 4 | 4 | | | JUSB2,type A |
| 5 | 5 | | | JUSB3,type C |
| 6 | 6 | | | |
| 7 | 7 | 1 | | |
| 8 | 8 | 2 | | |
| 9 | 9 | 3 | | |
| 10 | 10 | 4 | | |
| 11 | | 5 | | LAN |
| 12 | | 6 | | WLAN |
| 13 | | 7 | | |
| 14 | | 8 | | |
| 15 | | 9 | 0 | JSSD1 M.2 2280 SATA PCIe x4 |
| 16 | | 10 | 1 | |
| 17 | | 11 | | |
| 18 | | 12 | | |
| 19 | | 13 | 0 | JSSD2 M.2 2280 SATA PCIe x4 |
| 20 | | 14 | 1 | |
| 21 | | 15 | 2 | |
| 22 | | 16 | 3 | |

| USB2 | Function |
|---|---|
| 1 | JUSB1(Powershare) |
| 2 | JUSB2 |
| 3 | Caldera |
| 4 | ELC |
| 5 | Bluetooth |
| 6 | Touch screen |
| 7 | Camera |
| 8 | JUSB3 |
| 9 | |
| 10 | |
| 11 | |
| 12 | |
| 13 | |
| 14 | |

## Board ID TABLE

| ID | SKL | KBL |
|---|---|---|
| 0 | EVT | |
| 1 | DVT1 | EVT |
| 2 | DVT1.1 | |
| 3 | DVT2 | |
| 4 | GC6 | |
| 5 | MP | |
| 6 | | DVT1 |
| 7 | | DVT2 |
| 8 | | DVT2.1/GC6 |
| 9 | | MP |

| Part No. | Name | BOM |
|---|---|---|
| 431A3131L01 | SKL I5 G1 DIS 6G | SKL@, N17E@ ,TBT@, PD@, CMC@, EMI@, ESD@, RF@, CONN@ |
| 431A3131L02 | SKL I7 G1 DIS 6G | SKL@, N17E@ ,TBT@, PD@, CMC@, EMI@, ESD@, RF@, CONN@ |
| 431A3131L03 | KBL I5 G1 DIS | KBL@, N17E@ ,TBT@, PD@, CMC@, EMI@, ESD@, RF@, CONN@ |
| 431A3131L04 | KBL I7 G1 DIS | KBL@, N17E@ ,TBT@, PD@, CMC@, EMI@, ESD@, RF@, CONN@ |
| | | |

*Symbol Note :*

*Digital Ground*

*Analog Ground*

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Title: Notes list

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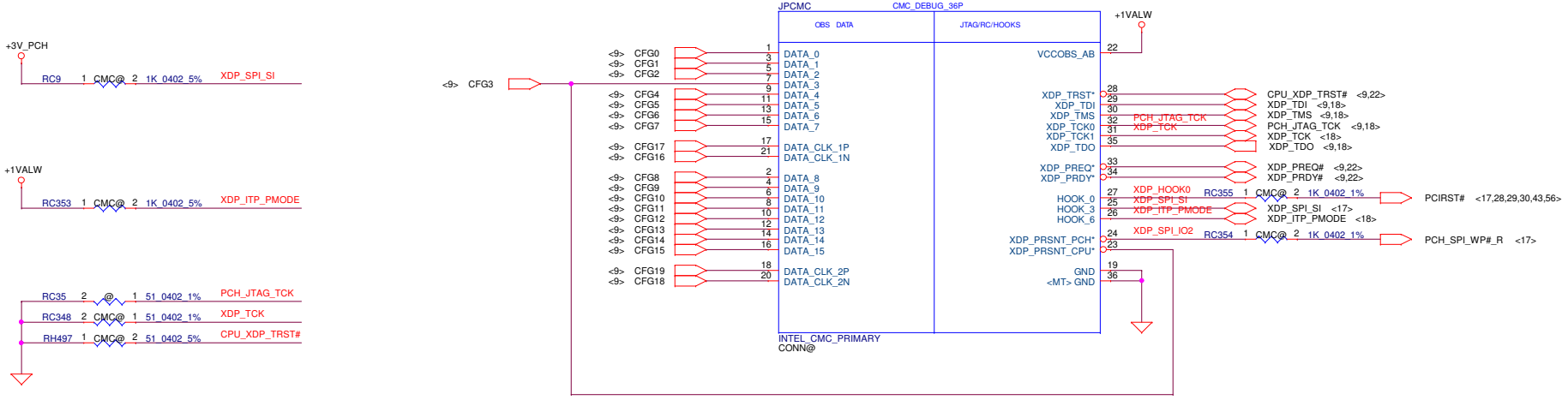




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Title: **CMC CONN.**

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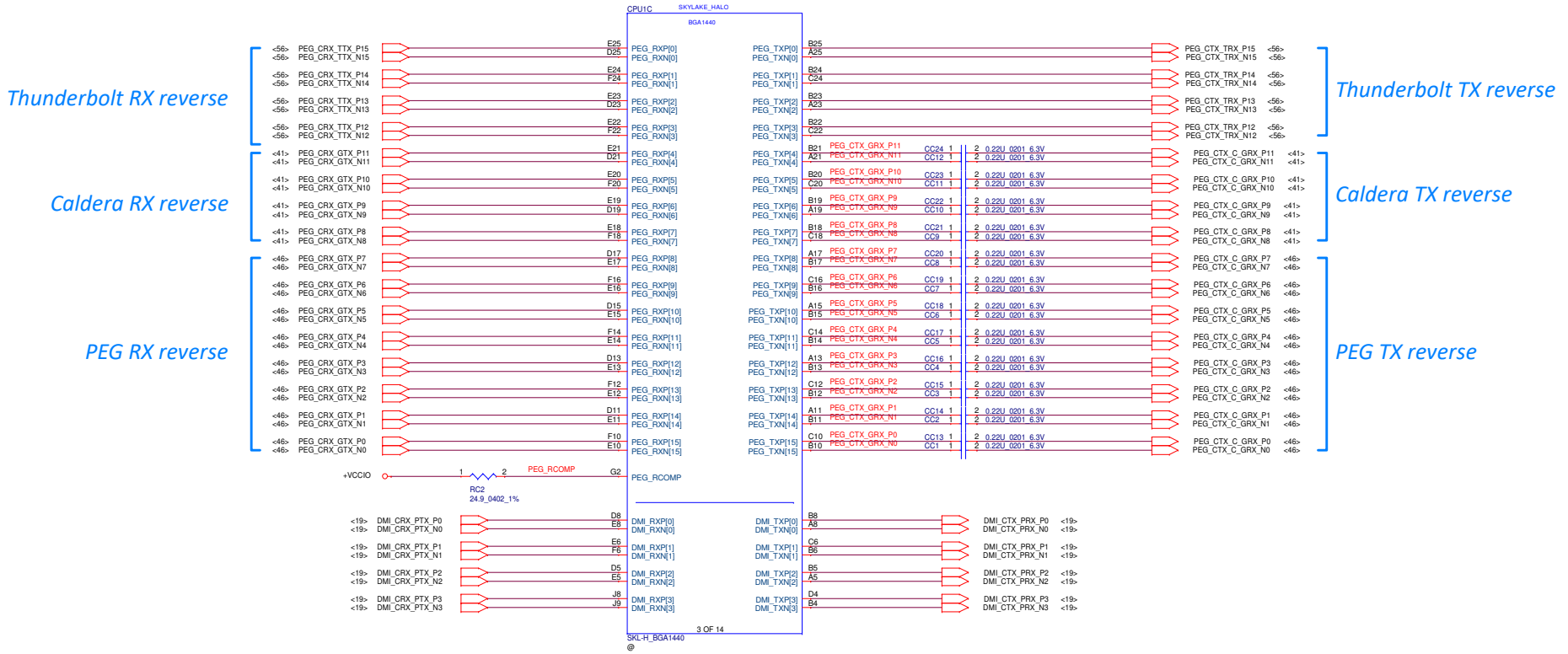


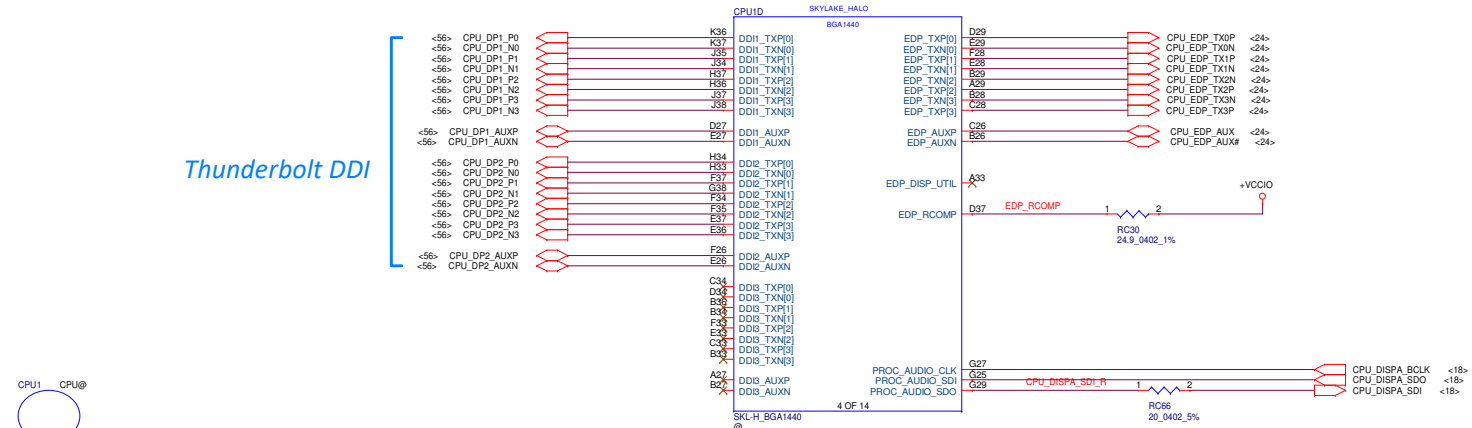


CPU1 CPU@

SA000097D2L

SKL-H_BGA1440

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|---|---|---|---|
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Title: CPU(1/7) DMI,PEG,DDI,EDP

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|---|---|---|
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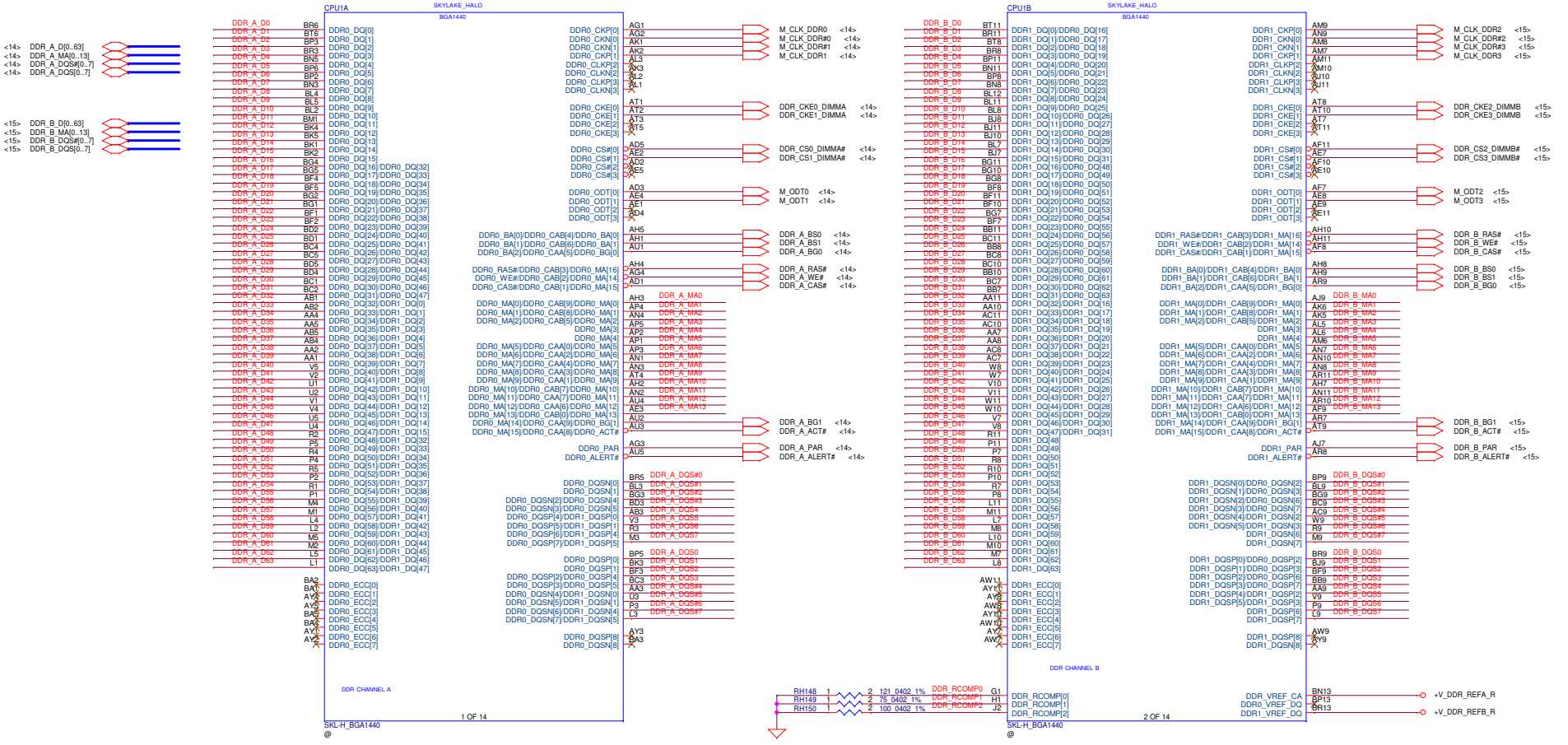
## Interleave



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Title: **CPU(2/7) DDR4**

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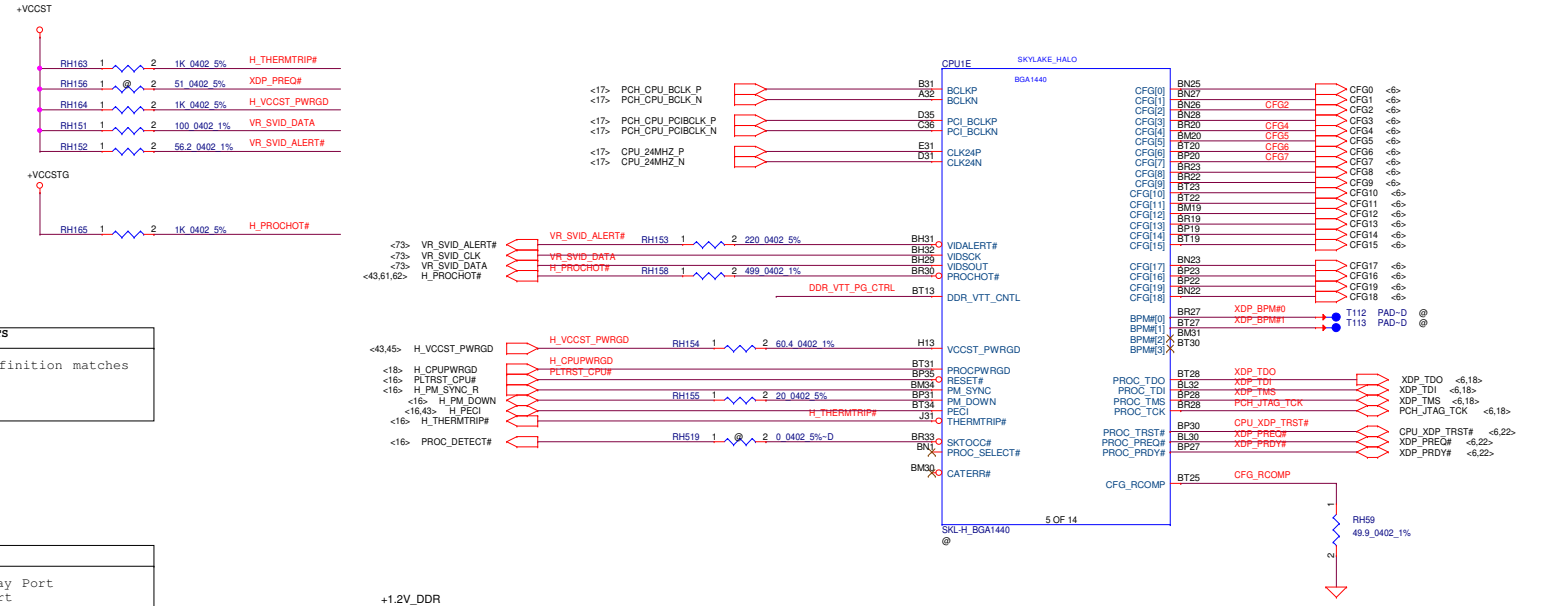


| PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS | |
|---|---|
| CFG2 | 1: Normal Operation; Lane # definition matches socket pin map definition<br>★ 0:Lane Reversed |

| Display Port Presence Strap | |
|---|---|
| CFG4 | 1 : Disabled; No Physical Display Port attached to Embedded Display Port<br>★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port |

| PCIE Port Bifurcation Straps | |
|---|---|
| CFG[6:5] | 11: (Default) x16 - Device 1 functions 1 and 2 disabled<br>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled<br>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)<br>★00: x8,x4,x4 - Device 1 functions 1 and 2 enabled |



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| | | | |
|---|---|---|---|
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| Title | CPU(3/7) CFG,XDP | | |
| Size | Document Number LA-D581P | | Rev 0.4 |
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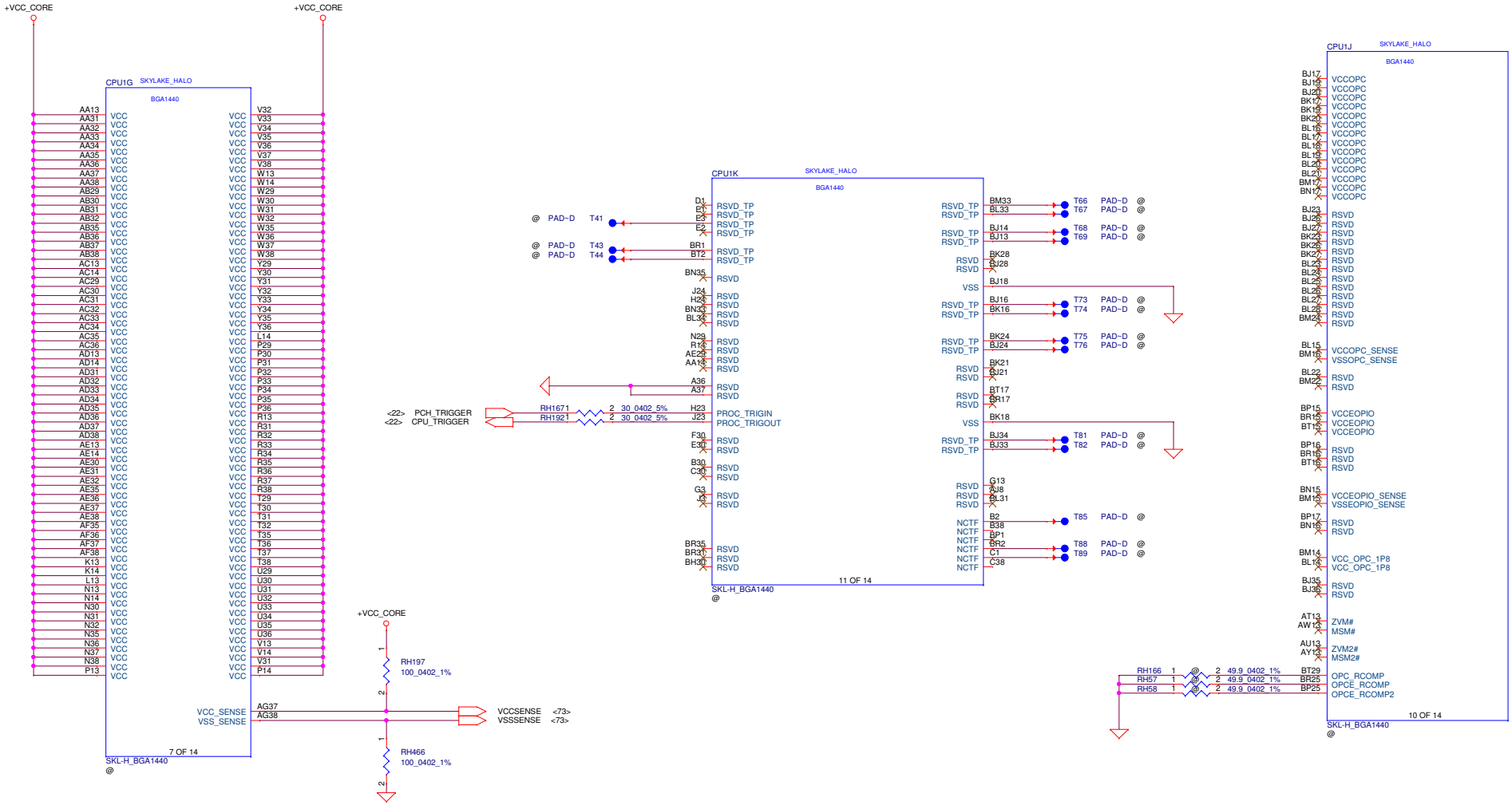




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Title: **CPU(4/7) +VCC_CORE,RSVD**

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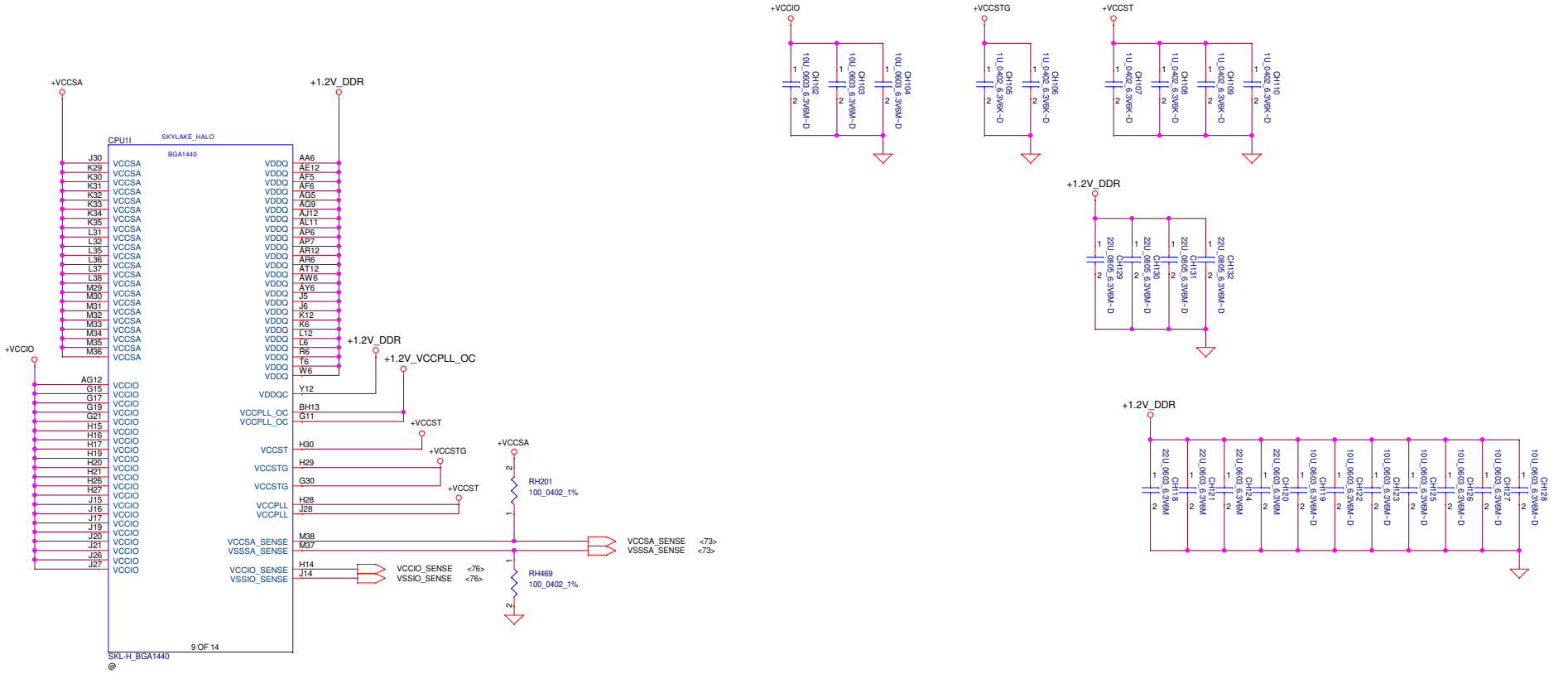


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Title: **CPU(5/7) +VCCSA,+VCCIO**

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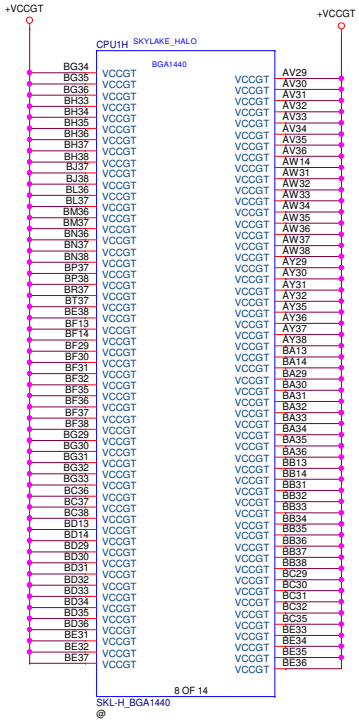


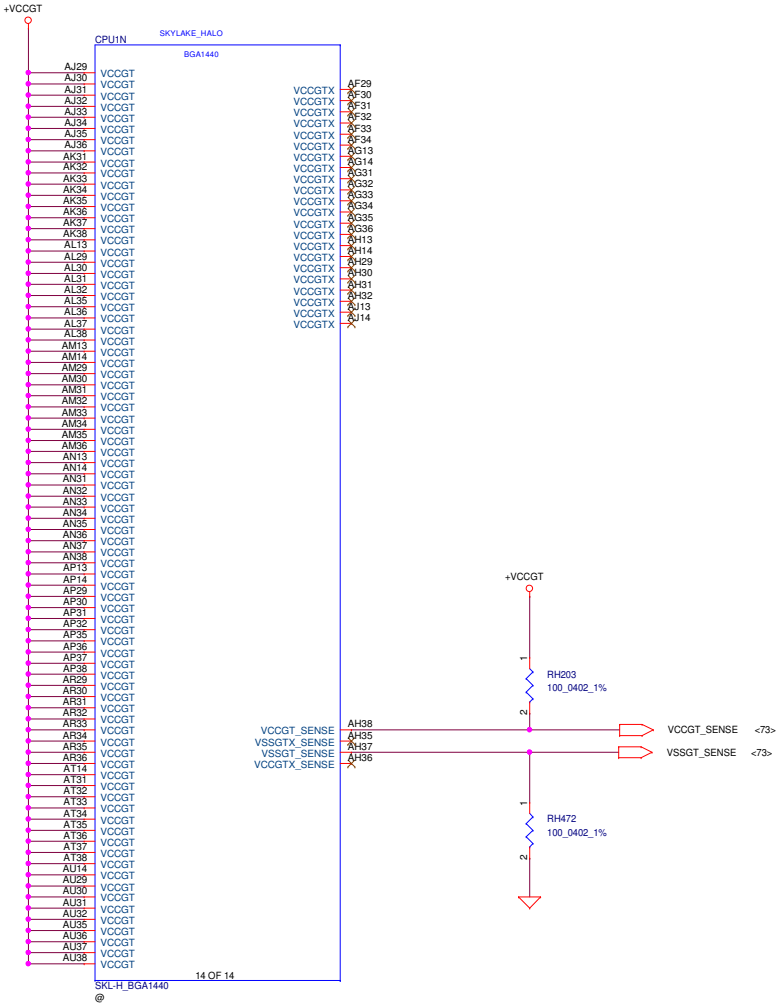


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Title: CPU(6/7) +VCCGT

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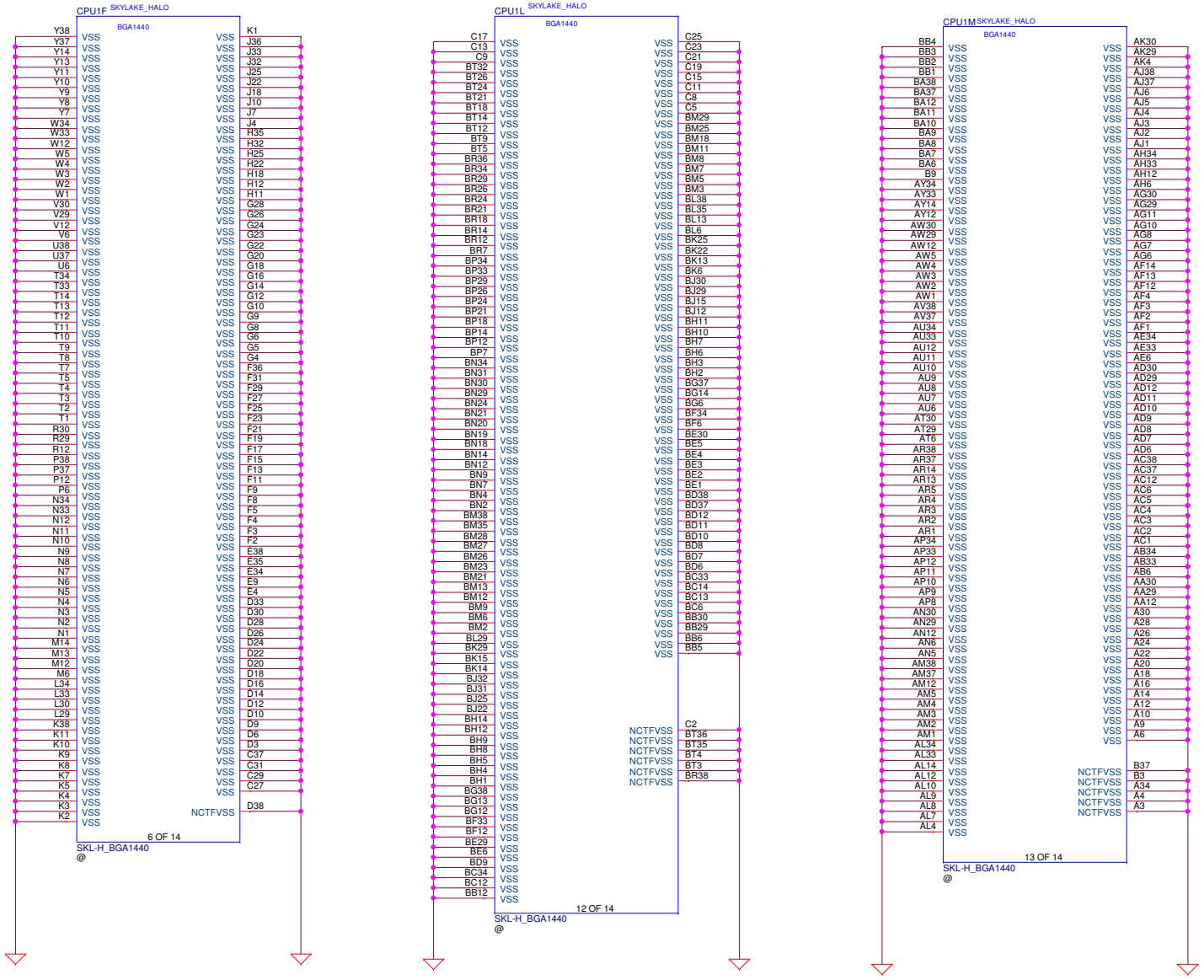




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Title: CPU(7/7) VSS

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4H , RVS

Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.258

Layout Note:
Place near JDIMM1.255

Layout Note:
Place near JDIMM1

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Title: **DDR4 DIMMA,RVS**

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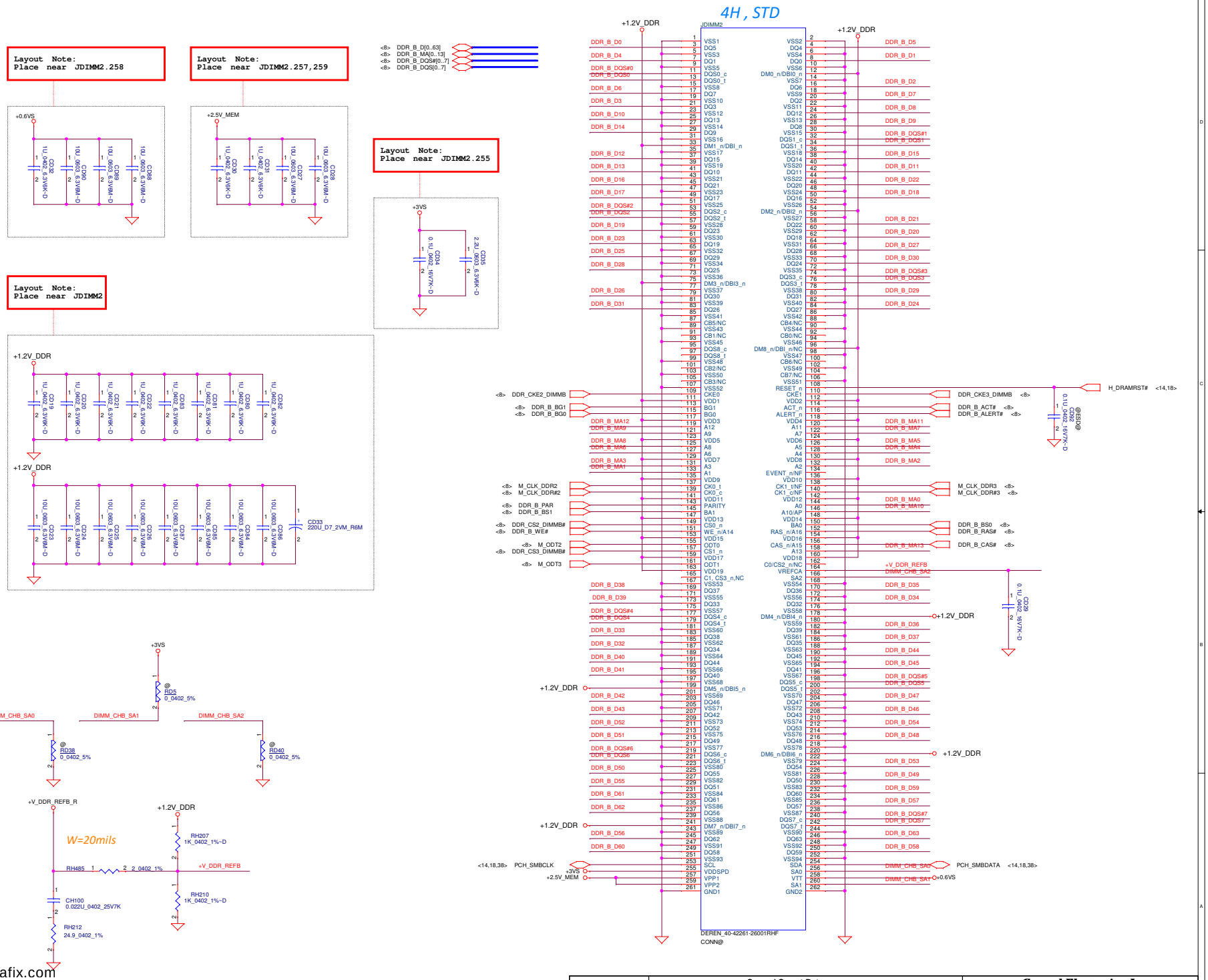


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Title: **DDR4 DIMMB,STD**

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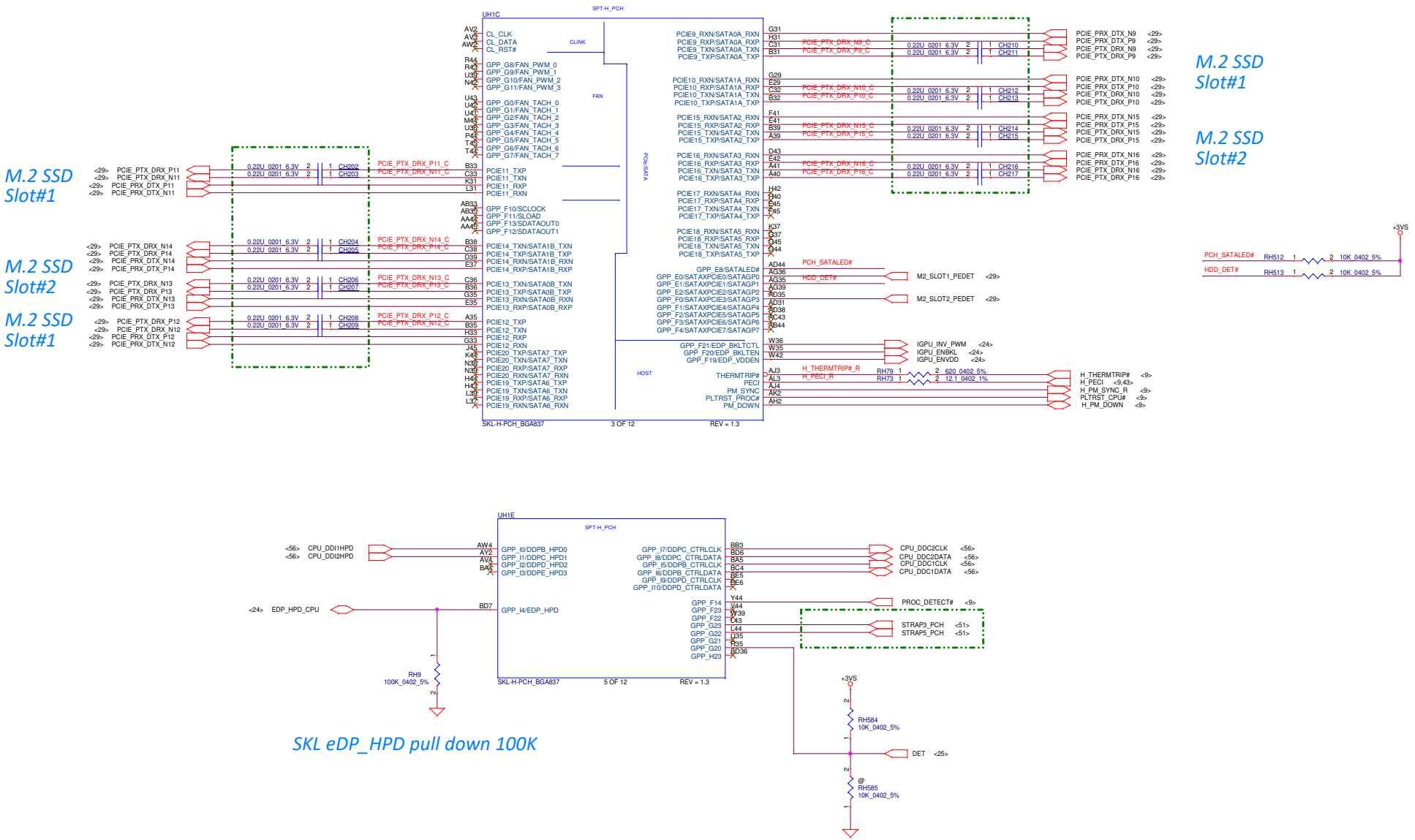


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Title: **PCH (1/7) SATA,DDC,PCIE**

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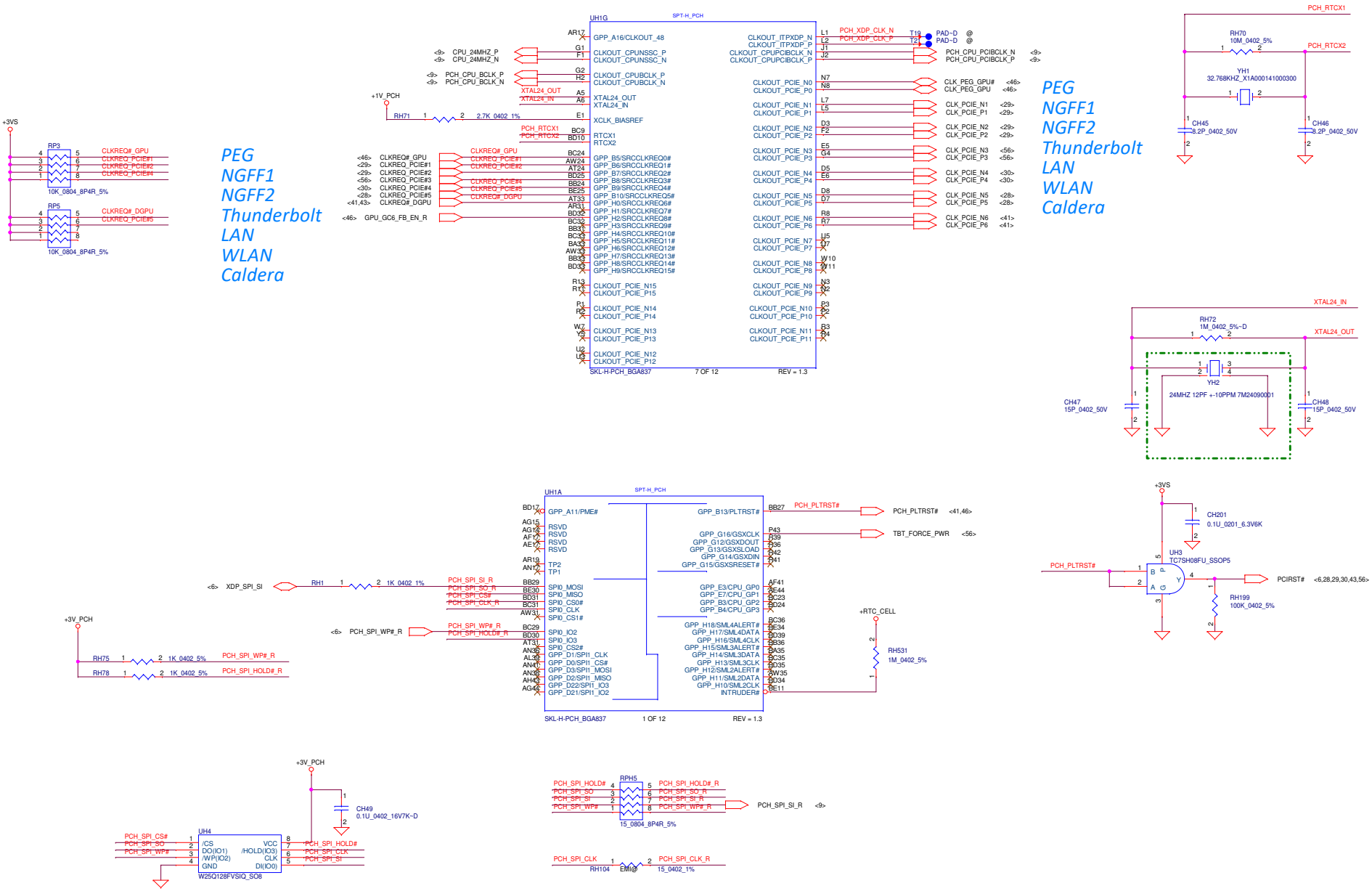


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Title: **PCH (2/7) CLK,SPI,PLTRST**

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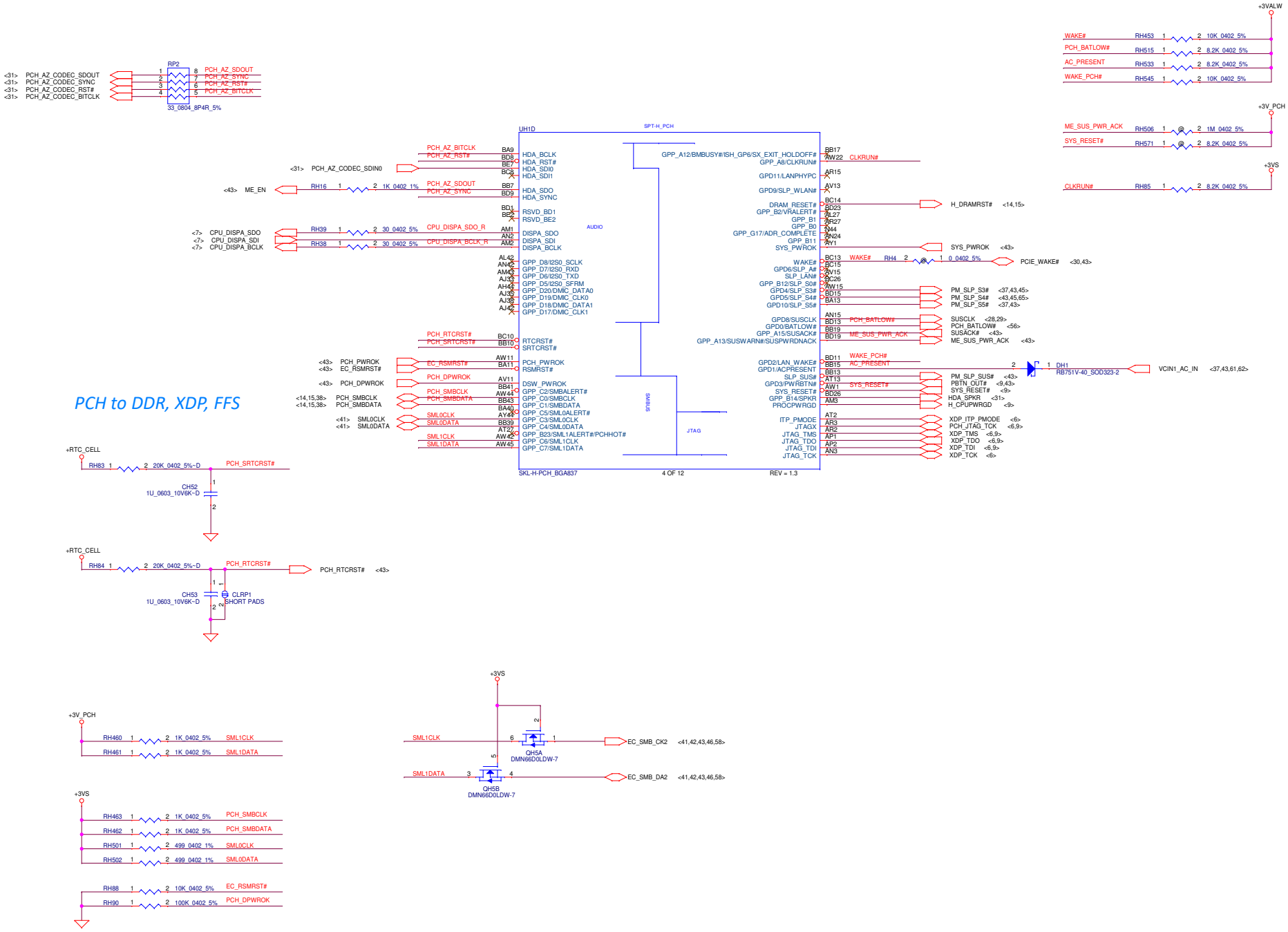


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Title: **PCH (3/7) PM,HDA,SMB,JTAG**

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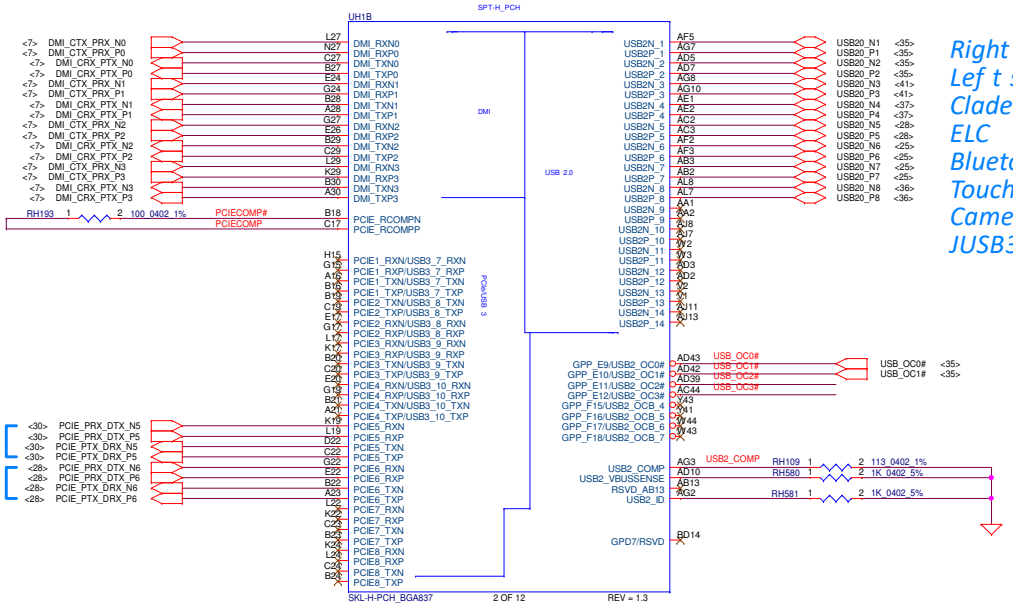



LAN

WLAN

Right side JUSB1(Powershare,debug port)

Left side USB2

Cladera

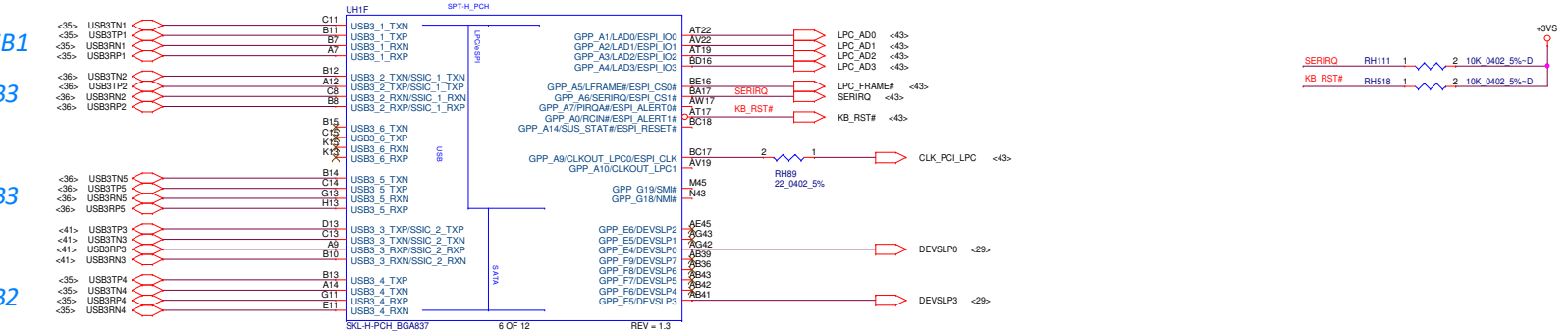
ELC

Bluetooth

Touch screen

Camera

JUSB3


Right side JUSB1

Left side USB3

Left side USB3

Caldera

Left side USB2

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Title: PCH (4/7) DMI,PCIE,USB,LPC

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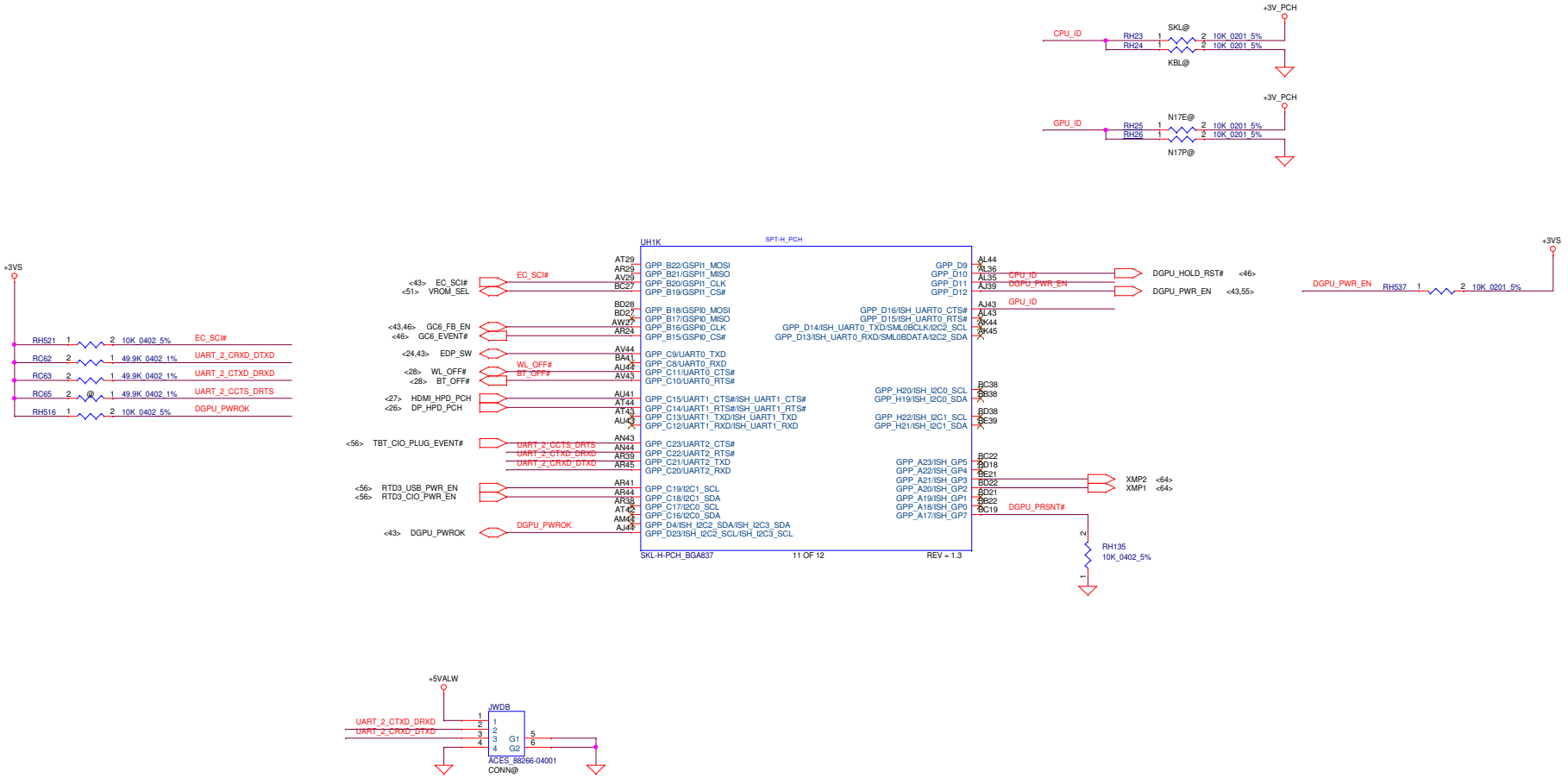




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



**Compal Electronics, Inc.**

Title: **PCH (5/7) I2C,GPIO**

| Size | Document Number | Rev |
|---|---|---|
| | LA-D581P | 0.4 |

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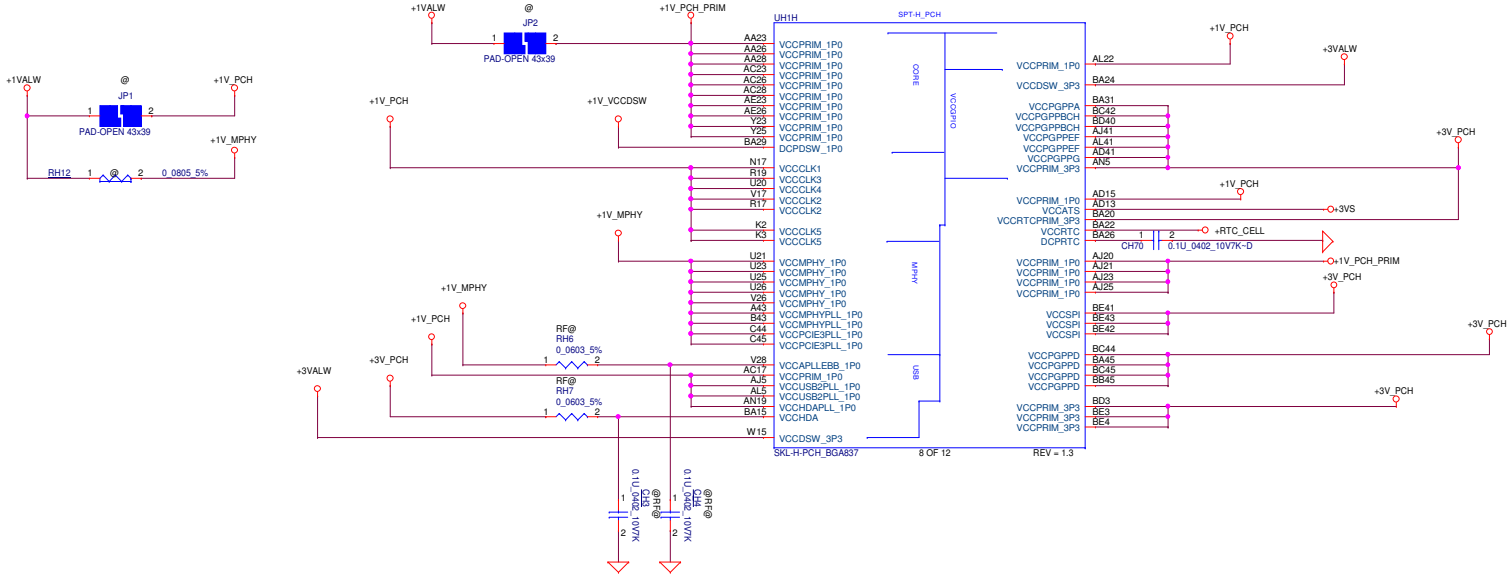
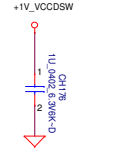
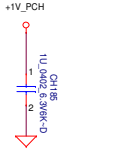
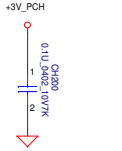


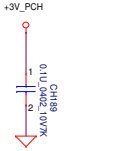

Close to BA29



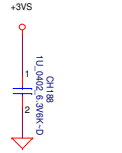

Close to AC17



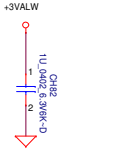

Close to BA15



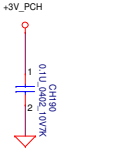

Close to AN5



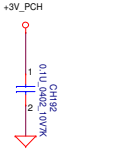

Close to AD13



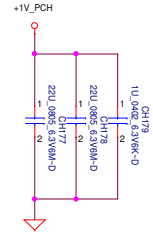

Close to W15



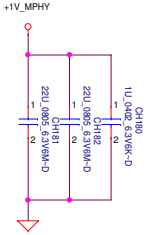

Close to AD41



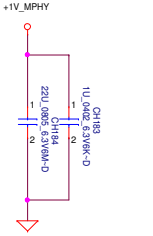

Close to BC42,BD40



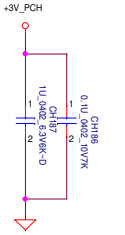

Close to K2,K3



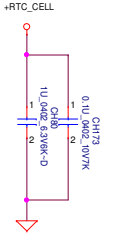

Close to A43,B43



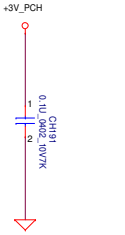

Close to U21,U23,U25,U26,V26




Close to BA20




Close to BA22




Close to AJ41,AL41



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



**Compal Electronics, Inc.**

Title: **PCH (6/7) PWR**

| Size | Document Number | Rev |
|---|---|---|
| | LA-D581P | 0.4 |

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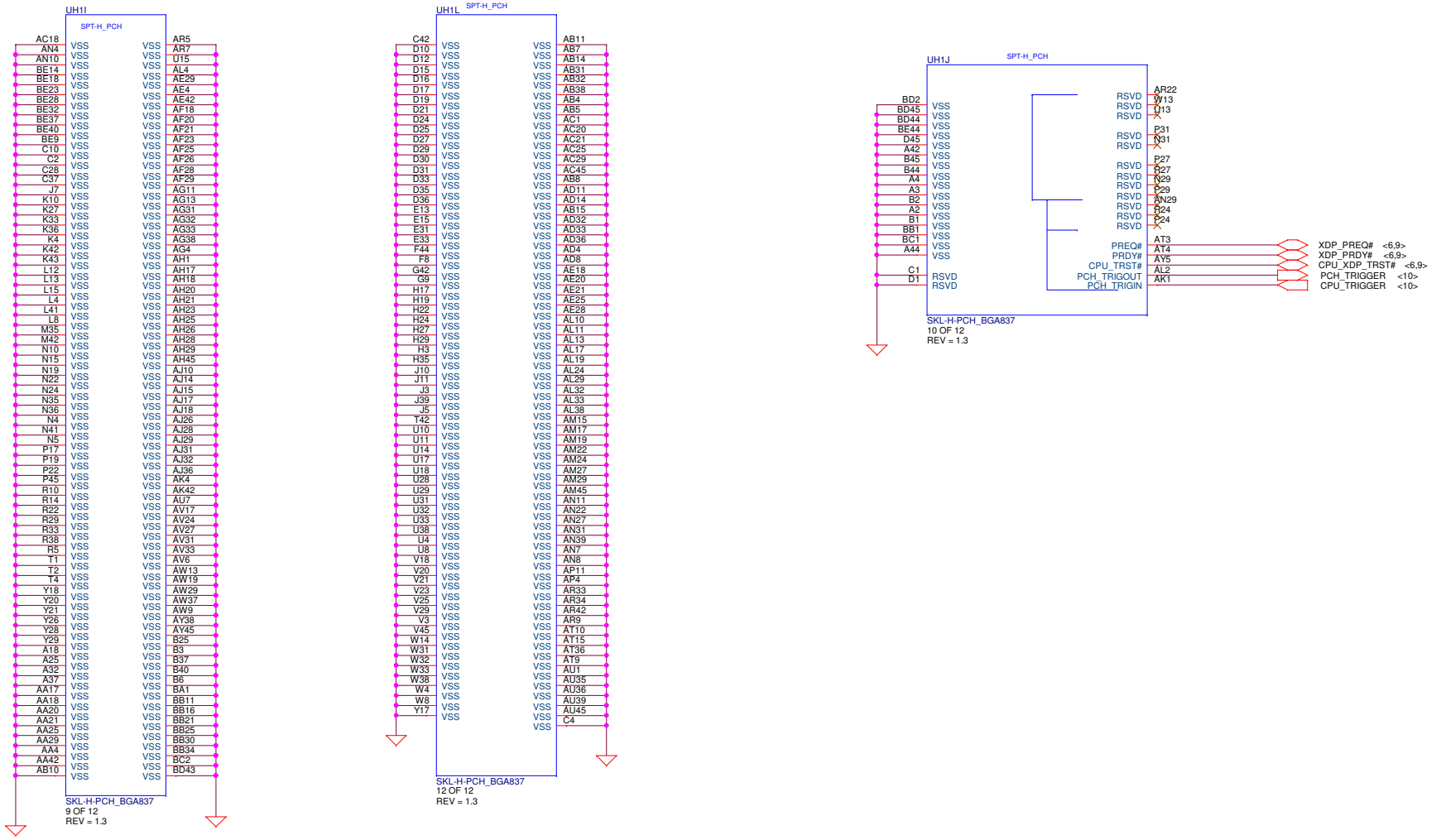




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



**Compal Electronics, Inc.**

Title: **PCH (7/7) VSS**

| Size | Document Number | Rev |
|---|---|---|
| | LA-D581P | 0.4 |

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IN1_AEQ#, IN2_AEQ#
Automatic EQ disable Internal pull down at ~150KΩ, 3.3V/O
L: Automatic EQ enable(default)
H: Automatic EQ disable

GPU

CPU

IN1_PEQ#, IN2_PEQ#
Programmable input equalization levels; Internal pull down at ~150KΩ, 3.3V/O
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

| S1 | OE | output | function |
|---|---|---|---|
| L | L | A=B1 | DGPU |
| H | L | A=B2 | IGPU |
| X | H | | |

I2C_CTL_EN
I2C Control Enable; Internal pull down at ~150KΩ, 3.3V/O
L: Pin control mode is selected
H: I2C control is selected with default address 0x66/67
M: I2C control is selected with alternative address 0xD8/D9

PI0
Auto test enable; Internal pull down at ~150KΩ, 3.3V/O
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

PC0
AUX interception disable for Port y(y = 1, 2). Internal pull down at ~150KΩ, 3.3V/O
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1
Output swing adjustment for Port y (y = 1, 2). Internal pull down at ~150KΩ, 3.3V/O
L: default
H: +20%
M: -16.7%



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|---|---|---|---|
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



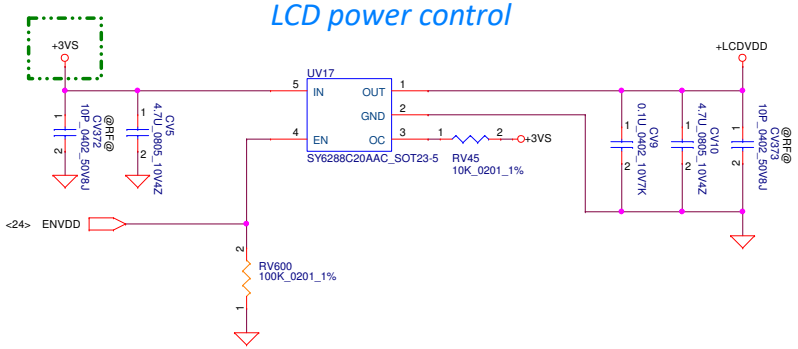
Compal Electronics, Inc.

Title: eDP MUX PS8331B

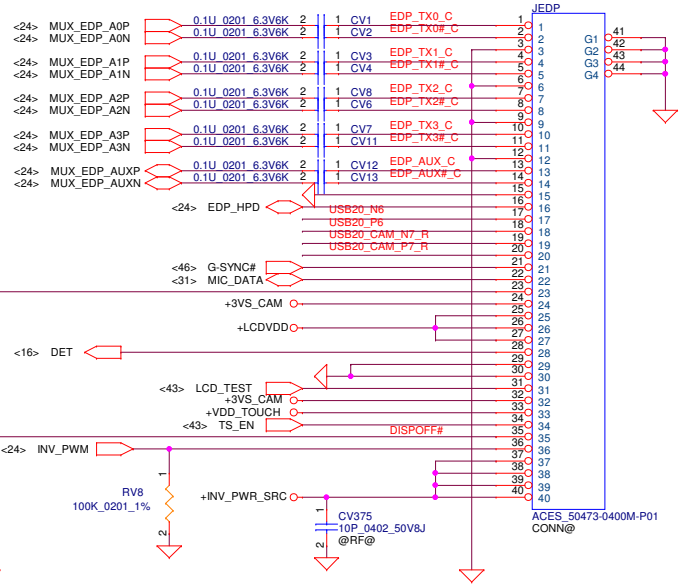
Size: Custom | Document Number: LA-D581P | Rev: 0.4

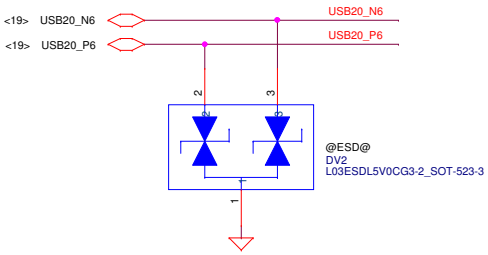
Date: Wednesday, September 07, 2016 | Sheet 24 of 80

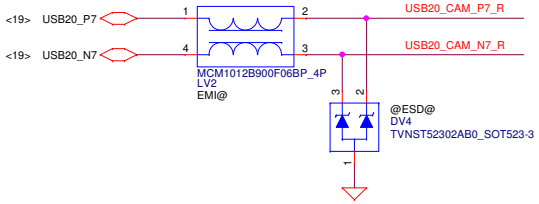
## LCD power control

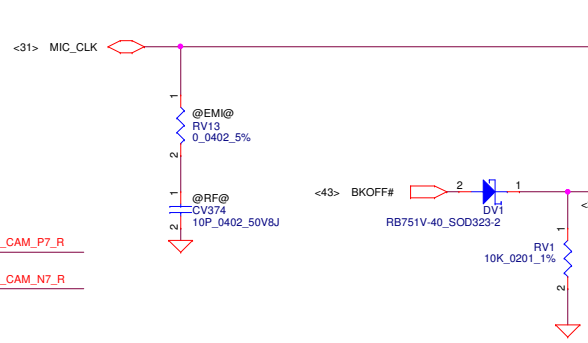



## eDP connector

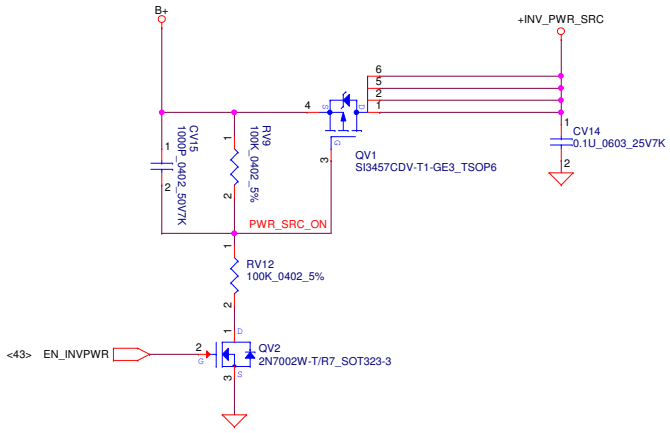


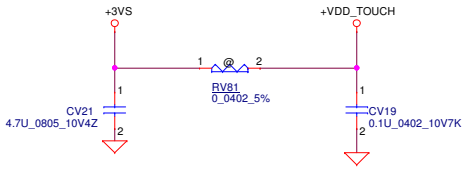



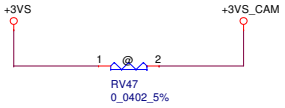

## LCD backlight power control

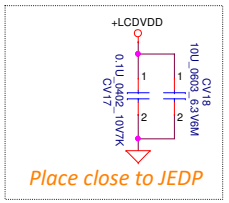



## Touch screen panel power




## Camera power




IR camera pindef i ne
IR_LED+
IR_LED+
IR_LED+/NC
IR_LED-/DET , connect to PCH GPIO
IR_LED-
IR_LED-
Diglog_loop , connect to PCH GPIO
DGND
D+
D-
USB3V3
MIC_SIG
MIC_CLK
DGND

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| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



**Compal Electronics, Inc.**

Title: eDP/camera/TS

Size: Custom | Document Number: LA-D581P | Rev: 0.4

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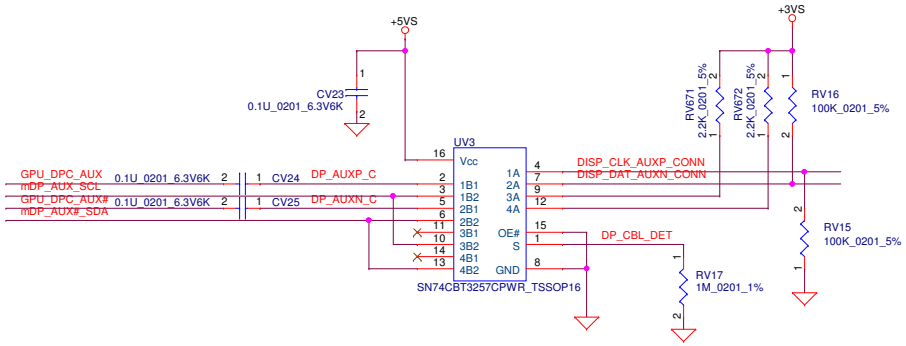
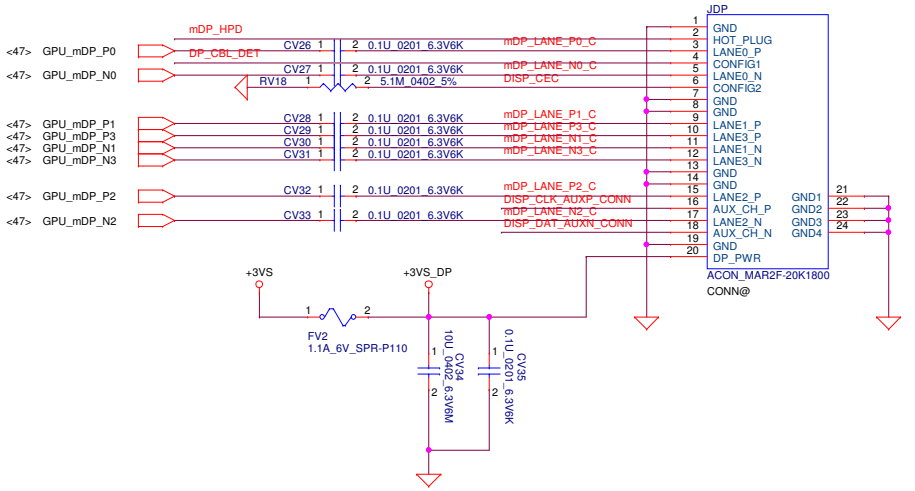
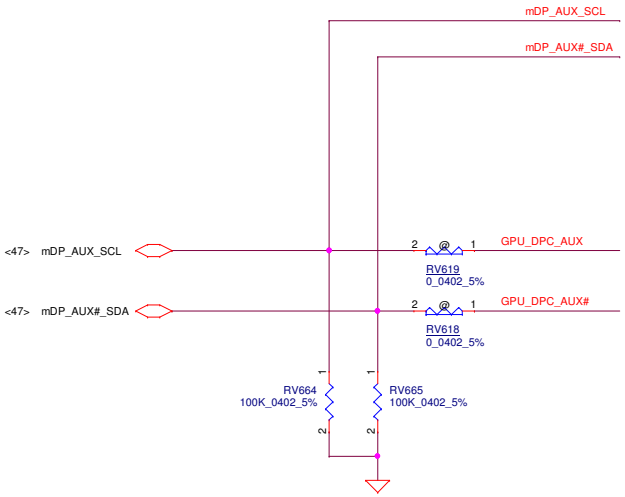
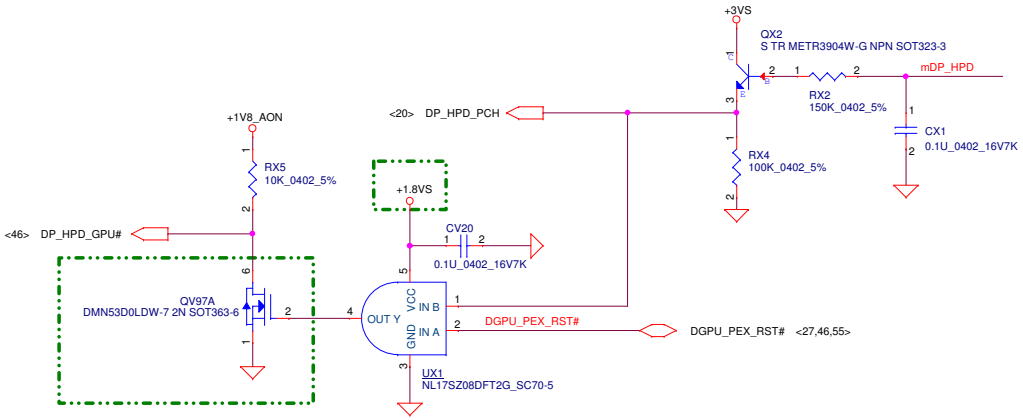



| Funct i on | S | OE# |
|---|---|---|
| mini DP cable | L | L |
| mini DP dongle | H | L |






| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



**Compal Electronics, Inc.**

Title: **Mini DP**

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-D581P | 0.4 |

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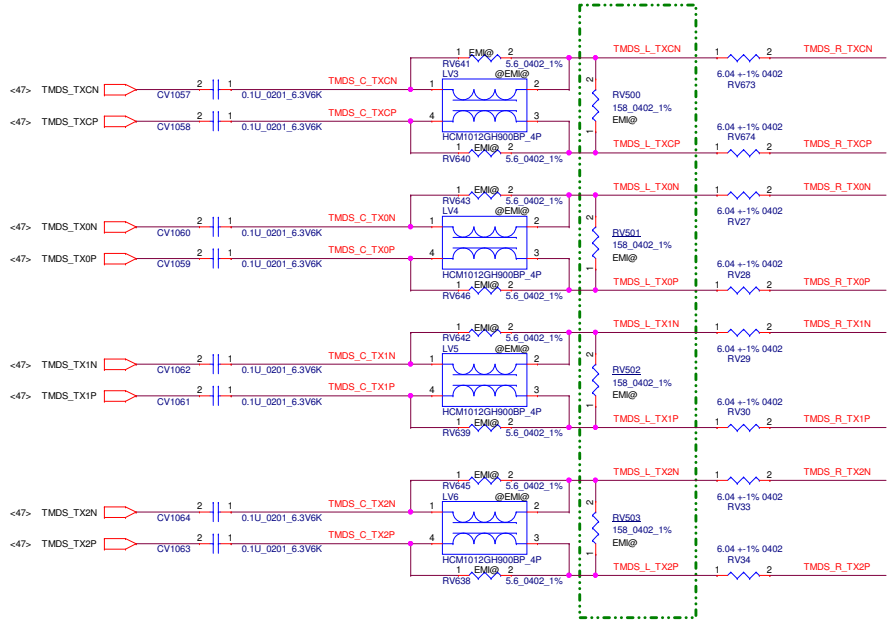
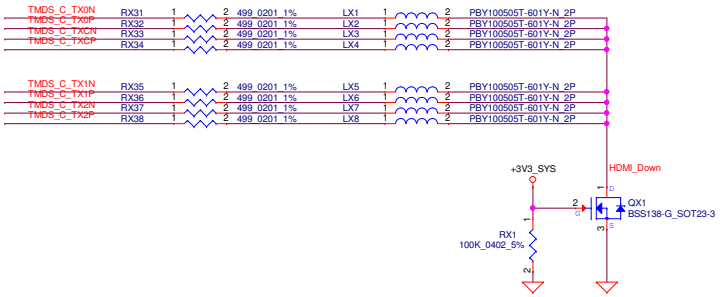
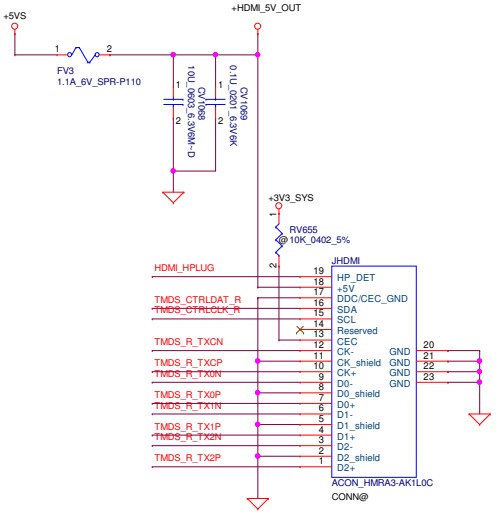
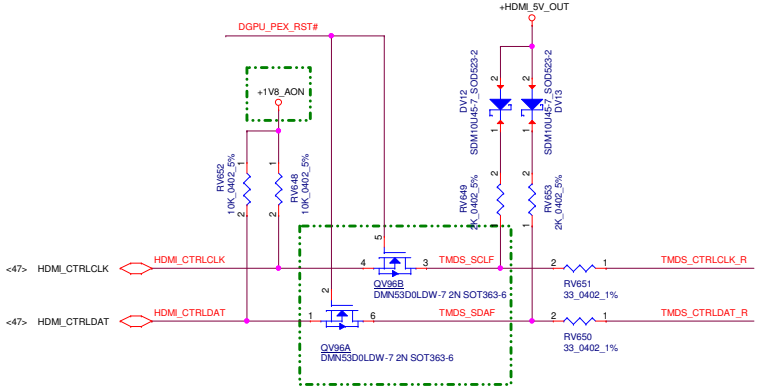


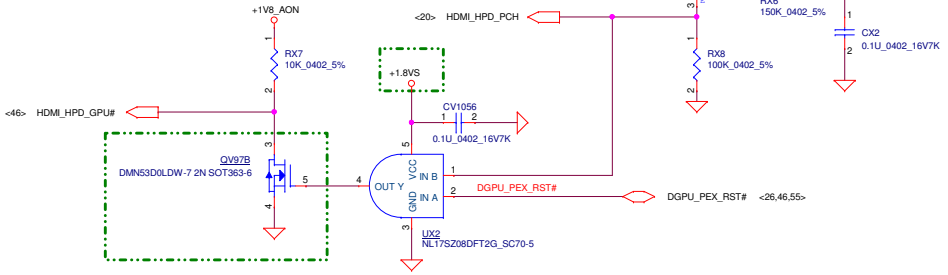







To GPU

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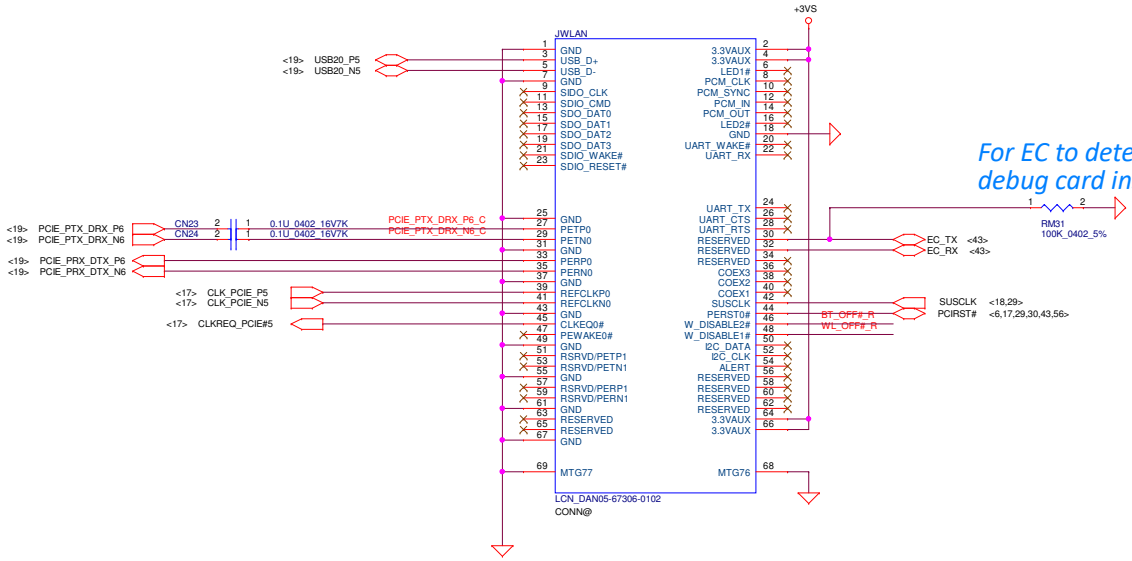
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



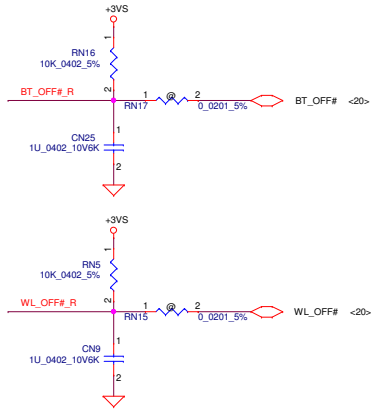
| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: HDMI | | | |
| Size: Custom | Document Number: LA-D581P | | Rev: 0.4 |
| Date: Wednesday, September 07, 2016 | Sheet 27 of 80 | | |

## M.2 2230 slot(type E)

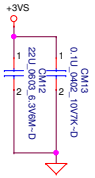



*For EC to detect debug card insert.*

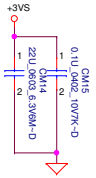



*closed to pin 2, 4*




*closed to pin 64, 66*




*WLAN power control*

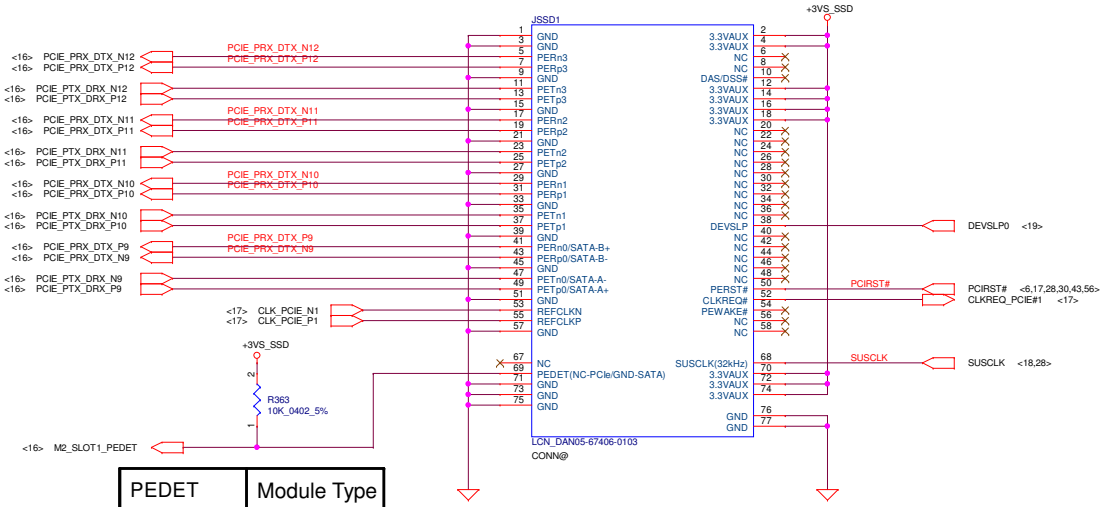



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |

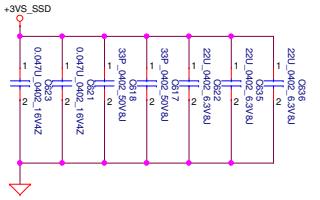


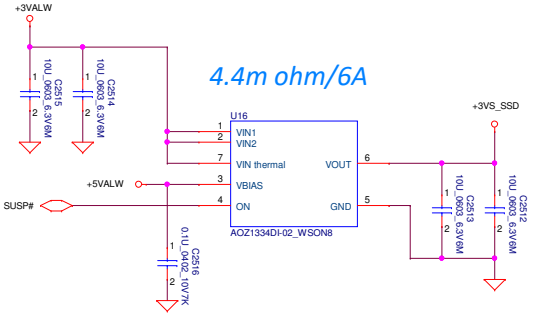
| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: NGFF WLAN/BT | | | |
| Size | Document Number: LA-D581P | | Rev: 0.4 |
| Date: Wednesday, September 07, 2016 | Sheet 28 of 80 | | |

## SSD
## NGFF Slot_1 Key M

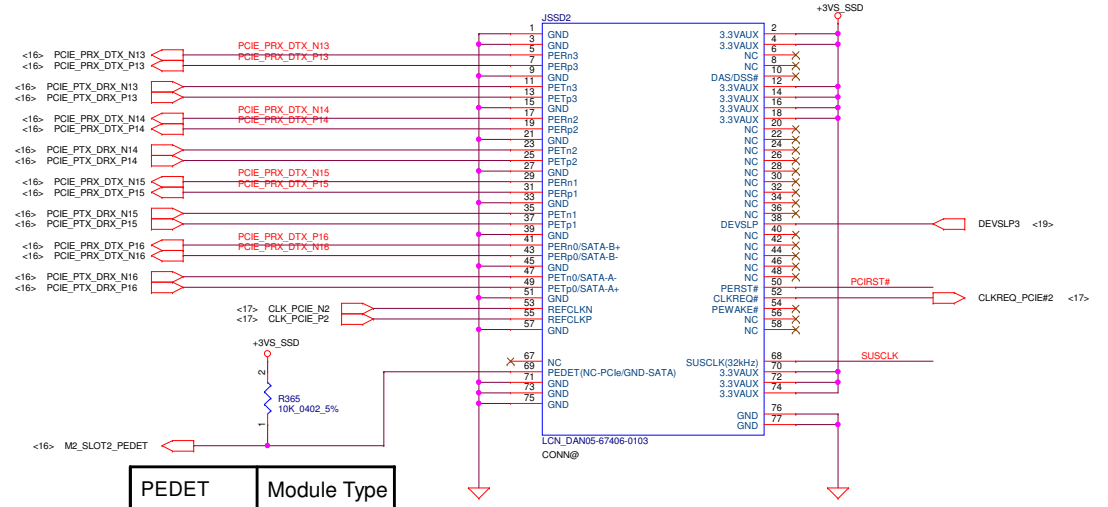



| PEDET | Module Type |
|---|---|
| 0 | SATA |
| 1 | PCIE |

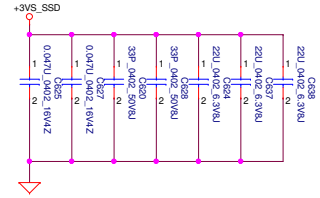



## SSD
## NGFF Slot_2 Key M




| PEDET | Module Type |
|---|---|
| 0 | SATA |
| 1 | PCIE |

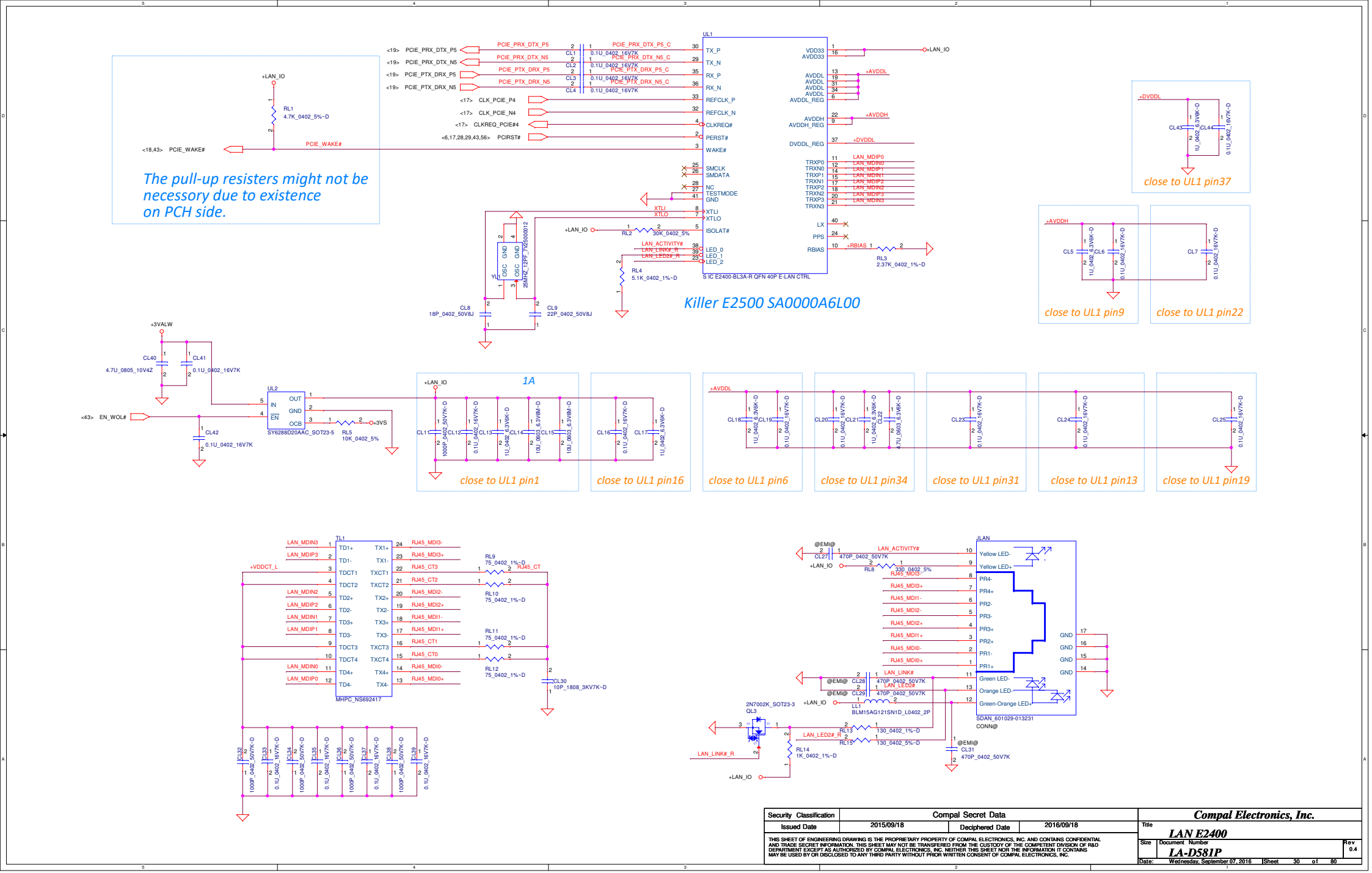





| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: NGFF SSD | | | |
| Size | Document Number: LA-D581P | | Rev: 0.4 |
| Date: Wednesday, September 07, 2016 | Sheet 29 of 80 | | |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



**Compal Electronics, Inc.**

Title: **LAN E2400**

| Size | Document Number | Rev |
|---|---|---|
| | LA-D581P | 0.4 |

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CA1,CA2 close to UA1 pin19

CA12,CA13 close to UA1 pin7

EC Beep

MCU Beep

Moat

Place on the moat between GND & GNDA.

GNDA GND

Set ting the Turn-Off Tim
Ton (ms) = 0.02 x Cset (pF)

Close to UA1 Pin53

Near Codec

W=40mils
W=40mils

Jack1 : Global Headset
OMTP/CTIA headset, Headphone, Line-Out

Re-tasking port
Headphone, Line-Out, Mic-In, Line-In

ALC3266-CG_QFN56_7X7

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| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



Compal Electronics, Inc.

Title: Audio codec ALC3266

Size: | Document Number: LA-D581P | Rev: 0.4

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CA64, CA65 close to PIN16

CA52, CA53 and CA54 close to PIN1,56

CA55, CA56 and CA57 close to PIN42,43

CA58, CA59 close to PIN17

CA60 close to PIN21

CA61, CA62 and CA63 close to PIN37

CA52, CA53 and CA54 close to PIN 51

CA52, CA53 and CA54 close to PIN 48

RA58.1 should from RA57.1 directly
RA59.1 should from RA57.2 directly
RA61.1 should from JSPK.4 directly

RA63.1 should from RA60.1 directly
RA64.1 should from RA60.2 directly
RA65.1 should from JSPK.2 directly

CA77, CA78 close to PIN22

# Int. Speaker Conn.

40 mils = For 4 ohm 3W Speaker

*Close to UA1 Pin42,43,44,45*

*Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-*
*Speaker 4 ohm : 40 mil*
*Speaker 8 ohm : 20 mil*

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2014/09/08 | Deciphered Date | 2016/09/18 |

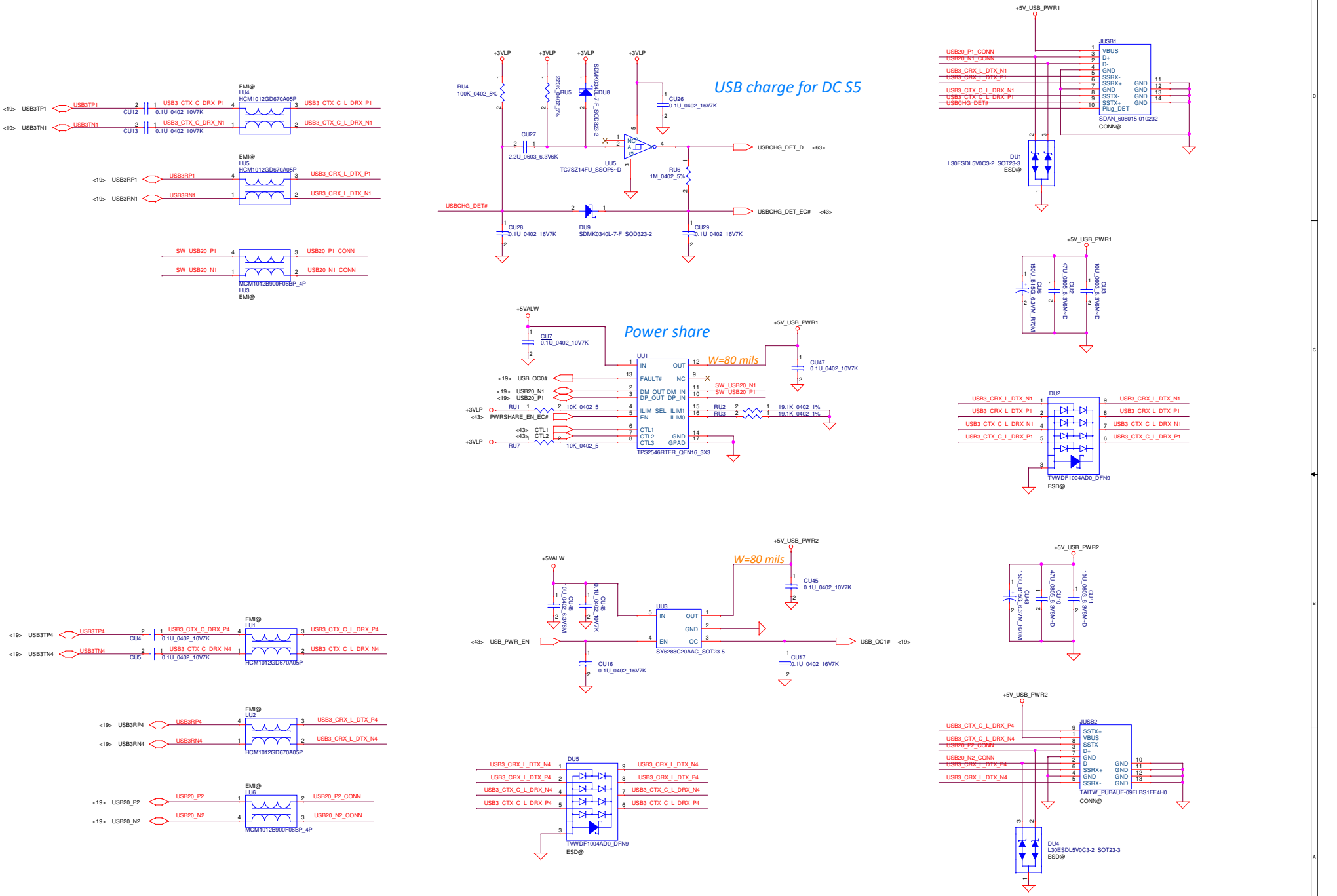


Compal Electronics, Inc.

Title: ALC1309

Size: | Document Number: LA-D581P | Rev: 0.4

Date: Wednesday, September 07, 2016 | Sheet 32 of 80

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| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |

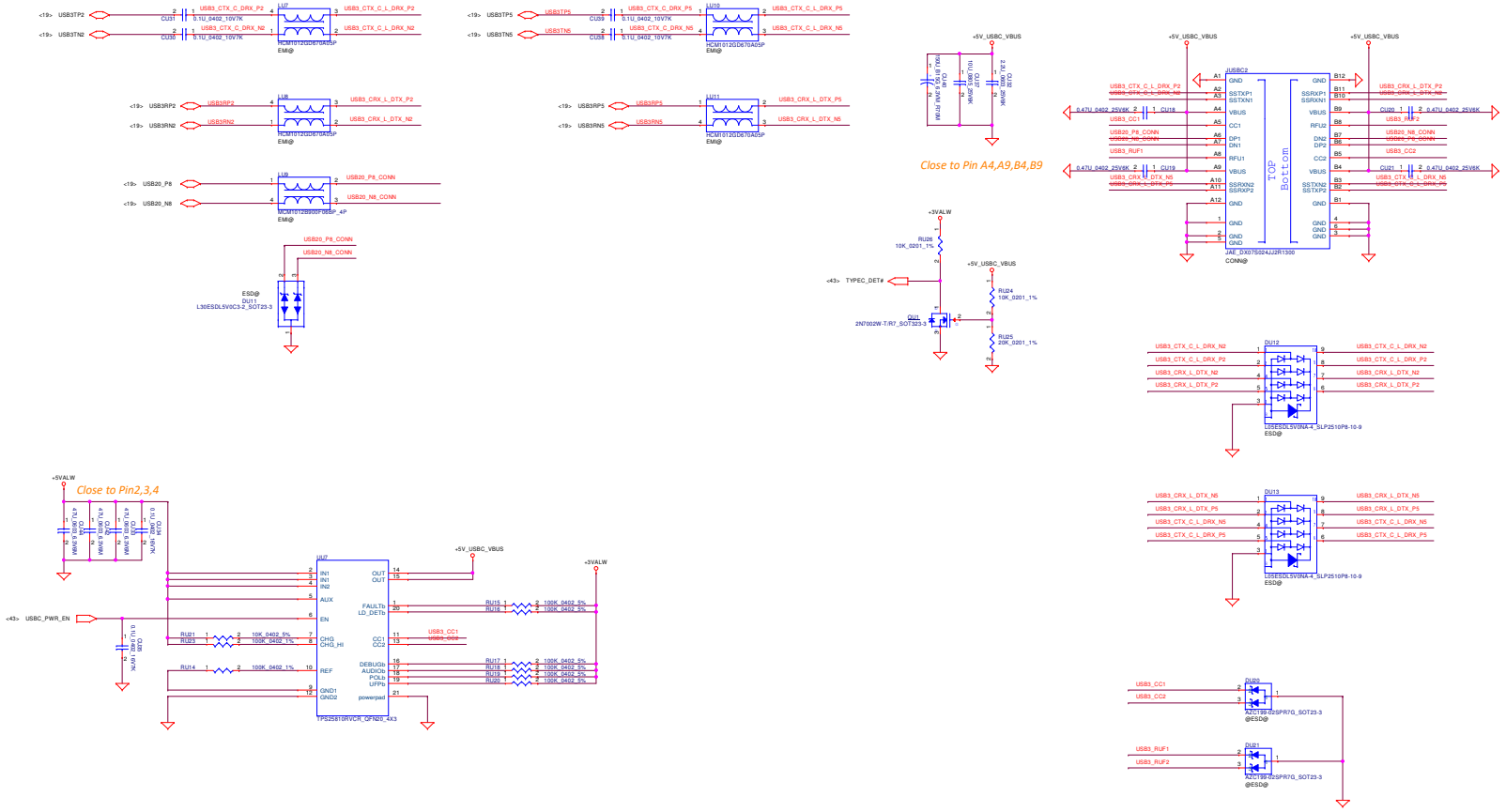


Compal Electronics, Inc.

Title: USB3.0/2.0 (Type A) x2

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-D581P | 0.4 |

Date: Wednesday, September 07, 2016 Sheet 35 of 80




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/01/06 | Deciphered Date | 2016/09/18 |

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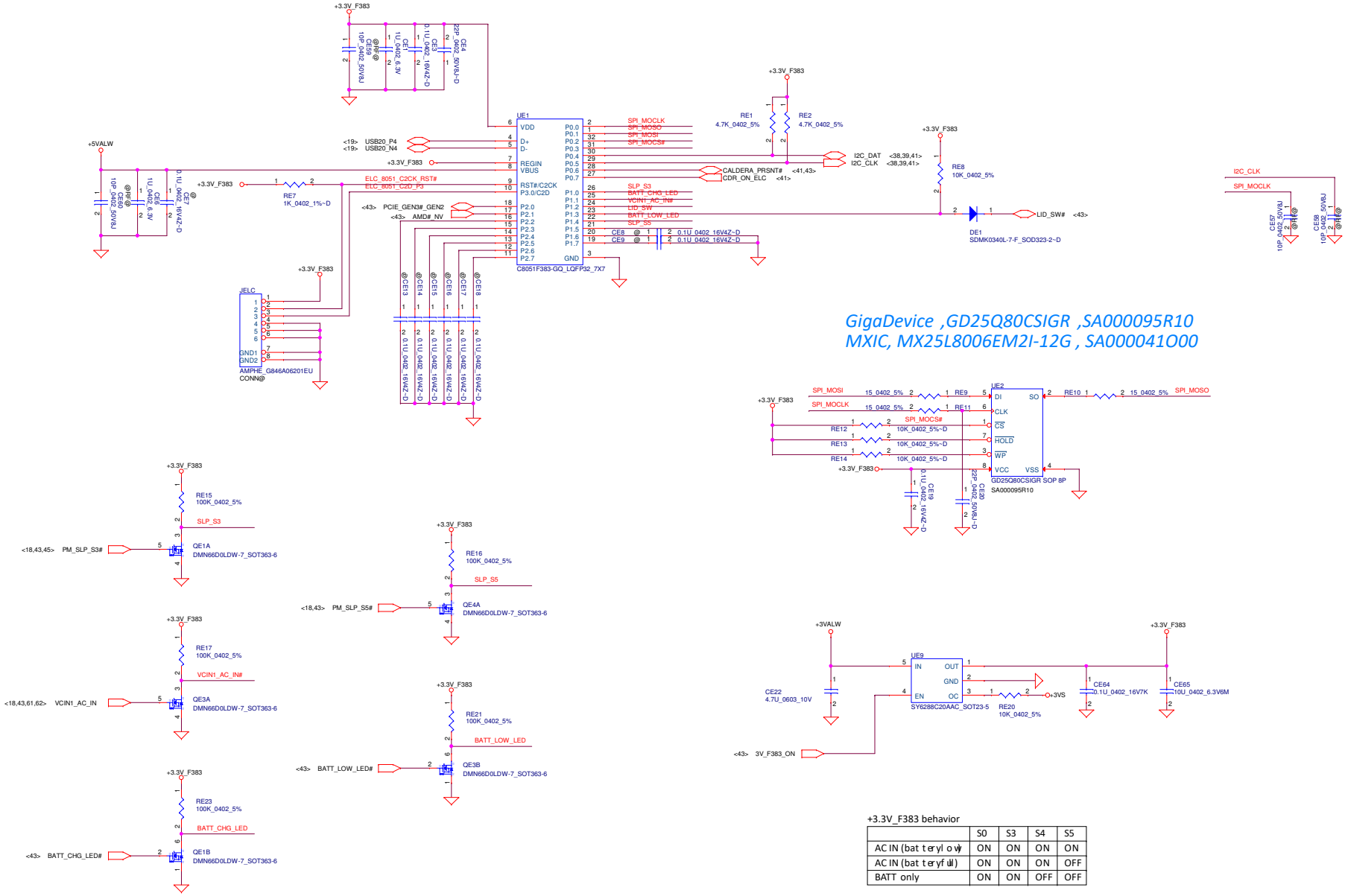
**Compal Electronics, Inc.**

Title: **USB3.0/2.0 (TypeC)**

Size: Document Number: **LA-D581P** Rev: 0.4

Date: Wednesday, September 07, 2016 Sheet 36 of 80




| +3.3V_F383 behavior | | | | |
|---|---|---|---|---|
| | S0 | S3 | S4 | S5 |
| AC IN (bat ter y l ow) | ON | ON | ON | ON |
| AC IN (bat ter y full) | ON | ON | ON | OFF |
| BATT only | ON | ON | OFF | OFF |



| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |

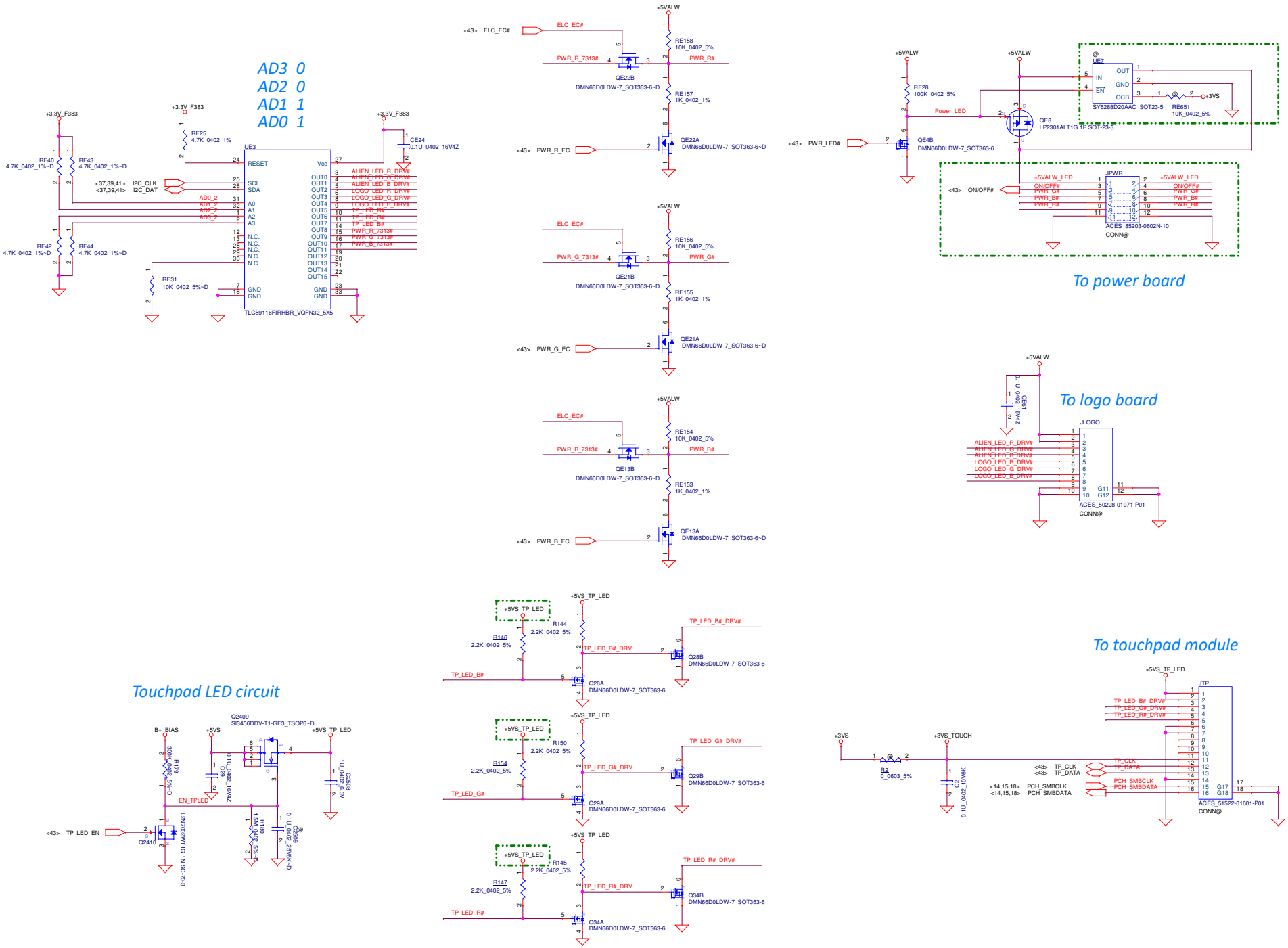


Compal Electronics, Inc.

Title: ELC (1) C8051F383

Size: Custom | Document Number: LA-D581P | Rev: 0.4

Date: Wednesday, September 07, 2016 | Sheet 37 of 80

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| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



Compal Electronics, Inc.

Title: ELC (2)/TP/PWR/LOGO

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-D581P | 0.4 |

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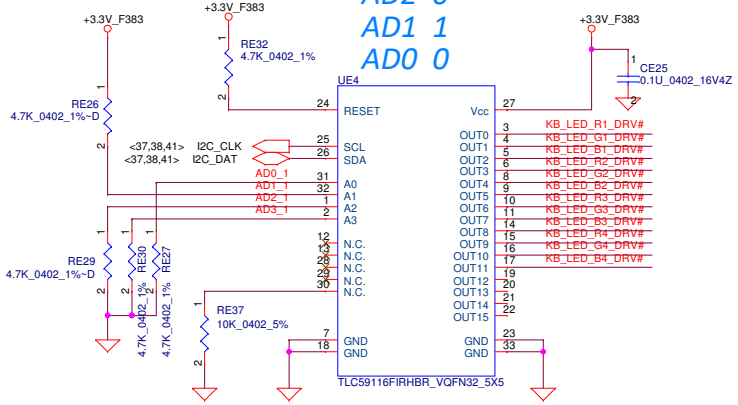
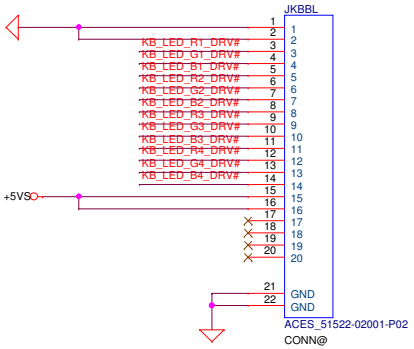
## KB Backlight

AD3 0
AD2 0
AD1 1
AD0 0




## KB BL LED






| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |

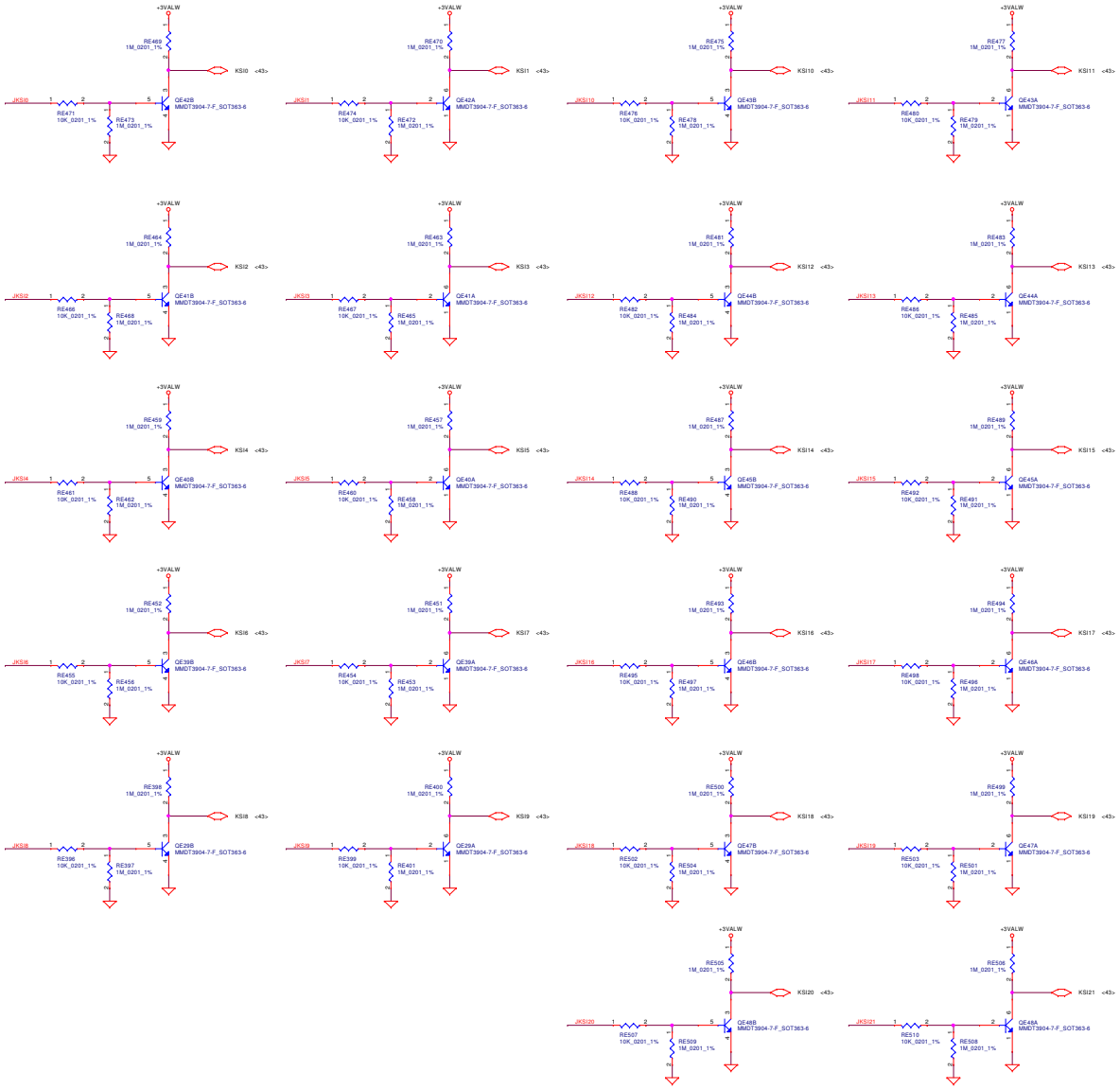


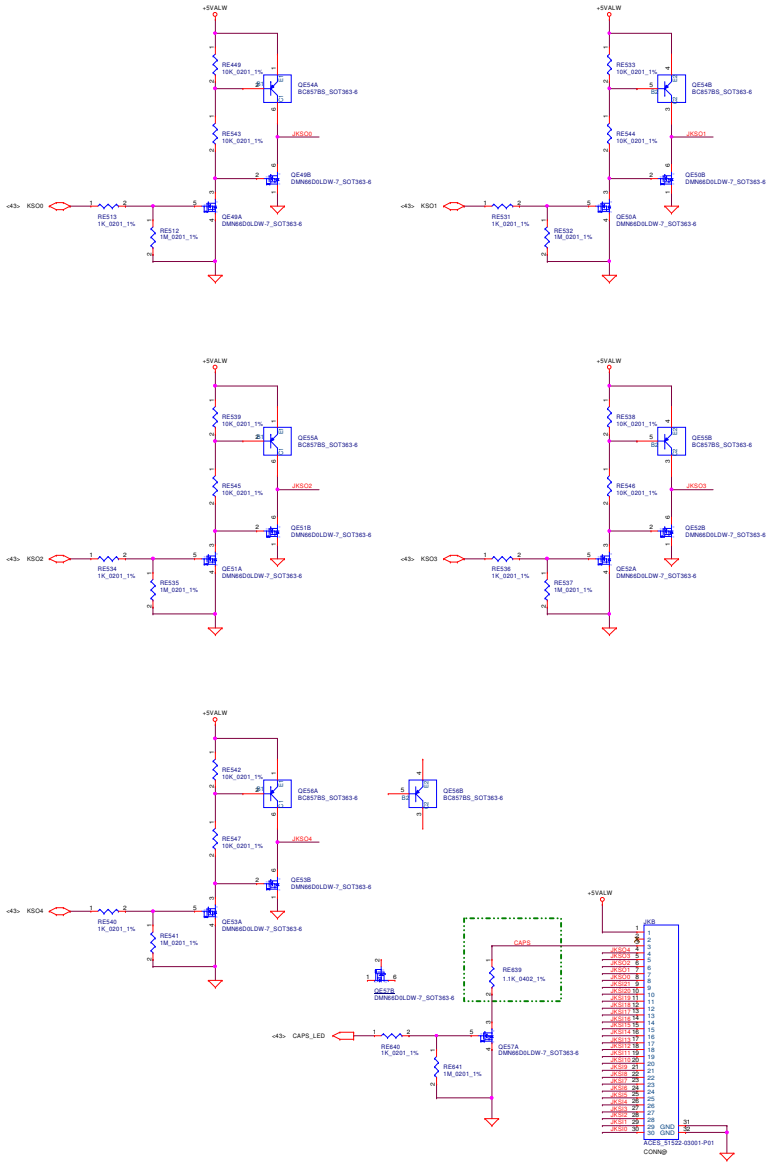
Compal Electronics, Inc.

Title: KBBL

Size: Custom | Document Number: LA-D581P | Rev: 0.4

Date: Wednesday, September 07, 2016 | Sheet 39 of 80

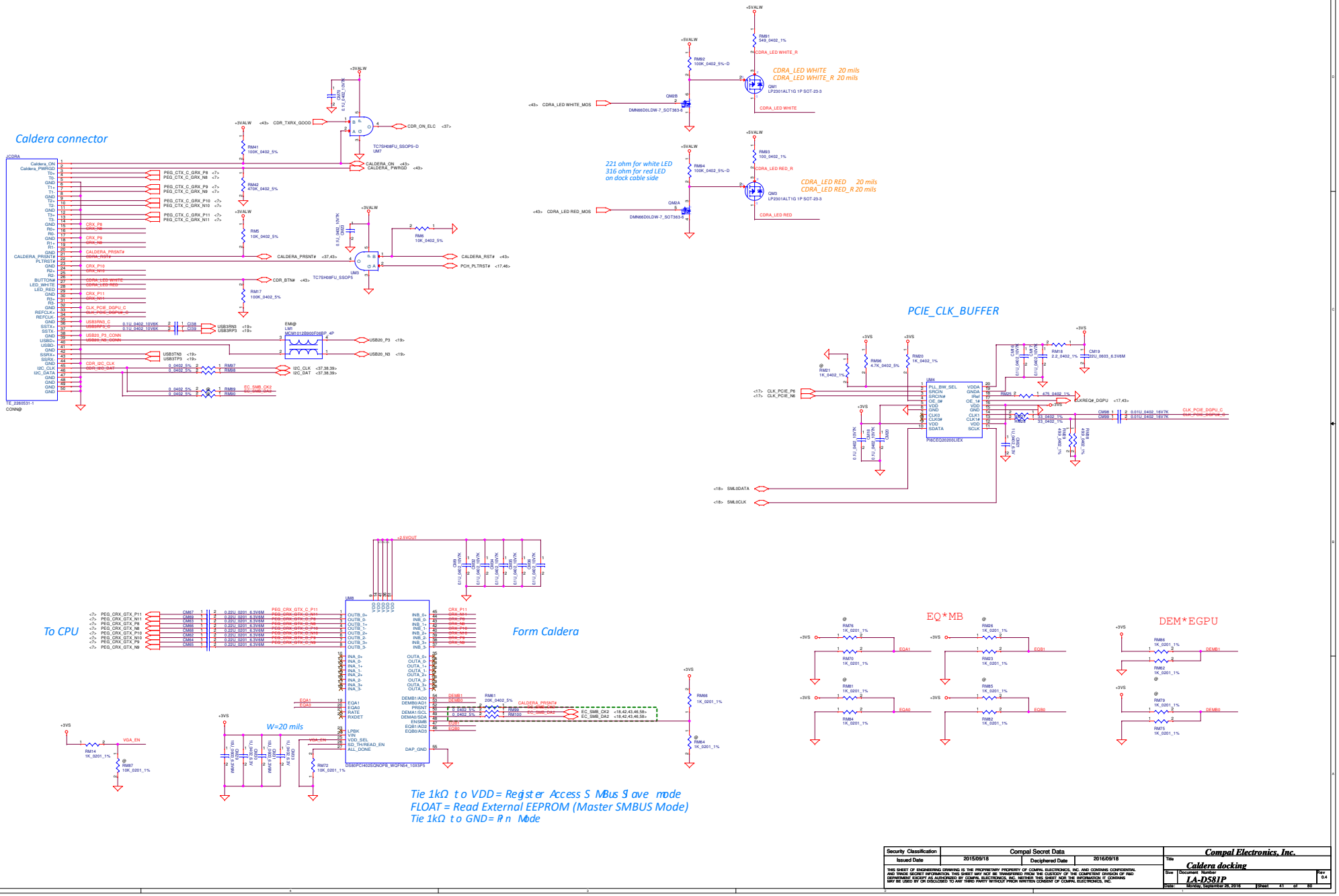



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



| | | | |
|---|---|---|---|
| Title | NKRO KB | | |
| Size | Document Number | | Rev |
| D | LA-D581P | | 0.4 |
| Date: | Wednesday, September 07, 2016 | Sheet | 46 of 80 |




| | | | |
|---|---|---|---|
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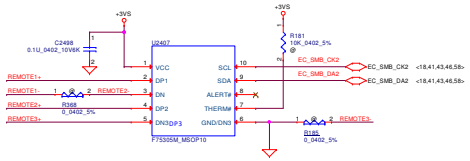
Compal Electronics, Inc.

Title: Caldera docking

Size: Document Number: LA-D581P Rev: 0.4

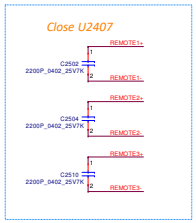
Date: Monday, September 26, 2016 Sheet 41 of 80

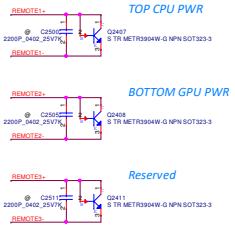
## Fintek thermal sensor---> CPU core, DIMM

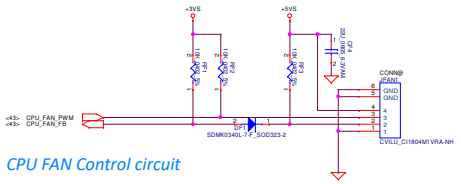


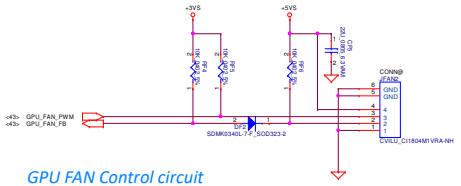

Address 1001_101xb

2nd source
SA000029210-->EMC1403-2-AIZL-TR




| | | | |
|---|---|---|---|
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| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |
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| | | | Size: Document Number: LA-D581P Rev: 0.4 |
| | | | Date: Wednesday, September 07, 2016 Sheet 42 of 80 |

## Power ON circuit

SD028000080 0_0402_5%
SD034120280 12K_0402_1%
SD034150280 15K_0402_1%
SD028200280 20K_0402_1%
SD034270280 27K_0402_1%
SD034330280 33K_0402_1%
SD034430280 43K_0402_1%
SD034560280 56K_0402_1%
SD034750280 75K_0402_1%
SD034100380 100K_0402_1%
SD034130380 130K_0402_1%
SD034160380 160K_0402_1%
SD034200380 200K_0402_1%
SD000001B80 240K_0402_1%
SD00000G280 270K_0402_1%
SD034330380 330K_0402_1%
SD028430380 430K_0402_1%

+3VLP
RE63 100K_0402_5%
@SW1
ON/OFF#
ON/OFF# <38>
TST71A-N-220-S017 SPST
@SW2
TST71A-N-220-S017 SPST
CE27 0.1U_0402_16V7K

+3VALW
CE29 0.1U_0402_10V7K
CE30 0.1U_0402_10V7K
@EMI@ CE31 1000P_0402_50V7K
@EMI@ CE32 1000P_0402_50V7K
EMI@ LE1 FBMA-L11-160808-800LMT_0603
+EC_VCCA
CE33 0.1U_0402_10V7K
ECAGND
ECAGND <61>

+3VLP
9 22 36 96 111 125 67

UE5
KB9022QD_LQFP128_14X14

VCC_LPC VCC VCC VCC VCC VCC AVCC

RE646 0_0201_5%
<20,55> DGPU_PWR_EN
<19> KB_RST#
<19> SERIRQ
<19> LPC_FRAME#
<19> LPC_AD3
<19> LPC_AD2
<19> LPC_AD1
<19> LPC_AD0
<19> CLK_PCI_LPC
<20> EC_SCI#
<18> PM_SLP_SUS#

GATEA20/GPIO00
KBRST#/GPIO01
SERIRQ
LPC_FRAME#
LPC_AD3
LPC_AD2
LPC_AD1
LPC_AD0
CLK_PCI_EC
PCIRST#/GPIO05
EC_RST#
EC_SCI#/GPIO0E
CLKRUN#/GPIO1D

LPC & MISC

@EMI@ CE36 0.1U_0402_10V7K
@EMI@ RE89 0_0402_5%
<6,17,28,29,30,56> PCIRST#
ESD@ CE34 0.047U_0402_16V4Z

PWM Output
EC_VCCST_PG/GPIO0F
BEEP#/GPIO10
EC_FAN_PWM/GPIO12
AC_OFF/GPIO13
CDRA_LED WHITE_MOS <41>
BEEP# <31>
CPU_FAN_PWM <42>
GPU_FAN_PWM <42>

CE35 100P_0402_50V8J ECAGND

AD Input
VCIN1_BATT_TEMP/AD0/GPIO38
VCIN1_BATT_DROP/AD1/GPIO39
ADP_I/AD2/GPIO3A
AD_BID/AD3/GPIO3B
AD4/GPIO42
AD5/GPIO43
VCIN_BATT_TEMP <61,62>
PCIE_WAKE# <18,30>
ADP_I <61,62>
AD_BID
USBCHG_DET_EC# <35>
ENBKL <24>

DA Output
DA0/GPIO3C
EN_DFAN1/DA1/GPIO3D
DA2/GPIO3E
DA3/GPIO3F
EN_INVPWR <25>
TBT_PCIE_WAKE# <56>
ME_SUS_PWR_ACK <18>
LCD_TEST <25>

PS2 Interface
EC_MUTE#/PSCLK1/GPIO4A
USB_EN#/PSDAT1/GPIO4B
PSCLK2/GPIO4C
PSDAT2/GPIO4D
TP_CLK/GPIO4E
TP_DATA/GPIO4F
I2C0_SCL_EC <31,32>
I2C0_SDA_EC <31,32>
KSI20 <40>
KSI21 <40>
TP_CLK <38>
TP_DATA <38>
TP_CLK
TP_DATA

SPI Device Interface
ENKBL/GPXIOA00
WOL_EN/GPXIOA01
ME_EN/GPXIOA02
VCIN0_PH1/GPXIOD00
SUSACK# <18>
EDP_SW <20,24>
ME_EN <18>
VCIN0_PH1 <61>

SPI Flash ROM
MISO/GPIO5B
MOSI/GPIO5C
SPICLK/GPIO5B
SPICS#/GPIO5A
PWRSHARE_EN_EC# <35>
CDR_BTN# <41>
CDRA_LED RED_MOS <41>
3V_F383_ON <37>
3V_F383_ON

Int. K/B Matrix
KSI0/GPIO30
KSI1/GPIO31
KSI2/GPIO32
KSI3/GPIO33
KSI4/GPIO34
KSI5/GPIO35
KSI6/GPIO36
KSI7/GPIO37
KSO0/GPIO20
KSO1/GPIO21
KSO2/GPIO22
KSO3/GPIO23
KSO4/GPIO24
KSO5/GPIO25
KSO6/GPIO26
KSO7/GPIO27
KSO8/GPIO28
KSO9/GPIO29
KSO10/GPIO2A
KSO11/GPIO2B
KSO12/GPIO2C
KSO13/GPIO2D
KSO14/GPIO2E
KSO15/GPIO2F
KSO16/GPIO48
KSO17/GPIO49

<40> KSI0
<40> KSI1
<40> KSI2
<40> KSI3
<40> KSI4 KSI4
<40> KSI5 KSI5
<40> KSI6 KSI6
<40> KSI7 KSI7
<40> KSO0
<40> KSO1
<40> KSO2
<40> KSO3 KSO3
<40> KSO4
<40> KSI16
<40> KSI17
<40> KSI8
<40> KSI9
<40> KSI10
<40> KSI11
<40> KSI12
<40> KSI13
<40> KSI14
<40> KSI15
<40> KSI18
<40> KSI19

+3VALW
RE79 10K_0402_5% EN_WOL#
RE70 10K_0402_5% LID_SW#
RE642 4.7K_0402_5% EC_ESB_CLK
RE643 4.7K_0402_5% EC_ESB_DAT
RE644 100K_0402_5% GPU_ALERT#
RE645 10K_0402_5% USB_PWR_EN
RE647 10K_0402_5% USBC_PWR_EN
RE75 10K_0402_5% PCH_PWROK
RE83 10K_0402_5% 3V_F383_ON

SM Bus
EC_SMB_CK1
EC_SMB_DA1
EC_SMB_CK2
EC_SMB_DA2
<61,62> EC_SMB_CK1
<61,62> EC_SMB_DA1
<18,41,42,46,58> EC_SMB_CK2
<18,41,42,46,58> EC_SMB_DA2
EC_SMB_CLK1/GPIO44
EC_SMB_DAT1/GPIO45
EC_SMB_CLK2/GPIO46
EC_SMB_DAT2/GPIO47

GPIO
SYS_PWROK
SYS_PWROK/AD7/GPIO41
GPIO50
BATT_CHG_LED#/GPIO52
CAPS_LED#/GPIO53
PWR_LED#/GPIO54
BATT_LOW_LED#/GPIO55
SYSON/GPIO56
VR_ON/GPIO57
DPWROK_EC/GPIO59
EC_CIR_RX/AD6/GPIO40
PM_SLP_S4# <18,45,65>
SYS_PWROK <18>
PD_IRQ# <58>
BATT_CHG_LED# <37>
CAPS_LED <40>
PWR_LED# <38>
BATT_LOW_LED# <37>
SYSON
PCH_DPWROK <18>

+3VALW
+3VS
RE92 2.2K_0201_5% EC_SMB_CK1
RE93 2.2K_0201_5% EC_SMB_DA1
RE94 2.2K_0201_5% EC_SMB_CK2
RE95 2.2K_0201_5% EC_SMB_DA2

GPIO/GPO
PM_SLP_S3#
PM_SLP_S5#
<18,37,45> PM_SLP_S3#
<18,37> PM_SLP_S5#
<56> TBT_RESET_N_EC
<61> PS_ID
EC_ESB_CLK
EC_ESB_DAT
PM_SLP_S3#/GPIO04
GPIO07
GPIO08
GPIO0A
GPIO0B
GPIO0C
AC_PRESENT/GPIO0D
<17,41> CLKREQ#_DGPU
<38> TP_LED_EN
<42> CPU_FAN_FB
<42> GPU_FAN_FB
<28> EC_TX
<28> EC_RX
<18> PCH_PWROK
PWM2/GPIO11
FAN_SPEED1/GPIO14
FANFB1/GPIO15
EC_TX/GPIO16
EC_RX/GPIO17
PCH_PWROK/GPIO18
SUSP_LED#/GPIO19
NUM_LED#/GPIO1A
EC_TX
EC_RX
PCH_PWROK
EC_RTCRST

GPIO/GPO
EC_RSMRST#/GPXIOA03
GPXIOA04
VCIN1_ADP_PROCHOT/GPXIOA05
VCOUT1_PROCHOT#/GPXIOA06
VCOUT0_MAIN_PWR_ON/GPXIOA07
BKOFF#/GPXIOA08
GPXIOA09
PCH_PWR_EN/GPXIOA10
PWR_VCCST_PG/GPXIOA11
EC_RSMRST# <18>
VR_PWRGD <73>
VCIN1_ADP_PROCHOT <61>
VCOUT1_PROCHOT#
VCOUT0_MAIN_PWR_ON# <63>
BKOFF# <25>
PBTN_OUT# <9,18>
CALDERA_ON <41>
RE74 43_0402_1%
PCH_PWR_EN <45,66>

GPI
VCIN1_AC_IN/GPXIOD01
EC_ON/GPXIOD02
ON/OFF#/GPXIOD03
LID_SW#/GPXIOD04
SUSP#/GPXIOD05
GPXIOD06
PECI/GPXIOD07
EC_ON <63>
ON/OFF#
LID_SW#
SUSP# <29,45,56,64,67,76>
USB_PWR_EN <35>
PECI_KB9012
H_PECI <9,16>
VCIN1_AC_IN <18,37,61,62>
EMI@ CE40 100P_0402_50V8J

<66> +1VALWP_PGOOD
<9,45> H_VCCST_PWRGD
PBTN_OUT#/GPIO5D
PM_SLP_S4#/GPIO5E
V18R/VCC_IO2
+V18R
RE76 43_0402_1%
RE24 0_0603_5%
+3VALW

GND GND GND GND GND
11 35 94 113 69
AGND

LE2 FBMA-L11-160808-800LMT_0603
ECAGND

PM_SLP_S3#
CE41 ESD@ 0.1U_0402_10V7K
PM_SLP_S5#
CE45 ESD@ 0.1U_0402_10V7K
Please close to EC

<18> PCH_RTCRST#
QE5 2N7002W-T/R7_SOT323-3
EC_RTCRST
RE650 10K_0402_5%

KSO3
KSI6
KSI7
KSI4
KSI5
EC_TX
EC_RX
JEC
GND1
GND2
ACES_50521-0084N-P01
CONN@

<9,61,62> H_PROCHOT#
<73> VR_HOT#
RE78 0_0402_5%
QE2 2N7002W-T/R7_SOT323-3
+3VS
RE84 10K_0402_5%
VCOUT1_PROCHOT#
RE85 53.6K_0402_5%
CE51 0.033U_0402_25V

Reserve for abnormal shutdown
<61,63> POK
DE2 RB751V-40_SOD323-2 EC_RSMRST#
DE3 RB751V-40_SOD323-2 PCH_PWROK
DE4 RB751V-40_SOD323-2 PCH_DPWROK

+3VALW
RE530 47K_0402_5%
CE83 0.1U_0402_16V7K-D
UE10
KC3810_QFN24_4X4
EC_ESB_CLK
<32> SPEAKER_SEL
EC_ESB_DAT
USBC_PWR_EN
<36> USBC_PWR_EN
<38> ELC_EC#
<58> PD_RESET
<20,46> GC6_FB_EN
<46> GPU_ALERT#
<31> EC_MUTE#
ESB_CLK
GPIO00
RST#
ESB_DAT
GPIO01
GPIO02
GPIO03
GPIO04
GPIO05
GPIO06
GPIO07/CAS_CLK
GND
TEST_EN#
GPIO08/CAS_DAT
GPIO09
GPIO0A
GPIO0B
GPIO0C/PWM0
GPIO0D/PWM1
GPIO0E/PWM2
GPIO0F/PWM3
GPIO10/ESB_RUN#
GPIO11/BaseAddOpt
VCC
EN_WOL#
EC_NVVDD1_EN <55>
EC_FBVDD/Q_EN <55>
EC_PEX_VDD_EN <68>
TYPEC_DET# <36>
EC_NVVDD2_EN <55>
EC_3V3_SYS_EN <55>
EC_1V8_AON_EN <55>
+3VALW
CE52 0.1U_0402_16V4Z

Board ID
+3VALW
RE64 100K_0402_1%
Ra
AD_BID
Rb
RE66 33K_0402_1%
CE28 0.1U_0402_10V7K

+3VALW
CH2 0.1U_0402_16V4Z-D
UH5 AH1806-W-7 SC59 3P OMNIPOLAR SW
VDD
OUTPUT
GND
LID_SW#
LID_SW# <37>
CH1 10P_0402_50V8J~D

+3VS_TOUCH
TP_CLK
TP_DATA
RE100 4.7K_0402_5%
RE101 4.7K_0402_5%

ESD@ CE38 0.1U_0402_10V7K
SYSON <45,64>
CE42 0.1U_0402_10V7K
IMVP_VR_ON <45,73>

LID_SW#
PCH_PWROK
SYS_PWROK
ESD@ CE43 0.1U_0402_10V7K
ESD@ CE44 0.1U_0402_10V7K
ESD@ CE46 0.1U_0402_10V7K

+3VALW
RE91 47K_0402_5%
CE55 0.1U_0402_16V7K-D
RST#
UE6
KC3810_QFN24_4X4
EC_ESB_CLK
<31> DEPOP#_EC
RST#
EC_ESB_DAT
<37,41> CALDERA_PRSNT#
<38> PWR_R_EC
<35> CTL1
<35> CTL2
<46> EC_AC_BAT#
<38> PWR_G_EC
<37> PCIE_GEN3#_GEN2
ESB_CLK
GPIO00
RST#
ESB_DAT
GPIO01
GPIO02
GPIO03
GPIO04
GPIO05
GPIO06
GPIO07/CAS_CLK
GND
TEST_EN#
GPIO08/CAS_DAT
GPIO09
GPIO0A
GPIO0B
GPIO0C/PWM0
GPIO0D/PWM1
GPIO0E/PWM2
GPIO0F/PWM3
GPIO10/ESB_RUN#
GPIO11/BaseAddOpt
VCC
TS_EN
TS_EN <25>
CALDERA_PWRGD <41>
CALDERA_RST# <41>
CDR_TXRX_GOOD <41>
DGPU_PWROK <20>
AMD#_NV <37>
GPU_OVERT# <55>
PWR_B_EC <38>
+3VALW
CE56 0.1U_0402_16V4Z



| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



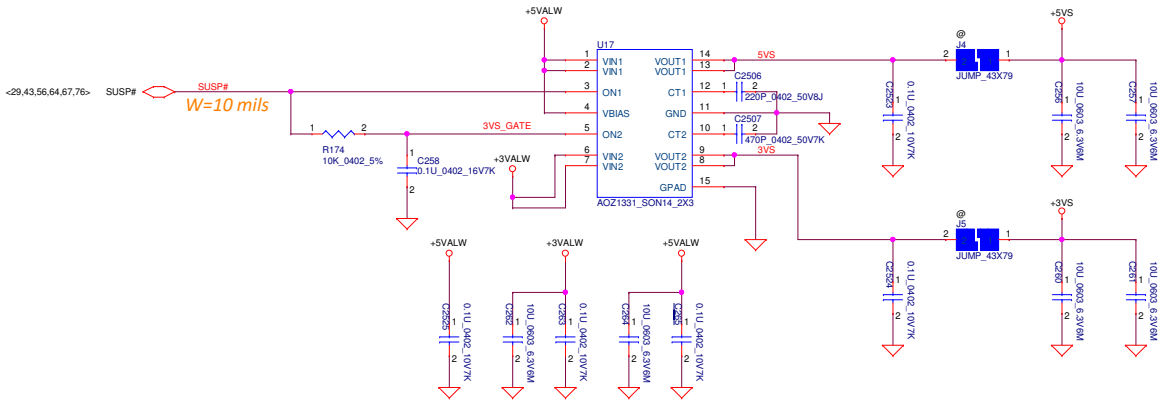
Compal Electronics, Inc.

Title: EC ENE-KB9022/KB3810

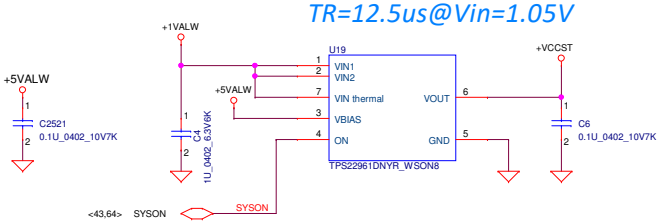
Size: | Document Number: LA-D581P | Rev: 0.4

Date: Wednesday, September 07, 2016 | Sheet 43 of 80

## 20m ohm/6A per channel

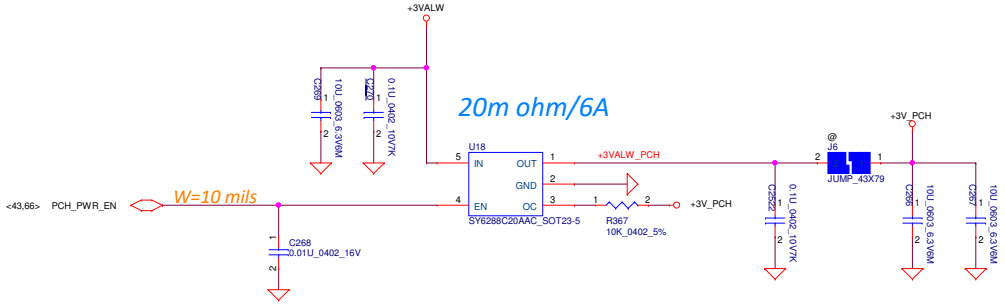



## +VCCST switch
## 4.4mohm/6A
## TR=12.5us@Vin=1.05V

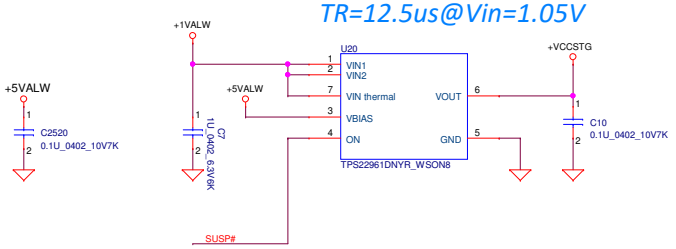



Main source TI SA00007XR00 (SIC TPS22961DNYR WSON 8P LOAD SWITCH)
2nd source AOS SA00008A800(SIC AOZ1334DI-01 DFN 8P SINGLE LOAD SW
3rd source EMC SA00008R600(SIC EM5201V DFN3X3 8P LOAD SWITCH)
4st source APEC SA00006V300(SIC APE8939GN3 DFN 8P LOAD SWITCH)

## 20m ohm/6A

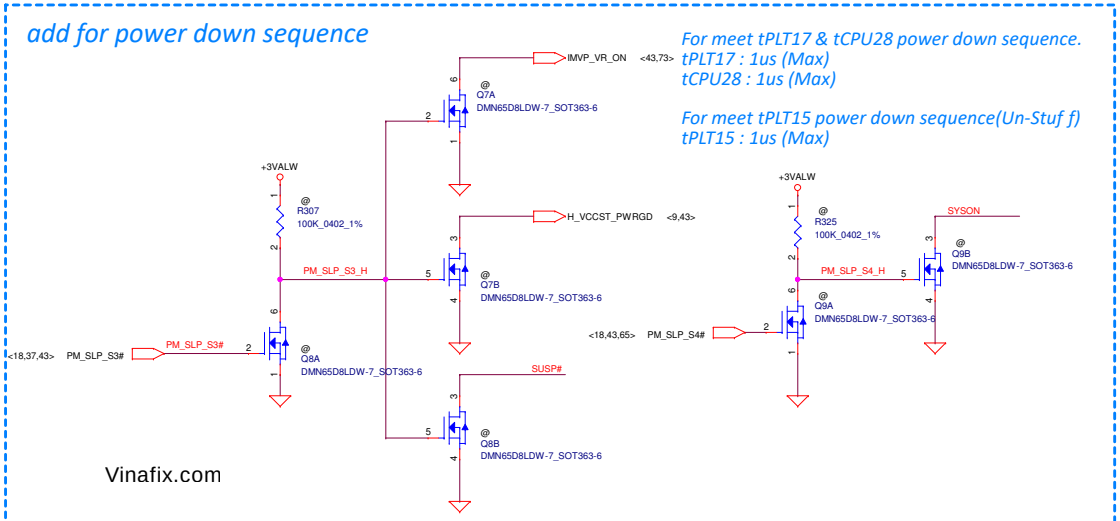



## +VCCSTG switch
## 4.4mohm/6A
## TR=12.5us@Vin=1.05V




Main source TI SA00007XR00 (SIC TPS22961DNYR WSON 8P LOAD SWITCH)
2nd source AOS SA00008A800(SIC AOZ1334DI-01 DFN 8P SINGLE LOAD SW
3rd source EMC SA00008R600(SIC EM5201V DFN3X3 8P LOAD SWITCH)
4st source APEC SA00006V300(SIC APE8939GN3 DFN 8P LOAD SWITCH)

## add for power down sequence




*For meet tPLT17 & tCPU28 power down sequence.*
*tPLT17 : 1us (Max)*
*tCPU28 : 1us (Max)*

*For meet tPLT15 power down sequence(Un-Stuf f)*
*tPLT15 : 1us (Max)*

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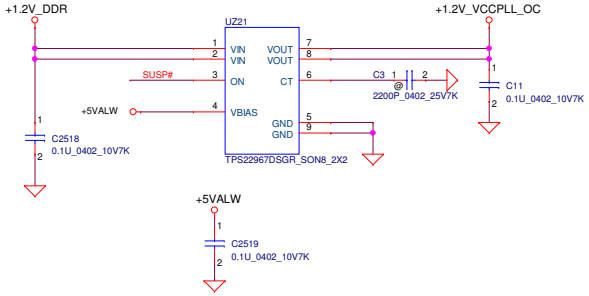
## +1.2V_VCCPLL_OC switch
## 22mohm/4A
## TR=520us@Vin=0.8V




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |

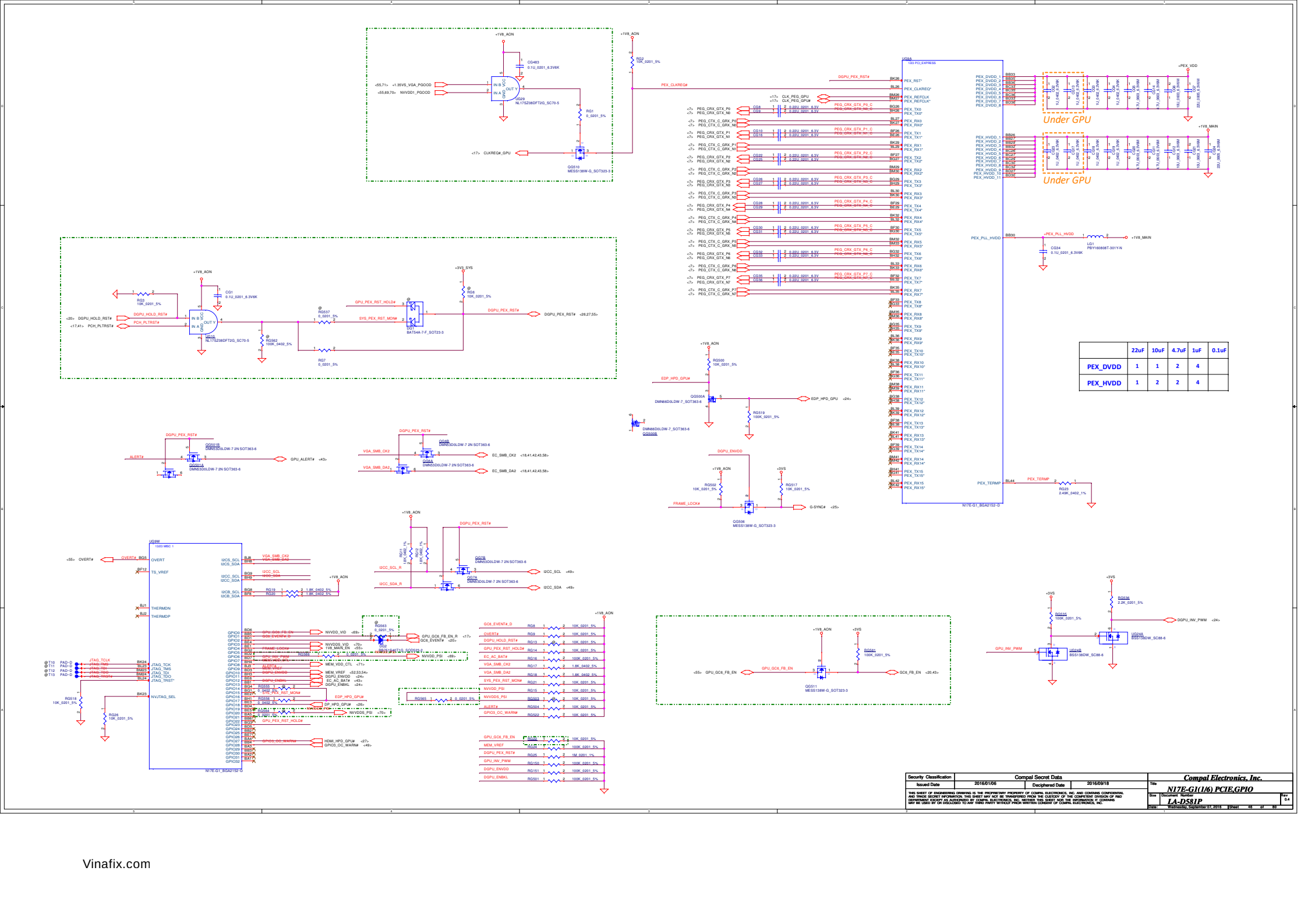


**Compal Electronics, Inc.**

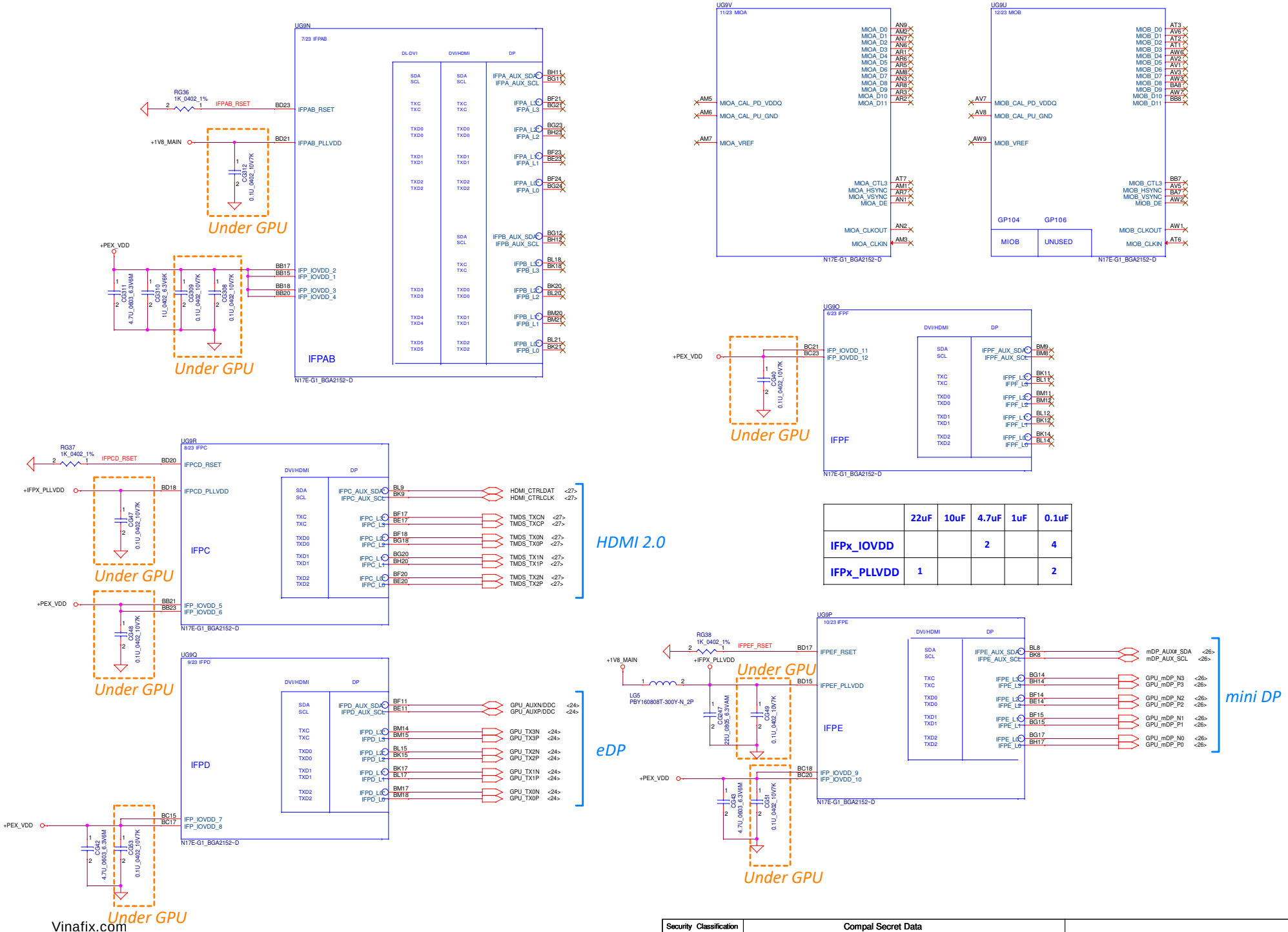
Title: **DC/DC interface**

Size: | Document Number: **LA-D581P** | Rev: 0.4

Date: Wednesday, September 07, 2016 | Sheet 45 of 80




| | 22uF | 10uF | 4.7uF | 1uF | 0.1uF |
|---|---|---|---|---|---|
| PEX_DVDD | 1 | 1 | 2 | 4 | |
| PEX_HVDD | 1 | 2 | 2 | 4 | |




| | 22uF | 10uF | 4.7uF | 1uF | 0.1uF |
|---|---|---|---|---|---|
| IFPx_IOVDD | | | 2 | | 4 |
| IFPx_PLLVDD | 1 | | | | 2 |

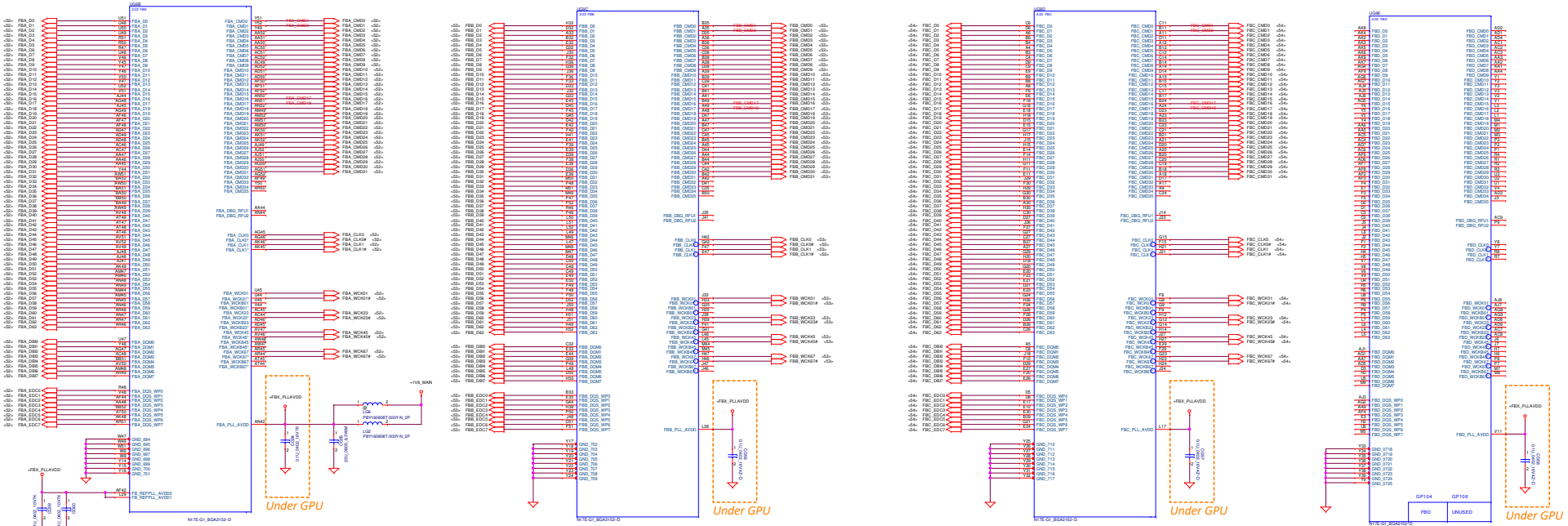
| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



Title: N17E-G1(2/6) eDP,HDMI,mDP

| Size | Document Number | Rev |
|---|---|---|
| C | LA-D581P | 0.4 |

Date: Wednesday, September 07, 2016 | Sheet 47 of 80




| | 22uF | 10uF | 4.7uF | 1uF | 0.1uF |
|---|---|---|---|---|---|
| FBx_PLL_AVDD | | | | | 4 |



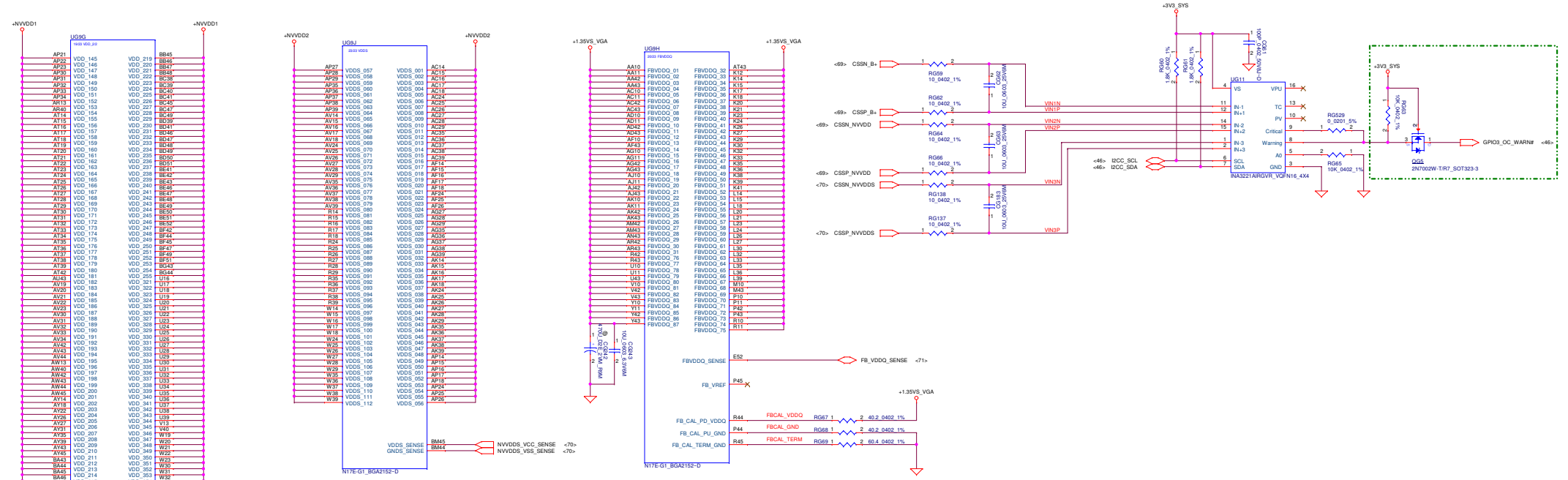
| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



Title: N17E-GI(3/6) MEM interface

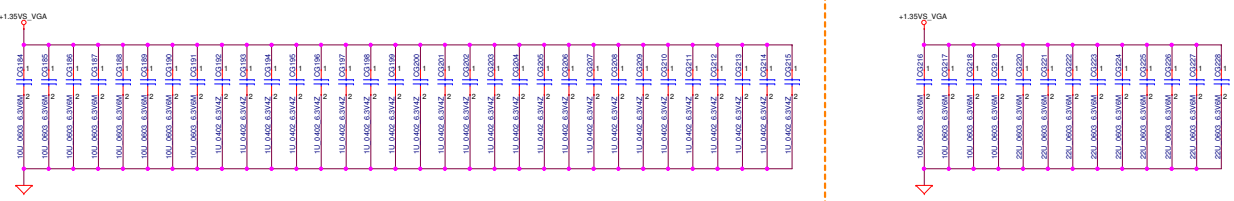
| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-D581P | 0.4 |

Date: Wednesday, September 07, 2016 Sheet 46 of 60




| | 470uF | 22uF | 10uF | 4.7uF | 1uF | 0.1uF |
|---|---|---|---|---|---|---|
| FBVDDQ | 1 | 9 | 13 | | 24 | |

*Place under GPU*



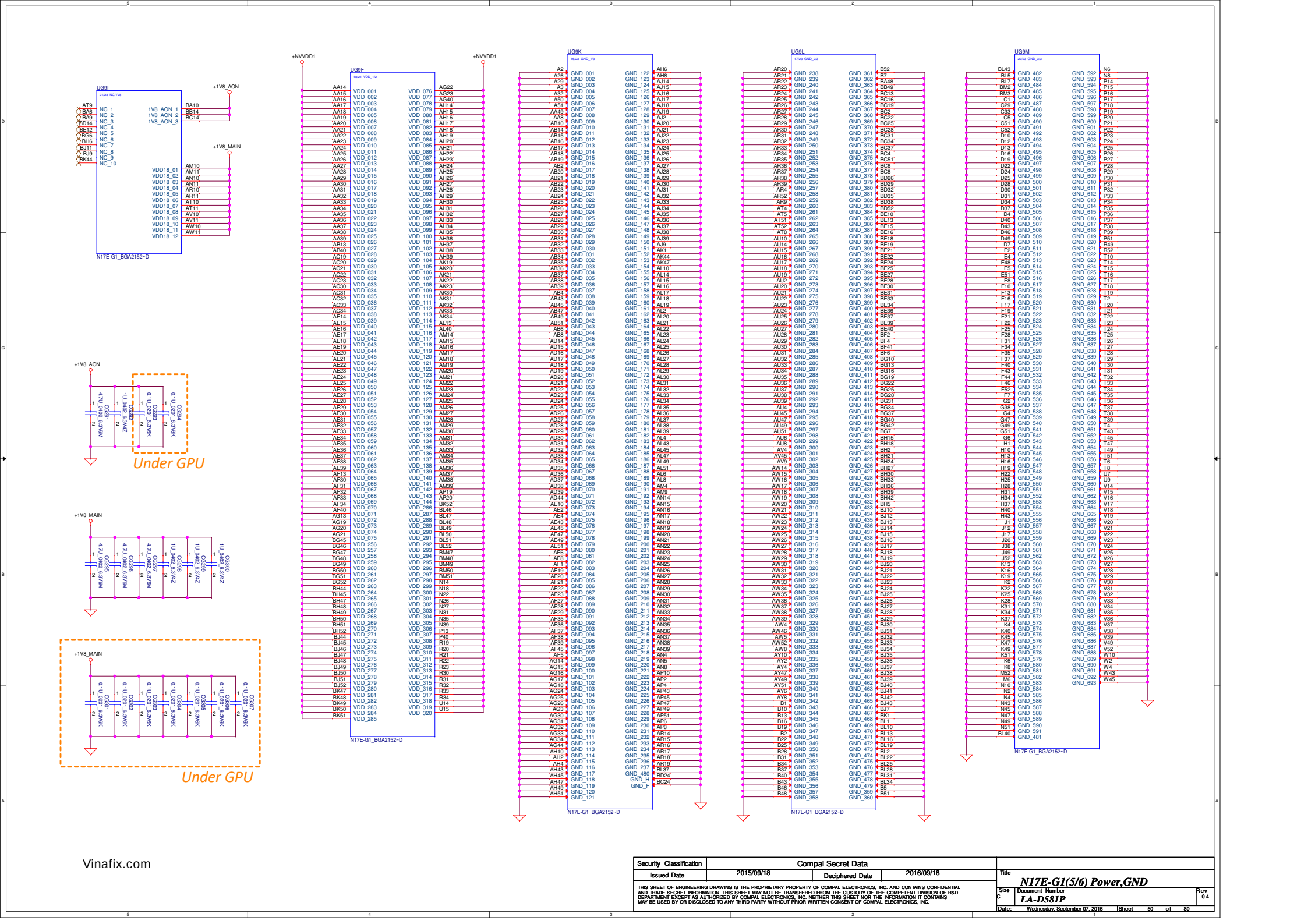

| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



Title: *N17E-G1(4/6) Power*

Size: Custom | Document Number: *LA-D581P* | Rev: 0.4

Date: Wednesday, September 07, 2016 | Sheet 49 of 80

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| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |

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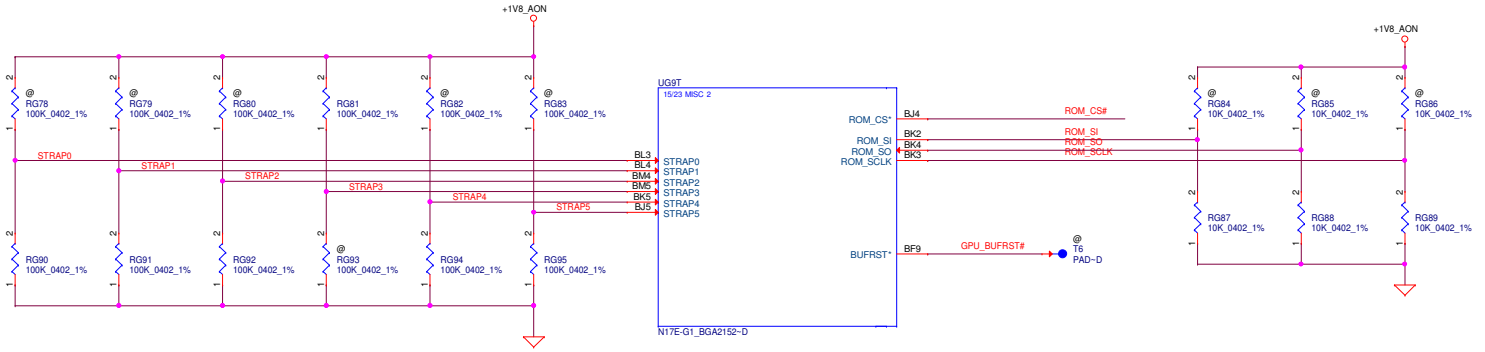
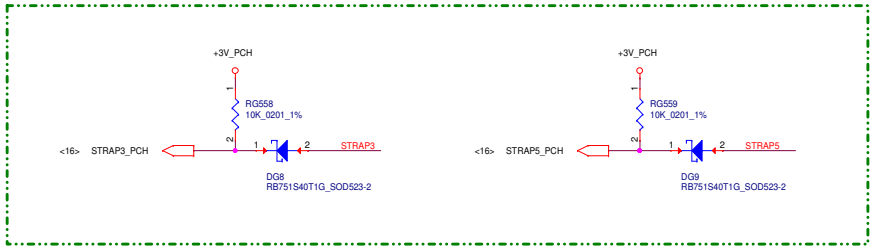
Title: *N17E-G1(5/6) Power,GND*

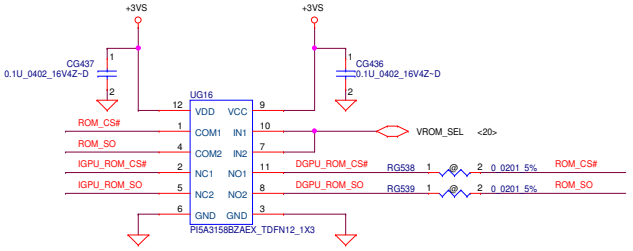
| Size | Document Number | Rev |
|---|---|---|
| C | *LA-D581P* | 0.4 |

Date: Wednesday, September 07, 2016 | Sheet 50 of 80

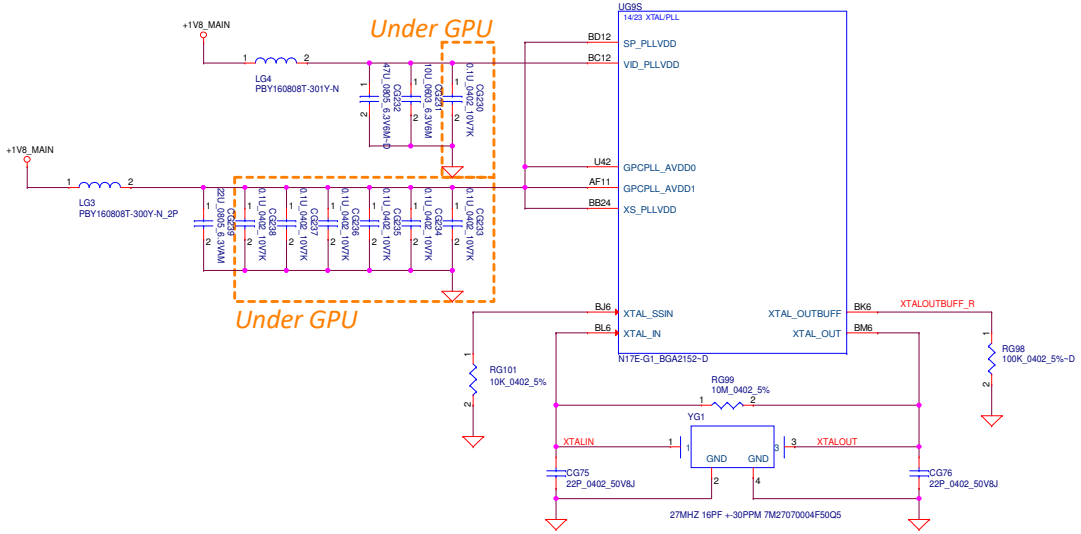
| | 47uF | 22uF | 10uF | 4.7uF | 1uF | 0.1uF |
|---|---|---|---|---|---|---|
| VID_PLLVDD | 1 | | 1 | | | 1 |
| SP_PLLVDD<br>GPCPLL_AVDD | | 1 | | | | 6 |

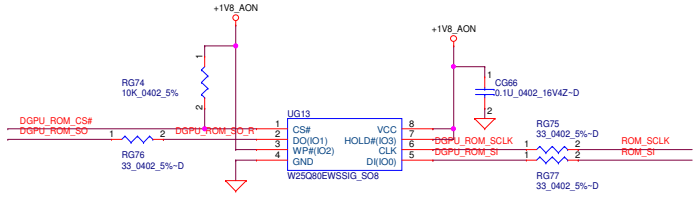


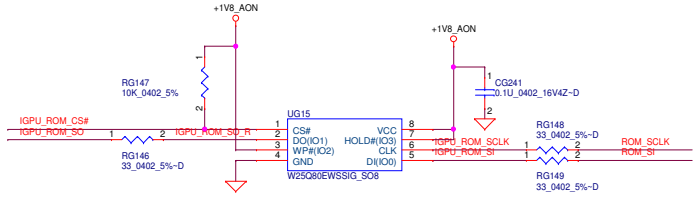




| Funct i on | VROM_SEL |
|---|---|
| COM = NC | L |
| COM = NO | H |




DGPU VBIOS ROM




Opti mus VBIOS ROM

| N17E VRAM | Strap0 | Strap1 | Strap2 | Strap3 | Strap4 | Strap5 | RAMCFG |
|---|---|---|---|---|---|---|---|
| SAMSUNG , K4G80325FB-HC25 | L | L | L | H | L | L | 0 |
| MICRON , MT51J256M32HF-80:A | H | L | L | H | L | L | 1 |
| HYNIX , H5GQ8H24MJR-R4C | L | H | L | H | L | L | 2 |

| N17P VRAM | Strap0 | Strap1 | Strap2 | Strap3 | Strap4 | Strap5 | RAMCFG |
|---|---|---|---|---|---|---|---|
| SAMSUNG , K4G80325FB-HC28 | L | L | L | H | L | L | 0 |
| MICRON , MT51J256M32HF-70:A | H | L | L | H | L | L | 1 |
| HYNIX , H5GC8H24MJR-R0C | L | H | L | H | L | L | 2 |
| SAMSUNG , K4G41325FE-HC28 | H | H | H | H | L | L | 7 |
| HYNIX , H5GC4H24AJR-R0C | L | H | H | H | L | L | 6 |



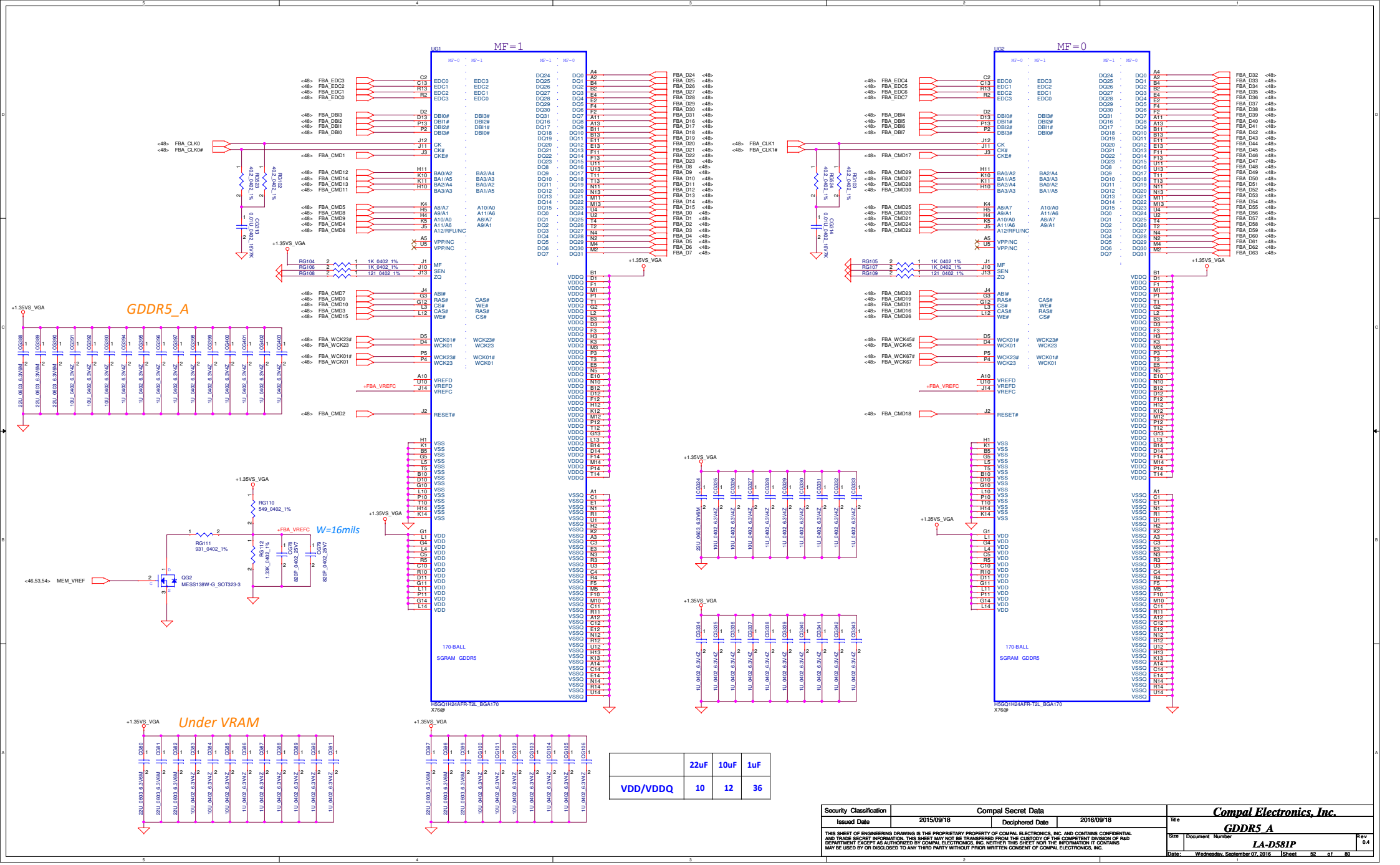
| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



Title: N17E-G1(6/6) strap pin,ROM

| Size | Document Number | Rev |
|---|---|---|
| C | LA-D581P | 0.4 |

Date: Monday, September 26, 2016 Sheet 51 of 80




| | 22uF | 10uF | 1uF |
|---|---|---|---|
| VDD/VDDQ | 10 | 12 | 36 |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |

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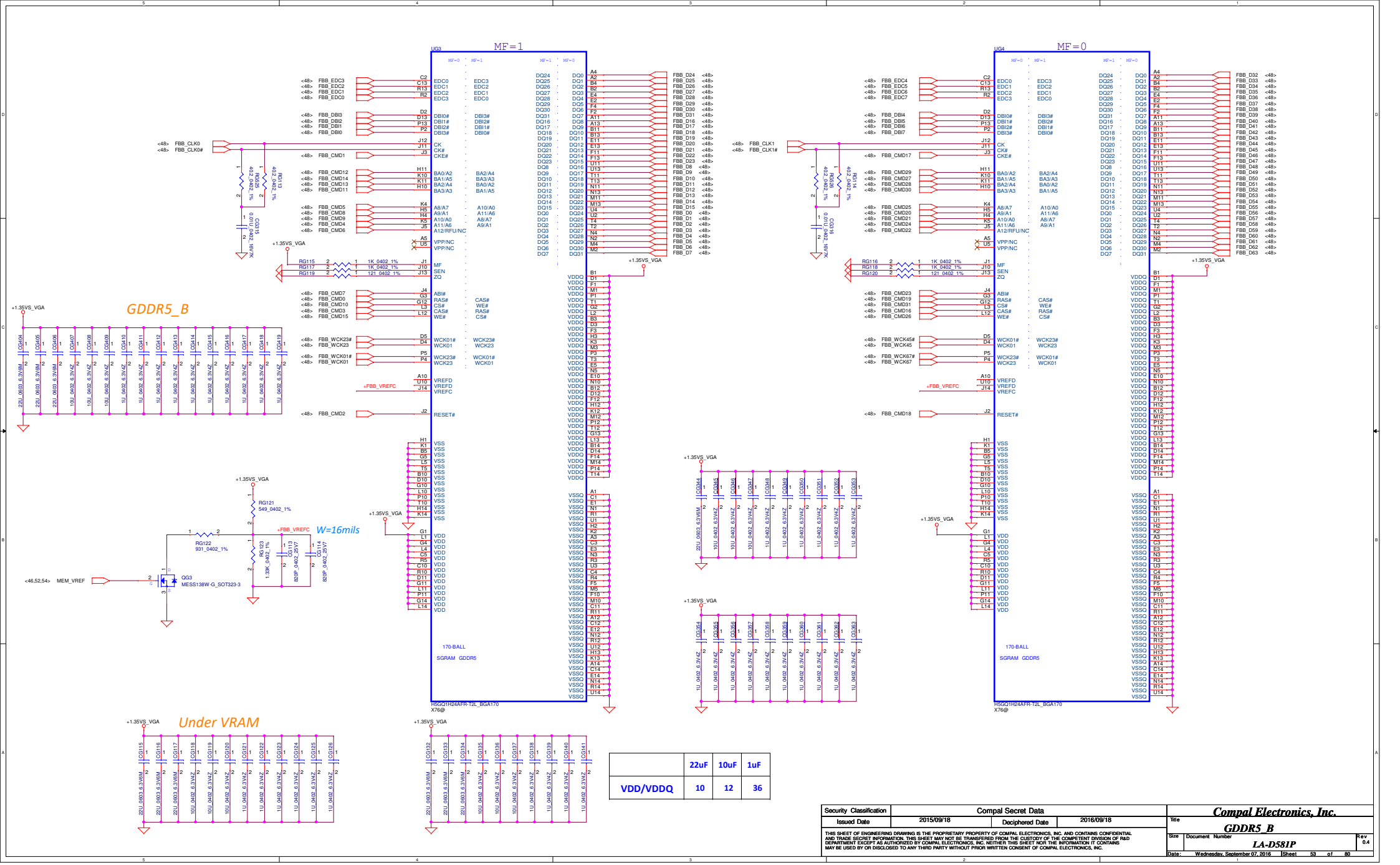
Title: GDDR5_A

Size: | Document Number: LA-D581P | Rev: 0.4

Date: Wednesday, September 07, 2016 | Sheet 52 of 80




| | 22uF | 10uF | 1uF |
|---|---|---|---|
| VDD/VDDQ | 10 | 12 | 36 |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |

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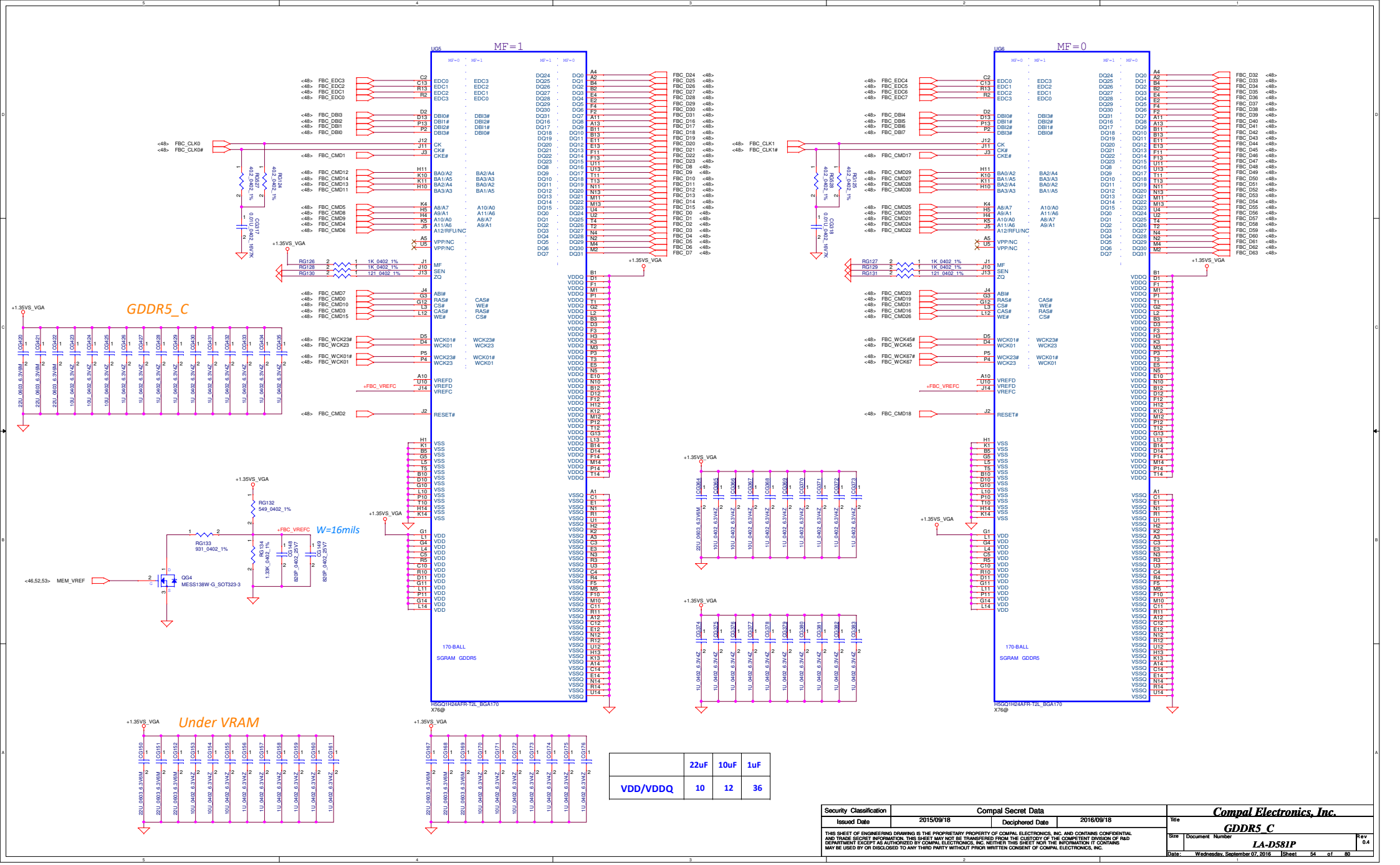
**Compal Electronics, Inc.**

Title: GDDR5_B

Size: | Document Number: LA-D581P | Rev: 0.4

Date: Wednesday, September 07, 2016 | Sheet 53 of 80




| | 22uF | 10uF | 1uF |
|---|---|---|---|
| VDD/VDDQ | 10 | 12 | 36 |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |

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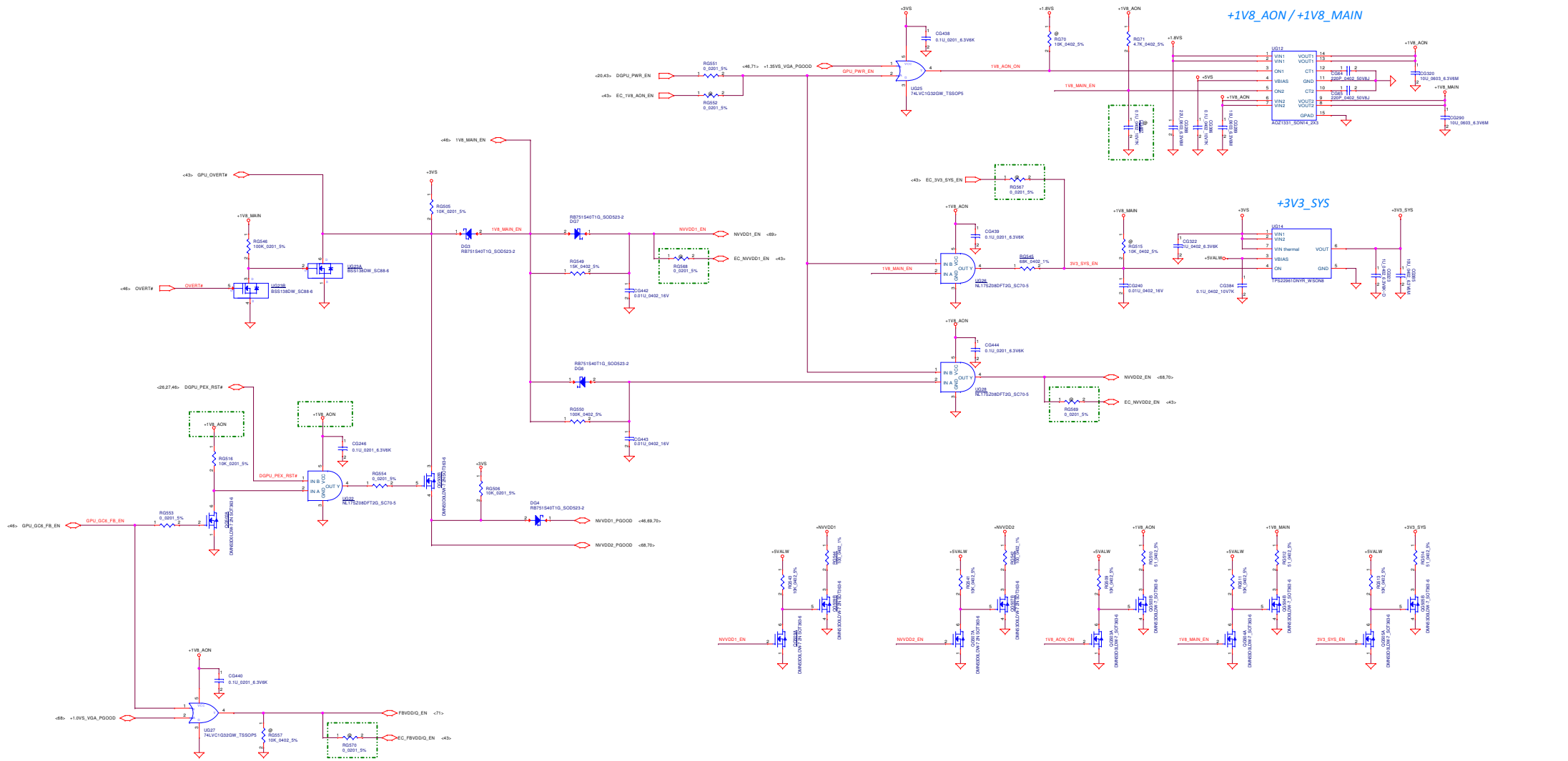
**Compal Electronics, Inc.**

Title: GDDR5_C

Size: | Document Number: LA-D581P | Rev: 0.4

Date: Wednesday, September 07, 2016 | Sheet 54 of 80




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |

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**Compal Electronics, Inc.**

Title: **GPU power control**

Size: Document Number: **LA-D581P** Rev: 0.4

Date: Wednesday, September 07, 2016 Sheet 55 of 80

UT1

S IC DSL6340 SLKYB B0 FC-CSP I/O CONTROL
SA000090N0L
ARES2R1@

UT1

S IC A31 DSL6340 QSCX B0 THUNDERBOLT
SA000090N2L
ARQSR1@

UT1

S IC DSL6340 SLL42 B1 FCCSP 337P THUNDERBOLT A31 !
SA000090N5L
ARQSR3@

PEG X4 Bus

PEG CLK
(From PCH CLKOUT3)

CPU DDI1

Reserve for common DP design

CPU DDI2

UT1A

PCIe GEN3

SINK PORT 0

SOURCE PORT 0

LC GPIO

POC GPIO

SINK PORT 1

Misc

MISC

TBT PORTS

Port A

PORT B

POC

DEBUG

ALPINE-RIDGE_BGA337

Closed to UT1

Close to UT2

JTAG

ACES_50228-0067N-001

CONN@

RPT1

TBT@ 2.2K_0804_8P4R_5%

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| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2016/01/06 | Deciphered Date | 2016/09/18 |

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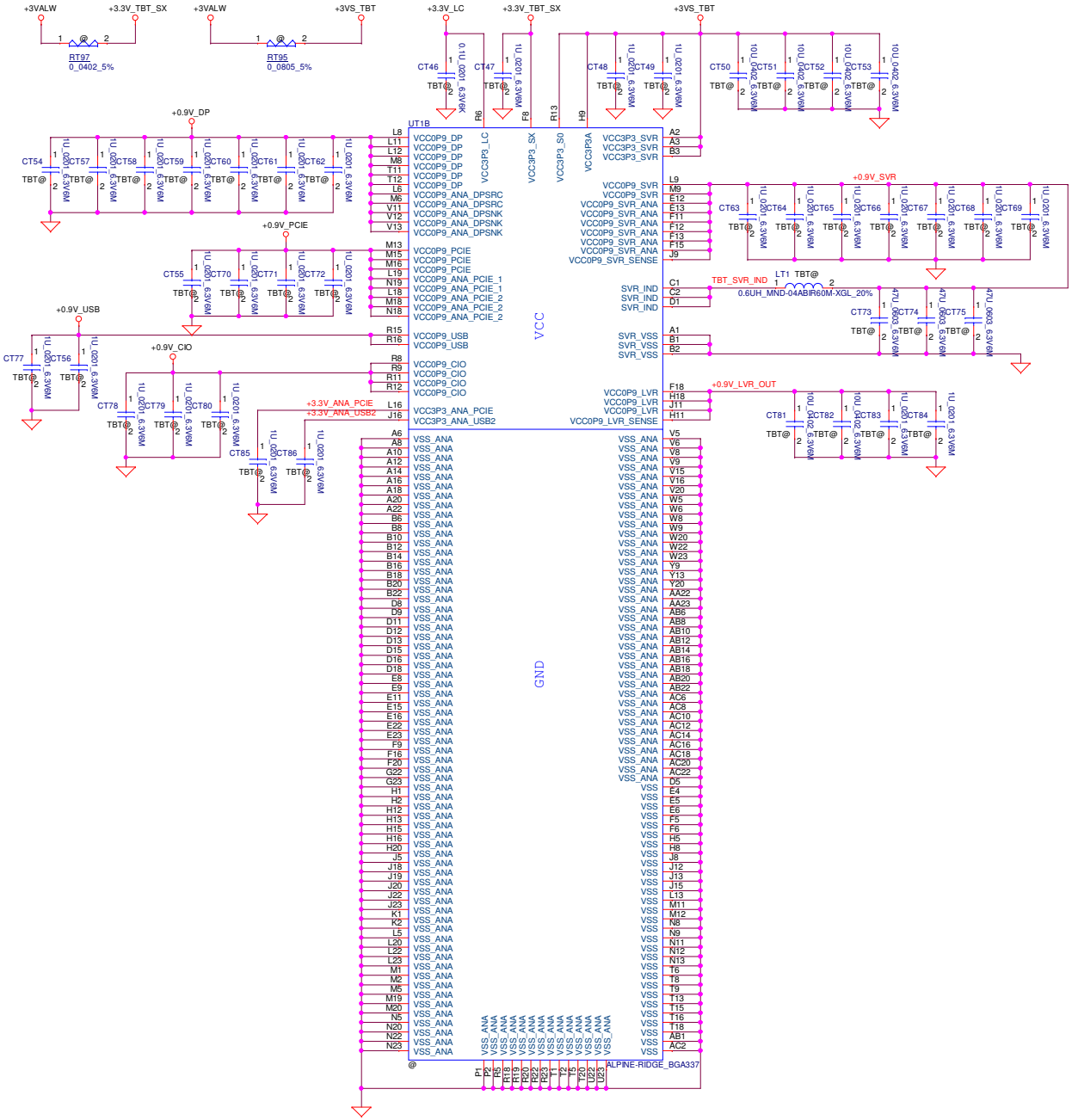
**Compal Electronics, Inc.**

Title: **Thunderbolt (1/2)**

| Size | Document Number | Rev |
|---|---|---|
| | LA-D581P | 0.4 |

Date: Wednesday, September 07, 2016 | Sheet 56 of 80

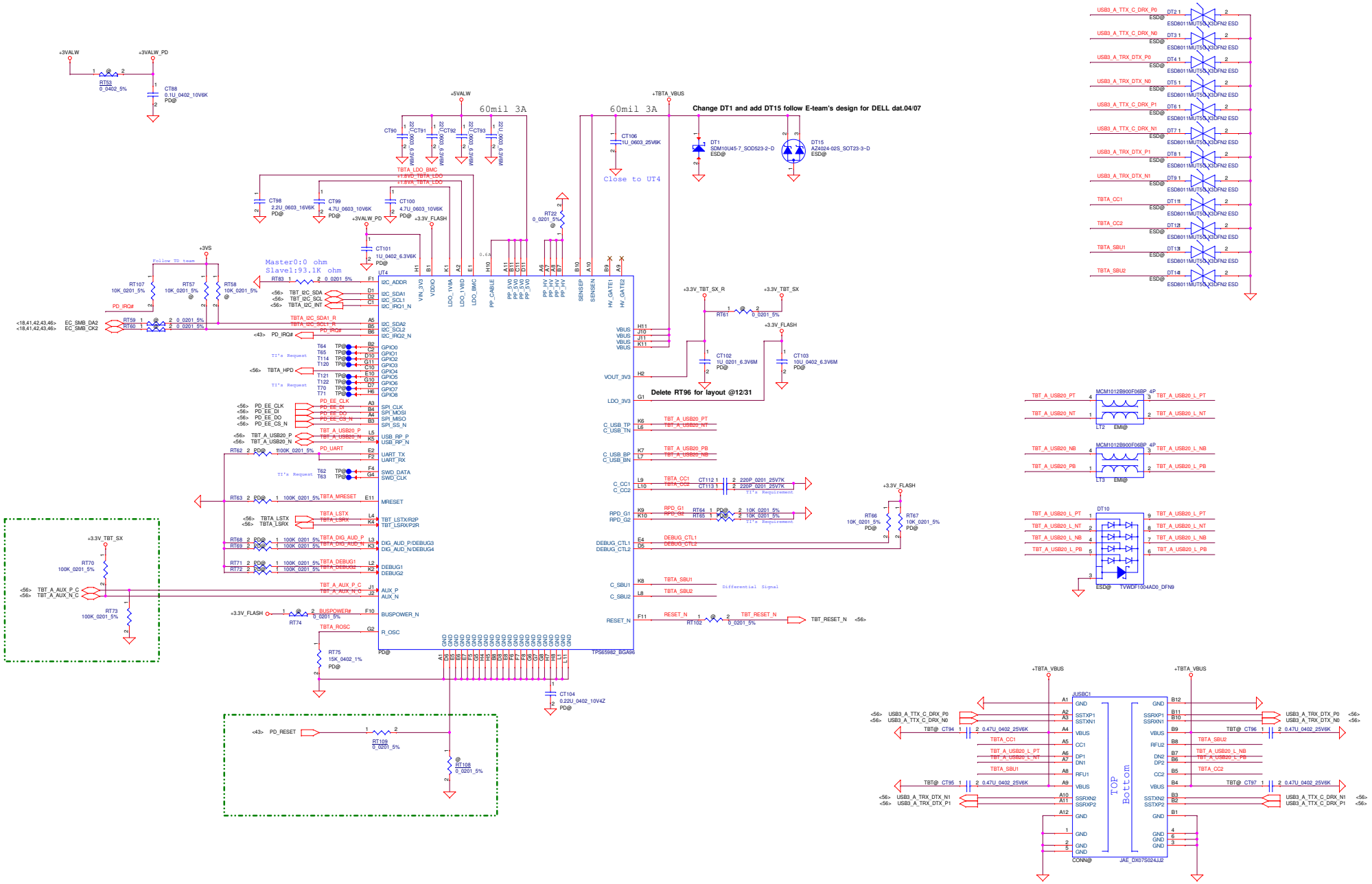





| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/01/06 | Deciphered Date | 2016/09/18 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | Thunderbolt (2/2) | | |
| Size | Document Number | | Rev |
| | LA-D581P | | 0.4 |
| Date: | Wednesday, September 07, 2016 | Sheet | 57 of 80 |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/01/06 | Deciphered Date | 2016/09/18 |

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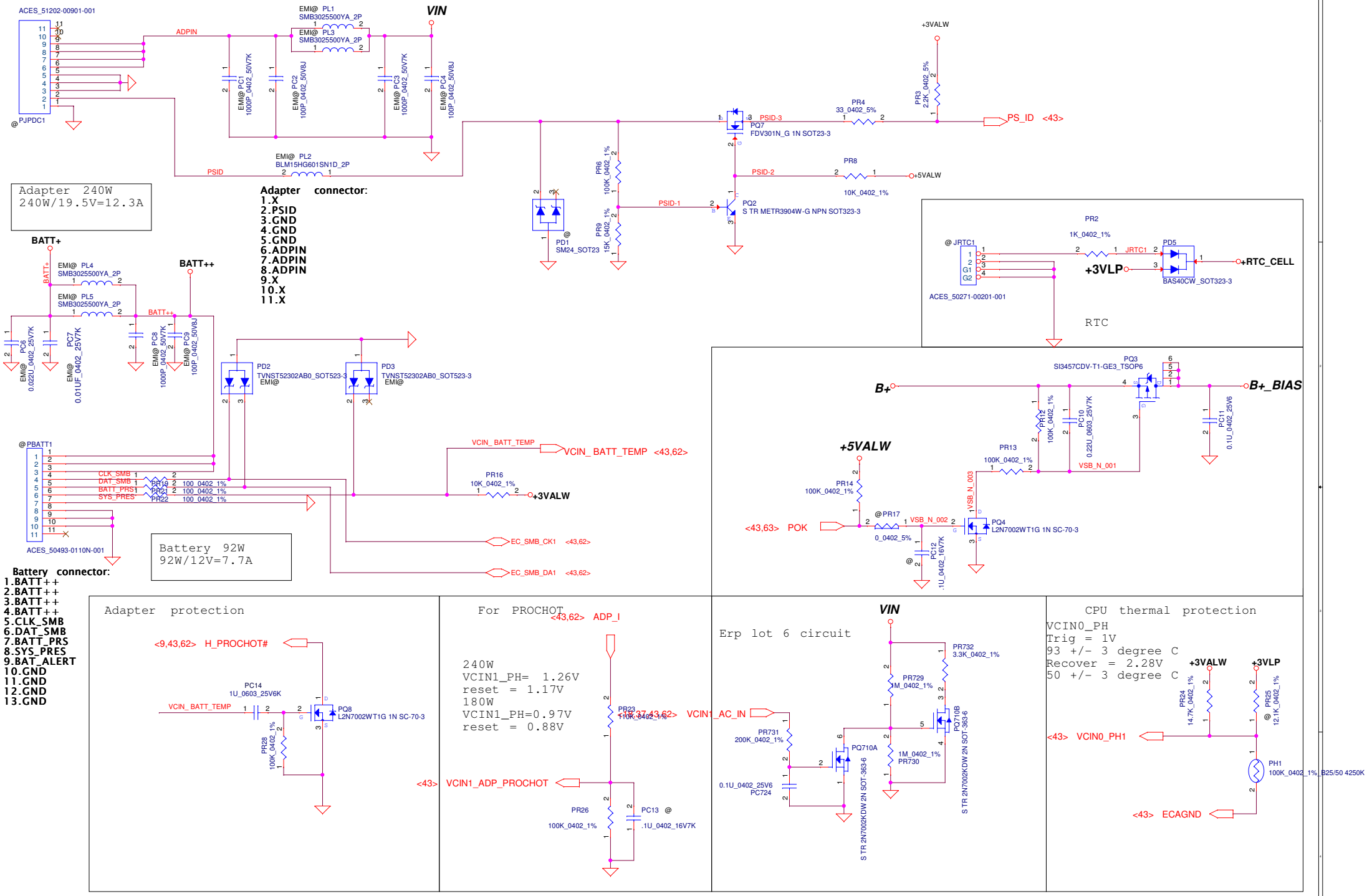
**Compal Electronics, Inc.**

Title: **PD+USB3.1 type C**

Size: | Document Number: **LA-D581P** | Rev: 0.4

Date: Wednesday, September 07, 2016 | Sheet 58 of 80

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| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |



**Compal Electronics, Inc.**

Title: **PWR-DCIN / BATT CONN / OTP**

| Size | Document Number | Rev |
|---|---|---|
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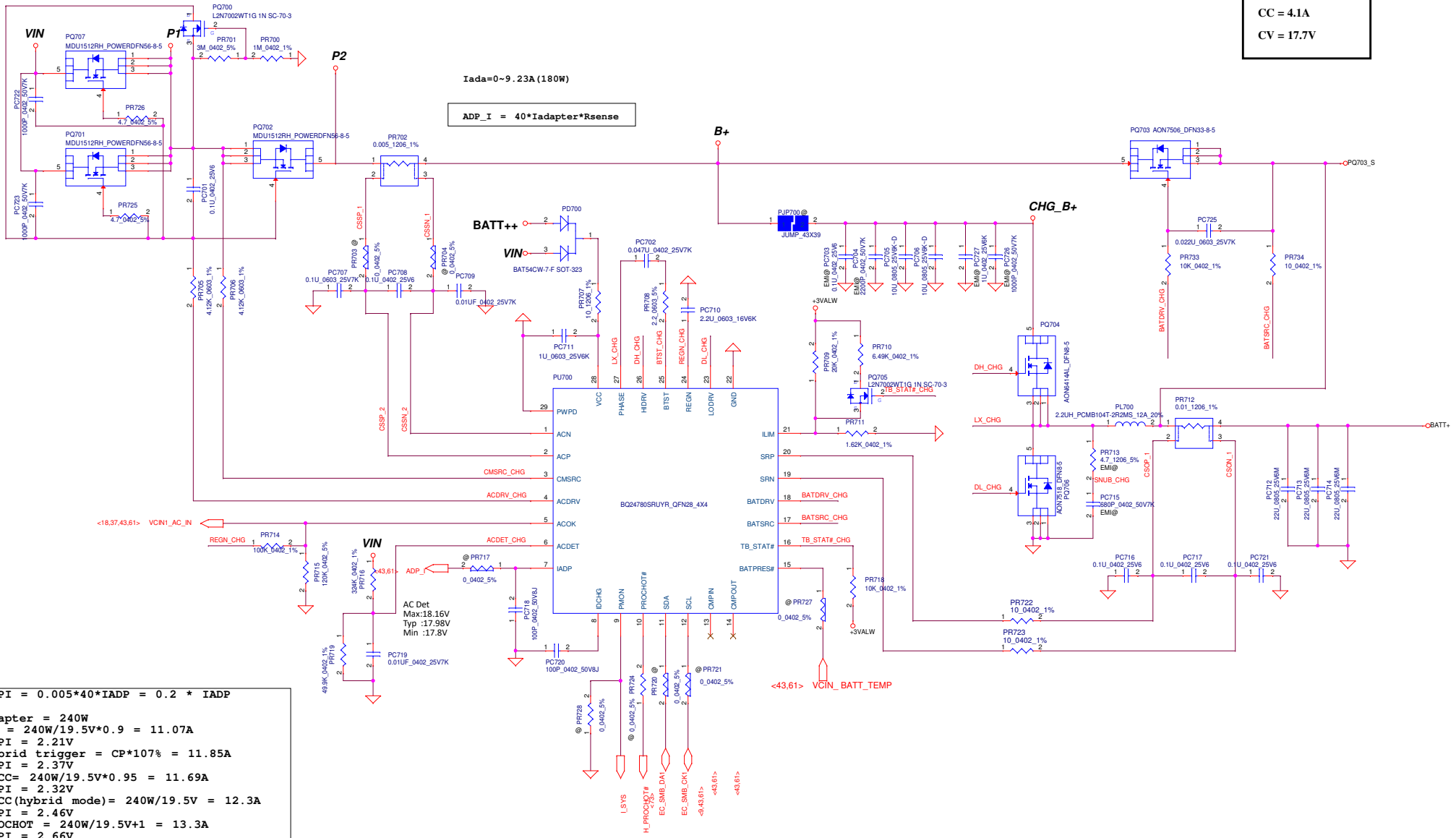


ADPI = 0.005*40*IADP = 0.2 * IADP

Adapter = 240W
CP = 240W/19.5V*0.9 = 11.07A
ADPI = 2.21V
Hybrid trigger = CP*107% = 11.85A
ADPI = 2.37V
IPCC= 240W/19.5V*0.95 = 11.69A
ADPI = 2.32V
IPCC(hybrid mode)= 240W/19.5V = 12.3A
ADPI = 2.46V
PROCHOT = 240W/19.5V+1 = 13.3A
ADPI = 2.66V

Adapter = 180W
CP = 180W/19.5V*0.9 = 8.30A
APDI = 1.66V
Hybrid trigger = CP*107% = 8.88A
ADPI = 1.77V
IPCC = 180W/19.5V*(1*0.95) = 8.77A
ADPI = 1.75V
IPCC(hybrid mode)= 180W/19.5V = 9.23A
ADPI = 1.85V
PROCHOT = 180W/19.5V+1 = 10.23A
ADPI = 2.04V



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| Title | PWR_CHARGER | | |
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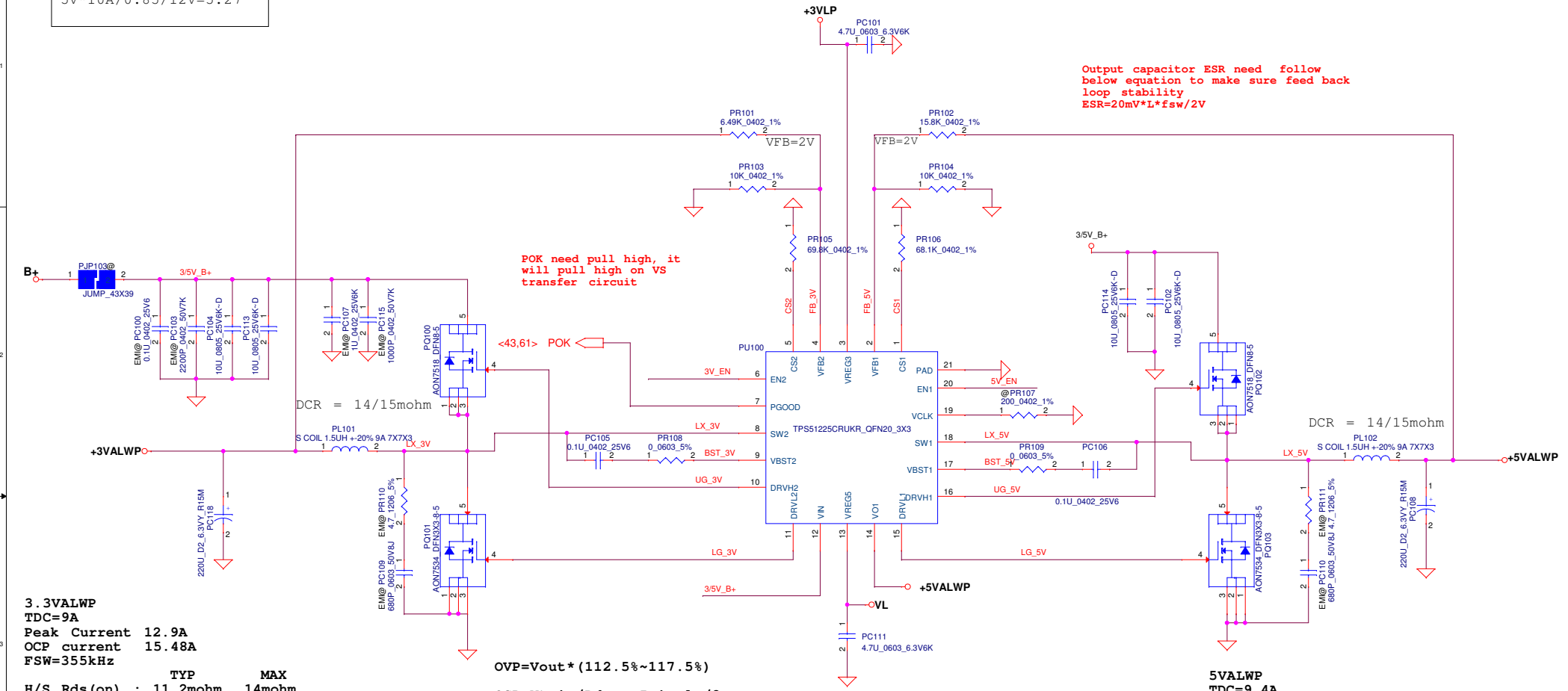
Input Current: 7.5A
3.3V*10A/0.85/12V=2.23
5V*10A/0.85/12V=5.27

Output capacitor ESR need follow below equation to make sure feed back loop stability
ESR=20mV*L*fsw/2V

POK need pull high, it will pull high on VS transfer circuit




**3.3VALWP**
**TDC=9A**
**Peak Current 12.9A**
**OCP current 15.48A**
**FSW=355kHz**

| | TYP | MAX |
|---|---|---|
| H/S Rds(on) | 11.2mohm | 14mohm |
| L/S Rds(on) | 6.7mohm | 8.5mohm |

**OVP=Vout*(112.5%~117.5%)**

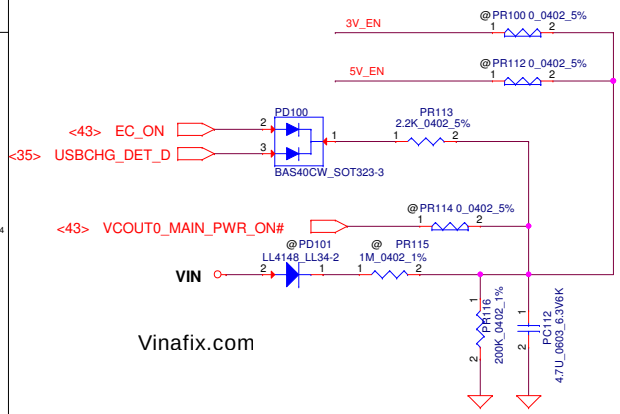
**OCP=Vtrip/Rdson+Iripple/2**
**Vtrip=Ics(min)*Rcs/8+1mV**
**Vcs=Ics*vcs should be in the range of 0.2~2V**

**Vout=VFB*(1+Rtop/Rbot)**
**VFB=2V**

**5VALWP**
**TDC=9.4A**
**Peak Current 13.46A (11.66 + 1.8)**
**OCP current 16.2A**
**FSW=300kHz**

| | TYP | MAX |
|---|---|---|
| H/S Rds(on) | 11.2mohm | 14mohm |
| L/S Rds(on) | 6.7mohm | 8.5mohm |

EN
Rising=1.6~0.3V







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**Compal Electronics, Inc.**

Title: **PWR-3.3VALWP/5VALWP**

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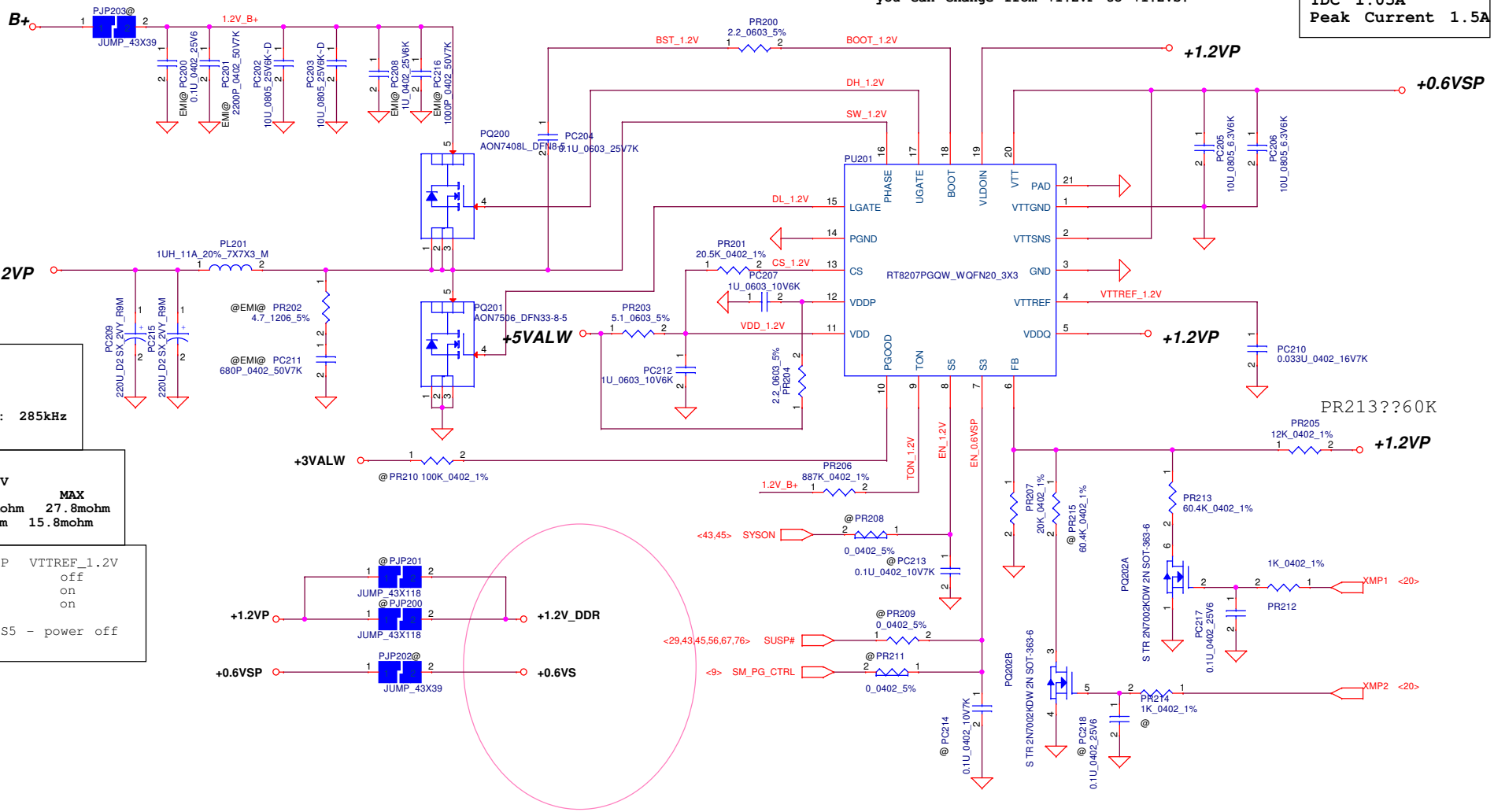
Input Current: 1A
1.2V*8.88A/0.85/12V=1

Pin19 need pull separate from +1.2VP.
If you have +1.2V and +0.6V sequence question,
you can change from +1.2VP to +1.2VS.

0.6VSP
TDC 1.05A
Peak Current 1.5A




1.2VP
TDC=7.66A
Ipeak=10.94A
OCP=13.12A
Switching Frequency: 285kHz

OVP: 110%~120%
VFB=0.75V, Vout=1.2V

| | TYP | MAX |
|---|---|---|
| H/S Rds(on) : | 23.2mohm | 27.8mohm |
| L/S Rds(on) : | 13mohm | 15.8mohm |

| Mode | Level | +0.6VSP | VTTREF_1.2V |
|---|---|---|---|
| S5 | L | off | off |
| S3 | L | off | on |
| S0 | H | on | on |

Note: S3 - sleep ; S5 - power off

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Title: PWR-1.2VP/0.6VSP

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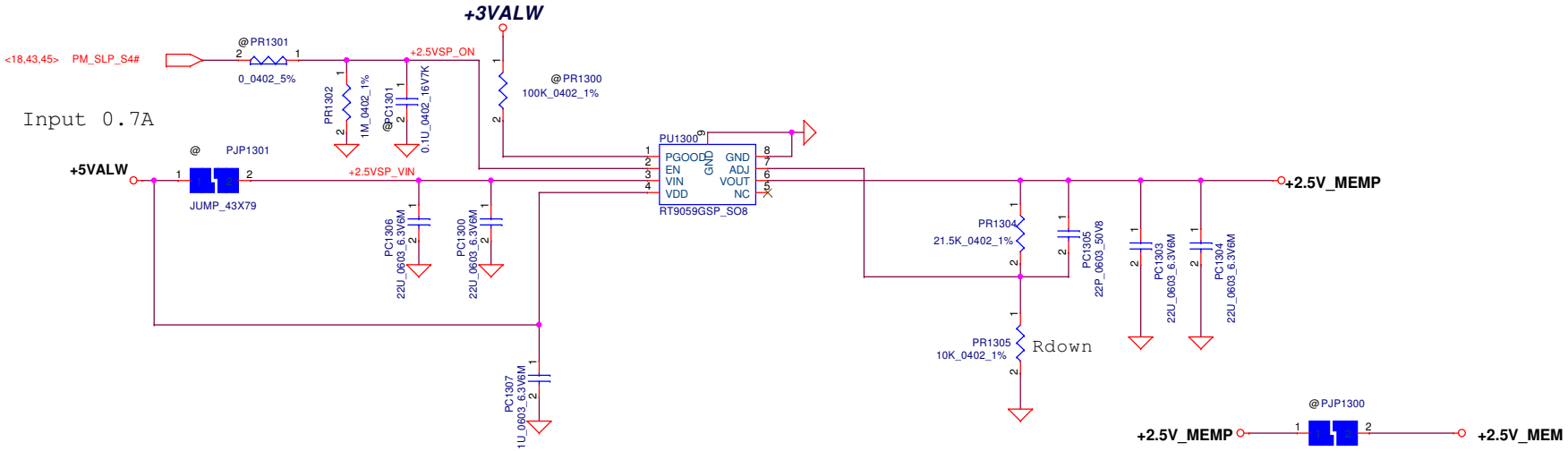


+2.5V_MEM
TDC 0.63A
Peak Current 0.9A
OCP Current 3.5A

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Title: PWR_+2.5V_MEM

Size | Document Number: LA-D581P | Rev: 0.3

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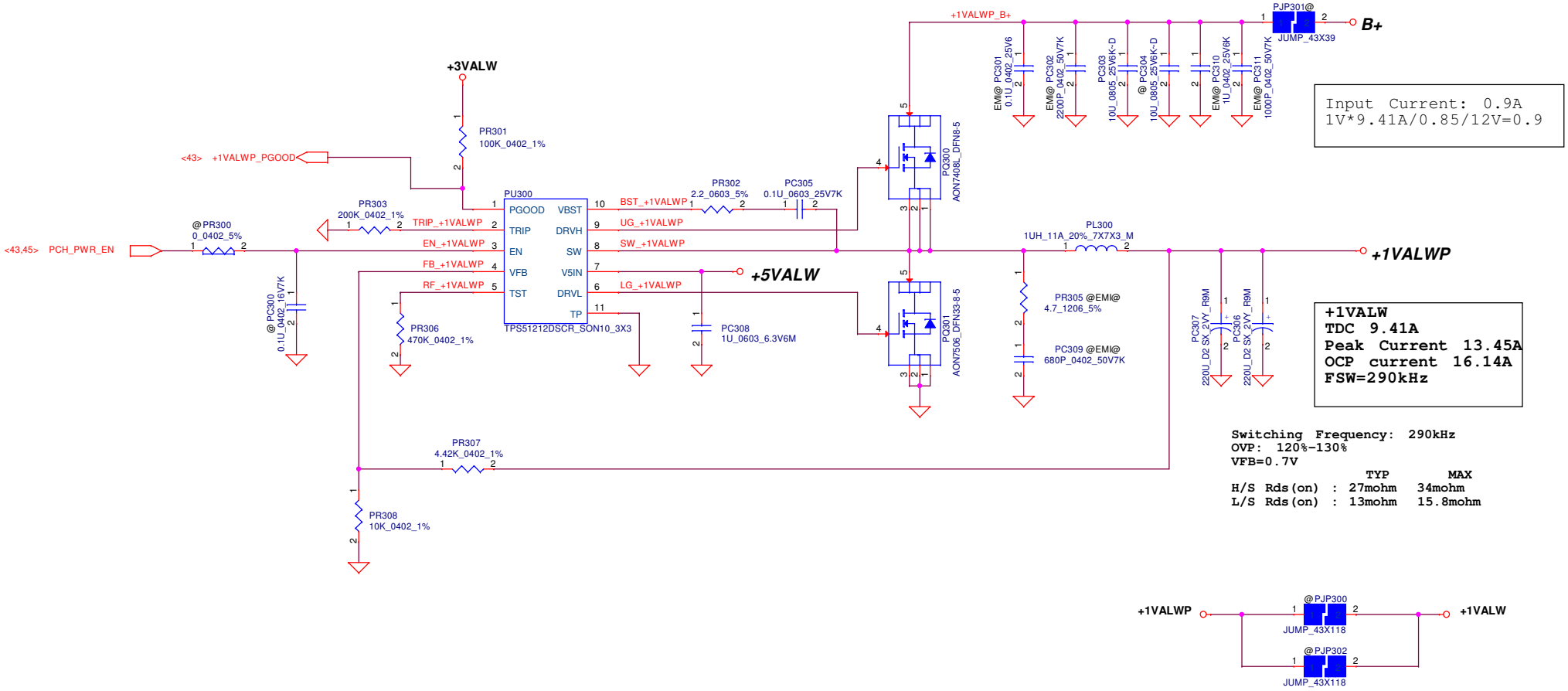


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Title: **PWR-+1VALWP**

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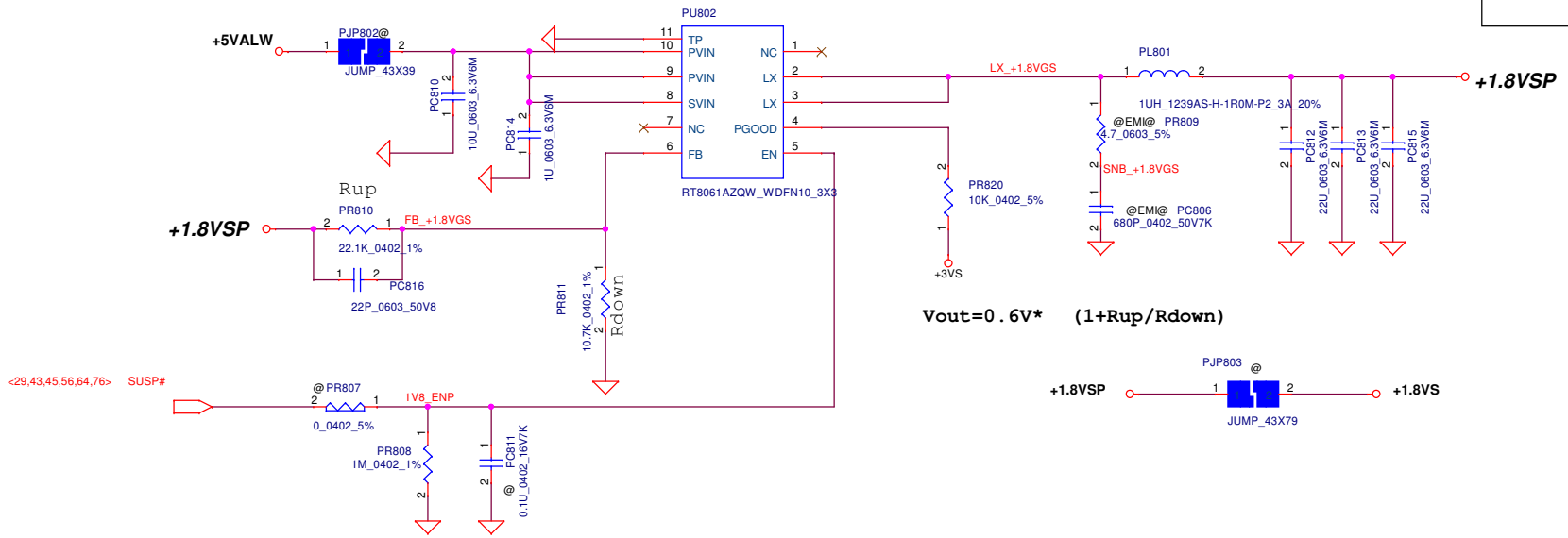
Date: Wednesday, September 07, 2016 | Sheet 66 of 80

+1.8VSP
TDC 2.26A
Peak Current 3A
OCP current 4A
FSW=1MHz

| | TYP | MAX |
|---|---|---|
| Choke DCR | 0.045mohm , | 0.059mohm |

Input 0.4A

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**Compal Electronics, Inc.**

Title: PWR_+1.8VSP/+1.8VGSP

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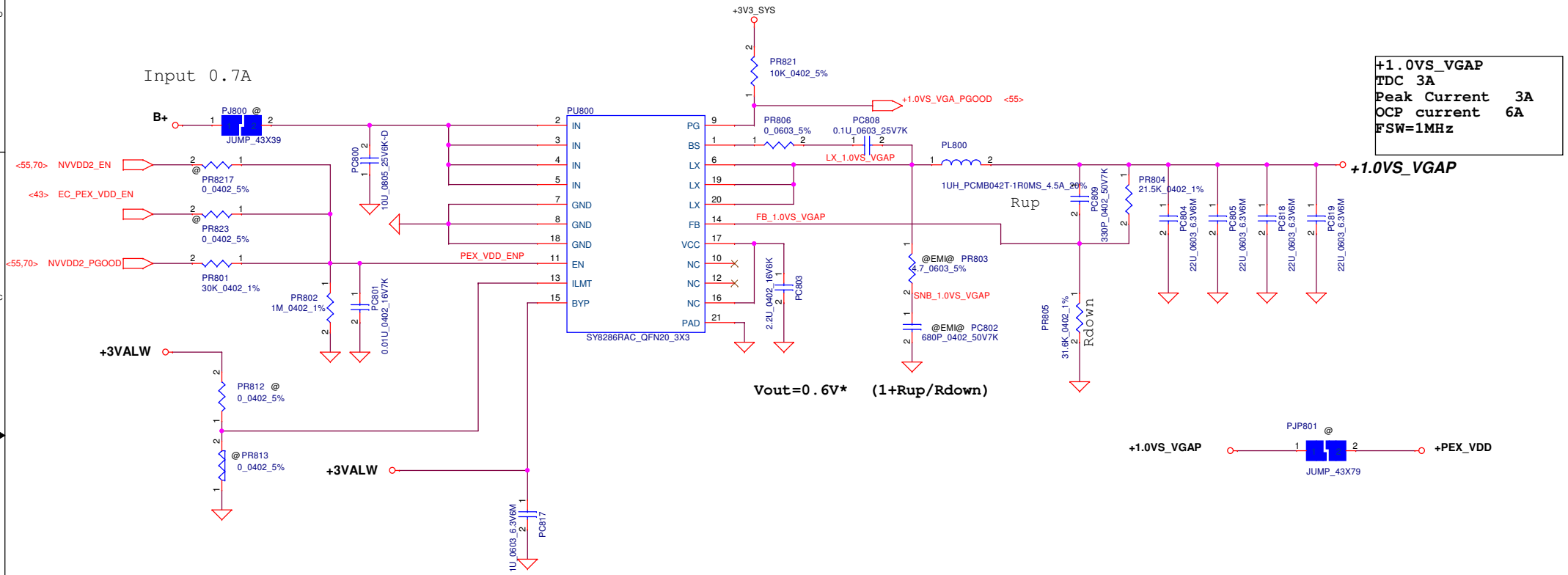


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| Issued Date | 2015/09/18 | Deciphered Date | 2016/09/18 |

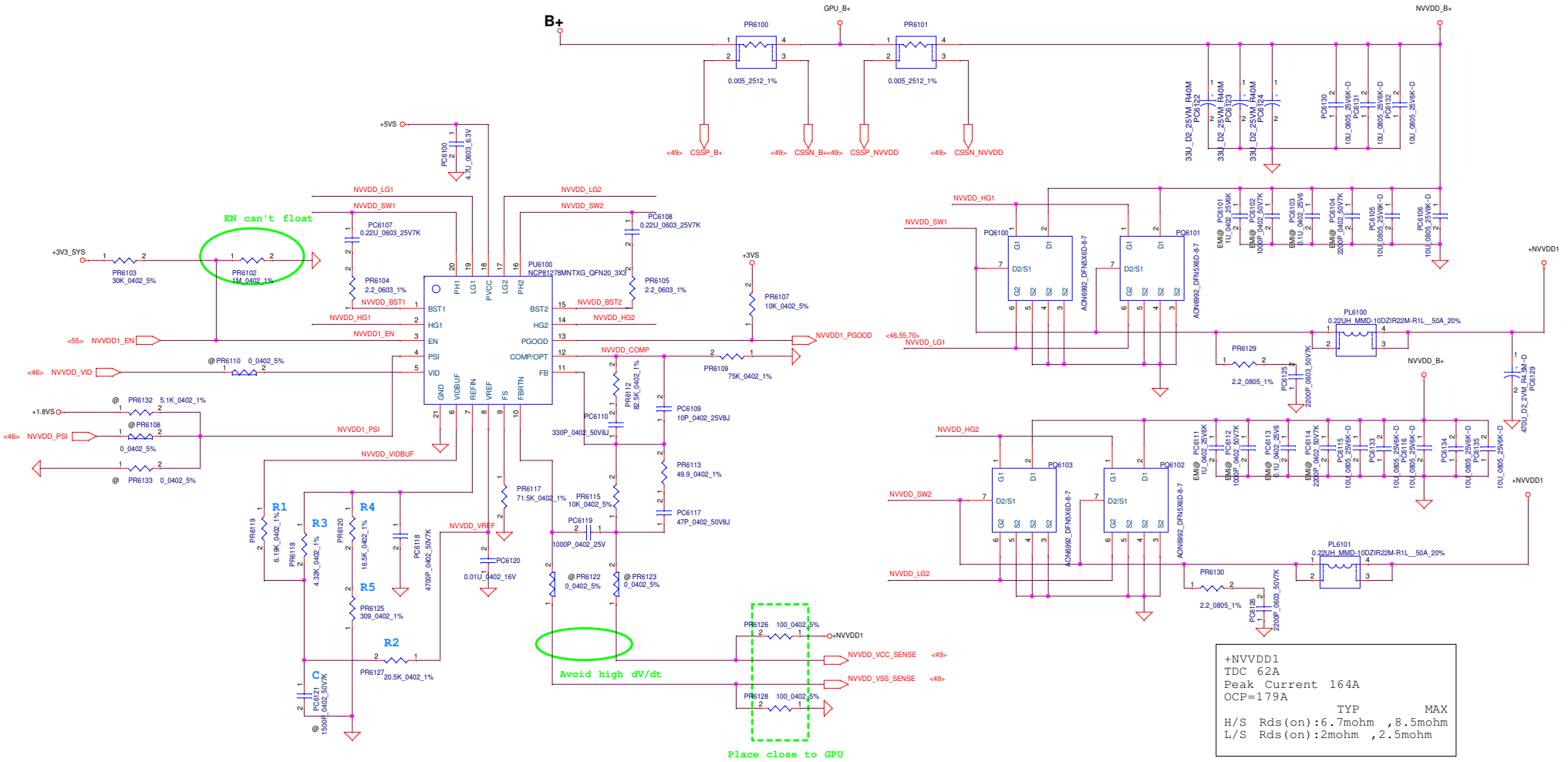


**Compal Electronics, Inc.**

Title: **PWR-1.0VS_VGA**

Size | Document Number: **LA-D581P** | Rev: 0.3

Date: Wednesday, September 07, 2016 | Sheet 68 of 80




| N17E_G1 | | VDD | VDDS |
|---|---|---|---|
| | TDC | 62 | 21 |
| | Peak | 164 | 50 |



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| Title: PWR-+NVVDD1 | | |
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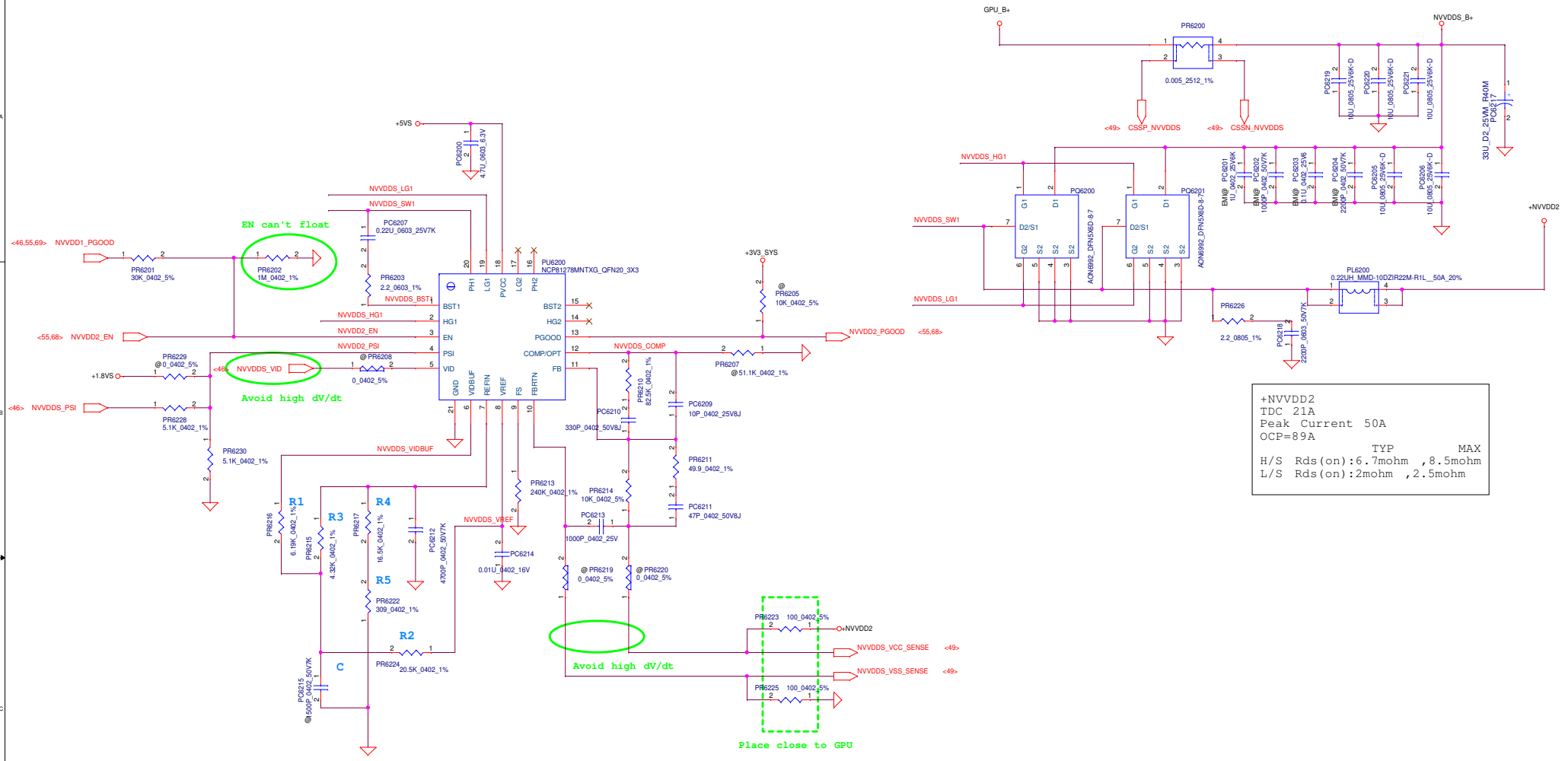


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Title: **PWR-+NVVDD2**

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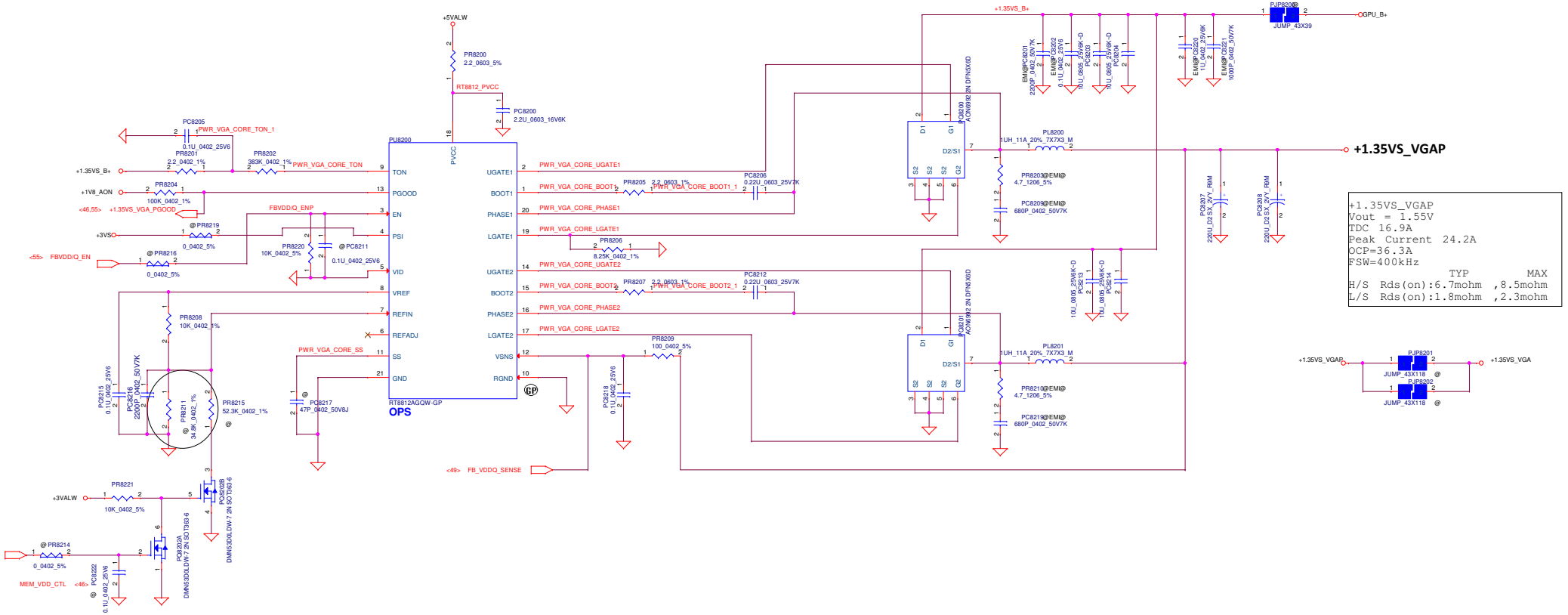


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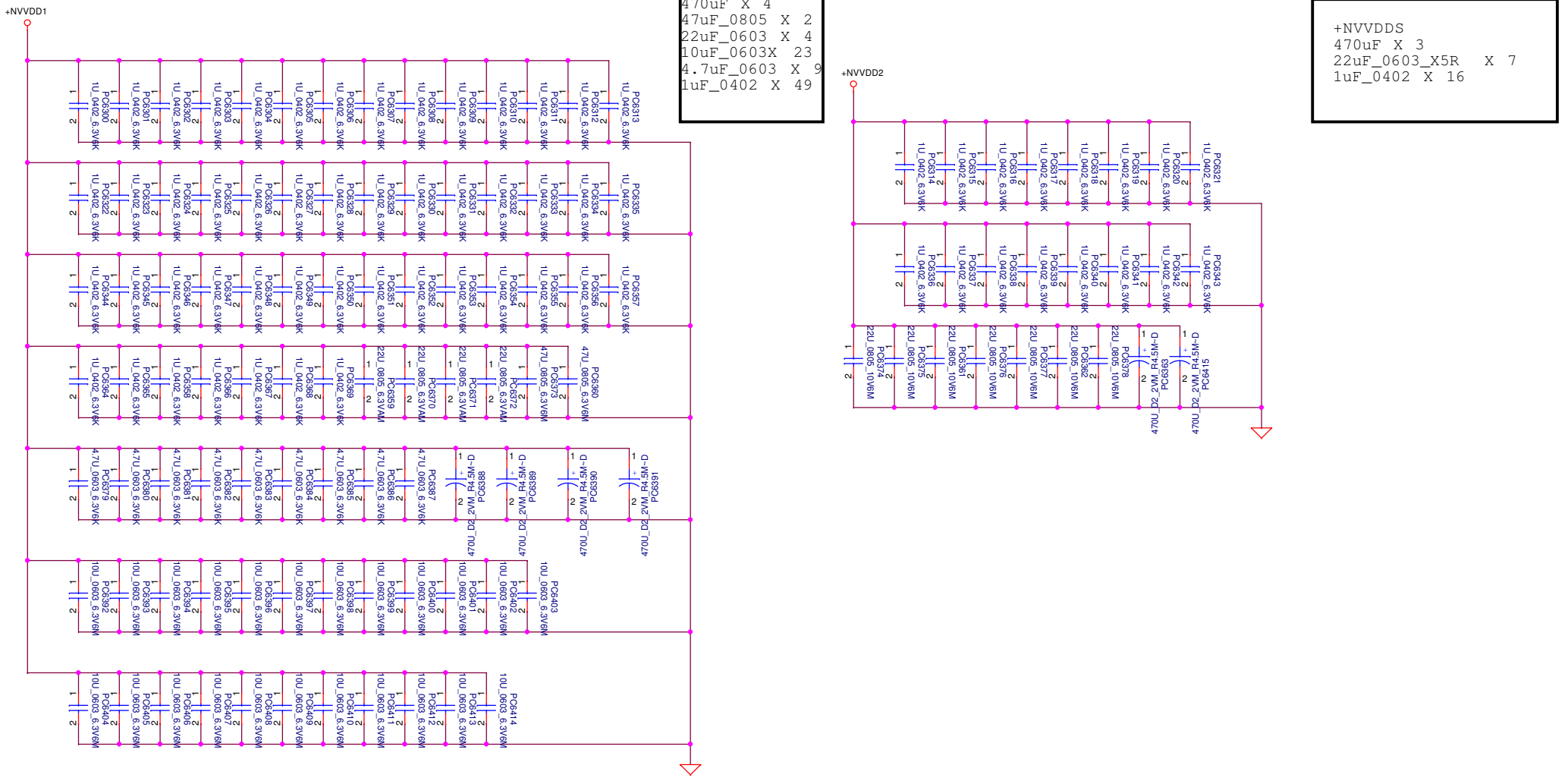


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Title: **VGA DECOUPLING**

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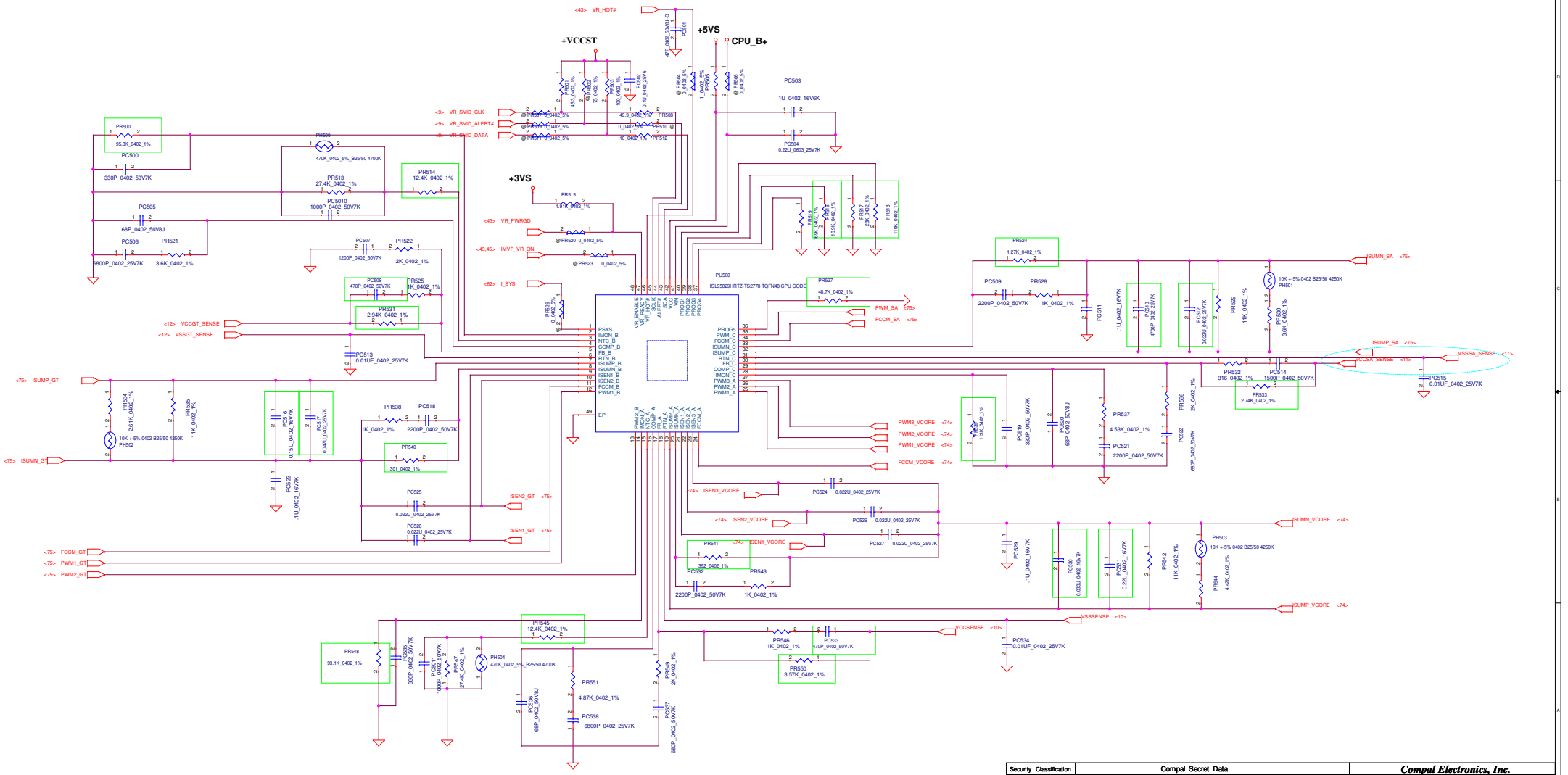


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**Compal Electronics, Inc.**

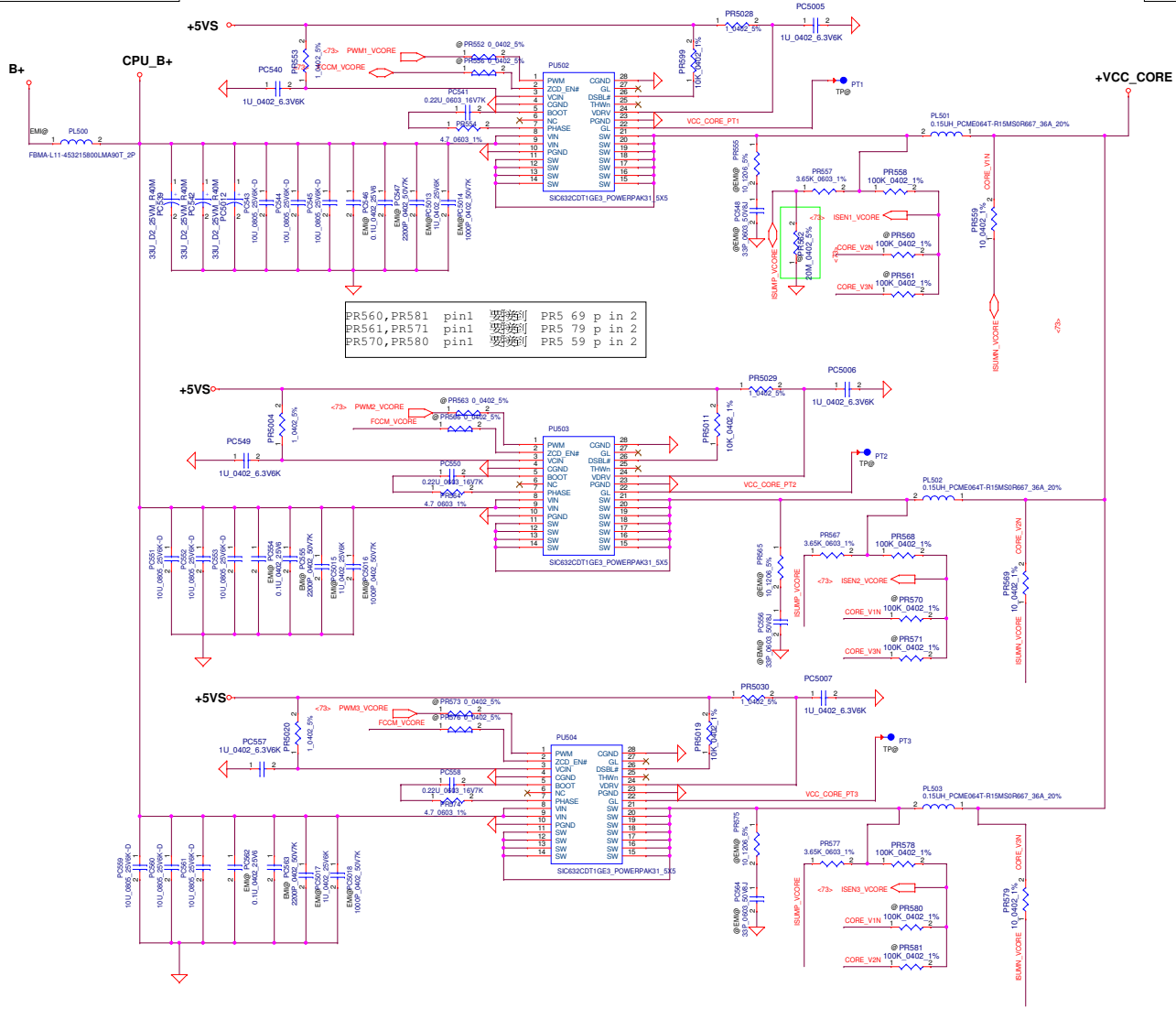
Title: PWR_VCORE_ISL95855

Size: | Document Number: LA-D581P | Rev: 0.3

Date: Wednesday, September 07, 2016 | Sheet 73 of 80

Input Current: 8.2A
1.5V*56A/0.85/12V=8.2

VCC_CORE
TDC PL2 :56A
Peak Current 68A
OCP Current 81.6A
DCR 0.66mohm +/-7%
Load Line 1.8mV/A

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Title: PWR_VCORE_+VCC_CORE

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Date: Wednesday, September 07, 2016 | Sheet 74 of 80

Input Current: 5.7A
1.5V*39A/0.85/12V=5.7

VCC_GT
TDC PL2 :39A
Peak Current 54A
OCP Current 64.8A
DCR 0.66mohm +/-7%
Load Line 2.65mV/A

+5VS
CPU_B+
+VCCGT
PU507
SIC632CDT1GE3_POWERPAK31_5X5
PR589 pin1 擺到 PR5 88 pin2
PR598 pin1 擺到 PR5 97 pin2

VCC_SA
TDC PL2 :10A
Peak Current 11A
OCP Current 13.2A
DCR 7.4mohm typ
Load Line 9.1mV/A

+5VS
PU510
SIC632CDT1GE3_POWERPAK31_5X5

Input Current: 1.0A
1.05V*10A/0.85/12V=1.0

CPU_B+
+VCCSA
SIC531CDT1GE3_POWERPAK22_4X3
PU511

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Title: PWR_VCORE_+VCCGT,+VCCSA

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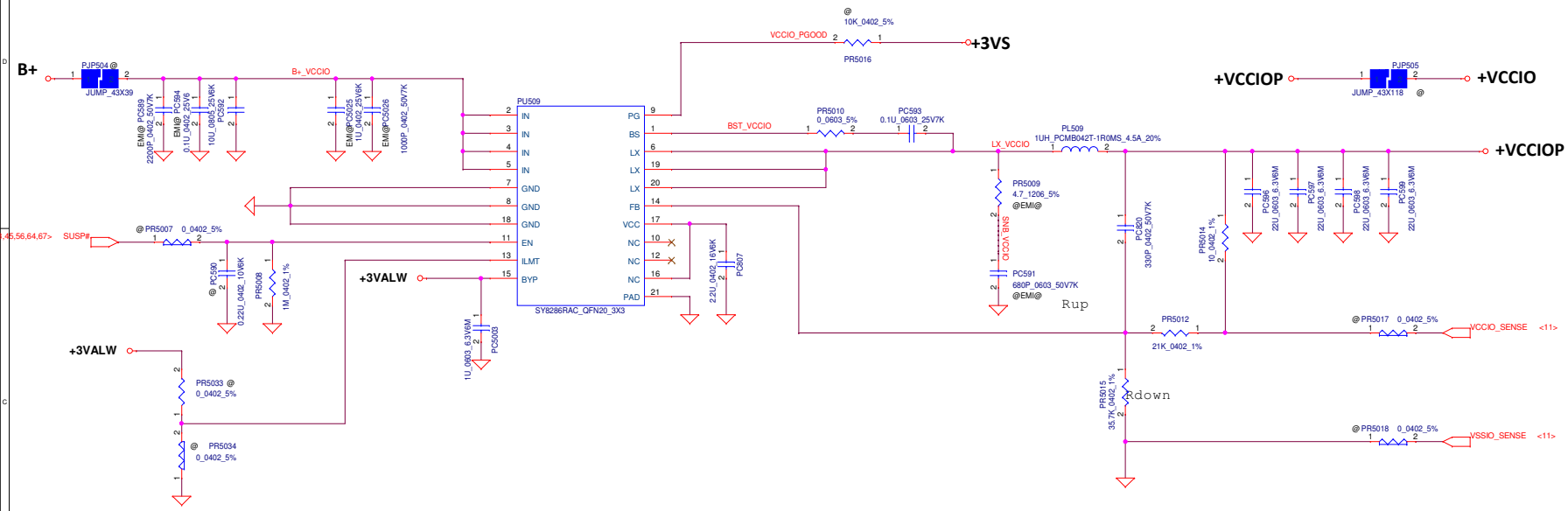


+VCCIO (0.95V)
TDC 3.85 A
Peak Current 5.5 A
OCP Current 6A Fix by IC

| | TYP | MAX |
|---|---|---|
| Choke DCR | 13.0mohm , | 14.0mohm |



| | | | |
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Title: PWR_+VCCIO

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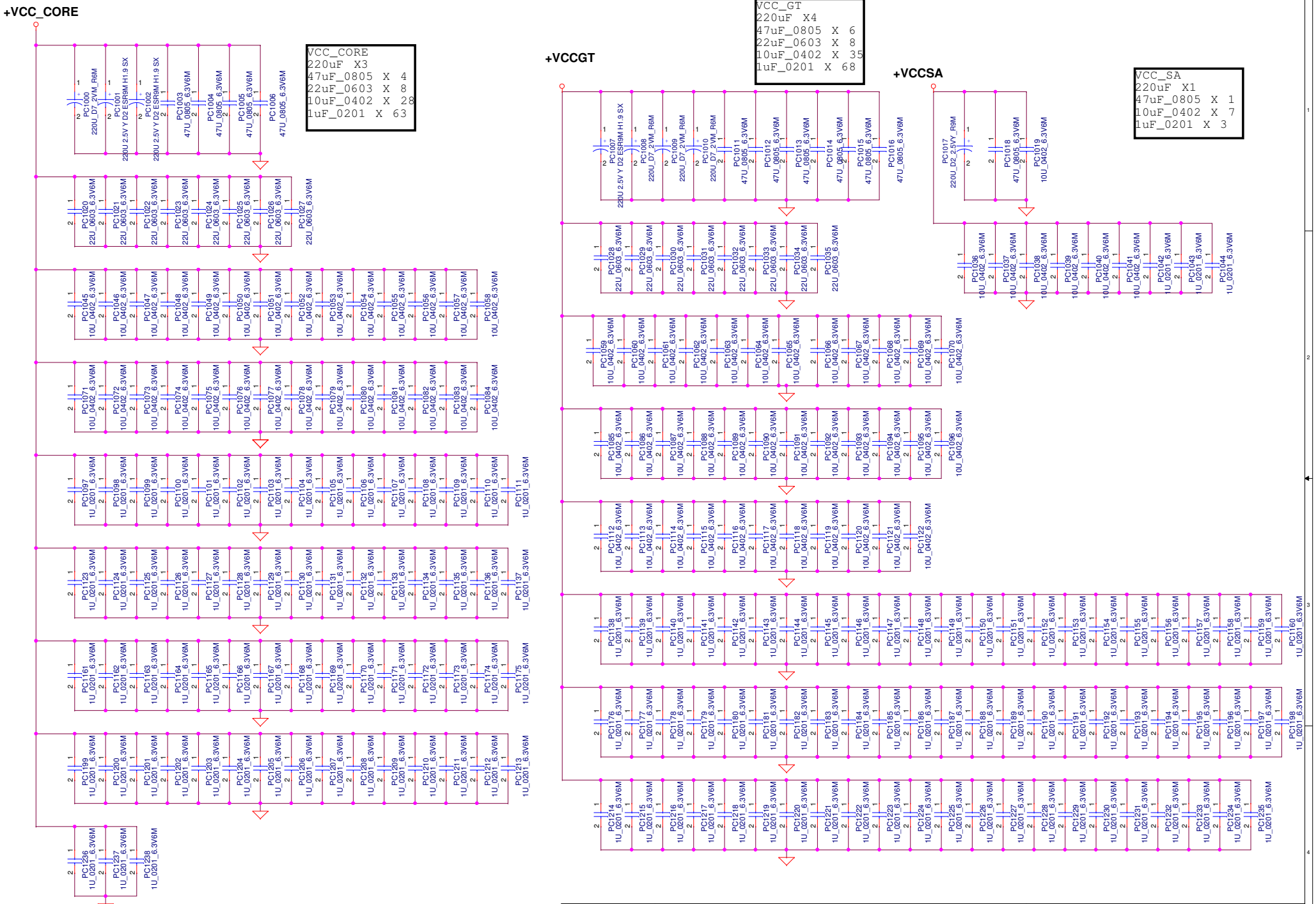


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**Compal Electronics, Inc.**

Title: **PWR_CPU DECOUPLING**

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