PCB Number: 13101

PAGE	TITLE	
01	COVER PAGE	
02	BLOCK DIAGRAM	
03	HW_CPU(PCIE/DMI)	
04	HW_CPU(THERMAL/CLK/PM/CFG)	
05	HW_CPU(DDR)	
06	(Reserved)HW_CPU (CFG)	
07	HW_CPU(VCC_CORE)	
08	HW_CPU(FDI/DDI/EDP)	
09	HW_CPU(VSS)	
10	HW_CPU(Power CAP)	
11	HW_PCH(Power CAP)	
12	HW_DDR3-SODIMM1	
13	HW_DDR3-SODIMM2	
14	(Reserved)SODIMM3_SODIMM4	
15	(Reserved)PCH(PCI/CRT/DDI	
16	HW_PCH(FDI/PCIE/DMI/USB)	
17	HW_PCH(RTC/HDA/SPI/PM/LP	
18	HW_PCH(CLOCK)	
19	HW_PCH(SATA/DP/VGA/CPU)	
20	HW_PCH(ESD)	
21	HW_PCH(POWER1)	
22	(Reserved)	
23	HW_PCH(VSS/STRAP)	
24	ECIO_NCT6683D	
25	HW_Flash(EC+PCH)/BAT	
26	Fan control	
27	Audio Codec_ALC272	
28	3W AUDIO_DSP OR AMP	
29	MIC/SPEAKER/AUDIO JACK	
30	LAN_8111GN/F	
31	RJ45_Transformer	
32	Card Reader_RTS5229	
33	CARD Reader CONN	
34	USB 2.0/ 3.0 Port _X	
35	USB Charger	
36	(Reserved)Power Plane Enable &Sequence	
37	ADAPTER OCP / S3 reduction	
38	DSW_PSU&ADAPTER	
39	1D05_ME	
40	HW_CPU(Reserved CFG)	
41	HW_PCH(Reserve)	
42	DCIN JACK_PSU/ADAPTER	
43	RTD3_POWER	
44	PWR_DUAL POWER_ADAPTER/PSU	
45	DC to DC_5V/3D3V_S0_PSU&AD	
46	CPU_CORE_PSU&Adapter_1	
47	CPU_CORE_PSU&Adapter_2	
48	DC to DC_1D05V_S0_AD/PSU	
49	DC to DC_1D5V_DD75V	
50	DC to DC_1D2V/1D8V	
51	DC to DC_1D5V _PCH	
52	LCD/Converter Connector	
53	CRT Board Connector	
54	HDMI Level Shifter/Conn	
55	RTD2135R eDP to LVDS	
56	HDD / ODD / NGFF_SSD	
57	(Reserve)E-SATA	
58	WLAN CONN	
59	(Reserve)WWAN CONN	
60	mSATA CONN	
61	LED Bard/Power Button	
62	(Res)Touch Pad	
63	IO Board Connector	
64	(Reserved)Hall Sensor	
65	Debug connector	
66	(Reserved)	
67	(Reserved)G Sensor	
68	(Reserved)Thunderbolt (1/5)	
69	(Reserve)Thunderbolt (2/5)	
70	Thunderbolt (3/5)	
71	Thunderbolt (4/5)	
72	Thunderbolt (5/5)	
73	GPU_PEG (1/5)	
74	GPU_DIGITALOUT (2/5)	
75	GPU_VRAM I/F (3/5)	

PAGE	TITLE	
76	GPU_GPIO/STRAP (4/5)	
77	GPU_POWER/GND (5/5)	
78	VRAM 1,2 (1/4)	
79	VRAM 3,4 (2/4)	
80	VRAM 5,6 (3/4)	
81	VRAM 7,8 (4/4)	
82	VGA_CORE NCP81172(PSU)	
83	DISCRETE VGA POWER	
84	Switchable GFX LCD(1/2)	
85	Switchable GFX CRT(2/2)	
86	UNUSED PARTS/EMI Capacitors	
87	NFC	
88	TPM/TCM	
89	Finger Print	
90	Express Card(Reserved)	
91	Smart Card Socket (Reserve)	
92	Switchable GFX eDP(Reserve)	
93	(Reserved)PCI	
94	Inter LAN WG1217LM(RES)	
95	LAN Switch(Reserved)	
96	CPU_XDP/ PCH_XDP/PORT80	
97	(Reserved)Table of Content	
98	GPIO table	
99	SYSTEM & GPU POWER SEQUENCE	
100	POWER DELIVERY CHART	
101	SMBUS Table	
102	(Reserved)	
103	PCB MAP	
104	[illegible] MAP	
105	RESET FOLLOW CHART	
106	Change History	

0805封裝尺寸/0603封裝尺寸/0603封裝尺寸1206封裝尺寸

封裝尺寸與功率關係：封裝尺寸與功率的對應關係

0201 1/20W
0402 1/16W
0603 1/10W
0805 1/8W
1206 1/4W

0402=1.0mmx0.5mm
0603=1.6mmx0.8mm
0805=2.0mmx1.2mm
1206=3.2mmx1.6mm
1210=3.2mmx2.5mm
1812=4.5mmx3.2mm
2225=5.6mmx6.5mm

Wistron P/N	Description
78.10324.2FLLL	CHIP CAP C 0.01U 50V K0402 X7R
78.10422.5FLLL	CHIP CAP C 0.1U 25V K0402 X5R
78.10491.4FLLL	CHIP CAP C 0.1U 16V Z0402 Y5V
78.10424.2BLLL	CHIP CAP C 0.1U 50V K0603 X7R
78.10520.5FLLL	CHIP CAP C 1U 6.3V K0402 X5R
78.10521.5BLLL	CHIP CAP C 1U 16V K0603 X5R
78.10324.2FLLL	CHIP CAP C 0.01U 50V K0402 X7R
78.10324.2FLLL	CHIP CAP C 0.01U 50V K0402 X7R
78.10324.2FLLL	CHIP CAP C 0.01U 50V K0402 X7R

Design note:

10KR3	10K value=10K	R resistor	3 Size=0603		
SCD1U10V2	S type=SMD	C capacitor	D1U value=0.1U	10V Withstang voltage=10V	2 Size=0402

BOM Configuration	BOM Configuration	BOM Configuration
(R):Unmount	(E):5W AMP	(TV):For TV Tuner
(M):Mount for both(S)and(V)	(T):Translater RTD2135	(MS):For MSATA
(S):For N15S-GT-S-AIO-A2	(D):Scalar RTD2586 and HDMI IN	(G):For Charger
(V):For N15V-GM-S-AIO-A2	(P):PSU	(NG):Non Charger
(O):For TPM	(A):Adapter	(BX):Recovery BIOS
(X):For debug	(U):U3 Controller and 3DWEBCAM	(HO):HDMI OUT
(C):3W AMP	(N):For NFC	(TCM): TCM

Build Net==>
(Part Value):'{Value}'!'{Part Number}'
(PCB Footprint) :'{PCB Footprint}'!'{PCB Footprint}'
'{Value}'!'{Part Number}' '{PCB Footprint}'!'{PCB Footprint}'

Build BOM==>
#Reference\tPart_Number\tSymbol\tGeometry\tF7\tFIN\tFIN1
{Reference}\t{Part Number}\t{Value}\t{PCB Footprint}\t{F7}\t{FIN}\t{FIN1}

#Reference\tPart_Number\tSymbol\tGeometry\tF7\tFIN\tFIN1{Reference}\t{Part Number}\t{Value}\t{PCB Footprint}\t{F7}\t{FIN}\t{FIN1}

Build VRT==>
Item Number\tReference\t<Core Design>\tBOM1\tValue\tDescription
{Item}\t{Reference}\t{Part Number}\t{F7}\t{Value}\t{Description}

Build VRT==>
Item Number\tReference\t<Core Design>\tBOM1\tValue\tDescription {Item}\t{Reference}\t{Part Number}\t{F7}\t{Value}\t{Description

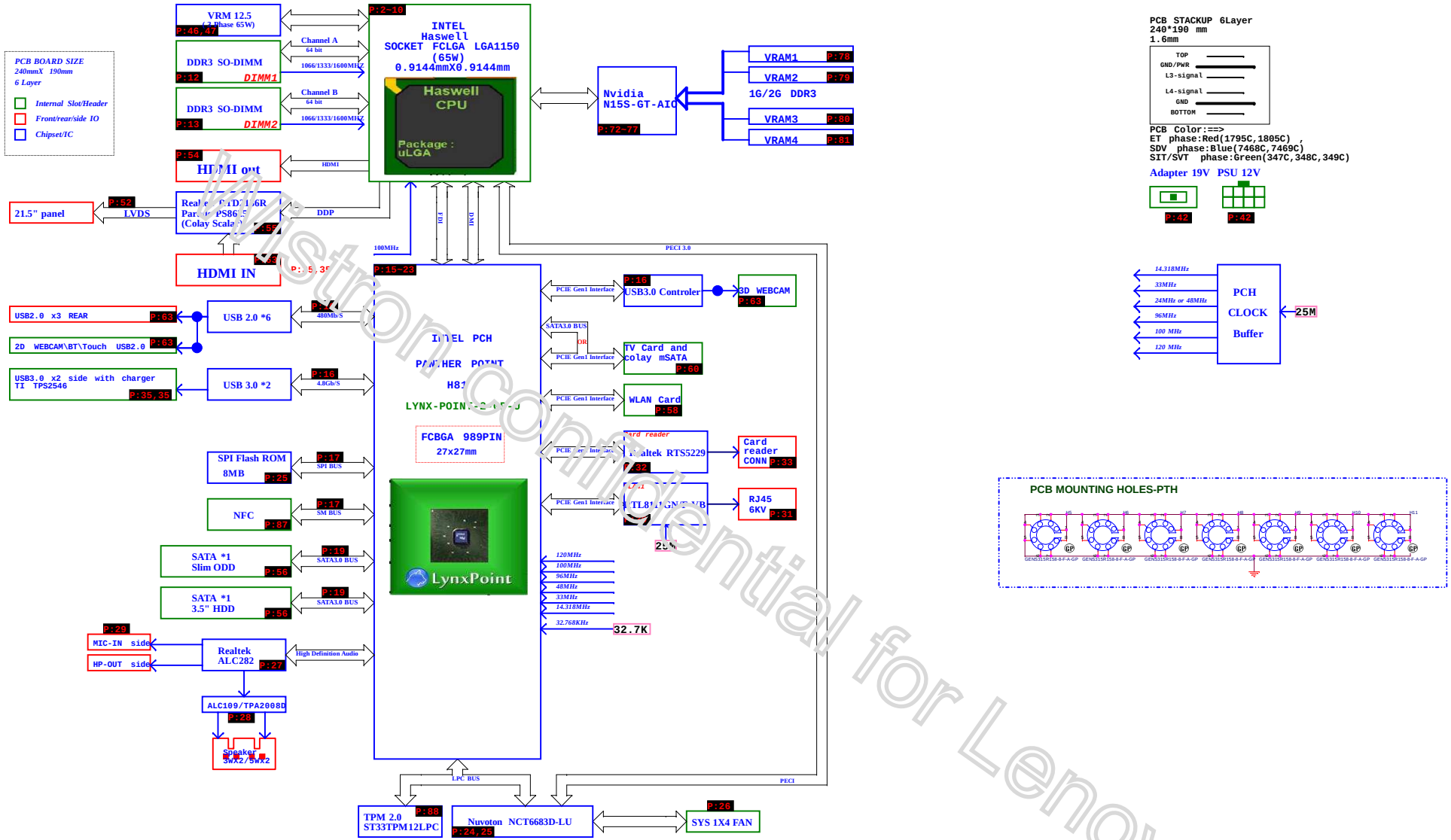
Build OLB File==>
1. 先開啟廠商的DSW檔案，並且將要用的元件複製起來(如果是晶組的話，只要其中一個即可)。
2. File->New->Design->將貼到Schematic的頁，貼上後會在Design Cache裡現一個*.OLB或者DM檔案
3. New->Library->將Design Cache裡面的*.OLB檔案拖移到Library裡面的*.Lib裡面其他的子元件(New->Page)
4. 將名字(Save)即可
5. 將*.OLB檔給Symbol team建此元件

BD Information:
T=1.6 +/-0.1MM 8layers
L*W=240mmX 150mm

How to option FUSE
FUSE calculate Current:A(A)
FUSE actual Current:A(A)
EXP calculate:
AI=X+0.8
1) A=AI+(+/-0.1)
2) AI+0.1<=A<=AI+0.4

Short-PAD
0402=ZZ.00PAD.M11
0603=ZZ.00PAD.M21
0805=ZZ.00PAD.M31
1206=?
1210=?

<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title: COVER PAGE
Size: D | Document Number: B560 with GPU | Rev: SA
Date: Tuesday, May 13, 2014 | Sheet 1 of 106


PCB BOARD SIZE
240mmX 190mm
6 Layer
Internal Slot/Header
Front/rear/side IO
Chipset/IC
VRM 12.5
(2 Phase 65W)
P:46,47
DDR3 SO-DIMM
P:12
DIMM1
DDR3 SO-DIMM
P:13
DIMM2
Channel A
64 bit
1066/1333/1600MHz
Channel B
64 bit
1066/1333/1600MHz
P:2~10
INTEL
Haswell
SOCKET FCLGA LGA1150
(65W)
0.9144mmX0.9144mm
Haswell CPU
Package : uLGA
Nvidia
N15S-GT-AIC
P:72~77
VRAM1 P:78
VRAM2 P:79
1G/2G DDR3
VRAM3 P:80
VRAM4 P:81
P:54
HDMI out
HDMI
21.5" panel
P:52
LVDS
DDP
100MHz
P:15~23
PECI 3.0
HDMI IN
INTEL PCH
PANTHER POINT
H81
LYNX-POINT-2
FCBGA 989PIN
27x27mm
LynxPoint
USB2.0 x3 REAR
P:63
2D WEBCAM\BT\Touch USB2.0
P:63
USB 2.0 *6
480Mb/S
USB3.0 x2 side with charger
TI TPS2546
P:35,35
USB 3.0 *2
P:16
4.8Gb/S
SPI Flash ROM
8MB
P:25
SPI BUS
NFC
P:87
SM BUS
SATA *1
Slim ODD
P:56
SATA3.0 BUS
SATA *1
3.5" HDD
P:56
SATA3.0 BUS
P:29
MIC-IN side
HP-OUT side
Realtek
ALC282
P:27
High Definition Audio
ALC109/TPA2008D
P:28
Speaker
3WX2/5WX2
PCIE Gen1 Interface
USB3.0 Controler
P:16
3D WEBCAM
P:63
SATA3.0 BUS
OR
PCIE Gen1 Interface
TV Card and colay mSATA
P:60
PCIE Gen1 Interface
WLAN Card
P:58
Card reader
PCIE Gen1 Interface
Realtek RTS5229
P:32
Card reader CONN P:33
LAN
PCIE Gen1 Interface
RJ45
6KV P:31
120MHz
100MHz
96MHz
48MHz
33MHz
14.318MHz
32.768KHz
32.7K
LPC BUS
PECI
TPM 2.0
ST33TPM12LPC
P:88
Nuvoton NCT6683D-LU
P:24,25
SYS 1X4 FAN
P:26
PCB STACKUP 6Layer
240*190 mm
1.6mm
TOP
GND/PWR
L3-signal
L4-signal
GND
BOTTOM
PCB Color:==>
ET phase:Red(1795C,1805C) ,
SDV phase:Blue(7468C,7469C)
SIT/SVT phase:Green(347C,348C,349C)
Adapter 19V PSU 12V
P:42
P:42
14.318MHz
33MHz
24MHz or 48MHz
96MHz
100 MHz
120 MHz
PCH
CLOCK
Buffer
25M
PCB MOUNTING HOLES-PTH
GEN5315R158-8-F-A-GP
Wistron Confidential for Lenovo
<Variant Name>
wistron
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
BLOCK DIAGRAM
Size
D
Document Number
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Rev
SA
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PCIEX8

73 EXP_A_TX_C_DP[7..0]
73 EXP_A_TX_C_DN[7..0]
73 EXP_A_RX_DP[7..0]
73 EXP_A_RX_DN[7..0]

DMI

16 DMI_IT_MR_DP[0..3]
16 DMI_IT_MR_DN[0..3]
16 DMI_MT_IR_DP[0..3]
16 DMI_MT_IR_DN[0..3]

CPU1C — 3 OF 10 — HASWELL

PEG_RX0 / PEG_RX#0
PEG_RX1 / PEG_RX#1
PEG_RX2 / PEG_RX#2
PEG_RX3 / PEG_RX#3
PEG_RX4 / PEG_RX#4
PEG_RX6 / PEG_RX#6
PEG_RX7 / PEG_RX#7
PEG_RX9 / PEG_RX#9
PEG_RX10 / PEG_RX#10
PEG_RX11 / PEG_RX#11
PEG_RX12 / PEG_RX#12
PEG_RX13 / PEG_RX#13
PEG_RX14 / PEG_RX#14
PEG_RX15 / PEG_RX#15
PEG_TX0 / PEG_TX#0
PEG_TX1 / PEG_TX#1
PEG_TX2 / PEG_TX#2
PEG_TX3 / PEG_TX#3
PEG_TX4 / PEG_TX#4
PEG_TX5 / PEG_TX#5
PEG_TX6 / PEG_TX#6
PEG_TX7 / PEG_TX#7
PEG_TX8 / PEG_TX#8
PEG_TX12 / PEG_TX#12
PEG_TX13 / PEG_TX#13
PEG_TX14 / PEG_TX#14
PEG_TX15 / PEG_TX#15

PEG Pair Imp:80ohm
T/B:5.5/5/5.5;Ohter:5/4/5

EXP_A_RX_DP7 … EXP_A_RX_DP0 / EXP_A_RX_DN7 … EXP_A_RX_DN0
EXP_A_TX_DP7 … EXP_A_TX_DP0 / EXP_A_TX_DN7 … EXP_A_TX_DN0

+V_VCCIOA_LOAD
R1002 24D9R2F-L-GP

DMI_IT_MR_DP0 … DMI_IT_MR_DP3 / DMI_IT_MR_DN0 … DMI_IT_MR_DN3
DMI_RX0 / DMI_RX#0
DMI_RX1 / DMI_RX#1
DMI_RX2 / DMI_RX#2
DMI_RX3 / DMI_RX#3
DMI_MT_IR_DP0 … DMI_MT_IR_DP3 / DMI_MT_IR_DN0 … DMI_MT_IR_DN3
DMI_TX0 / DMI_TX#0
DMI_TX1 / DMI_TX#1
DMI_TX2 / DMI_TX#2
DMI_TX3 / DMI_TX#3

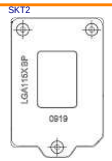
TPAD24 TP1000 … TPAD24 TP1003
TP_PEG_D1
TP_PEG_C2
TP_PEG_B3
TP_PEG_A4
PEG_COMP
RSVD_TP_D1
RSVD_TP_C2
RSVD_TP_B3
RSVD_TP_A4
PEG_RCOMP

BOM SKU = (62.10040.911)

SKT1

Load Plate
BOM SKU = (022.70001.0101)

SKT2



Back Plate
BOM SKU = (022.70001.0121)

2014.2.6
Julian

SKT3

ILMCOVER
(R)
BOM SKU = (22.78005.171)

Foxconn : 22.78006.001
Lotes : 22.78005.181

Foxconn : 22.78006.011
Lotes : 22.78002.011
Thickness:2.6mm

Foxconn : 22.78005.161
Lotes : 22.78005.171

CPU Load Plate:
Part Number: 022.70001.0101
Vendor Part Number: PT44L51-6401

CPU Socket:
Part Number: 062.10015.0051
Vendor Part Number: 3H993827-4M41-01H

PEG Static Lane Reversal PCIEx8

EXP_A_TX_DN7	C1017	1	SCD22U10V2KX-1-LL-GP	EXP_A_TX_C_DN7
EXP_A_TX_DN6	C1019	1	SCD22U10V2KX-1-LL-GP	EXP_A_TX_C_DN6
EXP_A_TX_DN5	C1021	1	SCD22U10V2KX-1-LL-GP	EXP_A_TX_C_DN5
EXP_A_TX_DN4	C1023	1	SCD22U10V2KX-1-LL-GP	EXP_A_TX_C_DN4
EXP_A_TX_DN3	C1025	1	SCD22U10V2KX-1-LL-GP	EXP_A_TX_C_DN3
EXP_A_TX_DN2	C1027	1	SCD22U10V2KX-1-LL-GP	EXP_A_TX_C_DN2
EXP_A_TX_DN1	C1029	1	SCD22U10V2KX-1-LL-GP	EXP_A_TX_C_DN1
EXP_A_TX_DN0	C1031	1	SCD22U10V2KX-1-LL-GP	EXP_A_TX_C_DN0
EXP_A_TX_DP7	C1018	1	SCD22U10V2KX-1-LL-GP	EXP_A_TX_C_DP7
EXP_A_TX_DP6	C1020	1	SCD22U10V2KX-1-LL-GP	EXP_A_TX_C_DP6
EXP_A_TX_DP5	C1022	1	SCD22U10V2KX-1-LL-GP	EXP_A_TX_C_DP5
EXP_A_TX_DP4	C1024	1	SCD22U10V2KX-1-LL-GP	EXP_A_TX_C_DP4
EXP_A_TX_DP3	C1026	1	SCD22U10V2KX-1-LL-GP	EXP_A_TX_C_DP3
EXP_A_TX_DP2	C1028	1	SCD22U10V2KX-1-LL-GP	EXP_A_TX_C_DP2
EXP_A_TX_DP1	C1030	1	SCD22U10V2KX-1-LL-GP	EXP_A_TX_C_DP1
EXP_A_TX_DP0	C1032	1	SCD22U10V2KX-1-LL-GP	EXP_A_TX_C_DP0

HOLE276R158 — CPU MOUNTING HOLE-PTH

H1 HOLE276R158-GP
H2 HOLE276R158-GP
H3 HOLE276R158-GP
H4 HOLE276R158-GP

=PCB_CPUPAD.U61

Combination:
U1 + SKT1 + SKT2 + SKT3

62.10055.761 (LOTES) + 22.78005.181 (LOTES)
+ 22.78002.011 (LOTES) + 22.78005.171 (LOTES)

62.10040.911 (FOXCONN) + 22.78006.011
FOXCONN) + 22.78005.161 (FOXCONN)

<Variant Name>

wistron

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12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU (PCIE/DMI/FDI)

Size: | Document Number: B560 with GPU | Rev: SA

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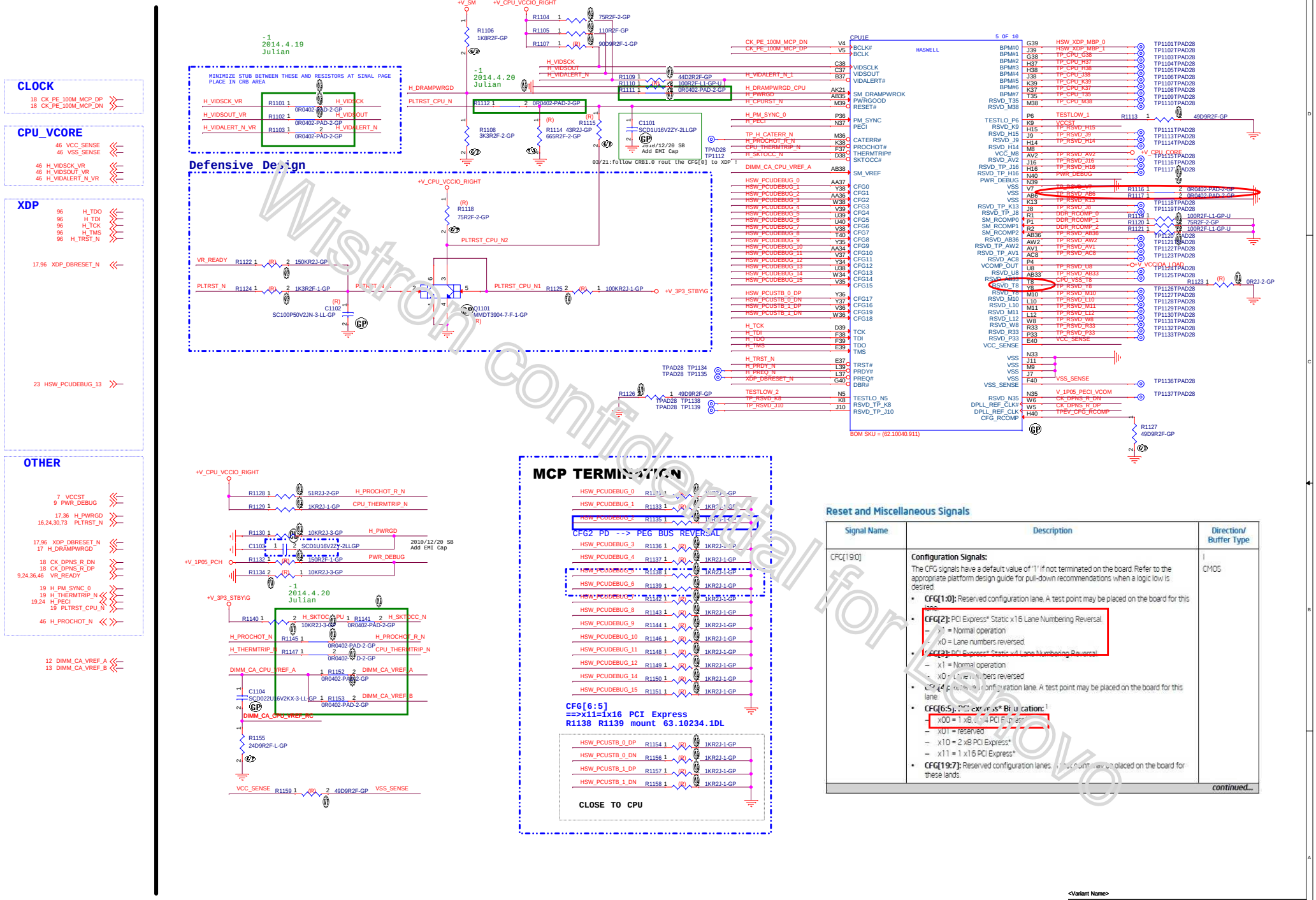

CLOCK
18 CK_PE_100M_MCP_DP
18 CK_PE_100M_MCP_DN
CPU_VCORE
46 VCC_SENSE
46 VSS_SENSE
46 H_VIDSCK_VR
46 H_VIDSOUT_VR
46 H_VIDALERT_N_VR
XDP
96 H_TDO
96 H_TDI
96 H_TCK
96 H_TMS
96 H_TRST_N
17,96 XDP_DBRESET_N
23 HSW_PCUDEBUG_13
OTHER
7 VCCST
9 PWR_DEBUG
17,36 H_PWRGD
16,24,30,73 PLTRST_N
17,96 XDP_DBRESET_N
17 H_DRAMPWRGD
18 CK_DPNS_R_DN
18 CK_DPNS_R_DP
9,24,36,46 VR_READY
19 H_PM_SYNC_0
19 H_THERMTRIP_N
19,24 H_PECI
19 PLTRST_CPU_N
46 H_PROCHOT_N
12 DIMM_CA_VREF_A
13 DIMM_CA_VREF_B
Defensive Design
MINIMIZE STUB BETWEEN THESE AND RESISTORS AT SINAL PAGE PLACE IN CRB AREA
MCP TERMINATION
CF62 PD --> PEG BUS REVERSAL
CFG[6:5]
==>x11=1x16 PCI Express
R1138 R1139 mount 63.10234.1DL
CLOSE TO CPU
Reset and Miscellaneous Signals
Signal Name
Description
Direction/ Buffer Type
CFG[19:0]
Configuration Signals:
The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.
CFG[1:0]: Reserved configuration lane. A test point may be placed on the board for this lane.
CFG[2]: PCI Express* Static x16 Lane Numbering Reversal
– x1 = Normal operation
– x0 = Lane numbers reversed.
CFG[3]: PCI Express* Static x4 Lane Numbering Reversal
– x1 = Normal operation
– x0 = Lane numbers reversed
CFG[4]: Reserved configuration lane. A test point may be placed on the board for this lane.
CFG[6:5]: PCI Express* Bifurcation:
– x00 = 1 x8, 2 x4 PCI Express*
– x01 = reserved
– x10 = 2 x8 PCI Express*
– x11 = 1 x16 PCI Express*
CFG[19:7]: Reserved configuration lanes. A test point may be placed on the board for these lands.
I
CMOS
continued...
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
CPU (THERMAL/CLOCK/PM)
Size C
Document Number B560 with GPU
Rev SA
Date: Tuesday, May 13, 2014
Sheet 4 of 106
Wistron confidential for Lenovo

DDR DATA

12 M_DATA_A[0..63]
13 M_DATA_B[0..63]

12 M_DQS_A_DP[0..7]
12 M_DQS_A_DN[0..7]

13 M_DQS_B_DP[0..7]
13 M_DQS_B_DN[0..7]

DDR CMD/ADD

12 M_MAA_A[0..15]
13 M_MAA_B[0..15]

12 M_WE_A_N
12 M_CAS_A_N
12 M_RAS_A_N
12 M_SBS_A0
12 M_SBS_A1
12 M_SBS_A2

13 M_WE_B_N
13 M_CAS_B_N
13 M_RAS_B_N
13 M_SBS_B0
13 M_SBS_B1
13 M_SBS_B2

DDR CTRL

12 M_SCS_A_N0
12 M_SCS_A_N1

12 M_SCKE_A0
12 M_SCKE_A1

12 M_ODT_A0
12 M_ODT_A1

13 M_SCS_B_N0
13 M_SCS_B_N1

13 M_SCKE_B0
13 M_SCKE_B1

13 M_ODT_B0
13 M_ODT_B1

DDR CLOCK

12 CK_M_DDR0_A_DP
12 CK_M_DDR0_A_DN
12 CK_M_DDR1_A_DP
12 CK_M_DDR1_A_DN

13 CK_M_DDR0_B_DP
13 CK_M_DDR0_B_DN
13 CK_M_DDR1_B_DP
13 CK_M_DDR1_B_DN

DDR OTHERS

12,13 DDR3_DRAMRST_N

13 DIMM_DQ_CPU_VREF_B
12 DIMM_DQ_CPU_VREF_A

CPU1A 1 OF 10 HASWELL

Can be left as no connects if no support ECC.

BOM SKU = (62.10040.911)

CPU1B 2 OF 10 HASWELL

Can be left as no connects if no support ECC.

BOM SKU = (62.10040.911)

C1203 SC100P50V2JN-3-LL-GP

C1201 SCD1U16V2ZY-2LLGP

C1202 SCD1U16V2ZY-2LLGP

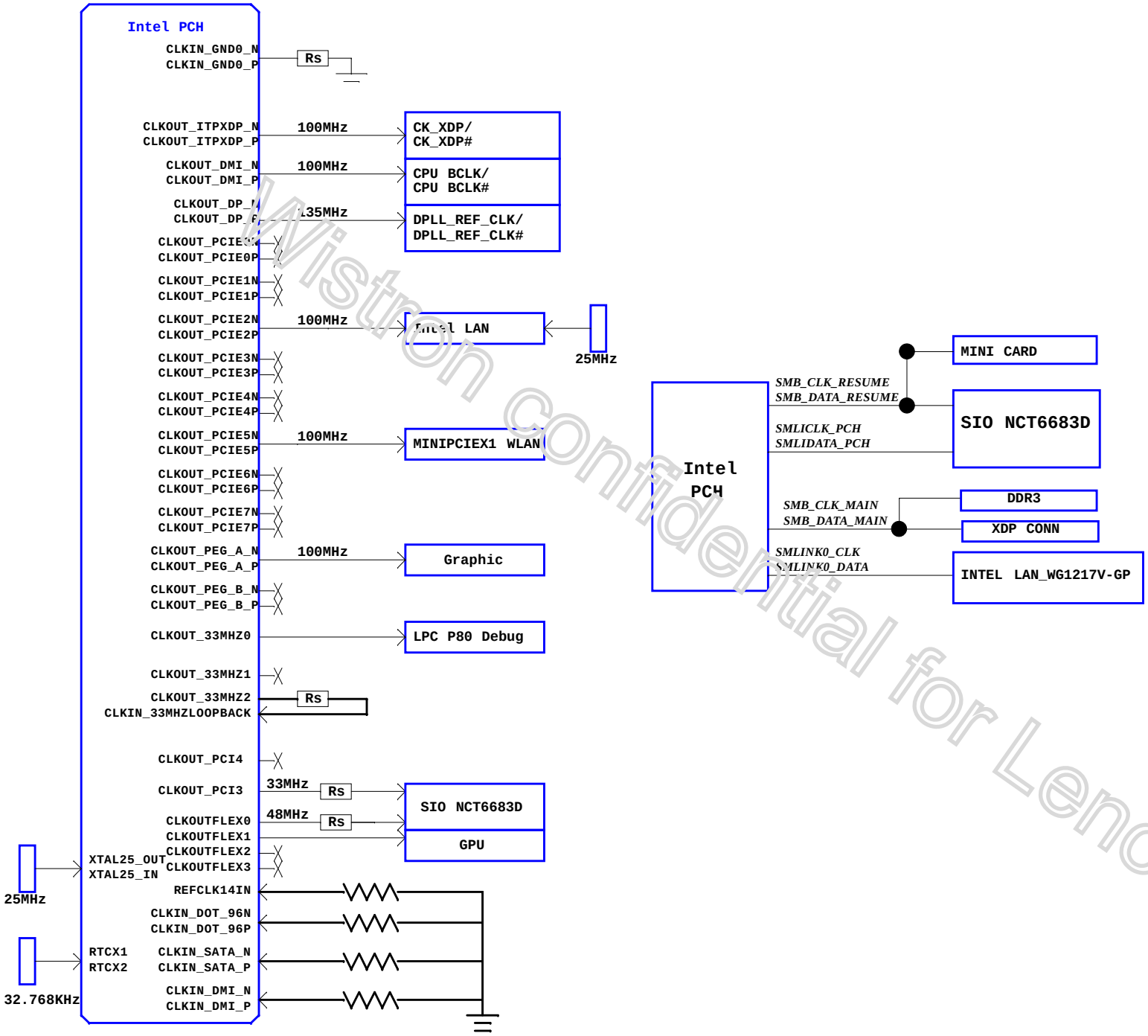
<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU (DDR)

Size: C | Document Number: B560 with GPU | Rev: SA

Date: Tuesday, May 13, 2014 | Sheet 5 of 106



Note: .... is Reserve

Note: Rs is series resister

<Variant Name>

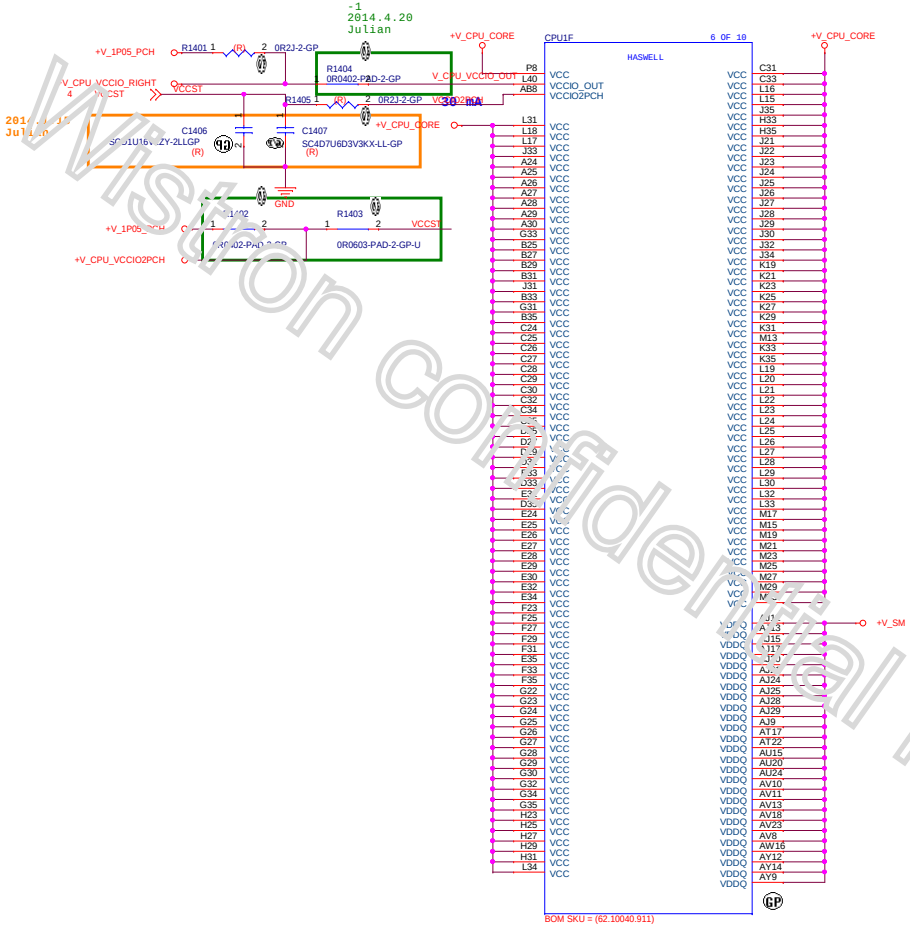
wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU (CFG)

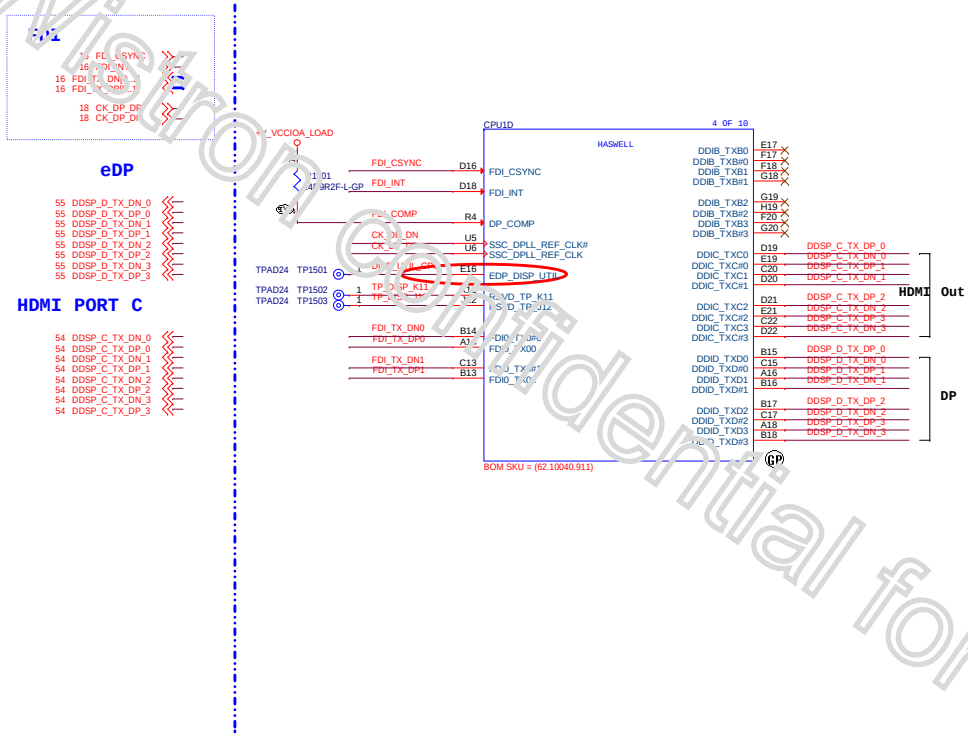
Size: C | Document Number: B560 with GPU | Rev: SA

Date: Tuesday, May 13, 2014 | Sheet 6 of 106



<Variant Name>

wistron	Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title: CPU (VCC_CORE)		
Size: C	Document Number: B560 with GPU	Rev: SA
Date: Tuesday, May 13, 2014	Sheet 7 of 106	



<Variant Name>

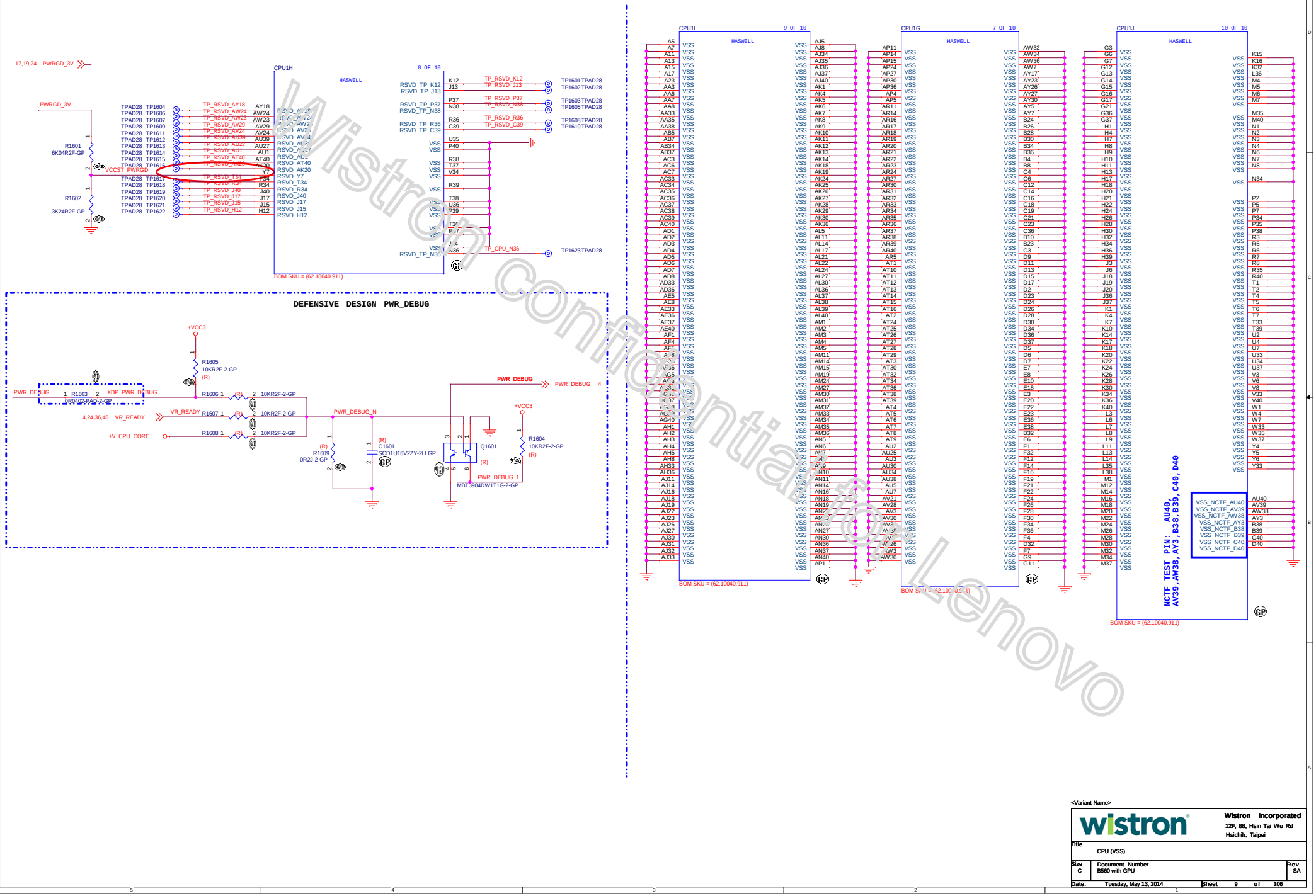
wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU (DDI/EDP)

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 8 of 106



<Variant Name>

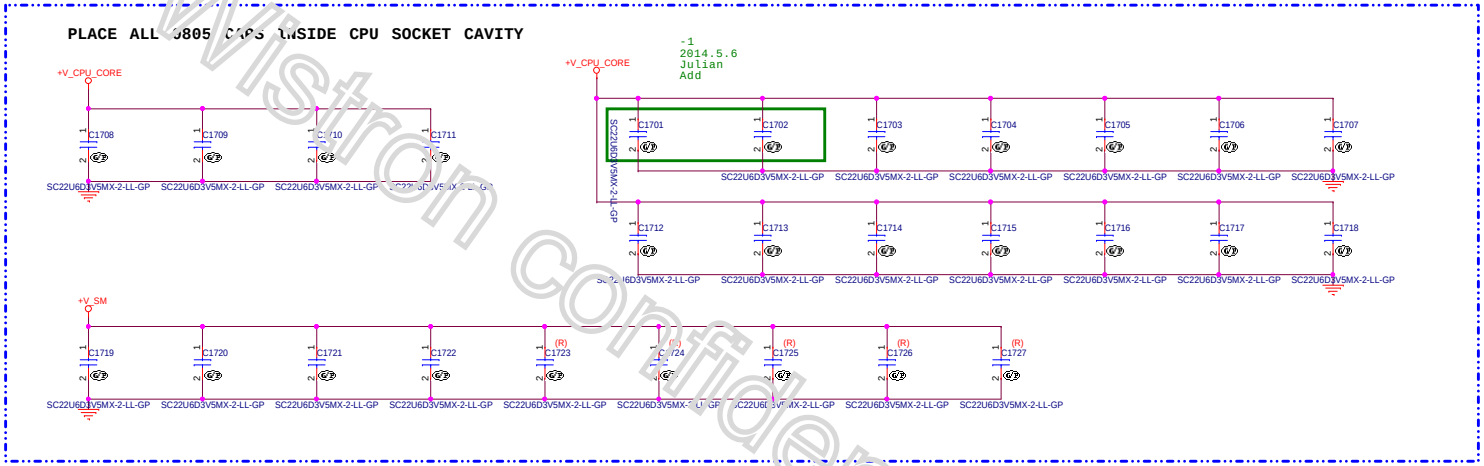
wistron

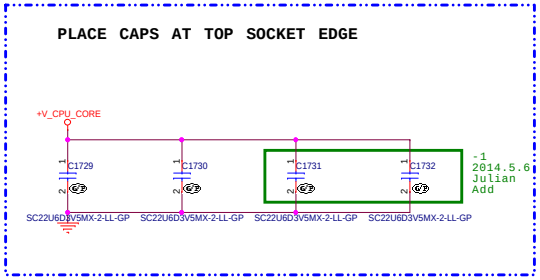
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

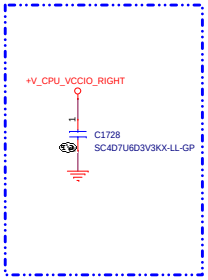
Title: CPU (VSS)

Size: C | Document Number: B560 with GPU | Rev: SA

Date: Tuesday, May 13, 2014 | Sheet 9 of 106



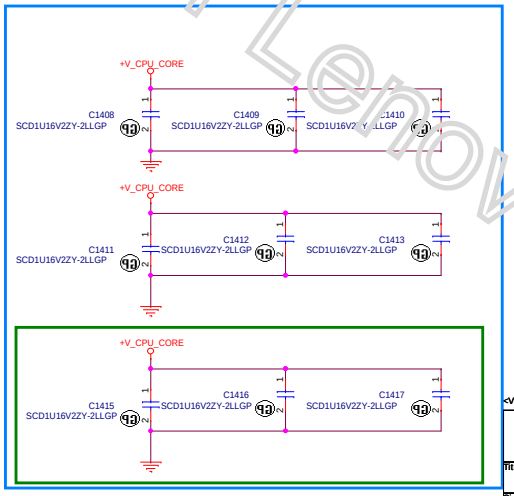




CPU Power Capacitor Quantity

SKU	CAP	AMOUNT
Vcore	22uF 0805	22
V_SM	22uF 0805	4+5(R)

1A 20140311 Darren Add



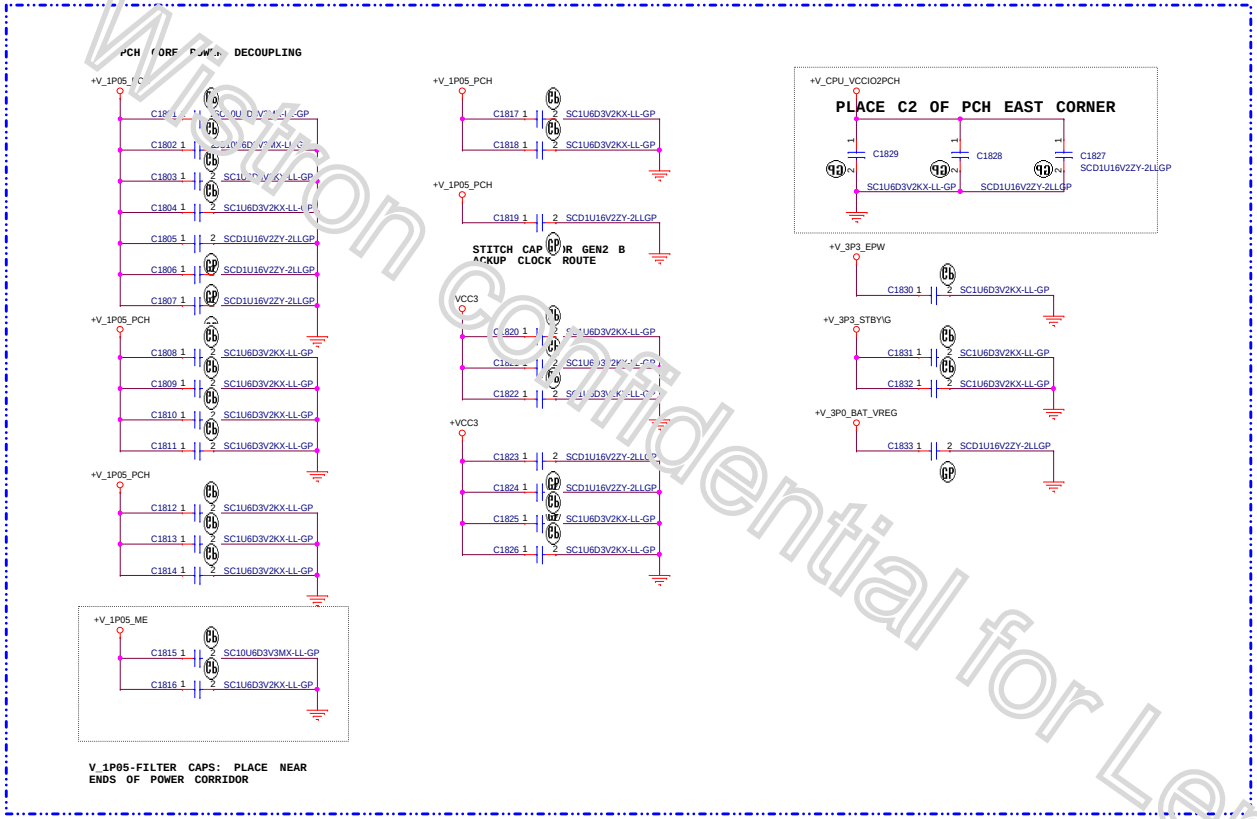
<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU (Power CAP)

Size: C | Document Number: B560 with GPU | Rev: SA

Date: Tuesday, May 13, 2014 | Sheet 10 of 106



<Variant Name>

wistron

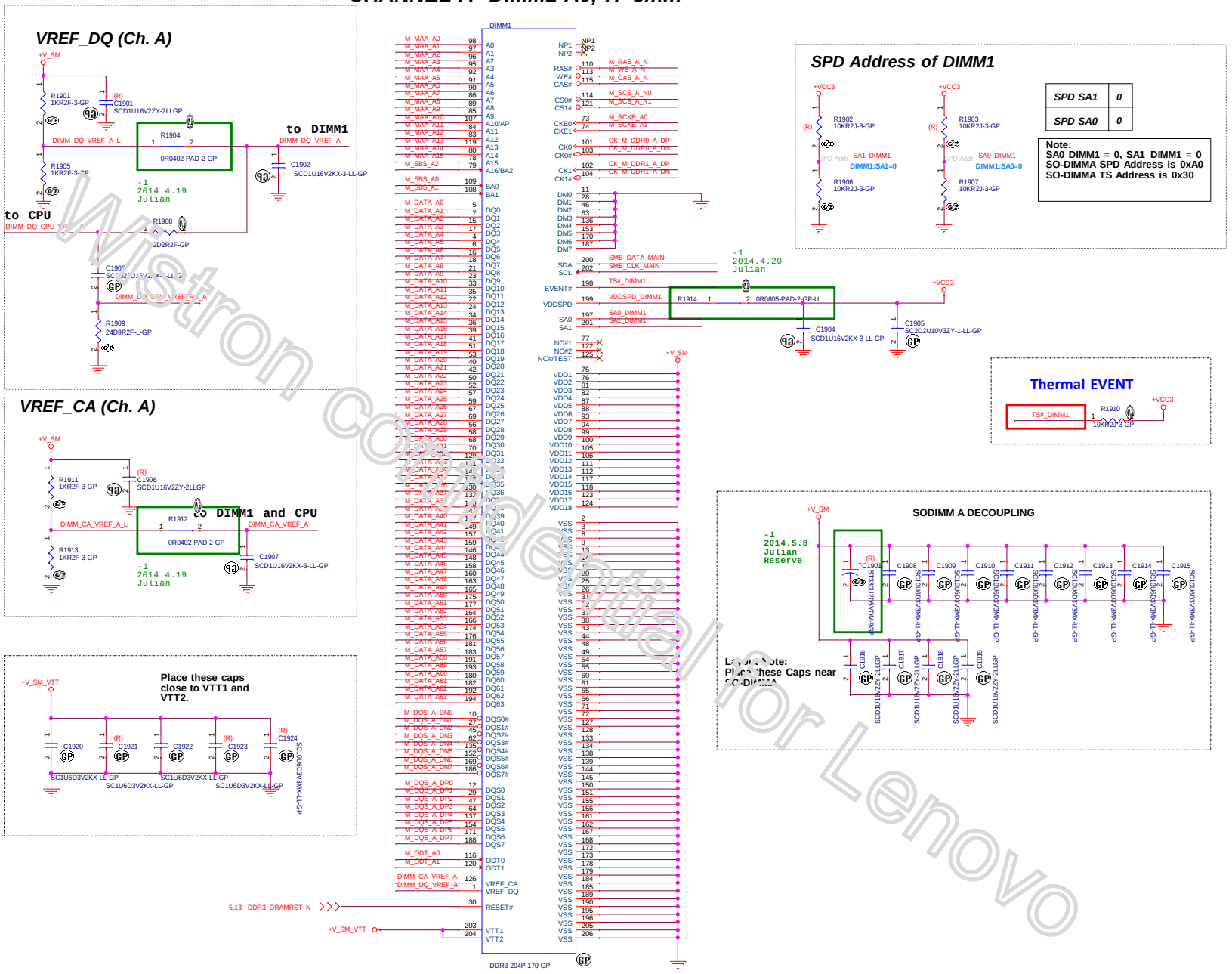
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PCH (Power CAP)

Size: C | Document Number: B560 with GPU | Rev: SA

Date: Tuesday, May 13, 2014 | Sheet 11 of 106

CHANNEL-A DIMM1 A0, H=8mm



DDR DATA

5 M_DATA_A[0..63]
5 M_DQS_A_DP[0..7]
5 M_DQS_A_DN[0..7]

DDR CMD/ADD

5 M_MAA_A[0..15]
5 M_WE_A_N
5 M_CAS_A_N
5 M_RAS_A_N
5 M_SBS_A0
5 M_SBS_A1
5 M_SBS_A2

DDR CTRL

5 M_SCS_A_N0
5 M_SCS_A_N1
5 M_SCKE_A0
5 M_SCKE_A1
5 M_ODT_A0
5 M_ODT_A1

DDR CLOCK

5 CK_M_DDR0_A_DP
5 CK_M_DDR0_A_DN
5 CK_M_DDR1_A_DP
5 CK_M_DDR1_A_DN

DDR OTHERS

5,13 DDR3_DRAMRST_N
13,17,58,60,87 SMB_DATA_MAIN
13,17,58,60,87 SMB_CLK_MAIN

5 DIMM_DQ_CPU_VREF_A
4 DIMM_CA_VREF_A

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	DDR3-SODIMM1		
Size C	Document Number B560 with GPU		Rev SA
Date: Tuesday, May 13, 2014		Sheet 12 of 106	

CHANNEL-B DIMM2, A4, H=4mm

DDR DATA

5 M_DATA_B[0..63]
5 M_DQS_B_DP[0..7]
5 M_DQS_B_DN[0..7]

DDR CMD/ADD

5 M_MAA_B[0..15]
5 M_WE_B_N
5 M_CAS_B_N
5 M_RAS_B_N
5 M_SBS_B0
5 M_SBS_B1
5 M_SBS_B2

DDR CTRL

5 M_SCS_B_N0
5 M_SCS_B_N1
5 M_SCKE_B0
5 M_SCKE_B1
5 M_ODT_B0
5 M_ODT_B1

DDR CLOCK

5 CK_M_DDR0_B_DP
5 CK_M_DDR0_B_DN
5 CK_M_DDR1_B_DP
5 CK_M_DDR1_B_DN

DDR OTHERS

5,12 DDR3_DRAMRST_N

5 DIMM_DQ_CPU_VREF_B
4 DIMM_CA_VREF_B

12,17,58,60,87 SMB_DATA_MAIN
12,17,58,60,87 SMB_CLK_MAIN

VREF_DQ (Ch. B)

+V_SM
R2001 1KR2F-3-GP
C2001 SCD1U16V2ZY-2LGP
R2004 0R0402-PAD-2-GP
to DIMM2
DIMM_DQ_VREF_B
DIMM_DQ_VREF_B_L
R2005 1KR2F-3-GP
C2002 SCD1U16V2KX-3-LL-GP
-1 2014.4.19 Julian
to CPU
DIMM_DQ_CPU_VREF_B
R2008 2D2R2F-GP
C2003 SC202U16V2KX-3-LL-GP
DIMM_DQ_CPU_VREF_RC_B
R2009 24D9R2F-L-GP

VREF_CA (Ch. B)

+V_SM
R2012 1KR2F-3-GP
C2006 SCD1U16V2ZY-2LGP
to DIMM1 and CPU
R2013 0R0402-PAD-2-GP
DIMM_CA_VREF_B
DIMM_CA_VREF_B_L
R2014 1KR2F-3-GP
C2007 SCD1U16V2KX-3-LL-GP
-1 2014.4.19 Julian

Place these caps close to VTT1 and VTT2.

+V_SM_VTT
C2021 C2022 C2023 C2024
SC1U6D3V2KX-LL-GP
SC1U6D3V2K2-LL-GP

CHANNEL-B DIMM2, A4, H=4mm

DIMM2
DDR3-204P-306-GP

M_MAA_B0 .. M_MAA_B15
M_SBS_B0 M_SBS_B1
M_DATA_B0 .. M_DATA_B63
M_DQS_B_DP0 .. M_DQS_B_DP7
M_DQS_B_DN0 .. M_DQS_B_DN7
M_DQS_B_DP8
M_DQS_B_DN8
M_ODT_B0 M_ODT_B1
DIMM_CA_VREF_B
DIMM_DQ_VREF_B
DDR3_DRAMRST_N
+V_SM_VTT

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16/BA2
BA0 BA1
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63
DQS0# DQS1# DQS2# DQS3# DQS4# DQS5# DQS6# DQS7#
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7
ODT0 ODT1
VREF_CA VREF_DQ
RESET#
VTT1 VTT2
NP1 NP2
M_RAS_B_N M_WE_B_N M_CAS_B_N
M_SCS_B_N0 M_SCS_B_N1
M_SCKE_B0 M_SCKE_B1
CK_M_DDR0_B_DP CK_M_DDR0_B_DN
CK_M_DDR1_B_DP CK_M_DDR1_B_DN
SMB_DATA_MAIN SMB_CLK_MAIN
TS#_DIMM2 VDDSPD_DIMM2 SA0_DIMM2 SA1_DIMM2
R2010 0R0805-PAD-2-GP-U
-1 2014.4.20 Julian
C2004 SCD1U16V2KX-3-LL-GP
C2005 SC2D2U10V3ZY-1-LL-GP
NC#1 NC#2 NC/TEST
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12
VSS

SPD Address of DIMM2

SPD SA1	1
SPD SA0	0

R2002 10KR2J-3-GP SA1_DIMM2 DIMM2:SA1=1
R2003 10KR2J-3-GP SA0_DIMM2 DIMM2:SA0=0
R2006 10KR2J-3-GP
R2007 10KR2J-3-GP

Note:
SA0 DIMM2 = 0, SA1_DIMM1 = 1
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34

TS#_DIMM1(EVENT#)must be connected to EC.(PH)

Thermal EVENT

TS#_DIMM2
R2011 10KR2J-3-GP

SODIMM B DECOUPLING

C2008 C2009 C2010 C2011 C2012 C2013 C2014 C2015
C2016 C2017 C2018 C2019 C2020
SCD1U16V2KX-LL-GP
SC4D7U6D3V3KX-LL-GP

Layout note:
Place these Caps near SO-DIMM2

SO-DIMMB is placed farther from the Processor than SO-DIMMA

DIMM slot
Standard Type

	FOXCONN	
DIMM1	62.10024.J21	
DIMM2	062.10011.0241	

SB
2014.1.23
Julian
Change

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DDR3-SODIMM2
Size: D
Document Number: 8560 with GPU
Rev: SA
Date: Tuesday, May 13, 2014
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<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
(Reserved)SODIMM3_SODIMM4

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 14 of 106

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
PCH (PCI/CRT/DDI)

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 15 of 106

DMI

PCIE

LAN

WLAN

USB2.0

USB3.0

FDI

OTHERS

Table 0-1. Desktop Lynx Point SKUs (Sheet 1 of 2)

Feature Set	Intel® 8 Series Express Chipset	Intel® 8 Series Express Chipset	Intel® 8 Series Express Chipset	Intel® 8 Series Express Chipset	Intel® 8 Series Express Chipset	Intel® 8 Series Express Chipset
SKU Name						
Flexible I/O	Yes	No	Yes	Yes	Yes	No
PCI Express* 2.0 Ports	8[4]	8	8	8[4]	8[4]	6
Total number of USB ports	14	14	14	14	14	10[5]
• USB 3.0 Capable Ports (SuperSpeed and all USB 2.0 Ports)	4[6]	4	4	4[6]	4[6]	2[5]
• USB 2.0 Only Ports	10[6]	10	10	10[6]	10[6]	8
Total number of SATA ports	6[2],[3]	6	6	4[2],[3]	4[2],[3]	4[1]
• SATA Ports (3 Gb/s and 1.5 Gb/s only)	6	4[1]	4[1]	6	6	3[1]
	6	2	2	6	0	2

Table 0-2. Desktop Lynx Point SKUs Hexible I/O Map

SKU	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12	Port13	Port14	Port15	Port16	Port17	Port18
B85	USB 3.0 Ports 1	USB 3.0 Ports 2	USB 3.0 Ports 3	USB 3.0 Ports 4	PCIe* Ports 1	PCIe* Ports 2	PCIe* Ports 3	PCIe* Ports 4	PCIe* Ports 5	PCIe* Ports 6	PCIe* Ports 7	PCIe* Ports 8	SATA Ports 0	SATA Ports 1	SATA Ports 2	SATA Ports 3	SATA Ports 4	SATA Ports 5

B85 USB3.0 Port Mapping

	USB 2.0 Signals	SuperSpeed Signals
USB Port 0	USB2N0 USB2P0	USB3TP1/N1 USB3RN1/P1
USB Port 1	USB2N1 USB2P1	USB3TP2/N2 USB3RN2/P2
USB Port 2	USB2N4 USB2P4	USB3TP3/N3 USB3RN3/P3
USB Port 3	USB2N5 USB2P5	USB3TP4/N4 USB3RN4/P4

Swap USB Port3 and Port9 net due to Intel USB3 xHCI controller doesn't support debug mode.

Overcurrent Pin Mapping

USB Ports Number	OC Pins Used
Port 0	OC0# (USB_OC0_R_N)
Port 1	OC1# (USB_CHARGE_OC_N)
Port 4,5,9	OC2# (port 4) OC3# (port 5) OC6# (port 9) (USB_OC_4_5_9_N)

OC[7:4]# for Device 26(Ports 8-13)

OC[3:0]# for Device 29(Ports 0-7)

These OC# pins are not used for USB overcurrent protection and should be configured as GPIOs. The unused USB ports can be left as no connect.

Each overcurrent pin is configured to protect one or more USB ports by setting bits in the USBOCM1 and USBOCM2 registers. It is system software's (BIOS) responsibility to program the USBOCM1 and USBOCM2 registers correctly and to make sure that each USB port is protected by only one overcurrent pin

FOR SIDE USB3.0(USB1)

FOR SIDE USB3.0(USB2)

FOR REAR IO USB2.0(USB3)

For Cap Touch

FOR REAR IO USB2.0(USB 5,6)

B85 Port6 and 7 are disable.

FOR MINI BT

FOR REAR IO USB2.0(USB DEBUG port)

FOR WEBCAM

FOR TV

PORT 12 DISABLE(Compatible with HP))

H81 PCIE{Port7/Port8} are disable

H81 USB3.0Port3/Port4} are disable

USB3.0 Controller

USB3.0 Controller

(U):U3 Controller and 3DWEBCAM

1ST:71.72020.A0U
2ST:71.72020.M01(Mount)

FOR LPT: GP70 STRAP - USB3 PORT4 GPT1 - USB3 PORTS SOFT STRAP TO DETERMINE NATIVE FUNCTION

PLACE NEAR PCH

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PCH (PCIE/USB)

Size: D | Document Number: B560 with GPU | Rev: SA

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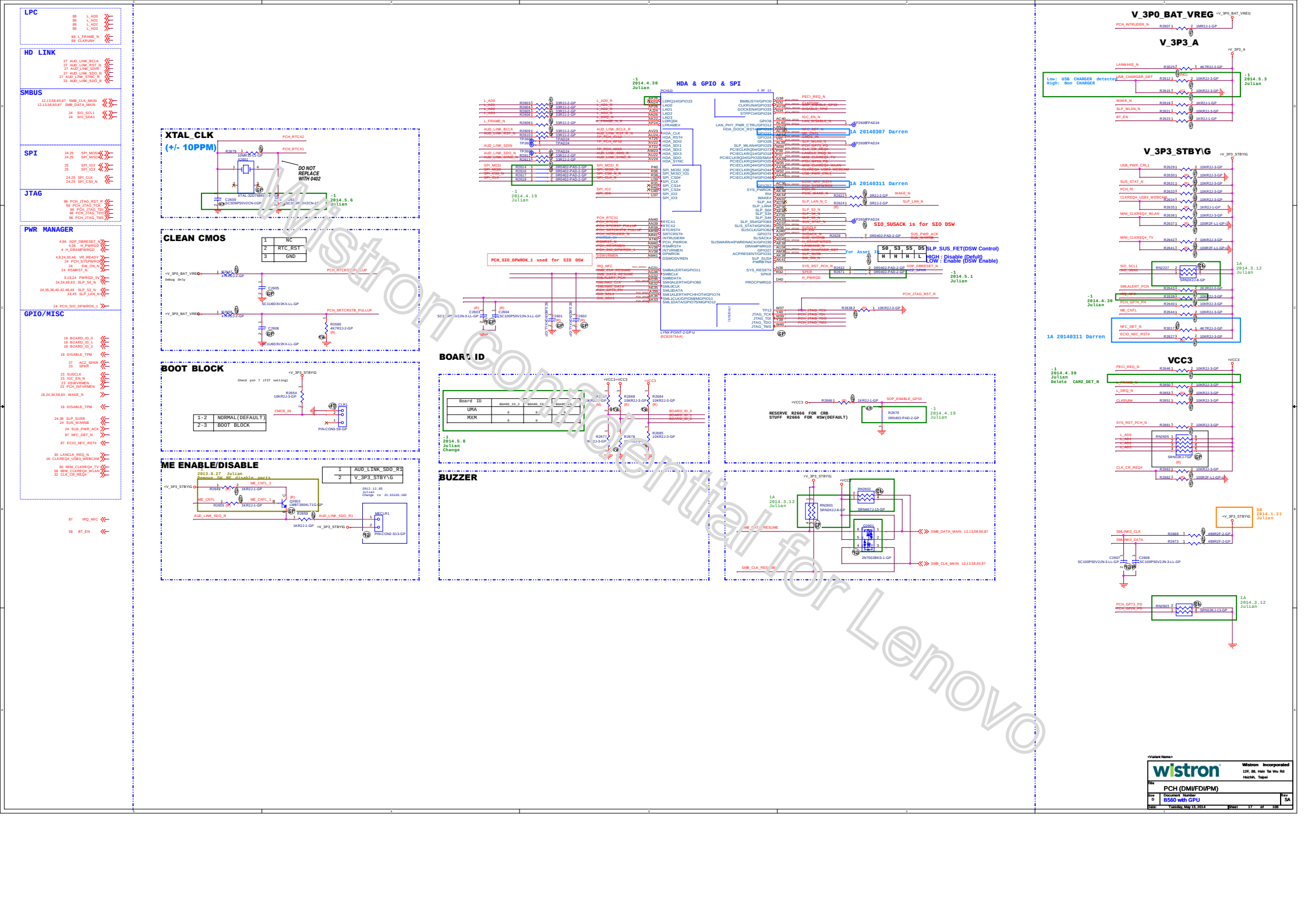
LPC
HD LINK
SMBUS
SPI
JTAG
PWR MANAGER
GPIO/MISC
XTAL_CLK
(+/- 10PPM)
DO NOT REPLACE WITH 0402
CLEAN CMOS
BOOT BLOCK
ME ENABLE/DISABLE
HDA & GPIO & SPI
BOARD ID
BUZZER
V_3P0_BAT_VREG
V_3P3_A
V_3P3_STBY\G
VCC3
PCH (DMI/FDI/PM)
B560 with GPU
Wistron Corporation
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Tuesday, May 13, 2014
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Wistron Confidential for Lenovo

CPU CLOCK

PCI CLOCK

88 CK_PCH_33M_TCM
88 CK_PCH_33M_TPM
16 CK_PCH_33M_FB
24 CK_PCH_33M_SIO

PCIE CLOCK

4 CK_DPNS_R_DN
4 CK_DPNS_R_DP

4 CK_PE_100M_MCP_DN
4 CK_PE_100M_MCP_DP

8 CK_DP_DN
8 CK_DP_DP

73 CLK_PCIE_PEG_P
73 CLK_PCIE_PEG_N

30 CK_PCIE_2_LAN_DN
30 CK_PCIE_2_LAN_DP
60 CK_PCIE_3_TV_DN
60 CK_PCIE_3_TV_DP
32 CLK_PCIE_CARD_P
32 CLK_PCIE_CARD_N
58 CLK_PCIE_MINI2_P
58 CLK_PCIE_MINI2_N

16 CLK_100_USB3_P
16 CLK_100_USB3_N

48M CLOCK

(Reserve)

GPIO

17 BOARD_ID_1
17 BOARD_ID_2

48M CLOCK

24 CK_PCH_48M_SIO

Empty when measure the PCI clock

To TPM
To TCM and
LOOPBACK CLK
To SIO

CK_PCH_33M_TPM R2503 22R2J-2-GP CK_33M_PCI0 AV5
CK_PCH_33M_TCM R2513 22R2J-2-GP CK_33M_PCI1 AV7
CK_PCH_33M_FB R2504 22R2J-2-GP CK_33M_PCI2 AU2
CK_PCH_33M_SIO R2505 22R2J-2-GP CK_33M_PCI3 AN9
AU5

CLKOUT_33MHZ0
CLKOUT_33MHZ1
CLKOUT_33MHZ2
CLKOUT_33MHZ3
CLKOUT_33MHZ4

To HWIO
To GPU

CLKOUTFLEX0 PCH_GPIO64 AV8
CLKOUTFLEX1 PCH_GPIO65 AT9
BOARD_ID_2 PCH_GPIO66 AV9
BOARD_ID_1 PCH_GPIO67 AU8

CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67

TPAD28 TP2505 SB 20[illegible] Julian [illegible]

+V_1P5_PCH
R2508 7K5R2F-1-GP XCLK_RCOMP R11
DIFFCLK_BIASREF
CK_14M_PCH AR7
REFCLK14IN

C2504 SCD1U16V2ZY-2LLGP (R)
C2505 SCD1U16V2ZY-2LLGP (R)

-1
2014.5.6
Julian
reserved

-1
2014.4.19
Julian

XTAL_25M_PCH_R_IN R2510 0R0402-PAD-2-GP XTAL_25M_PCH_IN
XTAL_25M_PCH_R_OUT R2512 0R0402-PAD-2-GP XTAL_25M_PCH_OUT
R2511 1MR3F-GP
X2501
XTAL-25MHZ-155-GP
C2501 SC12P50V2JN-3-LL-GP
C2502 SC12P50V2JN-3-LL-GP

NOTE:The 1Mohm Damping Resistor
Use 0603 and Can't change to 0402!

XTAL_IN should be pulled to GND via a 0-Ω resistor by default.
Intel reliability concerns

PCH1G
7 OF 11
LYNX-POINT-2-GP-U (0C626[illegible])

CLKIN_GND0# G16
CLKIN_GND0_P F16
CK_CSI_PCH_IN_DN
CK_CSI_PCH_IN_DP
R2501 10KR2J-3-GP
R2502 10KR2J-3-GP

CLKOUT_DMI# R2
CLKOUT_DMI_P T2
CK_PE_100M_MCP_DN
CK_PE_100M_MCP_DP
CLK OUT TO CPU for DMI

CLKOUT_DP# T3
CLKOUT_DP_P T5
CK_DP_DN
CK_DP_DP
CLK OUT TO CPU

CLKOUT_DPNS# W2
CLKOUT_DPNS_P U2
CK_DPNS_R_DN
CK_DPNS_R_DP
CLK OUT TO CPU

CLKOUT_ITPXDP# U6
CLKOUT_ITPXDP_P U7
CK_100M_CPU_XDP_DN
CK_100M_CPU_XDP_DP
TP2501 TPAD28
TP2502 TPAD28
CLK OUT TO XDP

CLKOUT_PEG_A# AA3
CLKOUT_PEG_A_P AA2
CLK_PCIE_PEG_N
CLK_PCIE_PEG_P
CLK OUT TO Graphic

CLKOUT_PEG_B# AE6
CLKOUT_PEG_B_P AE7

CLKOUT_PCIE_N0 AE10
CLKOUT_PCIE_P0 AE11

CLKOUT_PCIE_N1 AC6
CLKOUT_PCIE_P1 AC7
CLK_PCIE_CARD_N
CLK_PCIE_CARD_P
CLK OUT TO Card reader

CLKOUT_PCIE_N2 AC11
CLKOUT_PCIE_P2 AC10
CK_PCIE_2_LAN_DN
CK_PCIE_2_LAN_DP
CLK OUT TO PCIEX1 for LAN

CLKOUT_PCIE_N3 W11
CLKOUT_PCIE_P3 W10
CK_PCIE_3_TV_DN
CK_PCIE_3_TV_DP
CLK OUT TO PCIEX1 for TV

CLKOUT_PCIE_N4 Y4
CLKOUT_PCIE_P4 Y2

CLKOUT_PCIE_N5 W7
CLKOUT_PCIE_P5 W6
CLK_PCIE_MINI2_N
CLK_PCIE_MINI2_P
CLK OUT TO MINIPCIEX1 WLAN

CLKOUT_PCIE_N6 AA7
CLKOUT_PCIE_P6 AA6
CLK_100_USB3_N
CLK_100_USB3_P
CLK OUT TO USB3.0 Controller

CLKOUT_PCIE_N7 R6
CLKOUT_PCIE_P7 R7

PCHHT1
HEAT-SINK16
(34.3KR13.001)

+V_1P05_PCH
C2503 SCD1U16V2ZY-2LLGP
Stitching Capacitors for CK_PCIE_5

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: C | Document Number: B560 with GPU | Rev: SA

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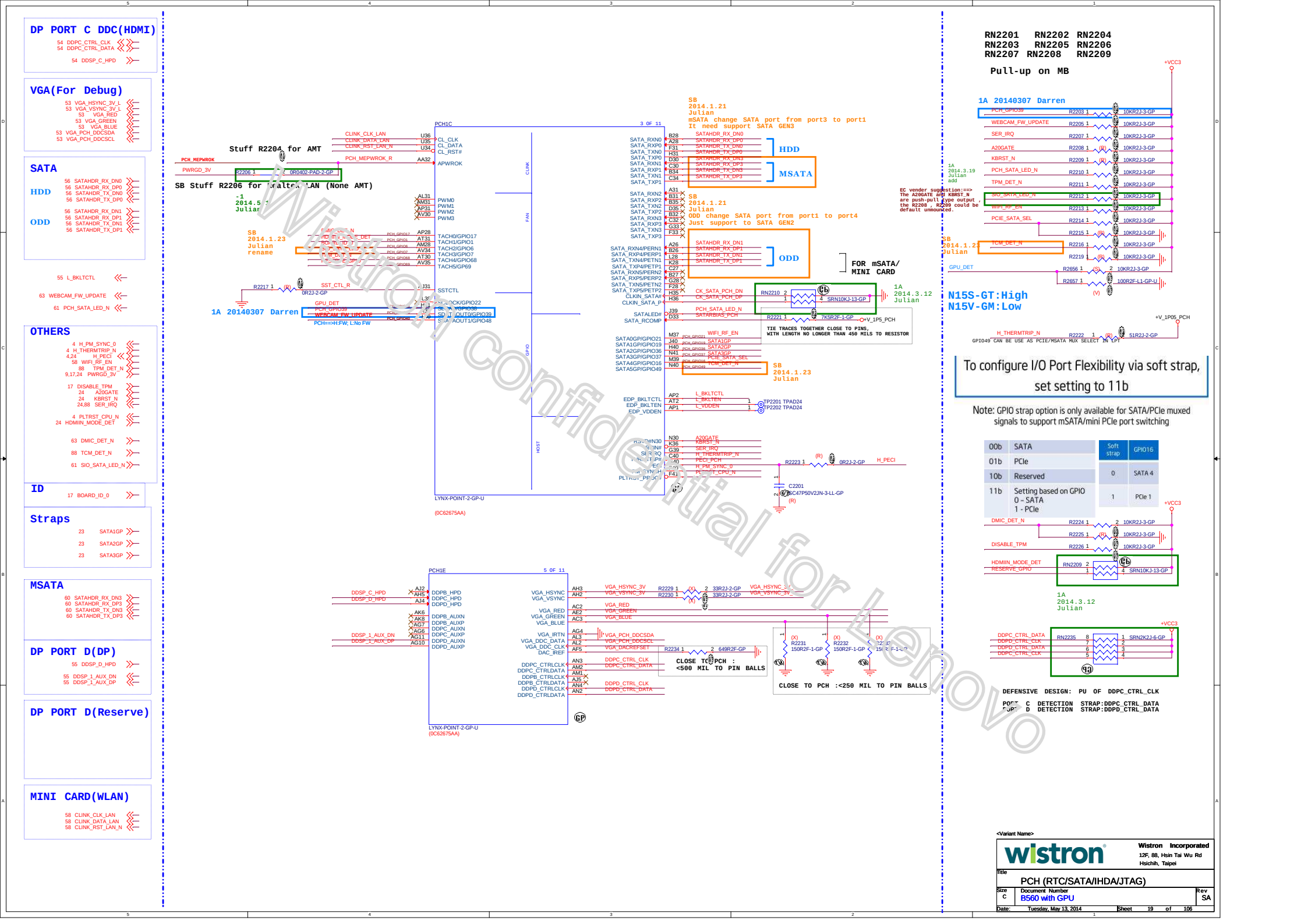

DP PORT C DDC(HDMI)
54 DDPC_CTRL_CLK
54 DDPC_CTRL_DATA
54 DDSP_C_HPD
VGA(For Debug)
53 VGA_HSYNC_3V_L
53 VGA_VSYNC_3V_L
53 VGA_RED
53 VGA_GREEN
53 VGA_BLUE
53 VGA_PCH_DDCSDA
53 VGA_PCH_DDCSCL
SATA
HDD
56 SATAHDR_RX_DN0
56 SATAHDR_RX_DP0
56 SATAHDR_TX_DN0
56 SATAHDR_TX_DP0
ODD
56 SATAHDR_RX_DN1
56 SATAHDR_RX_DP1
56 SATAHDR_TX_DN1
56 SATAHDR_TX_DP1
55 L_BKLTCTL
63 WEBCAM_FW_UPDATE
61 PCH_SATA_LED_N
OTHERS
4 H_PM_SYNC_0
4 H_THERMTRIP_N
4,24 H_PECI
58 WIFI_RF_EN
88 TPM_DET_N
9,17,24 PWRGD_3V
17 DISABLE_TPM
24 A20GATE
24 KBRST_N
24,88 SER_IRQ
4 PLTRST_CPU_N
24 HDMIIN_MODE_DET
63 DMIC_DET_N
88 TCM_DET_N
61 SIO_SATA_LED_N
ID
17 BOARD_ID_0
Straps
23 SATA1GP
23 SATA2GP
23 SATA3GP
MSATA
60 SATAHDR_RX_DN3
60 SATAHDR_RX_DP3
60 SATAHDR_TX_DN3
60 SATAHDR_TX_DP3
DP PORT D(DP)
55 DDSP_D_HPD
55 DDSP_1_AUX_DN
55 DDSP_1_AUX_DP
DP PORT D(Reserve)
MINI CARD(WLAN)
58 CLINK_CLK_LAN
58 CLINK_DATA_LAN
58 CLINK_RST_LAN_N
Stuff R2204 for AMT
SB Stuff R2206 for Realtek LAN (None AMT)
PCH_MEPWROK
PWRGD_3V
R2206 1
0R0402-PAD-2-GP
PCH_MEPWROK_R
AA32
APWROK
PCH1C
3 OF 11
CLINK_CLK_LAN
CLINK_DATA_LAN
CLINK_RST_LAN_N
U36
U35
U34
CL_CLK
CL_DATA
CL_RST#
SB
2014.1.21
Julian
mSATA change SATA port from port3 to port1
It need support SATA GEN3
SATAHDR_RX_DN0
SATAHDR_RX_DP0
SATAHDR_TX_DN0
SATAHDR_TX_DP0
SATAHDR_RX_DN3
SATAHDR_RX_DP3
SATAHDR_TX_DN3
SATAHDR_TX_DP3
HDD
MSATA
SB
2014.1.21
Julian
ODD change SATA port from port1 to port4
Just support to SATA GEN2
SATAHDR_RX_DN1
SATAHDR_RX_DP1
SATAHDR_TX_DN1
SATAHDR_TX_DP1
ODD
FOR mSATA/
MINI CARD
EC vender suggestion:==>
The A20GATE and KBRST_N
are push-pull type output ,
the R2208 , R2209 could be
default unmounted.
1A
2014.3.19
Julian
add
SB
2014.1.23
Julian
rename
PWM0
PWM1
PWM2
PWM3
TACH0/GPIO17
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
TACH4/GPIO68
TACH5/GPIO69
SSTCTL
SST_CTL_R
R2217 1
0R2J-2-GP
GPU_DET
WEBCAM_FW_UPDATE
PCH==>H:FW; L:No FW
1A 20140307 Darren
CK_SATA_PCH_DN
CK_SATA_PCH_DP
RN2210
SRN10KJ-13-GP
1A
2014.3.12
Julian
PCH_SATA_LED_N
SATARBIAS_PCH
R2221 1
7K5R2F-1-GP
+V_1P5_PCH
TIE TRACES TOGETHER CLOSE TO PINS,
WITH LENGTH NO LONGER THAN 450 MILS TO RESISTOR
WIFI_RF_EN
SATA1GP
SATA2GP
SATA3GP
PCIE_SATA_SEL
TCM_DET_N
SB
2014.1.23
Julian
L_BKLTCTL
L_BKLTEN
L_VDDEN
TP2201 TPAD24
TP2202 TPAD24
A20GATE
KBRST_N
SER_IRQ
H_THERMTRIP_N
PECI_PCH
H_PM_SYNC_0
PLTRST_CPU_N
R2223 1
0R2J-2-GP
H_PECI
C2201
SC47P50V2JN-3-LL-GP
LYNX-POINT-2-GP-U
(0C62675AA)
PCH1E
5 OF 11
DDSP_C_HPD
DDSP_D_HPD
DDSP_1_AUX_DN
DDSP_1_AUX_DP
DDPB_HPD
DDPC_HPD
DDPD_HPD
DDPB_AUXN
DDPB_AUXP
DDPC_AUXN
DDPC_AUXP
DDPD_AUXN
DDPD_AUXP
VGA_HSYNC
VGA_VSYNC
VGA_RED
VGA_GREEN
VGA_BLUE
VGA_IRTN
VGA_DDC_DATA
VGA_DDC_CLK
DAC_IREF
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPB_CTRLCLK
DDPB_CTRLDATA
DDPD_CTRLCLK
DDPD_CTRLDATA
VGA_HSYNC_3V
VGA_VSYNC_3V
R2229 1
R2230 1
33R2J-2-GP
VGA_PCH_DDCSDA
VGA_PCH_DDCSCL
VGA_DACREFSET
R2234 1
649R2F-GP
DDPC_CTRL_CLK
DDPC_CTRL_DATA
DDPD_CTRL_CLK
DDPD_CTRL_DATA
CLOSE TO PCH :
<500 MIL TO PIN BALLS
R2231
R2232
150R2F-1-GP
CLOSE TO PCH :<250 MIL TO PIN BALLS
RN2201 RN2202 RN2204
RN2203 RN2205 RN2206
RN2207 RN2208 RN2209
Pull-up on MB
+VCC3
1A 20140307 Darren
PCH_GPIO39
WEBCAM_FW_UPDATE
SER_IRQ
A20GATE
KBRST_N
PCH_SATA_LED_N
TPM_DET_N
SIO_SATA_LED_N
WIFI_RF_EN
PCIE_SATA_SEL
TCM_DET_N
GPU_DET
R2203
R2205
R2207
R2208
R2209
R2210
R2211
R2212
R2213
R2214
R2215
R2216
R2219
R2656
R2657
10KR2J-3-GP
100R2F-L1-GP-U
N15S-GT:High
N15V-GM:Low
+V_1P05_PCH
H_THERMTRIP_N
R2222
51R2J-2-GP
GPIO49 CAN BE USE AS PCIE/MSATA MUX SELECT IN LPT
To configure I/O Port Flexibility via soft strap, set setting to 11b
Note: GPIO strap option is only available for SATA/PCIe muxed signals to support mSATA/mini PCIe port switching
00b SATA
01b PCIe
10b Reserved
11b Setting based on GPIO
0 - SATA
1 - PCIe
Soft strap
GPIO16
0 SATA 4
1 PCIe 1
DMIC_DET_N
DISABLE_TPM
HDMIIN_MODE_DET
RESERVE_GPIO
R2224
R2225
R2226
RN2209
SRN10KJ-13-GP
1A
2014.3.12
Julian
DDPC_CTRL_DATA
DDPD_CTRL_CLK
DDPD_CTRL_DATA
DDPC_CTRL_CLK
RN2235
SRN2K2J-6-GP
DEFENSIVE DESIGN: PU OF DDPC_CTRL_CLK
PORT C DETECTION STRAP:DDPC_CTRL_DATA
PORT D DETECTION STRAP:DDPD_CTRL_DATA
<Variant Name>
wistron
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
PCH (RTC/SATA/IHDA/JTAG)
Size C
Document Number
B560 with GPU
Rev SA
Date: Tuesday, May 13, 2014
Sheet 19 of 106
Wistron confidential for Lenovo

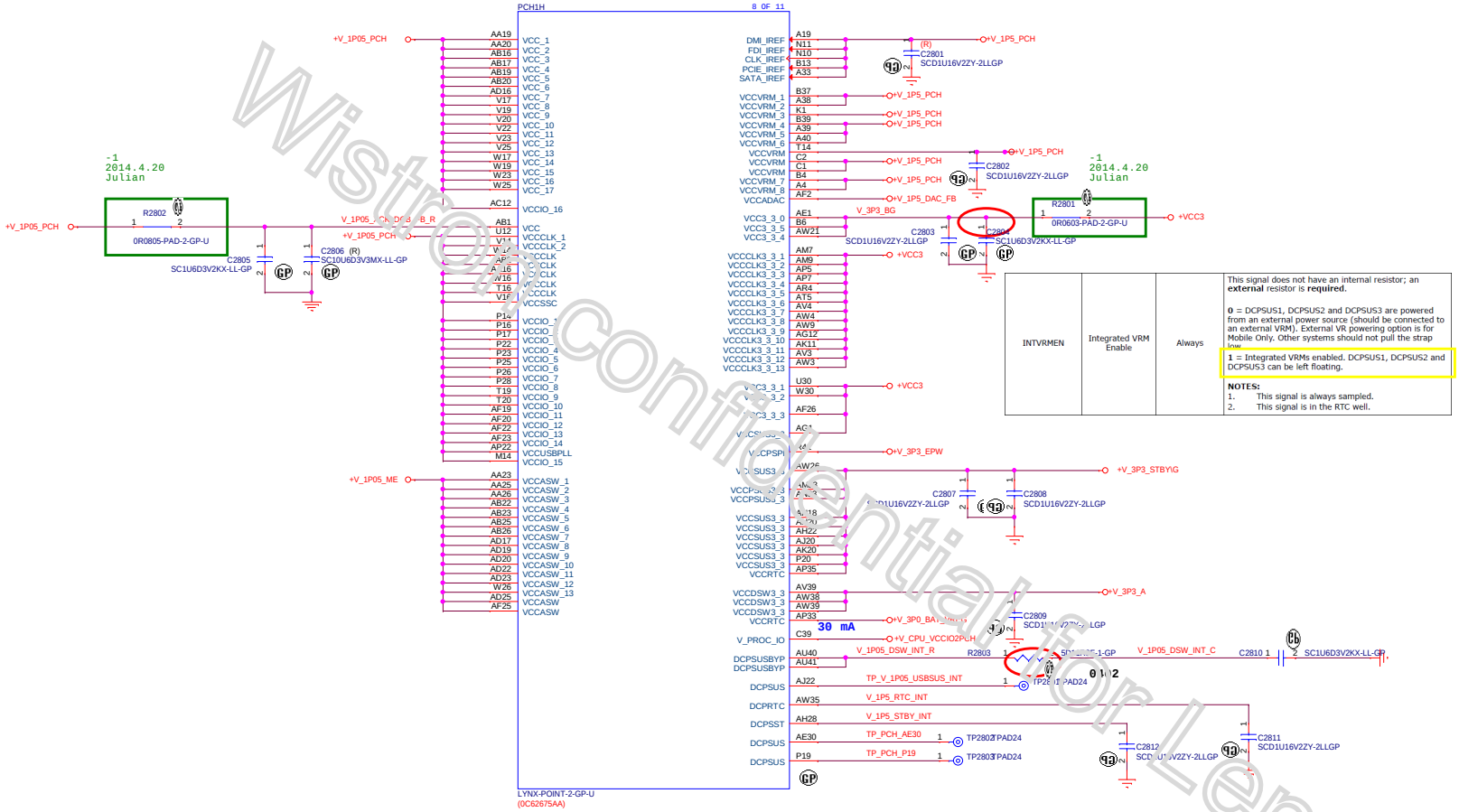
<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PCH (GPIO/CPU)

Size: C | Document Number: B560 with GPU | Rev: SA

Date: Tuesday, May 13, 2014 | Sheet 20 of 106



<Variant Name>

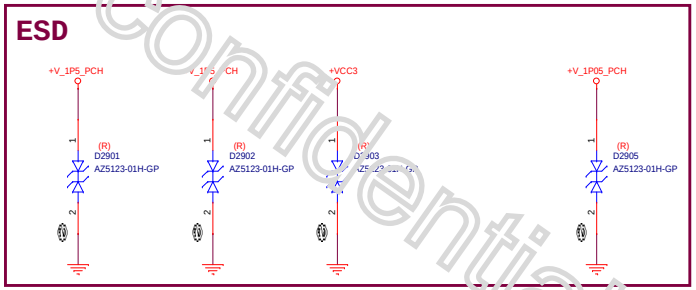
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PCH (POWER1)

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 21 of 106

ESD



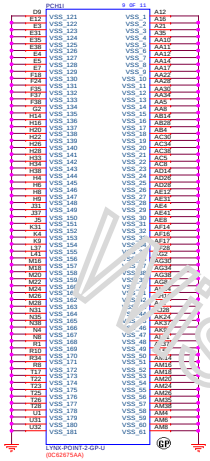
<Variant Name>

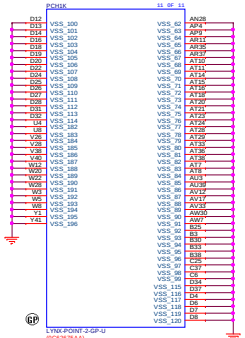
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

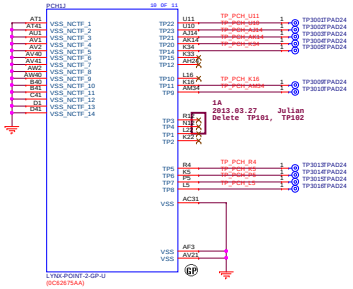
Title

Size	Document Number	Rev
C	B560 with GPU	SA

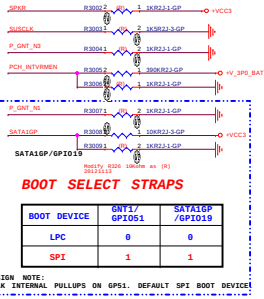
Date: Tuesday, May 13, 2014 Sheet 22 of 106

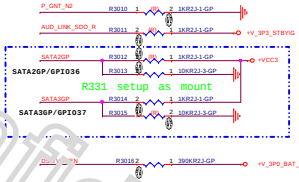


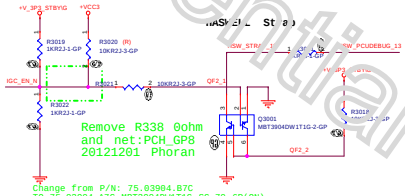




Straping Pin==> 20130510







Straping Pin define

Table 2-17. Functional Strap Definitions (Sheet 1 of 5)

Signal	Usage	When Sampled	Comment
SATA1GP / GPIO19	Boot BIOS Strap bit 0 (BBS0)	Rising edge of PWROK	This signal has a weak internal pull-up. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 / Bit 10 / Boot BIOS Destination 0 1 Reserved 1 0 Reserved 1 1 SPI (default) 0 0 LPC NOTES: 1. The internal pull-up is disabled after PLTRST# deasserts. 2. If option 00 (LPC) is selected, BIOS may still be placed on LPC, but the platform is required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GbE LAN. 4. See Chapter 10, "GCS—General Control and Status Register" for additional information.

Table 2-17. Functional Strap Definitions (Sheet 2 of 5)

Signal	Usage	When Sampled	Comment
GPIO51	Boot BIOS Strap bit 1 (BBS1)	Rising edge of PWROK	This signal has a weak internal pull-up. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. Bit11 / Bit 10 / Boot BIOS Destination 0 1 Reserved 1 0 Reserved 1 1 SPI (default) 0 0 LPC NOTES: 1. The internal pull-up is disabled after PLTRST# deasserts. 2. If option 00 (LPC) is selected, BIOS may still be placed on LPC, but the platform is required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GbE LAN. 4. See Chapter 10, "GCS—General Control and Status Register" for additional information.
SATA2GP / GPIO36	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. This signal should not be pulled high when strap is sampled.
SATA3GP / GPIO37	TLS Confidentiality	Rising edge of PWROK	This signal has a weak internal pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality) 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality) NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. A strong pull-up may be needed for GPIO functionality 3. This signal must be pulled up to support Intel AMT with TLS. Intel ME configuration parameters also need to be set correctly to enable TLS. 4. This signal is in the Core well.

Table 2-17. Functional Strap Definitions (Sheet 3 of 5)

Signal	Usage	When Sampled	Comment
HDA_SDO	Flash Descriptor Security Override	Rising edge of PWROK	This signal has a weak internal pull-down. 0 = Enable security measures defined in the Flash Descriptor. 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. NOTES: 1. The weak internal pull-down is disabled after PLTRST# deasserts. 2. If both HDA_SDO/HDA_SDO high on the rising edge of PWROK will also halt Intel® Management Engine after chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug. 3. This signal is in the Suspend well.
HDA_DOCK_EN# / GPIO33	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. This signal should not be pulled high when strap is sampled.
INTVRMEN	Integrated VRM Enable	Always	This signal does not have an internal resistor; an external resistor is required. 0 = DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source (should be connected to an external VRM). External VR powering option is for Mobile Only. Other systems should not pull the strap low. 1 = Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left floating. NOTES: 1. This signal is always sampled. 2. This signal is in the RTC well.
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	Rising edge of RSMRST#	This signal has a weak internal pull-up. 0 = Disable PLL On-Die voltage regulator. 1 = Enable PLL On-Die voltage regulator. NOTES: 1. The internal pull-up is disabled after RSMRST# deasserts. 2. This signal is in the Suspend well.

Table 2-17. Functional Strap Definitions (Sheet 4 of 5)

Signal	Usage	When Sampled	Comment
[illegible]	DeepSx Well On-Die Voltage Regulator Enable	Always	This signal does not have an internal resistor; an external resistor is required. 0 = Disable Integrated DeepSx Well (DSW) On-Die Voltage Regulator. 1 = Enable DSW 3.3V-to-1.05V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards; the external mode is only used for testing environments. NOTES: 1. This signal is always sampled. 2. This signal is in the RTC well.
GPIO8	Reserved	[illegible] of PWRSRST#	This signal has a weak internal pull-up but requires an external pull-down. NOTES: 1. The internal pull-up is disabled after RSMRST# deasserts. 2. This signal must be pulled low when strap is sampled. 3. This signal is in the Suspend well. 4. This signal has a weak internal pull-down.
SPKR	No Reboot	Rising edge of PWROK	0 = Disable [illegible] 1 = Enable [illegible] the TCO Timer will not reboot). NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. The status of this strap is reflected in the NO REBOOT bit (Chipset Config Registers: RCBA + Offset 3410h:Bit 5). 3. See Chapter 10, "GCS—General Control and Status Register" for additional information. 4. This signal is in the Core well.
GPIO53	Reserved	Rising edge of PWROK	This signal has a weak internal pull-up. NOTES: 1. The internal pull-up is disabled after PLTRST# deasserts. 2. This signal should not be pulled low when strap is sampled.

Table 2-17. Functional Strap Definitions (Sheet 5 of 5)

Signal	Usage	When Sampled	Comment
GPIO55	Top-Block Swap Override	Rising edge of PWROK	This signal has a weak internal pull-up. 0 = Enable "Top-Block Swap" mode - PCH will invert A16 for cycles going to the upper two 64 KB blocks in the FWH or appropriate address lines (A16, A17, A18, A19 or A20) as selected in BIOS Boot-Block size soft strap for SPI. 1 = Disable "Top-Block Swap" mode. NOTES: 1. The internal pull-up is disabled after PLTRST# deasserts. 2. Software will not be able to clear the Top-Block Swap bit until the system is rebooted. 3. This signal is in the Core well. 4. The status of this strap is readable using the Top-Block Swap bit (Chipset Config Registers: RCBA + Offset 3414h:Bit 0).
DDPB_CTRLDATA	Port B Detected	Rising edge of PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. 1 = Port B is detected. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts.
DDPC_CTRLDATA	Port C Detected	Rising edge of PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. 1 = Port C is detected. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts.
DDPD_CTRLDATA	Port D Detected	Rising edge of PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. 1 = Port D is detected. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts.

NOTE: See Section 3.1 for full details on pull-up/pull-down resistors.

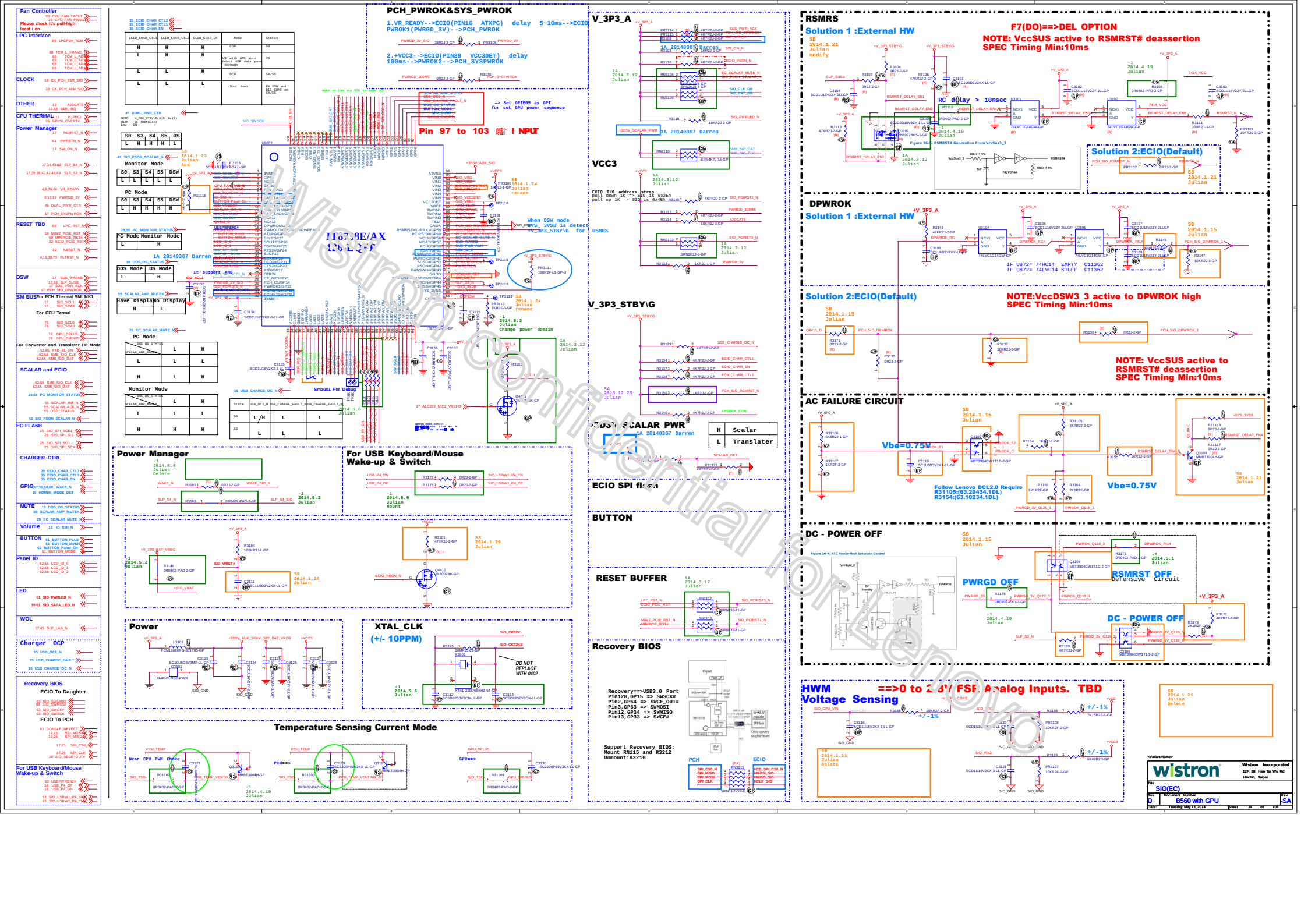
<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PCH(VSS)

Size: D | Document Number: B560 with GPU | Rev: SA

Date: Tuesday, May 13, 2014 | Sheet 23 of 105



Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: SIO(EC)

Size: D | Document Number: B560 with GPU | Rev: SA

Date: Tuesday, May 13, 2014 | Sheet 24 of 105

SPI ROM

17,24 SPI_MOSI
17,24 SPI_MISO
17 SPI_IO2
17 SPI_IO3
17,24 SPI_CLK
17,24 SPI_CS0_N
24 SIO_SBCE_OUT#

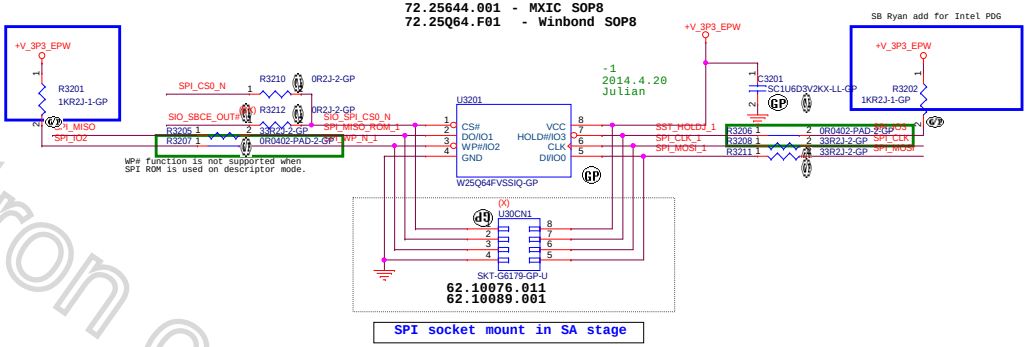
EC FW

24 SIO_SPI_SCE1_N
24 SIO_SPI_SI1
24 SIO_SPI_SO1
24 SIO_SPI_SCK1

PCH SPI ROM

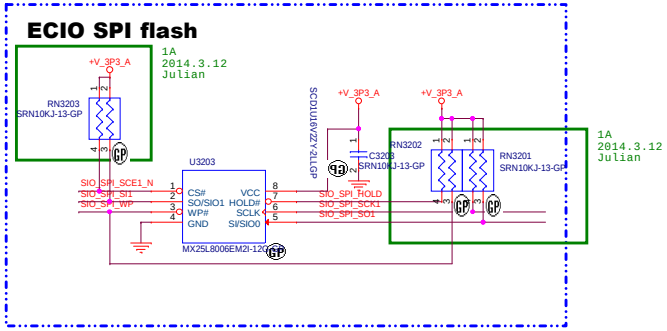
SOP8 for 8MB

72.25644.001 - MXIC SOP8
72.25Q64.F01 - Winbond SOP8

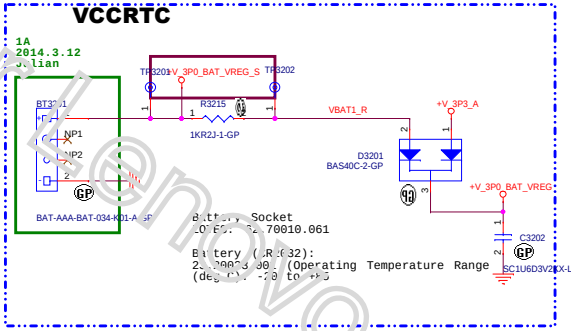


SPI socket mount in SA stage

ECIO SPI flash



VCCRTC



<Variant Name>

wistron

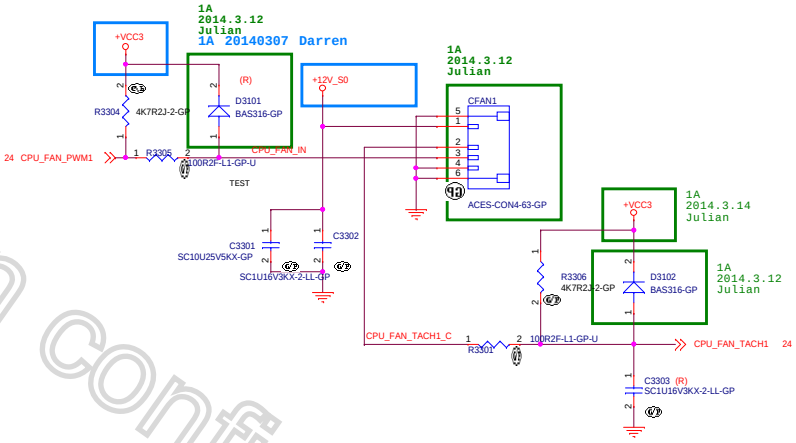
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Flash(EC+PCH)/BAT

Size: C | Document Number: B560 with GPU | Rev: SA

Date: Tuesday, May 13, 2014 | Sheet 25 of 106

CPU FAN



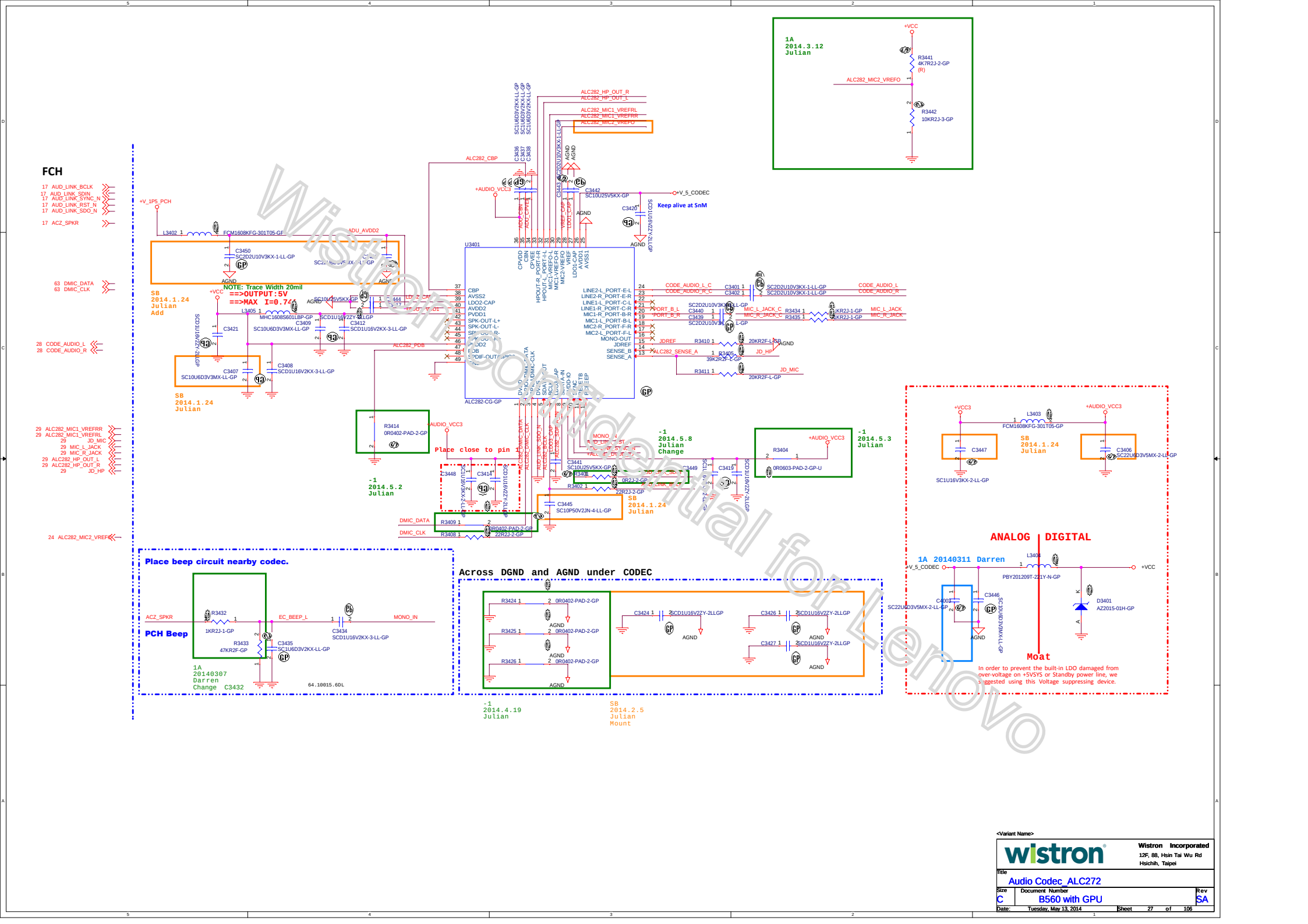
<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Fan control

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 26 of 106



<Variant Name>

Wistron Incorporated	12F, 88, Hsin Tai Wu Rd, Hsichih, Taipei
Title	Audio Codec_ALC272
Size	C
Document Number	B560 with GPU
Rev	SA
Date:	Tuesday, May 13, 2014
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F7==>(E):5W AMP
TPA3113==>5W

SHUTDOWN	TPA3111D2
L (0V~0.8V)	SHUTDOWN
H (2V ~ VDD)	ACTIVE

GAIN1	GAIN0	GAIN (dB)
0	0	20
1	0	26
~~0~~	~~1~~	~~32~~
~~1~~	~~1~~	~~36~~

LPF for fc(-3dB)=500Hz

SB 2014.2.5 Julian Add

SB 2014.4.27 Julian Mdify

SB 1202

-1 2014.4.19 Julian

-1 2014.5.7 Julian Modify

-1 2014.5.1 Julian

Audio Switch

SB 2014.1.21 Julian Swap L & R

SWING RANGE:
SWITCH:-2.2V~3.3V(DC:0.5V)
CODEC :0~5V(DC:2.5V)
SCALAR:0~3.3V(DC:1.65V)

L:CODEC PC Mode; H:Scalar Monitor mode

FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

Swing Limit

5W
3W
3W
5W

SB 2014.1.21 Julian Swap L & R net

-1 2014.4.30 Julian Solve POP noise issue Change to 0603 Size

1a 2014.3.18 Julian Finetune 5W Amp for 3W output

AMP MUTE

EC_SCALAR_MUTE_N
HIGH : MUTE AMP
LOW : UNMUTE AMP
SCALAR AMP MUTE CONTROL FROM SCALAR UNDER PC AND MONITOR MODE)
LOW : UNMUTE AMP WHEN NO DISPLAY
HIGH : MUTE AMP(WHEN HAVE DISPLAY)

ECIO_MUTE# (MUTE FROM ECIO UNDER PC MODE)
LOW : MUTE AMP UNDER POS
HIGH : UNMUTE AMP UNDER POS

ECIO_MUTE# (MUTE FROM ECIO UNDER MONITOR MODE)
KEEP HIGH : UNMUTE AMP

CODEC signals → 1 ON<==S0&Monitor mode
Switch Option 2 to 1
Scalar signals → 2 OFF
AMP Output ==>3W or ==>5W

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cy to fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the sup connected to PVCC. This "virtual" rail is 4 times the voltage at the PLIMIT pin. This output voltage can be usec calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L}$$ for unclipped power

Where:
R_S is the total series resistance including $R_{DS(on)}$ and any resistance in the output filter.
R_L is the load resistance.
V_P is the peak amplitude of the output possible within the supply rail.
$V_P = 4 \times$ PLIMIT voltage if PLIMIT < 4 × V_P
P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)

Table 2. PLIMIT Typical Operation

TEST CONDITIONS ()	PLIMIT VOLTAGE	OUTPUT POWER (W)	OUTPUT VOLTAGE AMPLITUDE (VP-P)
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=26dB	1.62	5	14
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=20dB	1.86	5	14.8
PVCC=12V, Vin=1Vrms, RL=8Ω, Gain=26dB	1.76	5	15

AMP PD# PIN MUTE TABLE

	S0		S5 HDMI IN mode	S5
EAPD#	1	0	NC(Q85 EC on)	NC(Q85 EC on)
SHDN_AMP_MUTE	1	1	1	0
ECIO_MUTE#	1	0	1	0
AMP	ON	OFF	on	OFF

EAPD#	0	0	1	1
SHDN_AMP_MUTE	0	1	1	0
ECIO_MUTE#	↓			
Audio_EC_SCALAR_MUTE_N	0	0	1	0

F7==>(C):3W AMP
Audio Ampify
ALC122==>3W

Please closed to chip

C3520 and C3506 closed to chip

From MCU or EC

G2	G1	Differential
0	0	11dB
0	1	14dB
1	0	19dB
1	1	24dB

Fixed Gain Mode (and Setting)

Mode1	Mode2	MODE	Pin11	Pin12
1	0	Fixed gain	G1	G2
0	1	I2C	SCL	SDA
1	1	PWM	PWM	Hold

Please Configure Mode selection according to your application

Volume (Gain) Control Mode selection=Fixed Gain Mode,BTL Mode

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Title: AUDIO_DSP OR AMP
Size: D | Document Number: B560 with GPU | Rev: SA
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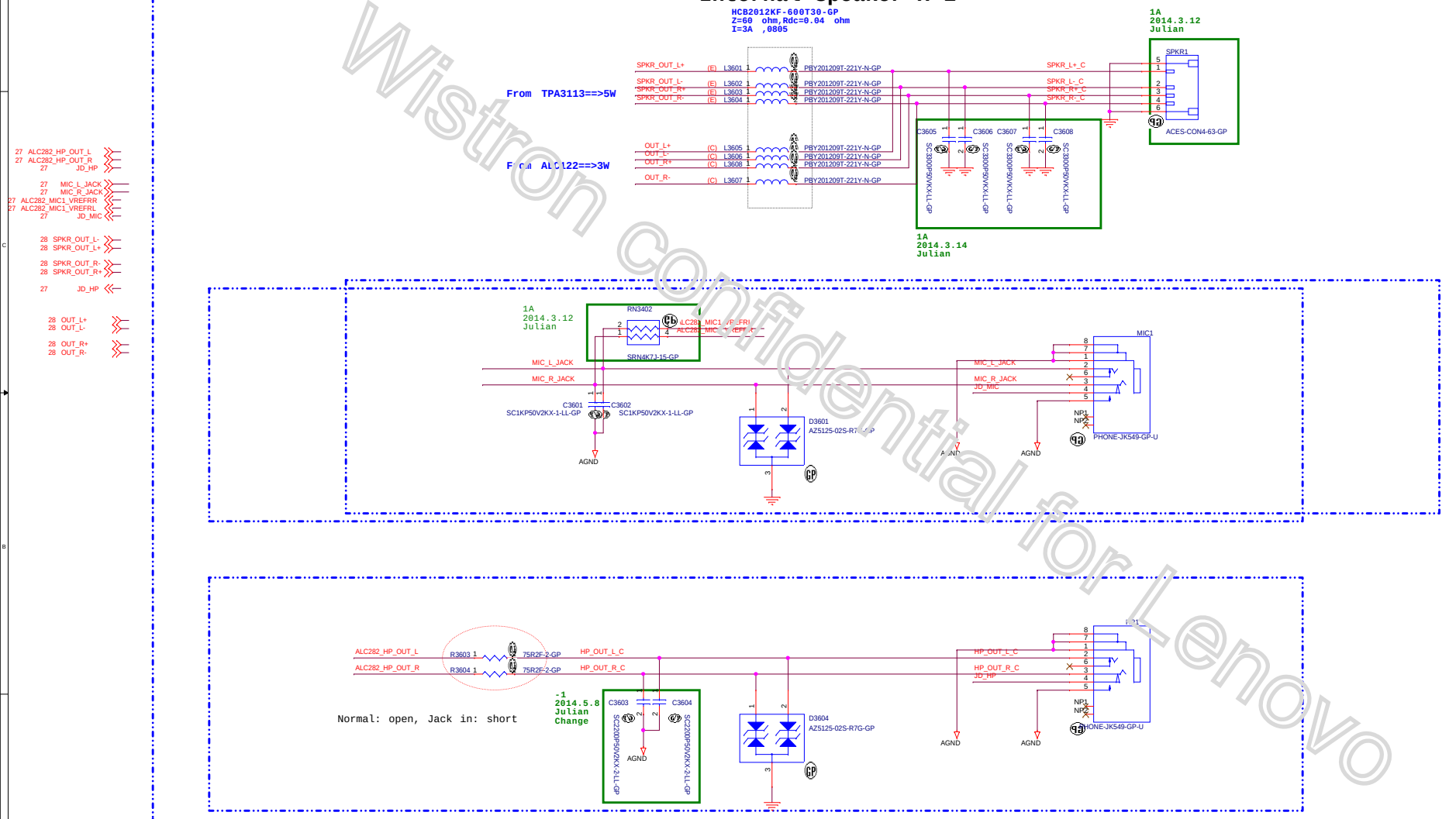
Internal Speaker x 2



27 ALC282_HP_OUT_L
27 ALC282_HP_OUT_R
27 JD_HP
27 MIC_L_JACK
27 MIC_R_JACK
27 ALC282_MIC1_VREFRR
27 ALC282_MIC1_VREFRL
27 JD_MIC
28 SPKR_OUT_L-
28 SPKR_OUT_L+
28 SPKR_OUT_R-
28 SPKR_OUT_R+
27 JD_HP
28 OUT_L+
28 OUT_L-
28 OUT_R+
28 OUT_R-

<Variant Name>

Wistron Incorporated
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Title: MIC/SPEAKER/AUDIO JACK

Size	Document Number	Rev
C	B560 with GPU	SA

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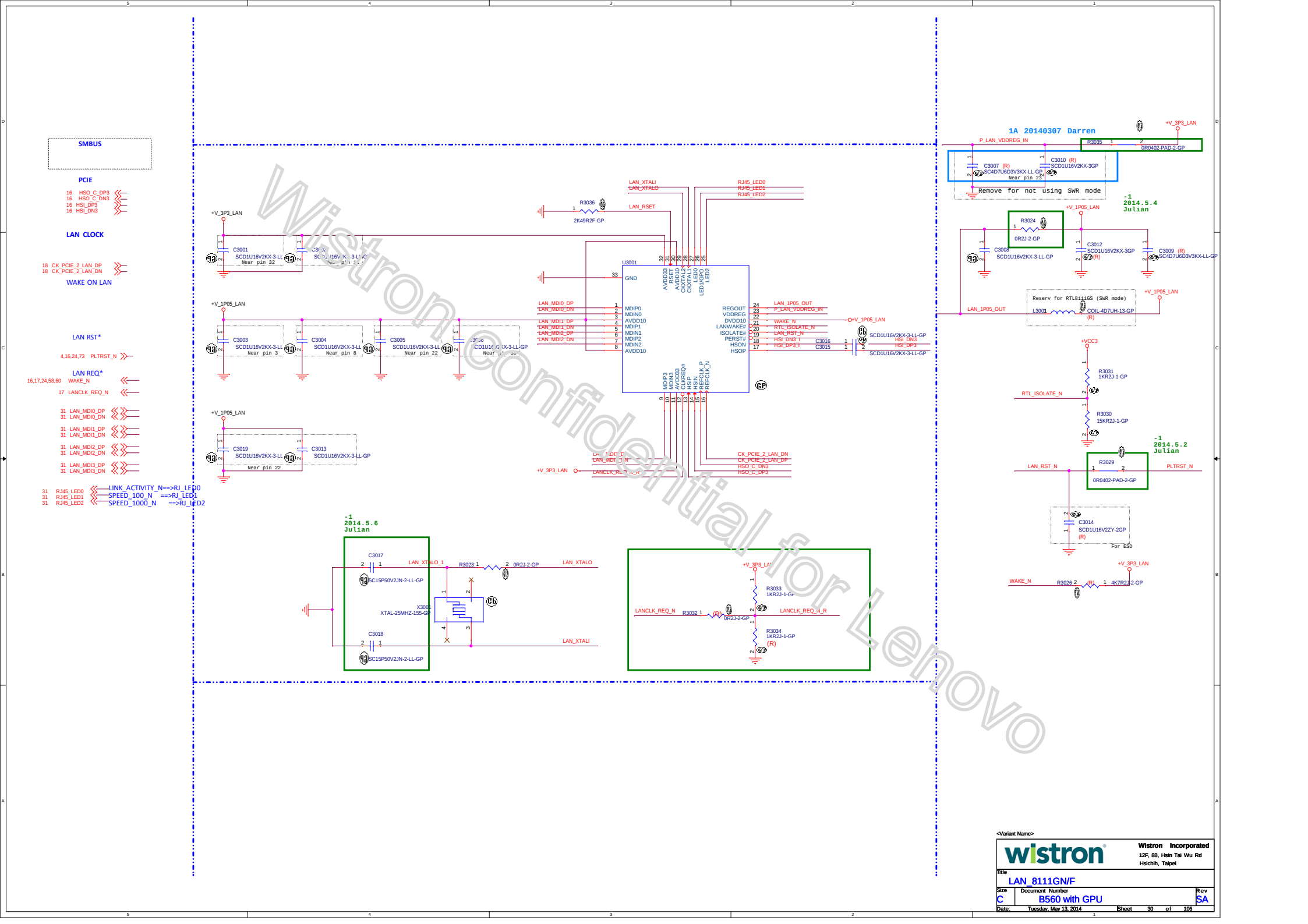

<Variant Name>

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Hsichih, Taipei

Title: LAN_8111GN/F

Size	Document Number	Rev
C	B560 with GPU	SA

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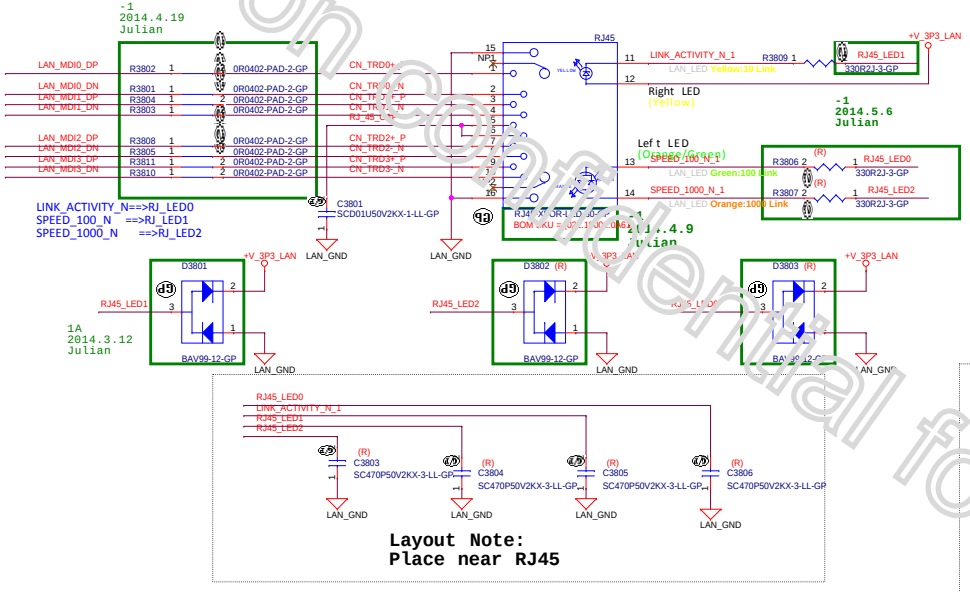
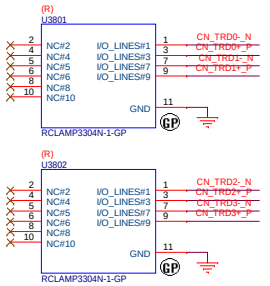
30 LAN_MDI0_DP
30 LAN_MDI0_DN
30 LAN_MDI1_DP
30 LAN_MDI1_DN
30 LAN_MDI2_DP
30 LAN_MDI2_DN
30 LAN_MDI3_DP
30 LAN_MDI3_DN
30 RJ45_LED0
30 RJ45_LED1
30 RJ45_LED2

Blink

		Giga	100	10
Left LED	Link	Blink	Blink	Yellow
Right LED	Act	Orange	Green	X

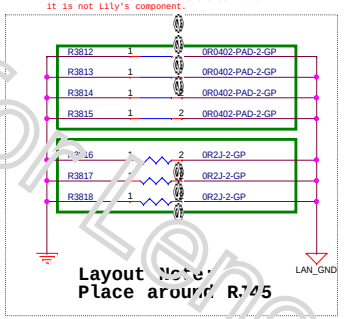


Reserve RClamp



L2 Previous component
60.00128.041: CHIP BEAD BK1005LL220-T TAIYO

C10 Previous component
70.18324.2FLLL: CHIP CAP C 0.01U 50V K0402 X7R
it is not Lily's component.



<Variant Name>

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Hsichih, Taipei Hsien

Title: RJ45+Transformer

Size	Document Number	Rev
C	B560 with GPU	SA

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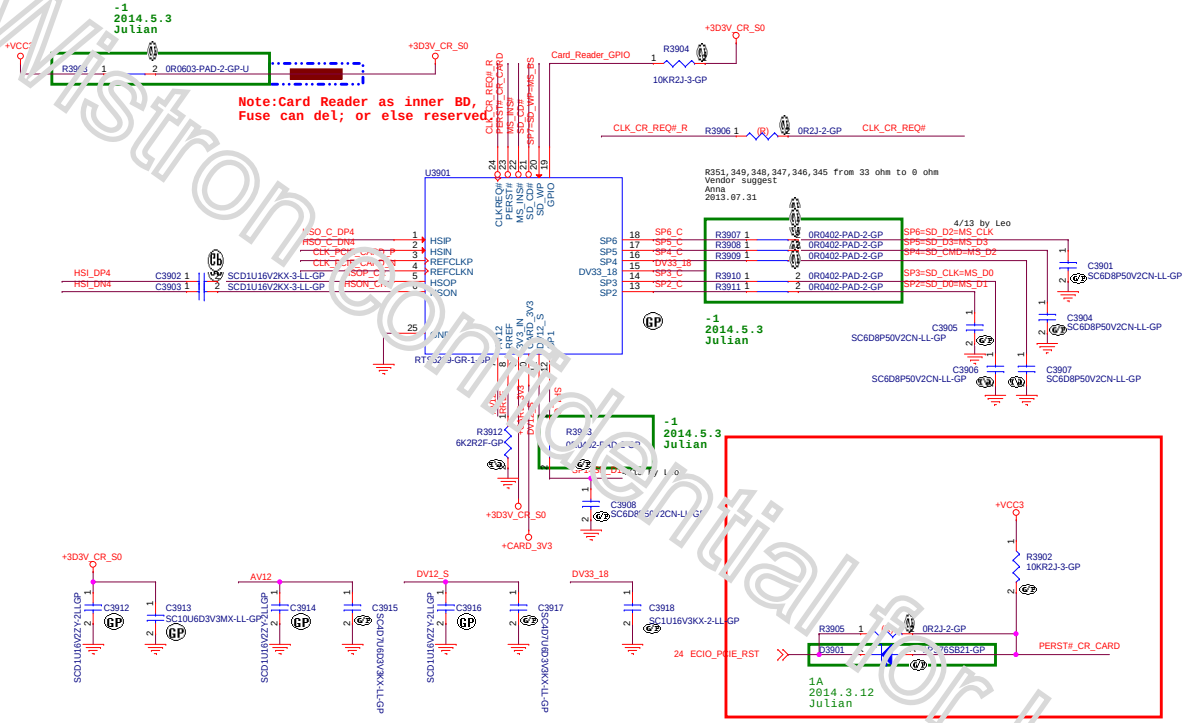
Card Reader



17 CLK_CR_REQ#

16 HSI_DN4
16 HSI_DP4
16 HSO_C_DN4
16 HSO_C_DP4

18 CLK_PCIE_CARD_P
18 CLK_PCIE_CARD_N

33 SP1=SD_D1
33 SP2=SD_D0=MS_D1
33 SP3=SD_CLK=MS_D0
33 SP4=SD_CMD=MS_D2
33 SP5=SD_D3=MS_D3
33 SP6=SD_D2=MS_CLK

33 SP7=SD_WP=MS_BS

33 SD_CD#
33 MS_INS#

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Card Reader_RTS5229

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 32 of 106

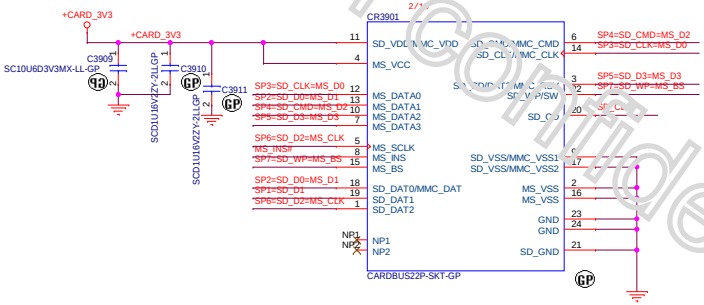
32 SP1=SD_D1
32 SP2=SD_D0=MS_D1
32 SP3=SD_CLK=MS_D0
32 SP4=SD_CMD=MS_D2
32 SP5=SD_D3=MS_D3
32 SP6=SD_D2=MS_CLK
32 SP7=SD_WP=MS_BS

32 SD_CD#
32 MS_INS#

6 in 1 :
SD, SDHC, SDXC/MMC, MS,
MS-Pro ,use PCI-E interface.
Support UHS-I SDXC/SDHC card.

SP7=SD_WP=MS_BS
SP6=SD_D2=MS_CLK
SP5=SD_D3=MS_D3
SP4=SD_CMD=MS_D2
SP3=SD_CLK=MS_D0
SP2=SD_D0=MS_D1
SP1=SD_D1

Share Pin



Pin No	For Card	Pin Assign	Function
1	SD	#9	SD-DAT2
2	MemoryStick	#10	MS-VSS
3	SD/MMC	#1	SD-CD/DAT3 MMC-RSV
4	MemoryStick	#9	MS-VCC
5	MemoryStick	#8	MS-SCLK
6	SD/MMC	#2	SD-CMD MMC-CMD
7	MemoryStick	#7	MS-DATA3
8	MemoryStick	#6	MS-INS
9	SD/MMC	#3	SD-VSS MMC-VSS1
10	MemoryStick	#5	MS-DATA2
11	SD/MMC	#4	SD-VDD MMC-VDD
12	MemoryStick	#4	MS-DATA0
13	MemoryStick	#3	MS-DATA1
14	SD/MMC	#5	SD-CLK MMC-CLK
15	MemoryStick	#2	MS-BS
16	MemoryStick	#1	MS-VSS
17	SD/MMC	#6	SD-VSS MMC-VSS2
18	SD/MMC	#7	SD-DAT0 MMC-DAT
19	SD	#8	SD-DAT1
20	SD	CD	SD-CD
21	SD	GND	SD-GND
22	SD	SW,WP	SD-WP(SW)

<Variant Name>

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Title: CARD Reader CONN

Size	Document Number	Rev
C	B560 with GPU	SA

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17,24,49,63 SLP_S4_N

USB2.0X2==>

16 USB_P1_DN
16 USB_P1_DP

USB3.0X2==>

16 USB3_RX2_DN
16 USB3_RX2_DP

16 USB3_TX2_DN
16 USB3_TX2_DP

16 USB_OC0_R_N

USB2.0

1A
2014.3.12
Julian

USB3.0 Colay USB2.0 PN:
22.10321.C91
UEA0112C-4FH1-4H
UEA0112C-4FH1-4F

+5V_DUAL
+USBVCC0
U4101
IN#2
IN#3
OUT#6
OUT#7
OUT#8
EN/EN#
FLT#
GND
GND
SLP_S4_N
USB_OC0_R_N
C4105
SCD1U16V2KX-3-LL-GP
TPS2001CDGNR-GP
TC4101
E100U16VM-65-GP
09.1071D.0RL

C4101
SCD01U50V2KX-1-LL-GP
C4102
SCD01U50V2KX-1-LL-GP

USB3_TX2_ESD_DP
USB3_TX2_ESD_DN
USB_P1_R_DN
USB_P1_R_DP
USB3_RX2_ESD_DP
USB3_RX2_ESD_DN

USB1
GND
STDA_SSTX+
VBUS
STDA_SSTX-
D-
GND_DRAIN
D+
STDA_SSRX+
GND
STDA_SSRX-
GND
SKT-USB11-102-GP

SB
2013.12.31
Julian

To PCH USB OC pin
SLP_S4_N: ==>From PCH Control
USBPWRENx: ==>From PCH Control

High SIDE USB3.0

SEC:Tripoli USB3.0==>022.10005.0221

ESD

D4102
LINE_1
LINE_2
GND
LINE_3
LINE_4
NC#10
NC#9
GND
NC#7
NC#6
AZ1045-04F-R7G-GP
BOM SKU = (075.3V3U4.0073)

D4103
I/O1
GND
I/O2
I/O4
VDD
I/O3
AZC099-04S-1-GP
C4111
SCD1U16V2ZY-2LGP

USB 2.0

1
2014.5.5
Julian
Delete co-lay parts

TR4103
USB_P1_DN
USB_P1_DP
USB_P1_R_DN
USB_P1_R_DP
COIL-90OHM-100MHZ-5-GP

USB 3.0

1
2014.5.5
Julian
Delete co-lay parts

SB
2014.1.16
Julian

TR4104
USB3_TX2_C_DN
USB3_TX2_C_DP
USB3_TX2_ESD_DN
USB3_TX2_ESD_DP
COIL-40OHM-GP

TR4105
USB3_RX2_DN
USB3_RX2_DP
USB3_RX2_ESD_DN
USB3_RX2_ESD_DP
COIL-40OHM-GP

Coupling caps

USB3_TX2_DP
USB3_TX2_DN
C4119
C4120
SCD1U16V2KX-3-LL-GP
USB3_TX2_C_DP
USB3_TX2_C_DN
From PCH USB3.0 port TX

<Variant Name>

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Title: USB 2.0/ 3.0 Port _X
Size: C
Document Number: B560 with GPU
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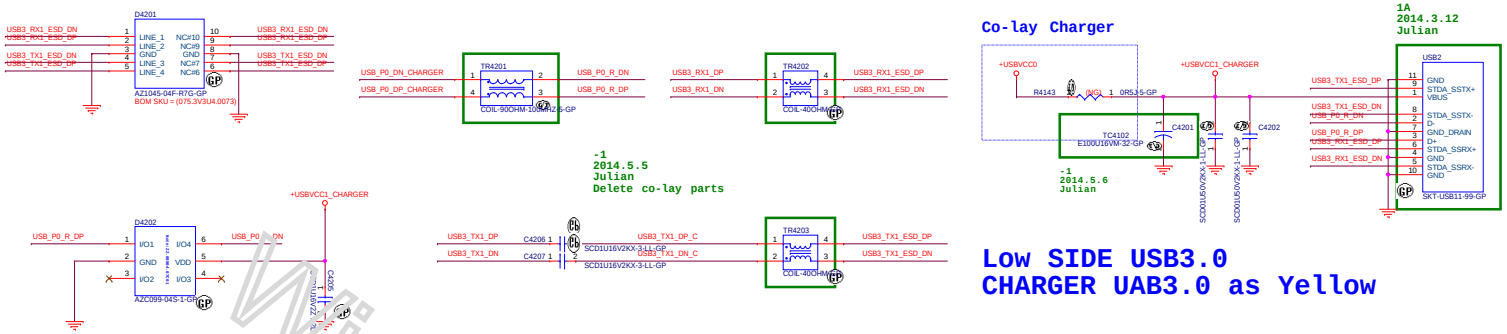
SIDE USB3.0 CONNECTOR



USB2.0
16 USB_P0_DN
16 USB_P0_DP

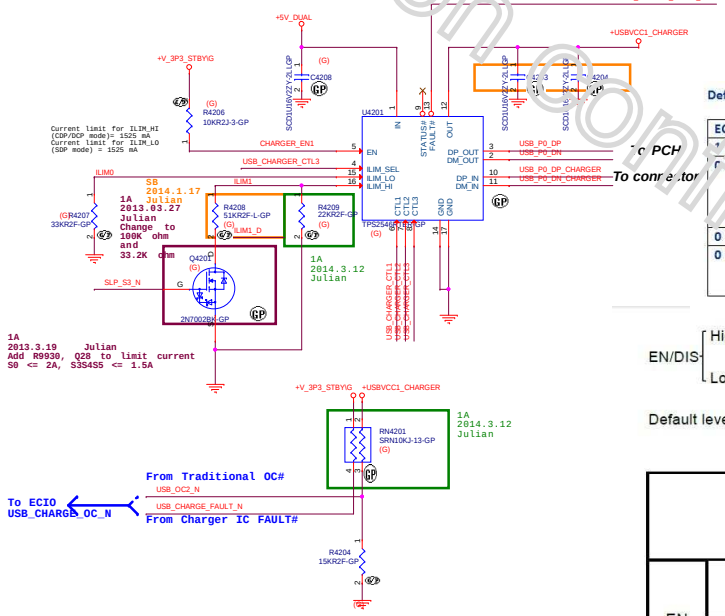
USB3.0
16 USB3_RX1_DN
16 USB3_RX1_DP
16 USB3_TX1_DN
16 USB3_TX1_DP

USB CHARGER (S0,S4,S5)

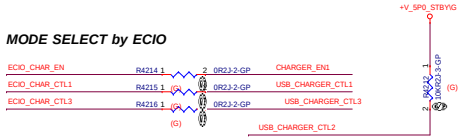
LOW SIDE USB3.0
S0: CDP(1.5A) S3: SDP(0.5A)
S4/S5: DCP(1.5A)

SB
2014.2.5
Julian
Change (G) to all SKU

OC EVENT FROM CHARGER IC



MODE SELECT by ECIO



Default status:

ECIO_CHAR_CTL1	ECIO_CHAR_CTL2	ECIO_CHAR_EN	Mode	State
1	1	1	CDP	S0
1	1	1	DCP with HID auto detect USB data pass through	S3
0	0	1	DCP	S4/S5
0	0	0	Shut down	EN DSW and DIS CHAR on S4/S5

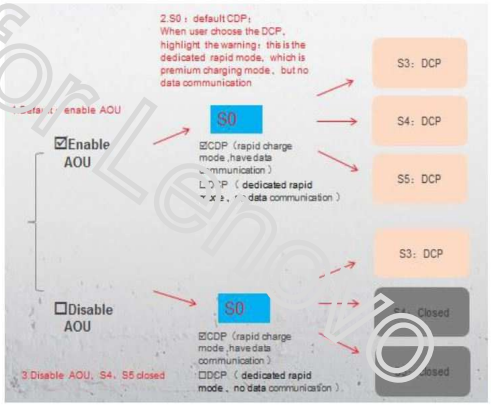
EN/DIS
- High: EN → Mode Select
- Low: Disable the charger function

Default level: EN/DIS GPIO: High
Mode selects GPIO: High

Control Signal		Mode Select	EN/DIS
		CNTL1	EN
EN	S0 CDP(1)	1	1
	S0 DCP	0	1
	S3 DCP	0	1
	S4/S5 DCP	0	1
DIS	S0 CDP	1	1
	S0 DCP	0	1
	S3 DCP	0	1
	S4/S5 Shut down	0/1	0

(1) Default status

1.2 DPM AP Function Control Introduce



6.3 Fault# signal application

Charger IC Fault# would trigger during over-temperature and current limit conditions and the charger IC would reset SMBUS (reset voltage and current) when Portable devices contact with Charger. So it would be erroneous triggered under current-limit and Charger IC discharger conditions.

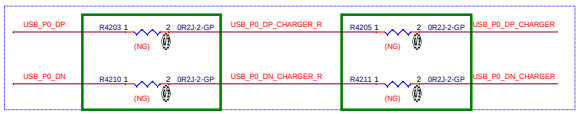
Suggestion:

6.3.1Blok Diagram

6.3.2 EC control

EC use traditional OC# and Charger IC Fault# to operation program to indicate short condition.
S0: Detect that if IC fault# signal is triggered, EC assert OC# to PCH.
S3: Detect that traditional OC'# and Charger IC fault# are both triggered, EC assert OC# to PCH.

Co-lay Charger



<Variant Name>

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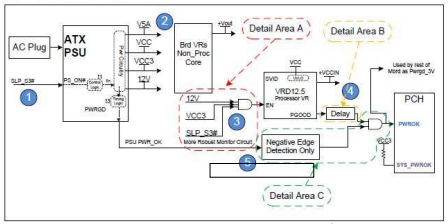
Title: USB Charger
Size: Custom | Document Number: B560 with GPU | Rev: SA
Date: Tuesday, May 13, 2014 | Sheet 35 of 106

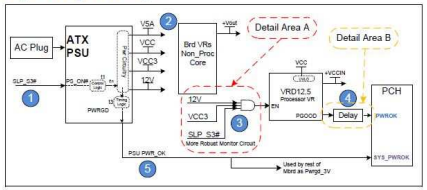
Figure 3-7. Option 3 Logic Flow Diagram



NOTES:

1. PS_ON# asserts, causing the PSU to turn on.
2. PSU main rails ramp, causing board VRs to start turning on
3. Core VR is enabled and ramps to Vboot once Main PSU rails are stable.
   a. Other Board VRs should already be ramped (and are assumed to be stable).
4. VR Pwrgood is asserted once Vboot, and after a small delay (~5-10 ms) (called out in Detail Area B in the above figure), the PCH's PWROK is asserted.
   a. PCH starts up clocks and other pre-reset activities.
5. PSU PWR_OK is only used for detecting AC power loss (i.e., negative edge detection) to trigger a clean shutdown

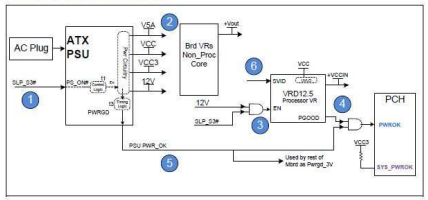
Figure 3-4. Option 2 Logic Flow Diagram



NOTES:

1. PS_ON# asserts, causing the PSU to turn on.
2. PSU main rails ramp, causing board VRs to start turning on.
3. Core VR is enabled and ramps to Vboot once Main PSU rails are stable.
   a. Other Board VRs should already be ramped (and are assumed to be stable).
4. VR Pwrgood is asserted once Vboot, and after a small delay (~5-10 ms) (called out in Detail Area B in the above figure), the PCH's PWROK is asserted.
   a. PCH starts up clocks and other pre-reset activities.
5. Eventually, PSU PWR_OK is asserted, which drives SYS_PWROK, causing Reset to de-assert.

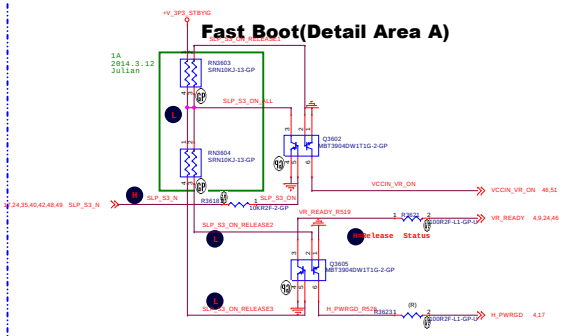
Figure 3-1. Option 1 Logic Flow Diagram

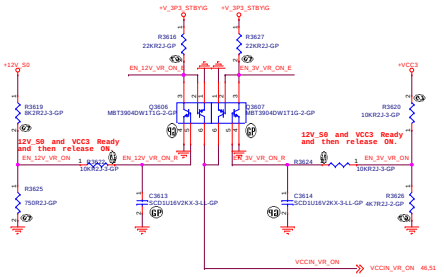


NOTES:

1. PS_ON# asserts, causing the PSU to turn on.
2. PSU main rails ramp, causing board VRs to start turning on.
3. Core VR is enabled and ramps to Vboot...
4. VR Pwrgood is asserted once Vboot is achieved.
5. Eventually, PSU PWR_OK is asserted. Now that both the processor VR Pwrgood and the PSU PWR_OK are both asserted, the PCH'S PWROK input is asserted.
   a. PCH starts up clocks and other pre-reset activities.
6. PCH asserts PROCPWRGD signal, which triggers SVID activity to ramp the Core VR.
7. Since SYS_PWROK is already asserted, there is no extra delay before Reset is de-asserted.

Fast Boot(Detail Area A)





Fast Boot(Detail Area B)

VR_READY-->SCHMITT-TRIGGER INVERTER to delay 5~10ms-->PWRGD_3V.
Reserve to implement by ECIO PWRGD_3V to PCH_PWROK.

Solution 2:ECIO(Default)

VR_READY-->ECIO(PIN16 ATXPG) delay 5~10ms-->ECIO PWROK1(PWRGD_3V)-->PCH_PWROK

PWRGD_3V → PWRGD_3V 9,17,19,24

19	16	ATXPG	DI	VCC3	***ATX Power Good*** The function of this symbol is ATX Power Good. PWROK1/2 will be (VCC3 power-level-detect **AND** SUSB# **AND** ATXPG) if bit 0 of Index 2Ch is 1, or (VCC3 power-level-detect **AND** SUSB#) if the bit is 0.
32	29	PWROK1	DOD8	VCC3	***Power OK 1 of VCC3*** The function of this symbol is Power OK 1 of VCC3.

SYS_PWROK

Detect VIN3(VCC3) and then delay 100MS
Reserve implement by ECIO PWRGD_100MS to PCH_SYSPWROK.

Solution 2:ECIO(Default)

+VCC3-->ECIO(PIN89 VCC3DET) delay 100ms-->PCH_SYSPWROK

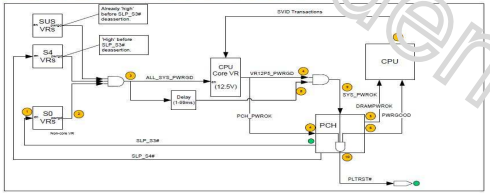
PCH_SYSPWROK → PCH_SYSPWROK 17,24

78	75	PWROK2	DOD8	VCC3	***Power OK 2 of VCC3*** The function of this symbol is Power OK 2 of VCC3.

U5 TO FIX 100MS DELAY ISSUE IN LPT A0.

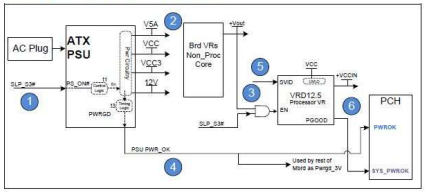
Since SYS_PWROK is already asserted, there is no extra delay before Reset is de-asserted.

POWER SEQUENCING



- SYS_PWROK can be optionally asserted with PCH_PWROK to reduce power-on latency.
- PCIe devices need to be under reset for 99ms after their power supplies are stable. However, mini-PCIe devices require only 1ms (refer PCI Express® Mini Card Electromechanical Specification Revision 1.21). System design can therefore set a delay between 1 to 99ms for ALL_SYS_PWRGD assertion to SYS_PWROK assertion.
- The separate rails for integrated graphics (VCCAXG), system agent (VCCSA), and the CPU I/O (VCCP) supplies have been replaced by the processor core rail (CPU VCC). SA_VR_PWROK is no longer required and hence is removed.
- The enable for the CPU VCC VR is tied to ALL_SYS_PWRGD and comes up immediately after ALL_SYS_PWRGD is asserted high to a predefined non-zero Vboot voltage. CPU SVID comes up later and is used by the CPU to read VR capabilities.
- UNCOREPWRGOOD, driven by the PCH, is repurposed to CPU PWRGOOD. It still indicates that clock is stable with the same timing but also signals CPU VCC power is good.

Figure 2-1. Typical Sugar Bay Logic Flow Diagram



Sequence:

1. PS_ON# asserts, causing the power supply unit (PSU) to turn on.
2. PSU main rails ramp, causing the board VRs to start turning on.
3. Core VR is enabled, but does not Ramp at this time
4. Eventually, PSU PWR_OK is asserted, which is feed into the PCH's PWROK input. PCH starts up clocks and other pre-reset activities.
5. PCH asserts PROCPWRGD signal, which triggers SVID activity to ramp the Core VR
6. Once the processor VR has ramped and its PwrGood output asserts, SYS_PWROK into the PCH is asserted, which releases Reset

Defensive Design for Typical Sugar Bay

<Variant Name>

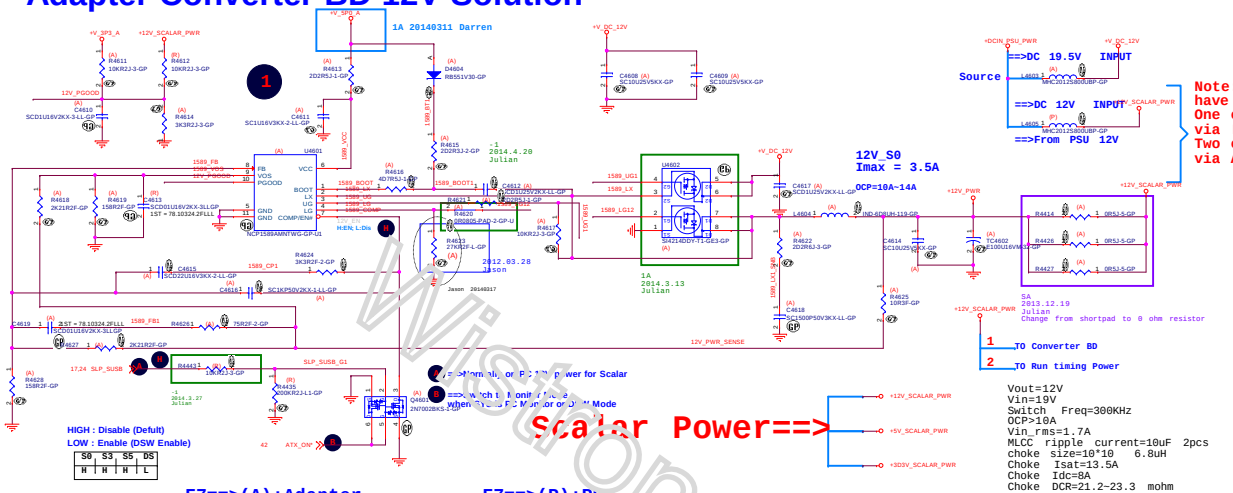
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
ADAPTER OCP / S3 reduction

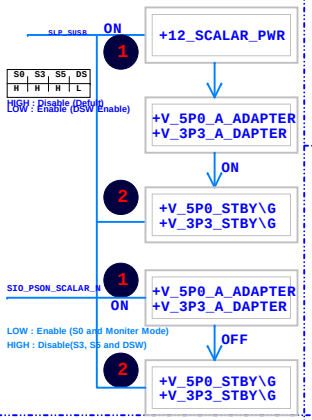
Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 37 of 106

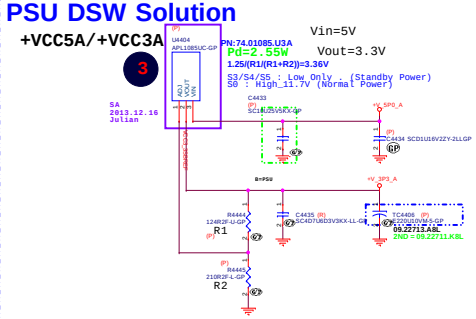
Adapter Converter BD 12V Solution



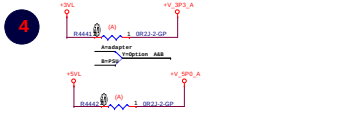
Vout=12V
Vin=19V
Switch Freq=300KHz
OCP>10A
Vin_rms=1.7A
MLCC ripple current=10uF 2pcs
choke size=10*10 6.8uH
Choke Isat=13.5A
Choke Idc=8A
Choke DCR=21.2~23.3 mohm
LIR=0.619
Vin Cap=10uF*2 pcs
Cout Cap=100u*1pcs
Cout cap_esr=24m ohm
OVP=RAMP VOS from 0.8 to 1.2



PSU DSW Solution

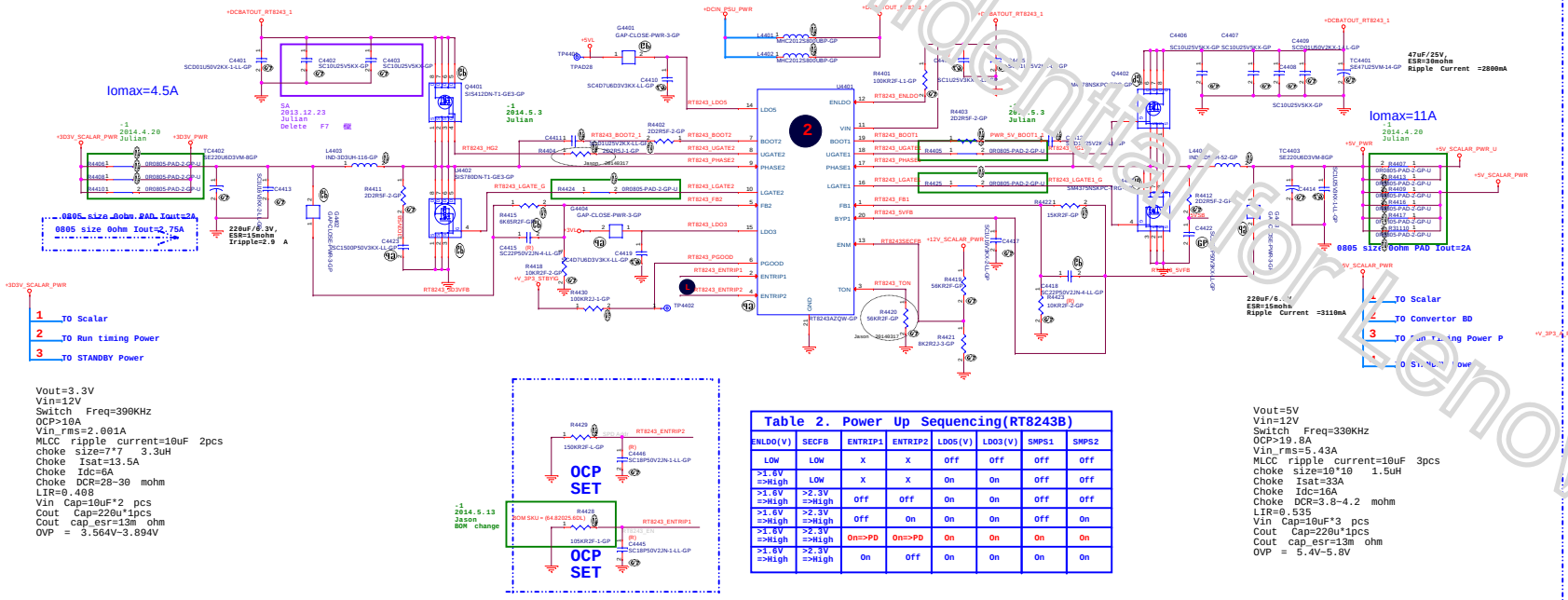


Adapter DSW Solution



Adapter DSW/Scalar Solution

Note :
+V_3P3_SCALAR==> +V_3P3_STBY\G
+V_5P0_SCALAR==> +V_5P0_STBY\G

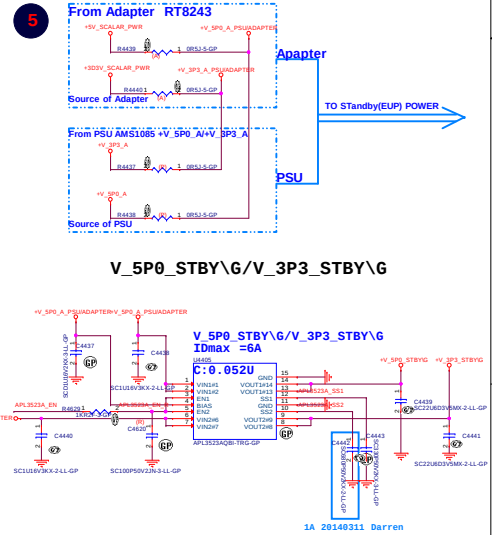


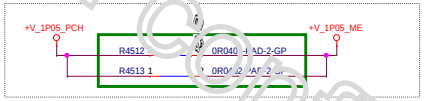
Vout=3.3V
Vin=12V
Switch Freq=390KHz
OCP>10A
Vin_rms=2.001A
MLCC ripple current=10uF 2pcs
choke size=7*7 3.3uH
Choke Isat=13.5A
Choke Idc=6A
Choke DCR=28~30 mohm
LIR=0.408
Vin Cap=10uF*2 pcs
Cout Cap=220u*1pcs
Cout cap_esr=13m ohm
OVP = 3.564V~3.894V

Table 2. Power Up Sequencing(RT8243B)							
ENLDO(V)	SECFB	ENTRIP1	ENTRIP2	LDO5(V)	LDO3(V)	SMPS1	SMPS2
LOW	LOW	X	X	Off	Off	Off	Off
>1.6V =>High	LOW	X	X	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	Off	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	On	On	On	Off	On
>1.6V =>High	>2.3V =>High	On=>PD	On=>PD	On	On	On	On
>1.6V =>High	>2.3V =>High	On	Off	On	On	On	On

Vout=5V
Vin=12V
Switch Freq=330KHz
OCP>19.8A
Vin_rms=5.43A
MLCC ripple current=10uF 3pcs
choke size=10*10 1.5uH
Choke Isat=33A
Choke Idc=16A
Choke DCR=3.8~4.2 mohm
LIR=0.535
Vin Cap=10uF*3 pcs
Cout Cap=220u*1pcs
Cout cap_esr=13m ohm
OVP = 5.4V~5.8V

Adapter/PSU EUP Solution





-1
2014.5.1
Julian

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 1D05_M

Size	Document Number	Rev
C	B560 with GPU	SA

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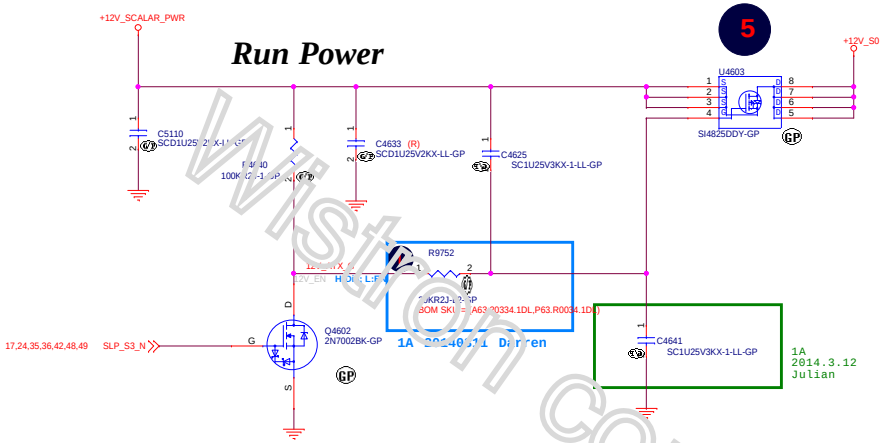
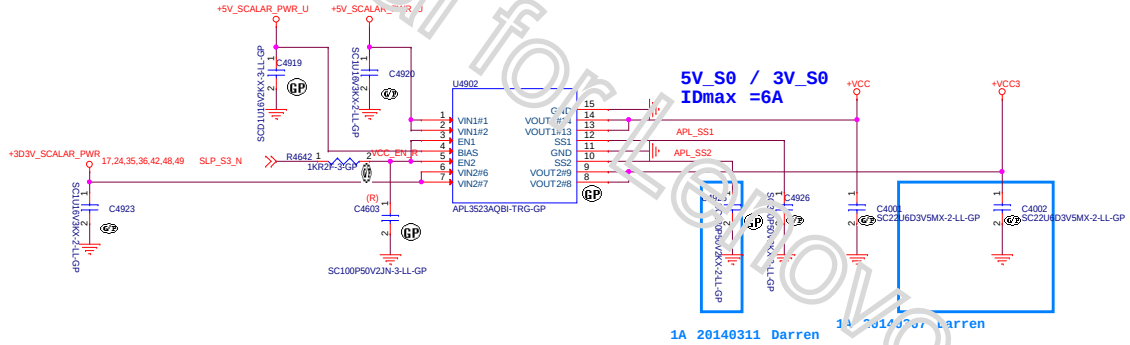
==>12V_S0



==>5V/3V_S0



<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PWR_RUN TIME POWER

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 40 of 106

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
(Reserved)

Size	Document Number	Rev
C	B560 with GPU	SA

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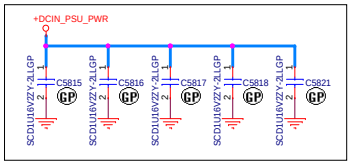
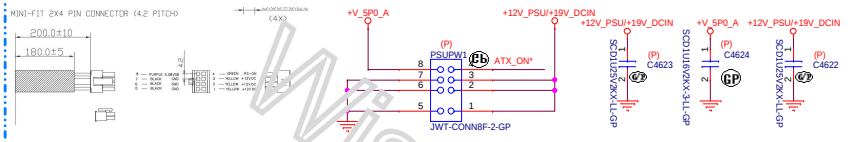
(1)PSU SOURCE==>

ATX CONNECTOR

SB
2014.1.27
Julian
Mount

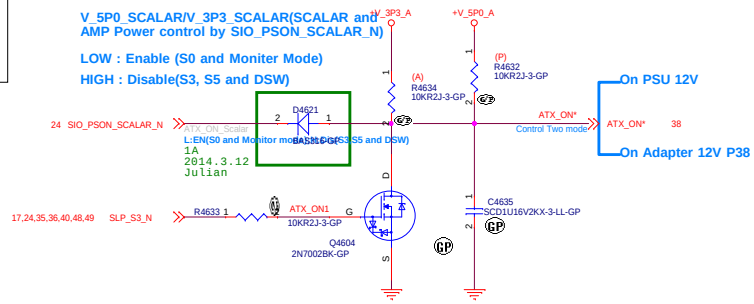




V_5P0_SCALAR/V_3P3_SCALAR(SCALAR and AMP Power control by SIO_PSON_SCALAR_N)

LOW : Enable (S0 and Moniter Mode)

HIGH : Disable(S3, S5 and DSW)

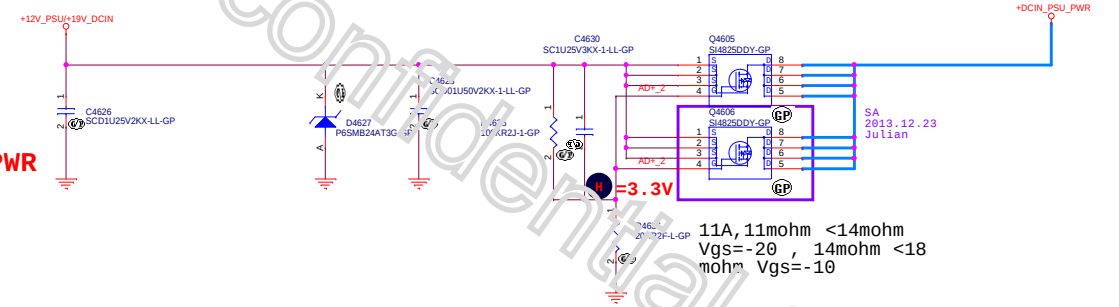


1==>PSU When ATX CONN

E7==>(P):PSU

E7==>(A):Adapter

3==>+DCIN_PSU_PWR

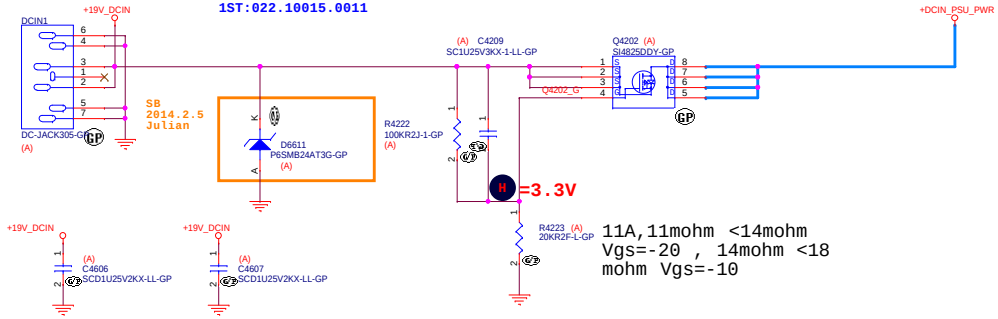


2==>Adapter when DCIN

(2)ADAPTER SOURCE==>

DCIN_CONNECTOR

==>DCIN1
PN:
1ST:022.10015.0011



<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DCIN JACK

Size: C | Document Number: B560 with GPU | Rev: SA

Date: Tuesday, May 13, 2014 | Sheet 42 of 106

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
BATT CONN

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 43 of 106

<Variant Name>

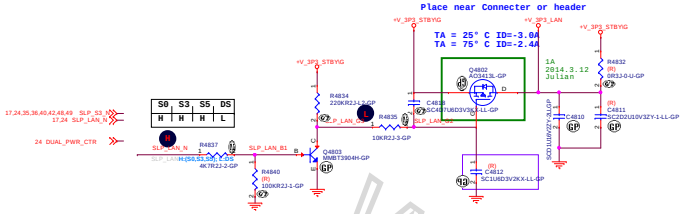
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
DC to DC_5V/3D3V_S0

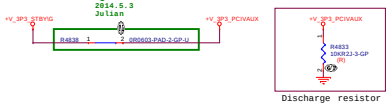
Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 44 of 106

V_3P3_LAN



V_3P3_A_PCIVAUX



V_3P3_EPW

Stuff when use Intel LAN Clarkville
For AMT M0-M3 support

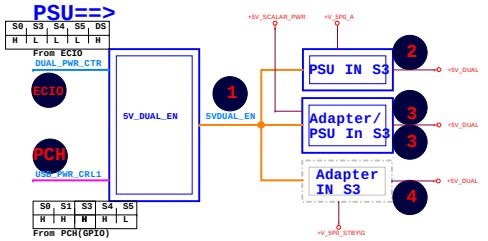
==>0.025A for BIOS POWER

Stuff when use
Relteak LAN <==B360 LAN:REALTEK

Lenovo suggestion:
Change R4844.2 +VCC3 to +V_3P3_STBY\G
20130807

==>FOR Adapter/PSU DUAL Enable

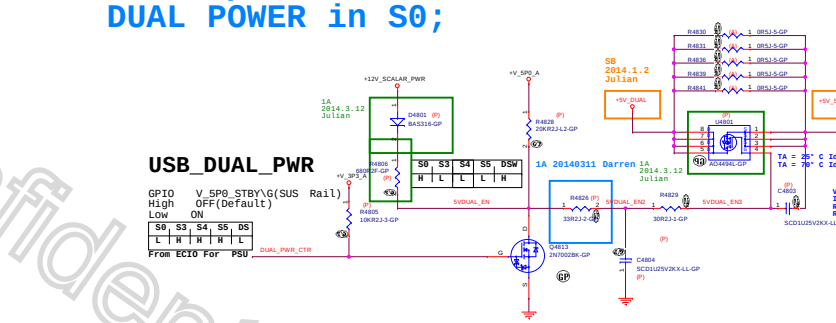
Rear USB PWR



==>Adapter/PSU Share
DUAL POWER in S0;

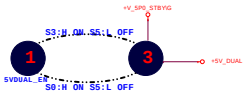
OUTPUT==
USB3.0x1(0.9A)+USB3.0 Chargerx1(2.0A)
USB2.0x3(1.5A)+Dimm(4.5A)=8.9A

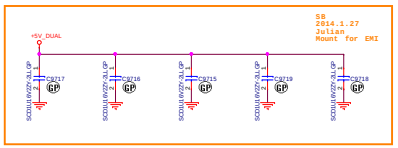
Charger==>ON:S0,S3,S4,S5
Adapter==>ON:S0,S3
PSU==>ON:S0



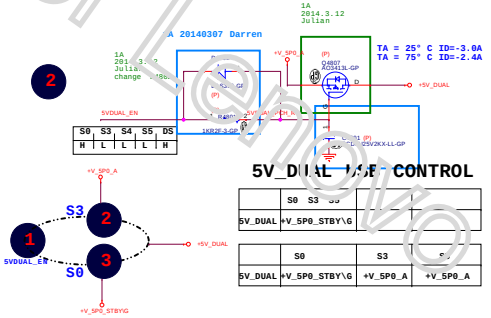
Dual Power Assign Case

	POWER	S0	S3	S4	S5	DS
Source(9.3A)	+5V_DUAL	ON	ON	ON	ON	OFF
USB1 Power(0.9A) Touch Power(0.5A)	+USBVCC1	ON	ON	OFF	OFF	OFF
USB3~USB5(1.5A)	+USBVCC4_USB5	ON	ON	OFF	OFF	OFF
Dimm power(4.5)	+PWR_1D5V_DDR_ATC	ON	ON	OFF	OFF	OFF
Charger Power(2.0A)	+USBVCC1_CHARGE	ON	ON	ON	ON	OFF





==>FOR PSU DUAL POWER in S3

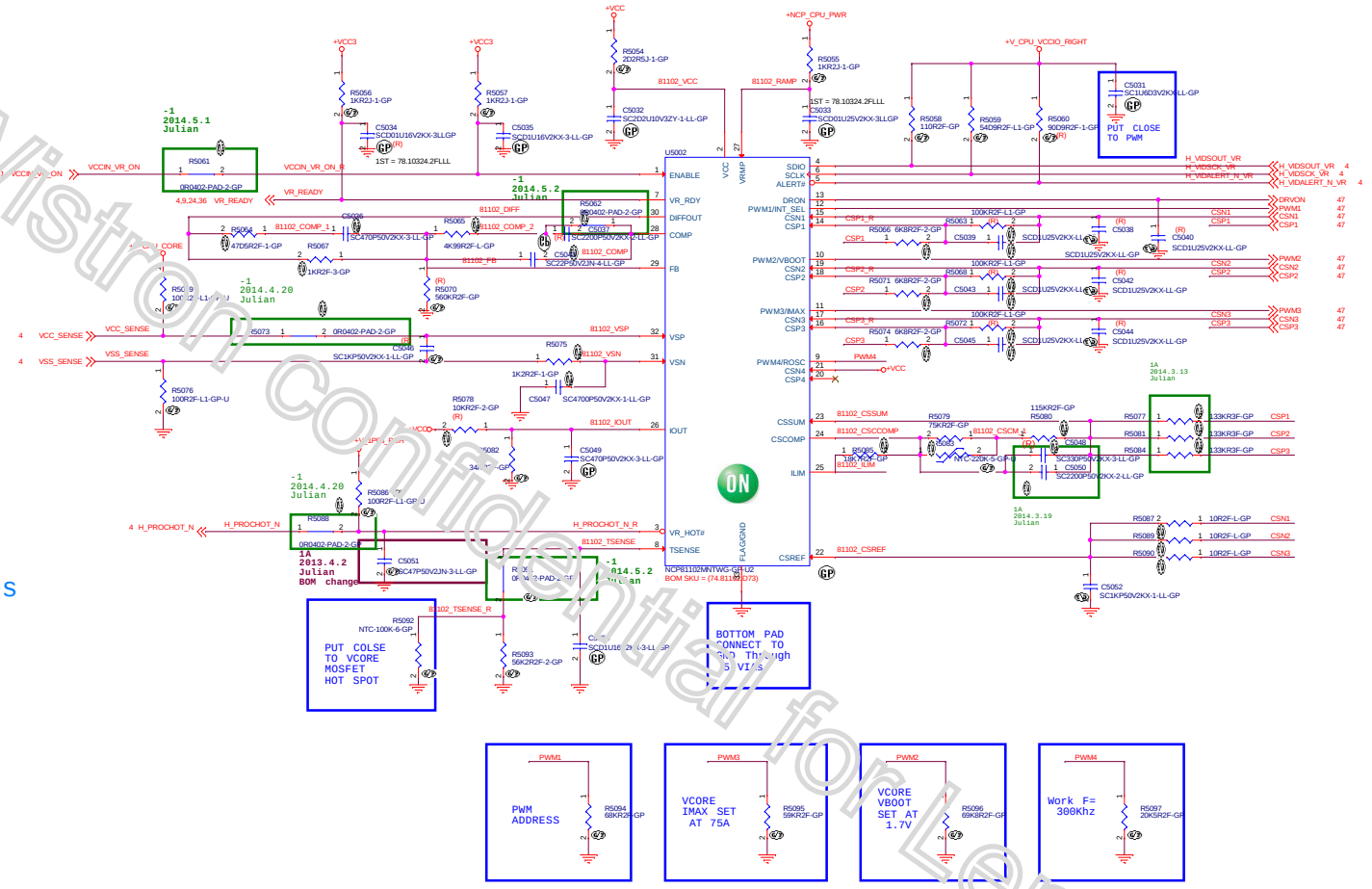


5V_DUAL_EN CONTROL

	S0	S3	S5
5V_DUAL	+V_5P0_STBY\G		

	S0	S3	S5
5V_DUAL	+V_5P0_STBY\G	+V_5P0_A	+V_5P0_A

VCC_CORE SharkBay VR12.5 POWER CKT - 3 PHASE



CPU VCORE POWER

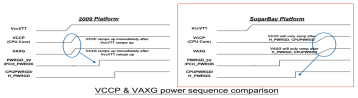
4 VCC_SENSE
4 VSS_SENSE
4 H_VIDSOUT_VR
4 H_VIDSCK_VR
4 H_VIDALERT_N_VR
47 PWM1
47 CSN1
47 CSP1
47 PWM2
47 CSN2
47 CSP2
47 PWM3
47 CSN3
47 CSP3
4,9,24,36 VR_READY

HOT

4 H_PROCHOT_N

Platform Power Sequence Changes

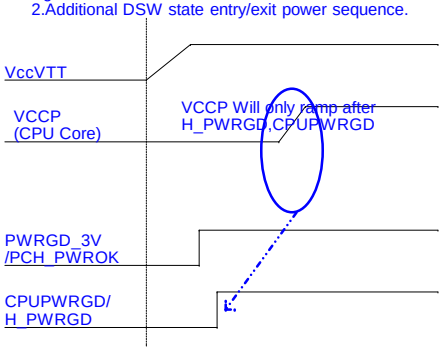
- Changes from 2009 Platform – Sugar Bay:
  1. VCCP (CPU Core) and VAXG rails only turn on AFTER the H_PWRGD, CPUPWRGD, and other uncore PWRGD signals assert.
  2. Additional DSW state entry/exit power sequence.



VCCP & VAXG power sequence comparison

Platform Power Sequence Changes

1.VCCP(CPU Core) rails only turn on after the H_PWRGD, CPUPWRGD, and other uncore PWRGD signals assert.
2.Additional DSW state entry/exit power sequence.



VCCP&VAXG power sequence comparison

<Variant Name>

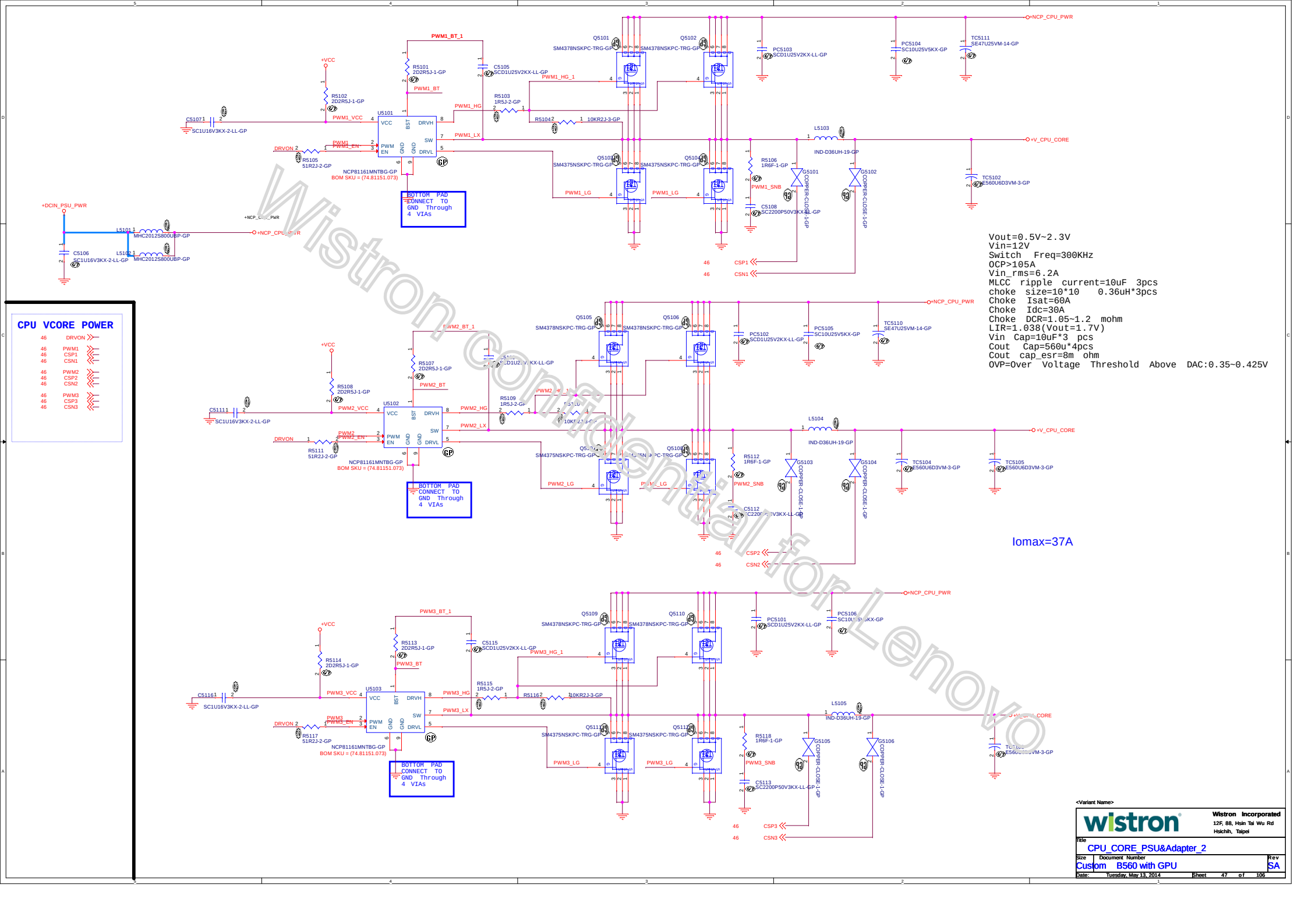
wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

title: CPU_CORE_PSU&Adapter_1

Size: Custom | Document Number: B560 with GPU | Rev: SA

Date: Tuesday, May 13, 2014 | Sheet 46 of 106


CPU VCORE POWER
DRVON
PWM1
CSN1
CSP1
PWM2
CSP2
CSN2
PWM3
CSP3
CSN3
+NCP_CPU_PWR
+V_CPU_CORE
+DCIN_PSU_PWR
+VCC
PWM1_BT_1
PWM1_BT
PWM1_VCC
PWM1_HG
PWM1_LX
PWM1_LG
PWM1_EN
PWM1_SNB
PWM1_HG_1
U5101
NCP81161MNTBG-GP
BOM SKU = (74.81151.073)
BOTTOM PAD CONNECT TO GND Through 4 VIAs
Q5101
Q5102
Q5103
Q5104
SM4378NSKPC-TRG-GP
SM4375NSKPC-TRG-GP
L5103
IND-D36UH-19-GP
R5101 2D2R5J-1-GP
R5102 2D2R5J-1-GP
R5103 1R5J-2-GP
R5104 10KR2J-3-GP
R5105 51R2J-2-GP
R5106 1R6F-1-GP
C5105 SCD1U25V2KX-LL-GP
C5106 SC1U16V3KX-2-LL-GP
C5107 SC1U16V3KX-2-LL-GP
C5108 SC2200P50V3KX-LL-GP
L5101 MHC2012S800UBP-GP
L5102 MHC2012S800UBP-GP
PC5103 SCD1U25V2KX-LL-GP
PC5104 SC10U25V5KX-GP
TC5111 SE47U25VM-14-GP
TC5102 E560U6D3VM-3-GP
G5101 COPPER-CLOSE-1-GP
G5102 COPPER-CLOSE-1-GP
PWM2_BT_1
PWM2_BT
PWM2_VCC
PWM2_HG
PWM2_LX
PWM2_LG
PWM2_EN
PWM2_SNB
PWM2_HG_1
U5102
Q5105
Q5106
Q5107
Q5108
L5104
R5107 2D2R5J-1-GP
R5108 2D2R5J-1-GP
R5109 1R5J-2-GP
R5111 51R2J-2-GP
R5112 1R6F-1-GP
C5111 SC1U16V3KX-2-LL-GP
C5112 C2200P50V3KX-LL-GP
PC5102 SCD1U25V2KX-LL-GP
PC5105 SC10U25V5KX-GP
TC5110 SE47U25VM-14-GP
TC5104 E560U6D3VM-3-GP
TC5105 E560U6D3VM-3-GP
G5103 COPPER-CLOSE-1-GP
G5104 COPPER-CLOSE-1-GP
PWM3_BT_1
PWM3_BT
PWM3_VCC
PWM3_HG
PWM3_LX
PWM3_LG
PWM3_EN
PWM3_SNB
PWM3_HG_1
U5103
Q5109
Q5110
Q5111
Q5112
L5105
R5113 2D2R5J-1-GP
R5114 2D2R5J-1-GP
R5115 1R5J-2-GP
R5116 10KR2J-3-GP
R5117 51R2J-2-GP
R5118 1R6F-1-GP
C5115 SCD1U25V2KX-LL-GP
C5116 SC1U16V3KX-2-LL-GP
C5113 SC2200P50V3KX-LL-GP
PC5101 SCD1U25V2KX-LL-GP
PC5106 SC10U25V5KX-GP
G5105 COPPER-CLOSE-1-GP
G5106 COPPER-CLOSE-1-GP
Vout=0.5V~2.3V
Vin=12V
Switch Freq=300KHz
OCP>105A
Vin_rms=6.2A
MLCC ripple current=10uF 3pcs
choke size=10*10 0.36uH*3pcs
Choke Isat=60A
Choke Idc=30A
Choke DCR=1.05~1.2 mohm
LIR=1.038(Vout=1.7V)
Vin Cap=10uF*3 pcs
Cout Cap=560u*4pcs
Cout cap_esr=8m ohm
OVP=Over Voltage Threshold Above DAC:0.35~0.425V
Iomax=37A
Wistron Confidential for Lenovo
<Variant Name>
wistron
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
CPU_CORE_PSU&Adapter_2
Size
Custom
Document Number
B560 with GPU
Rev
SA
Date: Tuesday, May 13, 2014
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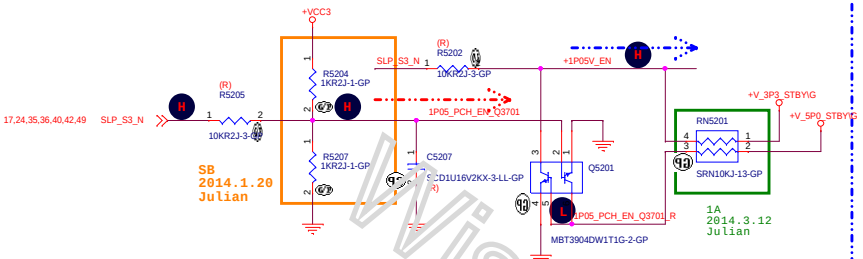
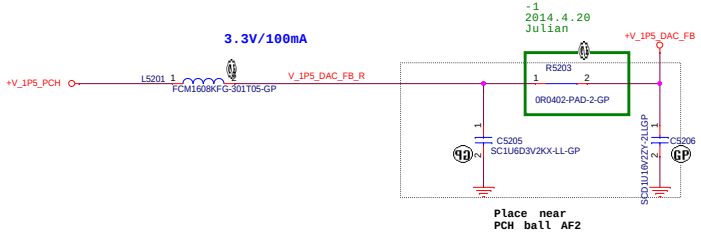
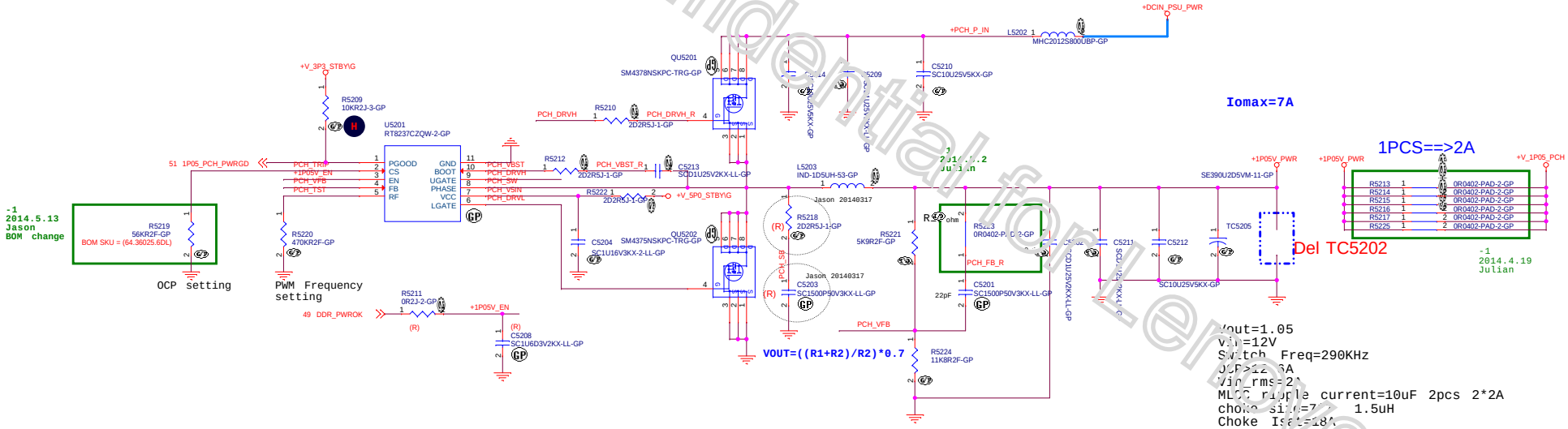
V_1P5_DAC_FB_R





V_1P05_PCH ==>FOR Adapter&PSU



Vout=1.05
Vin=12V
Switch Freq=290KHz
IOCP>12.6A
Vin_rms=2A
MLCC ripple current=10uF 2pcs 2*2A
choke size=7*7* 1.5uH
Choke Isat=18A
Choke Irms=9A
Choke DCR=14~15 mohm
LIR=0.325
Vin Cap=10uF*2 pcs
Cout Cap=820u*1pcs
Cout cap_esr=7m ohm
OVP點1.26V~1.365V

<Variant Name>

wistron Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DC to DC_1D05V_S0_PCH

Size	Document Number	Rev
C	B560 with GPU	SA

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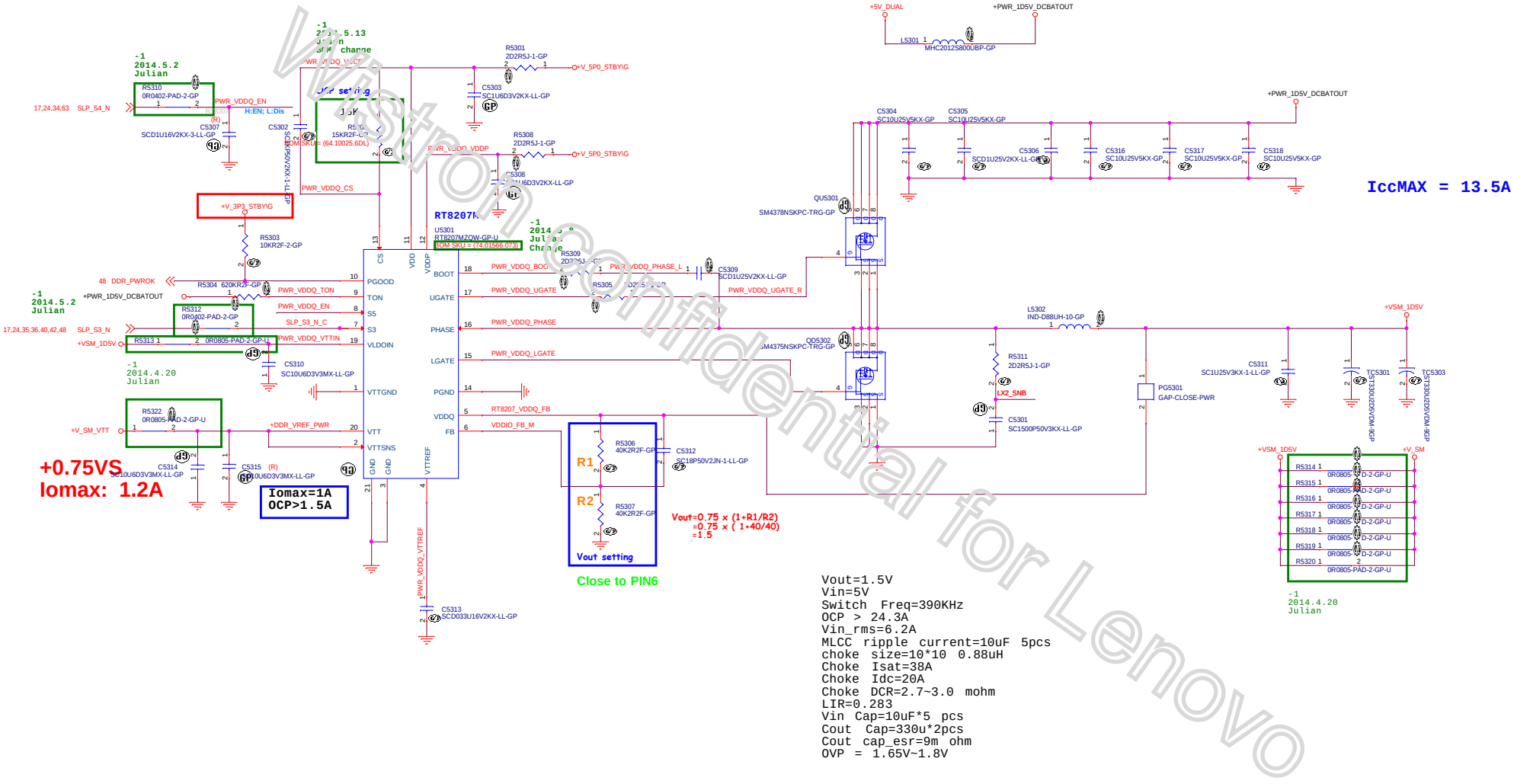

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DC to DC_1D35V_0D675V_DIMM

Size	Document Number	Rev
C	B560 with GPU	SA

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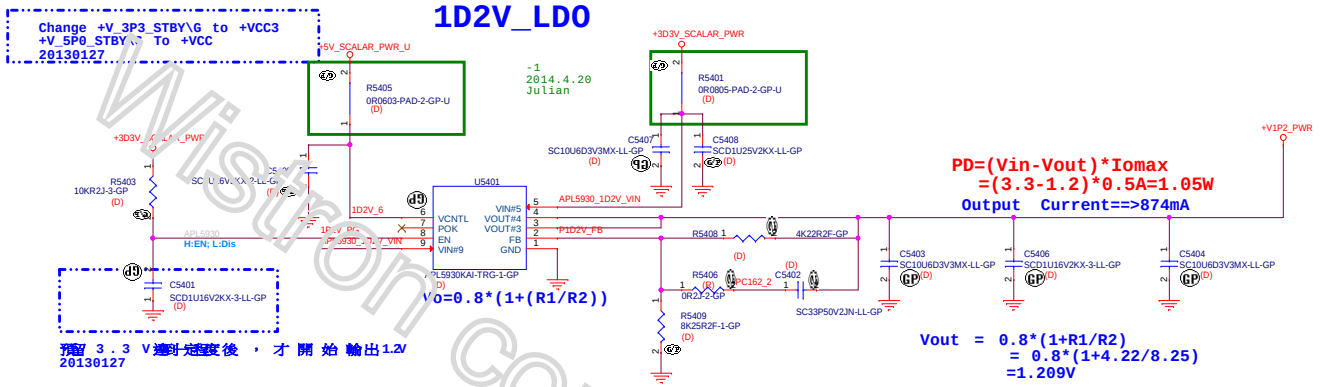
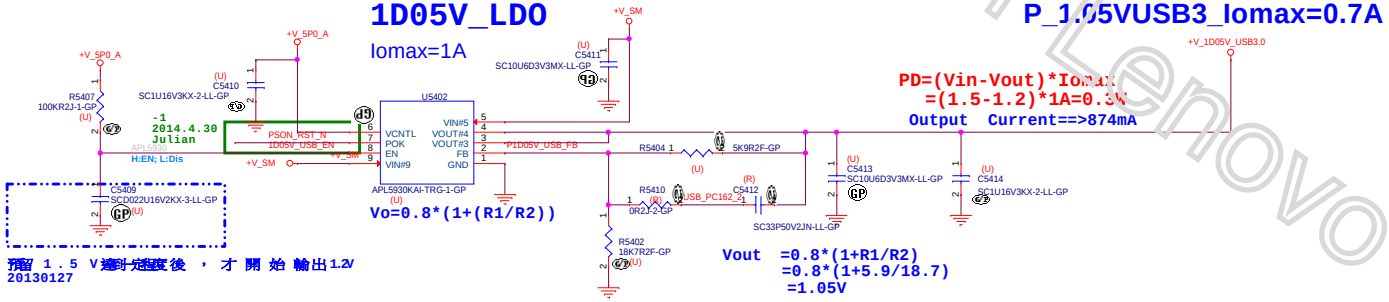
1D2V (Scalar)

1D2V_LDO

Iomax=0.5A



1D05V (USB3.0 Controller)



16 PSON_RST_N

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

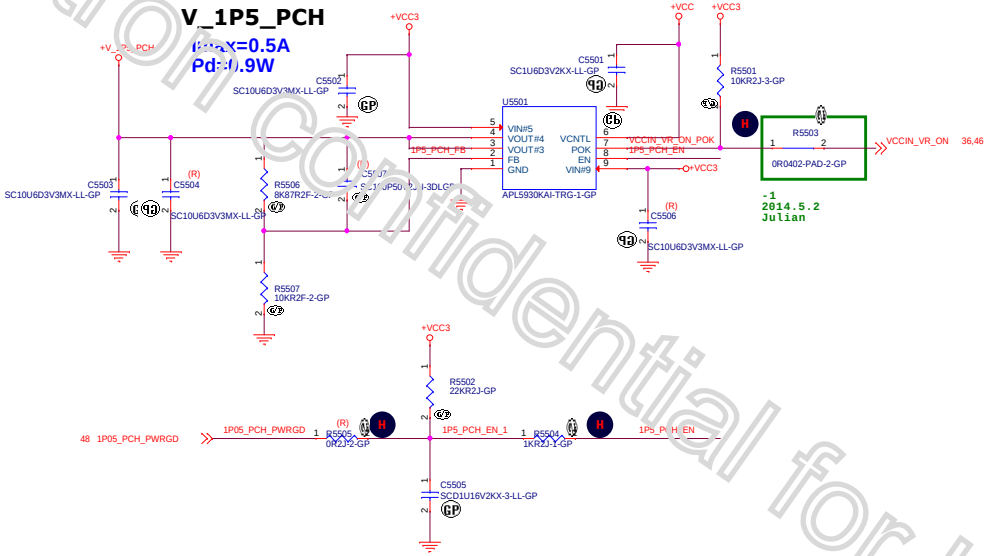
Title

DC to DC 1D8V 1D2V

Size C | Document Number | Rev SA

Date: Tuesday, May 13, 2014 | Sheet 50 of 106

PD=(Vin-Vout)*Iomax
=(3.3-1.5)*0.5A=0.9W



<Variant Name>

wistron

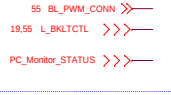
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DC to DC_1D5V_PCH

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 51 of 106

Panel Control



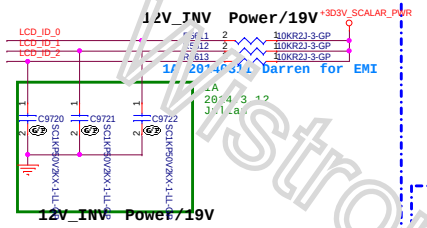
Panel ON/OFF

SA
2013.12.23
Julian

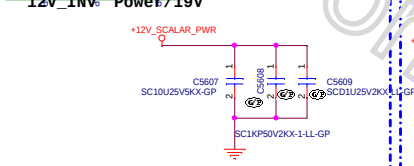
-1
2014.5.2
Julian

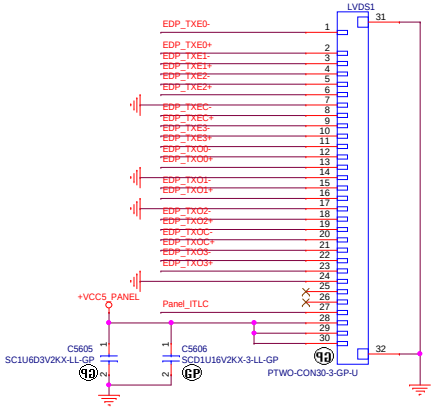
H: Enable
L: Disable

12V_INV Power/19V



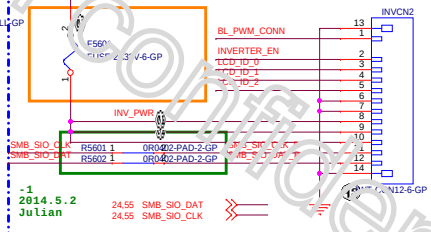
1/ 2014/3/1 Darren for EMI





Panel Size 21.5'&23'

SB
2014.1.16
Julian



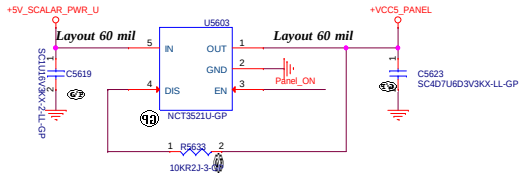
-1
2014.5.2
Julian

24,55 SMB_SIO_DAT
24,55 SMB_SIO_CLK

20130106 TRIPOLI SC
Add Brightness Control for WIN8
L:CODEC(PC mode)
H:SCALAR(Monitor mode)

FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON



PANEL_ON
1: PANEL POWER ON
0: PANEL POWER OFF

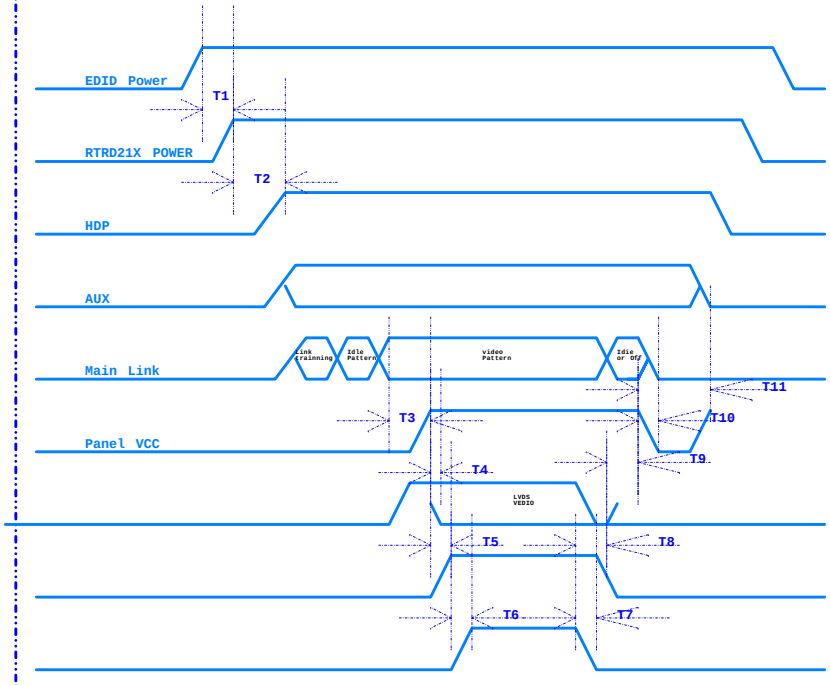


Table 7 Timing Parameters of Power on/off Sequence

Item	Description	Min.(ms)	Max.(ms)
T_1	Delay from EDID power active to DP2LVDS power active	0	--
T_2	Delay from DP2LVDS power active to HPD asserted	0	70
T_3	Falling time of Panel Vcc	0.5	10
T_4	Delay from Panel Vcc output enable to LVDS output enable	0	50
T_5	Delay from LVDS output enable to backlight output enable	200	--
T_6	Delay from PWM output enable to backlight output enable	0	--
T_7	Delay from backlight output disable to PWM out disable	0	--
T_8	Delay from backlight output disable to LVDS output disable	200	--
T_9	Delay from LVDS output disable to Panel Vcc out disable	0	50
T_{10}	Falling time of Panel Vcc	0.5	10
T_{11}	Delay between two panel power on/off sequence	500	--

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: LCD/Converter Connector

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 52 of 106

PCH CRT Header for Debug

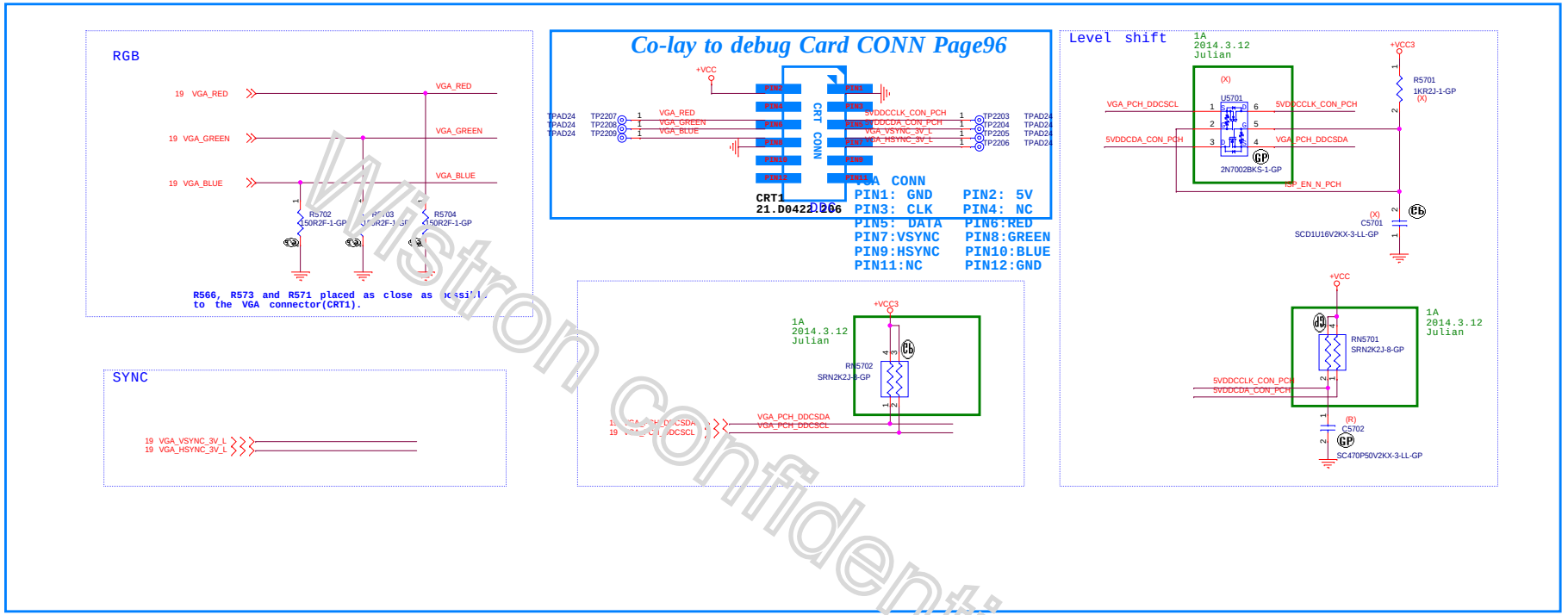


Table 0-2. Desktop Lynx Point SKUs Flexible I/O Map

SKU	High Speed I/O Ports																	
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15	Port 16	Port 17	Port 18
Q87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4 / PCIe* Port 1	SATA 6Gb/s Port 5 / PCIe* Port 2	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 6Gb/s Port 2	SATA 6Gb/s Port 3
Q85	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	PCIe* Port 1	PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 3Gb/s Port 4	SATA 3Gb/s Port 5	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 6Gb/s Port 2	SATA 6Gb/s Port 3
B85	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	PCIe* Port 1	PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 3Gb/s Port 4	SATA 3Gb/s Port 5	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 6Gb/s Port 2	SATA 6Gb/s Port 3
Z87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4 / PCIe* Port 1	SATA 6Gb/s Port 5 / PCIe* Port 2	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 6Gb/s Port 2	SATA 6Gb/s Port 3
H87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4 / PCIe* Port 1	SATA 6Gb/s Port 5 / PCIe* Port 2	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 6Gb/s Port 2	SATA 6Gb/s Port 3
H81	USB 3.0 Port 1	USB 3.0 Port 2	NA	NA	PCIe* Port 1	PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	NA	NA	SATA 3Gb/s Port 4	SATA 3Gb/s Port 5	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	NA	NA

NOTES:
1. Ports listed with NA are not available and are disabled.

Table 0-1. Desktop Lynx Point SKUs (Sheet 1 of 2)

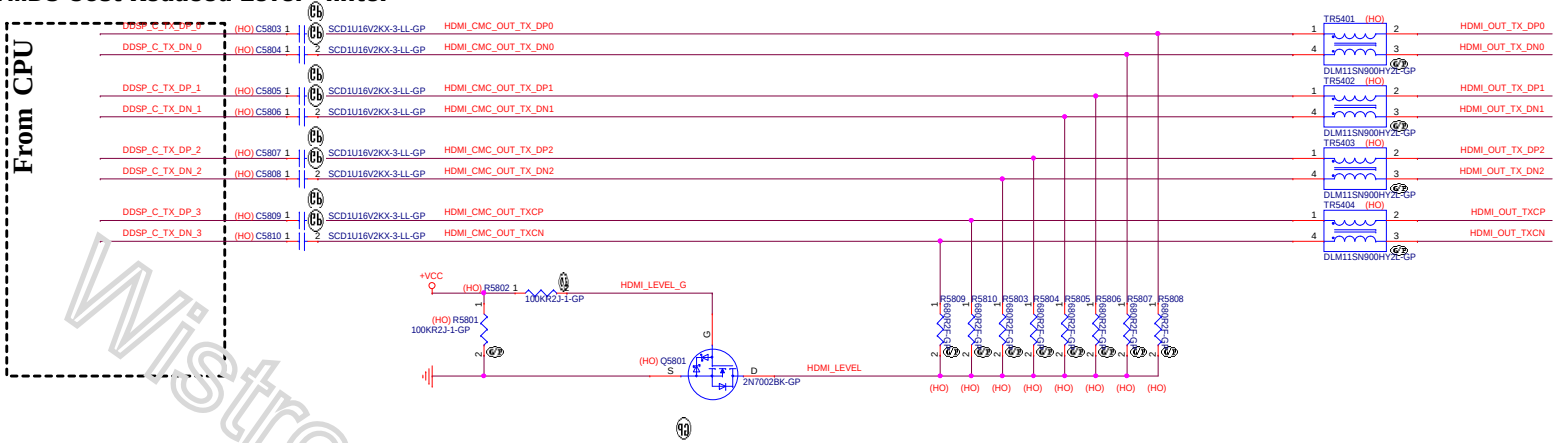
Feature Set	SKU Name					
	Intel® Q87 Express Chipset	Intel® Q85 Express Chipset	Intel® B85 Express Chipset	Intel® Z87 Express Chipset	Intel® H87 Express Chipset	Intel® H81 Express Chipset
Flexible I/O	Yes	No	No	Yes	Yes	No
PCI Express* 2.0 Ports	8[4]	8	8	8[4]	8[4]	6
Total number of USB ports	14	14	12[5]	14	14	10[6]
• USB 3.0 Capable Ports (SuperSpeed and all USB 2.0 speeds)	4(6)[7]	4	4	4(6)[7]	4(6)[7]	2[8]
• USB 2.0 Only Ports	10(8)[9]	10	8	10(8)[9]	10(8)[9]	8
Total number of SATA ports	4(6)[10]	6	6	4(6)[10]	4(6)[10]	4[11]
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)	6	4[12]	4[12]	6	6	2[13]
• SATA Ports (3 Gb/s and 1.5 Gb/s only)	0	2	2	0	0	2

<Variant Name>

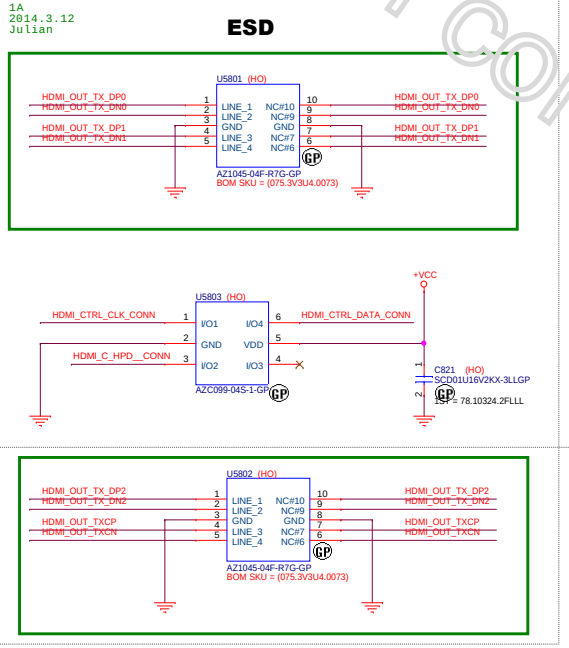
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CRT Board Connector
Size: C | Document Number: B560 with GPU | Rev: SA
Date: Tuesday, May 13, 2014 | Sheet 53 of 106

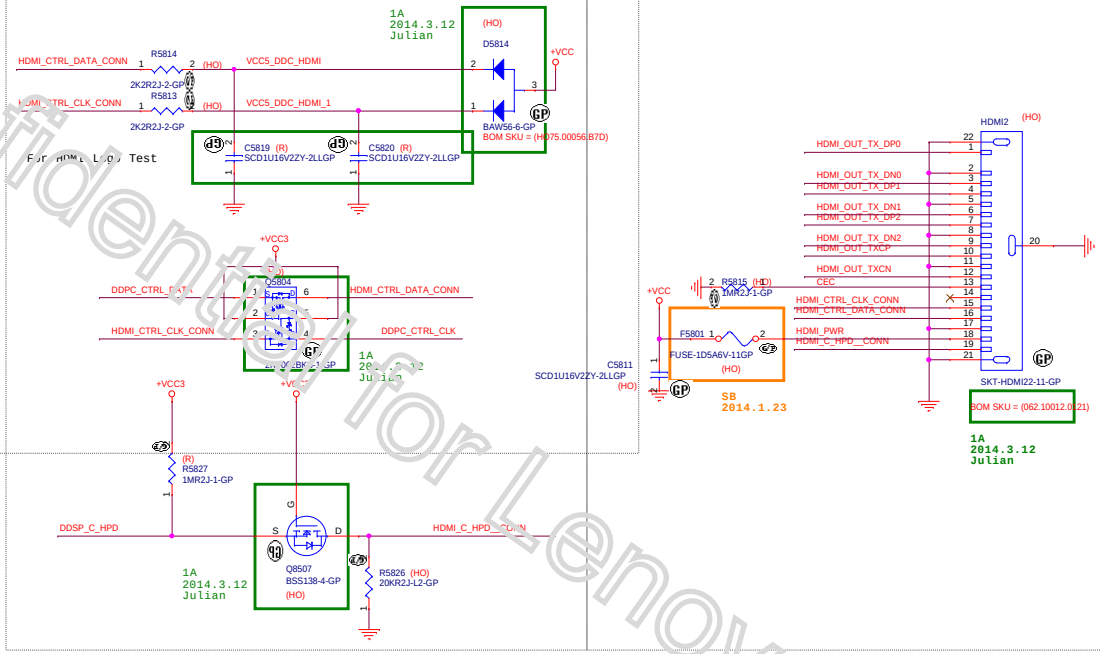
TMDS Cost Reduced Level Shifter



ESD



DDC(Display Date Channel)/HPD(Hot Plug Detect)HDMI OUT Connector



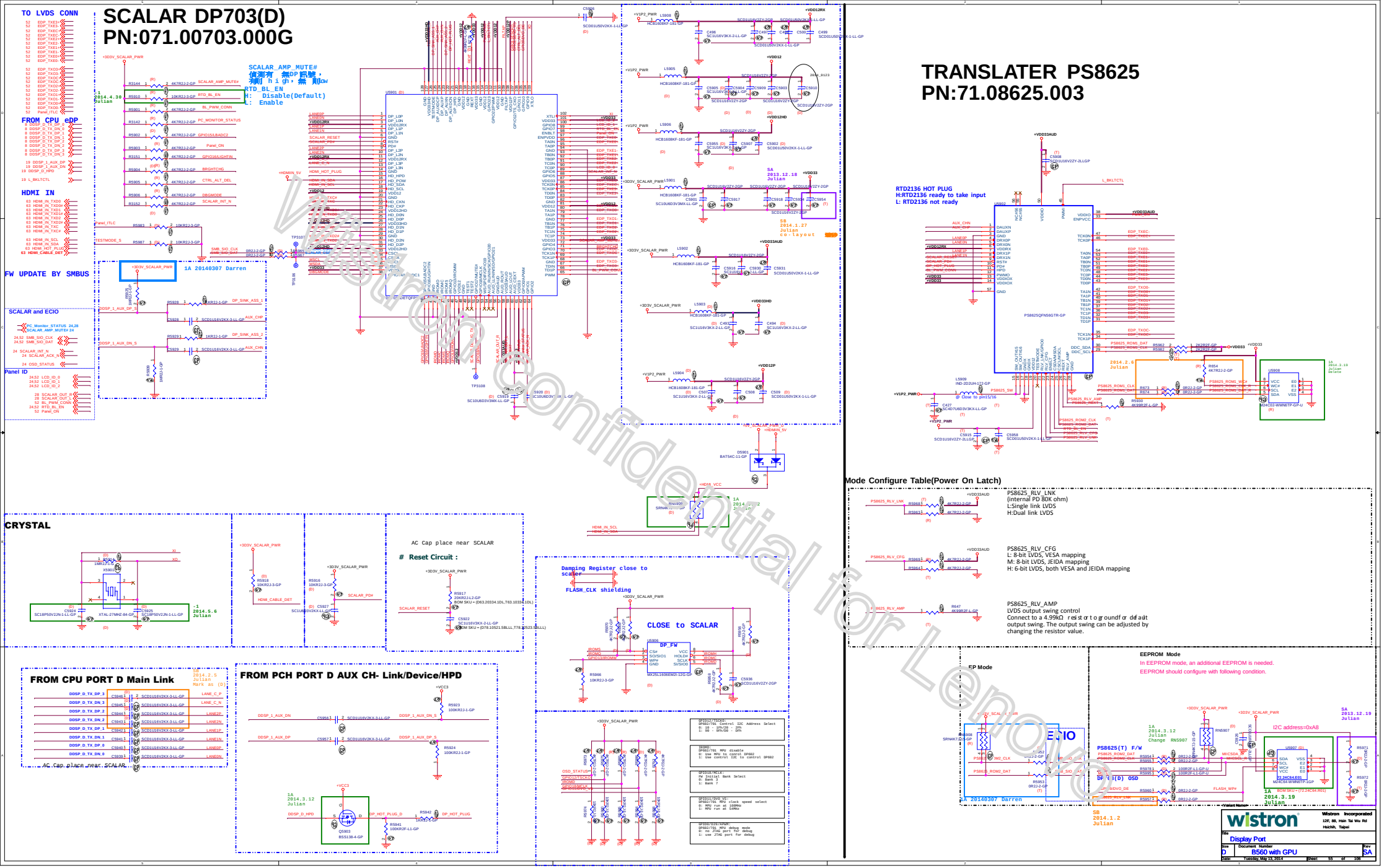
1A
2014.3.12
Julian

<Variant Name>

Wistron Incorporated	12F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	HDMI Level Shifter/Conn
Size	C
Document Number	B560 with GPU
Rev	SA
Date:	Tuesday, May 13, 2014
Sheet	54 of 106

SCALAR DP703(D)
PN:071.00703.000G

TRANSLATER PS8625
PN:71.08625.003



PCH SATA

19 SATAHDR_TX_DN1
19 SATAHDR_TX_DP1
19 SATAHDR_RX_DN1
19 SATAHDR_RX_DP1

19 SATAHDR_TX_DN0
19 SATAHDR_TX_DP0
19 SATAHDR_RX_DN0
19 SATAHDR_RX_DP0

D6610

SATAHDR_RX_R_DP1 / SATAHDR_RX_R_DN1 / SATAHDR_TX_R_DN1 / SATAHDR_TX_R_DP1

LINE_1 LINE_2 GND LINE_3 LINE_4 NC#10 NC#9 GND NC#7 NC#6

AZ1045-04F-R7G-GP
BOM SKU = (075.3V3U4.0073)

Rear CONN

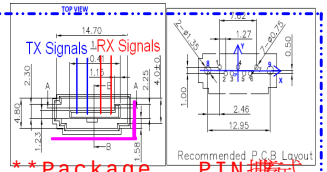
D6609

SATAHDR_RX_R_DP0 / SATAHDR_RX_R_DN0 / SATAHDR_TX_R_DN0 / SATAHDR_TX_R_DP0

LINE_1 LINE_2 GND LINE_3 LINE_4 NC#10 NC#9 GND NC#7 NC#6

AZ1045-04F-R7G-GP
BOM SKU = (075.3V3U4.0073)

Rear CONN



**Package PIN搬式有顛倒 180度現象，差分信號需要反接！！
20121207 Phoran

020.80095.0007 FOXCONN RED LOW SIDE ODD

SODD1

SATAHDR_RX_DP1 / SATAHDR_RX_DN1 / SATAHDR_TX_DP1 / SATAHDR_TX_DN1

C6001 C6003

SCD01U16V2KX-3LLGP

SKT-SATA7P-164-GP

SB
2014.1.21
Julian
Change SATA port from port1 to port4

1A
2014.3.12
Julian

HIGH SIDE HDD

SHDD1

SATAHDR_RX_DP0 / SATAHDR_RX_DN0 / SATAHDR_TX_DP0 / SATAHDR_TX_DN0

C6008 C6006 C6002 C6004

SCD01U16V2KX-3LLGP

1ST = 78.10324.2FLLL

SKT-SATA7P-76-GP
BOM SKU = (020.80065.0001)

-1
2014.3.31
Julian

SB
2014.1.20
Julian

+VCC → F6001 FUSE-1D5A6V-1SGP → +V_5HDD

C6011 SC1U16V3KX-2-LL-GP
C6014 SC10U6D3V3MX-LL-GP

+12V_S0 → F6002 FUSE-2A32V-6-GP → +12V_HDD

C6015 SC10U25V5KX-GP
C6009 SC1U16V3KX-2-LL-GP
C6017 SC10U25V5KX-GP
(R) TC6001 E100U16VM-32-GP

HD/OD Power CONN

Layout: Please put them together

SB
2014.1.23
Julian
Modify

SPWR1 → +12V_HDD, +V_5HDD

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: HDD / ODD / NGFF_SSD

Size: C | Document Number: B560 with GPU | Rev: SA

Date: Tuesday, May 13, 2014 | Sheet 56 of 106

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
(Reserve)E-SATA

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 57 of 106

Half_Mini Card Connector(Wireless LAN)

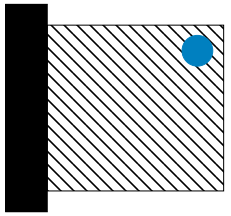
SSID = Wireless

MINI PCIE WLAN MOUNTING HOLE-PTH
STAND OFF HOLE197R102

H13
STF256R113-UH258-GP

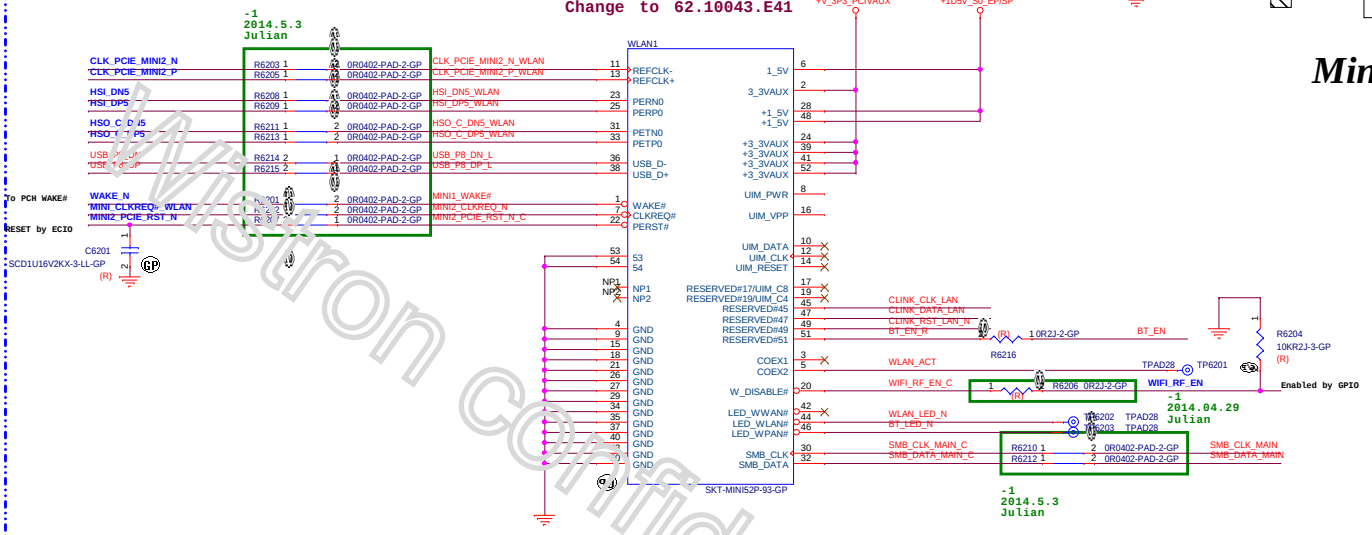
H13

Mini PCI-E Connector



1A
2013.3.12 Julian
Change to 62.10043.E41

-1
2014.5.3
Julian



-1
2014.04.29
Julian

-1
2014.5.3
Julian

PCIEX1 WLAN

16 HSO_C_DP5
16 HSO_C_DN5
16 HSI_DP5
16 HSI_DN5
18 CLK_PCIE_MINI2_P
18 CLK_PCIE_MINI2_N
24 MINI2_PCIE_RST_N

SMBUS

19 CLINK_CLK_LAN
19 CLINK_DATA_LAN
12,13,17,60,87 SMB_DATA_MAIN
12,13,17,60,87 SMB_CLK_MAIN

USB2.0

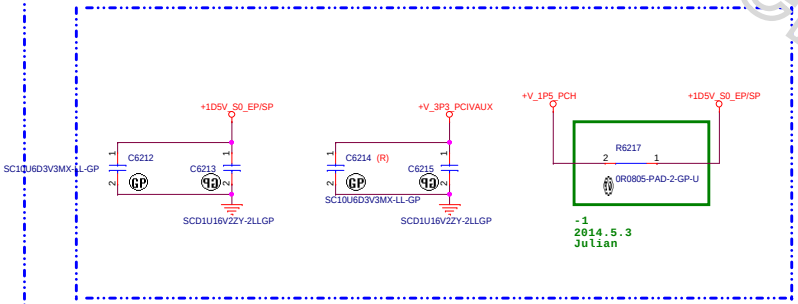
16 USB_P8_DP
16 USB_P8_DN

OTHERS

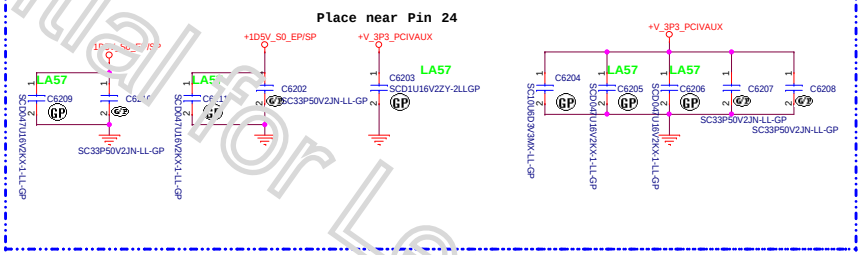
17 BT_EN

MSATA

16,17,24,30,60 WAKE_N
17 MINI_CLKREQ#_WLAN
19 WIFI_RF_EN
19 CLINK_RST_LAN_N



-1
2014.5.3
Julian



Half_Mini PCI-E CARD

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: WLAN CONN
Size: C
Document Number: B560 with GPU
Rev: SA
Date: Tuesday, May 13, 2014
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<Variant Name>

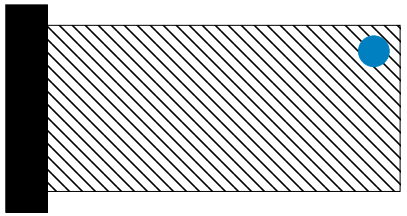
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
WWAN CONN

Size	Document Number	Rev
C	B560 with GPU	SA

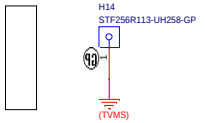
Date: Tuesday, May 13, 2014 Sheet 59 of 106

Full_Mini PCI-E CARD



MINI PCIE MSATA MOUNTING HOLE-PTH

H14



Full TV and Mini Card Connector(mSATA SSD co-lay)

(DO:TV)==For all Project Reserve

16,17,24,30,58 WAKE_N

16 HSO_C_DN2
16 HSO_C_DP2
16 HSI_DN2
16 HSI_DP2

18 CK_PCIE_3_TV_DN
18 CK_PCIE_3_TV_DP

19 SATAHDR_RX_DN3
19 SATAHDR_RX_DP3
19 SATAHDR_TX_DN3
19 SATAHDR_TX_DP3

17 MINI_CLKREQ#_TV

+1D5V_S0_EP/SP

1A
2013.3.12 Julian
Change to 62.10043.E41

+VCC3

TVCAR1

SKT-MINI52P-93-GP
(TVMS)

R6407 0R3J-0-U-GP +MINI_PWR
R6403 (R) 0R2J-2-GP +MINI_PWR1

12,13,17,58,87 SMB_CLK_MAIN
12,13,17,58,87 SMB_DATA_MAIN
R6408 0R2J-2-GP MINI_SMB_CLK
R6409 0R2J-2-GP MINI_SMB_DATA

CK_PCIE_3_TV_DN
CK_PCIE_3_TV_DP
TVI_DN_SATAHDR_RX_R_DP3
TVI_DP_SATAHDR_RX_R_DN3
TVO_DN_SATAHDR_TX_R_DN3
TVO_DP_SATAHDR_TX_R_DP3
USB_P11_R_DN
USB_P11_R_DP

R6405 (R) 0R2J-2-GP WAKE_N
TV1_WAKE#
TV_CLKQ_C
TV_PCIE_RST
MINI_CLKREQ#_TV
5/30 by Leo

USB_P11_DN 16
USB_P11_DP 16
MINIPCIE_RST# 24

C6418 SC47P50V2JN-3-LL-GP (R)

SATA and TV SWAP RX:P=N

TVI_DN_SATAHDR_RX_R_DP3 R6412 0R2J-2-GP HSI_DN2
TVI_DP_SATAHDR_RX_R_DN3 R6413 0R2J-2-GP HSI_DP2
TVO_DN_SATAHDR_TX_R_DN3 R6414 0R2J-2-GP HSO_C_DN2
TVO_DP_SATAHDR_TX_R_DP3 R6415 0R2J-2-GP HSO_C_DP2

TVI_DN_SATAHDR_RX_R_DP3 C6401 SATAHDR_RX_DP3
TVI_DP_SATAHDR_RX_R_DN3 C6402 SATAHDR_RX_DN3
TVO_DN_SATAHDR_TX_R_DN3 C6403 SATAHDR_TX_DN3
TVO_DP_SATAHDR_TX_R_DP3 C6404 SATAHDR_TX_DP3
SCD01U16V2KX-3LLGP
(MS) 1ST = 78.10324.2FLLL

SB
2014.1.21
Julian
mSATA change SATA port from port3 to port1
It need support SATA GEN3

+V_1P5_PCH -1 2014.5.1 Julian +1D5V_S0_EP/SP
R6406 0R0805-PAD-2-GP-U (TVMS)

+VCC3
C6405 SCD1U16V2ZY-2LLGP (TVMS)
C6406 SC4D7U6D3V3KX-LL-GP (TVMS)
C6407 SCD1U16V2ZY-2LLGP (TVMS)
C6408 SC10U6D3V3MX-LL-GP (TVMS)

+VCC3
C6409 (R) SC10U6D3V3MX-LL-GP (TVMS)
C6411 SCD1U16V2

+1D5V_S0_EP/SP
C6412 SCD1U16V2ZY-2LLGP (TVMS)

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: mSATA CONN
Size: C
Document Number: B560 with GPU
Rev: SA
Date: Tuesday, May 13, 2014
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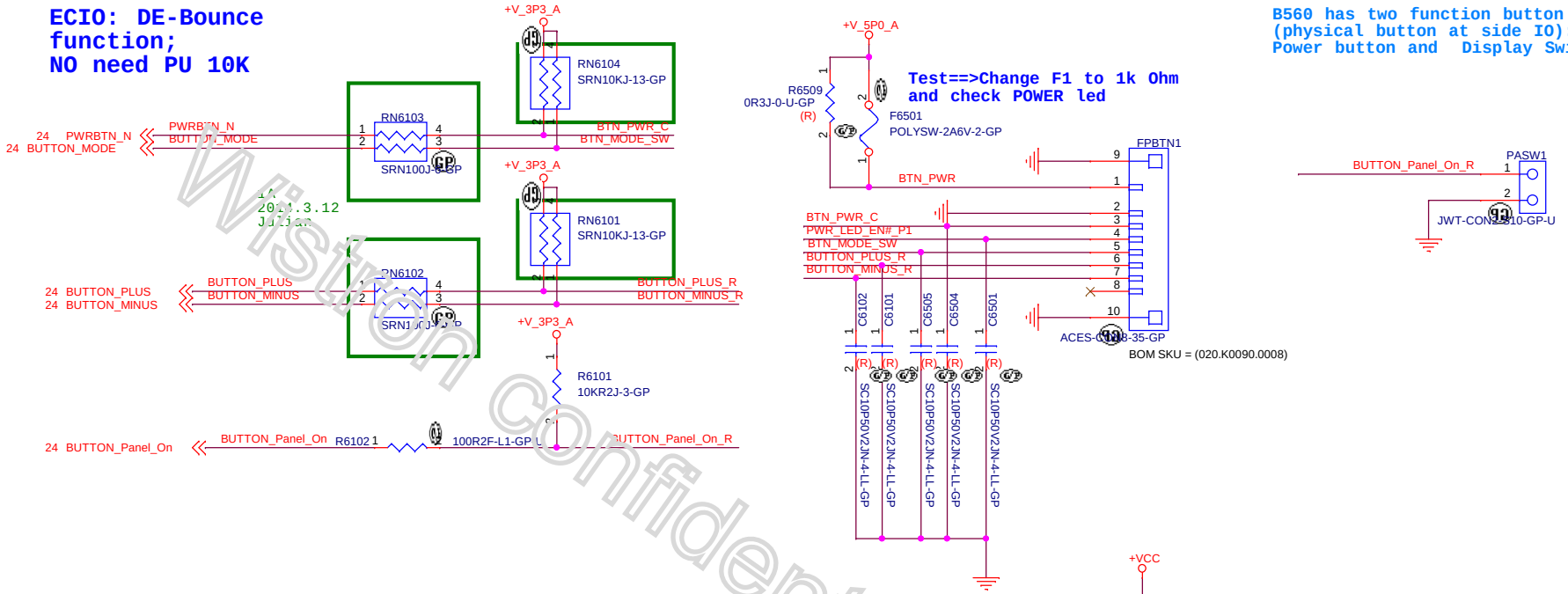
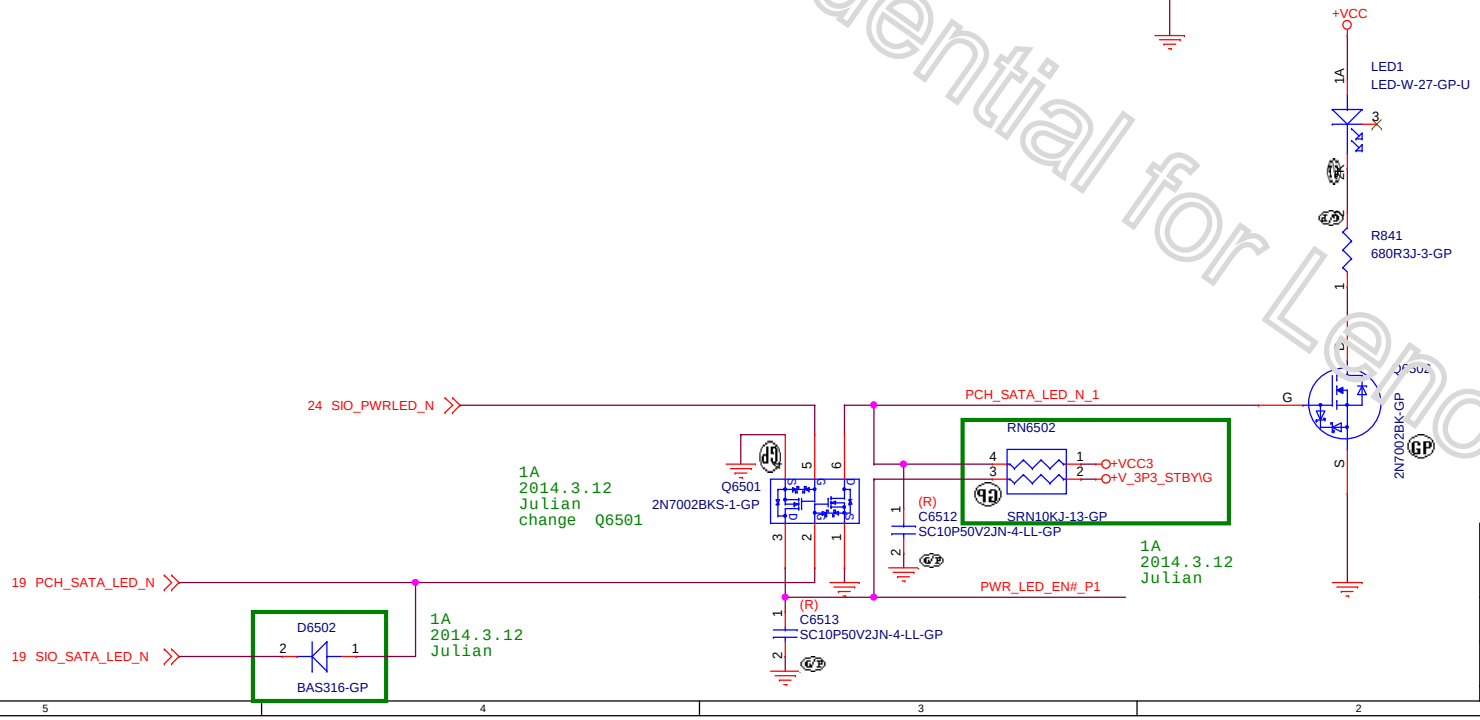
FUNCTION BOARD

ECIO: DE-Bounce function;
NO need PU 10K

B560 has two function button (physical button at side IO):
Power button and Display Switch (HDMI).





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wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: LED Bard/Power Button

Size	Document Number	Rev
Custom	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 61 of 106

<Variant Name>

Wistron Incorporated
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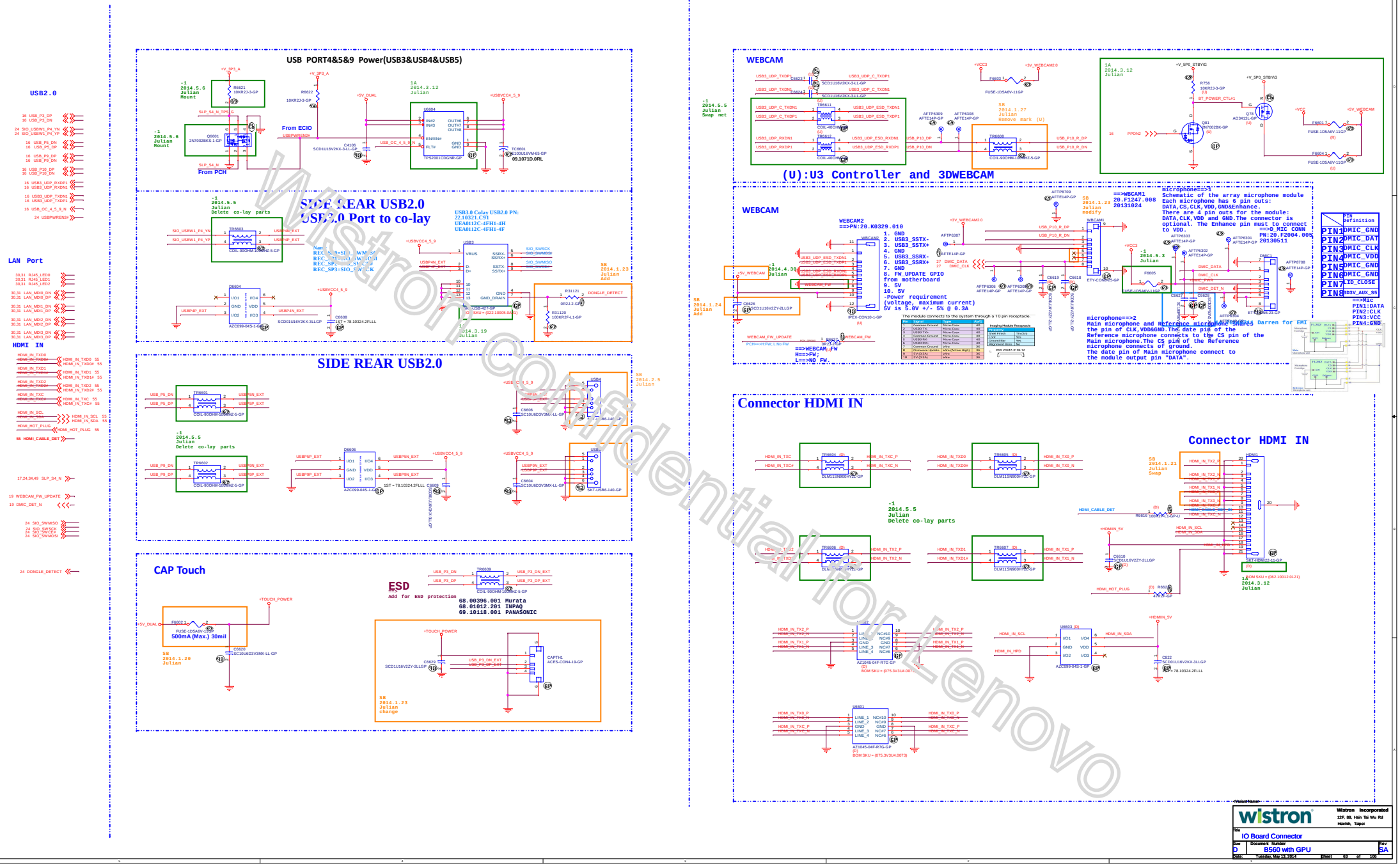
Hsichih, Taipei

Title
Touch Pad

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 62 of 106


USB2.0
LAN Port
HDMI IN
USB PORT4&5&9 Power(USB3&USB4&USB5)
SIDE REAR USB2.0
USB2.0 Port to co-lay
SIDE REAR USB2.0
CAP Touch
ESD
WEBCAM
(U):U3 Controller and 3DWEBCAM
Connector HDMI IN
Connector HDMI IN
Wistron Confidential for Lenovo
Wistron Incorporated
IO Board Connector
B560 with GPU

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
(Reserved)Hall Sensor

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 64 of 106

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Debug connector

Size	Document Number	Rev
C	B560 with GPU	SA

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<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
(Reserved)

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 66 of 106

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
(Res)G Sensor

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 67 of 106

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Thunderbolt (1/5)

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 68 of 106

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Thunderbolt (2/5)

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 69 of 106

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Thunderbolt (3/5)

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 70 of 106

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Thunderbolt (4/5)

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 71 of 106

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Thunderbolt (5/5)

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 72 of 106

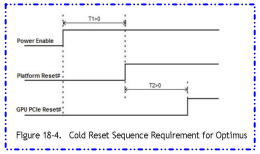


Figure 18-4. Cold Reset Sequence Requirement for Optimus

PCI_E x8

3 EXP_A_TX_C_DP[7..0]
3 EXP_A_TX_C_DN[7..0]
3 EXP_A_RX_DP[7..0]
3 EXP_A_RX_DN[7..0]

18 CLK_PCIE_PEG_N
18 CLK_PCIE_PEG_P
4,16,24,30 PLTRST_N

GPU Heat Sink Stand Off

For gpu thermal module: 87.96282.435 qty:4
change to 34.3NK02.001==>20130717

Note:N15S-GT PEX4~PEX7 as NC
N15V-GM PEX4~PEX7 need nect;
Note:N15S-GT PEX4~PEX7 as NC
N15V-GM PEX4~PEX7 need nect;

3.3V +/- 5%
120mA
(See NV DG)

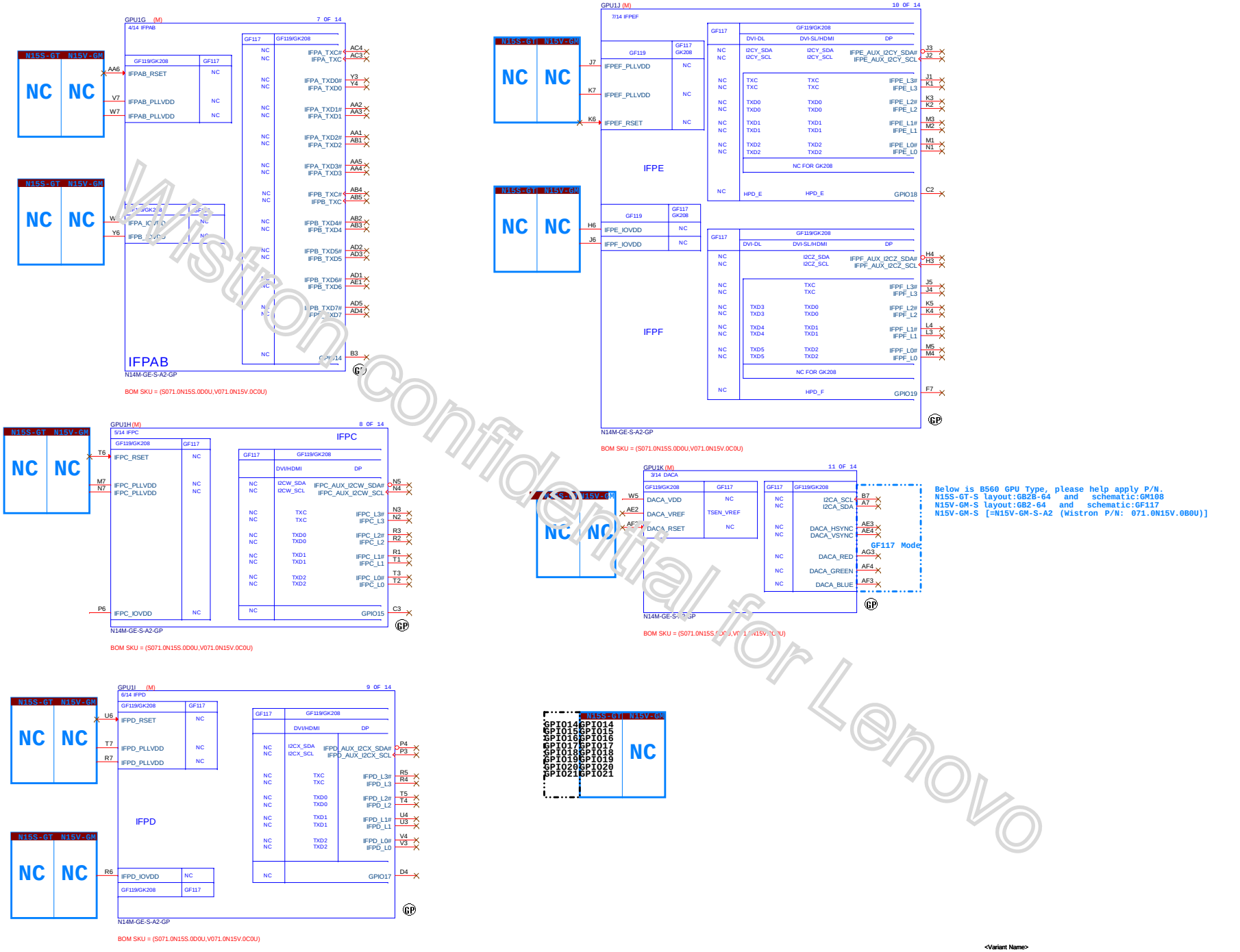
3V3 Power Islands
The 3.3V Power rail must be split into 3V3_MAIN and 3v3_AON Power rails.
While the 3V3_MAIN rail would be powered off during
GC6, 3V3_AON, or the "alway-on" rail, would stay
powered on during GC6 2.0 residency.
3V3_AON maintains minimum power necessary for GPU to conduct
GC6 2.0 Entry and exist sequence autonomously.

1.05V +/- 3%
120mA
(See NV DG)

PLACE NEAR GPU

B560: nVIDIA N15S-GT-AIO colay N15V-GM-AIO, DDR3 1G&2G
071.0N15S.0D0U:IC VGA N15S-GT-S-A2 GB2-64 FCBGA595 Size:23*23
071.0N15V.0C0U:IC VGA N15V-GM-S-A2 GB2-64 FCBGA 595P Size:23*23

Wistron	Wistron Incorporated		
	12F, 88, Hsin Tai Wu Rd		
	Hsichih, Taipei		
Title	GPU_PEG (1/5) _new		
Size	Document Number		Rev
D	B560 with GPU		SA
Date:	Tuesday, May 13, 2014	Sheet 73 of 105	



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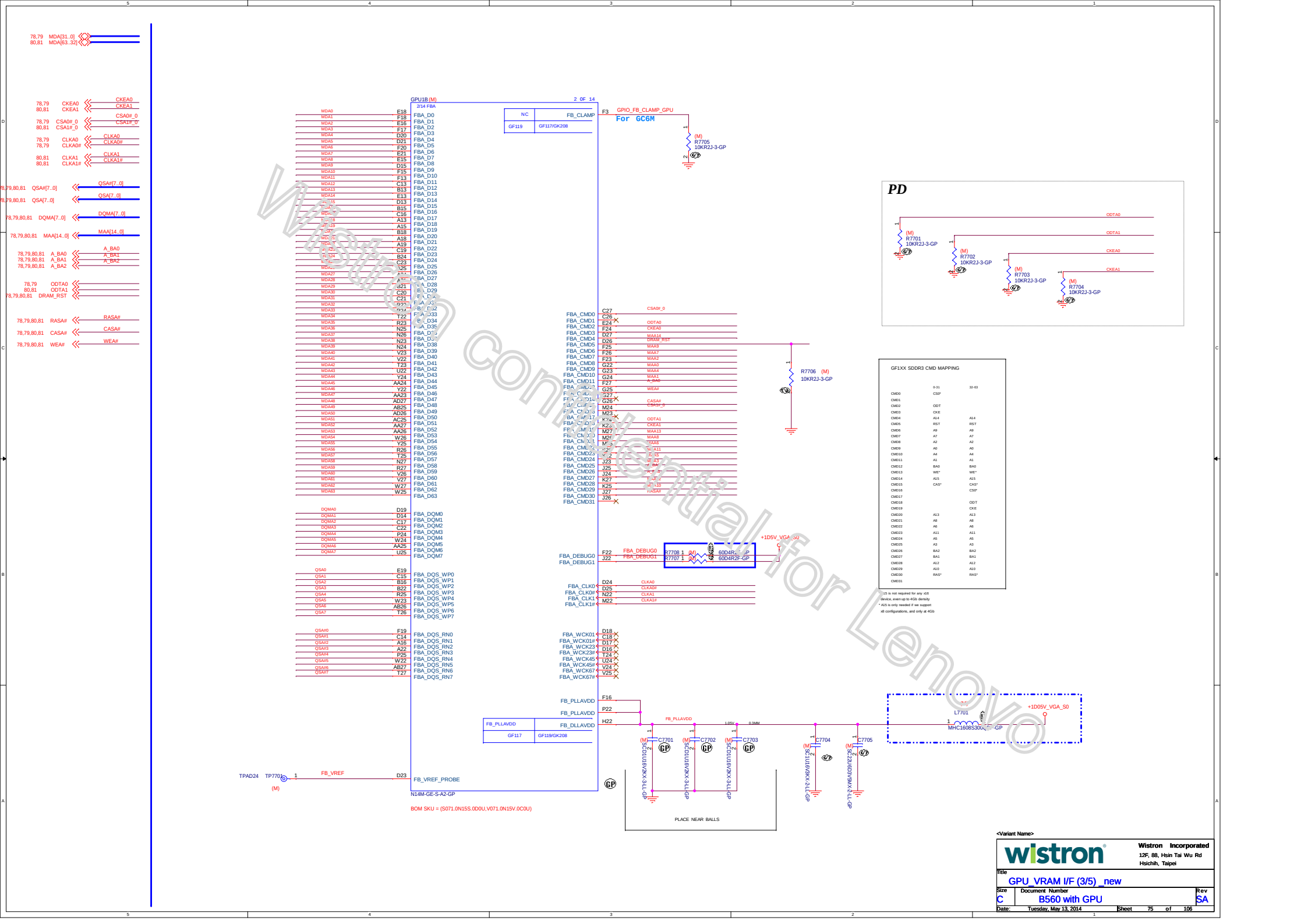
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: GPU_DIGITALOUT (2/5) _new

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 74 of 106



Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: GPU_VRAM I/F (3/5) _new

Size	Document Number	Rev
C	B560 with GPU	SA

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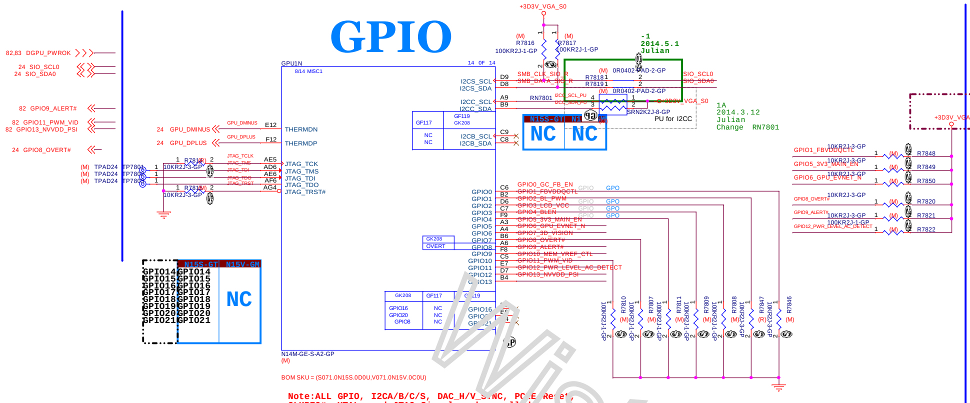
GPIO



Note:ALL GPIO, I2CA/B/C/S, DAC_H/V_SYNC, PCIE_Reset, CLKREQ#, XTAL, and JTAG Signals, and should be connected to 3V3_AON rail, also PEX_PLL_HVDD and PEX_3V3_SVDD must be source ... 3V3_AON.

GPIO	GF117
GPIO 0	FAN_PWM/FB_CLAMP/DEBUG Service
GPIO 1	MEM_VDD_CTL
GPIO 2	UNUSED
GPIO 3	UNUSED
GPIO 4	UNUSED
GPIO 5	Reserved
GPIO 6	FB_CLAMP_TGL_REQ
GPIO 7	3DVision(UNUSED)
GPIO 8	GPU Overtemp
GPIO 9	GPU Thermal Alert
GPIO 10	FB Vref Control
GPIO 11	NVVDD PWM_VID
GPIO 12	PWR_Level AC Detect
GPIO 13	UNUSED(No Need to Set in VBIOS)
GPIO 14	N/A on Package
GPIO 15	N/A on Package
GPIO 16	N/A on Package
GPIO 17	N/A on Package
GPIO 18	N/A on Package
GPIO 19	N/A on Package
GPIO 20	N/A on Package
GPIO 21	N/A on Package

Table 12-1. GB2B-64 and GB4B-128 GPIO Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor for GC6 1.0	
	GC6_FB_EN	O	FB Enable for GC6 2.0	10K pull-down to GND
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID: pull-up to 3V3_AON or pull-down to GND to set boot FBVDD/Q voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100k pull-down
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO5	3V3_MAIN_EN	O	GPU power sequencing	10K pull-up to 3V3_AON
GPIO6	FB_CLAMP_TGL_REQ	O	Clamp toggle request for GC6 1.0	10K pull-up to system 3.3V
	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10K pull-up to 3V3_AON
GPIO7	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO8	SYS_PEX_RST_MON#	I	System side PCIe reset Monitor	
GPIO9	ALERT	I/O	Active Low Thermal Alert	10K pull-up to 3V3_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 3V3_AON
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase.

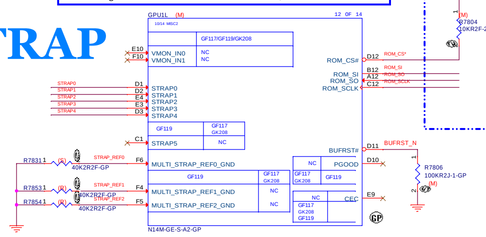
GPIO	GK208	GM108	GF117
GPIO 0	FBCLAMP_MONITOR	GC6_FB_EN	FAN_PWM/DEBUG Service
GPIO 1	MEM_VDD_CTL	MEM_VDD_CTL	MEM_VDD_CTL
GPIO 2	UNUSED	UNUSED	UNUSED
GPIO 3	UNUSED	UNUSED	UNUSED
GPIO 4	UNUSED	UNUSED	UNUSED
GPIO 5	GPIO_DEBUG_SRVC	GC6_PWR_EN	UNUSED
GPIO 6	Remote Sensor Error Correction	GPU_EVENT*	UNUSED
GPIO 7	UNUSED	GPIO_DEBUG_SRVC	UNUSED
GPIO 8	GPU Overtemp	SYS_PEX_RST_MON*	GPU Overtemp
GPIO 9	GPU Thermal Alert	GPU Thermal Alert	GPU Thermal Alert
GPIO 10	UNUSED	UNUSED	UNUSED
GPIO 11	NVVDD PWM_VID	NVVDD PWM_VID	NVVDD PWM_VID
GPIO 12	PWR_Level AC Detect	PWR_Level AC Detect	PWR_Level AC Detect
GPIO 13	NVVDD PSI	NVVDD PSI	NVVDD PSI
GPIO 14	UNUSED	UNUSED	N/A on Package
GPIO 15	UNUSED	UNUSED	N/A on Package
GPIO 16	FAN_PWM	FAN_PWM	N/A on Package
GPIO 17	UNUSED	UNUSED	N/A on Package
GPIO 18	UNUSED	UNUSED	N/A on Package
GPIO 19	UNUSED	UNUSED	N/A on Package
GPIO 20	UNUSED	GC5_MODE	N/A on Package
GPIO 21	UNUSED	GPU_PEX_RST_HOLD*	N/A on Package

GPIO0, GPIO6 is for GC6 feature, no need to connect since this project won' t support GC6
GPIO1 is for FB voltage control, no need to connect since the FBVDDQ is 1.5V for all P-States.
GPIO12 : High->AC Mode,Low->Battery Mode enter slow down functionpull for power saving.Recommand:Pull-High for AC mode.
GPIO13 PSI :Change Phase from two to one, and thean enter slow down functionpull for power saving.

BUILD BOM

U42 PN:71.0N15P.M01
N15P-Q1-A2-GP
IC VGA N15P-Q1-A2 GB4-128(QS)
1.Hynix -----PN:072.05224.000U -R5445: UNMOUNT -R5432 64.10026.6DL
2.Samsung PN:072.20325.000U -R5445: 64.49915.6DL; -R5432 UNMOUNT
3.Hynix -----PN:072.05424.000U -R5445: UNMOUNT -R5432 64.15026.6DL
4.Samsung PN:072.44132.000U -R5445: 64.20026.6DL; -R5432 UNMOUNT

STRAP



External BIOS ROM

Table 119. Device Specific Strap Mode Selection

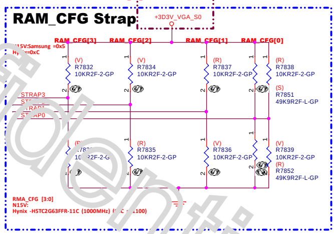
	N14M-GE/-GL	Other N14x GPUs
Multi_Strap_Ref2_GND (Only on GB2-64 package)	No Connect	N/A
Multi_Strap_Ref1_GND (Only on GB2-64 package)	No Connect	N/A
Multi_Strap_Ref0_GND	No Connect	40.2k 1% to GND
Strap Mode Selected	Binary	Multi-Level

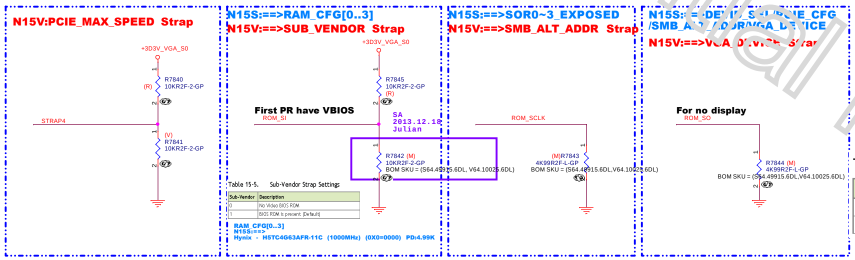
SUB_VENDOR Strap--ROM_SI_D3
SMB_ALT_ADDR Strap--ROM_SLK_D4
VGA_DEVICE Strap--ROM_SO_C4

Refer PDF:DG-06803-003-Secured

N15S:==>STARP[0..4]:Resered
STARP0:==USER[0..3] Keep PU and PD footprints and stuff 50kohm PU.
N15V:==>
STARP0==RAM_CFG[0]
STARP1==RAM_CFG[1]
STARP2==RAM_CFG[2]
STARP3==RAM_CFG[3]
STARP4==RAM_CFG[4]

RAM_CFG Strap





VRAM Reference:RVL-06891-001-V01

Multi-Level Straps

Table 10. Multi-level Strap Differences

Physical Strapping Pin	GPU	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	N15S-GT	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	ALL GN2B-64N14 and GN2B-64N15	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	N15S-GT	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STARP0	N15S-GT	Resered(Keep pull-up and pull-down footprints and stuff 50kohm pull-up)			
STARP1	N15S-GT	Resered(Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STARP2	N15S-GT	Resered(Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STARP3	N15S-GT	Resered(Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STARP4	N15S-GT	Resered(Keep pull-up and pull-down footprints and leave them no stuffed by default)			

Notes:
DEVID_SEL:This strap selects the pre-programmed Device IDs inside of the GB2B-64 N15x GPUs, replacing the PCI_DEVID Straps.
PCIE_CFG:This strap selects the pre-programmed PCIe settings inside of the GB2B-64 N15x GPUs, replacing the 3GIO-PADCFG Straps.

Binary Straps

Table 9. N15V-GM Binary Strap Mode Mapping

Strap Pin Name	strap mapping	Resistance	Polarty
ROM_SCLK	SMB_ALT_ADDR	10Kohm	Pull-down to GND
ROM_SI	SUB_VENDOR	10Kohm	Pull-up to 3V3 if Vbios ROM Exists; pull-dowm to GND IF No VBIOS ROM
ROM_SO	VGA_DEVICE	10Kohm	Pull-down to GND(no display)
STARP0	RAM_CFG[0]	10Kohm	See note below
STARP1	RAM_CFG[1]	10Kohm	See note below
STARP2	RAM_CFG[2]	10Kohm	See note below
STARP3	RAM_CFG[3]	10Kohm	See note below
STARP4	RAM_CFG[4]	10Kohm	Pull-down to GND

Notes:
Rrfer to the latest version of the N15V-GM Memory recommended Vendors List for the specific setting for each memory type and configuration.Pull-up to 3V3 for binary '1' and pull-down to GND for binary '0'.

Table1/7:N15S-GT/N15V-GM DDR3 Recommendec memories 128Mx16 Configuration

Configuration	Vender	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CLK(MHz)	Memory data code Minimum	Status	PN
N15S-GT 128Mx16	Samsung	0x8	1.5V/ 1.5V	K4W2G1646E-BC1A	1000	N/A	Preliminary	72.42164.N0U
	Micron	0x7	1.5V/ 1.5V	MT41J128M16JT-093G:K	1000	1322	Preliminary	72.52G63.N0U
	Hynix	0x6	1.5V/ 1.5V	H5TC2G63FFR-11C	1000	N/A	Preliminary	
N15V_GM 128Mx16	Micron	0x1	1.5V/ 1.5V	MT41J128M16JT-093G:K	1000	1234	Production ready	
	Samsung	0x5	1.5V/ 1.5V	K4W2G1646E-BC1A	1000	1204	Production ready	72.42164.N0U
	Hynix	0xC	1.5V/ 1.5V	H5TC2G63FFR-11C	1000	N/A	Production ready	72.52G63.N0U

Table 13. N15S-GT/GM DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
128M×16 DDR3	Hynix	0x6	1.5V/ 1.5V	H5TC2G63FFR-11C	1000	N/A	Preliminary
	Micron	0x7	1.5V/ 1.5V	MT41J128M16JT-093G:K	1000	1322	Preliminary
	Samsung	0x8	1.5V/ 1.5V	K4W2G1646Q-BC1A	1000	N/A	Preliminary

Table 1. N15V-GM DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
128M×16 DDR3	Micron	0x1	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production ready
	Samsung	0x5	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production ready
	Hynix	0xC	1.5 V/ 1.5 V	H5TC2G63FFR-11C	1000	N/A	Production ready

SMB_ALT_ADDR Strap: this strap is used to configure the I2CS address of a GPU on the I2CS Slave address.

Table 15-6. I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E (Default)
1	0x9[illegible] (Multi-GPU usage)

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
[illegible].1 kΩ	1101	0101
[illegible].8 kΩ	1110	0110
[illegible]5.3 kΩ	1111	0111

15.5.14 DEVID_SEL Strap

This strap selects the pre-programmed Device IDs inside the NVIDIA GPU, replacing the PCI_DEVID straps. This strap only exists in the GB2B-64 and GB4B-128 package GPUs. Set this strap to 0 by default. Please refer to the latest GPU specific *Platform Update Notification* for the latest configuration.

15.5.15 PCIE_CFG Strap

This strap selects the pre-programmed PCIe settings inside the NVIDIA GPU, replacing 3GIO_PADCFG. This strap only exists in the GB2B-64 and GB4B-128 package GPUs. Set this strap to 0 by default. Please refer to the latest GPU specific *Platform Update Notification* for the latest configuration.

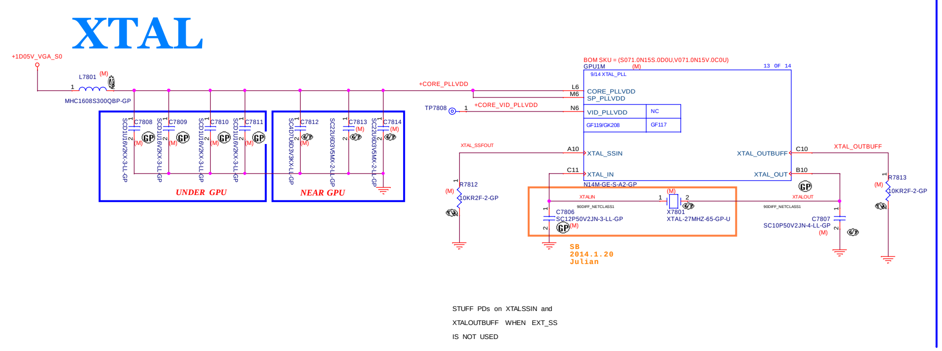
15.5.5 VGA_DEVICE Strap

The VGA_DEVICE strap is used to identify the device type (or class code) of the GPU within the PCI configuration space. Set 3D Acceleration Device for GPU in Optimus configuration or secondary GPU in SLI configuration.

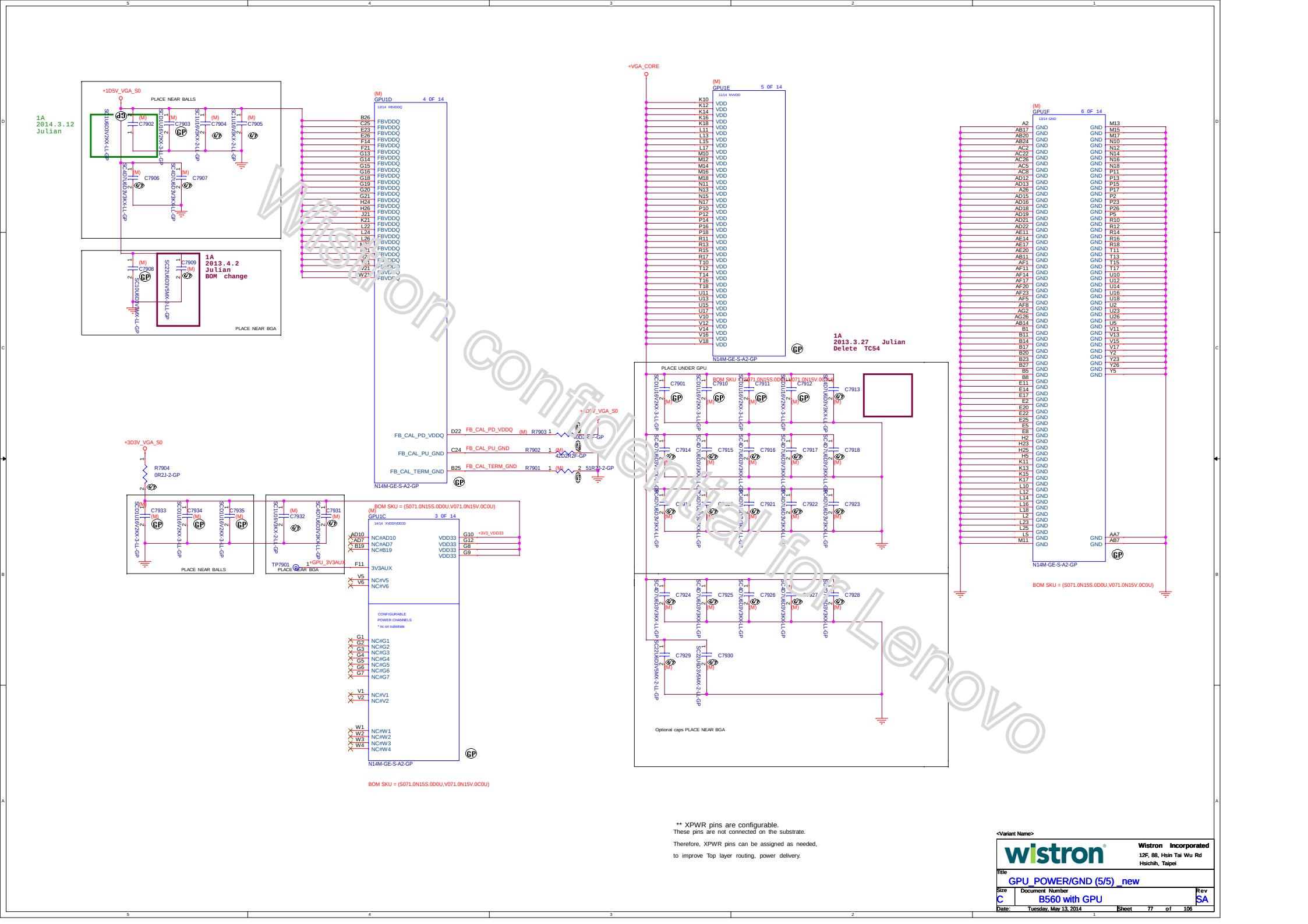
Table 15-7. VGA_DEVICE Settings

VGA_DEVICE	Description
0	Non-Primary 3D Acceleration Device (Class Code 302h)
1	Primary Display or VGA Device (Class Code 300h)

XTAL



THERMAL PROTECTION



CHANNEL A:Normal Type

VRAM Reference:RVL-06891-001-V01

Hynix:128Mx16 ==>72.52G63.N0U
IC VRAM H5TC2G63FFR-11C
FBG96P 1.5V 1GHZ
Samsung:128Mx16==>72.42164.N0U
IC VRAM K4W2G1646E-BC1A FBGA96P 128M*16

Table 12. N15V-GM DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Micron	0x1	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production ready
	Samsung	0x5	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production ready
	Hynix	0xC	1.5 V/ 1.5 V	H5TC2G63FFR-11C	000	N/A	Production ready

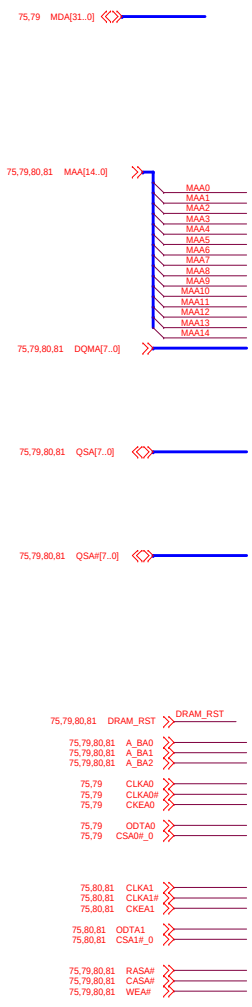
Table 13. N15S-GT/GM DDR3 Recommended Memories 128Mx16 Configuration

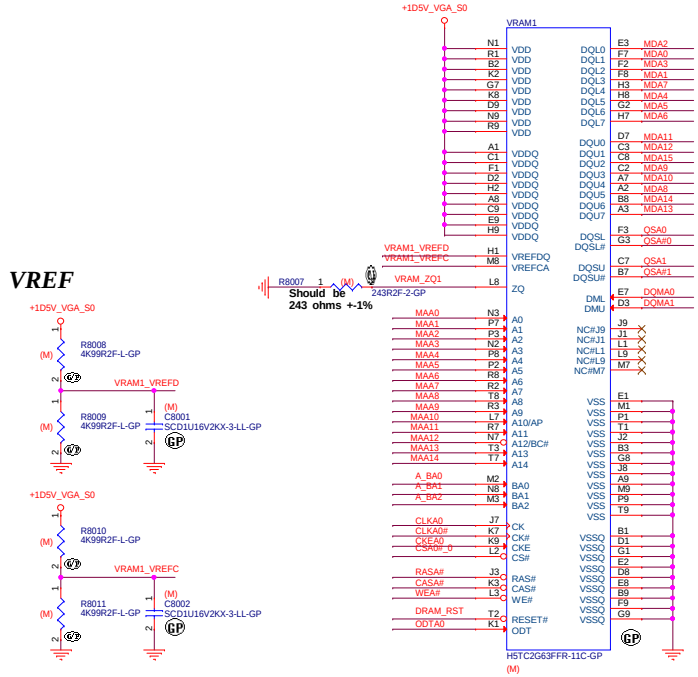
Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Hynix	0x6	1.5V/ 1.5V	H5TC2G63FFR-11C	1000	N/A	Preliminary
	Micron	0x7	1.5V/ 1.5V	MT41J128M16JT-093G:K	1000	1322	Preliminary
	Samsung	0x8	1.5V/ 1.5V	K4W2G1646Q-BC1A	1000	N/A	Preliminary

Package Ballout/Mechanical Dimension Pin Define — Please create symbol by function.

x16 Package Ball out (Top view): 96ball FBGA Package

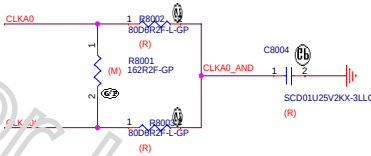
	1	2	3	4	5	6	7	8	9	
A	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	A
B	VSSQ	VDD	VSS				DQSU	DQU6	VSSQ	B
C	VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ	C
D	VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD	D
E	VSS	VSSQ	DQL0				DML	VSSQ	VDDQ	E
F	VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ	F
G	VSSQ	DQL6	DQSL				VDD	VSS	VSSQ	G
H	VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ	H
J	NC	VSS	RAS				CK	VSS	NC	J
K	ODT	VDD	CAS				CK	VDD	CKE	K
L	NC	CS	WE				A10/AP	ZQ	NC	L
M	VSS	BA0	BA2				NC	VREFCA	VSS	M
N	VDD	A3	A0				A12/BC	BA1	VDD	N
P	VSS	A5	A2				A1	A4	VSS	P
R	VDD	A7	A9				A11	A6	VDD	R
T	VSS	RESET	A13				A14	A8	VSS	T
	1	2	3	4	5	6	7	8	9	



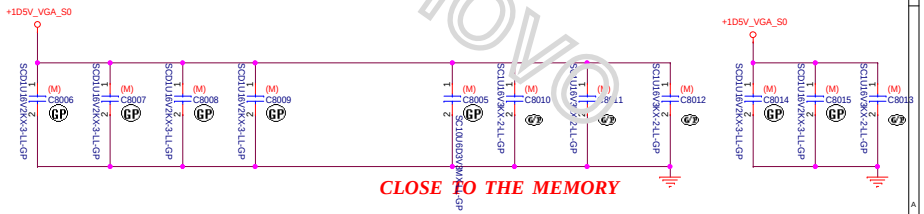


VREF

FBCLK Termination place on VRAM side



DG requires 5x0.1uF and 2x1.0uF and 1x10uF per VRAM chip



CLOSE TO THE MEMORY

<Variant Name>

wistron Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: VRAM 1,2 (1/4) _new
Size: C | Document Number: B560 with GPU | Rev: SA
Date: Tuesday, May 13, 2014 | Sheet 78 of 106

CHANNEL A:Mirrored Type

75,78 MDA[31..0]

75,78,80,81 MAA[14..0]
MAA0 MAA1 MAA2 MAA3 MAA4 MAA5 MAA6 MAA7 MAA8 MAA9 MAA10 MAA11 MAA12 MAA13 MAA14

75,78,80,81 DQMA[7..0]

75,78,80,81 QSA[7..0]

75,78,80,81 QSA#[7..0]

75,78,80,81 DRAM_RST — DRAM_RST

75,78,80,81 A_BA0
75,78,80,81 A_BA1
75,78,80,81 A_BA2

75,78 CLKA0
75,78 CLKA0#
75,78 CKEA0

75,78 ODTA0
75,78 CSA0#_0

75,80,81 CLKA1
75,80,81 CLKA1#
75,80,81 CKEA1

75,80,81 ODTA1
75,80,81 CSA1#_0

75,78,80,81 RASA#
75,78,80,81 CASA#
75,78,80,81 WEA#

VRAM Reference:RVL-06891-001-V01

Hynix:128Mx16 ==>72.52G63.N0U

IC VRAM H5TC2G63FFR-11C

FBG96P 1.5V 1GHZ

Samsung:128Mx16==>72.42164.N0U

IC VRAM K4W2G1646E-BC1A FBGA96P 128M*16

Table 1. N15V-GM DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Micron	0x1	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production ready
	Samsung	0x5	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production ready
	Hynix	0xC	1.5 V/ 1.5 V	H5TC2G63FFR-11C	1000	N/A	Production ready

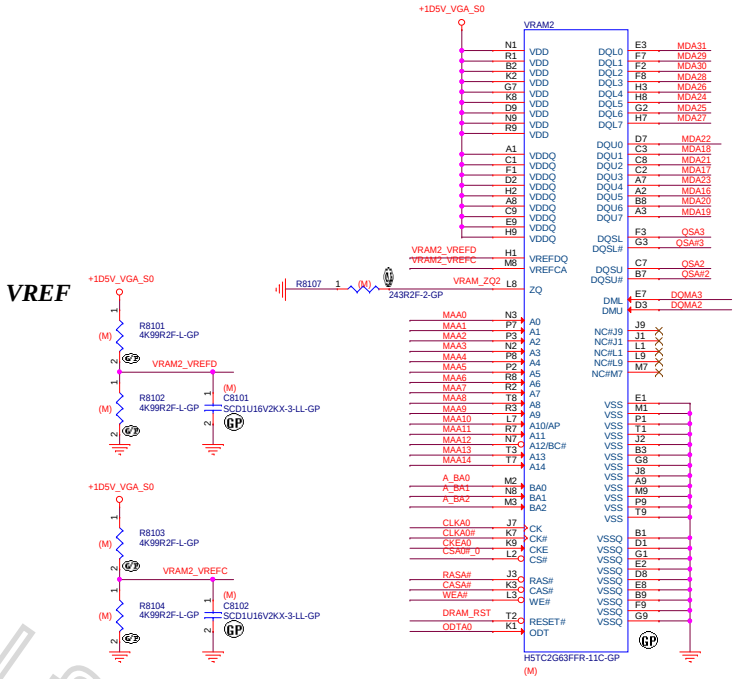
Table 13. N15S-GT/GM DDR3 Recommended Memories 128Mx16 Configuration

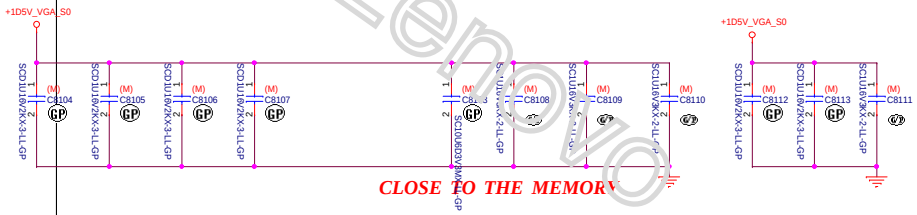
Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Hynix	0x6	1.5V/ 1.5V	H5TC2G63FFR-11C	1000	N/A	Preliminary
	Micron	0x7	1.5V/ 1.5V	MT41J128M16JT-093G:K	1000	1322	Preliminary
	Samsung	0x8	1.5V/ 1.5V	K4W2G1646Q-BC1A	1000	N/A	Preliminary

Package Ballout/Mechanical Dimension Pin Define — Please create symbol by function.

x16 Package Ball out (Top view): 96ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	A
B	VSSQ	VDD	VSS				DQSU	DQU6	VSSQ	B
C	VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ	C
D	VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD	D
E	VSS	VSSQ	DQL0				DML	VSSQ	VDDQ	E
F	VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ	F
G	VSSQ	DQL6	DQSL				VDD	VSS	VSSQ	G
H	VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ	H
J	NC	VSS	RAS				CK	VSS	NC	J
K	ODT	VDD	CAS				CK	VDD	CKE	K
L	NC	CS	WE				A10/AP	ZQ	NC	L
M	VSS	BA0	BA2				NC	VREFCA	VSS	M
N	VDD	A3	A0				A12/BC	BA1	VDD	N
P	VSS	A5	A2				A1	A4	VSS	P
R	VDD	A7	A9				A11	A6	VDD	R
T	VSS	RESET	A13				A14	A8	VSS	T





<Variant Name>

wistron Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: VRAM 3,4 (2/4) _new
Size: C | Document Number: B560 with GPU | Rev: SA
Date: Tuesday, May 13, 2014 | Sheet 79 of 106

CHANNEL A:Normal Type

VRAM Reference:RVL-06891-001-V01

Hynix:128Mx16 ==>72.52G63.N0U
IC VRAM H5TC2G63FFR-11C
FBG96P 1.5V 1GHZ
Samsung:128Mx16==>72.42164.N0U
IC VRAM K4W2G1646E-BC1A FBGA96P 128M*16

Table 1. N15V-GM DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Micron	0x1	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production ready
	Samsung	0x5	1.5 V/ 1.5 V	K4W2G1646Q-BC1A	1000	1204	Production ready
	Hynix	0xC	1.5 V/ 1.5 V	H5TC2G63FFR-11C	1000	N/A	Production ready

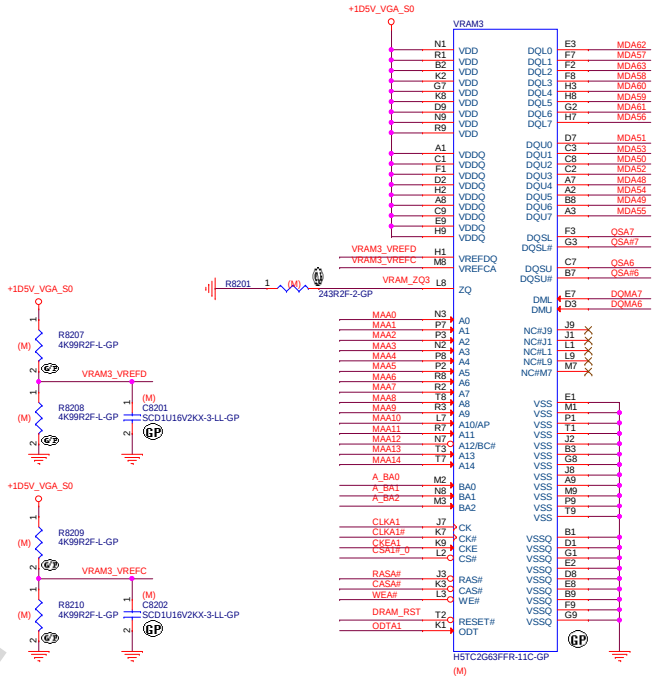
Table 13. N15S-GT/GM DDR3 Recommended Memories 128Mx16 Configuration

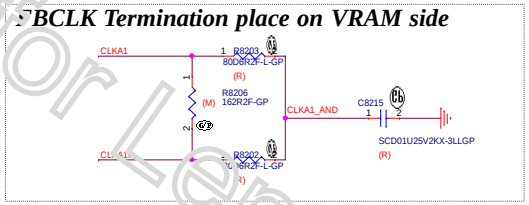
Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Hynix	0x6	1.5V/ 1.5V	H5TC2G63FFR-11C	1000	N/A	Preliminary
	Micron	0x7	1.5V/ 1.5V	MT41J128M16JT-093G:K	1000	1322	Preliminary
	Samsung	0x8	1.5V/ 1.5V	K4W2G1646Q-BC1A	1000	N/A	Preliminary

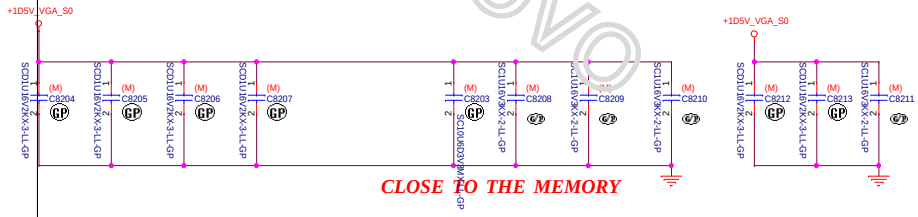
Package Ballout/Mechanical Dimension Pin Define — Please create symbol by function.

x16 Package Ball out (Top view): 96ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	A
B	VSSQ	VDD	VSS				DQSU	DQU6	VSSQ	B
C	VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ	C
D	VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD	D
E	VSS	VSSQ	DQL0				DML	VSSQ	VDDQ	E
F	VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ	F
G	VSSQ	DQL6	DQSL				VDD	VSS	VSSQ	G
H	VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ	H
J	NC	VSS	RAS				CK	VSS	NC	J
K	ODT	VDD	CAS				CK	VDD	CKE	K
L	NC	CS	WE				A10/AP	ZQ	NC	L
M	VSS	BA0	BA2				NC	VREFCA	VSS	M
N	VDD	A3	A0				A12/BC	BA1	VDD	N
P	VSS	A5	A2				A1	A4	VSS	P
R	VDD	A7	A9				A11	A6	VDD	R
T	VSS	RESET	A13				A14	A8	VSS	T







CLOSE TO THE MEMORY

CHANNEL A:Mirrored Type

VRAM Reference:RVL-06891-001-V01

Hynix:128Mx16 ==>72.52G63.N0U
IC VRAM H5TC2G63FFR-11C
FBG96P 1.5V 1GHZ
Samsung:128Mx16==>72.42164.N0U
IC VRAM K4W2G1646E-BC1A FBGA96P 128M*16

Table 12. N15V-GM DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Micron	0x1	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production ready
	Samsung	0x5	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production ready
	Hynix	0xC	1.5 V/ 1.5 V	H5TC2G63FFR-11C	1000	N/A	Production ready

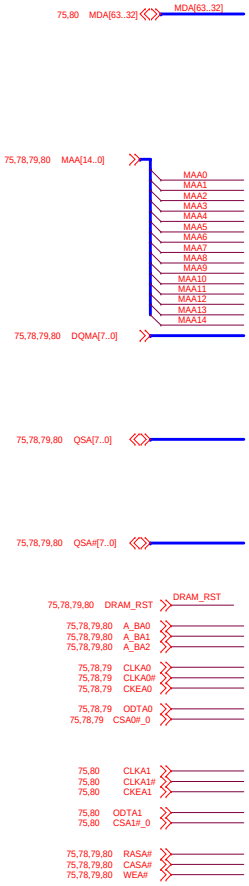
Table 13. N15S-GT/GM DDR3 Recommended Memories 128Mx16 Configuration

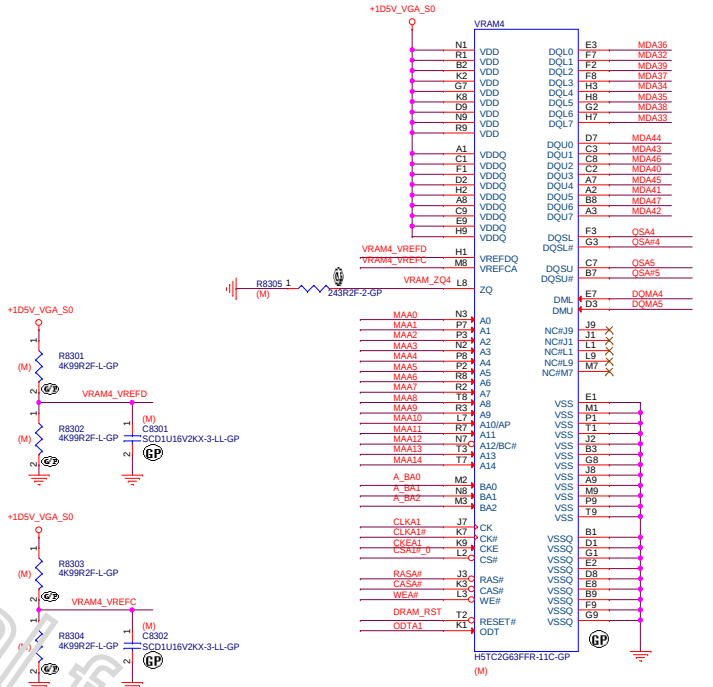
Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Hynix	0x6	1.5V/ 1.5V	H5TC2G63FFR-11C	1000	N/A	Preliminary
	Micron	0x7	1.5V/ 1.5V	MT41J128M16JT-093G:K	1000	1322	Preliminary
	Samsung	0x8	1.5V/ 1.5V	K4W2G1646Q-BC1A	1000	N/A	Preliminary

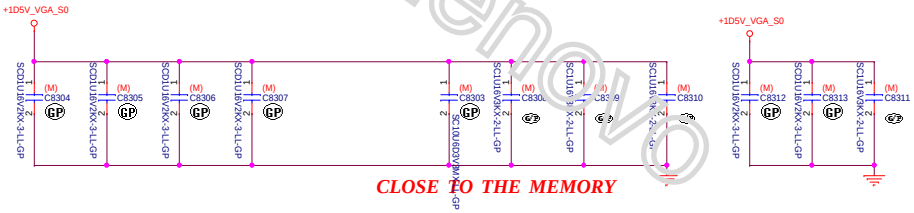
Package Ballout/Mechanical Dimension Pin Define — Please create symbol by function.

x16 Package Ball out (Top view): 96ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	A
B	VSSQ	VDD	VSS				DQSU	DQU6	VSSQ	B
C	VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ	C
D	VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD	D
E	VSS	VSSQ	DQL0				DML	VSSQ	VDDQ	E
F	VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ	F
G	VSSQ	DQL6	DQSL				VDD	VSS	VSSQ	G
H	VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ	H
J	NC	VSS	RAS				CK	VSS	NC	J
K	ODT	VDD	CAS				CK	VDD	CKE	K
L	NC	CS	WE				A10/AP	ZQ	NC	L
M	VSS	BA0	BA2				NC	VREFCA	VSS	M
N	VDD	A3	A0				A12/BC	BA1	VDD	N
P	VSS	A5	A2				A1	A4	VSS	P
R	VDD	A7	A9				A11	A6	VDD	R
T	VSS	RESET	A13				A14	A8	VSS	T
	1	2	3	4	5	6	7	8	9	







CLOSE TO THE MEMORY

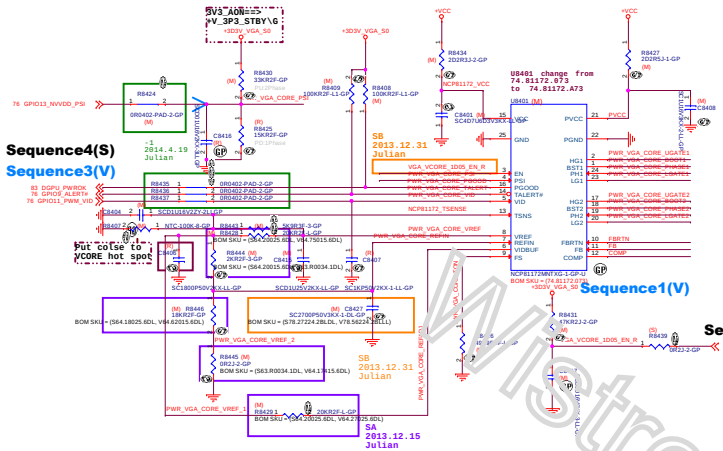
<Variant Name>

wistron — Wistron Incorporated, 12F, 88, Hsin Tai Wu Rd, Hsichih, Taipei

Title: VRAM 7,8 (4/4) _new

Size: C | Document Number: B560 with GPU | Rev: SA

Date: Tuesday, May 13, 2014 | Sheet 81 of 106



PWM-VID Specification					
		Config A	Config B	Config C	Config D
Vmin	V	0.6	0.6	0.65	0.9
Vmax	V	1.2	1.2	1.15	1.15
Vboot	V	0.875	0.9	0.9	1.028
Voltage Step Vstep	mV	6.25	6.25	25	12.5
Number of Voltage Levels N	level	96	96	20	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676	0.676
PWM Minimum Pulse Width T_{DMIN}	ns	9.26	9.26	74	74
VID Transient Time T	us	<100	<100	<100	<100
Component Value					
R1 (1%)	KΩ	39	20	39	27
R2 (1%)	KΩ	39	20	30	7.5
R3 (1%)	KΩ	1.5	2	3	0
R4 (1%)	KΩ	30	18	24	6.2
R5 (1%)	KΩ	1.5	0	3	1.74
C	nF	1.5	2.7	1.8	5.6

Please use different power config setting for N15S-GT and N15V-GM, use config B for N15S-GT, use config D for N15V-GM-S

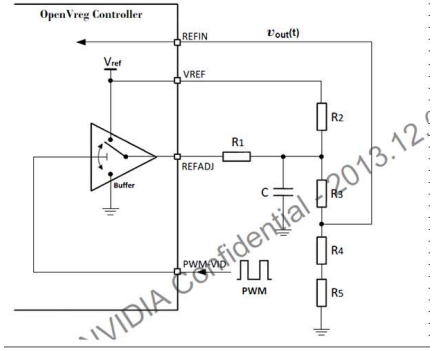
PSI==>SNASE Shedding
10K Pull up to 3V3_AON
to enable two phase.
PSI==>Power Saving interface
Power Save Command
Note:Power Saving Interface.
Logic high enables 2 phase CCM operation,
mid level enables 1-phase CCM operation,
and logic low enables 1-phase CCM/DCM operation.

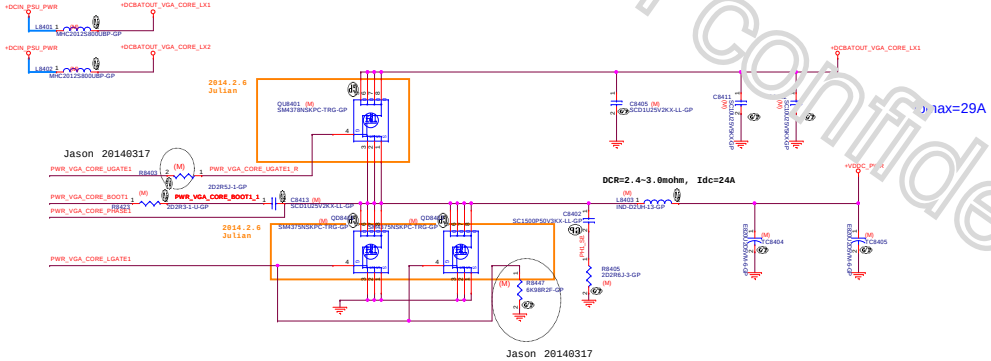
The NCP81172 has 3 power operation modes responding to PSI levels as shown in Table 1. The operation mode can be changed on the fly. In 1-phase operation, no switching in phase 2.

Table 1. Power Saving Interface (PSI) Configurations

PSI Level	Power Mode	Phase Configuration
High (PSI ≥ 2.4V)	PS0	2-Phase, DCM
Intermediate (0.9V < PSI < 2.4V)	PS1	1-Phase, FCCM
Low (PSI ≤ 0.9V)	PS2	1-Phase, Auto CCM/DCM

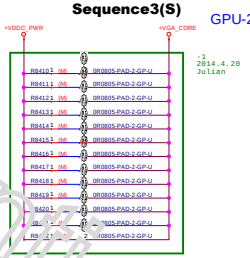
The NCP81172 is also able to support pure single-phase applications without a need to stuff components for phase 2. In this configuration, the four pins including BST2, HG2, LG2, and PHS can be float, but make sure the voltage at PSI pin is never in high level.



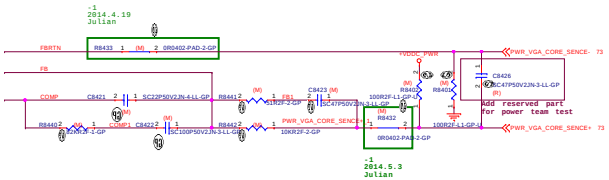


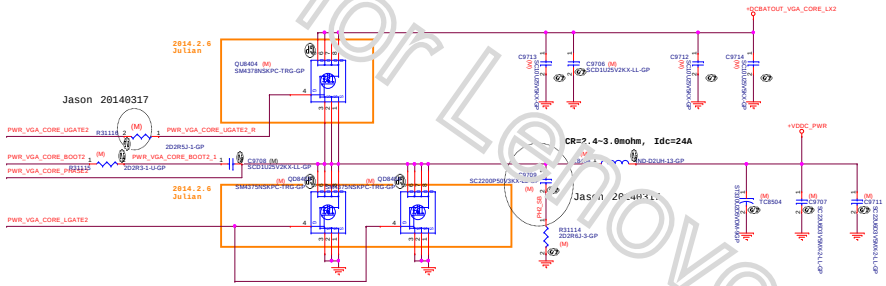
Sequence2(V)
Sequence3(S)

GPU-25Watt in B5030 GPU



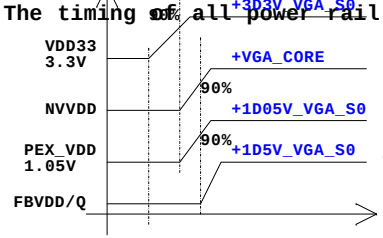
Vout=0.9V or 1.15V
Vin=12V
Switch Freq=300KHz
OCP>52.2A
Vin_rms=5A
MLCC ripple current=10uF 5pcs
choke size=7*7 0.2uH*2pcs
Choke Isat=41A
Choke Idc=24A
Choke DCR=2.4~3 mohm
LIR=0.645(Vout=0.9V)
Vin Cap=10uF*5 pcs
Cout Cap=820u*2pcs+330u*1pcs
Cout cap_esr=7m ohm & 9m ohm
OVP=Over Voltage Protection (OVP) Threshold(Voltage from FB to GND)=2V



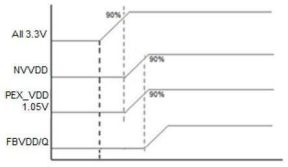


Power Sequencing Requiremen

Power-on:N15S-GT(S)
3D3V_VGA_S0-->NVVDD&1D05V_VGA_S0-->1D5V_VGA_S0
Power-on:N15V-GM(V)
3D3V_VGA_S0--->NVVDD-->1D5V_VGA_S0-->1D05V_VGA_S0
Power-off:
The timing of all power rail need power down to 0V under 10ms.



Note:the entire entry and exit sequence must complete within 200ms.



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Figure 3-6. Example of Power-up Sequencing Order

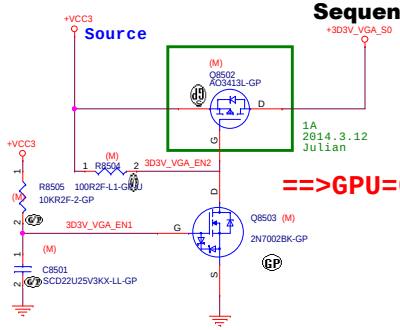
Note:
- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- A VDD33 must ramp up to 90% before NVVDD and PEXVDD in sequence can start ramping up. NVVDD must ramp up to 90% before FBVDD/Q in sequence can start ramping up
- No signal should be applied to the GPU before the power rails are fully ramped
- Refer to the JEDEC Memory Specification for memory related power sequencing.

NOTE*:-VDD33 includes all rails that use 3.3V
-PEX_VDD includes all rails that are shared

3V3 Power Islands
The 3.3V Power rail must be split into 3V3_MAIN and 3v3_AON Power rails.
While the 3V3_MAIN rail would be powered off during
GC6, 3V3_AON, or the "alway-on" rail, would stay
powered on during GC6 2.0 residency.
3V3_AON maintains minimum power necessary for GPU to conduct
GC6 2.0 Entry and exist sequence autonomously.

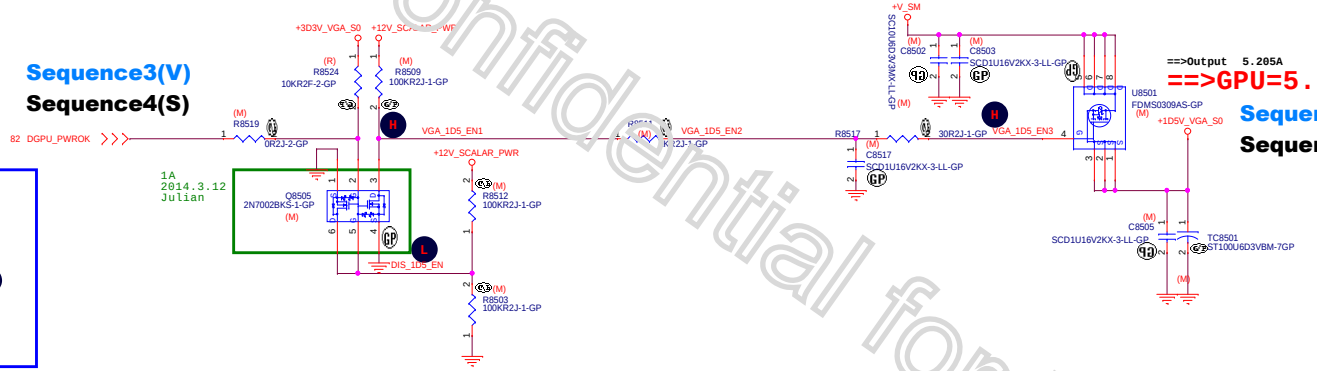
+3VS to 3.3V_DELAY Transfer
3V3_MAIN==>+3D3V_VGA_S0

Sequence1(V)
Sequence1(S)



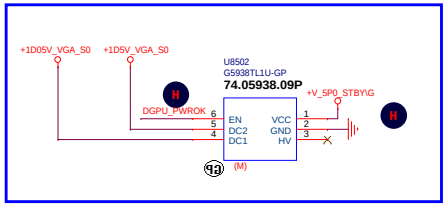
==>GPU=0.3A

Sequence3(V)
Sequence4(S)



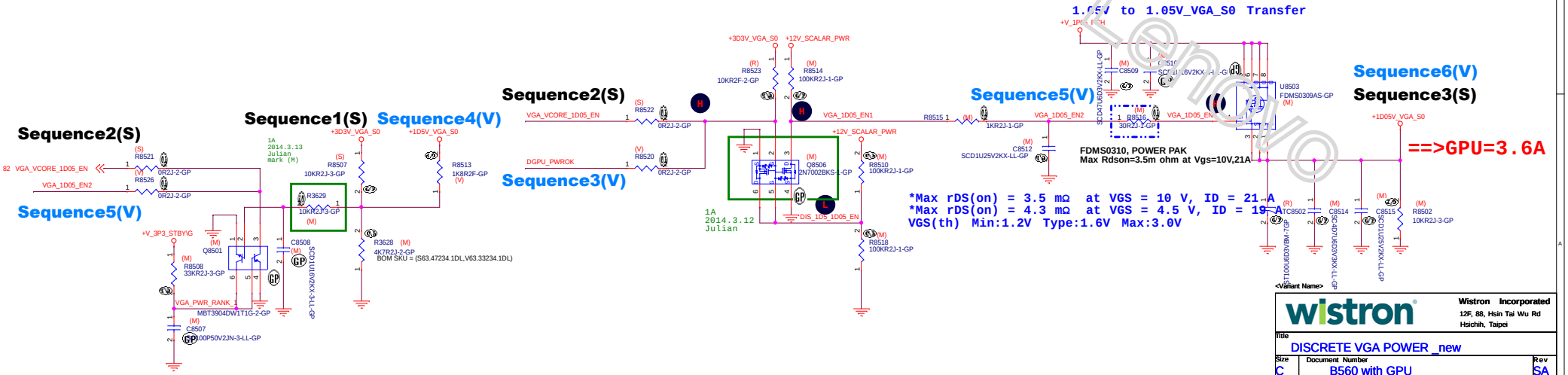
==>Output 5.205A
==>GPU=5.205A

Sequence4(V)
Sequence5(S)



1.05V to 1.05V_VGA_S0 Transfer

Sequence2(S)
Sequence1(S) Sequence4(V)
Sequence5(V)
Sequence2(S)
Sequence3(V)
Sequence5(V)
Sequence6(V)
Sequence3(S)



==>GPU=3.6A

<Variant Name>

wistron
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DISCRETE VGA POWER _new
Size: C | Document Number: B560 with GPU | Rev: SA
Date: Tuesday, May 13, 2014 | Sheet 83 of 106

<Variant Name>

Wistron Incorporated
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Hsichih, Taipei

Title
RES Switchable GFX LCD(1/2)

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 84 of 106

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
RES Switchable GFX CRT(2/2)

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 85 of 106

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
(Res) UNUSED PARTS/EMI Cap

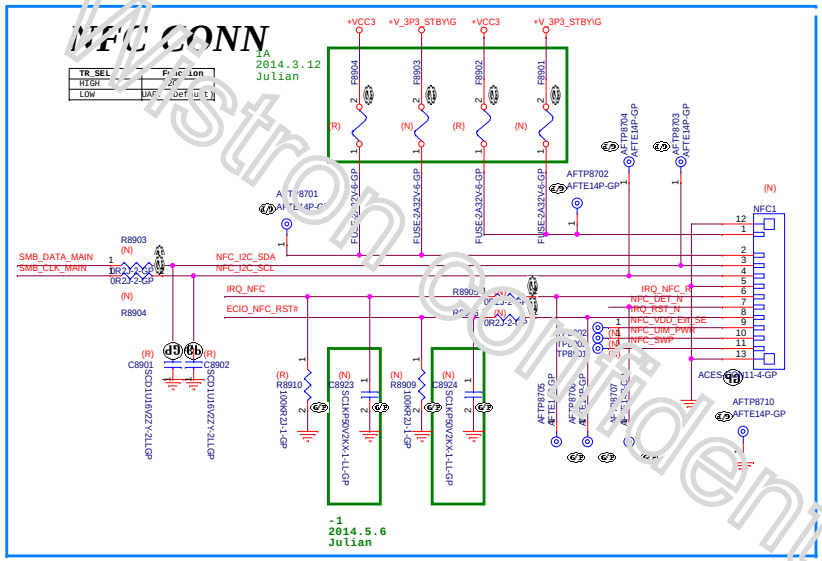
Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 86 of 106

12,13,17,58,60 SMB_CLK_MAIN
12,13,17,58,60 SMB_DATA_MAIN

17 ECIO_NFC_RST#
17 IRQ_NFC
17 NFC_DET_N

1A 2014.0311 Darren



NFC_Hardware Design Pin Def i ne

Pin	Symbol	I/O	Note
1	VBAT	Input	Power supply from battery (2.8V - 5.5V)
2	VDDIO	Input	Power supply to I/O (1.62V – 3.6V)
3	I²C -SDA	I/O	BSC Serial Data Line, active low
4	I²C -SCL	I	BSC Serial Clock
5	GND	G	Ground
6	IRQ-NFC	O	BSC request (active high)
7	NFC_PRESENCE	G	Ground
8	REG_UP	I	NFC Regulator power up (active high)
9	VDD_Ext_SE	Output	Power supply to External Secure Element (1.65V - 1.95V) (BCM20792S1 power switch: VDDSWP_OUT)
10	UIM_PWR	Input	Power supply to UICC (BCM20792S1 UICC supply: VDDSWP_IN) ETSI compliant to power class C (1.78V – 1.98V) ETSI compliant to power class B (2.9V – 3.3V)
11	SWP	I	SWP I/O 0 (Single-Wire Protocol interface)
S1	GND	G	Ground
S2	GND	G	Ground

Pin definition

Pin	Symbol	I/O	Note
1	VBAT	Input	Power supply from battery (2.3V - 5.5V)
2	VDDIO	Input	Power supply to I/O (1.62V – 3.6V)
3	VDD_Ext_SE	Output	Power supply to External Secure Element (1.65V - 1.95V)
4	I²C -SDA	I/O	BSC Serial Data Line, active low
5	I²C -SCL	I	BSC Serial Clock
6	GND	G	Ground
7	IRQ-NFC	O	BSC request, active high
8	UIM_PWR	Input	Power supply to UICC
9	SWP	I	SWP I/O 0 (Single-Wire Protocol interface)
10	NFC_PRESENCE	G	Ground
S1	GND	G	Ground
S2	GND	G	Ground

NFC CONN
==>PN:20.K0529.012
PIN:==>
PIN1 VBAT
PIN2 VDDIO
PIN3 I2C_SDA
PIN4 I2C-SCL
PIN5 GND
PIN6 IRQ_NFC
PIN7 NFC_PRESENCE
PIN8 REG_UP
PIN9 VDD_Ext_SE
PIN10 UIM_PWR
PIN11 SWP

<Variant Name>

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Hsichih, Taipei

Title: NFC
Size: C | Document Number: B560 with GPU | Rev: SA
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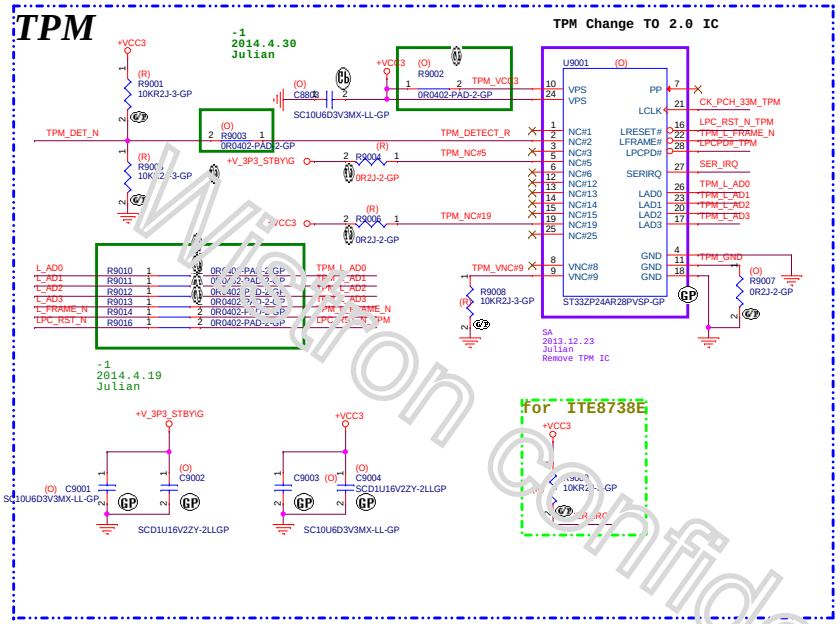
TPM



Pin Number	ST	NPCT
Pin 1	NC	GPIO0/XOR_OUT
Pin 2	NC	GPIO1
Pin 3	NC	NC
Pin 4	GND	VSS
Pin 5	NC	VSB
Pin 6	NC	GPIO2/GPX
Pin 7	PP	PP
Pin 8	VNC	TEST
Pin 9	VNC	GPIO3/BADD
Pin 10	VPS	NC
Pin 11	GND	NC
Pin 12	NC	NC
Pin 13	NC	NC
Pin 14	NC	NC
Pin 15	NC	CLKRUN#/GPIO4
Pin 16	LRESET#	LRESET#
Pin 17	LAD3	LAD3
Pin 18	GND	VSS
Pin 19	NC	VDD
Pin 20	LAD2	LAD2
Pin 21	LCLK	LCLK
Pin 22	LFRAME#	LFRAME#
Pin 23	LAD1	LAD1
Pin 24	VPS	VDD
Pin 25	NC	VSS
Pin 26	LAD0	LAD0
Pin 27	SERIRQ	SERIRQ
Pin 28	LPCPD#	LPCPD#

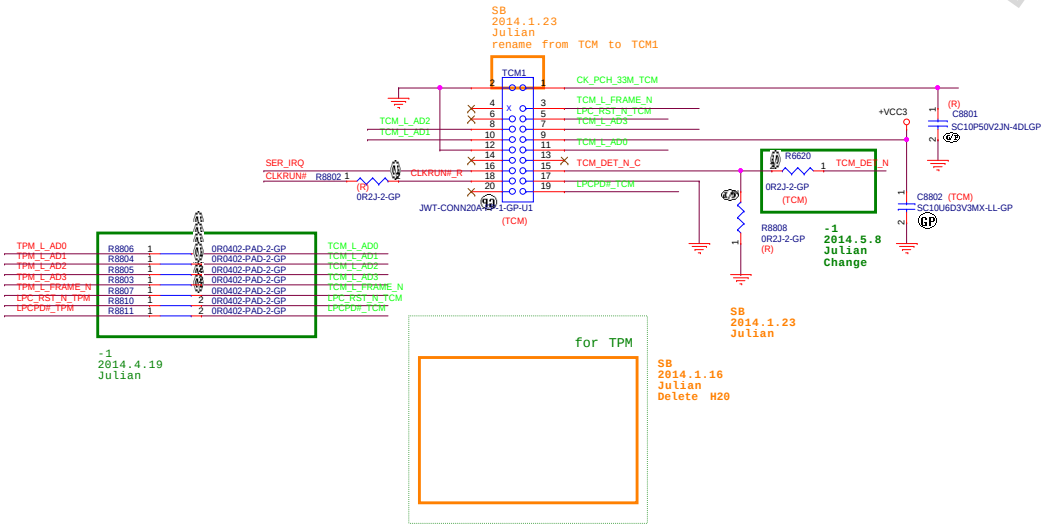
14. TPM (or TCM)Header
(1).Header color: BLACK
(2).Pin define:
pin1: LCLK pin2: GND
pin3: LFRAME# pin4: CUT
pin5: LRESET# pin6: VCC5
pin7: LAD3 pin8: LAD2
pin9: VCC3.3 pin10:LAD1
pin11:LAD0 pin12:GND
pin13:RSV0(Present#) pin14:RSV1(Disable)
pin15:3VSB pin16:SERIRQ
pin17:GND pin18:CLKRUN#
pin19:LPCPD# pin20:RSV2(Reserve GPIO,need pull high)

WPCT_Pin	GPIO0	GPIO1/SCI	ST_pin1
WPCT_Pin	GPIO1	GPIO2/SD	ST_pin2
WPCT_Pin	NC	ISO	ST_pin3
WPCT_Pin	GND	GND	ST_pin4
WPCT_Pin	VSB	NC	ST_pin5
WPCT_Pin	GPIO2(EN	GPIO3	ST_pin6
WPCT_Pin	PP	PP	ST_pin7
WPCT_Pin	NC	NC	ST_pin8
WPCT_Pin	GPIO3	GPIO4	ST_pin9
WPCT_Pin	NC	VDD	ST_pin10
WPCT_Pin	NC	NC	ST_pin11
WPCT_Pin	NC	VDD	ST_pin12
WPCT_Pin	NC	NC	ST_pin13
WPCT_Pin	NC	NC	ST_pin14
WPCT_Pin	GPIO4	GPIO5	ST_pin15
WPCT_Pin	LRESET#	LRESET#	ST_pin16
WPCT_Pin	LAD3	LAD3	ST_pin17
WPCT_Pin	GND	GND	ST_pin18
WPCT_Pin	VDD	NC	ST_pin19
WPCT_Pin	LAD2	LAD2	ST_pin20
WPCT_Pin	LCLK	LCLK	ST_pin21
WPCT_Pin	LFRAME#	LFRAME#	ST_pin22
WPCT_Pin	LAD1	LAD1	ST_pin23
WPCT_Pin	VDD	VDD	ST_pin24
WPCT_Pin	GND	NC	ST_pin25
WPCT_Pin	LAD0	LAD0	ST_pin26
WPCT_Pin	SERIRQ	SERIRQ	ST_pin27
WPCT_Pin	LPCPD#	LPCPD#	ST_pin28

17 L_AD0
17 L_AD1
17 L_AD2
17 L_AD3
17 L_FRAME_N
18 CK_PCH_33M_TCM
18 CK_PCH_33M_TPM
24 LPC_RST_N
19,24 SER_IRQ
19 TPM_DET_N
19 TCM_DET_N
17 CLKRUN#
17,19 DISABLE_TPM

24 TCM_L_AD0
24 TCM_L_AD1
24 TCM_L_AD2
24 TCM_L_AD3
24 LPCPD#_TCM
24 TCM_L_FRAME_N

TCM



2. Daughter Card Connecter

2.1 Connector Pin Out and Signal Description

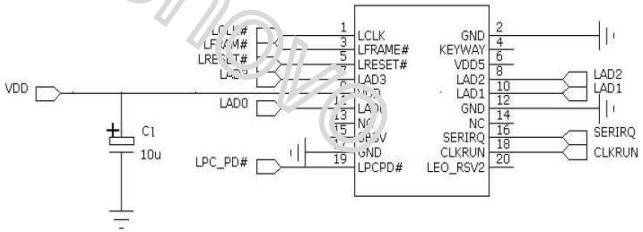


Figure 2-1 typical application

<Variant Name>

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12F, 88, Hsin Tai Wu Rd
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Title: TPM/TCM
Size: C | Document Number: B560 with GPU | Rev: SA
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<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
(Reserve) Finger Print

Size	Document Number	Rev
C	B560 with GPU	SA

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<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
(Reserve)Express Card

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 90 of 106

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
Res Smart Card Socket

Size	Document Number	Rev
C	B560 with GPU	SA

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<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
Res Switchable GFX eDP

Size	Document Number	Rev
C	B560 with GPU	SA

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<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
(Reserve) PCI

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 93 of 106

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
(Reserve)Inter LAN WG1217LM

Size	Document Number	Rev
C	B560 with GPU	SA

Date: Tuesday, May 13, 2014 Sheet 94 of 106

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
(Reserve) LAN Switch

Size	Document Number	Rev
C	B560 with GPU	SA

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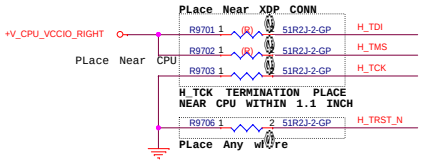
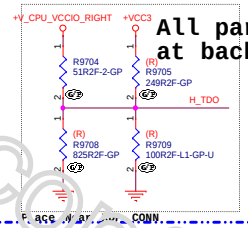
XDP for CPU

4 H_TDO
4 H_TDI
4 H_TMS
4 H_TCK
4 H_TRST_N

4,17 XDP_DBRESET_N
4,17,36 H_PWRGD



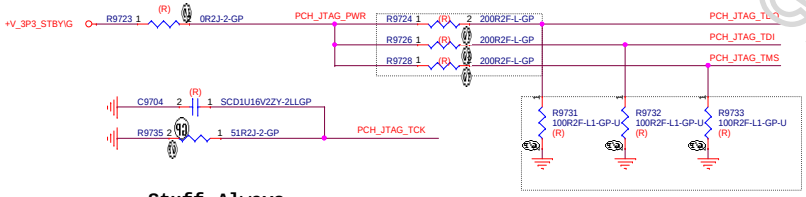


All parts can be placed at back side

XDP for PCH

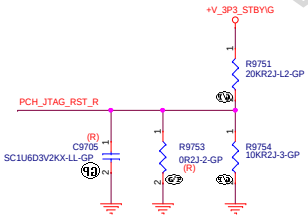
17 PCH_JTAG_RST_R
17 PCH_JTAG_TDO
17 PCH_JTAG_TDI
17 PCH_JTAG_TMS
17 PCH_JTAG_TCK

Stuff 200 ohm for ES2
Empty for production



Stuff Always

Stuff for ES2 and empty after production



All parts can be placed at back side

<Variant Name>

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Title: CPU_XDP ; PCH_XDP;PORT80

Size: C | Document Number: B560 with GPU | Rev: SA

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<Variant Name>

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Title: Table of Content

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C	B560 with GPU	SA

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<Variant Name>

Wistron Incorporated
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Title
GPIO table

Size	Document Number	Rev
C	B560 with GPU	SA

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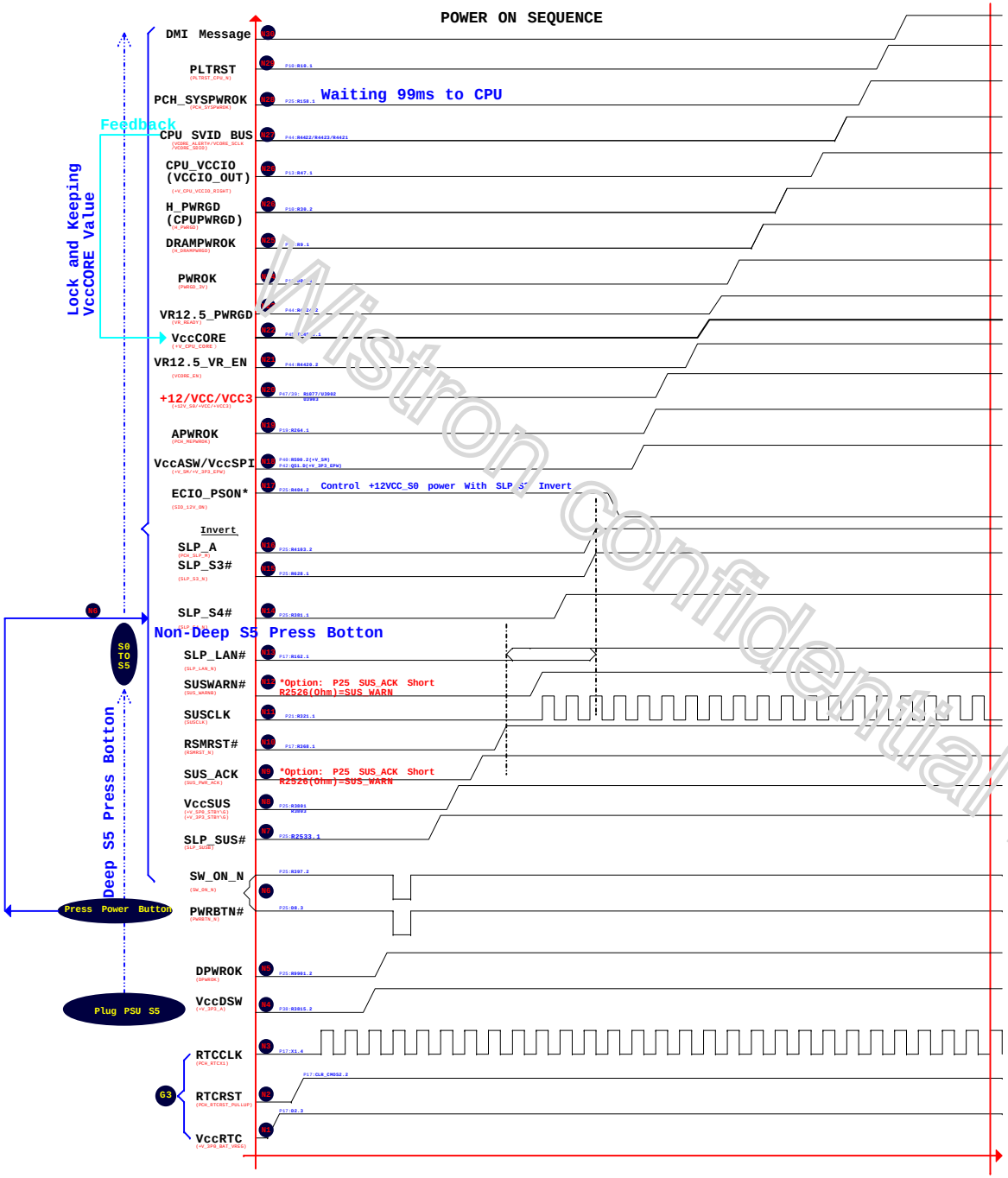
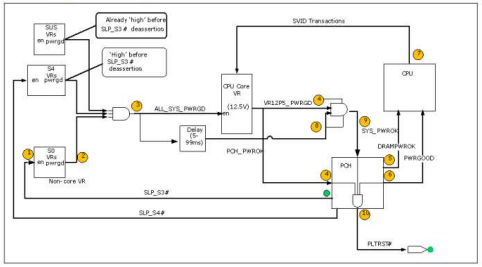
POWER ON SEQUENCE



datasheet 490828=page17

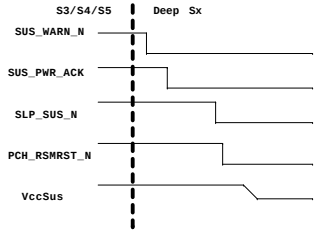
Figure 2-3. Flow Diagram for SYS_PWROK Generation – 2 Chip Platform



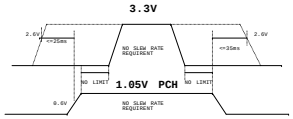
NOTES:

1. SYS_PWROK can be optionally asserted with PCH_PWROK. t14 may range from 5ms to 99ms depending on platform capabilities and/or requirements. t14 will need to be at least 99ms for designs supporting PCIe devices.
2. PCIe devices need to be under reset for 99ms after their power supplies are stable. However, mini-PCIe devices require only 1ms (refer PCI Express® Mini Card Electromechanical Specification Revision 1.21). System design can therefore set a delay between 5 to 99 ms for ALL_SYS_PWRGD assertion to SYS_PWROK assertion.

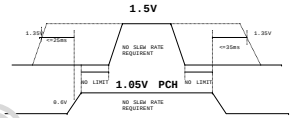
S3/S4/S5 to Deep Sx SEQUENCE



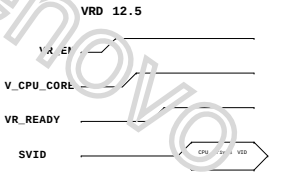
Sequencing Requirements between PCH VCC3_3 and VCC Core Rail



Sequencing Requirements between PCH VCC3_3 and VCC Core Rail



VRD 12.5



SVIDs can be driven by the CPU between PWRGOOD and PLTRST# deassertion

<Variant Name>

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Title: SYSTEM & GPU POWER SEQUENCE

Size: D | Document Number: B560 with GPU | Rev: SA

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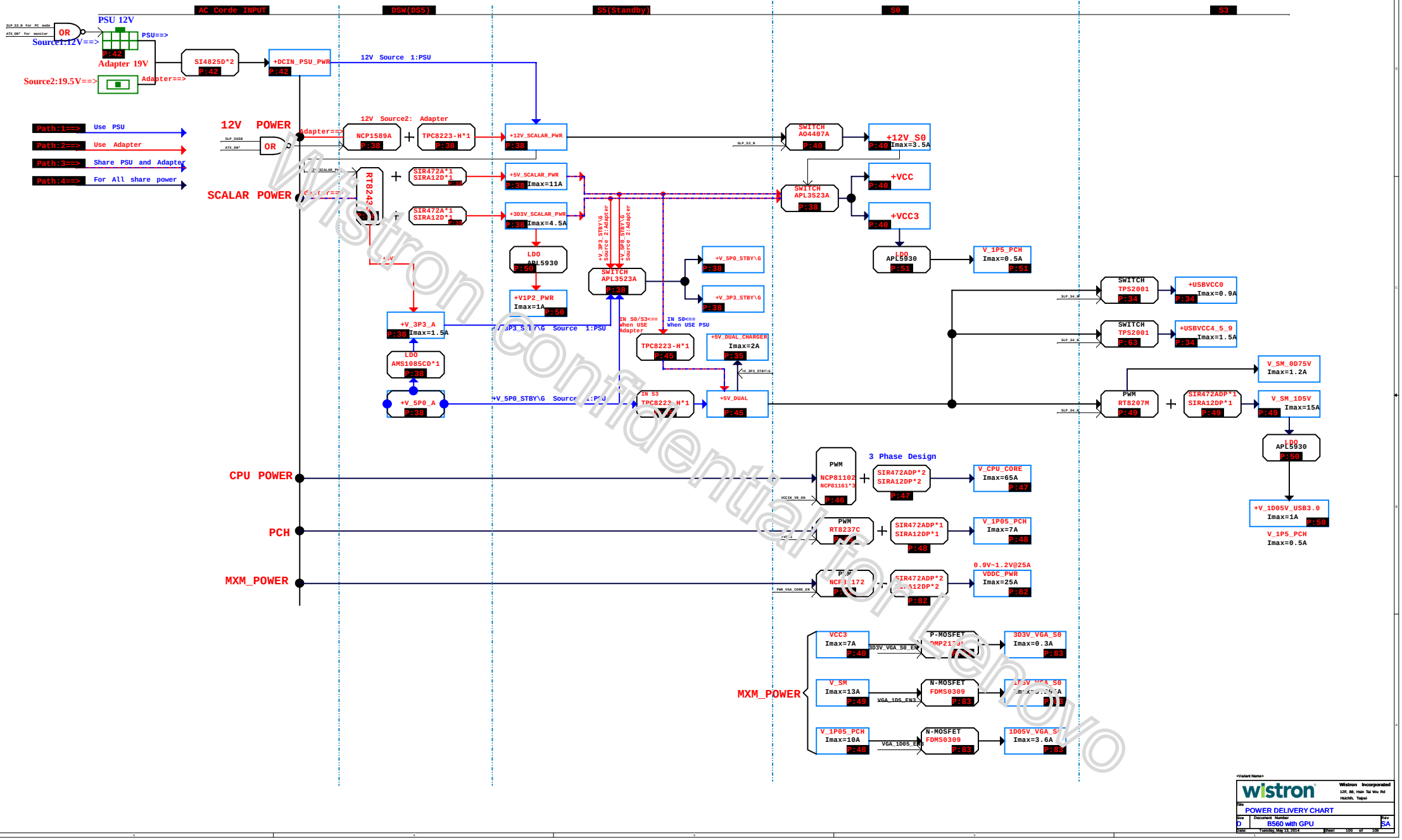

<Variant Name>

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Title: SMBUS table

Size	Document Number	Rev
D	B560 with GPU	SA

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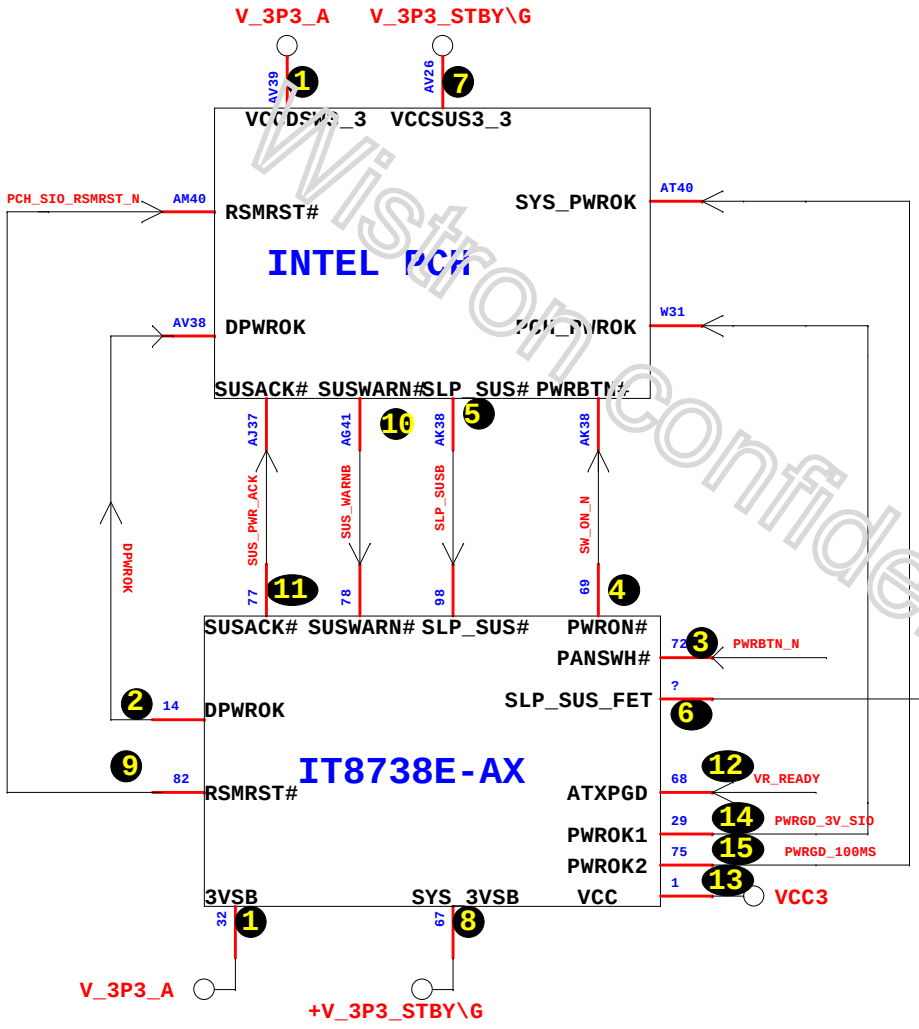
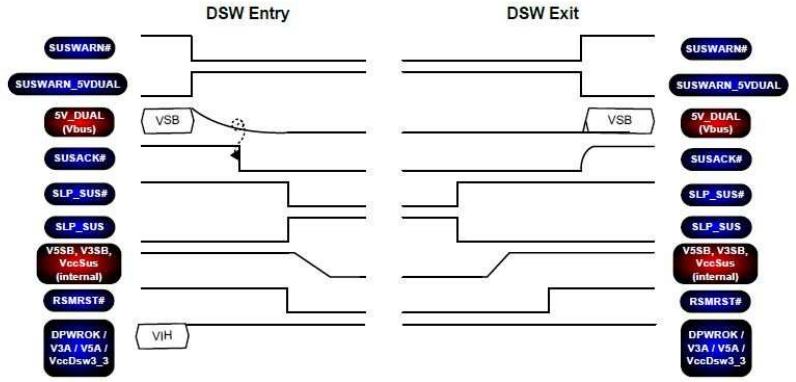


DSW Power Sequence



SLP_SUS_FET → Q34 → V_3P3_STBY\G

<Variant Name>

wistron Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: (Reserved)

Size	Document Number	Rev
C	B560 with GPU	SA

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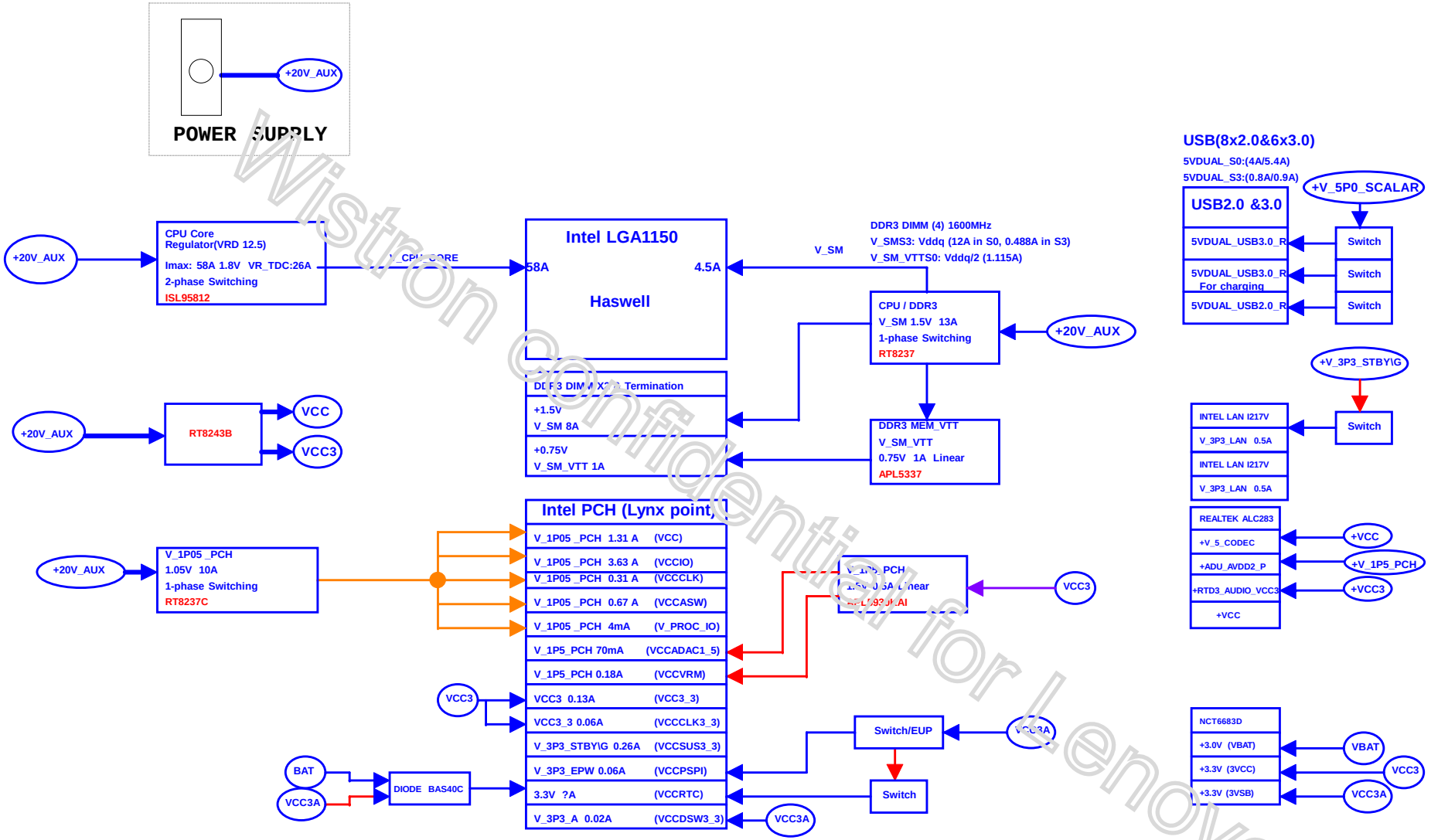

<Variant Name>

wistron

Wistron Incorporated
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Hsichih, Taipei

Title: POWER MAP

Size	Document Number	Rev
C	B560 with GPU	SA

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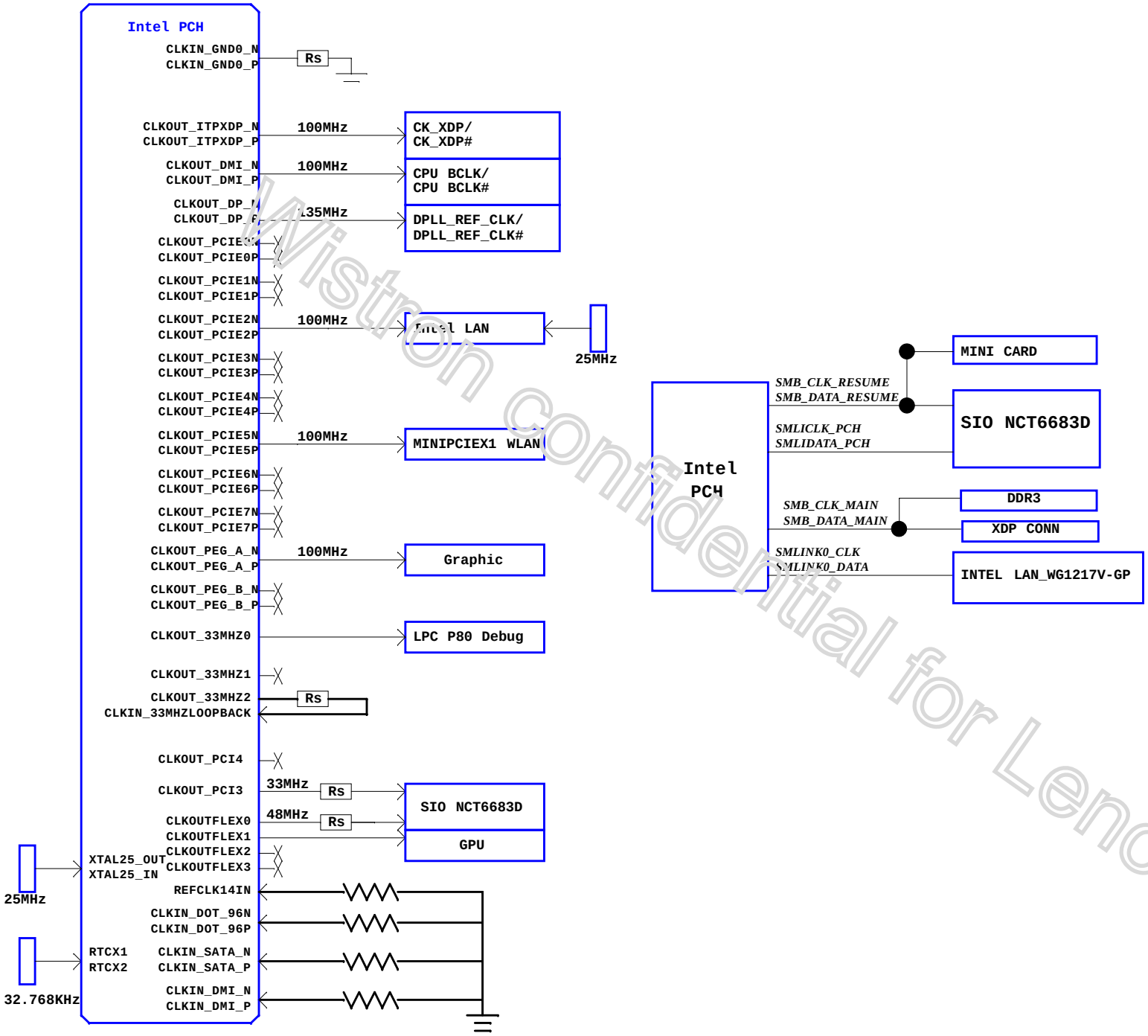


Note: .... is Reserve

Note: Rs is series resister

<Variant Name>

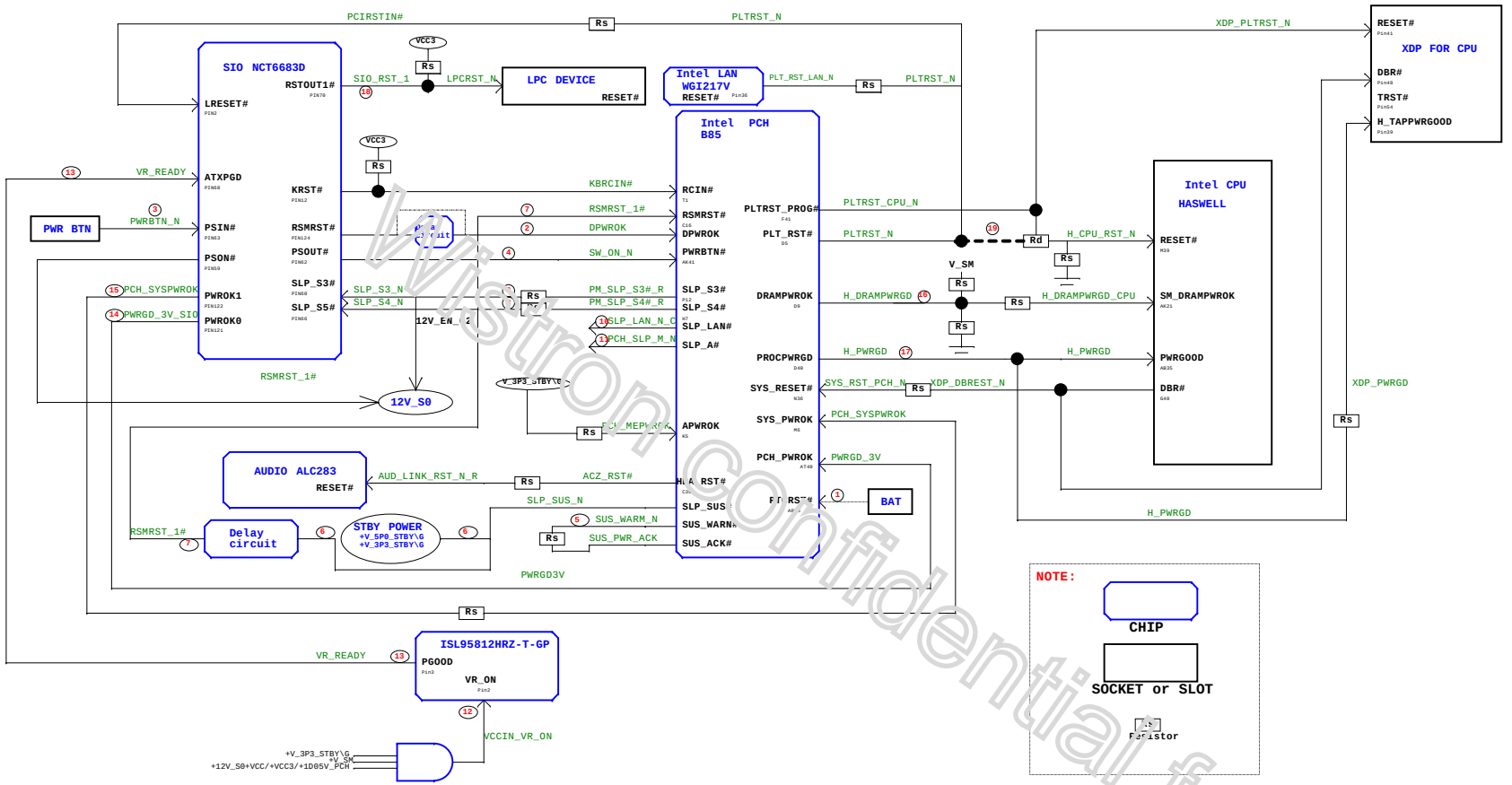
wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CLOCK MAP

Size: C | Document Number: B560 with GPU | Rev: SA

Date: Tuesday, May 13, 2014 | Sheet 104 of 106



<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Change History

Size	Document Number	Rev
C	B560 with GPU	SA

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