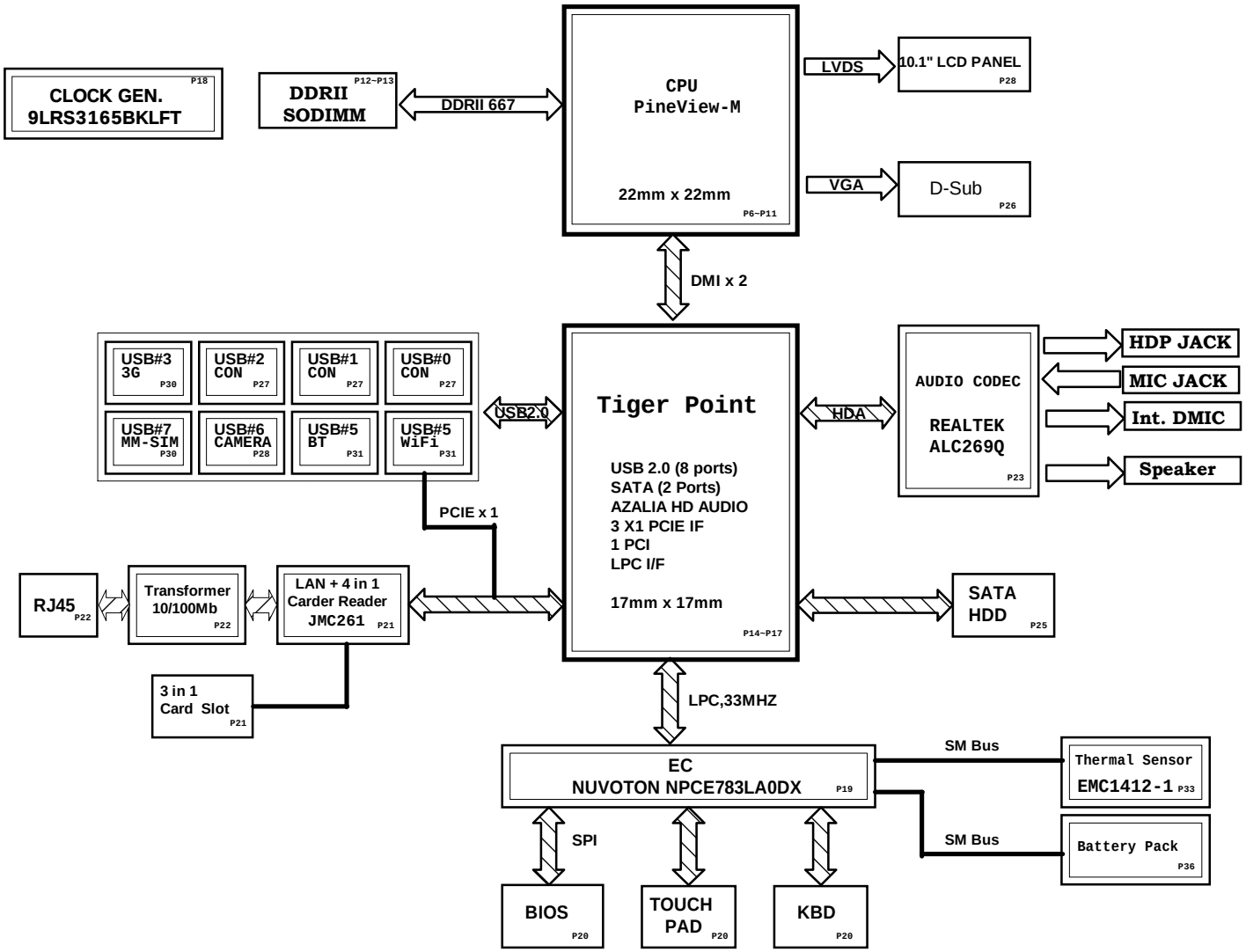
M9F1 Block Diagram R1.0



TI Charger BQ24753ARHDR P.36	
Inputs	Outputs
DC_IN	DCBATOUT BT+

System DC/DC TPS51125RGER P.37	
Inputs	Outputs
DCBATOUT	+3VALW +5VALW +5VALW_LDO +ECVCC

System DC/DC TPS51124RGER P.38	
Inputs	Outputs
DCBATOUT	+1_8VSUS VCCGFX

CPU DC/DC MAX8796GTJ+ P.39	
INPUTS	OUTPUT
DCBATOUT	VHCORE

System DC/DC G2998BP11U P.40	
Inputs	Outputs
+1_8VSUS	+0_9VRUN

System DC/DC G9731F11U P.40	
Inputs	Outputs
+1_8VSUS	+1_5VRUN

System DC/DC G9731F11U P.40	
Inputs	Outputs
+1_8VSUS	+1_05VRUN

[redacted]

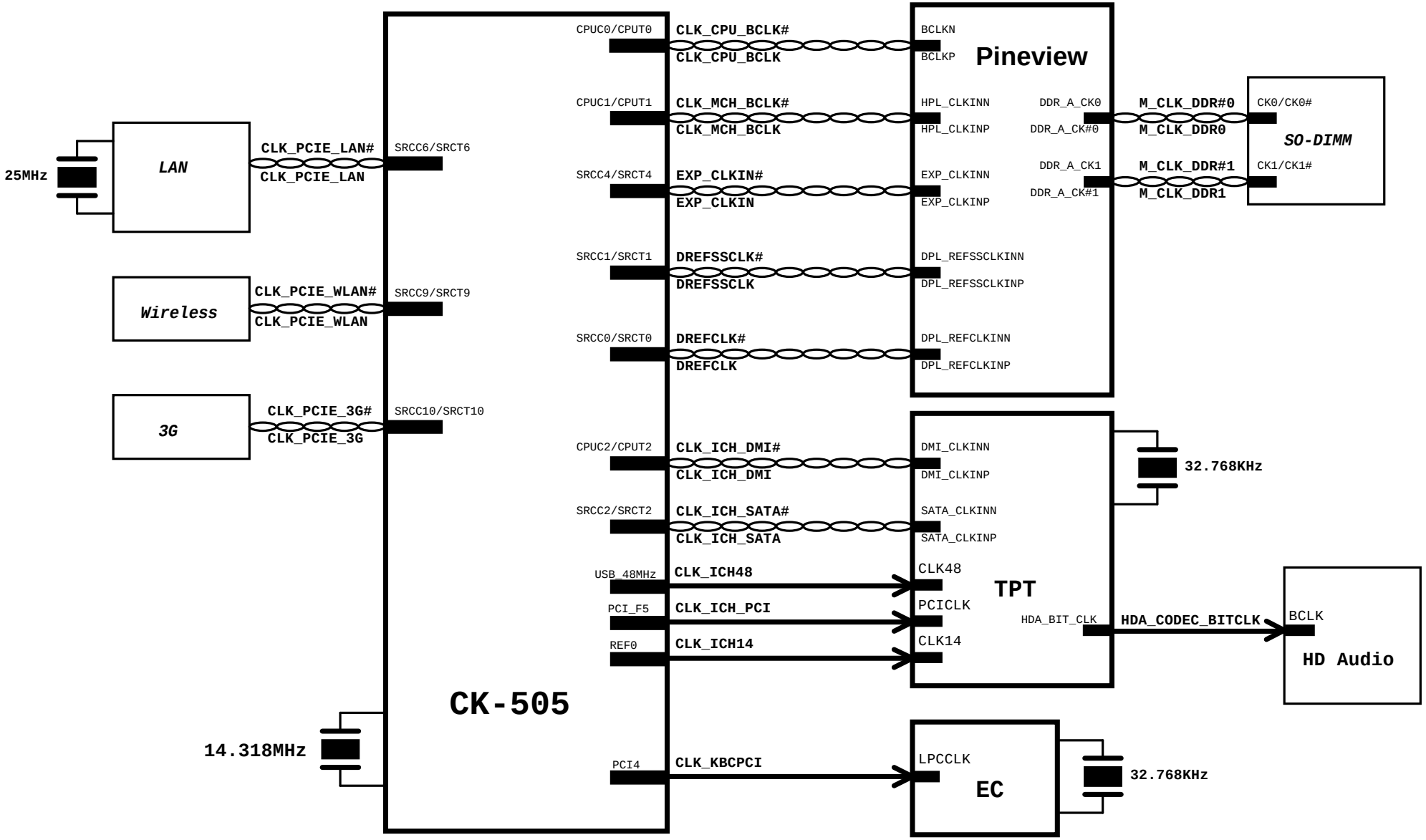
CCPBG

Title: **Block Diagram**

Size: A2 | Document Number: *M9F1* | Rev: 0.1

Date: Wednesday, March 17, 2010 | Sheet 1 of 44

http://hobi-elektronika.net



[redacted]

CCPBG

Title	Clock distribution	
Size A3	Document Number M9F1	Rev 0.1
Date: Wednesday, March 17, 2010	Sheet 2 of 44	

Pine Trail Power Flowchart for M9F1

Voltage Rails O MEANS ON X MEANS OFF

power plane / State	+5VALW_LDO +ECVCC	+5VALW +3VALW	+3VSUS +1_8VSUS	+5VRUN +3VRUN +1_8VRUN +1_5VRUN +1_05VRUN +0_9VRUN VCCGFX VHCORE
S0	0	0	0	0
S3	0	0	0	X
S5/AC, S4	0	0	X	X
S5 Battery only	0	X	X	X
S5 S4/AC & Battery don't exist (G3)	X	X	X	X

S3 : STR

S4 : STD

S5 : SOFT OFF

G3 : ME OFF

[redacted]

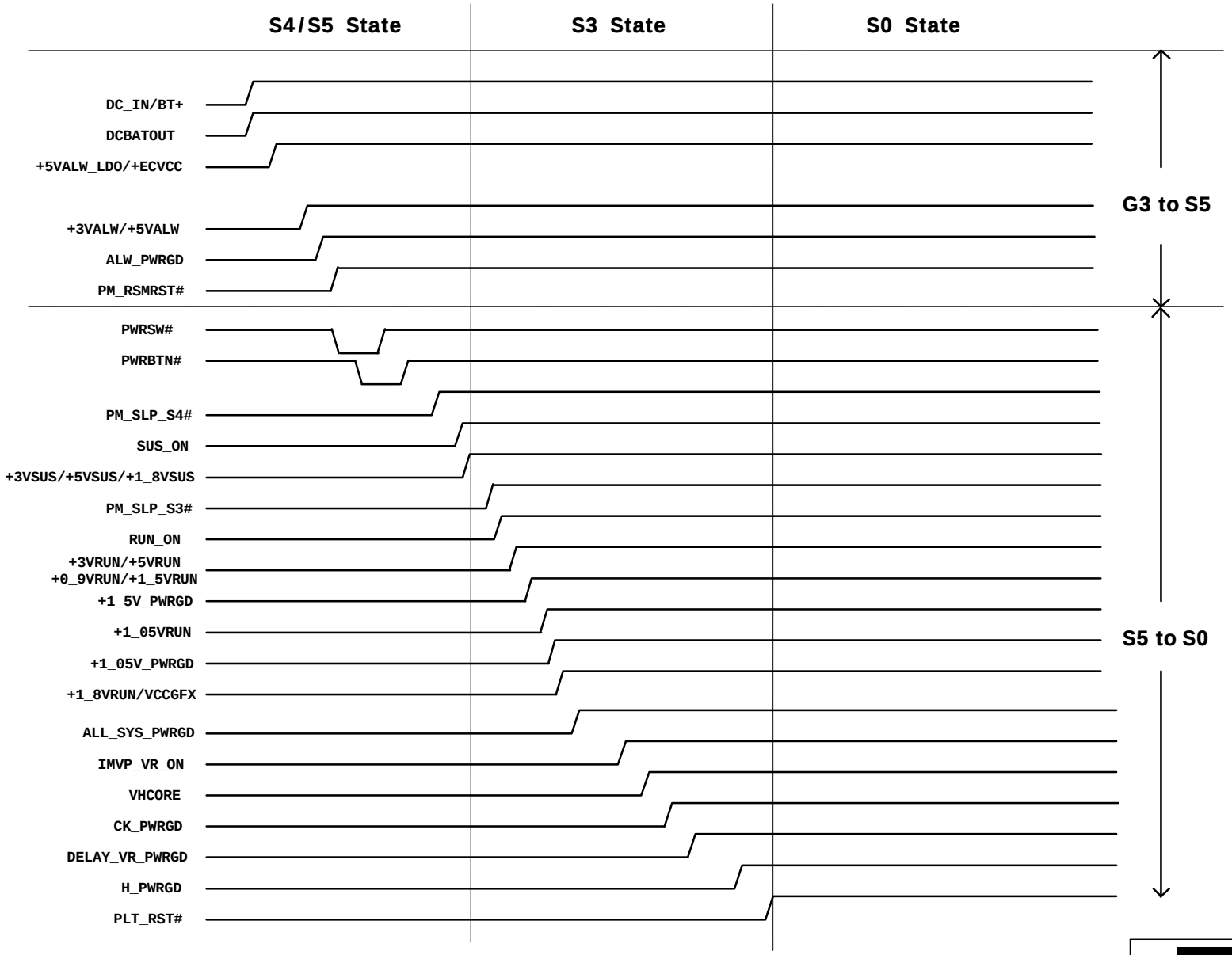
CCPBG

Title: Power Flowchart		
Size: A3	Document Number: M9F1	Rev: 0.1
Date: Wednesday, March 17, 2010	Sheet 3 of 44	

Pine Trail Power On Sequence

http://hobi-elektronika.net

REV : 2009/08/17



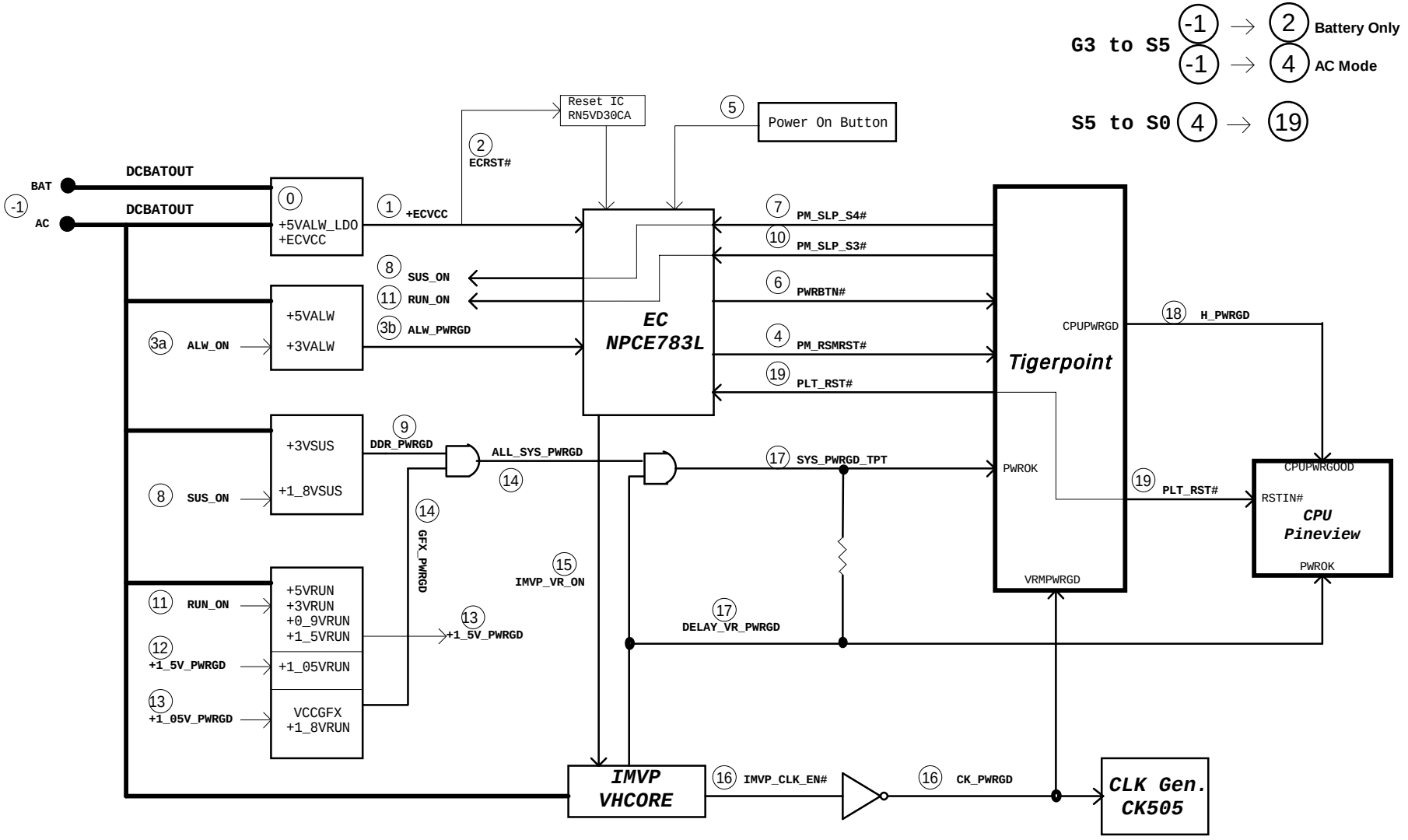
[redacted]

CCPBG

Title	Power On Sequence(1)	
Size: Custom	Document Number: M9F1	Rev: 0.1
Date: Wednesday, March 17, 2010	Sheet 4 of 44	

REV : 2009/08/18

Pine Trail Power On Sequence



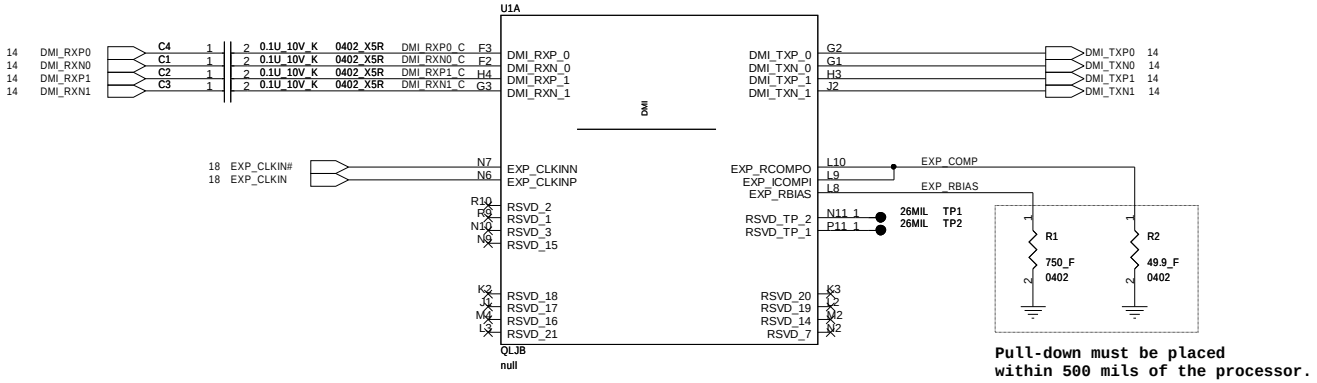
[redacted]

CCPBG

Title: Power On Sequence(2)

Size: Custom | Document Number: M9F1 | Rev: 0.1

Date: Wednesday, March 17, 2010 | Sheet 5 of 44

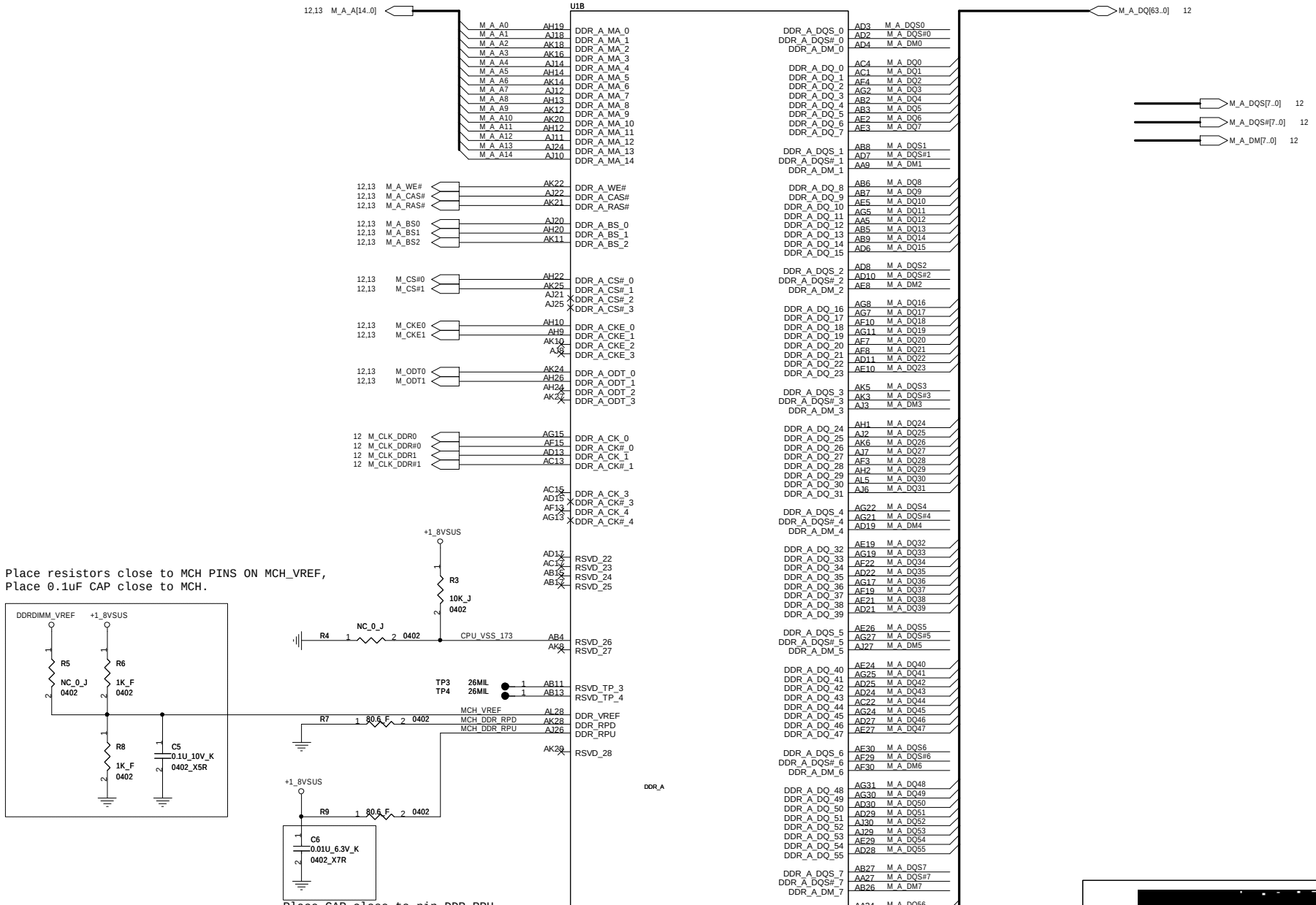


Pull-down must be placed within 500 mils of the processor.

[redacted]

CCPBG

Title	**CPU- Pineview (1)**	
Size A3	Document Number *M9F1*	Rev 0.1
Date: Wednesday, March 17, 2010	Sheet 6 of 44	

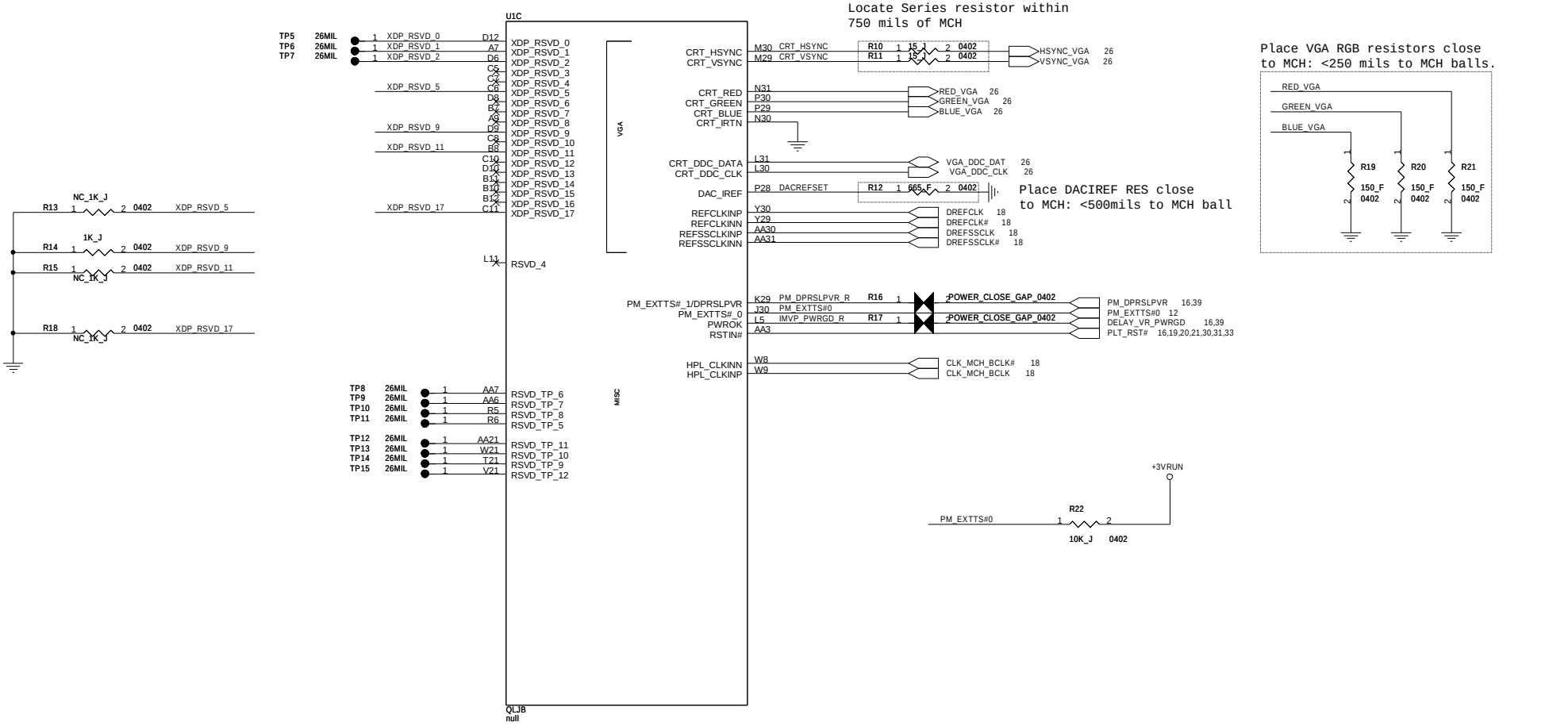


[redacted]

CCPBG

Title: **CPU- Pineview (2)**

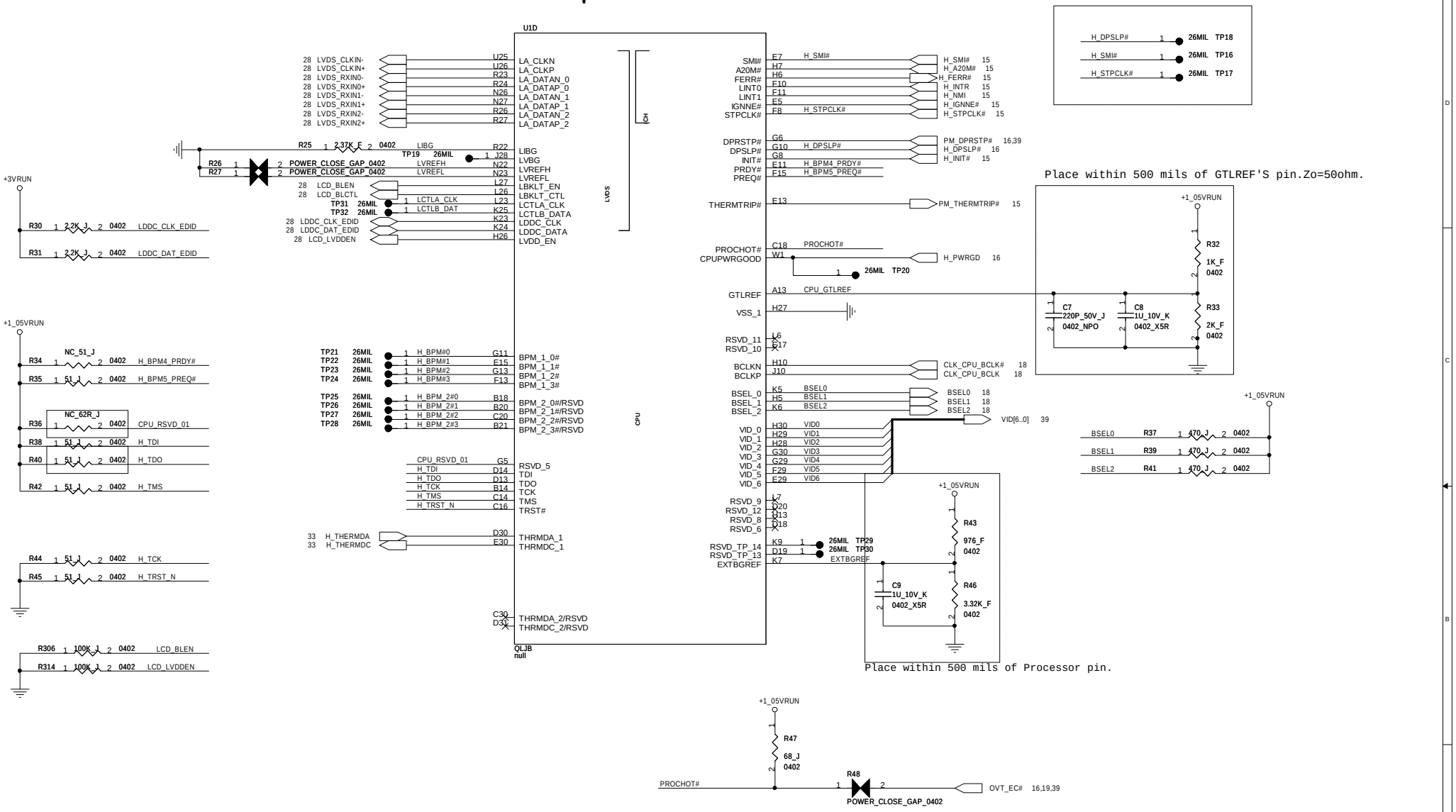
Size	Document Number	Rev
A3	*M9F1*	0.1
Date: Wednesday, March 17, 2010	Sheet 7 of 44	



[redacted]

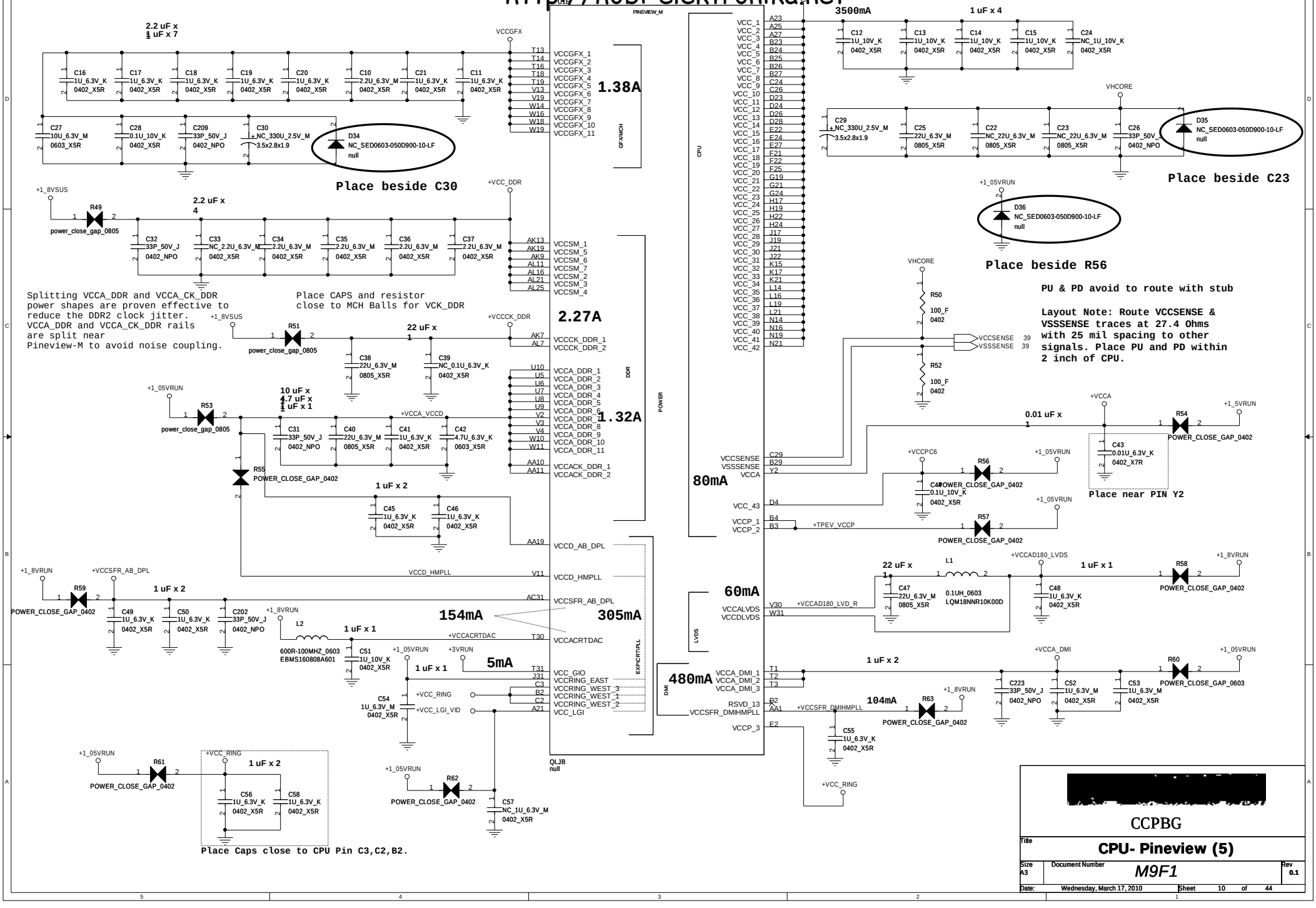
CCPBG

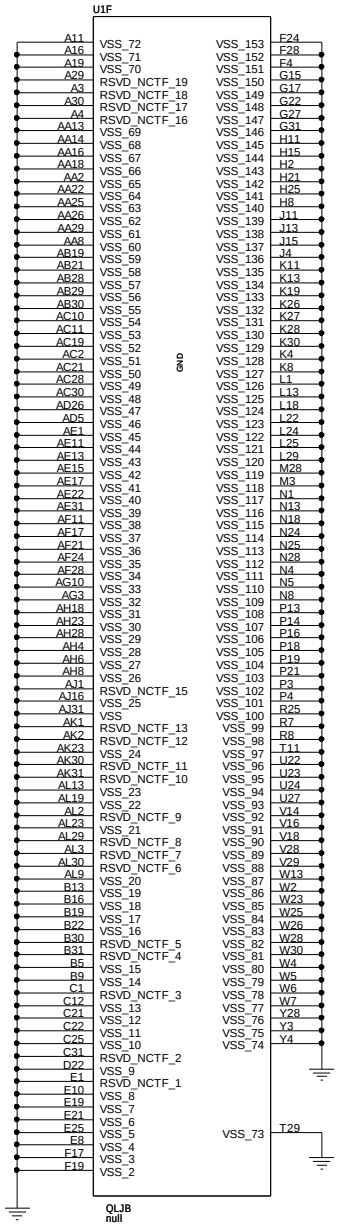
Title	**CPU- Pineview (3)**	
Size A3	Document Number *M9F1*	Rev 0.1
Date: Wednesday, March 17, 2010	Sheet 8 of 44	



CCPBG

Title	CPU- Pineview (4)	
Size A3	Document Number M9F1	Rev 0.1
Date: Wednesday, March 17, 2010	Sheet 9 of 44	





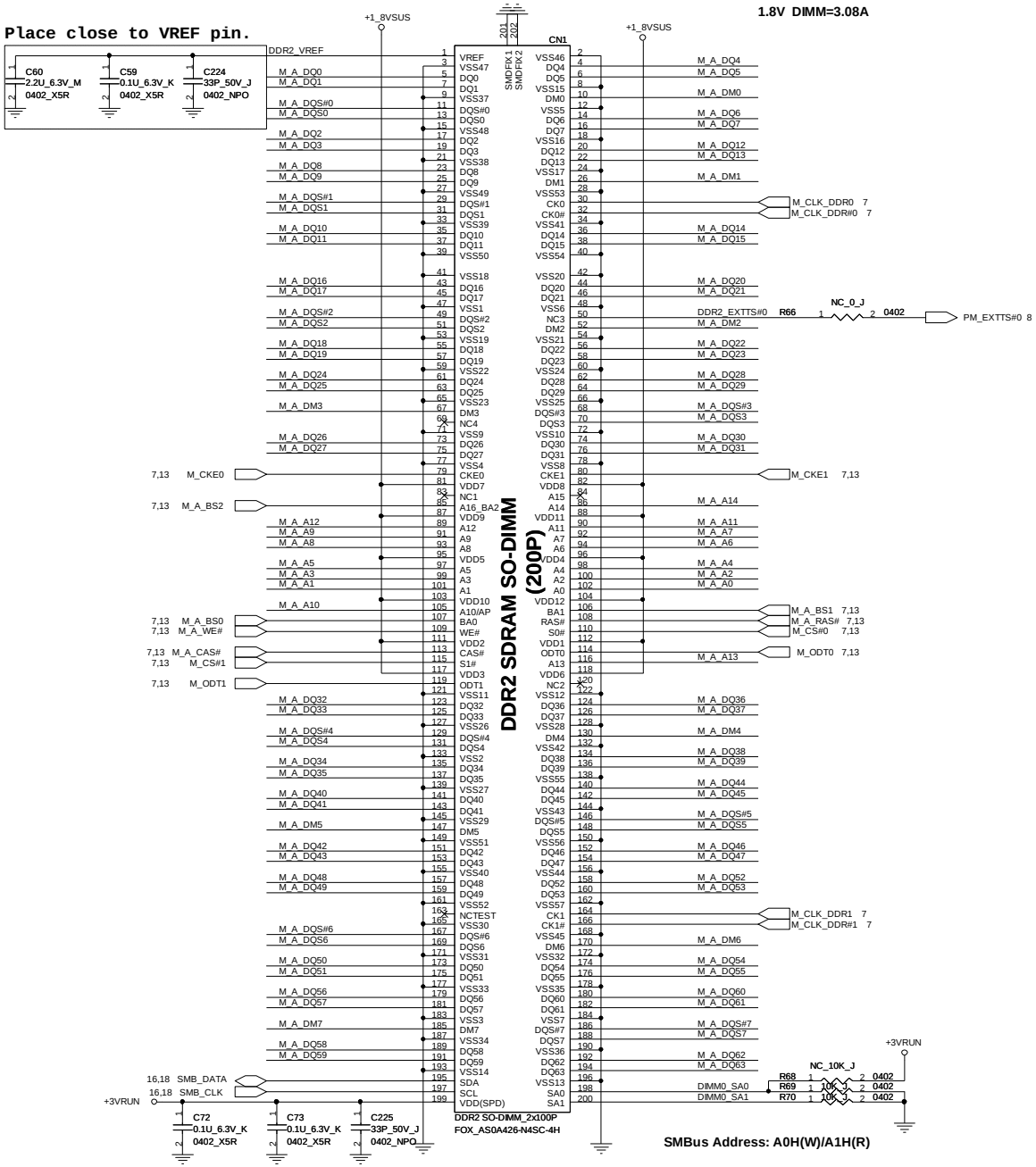
[redacted]

CCPBG

Title	**CPU- Pineview (6)**	
Size A3	Document Number *M9F1*	Rev 0.1
Date: Wednesday, March 17, 2010	Sheet 11 of 44	

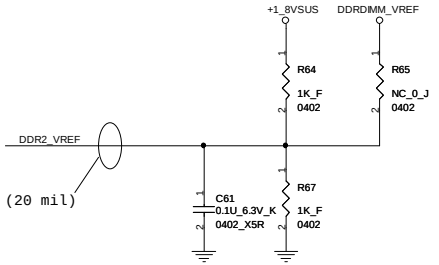
Place close to VREF pin.

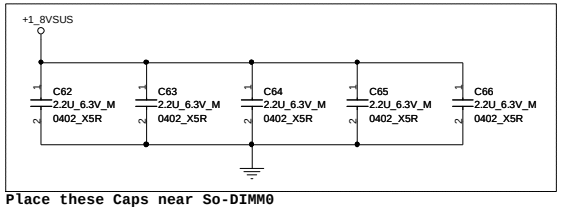
1.8V DIMM=3.08A



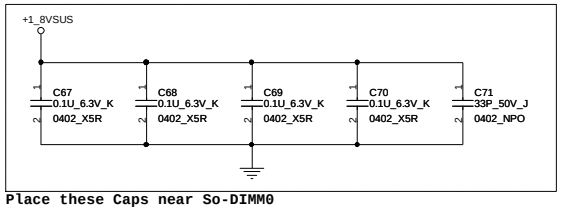
SMBus Address: A0H(W)/A1H(R)

7 M_A_DQ[63:0]
7,13 M_A_A[14..0]
7 M_A_DQS[7..0]
7 M_A_DQS#[7..0]
7 M_A_DM[7..0]





Place these Caps near So-DIMM0

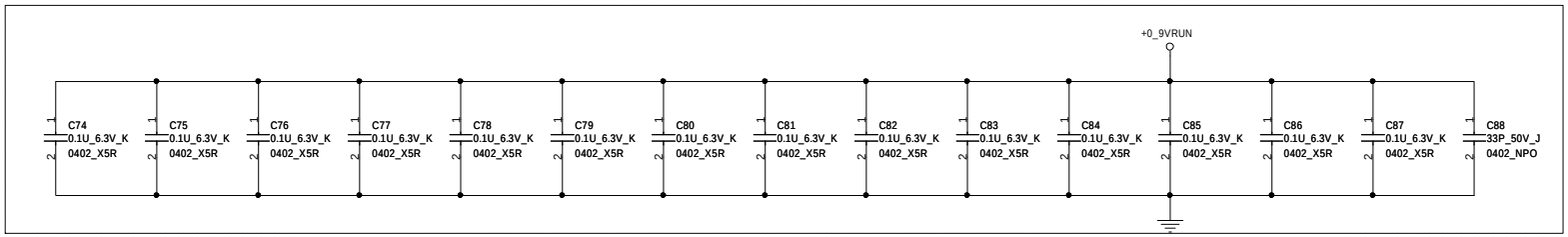


Place these Caps near So-DIMM0

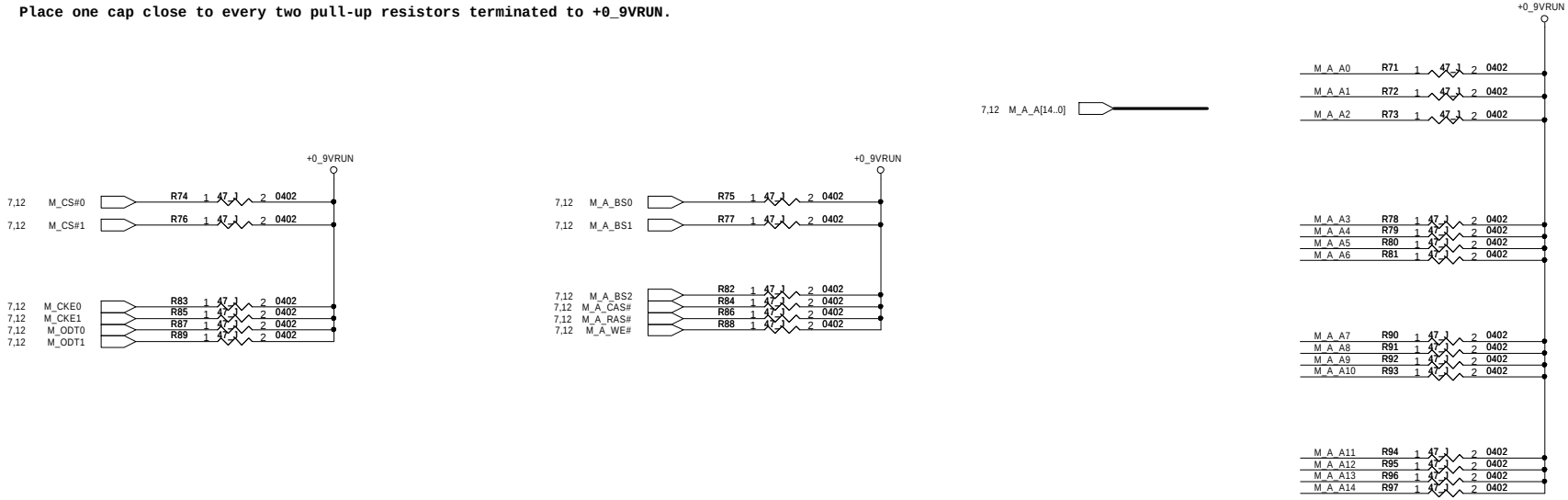
[redacted]

CCPBG

Title	DDRII(SO-DIMM0)		
Size: Custom	Document Number: M9F1		Rev: 0.1
Date: Wednesday, March 17, 2010	Sheet 12 of 44		



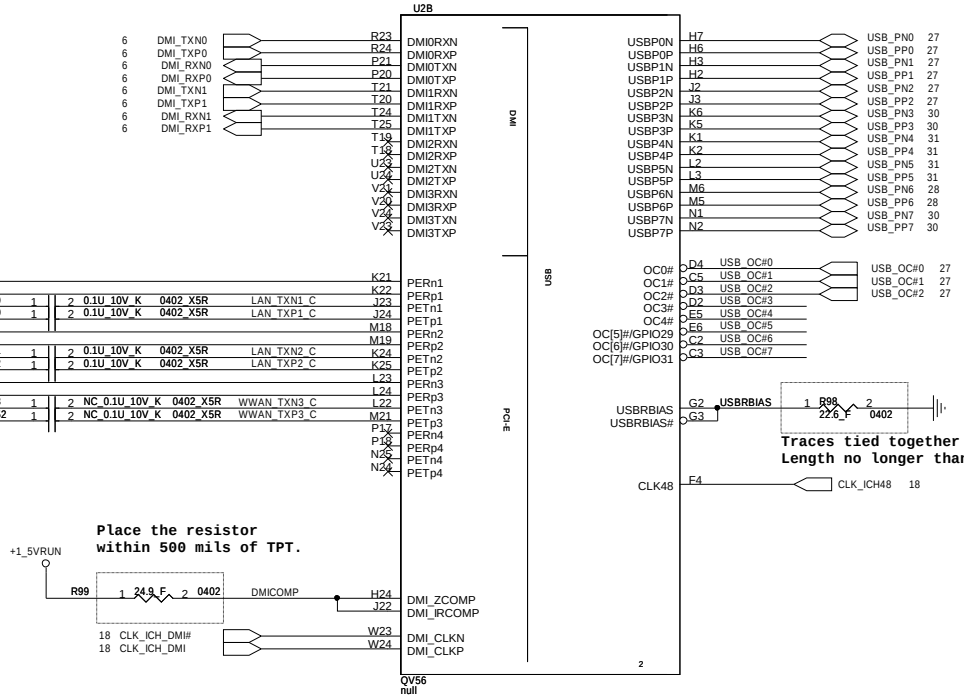
Place one cap close to every two pull-up resistors terminated to +0_9VRUN.



[redacted]

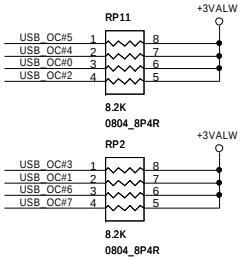
CCPBG

Title	DDRII (Termination)	
Size A3	Document Number M9F1	Rev 0.1
Date: Wednesday, March 17, 2010	Sheet 13 of 44	



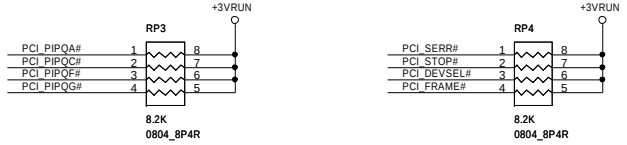
USB port table

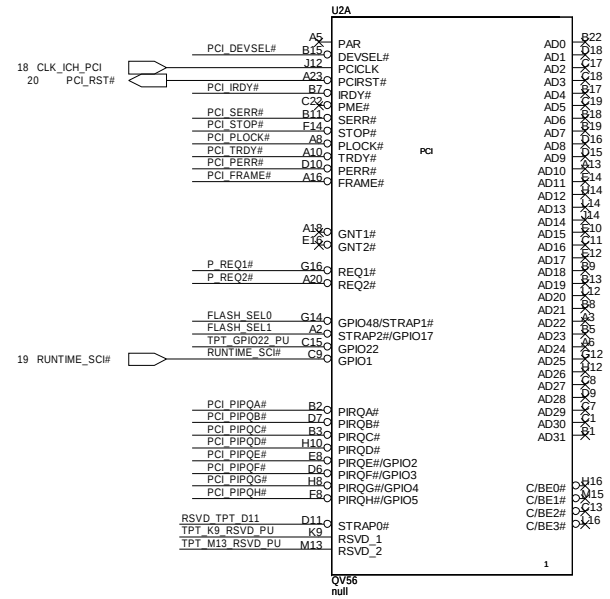
Port0	External USB1
Port1	External USB2
Port2	External USB3
Port3	WWAN (3G/GPS)
Port4	WLAN(WIFI)
Port5	Bluetooth
Port6	Camera module
Port7	MM-SIM



Traces tied together close to Pin
Length no longer than 200 mil to Resistor.

Place the resistor
within 500 mils of TPT.

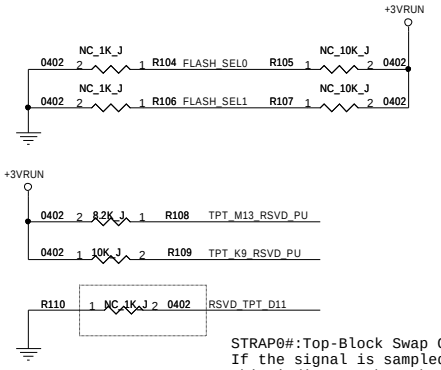




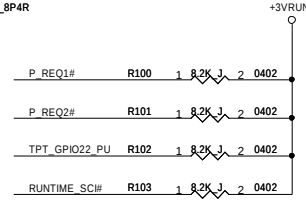
Straping Options Flash

STRAP2#/ GPIO17	STRAP1#/ GPIO48	Routing
0	1	SPI
1	0	PCI
1	1	LPC

STRAP2#/GPIO17 and STRAP1#/GPIO48
have weak internal pull-ups



STRAP0#:Top-Block Swap Override.
If the signal is sampled low,
this indicates that the system is
strapped to the "top-block swap" mode
(Tiger Point inverts A16 for all cycles targeting FWH BIOS space)



TPT Strap Pin

Strap Pin	Internal PU/PD	External PU/PD
STRAP0#	PU 20K	PU 10K(NC) to +3VRUN/PD 1K(NC)
STRAP1#	PU 20K	PU 10K(NC) to +3VRUN/PD 1K(NC)
STRAP2#	PU 20K	PU 10K(NC) to +3VRUN/PD 1K(NC)

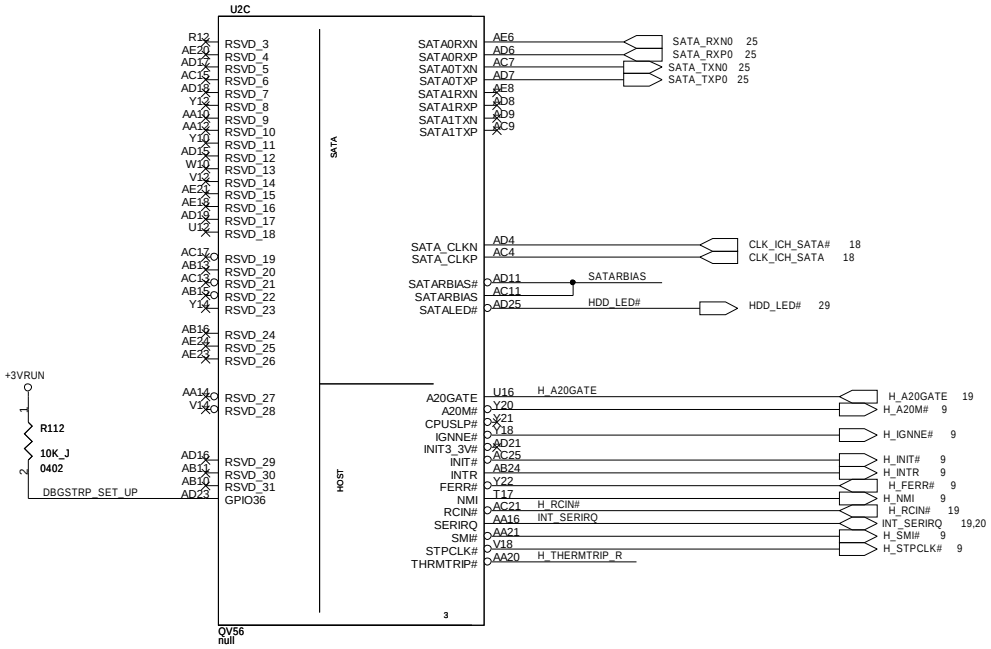
[redacted]

CCPBG

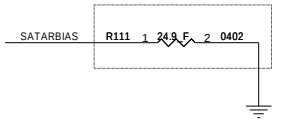
Title: **Tiger Point (1)**

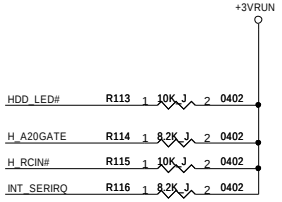
Size	Document Number	Rev
A3	*M9F1*	0.1

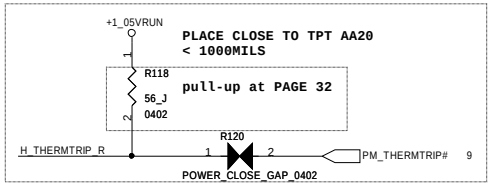
Date: Wednesday, March 17, 2010 Sheet 14 of 44



PLACE SATARBIAS RESISTORS CLOSE TO ICH: <500 MILS TO ICH BALLS



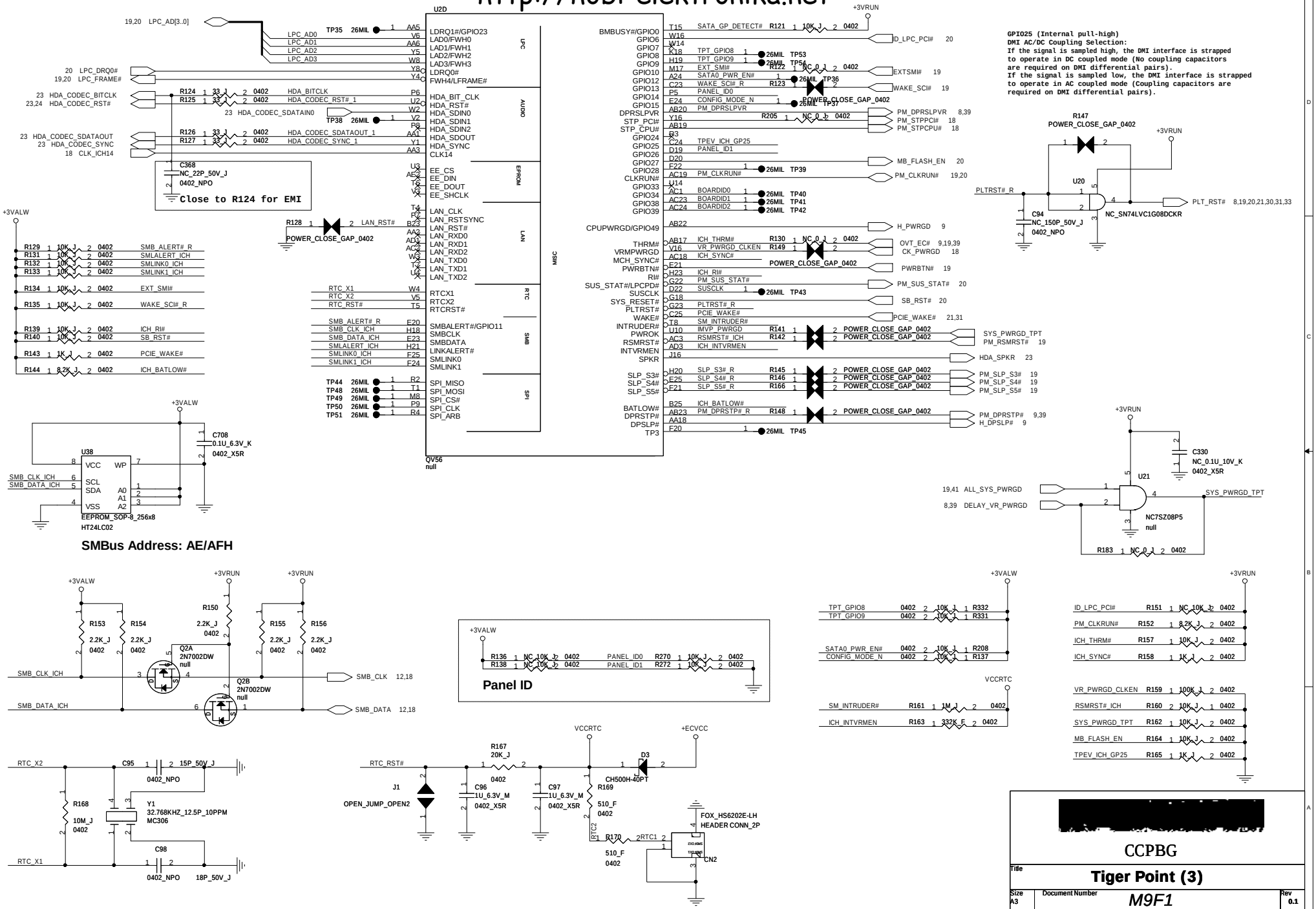




[redacted]

CCPBG

Title: **Tiger Point (2)**		
Size: A3	Document Number: *M9F1*	Rev: 0.1
Date: Wednesday, March 17, 2010	Sheet 15 of 44	



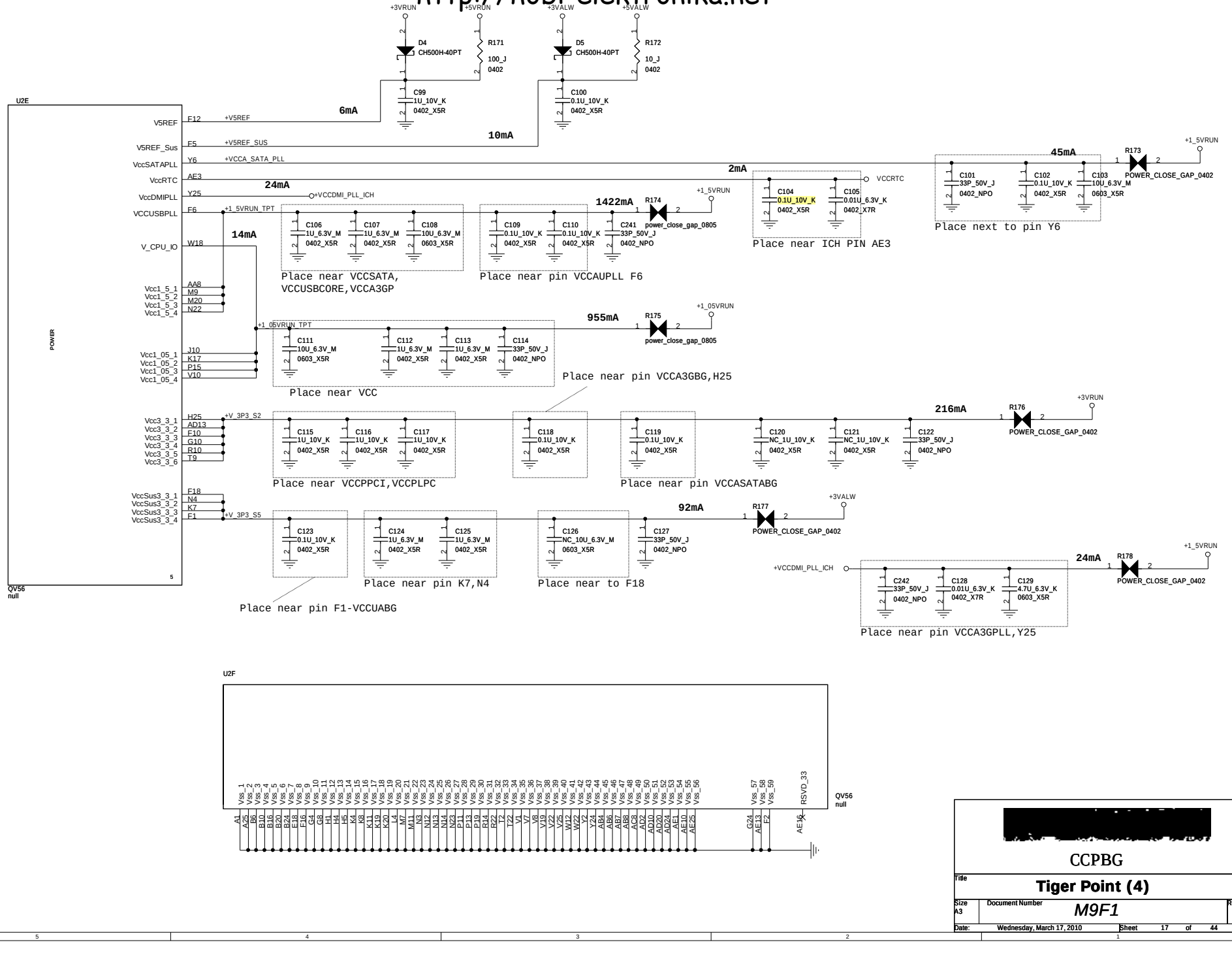
[redacted]

CCPBG

Title: **Tiger Point (3)**

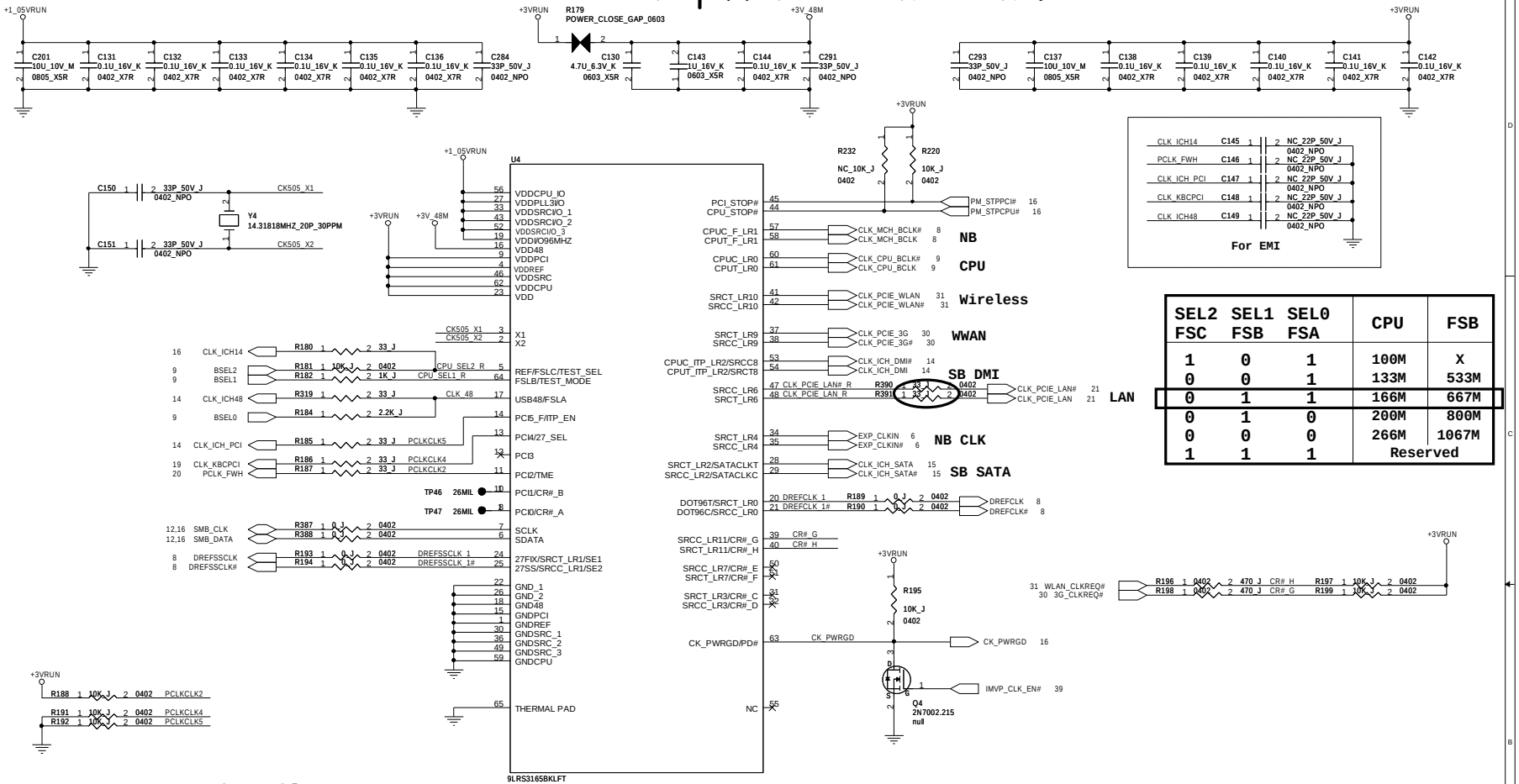
Size	Document Number	Rev
A3	*M9F1*	0.1

Date: Wednesday, March 17, 2010 Sheet 16 of 44



CCPBG

Title	Tiger Point (4)	
Size A3	Document Number M9F1	Rev 0.1
Date: Wednesday, March 17, 2010	Sheet 17 of 44	



SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M
1	1	1	Reserved	

ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

[redacted]

CCPBG

Title: CLOCK GEN

Size	Document Number	Rev
Custom	M9F1	0.1

Date: Wednesday, March 17, 2010 Sheet 18 of 44

Use EC to implement power limit
Wireless switch should use U5.124, reserve U5.100 A/D for detecting voltage level
(Default setting -- Hardware Power Limit)
If use EC to implement, it should do setting as below.

Stuff
C720, C721, R233, R359, PR144, PR145, PR146

NC
R357, PR139, PU9, PC115, PC116, PR118, PR123, PR124

100mA

LID Switch

T/P

EC RESET

Place at EC side.

SYSTEM ID0-1

GPIO (wake-up capability)

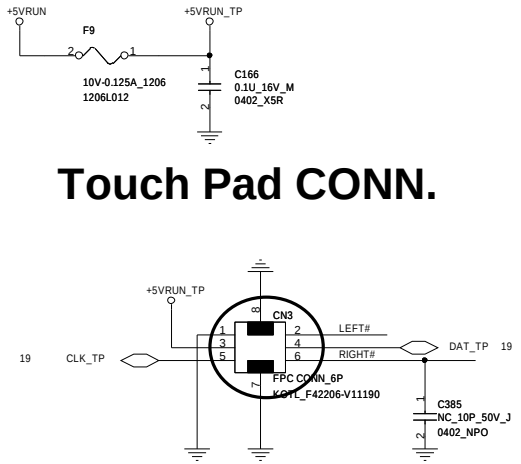
GPIO (no wake-up capability)

WLAN_EN changes to HIGH enable

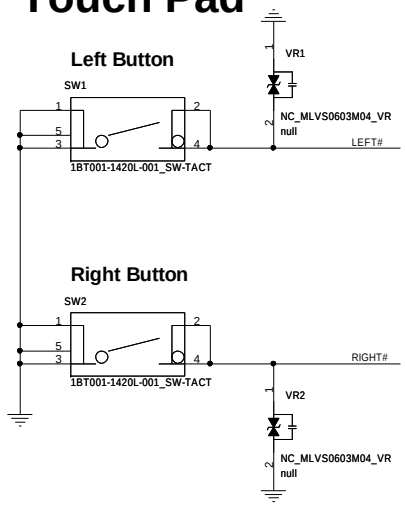
CCPBG

Title	EC (NPCE783L)
Size: Custom	Document Number: M9F1
Rev	0.1
Date: Wednesday, March 17, 2010	Sheet 19 of 44

Touch Pad CONN.



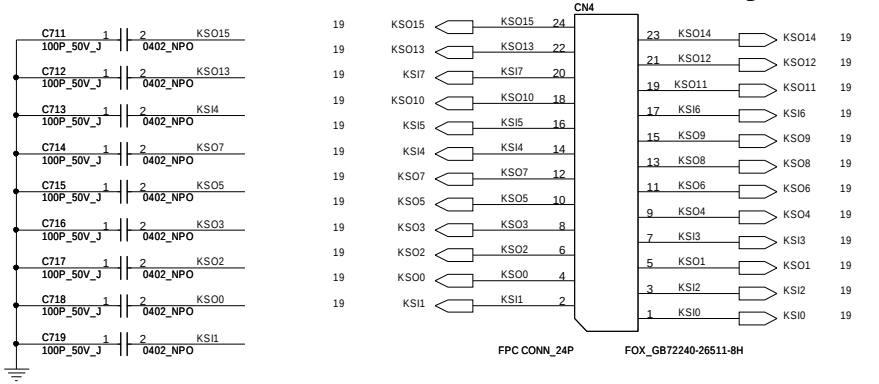
Touch Pad



BFT Test Point for Touch Pad (BOTTOM side)

tpc60b_100	TP100	1	GND
tpc60b_100	TP109	1	LEFT#
tpc60b_100	TP110	1	RIGHT#
tpc60b_100	TP111	1	DAT_TP
tpc60b_100	TP112	1	CLK_TP
tpc60b_100	TP113	1	+5VRUN_TP

Keyboard



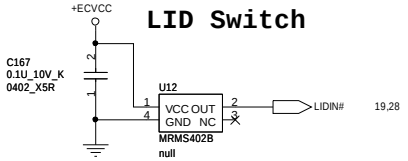
Place these caps close to CN4.

BFT Test Point for Keyboard (BOTTOM side)

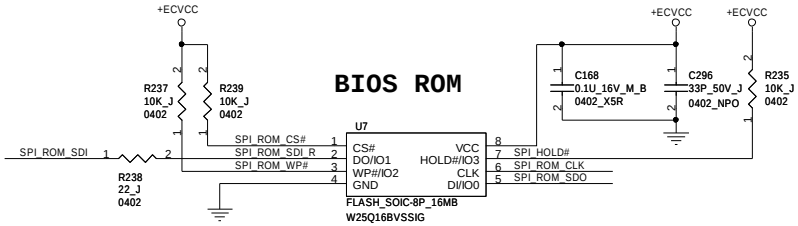
tpc60b_100	TP96	1	KSI4
tpc60b_100	TP97	1	KSO7
tpc60b_100	TP98	1	KSO5
tpc60b_100	TP99	1	KSI2

tpc40t_75	TP101	1	SPI_ROM_CS#
tpc40t_75	TP102	1	SPI_ROM_SDI_R
tpc40t_75	TP103	1	SPI_ROM_WP#
tpc40t_75	TP104	1	GND
tpc40t_75	TP105	1	+ECVCC
tpc40t_75	TP106	1	SPI_HOLD#
tpc40t_75	TP107	1	SPI_ROM_CLK
tpc40t_75	TP108	1	SPI_ROM_SDO

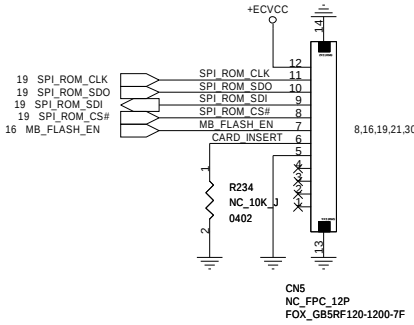
LID Switch



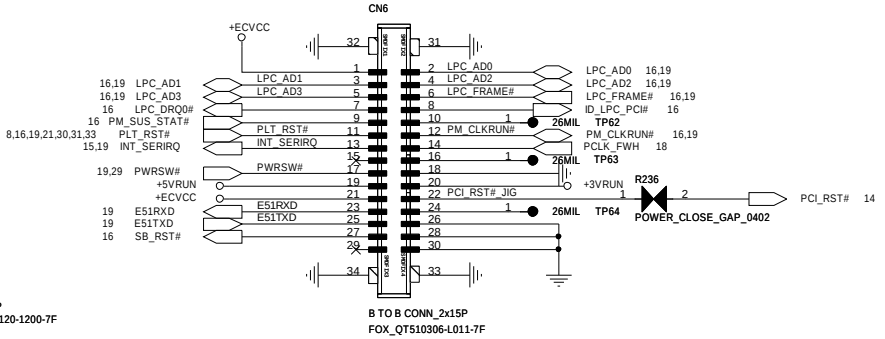
BIOS ROM



EXTERNAL SPI ROM INTERFACE



Debug Port



[redacted]

CCPBG

Title: **KB/TP/Debug Port**

Size	Document Number	Rev
A3	*M9F1*	0.1

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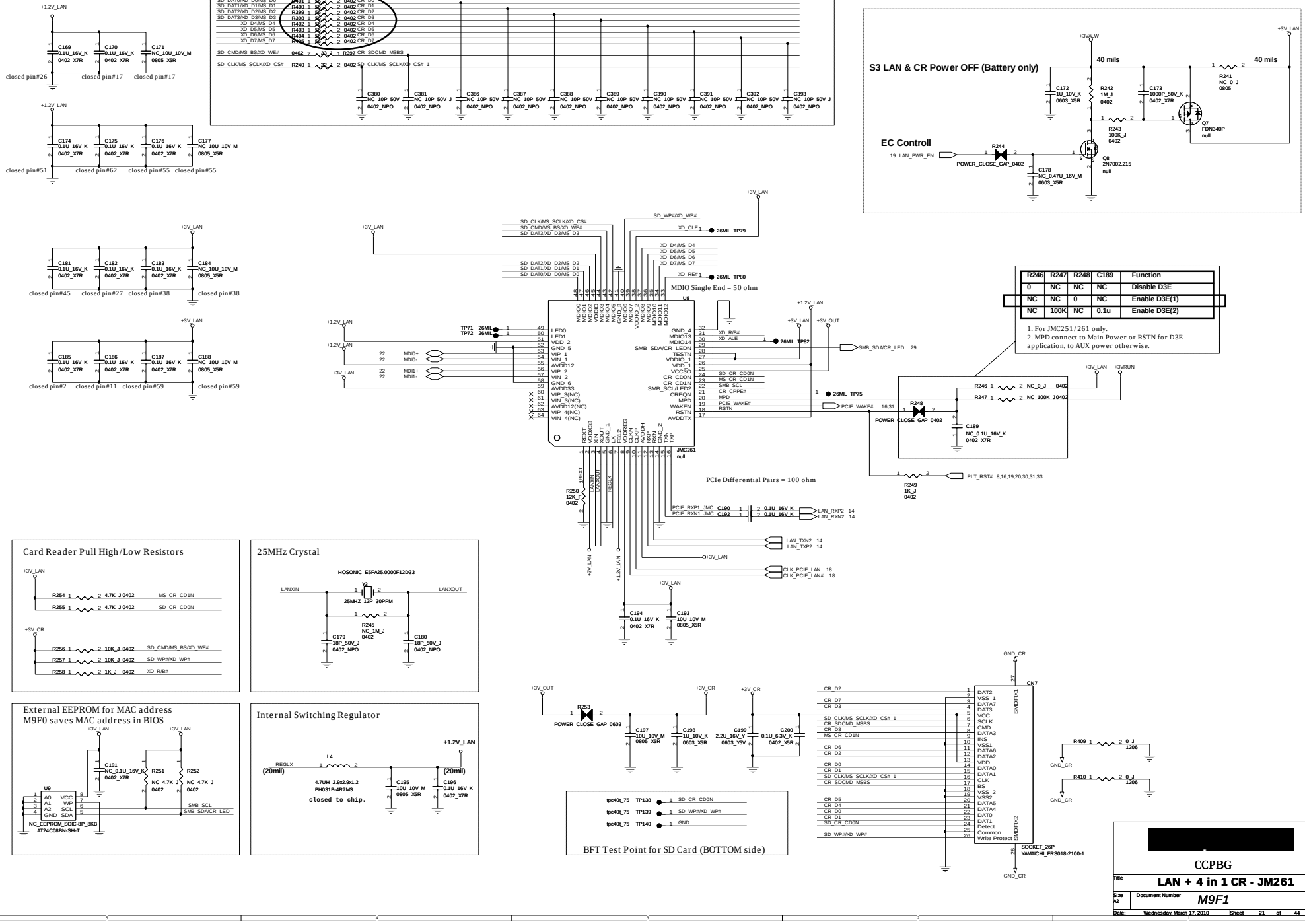
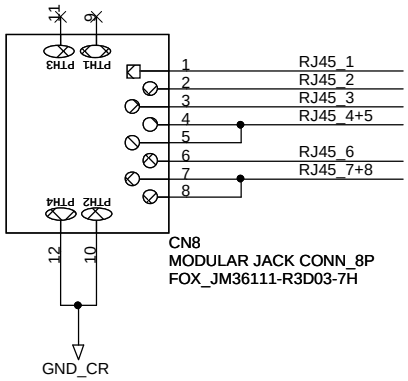
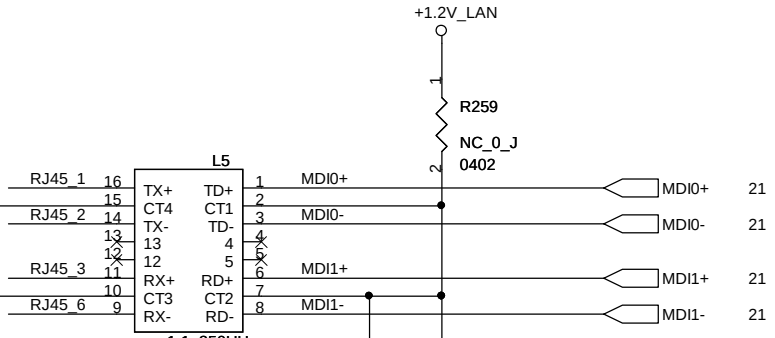


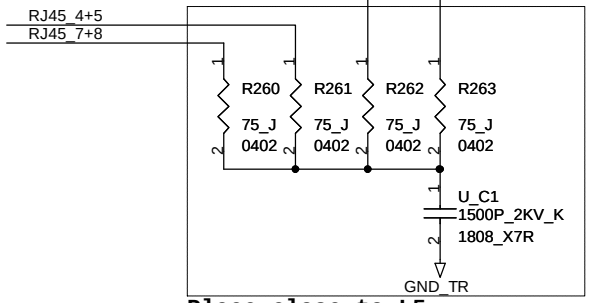
R246	R247	R248	C189	Function
0	NC	NC	NC	Disable D3E
NC	NC	0	NC	Enable D3E(1)
NC	100K	NC	0.1u	Enable D3E(2)

1. For JMC251/261 only.
2. MPD connect to Main Power or RSTN for D3E application, to AUX power otherwise.

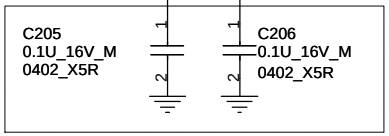


Zdiff = 100 Ohm





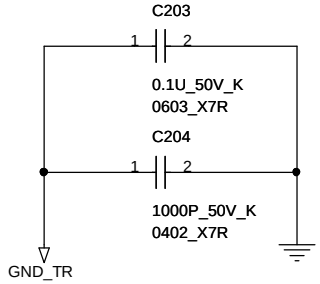
Place close to L5



C205, C206 close to Pin2, Pin7 of L5 each

BFT Test Point for RJ45 (BOT side)

tpc40t_75	TP153	1	RJ45_1
tpc40t_75	TP154	1	RJ45_2
tpc40t_75	TP155	1	RJ45_3
tpc40t_75	TP156	1	RJ45_4+5
tpc40t_75	TP157	1	RJ45_6
tpc40t_75	TP158	1	RJ45_7+8



[redacted]

CCPBG

Title: **Transformer & RJ45**

Size	Document Number	Rev
A4	*M9F1*	0.1

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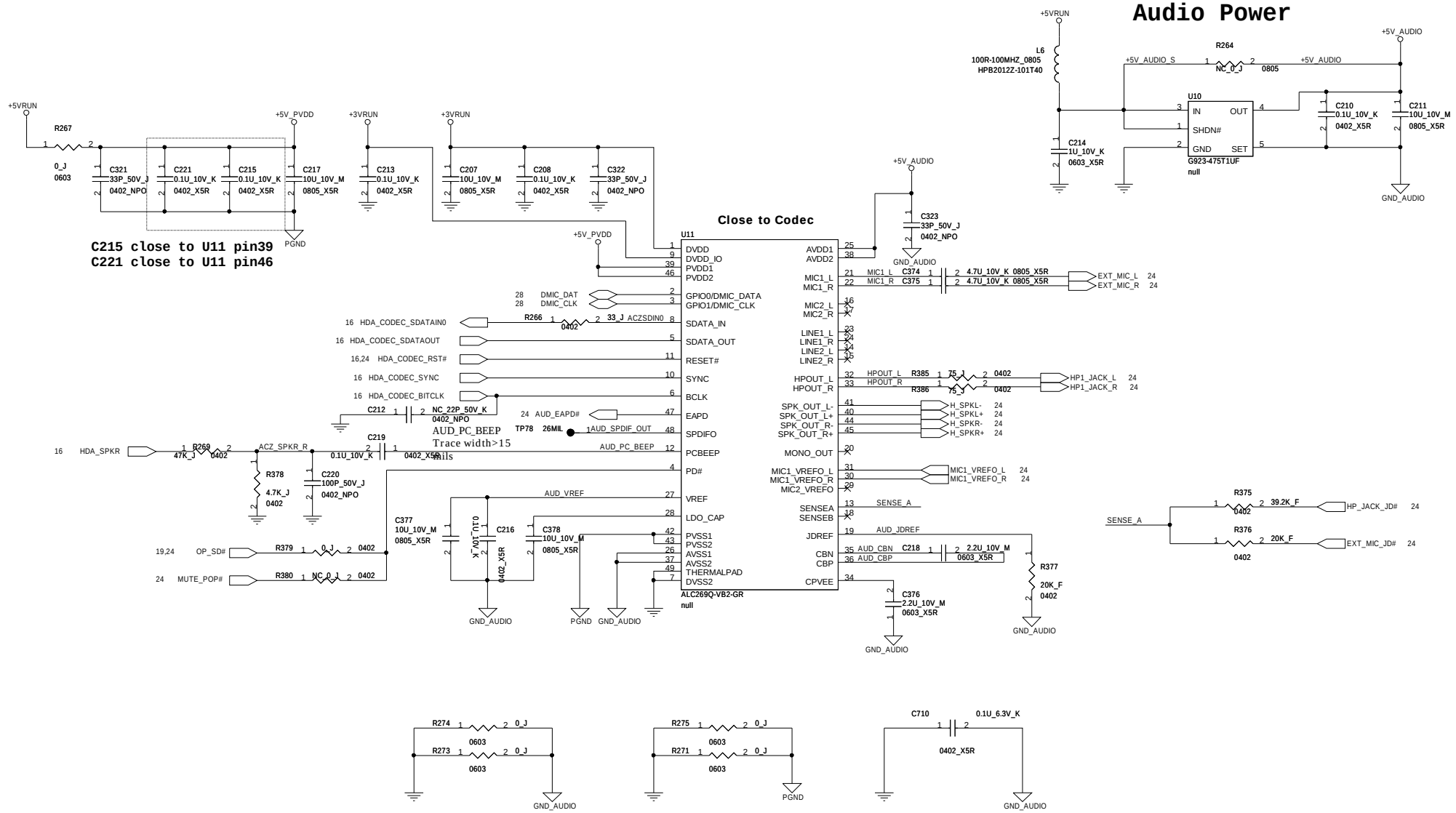
Audio Power



[redacted]
CCPBG

Title	**Audio Codec ALC269Q**	
Size A3	Document Number *M9F1*	Rev 0.1
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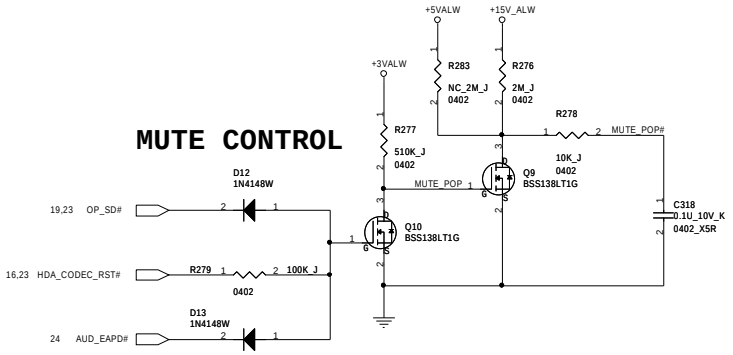
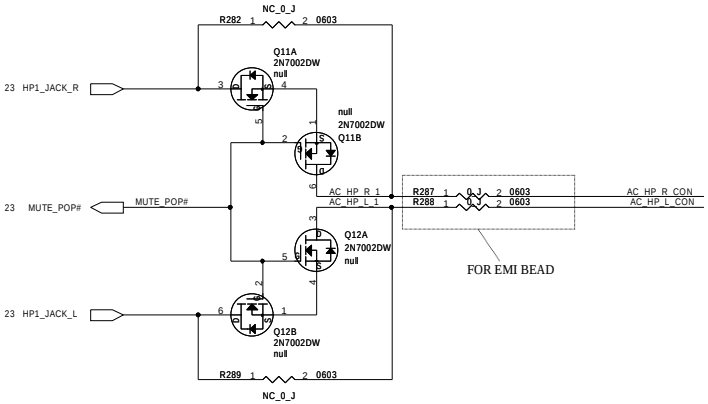
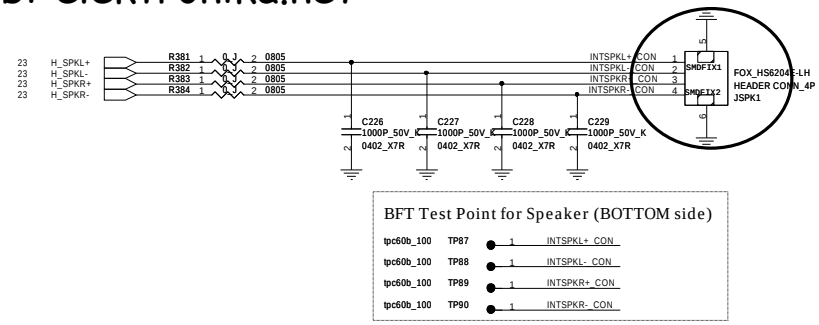
MUTE CONTROL

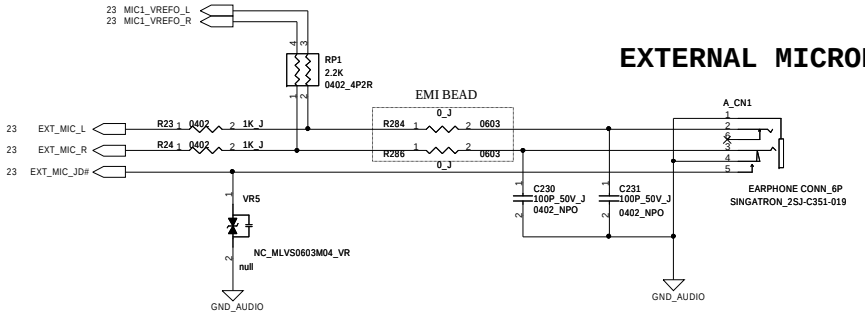


HP CONN

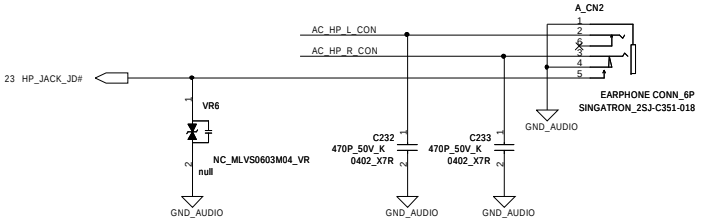




EXTERNAL MICROPHONE



HEADPHONE



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CCPBG

Title	MIC & Audio Jack	
Size: Custom	Document Number: M9F1	Rev: 0.1
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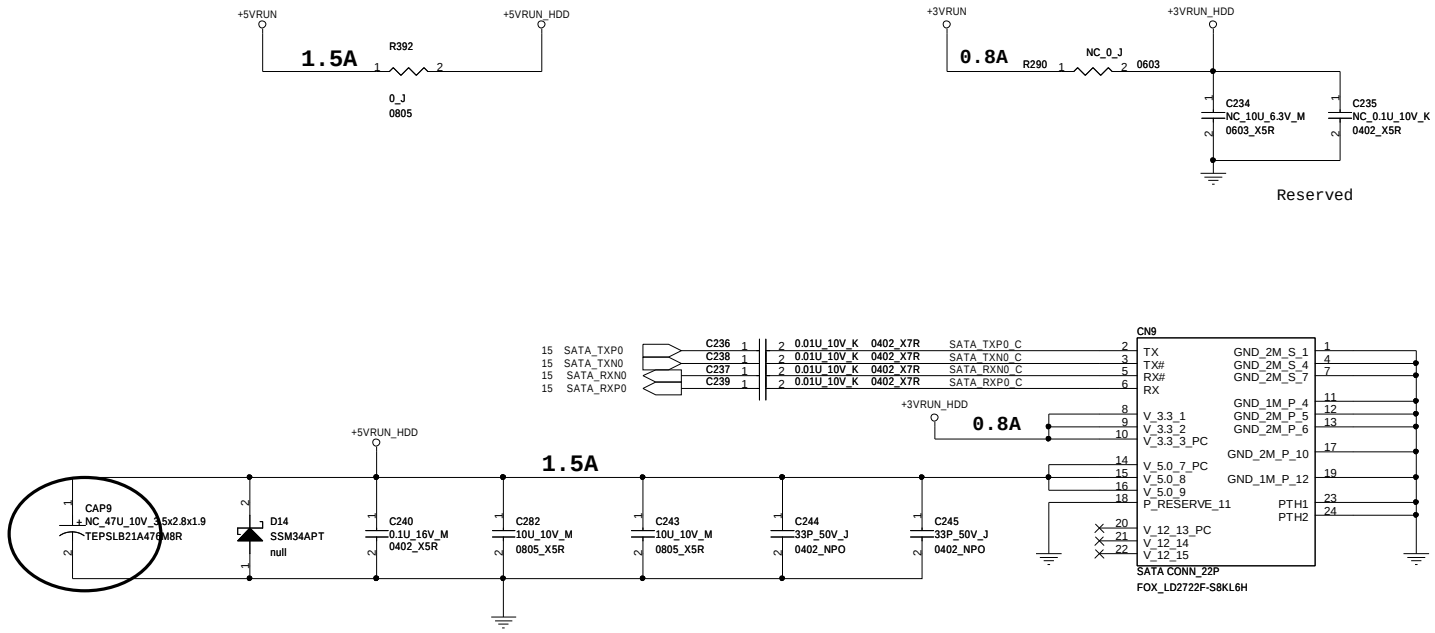

SATA HDD CONN.

[redacted]

CCPBG

Title	SATA HDD	
Size A3	Document Number M9F1	Rev 0.1
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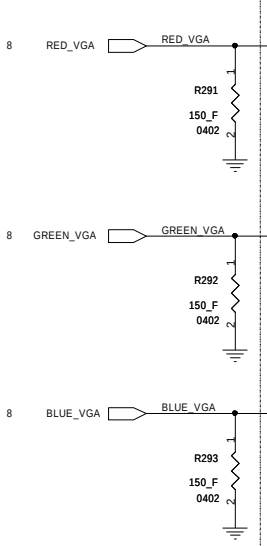
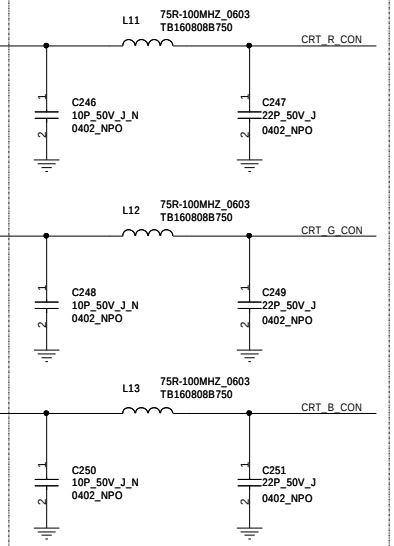
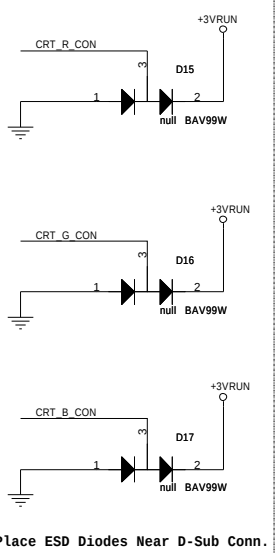
Terminal Resistor



Filter Circuit (1 pole)

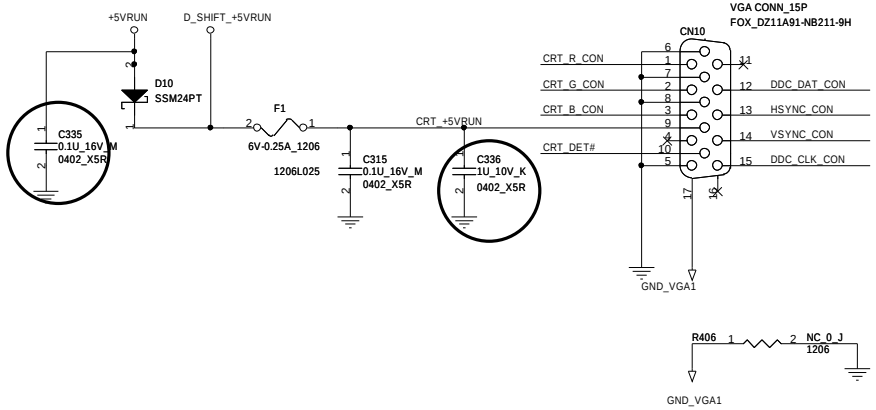


ESD Protection Circuit



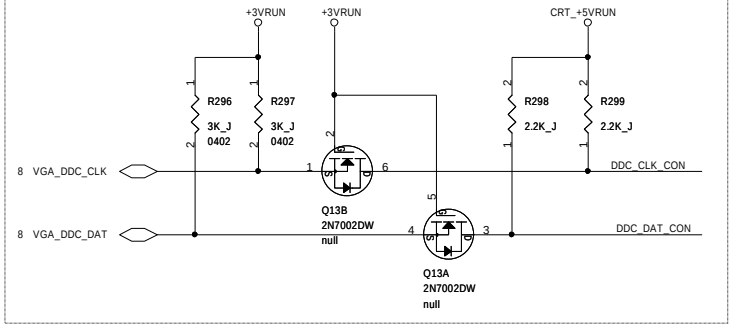
Place ESD Diodes Near D-Sub Conn.

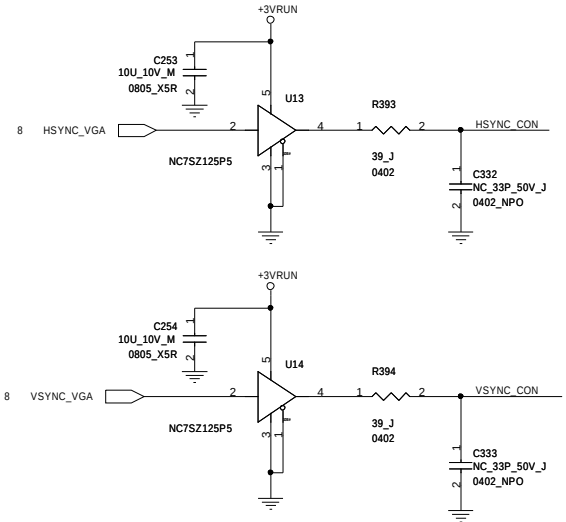
RGB routing
1. from SCH to the first 150 ohm resistor: 12 mils(min. 6 mils spacing)
2. from the first 150 ohm res. to the second 150 ohm resistor: 7 mils
3. from the second 150 ohm resistor to connector: 4 mils
4. spacing minimum 6 mils, 30 mils spacing is recommended
5. R,G,B should be length matched to 200 mils, max. length is 8400 mils
6. R,G,B signals should be ground referenced

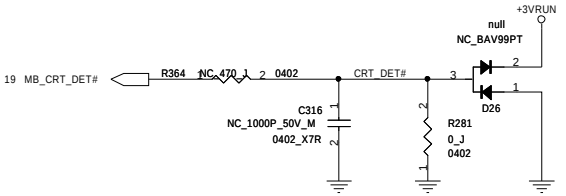


The 150 Ohm resistors near VGA connector and minimizing length to filter. The filters to VGA connector maximum distance 800 mils.

Level Shifter for DDC BUS







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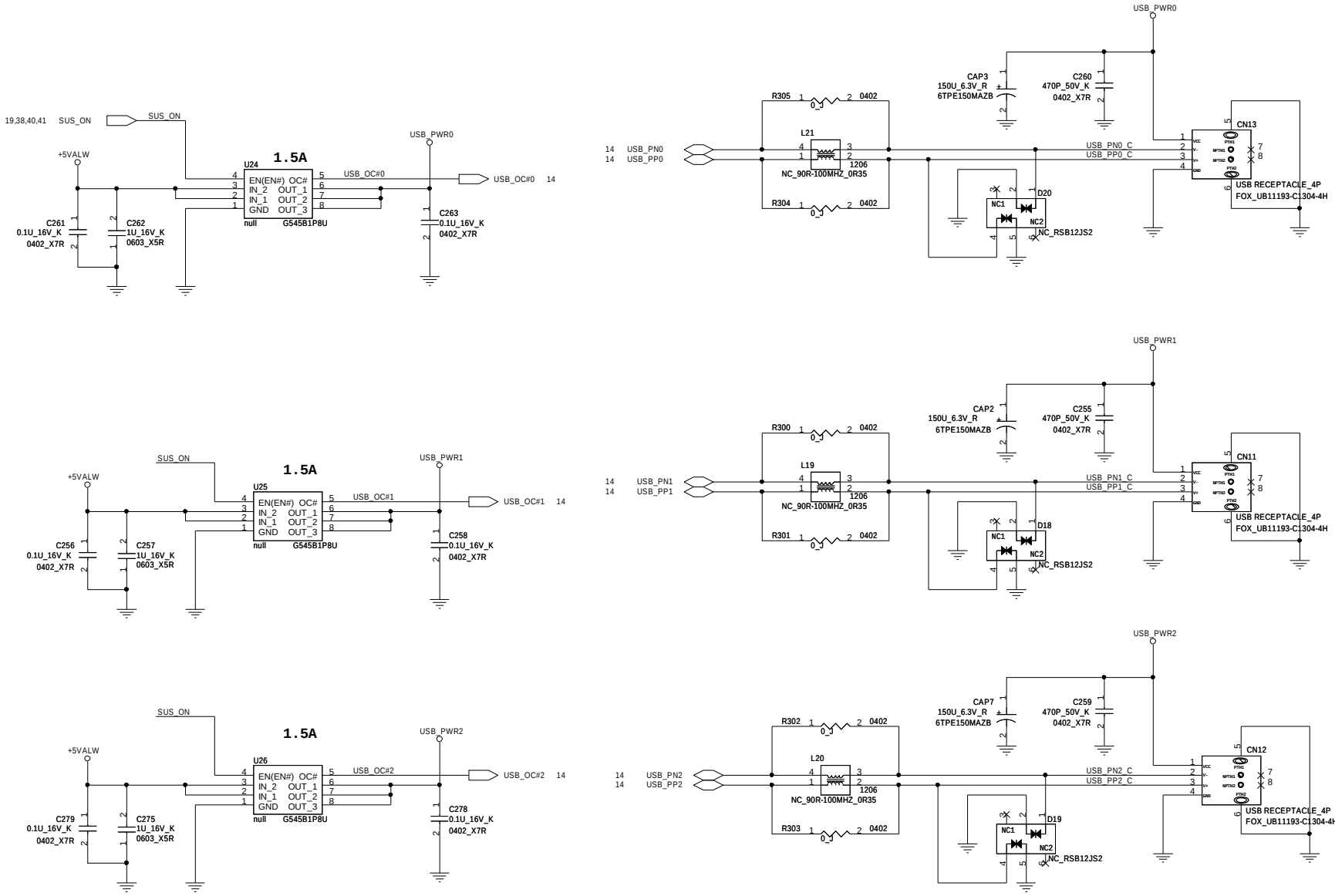
CCPBG

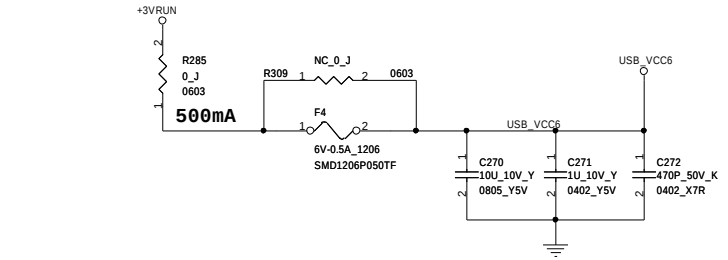
Title	VGA Connector (D-Sub)	
Size A3	Document Number M9F1	Rev 0.1
Date: Wednesday, March 17, 2010	Sheet 26 of 44	



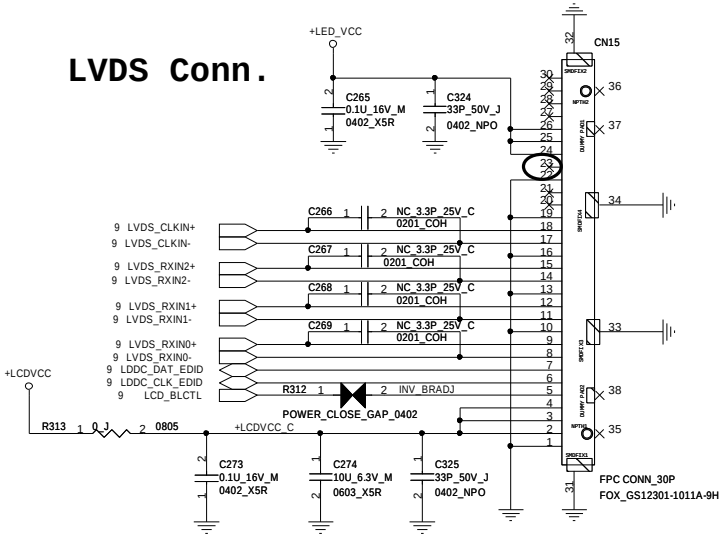
[redacted]

CCPBG

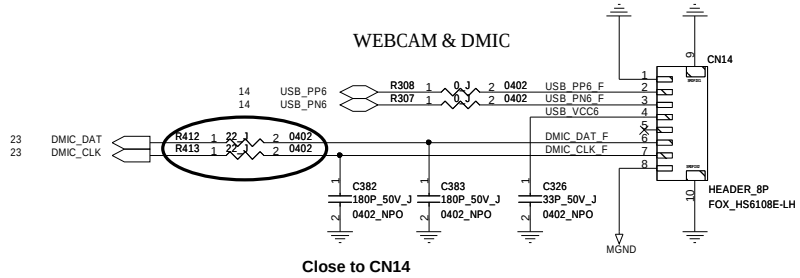
Title	**USB Connector x 3**	
Size: Custom	Document Number: *M9F1*	Rev: 0.1
Date: Wednesday, March 17, 2010	Sheet 27 of 44	



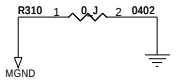
LVDS Conn.



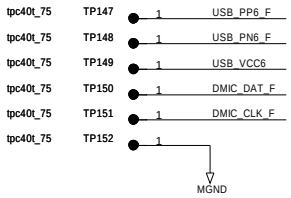
WEBCAM & DMIC



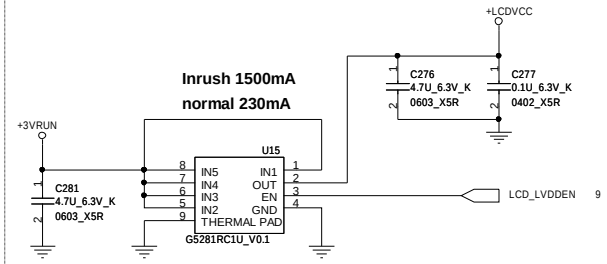
Close to CN14



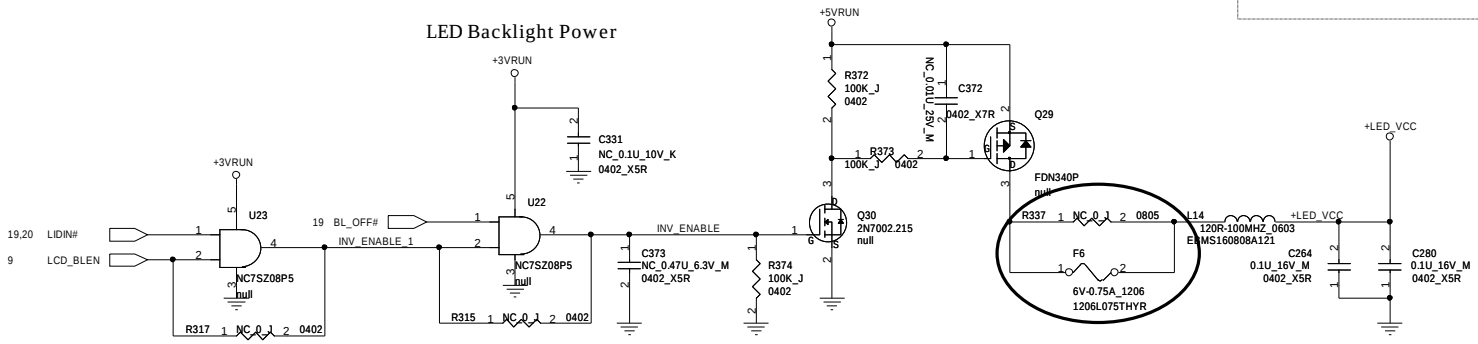
BFT Test Point for Camera (BOTTOM side)



LCD Core Power



LED Backlight Power



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CCPBG

LVDS & WEBCAM

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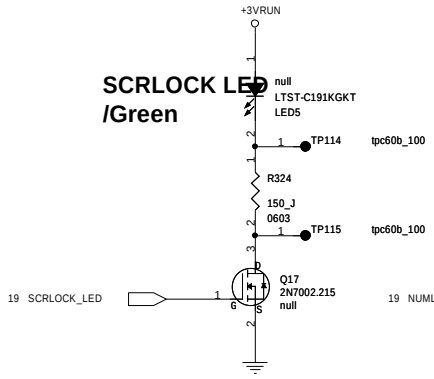
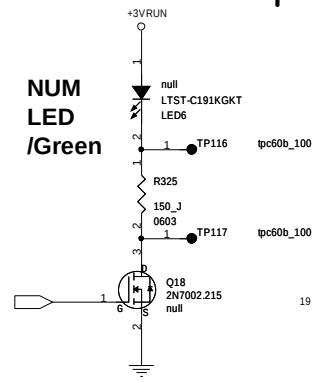
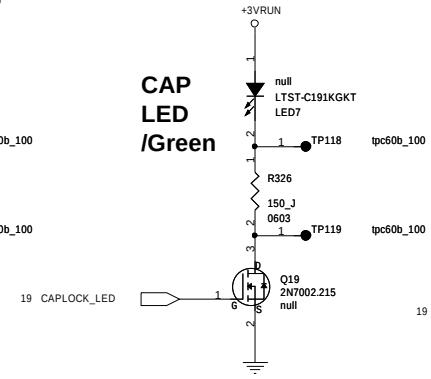
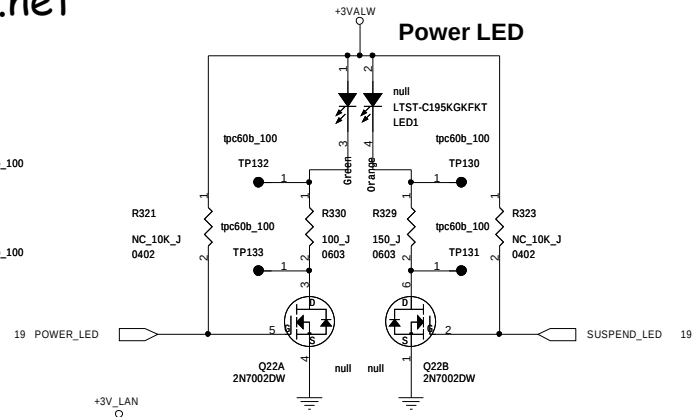
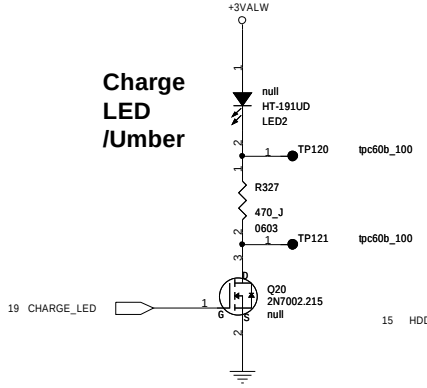
http://hobi-elektronika.net

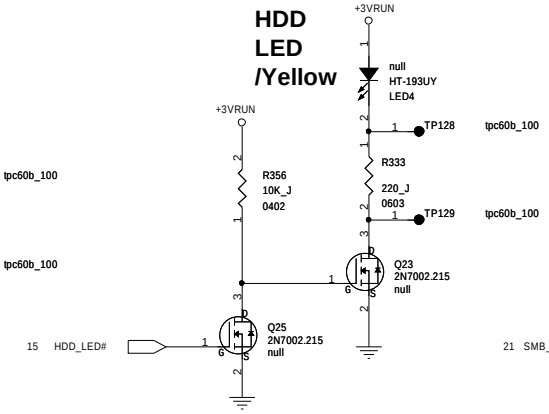


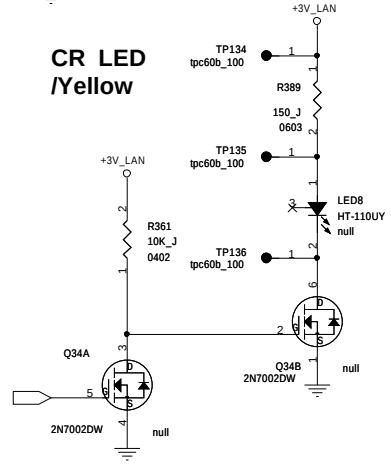


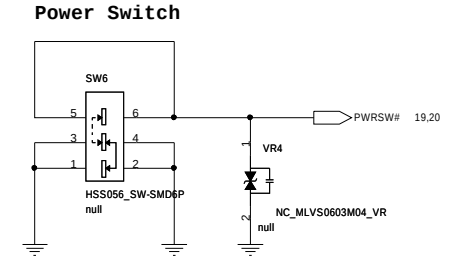


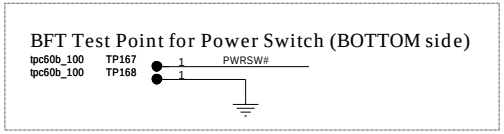


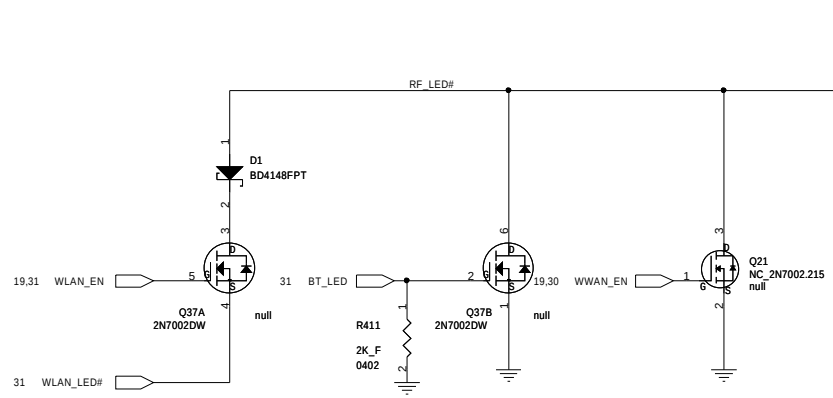


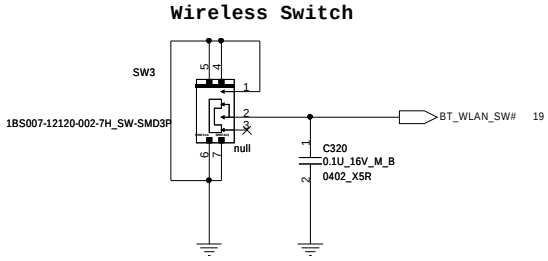












[redacted]

CCPBG

Title: **Power Switch & LED**		
Size: A3	Document Number: *M9F1*	Rev: 0.1
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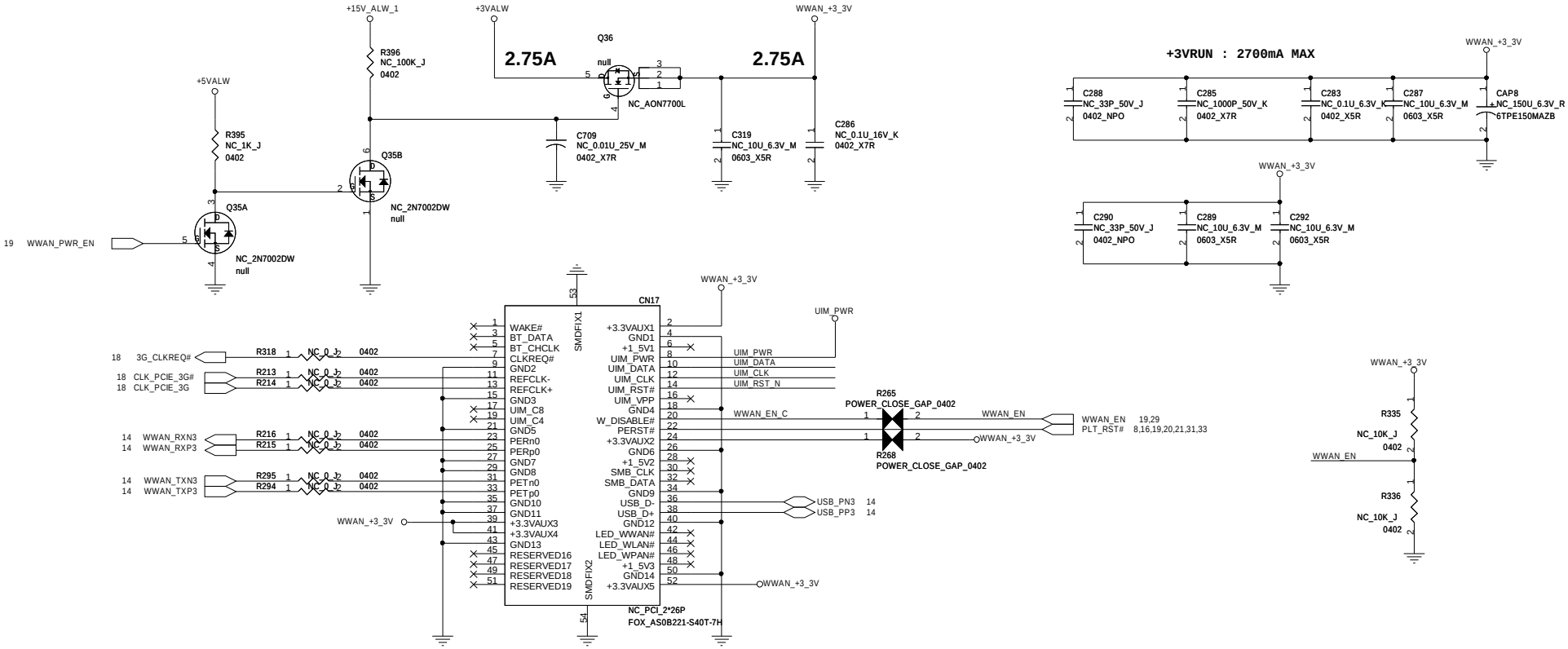
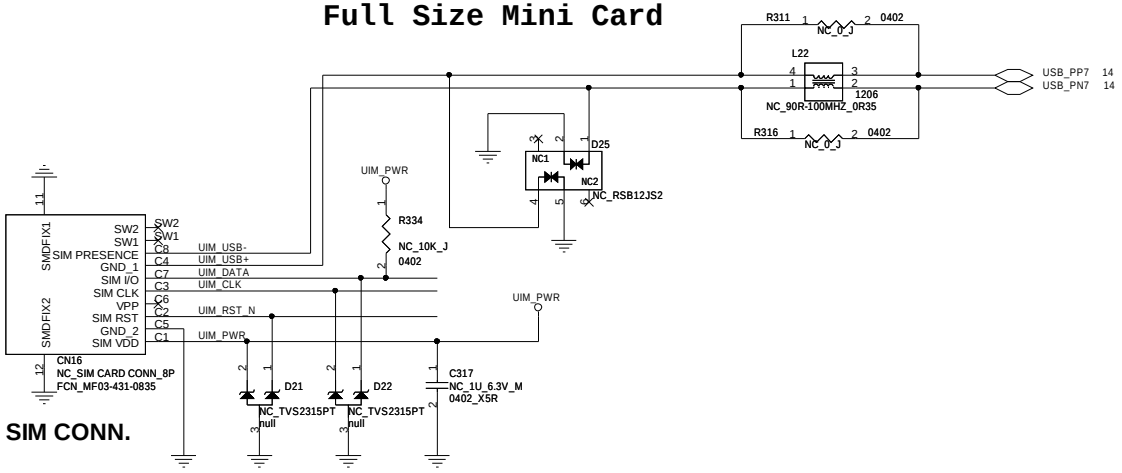
For M9F0 MP, these components are NC in this page.



Full Size Mini Card



SIM CONN.

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CCPBG

Title	Mini PCIE - 3G		
Size A3	Document Number M9F1		Rev 0.1
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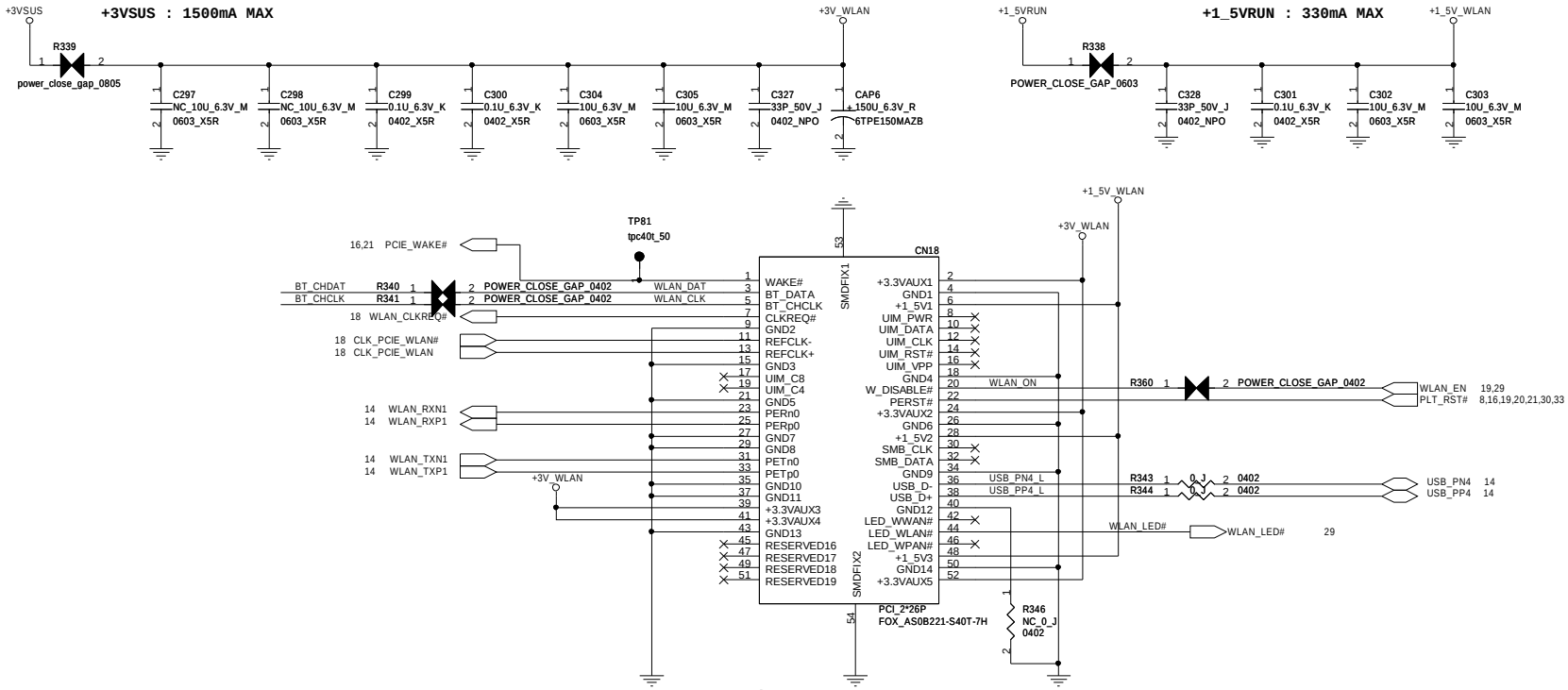
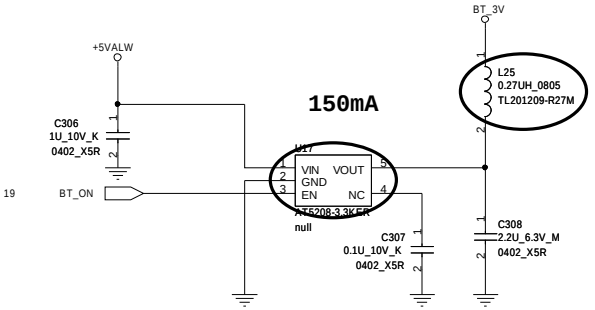
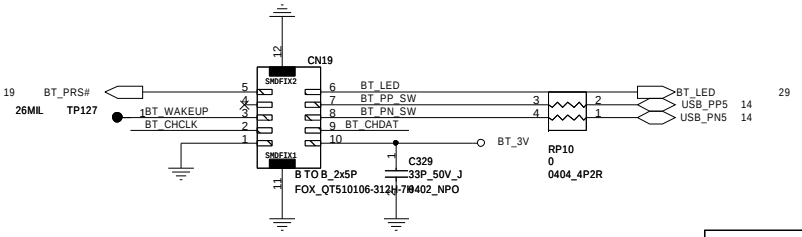
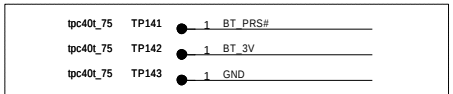


Half Size Mini Card



Bluetooth CONN.





BFT Test Point for Bluetooth (BOTTOM side)

[redacted]

CCPBG

Title	Mini PCIE - WIFI & BT	
Size: Custom	Document Number: M9F1	Rev: 0.1
Date: Wednesday, March 17, 2010	Sheet 31 of 44	

[redacted]

CCPBG

Title	**Reserved**	
Size A3	Document Number *M9F1*	Rev 0.1
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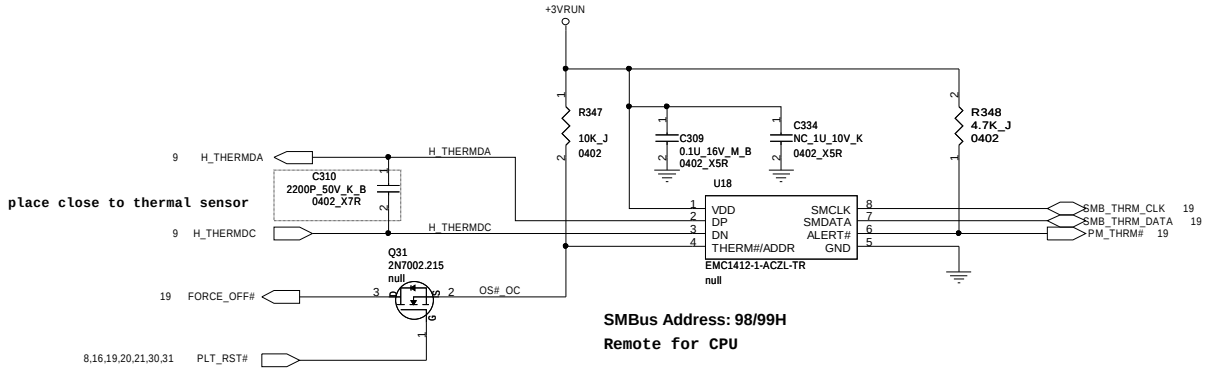
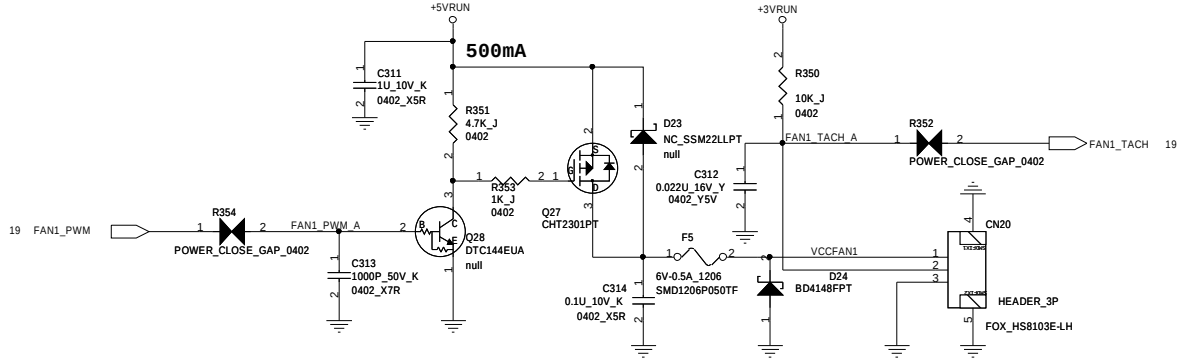
CPU Thermal Sensor



FAN



BFT Test Point for FAN (BOT side)

tpc60b_100	TP83	1	VCCFAN1
tpc60b_100	TP84	1	FAN1_TACH_A
tpc60b_100	TP85	1	
tpc60b_100	TP86	1	FAN1_PWM_A

[redacted]

CCPBG

Title: **Thermal & Fan**

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A3	*M9F1*	0.1

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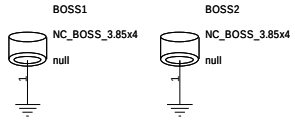
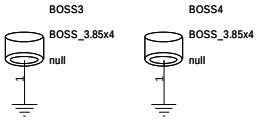
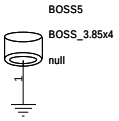


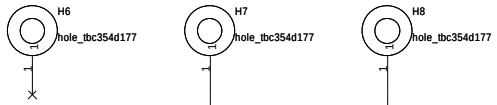
BOSS for WWAN

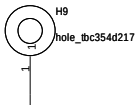


BOSS for WLAN

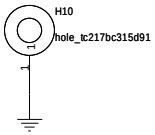


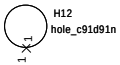
BOSS for Thermal Module





Screw Hole for Thermal Module





Bluetooth

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Title
ME NUT & EMI

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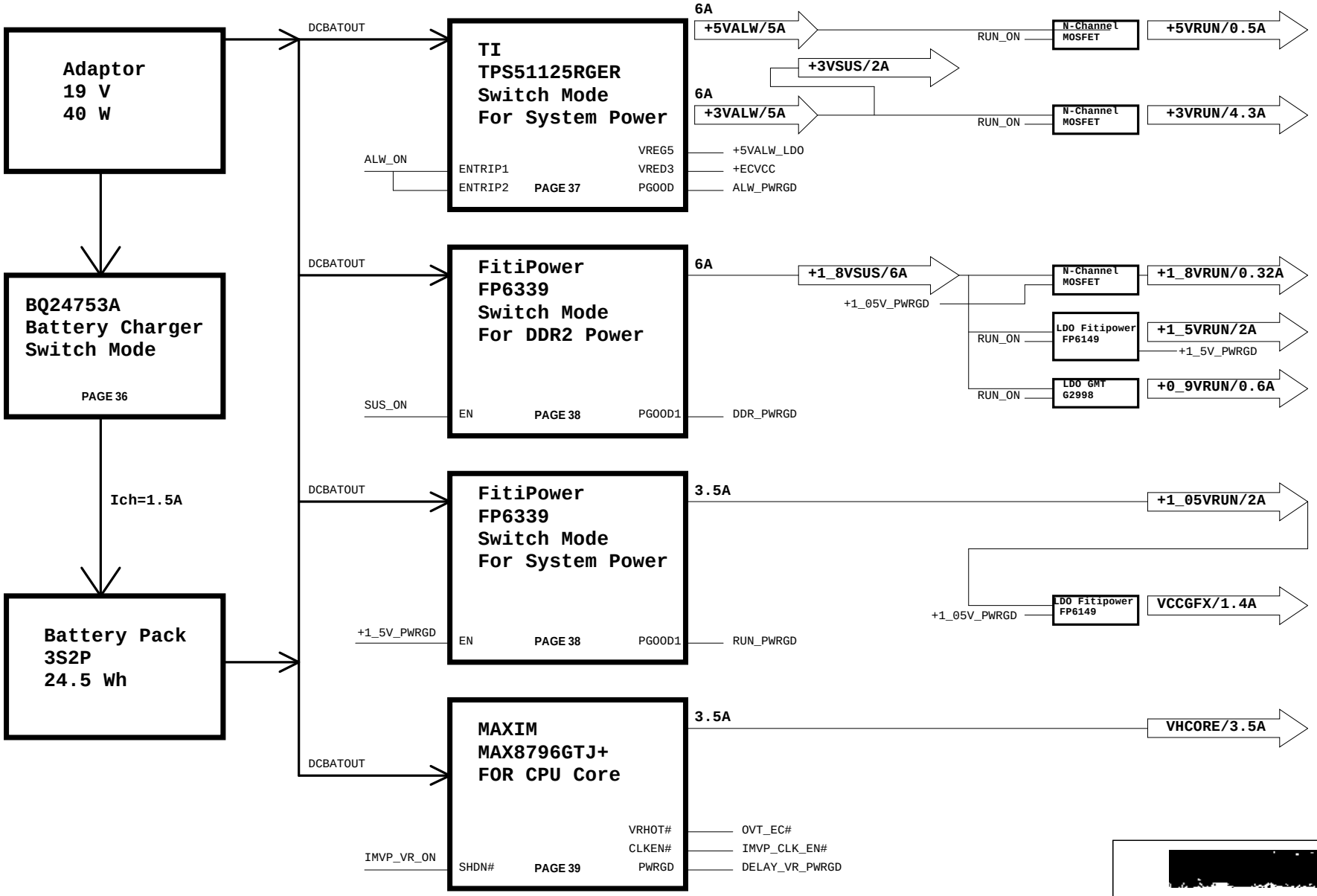
M9F1 Power Block Diagram



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Title	Power Block Diagram	
Size A3	Document Number M9F1	Rev 0.1
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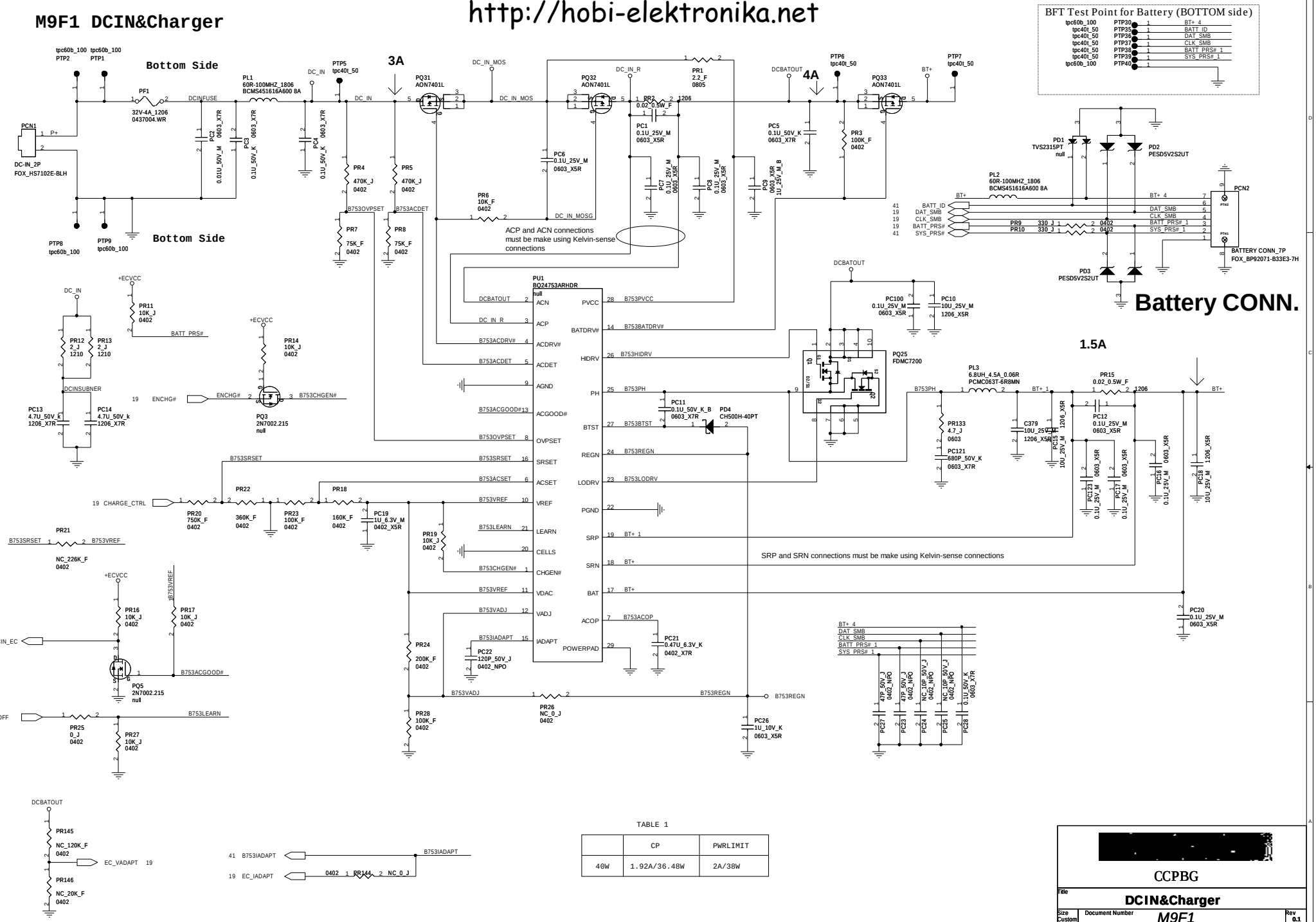
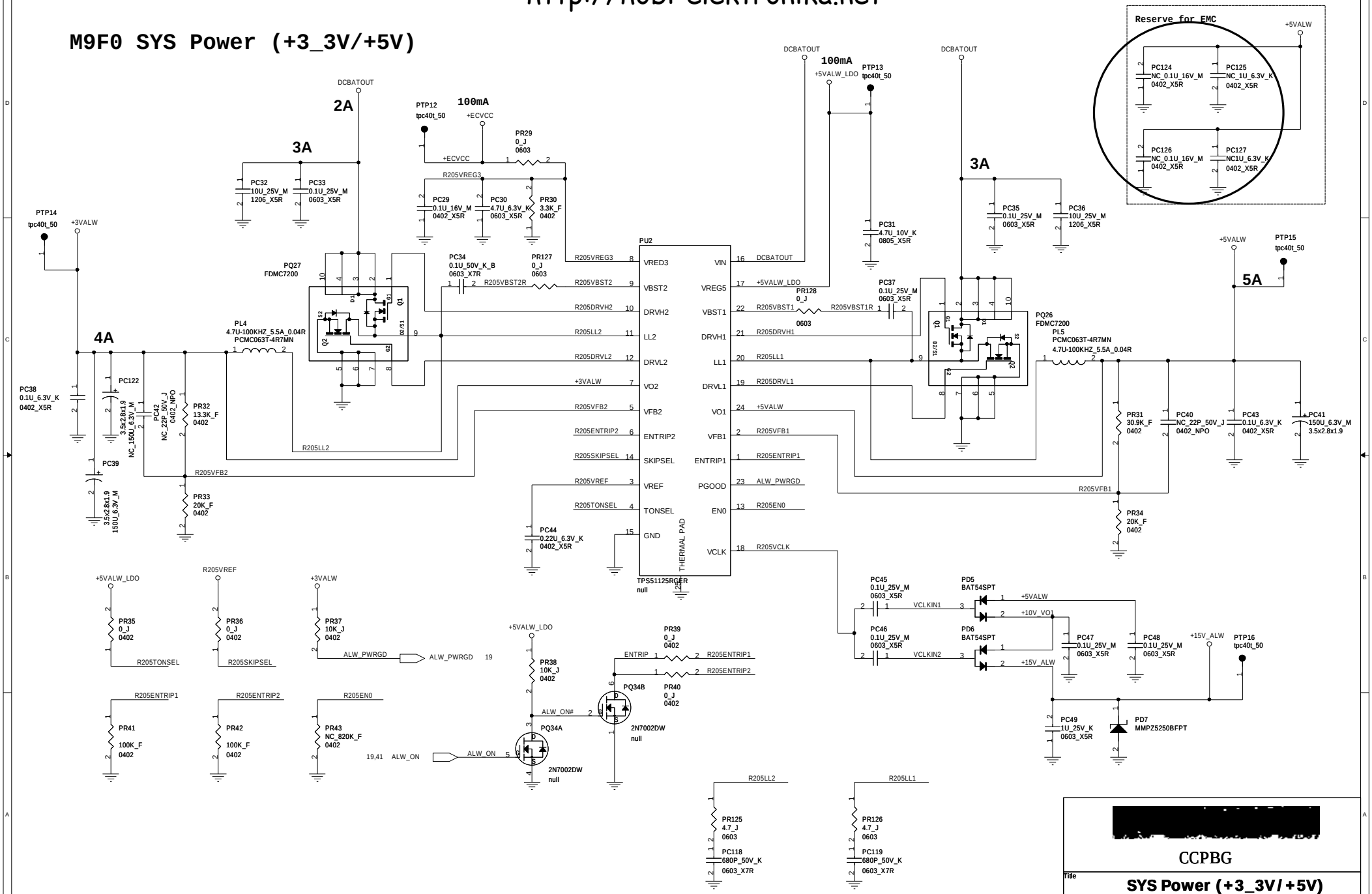
M9F1 DCIN&Charger

http://hobi-elektronika.net



M9F0 SYS Power (+3_3V/+5V)



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Title	SYS Power (+3_3V/+5V)	
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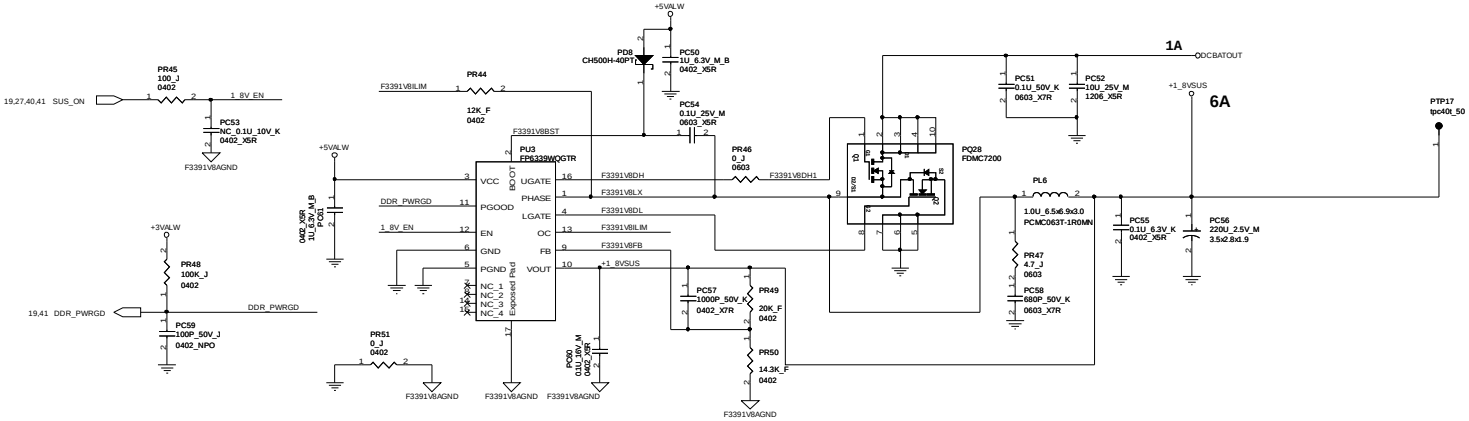
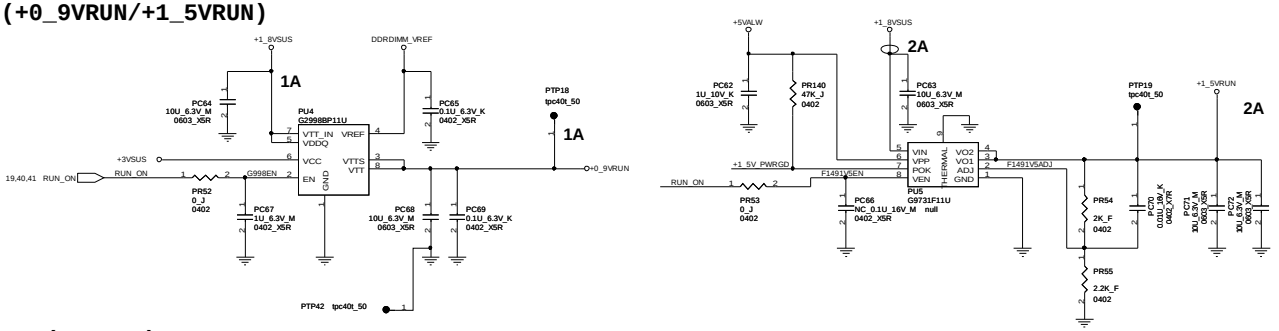
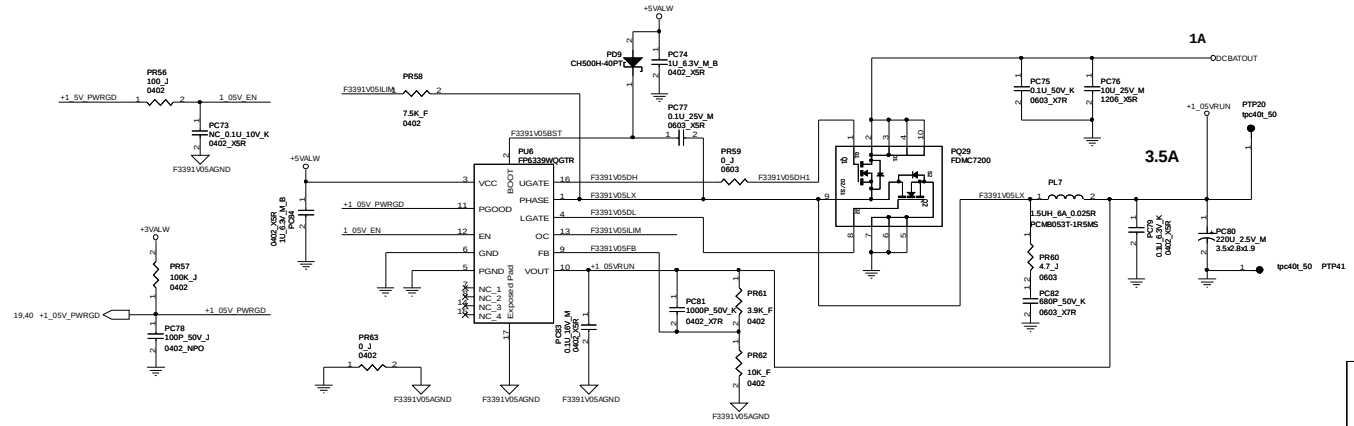
M9F1 SYS Power(+1_8VSUS)



M9F1 SYS Power(+0_9VRUN/+1_5VRUN)



M9F1 SYS Power(+1_05V)



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Title	SYS Power(+1_8V/+1_05V)	
Size A2	Document Number M9F1	Rev 0.1
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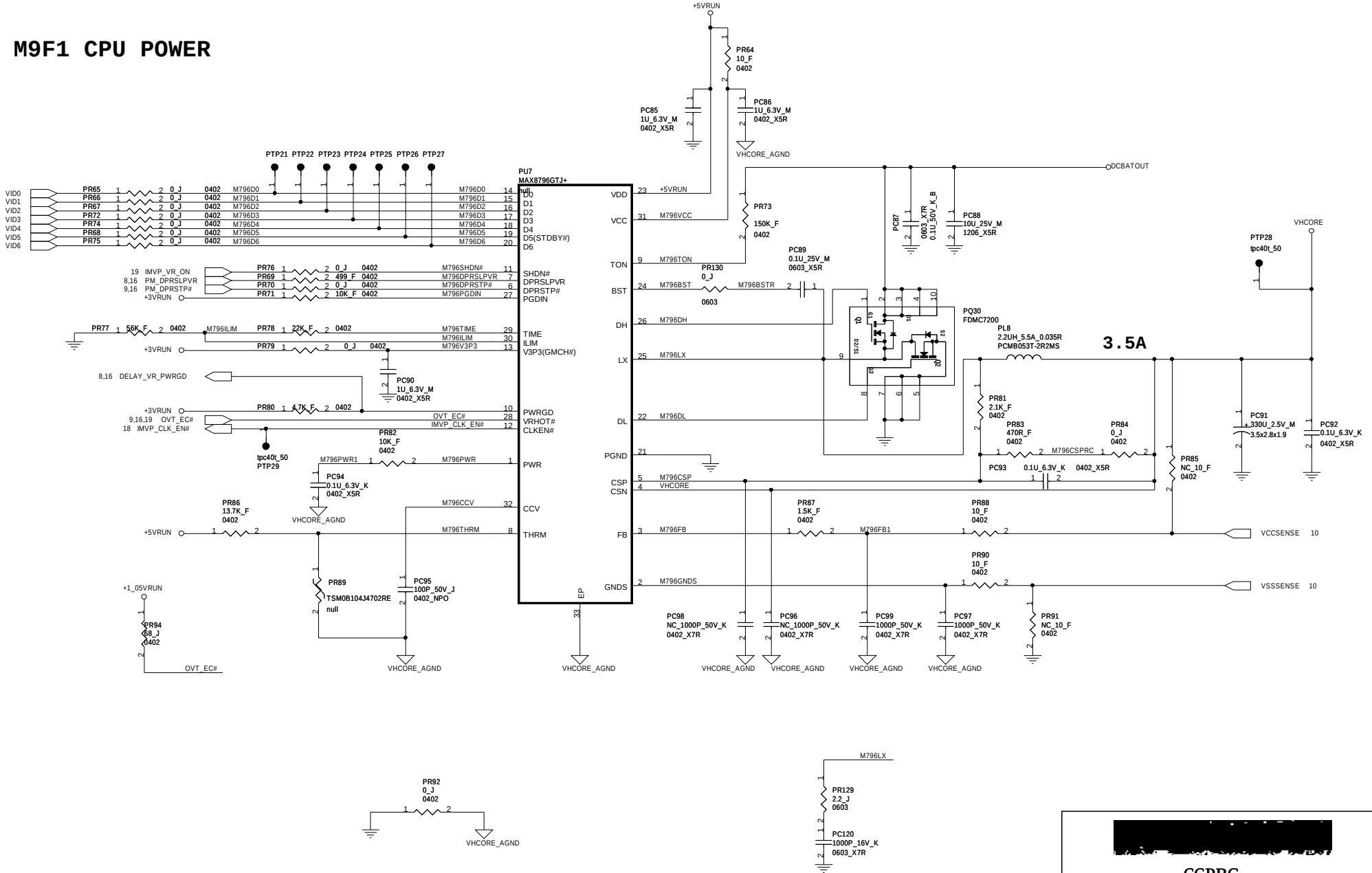
M9F1 CPU POWER



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Title	CPU POWER	
Size A3	Document Number M9F1	Rev 0.1
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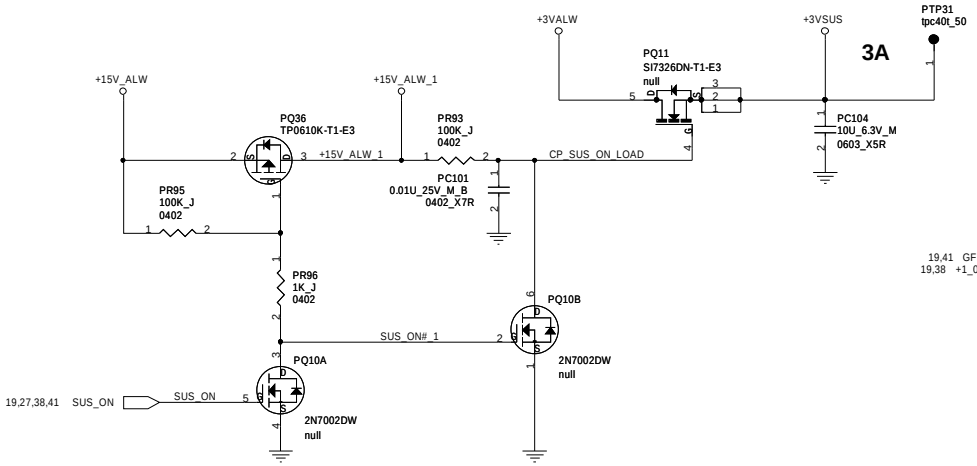
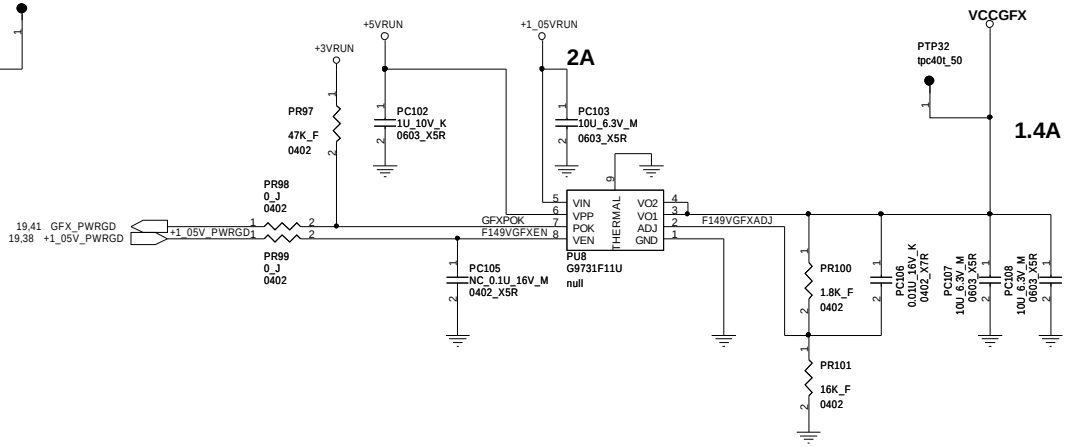
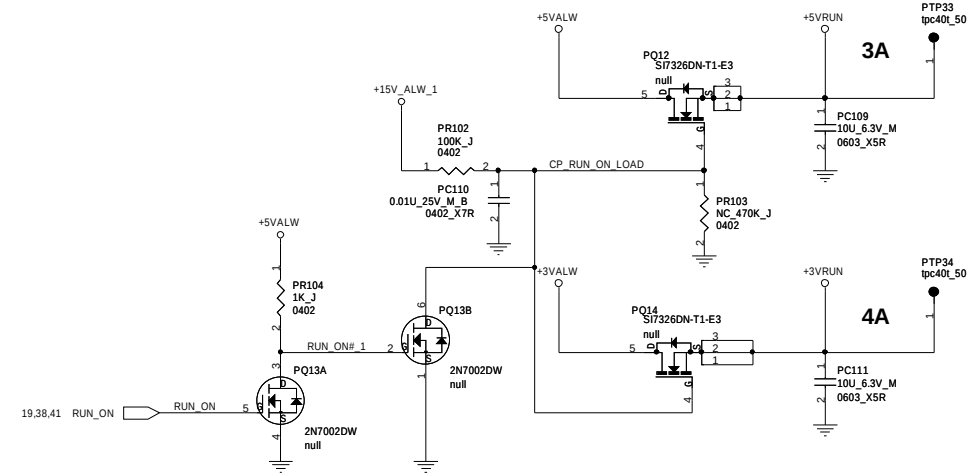
M9F1 Others power plan (+3VSUS)



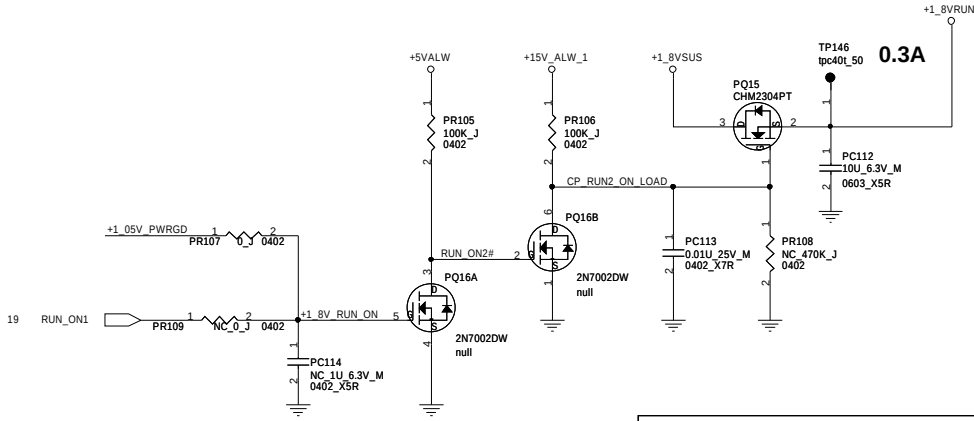
M9F1 GFX Power (VCCGFX/+0.89V)



M9F1 Others power plan (+5VRUN/+3VRUN)



M9F1 Others power plan (+1_8VRUN)



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Title	**Others power plan**	
Size: Custom	Document Number: *M9F1*	Rev: 0.1
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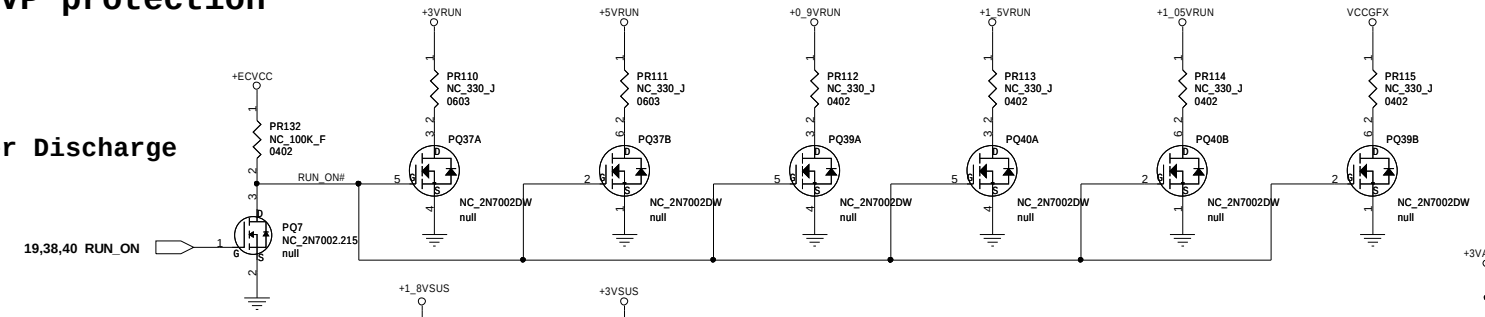
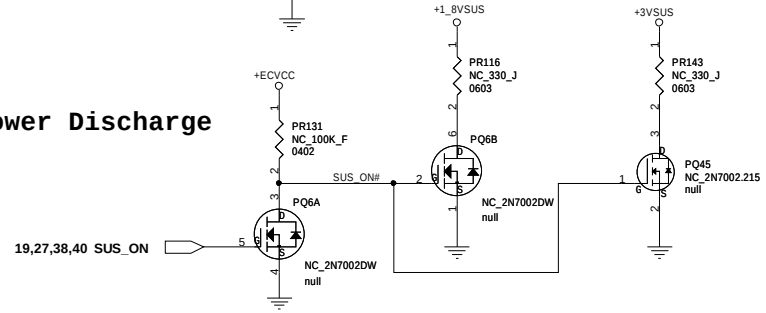
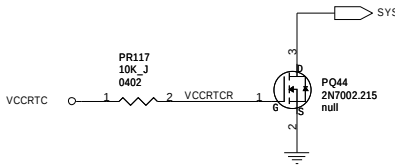
M9F1 OVP protection

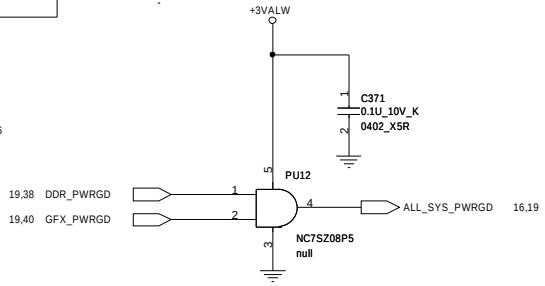
S0 Power Discharge



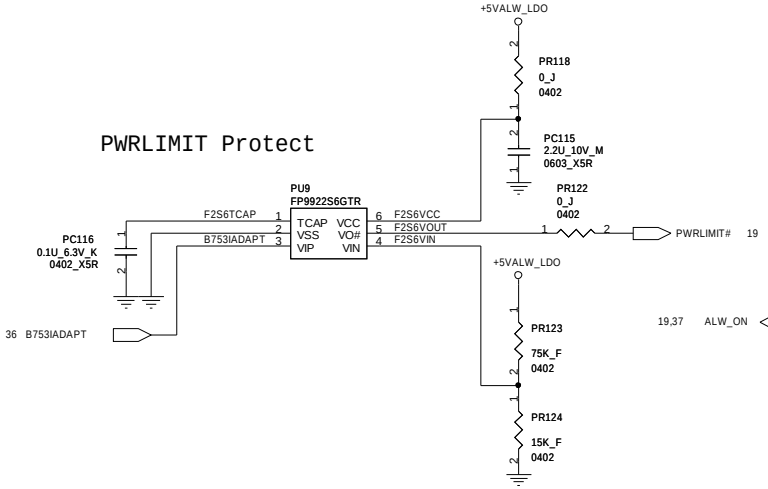
S3 Power Discharge

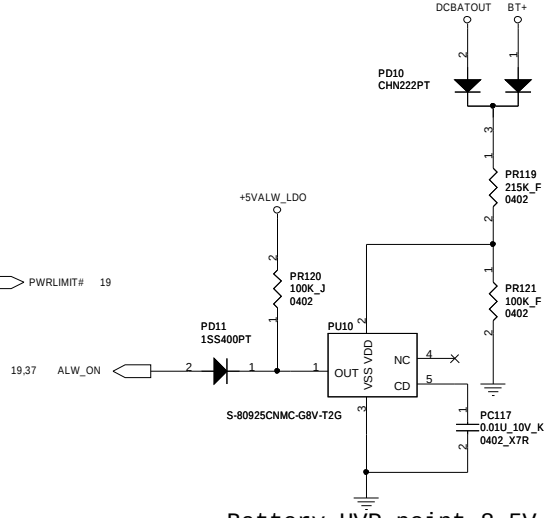




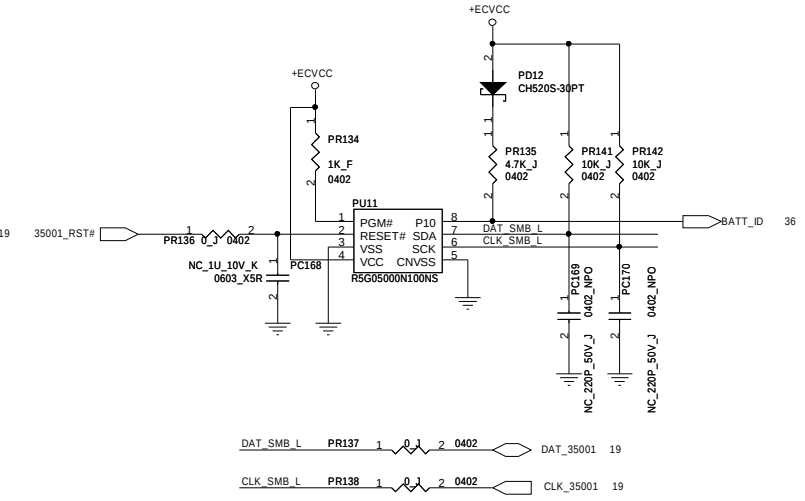


PWRLIMIT Protect





Battery UVP point 8.5V



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Title: OVP protection		
Size: A3	Document Number: M9F1	Rev: 0.1
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M9F1 EVT

2010/01/27

1. P22, Remove net "GND_VGA" and make CN8.9 & CN8.11 no connect
2. P26, Remove net "GND_VGA" and make CN10.16 no connect
3. P26, Delete R407

2010/02/01

1. P21, Change R409 and R410 footprints from 0805 to 1206.
2. P26, Change R406 footprint from 0805 to 1206.

2010/02/02

1. P28, Add U23, Reserve R317 for Lid Switch control LVDS backlight.
2. P19, Delete RF_LED#.
3. P29, Add Q37, D1, Q3, Reserve D2, R411 for wireless LED.
4. P30, Add WWAN_LED#.
5. P31, Delete TP91, TP126.
6. P34, Unconnect H6 to GND.
7. P36, Add PR139, PR144 for powerlimit EC control.
8. P41, NC PC116, PU9, PR118, PC115, PR122, PR123, PR124 for powerlimit EC control.
9. P19, Add C720.
10. P40, Change PQ11, PQ12, PQ14 to SI7326DN-T1-E3.
11. U39 Co-layout with U12.

2010/02/03

1. P19, Add C721.
2. P36, Add PR145, PR146.
3. P36, Change PR18 to 160K.
4. P19, Change EC_VADAPT to U5.100, BT_WLAN_SW# to U5.124.
5. P21, Reserve C381, C386, C387, C388, C389, C390, C391, C392, C393.
6. P29, Delete D2.
7. P30, Delete WWAN_LED#.
8. P37, Stuff PC39, NC PC122.
9. P28, NC CN15.32, CN15.34.

2010/02/04

1. P29, Change R411 to 100K.

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Title: EVT Change Note			
Size: A3	Document Number: M9F1		Rev: 0.1
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M9F1 DVT

2010/02/05

1. P26, Change U13, U14 to 14-NC7S212-5P00.

2010/02/10

1. P19, Add R233 to reserve one GPIO for BT_WLAN_SW# (default NC, use U5.100 to be wireless switch)
2. P19, Add R357 and R359 to reserve U5.100 for wireless switch and power limit (default R357 is 0ohm and R359 is NC)
3. P19, set C720 and C721 to be NC.
4. P16, stuff PU9, PC116, PR118, PC115, PR123 and PR124 for hardware power limit
5. P41, Set R136 and R138 to be NC, and set R270 and R272 to be 10K. MB ID = 00 for M9F1

2010/02/22

1. P20, Delete U39
2. P28, CN15.32 and CN15.34 connects to GND.
3. P16, Change CN2 to 1N-0002009-M1T0.
5. P34, Delete SPR1.
6. P36, Change PCN2 to 2N-000700Y-MKG0.
7. P29, Change R411 to 2K.

2010/02/23

1. P41, NC PR132, PR110, PR111, PR112, PR113, PR114, PR115, PR131, PR116, PR143, PQ7, PQ37, PQ39, PQ40, PQ6, PQ45.

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Title	**DVT Change Note**	
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M9F1 PVT

2010/03/11

1. P24, Change JSPK1 to 1N-000400C-M1T0.
2. P31, Change U17 to 15-AT52083-0000, change R358 to L25 .
3. P20, Change CN3 to 1N-0006004-FXT0.
4. P28, Change CN15.23 from GND to NC.
5. P28, Change L23, L24 to R412, R413.
6. P36, Delete PR139.
7. P19, Change R357 to close jump.
8. P26, Add C335, C722.
9. P21, Change R398, R399, R400, R401, R402, R403, R404, R405 to 56ohm.

2010/03/12

1. P19, Stuff R342, R345 for system ID.
2. P25, Reserve CAP9.
3. P10, Reserve D34, D35, D36.

2010/03/15

1. P26, C722 change to C336
2. P24, JSPK1 changes net name for speaker pin compatible
3. P37, Add PC124, PC125, PC126 and PC127 for EMC
4. P18, Add R390, R391.
5. P25, Change CAP9 to 1C-44R0476-M200.
6. P21, Change R409, R410 to stuff.

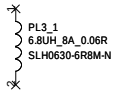
2010/03/15

1. P28, Change F6 to 1M-F6V0A75-0002, NC R337.
2. P18, Change R390, R391 to 33ohm.

CCPBG

Title	PVT Change Note		
Size: Custom	Document Number: *M9F1*		Rev: 0.1
Date: Wednesday, March 17, 2010	Sheet 44 of 44		

Main Source: 1L-DPCMC06-3T07.
2nd Source: 1L-DSLH063-0600.



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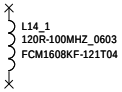

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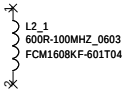

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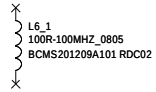
L1

Main Source: 1L-BHPB082-1000.
2nd Source: 1L-BBCMS20-1202.



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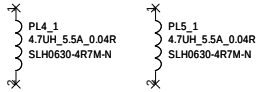

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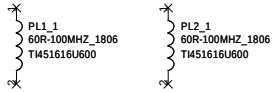

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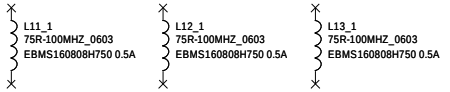

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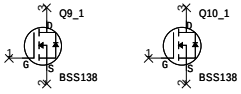

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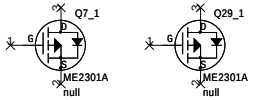

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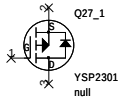

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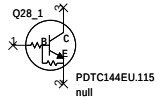

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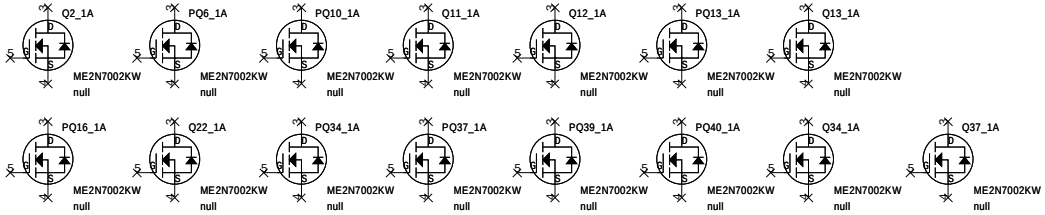

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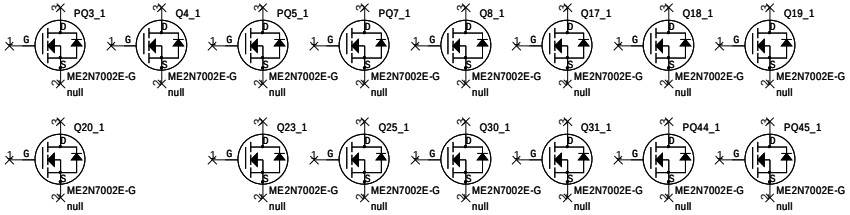

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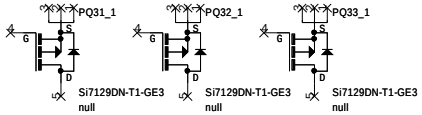
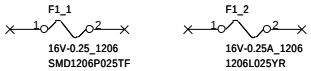


Title: **2nd Source_1**		
Size: A3	Document Number: *M9F0*	Rev: 0.1
Date: Wednesday, March 17, 2010	Sheet 45 of 46	

Main Source: 1M-F6V0A25-F000.
2nd Source: 1M-F16VA25-F000.



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2nd Source: 1M-F30VA12-F000.

F9

Main Source: 1C-30R0157-M100.
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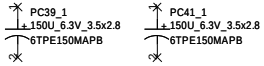

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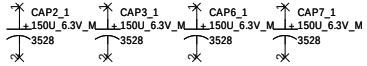

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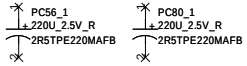
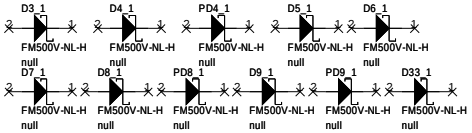


Main Source: 16-BAT54SP-T000.
2nd Source: 16-BAT54S0-0002.

PD5,PD6

Main Source: 16-MMP2525-0B01.
2nd Source: 16-MM3220V-C000.

Main Source: 16-CH500H4-0P00.
2nd Source: 16-FM500VN-L000.



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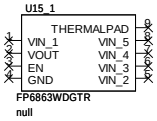

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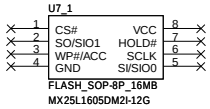

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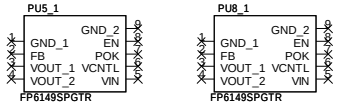

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CN15

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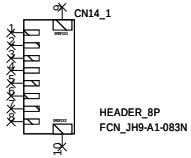

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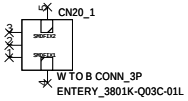

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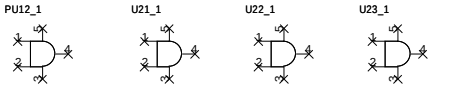

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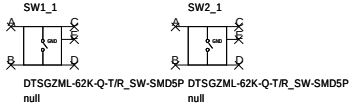

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Size: A3	Document Number: *M9F0*	Rev: 0.1
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