LCFC Confidential

L350 RENOIR+N18P-G61/G62 MB Schematics Document

RENOIR-H with DDR4 + N18P-G61/G62

2020-05-09

REV:1.0

Security Classification	LC Future Center Secret Data		
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Title: Cover Page

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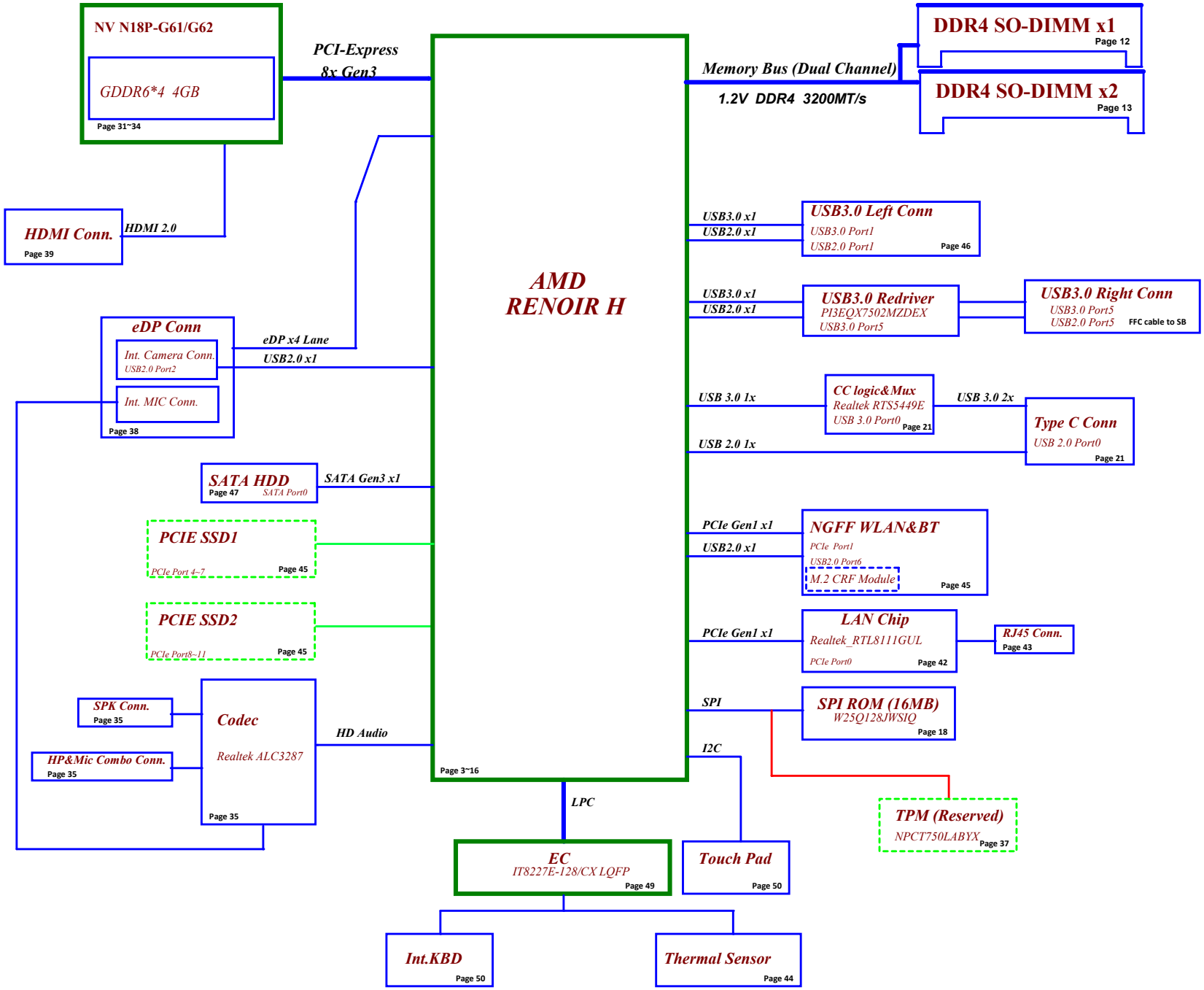

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Title: **Block Diagram**

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE / SIGNAL		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT		Function
USB3.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	4	NC
	5	NC
	6	NC
USB2.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	4	Finger Print
	5	Cardreader
	6	Touch Panel
	7	Bluetooth
	8	Camera
	9	NC
	10	NC
PCIE	1~4 X4 PCIE	DGPU
	5	LAN
	6	WLAN
	7	SATA HDD
	8	SATA ODD
	9~12 X4 PCIE	Optane Memory
SATA	0	HDD
	1A	ODD
	1B	used as PCIE
	2	used as PCIE

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
17@	For 17" part
15or17@	For 15" or 17" part
Cannonlake@	For Cannonlake part
CD@	For C cost down
DUALMIC@	For Dual MIC part
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC nu-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ES@	For ES CPU
EXO@	For EXO GPU
ME@	For ME part
TS@	For touch screen part
TS_NS@	For nu-touch part
DIS@	For GPU part
OPT@	For NV GPU part
PX@	For AMD GPU part
RANKA@	For VRAM rank A part
RANKB@	For VRAM rank B part
Realtek_SD@	For Realtek SD part
SINGLEMIC@	For single MIC part
SINGLERANK@	For single VRAN rank part
DUALRANK@	For dual VRAN rank part
TPM@	For TPM part
UMA@	For UMA part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
PCH	need to update
DGPU	need to update

EC SMBus3 address

Device	Address
PMIC	need to update

PCH SM Bus address

Device	Address
DDR4 SODIMM	need to update
Wlan	Reserved

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Title	Notes List		
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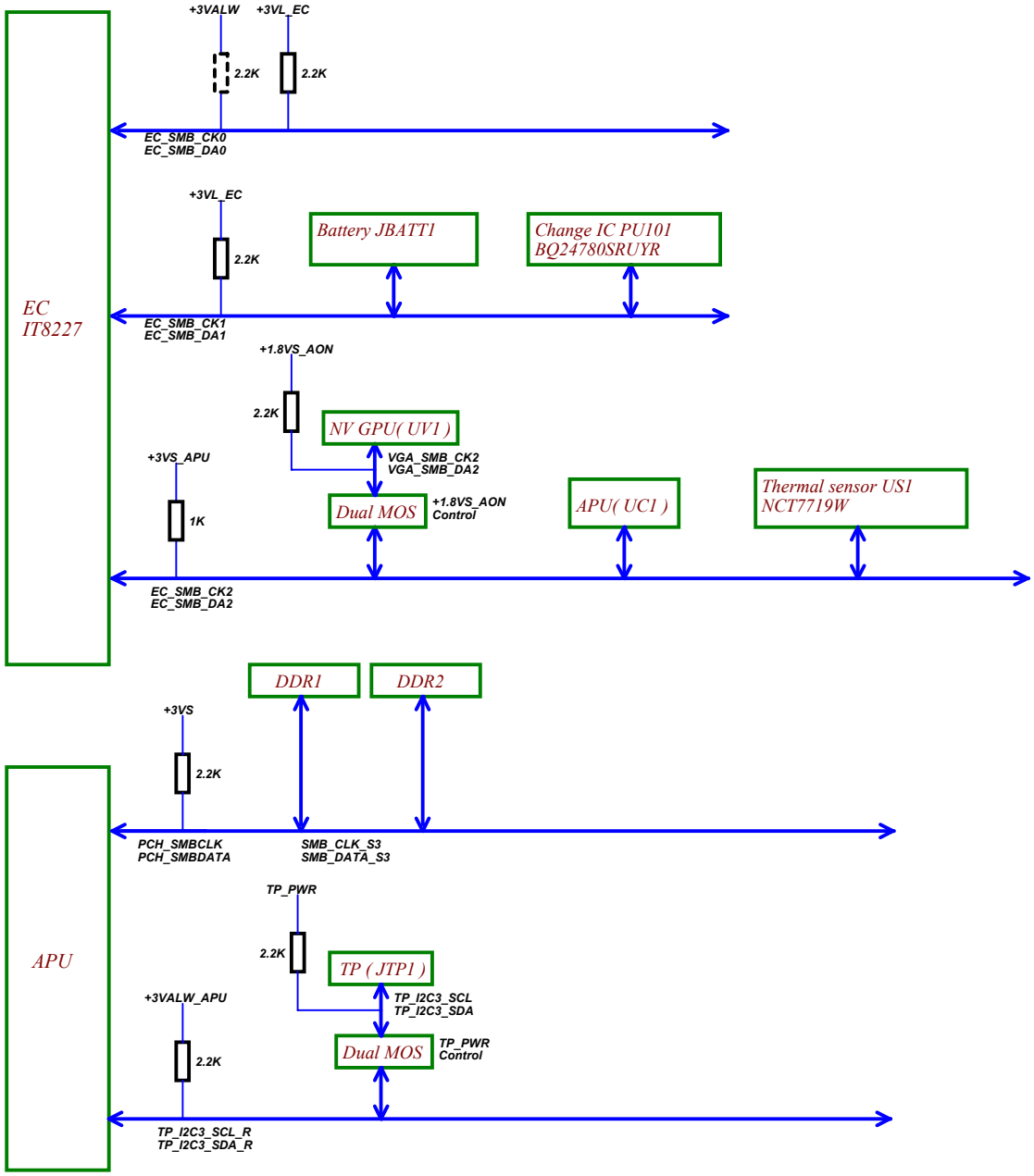

SMBUS Control Table

	SOURCE	VGA	BATT	IT8227E	SODIMM	WLAN WiMAX	Thermal Sensor	APU	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8227 +3VL_EC	X	V	V +3VL_EC	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8227 +3VS_APU	V +1.8VS_AON	X	V +3VS_APU	X	X	V	V	X	X
PCH_SMB_CLK PCH_SMB_DATA	APU +3VS	X	X	X	V	X	X	V +3VS	X	X
TP_I2C3_SCL_R TP_I2C3_SDA_R	APU +3VALW_APU	X	X	X	X	X	X	V +3VALW_APU	V TP_PWR	X

EC SM Bus1 address

Device	
Smart Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor NCT7719W	1001_101xb
VGA	0x9E(default)
APU	0x98

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb

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Title: I2C Block

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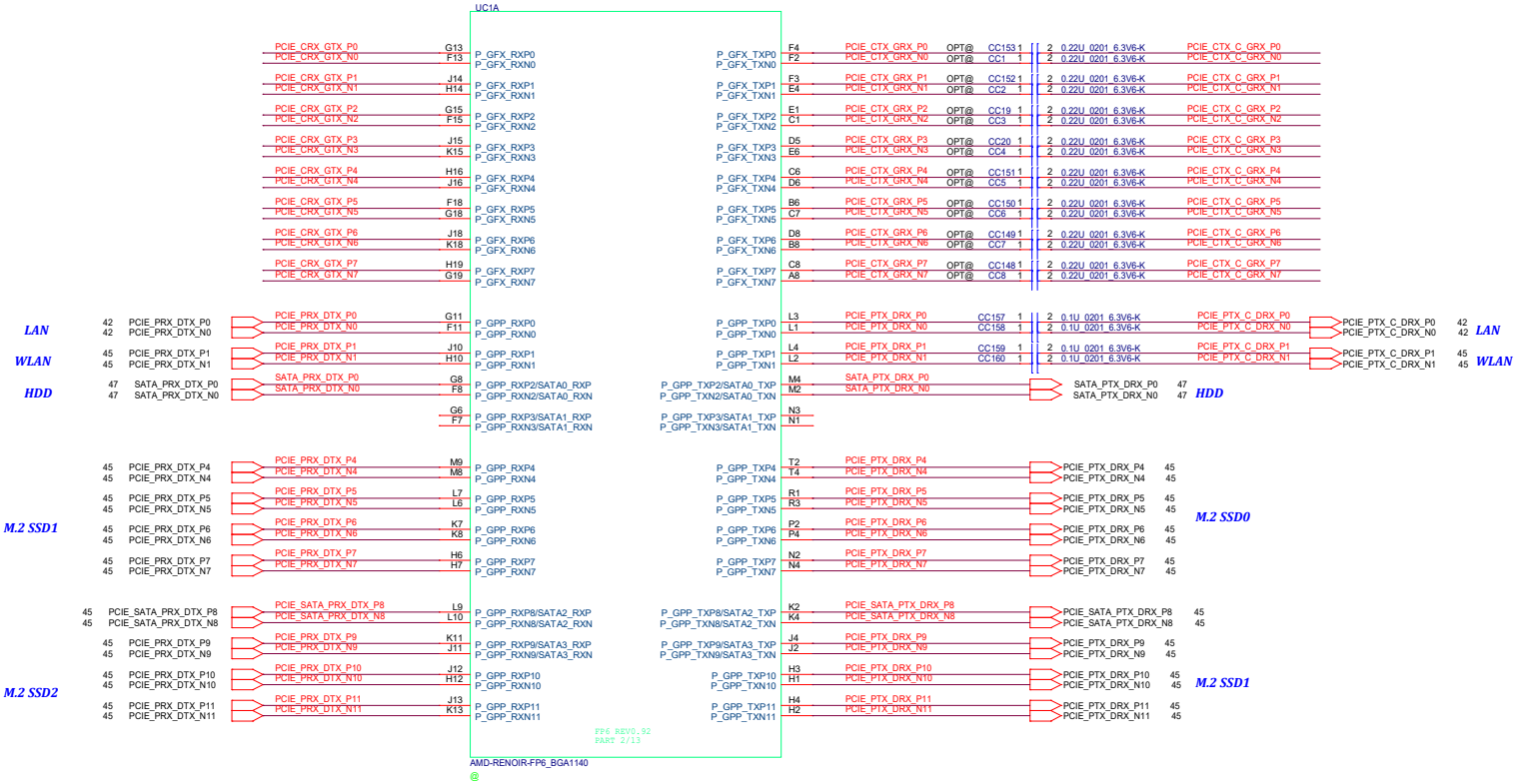
25 PCIE_CRX_GTX_N[0..7]

25 PCIE_CRX_GTX_P[0..7]

PCIE_CTX_C_GRX_N[0..7] 25

PCIE_CTX_C_GRX_P[0..7] 25



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Title: FP5 (PCIE SATA I/F)

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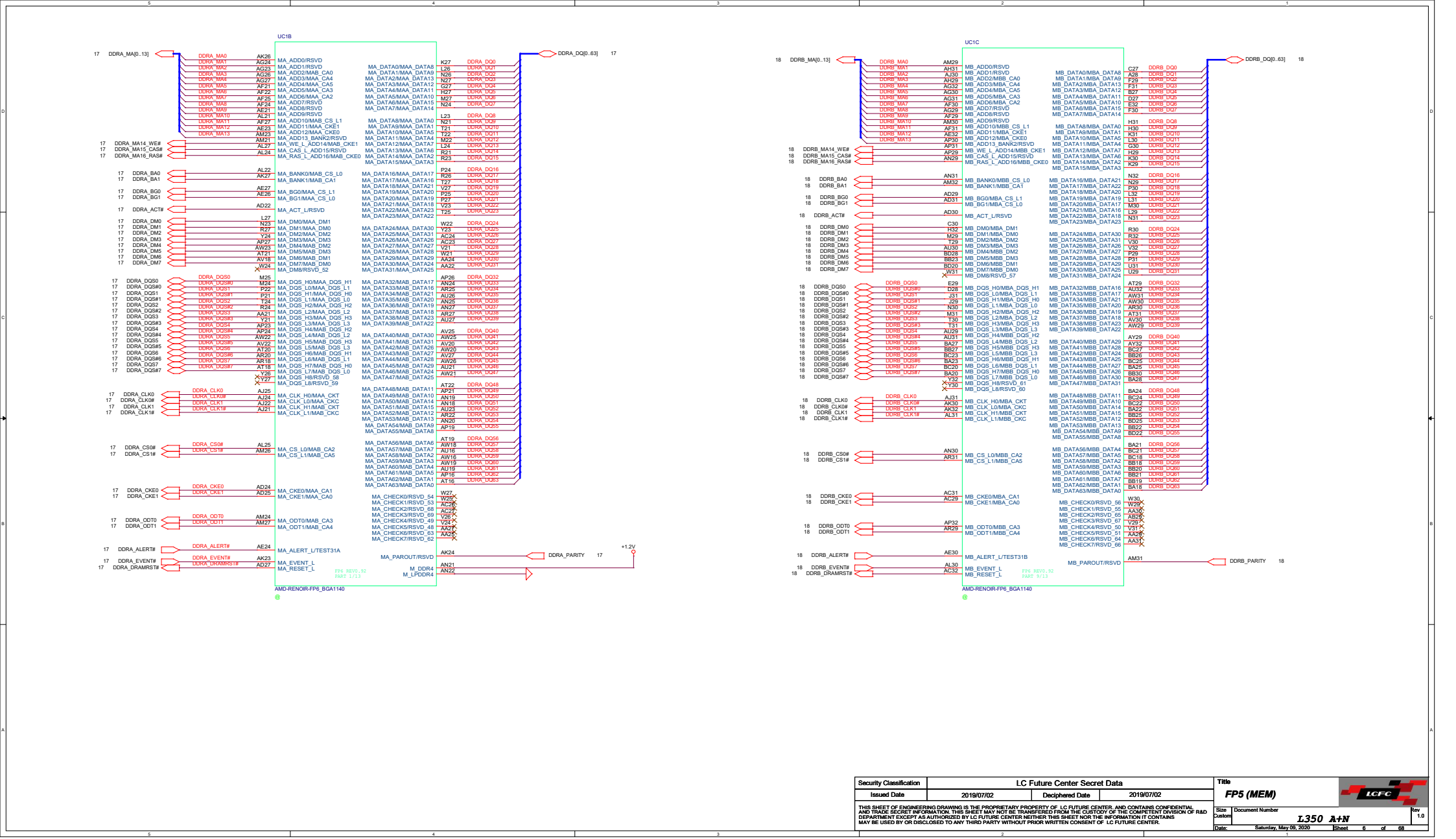

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Issued Date	2019/07/02	Deciphered Date	2019/07/02

Title: **FP5 (MEM)**

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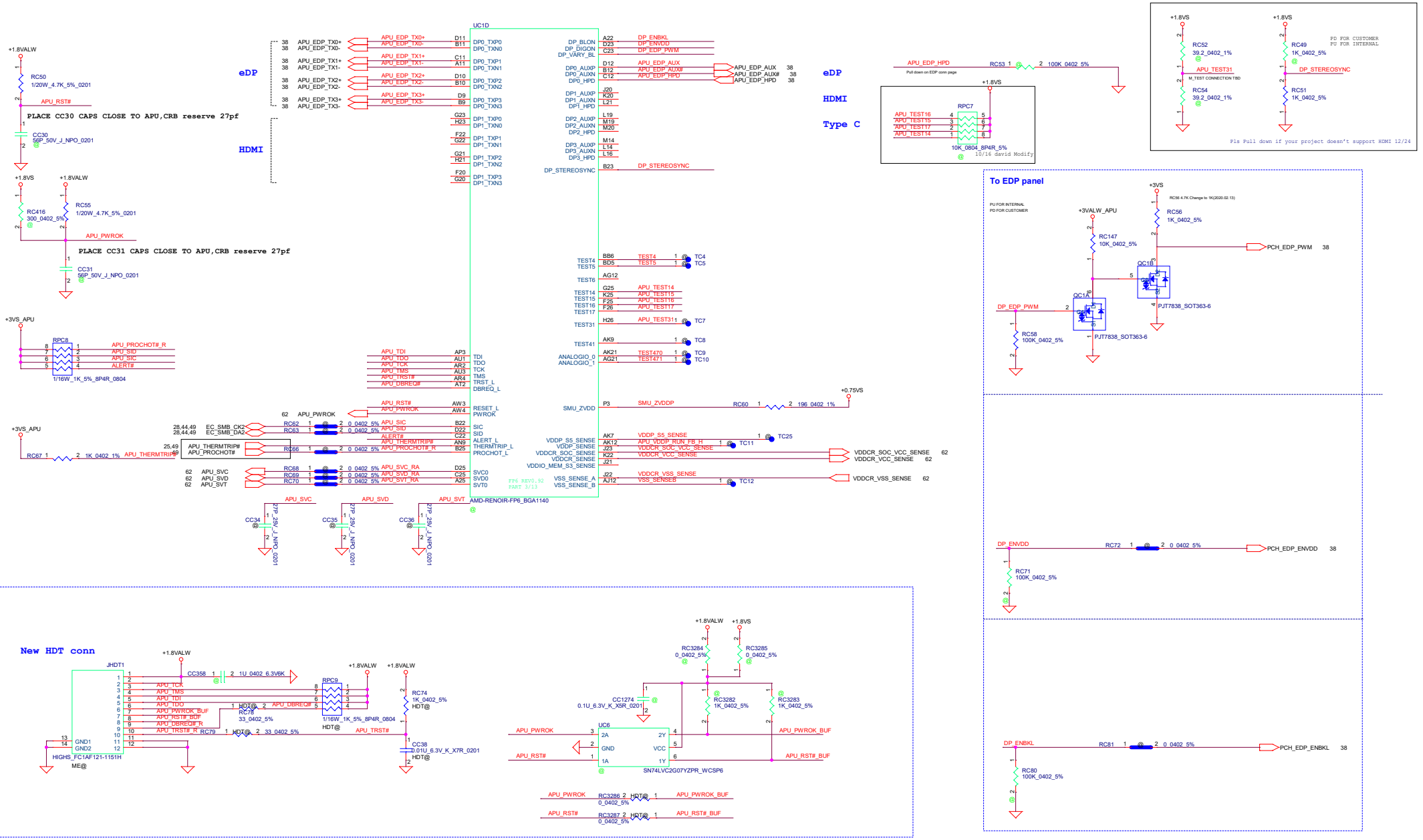

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Title: FP5 (DP/JTAG/SIV2/MISC)

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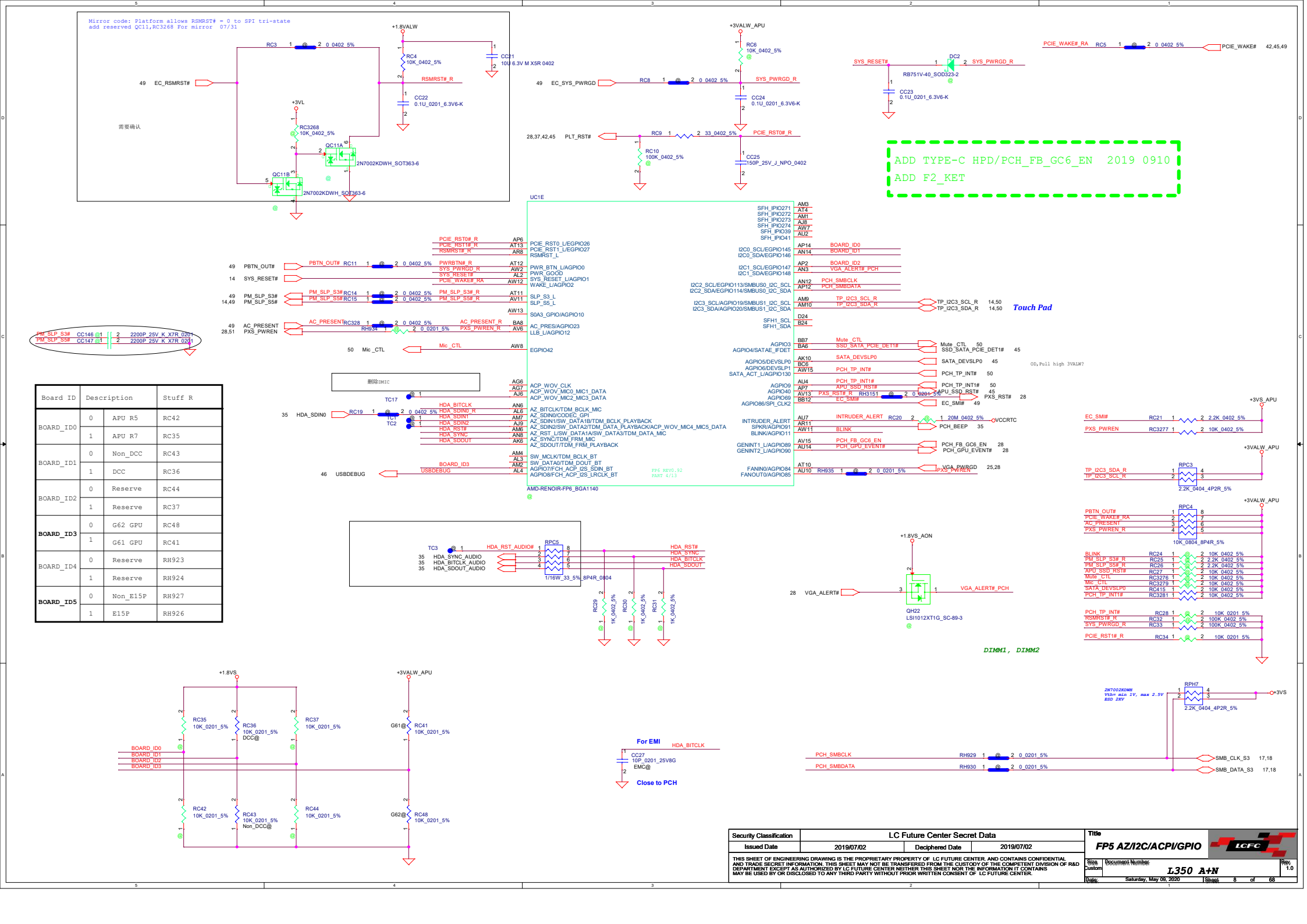

Board ID		Description	Stuff R
BOARD_ID0	0	APU R5	RC42
	1	APU R7	RC35
BOARD_ID1	0	Non_DCC	RC43
	1	DCC	RC36
BOARD_ID2	0	Reserve	RC44
	1	Reserve	RC37
BOARD_ID3	0	G62 GPU	RC48
	1	G61 GPU	RC41
BOARD_ID4	0	Reserve	RH923
	1	Reserve	RH924
BOARD_ID5	0	Non_E15P	RH927
	1	E15P	RH926

Title	FP5 AZ/I2C/ACPI/GPIO		
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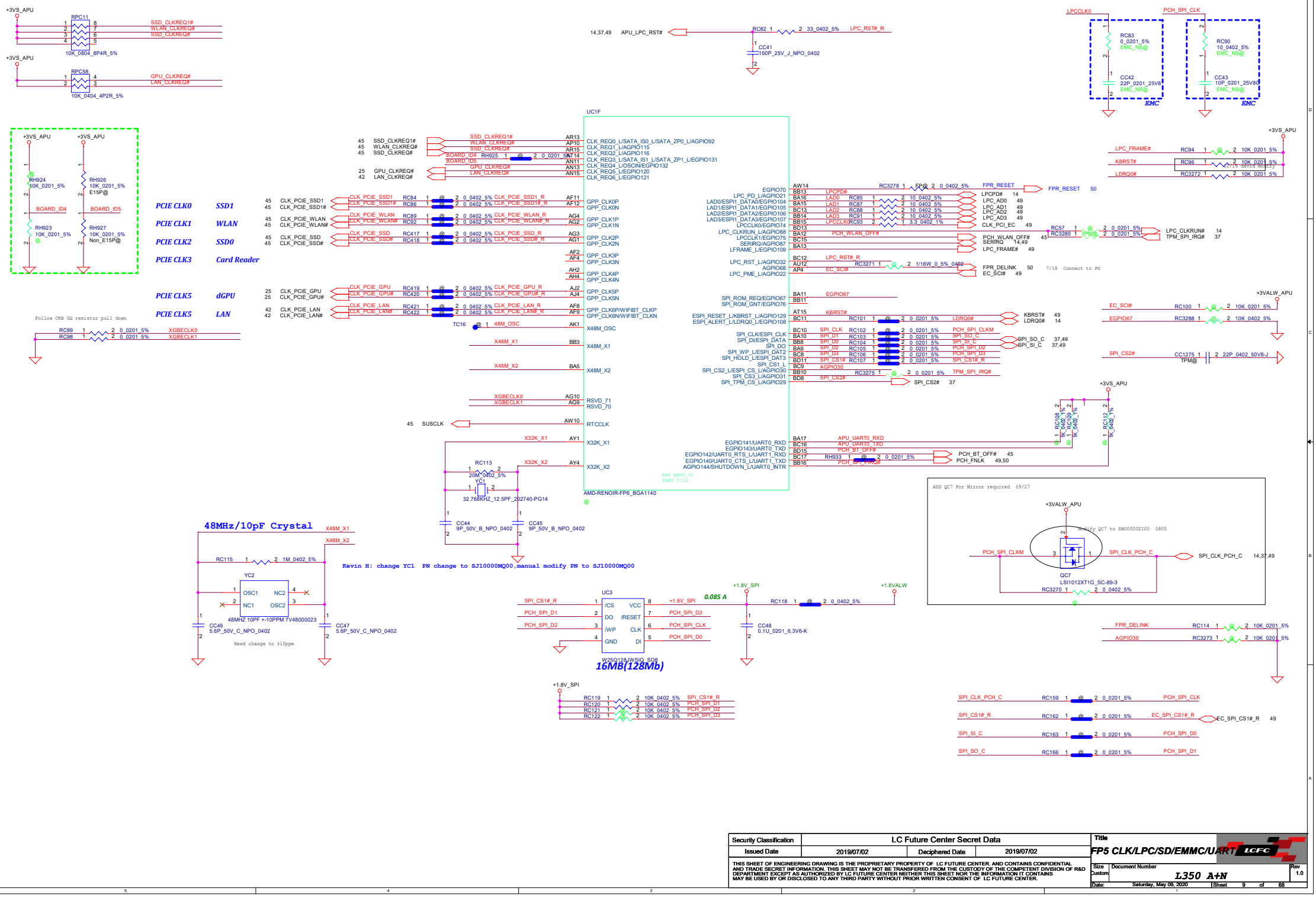

Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2019/07/02

Title: FP5 CLK/LPC/SD/EMMC/UART

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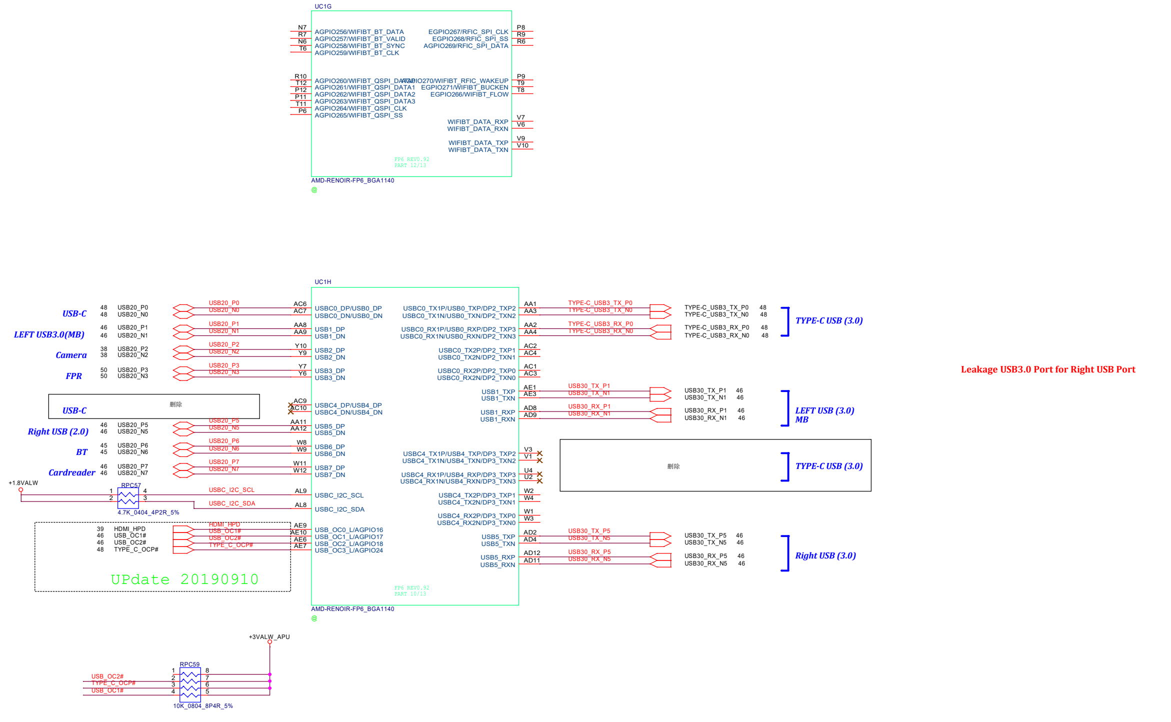

Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2019/07/02

Title: FP5 USB/WIFI

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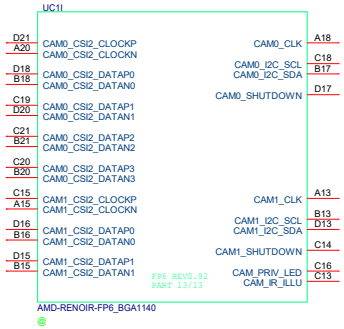

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Title: **FP5 CAM**

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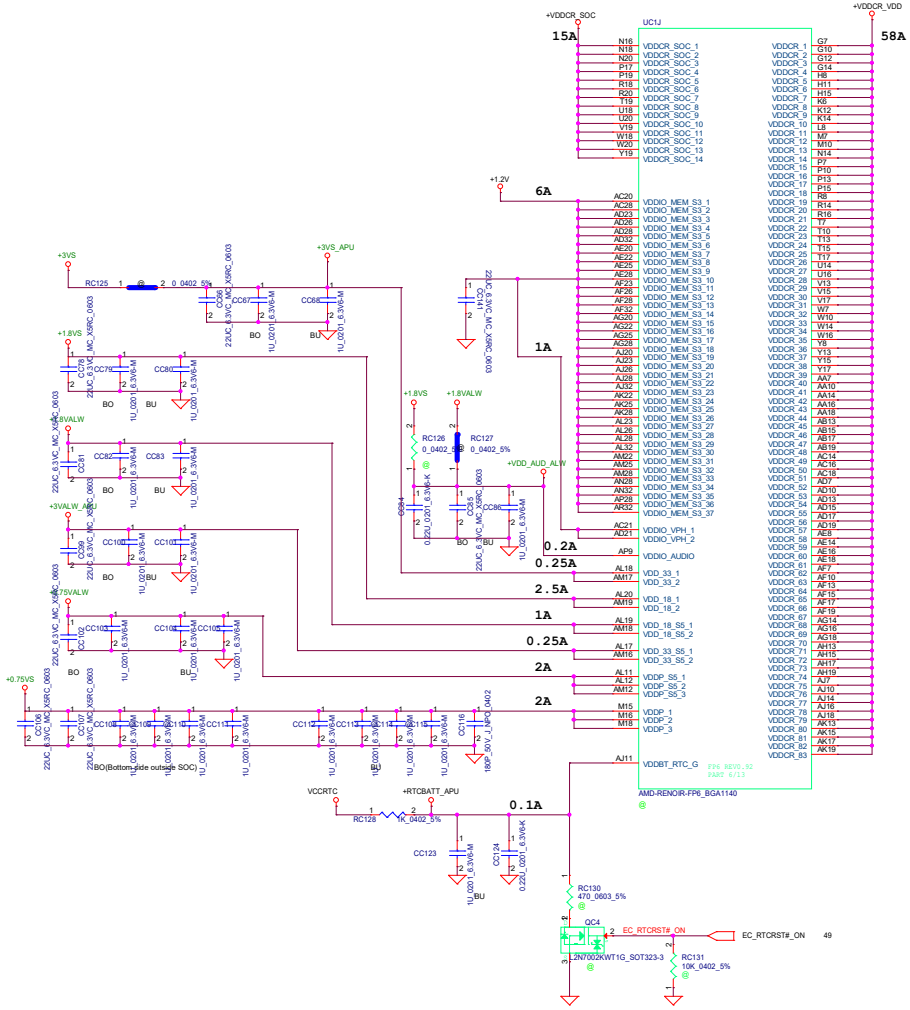

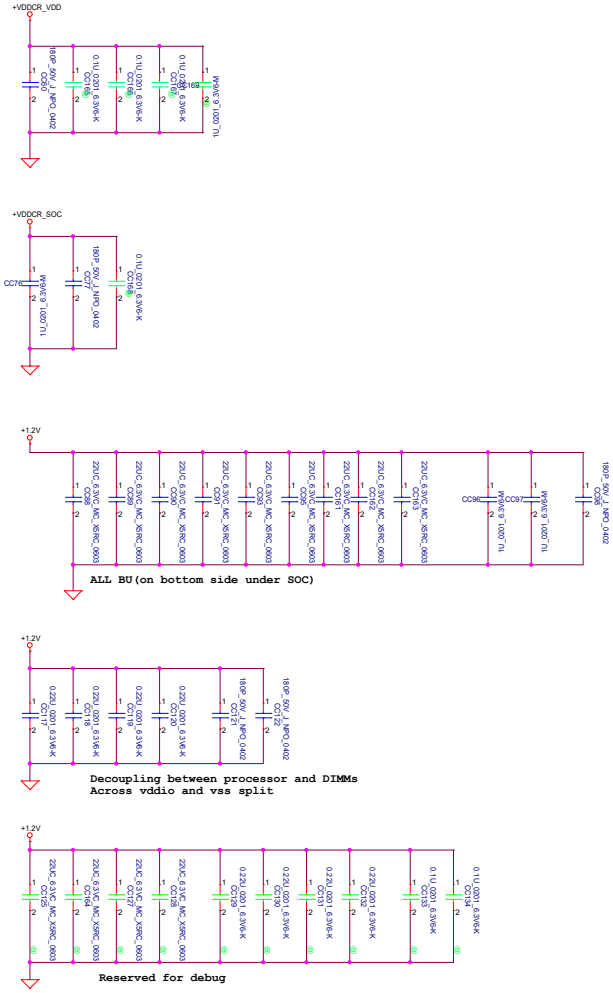

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Title	FP5 POWER
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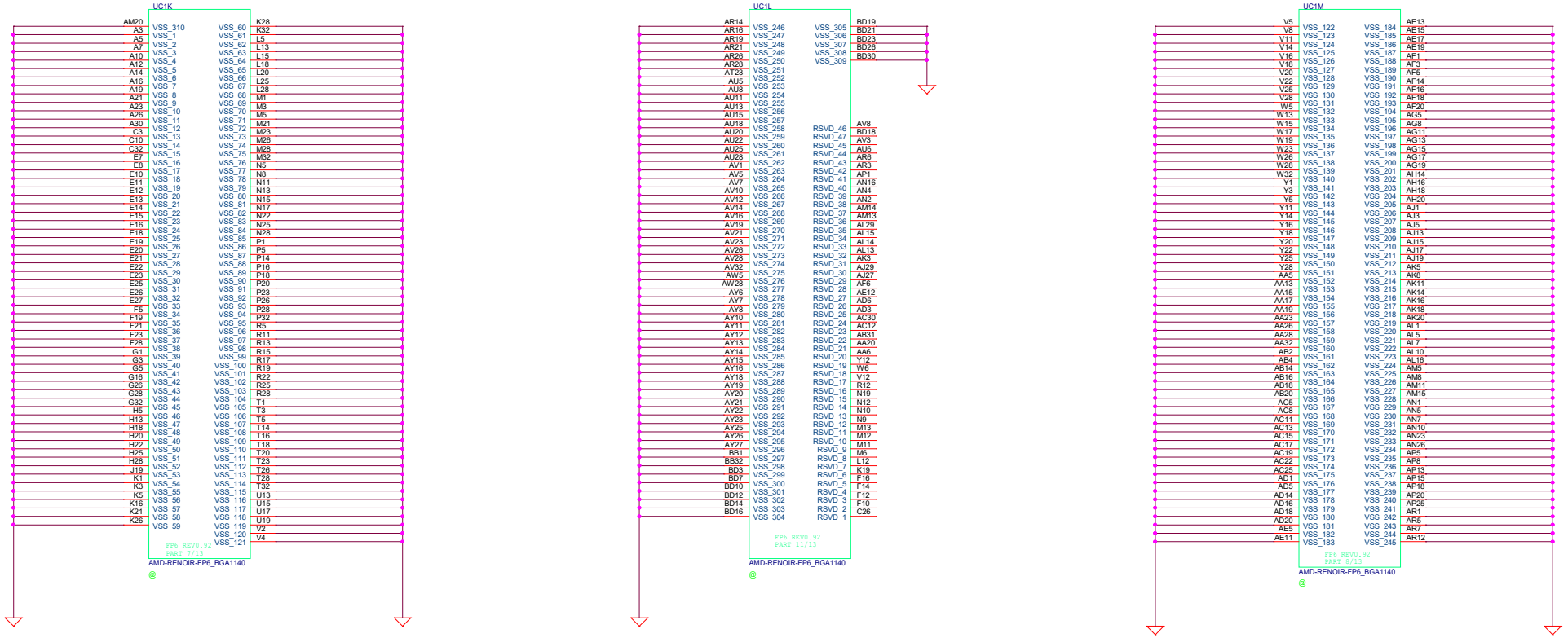

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Title: **FP5 GND**

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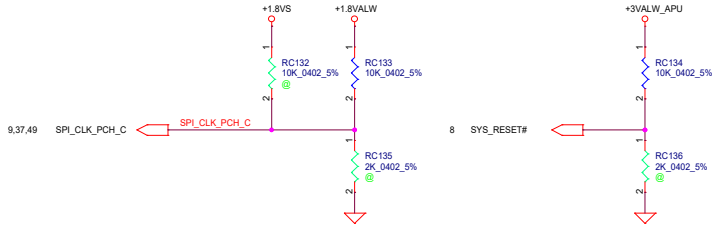
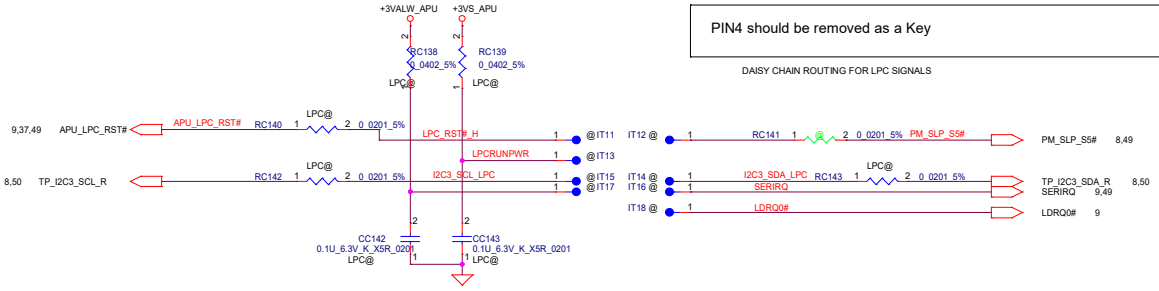
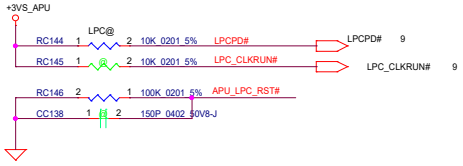


STRAP PINS	SYS_RESET#
PCH_SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RESET#	1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE

LPC ROM EMULATOR HEADER





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Title: **FP5 Straps**

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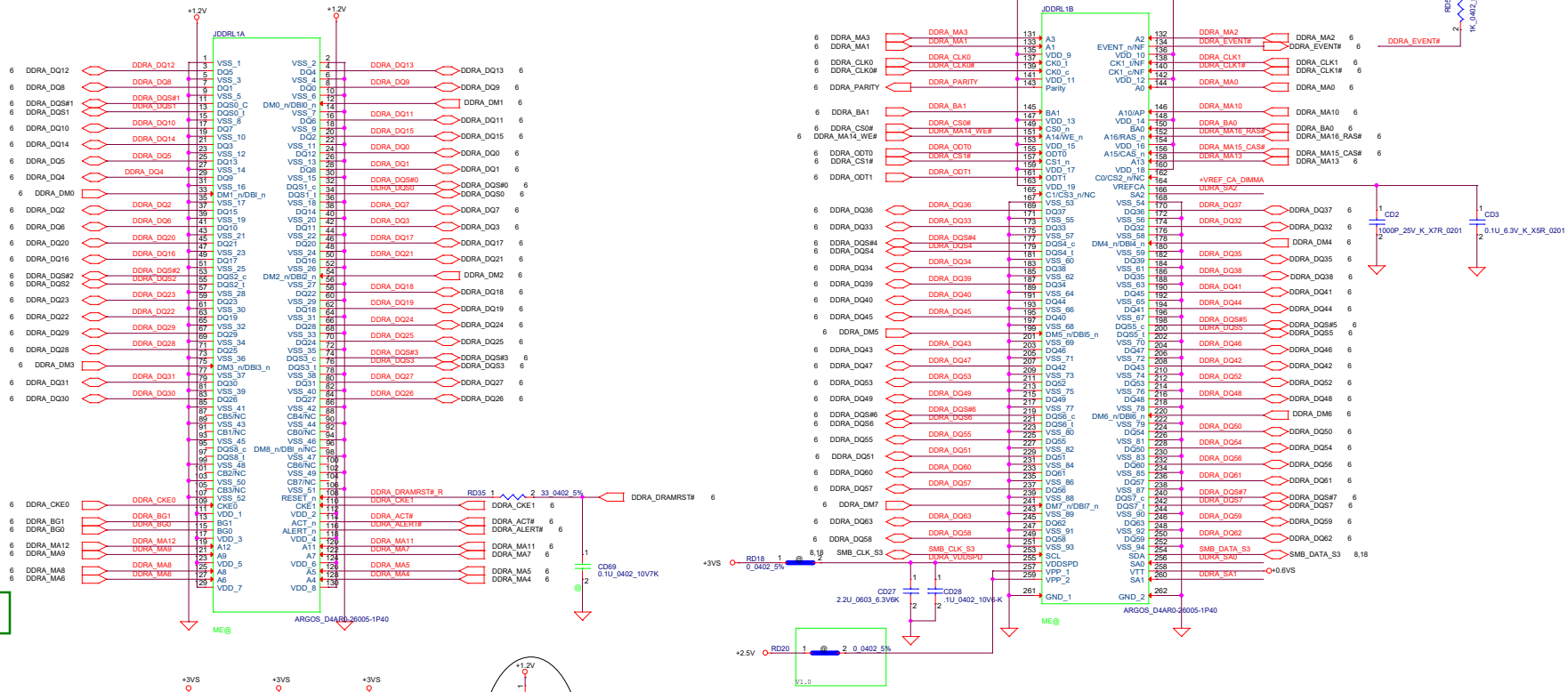
DDR4 SO-DIMM A



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Title	DDRVI SO-DIMM A		
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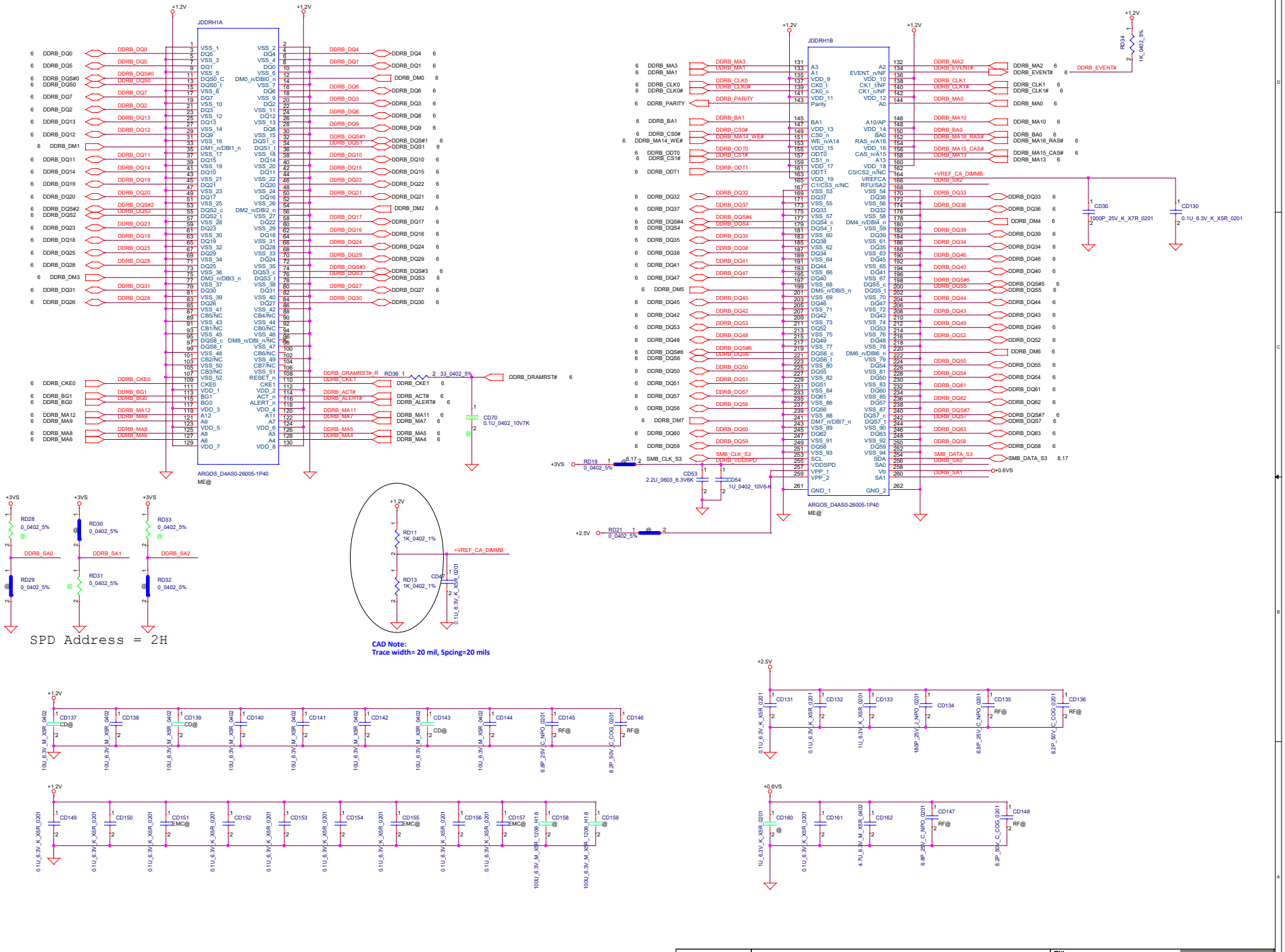
DDR4 SO-DIMM B



Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2019/07/02

Title	DDRVI SO-DIMM B
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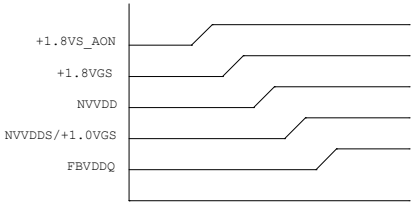
N18P-G61 G62 GPIO

GPIO	I/O	ACTIVE	Function Description	I/O Termination
GPIO0	OUT	-	PWM Output to control NVVDD	
GPIO1	OUT	-	FB Enable for GC6 2.1	
GPIO2	IN	-	GPU EVENT	
GPIO3	OUT	-	GPU MUX controler	
GPIO4	OUT	-	GPU power sequencing for GC6 2.1 --- 1V8_MAIN_EN	
GPIO5	IN	N/A	Active low Frame Lock	
GPIO6	OUT	-	Phase Shedding, NVVDD_PSI	
GPIO7	OUT	N/A	Panel Backlight (PWM)enable	
GPIO8	OUT	-	Memory voltage Control	
GPIO9	I/O	-	Active Low Thermal Alert	
GPIO10	OUT	-	Memory VREF Control (100K pull Down)	
GPIO11	OUT	-	Panel Power (LCD_VDD)enable	
GPIO12	IN	-	AC power detect or power supply overdraw input	(10K pull High)
GPIO13	IN	N/A	IGPU Backlight Enable	
GPIO14	IN	N/A	Hot Plug Detect for IFPA(TYPE-C)	
GPIO15	IN	N/A	Hot Plug Detect for IFPB(NA)	
GPIO16	OUT	-	DGPU PWM switch select	
GPIO17	IN	N/A	Hot Plug Detect for IFPD(DGPU eDP HPD)	
GPIO18	IN	N/A	Hot Plug Detect for IFPE(NA)	
GPIO19		N/A	NA	
GPIO20		N/A	GC6_MODE	
GPIO21	O	N/A	DGPU Backlight Enable	
GPIO22	O	N/A	ADC MUX select	
GPIO23	OUT	-	GPU PCIe self-reset control	
GPIO24		N/A	NA	
GPIO25			FVDDQ_PSI	
GPIO26		N/A	FP-FUSE	
GPIO27	IN	N/A	Hot Plug Detect for IFPC(HDMI)	

N18P-G61 G62 Power Sequence

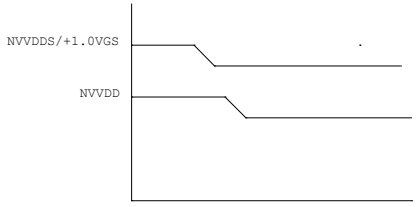


1. All power rail ramp up time should be larger than 40us and is recommended to be less than 2ms.

2. T (from 1V8_MAIN_EN to PEX_DVDD/NVVDD_Pgood) must NOT exceed 4ms.

3. All 3.3V devices that connect to the GPU must be powered after 1V8_AON; GPU can NOT have any 3.3V leakage path before 1V8_AON present.

4. The previous power rail must ramp up to 90% before the next power rail can start ramping up.



1. NVVDDS/PEX_DVDD must ramp down before NVVDD, all other power rails can ramp down together with NVVDD.

2. All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1V8_AON and 1.8V_MAIN power down.

3. The previous power rail must ramp down to 10% before the next power rail can start ramping down.

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	1111 DEFAULT
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

1:ENABLE 0:DISABLE

SOR0/1/2/3 ENABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

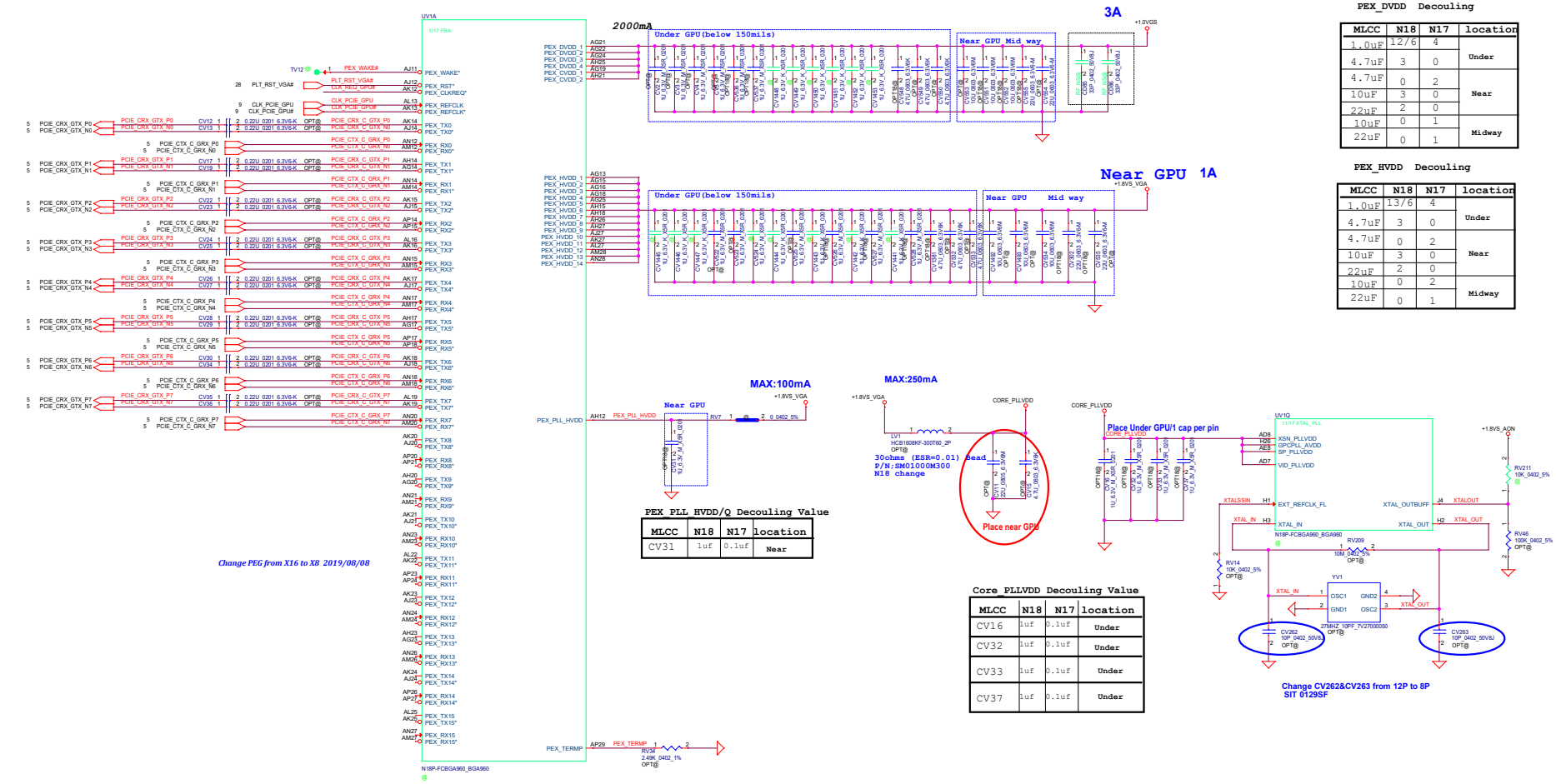
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2019/07/02

Title: VGA Notes List

Size	Document Number	Rev
C	L350 A+N	1.0

Date: Saturday, May 09, 2020 | Sheet 24 of 68



Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2019/07/02

Title: N18P_(1/6):PEG I/F

Size: Custom | Document Number: L350 A+N | Rev: 1.0

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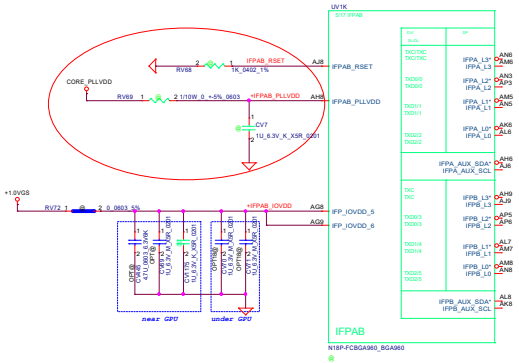
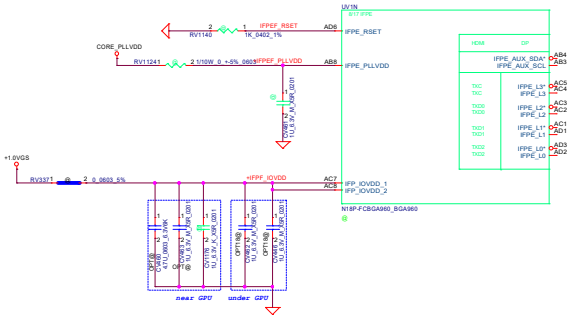
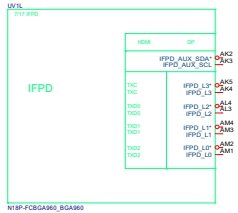
Ref NV DG-08780-001
If an IFP link is unused, in general it should be left unconnected.
This includes Main and Aux links.
IFPxy_RSET and IFPxy_PLLVDD (xy=AB,CD,EF)
can be left unconnected if neither of IFPx /IFPy is in use

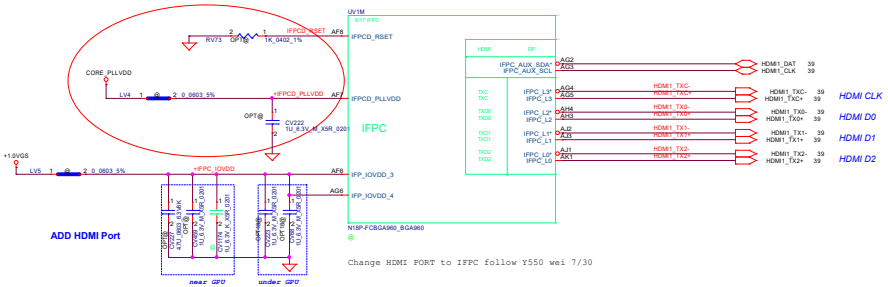




Decouling Value

MLCC	N18	N17	location
CV7	1uf	0.1uf	Under
CV222	1uf	0.1uf	Under
CV461	1uf	0.1uf	Under
CV70	1uf	0.1uf	Under
CV71	1uf	0.1uf	Under
CV223	1uf	0.1uf	Under
CV68	1uf	0.1uf	Under
CV462	1uf	0.1uf	Under
CV484	1uf	0.1uf	Under





For HDMI

ADD HDMI Port

Change HDMI PORT to IFPC follow Y550 wei 7/30

Security Classification	LC Future Center Secret Data			Title	N18P_(3/6):VRAM I/F
Issued Date	2019/07/02	Deciphered Date	2019/07/02		
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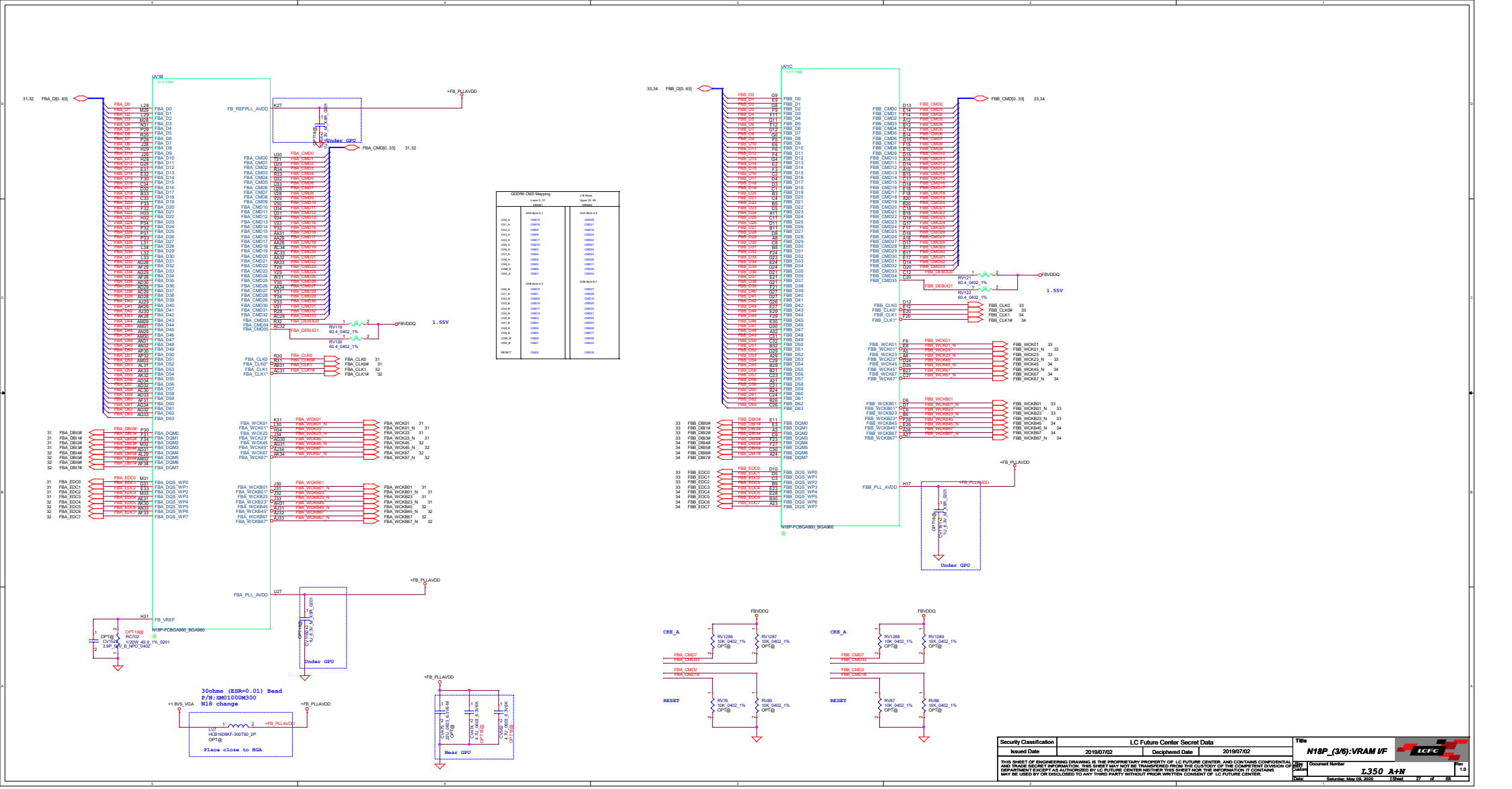
				Date: Saturday, May 09, 2020	Sheet 26 of 68



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Issued Date	2019/07/02	Deciphered Date	2019/07/02

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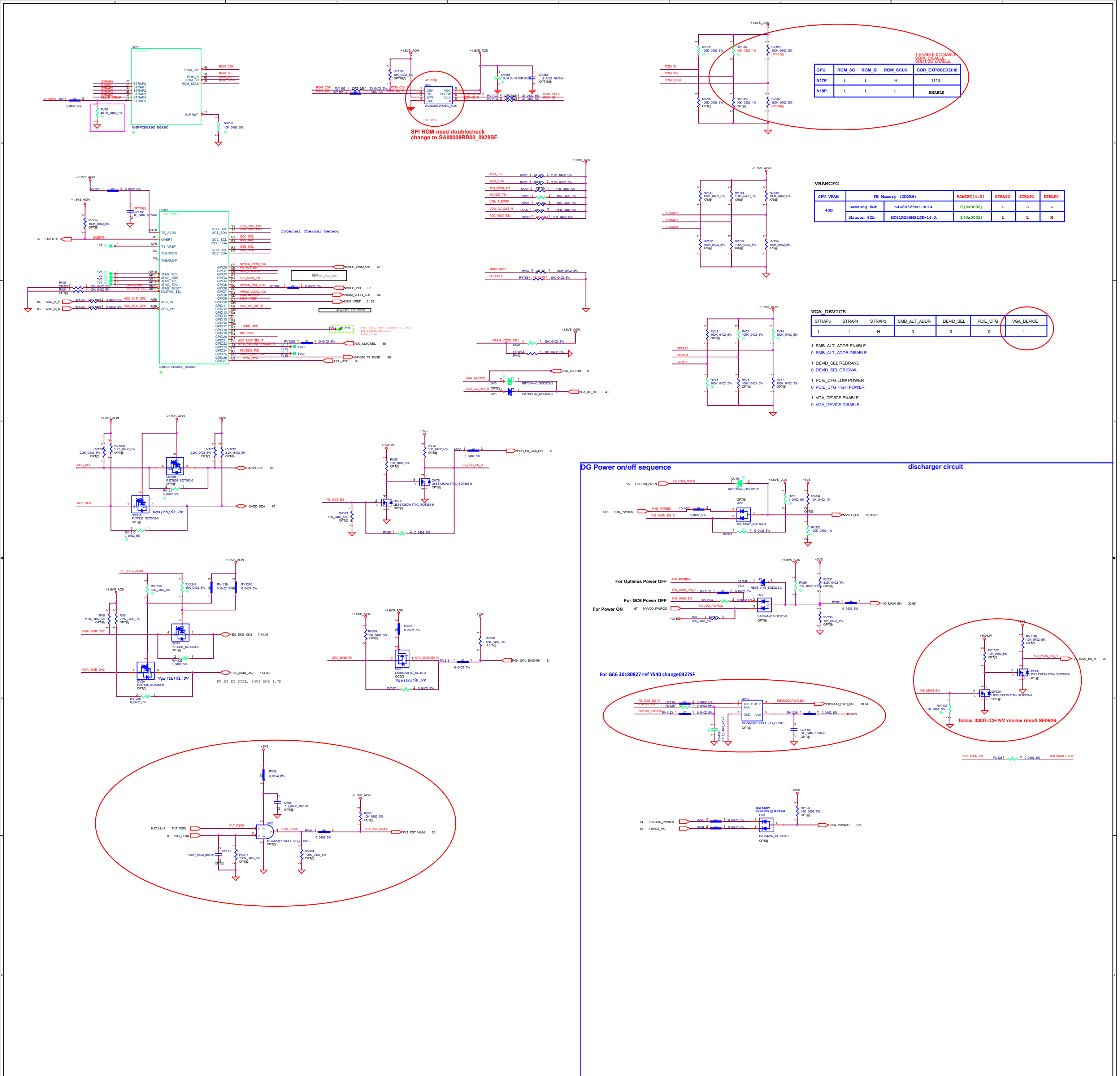
Title: N18P_(3/6):VRAM I/F

Size	Document Number	Rev
Custom	I350 A+N	1.0

Date: Saturday, May 09, 2020 Sheet 27 of 68



1:ENABLE 0:DISABLE
SOR0 DISABLE
SOR1/2/3 ENABLE

GPU	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N17P	L	L	H	1110
N18P	L	L	L	ENABLE

VRAMCFG

GPU VRAM	FB Memory (GDDR6)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
4GB	Samsung 8Gb	K4Z80325BC-HC14	0(0x0000)	L	L	L
	Micron 8Gb	MT61K256M32JE-14:A	1(0x0001)	L	L	H

VGA_DEVICE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	H	0	0	0	1

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE

Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2019/07/02

Title: N18P_(4/6):GPIO

Size: Custom | Document Number: L350 A+N | Rev: 1.0

5A Peak 8A

1.8V Total 1A (AON+MAIN)

0.5A

Cost down list:
1U 4Pcs

Partition A Under GPU(below 150mils)

Partition B Under GPU(below 150mils)

for N18P reserve 0928sf

Under GPU(below 150mils)

Near GPU

under GPU

near GPU

1.8VS_AON Decouling Value

MLCC	N18	N17	location
CV205	1uf	0.1uf	Under
CV206	1uf	0.1uf	Under
CV1475	@	@	Under
CV1476	@	@	Under
RV94	40.2ohm	60.4ohm	

CALIBRATION PIN	N17P	N18P
FB_CAL_x_PD_VDDQ	40.20hm	40.20hm
FB_CAL_x_PU_GND	40.20hm	40.20hm
FB_CAL_xTERM_GND	60.40hm	40.20hm

Place near balls

PLACE MIDWAY BETWEEN FBA AND FBB

only for N18P

Table 15. N17/GB4C-128 and N18/GB4D-128 FB BOM Differences

FB Pin	What to do for N18/GB4D-128	What to do for N17/GB4C-128
GPU FB_VREF	Pull down to 49.9 ohm	Leave unconnected and floating
FB_CAL_TERM_GND	Pull down to 40.2 ohm	Pull down to 60.4 ohm

AG26,AJ28 NC pin,
only for under GPU 1.8VS_VGA layout trace

2A

V20B+

AON7408L
Vds=30V
Ids=15A
Rdson=28mohm@Vgs=4.66V
=20mohm@Vgs=6V
=18mohm@Vgs>10V
Vgs=+-20V
Vgsth=1~3V

Vg=16.4V@AC
Vg=7.38V@Battery

+1.8V_MAIN discharger circuit

Reserve PD3/PR4/PR5/CV38 for NV sequence requirement

Security Classification	LC Future Center Secret Data	
Issued Date	2019/07/02	Deciphered Date 2019/07/02

Title: N18P_(5/6):PWR

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BOTH GP107 AND N18P-G5 NEED
NC AF30,AF32,AK31,AM34,E34,H30,M30,M34,
A30,A9,B2,B23,D22,D28,D9,E4

UV1D

UV1F

UV1G

UV1E

CONFIGURABLE POWER CHANNELS

N18P-FCBGA960_BGA960

NVVDD

UNDER GPU

NEAR GPU

trace width: 16mils
differential voltage sensing.
differential signal routing.

VDD_SENSE L4 NVVDD_VDD_SENSE NVVDD_VDD_SENSE 67

GND_SENSE L5 NVVDD_VSS_SENSE NVVDD_VSS_SENSE 67

Add RV332 for NVVDDS discharge Hai Y520 SVT

Change NVVDDS & +1.0VGS discharge circuit
HLZ SIV 0725

+5VALW

+1.0VGS

RV1292 47K_0402_5%

NVVDD_EN# QV29 AO3402_SOT-23-3

28,29,67 NVVDD_EN QV49 L8S3109WT1G_SC70-3

RV60 47K_0402_5% OPT@

1V0_MAIN_EN# QV12 AO3402_SOT-23-3 OPT@

28,65 1V0_MAIN_EN QV11 L8S3109WT1G_SC70-3 OPT@

Change QV6/RV48/QV4/RV62 from REV@ to ns Hai Y520 SVT

FBVDDQ

RV48 47K_0402_5%

RV61 470_0603_5%

QV6B 2N7002KDWH_SOT363-6

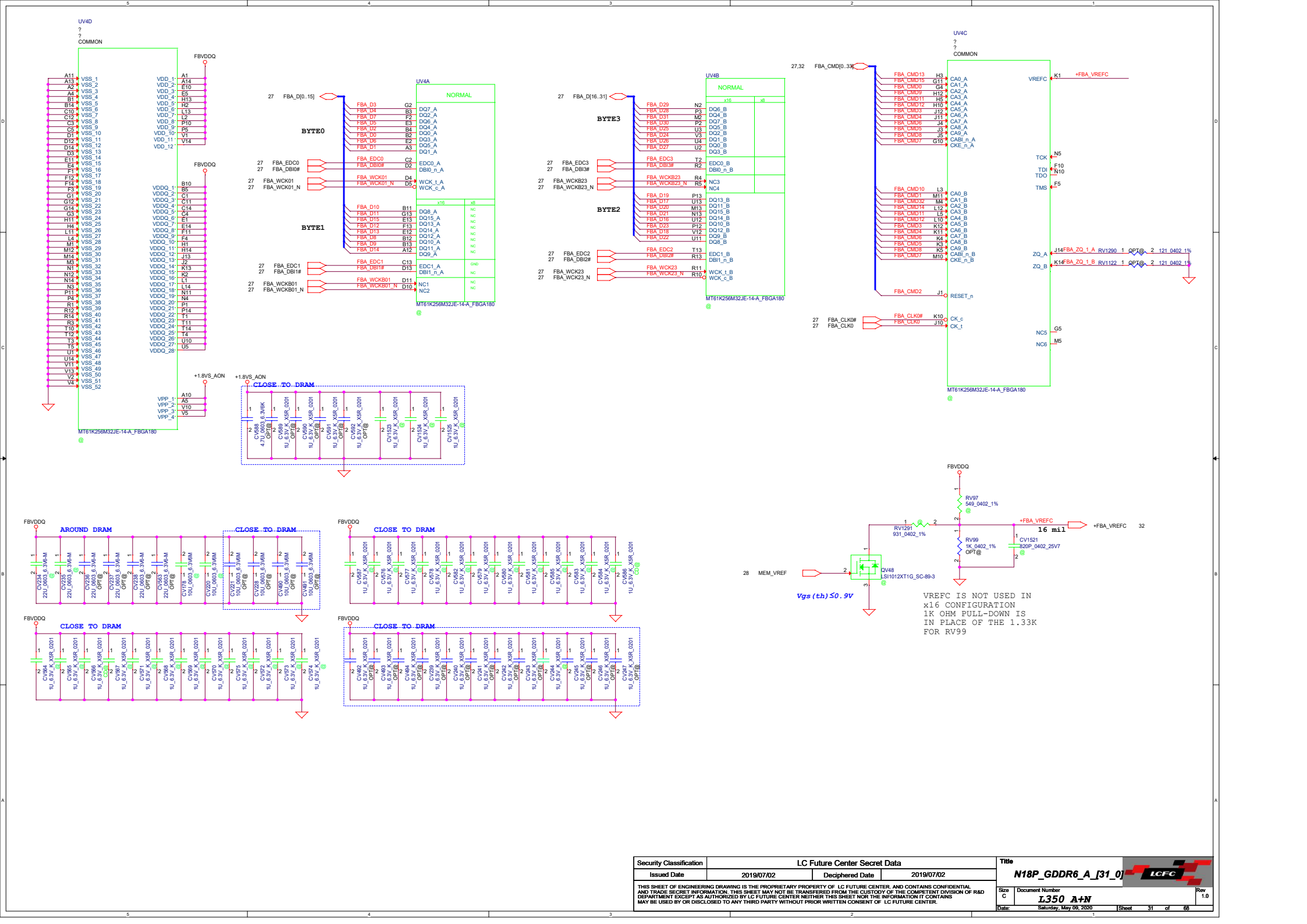
28,64 FBVDDQ_PWR_EN QV6A 2N7002KDWH_SOT363-6

Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2019/07/02

Title: N18P_(6/6):PWR,VSS

Size: Custom | Document Number: L350 A+N | Rev: 1.0

Date: Saturday, May 09, 2020 | Sheet 30 of 68



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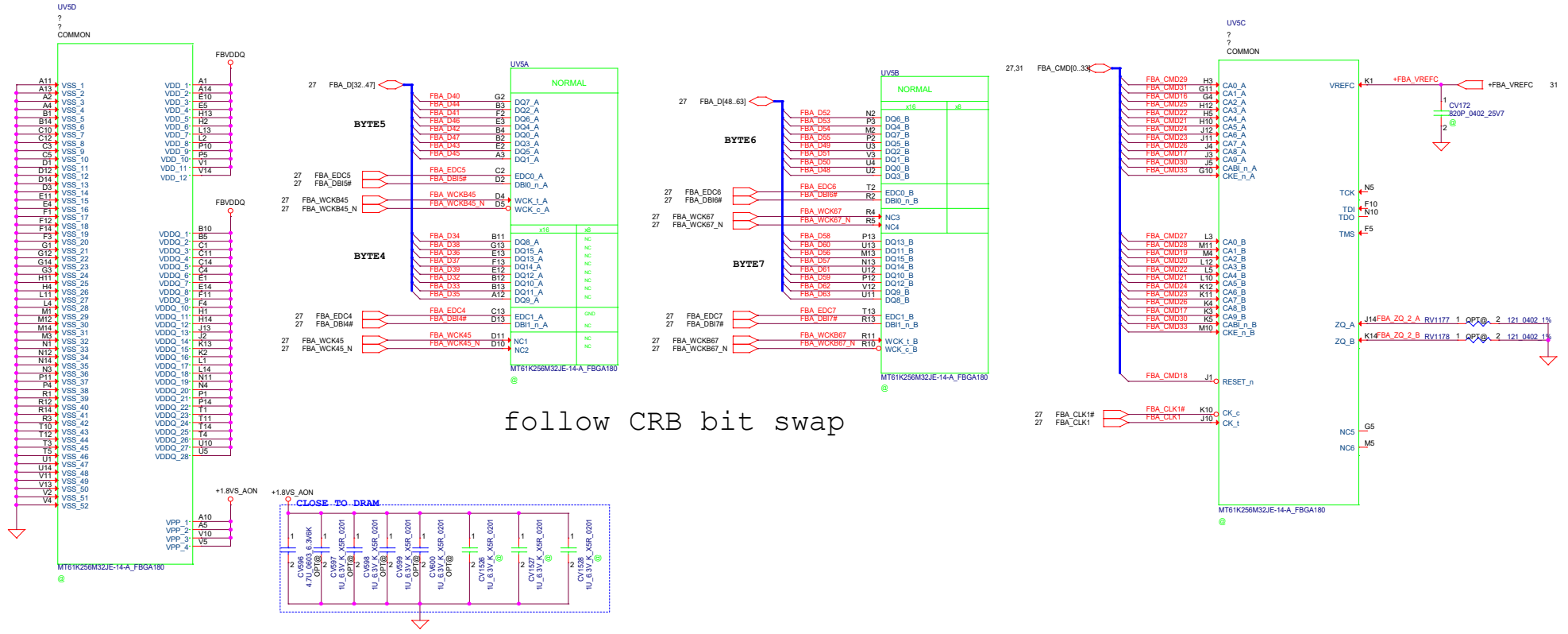
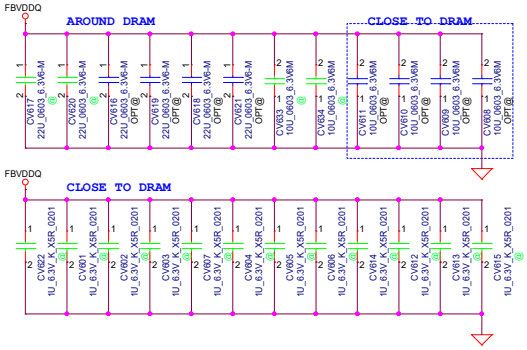
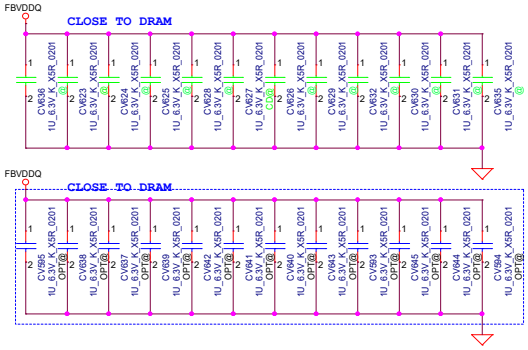
Title: N18P_GDDR6_A_[31_0]

Size	Document Number	Rev
C	L350 A+N	1.0

Date: Saturday, May 09, 2020 | Sheet 31 of 68





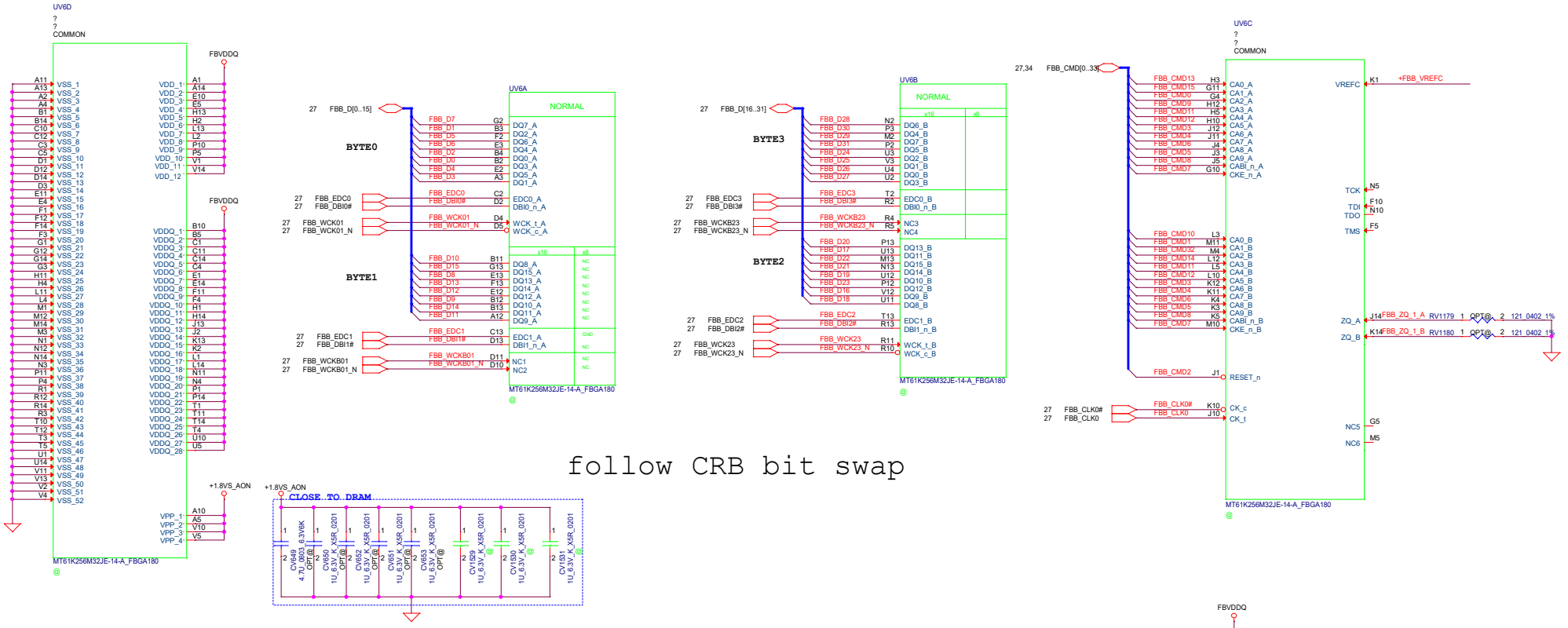


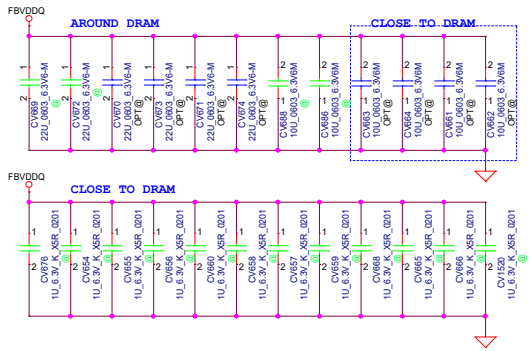
Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2019/07/02

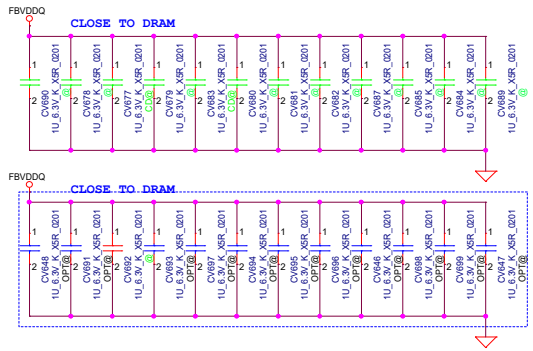
Title: N18P_GDDR6_A_[63_32]

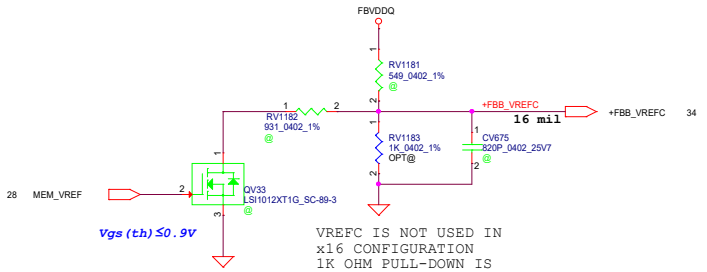
Size	Document Number	Rev
C	L350 A+N	1.0

Date: Saturday, May 09, 2020 | Sheet 32 of 68









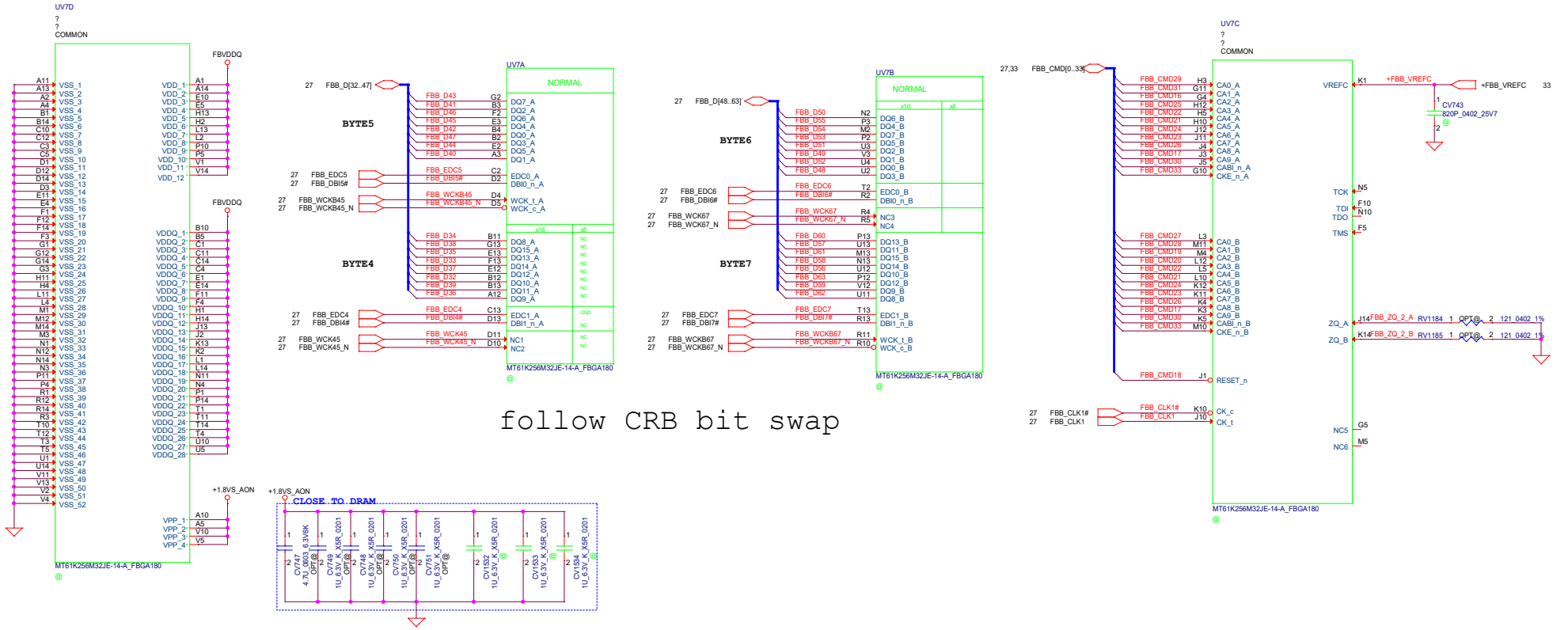
VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR RV1183

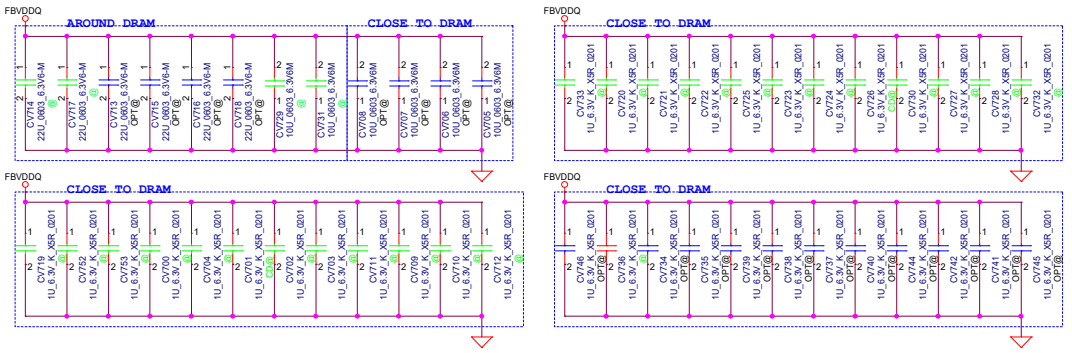
Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2019/07/02

Title: N18P_GDDR6_B_[31_0]

Size	Document Number	Rev
C	L350 A+N	1.0

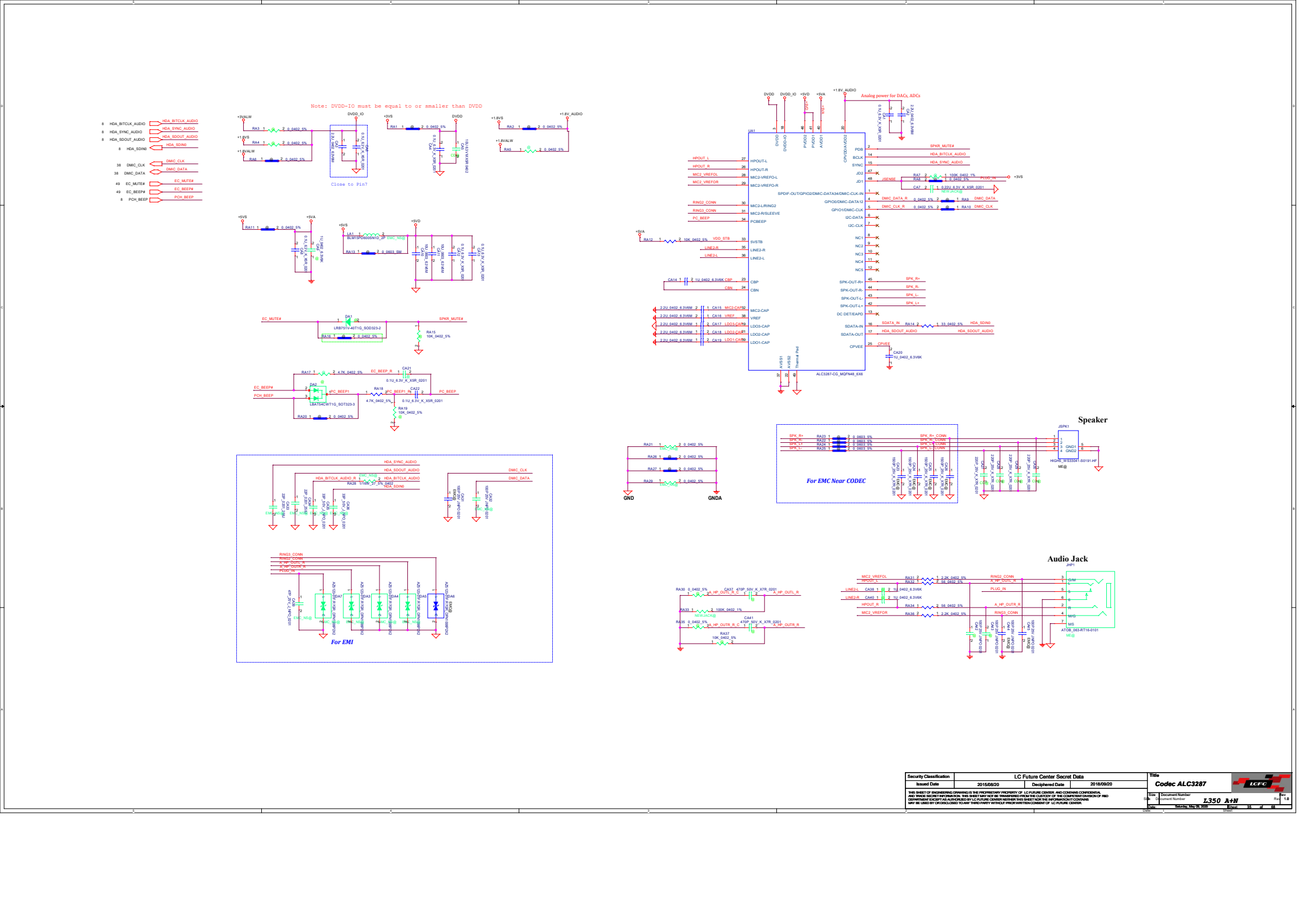
Date: Saturday, May 09, 2020 | Sheet 33 of 68





Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2019/07/02

Title	N18P_GDDR6_B_[63_32]		
Size C	Document Number L350 A+N		Rev 1.0
Date: Saturday, May 09, 2020	Sheet 34 of 68		


Note: DVDD-IO must be equal to or smaller than DVDD
Close to Pin7
Analog power for DACs, ADCs
Speaker
For EMC Near CODEC
Audio Jack
For EMI
ALC3287-CG_MQFN48_6X6
Codec ALC3287
LC Future Center Secret Data
Issued Date 2015/08/20
Deciphered Date 2016/09/20
L350 A+N
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Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title

Card Reader

Size: Custom	Document Number: L350 A+N	Rev: 1.0
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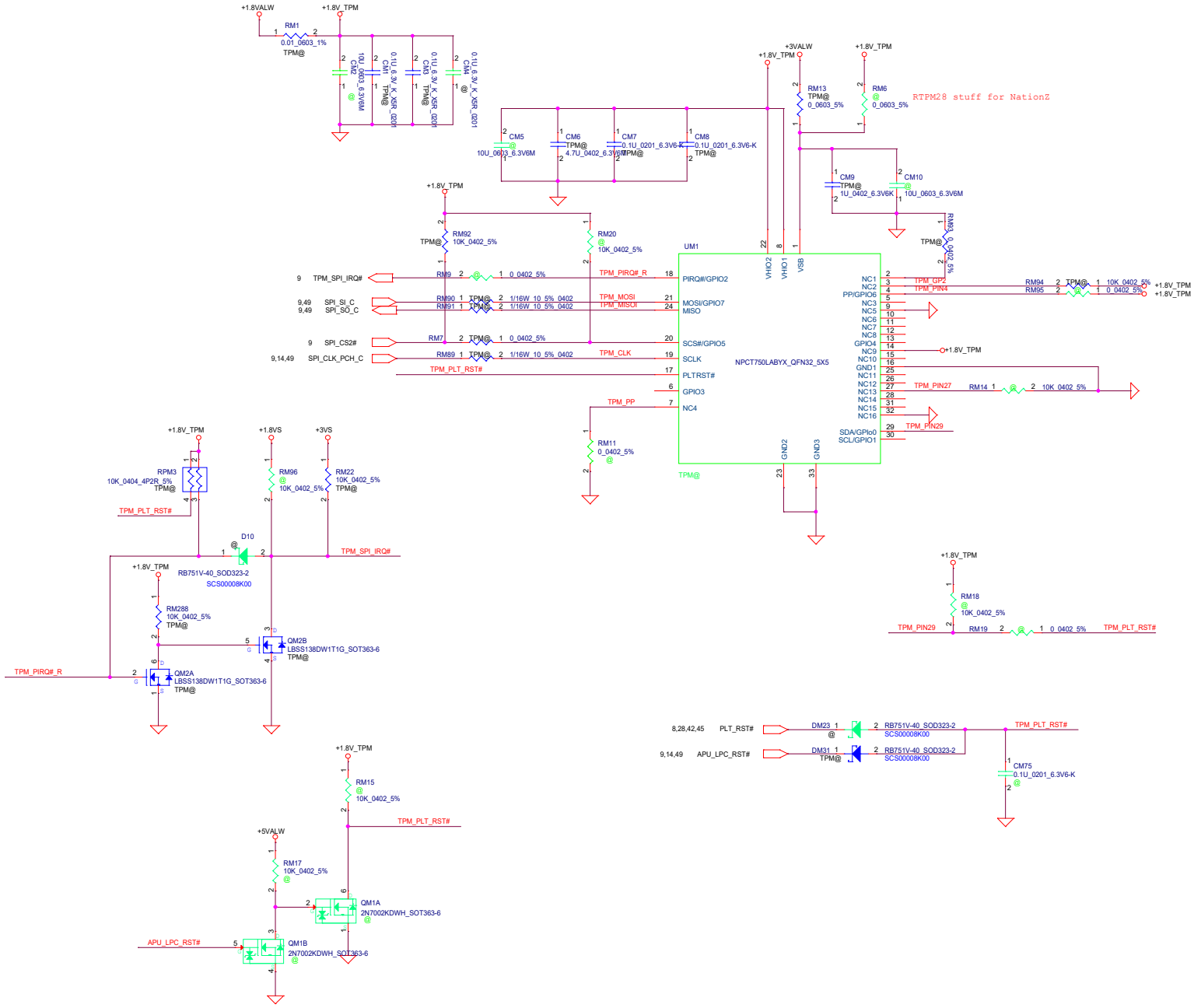

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title: **TPM**

Size	Document Number	Rev
C	L350 A+N	1.0
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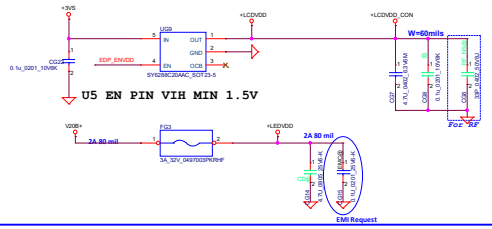
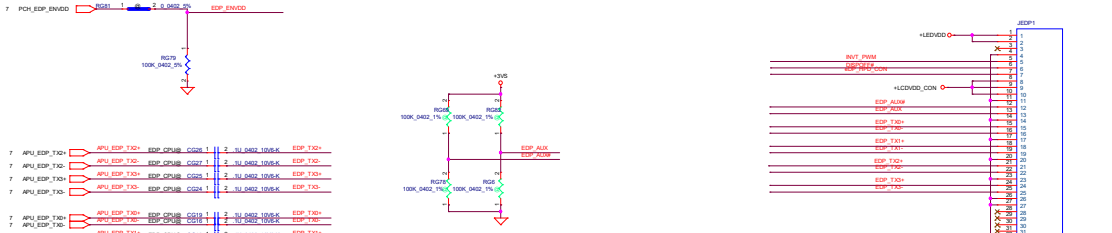
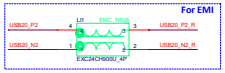
LCD POWER CIRCUIT

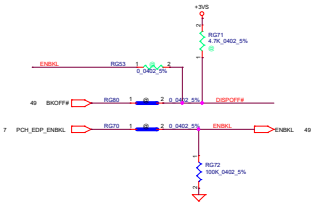


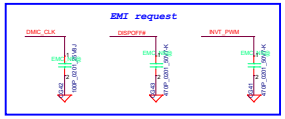
CMOS Camera

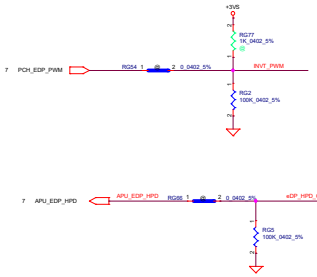


EDP symbol:
1.update to 40pin reserved for 144HZ panel 6/20 wei









Touch Screen delete TS function0704SF

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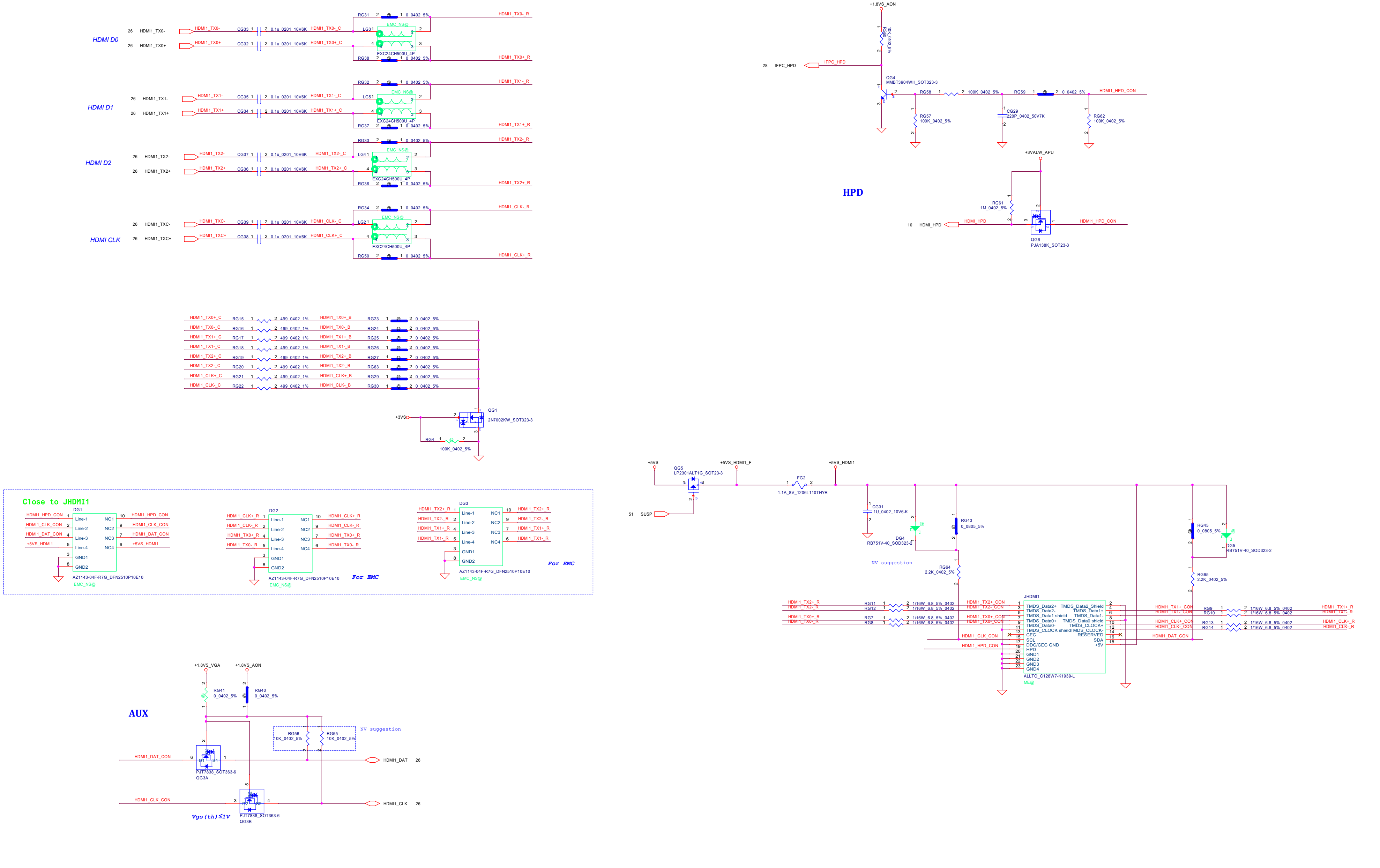
Title	eDP/CMOS/Touch screen		
Size	Document Number		Rev
Custom	L350 A+N		1.0
Date:	Saturday, May 09, 2020	Sheet	38 of 68



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title: HDMI_CONN

Size: D | Document Number: L350 A+N | Rev: 1.0

Date: Saturday, May 09, 2020 | Sheet 39 of 68

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title

Blank

Size	Document Number	Rev
Custom	L350 A+N	1.0

Date: Saturday, May 09, 2020 Sheet 40 of 68

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title

XDP

Size	Document Number	Rev
C	L350 A+N	1.0

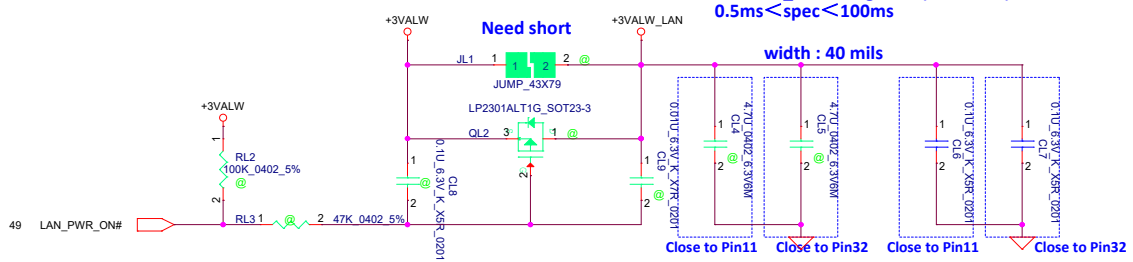
Date: Saturday, May 09, 2020 | Sheet 41 of 68

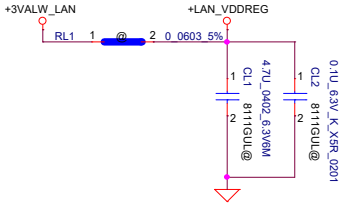
+3VALW TO +3VALW_LAN

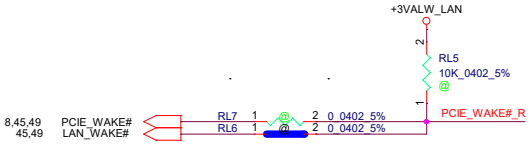
+3VALW_LAN rising time (10%~90%):
0.5ms＜spec＜100ms

Need short

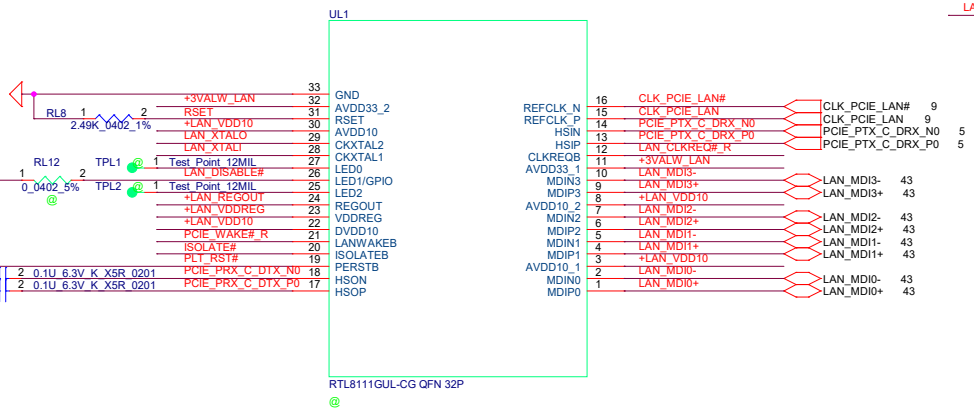
width : 40 mils

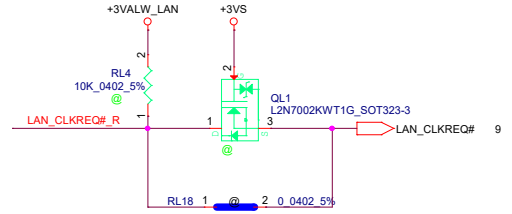


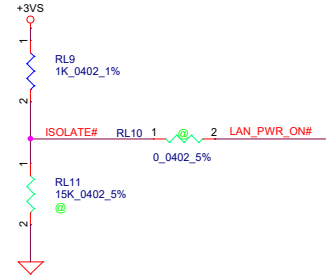




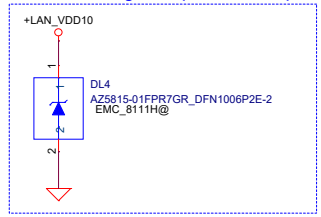
manual change the PN to RTL8111GUL-CG

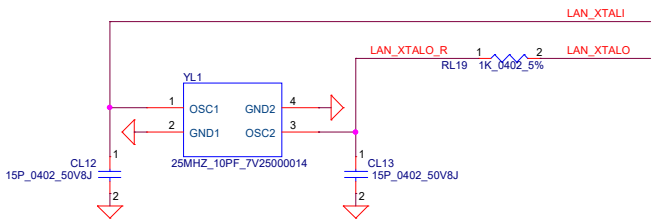




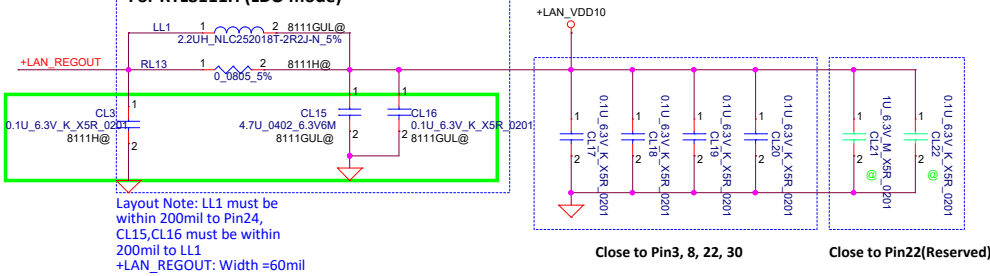


2018/01/24: add AZ5815-01F.R7GR for RTL8111H Lan Surge issue (Default reserve)





For RTL8111GUL(SWR mode)
For RTL8111H (LDO mode)



Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

Close to Pin3, 8, 22, 30

Close to Pin22(Reserved)

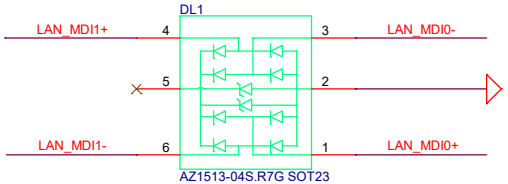
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

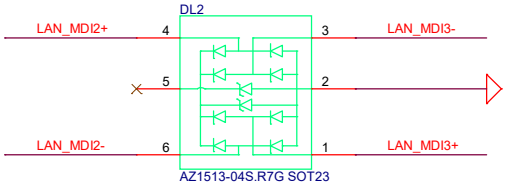
Title: LAN_RTL8111H_CG

Size: Custom | Document Number: L350 A+N | Rev: 1.0

Date: Saturday, May 09, 2020 | Sheet 42 of 68

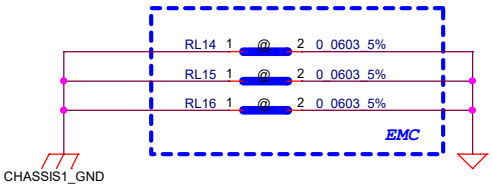
Default DL1/DL2 use
S DIO(BR) AZ1513-04S.R7G SOT23-6L
for 8111H, L340 project

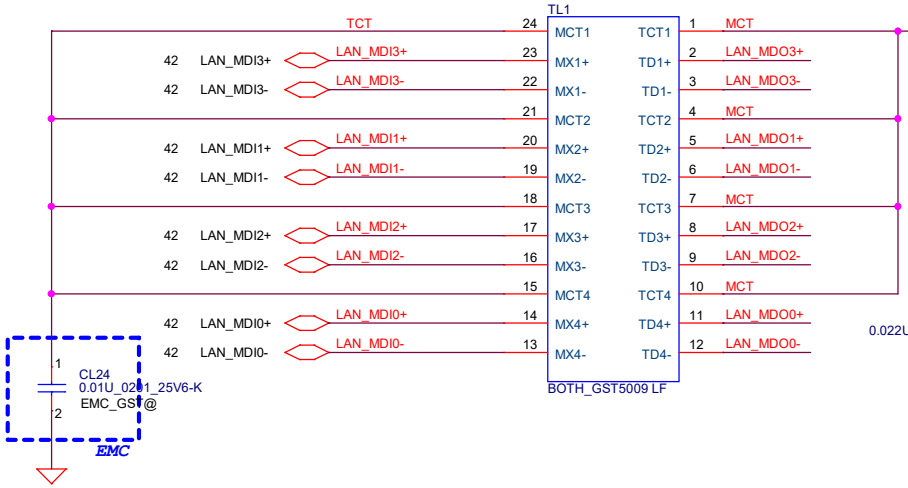


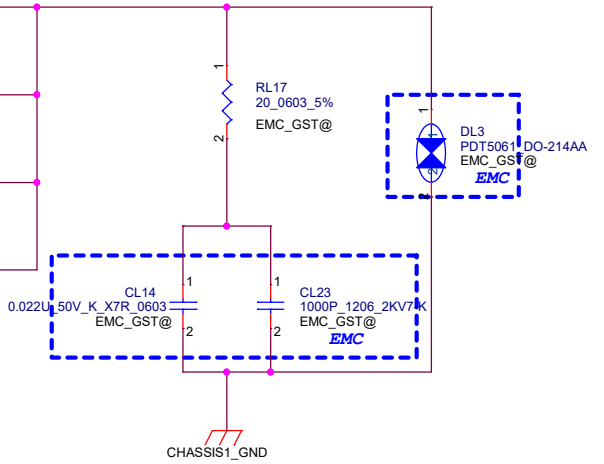


Place Close to TL1 EMC

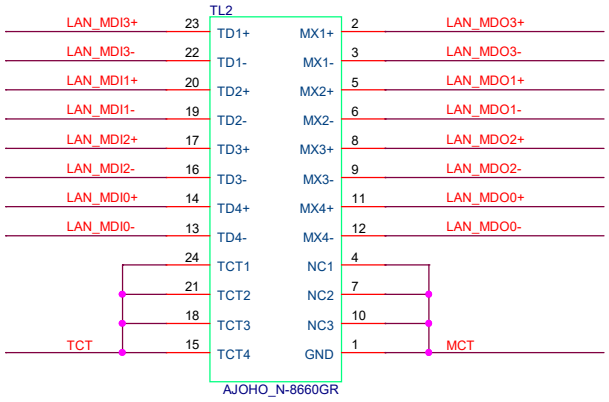
Place Close to TL1 EMC

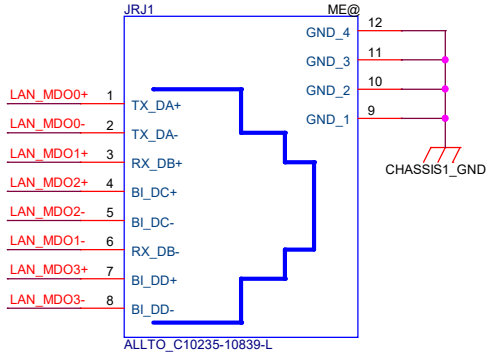






只有 8111H可使用，8111GUL不可用





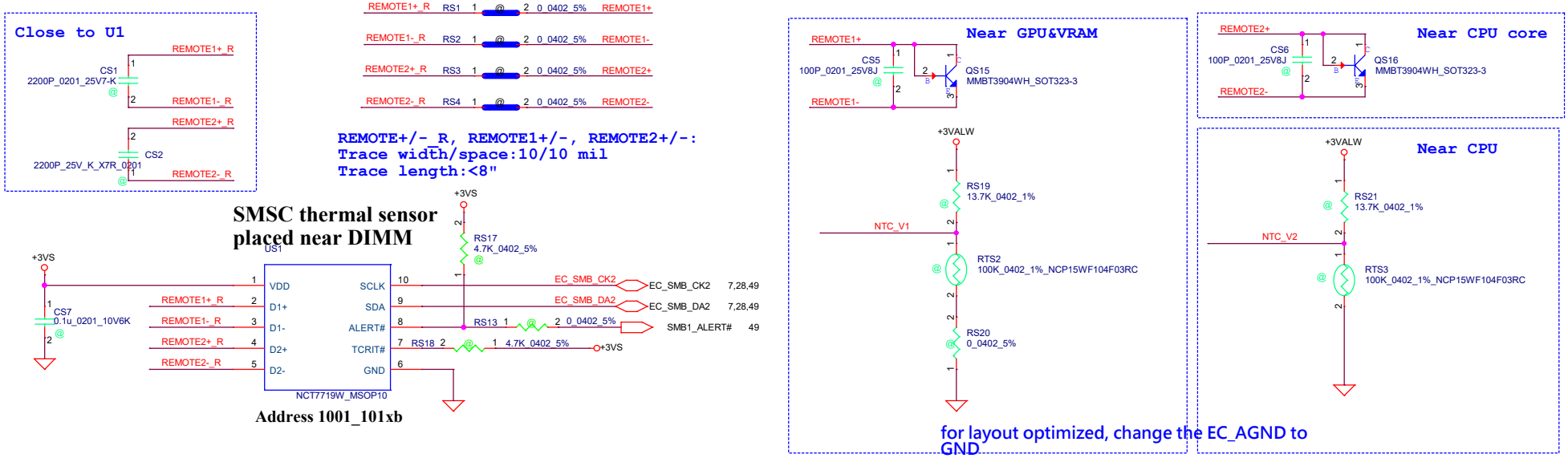
8/16 Update RJ45 P/N DC021608091 wei

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title: LAN_Transformer

Size	Document Number	Rev
B	L350 A+N	1.0

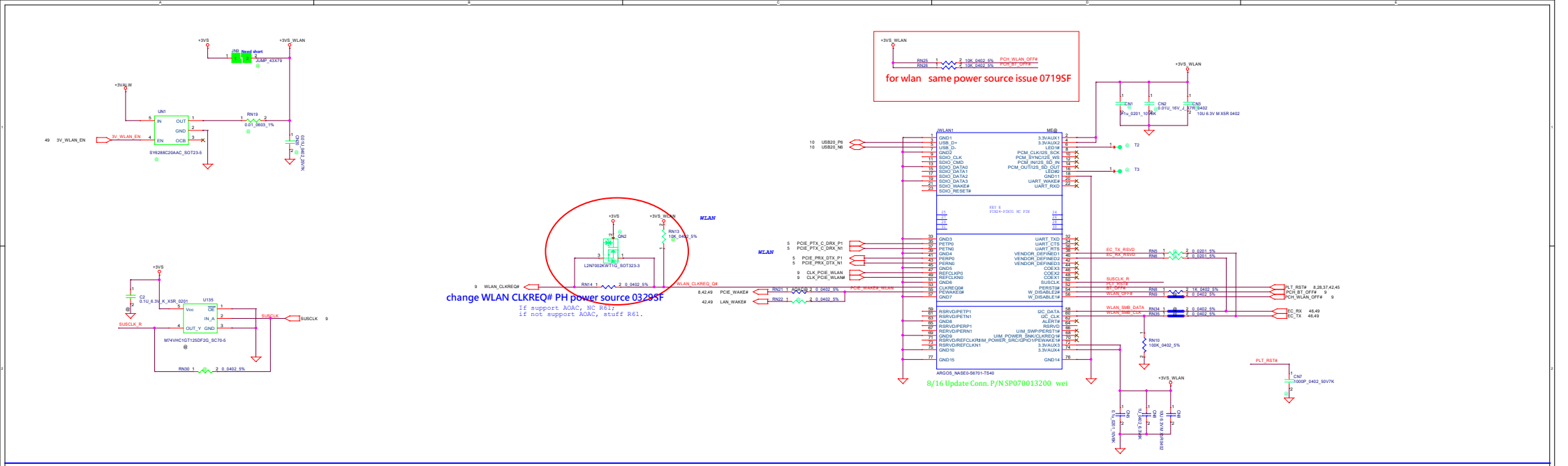
Date: Saturday, May 09, 2020 Sheet 43 of 68

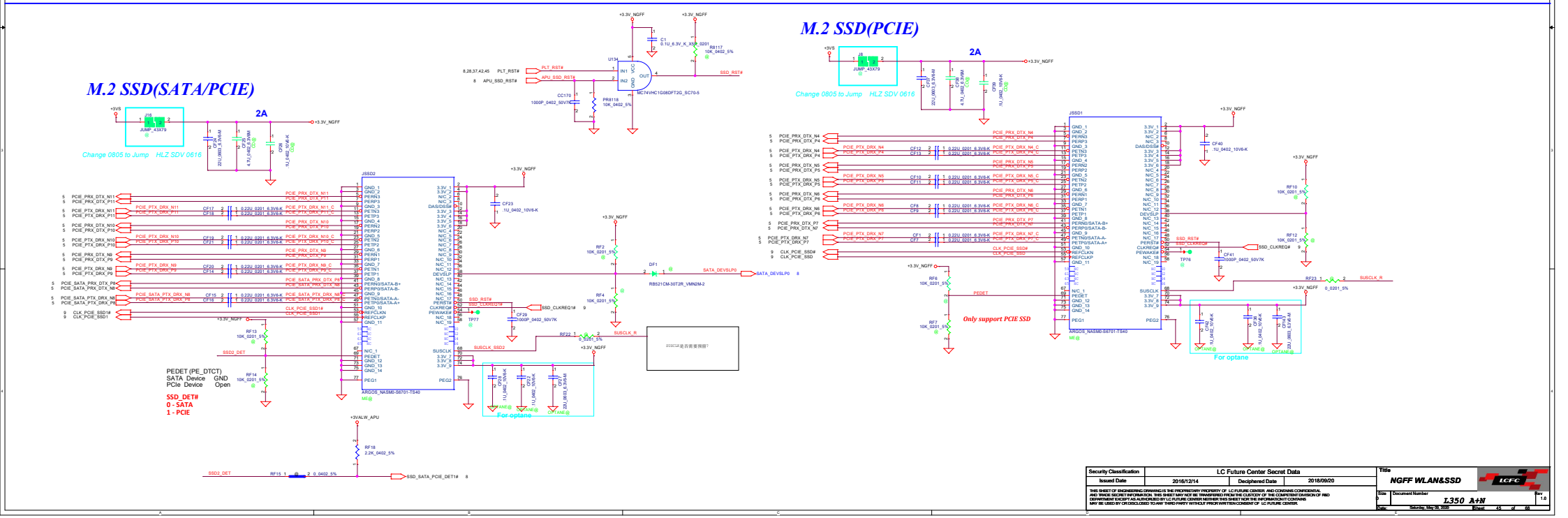


Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2018/09/20

Title: Thermal sensor/FAN CONN

Size: Custom	Document Number: L350 A+N	Rev: 1.0
Date: Saturday, May 09, 2020	Sheet 44 of 68	





Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2016/09/20

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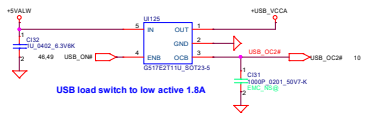
Title: NGFF WLAN&SSD

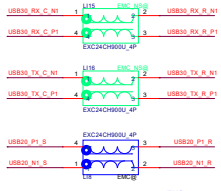
Size: D | Document Number: L350 A+N | Rev: 1.0

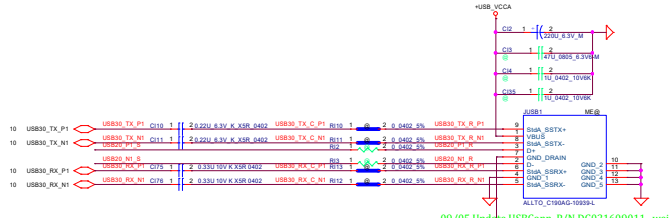
Date: Saturday, May 09, 2020 | Sheet 45 of 68

LEFT SIDE USB3.0 PORT x2

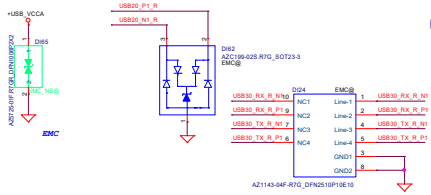


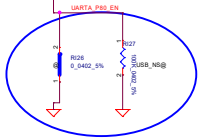
USB load switch to low active 1.8A





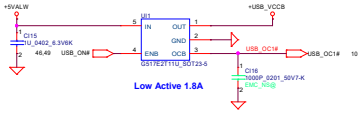
09/05 Update USBConn. P/N DC021609011 wei



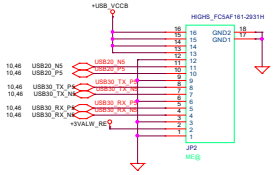


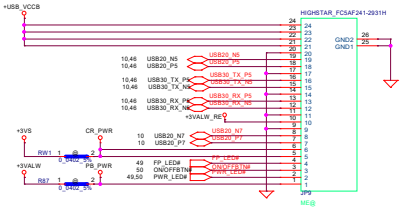
09/20SF Update USB debug CONN GND pin follow TINY5

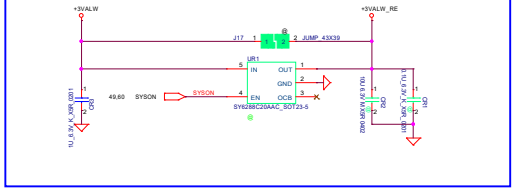
RIGHT SIDE USB3.0 PORT x2



Low Active 1.8A

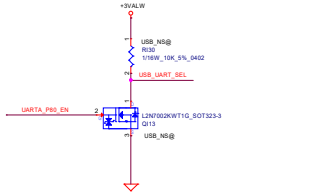


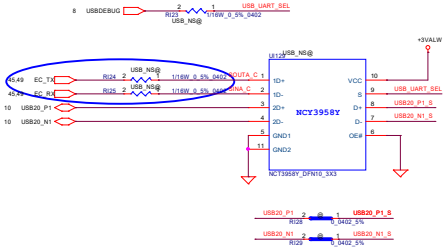




For USB Debug Function 是否有必要

09/20SF add USB debug follow TINY5
change from SA00007WL0D to SA00007WL00 SF1001
SVT non-staff0322SF





USBDEBUG	Kernel debug
Set input	Set input
Set output low	ENABLE

UART4_P80_EN	POST 80
Set input	DISABLE
Set output low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D1+/-1 to D1+/-1
L	H	D1+/-1 to D2+/-1

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/09/20

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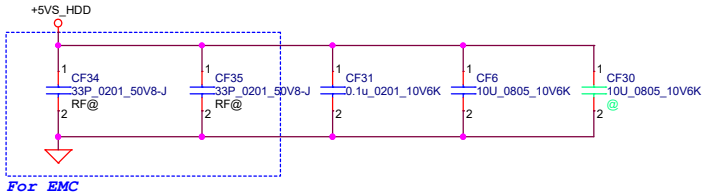
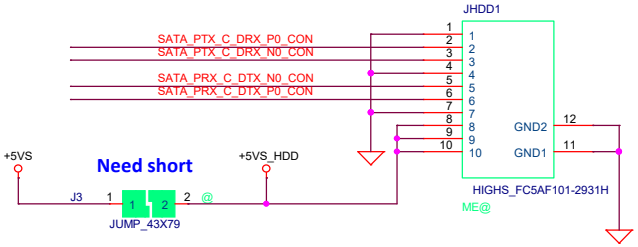
Title: **USB3.0 PORT (LEFT)**

Size: D | Document Number: L350 A+N | Rev: 1.0

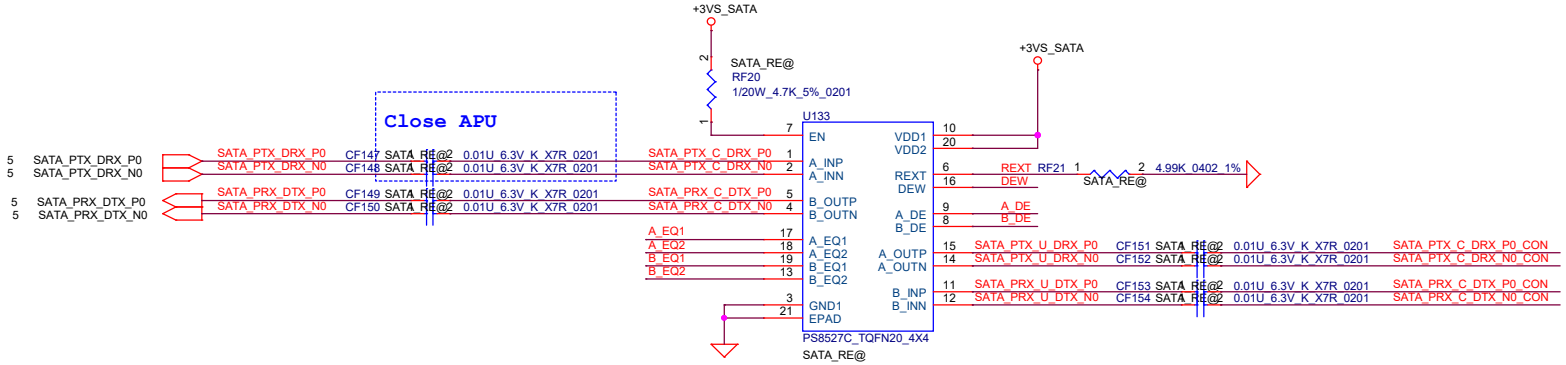
Date: Saturday, May 09, 2020 | Sheet 48 of 68

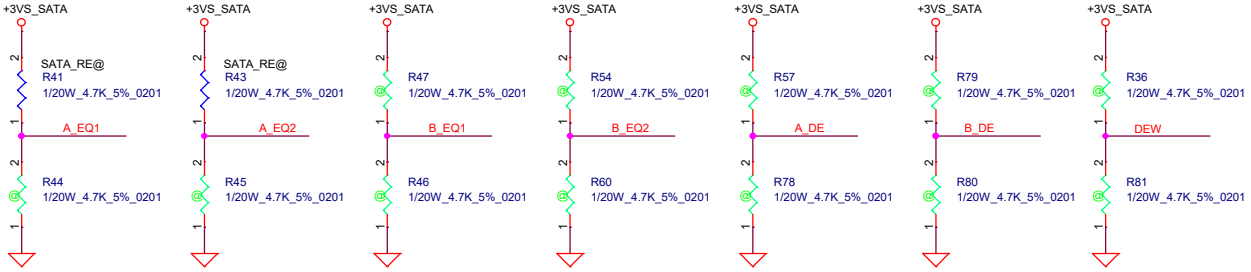
SATA HDD Conn.





SATA HDD Redriver(NEW ADD 20190614)

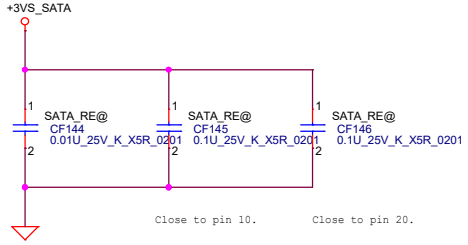




Equalization level setting for Channel x(x=A/B),
internally tied to VDD/2
[x_EQ2, x_EQ1] ==
L/M: for channel loss up to 2.4dB
L/L: for channel loss up to 7.4dB
L/H: for channel loss up to 14.4dB
M/M: for channel loss up to 12.2dB (default)
M/L: for channel loss up to 9.4dB
M/H: for channel loss up to 13.3dB
H/M: for channel loss up to 6.2dB
H/L: for channel loss up to 11.2dB
H/H: for channel loss up to 5dB

De-emphasis level setting for Channel x(x=A/B),
internally tied to VDD/2
[x_DE] ==
M: -3.5dB (default)
L: 0dB
H: -6dB

De-emphasis widith adjustment,
internally pulled down
[DEW] ==
M: for SATA3(default)
L: for SATA3
H: for SATA2



Follow Vendor suggest

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title: **HDD CONN**

Size	Document Number	Rev
Custom	L350 A+N	1.0
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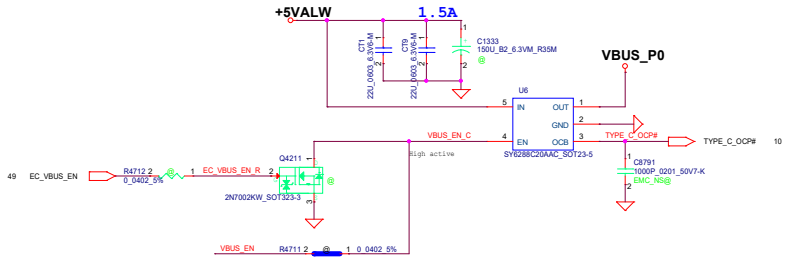
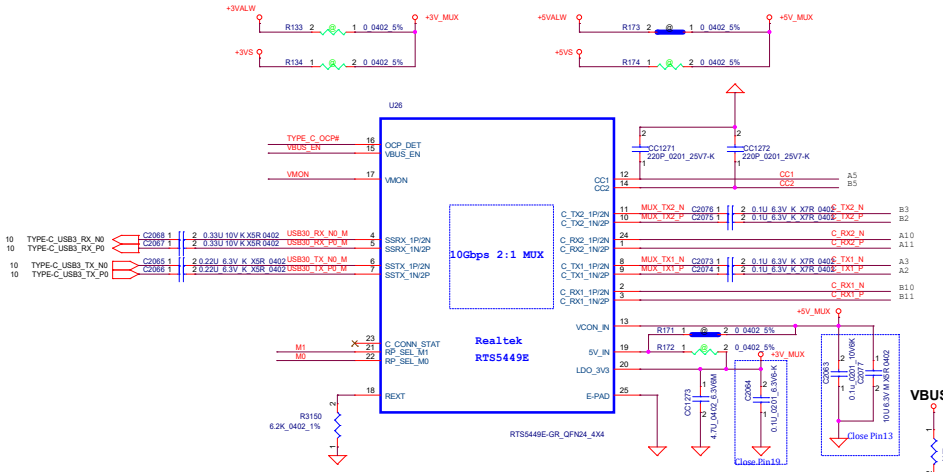
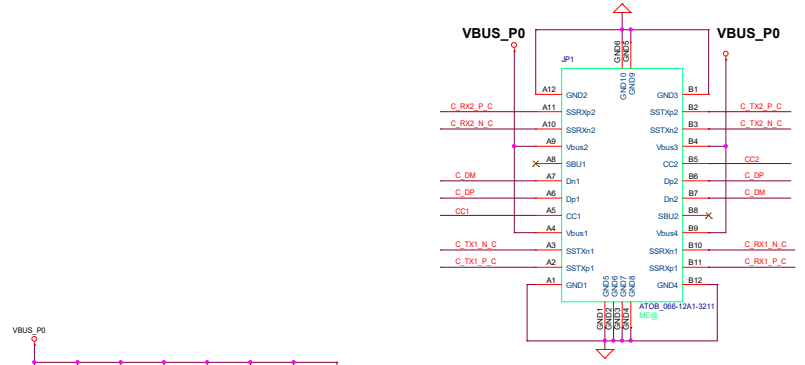
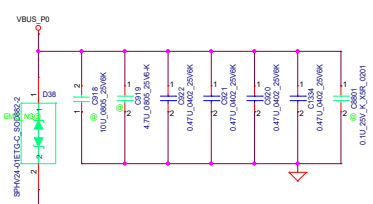
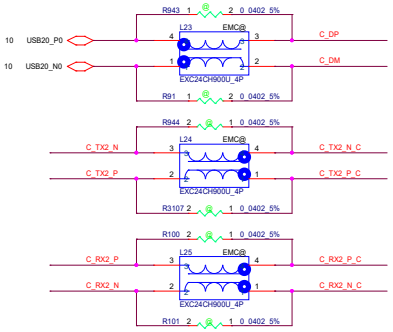
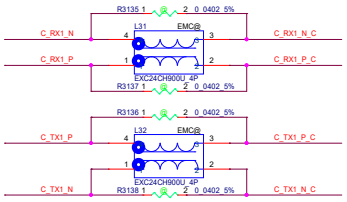


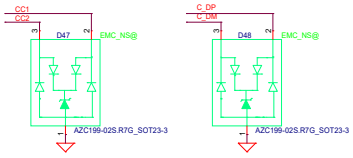




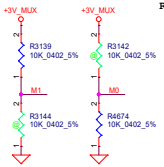








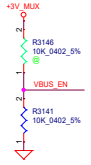
For ESD



Rp configuration

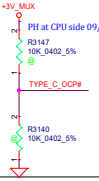
Rp:1.5A (now)

	M1	M0	Note
Rp:900mA	0	1	R3144/R4674 mount
Rp:1.5A	1	0	R3139/R4674 mount
Rp:3.0A	1	1	R3139/R3142 mount



For C_VBUS power switch enable pin

Power switch enable pin	Note
Low Active	R3146 mount
High Active	R3141 mount



For C_VBUS power switch OCP pin

Power switch OCP pin	Note
Low Active	R3147 mount
High Active	R3140 mount

Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title	Type-C RTS5449E
Size	Custom
Document Number	L350 A+N
Rev	1.0
Date:	Saturday, May 09, 2020
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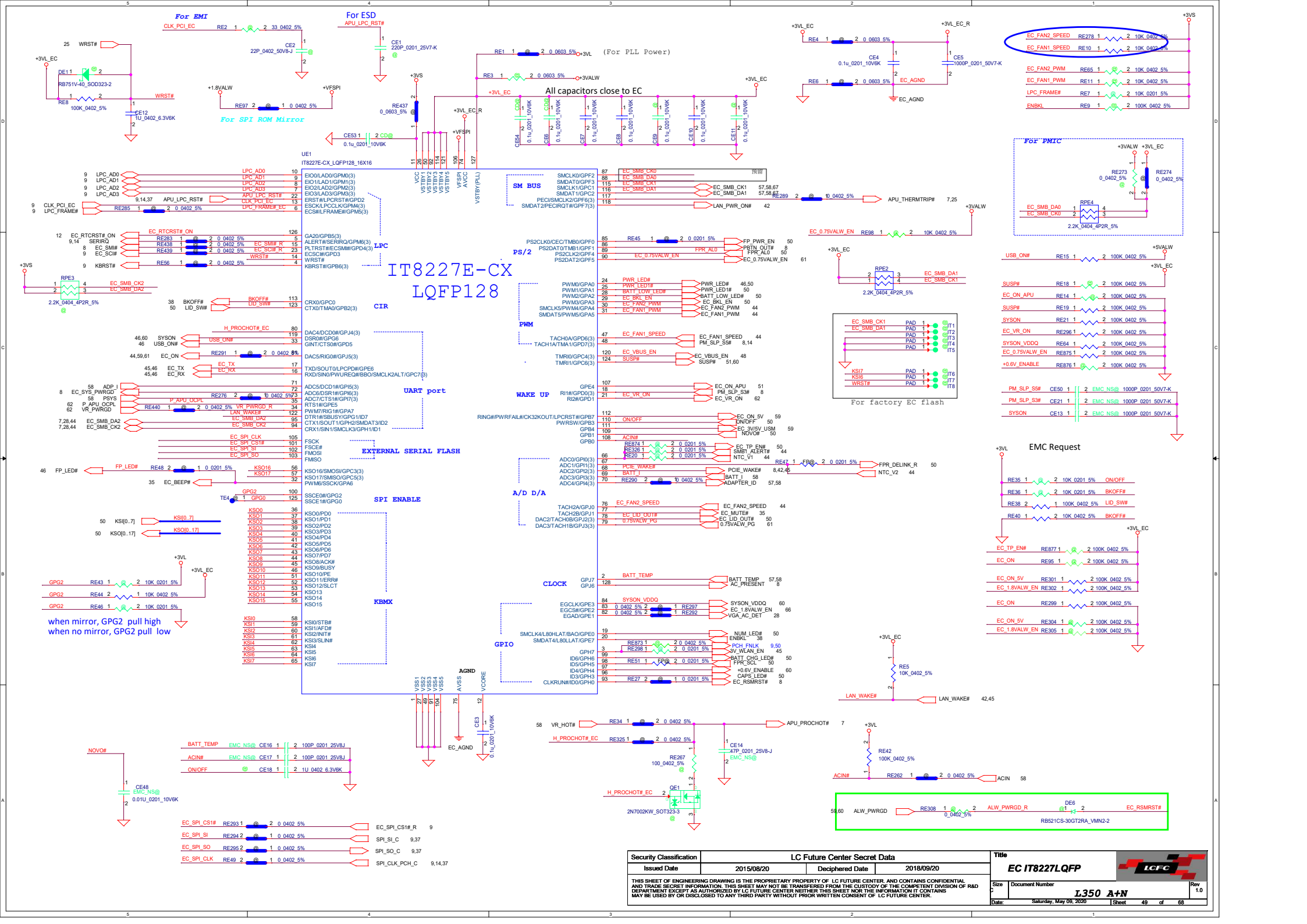
For EMI
For ESD
For PLL Power
All capacitors close to EC
For SPI ROM Mirror
For PMIC
For factory EC flash
EMC Request
IT8227E-CX
LQFP128
SM BUS
LPC
PS/2
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
A/D D/A
CLOCK
GPIO
KBMX
CIR
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
Security Classification
LC Future Center Secret Data
Issued Date
2015/08/20
Deciphered Date
2018/09/20
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Title
EC IT8227LQFP
Size
C
Document Number
L350 A+N
Rev
1.0
Date:
Saturday, May 09, 2020
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of
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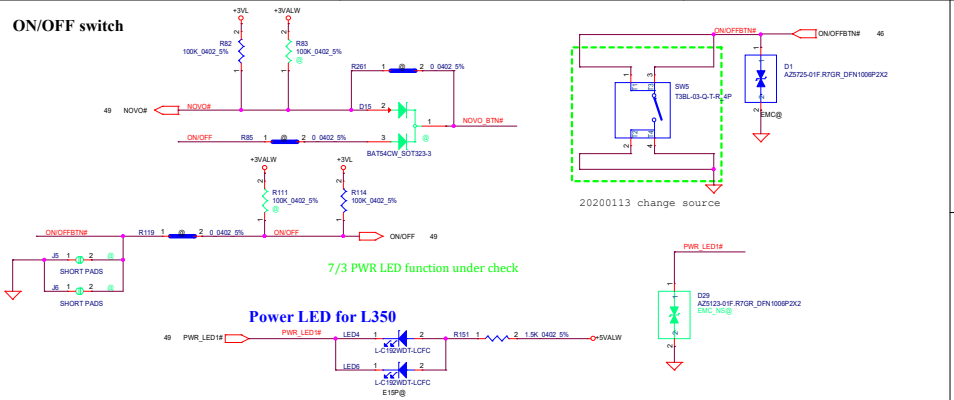
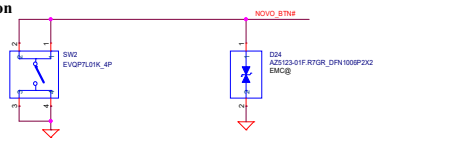
ON/OFF switch

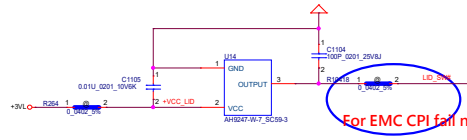


Novo button

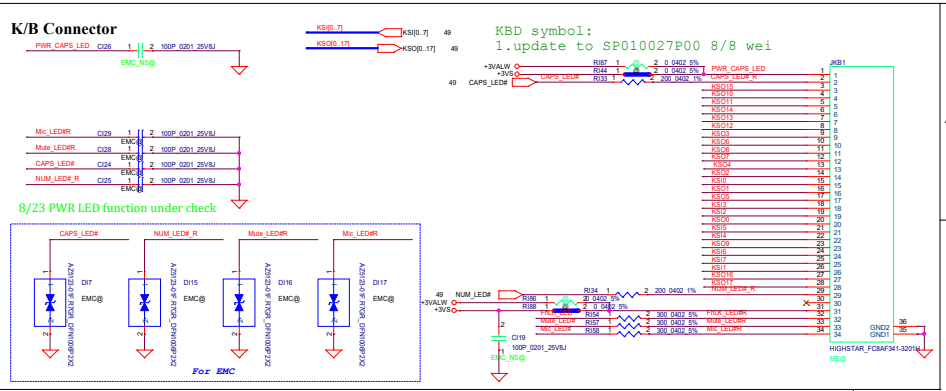


8/31 Update the P/N SN100008W00 wei

LID switch

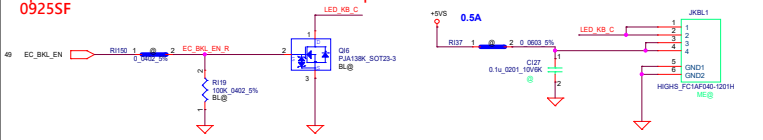


K/B Connector

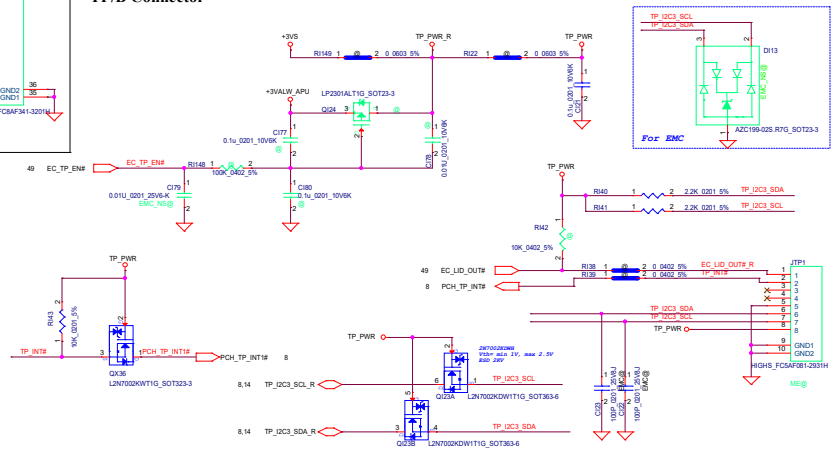


KB Backlight Connector

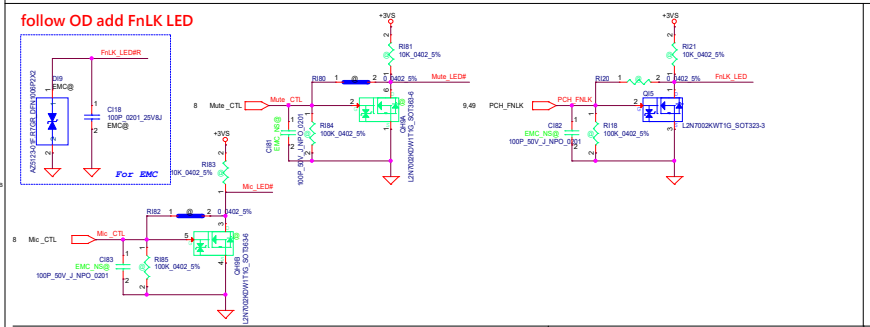
update BL circuit and need too be confirm conn pin define
0925SF

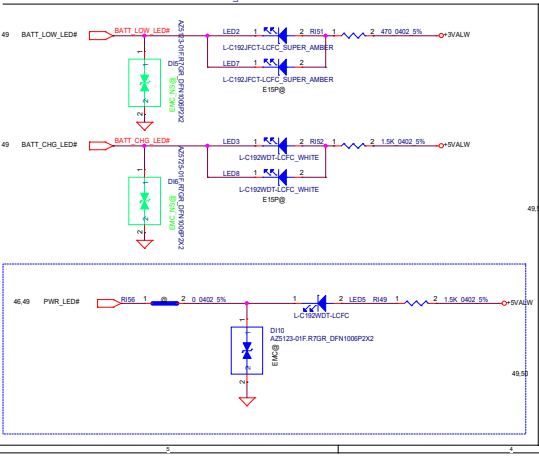


TP/B Connector

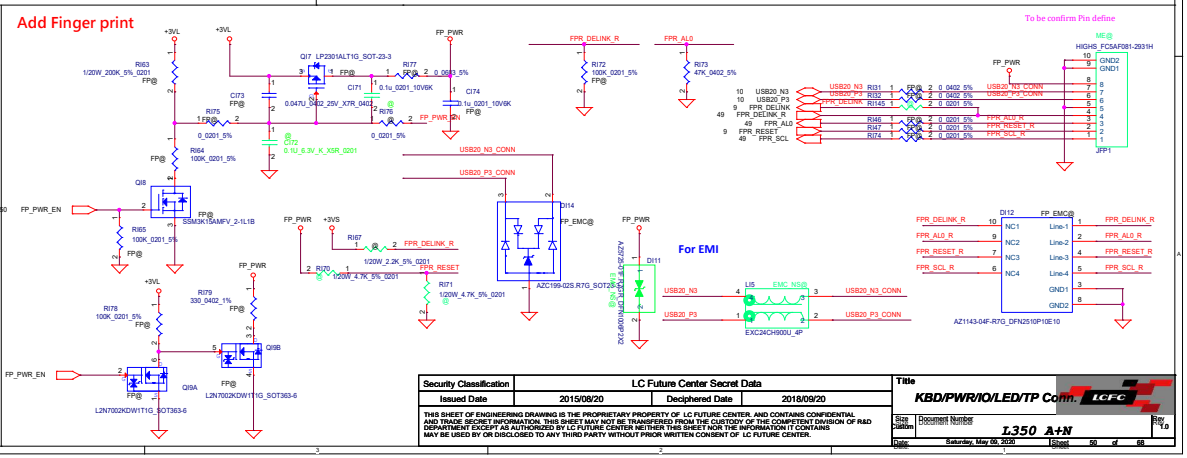


follow OD add FnLK LED





Add Finger print



Security Classification	LC Future Center Secret Data	
Issued Date	2015/08/20	Deciphered Date 2018/09/20

Title: KBD/PWR/IO/LED/TP Conn.

Size: Custom | Document Number: L350 A+N | Rev: 1.0

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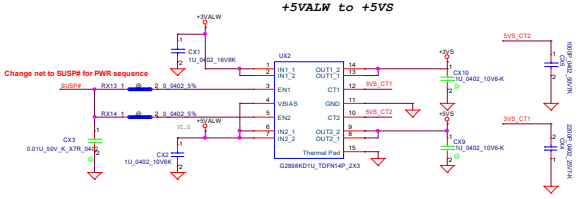

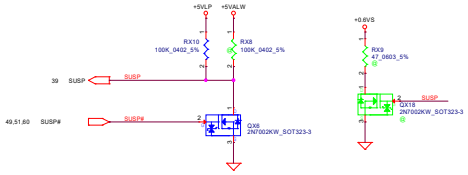

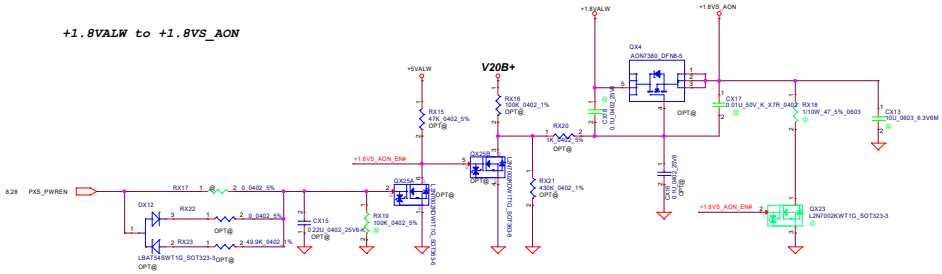

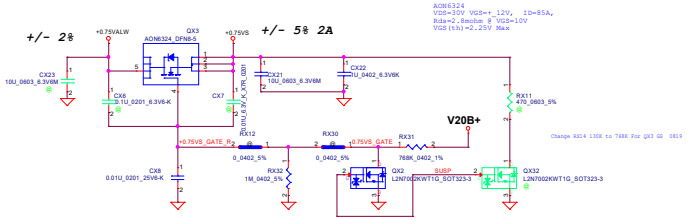

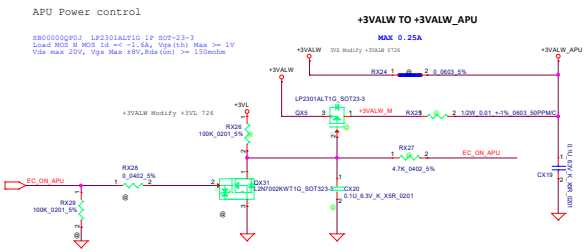

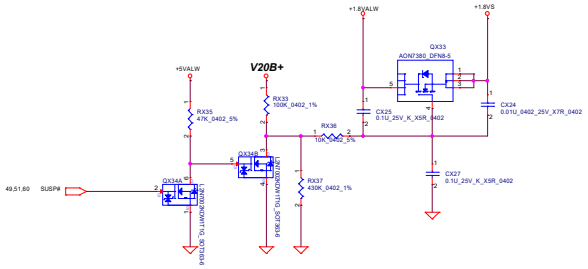

Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2019/07/02

Title	DC V TO VS INTERFACE		
Size	Document Number		Rev
D	L350 A+N		1.0
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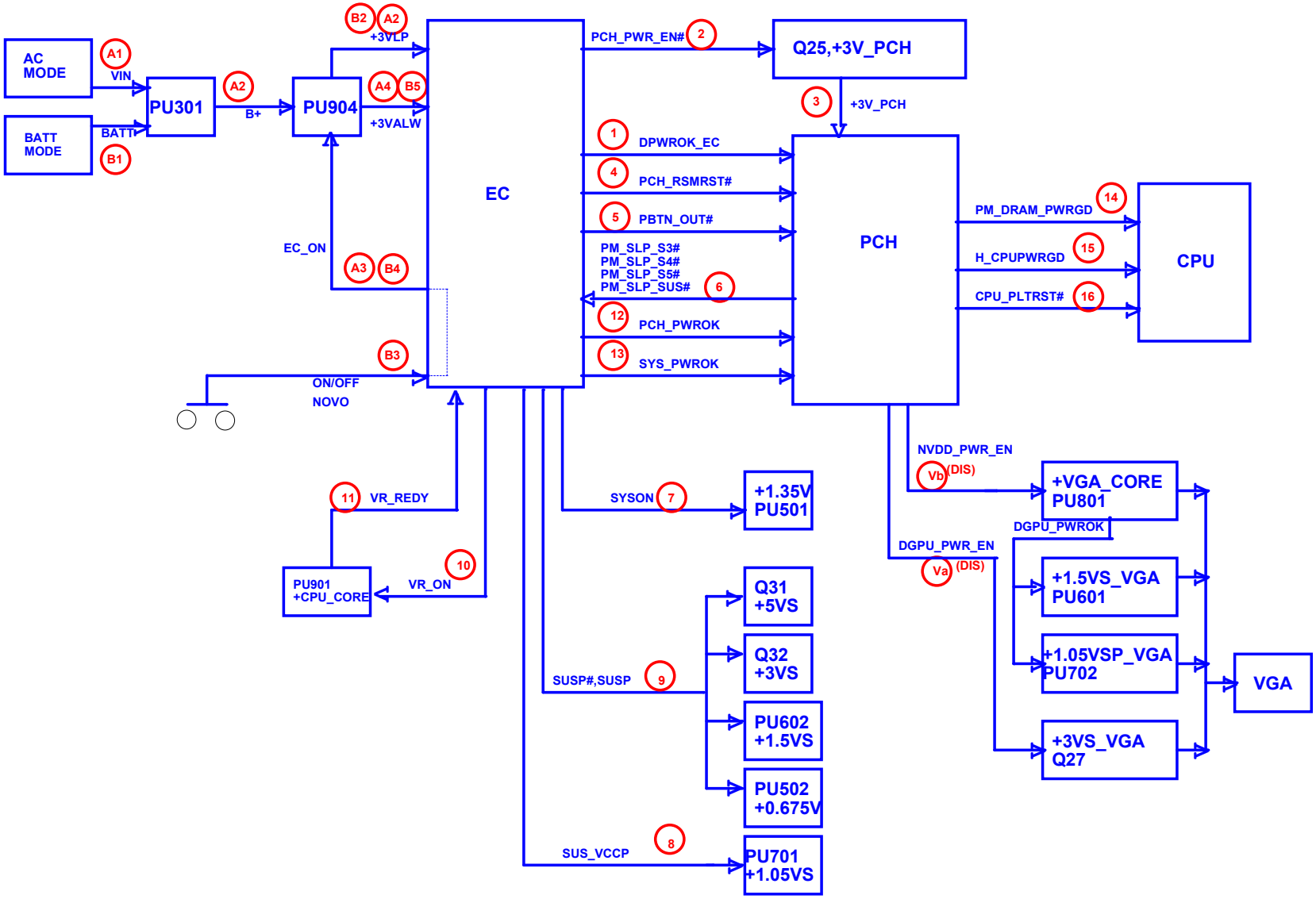

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title: **Power sequence block**

Size	Document Number	Rev
Custom	L350 A+N	1.0

Date: Saturday, May 09, 2020 Sheet 52 of 68

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title

Virtual symbol

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GPU Thermal Holex2 Close to RJ45 DC-IN x2

CPU Thermal Holex3 WLAN Standoff

PCB Fedical Mark PAD

FD1 FD2 FD3 FD4 FD5 FD6

H1 HOLEA PAD_D2P4
H2 HOLEA PAD_D2P4
H3 HOLEA PAD_D2P4
H10 HOLEA PAD_D2P4
H11 HOLEA PAD_D3P0X2P7
H4 HOLEA PAD_CT7P0B6P0D3P0
H5 HOLEA PAD_CT7P0B6P0D3P0
H6 HOLEA PAD_CT7P0B6P0D3P0
H7 HOLEA PAD_D2P7
H8 HOLEA PAD_CT7P0B6P0D3P0
H9 HOLEA PAD_C2P7D2P7N
H12 HOLEA PAD_C7P0D2P8
H15 HOLEA PAD_C7P0D3P3
H20 HOLEA PAD_C6P0D2P4
20200115 add
H13 HOLEA PAD_CT7P0B6P0D3P0
H16 HOLEA PAD_CT7P0B6P0D2P8
H17 HOLEA PAD_C7P0D2P8
H18 HOLEA PAD_O9P5X7D5P3X2P8
H19 HOLEA PAD_CT7P0B6P0D3P0

Close to Audio jack

follow layout list update 20190819 weiwei

USB3.0 Shielding

SH7 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH8 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH9 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH10 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH11 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH12 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P

DDR4 Shielding

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title: Hole

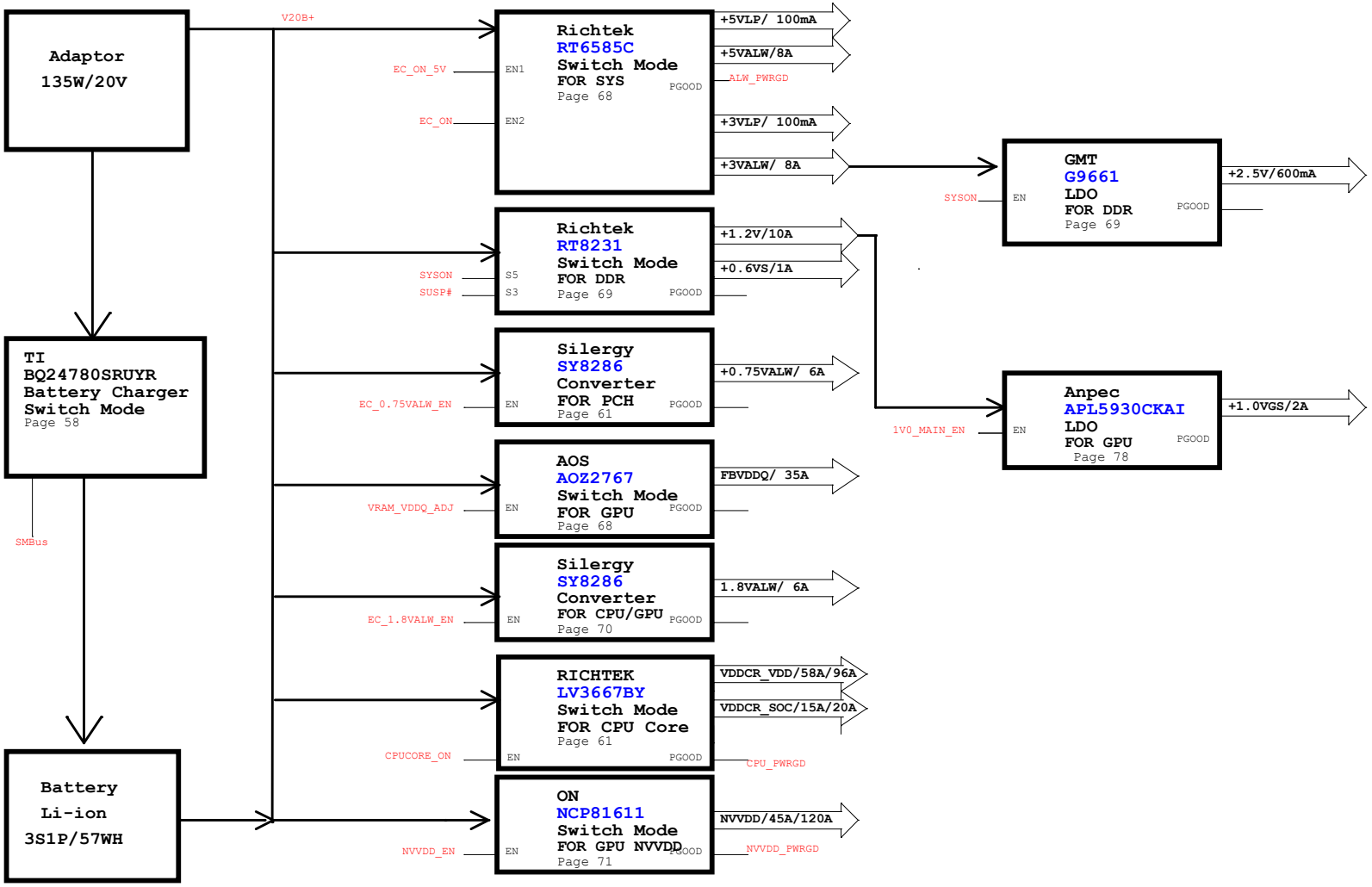
Size: B | Document Number: L350 A+N | Rev: 1.0

Date: Saturday, May 09, 2020 | Sheet 54 of 68

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/09/20

Title: XXX

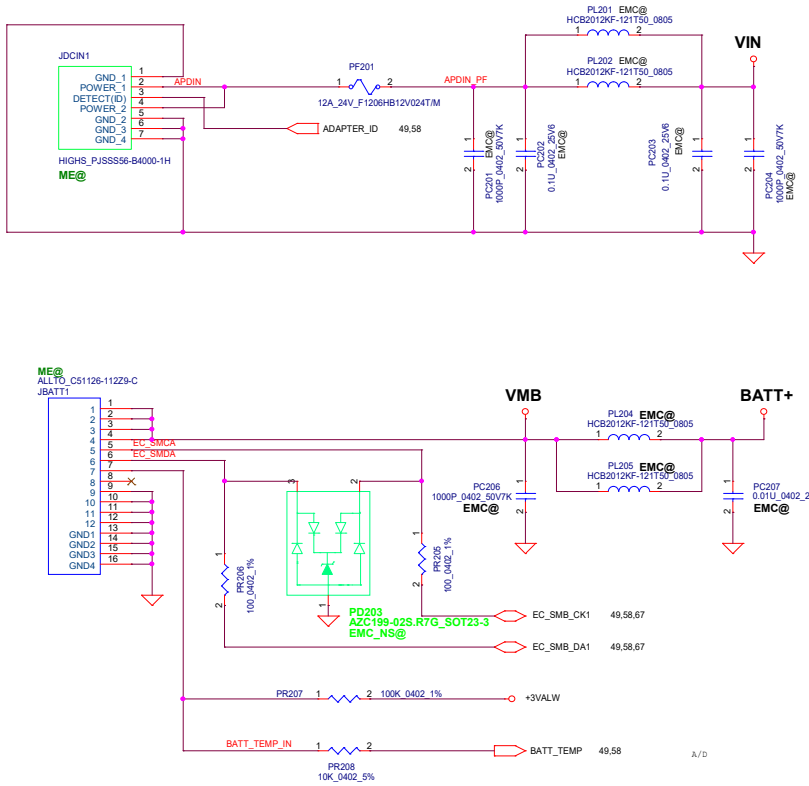
Size: D	Document Number: L350 A+N	Rev: 1.0
Date: Saturday, May 09, 2020	Sheet 55 of 68	

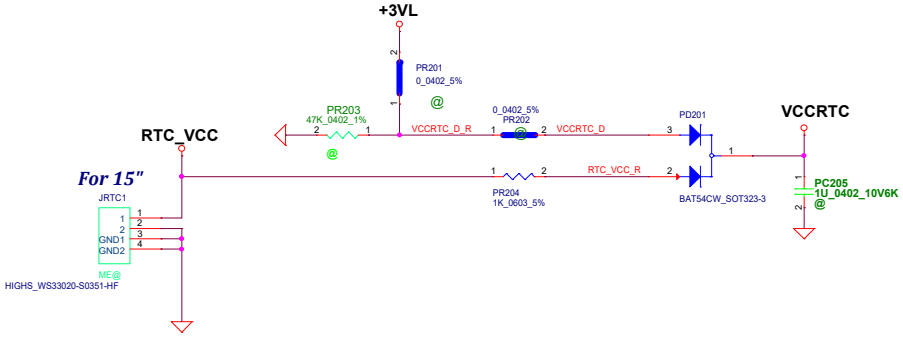


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR-Power Diagram

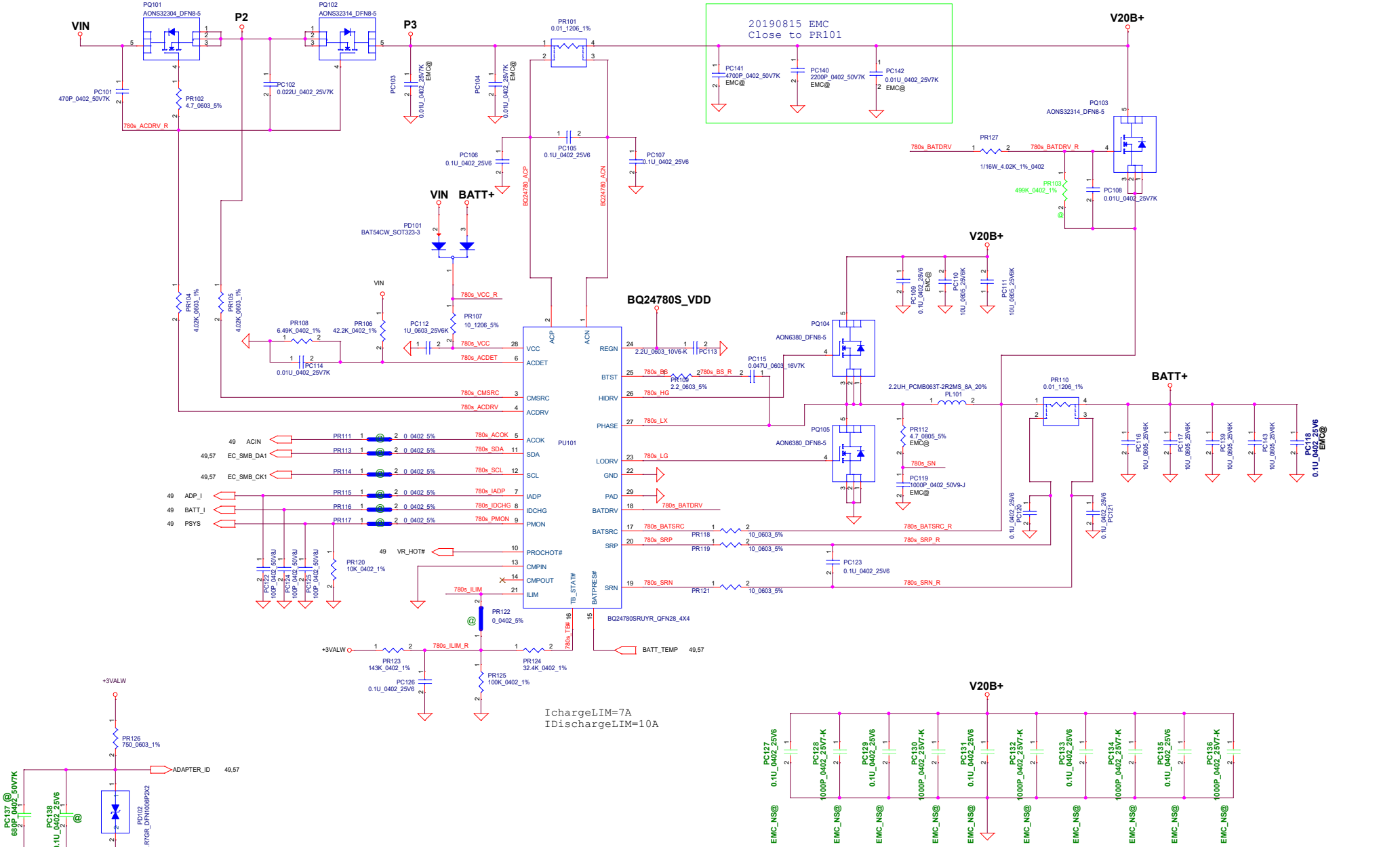
Size: Custom	Document Number: L350 A+N	Rev: 1.0
Date: Saturday, May 09, 2020	Sheet 56 of 68	





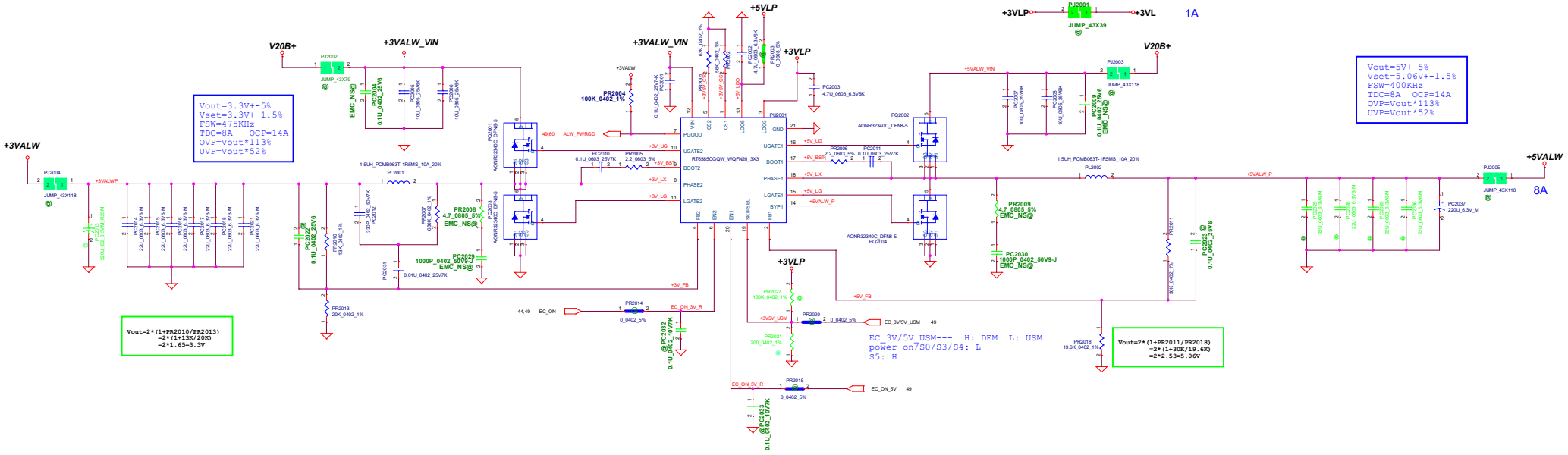
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-DCIN /BATT/ RTC charg		
Size C	Document Number L350 A+N		Rev 1.0
Date: Saturday, May 09, 2020		Sheet 57 of 68	



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	Charger-BQ24780SRUYR		
Size: Custom	Document Number: L350 A+N		Rev: 1.0
Date: Saturday, May 09, 2020	Sheet 58 of 68		



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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Title: PWR-3V/5V-RT6585BGQW

Size	Document Number	Rev
Custom	L350 A+N	1.0

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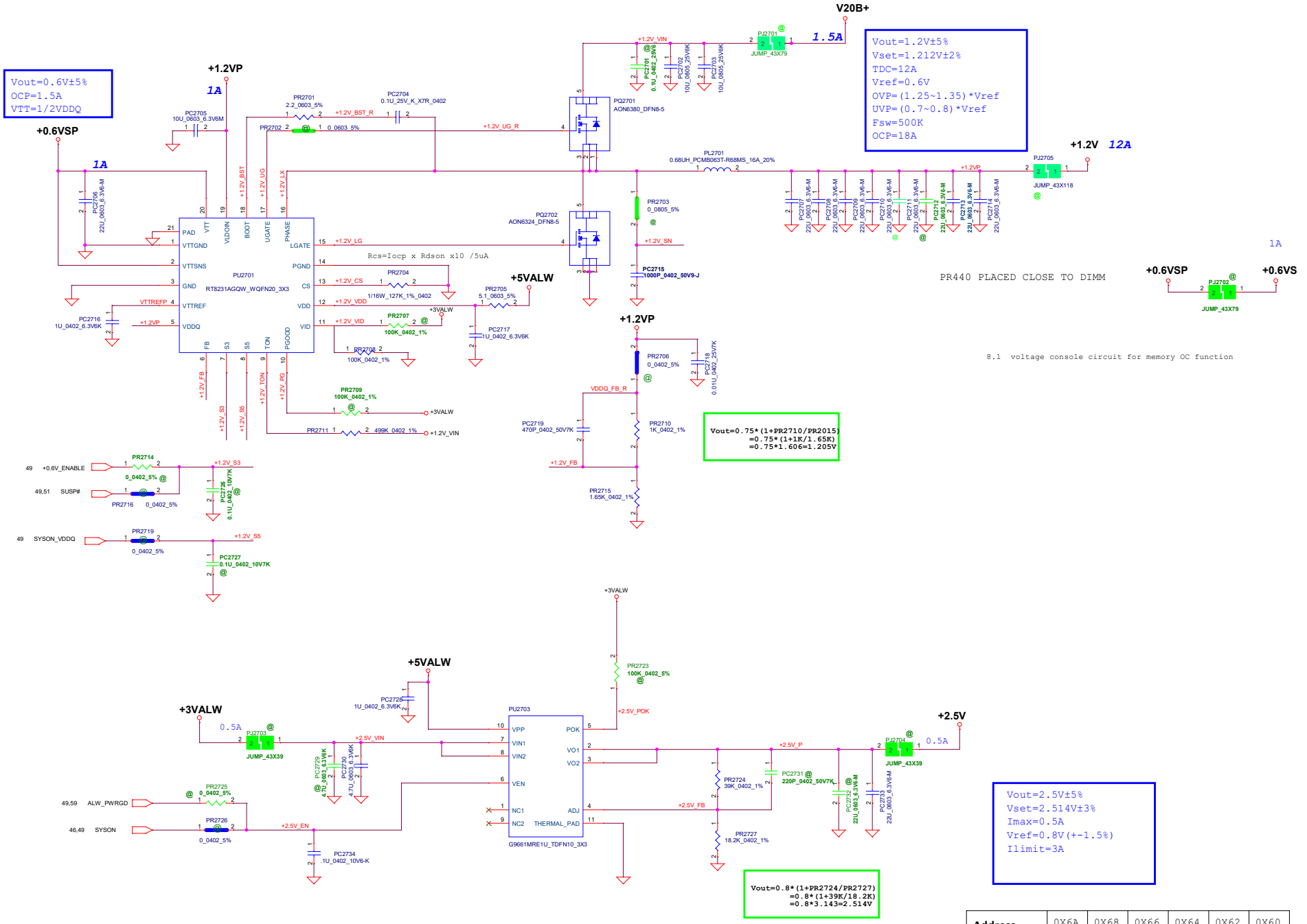


STATE	EN1	EN2	VDDQ	VTT_REFP	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

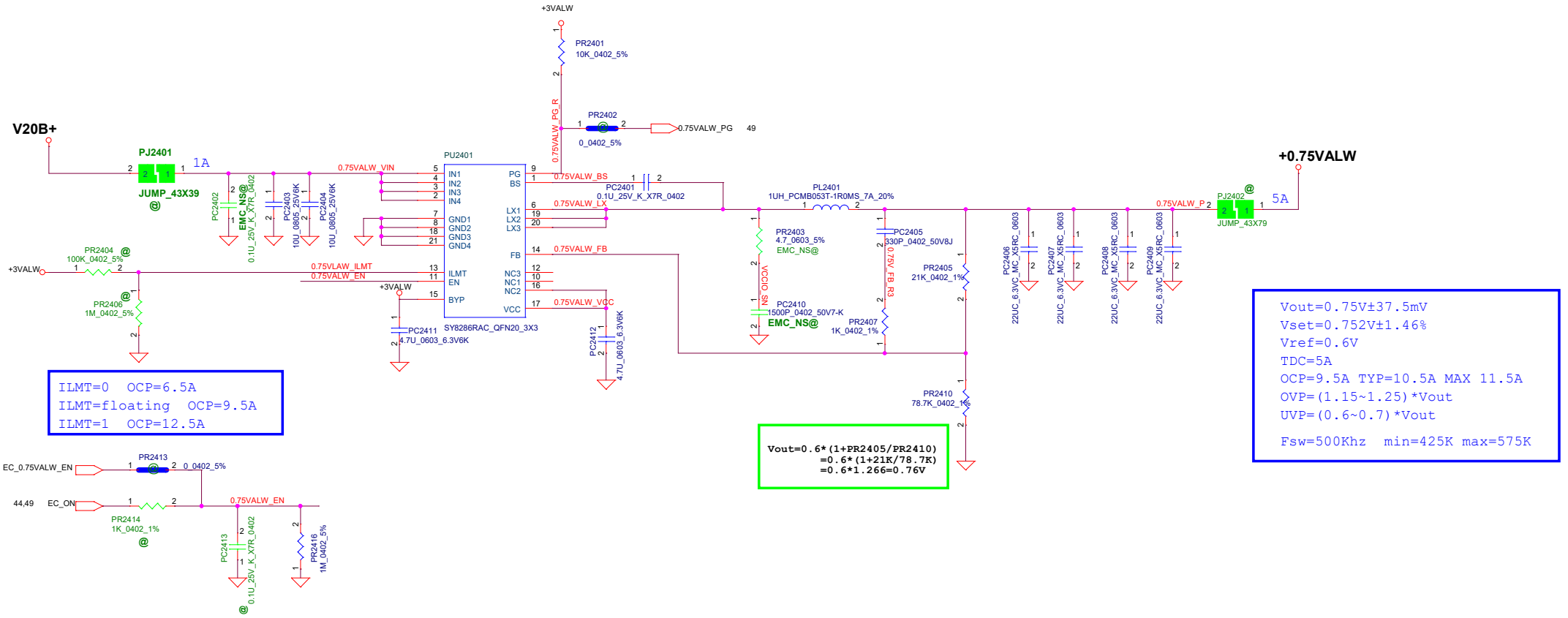
Note: S3 - sleep ; S5 - power off

Address	0X6A	0X68	0X66	0X64	0X62	0X60
TOP R (Kohm)	OPEN	3.9	3	2.3	1.3	10
BOT R (Kohm)	10	1.3	2.3	3	3.9	OPEN
Bus_sel Volt (% of VCC)	0%	25%	40%	60%	75%	100%

Title: PWR-1.2V/0.6VS/2.5V-RT8231

Size: Custom | Document Number: L350 A+N | Rev: 1.0

Date: Saturday, May 09, 2020 | Sheet 60 of 68



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-VCCIO**

Size	Document Number	Rev
Custom	L350 A+N	1.0

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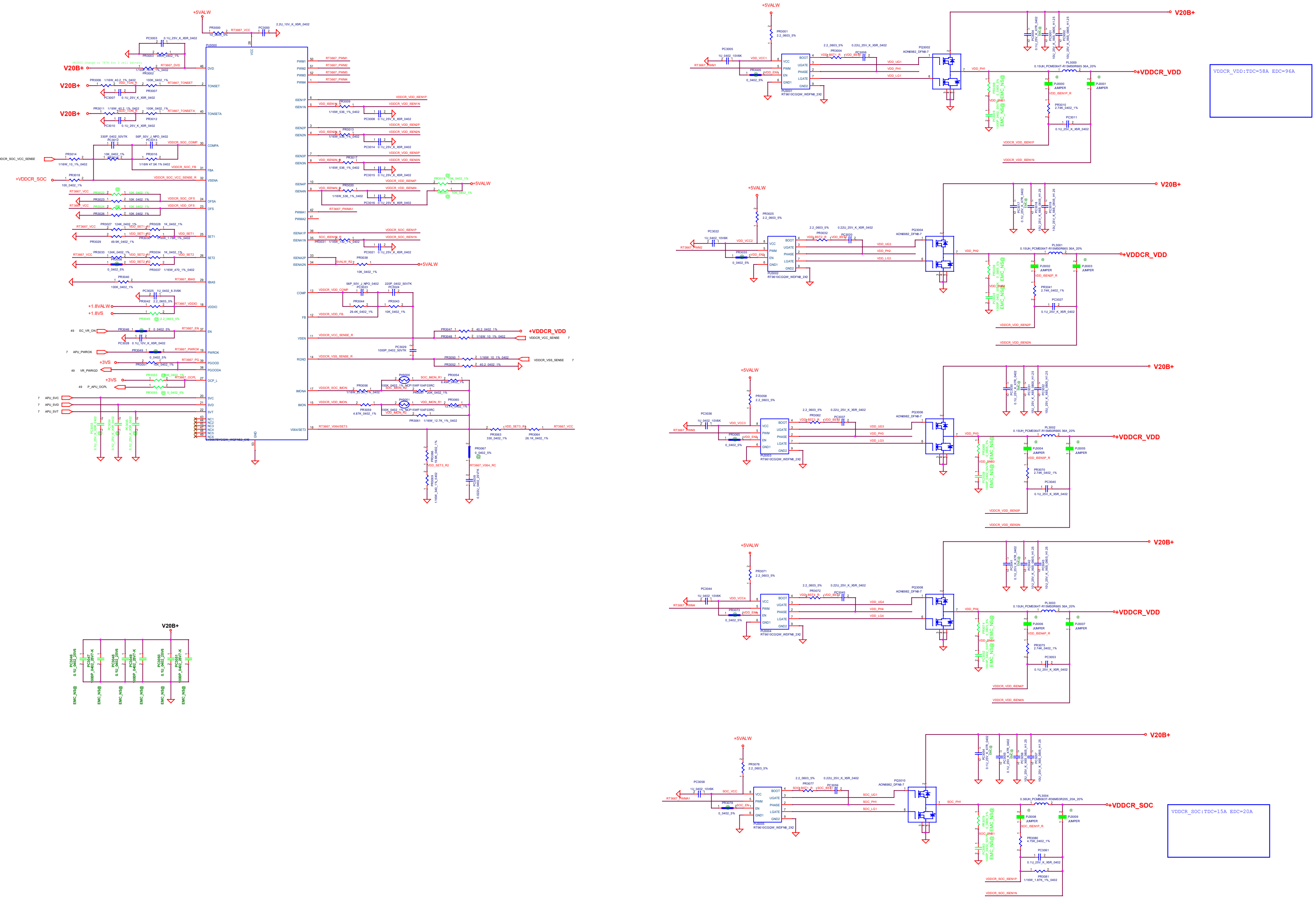

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VDDCR_SOC:TDC=15A EDC=20A

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

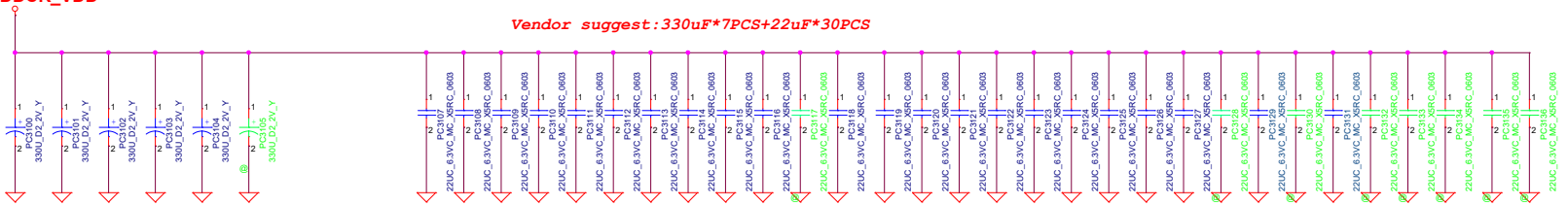
Title: PWR_VDD/SOC

LCFC

Size: Custom | Document Number: L350 A+N | Rev 1.0

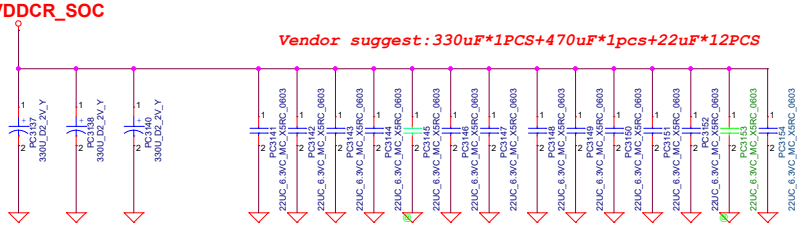
+VDDCR_VDD

*Vendor suggest:330uF*7PCS+22uF*30PCS*



+VDDCR_SOC

*Vendor suggest:330uF*1PCS+470uF*1pcs+22uF*12PCS*



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: PWR_VDD/SOC

Size: A2 | Document Number: L350 A+N | Rev: 1.0

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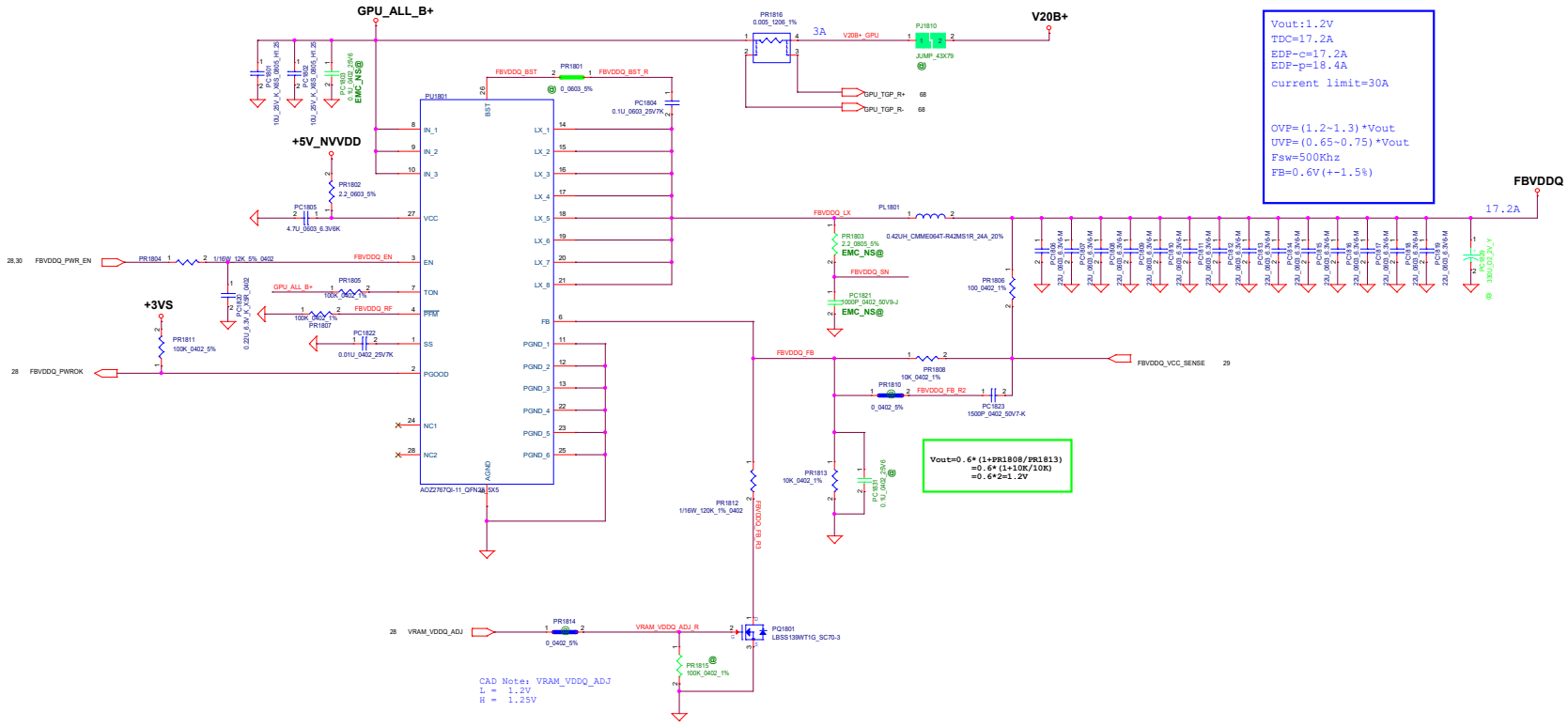
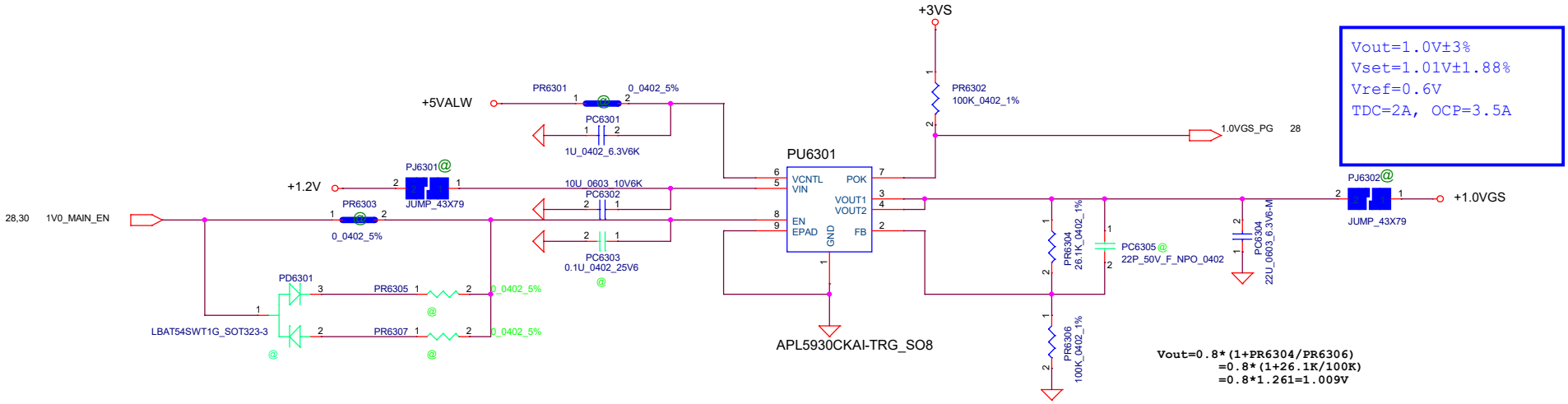


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-FBVDDQ-AOZ2767QI		
Size: Custom	Document Number: L350 A+N		Rev: 1.0
Date: Saturday, May 09, 2020	Sheet 64 of 68		

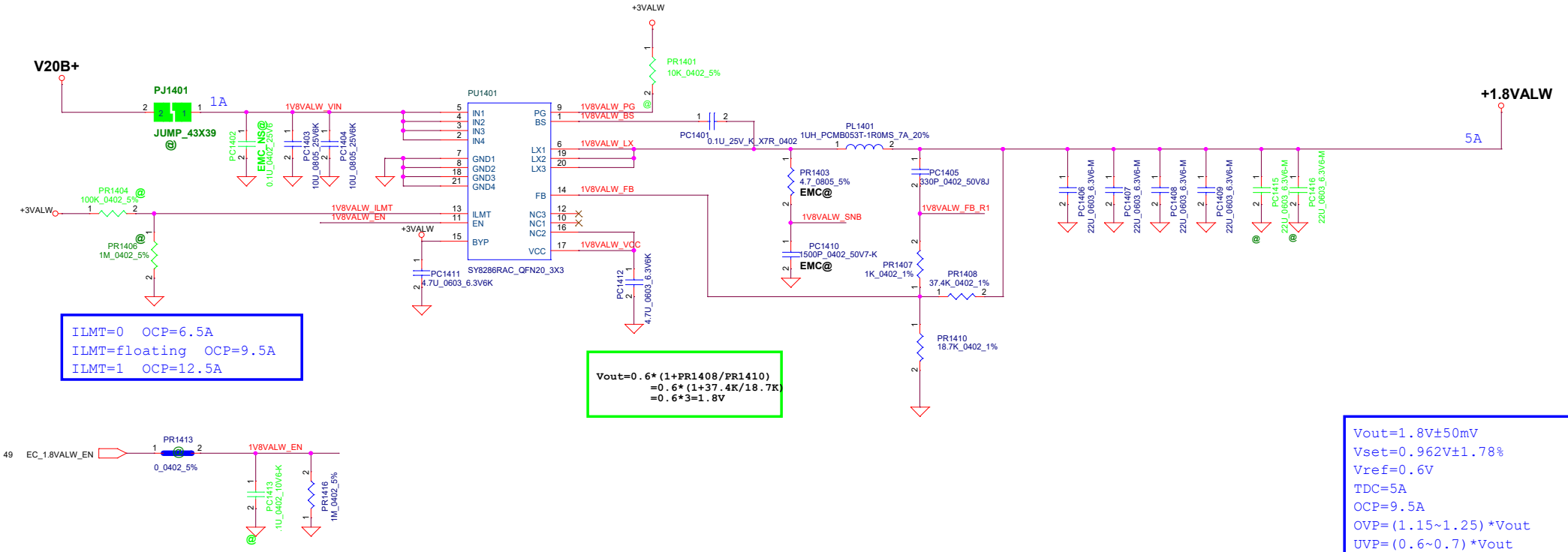


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR-+1.0VGS-APL5930

Size	Document Number	Rev
Custom	L350 A+N	1.0

Date: Saturday, May 09, 2020 Sheet 65 of 68



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR-VCCIO-SY8286RAC

Size	Document Number	Rev
Custom	L350 A+N	1.0

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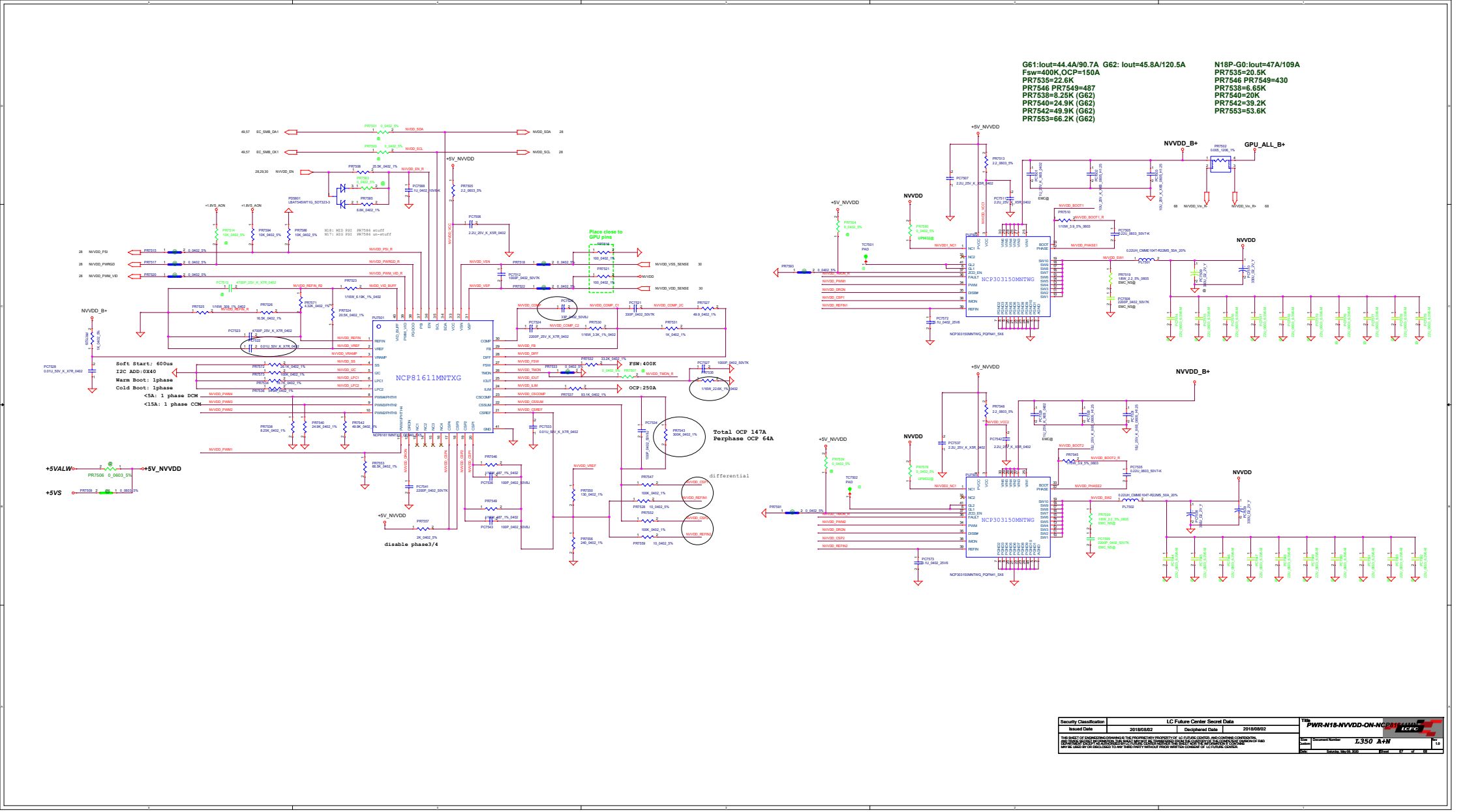

Security Classification	LC Future Center Secret Data		Title: PWR-N18-NVVDD-ON-NCP81611MNTXG
Issued Date	2018/08/02	Deciphered Date	2018/08/02
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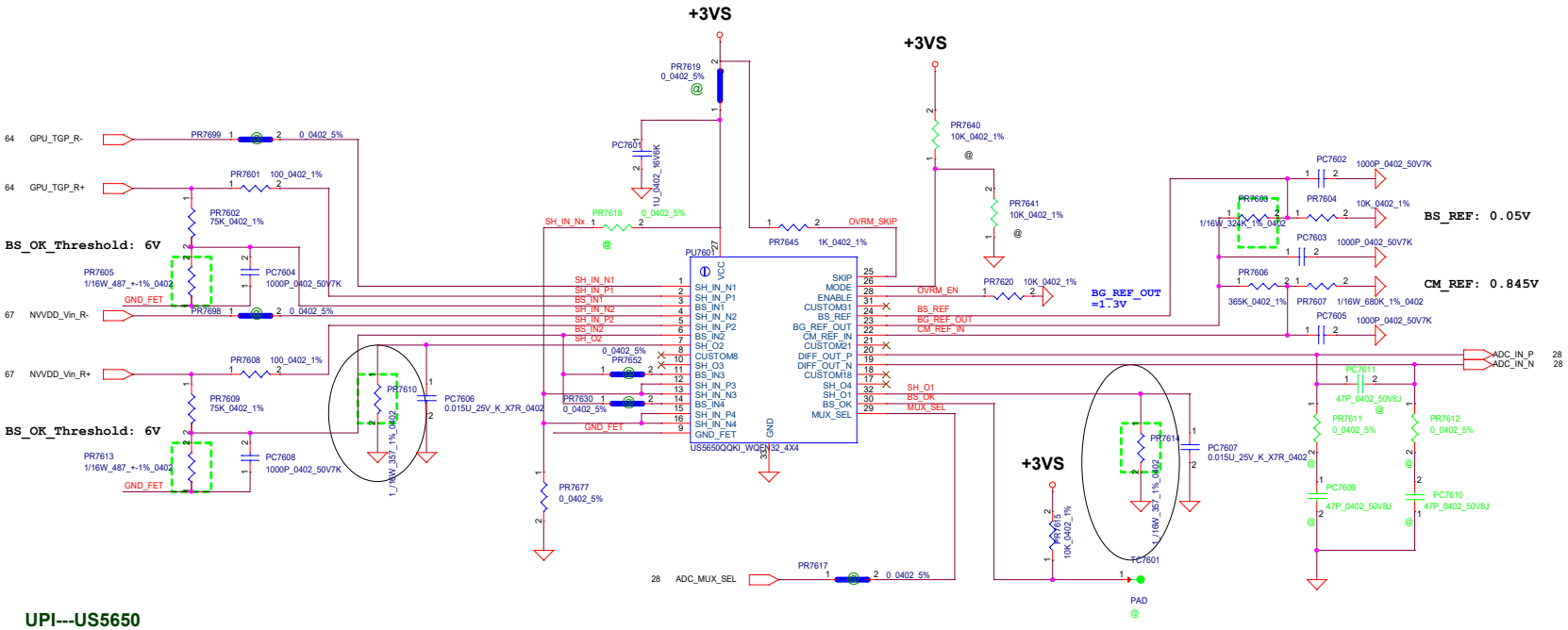
			Date: Saturday, May 09, 2020 Sheet 67 of 68



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PR7605=487
PR7613=487
PR7610=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
PR7614=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
PR7603=324K
PR7602=75K
PR7609=75K
PC7604=1nF
PC7608=1nF

ON---NCP45491
PR7605=649
PR7613=649
PR7610=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
PR7614=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
PR7603=243K
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PC7604=1nF
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Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-N18-OVRM&IIC-US5650		
Size C	Document Number L350 A+N		Rev 1.0
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