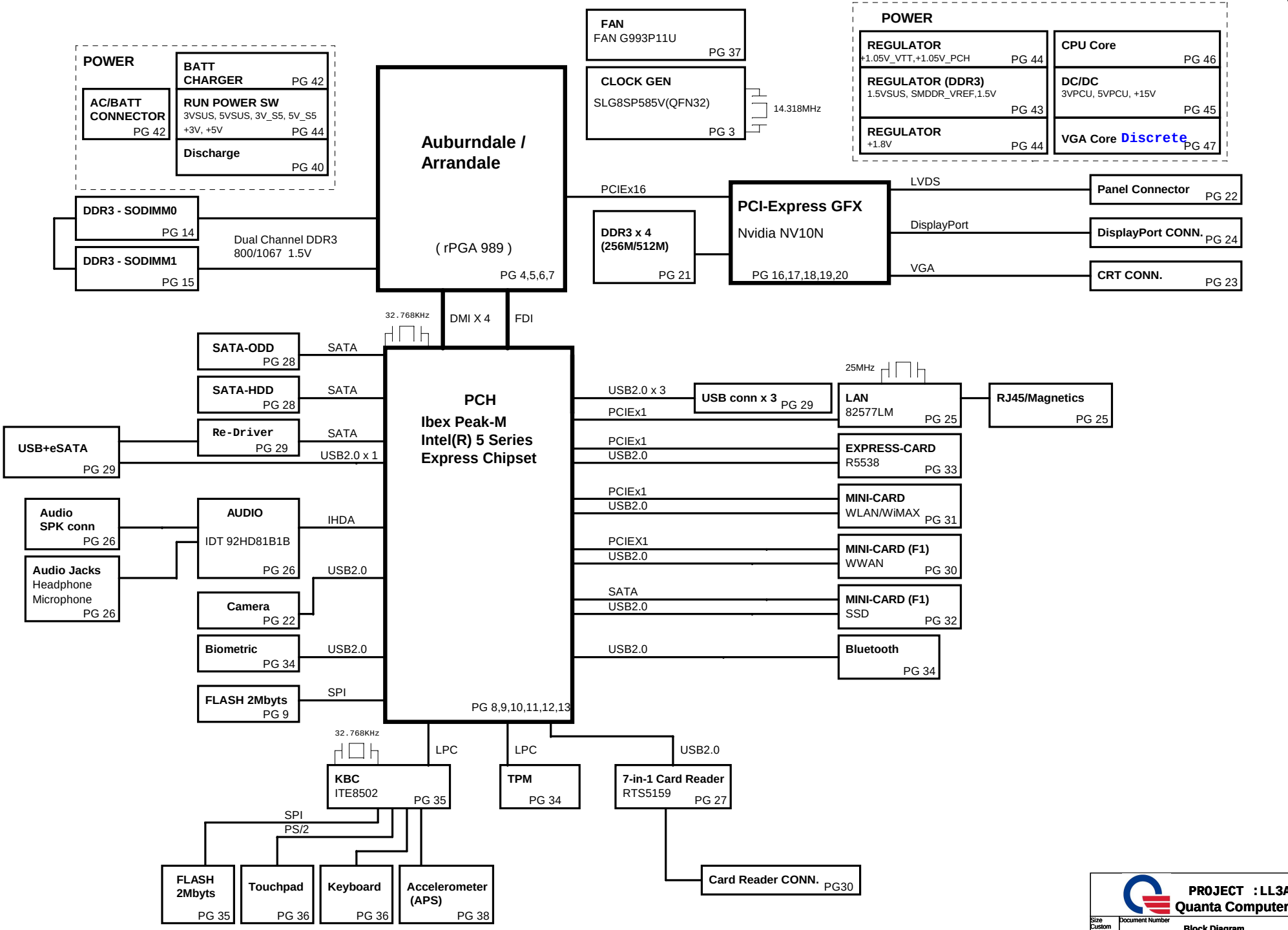
LL3A Intel Calpella Platform with Discrete GFX

01



PROJECT : LL3A
Quanta Computer Inc.

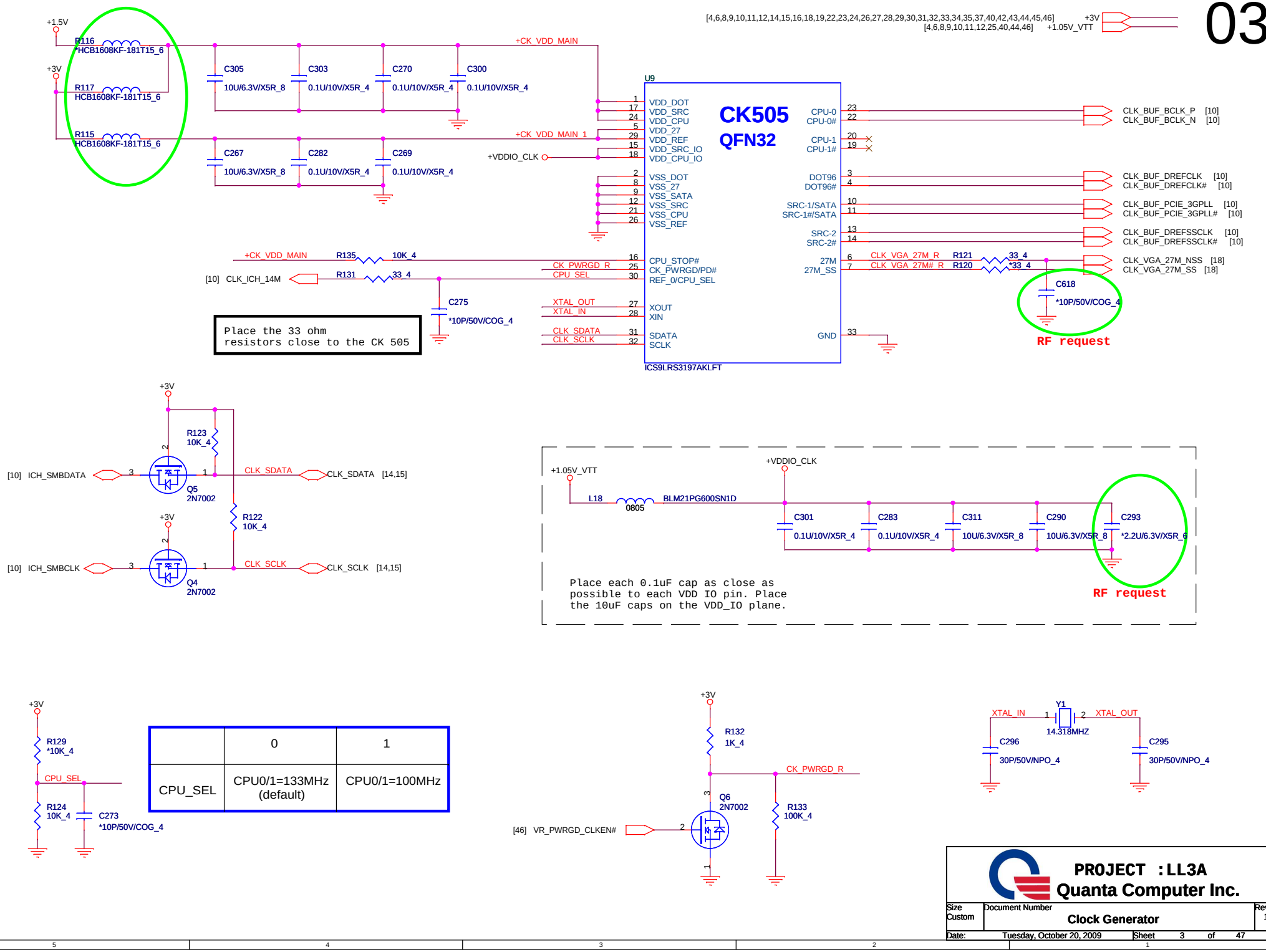
Size	Document Number	Rev
Custom	Block Diagram	1C

Date: Tuesday, October 20, 2009 Sheet 1 of 47

Table of Contents

Power States

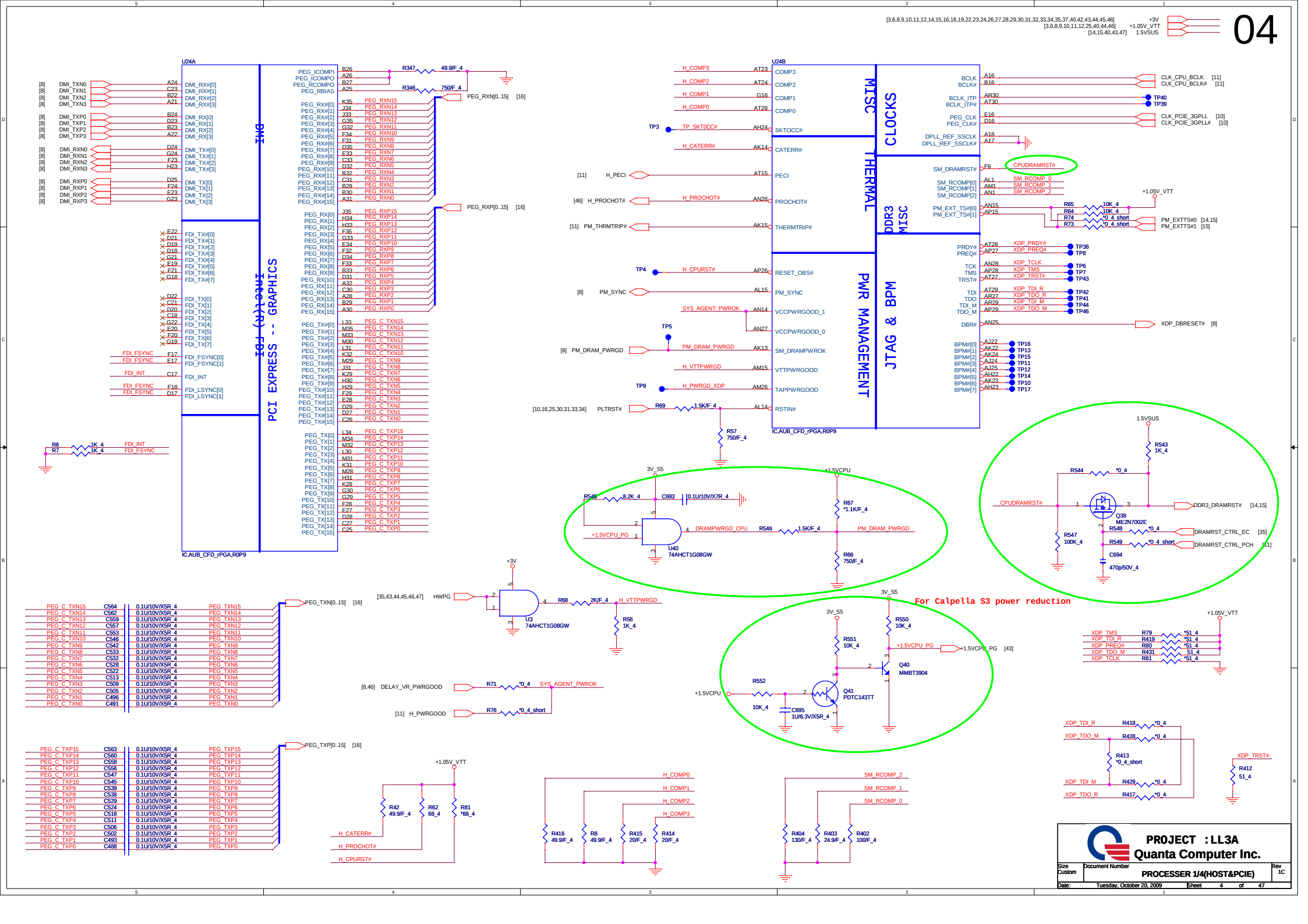
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	23,32,43,44,45,46,47,48,49,50	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	9,12,41	RTC		S0~S5
3VPCU	+3.3V	9,23,27,30,32,35,39,41,43,44,47	ITE8052 POWER	3V5V_EN	S0~S5
5VPCU	+5V	14,43,44,45,46,47,49,50	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	23,38,43,45,46,47	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	27,43	LAN POWER	LAN_ON	
5V_S5	+5V	12,29,30,43	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	8,9,10,11,12,43,52	Sys Management,PCH Resume Well,Intel HD Audio,USB,WLAN WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V	23,39,43,48	SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V	14,15,30,34,41,43,49	SLP_S4# CTRLD POWER	SUSON	S0~S3
1.5VSUS	+1.5V	4,6,14,15,43,45,46,49,50	SODIMM POWER	SUSON	S0~S3
0.75VSMDDR_VTERM	+0.75V	14,15,43,45	DDR3 SODIMM REFERENCE POWER	MAIN_ON	S0
+5V	+5V	12,18,23,24,25,26,28,35,37,41,43,44	SLP_S3# CTRLD POWER	MAIN_ON	S0
+3V	+3.3V	3,4,8,9,10,11,12,14,15,17,23,25,26,27,28,29,30,31,32,33,34,36,37,38,39,40,41,43,44,45,46,47,48,50,52	SLP_S3# CTRLD POWER	MAIN_ON	S0
+1.8V	+1.8V	6,12,17,18,21,22,33,43,50	LVDS,NVM POWER	MAIN_ON	S0
+1.5V	+1.5V	12,18,19,20,31,32,34,45,46	Mini PCIe,Express Card POWER	MAIN_ON	S0
+1.05V_VTT	+1.05V	4,6,11,12,43,46,48,52	AuBurndale VTT POWER	MAIN_ON	S0
+1.05V_PCH	+1.05V	3,10,12,43,46,52	PCH CORE POWER	1.05V_RUN_ON	S0
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,43,49	VGA CORE POWER	GFXVR_EN	S0
VCC_CORE		6,43,48	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	23	LCD Power	ENVDD	S0
+5V_ODD	+5V	28	ODD Power	MAIN_ON	S0
+5V_HDD	+5V	28	HDD Power	MAIN_ON	S0
BAT-V	+10V~+17V	44	MAIN BATTERY	CHG_PBATT	S0~S5



	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

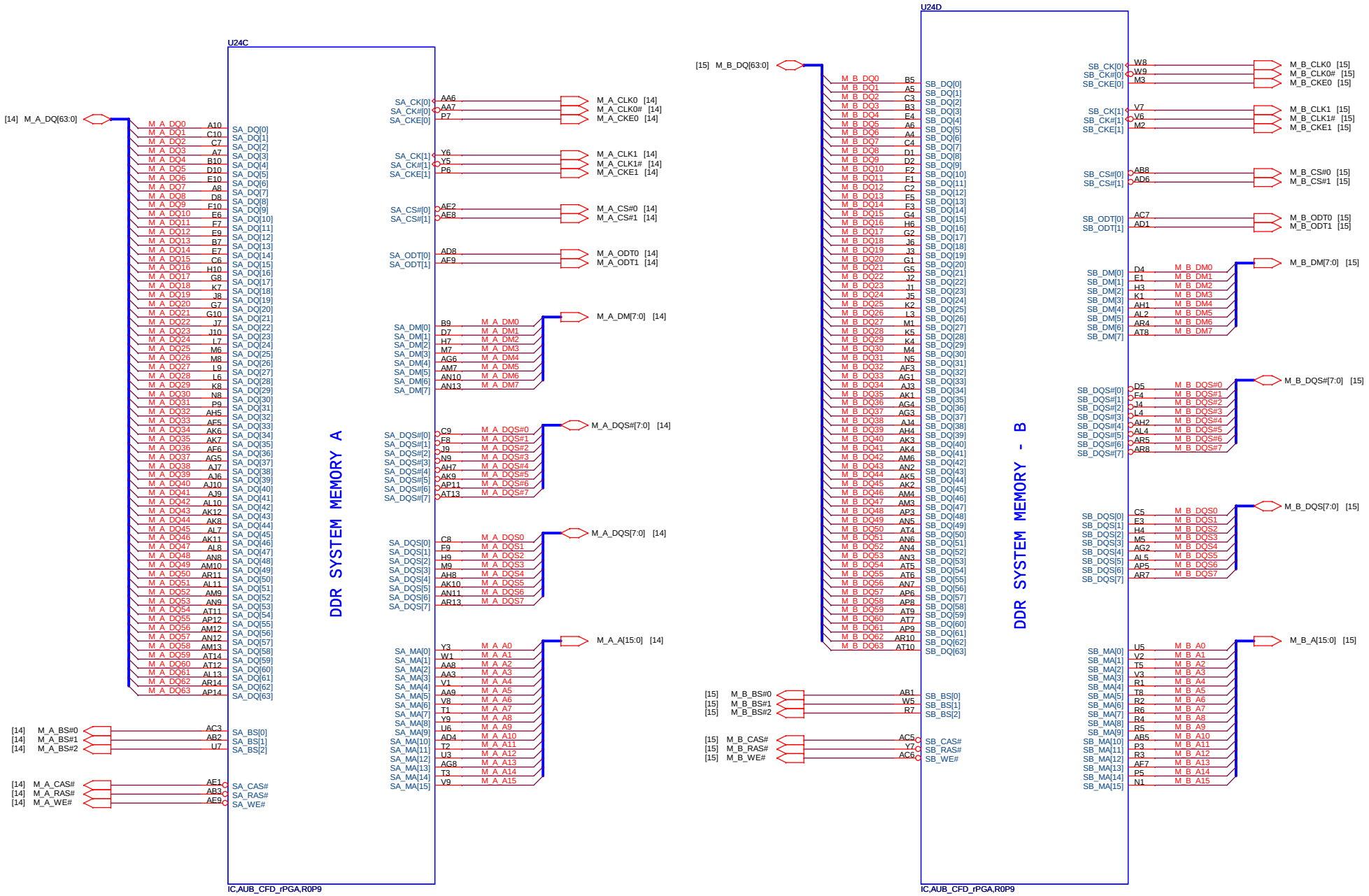
PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Generator	1C
Date: Tuesday, October 20, 2009	Sheet 3 of 47	


U24A
DMI
PCI EXPRESS -- GRAPHICS
FDI
Intel(R) FDI
IC,AUB_CFD_rPGA,R0P9
U24B
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
IC,AUB_CFD_rPGA,R0P9
For Calpella S3 power reduction
PROJECT : LL3A
Quanta Computer Inc.
PROCESSER 1/4(HOST&PCIE)
Tuesday, October 20, 2009

AUBURNDALE PROCESSOR (DDR3)

05



PROJECT : LL3A		
Quanta Computer Inc.		
Size: Custom	Document Number: PROCESSER 2/4(DDR)	Rev: 1C
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AUBURNDALE PROCESSOR (GRAPHICS POWER)

06

[40,46] VCC_CORE
[3,4,8,9,10,11,12,25,40,44,46] +1.05V_VTT
[4,14,15,40,43,47] 1.5VSUS
[10,12,18,39,40,44] +1.8V

U24F

1.1V RAIL POWER

CPU CORE SUPPLY

CPU VIDS

SENSE LINES

POWER

IC,AUB_CFD_rPGA,R0P9

U24G

GRAPHICS

SENSE LINES

GRAPHICS VIDS

DDR3 - 1.5V RAILS

1.1V

1.8V

FDI

PEG & DMI

POWER

IC,AUB_CFD_rPGA,R0P9

Lenovo Request

CPU thermal protection

U26
*MAX6509

PROJECT : LL3A
Quanta Computer Inc.

PROCESSOR 3/4(POWER)

Size: Custom | Document Number | Rev: 1C

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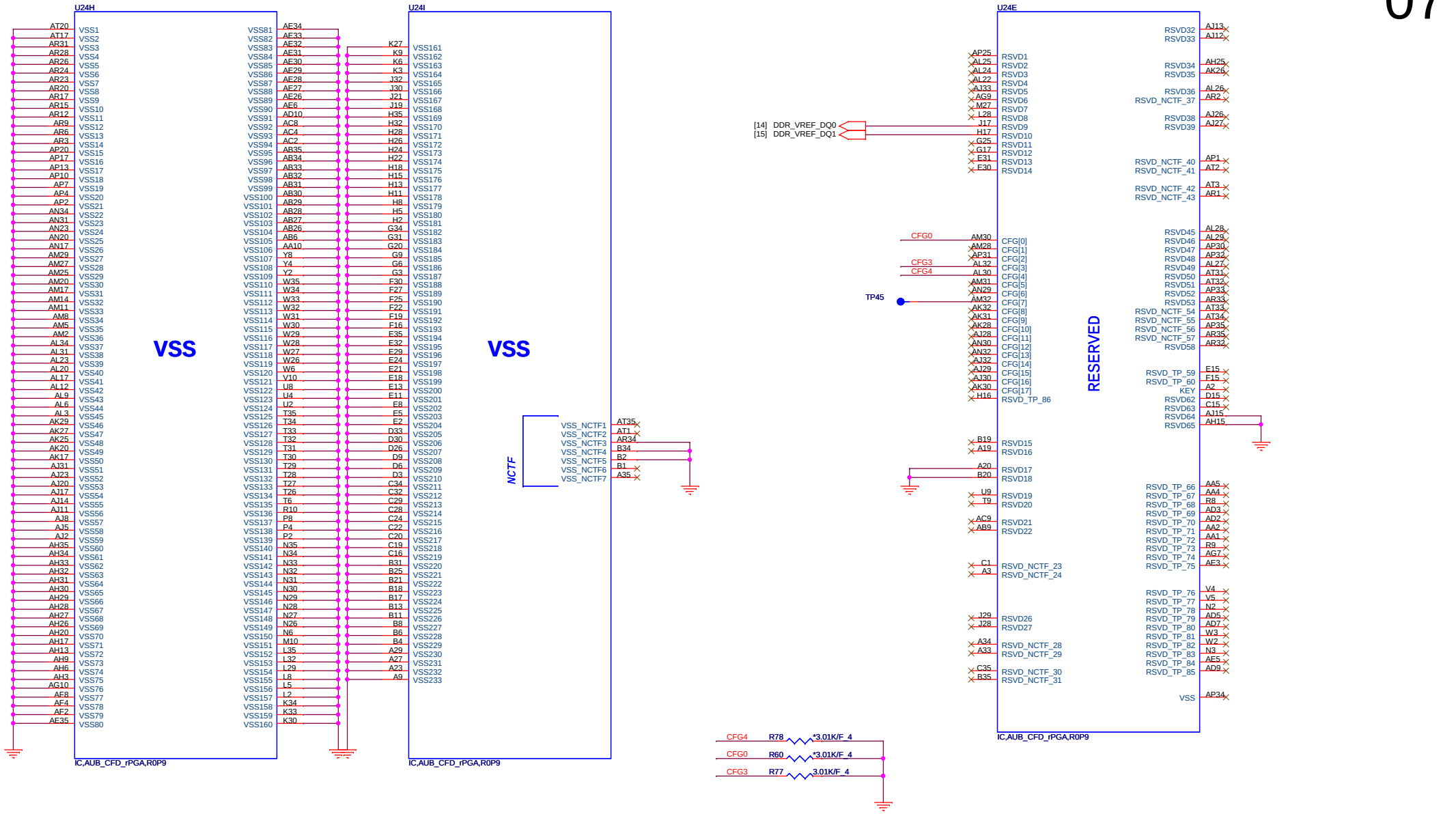
AUBURNDALE PROCESSOR (GND)

AUBURNDALE PROCESSOR(RESERVED, CFG)

07

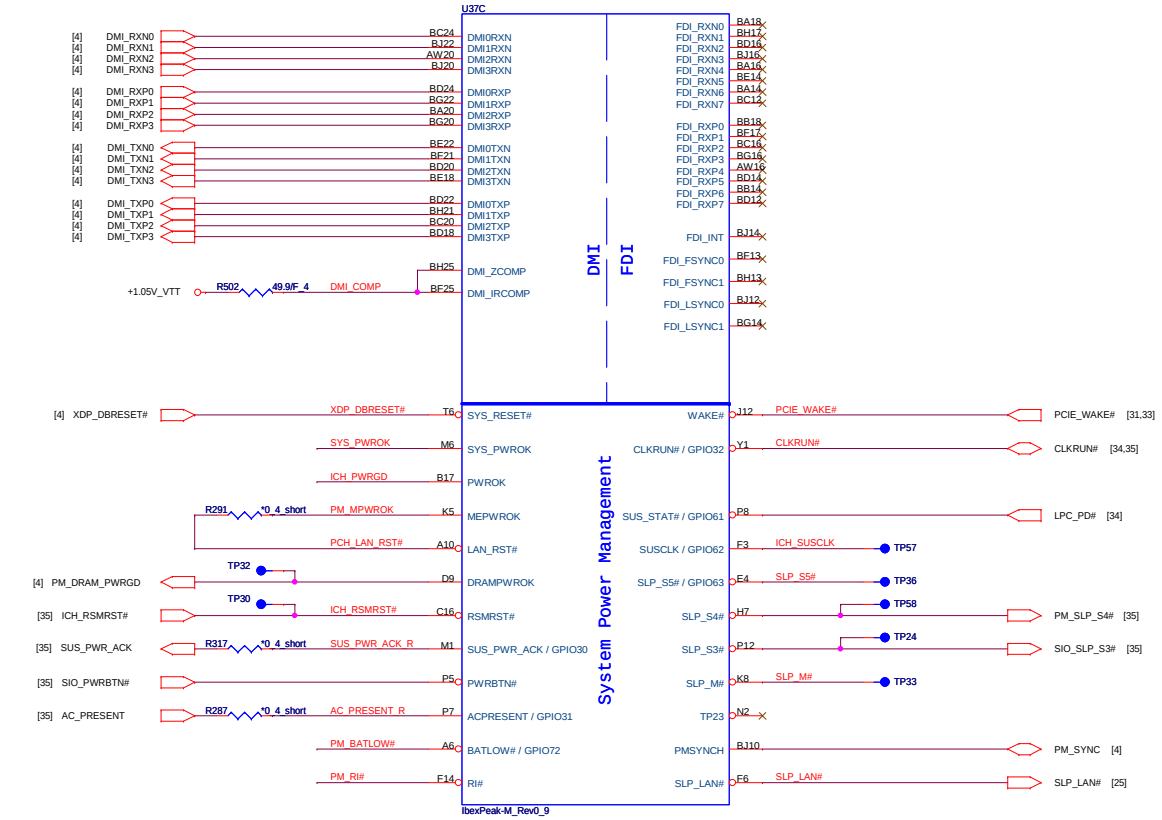


	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

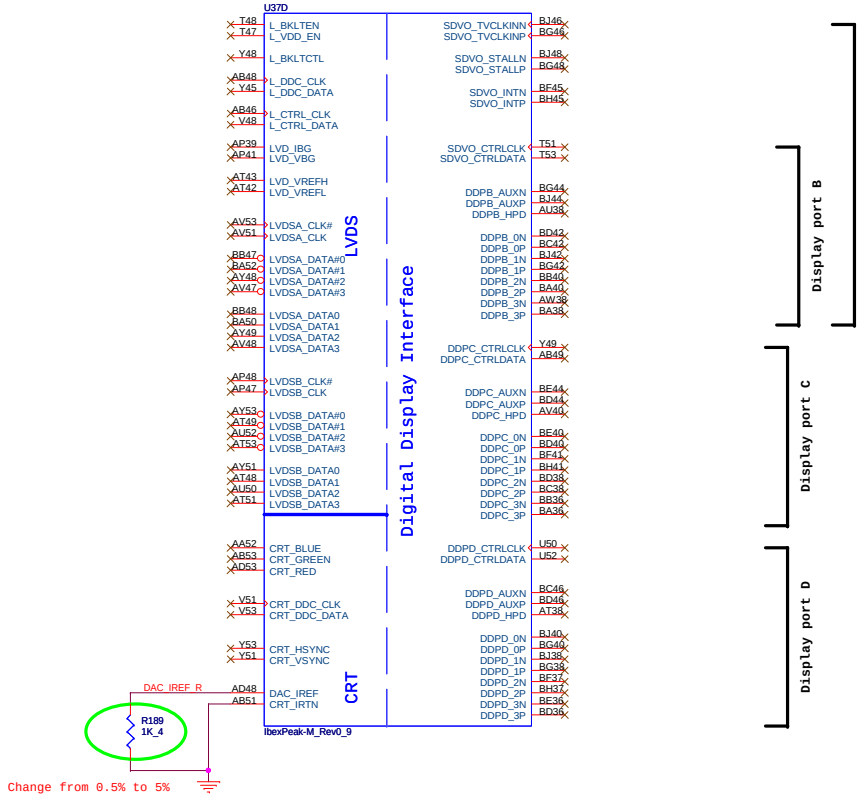
PROJECT : LL3A
Quanta Computer Inc.

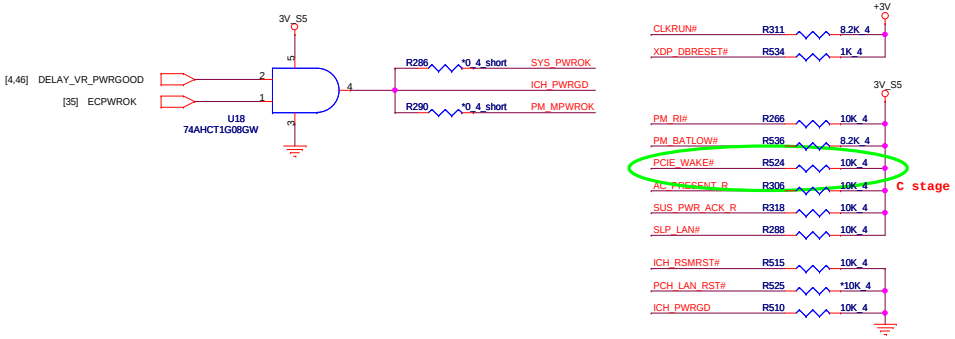
Size	Document Number	Rev
Custom	PROCESSER 4/4(GND)	1C
Date: Tuesday, October 20, 2009	Sheet 7 of 47	

IBEX PEAK-M (DMI,FDI,GPIO)



IBEX PEAK-M (LVDS,DDI)





PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/6 (DMI&VIDEO)	1C
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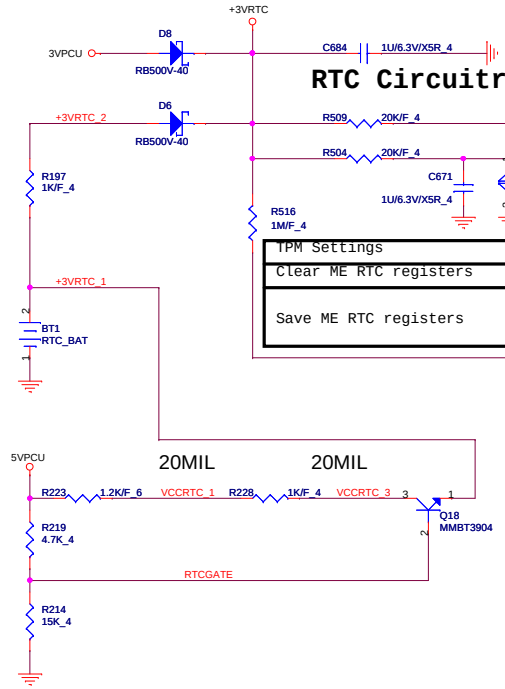
[12,35] +3VRTC
[22,25,28,35,36,37,39,40,42,44,45,47] 3VPCU
[3,4,6,8,10,11,12,14,15,16,18,19,22,23,24,26,27,28,29,30,31,32,33,34,35,37,40,42,43,44,45,46] +3V
[4,8,10,11,12,25,31,40] 3V_S5
[3,4,6,8,10,11,12,25,40,44,46] +1.05V_VTT

RTC Circuitry

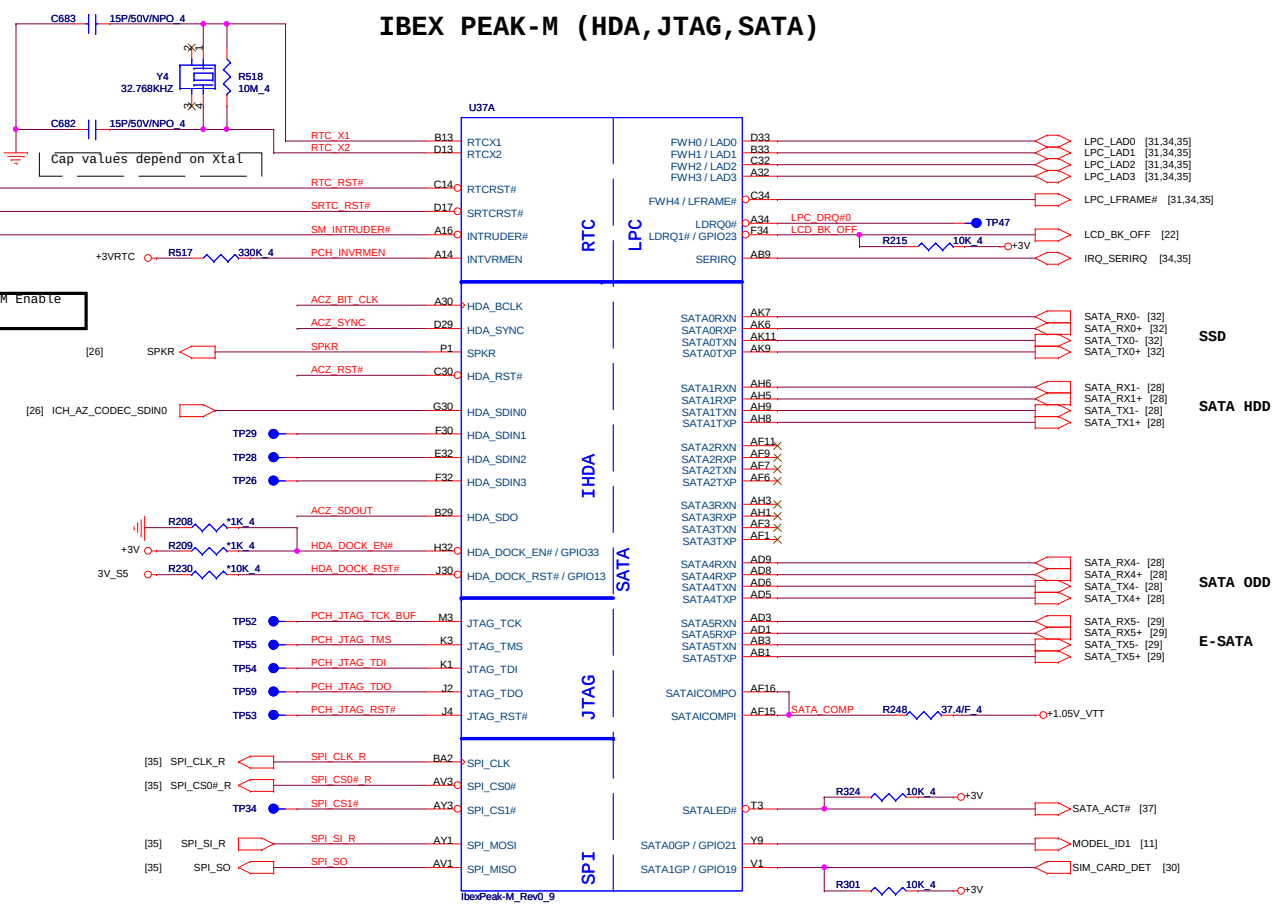
CMOS Settings	J5
Clear CMOS	1-2
Save CMOS	1-X (Default)

TPM Settings	J4
Clear ME RTC registers	1-2
Save ME RTC registers	1-X (Default)

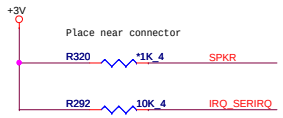


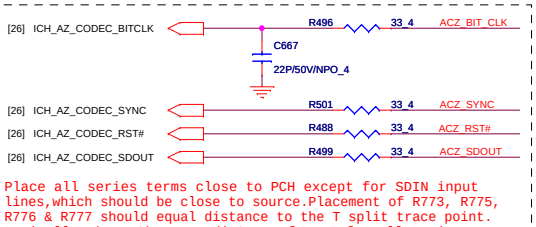
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)



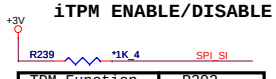
No Reboot Strap





Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

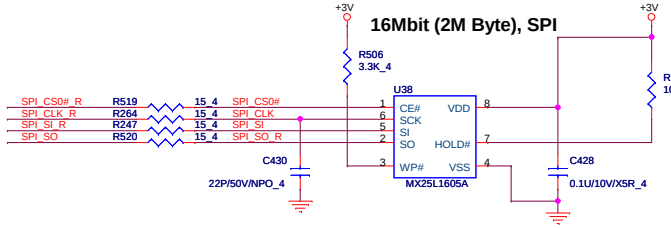
iTPM ENABLE/DISABLE



TPM Function	R292
Enable	Stuff
Disable	NC (Default)

For ME F/W

16Mbit (2M Byte), SPI



PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA&HDA&JTA)	1C
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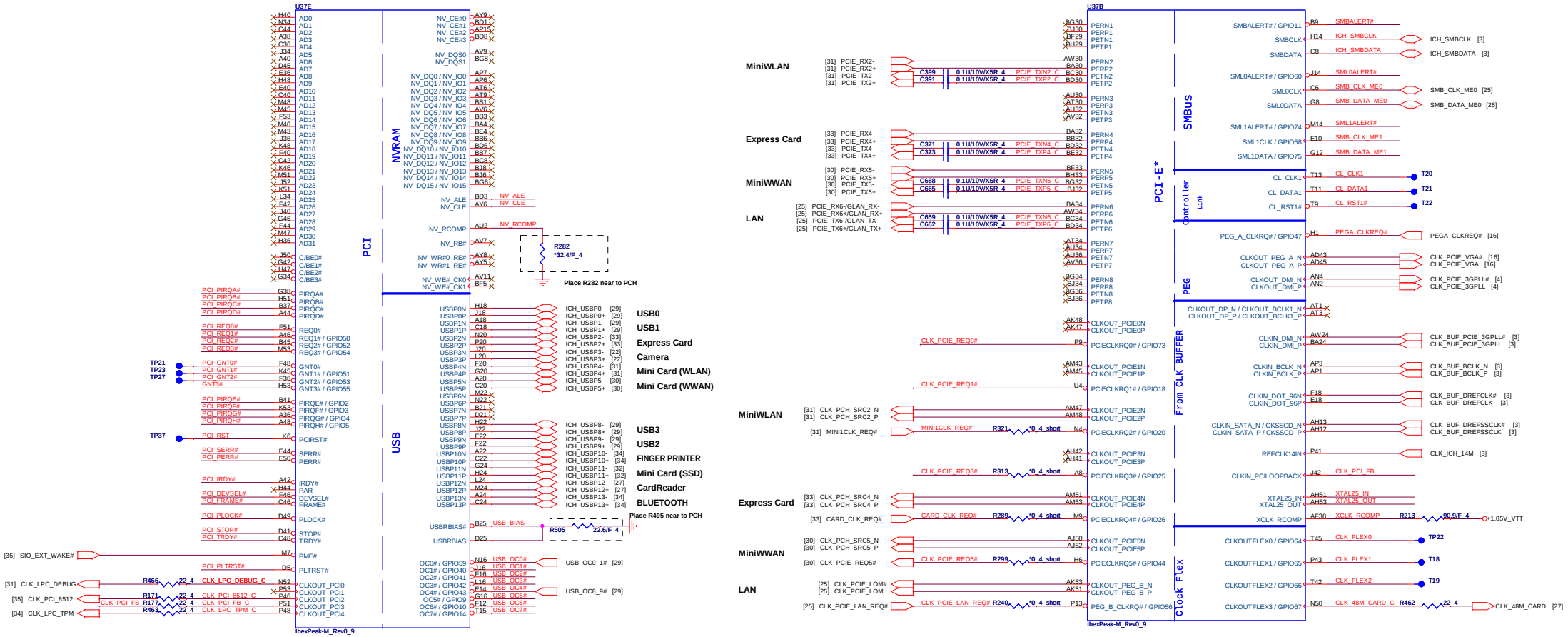
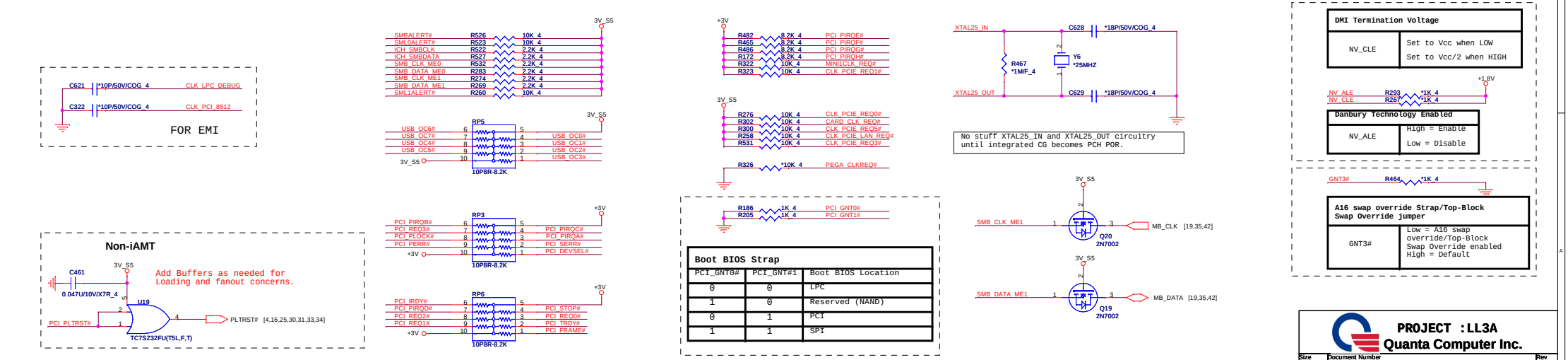
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

[3,4,6,8,9,11,12,14,15,16,18,19,22,23,24,26,27,28,29,30,31,32,33,34,35,37,40,42,43,44,45,46] +3V
[4,8,9,11,12,25,31,40] 3V_S5
[3,4,6,8,9,11,12,25,40,44,46] +1.05V_VTT
[6,12,18,39,40,44] +1.8V





Boot BIOS Strap

PCI_GNT0#	PCI_GNT#1	Boot BIOS Location
0	0	LPC
1	0	Reserved (NAND)
0	1	PCI
1	1	SPI

DMI Termination Voltage

NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

Danbury Technology Enabled

NV_ALE	High = Enable Low = Disable

A16 swap override Strap/Top-Block Swap Override jumper

GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 3/6 (PCI)	1C

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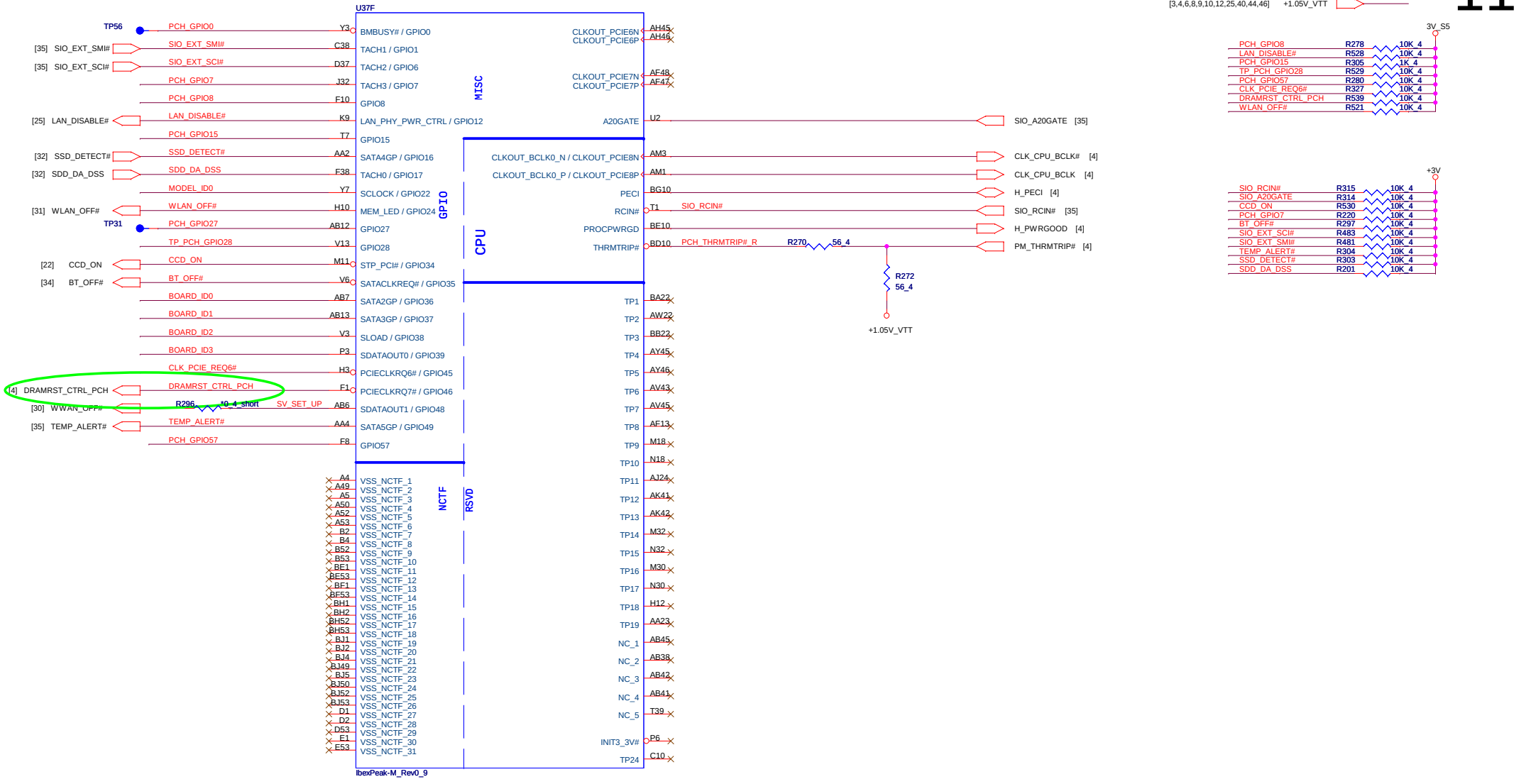
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

[3,4,6,8,9,10,12,14,15,16,18,19,22,23,24,26,27,28,29,30,31,32,33,34,35,37,40,42,43,44,45,46] +3V
[4,8,9,10,12,25,31,40] 3V_S5
[3,4,6,8,9,10,12,25,40,44,46] +1.05V_VTT



3V_S5

PCH_GPIO8	R278	10K_4
LAN_DISABLE#	R528	10K_4
PCH_GPIO15	R305	1K_4
TP_PCH_GPIO28	R529	10K_4
PCH_GPIO57	R280	10K_4
CLK_PCIE_REQ6#	R327	10K_4
DRAMRST_CTRL_PCH	R539	10K_4
WLAN_OFF#	R521	10K_4

+3V

SIO_RCIN#	R315	10K_4
SIO_A20GATE	R314	10K_4
CCD_ON	R530	10K_4
PCH_GPIO7	R220	10K_4
BT_OFF#	R297	10K_4
SIO_EXT_SCI#	R483	10K_4
SIO_EXT_SMI#	R481	10K_4
TEMP_ALERT#	R304	10K_4
SSD_DETECT#	R303	10K_4
SDD_DA_DSS	R201	10K_4

Board ID

Board ID For Function	ID3 GPIO39	ID2 GPIO38	ID1 GPIO37	ID0 GPIO36
SDV	0	0	0	0
SIV	0	0	0	1
SIT	0	0	1	0
SVT	0	0	1	1
SOVP	0	1	0	0

+3V
R535 *10K_4 BOARD_ID0 R533 10K_4
R309 *10K_4 BOARD_ID1 R308 10K_4
R319 *10K_4 BOARD_ID2 R312 10K_4
R325 *10K_4 BOARD_ID3 R316 10K_4

Model ID

Model ID	MODEL_ID0	MODEL_ID1
Default	0	0
LL3/LL3A	0	1
LL5/LL5A	1	0
	1	1

+3V
R273 *10K_4
MODEL_ID0 R294 10K_4
+3V
R538 10K_4
[9] MODEL_ID1 R541 *10K_4

+3V
SV_SET_UP R295 10K_4

SV_SET_UP	1-X High = Strong (Default)

PROJECT : LL3A
Quanta Computer Inc.

Size: Custom	Document Number: PCH 4/6 (GPIO)	Rev: 1C
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[3,4,6,8,9,10,11,14,15,16,18,19,22,23,24,26,27,28,29,30,31,32,33,34,35,37,40,42,43,44,45,46] +3V
[4,8,9,10,11,25,31,40] 3V_S5
[29,40] 5V_S5
[22,23,24,26,28,34,35,36,37,38,40,42] +5V
[3,4,6,8,9,10,11,25,40,44,46] +1.05V_VTT
[6,10,18,39,40,44] +1.8V
[9,35] +3VRTC

VccCORE : 1432mA max
VccDAC : 69mA max
VccIO : 3062mA max
VccVRM : 196mA max
VccDMI : 58mA max
VccPNAND : 156mA max
VccME3_3 : 85mA max
Vcc3_3 : 357mA max
VccADPLLA : 68mA max
VccADPLLB : 69mA max
VccLAN : 320mA max
VccME : 1849mA max
V_CPU_IO : <1mA max
VccRTC : 2mA max
VccSUS3_3 : 163mA max
V5REF_SUS : <1mA max
V5REF : <1mA max
VccSUSHDA : 6mA max

POWER

U37G

VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI

U37J

USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
RTC
HDA

IbexPeak-M_Rev0_9

PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/6 (POWER)	1C

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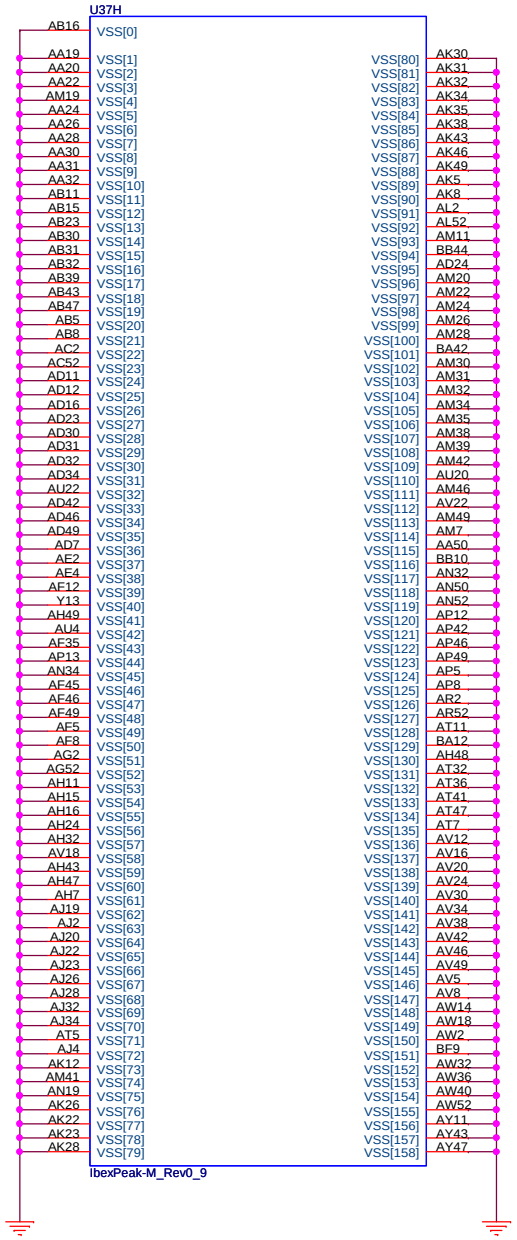
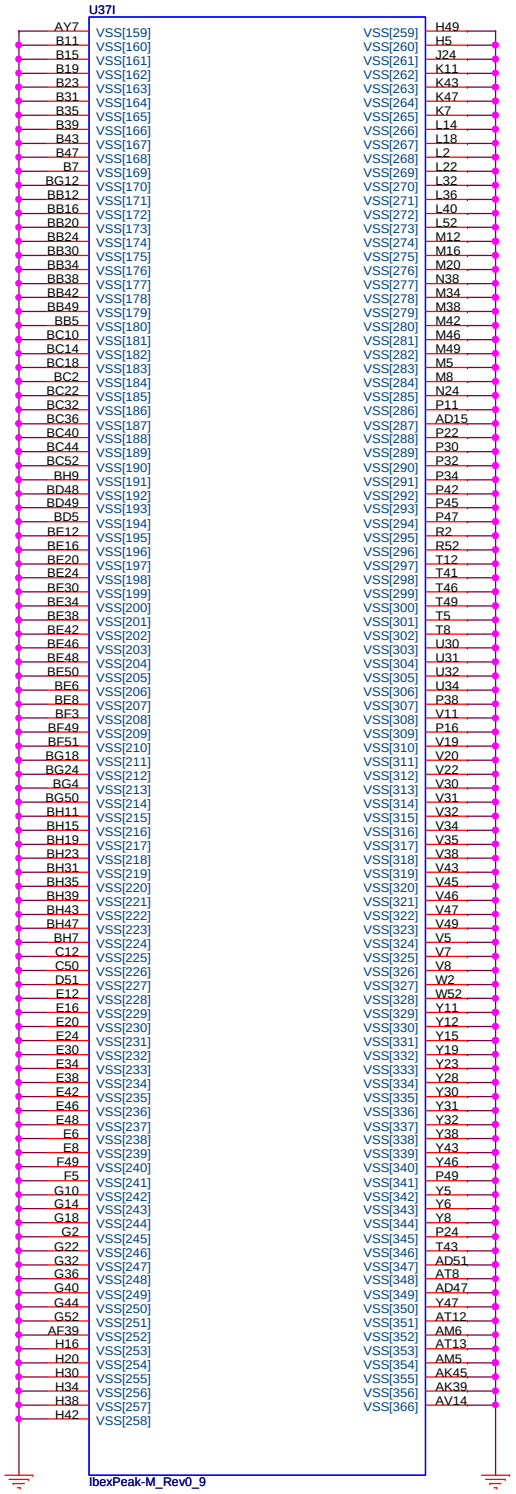
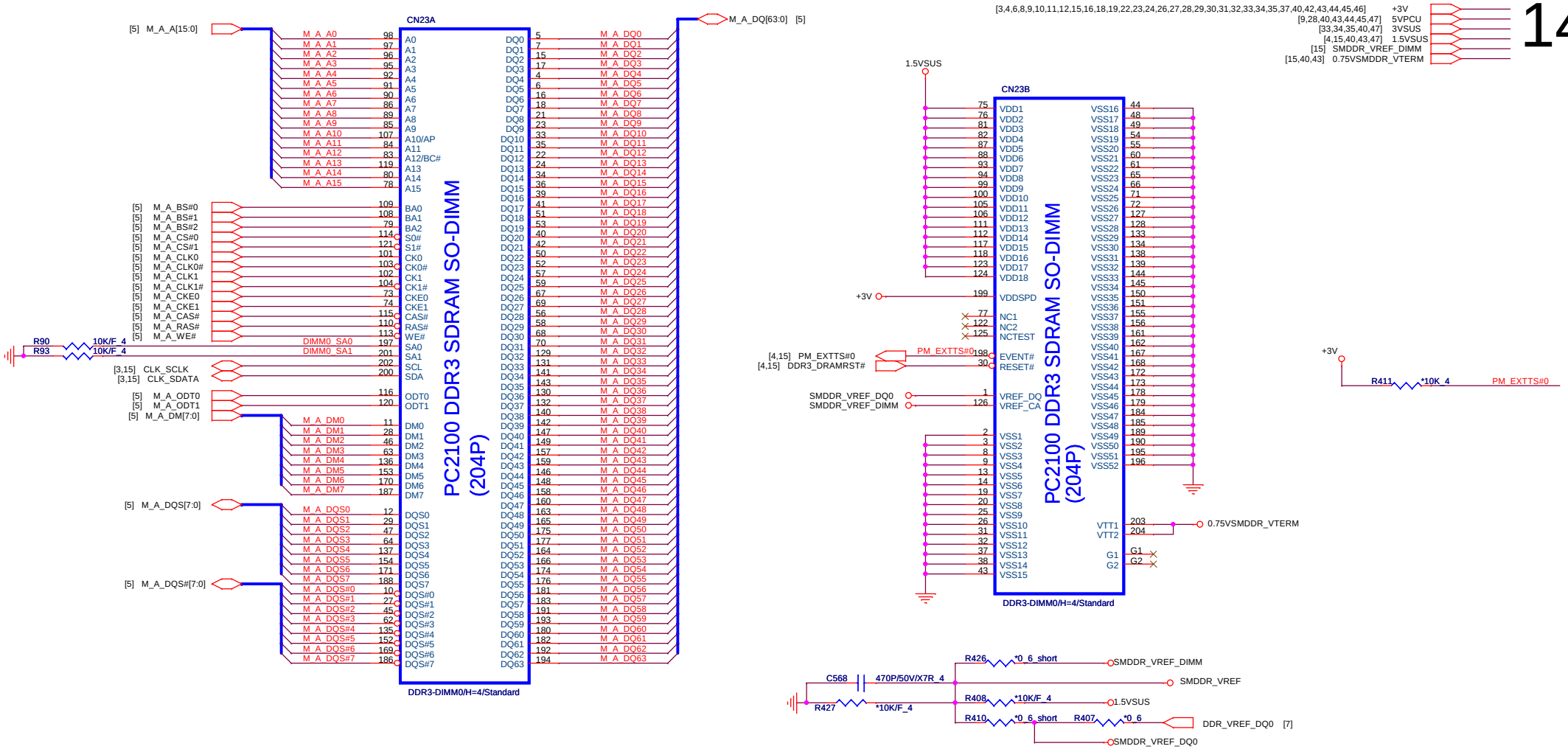
IBEX PEAK-M (GND)



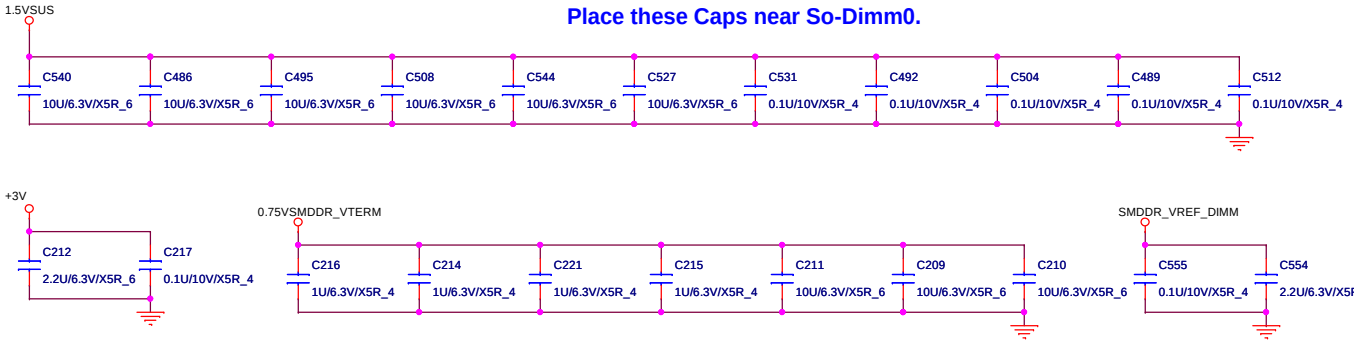


PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1C
Date: Tuesday, October 20, 2009	Sheet 13 of 47	



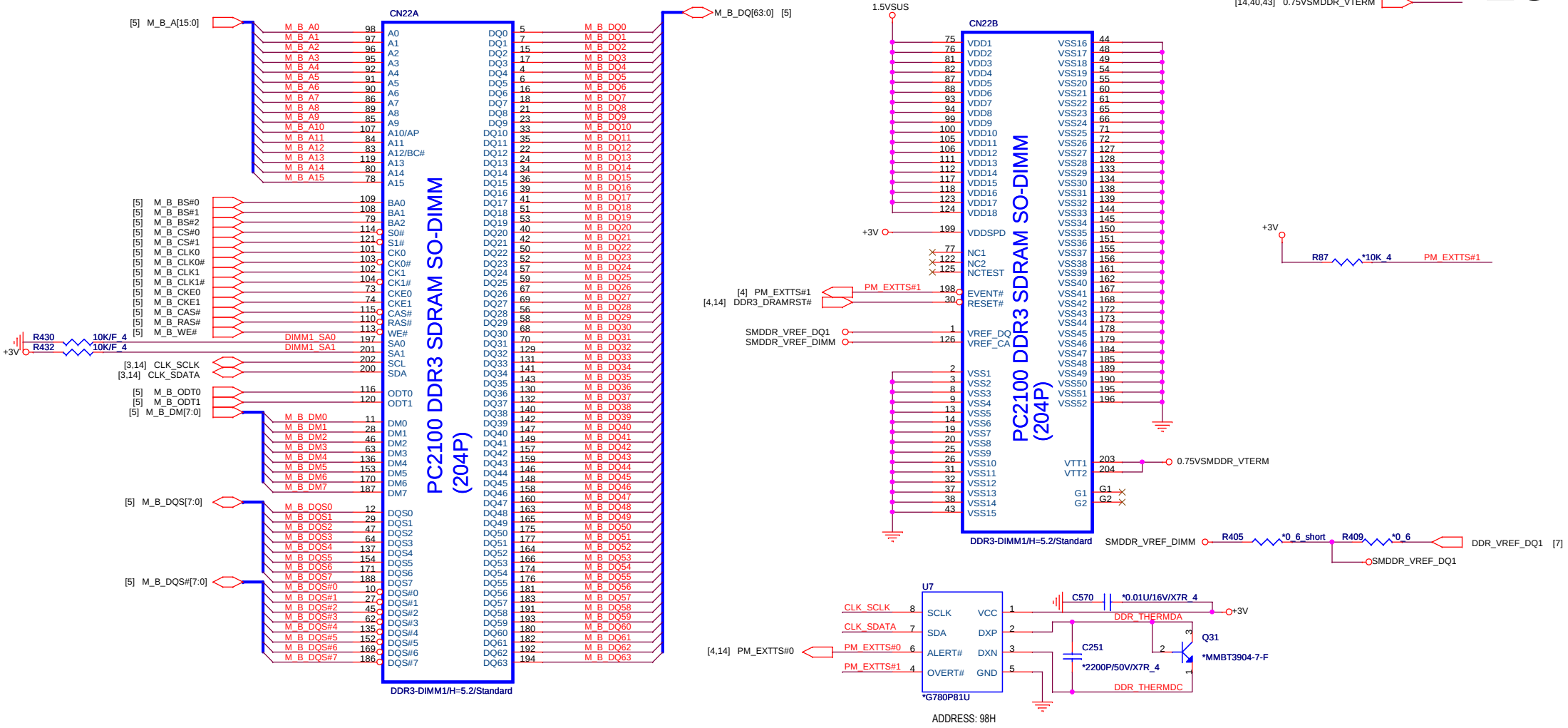
Place these Caps near So-Dimm0.



PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-0(H=5.2)	1C
Date: Tuesday, October 20, 2009	Sheet 14 of 47	

[3,4,6,8,9,10,11,12,14,16,18,19,22,23,24,26,27,28,29,30,31,32,33,34,35,37,40,42,43,44,45,46] +3V
[33,34,35,40,47] 3VSUS
[4,14,40,43,47] 1.5VSUS
[14] SMDDR_VREF_DIMM
[14,40,43] 0.75VSMDDR_VTERM



Place these Caps near So-Dimm1.

1.5VSUS

C530	C482	C485	C552	C521	C541	C494	C490	C503	C510	C520
10U/6.3V/X5R_6	10U/6.3V/X5R_6	10U/6.3V/X5R_6	10U/6.3V/X5R_6	10U/6.3V/X5R_6	10U/6.3V/X5R_6	0.1U/10V/X5R_4	0.1U/10V/X5R_4	0.1U/10V/X5R_4	0.1U/10V/X5R_4	0.1U/10V/X5R_4

+3V		0.75VSMDDR_VTERM						SMDDR_VREF_DIMM		SMDDR_VREF_DQ1	
C218	C571	C577	C226	C578	C227	C579	C229	C230	C565	C566	C11	C12
2.2U/6.3V/X5R_6	0.1U/10V/X5R_4	1U/6.3V/X5R_4	1U/6.3V/X5R_4	1U/6.3V/X5R_4	1U/6.3V/X5R_4	10U/6.3V/X5R_6	10U/6.3V/X5R_6	10U/6.3V/X5R_6	0.1U/10V/X5R_4	2.2U/6.3V/X5R_6	0.1U/10V/X5R_4	2.2U/6.3V/X5R_6

PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1(H=9.2)	1C
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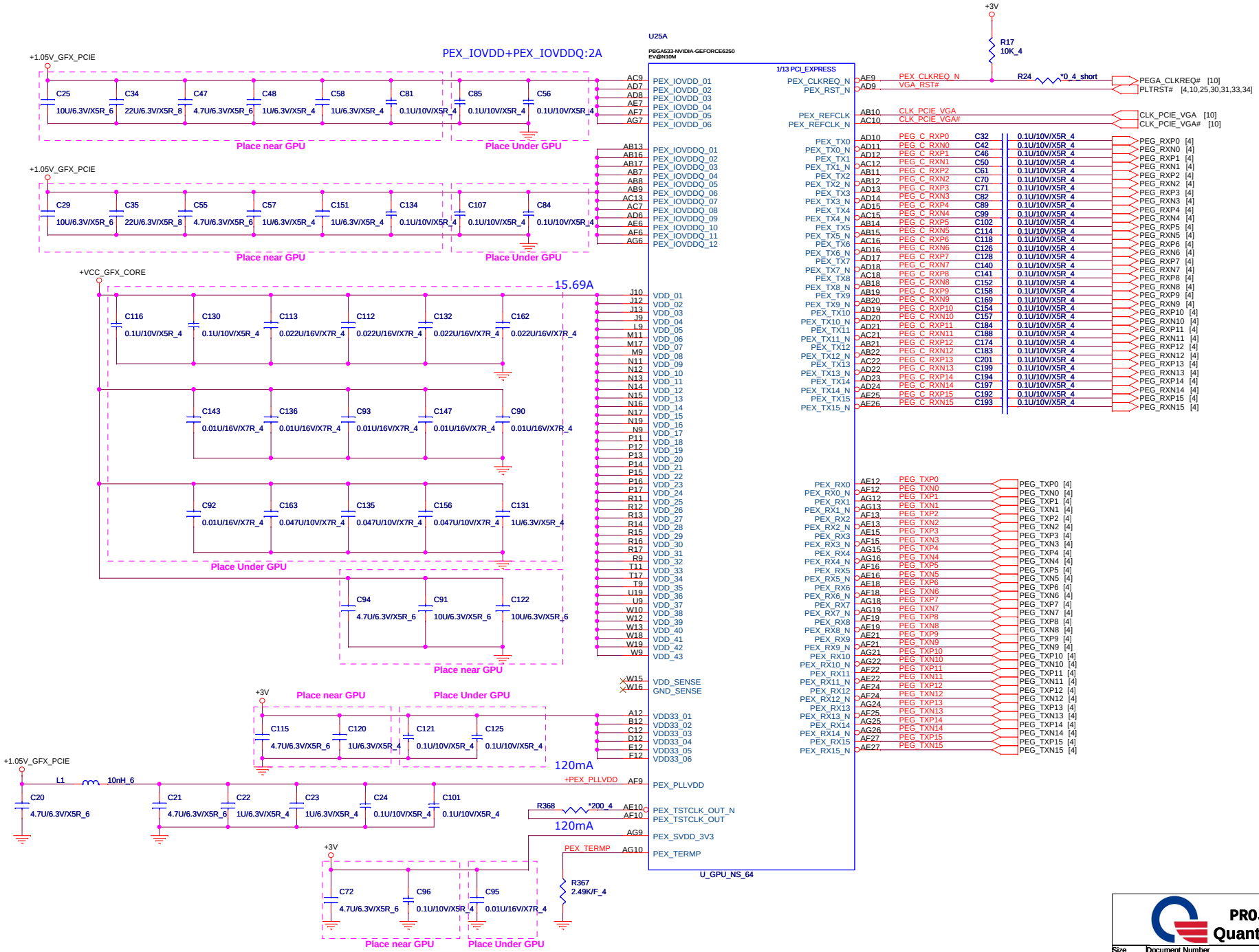
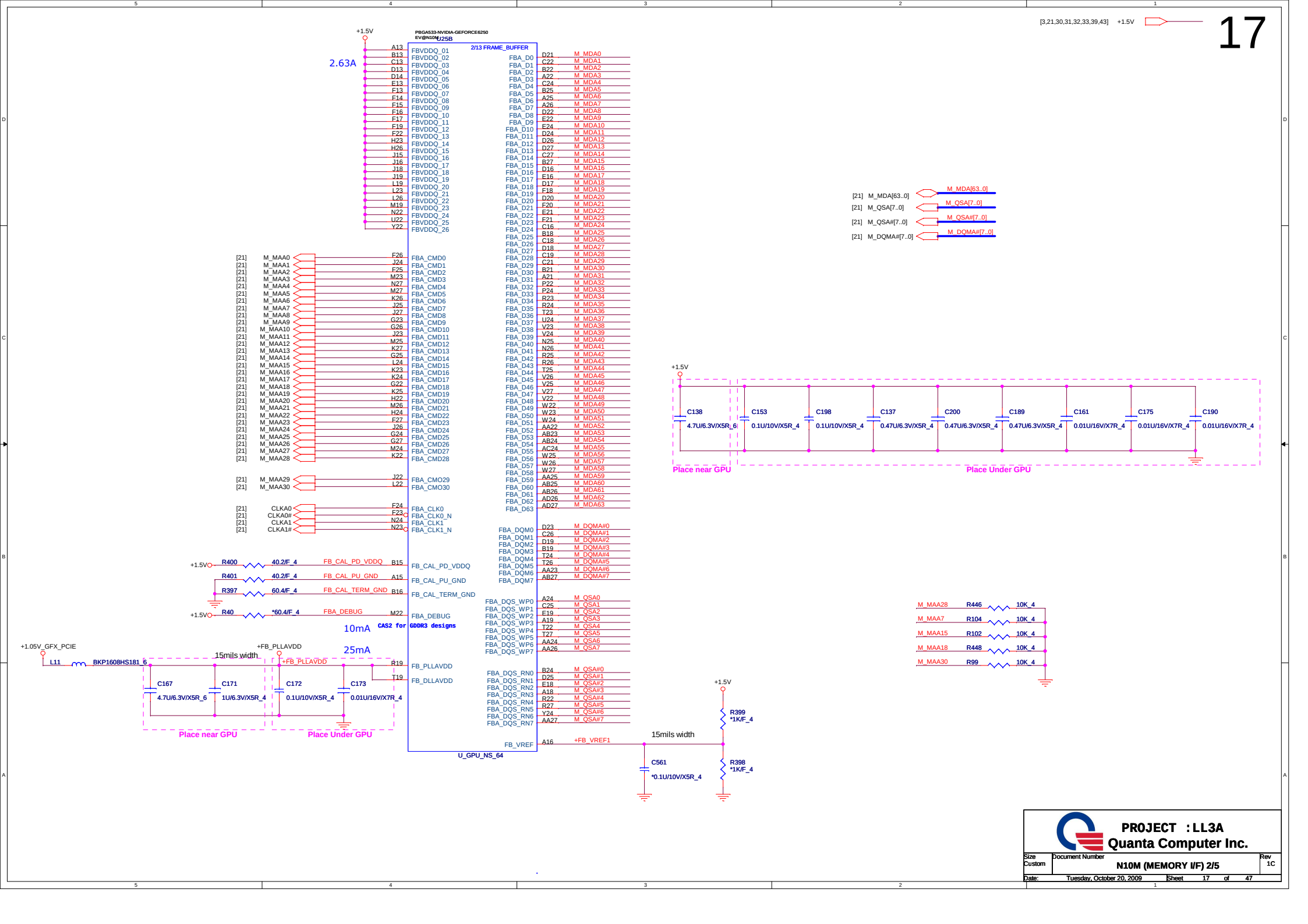
[3,4,6,8,9,10,11,12,14,15,18,19,22,23,24,26,27,28,29,30,31,32,33,34,35,37,40,42,43,44,45,46] +3V
[17,18,40,47] +1.05V_GFX_PCIE
[39,40,47] +VCC_GFX_CORE




[3,21,30,31,32,33,39,43] +1.5V
+1.5V
2.63A
PBGA533-NVIDIA-GEFORCE6250
EV@N10M
U25B
2/13 FRAME_BUFFER
FBVDDQ_01 A13
FBVDDQ_02 B13
FBVDDQ_03 C13
FBVDDQ_04 D13
FBVDDQ_05 D14
FBVDDQ_06 E13
FBVDDQ_07 F13
FBVDDQ_08 F14
FBVDDQ_09 F15
FBVDDQ_10 F16
FBVDDQ_11 F17
FBVDDQ_12 F19
FBVDDQ_13 F22
FBVDDQ_14 H23
FBVDDQ_15 H26
FBVDDQ_16 J15
FBVDDQ_17 J16
FBVDDQ_18 J18
FBVDDQ_19 J19
FBVDDQ_20 L19
FBVDDQ_21 L23
FBVDDQ_22 L26
FBVDDQ_23 M19
FBVDDQ_24 N22
FBVDDQ_25 U22
FBVDDQ_26 Y22
FBA_D0 D21 M_MDA0
FBA_D1 C22 M_MDA1
FBA_D2 B22 M_MDA2
FBA_D3 A22 M_MDA3
FBA_D4 C24 M_MDA4
FBA_D5 B25 M_MDA5
FBA_D6 A25 M_MDA6
FBA_D7 A26 M_MDA7
FBA_D8 D22 M_MDA8
FBA_D9 E22 M_MDA9
FBA_D10 E24 M_MDA10
FBA_D11 D24 M_MDA11
FBA_D12 D26 M_MDA12
FBA_D13 D27 M_MDA13
FBA_D14 C27 M_MDA14
FBA_D15 B27 M_MDA15
FBA_D16 D16 M_MDA16
FBA_D17 E16 M_MDA17
FBA_D18 D17 M_MDA18
FBA_D19 F18 M_MDA19
FBA_D20 D20 M_MDA20
FBA_D21 F20 M_MDA21
FBA_D22 E21 M_MDA22
FBA_D23 F21 M_MDA23
FBA_D24 C16 M_MDA24
FBA_D25 B18 M_MDA25
FBA_D26 C18 M_MDA26
FBA_D27 D18 M_MDA27
FBA_D28 C19 M_MDA28
FBA_D29 C21 M_MDA29
FBA_D30 B21 M_MDA30
FBA_D31 A21 M_MDA31
FBA_D32 P22 M_MDA32
FBA_D33 P24 M_MDA33
FBA_D34 R23 M_MDA34
FBA_D35 R24 M_MDA35
FBA_D36 T23 M_MDA36
FBA_D37 U24 M_MDA37
FBA_D38 V23 M_MDA38
FBA_D39 V24 M_MDA39
FBA_D40 N25 M_MDA40
FBA_D41 N26 M_MDA41
FBA_D42 R25 M_MDA42
FBA_D43 R26 M_MDA43
FBA_D44 T25 M_MDA44
FBA_D45 V26 M_MDA45
FBA_D46 V25 M_MDA46
FBA_D47 V27 M_MDA47
FBA_D48 V22 M_MDA48
FBA_D49 W22 M_MDA49
FBA_D50 W23 M_MDA50
FBA_D51 W24 M_MDA51
FBA_D52 AA22 M_MDA52
FBA_D53 AB23 M_MDA53
FBA_D54 AB24 M_MDA54
FBA_D55 AC24 M_MDA55
FBA_D56 W25 M_MDA56
FBA_D57 W26 M_MDA57
FBA_D58 W27 M_MDA58
FBA_D59 AA25 M_MDA59
FBA_D60 AB25 M_MDA60
FBA_D61 AB26 M_MDA61
FBA_D62 AD26 M_MDA62
FBA_D63 AD27 M_MDA63
[21] M_MDA[63..0]
M_MDA[63..0]
[21] M_QSA[7..0]
M_QSA[7..0]
[21] M_QSA#[7..0]
M_QSA#[7..0]
[21] M_DQMA#[7..0]
M_DQMA#[7..0]
[21] M_MAA0 F26 FBA_CMD0
[21] M_MAA1 J24 FBA_CMD1
[21] M_MAA2 F25 FBA_CMD2
[21] M_MAA3 M23 FBA_CMD3
[21] M_MAA4 N27 FBA_CMD4
[21] M_MAA5 M27 FBA_CMD5
[21] M_MAA6 K26 FBA_CMD6
[21] M_MAA7 J25 FBA_CMD7
[21] M_MAA8 J27 FBA_CMD8
[21] M_MAA9 G23 FBA_CMD9
[21] M_MAA10 G26 FBA_CMD10
[21] M_MAA11 J23 FBA_CMD11
[21] M_MAA12 M25 FBA_CMD12
[21] M_MAA13 K27 FBA_CMD13
[21] M_MAA14 G25 FBA_CMD14
[21] M_MAA15 L24 FBA_CMD15
[21] M_MAA16 K23 FBA_CMD16
[21] M_MAA17 K24 FBA_CMD17
[21] M_MAA18 G22 FBA_CMD18
[21] M_MAA19 K25 FBA_CMD19
[21] M_MAA20 H22 FBA_CMD20
[21] M_MAA21 M26 FBA_CMD21
[21] M_MAA22 H24 FBA_CMD22
[21] M_MAA23 F27 FBA_CMD23
[21] M_MAA24 J26 FBA_CMD24
[21] M_MAA25 G24 FBA_CMD25
[21] M_MAA26 G27 FBA_CMD26
[21] M_MAA27 M24 FBA_CMD27
[21] M_MAA28 K22 FBA_CMD28
[21] M_MAA29 J22 FBA_CMO29
[21] M_MAA30 L22 FBA_CMO30
[21] CLKA0 F24 FBA_CLK0
[21] CLKA0# F23 FBA_CLK0_N
[21] CLKA1 N24 FBA_CLK1
[21] CLKA1# N23 FBA_CLK1_N
+1.5V
R400 40.2/F_4 FB_CAL_PD_VDDQ B15 FB_CAL_PD_VDDQ
R401 40.2/F_4 FB_CAL_PU_GND A15 FB_CAL_PU_GND
R397 60.4/F_4 FB_CAL_TERM_GND B16 FB_CAL_TERM_GND
+1.5V
R40 *60.4/F_4 FBA_DEBUG M22 FBA_DEBUG
10mA
CAS2 for GDDR3 designs
FBA_DQM0 D23 M_DQMA#0
FBA_DQM1 C26 M_DQMA#1
FBA_DQM2 D19 M_DQMA#2
FBA_DQM3 B19 M_DQMA#3
FBA_DQM4 T24 M_DQMA#4
FBA_DQM5 T26 M_DQMA#5
FBA_DQM6 AA23 M_DQMA#6
FBA_DQM7 AB27 M_DQMA#7
FBA_DQS_WP0 A24 M_QSA0
FBA_DQS_WP1 C25 M_QSA1
FBA_DQS_WP2 E19 M_QSA2
FBA_DQS_WP3 A19 M_QSA3
FBA_DQS_WP4 T22 M_QSA4
FBA_DQS_WP5 T27 M_QSA5
FBA_DQS_WP6 AA24 M_QSA6
FBA_DQS_WP7 AA26 M_QSA7
FBA_DQS_RN0 B24 M_QSA#0
FBA_DQS_RN1 D25 M_QSA#1
FBA_DQS_RN2 E18 M_QSA#2
FBA_DQS_RN3 A18 M_QSA#3
FBA_DQS_RN4 R22 M_QSA#4
FBA_DQS_RN5 R27 M_QSA#5
FBA_DQS_RN6 Y24 M_QSA#6
FBA_DQS_RN7 AA27 M_QSA#7
FB_VREF A16 +FB_VREF1
15mils width
C561 *0.1U/10V/X5R_4
+1.5V
R399 *1K/F_4
R398 *1K/F_4
U_GPU_NS_64
+1.05V_GFX_PCIE
L11 BKP1608HS181_6
15mils width
+FB_PLLAVDD
25mA
+FB_PLLAVDD R19 FB_PLLAVDD
T19 FB_DLLAVDD
C167 4.7U/6.3V/X5R_6
C171 1U/6.3V/X5R_4
C172 0.1U/10V/X5R_4
C173 0.01U/16V/X7R_4
Place near GPU
Place Under GPU
+1.5V
C138 4.7U/6.3V/X5R_6
C153 0.1U/10V/X5R_4
C198 0.1U/10V/X5R_4
C137 0.47U/6.3V/X5R_4
C200 0.47U/6.3V/X5R_4
C189 0.47U/6.3V/X5R_4
C161 0.01U/16V/X7R_4
C175 0.01U/16V/X7R_4
C190 0.01U/16V/X7R_4
Place near GPU
Place Under GPU
M_MAA28 R446 10K_4
M_MAA7 R104 10K_4
M_MAA15 R102 10K_4
M_MAA18 R448 10K_4
M_MAA30 R99 10K_4
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Quanta Computer Inc.
Size Custom
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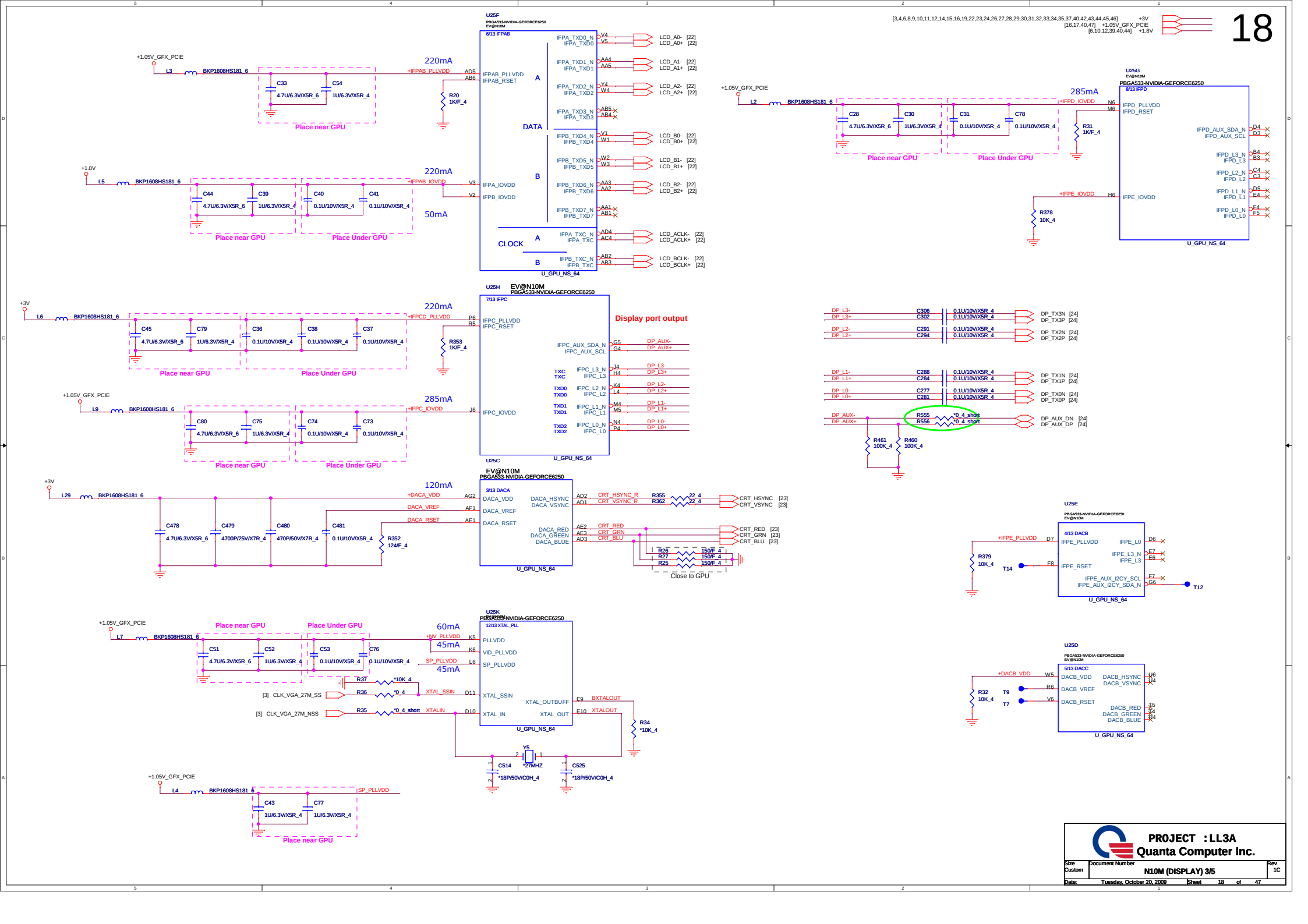
U25F
PBGA533-NVIDIA-GEFORCE6250
EV@N10M
6/13 IFPAB
IFPAB_PLLVDD
IFPAB_RSET
DATA
A
B
CLOCK
IFPA_IOVDD
IFPB_IOVDD
U_GPU_NS_64
+1.05V_GFX_PCIE
L3
BKP1608HS181_6
220mA
+IFPAB_PLLVDD
C33
4.7U/6.3V/X5R_6
C54
1U/6.3V/X5R_4
R20
1K/F_4
Place near GPU
+1.8V
L5
+IFPAB_IOVDD
50mA
C44
C39
C40
0.1U/10V/X5R_4
C41
Place Under GPU
LCD_A0-
LCD_A0+
LCD_A1-
LCD_A1+
LCD_A2-
LCD_A2+
LCD_B0-
LCD_B0+
LCD_B1-
LCD_B1+
LCD_B2-
LCD_B2+
LCD_ACLK-
LCD_ACLK+
LCD_BCLK-
LCD_BCLK+
[3,4,6,8,9,10,11,12,14,15,16,19,22,23,24,26,27,28,29,30,31,32,33,34,35,37,40,42,43,44,45,46] +3V
[16,17,40,47] +1.05V_GFX_PCIE
[6,10,12,39,40,44] +1.8V
U25G
EV@N10M
PBGA533-NVIDIA-GEFORCE6250
8/13 IFPD
IFPD_PLLVDD
IFPD_RSET
IFPE_IOVDD
U_GPU_NS_64
L2
C28
4.7U/6.3V/X5R_6
C30
1U/6.3V/X5R_4
C31
0.1U/10V/X5R_4
C78
285mA
+IFPD_IOVDD
R31
1K/F_4
R378
10K_4
IFPD_AUX_SDA_N
IFPD_AUX_SCL
IFPD_L3_N
IFPD_L3
IFPD_L2_N
IFPD_L2
IFPD_L1_N
IFPD_L1
IFPD_L0_N
IFPD_L0
U25H
EV@N10M
PBGA533-NVIDIA-GEFORCE6250
7/13 IFPC
IFPC_PLLVDD
IFPC_RSET
IFPC_IOVDD
U_GPU_NS_64
Display port output
+3V
L6
BKP1608HS181_6
220mA
+IFPCD_PLLVDD
C45
4.7U/6.3V/X5R_6
C79
1U/6.3V/X5R_4
C36
C38
C37
R353
1K/F_4
+1.05V_GFX_PCIE
L9
285mA
+IFPC_IOVDD
C80
C75
C74
C73
IFPC_AUX_SDA_N
IFPC_AUX_SCL
IFPC_L3_N
IFPC_L3
IFPC_L2_N
IFPC_L2
IFPC_L1_N
IFPC_L1
IFPC_L0_N
IFPC_L0
DP_AUX-
DP_AUX+
DP_L3-
DP_L3+
DP_L2-
DP_L2+
DP_L1-
DP_L1+
DP_L0-
DP_L0+
DP_L3-
DP_L3+
DP_L2-
DP_L2+
C306
C302
C291
C294
DP_TX3N [24]
DP_TX3P [24]
DP_TX2N [24]
DP_TX2P [24]
DP_L1-
DP_L1+
DP_L0-
DP_L0+
C288
C284
C277
C281
DP_TX1N [24]
DP_TX1P [24]
DP_TX0N [24]
DP_TX0P [24]
DP_AUX-
DP_AUX+
R555
R556
*0_4_short
DP_AUX_DN [24]
DP_AUX_DP [24]
R461
100K_4
R460
100K_4
U25C
EV@N10M
PBGA533-NVIDIA-GEFORCE6250
3/13 DACA
DACA_VDD
DACA_VREF
DACA_RSET
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
U_GPU_NS_64
+3V
L29
BKP1608HS181_6
120mA
+DACA_VDD
DACA_VREF
DACA_RSET
C478
4.7U/6.3V/X5R_6
C479
4700P/25V/X7R_4
C480
470P/50V/X7R_4
C481
0.1U/10V/X5R_4
R352
124/F_4
CRT_HSYNC_R
CRT_VSYNC_R
R355
22_4
R362
22_4
CRT_HSYNC [23]
CRT_VSYNC [23]
CRT_RED
CRT_GRN
CRT_BLU
CRT_RED [23]
CRT_GRN [23]
CRT_BLU [23]
R26
R27
R25
150/F_4
Close to GPU
U25E
PBGA533-NVIDIA-GEFORCE6250
EV@N10M
4/13 DACB
IFPE_PLLVDD
IFPE_RSET
IFPE_L0
IFPE_L3_N
IFPE_L3
IFPE_AUX_I2CY_SCL
IFPE_AUX_I2CY_SDA_N
U_GPU_NS_64
+IFPE_PLLVDD
R379
10K_4
T14
T12
U25K
PBGA533-NVIDIA-GEFORCE6250
12/13 XTAL_PLL
PLLVDD
VID_PLLVDD
SP_PLLVDD
XTAL_SSIN
XTAL_OUTBUFF
XTAL_IN
XTAL_OUT
U_GPU_NS_64
+1.05V_GFX_PCIE
L7
BKP1608HS181_6
Place near GPU
Place Under GPU
60mA
+NV_PLLVDD
45mA
SP_PLLVDD
45mA
C51
4.7U/6.3V/X5R_6
C52
1U/6.3V/X5R_4
C53
C76
0.1U/10V/X5R_4
R37
*10K_4
R36
*0_4
XTAL_SSIN
[3] CLK_VGA_27M_SS
R35
*0_4_short
XTALIN
[3] CLK_VGA_27M_NSS
BXTALOUT
XTALOUT
R34
*10K_4
Y5
*27MHZ
C514
*18P/50V/C0H_4
C525
*18P/50V/C0H_4
U25D
PBGA533-NVIDIA-GEFORCE6250
EV@N10M
5/13 DACC
DACB_VDD
DACB_VREF
DACB_RSET
DACB_HSYNC
DACB_VSYNC
DACB_RED
DACB_GREEN
DACB_BLUE
U_GPU_NS_64
+DACB_VDD
R32
10K_4
T9
T7
+1.05V_GFX_PCIE
L4
BKP1608HS181_6
SP_PLLVDD
C43
1U/6.3V/X5R_4
C77
1U/6.3V/X5R_4
Place near GPU
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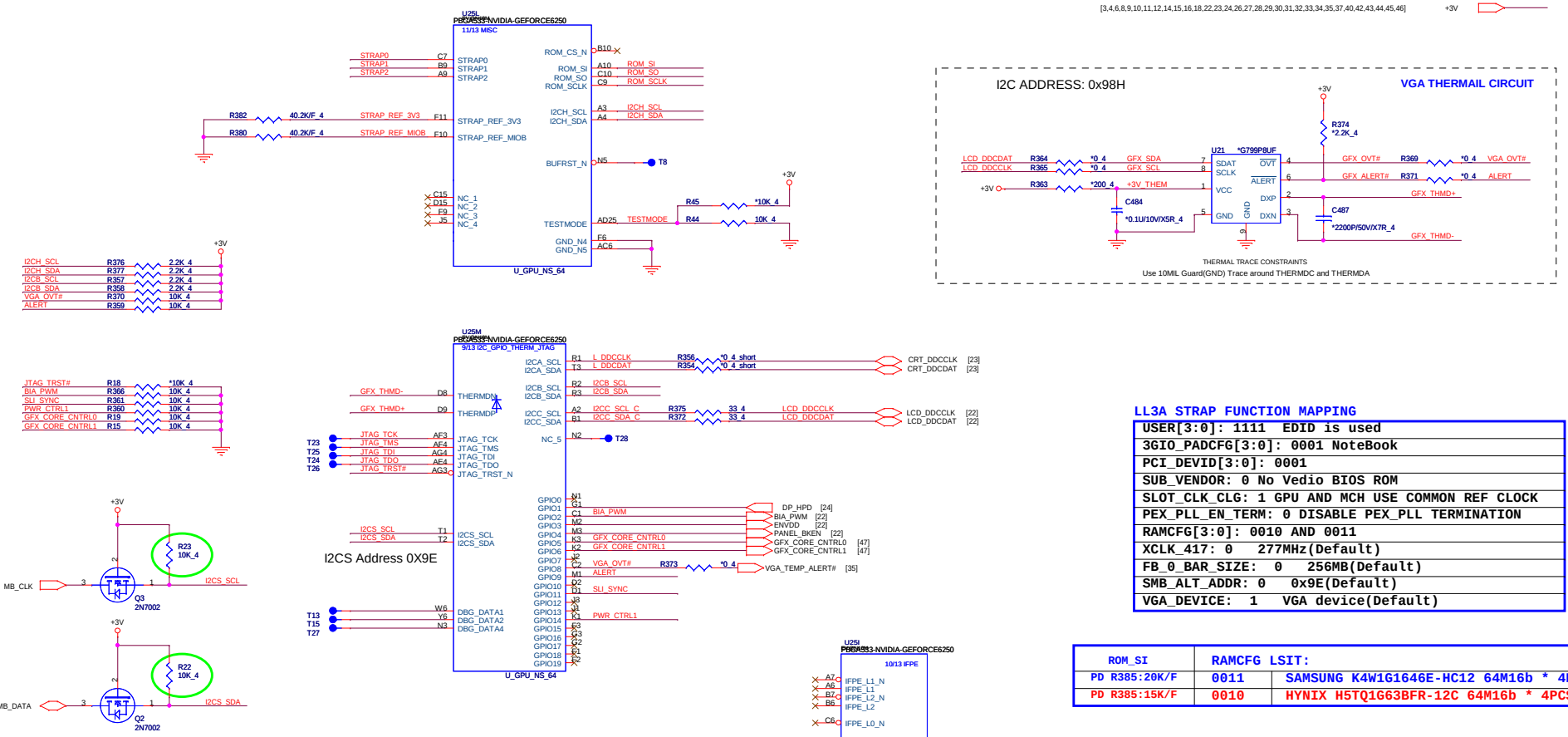


[3,4,6,8,9,10,11,12,14,15,16,18,22,23,24,26,27,28,29,30,31,32,33,34,35,37,40,42,43,44,45,46] +3V

I2C ADDRESS: 0x98H

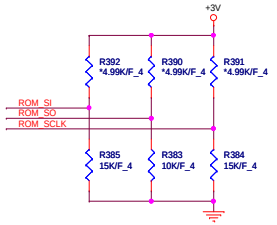
VGA THERMAIL CIRCUIT

LL3A STRAP FUNCTION MAPPING

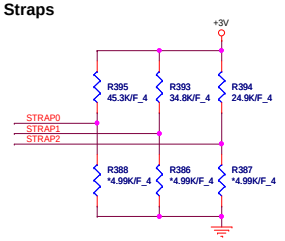
USER[3:0]: 1111 EDID is used
3GIO_PADCFG[3:0]: 0001 NoteBook
PCI_DEVID[3:0]: 0001
SUB_VENDOR: 0 No Vedio BIOS ROM
SLOT_CLK_CLG: 1 GPU AND MCH USE COMMON REF CLOCK
PEX_PLL_EN_TERM: 0 DISABLE PEX_PLL TERMINATION
RAMCFG[3:0]: 0010 AND 0011
XCLK_417: 0 277MHz(Default)
FB_0_BAR_SIZE: 0 256MB(Default)
SMB_ALT_ADDR: 0 0x9E(Default)
VGA_DEVICE: 1 VGA device(Default)

ROM_SI	RAMCFG LSIT:	
PD R385:20K/F	0011	SAMSUNG K4W1G1646E-HC12 64M16b * 4PCS
PD R385:15K/F	0010	HYNIX H5TQ1G63BFR-12C 64M16b * 4PCS

PCI_DEVID[4] / SUBVENDOR



Straps



Logical Strap Bit Mapping

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPIO ASSIGNMENTS

GPIO	NB9X	N10X	I/O	ACTIVE	Function Description
0	General Purpose	General Purpose	I/O	N/A	
1	HPD-C	HPD-C	I	N/A	Hot Plug Detect for IFP Link C
2	LCD0_BL_PWM	LCD0_BL_PWM	O	H	Panel Backlight Brighness Control (PWM Capable)
3	LCD0_VDD	LCD0_VDD	O	H	Panel Power Enable
4	LCD0_BL_PWM	LCD0_BL_PWM	O	H	Panel Backlight ON/OFF
5	GPU_VID0	GPU_VID0	O	N/A	GPU_VID0
6	GPU_VID1	GPU_VID1	O	N/A	GPU_VID1
7	GPU_VID2/MEM_VID	GPU_VID2	O	N/A	GPU_VID2
8	OVERT	OVERT	I/O	L	Thermal Over Temperature
9	FAN_PWM/ALERT	ALERT	I/O	L	Thermal Alert (PWM Capable)
10	MEM_VREF	MEM_VREF	O	N/A	Memory VREF Switch
11	SLI_SYNC	SLI_SYNC	I/O	L	SLI SYNC0
12	AC_DET	PWR_LEVEL (in)	I	N/A	Power Level Detect
13	PWR_CTRL0	MEM_VID (out)	O	L	MEM_VID0
14	PWR_CTRL1	PWR_CTRL1	O	N/A	Power Supply Control
15	HPD-E	HPD-E	I	N/A	Hot Plug Detect for IFP Link E
16	DVI_MODE1	FAN_PWM(out)	O		Fan PWM Control
17	HDMI_DETECT0	Reserved	N/A		
18	DVI_MODE1	Reserved	N/A		
19	HDMI_DETECT1	HPD-D	I	N/A	Hot Plug Detect for IFP Link D

Starps	NB9X	N10X	Function Description
ROM_SO	XCLK_277 TVMODE(2) TVMODE(1) TVMODE(0)	XCLK_277 TVMODE(2) TVMODE(1) TVMODE(0)	55nm PU 5K/F ohm 40nm PD 10K/F ohm
ROM_SCLK	PCI_DEVID_EXT SUB_VENDOR SLOT_CLK_CFG PEX_PLL_EN_TERM	PCI_DEVID_EXT SUB_VENDOR SLOT_CLK_CFG PEX_PLL_EN_TERM	55nm/40nm PD 15K/F ohm
ROM_SI	RAMCFG(3) RAMCFG(2) RAMCFG(1) RAMCFG(0)	RAMCFG(3) RAMCFG(2) RAMCFG(1) RAMCFG(0)	Hynix PD 15K/F ohm Samsung PD 20K/F ohm
Strap 2	PCI_DEVID(3) PCI_DEVID(2) PCI_DEVID(1) PCI_DEVID(0)	PCI_DEVID(3) PCI_DEVID(2) PCI_DEVID(1) PCI_DEVID(0)	55nm PU 25K/F ohm 40nm/GS PU 10K/F ohm 40nm/GE PU 5K/F ohm 40nm/NS PU 25K/F ohm
Strap 1	3GIO_PADCFG(3) 3GIO_PADCFG(2) 3GIO_PADCFG(1) 3GIO_PADCFG(0)	3GIO_PADCFG(3) 3GIO_PADCFG(2) 3GIO_PADCFG(1) 3GIO_PADCFG(0)	40nm/NS PU 34.9K/F ohm
Strap 0	USER(3) USER(2) USER(1) USER(0)	USER(3) USER(2) USER(1) USER(0)	

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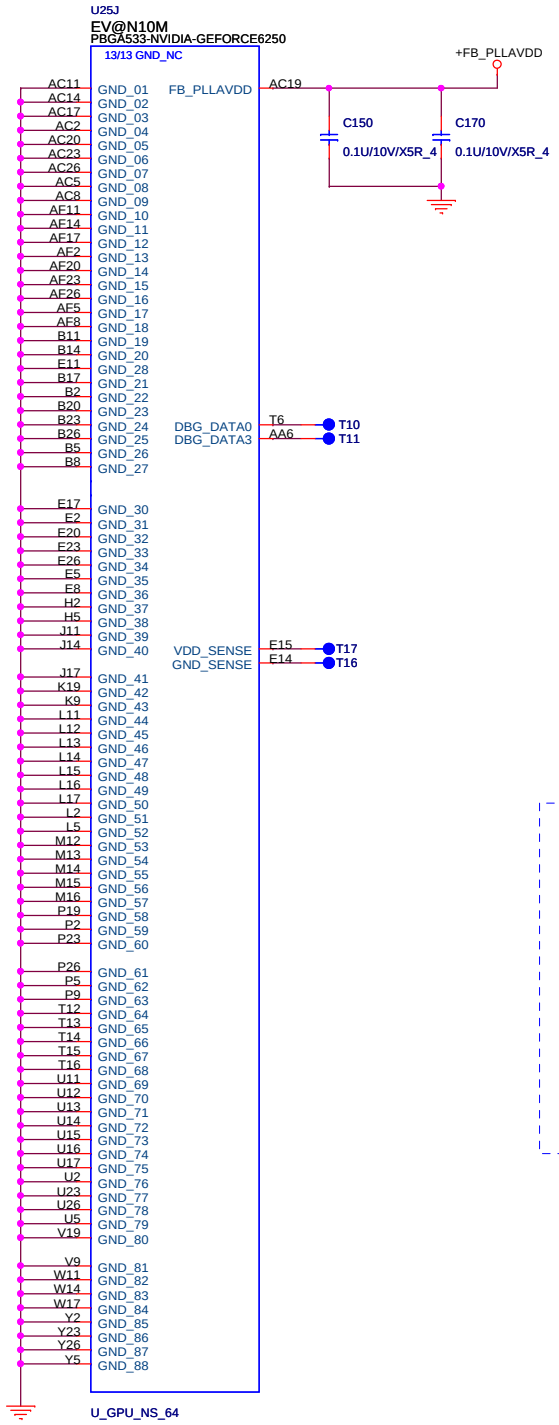
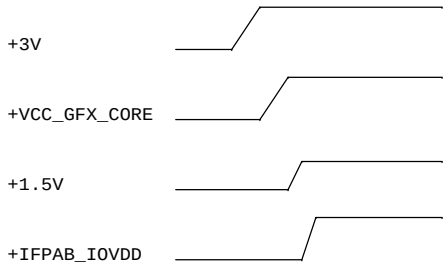


power up sequence



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256MB/ 512MB DDR3

[17] M_MDA[63..0] M_MDA[63..0]
[17] M_QSA[7..0] M_QSA[7..0]
[17] M_QSA#[7..0] M_QSA#[7..0]
[17] M_DQMA#[7..0] M_DQMA#[7..0]

[3,17,30,31,32,33,39,43] +1.5V

U4 — VRAM_DDR3 — 96-BALL SDRAM DDR3
U28 — VRAM_DDR3 — 96-BALL SDRAM DDR3
U27 — VRAM_DDR3 — 96-BALL SDRAM DDR3
U5 — VRAM_DDR3 — 96-BALL SDRAM DDR3

Should be 240 Ohms +-1%
R51 243/F_4
R447 243/F_4
R406 243/F_4
R103 243/F_4

R52 4.99K/F_4
R53 4.99K/F_4
R97 4.99K/F_4
R98 4.99K/F_4
R100 4.99K/F_4
R101 4.99K/F_4
R50 4.99K/F_4
R49 4.99K/F_4
R55 4.99K/F_4
R54 4.99K/F_4
R444 4.99K/F_4
R445 4.99K/F_4
R106 4.99K/F_4
R105 4.99K/F_4
R72 4.99K/F_4
R70 4.99K/F_4

VREFC_VMA1 VREFD_VMA1 VREFC_VMA2 VREFD_VMA2 VREFC_VMA3 VREFD_VMA3 VREFC_VMA4 VREFD_VMA4

C204 0.1U/10V/X5R_4
C239 0.1U/10V/X5R_4
C240 0.1U/10V/X5R_4
C203 0.1U/10V/X5R_4
C205 0.1U/10V/X5R_4
C584 0.1U/10V/X5R_4
C247 0.1U/10V/X5R_4
C208 0.1U/10V/X5R_4

close to U3003 AND U3004
C248 C600 C596 C569 C598 — 10U/6.3V/X5R_6

close to U3003
C246 C242 1U/6.3V/X5R_4 C245 C223 C241 C238 C224 — 1U/6.3V/X5R_4
C219 1U/6.3V/X5R_4

close to U3004
C591 C572 C582 C585 C581 C592 C586 C593 — 1U/6.3V/X5R_4

close to U3006 AND U3007
C597 C233 C225 C580 C599 — 10U/6.3V/X5R_6

close to U3006
C213 C237 C576 C236 C244 C243 C588 C567 — 1U/6.3V/X5R_4

close to U3007
C595 C573 C589 C590 C574 C594 C583 C587 — 1U/6.3V/X5R_4

CLKA1 R442 243/F_4 CLKA1#
CLKA0 R443 243/F_4 CLKA0#
Place near VRAM

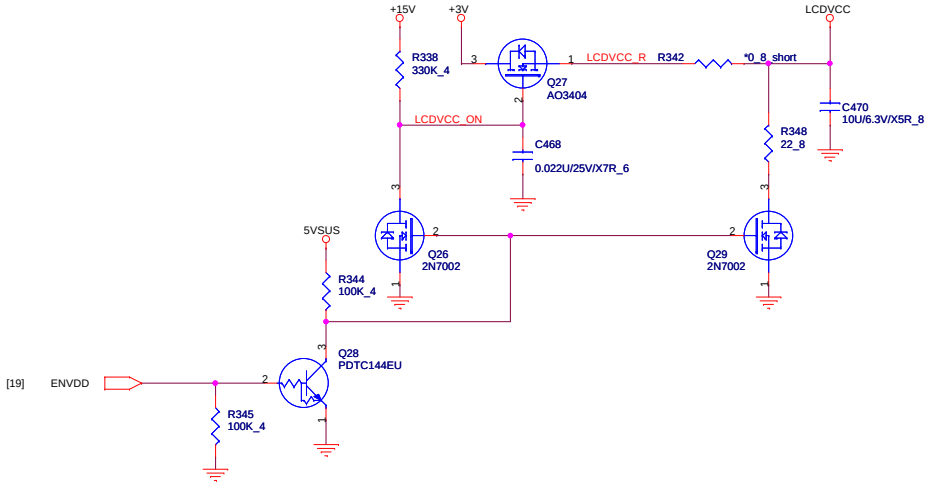
MB ASSY' PN	Memory Straps	
31GC5MB0000	800MHz 512MB(64M*16)	AKD5LZGTW00 QuantaBuy
		AKD5LZGTW02 VOL B/S
		QuantaBuy
		VOL B/S
		QuantaBuy
		VOL B/S
		QuantaBuy
		VOL B/S
		QuantaBuy
		VOL B/S
		QuantaBuy
		VOL B/S

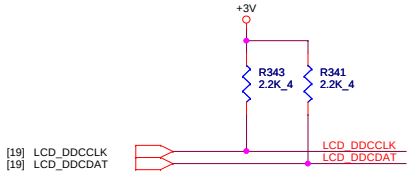
PROJECT : LL3A
Quanta Computer Inc.

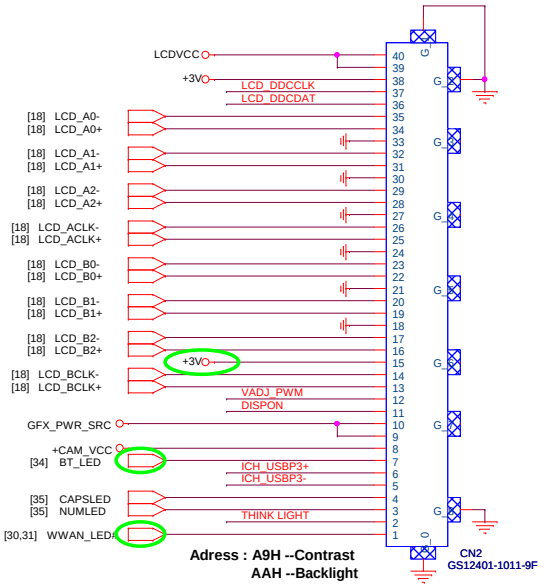
Size	Document Number	Rev
Custom	VRAM_DDR3_512M	1C
Date: Tuesday, October 20, 2009	Sheet 21 of 47	

[3,4,6,8,9,10,11,12,14,15,16,18,19,23,24,26,27,28,29,30,31,32,33,34,35,37,40,42,43,44,45,46] +3V
[28,40,43,45] +15V
[39,40,46] 5VSUS
[9,25,28,35,36,37,39,40,42,44,45,47] 3VPCU
[39,41,42,43,44,45,46,47] VIN
[12,23,24,26,28,34,35,36,37,38,40,42] +5V

LCDVCC

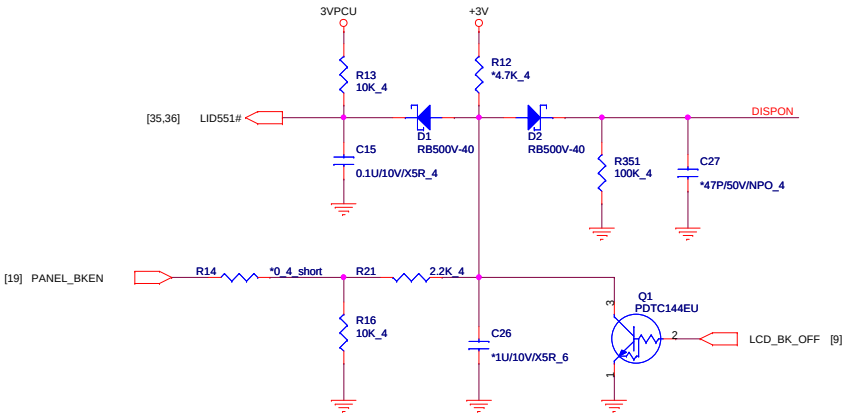




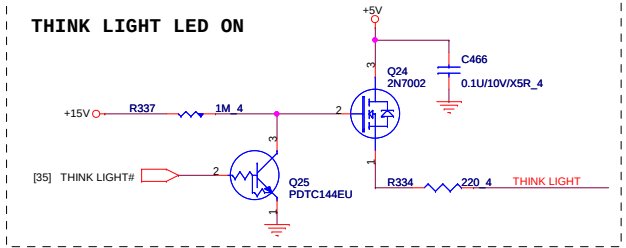


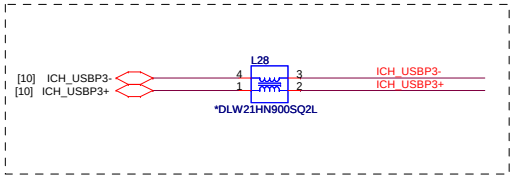
Adress : A9H --Contrast
AAH --Backlight

back light

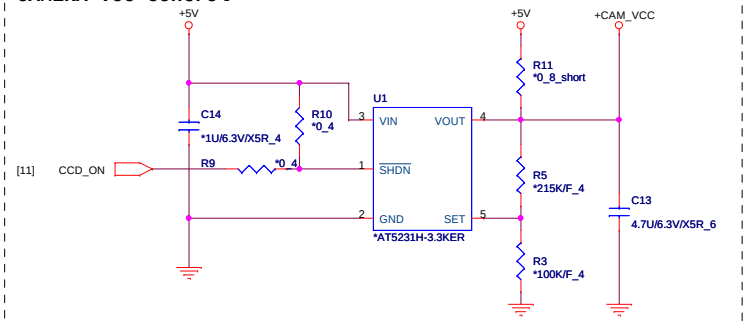


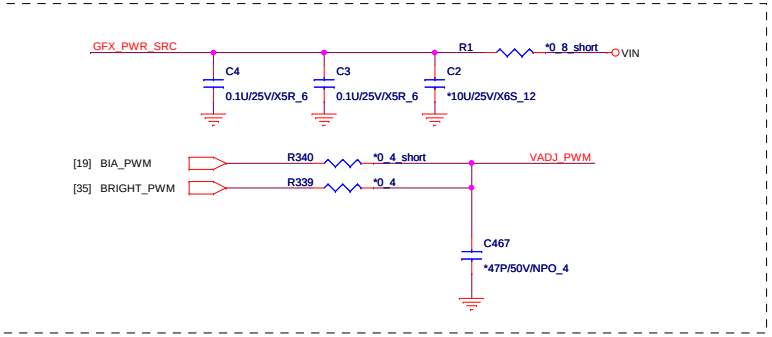
THINK LIGHT LED ON





CAMERA VCC Control





PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN	1C
Date: Tuesday, October 20, 2009	Sheet 22 of 47	

[12,22,24,26,28,34,35,36,37,38,40,42] +5V
[3,4,6,8,9,10,11,12,14,15,16,18,19,22,24,26,27,28,29,30,31,32,33,34,35,37,40,42,43,44,45,46] +3V

Layout Note:
Setting R,G,B trace
impedance to 50 ohm.

[18] CRT_RED
[18] CRT_GRN
[18] CRT_BLU

L15 BLM18BA470SN1
L14 BLM18BA470SN1
L12 BLM18BA470SN1

CRT_R1
CRT_G1
CRT_B1

R43 150/F_4
R41 150/F_4
R39 150/F_4
C196 5.6P/50V/COG_4
C186 5.6P/50V/COG_4
C165 5.6P/50V/COG_4
C164 5.6P/50V/COG_4
C185 5.6P/50V/COG_4
C195 5.6P/50V/COG_4

TP2

CRT_VCC
D3 RB500V-40
C127 0.1U/10V/X5R_4
+5V
F1 FUSE1A6V_POLY
CRT_VCC_R
C133 *VARISTOR_4

CN24 070546FR015S238CR

ESD PROTECTION

D20 *TVSS5VESPT CRT_R1
D19 *TVSS5VESPT CRT_G1
D18 *TVSS5VESPT CRT_B1
D16 *TVSS5VESPT CRTVSYNC
D17 *TVSS5VESPT CRTHSYNC
D15 *TVSS5VESPT DDCCLK3
D21 *TVSS5VESPT DDCDAT3

+5V

[18] CRT_VSYNC
[18] CRT_HSYNC

U22 AHCT1G125DCH
U23 AHCT1G125DCH

C83 0.1U/10V/X5R_4

VGAVSYNC_R
VGAHSYNC_R

R33 10_4
R38 10_4

Place near
U5001,U5002 < 200 mil

CRTVSYNC1
CRTHSYNC1

C111 *10P/50V/COG_4
C65 *10P/50V/COG_4

L8 HB-1T1608-121JT CRTVSYNC
L10 HB-1T1608-121JT CRTHSYNC

C117 10P/50V/COG_4
C88 10P/50V/COG_4

Place near CN5002 connector
< 200 mil

+3V
CRT_VCC

R48 10K_4
R29 10K_4
R46 2.2K_4
R30 2.2K_4

[19] CRT_DDCCLK
[19] CRT_DDCDAT

Q30 2N7002K-T1-E3
Q32 2N7002K-T1-E3

DDCCLK2 R28 *0_6_short DDCCLK3
DDCDAT2 R47 *0_6_short DDCDAT3

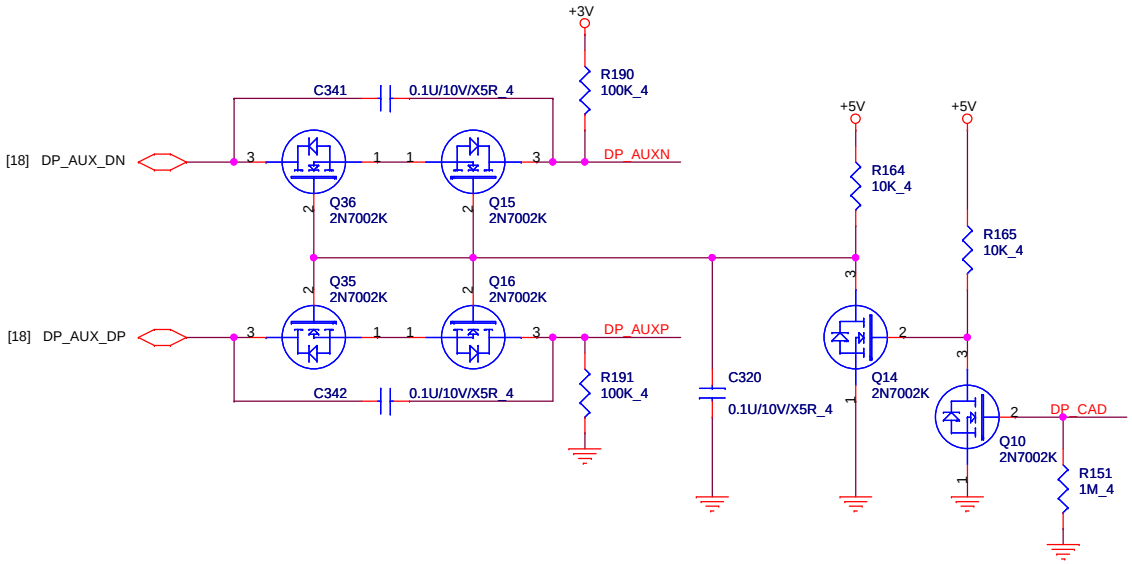
C202 *10P/50V/COG_4
C49 *10P/50V/COG_4

PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT CONN	1C
Date: Tuesday, October 20, 2009	Sheet 23 of 47	

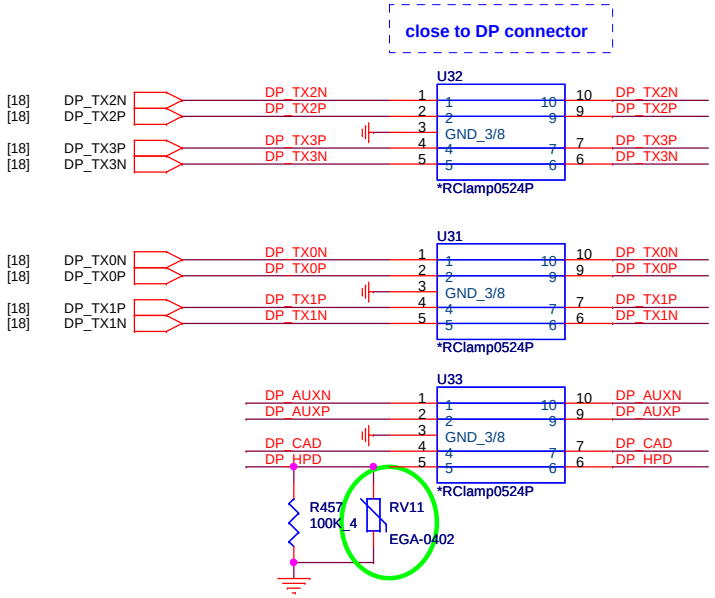
DisplayPort

[3,4,6,8,9,10,11,12,14,15,16,18,19,22,23,26,27,28,29,30,31,32,33,34,35,37,40,42,43,44,45,46] +3V
[12,22,23,26,28,34,35,36,37,38,40,42] +5V

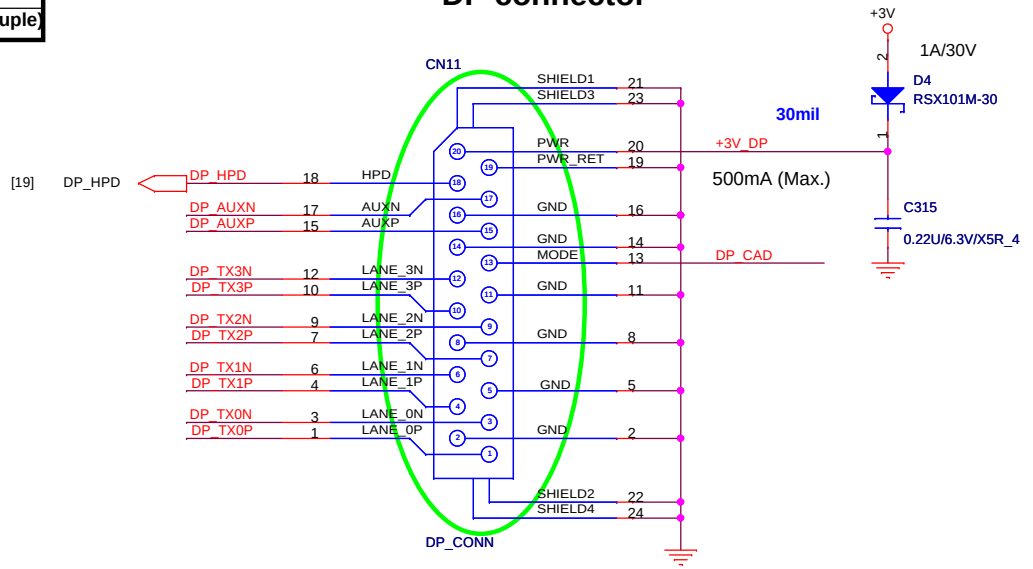


DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)

ESD Protect



DP connector

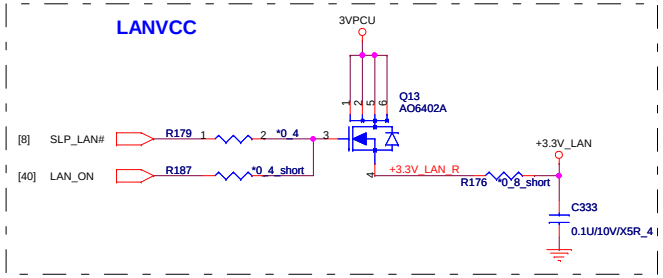


PROJECT : LL3A
Quanta Computer Inc.

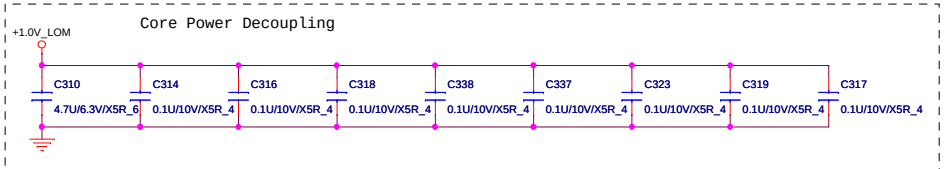
Size	Document Number	Rev
Custom	DISPLAYPORT CONN	1C
Date: Tuesday, October 20, 2009	Sheet 24 of 47	

[4,8,9,10,11,12,31,40] 3V_S5
[3,4,6,8,9,10,11,12,40,44,46] +1.05V_VTT
[9,22,28,35,36,37,39,40,42,44,45,47] 3VPCU

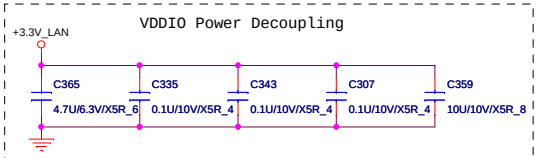
LANVCC



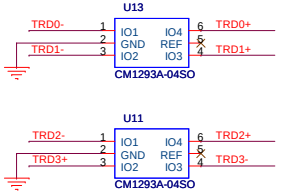
Core Power Decoupling

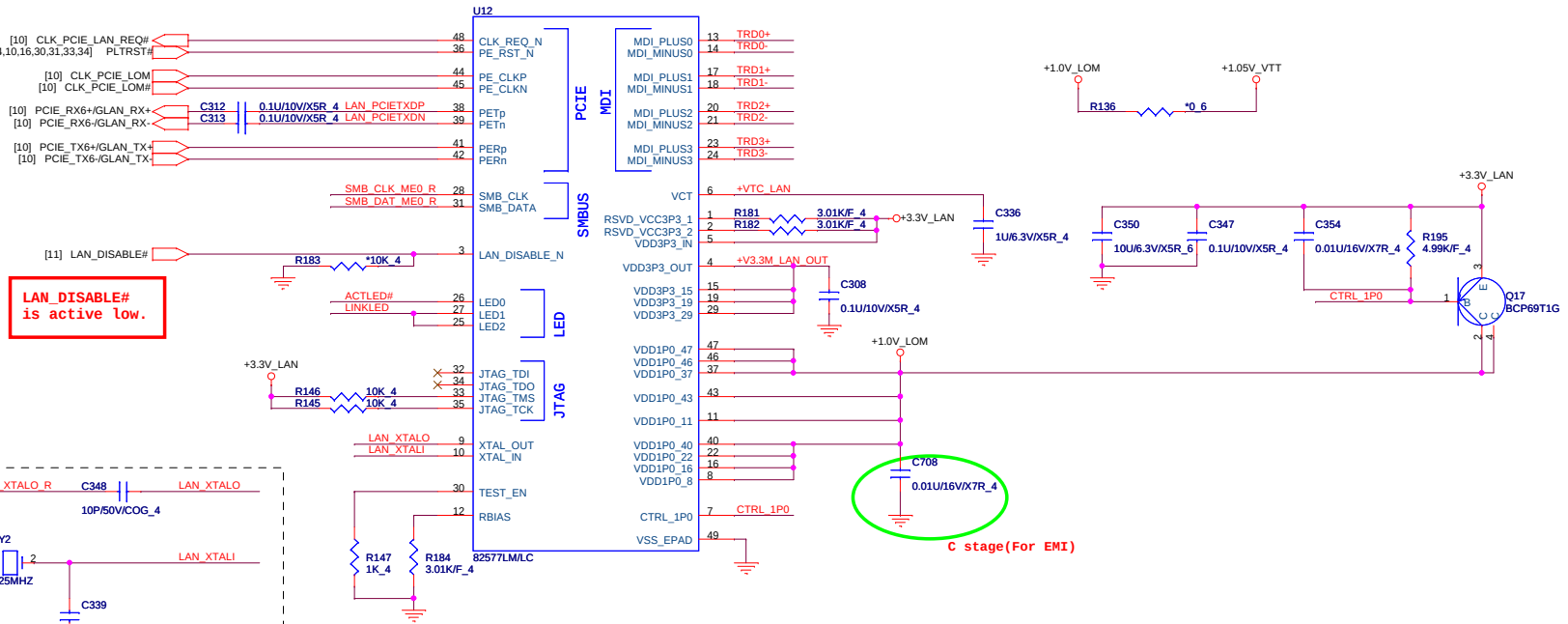


VDDIO Power Decoupling

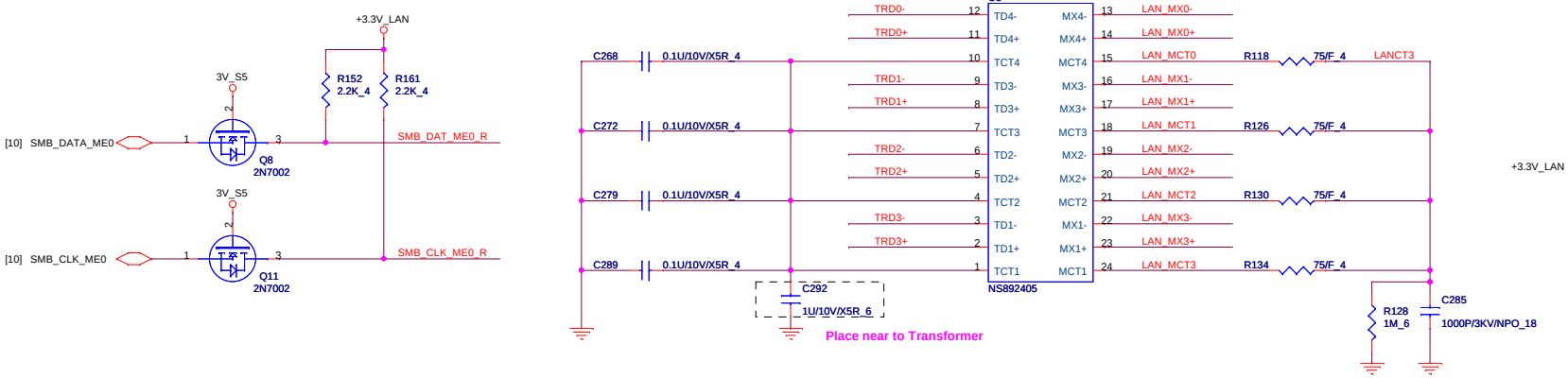


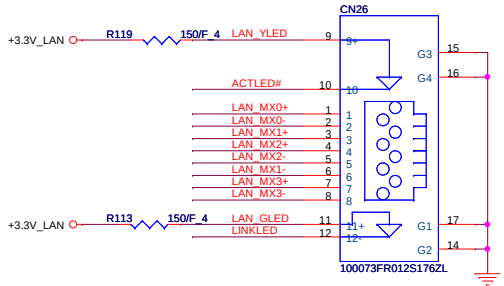
RJ45 Connector





Tramsformer





PROJECT : LL3A		
Quanta Computer Inc.		
Size: Custom	Document Number: LAN(82577LM)	Rev: 1C
Date: Tuesday, October 20, 2009	Sheet 25 of 47	

Close to codec (12mA)

DVDD_IO should match HDA Bus.

Close to codec

Close to codec (66mA)

(1.35A)

Close to codec

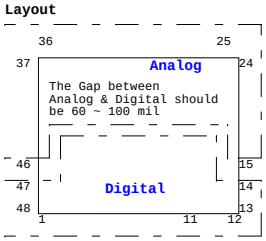
U17 — 92HD81B1B5NLGXYDX8

92HD81:
AVDD:65.72mA
PVDD:1.35A
DVDD,DVDD_IO:120mA

Codec

PORT_X Pin: W/S=10/12
VREFOUT_X Pin: W/S=10/10
Power Pin : 20mil

Layout



Sense_A	Sense_B	RES
Port_ A	Port_ E	39.2K
Port_ B	Port_ F	20K

INT Speaker

CN16 R-SPEAKERS
CN17 L-SPEAKERS

INT MIC

CN9 RTC_CON

PC BEEP

U15 TC7SH86FU

EMI Reserved

C stage

Layout Note:
Place close to Audio Codec.

Headphone out

CN15 HEADPHONE_JACK

Normal Open

External Microphone Jack

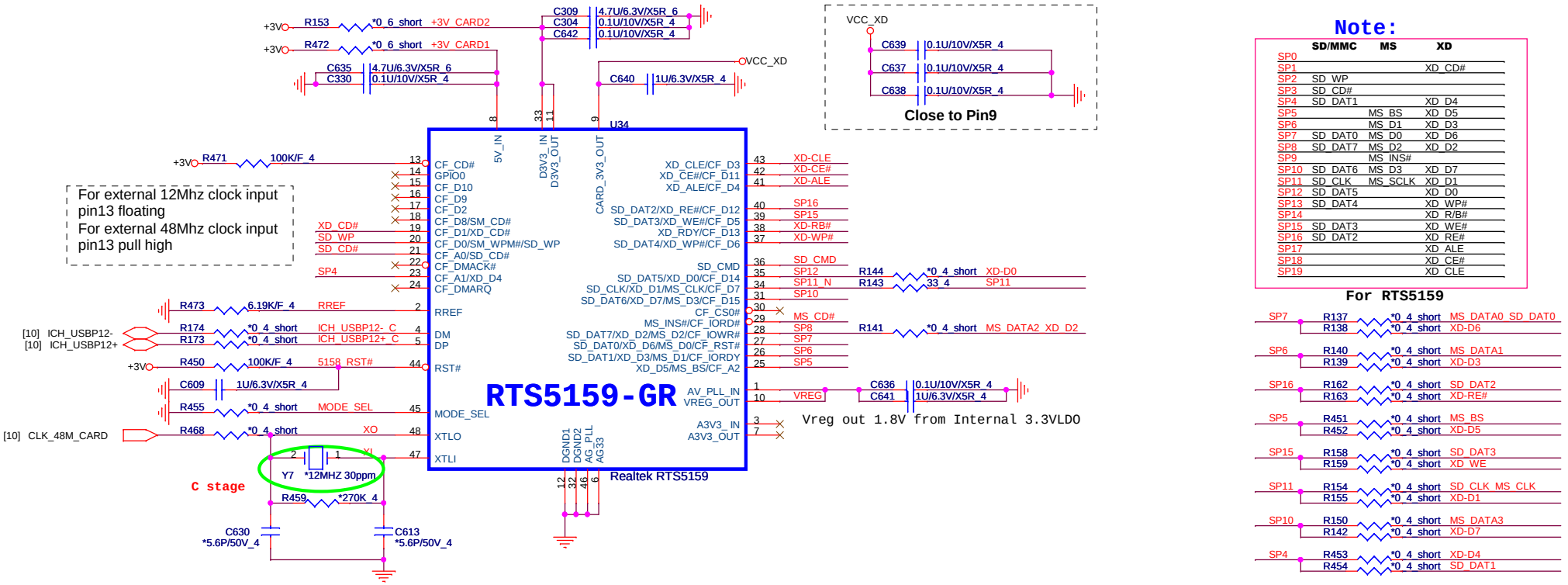
Stereo MIC

CN13 MIC_JACK

Normal Open

PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AUDIO CODEC (IDT 92HD81)	1C
Date: Tuesday, October 20, 2009	Sheet 26 of 47	



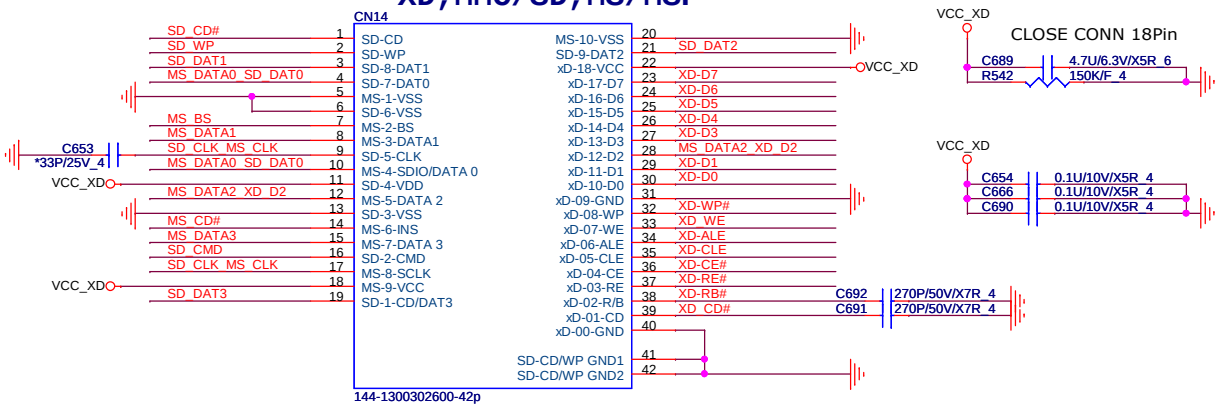
Note:

	SD/MMC	MS	XD
SP0			
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

For RTS5159

SP7	R137	*0_4_short	MS_DATA0_SD_DAT0
	R138	*0_4_short	XD-D6
SP6	R140	*0_4_short	MS_DATA1
	R139	*0_4_short	XD-D3
SP16	R162	*0_4_short	SD_DAT2
	R163	*0_4_short	XD-RE#
SP5	R451	*0_4_short	MS_BS
	R452	*0_4_short	XD-D5
SP15	R158	*0_4_short	SD_DAT3
	R159	*0_4_short	XD_WE
SP11	R154	*0_4_short	SD_CLK_MS_CLK
	R155	*0_4_short	XD-D1
SP10	R150	*0_4_short	MS_DATA3
	R142	*0_4_short	XD-D7
SP4	R453	*0_4_short	XD-D4
	R454	*0_4_short	SD_DAT1

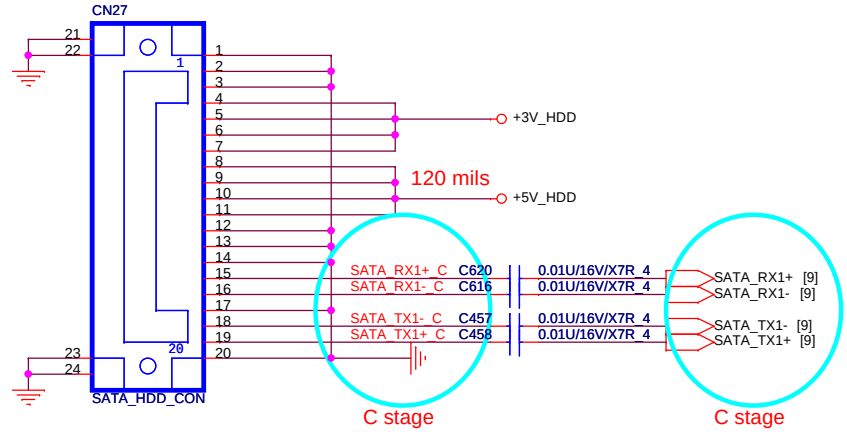
5 IN1 CARD READER
XD,MMC/SD,MS/MSP



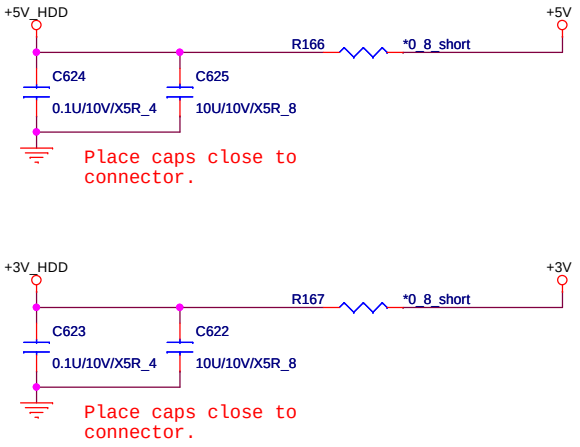
PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
B	Card Reader (RTS5159)	1C
Date: Tuesday, October 20, 2009	Sheet 27 of 47	

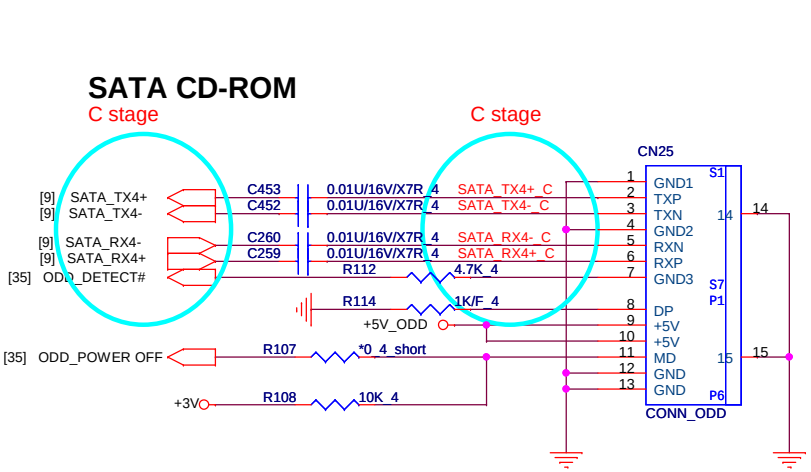
SATA-HDD CONNECTOR

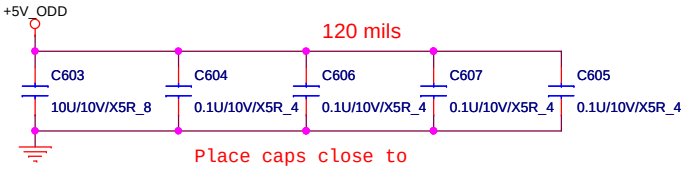


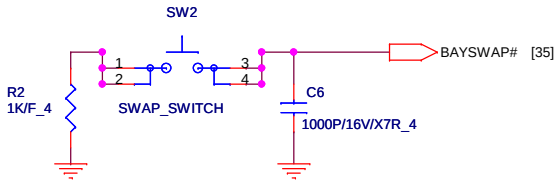
[3,4,6,8,9,10,11,12,14,15,16,18,19,22,23,24,26,27,29,30,31,32,33,34,35,37,40,42,43,44,45,46] +3V
[12,22,23,24,26,34,35,36,37,38,40,42] +5V
[22,40,43,45] +15V
[9,40,43,44,45,47] 5VPCU
[9,22,25,35,36,37,39,40,42,44,45,47] 3VPCU

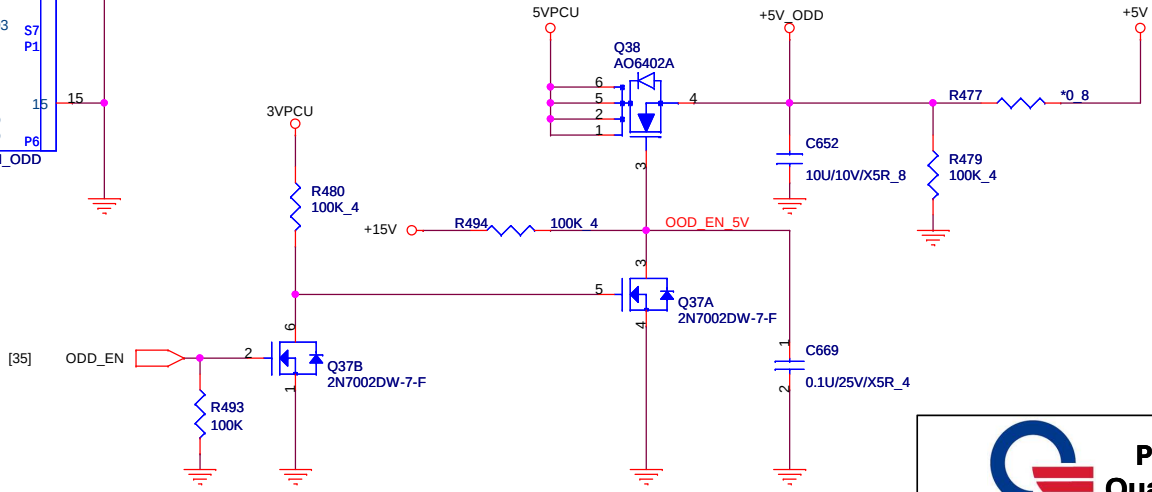


SATA CD-ROM





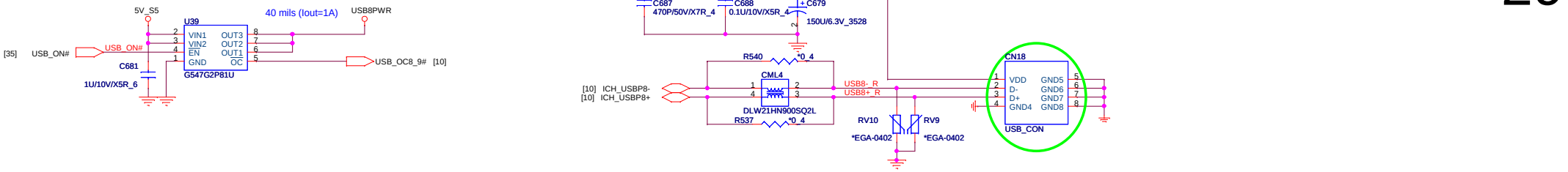




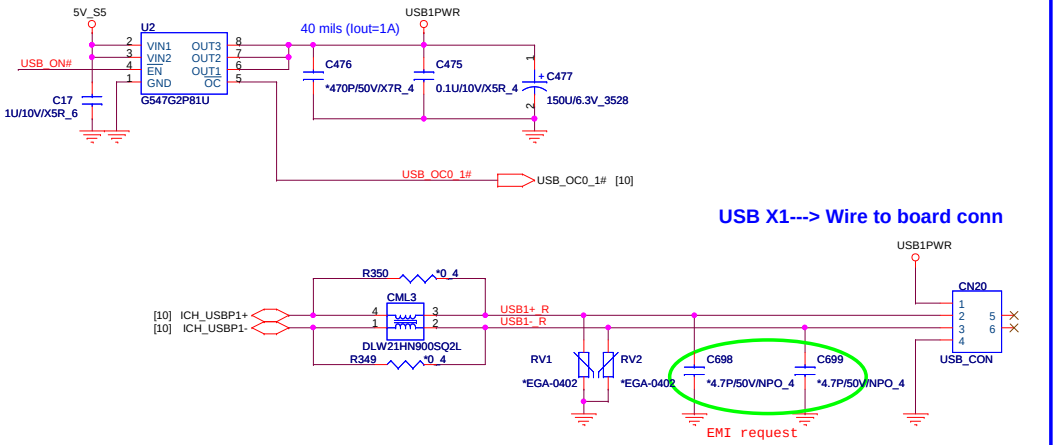
PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/ODD	1C
Date: Tuesday, October 20, 2009	Sheet 28 of 47	

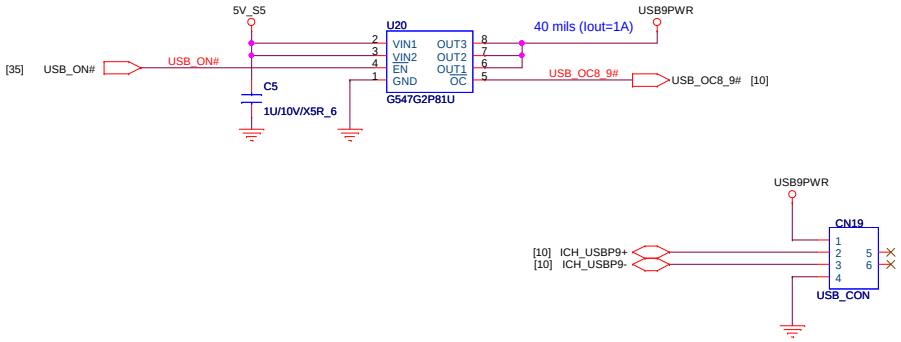
USB 3



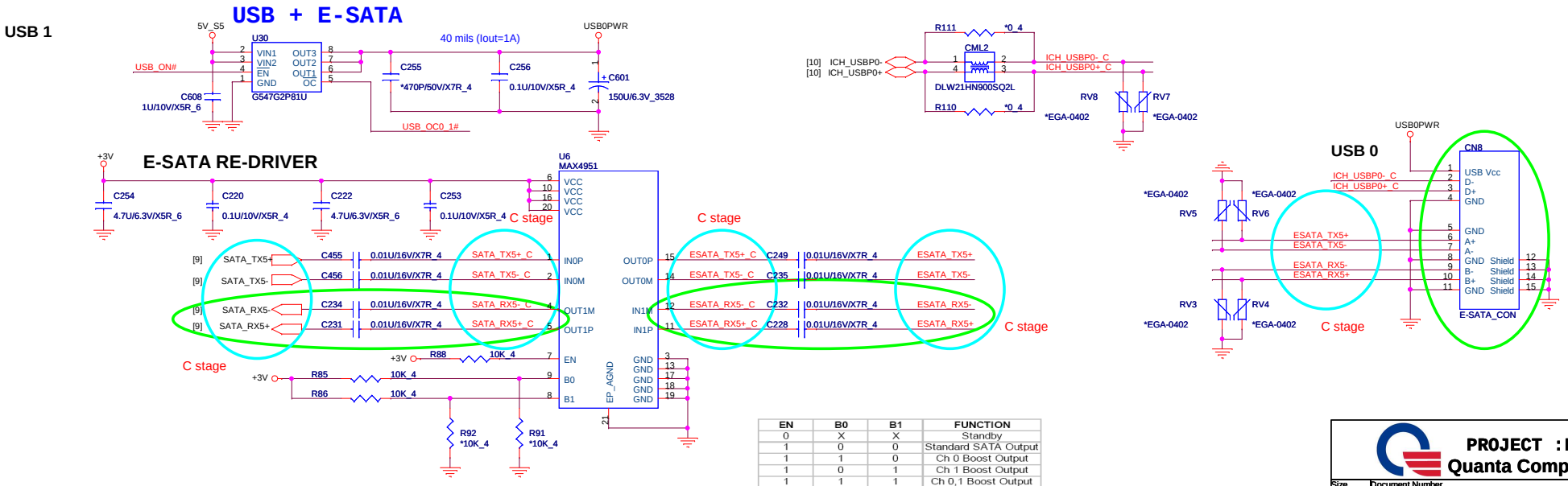
USB 2



USB 4



USB 1



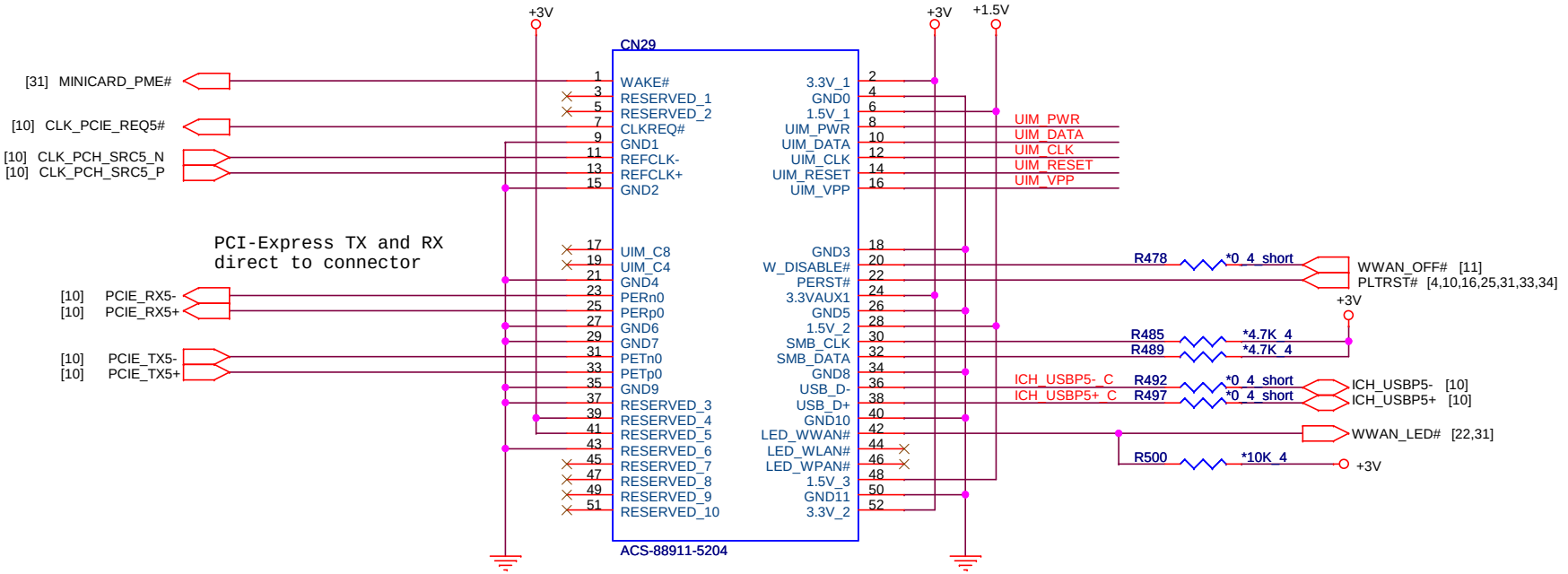
EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

PROJECT : LL3A
Quanta Computer Inc.

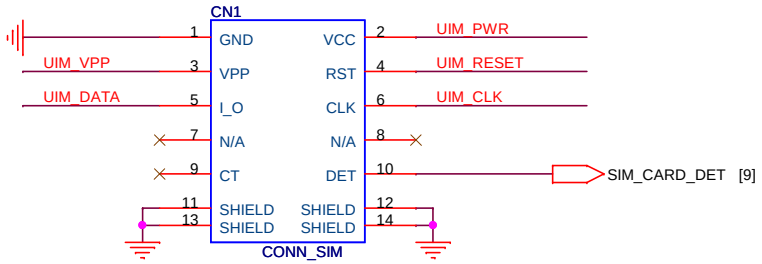
Size	Document Number	Rev
Custom	USB X3/USB+ESATA	1C
Date: Tuesday, October 20, 2009	Sheet 29 of 47	

[3,4,6,8,9,10,11,12,14,15,16,18,19,22,23,24,26,27,28,29,31,32,33,34,35,37,40,42,43,44,45,46] +3V
[3,17,21,31,32,33,39,43] +1.5V

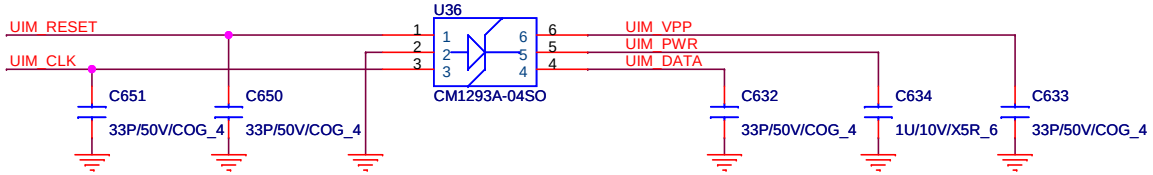
MiniCard WWAN connector

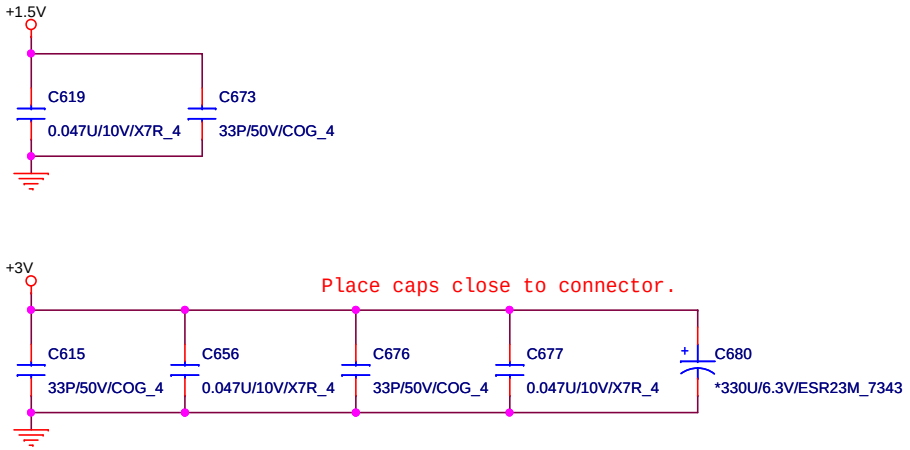


SIM Card CONN



Layout Note:
UIM_RESET,UIM_CLK,UIM_DATA routting as short as possible



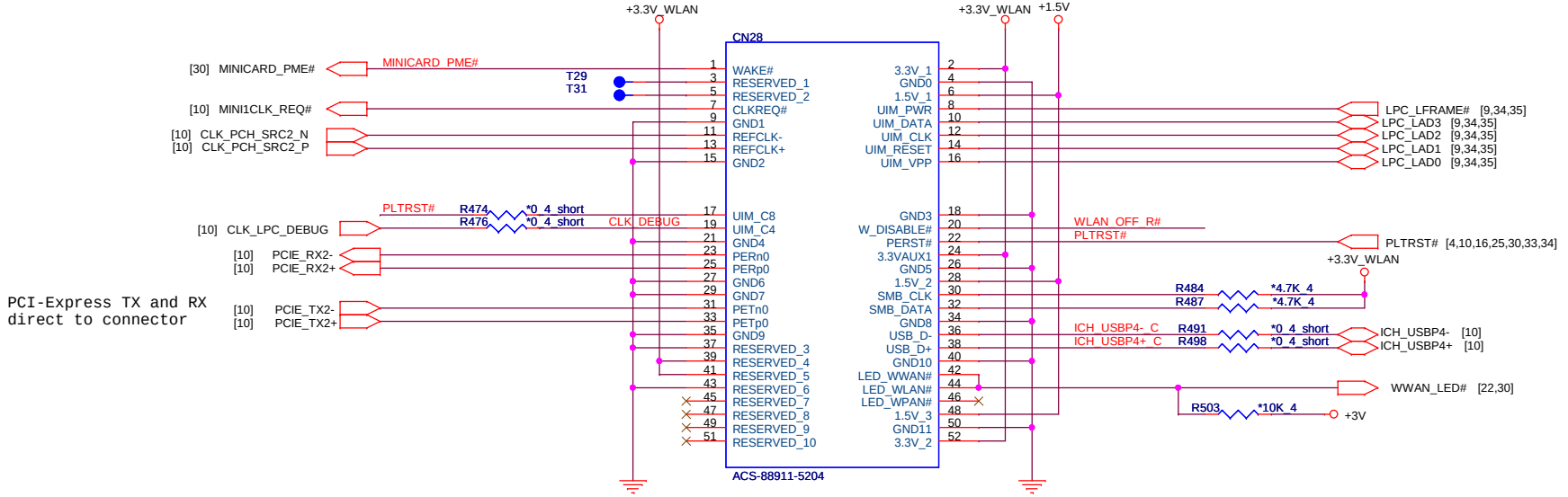


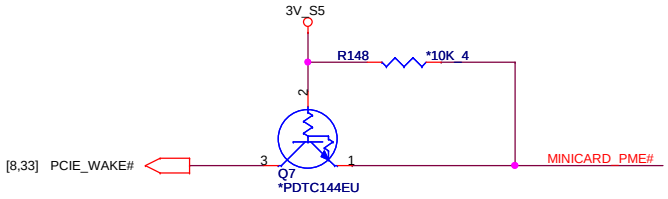
PROJECT : LL3A
Quanta Computer Inc.

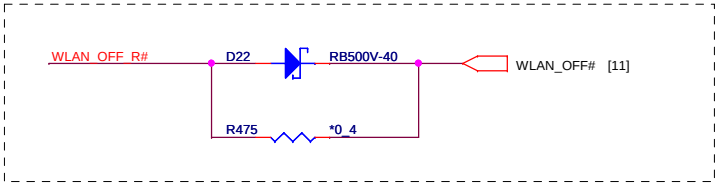
Size	Document Number	Rev
Custom	MINI-Card (WWAN)	1C
Date: Tuesday, October 20, 2009	Sheet 30 of 47	

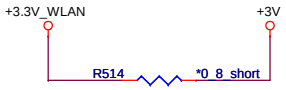
[3,4,6,8,9,10,11,12,14,15,16,18,19,22,23,24,26,27,28,29,30,32,33,34,35,37,40,42,43,44,45,46] +3V
[3,17,21,30,32,33,39,43] +1.5V
[4,8,9,10,11,12,25,40] 3V_S5

MiniCard WLAN/WiMAX connector

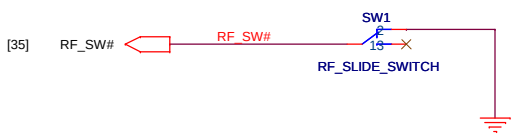


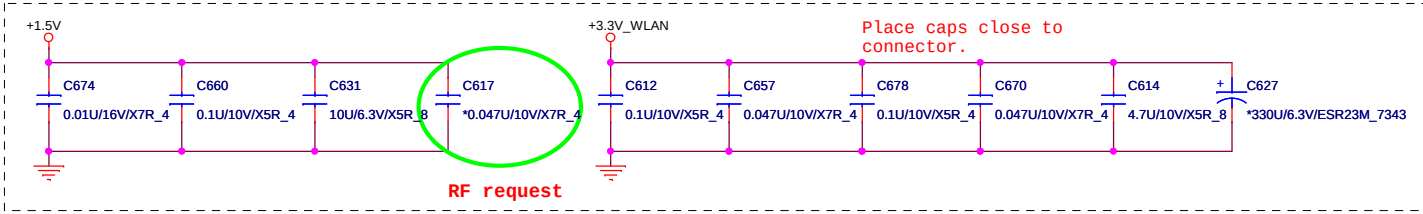






RF ON/OFF SWITCH





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Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI-Card (WLAN)	1C
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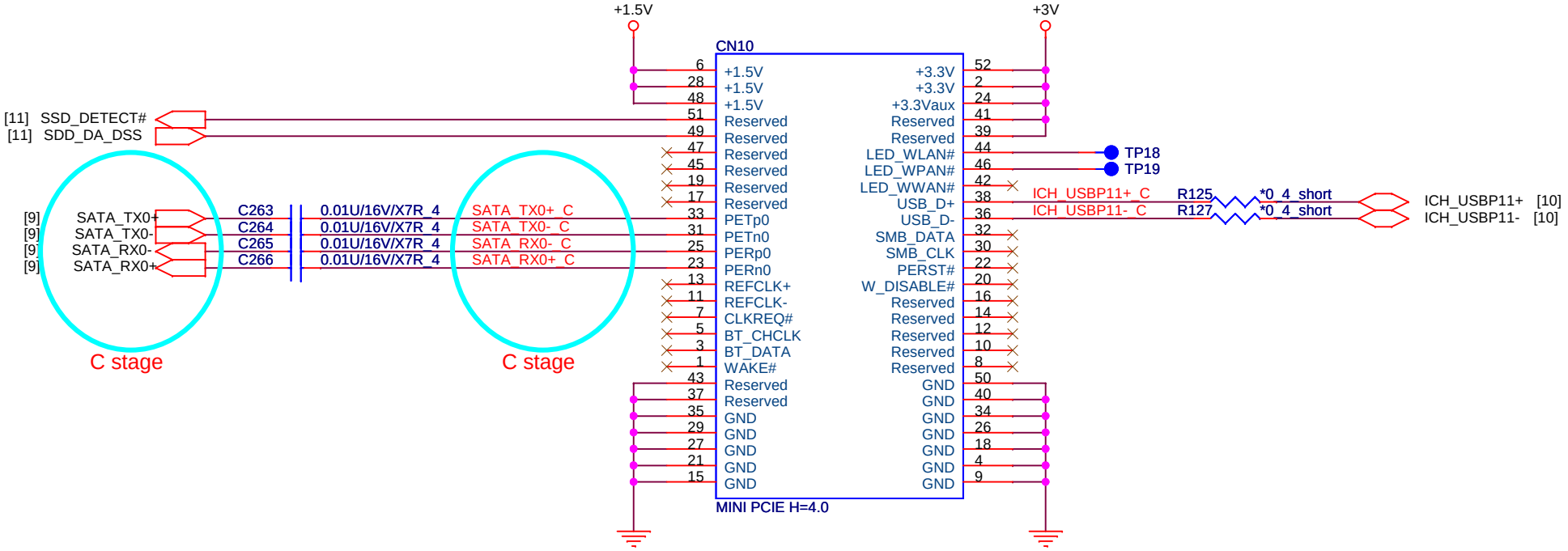
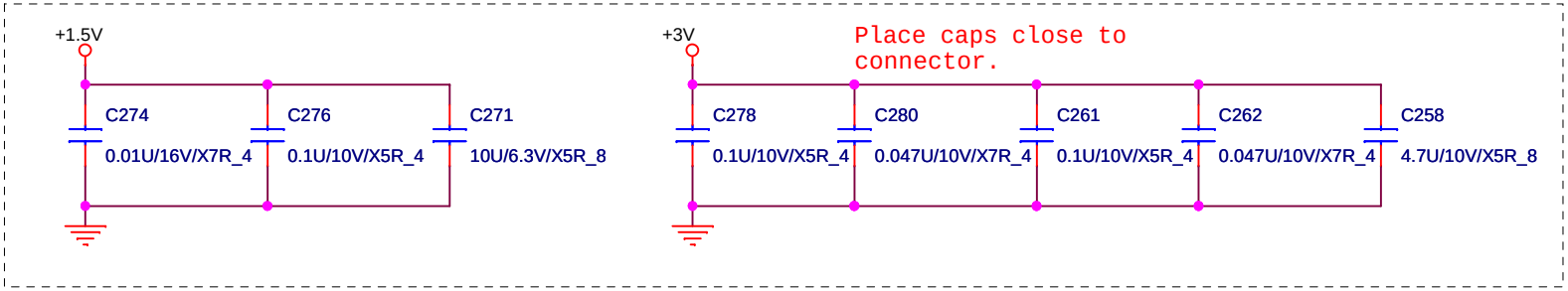
Mini PCI-E Card 3 SSD

[3,17,21,30,31,33,39,43] +1.5V
[3,4,6,8,9,10,11,12,14,15,16,18,19,22,23,24,26,27,28,29,30,31,33,34,35,37,40,42,43,44,45,46] +3V





PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI Card (SSD)	1C
Date: Tuesday, October 20, 2009	Sheet 32 of 47	

Express Card

[3,4,6,8,9,10,11,12,14,15,16,18,19,22,23,24,26,27,28,29,30,31,32,34,35,37,40,42,43,44,45,46] +3V
[3,17,21,30,31,32,39,43] +1.5V
[34,35,40,47] 3VSUS

33

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA.

[10] ICH_USBP2+
[10] ICH_USBP2-
L30
*DLW21HN900SQ2L
ICH_USBP2+
ICH_USBP2-

U35
ExpressSwitch
G577BSR91U/ RT9716AGQW
+1.5V +3V 3VSUS
+3.3V_CARDAUX +3.3V_CARD +1.5V_CARD
AUXIN AUXOUT
3.3VIN_0 3.3VOUT_0
3.3VIN_1 3.3VOUT_1
1.5VIN_0 1.5VOUT_0
1.5VIN_1 1.5VOUT_1
SHDN# PERST#
STBY# CPPE#
SYSRST# CPUSB#
OC#
NC
GND0
RCLKEN

3VSUS R458 *100K_4 2231_SHDN#
R456 *100K_4 2231_STBY#
[4,10,16,25,30,31,34] PLTRST#
CARD_RESET#
EXPRCRD_PWREN# R470 *100K_4
CPUSB# R469 *100K_4
T30
T32

CN12
48303-0033
GND_1
USB-
USB+
CPUSB#
RSV_0
RSV_1
SMBCLK
SMBDATA
+1.5V_0
+1.5V_1
WAKE#
+3.3VAUX
PERST#
+3.3V_1
+3.3V_2
CLKREQ#
CPPE#
REFCLK-
REFCLK+
GND_2
PERn0
PERp0
GND_3
PETn0
PETp0
GND_4
NC1 NC2 NC3 NC4 NC5
ICH_USBP2-
ICH_USBP2+
CPUSB#
+3.3V_CARDAUX
R495 10K_4
R490 10K_4
+1.5V_CARD
[8,31] PCIE_WAKE#
+3.3V_CARDAUX
CARD_RESET#
+3.3V_CARD
[10] CARD_CLK_REQ#
EXPRCRD_PWREN#
[10] CLK_PCH_SRC4_N
[10] CLK_PCH_SRC4_P
[10] PCIE_RX4-
[10] PCIE_RX4+
[10] PCIE_TX4-
[10] PCIE_TX4+

PCI-Express TX and RX direct to connector.

JAE PX10FS16PH-26P

+1.5V C644 0.1U/10V/X5R_4 10
Please the cap near pin 12 & 14(1.5VIN).

+3V C611 0.1U/10V/X5R_4 10
Please the cap near pin 2 & 4 (3.3VIN).

3VSUS C626 0.1U/10V/X5R_4 10
Please the cap near pin 17 (AUXIN).

+3.3V_CARDAUX C645 0.1U/10V/X5R_4
Please the cap near pin 15 (AUXOUT).

+3.3V_CARD C610 0.1U/10V/X5R_4
Please the cap near pin 3 & 5 (3.3VOUT).

+1.5V_CARD C643 0.1U/10V/X5R_4
Please the cap near pin 11 & 13(1.5VOUT).

+1.5V_CARD C661 0.1U/10V/X5R_4 C664 0.1U/10V/X5R_4
Please the cap near connector.

+3.3V_CARD C648 0.1U/10V/X5R_4 C647 0.1U/10V/X5R_4 C646 10U/6.3V/X5R_6
Please the cap near connector.

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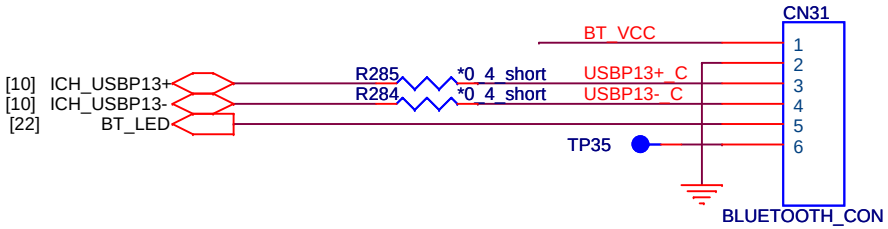
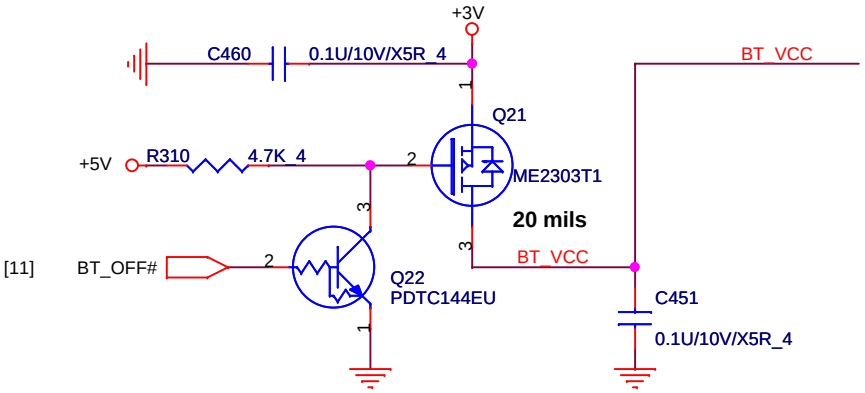
Size	Document Number	Rev
Custom	Express Card	1C
Date: Tuesday, October 20, 2009	Sheet 33 of 47	

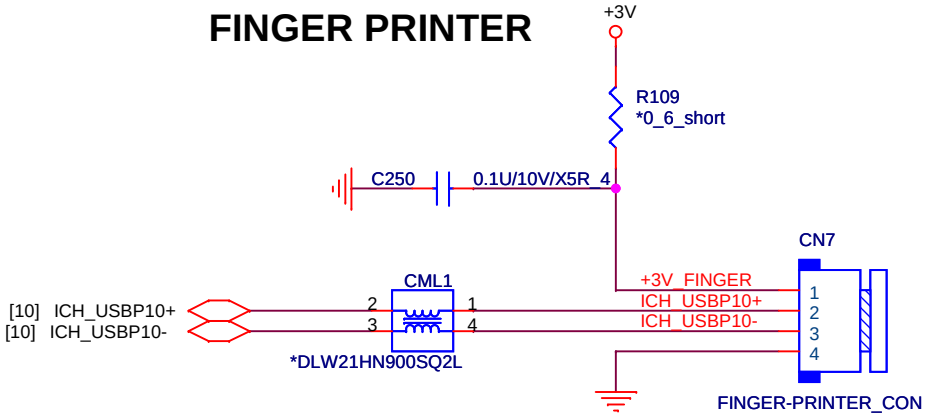
[3,4,6,8,9,10,11,12,14,15,16,18,19,22,23,24,26,27,28,29,30,31,32,33,35,37,40,42,43,44,45,46] +3V
[12,22,23,24,26,28,35,36,37,38,40,42] +5V
[33,35,40,47] 3VSUS

BLUETOOTH

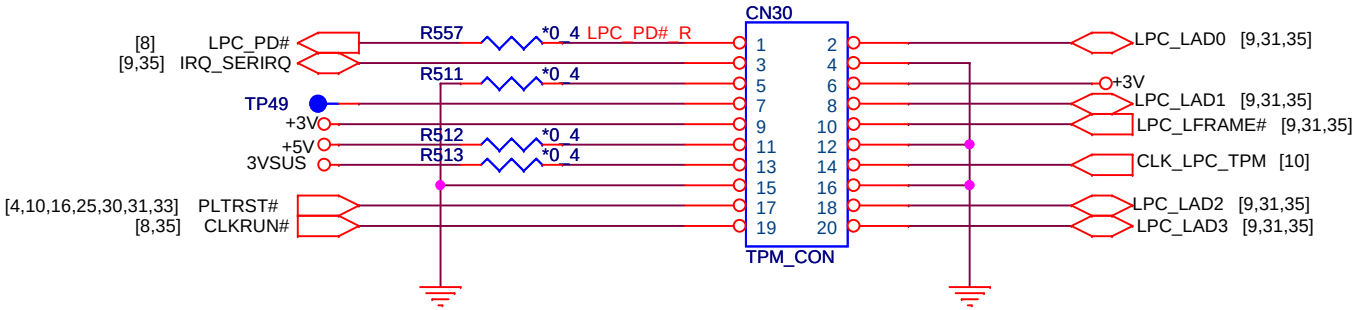




FINGER PRINTER



TPM



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/FP/TPM	1C
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IT8502E

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

TMKBC Function	
High	Enable
Low	Disable

R298	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

(For PLL Power)

DIS =>R169
UMA=>R168

C stage

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

EMI suggestion:
Add a 15p bypass CAP on CLK_PCI_8512

RF ON/OFF SWITCH

POWER SWITCH/ NOVO BUTTON

16Mbit (2M Byte), SPI

Winbond	AKE38ZP0N00
SST	AKE28FP0K07
MX	AKE37FP0Z13

Width = 6mils Spacing = 10 mils

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Quanta Computer Inc.	
Size: Custom	Document Number: KBC IT8502E
Rev: 1C	
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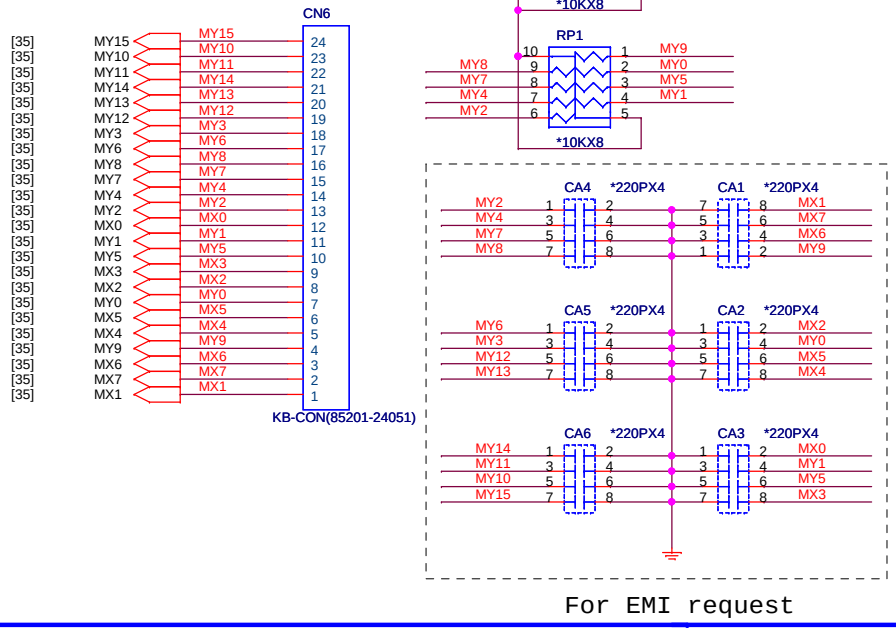
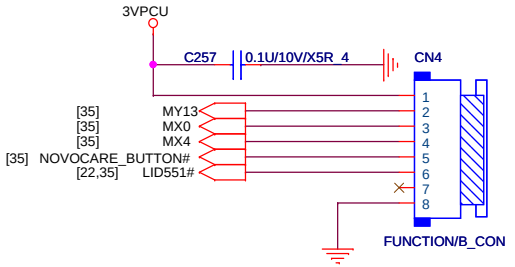
[9,22,25,28,35,37,39,40,42,44,45,47] 3VPCU
[12,22,23,24,26,28,34,35,37,38,40,42] +5V
[3,4,6,8,9,10,11,12,14,15,16,18,19,22,23,24,26,27,28,29,30,31,32,33,34,35,37,40,42,43,44,45,46] +3V

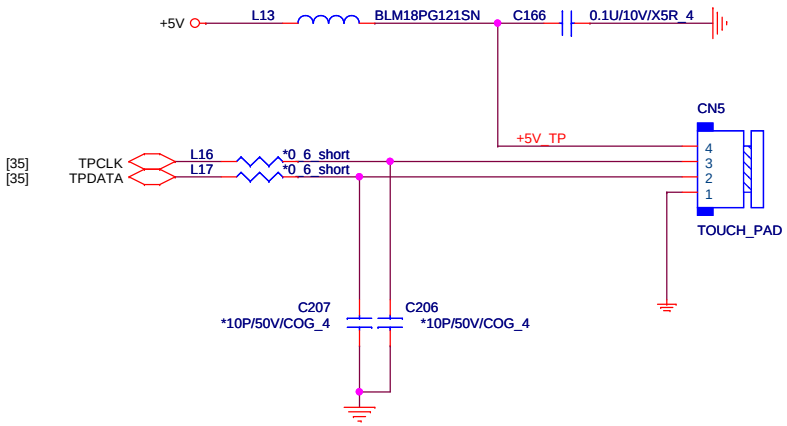
KEYBOARD



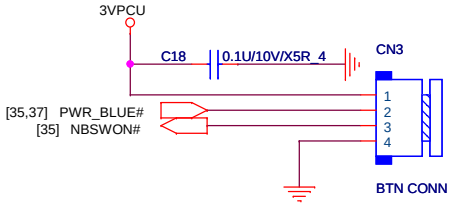
FUNCTION BUTTON BOARD



TOUCH PAD



POWER BUTTON BOARD



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Custom	KB/TP/PW-B/FN-B	1C
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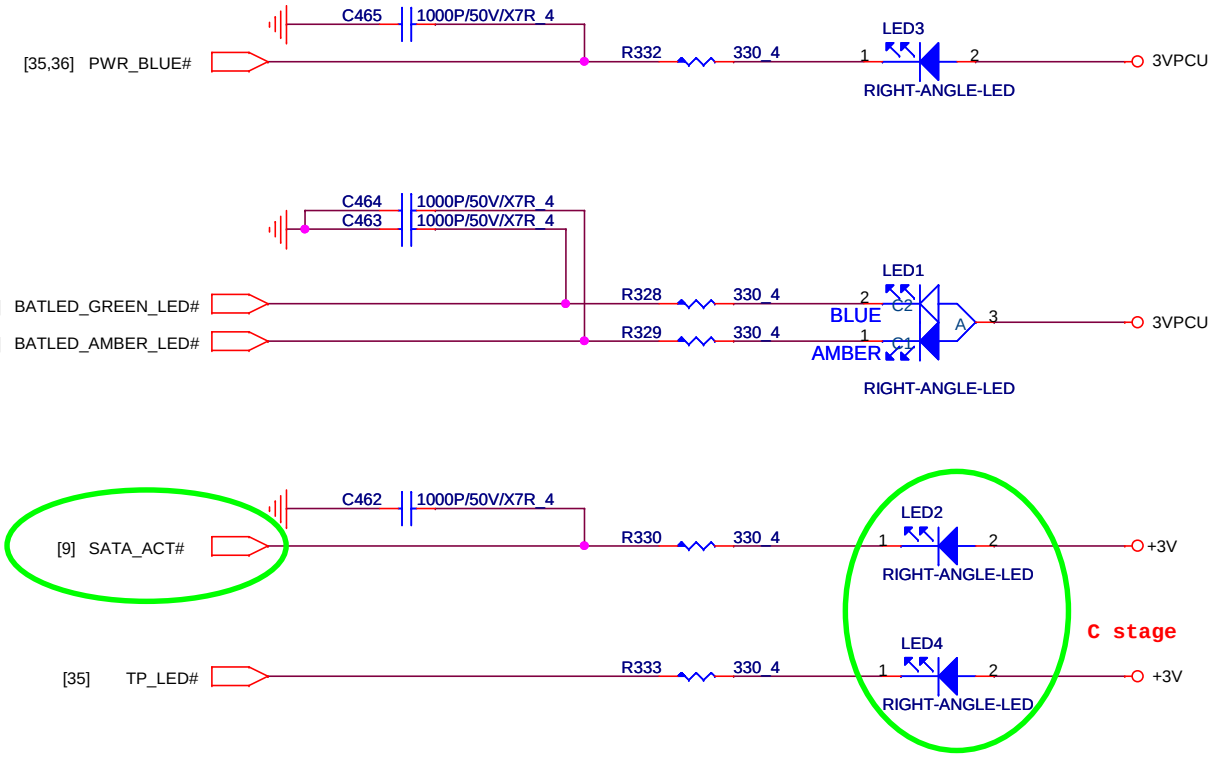
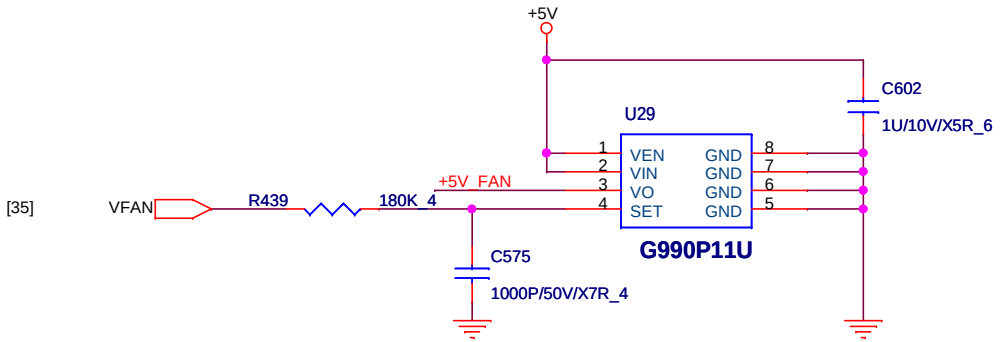
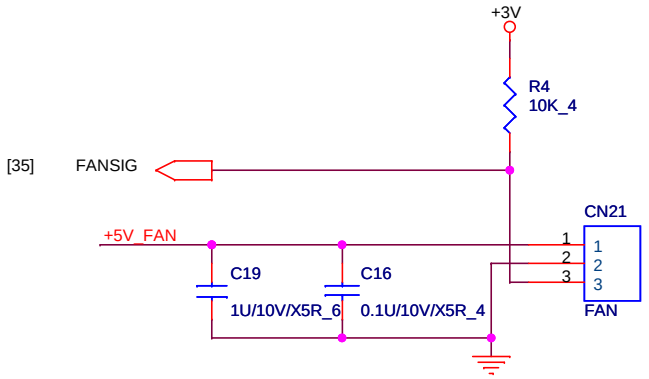
LED

[3,4,6,8,9,10,11,12,14,15,16,18,19,22,23,24,26,27,28,29,30,31,32,33,34,35,40,42,43,44,45,46] +3V
[12,22,23,24,26,28,34,35,36,38,40,42] +5V



FAN CONTROL





PROJECT : LL3A
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Size	Document Number	Rev
Custom	LED/FAN	1C
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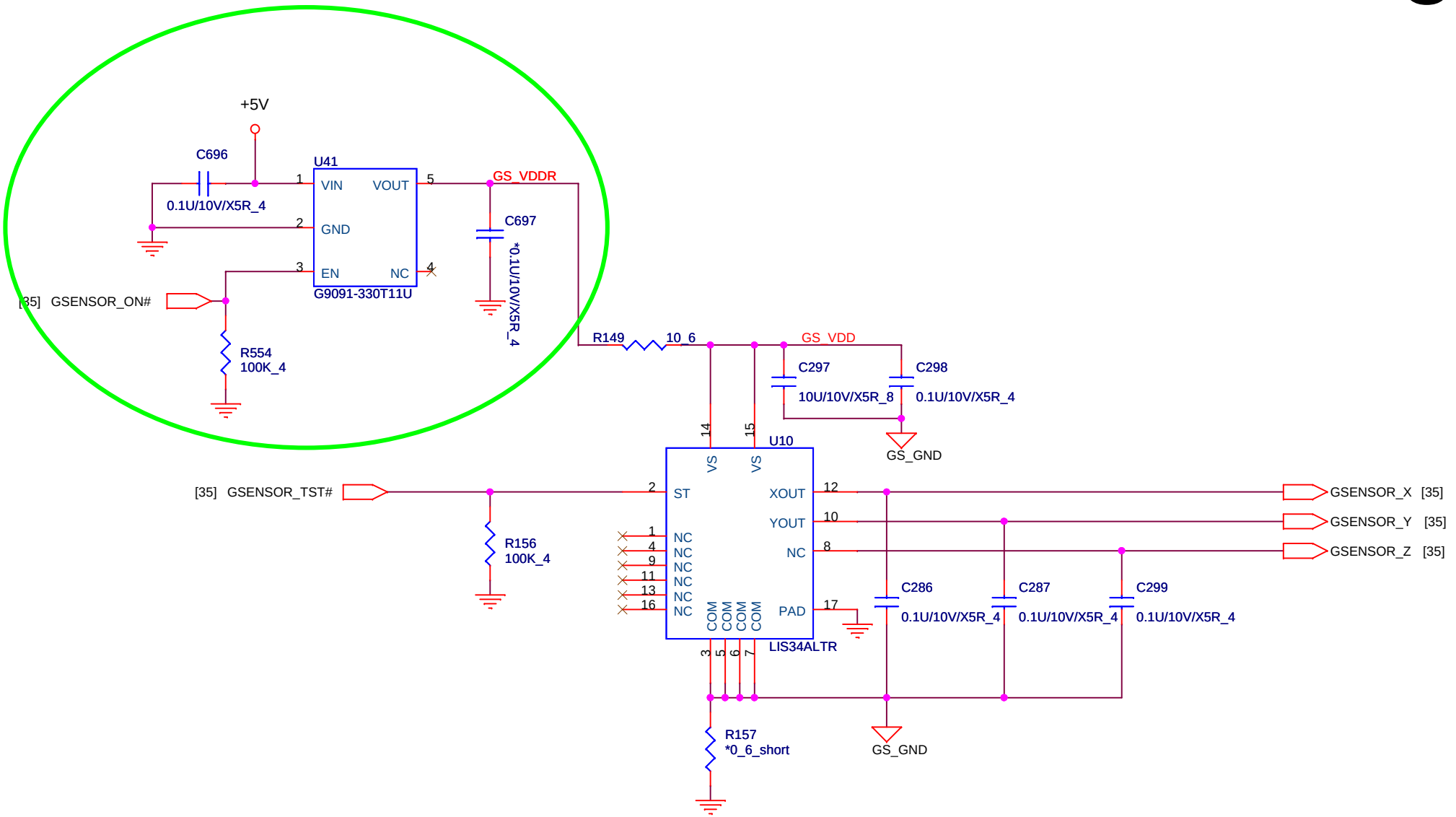
G-SENSOR (3-Axial)

[3,4,6,8,9,10,11,12,14,15,16,18,19,22,23,24,26,27,28,29,30,31,32,33,34,35,37,40,42,43,44,45,46] +3V
[22,28,40,43,45] +15V



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	G-SENSOR	1C
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Hole for CPU support

HOLE8 *H-C142D142N
HOLE5 *H-C142D142N
HOLE7 *H-C142D142N

Hole for CPU Nut

HOLE4 H-TC216BC152D142NP2

VGA nut

HOLE21 H-TC238BC134D134P2
HOLE23 H-TC238BC134D134P2

MINI CARD nut (SSD)

HOLE14 H-C216D142P2
HOLE15 H-C216D142P2

MINI CARD nut (WLAN)

HOLE32 h-tc256bc157d157p2
HOLE25 h-tc256bc157d157p2

MINI CARD nut (WWAN)

HOLE24 h-tc256bc157d157p2
HOLE31 h-tc256bc157d157p2

Hole for PCH Thermal

HOLE28 H-TC236BC134D134P2
HOLE33 H-TC236BC134D134P2

Drink Hole

HOLE11 *H-C336D220P2
HOLE10 *H-C336D220P2

HOLE20 *H-C276D106P2
HOLE9 *H-C276D106P2
HOLE3 *H-C276D106P2
HOLE1 *H-C276D106P2
HOLE6 *H-C276D106P2
HOLE19 *H-C276D106P2
HOLE18 *H-C276D106P2
HOLE13 *O-K46-1
HOLE17 *H-C87D87N
HOLE2 *H-C87D87N
HOLE34 *SPAD-RE1110X350
HOLE22 *SPAD-RE240X330
HOLE35 *SPAD-RE80X200
HOLE36 *SPAD-RE80X200

VIN C7 0.1U/25V/X5R_4
VIN C119 *0.1U/25V/X5R_4
VIN C98 *0.1U/25V/X5R_4
VIN C252 *0.1U/25V/X5R_4
VIN C483 *0.1U/25V/X5R_4
5VSUS C8 *0.1U/10V/X5R_4
5VSUS C469 *0.1U/10V/X5R_4
+1.8V C358 *0.1U/10V/X5R_4
VBATT_A C1 0.1U/25V/X5R_4
VBATT_B C100 0.1U/25V/X5R_4
BAT-V C700 0.1U/25V/X5R_4

3VPCU C701 2200P/50V/X7R_4
+1.5V C702 2200P/50V/X7R_4
+VCC_GFX_CORE C703 2200P/50V/X7R_4
+VCC_GFX_CORE C704 2200P/50V/X7R_4
+VCC_GFX_CORE C705 2200P/50V/X7R_4
+VCC_GFX_CORE C706 2200P/50V/X7R_4
+VCC_GFX_CORE C707 2200P/50V/X7R_4

EMI request

Hole for TPM Module

HOLE29 H-TC216BC58D58P2
HOLE26 H-TC216BC58D58P2
HOLE30 H-TC216BC58D58P2
HOLE27 H-TC216BC58D58P2

PAD1 *Spad-re468x1426np

PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HOLD & SKEW	1C
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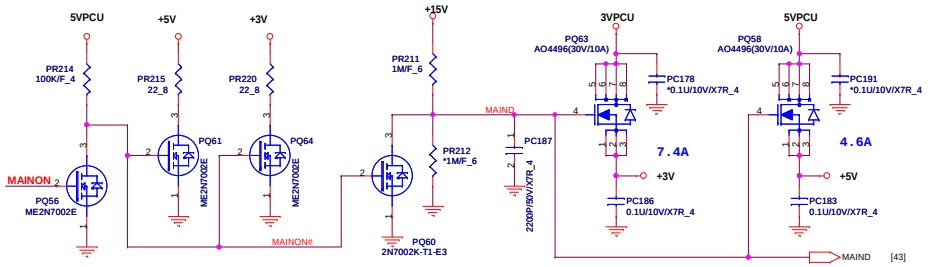
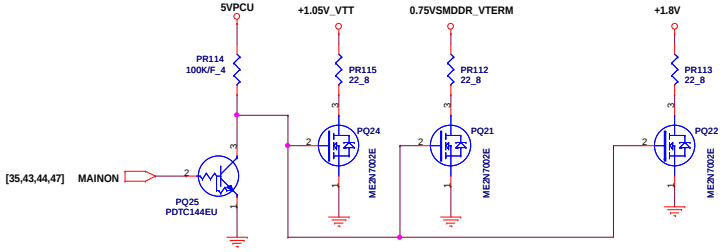
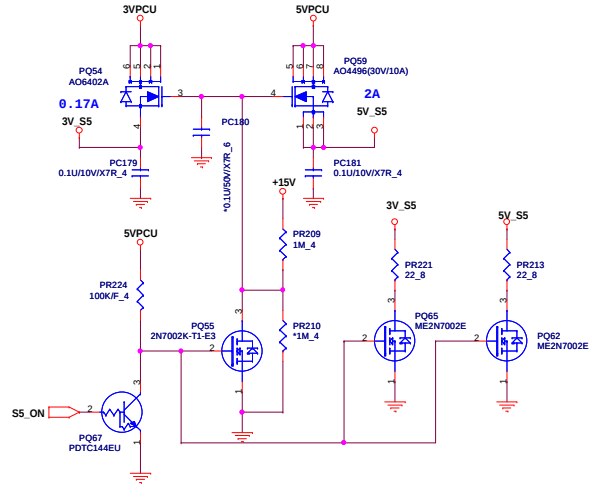
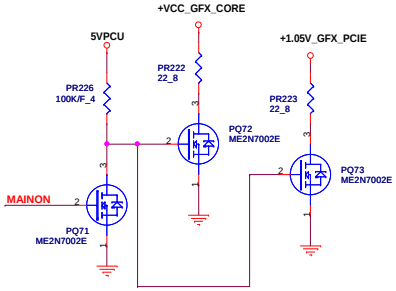
+3V, +5V



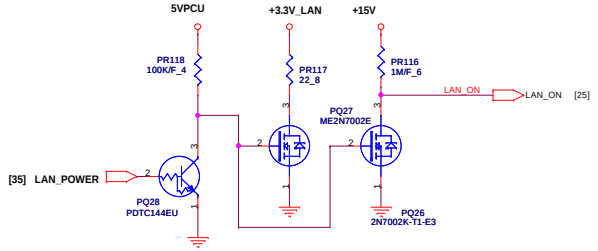


3V_S5, 5V_S5

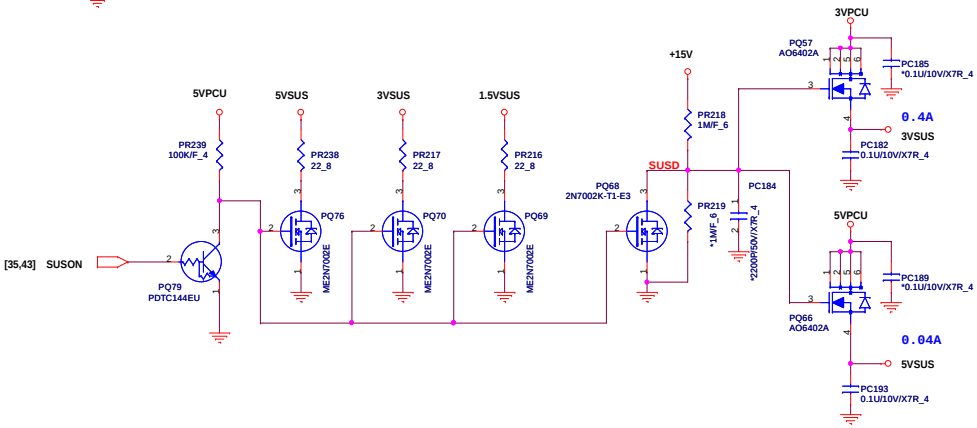


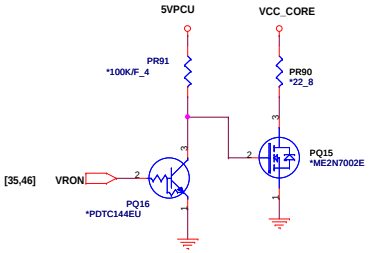


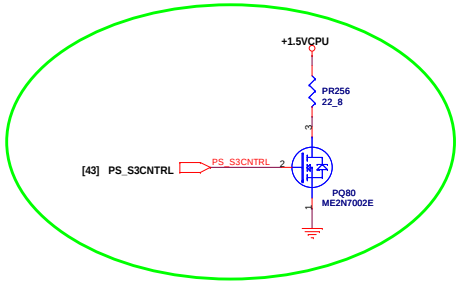
LANVCC



3VSUS, 5VSUS







PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge	1C
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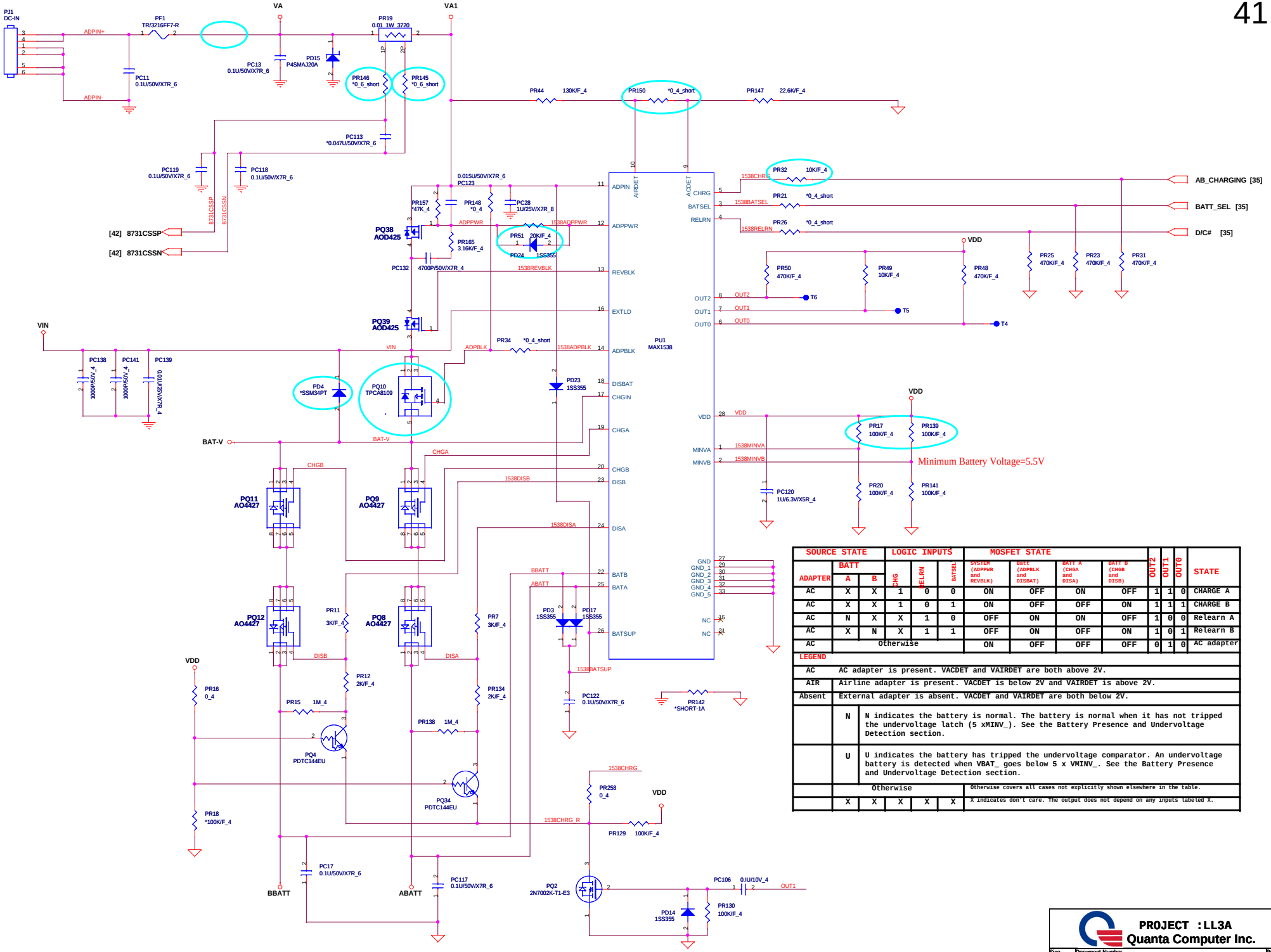

SOURCE STATE			LOGIC INPUTS			MOSFET STATE							
	BATT												
ADAPTER	A	B	CHG	DELRN	BATSEL	SYSTEM (ADPPWR and REVBLK)	Batt (ADPBLK and DISBAT)	BATT A (CHGA and DISA)	BATT B (CHGB and DISB)	OUT2	OUT1	OUT0	STATE
AC	X	X	1	0	0	ON	OFF	ON	OFF	1	1	0	CHARGE A
AC	X	X	1	0	1	ON	OFF	OFF	ON	1	1	1	CHARGE B
AC	N	X	X	1	0	OFF	ON	ON	OFF	1	0	0	Relearn A
AC	X	N	X	1	1	OFF	ON	OFF	ON	1	0	1	Relearn B
AC	Otherwise					ON	OFF	OFF	OFF	0	1	0	AC adapter

LEGEND		
AC	AC adapter is present. VACDET and VAIRDET are both above 2V.	
AIR	Airline adapter is present. VACDET is below 2V and VAIRDET is above 2V.	
Absent	External adapter is absent. VACDET and VAIRDET are both below 2V.	
	N	N indicates the battery is normal. The battery is normal when it has not tripped the undervoltage latch (5 xMINV_). See the Battery Presence and Undervoltage Detection section.
	U	U indicates the battery has tripped the undervoltage comparator. An undervoltage battery is detected when VBAT_ goes below 5 x VMINV_. See the Battery Presence and Undervoltage Detection section.
	Otherwise	Otherwise covers all cases not explicitly shown elsewhere in the table.
	X	X indicates don't care. The output does not depend on any inputs labeled X.

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Size	Document Number	Rev
C	Battery Selector (MAX1538)	1C
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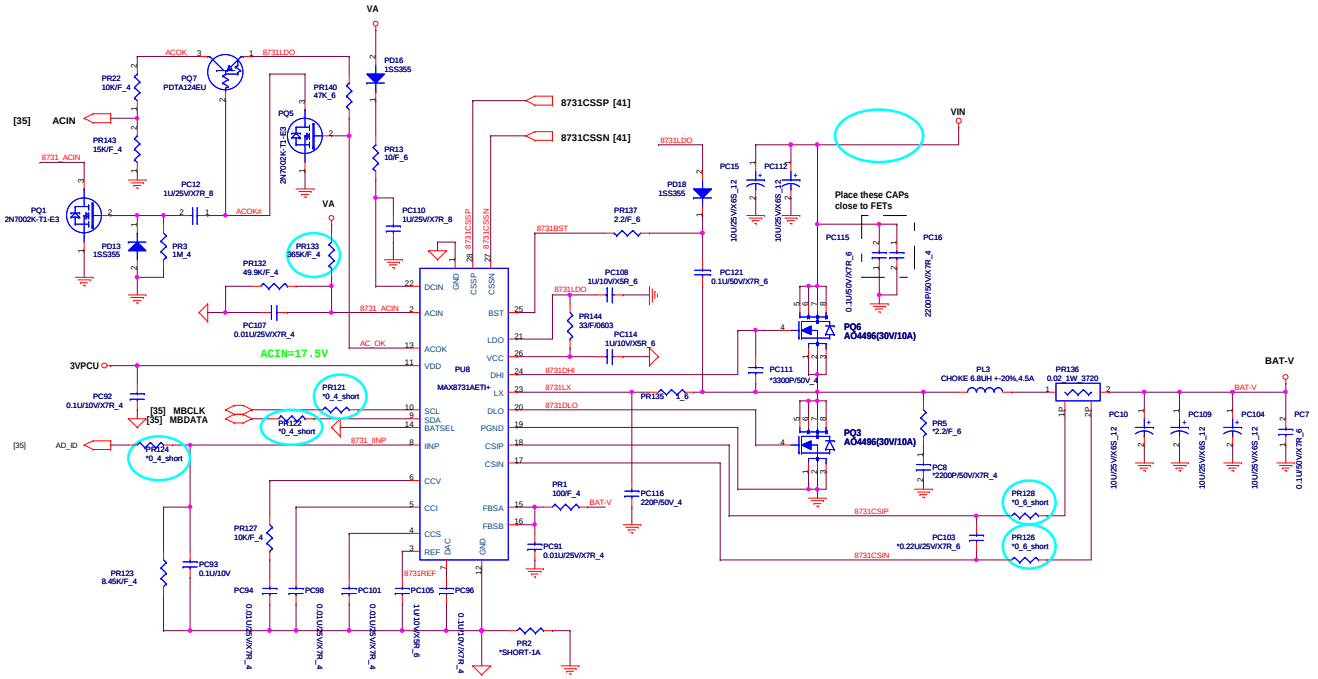

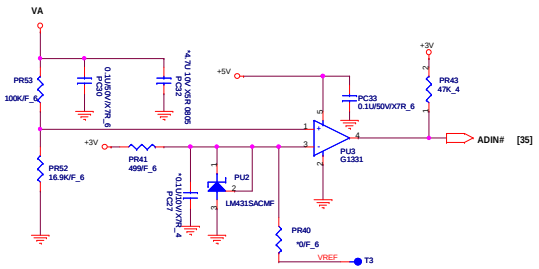

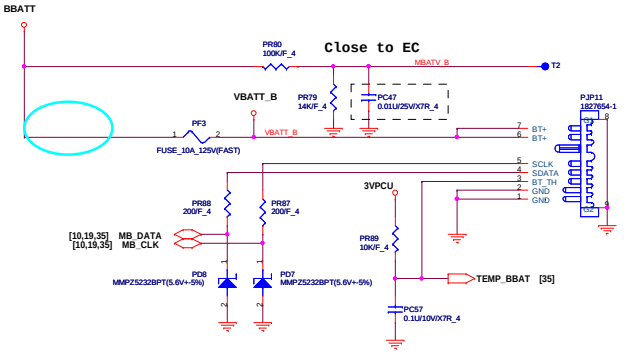

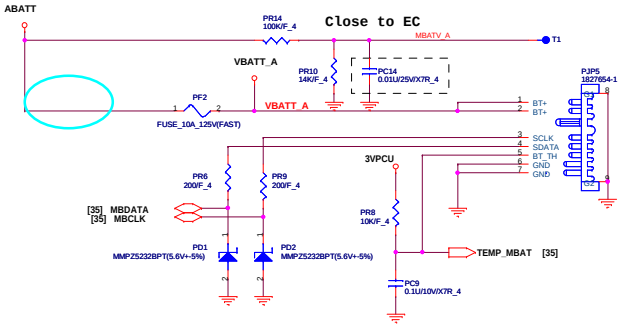

PROJECT : LL3A Quanta Computer Inc.		
Size: Custom	Document Number: Charger(MAX8731)	Rev: 1C
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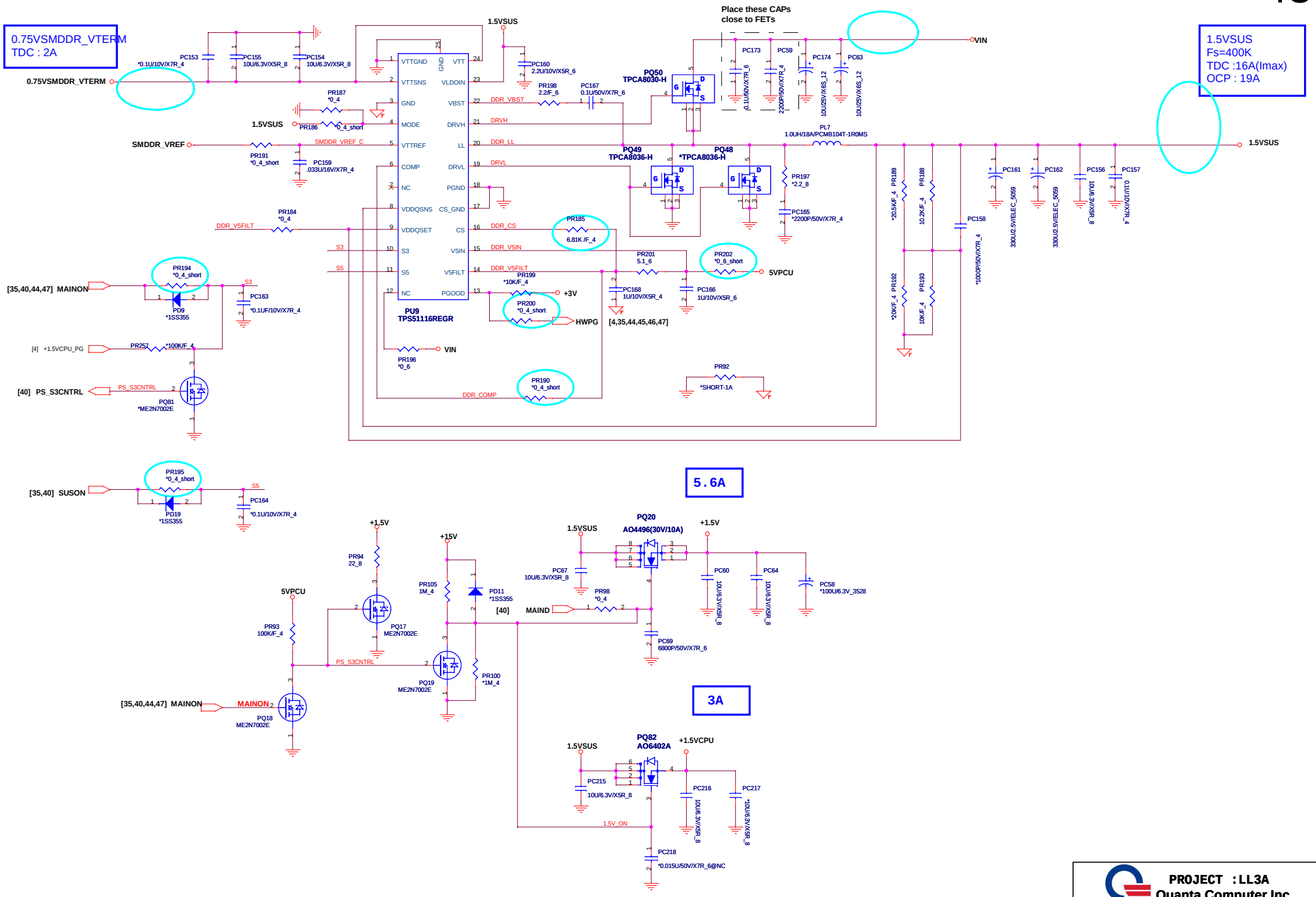
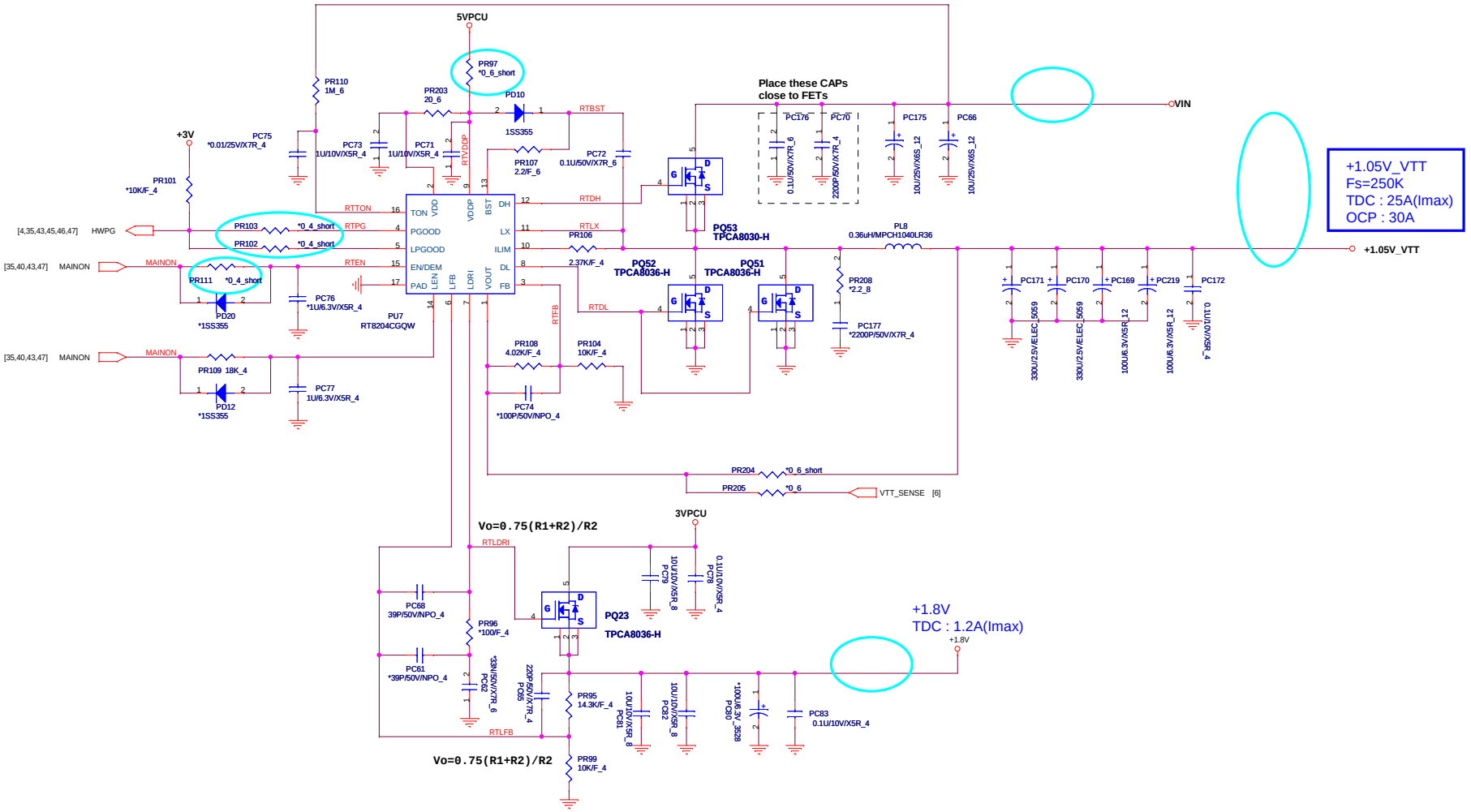

0.75VSMDDR_VTERM
TDC : 2A
1.5VSUS
Fs=400K
TDC :16A(Imax)
OCP : 19A
Place these CAPs close to FETs
PU9 TPS51116REGR
PQ50 TPCA8030-H
PQ49 TPCA8036-H
PQ48 *TPCA8036-H
PL7 1.0UH/18A/PCMB104T-1R0MS
PQ20 AO4496(30V/10A)
PQ82 AO6402A
PQ17 ME2N7002E
PQ18 ME2N7002E
PQ19 ME2N7002E
PQ81 *ME2N7002E
PD9 *1SS355
PD19 *1SS355
PD11 *1SS355
5.6A
3A
PROJECT : LL3A
Quanta Computer Inc.
DDR3/0.75VSMDDR (TPS51116REGR)
Tuesday, October 20, 2009



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Size: Custom	Document Number: 1.05V_VTT(RT8204) / 1.8V	Rev: 1C
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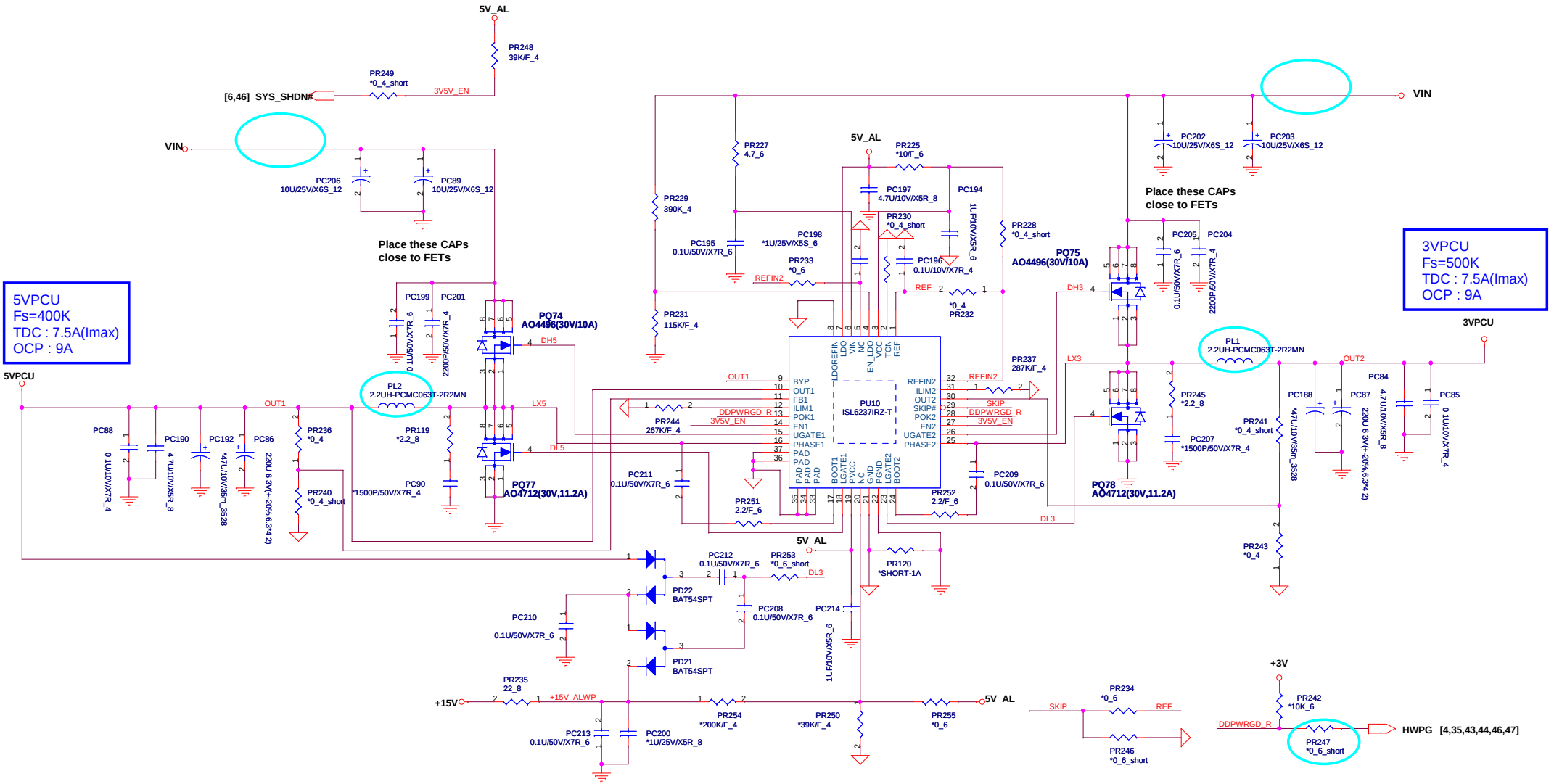
[9,22,25,28,35,36,37,39,40,42,44,47] 3VPCU
[9,28,40,43,44,47] 5VPCU
[22,28,40,43] +15V
[22,39,41,42,43,44,46,47] VIN



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Quanta Computer Inc.			
Size: Custom	Document Number: 3V/5V (ISL6237IRZ-T)		Rev: 1C
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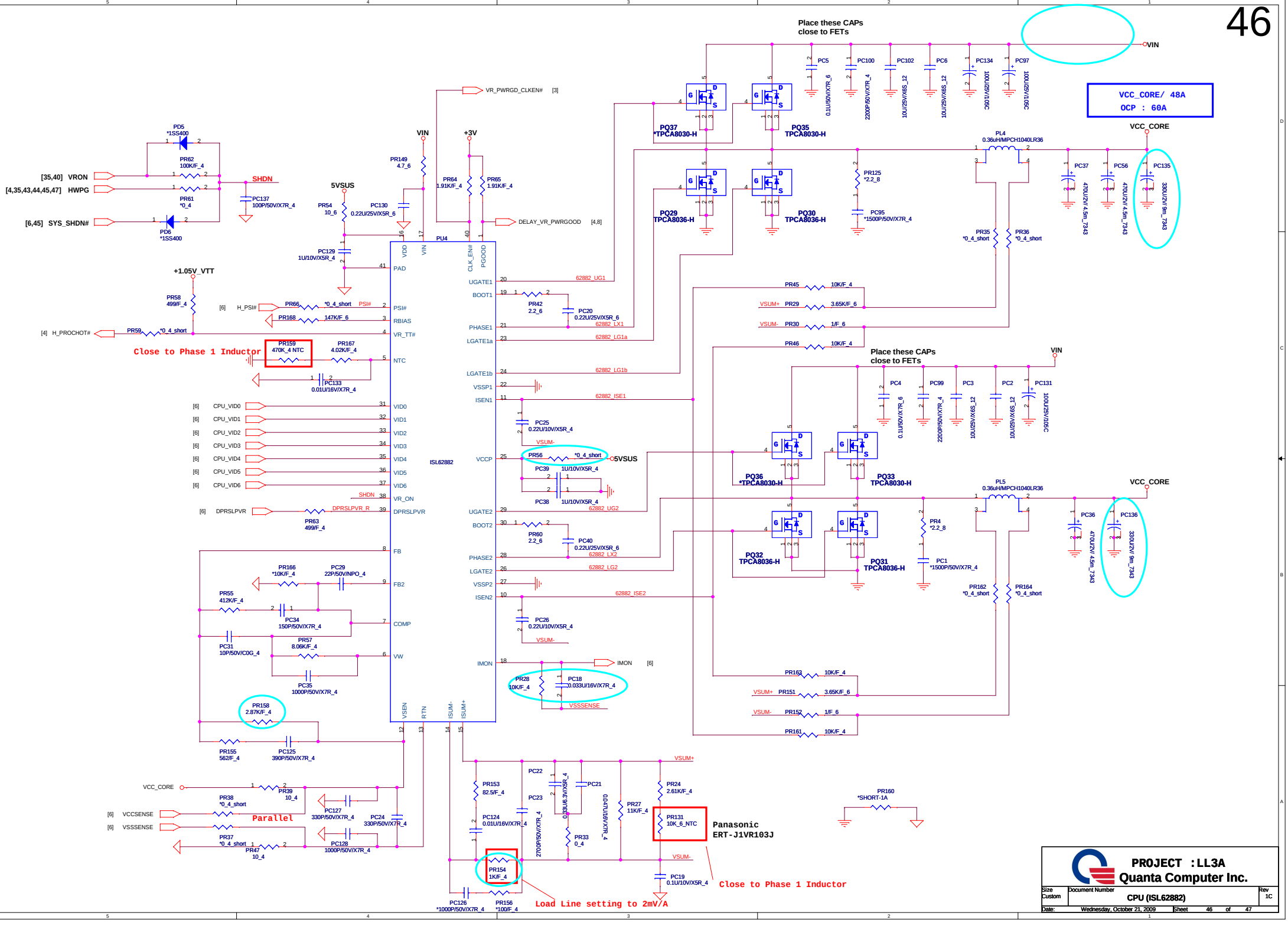

PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU (ISL62882)	1C
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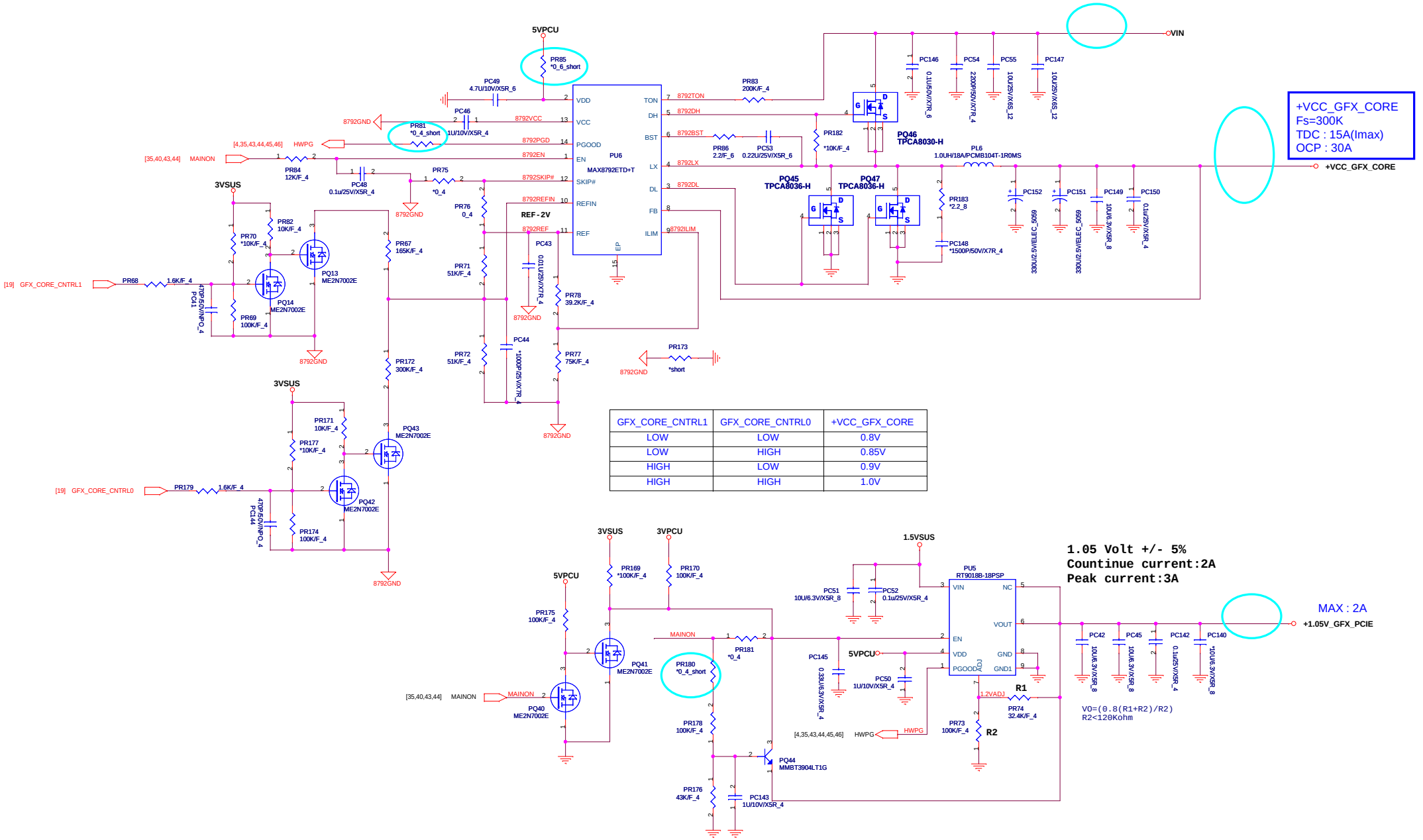
For Descrete N10M VGA Only



GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VCC_GFX_CORE
LOW	LOW	0.8V
LOW	HIGH	0.85V
HIGH	LOW	0.9V
HIGH	HIGH	1.0V

PROJECT : LL3A Quanta Computer Inc.		
Size: Custom	Document Number: DIS_GFX_VCC (MAX8792)	Rev: 1C
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