Wistron Confidential

PV

2009/10/19 REV :PV-01

<Variant Name>

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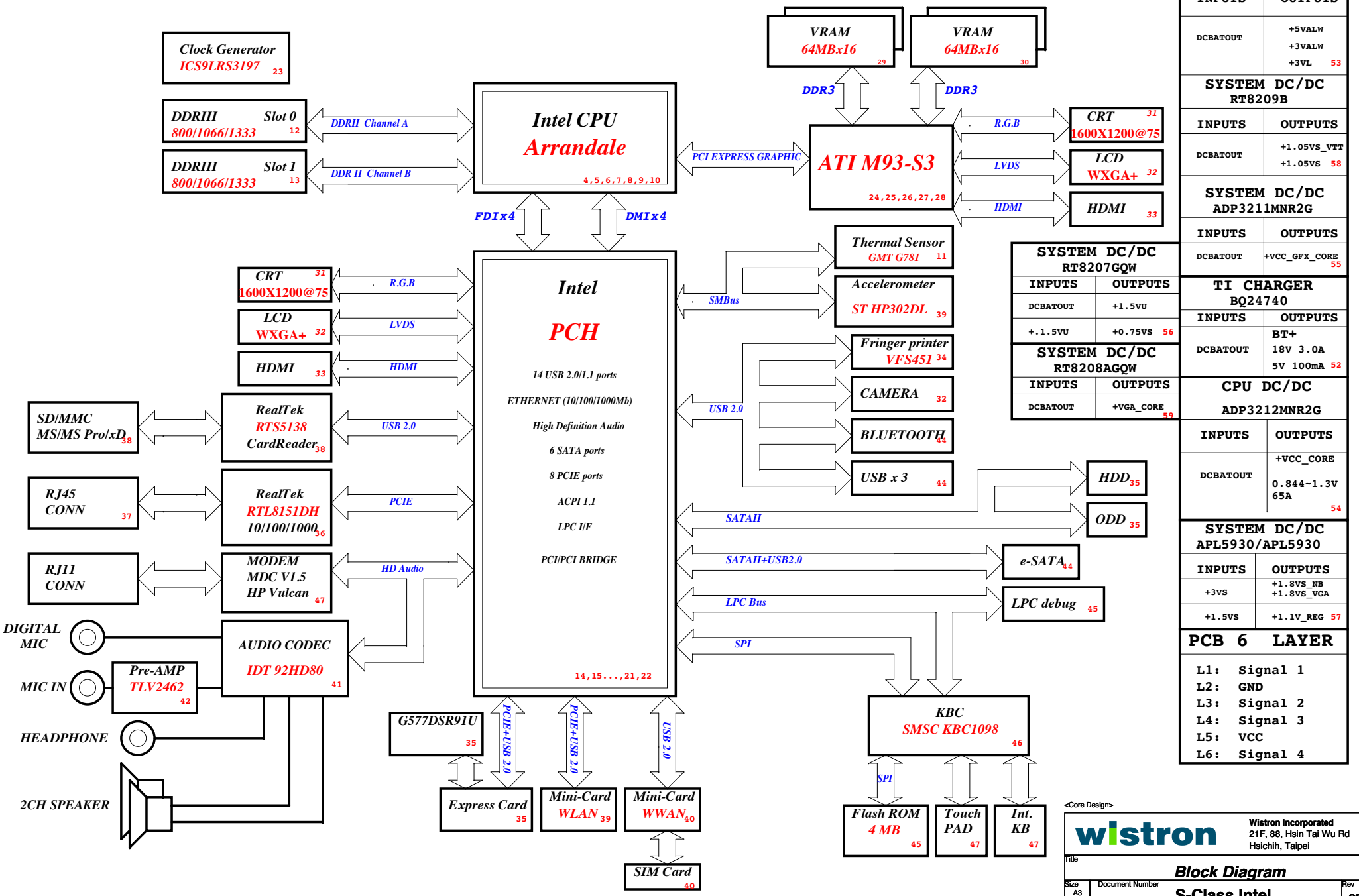
Title: S-Class Intel

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 1 of 62

Intel Calpella Arrandale Block Diagram



SYSTEM DC/DC RT8205A	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +3VALW +3VL 53

SYSTEM DC/DC RT8209B	
INPUTS	OUTPUTS
DCBATOUT	+1.05VS_VTT +1.05VS 58

SYSTEM DC/DC ADP3211MNR2G	
INPUTS	OUTPUTS
DCBATOUT	+VCC_GFX_CORE 55

SYSTEM DC/DC RT8207GQW	
INPUTS	OUTPUTS
DCBATOUT	+1.5VU
+.1.5VU	+0.75VS 56

SYSTEM DC/DC RT8208AGQW	
INPUTS	OUTPUTS
DCBATOUT	+VGA_CORE 59

TI CHARGER BQ24740	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA 52

CPU DC/DC ADP3212MNR2G	
INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 0.844-1.3V 65A 54

SYSTEM DC/DC APL5930/APL5930	
INPUTS	OUTPUTS
+3VS	+1.8VS_NB +1.8VS_VGA
+1.5VS	+1.1V_REG 57

PCB 6 LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

<Core Design>

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Title: **Block Diagram**

Size: A3 | Document Number: **S-Class Intel** | Rev: SD

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PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing page 15

LANE2	EXP
LANE4	WLAN
LANE6	LAN

USB Table page 18

Pair	Device
0	External USB2
1	USB1 (Debug port)
2	ESATA USB4
3	Card Reader
4	NEW CARD
5	FREE
6	WLAN
7	FREE
8	BLUETOOTH
9	WWAN
10	Fingerprint
11	External USB3
12	CAMERA
13	FREE

091019-1

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

090901-1

SMBUS Control Table

	SOURCE	BATT	THERMAL SENSOR	CLK GEN	SODIMM	G-SENSOR	SMSC1098	M93
AB1A_DATA AB1A_CLK	SMSC1098	V	X	X	X	X	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	V	V
PCH_SMB_DATA PCH_SMB_CLK	Calpella	X	V	V	V	V	X	X

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Title: Notes List

Size: A3 | Document Number: S-Class Intel | Rev: SD

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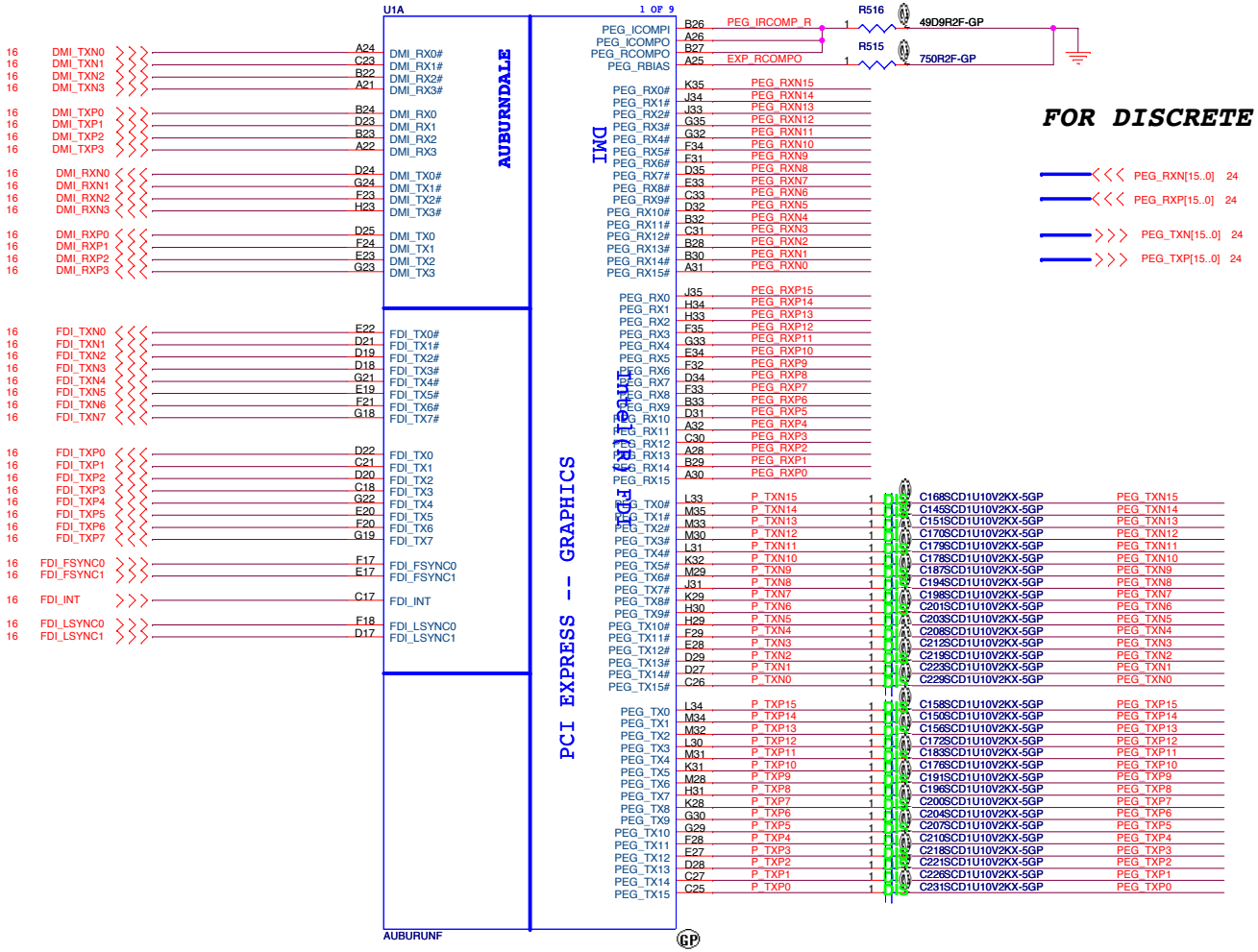
CPU(1/7)



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Title: CPU (1/7)-PEG / DMI / FDI

Size: A3 | Document Number: S-Class Intel | Rev: SD

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CPU(2/7)

5

Processor Pullups

+1.05VS_VTT
R157 1 49D9R2F-GP H_CATERR#
R171 1 DY 68R2-GP H_CPURST#_R

Processor Compensation Signals

R460 1 20R2F-GP H_COMP3
R462 1 20R2F-GP H_COMP2
R501 1 49D9R2F-GP H_COMP1
R463 1 49D9R2F-GP H_COMP0
TP60 TPAD14-GP 1 SKTOCC#_R

U1B 2 OF 9

COMP3	AT23
COMP2	AT24
COMP1	G16
COMP0	AT26
SKTOCC#	AH24
CATERR#	AK14
PECI	AT15
PROCHOT#	AN26
THERMTRIP#	AK15
RESET_OBS#	AP26
PM_SYNC	AL15
VCCPWRGOOD_1	AN14
VCCPWRGOOD_0	AN27
SM_DRAMPWROK	AK13
VTTPWRGOOD	AM15
TAPPWRGOOD	AM26
RSTIN#	AL14
AUBURUNF	

H_CATERR# AK14
19 H_PECI AT15 — R379 1 68R2-GP +1.05VS_VTT
11,54 H_PROCHOT# AN26
11,19,25 H_THRMTRIP-A# AK15
H_CPURST# — R176 1 0R0402-PAD-1-GP 2 H_CPURST#_R AP26
16 H_PM_SYNC AL15
19 H_PWRGD — R121 1 0R0402-PAD-1-GP 2 VCCPWRGOOD AN14
VCCP_1.5VSPWRGD 49 — R117 1 0R0402-PAD-1-GP 2 VCCPWRGOOD_0 AN27
R128 1K5R2F-2-GP
16 PM_DRAM_PWRGD — R130 1 0R0402-PAD-1-GP 2 VDDPWRGOOD_R AK13
49 H_VTTPWRGD AM15
H_PWRGD_XDP AM26
VDDPWRGOOD_R
R124 750R2F-GP
18,26,35,36,39,45 PLT_RST# — R127 1K5R2F-2-GP PLT_RST#_R AL14
R129 750R2F-GP

AUBURN CLOCKS

BCLK BCLK#	A16 B16	BCLK_CPU_P_R BCLK_CPU_N_R	RN62 SRN0J-10-GP-U
BCLK_ITP BCLK_ITP#	AR30 AT30	BCLK_ITP_P_R BCLK_ITP_N_R	RN4 SRN0J-10-GP-U
PEG_CLK PEG_CLK#	E16 D16	PEG_CLK_R PEG_CLK#_R	RN60 SRN0J-10-GP-U
DPLL_REF_SSCLK DPLL_REF_SSCLK#	A18 A17	DPLL_REF_SSCLK_R DPLL_REF_SSCLK#_R	RN61 SRN0J-10-GP-U

BCLK_CPU_P_R 19 / BCLK_CPU_N_R 19
CLK_CPU_XDP / CLK_CPU_XDP#
CLK_EXP_P 15 / CLK_EXP_N 15
CLK_DP_P 15 / CLK_DP_N 15

THERMAL DDR3 MISC

SM_DRAMRST# F6 DDR3_DRAMRST#_R
SM_RCOMP0 AL1 SM_RCOMP_0
SM_RCOMP1 AM1 SM_RCOMP_1
SM_RCOMP2 AN1 SM_RCOMP_2
RN54 SRN10KJ-5-GP +1.05VS_VTT
PM_EXT_TS0# AN15 — PM_EXTTS#0_R 12
PM_EXT_TS1# AP15 — PM_EXTTS#1_R 13
R105 12K4R2F-GP DY
R108 12K4R2F-GP DY

PWR MANAGEMENT

PRDY#	AT28	XDP_PRDY#
PREQ#	AP27	XDP_PREQ#
TCK	AN28	XDP_TCK
TMS	AP28	XDP_TMS
TRST#	AT27	XDP_TRST#
TDI	AT29	XDP_TDI
TDO	AR27	XDP_TDO
TDI_M	AR29	XDP_TDI_TDO_M
TDO_M	AP29	XDP_TDI_TDO_M_R — R461 1 2 0R0402-PAD-1-GP
DBR#	AN25	XDP_DBRESET#

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BPM0#	AJ22	XDP_BPM#0		
BPM1#	AK22	XDP_BPM#1		
BPM2#	AK24	XDP_BPM#2		
BPM3#	AJ24	XDP_BPM#3		
BPM4#	AJ25	XDP_BPM#4_R	R168	XDP_BPM#4
BPM5#	AH22	XDP_BPM#5_R	R158	XDP_BPM#5
BPM6#	AK23	XDP_BPM#6_R	R150	XDP_BPM#6
BPM7#	AH23	XDP_BPM#7_R	R145	XDP_BPM#7

(all 0R0402-PAD-1-GP)

DDR3 Compensation Signals

SM_RCOMP_0 — R136 100R2F-L1-GP-U
SM_RCOMP_1 — R135 24D9R2F-L-GP
SM_RCOMP_2 — R134 130R2F-1-GP

R252 DX 0R2J-2-GP — Q17 BSS138-7F-GP — R257 1KR2J-1-GP +1.5VU
DDR3_DRAMRST# 12,13
R253 100KR2J-1-GP
090813-1-SI
091019-1
R771 0R0402-PAD-1-GP PCH_DDR_RST 19
C978 SC470P50V2KX-3GP

XDP_TMS — R132 DX 51R2J-2-GP +1.05VS_VTT
XDP_PREQ# — R141 DX 51R2J-2-GP

closed to XDP

XDP_TRST# — R431 51R2J-2-GP

XDP1 STC-CONN60A-GP 20.F0971.060

XDP_PREQ#	3	4	
XDP_PRDY#	5	6	
XDP_BPM#0	9	10	
XDP_BPM#1	11	12	
XDP_BPM#2	15	16	
XDP_BPM#3	17	18	
XDP_BPM#4	27	28	
XDP_BPM#5	29	30	
XDP_BPM#6	33	34	
XDP_BPM#7	35	36	
CLK_CPU_XDP	39	40	
CLK_CPU_XDP#	41	42	
XDP_RST#_R	45	46	XR4 1 DX 1KR2J-1-GP H_CPURST#
XDP_DBRESET#_R	47	48	XR2 1 DY 0R2J-2-GP XDP_DBRESET# 16
XDP_TRST#	53	54	
XDP_TDI	55	56	
XDP_TMS	57	58	
XDP_TCK	59	60	

090824-1-SI
H_PWRGD — XR1 1 DY 1KR2J-1-GP H_CPUPWRGD_R
16,45,46 PWRBTN_OUT#
+1.05VS_VTT
H_PWRGD_XDP
TPAD14-GP TP4 — XDP1_TP2
TPAD14-GP TP3 — XDP1_TP3
XDP_TCK

+1.05VS_VTT — R435 10KR2J-3-GP — +3VS
R434 51R2J-2-GP
XDP_TDO

XDP_RST#_R XR3 1 DY 0R2J-2-GP PLT_RST# 18,26,35,36,39,45

Place those AFTP at bottom side.

XDP_TDO	TP38	TPAD14-GP
XDP_TRST#	TP37	TPAD14-GP
XDP_TMS	TP40	TPAD14-GP
XDP_TDI	TP36	TPAD14-GP
XDP_TCK	TP2	TPAD14-GP

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Title: CPU (2/7)-HOST
Size: A3 | Document Number: S-Class Intel | Rev: SD
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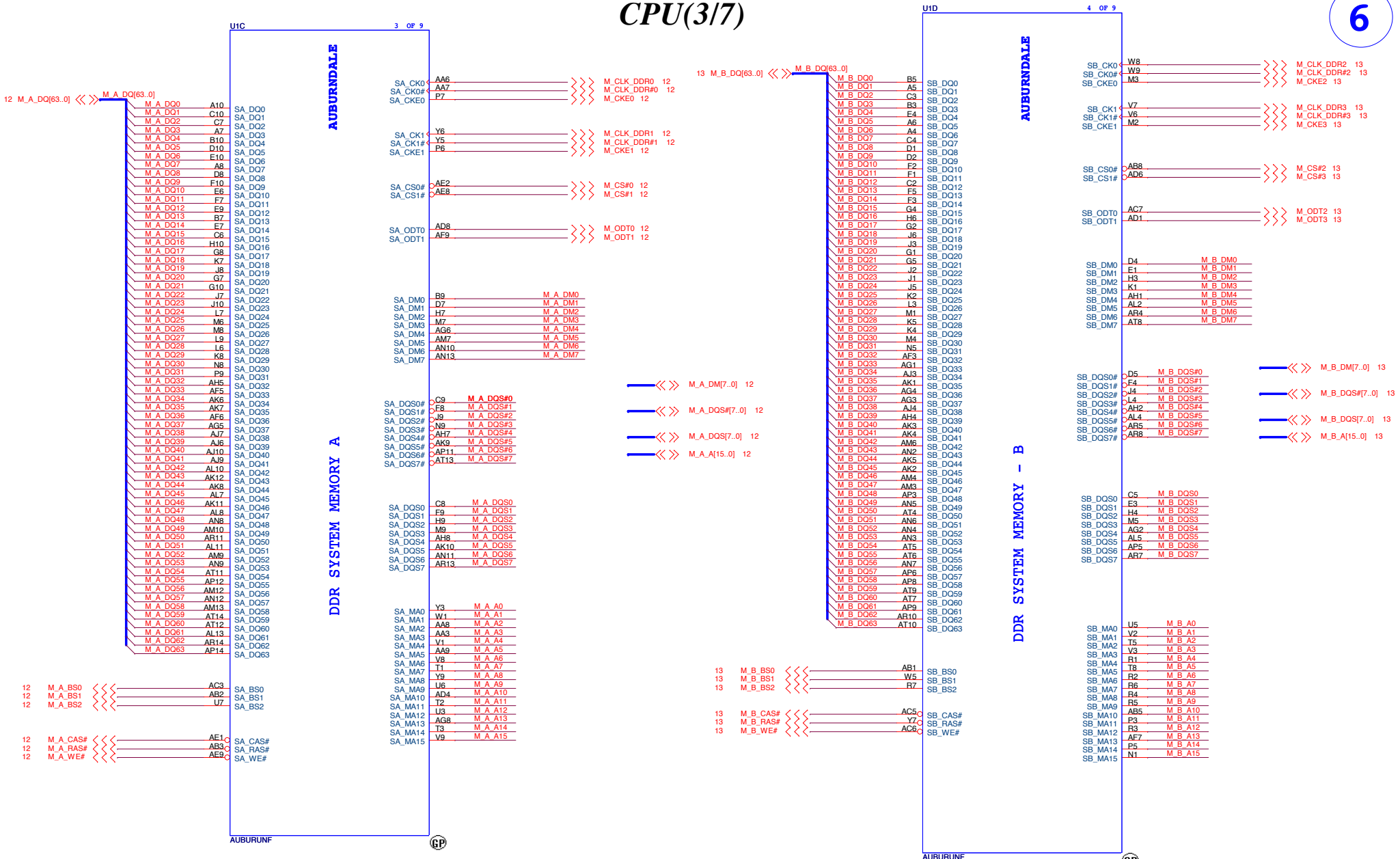
CPU(3/7)



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Title: CPU (3/7)-MEM INTERFACE

Size	Document Number	Rev
A3	S-Class Intel	SD

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CPU(4/7)

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PROCESSOR CORE POWER
40A

+VCC_CORE

091015-1

C520 C504 C107 C531 C556 C553
C495 C539 C485 C118 C121 C110
C132 C98 C104 C131 C96 C92 C130 C563
C137 C133 C558 C557 C492 C500 C511 C90

SC10U6D3V5MX-3GP
SC22U6D3V5MX-2GP
DY

U1F

AUBURNDALE

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

AUBURUNF

+1.05VS_VTT

C616 C491 C590 C555 C499 C135 C528 C93 C99
SC10U6D3V5MX-3GP

C115 C134 C119
SC22U6D3V5MX-2GP

C129 C108
SC22U6D3V5MX-2GP

+VTT_43 +VTT_44
R624 R700
0R0402-PAD-1-GP

091019-1

PSI# PSI# 54
H_VID[6..0] 54
H_VID0 H_VID1 H_VID2 H_VID3 H_VID4 H_VID5 H_VID6
PM_DPRSLPVR 54
VTT_SELECT H_VTTVID1 TP63 TPAD14-GP

H_VTTVID1 = Low, 1.1V
H_VTTVID1 = High, 1.05V

ISENSE IMVP_IMON 54
VCC_SENSE VSS_SENSE
VCC_SENSE_R VSS_SENSE_R
R178 R173
VCC_SENSE 54
VSS_SENSE 54
VTT_SENSE VSS_SENSE_VTT
VTT_SENSE 58
VSS_SENSE_VTT 58

R177 R172
100R2F-L1-GP-U

R512 R508
100R2F-L1-GP-U

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail values are
Auburndale VTT=1.05V
Clarksfield VTT=1.1V

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Title: CPU (4/7)-POWER

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CPU(5/7)

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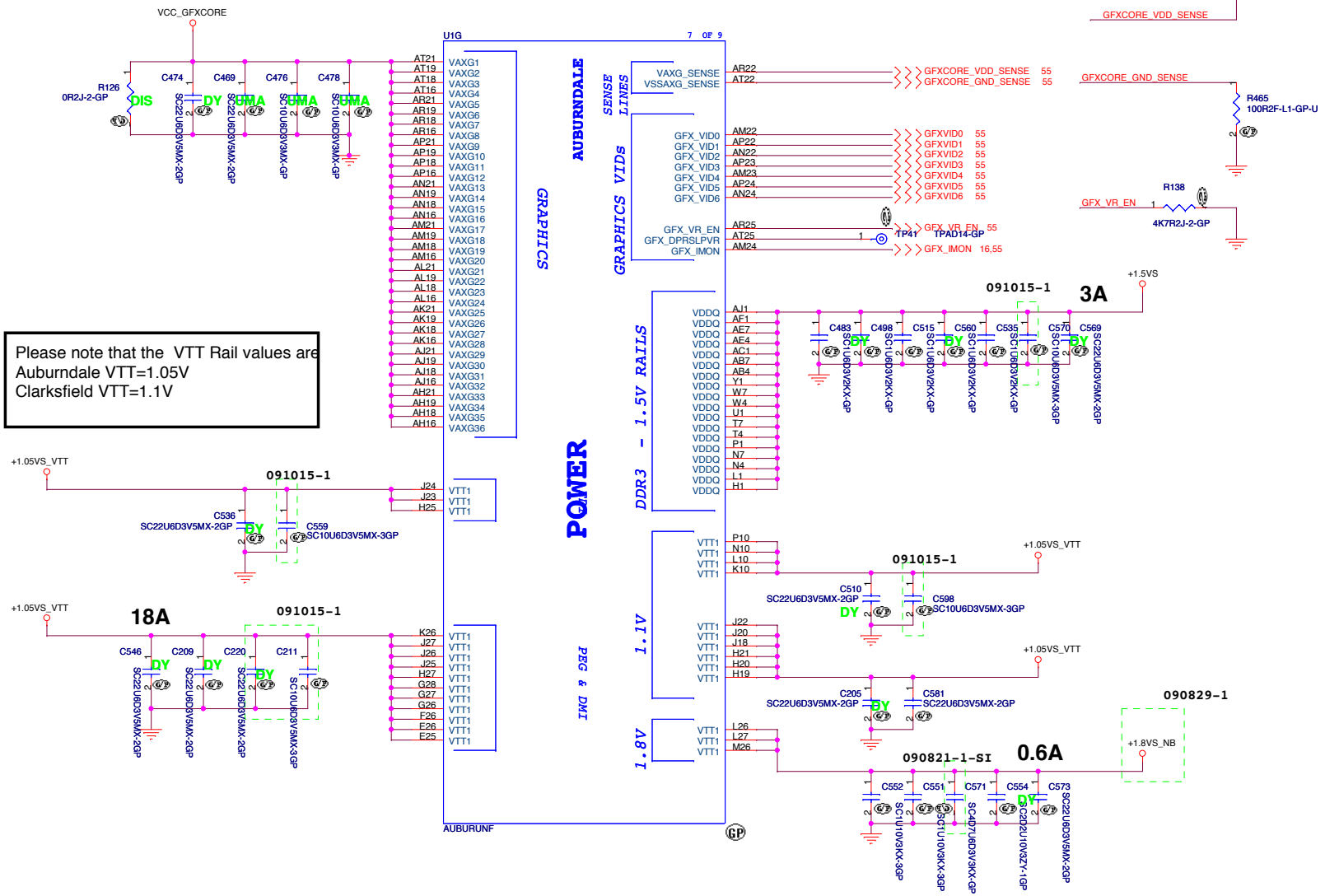
UMA 22A



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Title: CPU (5/7)-Graphic POWER

Size	Document Number	Rev
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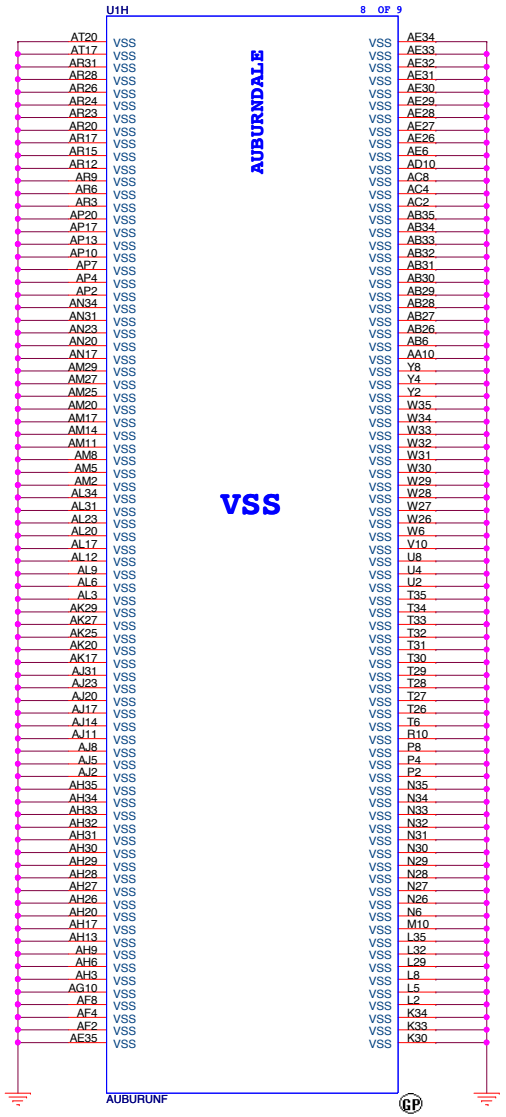
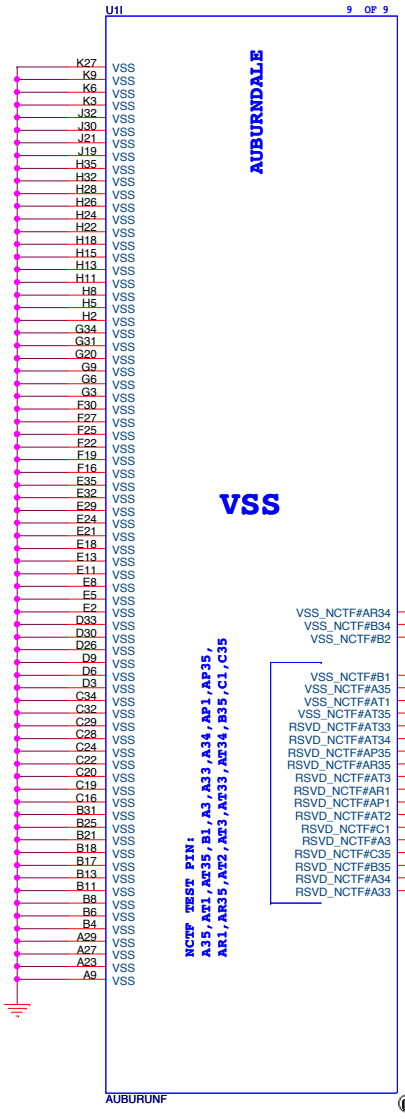
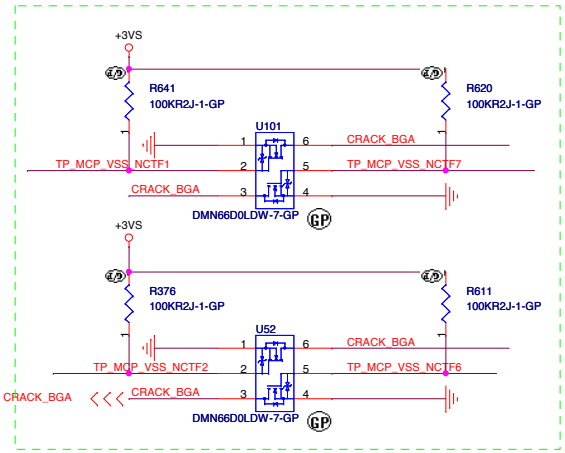
CPU(6/7)





All NCTF pins should be Test Points and should be routed as trace.

090829-1



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Title: CPU (6/7)-VSS

Size: A3 | Document Number: S-Class Intel | Rev: SD

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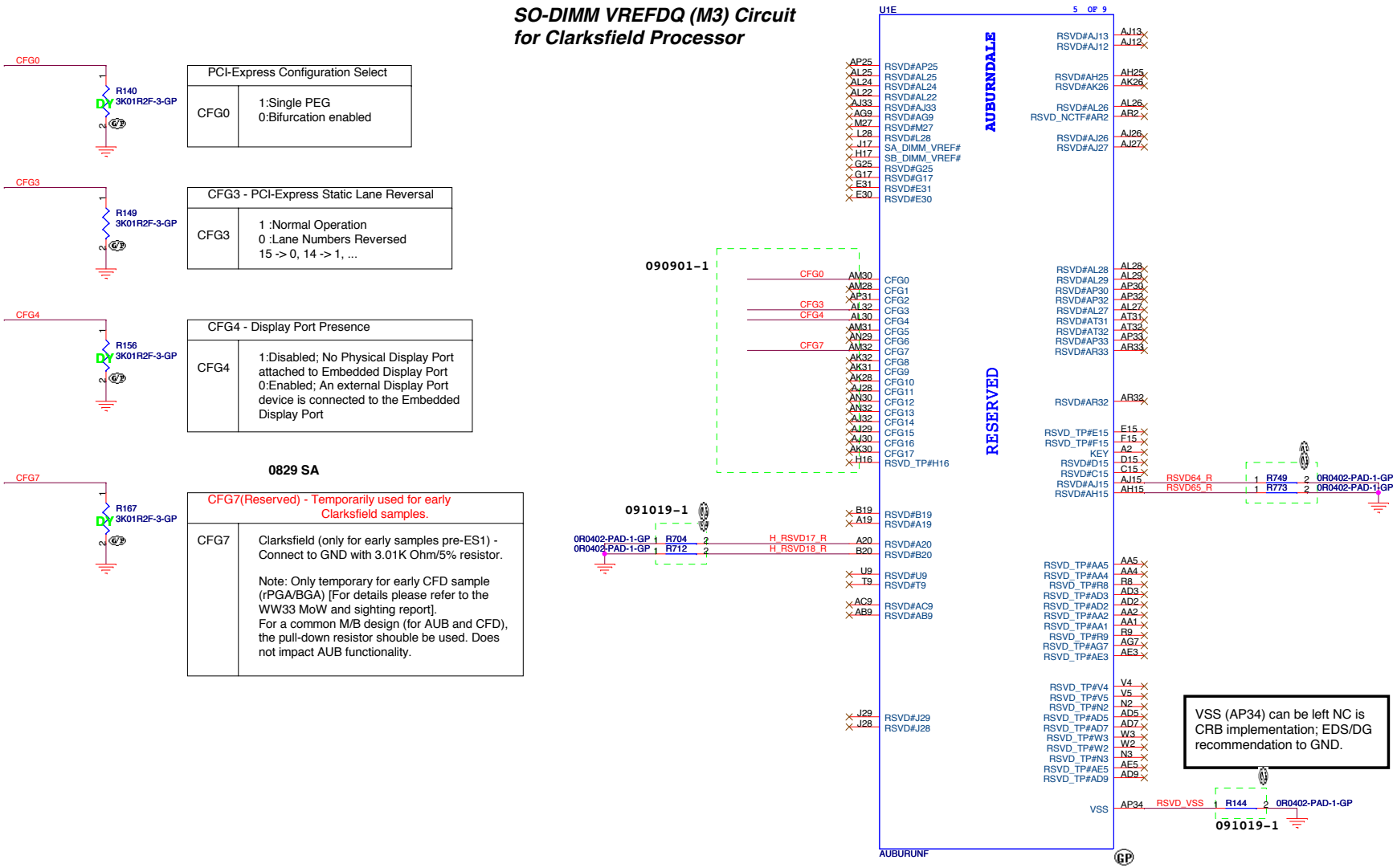
CPU(7/7)

SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor



<Core Design>

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Title: CPU (7/7)-RESERVED

Size: A3 | Document Number: S-Class Intel | Rev: SD

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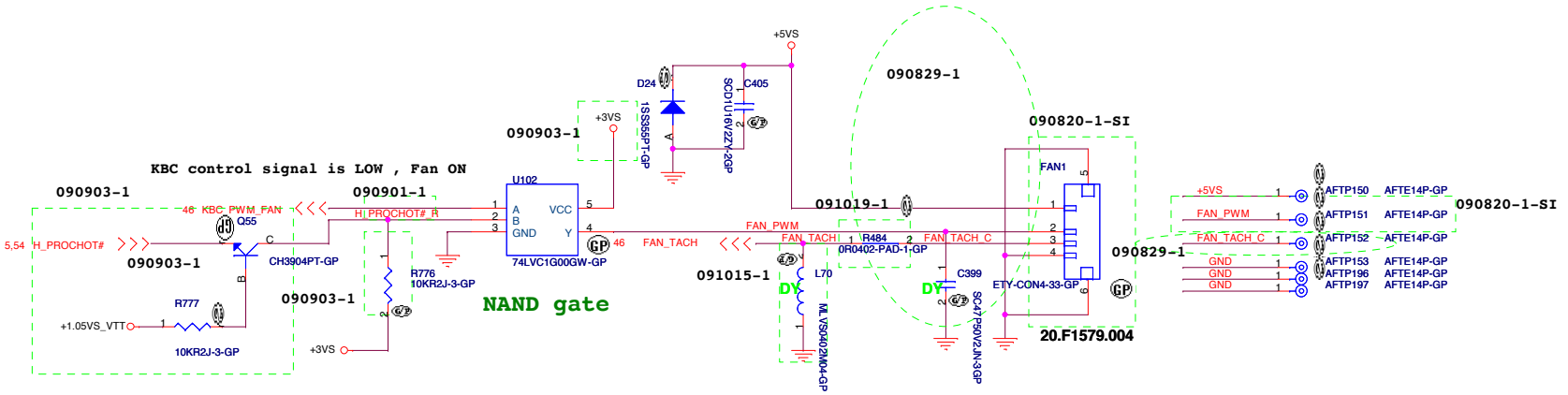
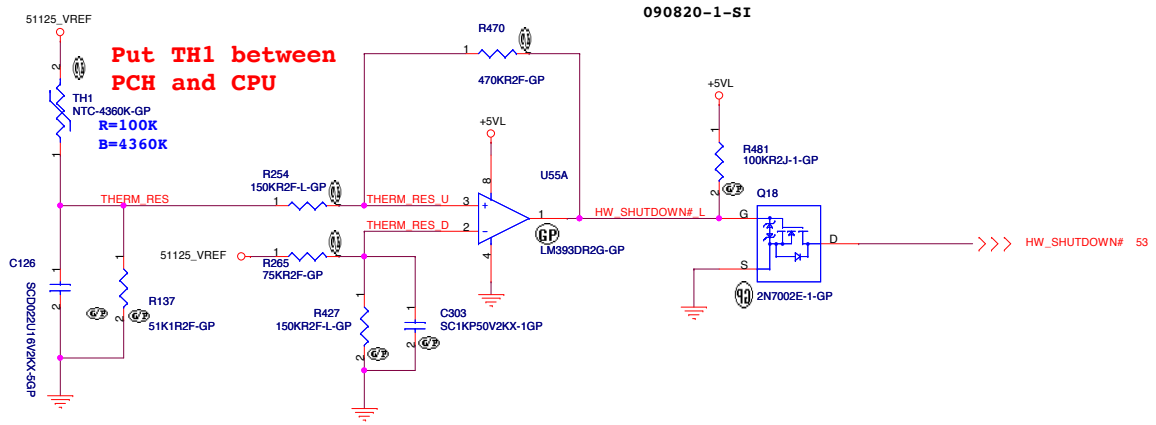
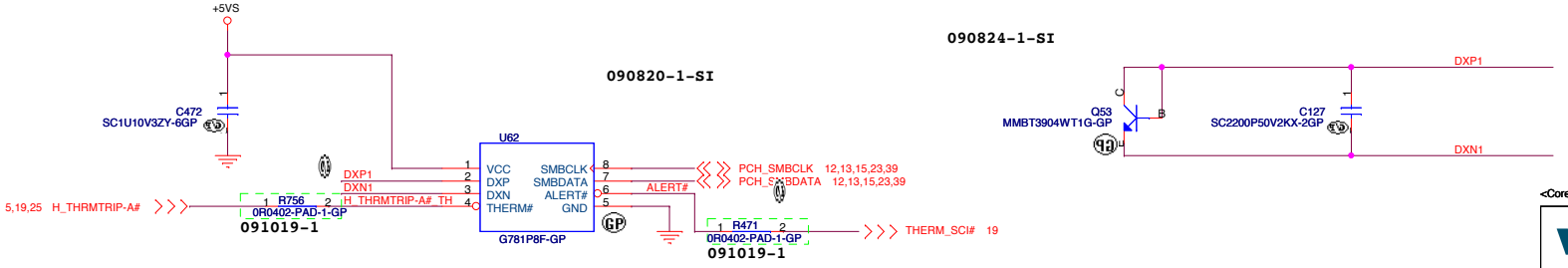
4 WIRE PWM Fan Control circuit



T8 H/W Shutdown Control circuit



Thermal IC Control circuit



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Title: G787S11U-GP THERMAL

Size: A3 | Document Number: S-Class Intel | Rev: SD

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DIMM2

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Place between DM1 and DM2.

Place these caps close to VTT1 and VTT2.

SODIMM A DECOUPLING

Layout Note:
Place these Caps near SO-DIMMA.

H = 9.2mm

62.10017.I11

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Title: DDRIII Socket DM1

Size: Custom | Document Number: S-Class Intel | Rev: SD

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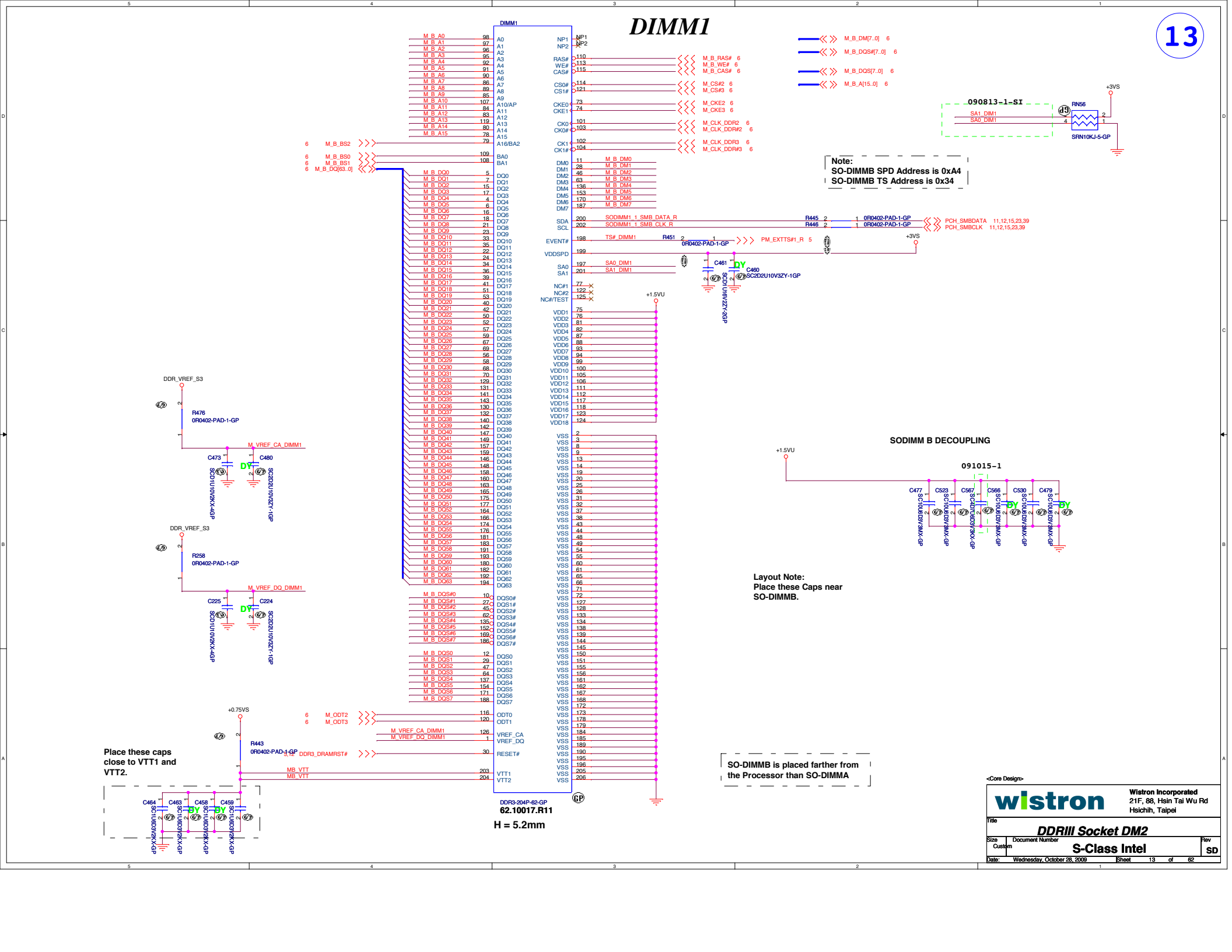
DIMM1



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Title: DDRIII Socket DM2

Size	Document Number	Rev
Custom	S-Class Intel	SD

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PCH(1/9)

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

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RTC: RTCX1 B13, RTCX2 D13, RTCRST# C14, SRTCRST# D17, INTRUDER# A16, INTVRMEN A14
LPC: FWH0/LAD0 D33, FWH1/LAD1 B33, FWH2/LAD2 C32, FWH3/LAD3 A32, FWH4/LFRAME# C34, LDRQ0# A34, LDRQ1#/GPIO23 F34, SERIRQ AB9
IHDA: HDA_BCLK A30, HDA_SYNC D29, SPKR P1, HDA_RST# C30, HDA_SDIN0 G30, HDA_SDIN1 F30, HDA_SDIN2 E32, HDA_SDIN3 F32, HDA_SDO B29
SATA: HDA_DOCK_EN#/GPIO33 H32, HDA_DOCK_RST#/GPIO13 J30; SATA0RXN AK7, SATA0RXP AK6, SATA0TXN AK11, SATA0TXP AK9; SATA1RXN AH6, SATA1RXP AH5, SATA1TXN AH9, SATA1TXP AH8; SATA2RXN AF11, SATA2RXP AF9, SATA2TXN AF7, SATA2TXP AF6; SATA3RXN AH3, SATA3RXP AH1, SATA3TXN AF3, SATA3TXP AF1; SATA4RXN AD9, SATA4RXP AD8, SATA4TXN AD6, SATA4TXP AD5; SATA5RXN AD3, SATA5RXP AD1, SATA5TXN AB3, SATA5TXP AB1; SATAICOMPO AF16, SATAICOMPI AF15; SATALED# T3; SATA0GP/GPIO21 Y9; SATA1GP/GPIO19 V1
JTAG: JTAG_TCK M3, JTAG_TMS K3, JTAG_TDI K1, JTAG_TDO J2, TRST# J4
SPI: SPI_CLK BA2, SPI_CS0# AV3, SPI_CS1# AY3, SPI_MOSI AY1, SPI_MISO AV1
IBEXPEAK-M-GP-NF

LPC_AD[0..3] 45,46; LPC_FRAME# 45,46; SIRQ 45,46; PCH_GPIO23; TP112 TPAD14-GP; 090821-1-SI

HDD: SATA_RXN0 35, SATA_RXP0 35, SATA_TXN0 35, SATA_TXP0 35
ODD: SATA_RXN1 35, SATA_RXP1 35, SATA_TXN1 35, SATA_TXP1 35
ESATA: SATA_RXN4 44, SATA_RXP4 44, SATA_TXN4 44, SATA_TXP4 44

SATAICOMP R634 37D4R2F-GP; +1.05VS
SATA_LED# 090901-1; EC984 SC470P50V2KX-3GP
SATA_LED# 34; 10KR2J-3-GP; +3VS
HDD_HALTLED R323 10KR2J-3-GP
HDD_HALTLED_1 R326 0R0402-PAD-1-GP 091019-1; HDD_HALTLED 34

+RTCVCC
R365 20KR2J-L2-GP
C395 SC1U10V3KX-3GP
G24 GAP-OPEN
R364 20KR2J-L2-GP
C390 SC1U10V3KX-3GP
R699 1MR2J-1-GP
R707 330KR2F-L-GP

HDA_BITCLK_CODEC
HDA_BITCLK_MDC
C392 SC33P50V2JN-3GP
C391 SC33P50V2JN-3GP
090909-1
R785 0R2J-2-GP
R786 0R2J-2-GP
091015-1 091015-1

RN50 SRN33J-7-GP
41 HDA_BITCLK_CODEC
41 HDA_SYNC_CODEC
41 HDA_RST#_CODEC
41 HDA_SDOUT_CODEC
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
RN49 SRN33J-7-GP
47 HDA_BITCLK_MDC
47 HDA_SYNC_MDC
47 HDA_RST#_MDC
47 HDA_SDOUT_MDC
HDA_SDOUT

41 HDA_SPKR
41 HDA_SDIN0
47 HDA_SDIN1
TPAD14-GP TP117
TPAD14-GP TP110

ICH_RTCX1
ICH_RTCX2
ICH_RTCRST#
SRTCRST#
SM_INTRUDER#
ICH_INTVRMEN

NO REBOOT STRAP

+3VS
R336 10KR2J-3-GP HDA_SPKR
R636 10KR2J-3-GP SIRQ
090829-1

No Reboot Strap R336	
HDA_SPKR	Low = Default High = No Reboot

VTAP Assumed as 1.1V

PCH_JTAG_RST# R347 51R2F-2-GP
PCH_JTAG_TCK R338 4K7R2J-2-GP
+1.05VS
PCH_JTAG_TMS R342 51R2F-2-GP
PCH_JTAG_TDO R351 51R2F-2-GP
PCH_JTAG_TDI R345 51R2F-2-GP
PCH_JTAG_RST# R349 10KR2J-3-GP

Place the resistors on RST, TCK, TMS, and TDI near PCH.

Place the resistors on TDO near XDP.

090829-1
091008-1
090813-1-SI
091019-1

46 KBC_SPI_CLK R295 33R2J-2-GP KBC_SPI_CLK_R; R58 100KR2J-1-GP
46 KBC_SPI_CS0# R303 0R0402-PAD-1-GP KBC_SPI_CS0#_R
46 KBC_SPI_CS1# R300 0R0402-PAD-1-GP KBC_SPI_CS1#_R
46 KBC_SPI_SI R297 33R2J-2-GP KBC_SPI_SI_R
46 KBC_SPI_SO

Oscillator

ICH_RTCX1
ICH_RTCX2
R358 10MR2J-L-GP
090903-1
X1
090825-1-SI
090825-1-SI
C386 SC15P50V2JN-2GP
C387 SC15P50V2JN-2GP
X-32D768KHZ-38GPU
82.30001.691
32.768Khz 12.5pf 10ppm
1st: 82.30001.691 (KDS)

BIOS have Default code & Run code. If we want to flash default code area, we should set GPIO33 be Low when SYS_PWROK assert.

+3VS
R719 10KR2J-3-GP
R692 1KR2F-3-GP GPIO33
Q48 2N7002E-1-GP
46,51 WHITE_BATLED#
R718 0R2J-2-GP

RTC Battery

+RTCVCC
091019-1 W=20mils
R352 0R0402-PAD-1-GP
RTC_PWR_L
C372 SC1U10V3KX-3GP
090919-1
U43 CH715FPT-GP
RTC_PWR W=20mils
090829-1
3D3V_AUX_S5_5_51125
BATT1.1
R353 1KR2J-1-GP W=20mils
090819-1-SI
RTC1
PWR GND NP1 NP2
BAT-BB0201-C1401-7H-GP
62.70001.031
090829-1

<Core Design>

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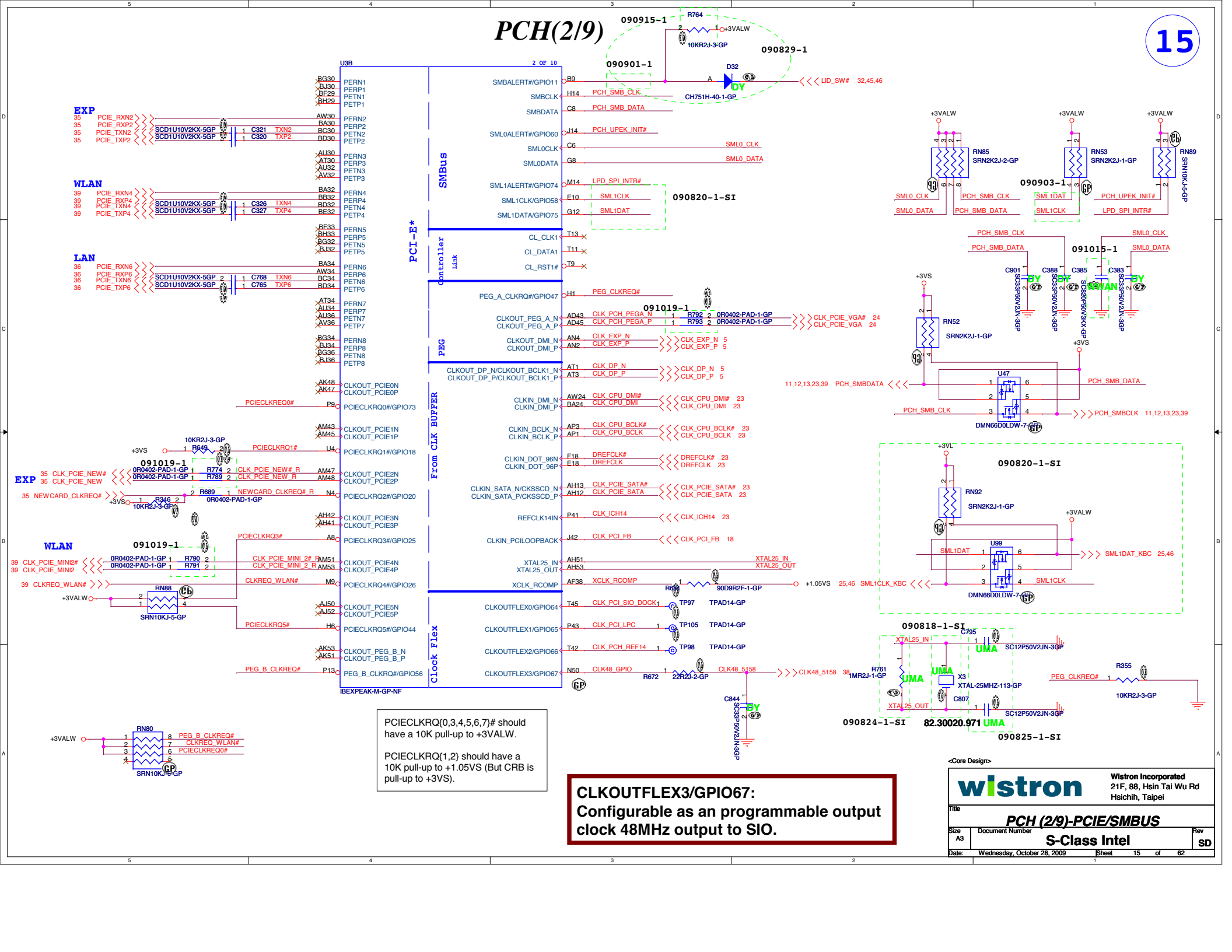
Title: PCH (1/9)-SATA/SPI/LPC
Size: A3 | Document Number: S-Class Intel | Rev: SD
Date: Wednesday, October 28, 2009 | Sheet 14 of 62

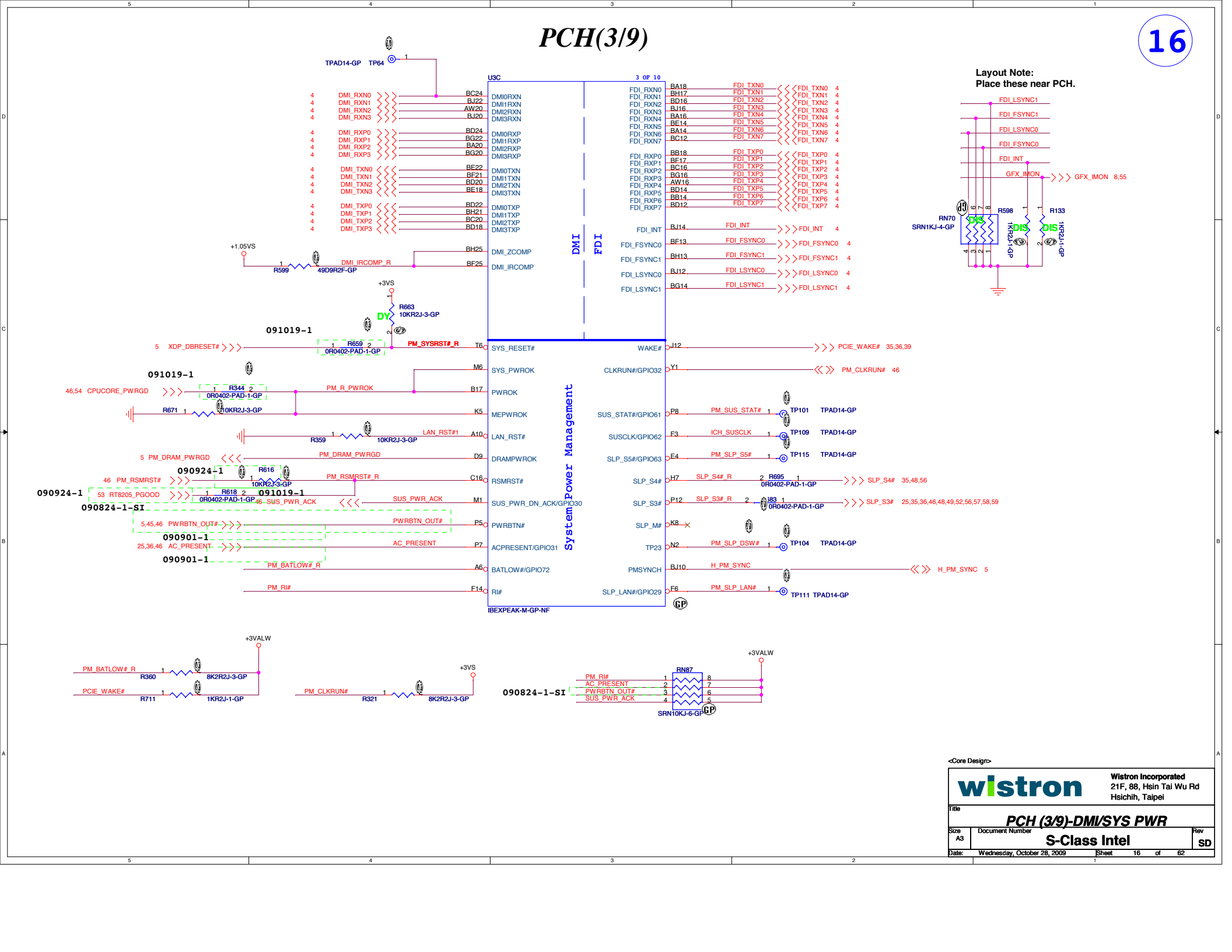
PCH(2/9)


15
U3B
2 OF 10
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
IBEXPEAK-M-GP-NF
EXP
WLAN
LAN
SMBALERT#/GPIO11
SMBCLK
SMBDATA
SML0ALERT#/GPIO60
SML0CLK
SML0DATA
SML1ALERT#/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
CL_CLK1
CL_DATA1
CL_RST1#
PEG_A_CLKRQ#/GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N/CLKOUT_BCLK1_N
CLKOUT_DP_P/CLKOUT_BCLK1_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_BCLK_N
CLKIN_BCLK_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N/CKSSCD_N
CLKIN_SATA_P/CKSSCD_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
PCIECLKRQ0/GPIO73
PCIECLKRQ1/GPIO18
PCIECLKRQ2/GPIO20
PCIECLKRQ3/GPIO25
CLKREQ_WLAN#
PCIECLKRQ5/GPIO44
PEG_B_CLKREQ#
090915-1
090829-1
090901-1
090820-1-SI
091019-1
090903-1
091015-1
090818-1-SI
090824-1-SI
090825-1-S
82.30020.971 UMA
D32
CH751H-40-1-GP
LID_SW#
PCH_SMB_CLK
PCH_SMB_DATA
PCH_UPEK_INIT#
SML0_CLK
SML0_DATA
SML1CLK
SML1DAT
LPD_SPI_INTR#
RN85 SRN2K2J-2-GP
RN53 SRN2K2J-1-GP
RN89 SRN10KJ-5-GP
RN52 SRN2K2J-1-GP
RN92 SRN2K2J-1-GP
RN80 SRN10KJ-5-GP
RN88 SRN10KJ-5-GP
U47
U99
DMN66D0LDW-7-GP
PCH_SMBCLK
PCH_SMBDATA
SML1DAT_KBC
SML1CLK_KBC
CLK_PCIE_VGA
CLK_PCIE_VGA#
CLK_EXP_N
CLK_EXP_P
CLK_DP_N
CLK_DP_P
CLK_CPU_DMI
CLK_CPU_DMI#
CLK_CPU_BCLK
CLK_CPU_BCLK#
CLK_PCIE_SATA
CLK_PCIE_SATA#
CLK_ICH14
CLK_PCI_FB
DREFCLK
DREFCLK#
CLK_PCI_SIO_DOCK
CLK_PCI_LPC
CLK_PCH_REF14
CLK48_GPIO
CLK48_5158
TP97 TPAD14-GP
TP105 TPAD14-GP
TP98 TPAD14-GP
R672 22R2J-2-GP
R761 1MR2J-1-GP
X3 XTAL-25MHZ-113-GP
C844 SC33P50V2JN-3GP
C795 SC12P50V2JN-3GP
C807 SC12P50V2JN-3GP
C901 SC33P50V2JN-3GP
C388 SC33P50V2JN-3GP
C385 SC820P50V3KX-GP
C383 SC33P50V2JN-3GP
R355 10KR2J-3-GP
R649 10KR2J-3-GP
R346 10KR2J-3-GP
R689 0-0402-PAD-1-GP
R774 0R0402-PAD-1-GP
R789 0R0402-PAD-1-GP
R790 0R0402-PAD-1-GP
R791 0R0402-PAD-1-GP
R792 0R0402-PAD-1-GP
R793 0R0402-PAD-1-GP
R90 90D9R2F-1-GP
PCIECLKREQ0#
PCIECLKREQ1#
CLK_PCIE_NEW#
CLK_PCIE_NEW_R
NEWCARD_CLKREQ#
NEWCARD_CLKREQ#_R
CLK_PCIE_MINI_2#_R
CLK_PCIE_MINI_2_R
CLKREQ_WLAN#
PCIECLKRQ3#
PCIECLKRQ5#
PEG_B_CLKREQ#
CLK48_5158
XTAL25_IN
XTAL25_OUT
+3VALW
+3VS
+1.05VS
+3VL
UMA
PCIECLKREQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKREQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
CLKOUTFLEX3/GPIO67: Configurable as an programmable output clock 48MHz output to SIO.
<Core Design>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
PCH (2/9)-PCIE/SMBUS
Size A3
Document Number
S-Class Intel
Rev SD
Date: Wednesday, October 28, 2009
Sheet 15 of 62

PCH(3/9)

16

Layout Note:
Place these near PCH.



<Core Design>

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Title: PCH (3/9)-DMI/SYS PWR

Size	Document Number	Rev
A3	S-Class Intel	SD

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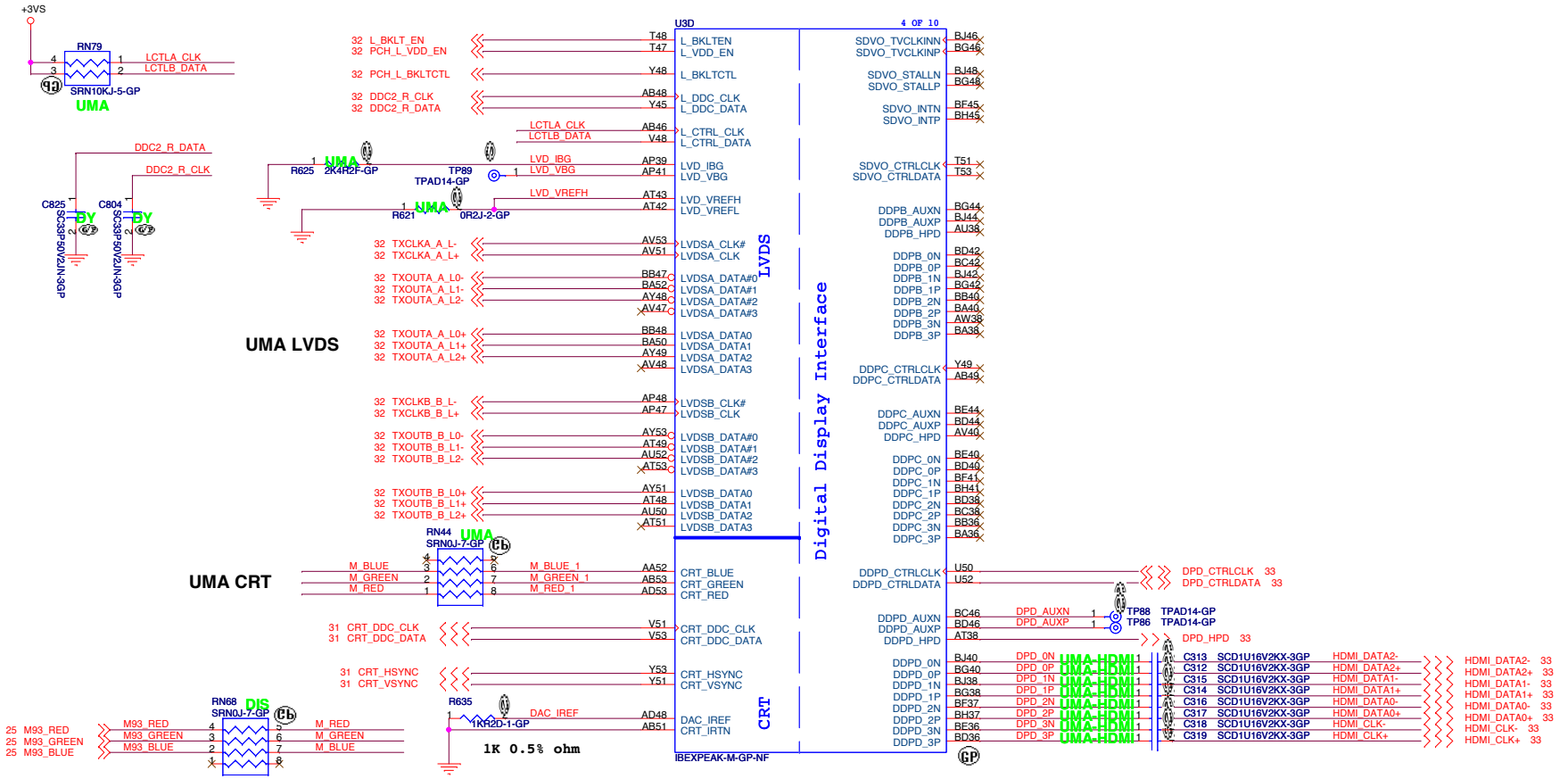
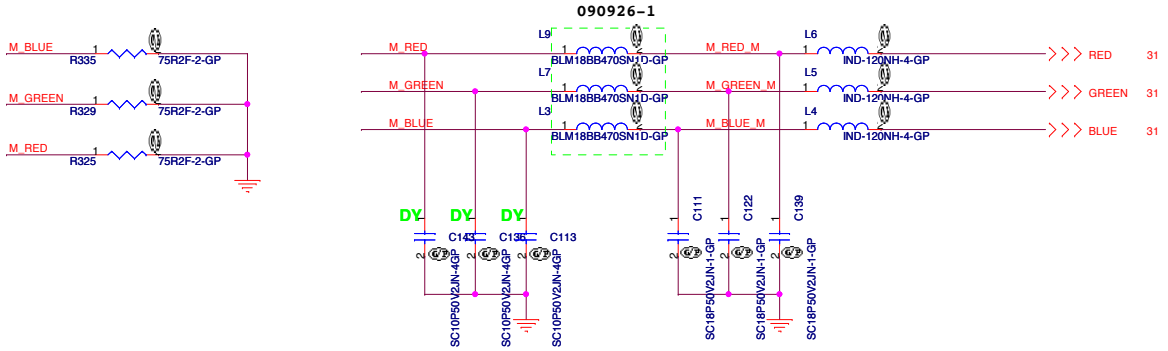
PCH(4/9)





<Core Design>

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Title: PCH (4/9)-LVDS/CRT

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 17 of 62

PCH(5/9)

U3E — 5 OF 10 — IBEXPEAK-M-GP-NF

BOOT BIOS Strap

PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
0	1	Reserved
1	0	PCI
1	1	SPI

USE SPI

USB

Pair	Device
0	External USB2
1	USB1 (Debug port)
2	ESATA USB4
3	Card Reader
4	NEW CARD
5	FREE
6	WLAN
7	FREE
8	BLUETOOTH
9	WWAN
10	Fingerprint
11	External USB3
12	CAMERA
13	FREE

091019-1

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

Danbury Technology:
Disabled when Low.
Enable when High.

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	

Low = A16 swap override/Top-Block Swap Override enabled
High = Default

<Core Design>

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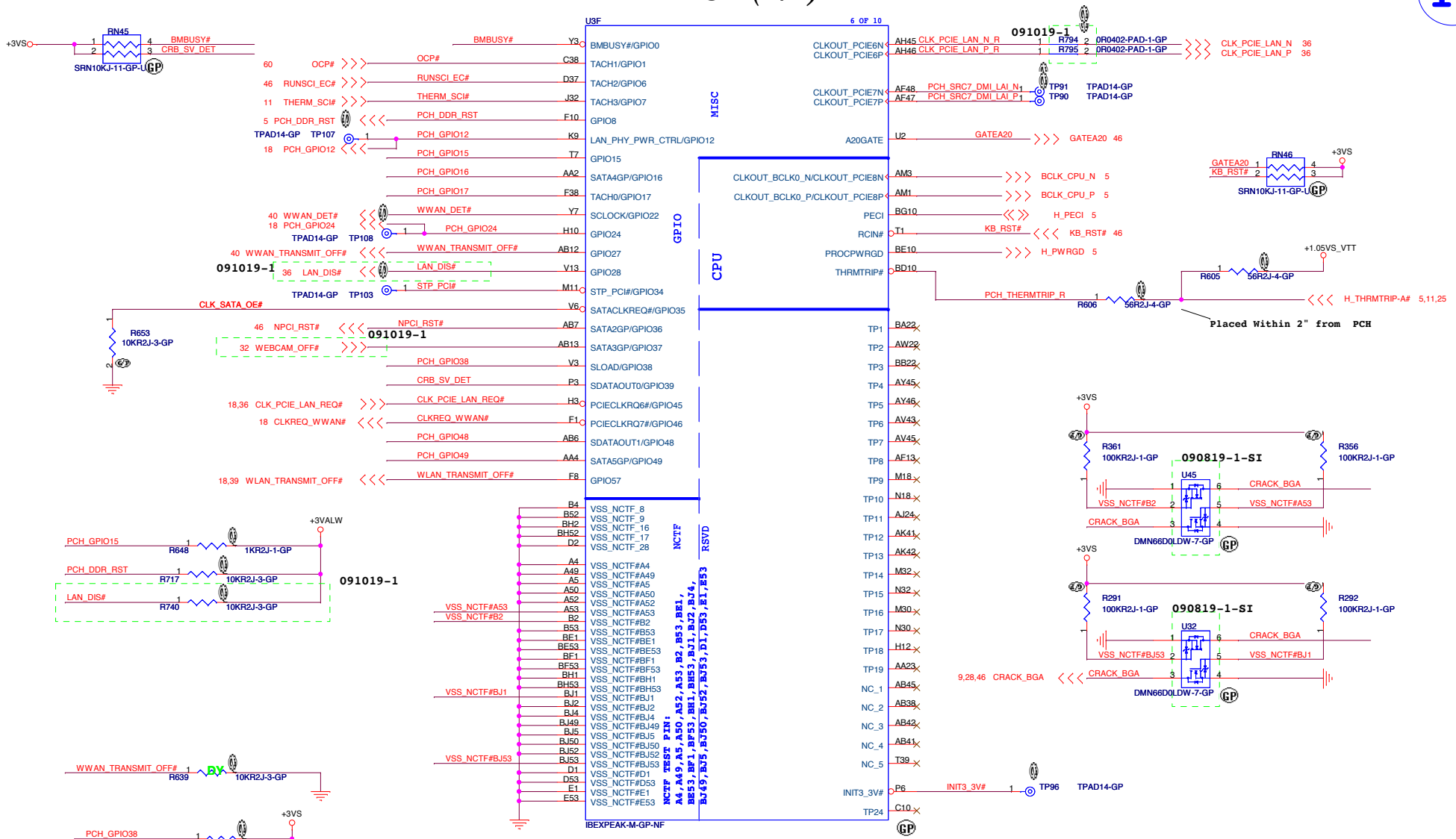
Title: PCH (5/9)-PCI/USB

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 18 of 62

PCH(6/9)

19



<Core Design>

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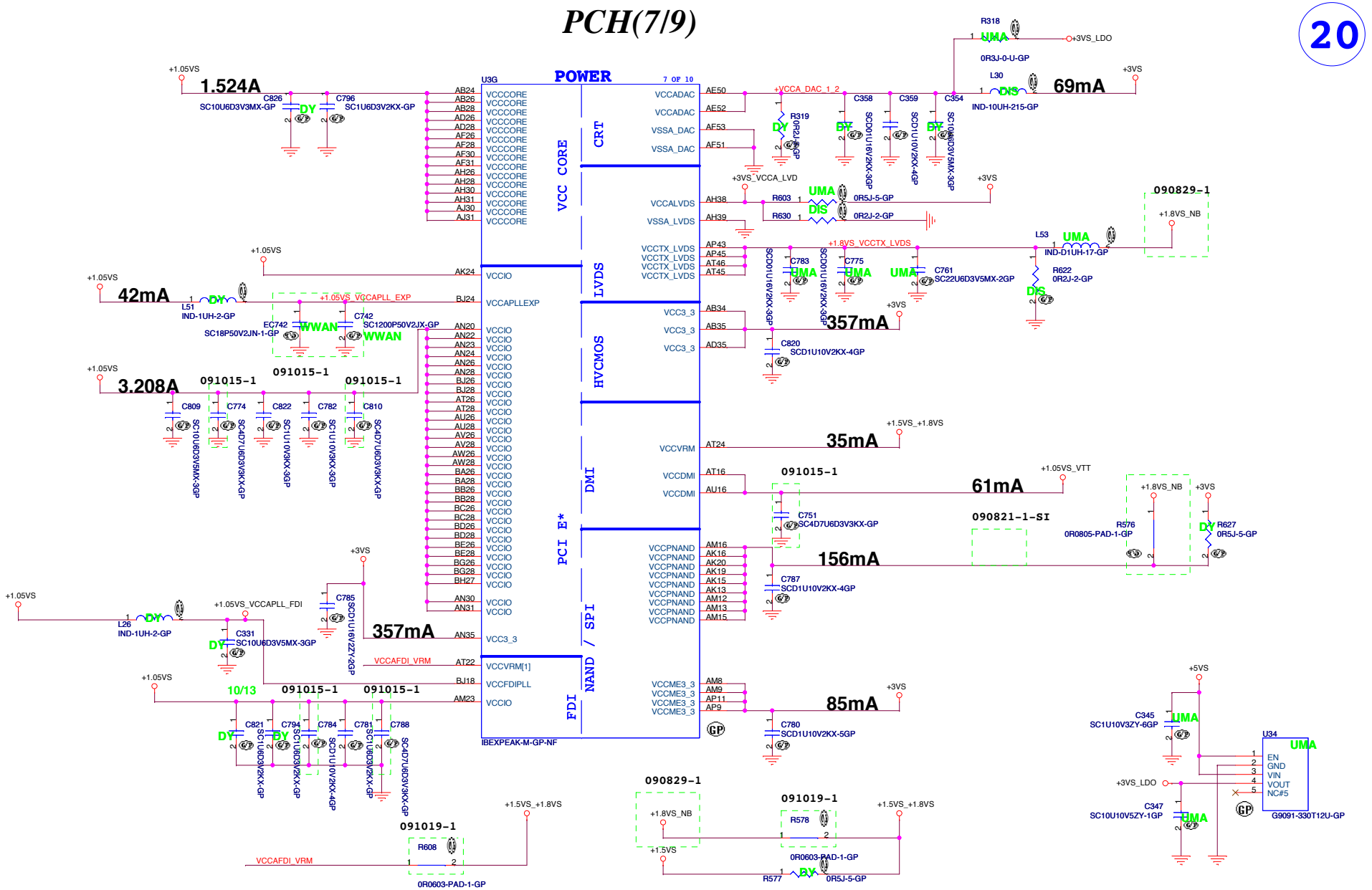
Hsichih, Taipei

Title: PCH (6/9)-GPIO

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 19 of 62

PCH(7/9)



<Core Design>

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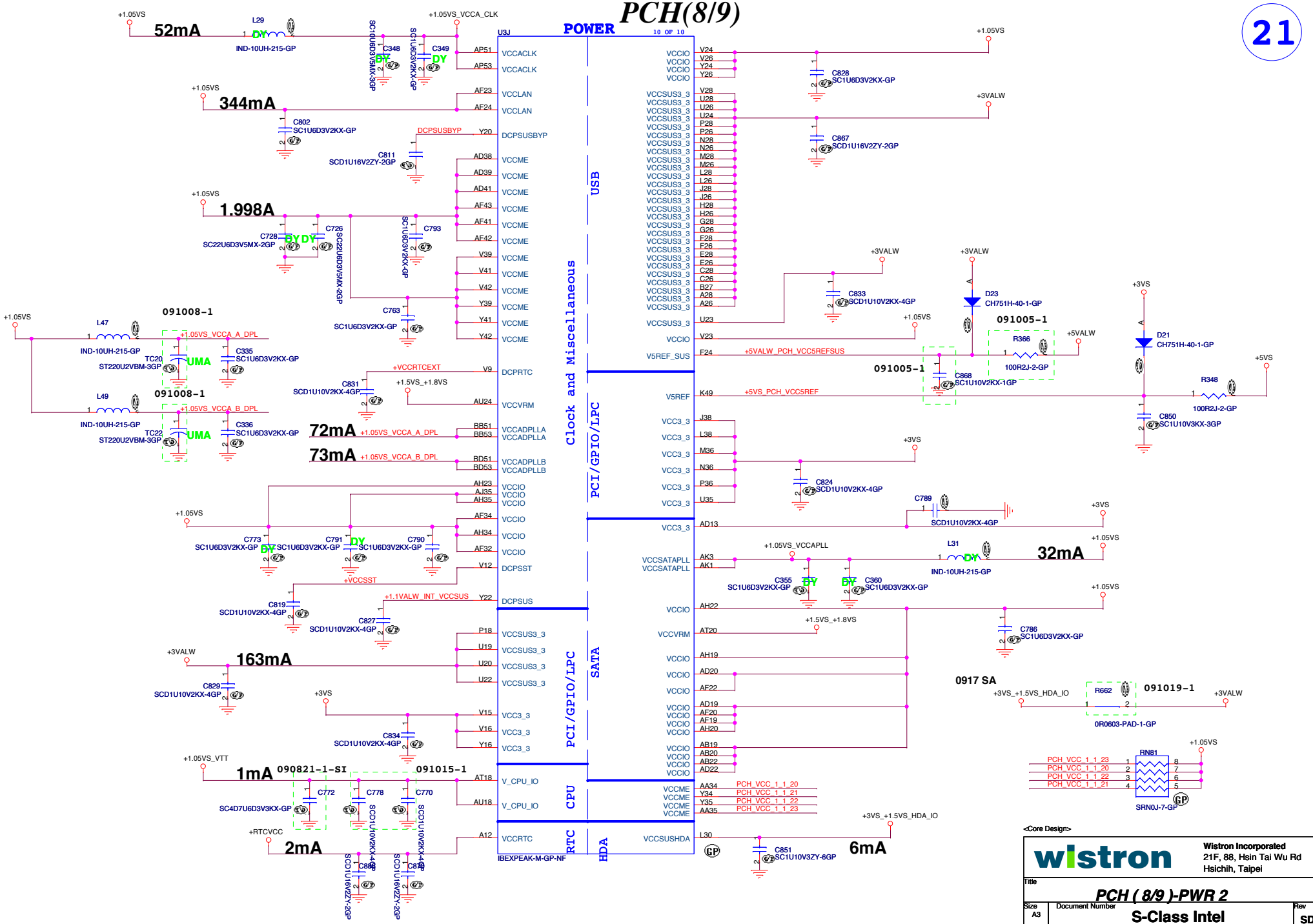
Title: PCH (7/9)-PWR 1

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 20 of 62

PCH(8/9)



<Core Design>

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Title: PCH (8/9)-PWR 2

Size: A3 | Document Number: S-Class Intel | Rev: SD

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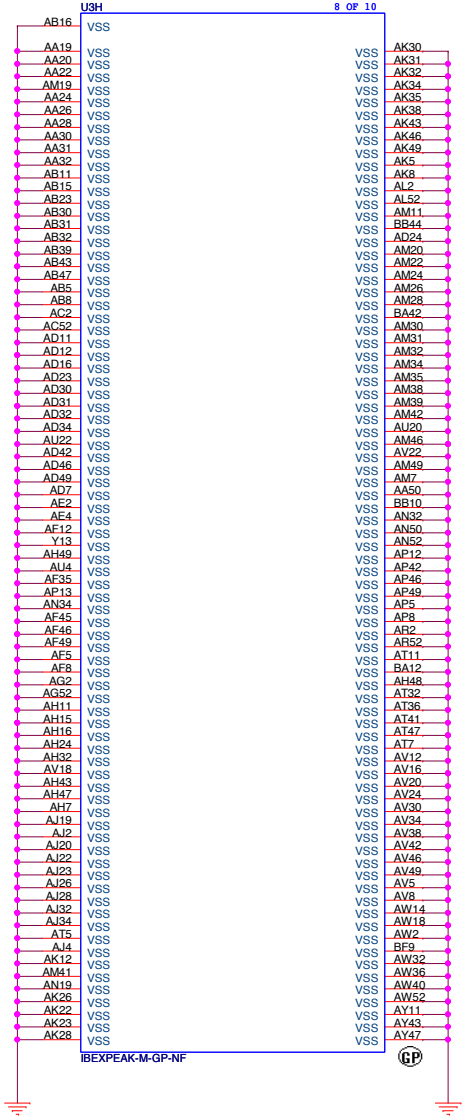
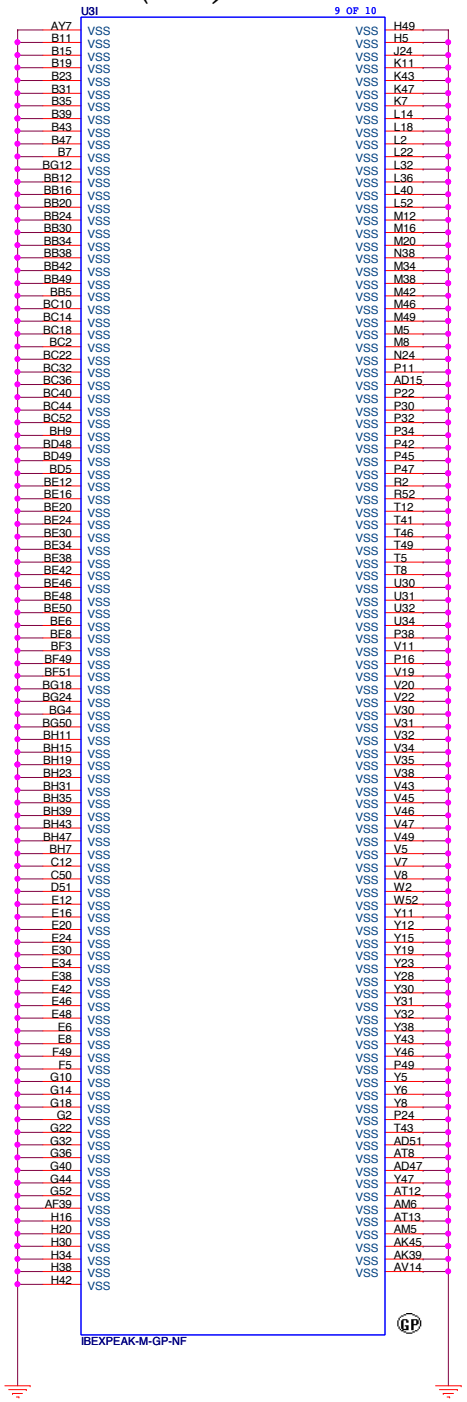
PCH(9/9)





<Core Design>

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Hsichih, Taipei

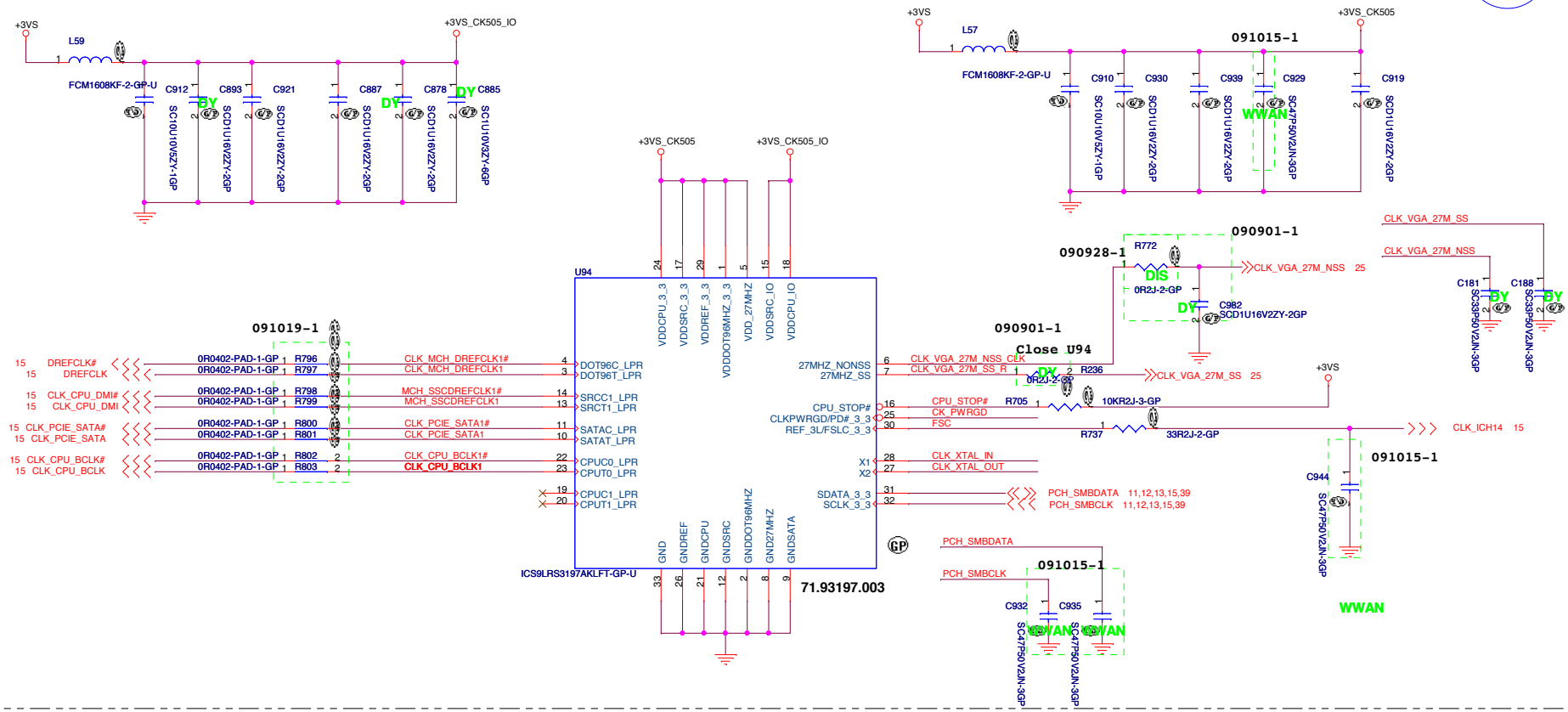
Title: PCH (9/9)-VSS

Size	Document Number	Rev
A3	S-Class Intel	SD

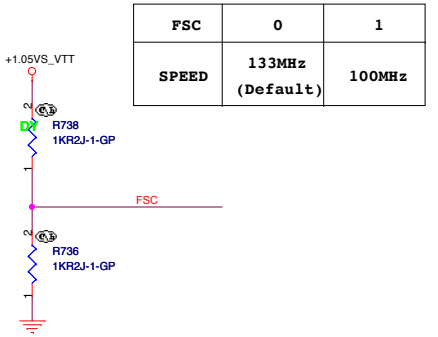
Date: Wednesday, October 28, 2009 Sheet 22 of 62

CLOCK GENERATOR

23

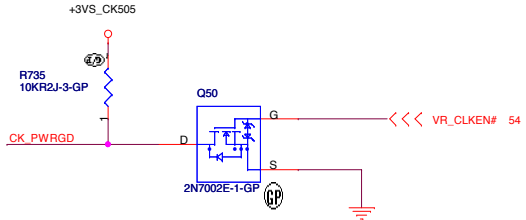


FSB Frequency Select

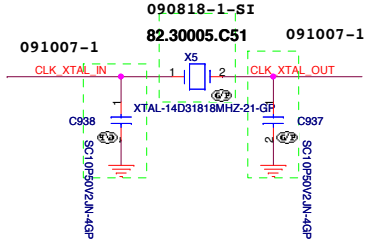


FSC	0	1
SPEED	133MHz (Default)	100MHz

Clock Gen. Eable



Clock Gen. Crystal



<Core Design>

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Hsichih, Taipei

Title: Clock Generator ICS9LRS3197

Size: A3 | Document Number: S-Class Intel | Rev: SD

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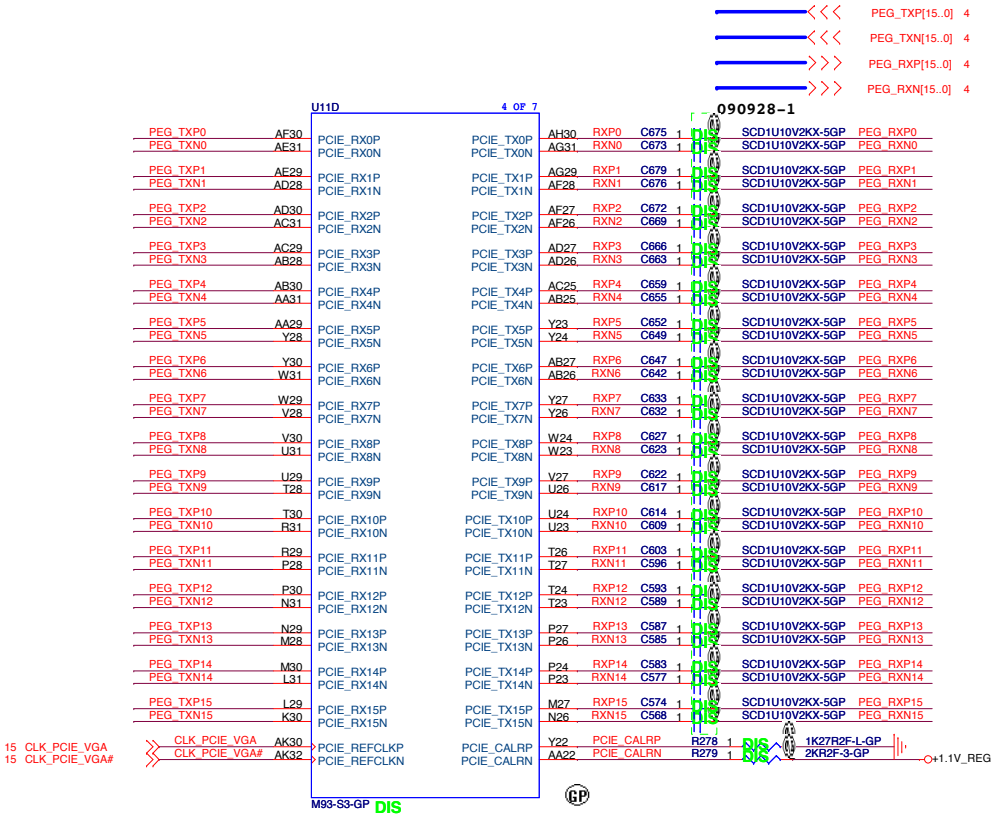
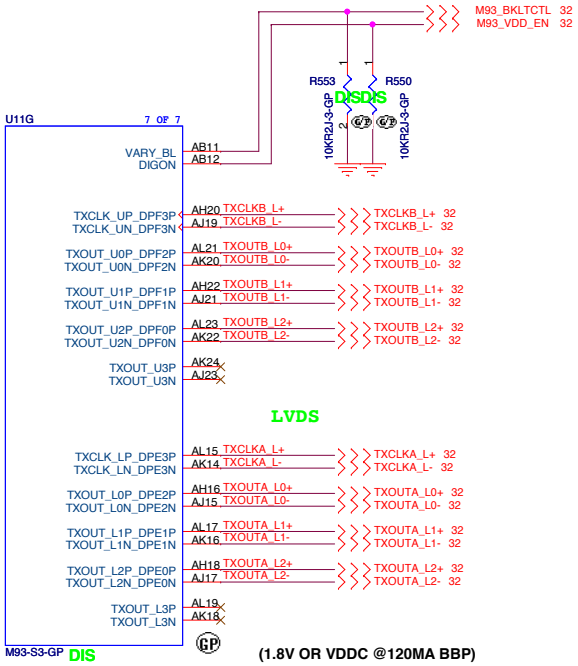
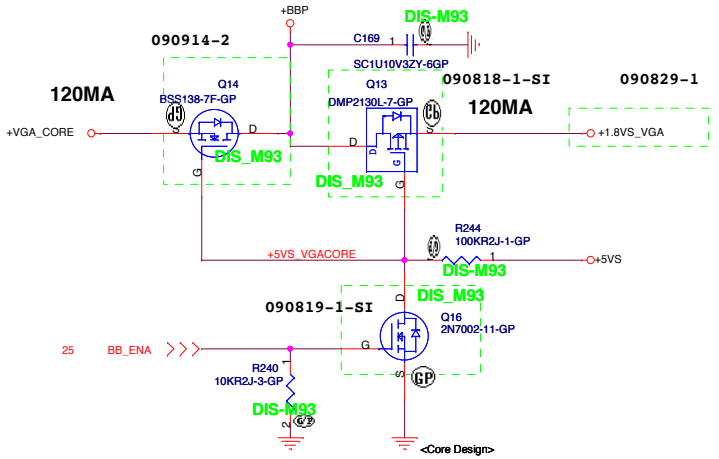
M93 GPU(1/5)

24







<Core Design>

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Hsichih, Taipei

Title: VGA-PCIE/LVDS(1/5)

Size	Document Number	Rev
A3	S-Class Intel	SD

Date: Wednesday, October 28, 2009 Sheet 24 of 62

M93 GPU(2/5)

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

0 = DON'T INSTALL RES
1 = INSTALL 10K RES
X = DESIGN DEPENDANT
N/A = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M93-S3
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD BIF_VGA DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROM ID CFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 XX

Aperture Conig. PIN	M93S3 GPIO	Strapping Resistor	64MB VRAM	128MB VRAM	256MB VRAM
CONFIG0	GPIO_11	R243	0	0	1
CONFIG1	GPIO_12	R246	1	0	0
CONFIG2	GPIO_13	R250	0	0	0

VRID 3 2 1 0	Vendor	Type	Vendor P/N
0000	Hynix Orion-die	64*16-800MHZ	H5TQ1G63BFR-12C
0001	Samsung E-die	64*16-800MHZ	K4W1G1646E-HC12

090824-1-SI

VRAM ID:
BIT0 --> L:Quanta ; H:Wistron
BIT1 --> L:512M ; H:1GB
BIT2 --> L:Samsung ; H:Hynix
BIT3 -->N/A

090829-1

VRAM ID

090824-1-SI

M93 LP: VDDC=0.9/1.1V

GPIO20_VID1	GPIO15_VID0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V

LVDS

32 DDC2_CLK
32 DDC2_DATA

091019-1

0R0402-PAD-1-GP R804
0R0402-PAD-1-GP R805

GPU_LVDS_SCL
GPU_LVDS_SDA

R1 SCL
R3 SDA

091008-1

090820-1-SI

16,36,46 AC_PRESENT

D39 1SS355PT-GP

DDC2_CLK
DDC2_DATA

32 M93_BKLT_EN

C177 C182 2200P/50V/X7R-2-GP

090820-1-SI

TPAD14-GP TP74
TPAD14-GP TP124

GPIO0 GPIO1 GPIO2 GPIO3_SMBDATA GPIO4_SMBCLK GPIO5_ACBATT GPIO6 GPIO7_BLON GPIO8_ROMSO GPIO9_ROMSI GPIO10_ROMSCK GPIO11 GPIO12 GPIO13 M93_HPD2

GPIO0 U6
GPIO1 U10
GPIO2 T10
GPIO3_SMBDATA U8
GPIO4_SMBCLK U7
GPIO5_ACBATT T9
GPIO6 T8
GPIO7_BLON T7
GPIO8_ROMSO P10
GPIO9_ROMSI P4
GPIO10_ROMSCK P2
GPIO11 N6
GPIO12 N5
GPIO13 N3
M93_HPD2 Y9

090901-1

GPIO17_THERMAL_INT R6
M93_HPD3 W10

GPIO15_PWRCNTL0 M4
GPIO16_SSIN M2
GPIO17_THERMAL_INT M1
GPIO18_HPD3 P8
GPIO19_CTF P7
GPIO20_PWRCNTL1 P2
GPIO21_BB_EN N8
GPIO22_ROMCS# N4
GPIO23_CLKREQB N7

59 GPIO15_VID0
23 CLK_VGA_27M_SS
59 GPIO20_VID1
24 BB_ENA

TPAD14-GP TP125

GPU_CTF

Q15 2N7002E-1-GP

R245 0R0402-PAD-1-GP

5,11,19 H_THRMTRIP-A#
H_THRMTRIP-A#_R

091019-1

090903-1

+3.3V_DELAY

GPIO11 R243 10KR2J-3-GP
GPIO12 R246 10KR2J-3-GP
GPIO13 R250 10KR2J-3-GP
GPIO23_CLKREQB R237 10KR2J-3-GP
GPIO5 R255 10KR2J-3-GP
GPU_CTF R241 10KR2J-3-GP
M93_HPD2 R552 100KR2J-1-GP
M93_HPD3 R551 100KR2J-1-GP
M93_HPD4 R548 100KR2J-1-GP

RN16 SRN10KJ-3-GP

GPIO0 GPIO1 GPIO2 GPIO8 GPIO9 GPIO22 GENERICA

RN15 SRN10KJ-1T-GP

GENERICB GENERICC

090829-1

+1.8VS_VGA

R277 5K11R2F-L1-GP
R275 5K11R2F-L1-GP

TESTEN

R565 499R2F-2-GP
R561 249R2F-GP

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = .6V)

C705 SCD1U10V2KX-4GP

28 GPU_TESTEN#2

R517 10KR2J-3-GP

TPAD14-GP TP71
TPAD14-GP TP72
TPAD14-GP TP69
TPAD14-GP TP67

JTAG_TRSTB JTAG_TDI JTAG_TCK JTAG_TMS JTAG_TDO

L6 JTAG_TRST#
L5 JTAG_TDI
L3 JTAG_TCK
L1 JTAG_TMS
K4 JTAG_TDO
AF24 TESTEN

GENERICA AB13
GENERICB W8
GENERICC W9
W7
AD10 GENERICE_HPD4

M93_HPD4

33 HDMI_M93_HPD

AC14 HPD1

GPU_TESTEN#2 AC16 VREFG

091019-1

(1.8V @ 120MA DPLL_PVDD)

+1.8VS_VGA L40 BLM18PG471SN1D-GP

SC10U6D3V3MX-GP SCD1U10V2KX-4GP

DPLL_PVDD

090829-1 470R_1000mA

C719 C706 C670 SC1U6D3V2KX-GP

DPLL_PVSS

(1.1V @300MA DPLL_VDDC)

+1.1V_REG L17 BLM18PG471SN1D-GP

SC10U6D3V3MX-GP SCD1U10V2KX-4GP

DPLL_VDDC

470R_1000mA

C277 C268 C661 SC1U6D3V2KX-GP

DPLL_PVSS

091019-1

(1.8V @20MA TSVDD)

+1.8VS_VGA L24 BLM15BD121SS1D-GP

SC10U6D3V3MX-GP SCD1U10V2KX-4GP

TSVDD

090829-1

C307 C300 C298 SC1U6D3V2KX-GP

TSVSS

23 CLK_VGA_27M_NSS

R232 121R2F-GP

VOLTAGE DIVIDER TO MAKE
XTALIN VOLTAGE LEVEL OF 1.8V

R233 147R2F-GP

3.3V => 147 ohm

CLK_VGA_27M_NSS_R

TPAD14-GP TP15

XTALOUT_M93 AK28 XTALOUT

090824-1-SI

TPAD14-GP TP16
TPAD14-GP TP17

M93_DXP1_R T4 DPLUS
M93_DXN1_R T2 DMINUS

TSVDD R5

TS_FDO AD17
TSVDD AC17
TSVSS

DPLL_PVDD AF14
DPLL_PVSS AE14
DPLL_VDDC AD14

090820-1-SI

+3VS

RN93 SRN2K2J-1-GP

090903-1

U100 DMN66D0LDW-7-GP

GPIO3_SMBDATA
GPIO3_SMBCLK

SML1DAT_KBC 15,46
SML1CLK_KBC 15,46

U11E

M93-S3-GP

5 OF 7

DVCNTL0 AE9
DVCNTL1 L9
DVCNTL2 N9

VRID_0 Y7
VRID_1 Y8
VRID_2 AB2
VRID_3 AB4

DVDATA0 AB6
DVDATA1 AB7
DVDATA2 AB8
DVDATA3 AB9
DVDATA4 AC7
DVDATA5 AC8
DVDATA6 AD7
DVDATA7 AC10
DVDATA8 AD9
DVDATA9 AE8
DVDATA10
DVDATA11
DVDATA12

TP84 TP68 TP73
TP76 TP77 TP79 TP75 TP78 TP80 TP82 TP83 TP81

TX2P_DPA0P AK3
TX2M_DPA0N AK1
TX1P_DPA1P AH3
TX1M_DPA1N AH1
TX0P_DPA2P AG3
TX0M_DPA2N AG5
TXCAP_DPA3P AF2
TXCAM_DPA3N AF4

HDMI_DPA0P 33
HDMI_DPA0N 33
HDMI_DPA1P 33
HDMI_DPA1N 33
HDMI_DPA2P 33
HDMI_DPA2N 33
HDMI_DPA3P 33
HDMI_DPA3N 33

HDMI

TX5P_DPB0P AK8
TX5M_DPB0N AL7
TX4P_DPB1P AJ7
TX4M_DPB1N AH6
TX3P_DPB2P AK6
TX3M_DPB2N AM5
TXCBP_DPB3P AK5
TXCBM_DPB3N AM3

TX2P_DPC0P AA3
TX2M_DPC0N Y2
TX1P_DPC1P Y4
TX1M_DPC1N W5
TX0P_DPC2P W3
TX0M_DPC2N V2
TXCCP_DPC3P V4
TXCCM_DPC3N U5

M93_VGA_HSYNC
M93_VGA_VSYNC

RN18 SRN10KJ-11-GP-1-GP

+3.3V_DELAY

R AM26 M93_RED
RB AK26 M93_RB
G AL25 M93_GREEN
GB AJ25 M93_GB
B AH24 M93_BLUE
BB AG25 M93_BB

CRT

HSYNC AH26 M93_VGA_HSYNC 31
VSYNC AJ27 M93_VGA_VSYNC 31

RSET AD22 VGA_RSET R530 499R2F-2-GP

AVDD AG24 AVDD
AVSSQ AE22

VDD1DI AE23 M93_AGND VDD1_DI
VSS1DI AD23

NC#AM12_R2 AM12
NC#AK12_R2B AK12
NC#AL11_G2 AL11
NC#AJ11_G2B AJ11
NC#AK10_B2 AK10
NC#AL9_B2B AL9
NC#AH12_C AH12
NC#AM10_Y AM10
NC#AJ9_COMP AJ9

R532 0R2J-2-GP
M93_AGND

H2SYNC AL13 DAC2_HSYNC
V2SYNC AJ13 DAC2_VSYNC

RN20 SRN10KJ-11-GP-1-GP

+3.3V_DELAY

NC#AD19_VDD2DI AD19
NC#AC19_VSS2DI AC19
VDD2_DI

NC#AE20_A2VDD AE20 A2VDD
NC#AE17_A2VDDQ AE17 A2VDDQ
A2VSSQ AE19 M93_AGND

VGA_R2SET AG13 NC#AG13_R2SET R544 715R2F-GP

DIS_PARK

DDC1CLK AE6 DDC1_CLK 33
DDC1DATA AE5 DDC1_DATA 33

HDMI

AUX1P AD2
AUX1N AD4

090820-1-SI

DDC2CLK AC11
DDC2DATA AC13

AUX2P AD13
AUX2N AD11

AB22 RSVD#AB22
AC22 RSVD#AC22

RN66 SRN0J-10-GP-U

DIS_PARK

RSVD#AB22
RSVD#AC22

DDCCLK_AUX5P AE16
DDCDATA_AUX5N AD16

DDC6CLK AC1 DDC6_CLK 31
DDC6DATA AC3 DDC6_DATA 31

CRT

DDCCLK_UX3P AD20
DDCDATA_AUX3N AC20

090820-1-SI

(1.8V @ 70MA AVDD)

AVDD SCD1U10V2KX-4GP SC10U6D3V3MX-GP L25 BLM15BD121SS1D-GP +1.8VS_VGA

C299 C295 C305 SC1U6D3V2KX-GP

091019-1 090829-1

(1.8V @ 45MA VDD1DI)

VDD2_DI VDD1_DI

R568 0R2J-2-GP DIS_PARK

SCD1U10V2KX-4GP SC10U6D3V3MX-GP L41 BLM15BD121SS1D-GP +1.8VS_VGA

C696 C703 C714 SC1U6D3V2KX-GP

091019-1 090829-1

(1.8V @ 2MA A2VDDQ)

091019-1

A2VDDQ SCD1U10V2KX-4GP SC10U6D3V3MX-GP L48 BLM15BD121SS1D-GP +1.8VS_VGA

C727 C724 C730 SC1U6D3V2KX-GP

DIS_PARK DIS_PARK DIS_PARK

090829-1

(3.3V @ 65MA A2VDD)

A2VDD R274 0R2J-2-GP +3.3V_DELAY

DIS_PARK

DO NOT INSTALL for M93-S3
Only for PARK-S3

M93_RED 17
M93_GREEN 17
M93_BLUE 17
M93_BB
M93_GB
M93_RB

R545 R546 R547 0R2J-2-GP

090818-1-SI

+3VS

Q23 DMP2130L-7-GP

+3.3V_DELAY

R298 100KR2J-1-GP

DIS_M93

+3VS_+3.3V_DELAY

090819-1-SI

DIS_M93

49,58 VTT_EN

R302 0R2J-2-GP

R304 0R2J-2-GP

R301 0R2J-2-GP

Q22 2N7002-11-GP

DIS-M93

C342 SCD1U16V2ZY-2GP

16,35,36,46,48,49,52,56,57,58,59 SLP_S3#

Optional RC network to fine tune PWR SEQ.

<Core Design>

wistron

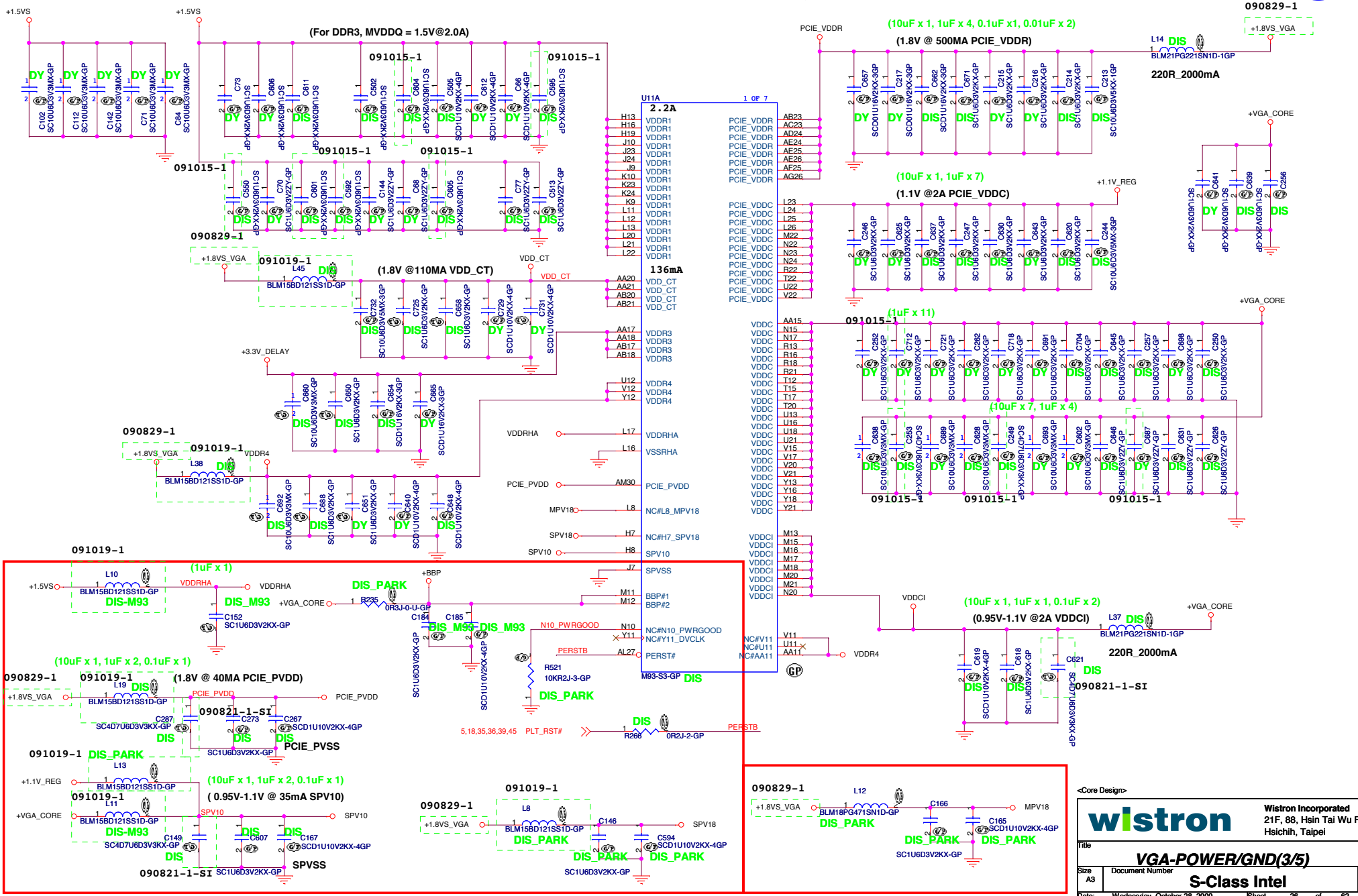
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: LCD/CRT/HDMI PORT(2/5)

Size: A2 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 25 of 62

M93 GPU(3/5)



<Core Design>

wistron

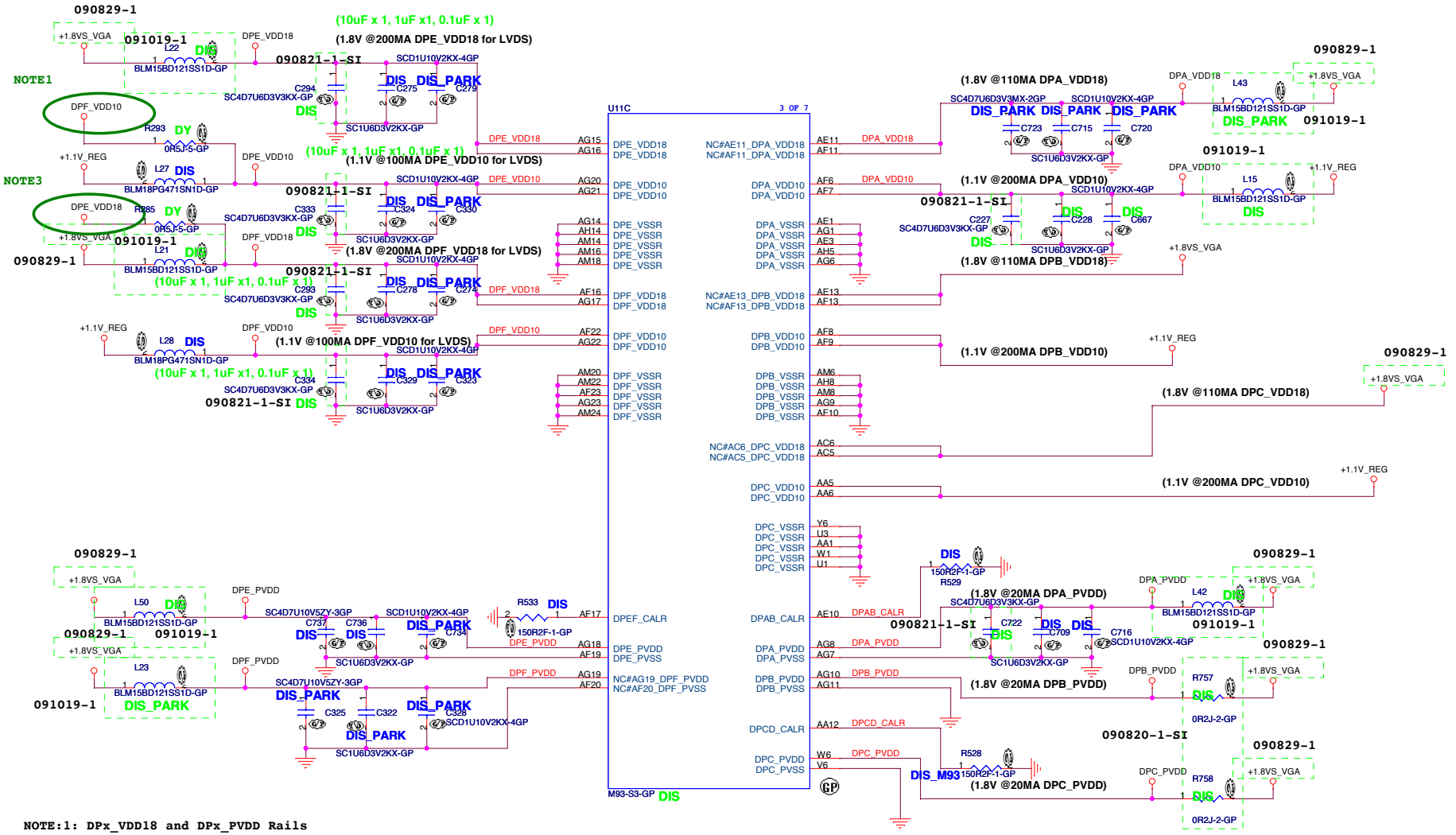
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: VGA-POWER/GND(3/5)

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 26 of 62

M93 GPU(4/5)



NOTE:1: DPx_VDD18 and DPx_PVDD Rails can be join together and remove Decoupling Capacitors and BEAD for DPx_PVDD if signal integrity for DP lanes are OK.

NOTE:2: DPA_VDD10 / DPB_VDD10 and DPE_VDD10 / DPF_VDD10 Rails can be join together and remove Decoupling Capacitors and BEADfor one rail of each pair if signal integrity for DP lanes are OK. We also need to Change BEAD to minimum 400mA rating.

NOTE:3: DPx_VDD18 Rails can be join together as shown in schematic for Dual -Link DVI or LVDS setting and remove DecouplingCapacitors and BEAD of any one rail of the pair if signal integrity for DP lanes are OK. We need at least 500mA Bead to supportjoin rails.

<Core Design>

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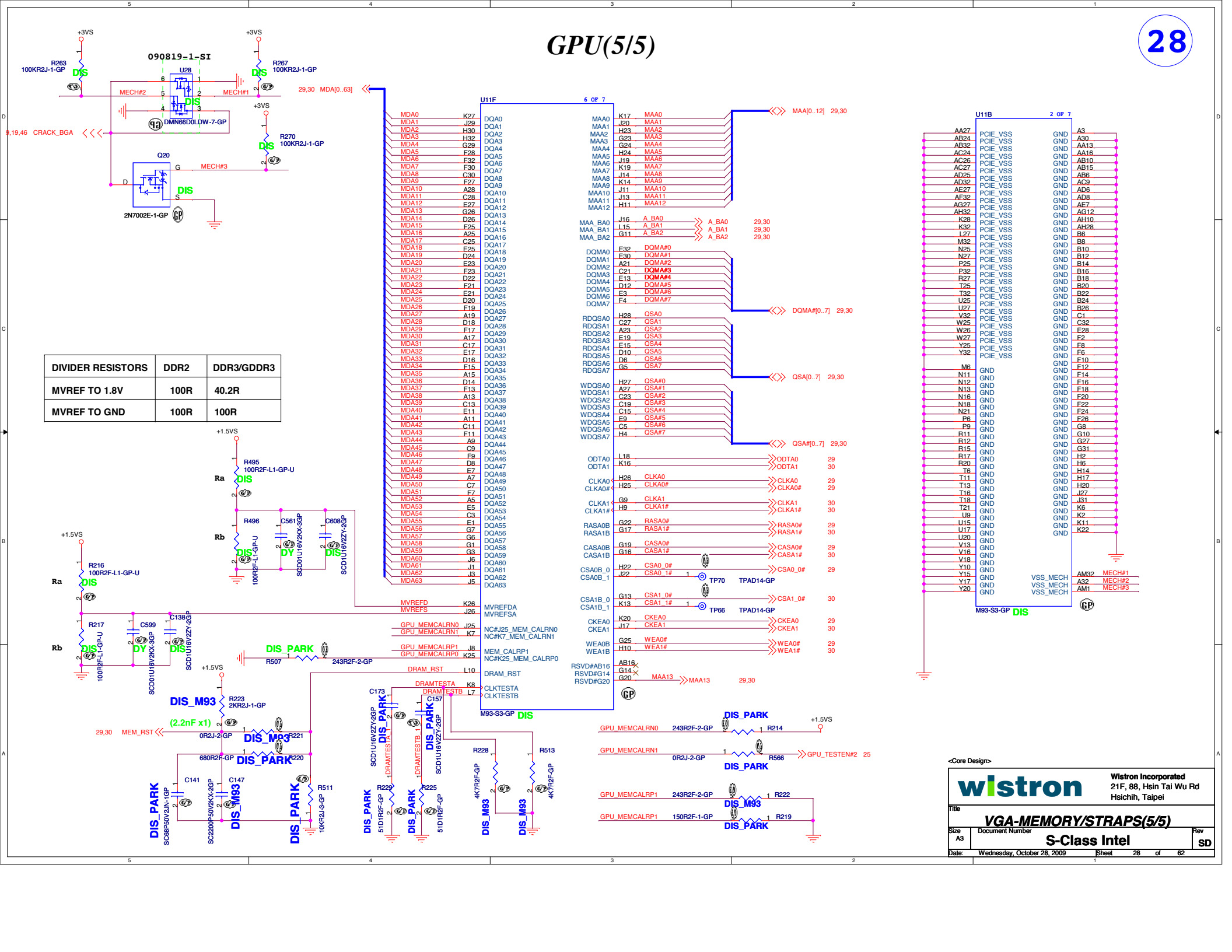
Title: VGA-POWER/GND(4/5)

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 27 of 62

GPU(5/5)

DIVIDER RESISTORS	DDR2	DDR3/GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: VGA-MEMORY/STRAPS(5/5)

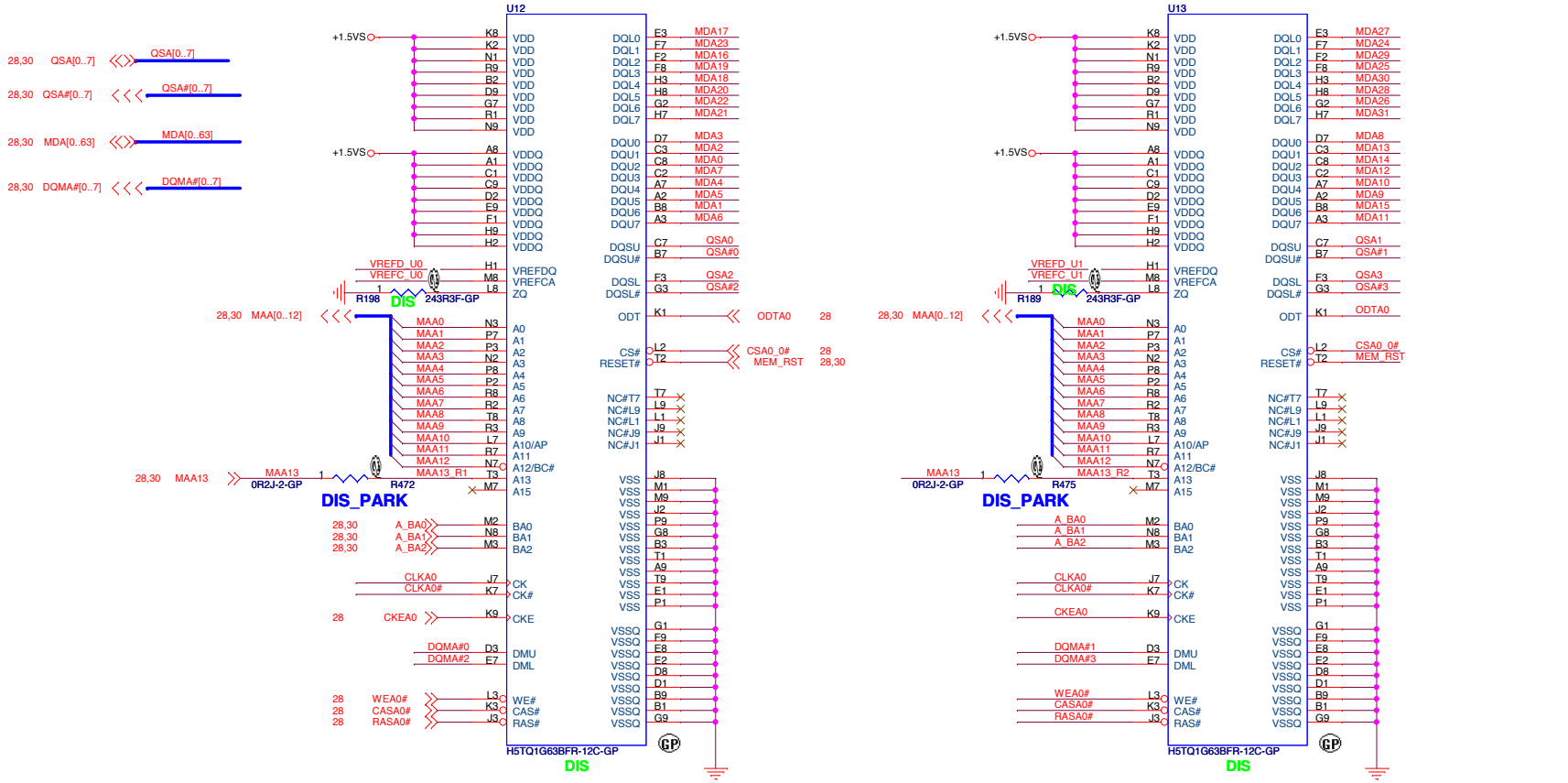
Size: A3 | Document Number: S-Class Intel | Rev: SD

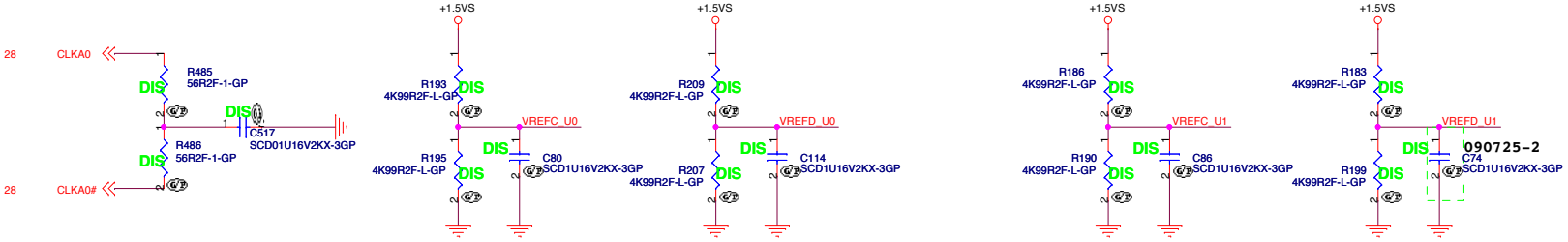
Date: Wednesday, October 28, 2009 | Sheet 28 of 62

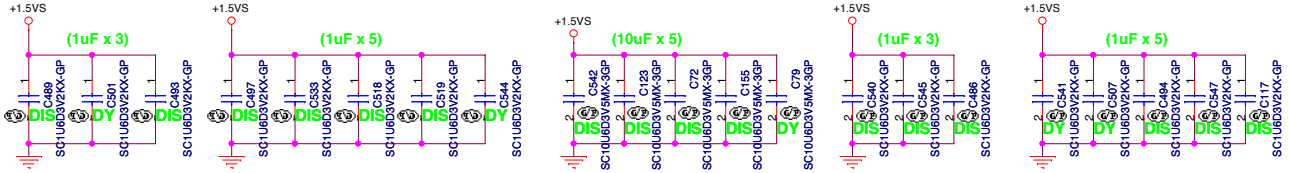
VRAM DDR3 (1/2)

256MB/512MB DDR3

29







<Core Design>

wistron

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Hsichih, Taipei

Title: VGA-MEMORY/STRAPS(2/4)

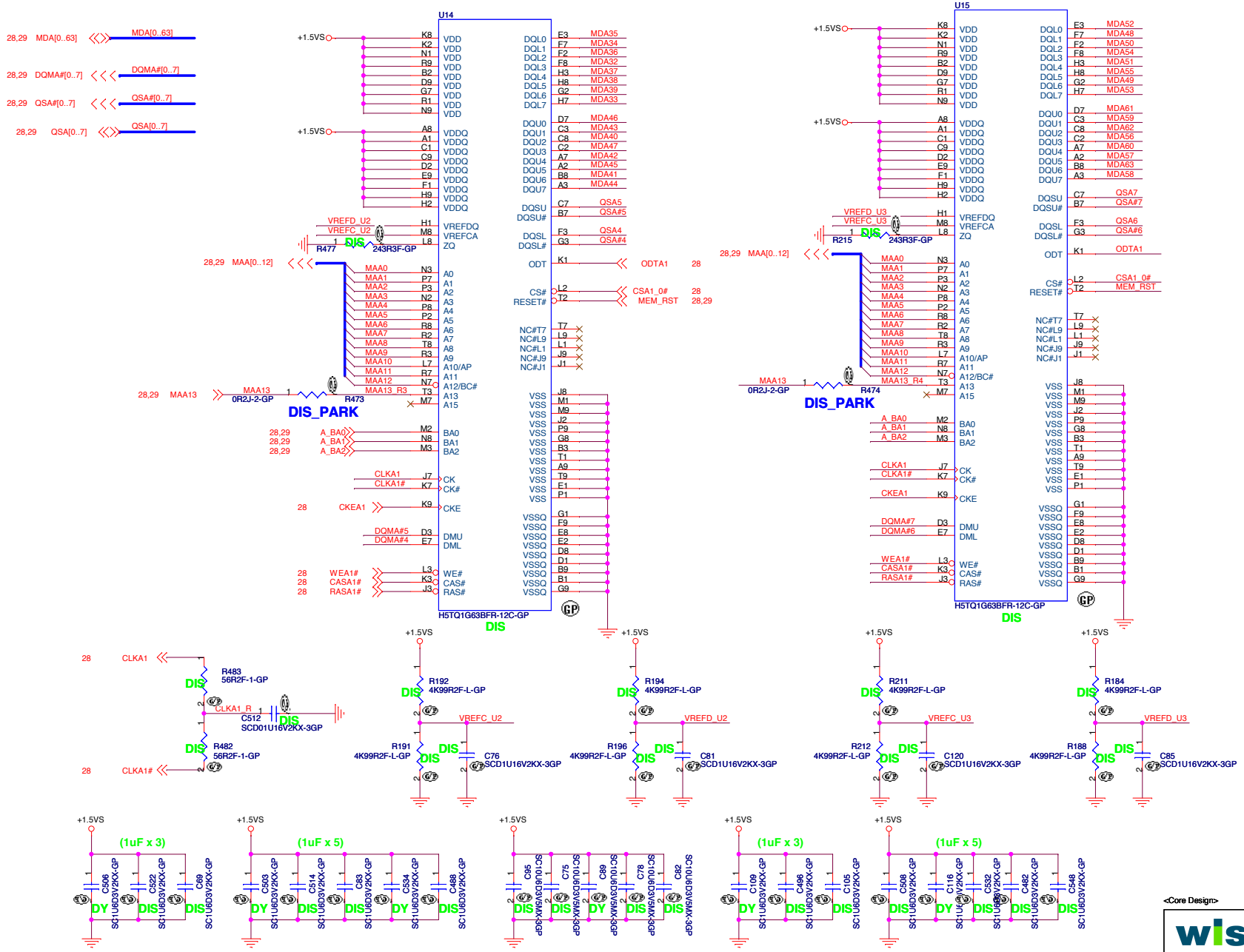
Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 29 of 62

VRAM DDR3 (2/2)

256MB/512MB DDR3

30



<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

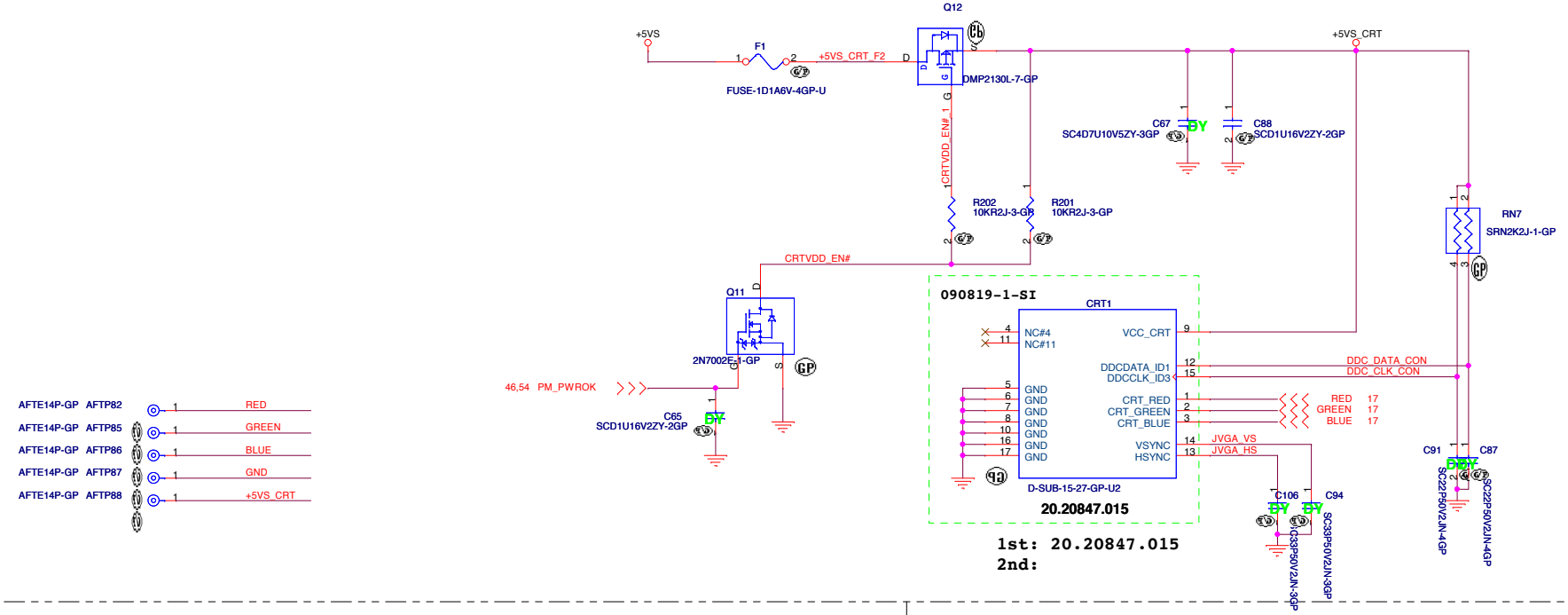
Title: VGA-MEMORY/STRAPS(4/4)

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 30 of 62

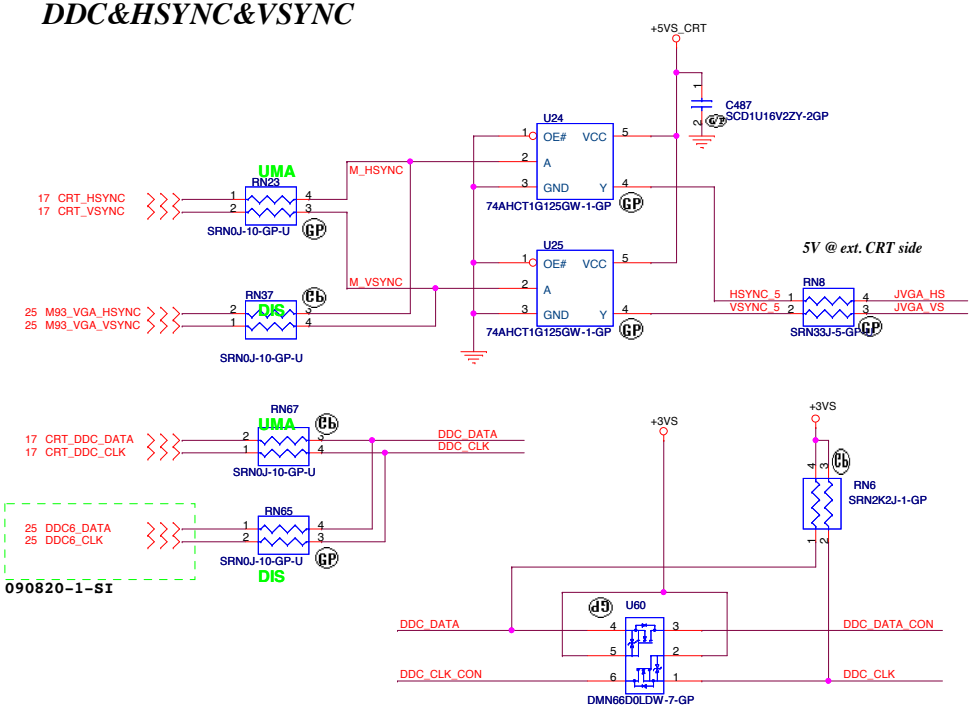
CRT I/F & CONNECTOR

31

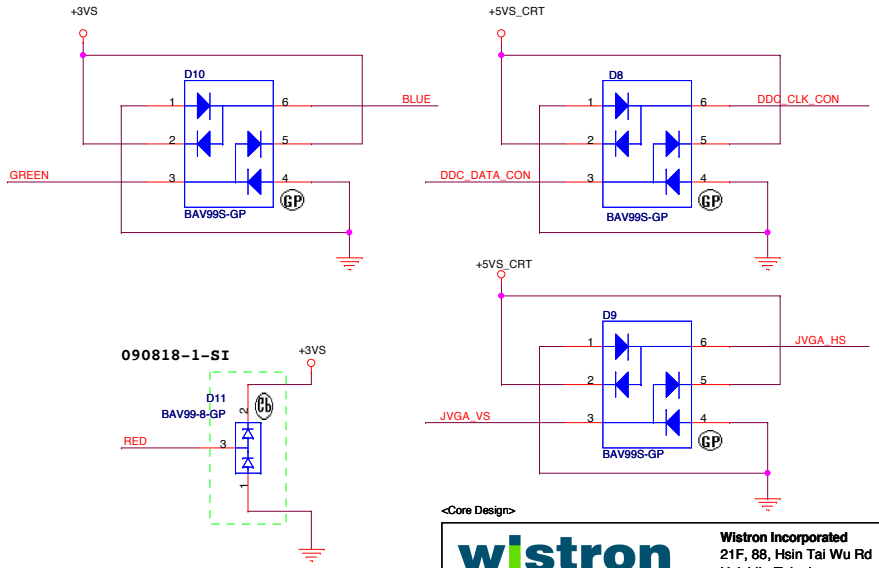


1st: 20.20847.015
2nd:

DDC&HSYNC&VSYNC



ESD



<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

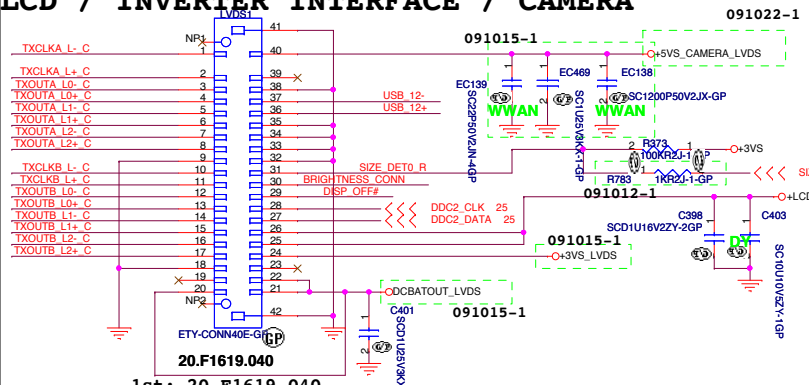
Title: CRT Connector

Size: A3 | Document Number: S-Class Intel | Rev: SD

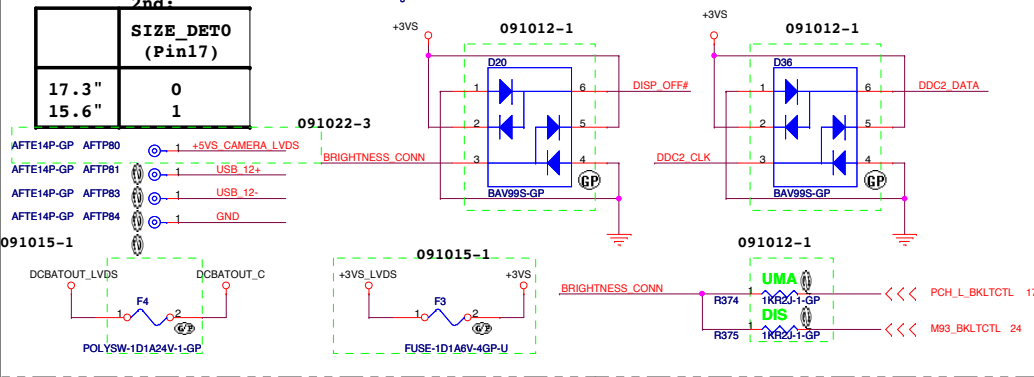
Date: Wednesday, October 28, 2009 | Sheet 31 of 62

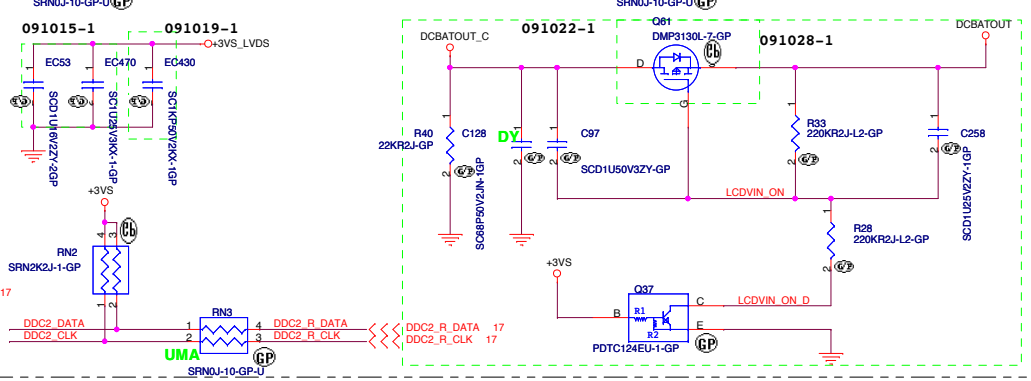
LVDS CONNECTOR

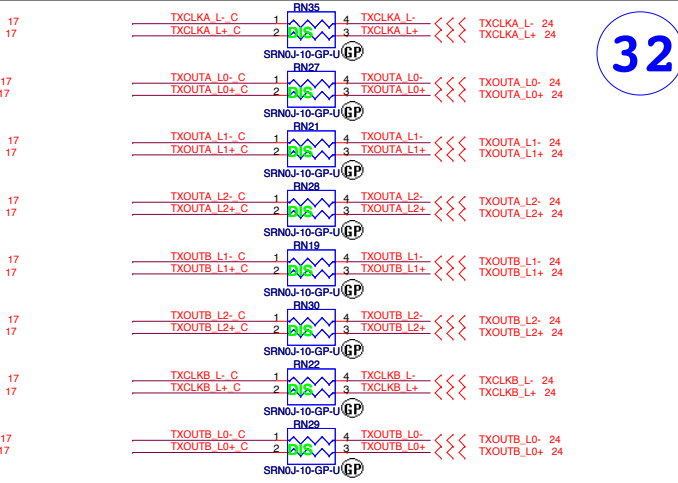
LCD / INVERTER INTERFACE / CAMERA



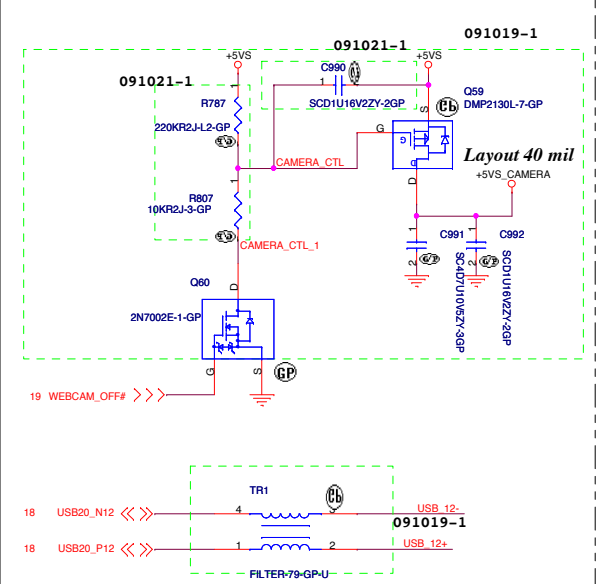
	SIZE_DET0 (Pin17)
17.3"	0
15.6"	1



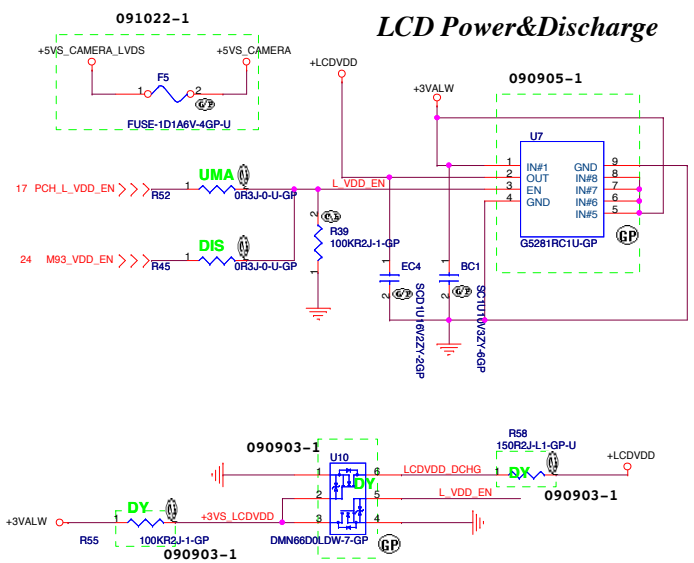


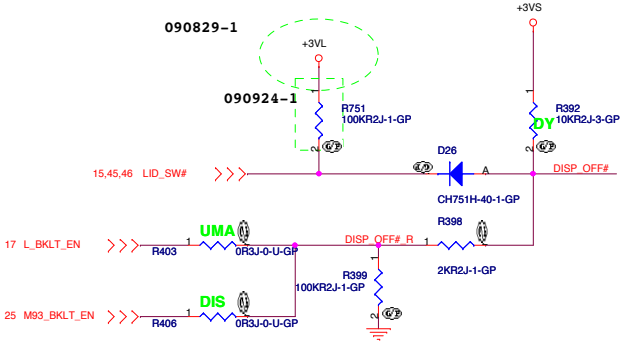


Camera Power&Interface



LCD Power&Discharge





<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: LCD/Inverter Connector/CAM/LED

Size: Custom | Document Number: S-Class Intel | Rev: SD

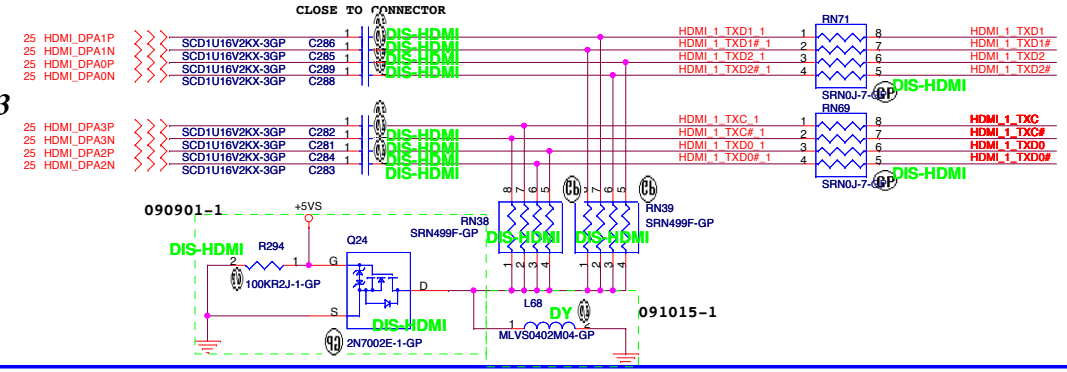
Date: Wednesday, October 28, 2009 | Sheet 32 of 62

HDMI CONNECTOR

33

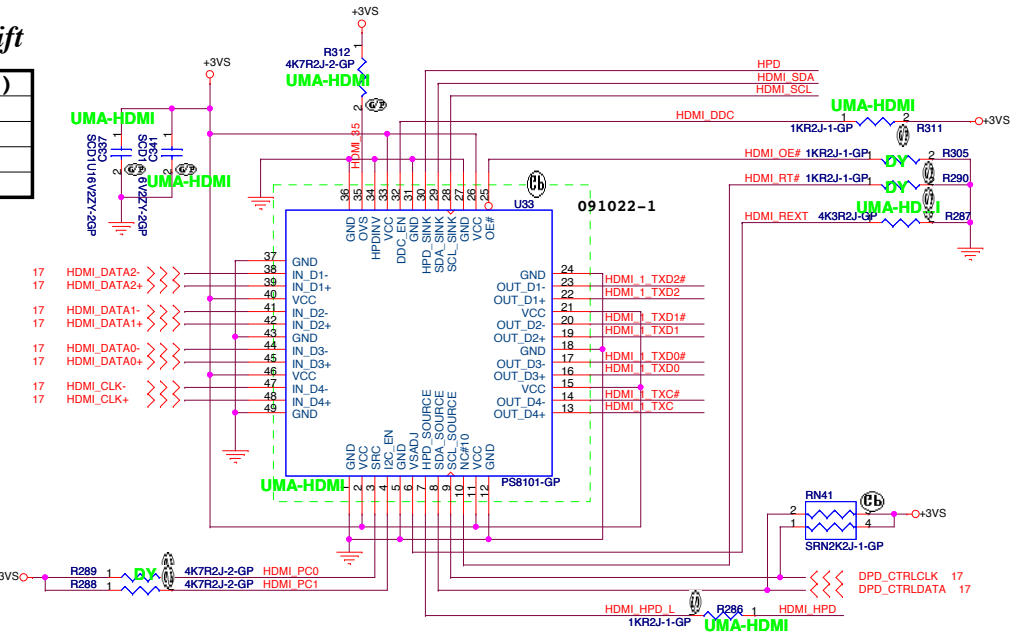
M93

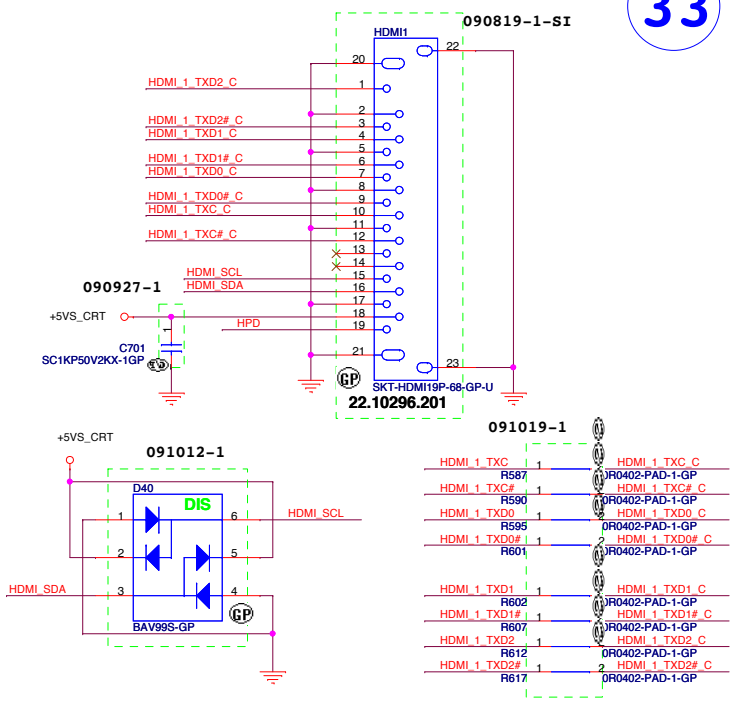
PLACE AC CAPS CLOSE TO CONNECTOR



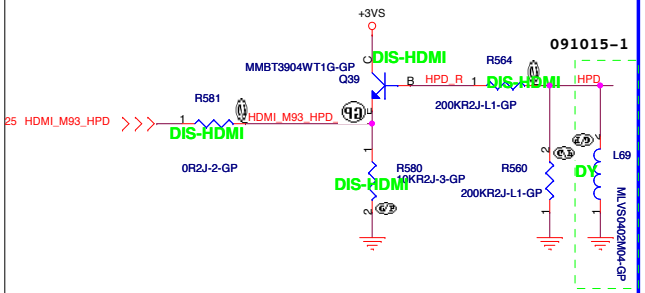
PCH Level Shift

PC1	PC0	(dB)
0	0	8
0	1	4
1	0	12
1	1	0

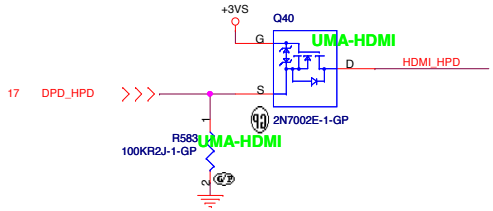




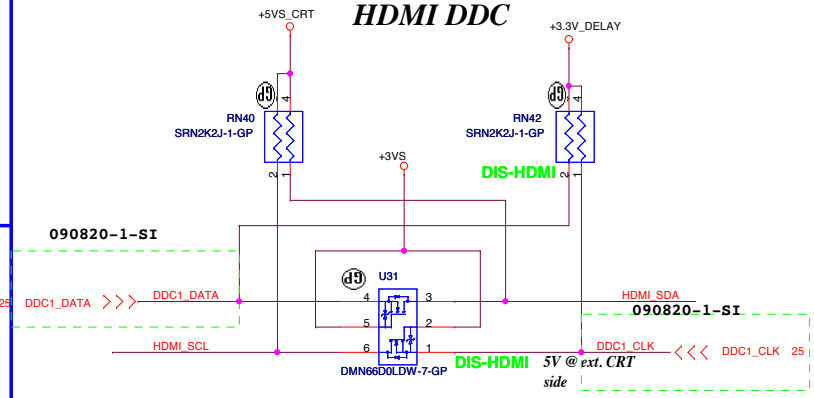
DIS HPD



UMA HPD



HDMI DDC



<Core Design>

wistron

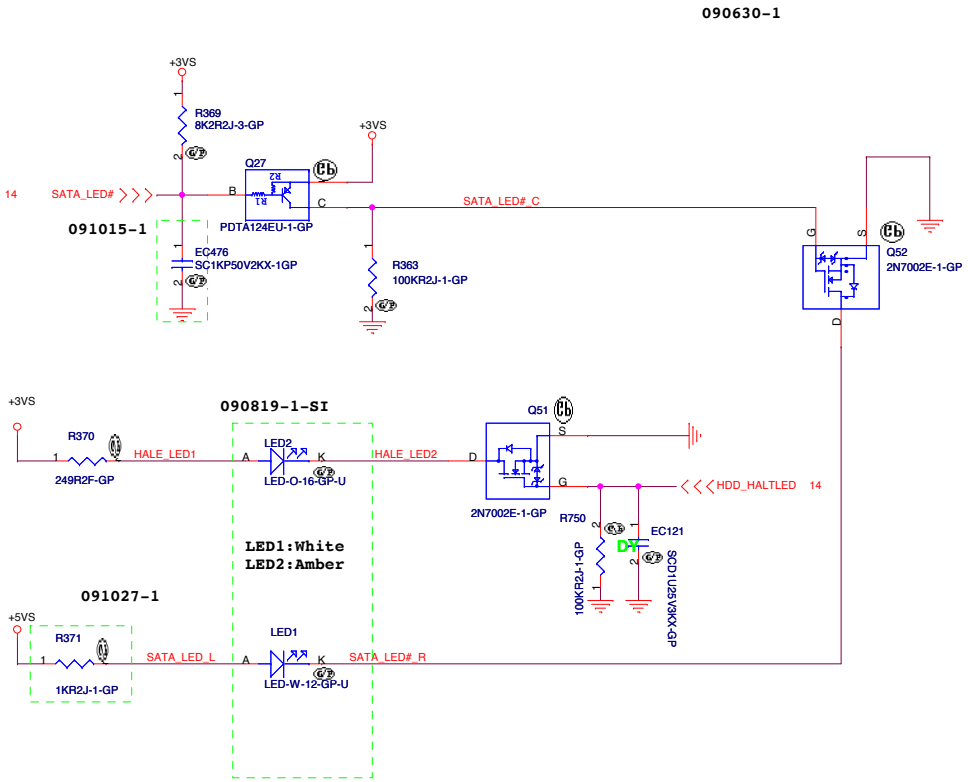
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: HDMI CONN.

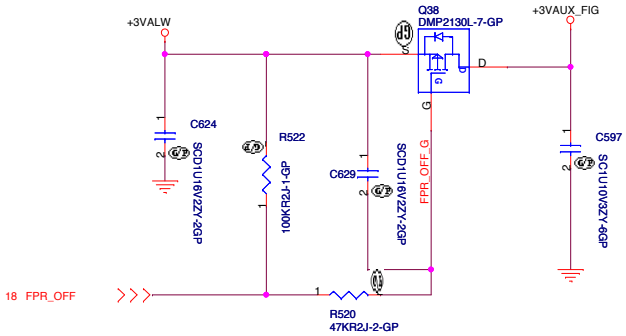
Size: A3 | Document Number: S-Class Intel | Rev: SD

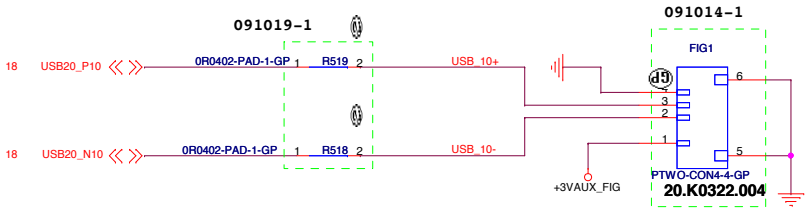
Date: Wednesday, October 28, 2009 | Sheet 33 of 62

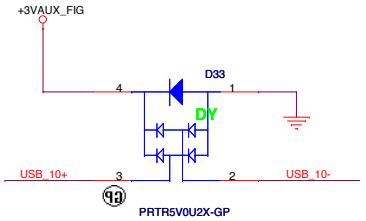
SATA LED FOR HDD

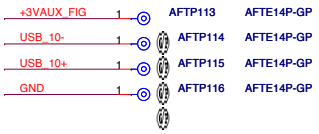


Fingerprint









<Core Design>

wistron

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: SATA&CAP LED&GOLDEN FINGER

Size: A3 | Document Number: S-Class Intel | Rev: SD

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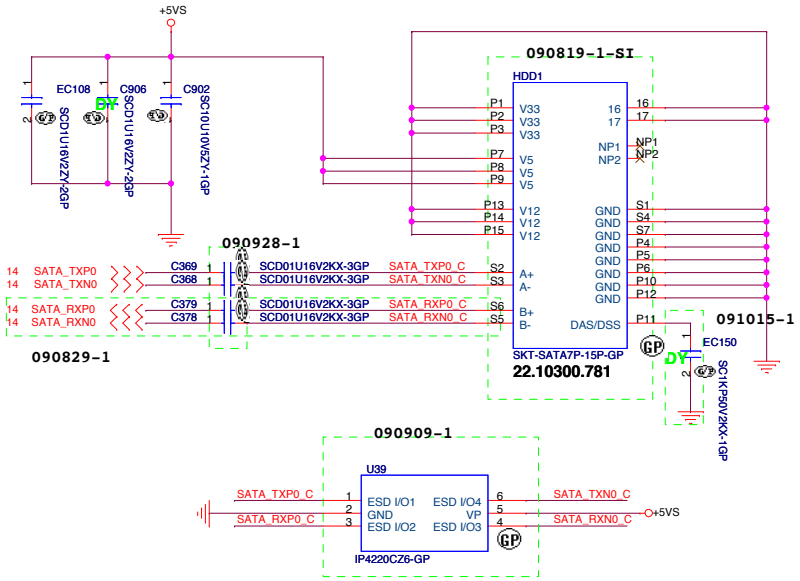
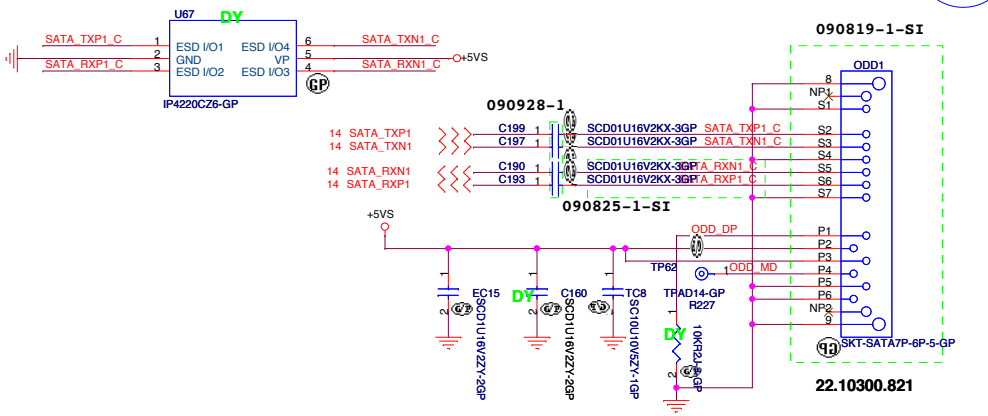
SATA HD Connector

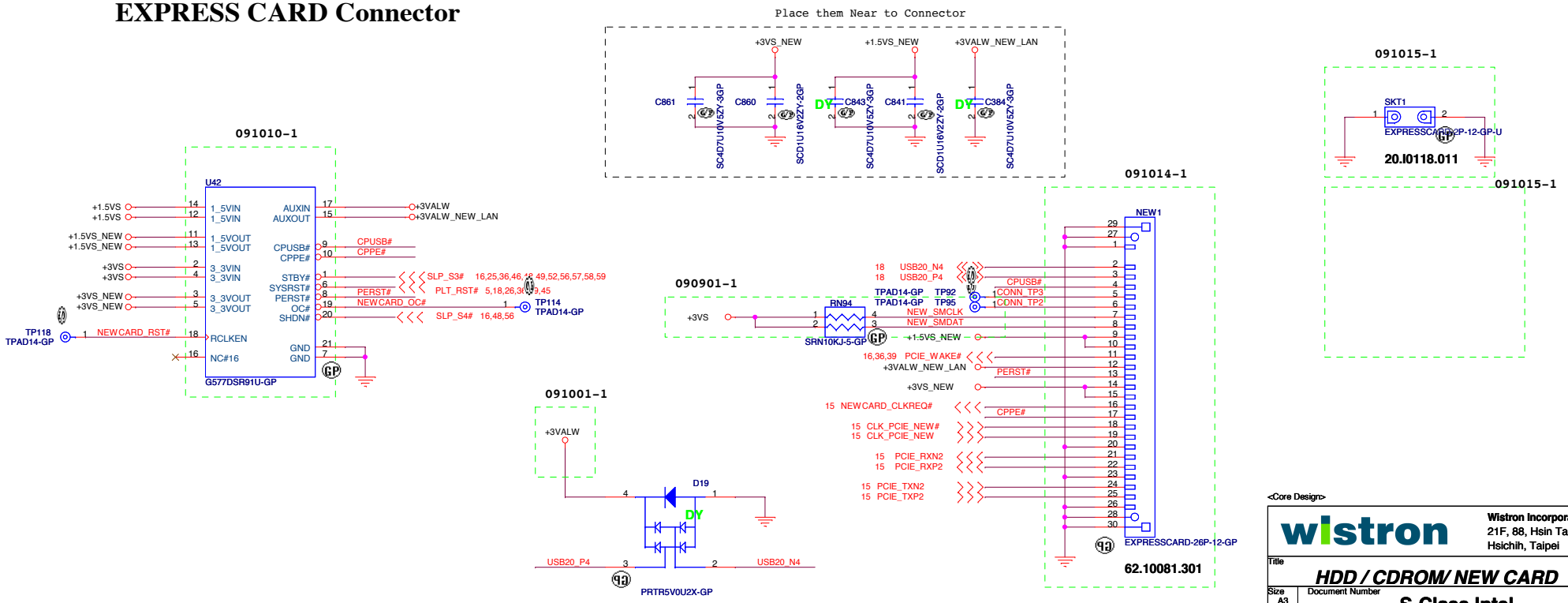


ODD Connector



35

EXPRESS CARD Connector



<Core Design>

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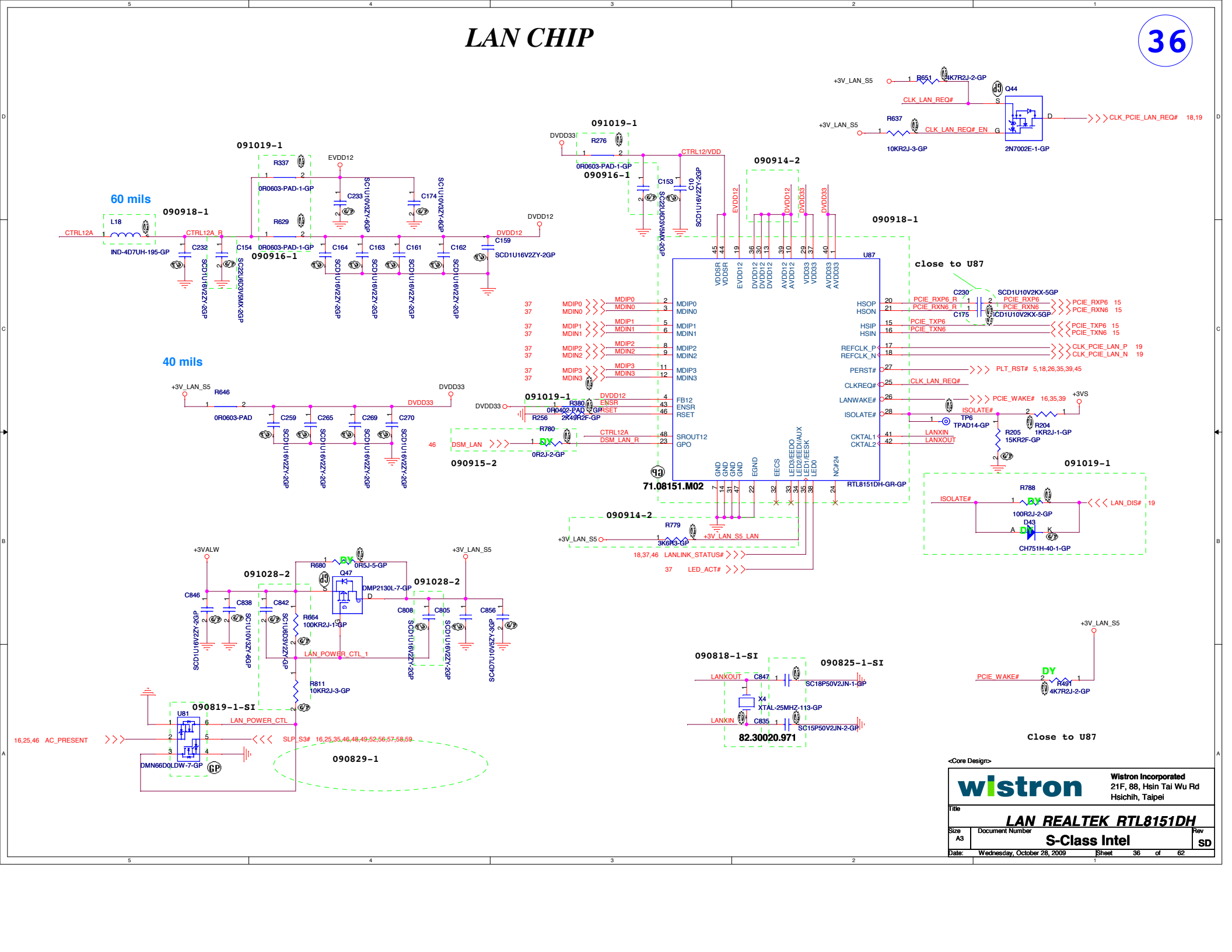
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: HDD / CDROM/ NEW CARD

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 35 of 62

LAN CHIP



<Core Design>

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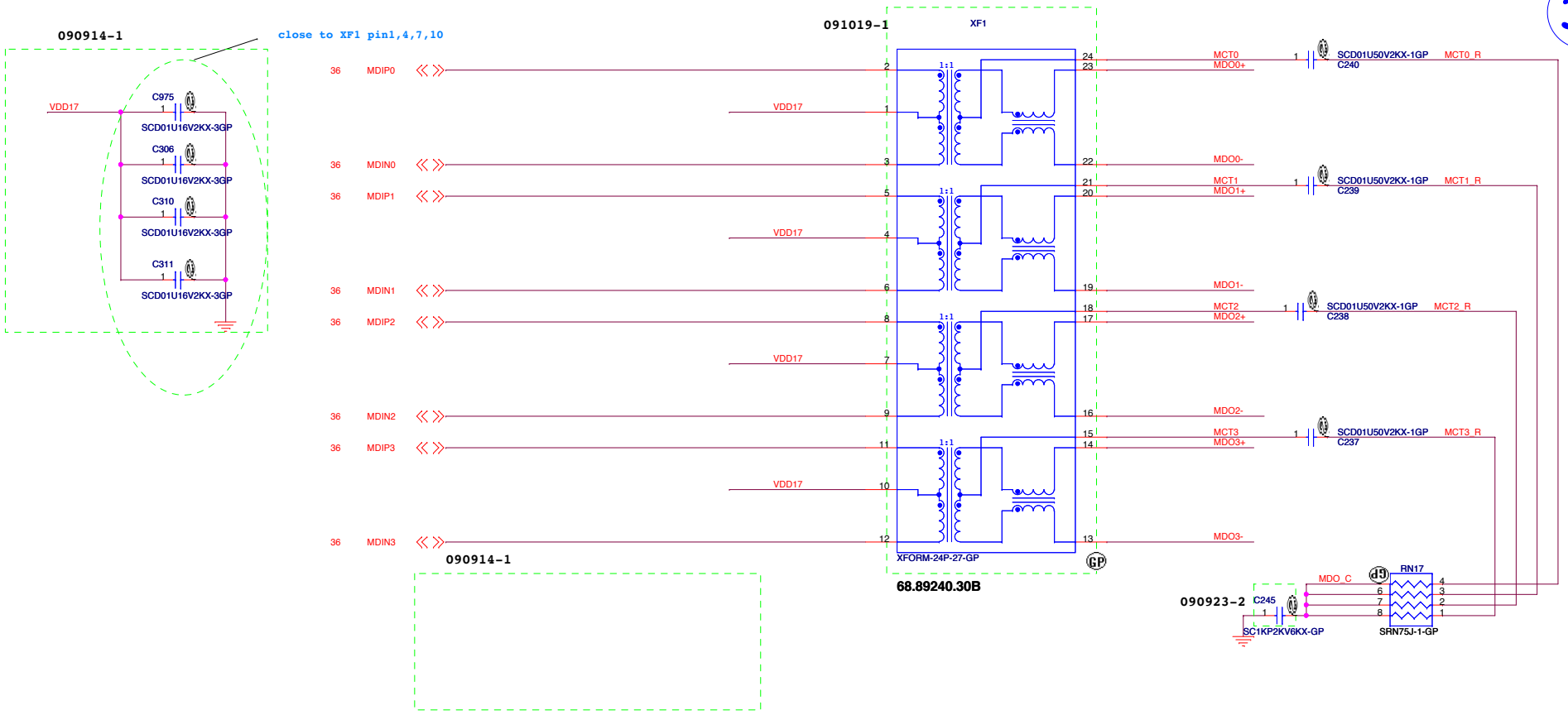
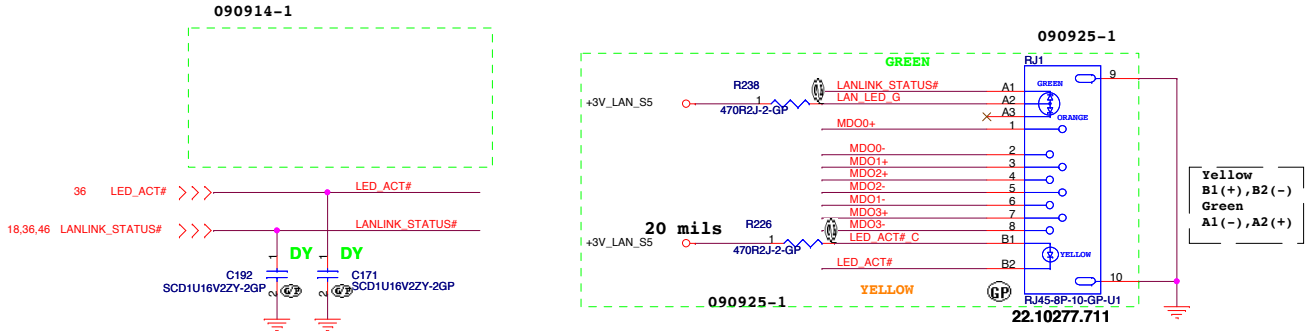
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: LAN REALTEK RTL8151DH

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 36 of 62





IF NOT OVER CLOCKING, LED_ACT# WILL ACT HIGH

Check LAN chip for LED_ACT# function on RJ45 connector pin define.

<Core Design>

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Wistron Incorporated
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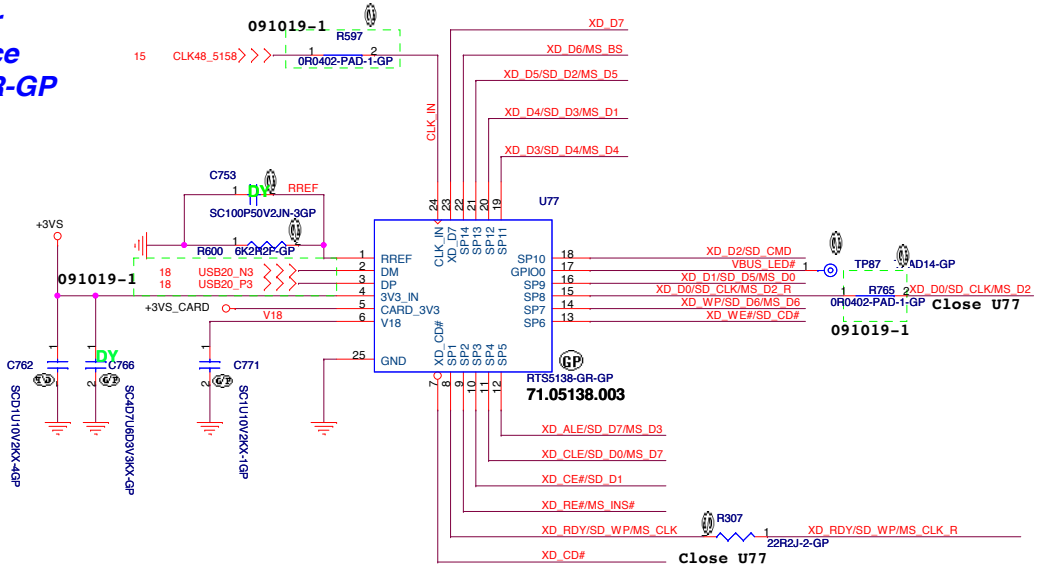
Hsichih, Taipei

Title: Magnetic & RJ45

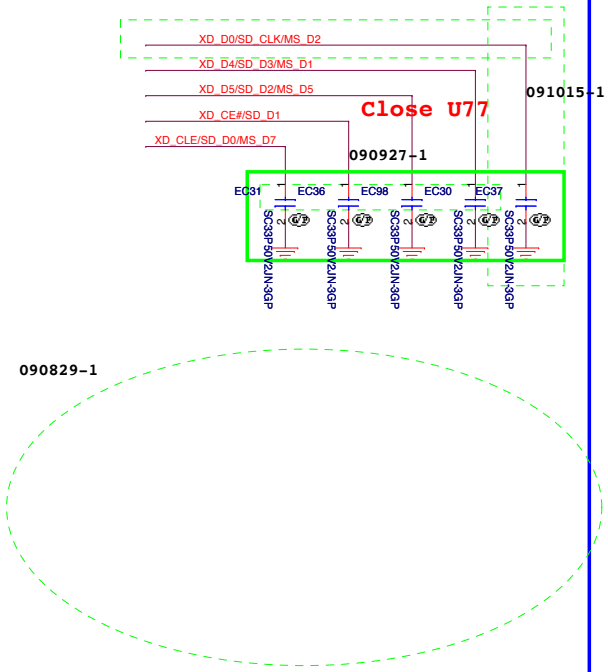
Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 37 of 62

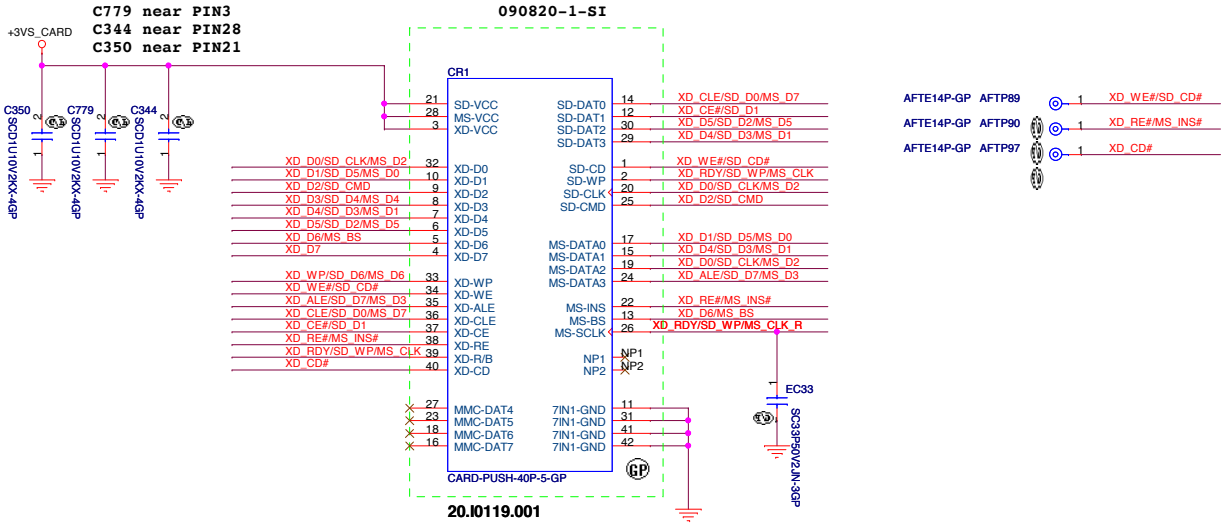
Card Reader
USB Interface
RTS5138-GR-GP



EMI Reserve Cap



4 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)



<Core Design>

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Hsichih, Taipei

Title: CardReader RTS5138

Size	Document Number	Rev
A3	S-Class Intel	SD

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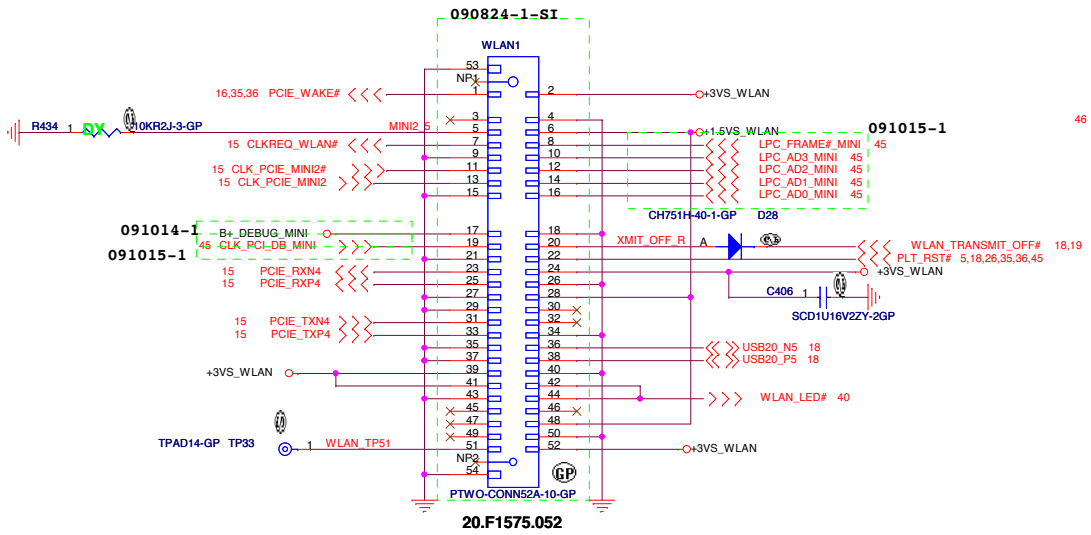
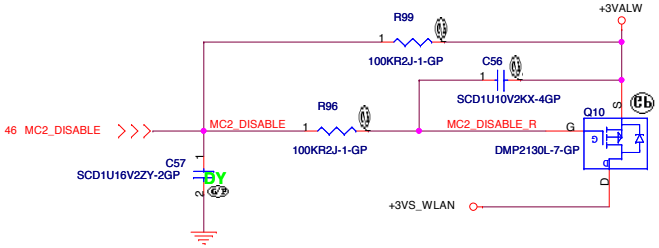
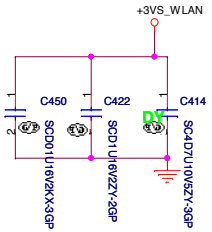
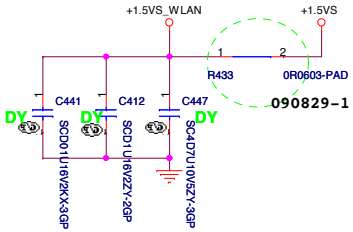
Mini-Card--WLAN

Half minicard

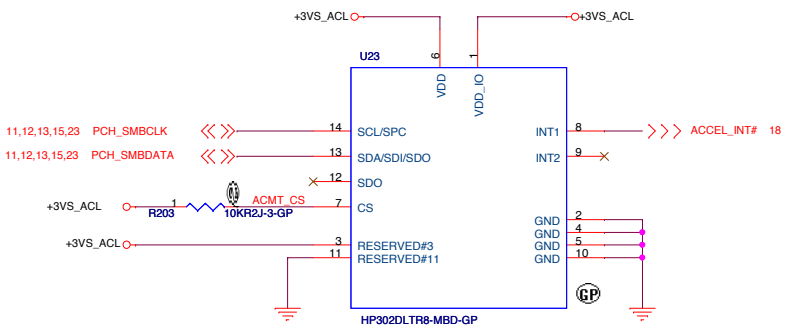


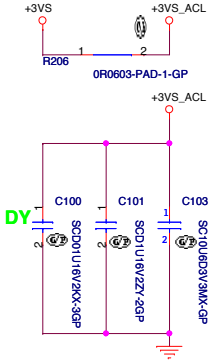






ACCELEROMETER





<Core Design>

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Wistron Incorporated
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Hsichih, Taipei

Title: Mini-Card/Accelerometer

Size: A3 | Document Number: S-Class Intel | Rev: SD

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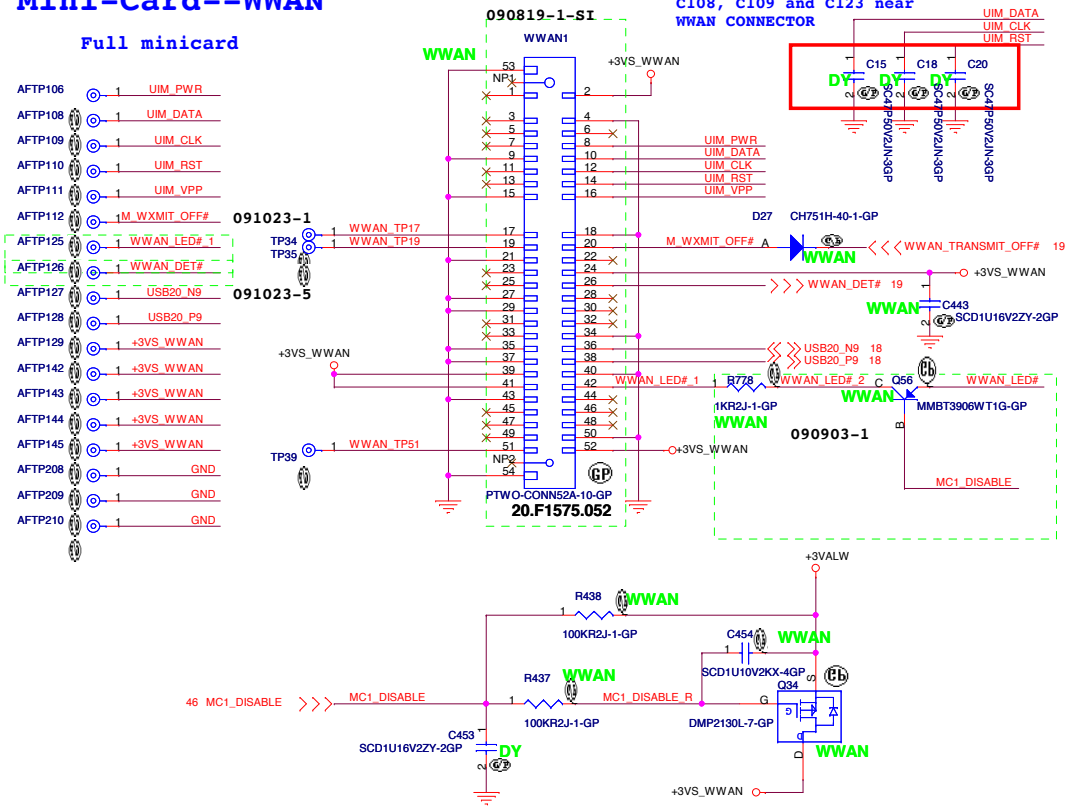
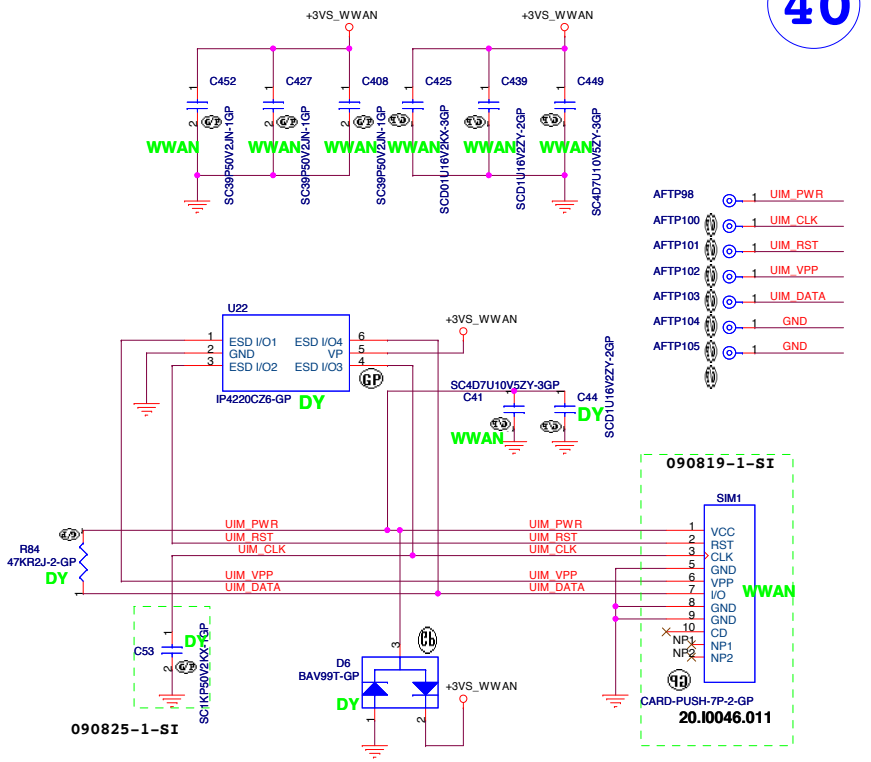
Mini-Card--WWAN

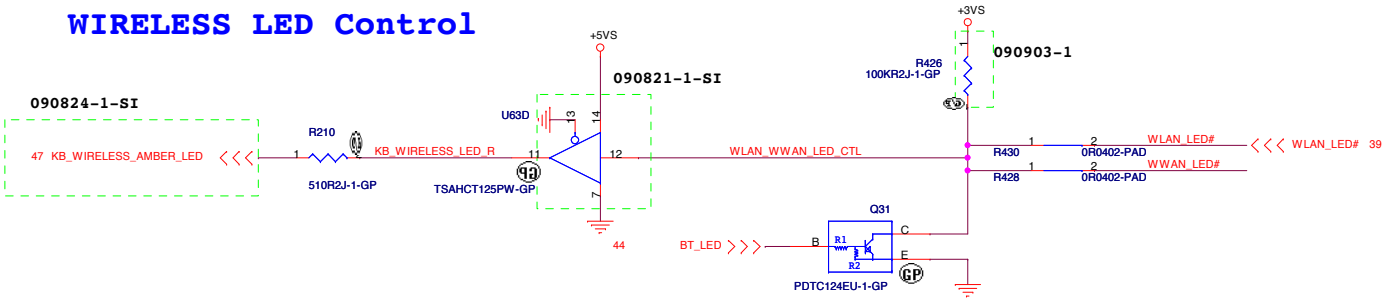
Full minicard

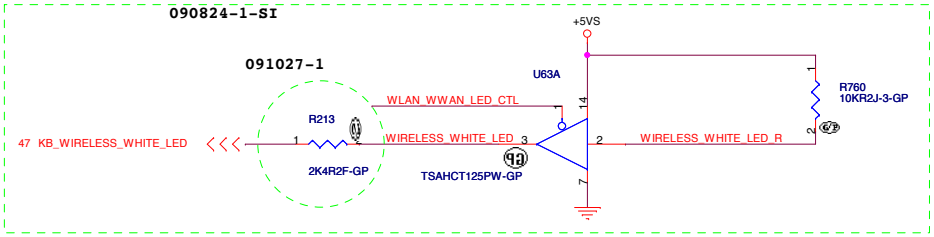


SIM Card Slot



WIRELESS LED Control





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Hsichih, Taipei

Title: Mini-Card/Accelerometer

Size: A3 | Document Number: S-Class Intel | Rev: SD

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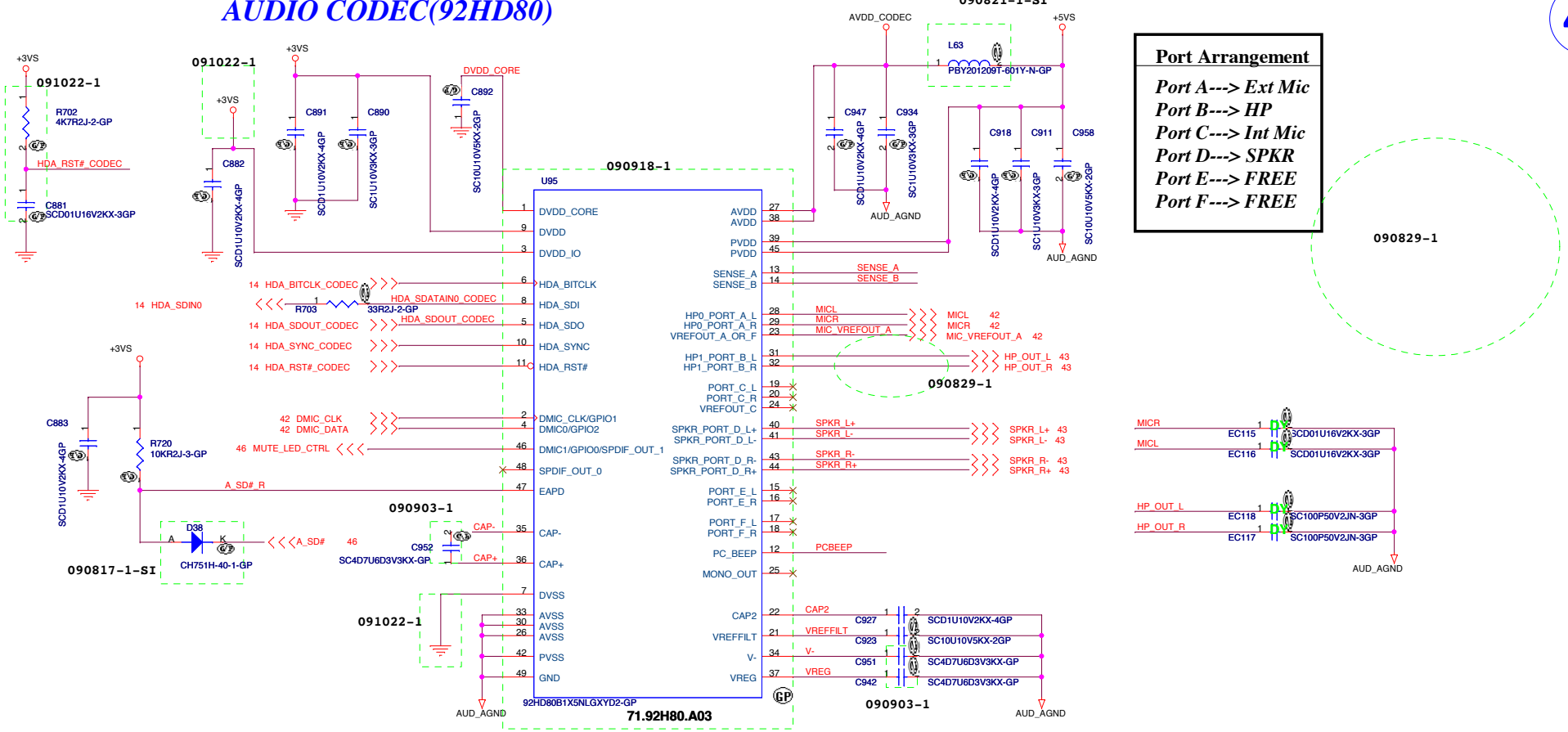
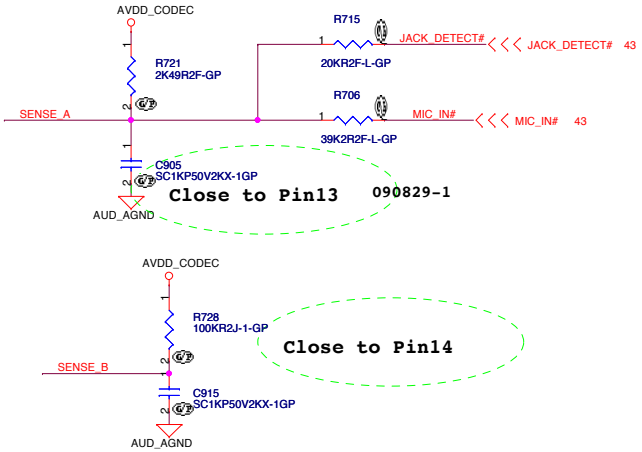
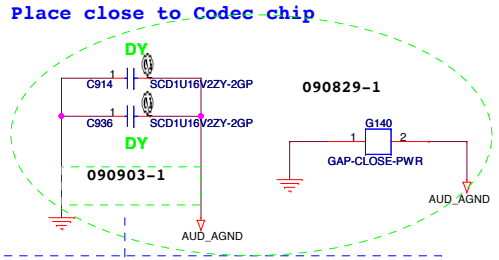
AUDIO CODEC(92HD80)



SENSE Detect

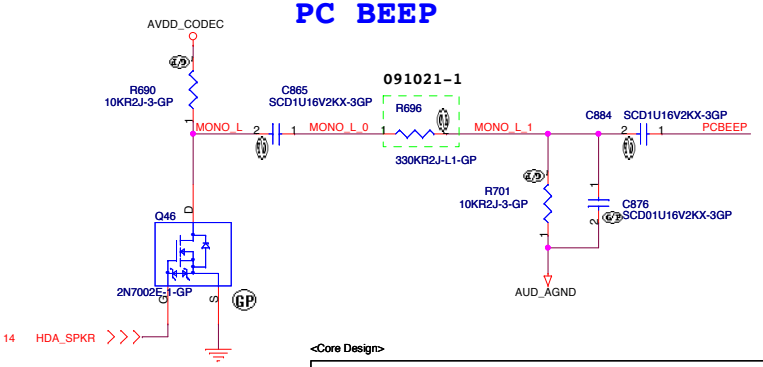


Digital GND & AUD_AGND



audio ground must be connect to digital ground with an 80 mil copper bridge located directly under codec to prevent ESD latch up.

PC BEEP



<Core Design>

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Hsichih, Taipei

Title: AUDIO 92HD80 / OP AMP

Size	Document Number	Rev
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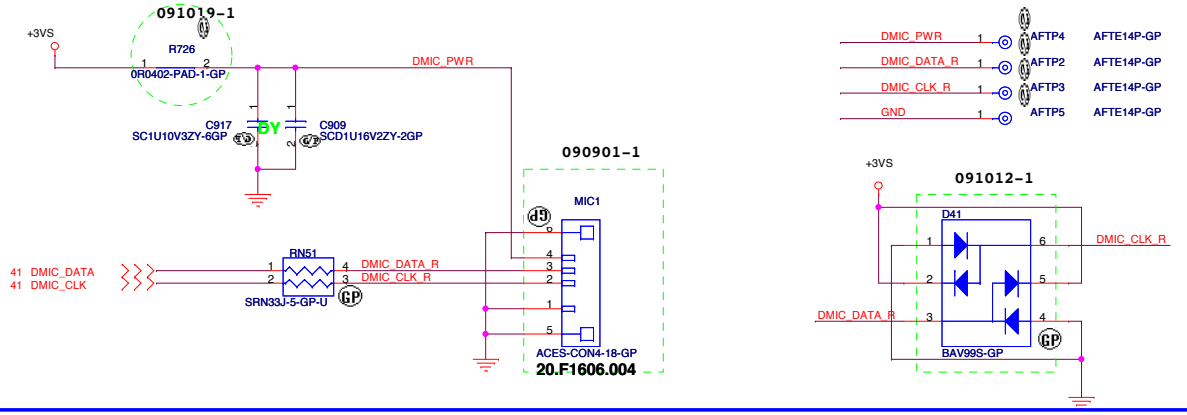
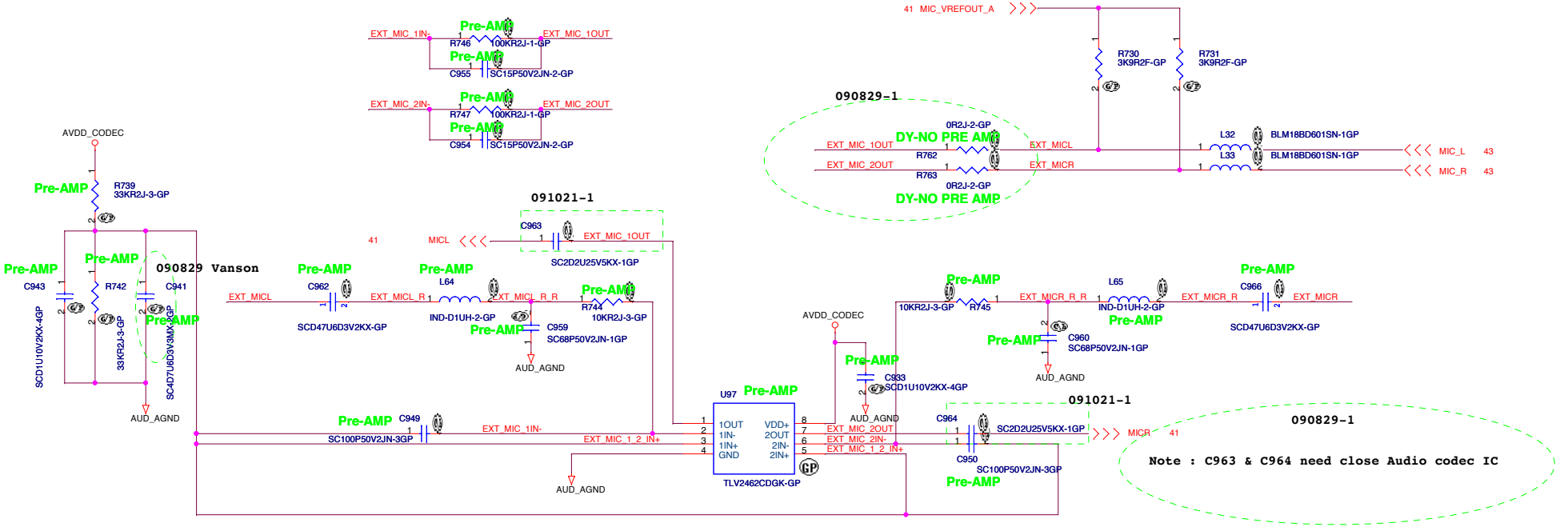
Internal Digital MIC



Ppre-AMP. for External MIC



<Core Design>

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Hsichih, Taipei

Title: AUDIO Pre-AMP / CONN

Size	Document Number	Rev
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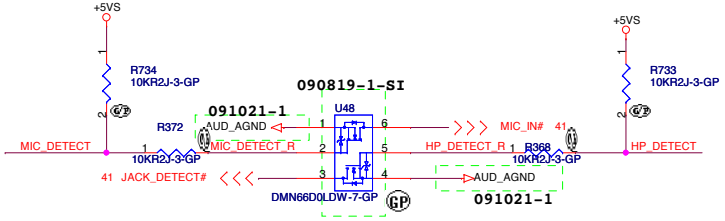
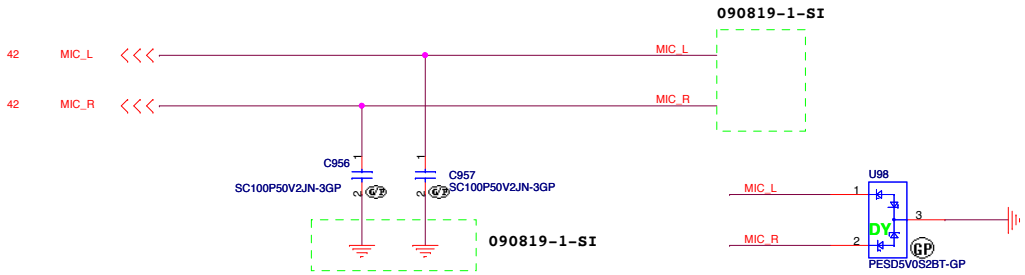
Jack Detect



MIC IN



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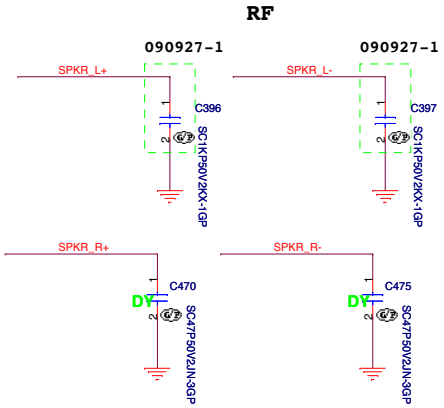
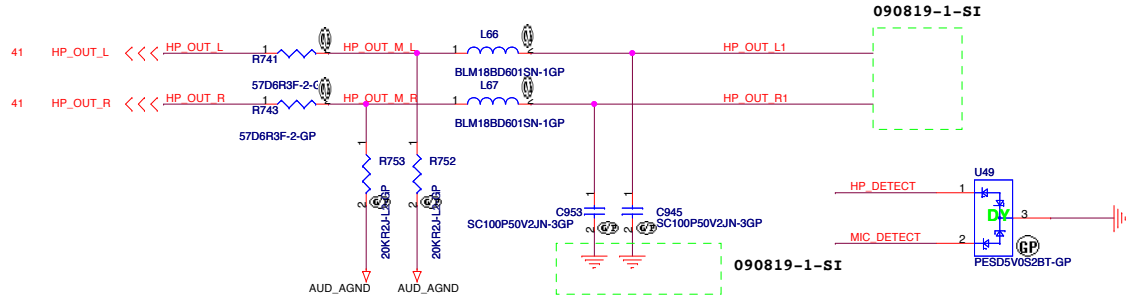
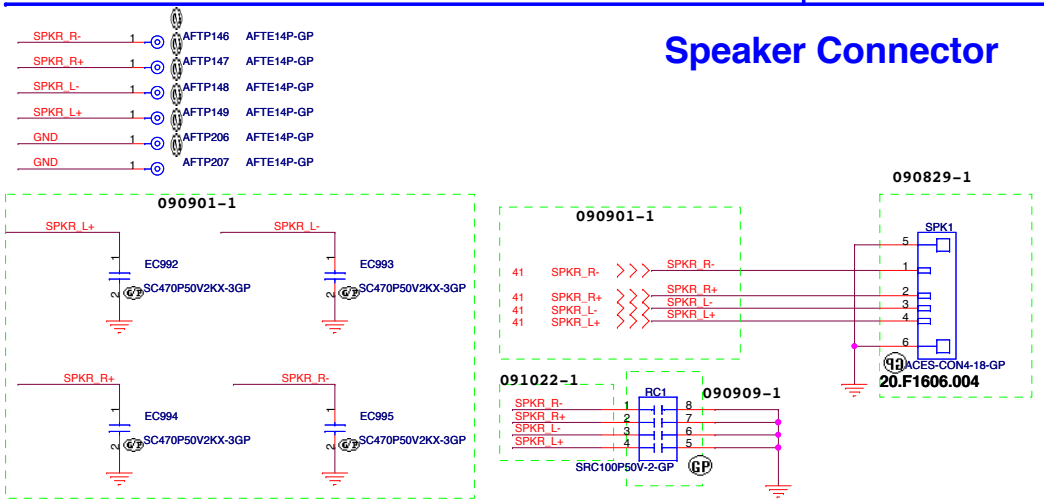
RF Reserver Cap



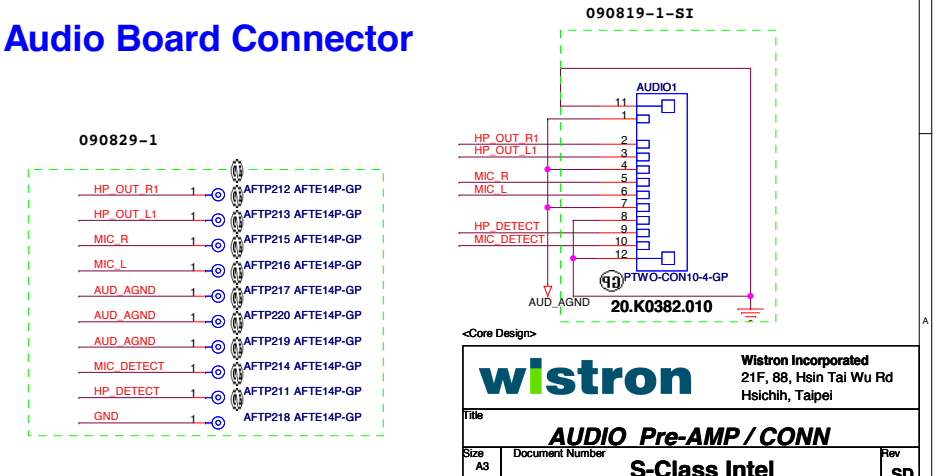
HeadPhone OUT



Speaker Connector



Audio Board Connector



<Core Design>

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Hsichih, Taipei

Title: AUDIO Pre-AMP / CONN

Size: A3 | Document Number: S-Class Intel | Rev: SD

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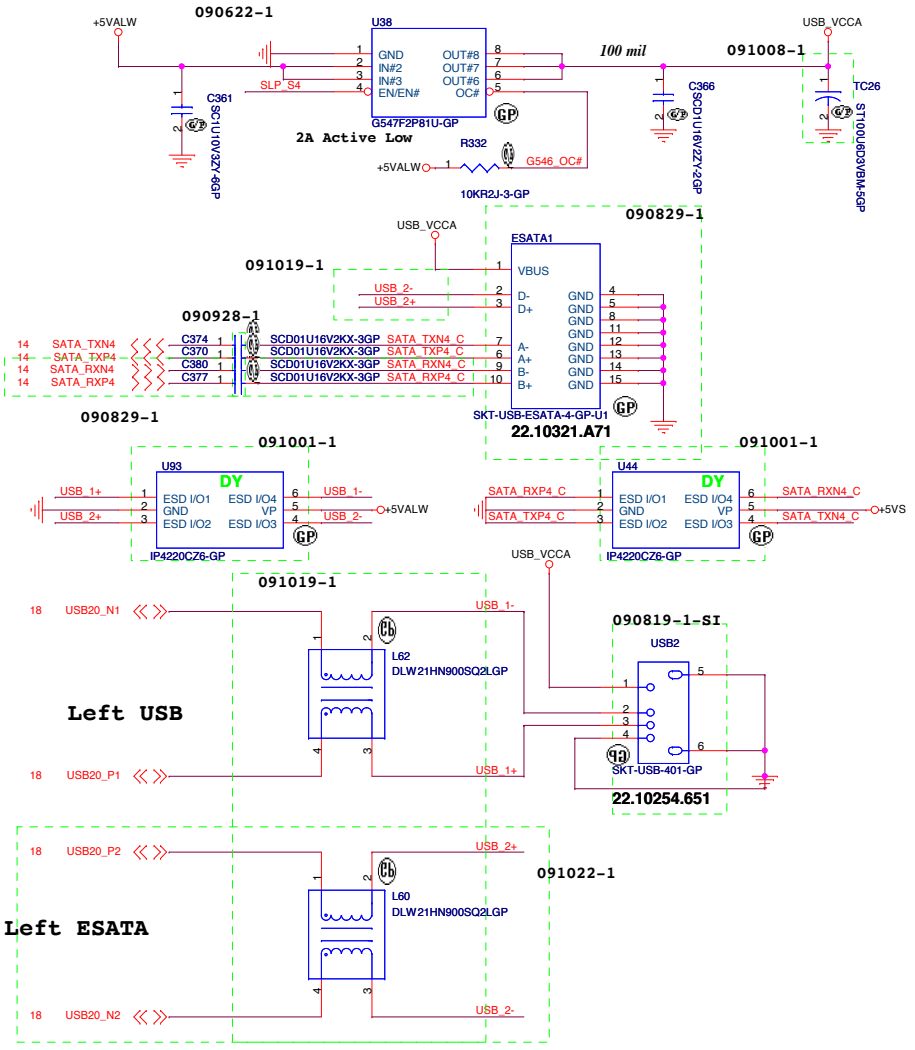
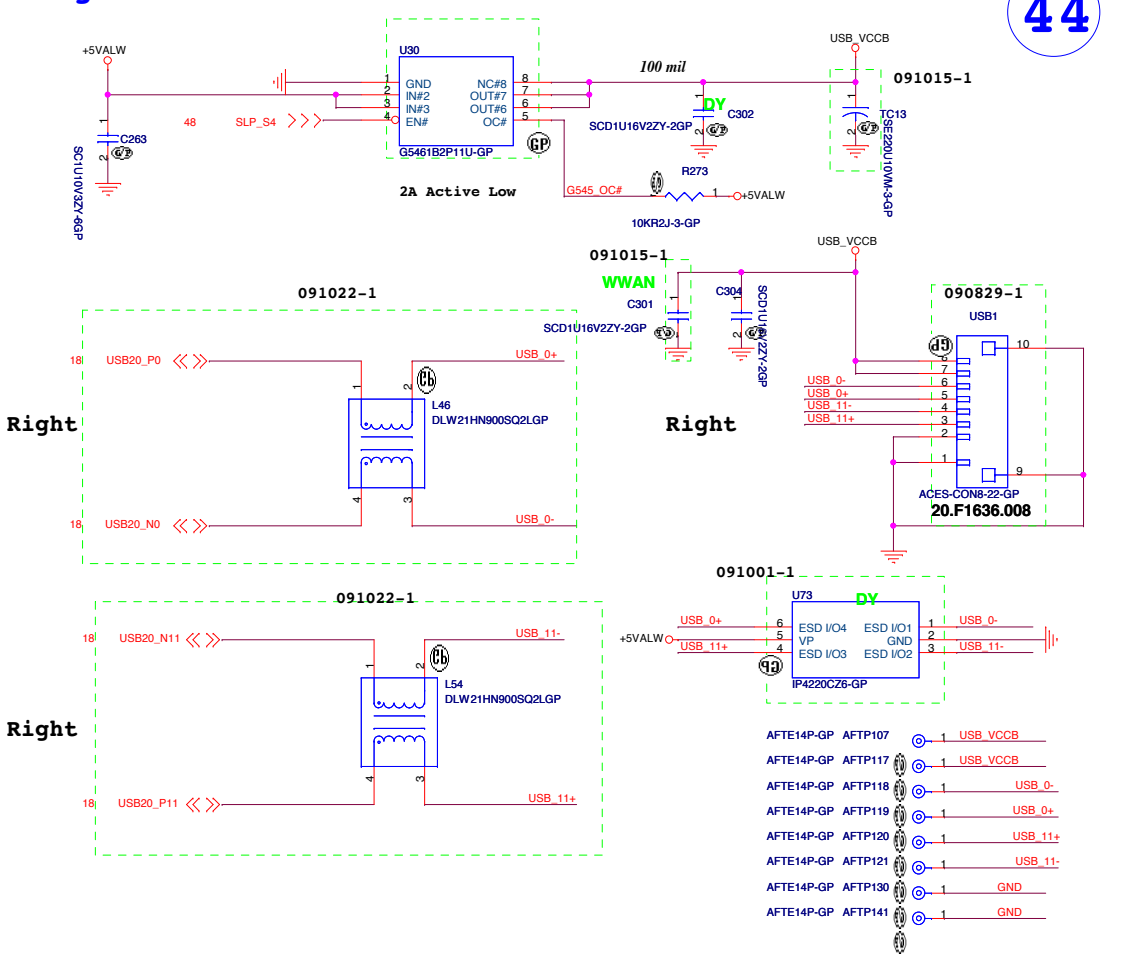
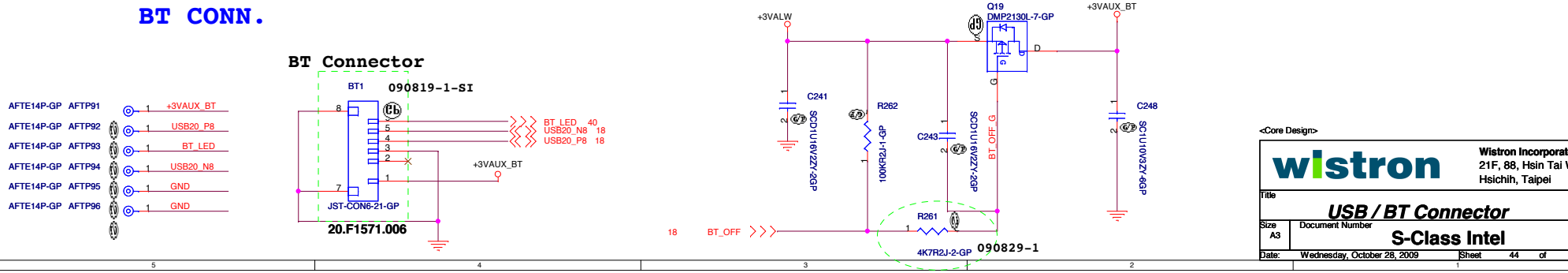
Left Side USB + ESATA Port



Right Side USB x 2



BT CONN.



<Core Design>

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Hsichih, Taipei

Title: USB / BT Connector

Size: A3 | Document Number: S-Class Intel | Rev: SD

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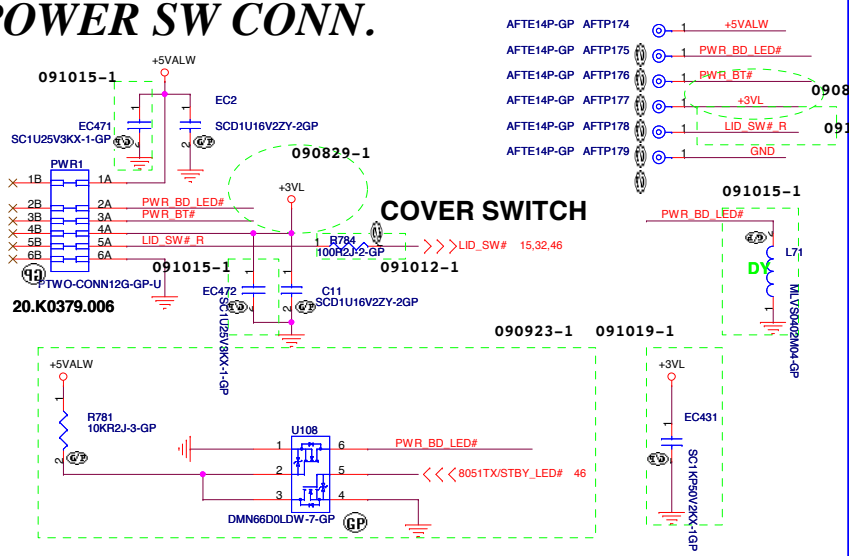
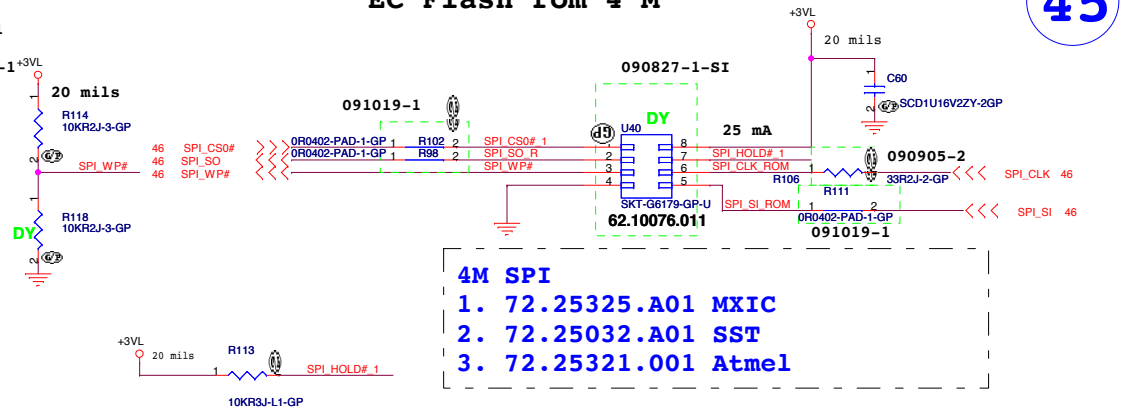
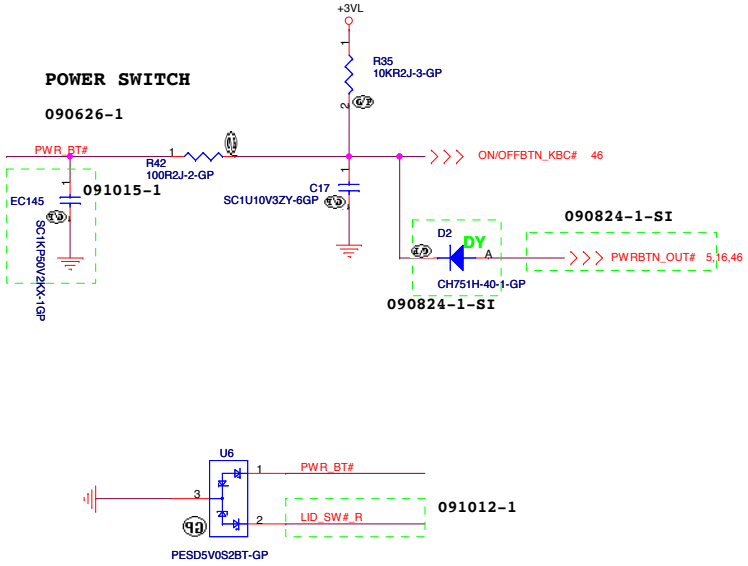
POWER SW CONN.



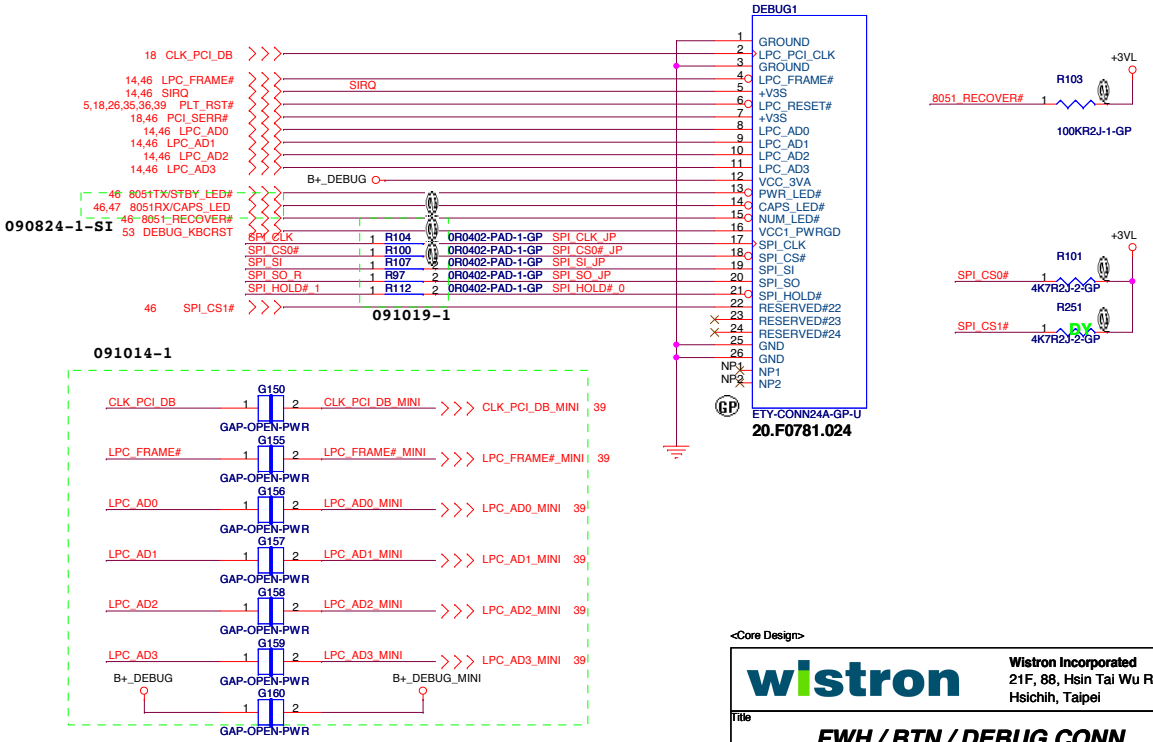
EC Flash rom 4 M



Power SW Circuit



24 PIN LPC DEBUG CONN.



<Core Design>

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Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: FWH / BTN / DEBUG CONN.

Size: A3 | Document Number: S-Class Intel | Rev: SD

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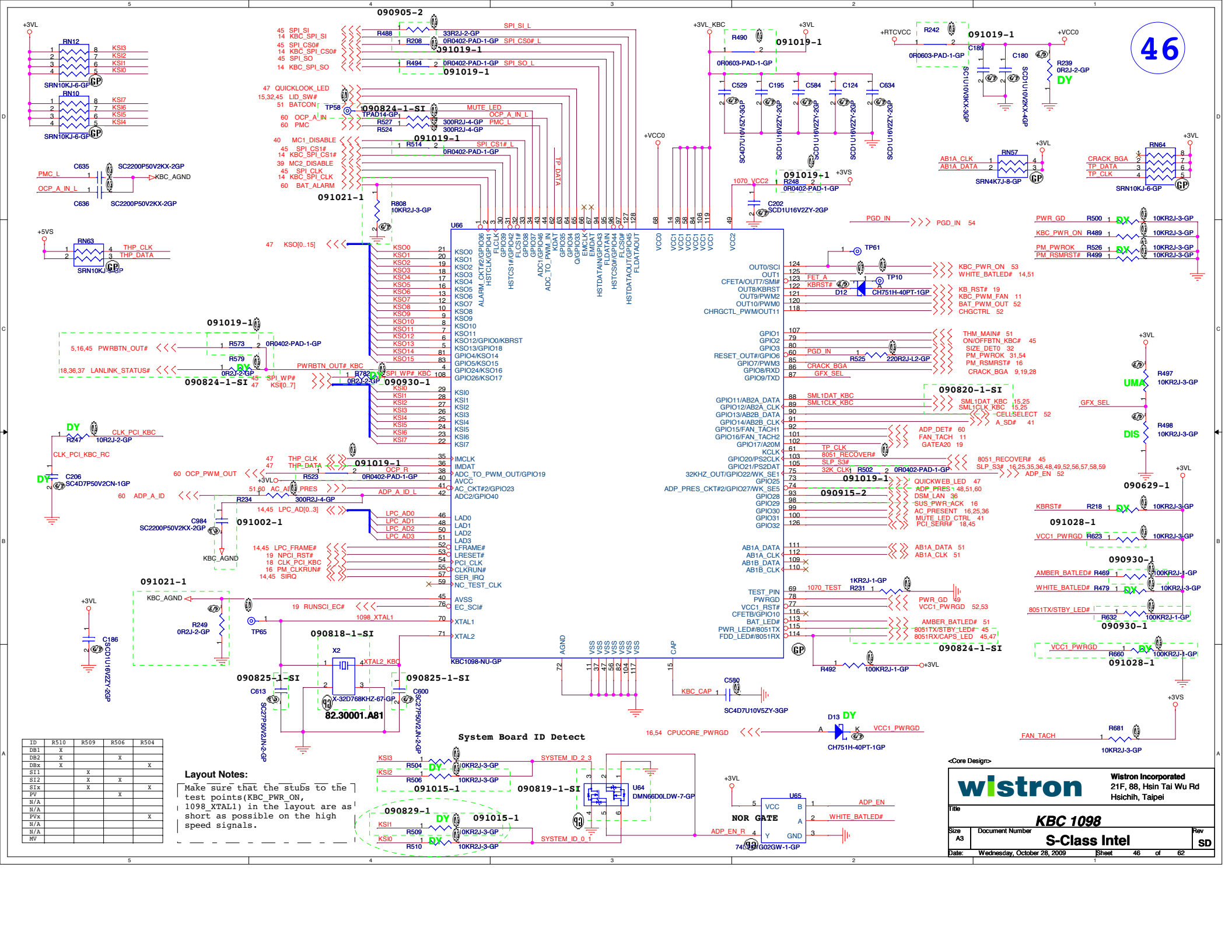
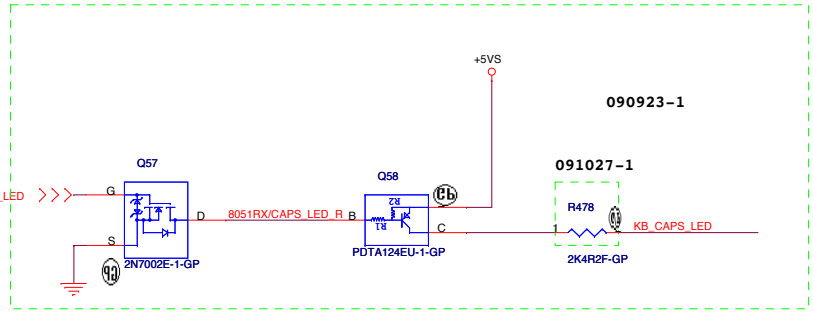
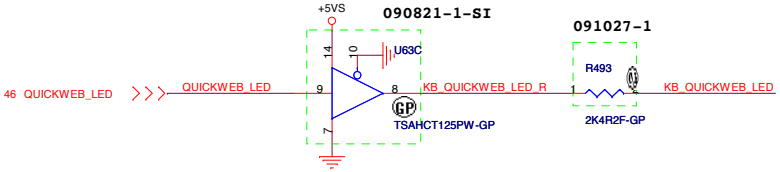
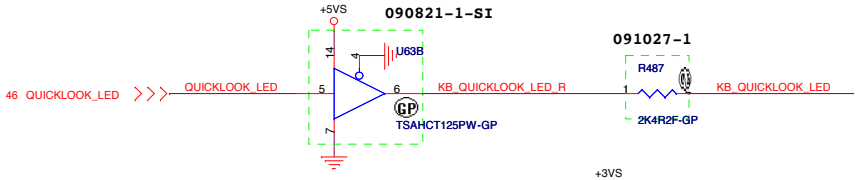


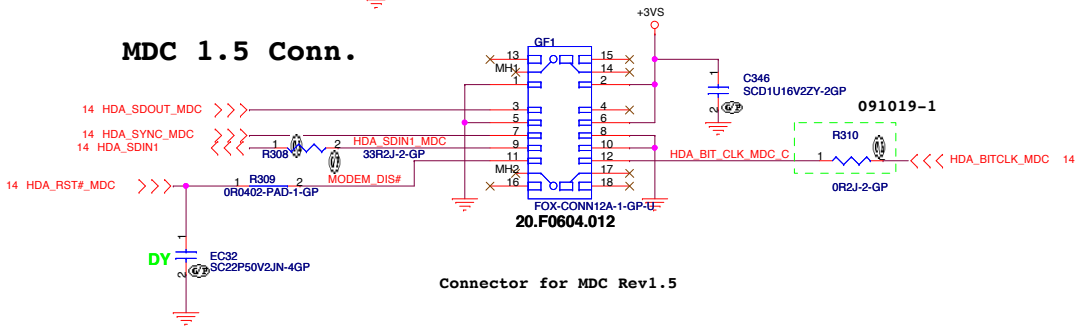
ID	R510	R509	R506	R504
DB1	X			
DB2	X		X	
DBx	X			X
SI1		X		
SI2		X	X	
SIx		X		X
PV			X	
N/A				
N/A				
PVx				X
N/A				
N/A				
MV				





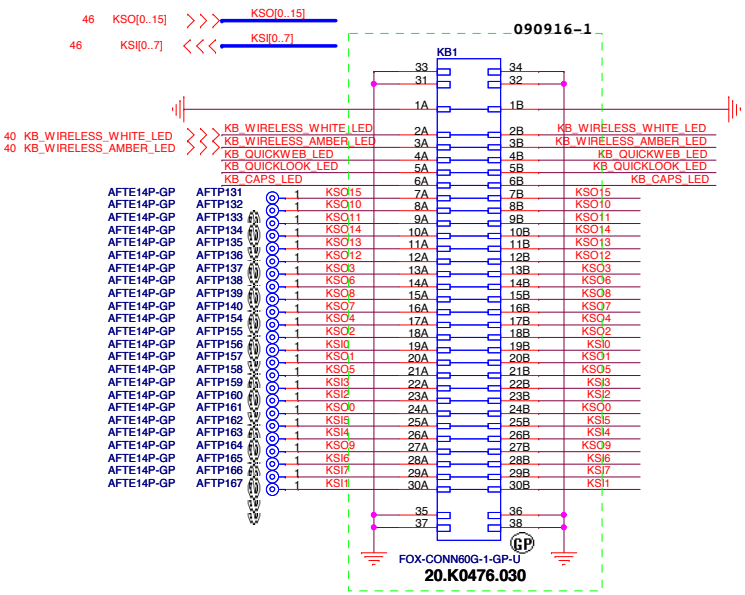


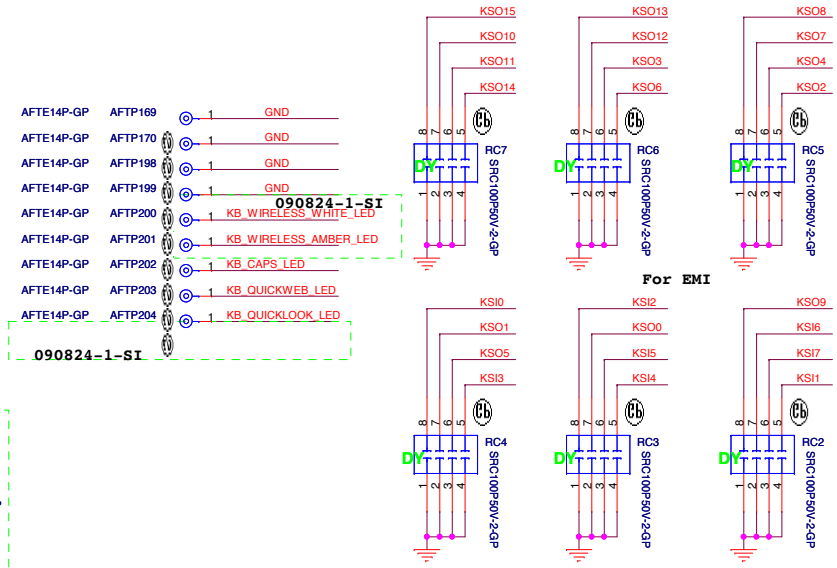
MDC 1.5 Conn.



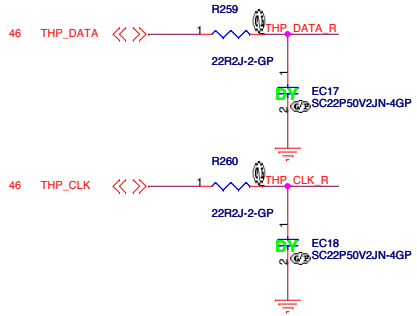
Connector for MDC Rev1.5

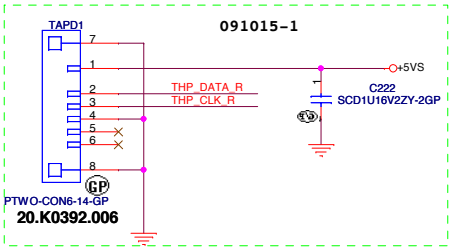
INT_KBD CONN.

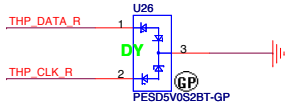


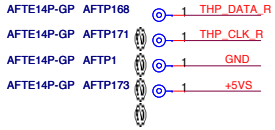


Touch_Pad CONN.









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Hsichih, Taipei

Title: MDC/KBD/ON OFF/T.P.

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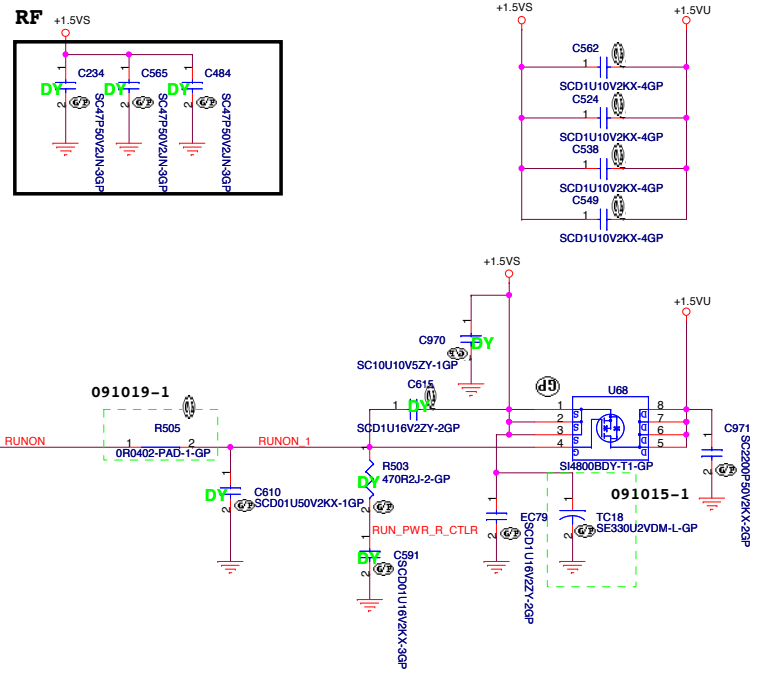
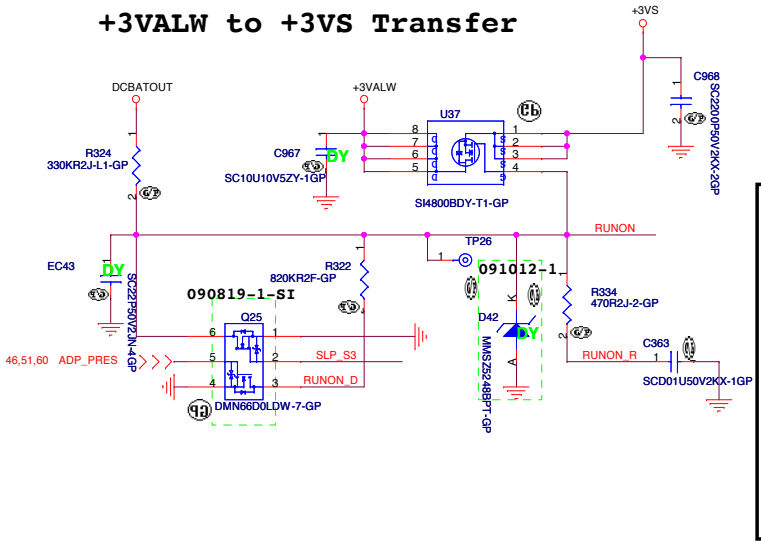
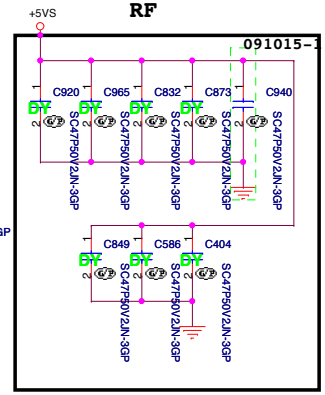
+1.5VU to +1.5VS Transfer

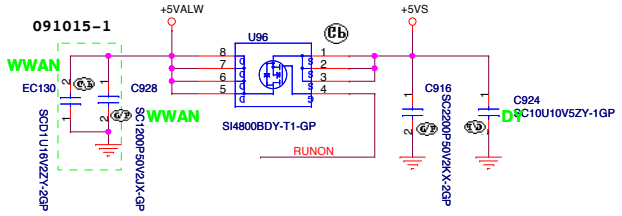


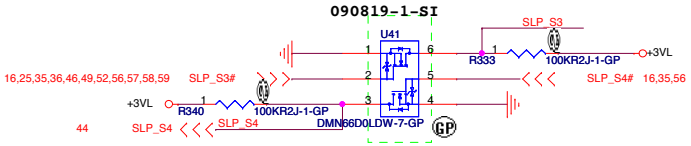
+3VALW to +3VS Transfer



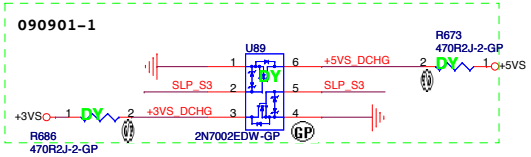


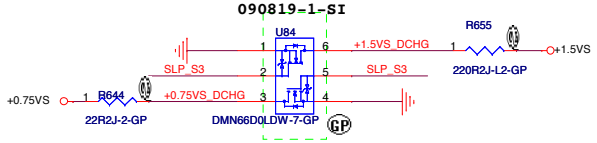
+5VALW to +5VS Transfer

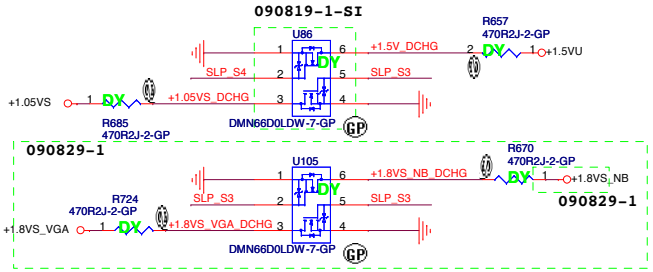




Discharge circuit-1







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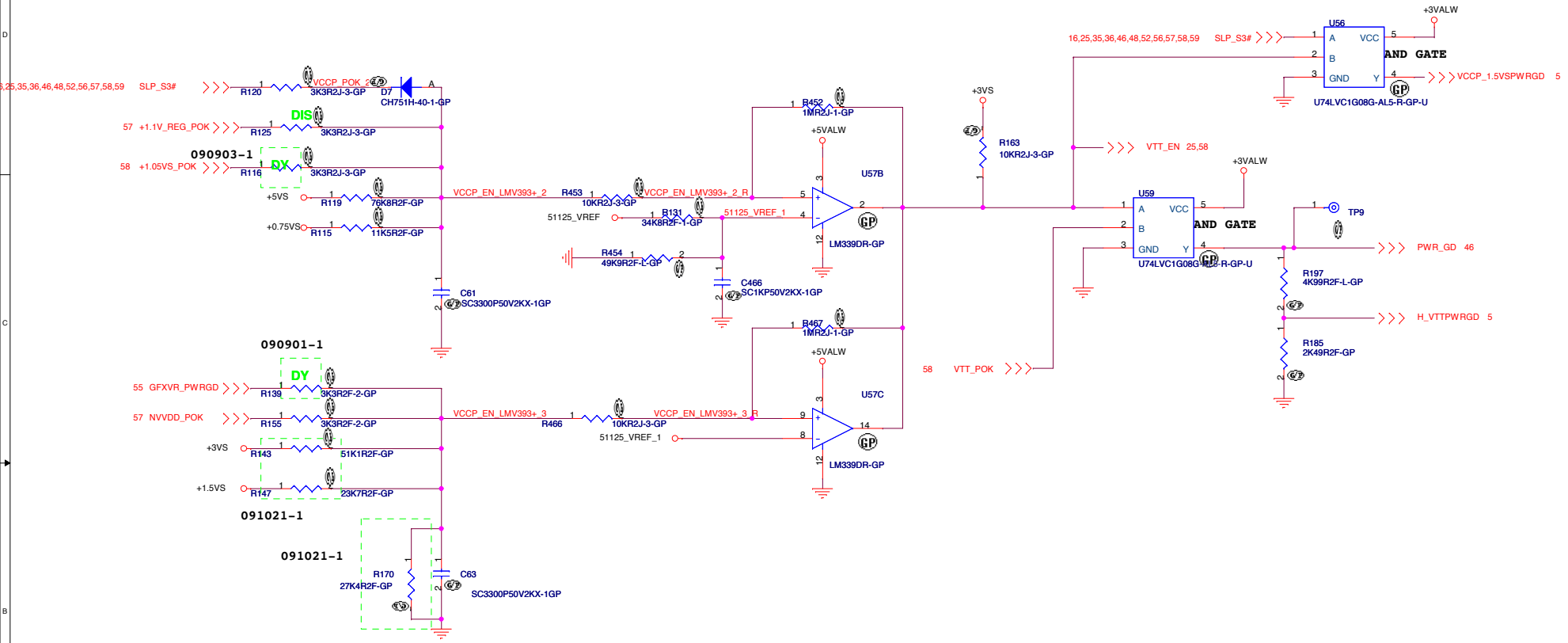
Title: DC/DC Circuit

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 48 of 62



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Title: POK CKT

Size: A3 | Document Number: S-Class Intel | Rev: SD

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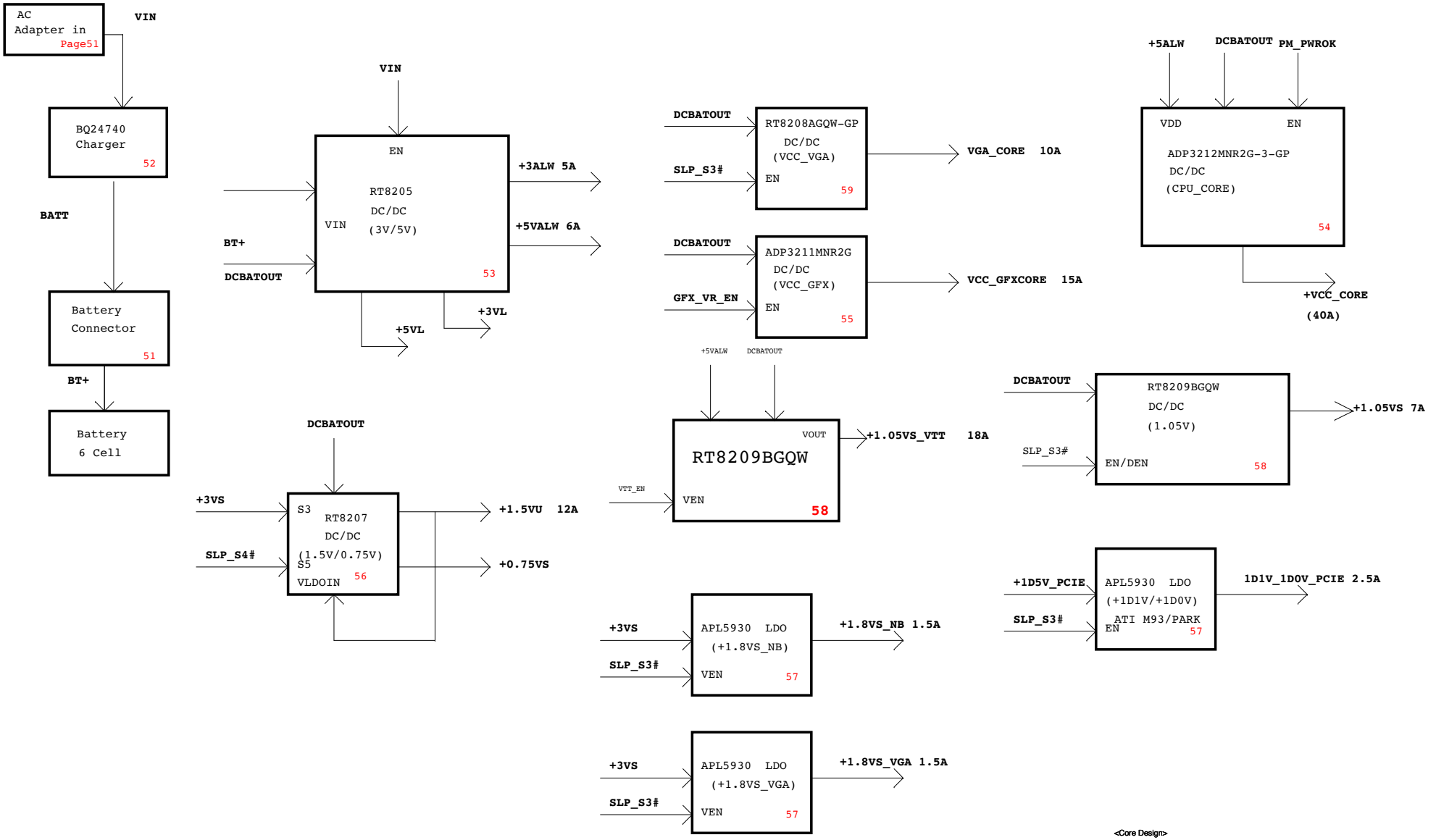
Power Block Diagram

50



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Title: Power Block Diagram

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A3	S-Class Intel	SD

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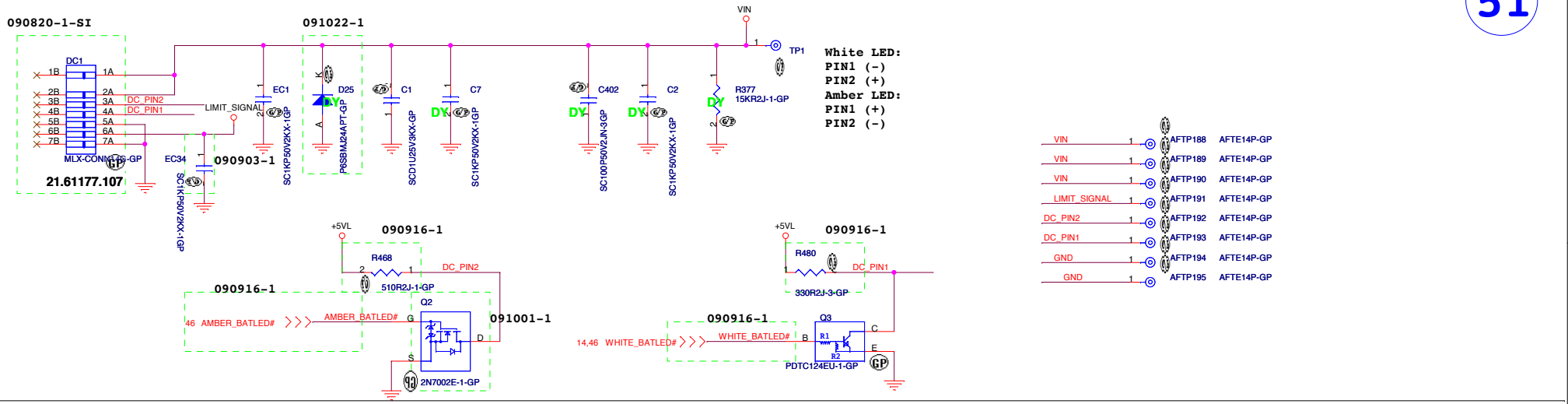
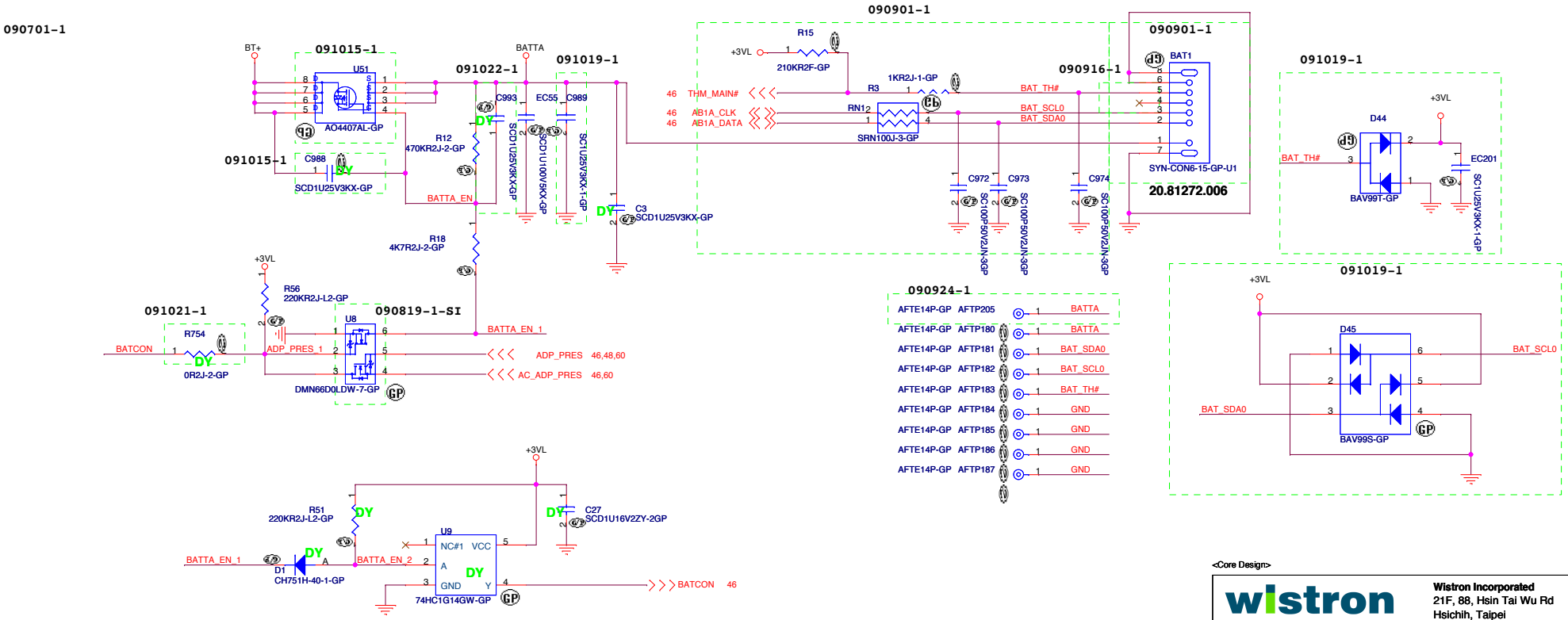
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title: DC & BATTERT CONN.

Size: Custom | Document Number: S-Class Intel | Rev: SD

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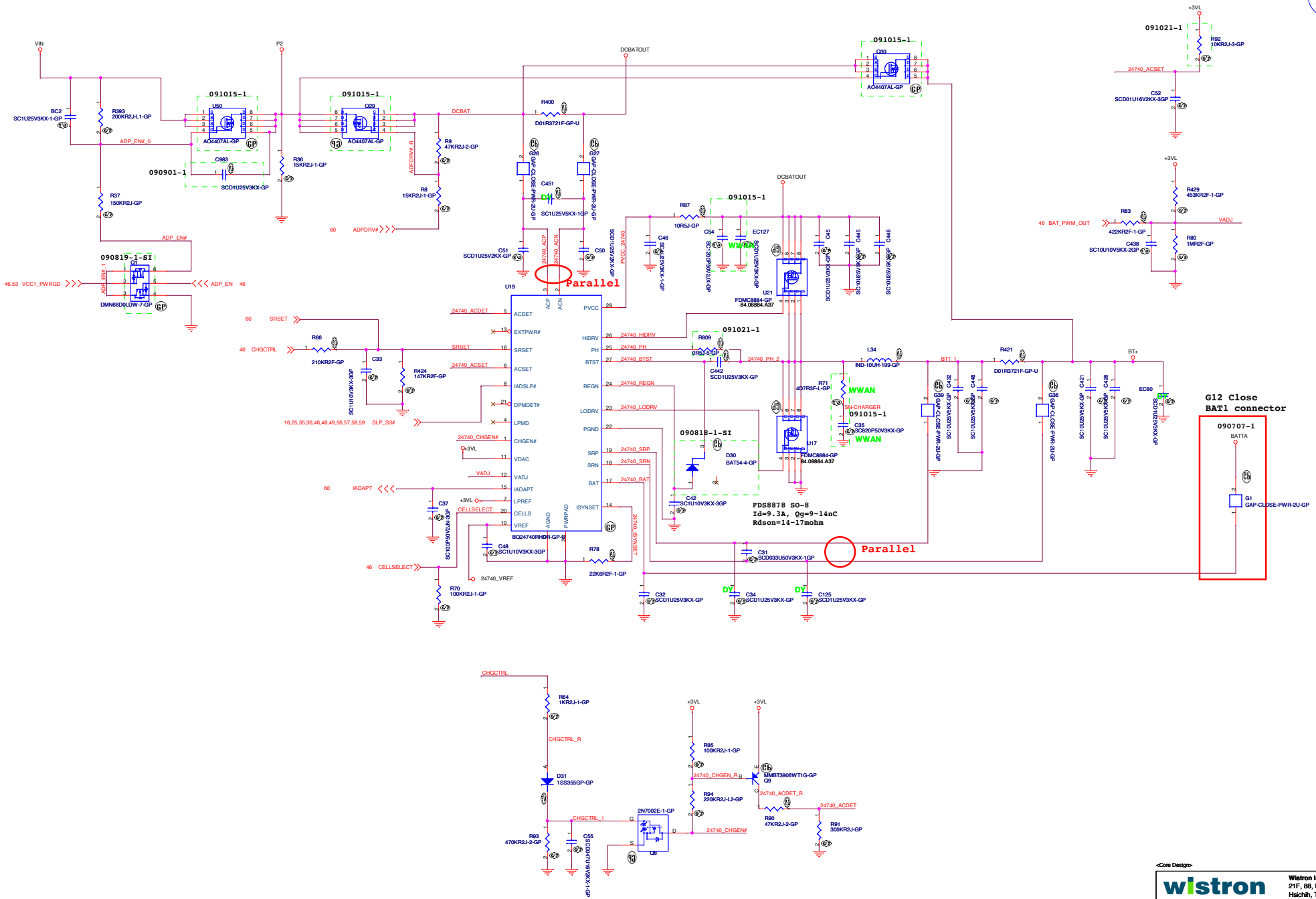

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Hsichih, Taipei

Title: CHARGER BQ24740

Size: A2 | Document Number: S-Class Intel | Rev: SD

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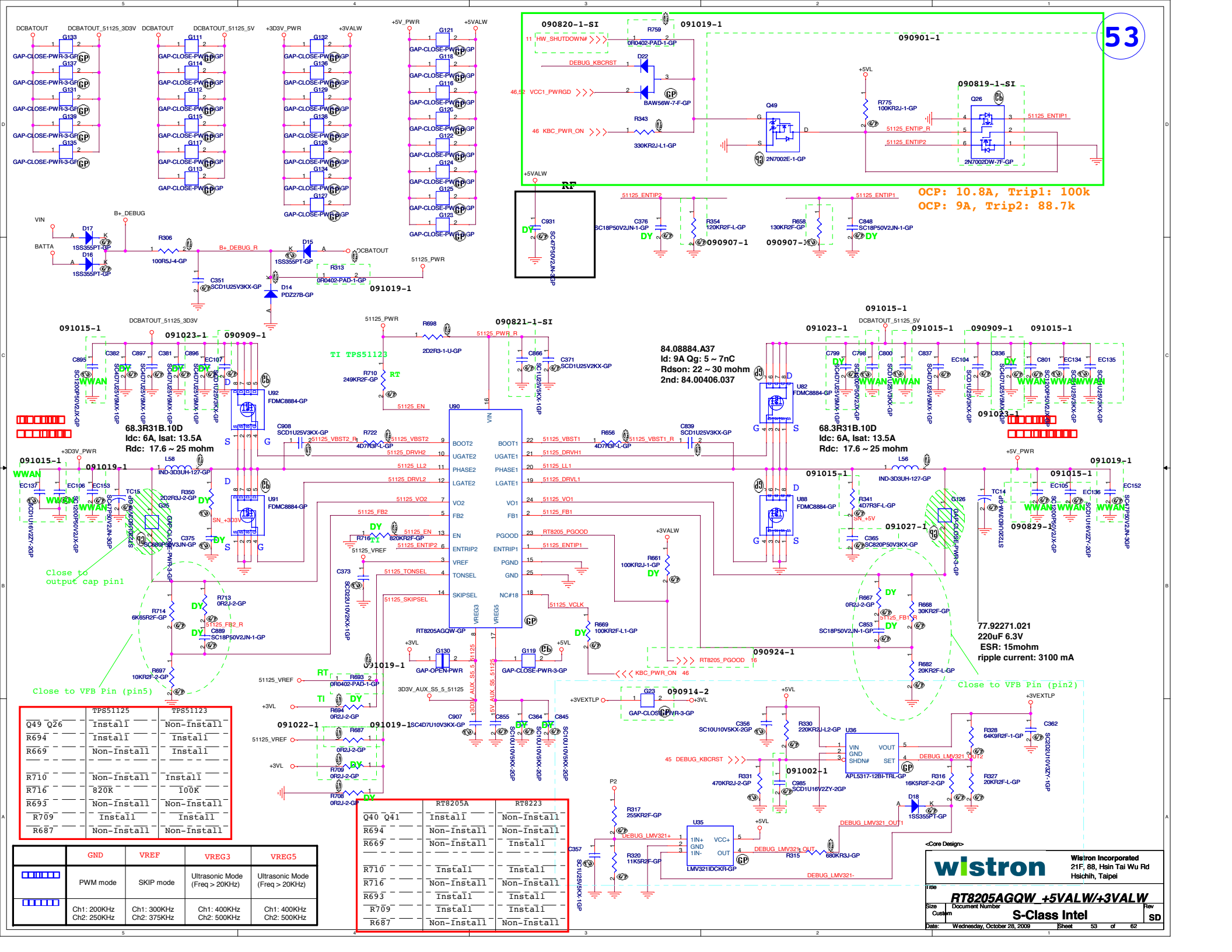
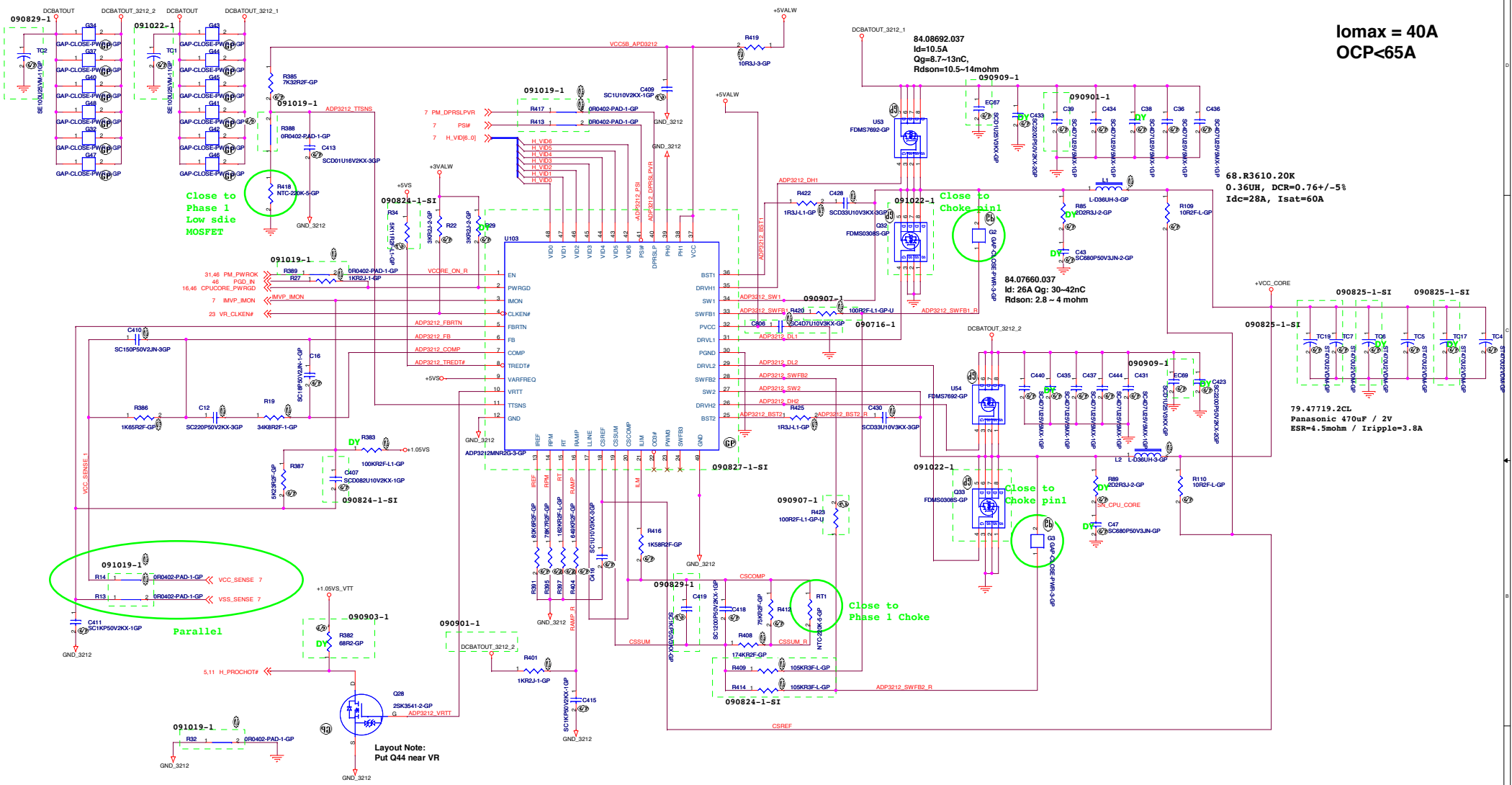


	TPS51125	TPS51123
Q49 Q26	Install	Non-Install
R694	Install	Install
R669	Non-Install	Install
R710	Non-Install	Install
R716	820K	100K
R693	Non-Install	Non-Install
R709	Install	Install
R687	Non-Install	Non-Install

	GND	VREF	VREG3	VREG5
	PWM mode	SKIP mode	Ultrasonic Mode (Freq > 20KHz)	Ultrasonic Mode (Freq > 20KHz)
	Ch1: 200KHz Ch2: 250KHz	Ch1: 300KHz Ch2: 375KHz	Ch1: 400KHz Ch2: 500KHz	Ch1: 400KHz Ch2: 500KHz

	RT8205A	RT8223
Q40 Q41	Install	Non-Install
R694	Non-Install	Non-Install
R669	Non-Install	Install
R710	Install	Install
R716	Non-Install	Non-Install
R693	Install	Install
R709	Install	Install
R687	Non-Install	Non-Install



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Title: ADP3212MNR2G_CPU CORE

Size	Document Number	Rev
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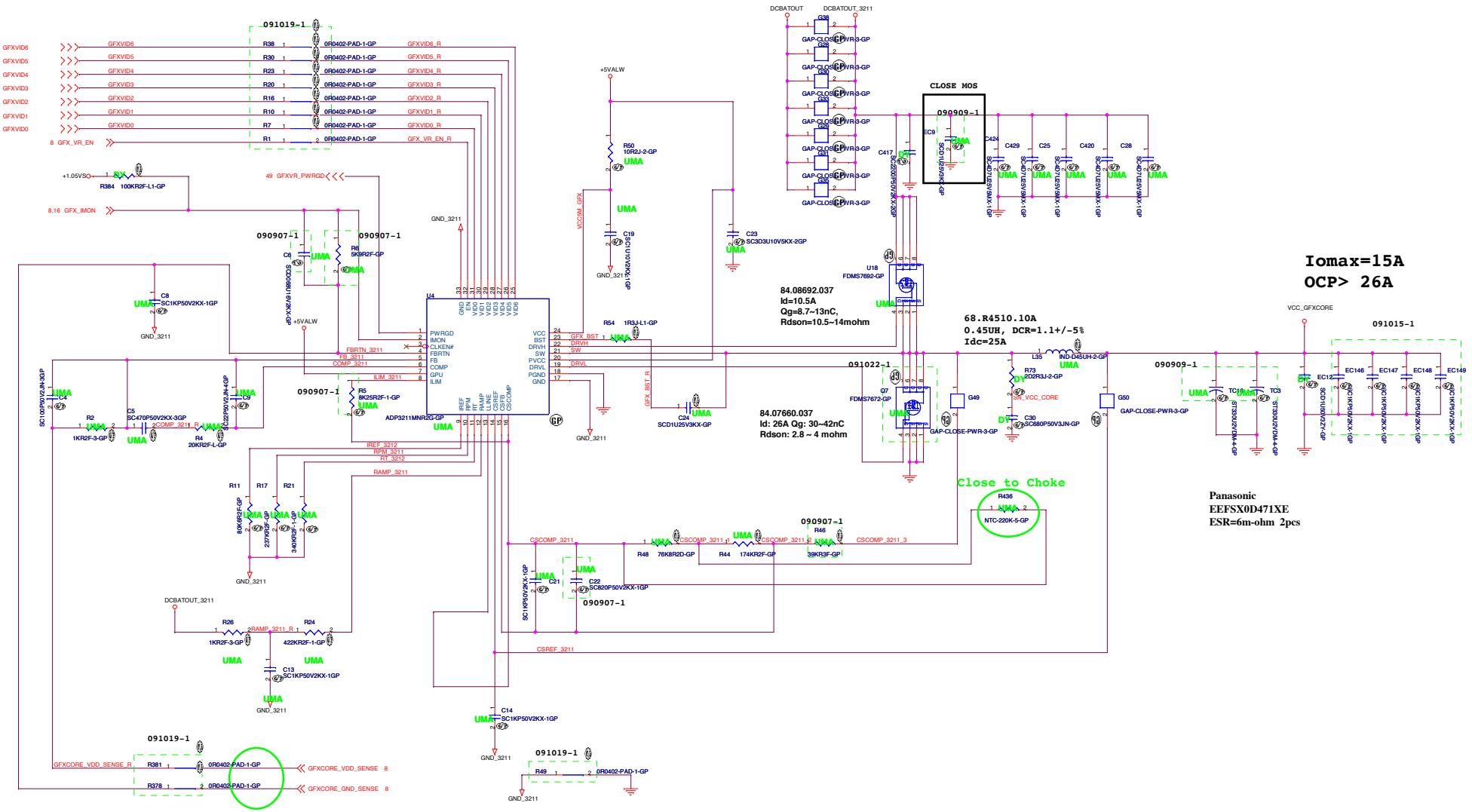

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Title: ADP3211MNR2G_+VCC_GFX_CORE

Size: A2 | Document Number: S-Class Intel | Rev: SD

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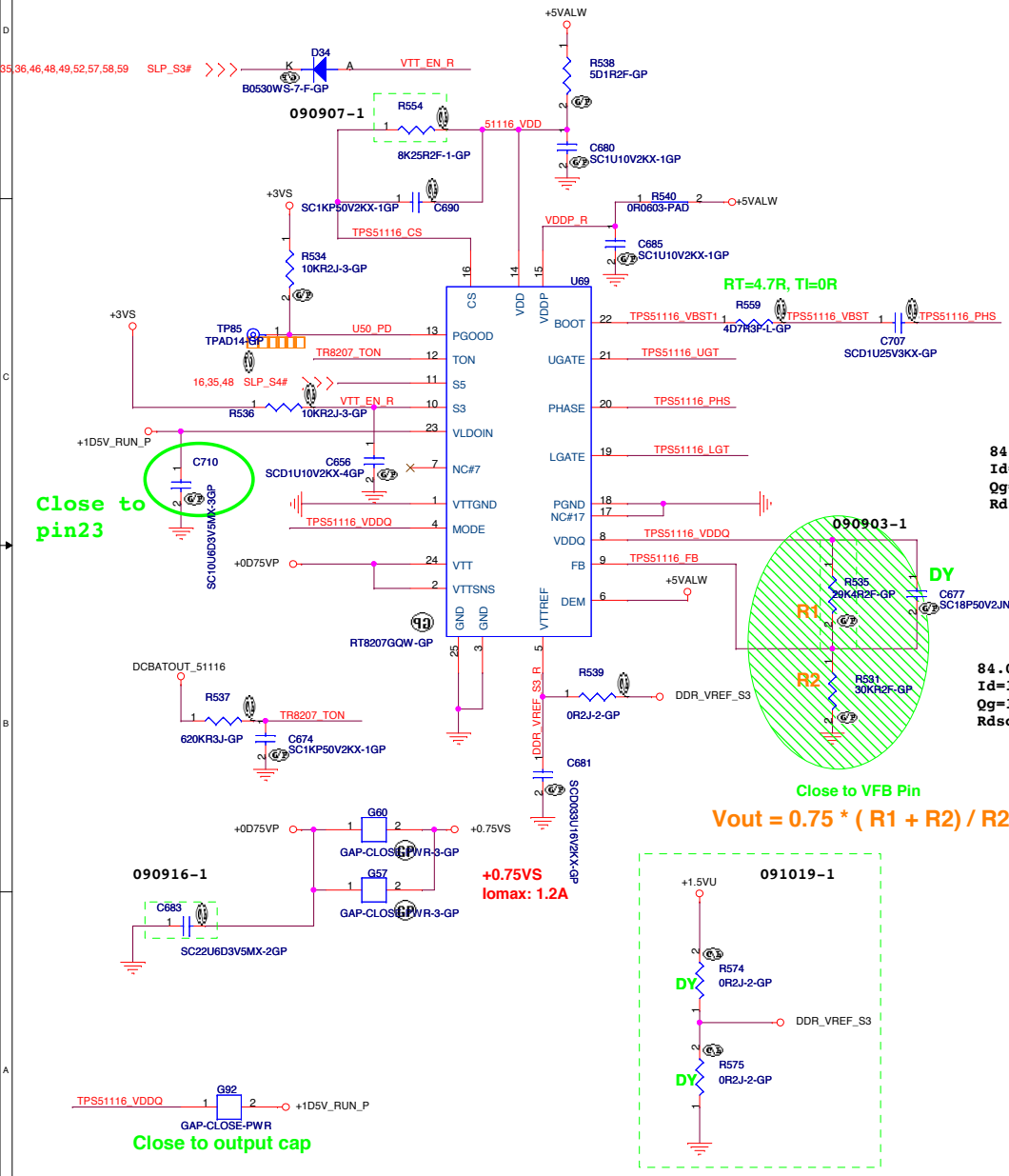
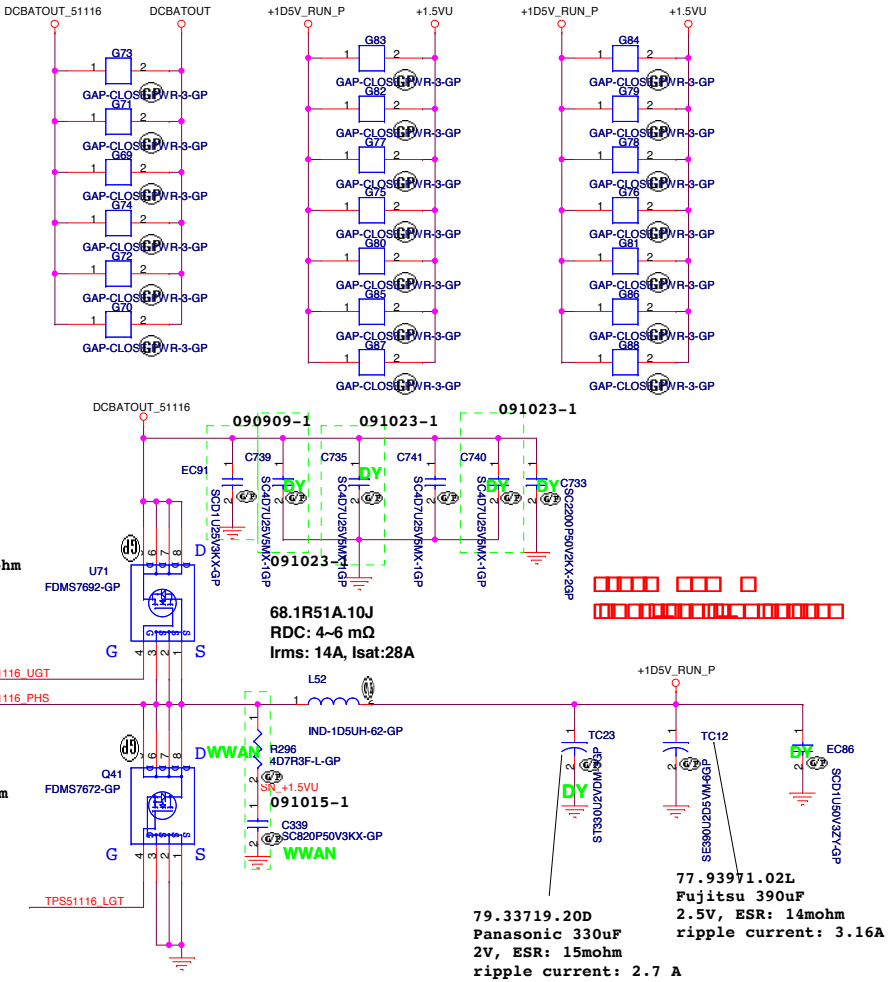
RT8207 for 1D5V and 0D75V



84.08692.037
Id=10.5A
Qg=8.7-13nC,
Rdson=10.5-14mohm

84.07672.037
Id=15A
Qg=15-21nC,
Rdson=5.2-6.9mohm



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Title: RT8207GQW +1.5VU / +0.75VS

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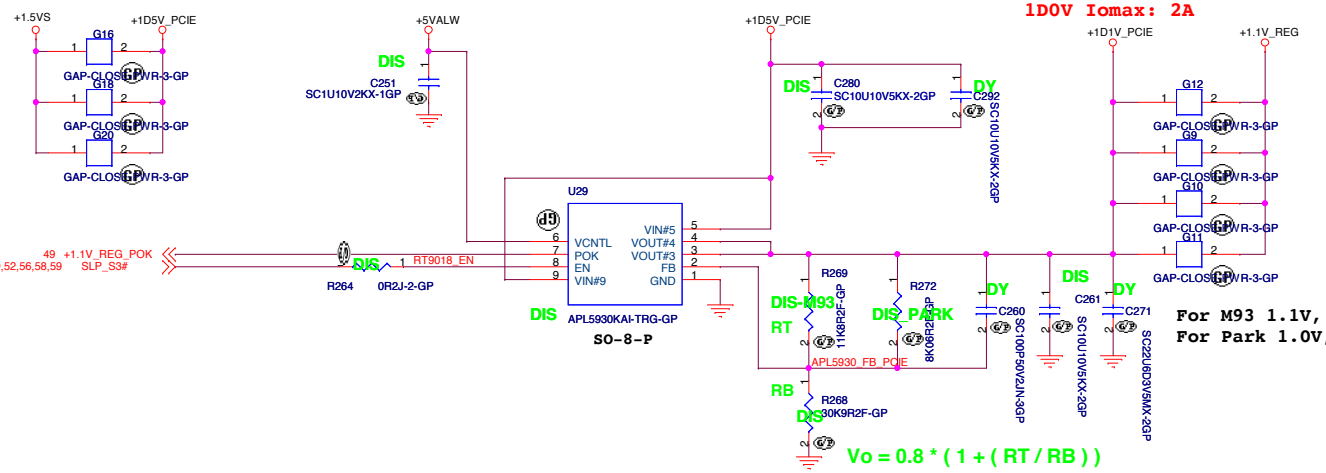
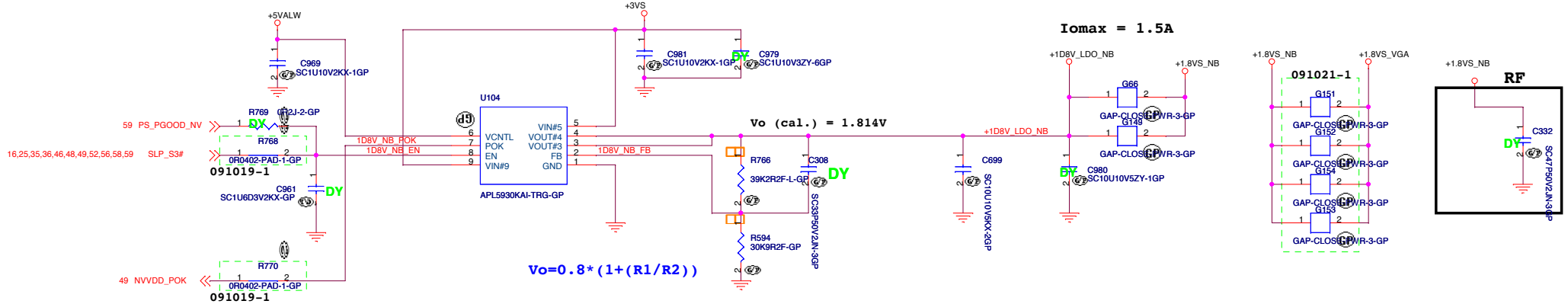
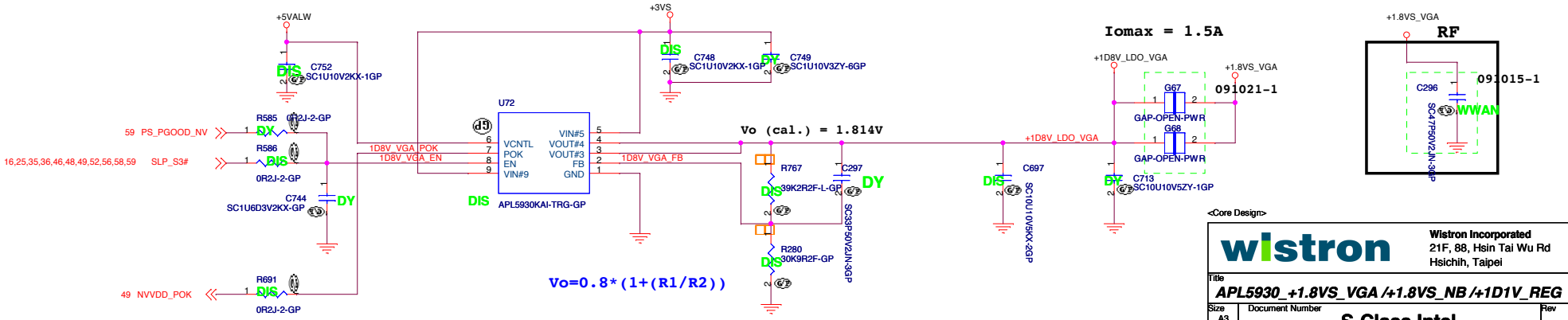
1D1V Iomax: 2.5A
1D0V Iomax: 2A







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Title: APL5930_+1.8VS_VGA /+1.8VS_NB /+1D1V_REG

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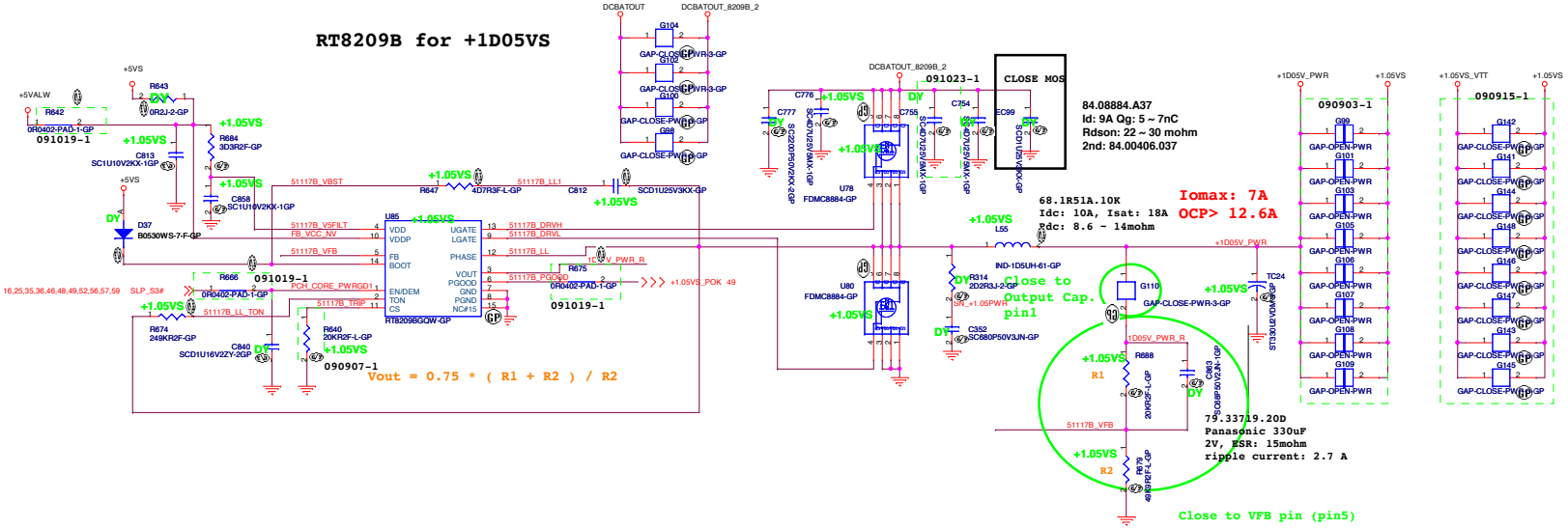
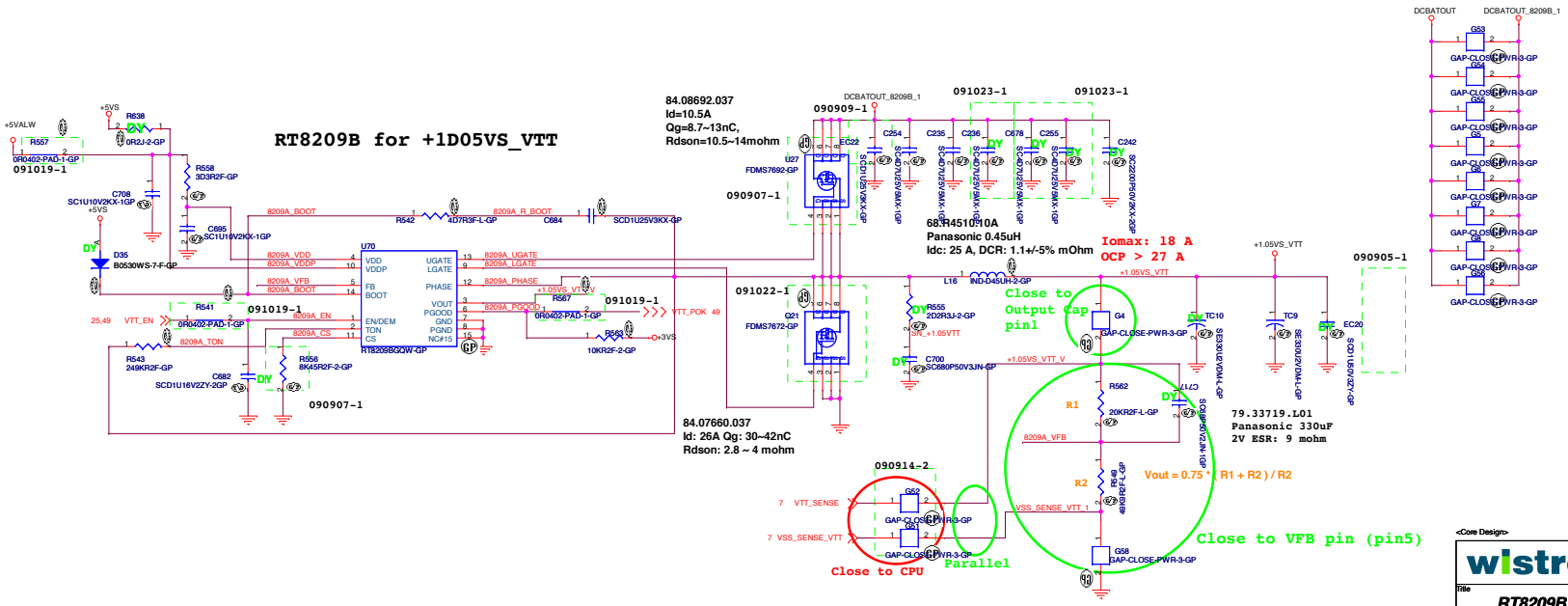
RT8209B for +1D05VS



RT8209B for +1D05VS_VTT



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Title: RT8209B +1.05VS_VTT/+1.05VS

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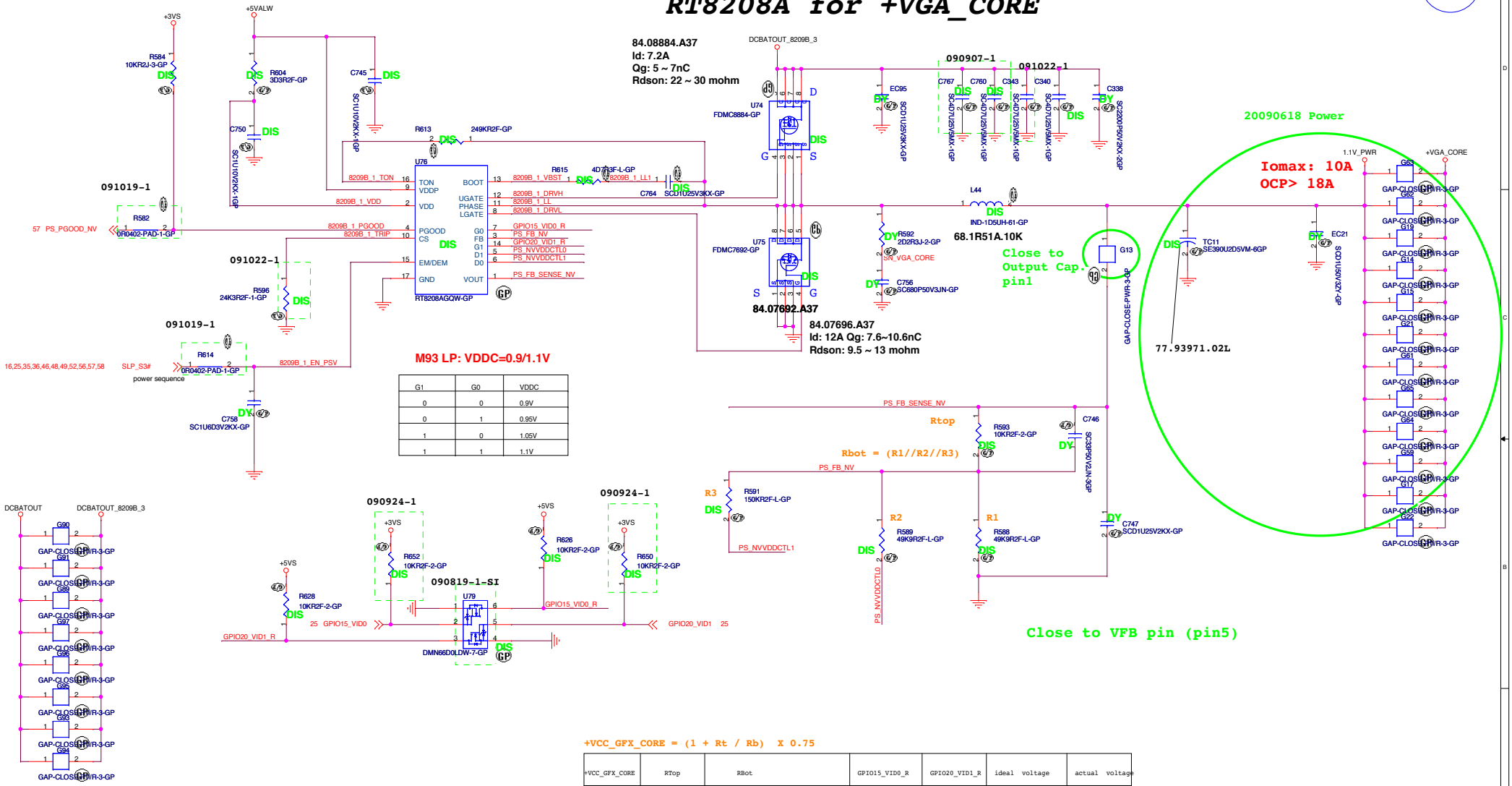
RT8208A for +VGA_CORE



G1	G0	VDDC
0	0	0.9V
0	1	0.95V
1	0	1.05V
1	1	1.1V

+VCC_GFX_CORE = (1 + Rt / Rb) X 0.75

+VCC_GFX_CORE	RTop	RBot	GPIO15_VID0_R	GPIO20_VID1_R	ideal voltage	actual voltage
0.9v	10k	R1 49.9k	LOW	LOW	0.9003	
0.95v	10k	R1 R2 49.9k // 49.9k	LOW	HIGH	0.9493	
1.05v	10k	R1 R3 49.9k // 150k	HIGH	LOW	1.0506	
1.1v	10k	R1 R2 R3 49.9k // 49.9k // 150k	HIGH	HIGH	1.0997	

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Title: RT8208AGQW_+VGA_CORE

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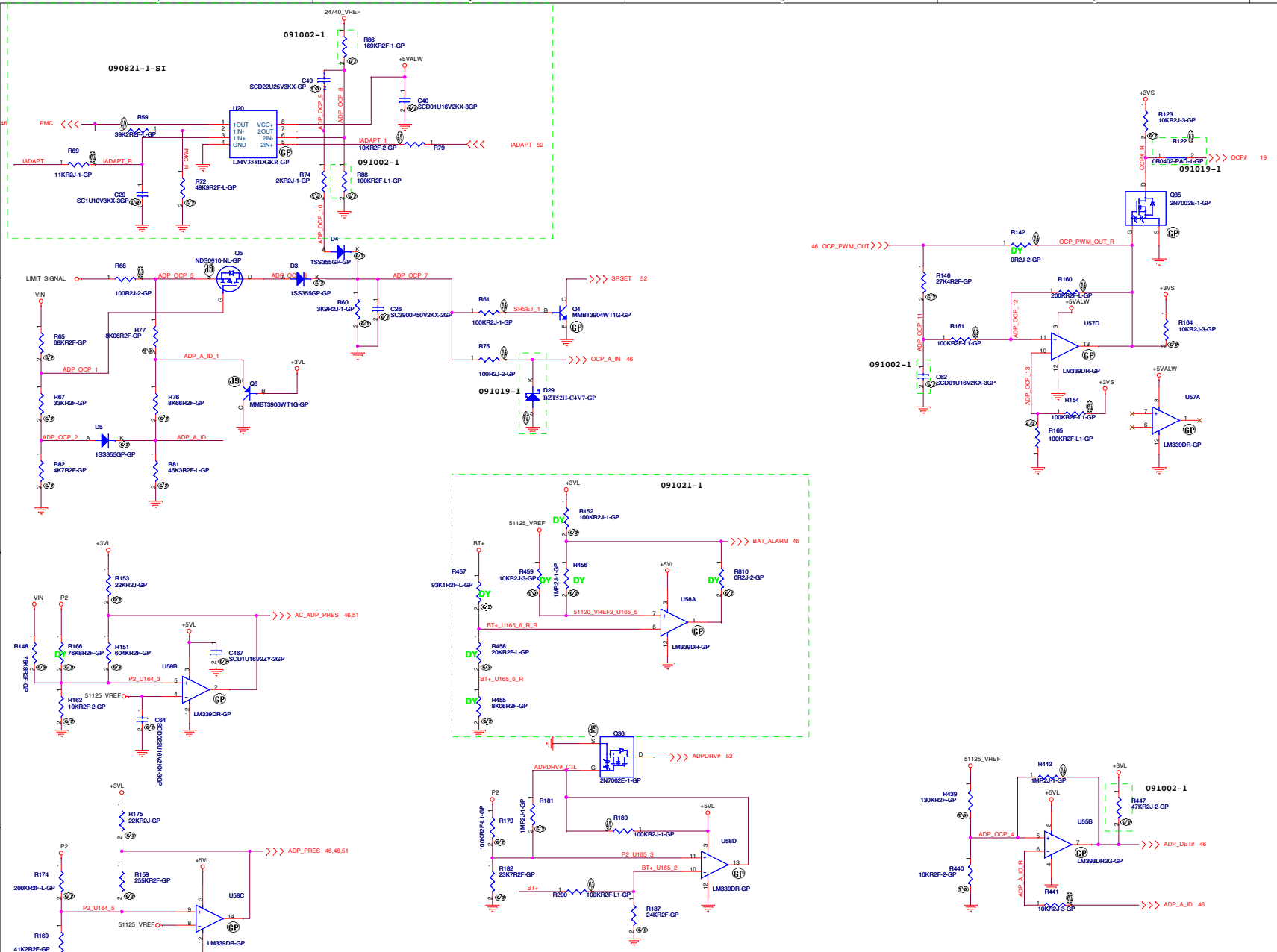

When AC_ADP_PRES=0 -->1
Vin*(R162//R151)/ [(R162//R151)+R148]=51125_VREF
Vin=17.6145V

When AC_ADP_PRES=1 --> 0
[(Vin-51125_VREF)/R148]+[(+3VL-51125_VREF)/(R151+R153)]=51125_VREF/R162

Vin=17.212554V

When ADP_PRES=0->1

P2*(R169//R159)/ [(R169//R159)+R174]=51125_VREF

P2=13.325V

When ADP_PRES=1->0

[(P2-51125_VREF)/R169]+[(+3VL-51125_VREF)/(R175+R159)]=51125_VREF/R169

P2=10.894V

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Title: ADP OCP

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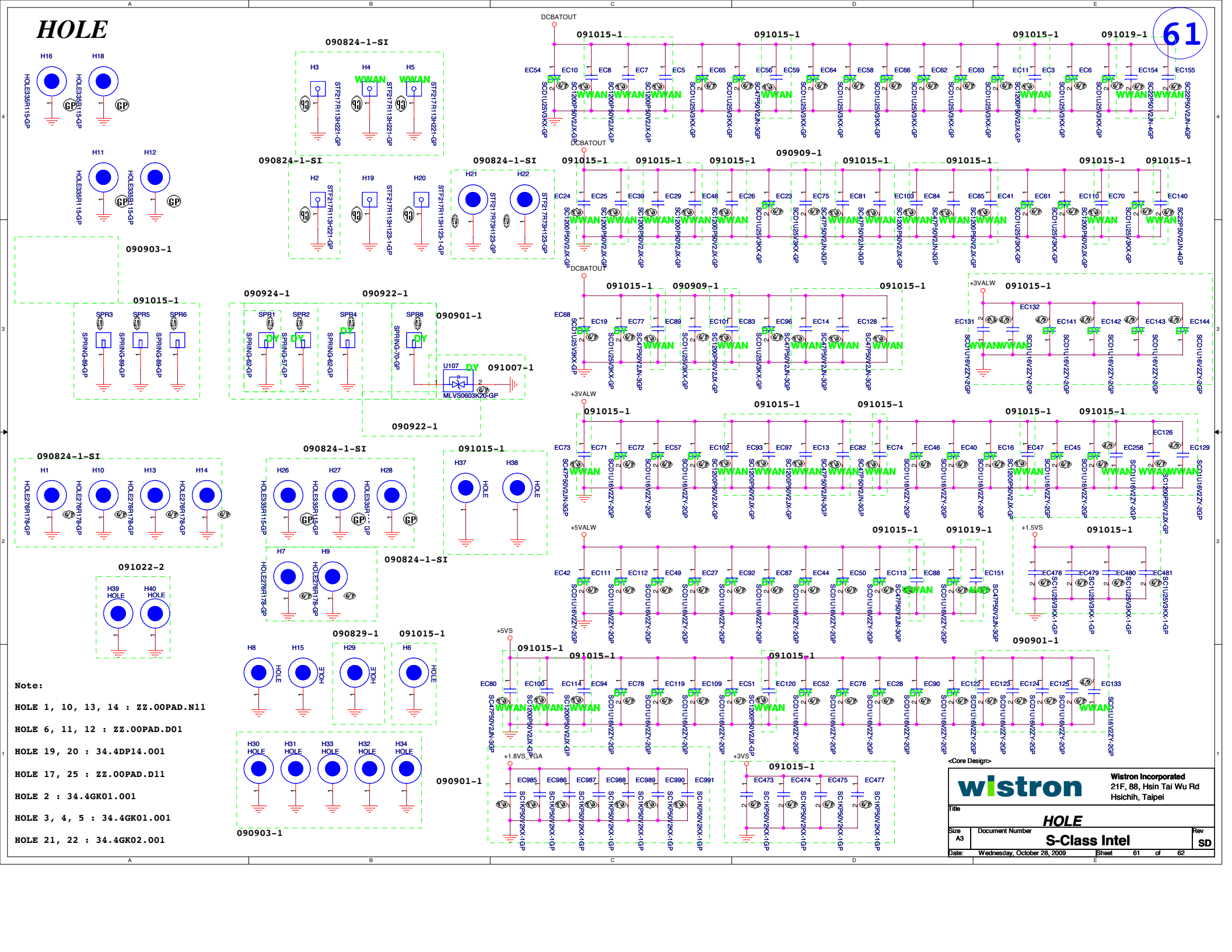
HOLE



Note:

HOLE 1, 10, 13, 14 : ZZ.00PAD.N11

HOLE 6, 11, 12 : ZZ.00PAD.D01

HOLE 19, 20 : 34.4DP14.001

HOLE 17, 25 : ZZ.00PAD.D11

HOLE 2 : 34.4GK01.001

HOLE 3, 4, 5 : 34.4GK01.001

HOLE 21, 22 : 34.4GK02.001

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Title: HOLE

Size: A3 | Document Number: S-Class Intel | Rev: SD

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Title

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