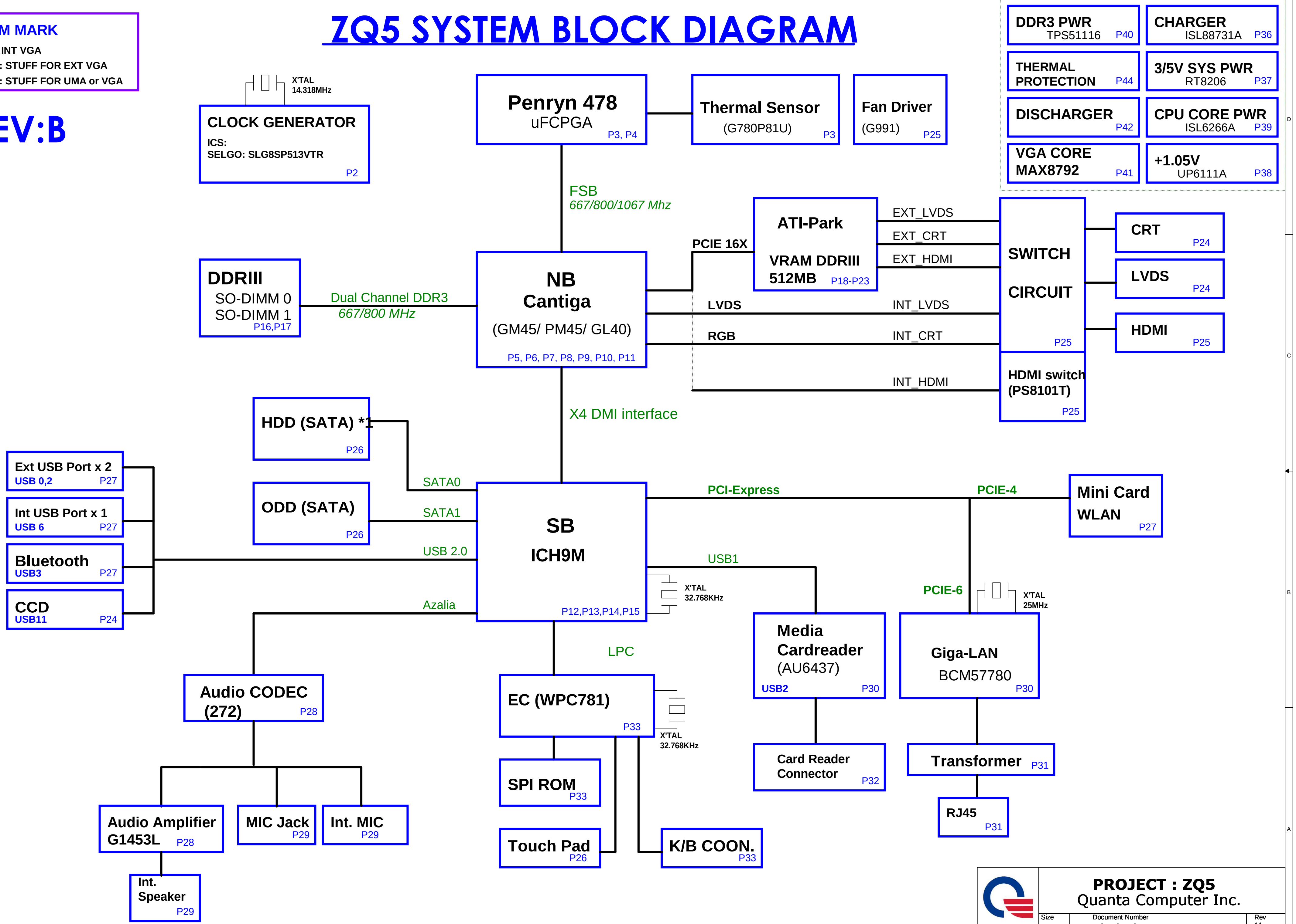
ZQ5 SYSTEM BLOCK DIAGRAM

BOM MARK
IV@: INT VGA
EV@: STUFF FOR EXT VGA
SP@: STUFF FOR UMA or VGA

REV:B



PROJECT : ZQ5
Quanta Computer Inc.

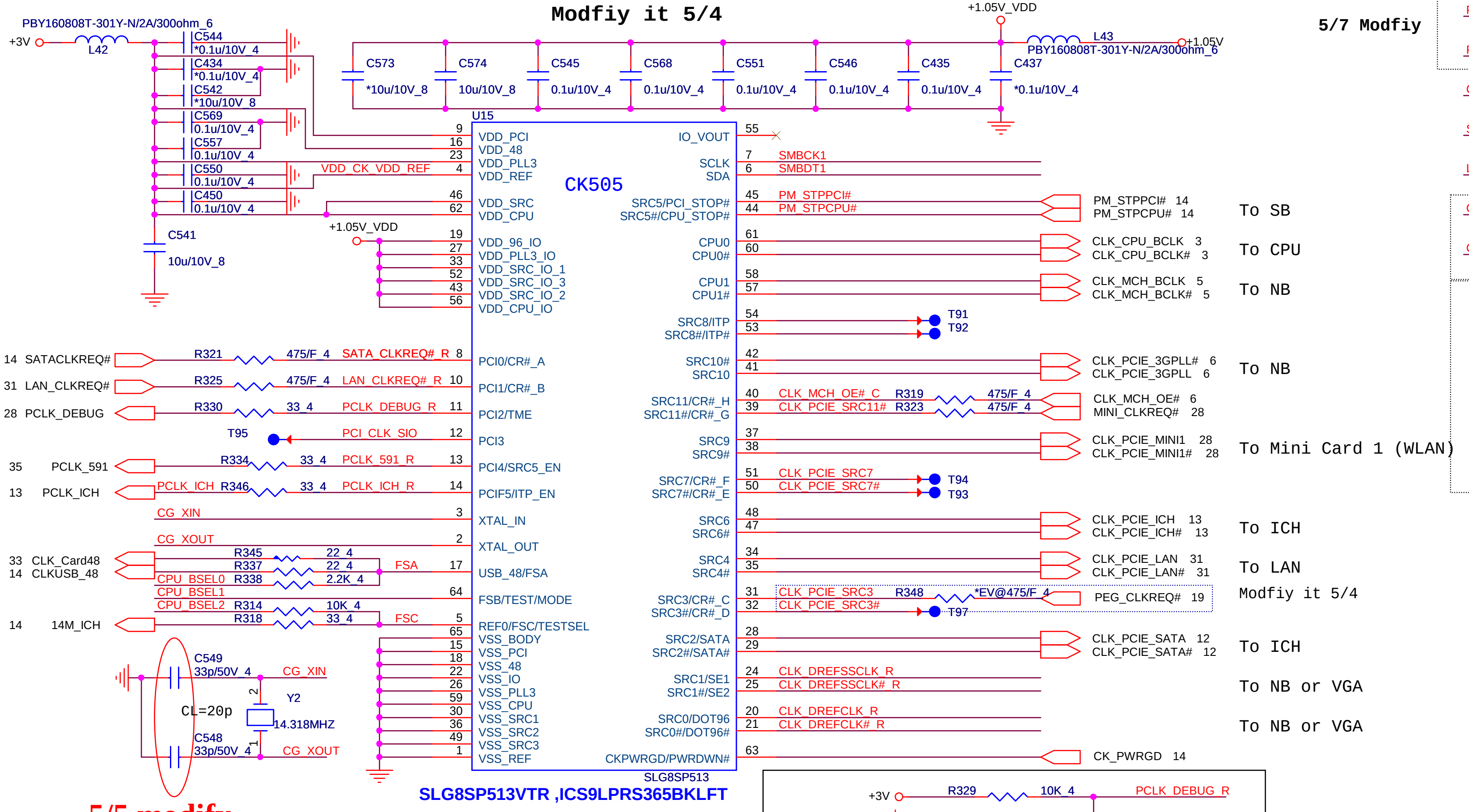
Size	Document Number	Rev
	Block Diagram	1A

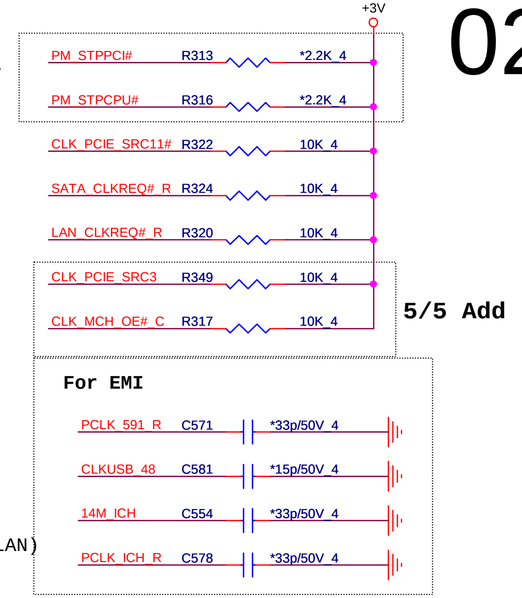
Date: Monday, June 21, 2010 Sheet 1 of 43

Clock Generator(CLK)

02

Modfiy it 5/4





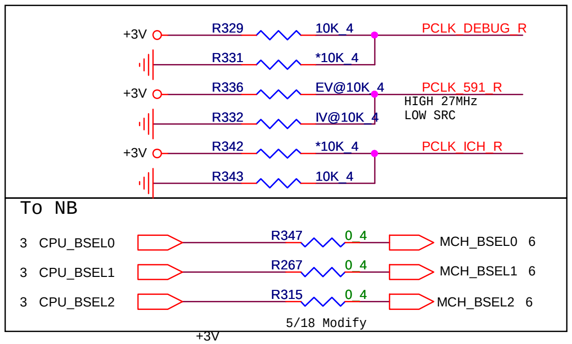
SEL2 SEL1 SEL0

Frequence select

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	Reserved		

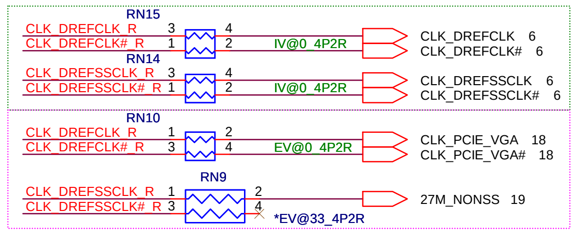
Default

	ICS9LRS3165BKLFT (ALPRS365000)	RTM875T-606 (AL000875000)	PULL HIGH	PULL DOWN
Pin 11	PCI2/TME	PCI2/TME internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 12	PCI-3	PCI-3/SRC5_EN internal PD	PIN37/38 IS SRC5	PIN37/38 IS PCI_STOP/CPU_STOP (default)
Pin 13	PCI-4/27M_SEL	PCI-4/27M_SEL internal PD	PIN 17/18 IS 27MHz	PIN 17/18 IS SRC/DOT (default)
Pin 14	PCIF-5/ITP_EN	PCIF-5/ITP_EN internal PD	PIN 46/47 IS CPUITP	PIN 46/47 IS SRC8 (default)



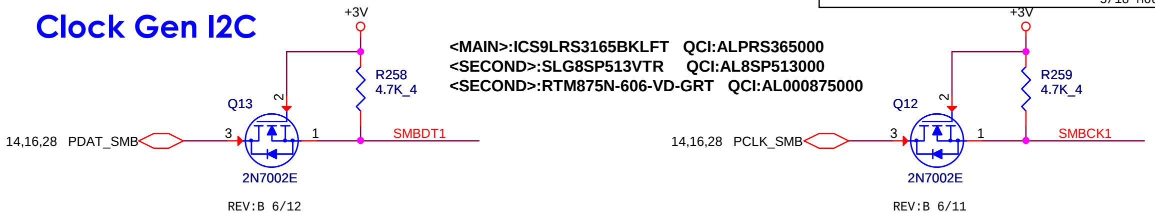
From GMCH

From Deiscerete



5/22 modify

Clock Gen I2C



<MAIN>:ICS9LRS3165BKLFT QCI:ALPRS365000
<SECOND>:SLG8SP513VTR QCI:AL8SP513000
<SECOND>:RTM875N-606-VD-GRT QCI:AL000875000

PROJECT : ZQ5
Quanta Computer Inc.

Size | Document Number: CLOCK GENERATOR | Rev 1A

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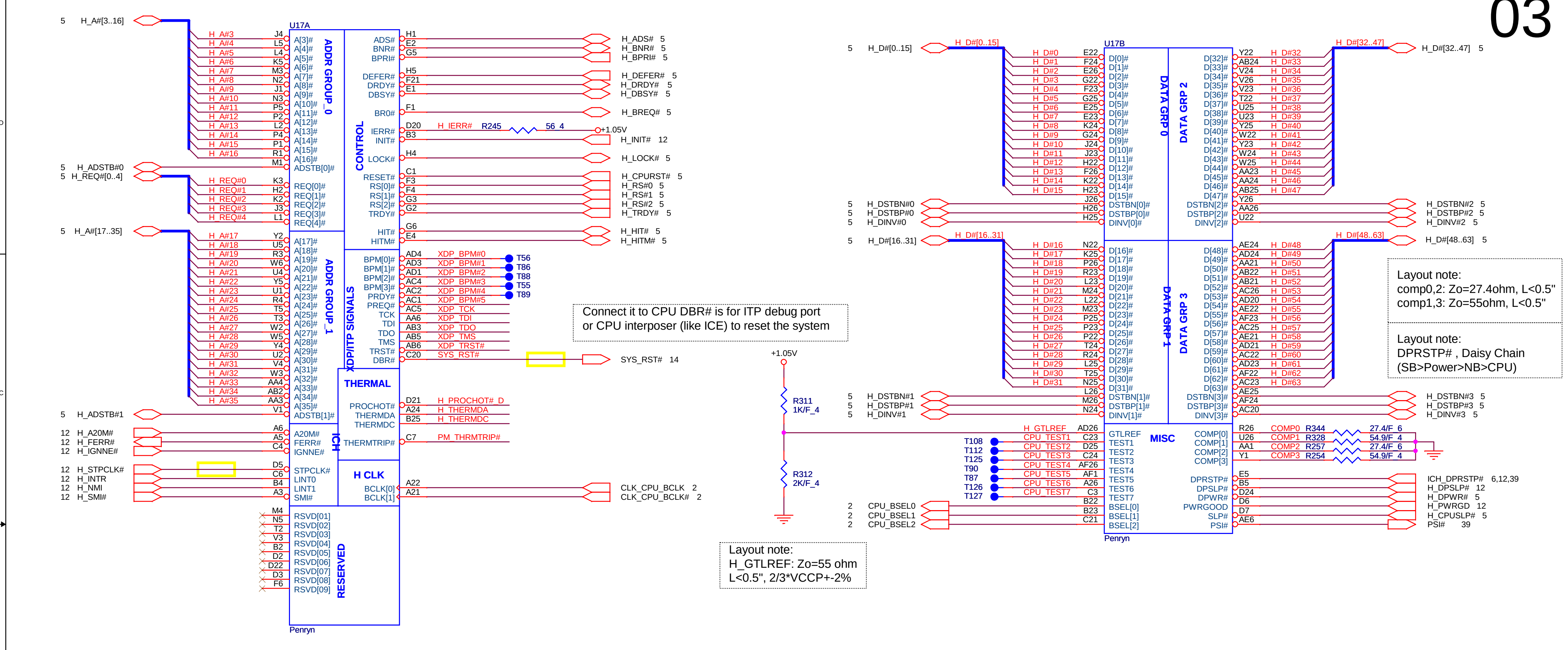
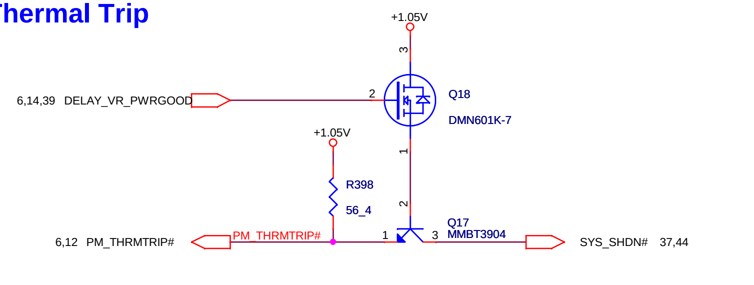
03



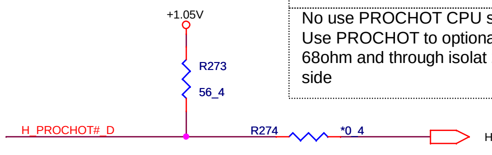
Thermal Trip



Processor hot

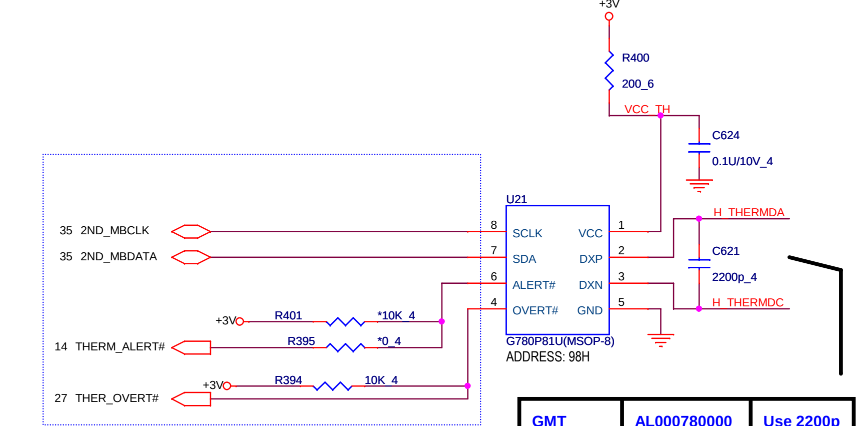
No use Thermal trip CPU side still PU 56ohm.
Use Thermal trip can share PU at SB side

No use PROCHOT CPU side still PU 56ohm.
Use PROCHOT to optional receiver CPU side PU 68ohm and through isolat 2.2K ohm to receiver side



CPU 1/2

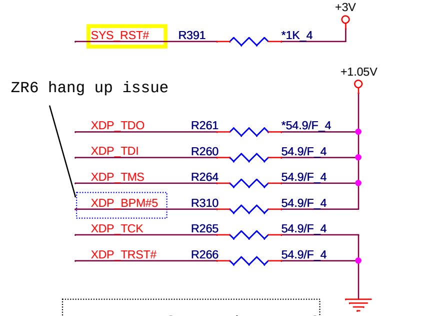
CPU Thermal monitor



4/20 Modify

GMT	AL000780000	Use 2200p
NS	AL095245000	Use 2200p
WINDBOND	AL83L771K01	Use 2200p

XDP PU/PD



XDP_DBRESET# and XDP_TDO reserve for XDP

PROJECT : ZQ5
Quanta Computer Inc.

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	CPU Host Bus	1A

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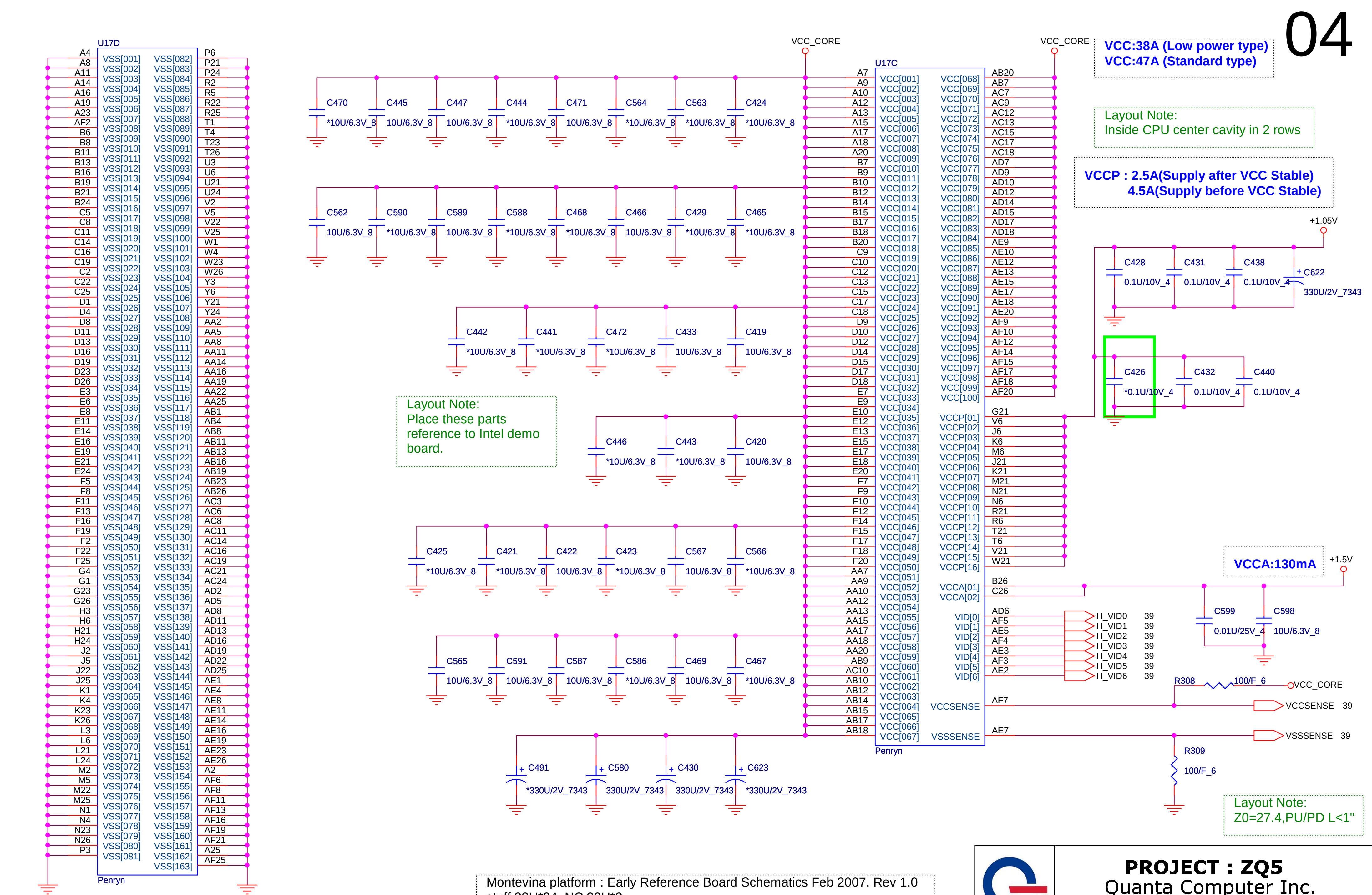

CPU 2/2

Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2

PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	CPU Power	1A

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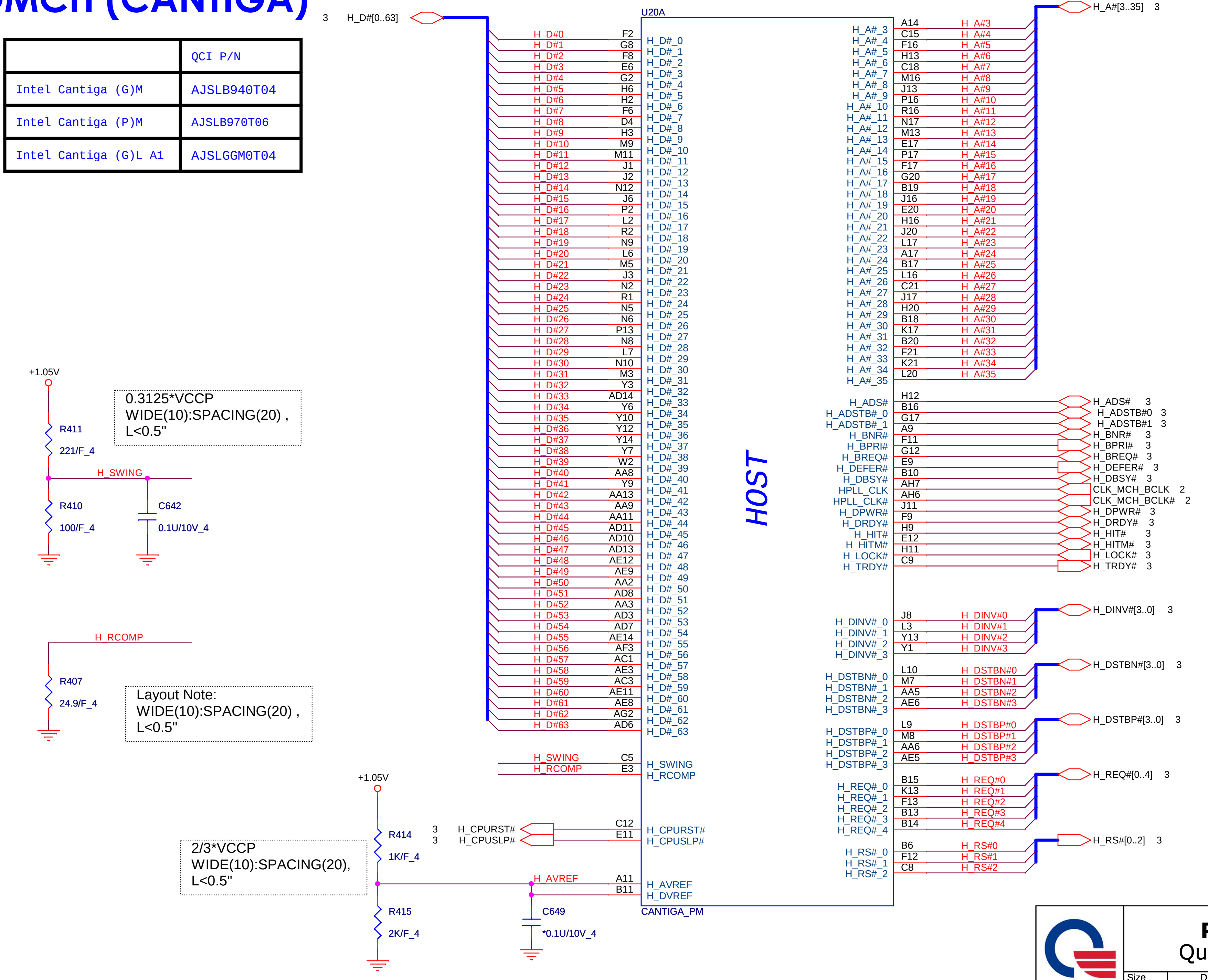
GMCH (CANTIGA)

05

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06
Intel Cantiga (G)L A1	AJSLGGM0T04



PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH HOST	1A
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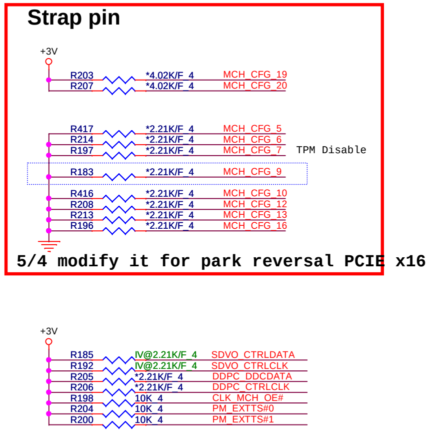
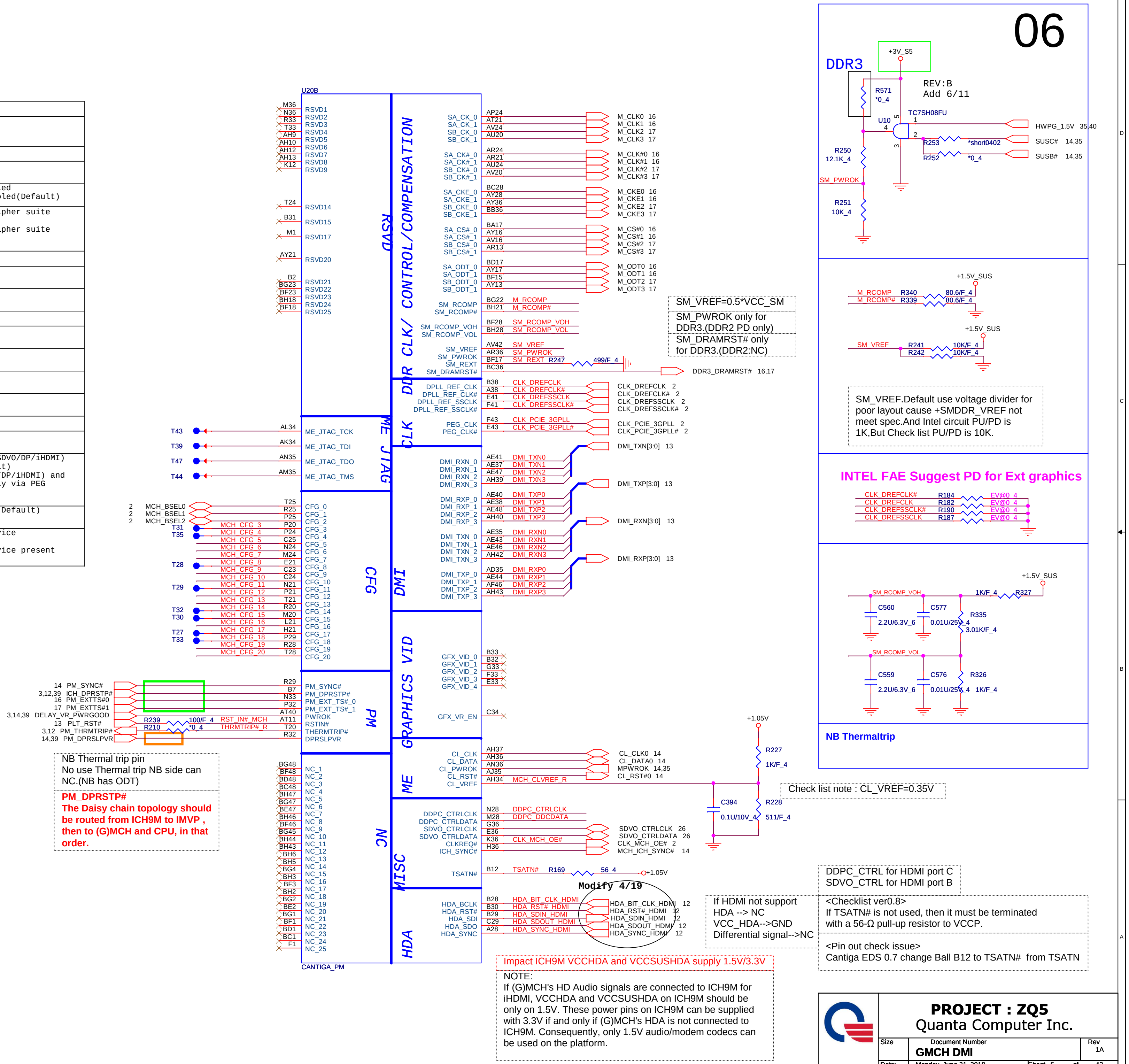
IV@
EV@

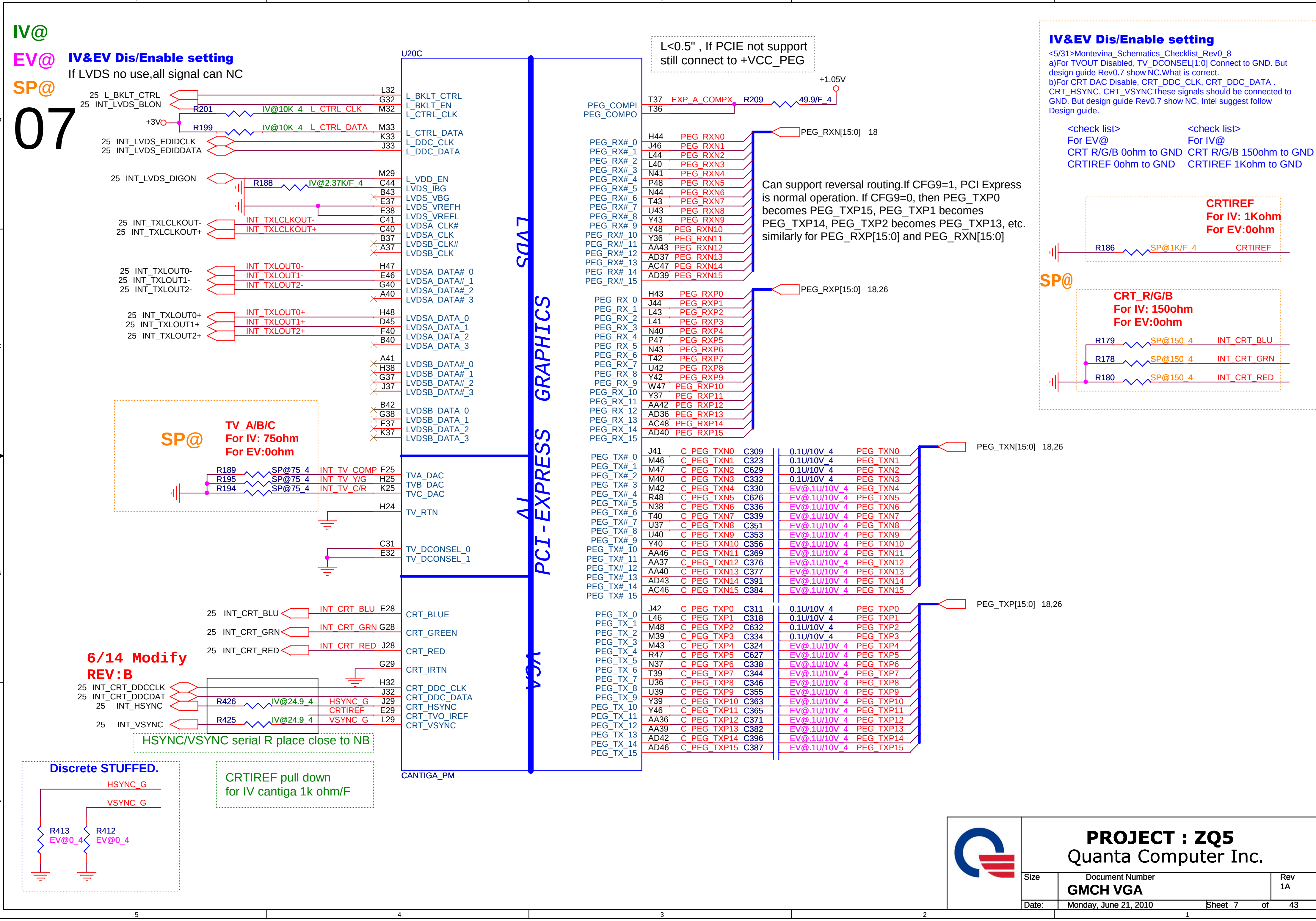
Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present





GMCH (CANTIGA)



IV@
EV@
SP@
07
IV&EV Dis/Enable setting
If LVDS no use,all signal can NC
U20C
L<0.5" , If PCIE not support still connect to +VCC_PEG
+1.05V
25 L_BKLT_CTRL
25 INT_LVDS_BLON
R201
IV@10K_4
L_CTRL_CLK
+3V
R199
IV@10K_4
L_CTRL_DATA
25 INT_LVDS_EDIDCLK
25 INT_LVDS_EDIDDATA
25 INT_LVDS_DIGON
R188
IV@2.37K/F_4
25 INT_TXLCLKOUT-
25 INT_TXLCLKOUT+
INT_TXLCLKOUT-
INT_TXLCLKOUT+
25 INT_TXLOUT0-
25 INT_TXLOUT1-
25 INT_TXLOUT2-
25 INT_TXLOUT0+
25 INT_TXLOUT1+
25 INT_TXLOUT2+
L_BKLT_CTRL
L_BKLT_EN
L_CTRL_CLK
L_CTRL_DATA
L_DDC_CLK
L_DDC_DATA
L_VDD_EN
LVDS_IBG
LVDS_VBG
LVDS_VREFH
LVDS_VREFL
LVDSA_CLK#
LVDSA_CLK
LVDSB_CLK#
LVDSB_CLK
LVDSA_DATA#_0
LVDSA_DATA#_1
LVDSA_DATA#_2
LVDSA_DATA#_3
LVDSA_DATA_0
LVDSA_DATA_1
LVDSA_DATA_2
LVDSA_DATA_3
LVDSB_DATA#_0
LVDSB_DATA#_1
LVDSB_DATA#_2
LVDSB_DATA#_3
LVDSB_DATA_0
LVDSB_DATA_1
LVDSB_DATA_2
LVDSB_DATA_3
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
SP@
TV_A/B/C
For IV: 75ohm
For EV:0ohm
R189 SP@75_4 INT_TV_COMP
R195 SP@75_4 INT_TV_Y/G
R194 SP@75_4 INT_TV_C/R
TVA_DAC
TVB_DAC
TVC_DAC
TV_RTN
TV_DCONSEL_0
TV_DCONSEL_1
25 INT_CRT_BLU
25 INT_CRT_GRN
25 INT_CRT_RED
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_IRTN
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_TVO_IREF
CRT_VSYNC
6/14 Modify
REV:B
25 INT_CRT_DDCCLK
25 INT_CRT_DDCDAT
25 INT_HSYNC
25 INT_VSYNC
R426 IV@24.9_4 HSYNC_G
CRTIREF
R425 IV@24.9_4 VSYNC_G
HSYNC/VSYNC serial R place close to NB
Discrete STUFFED.
HSYNC_G
VSYNC_G
R413 EV@0_4
R412 EV@0_4
CRTIREF pull down
for IV cantiga 1k ohm/F
CANTIGA_PM
PEG_COMPI
PEG_COMPO
T37 EXP_A_COMPX R209 49.9/F_4
PEG_RXN[15:0] 18
PEG_RXP[15:0] 18,26
PEG_TXN[15:0] 18,26
PEG_TXP[15:0] 18,26
Can support reversal routing.If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG_TXP0 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]
0.1U/10V_4
EV@.1U/10V_4
IV&EV Dis/Enable setting
<5/31>Montevina_Schematics_Checklist_Rev0_8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA . CRT_HSYNC, CRT_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.
<check list>
For EV@
CRT R/G/B 0ohm to GND
CRTIREF 0ohm to GND
<check list>
For IV@
CRT R/G/B 150ohm to GND
CRTIREF 1Kohm to GND
CRTIREF
For IV: 1Kohm
For EV:0ohm
R186 SP@1K/F_4 CRTIREF
SP@
CRT_R/G/B
For IV: 150ohm
For EV:0ohm
R179 SP@150_4 INT_CRT_BLU
R178 SP@150_4 INT_CRT_GRN
R180 SP@150_4 INT_CRT_RED
PROJECT : ZQ5
Quanta Computer Inc.
Size
Document Number
GMCH VGA
Rev
1A
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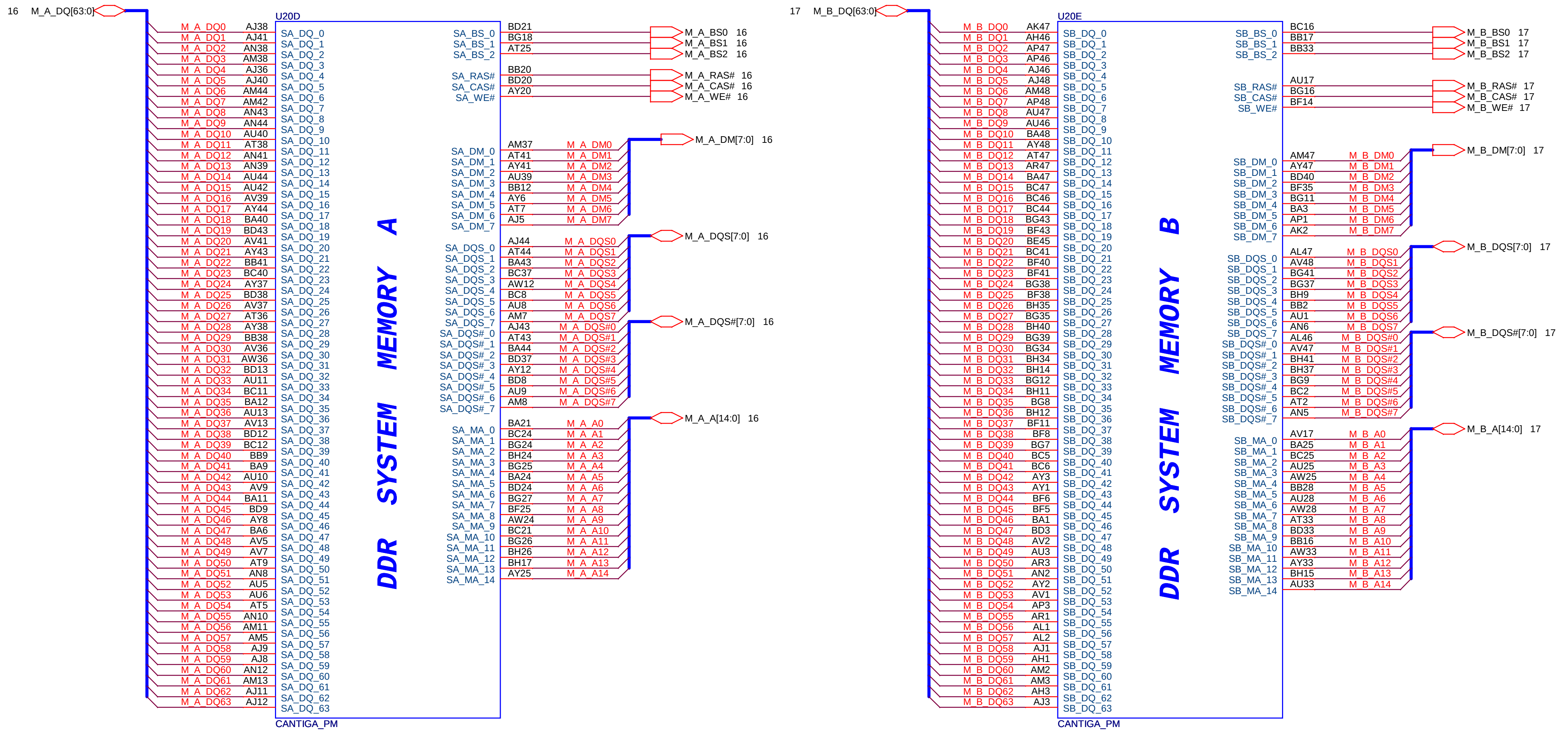

GMCH (CANTIGA)

PROJECT : ZQ5 Quanta Computer Inc.		
Size	Document Number GMCH DDRII	Rev 1A
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IV@

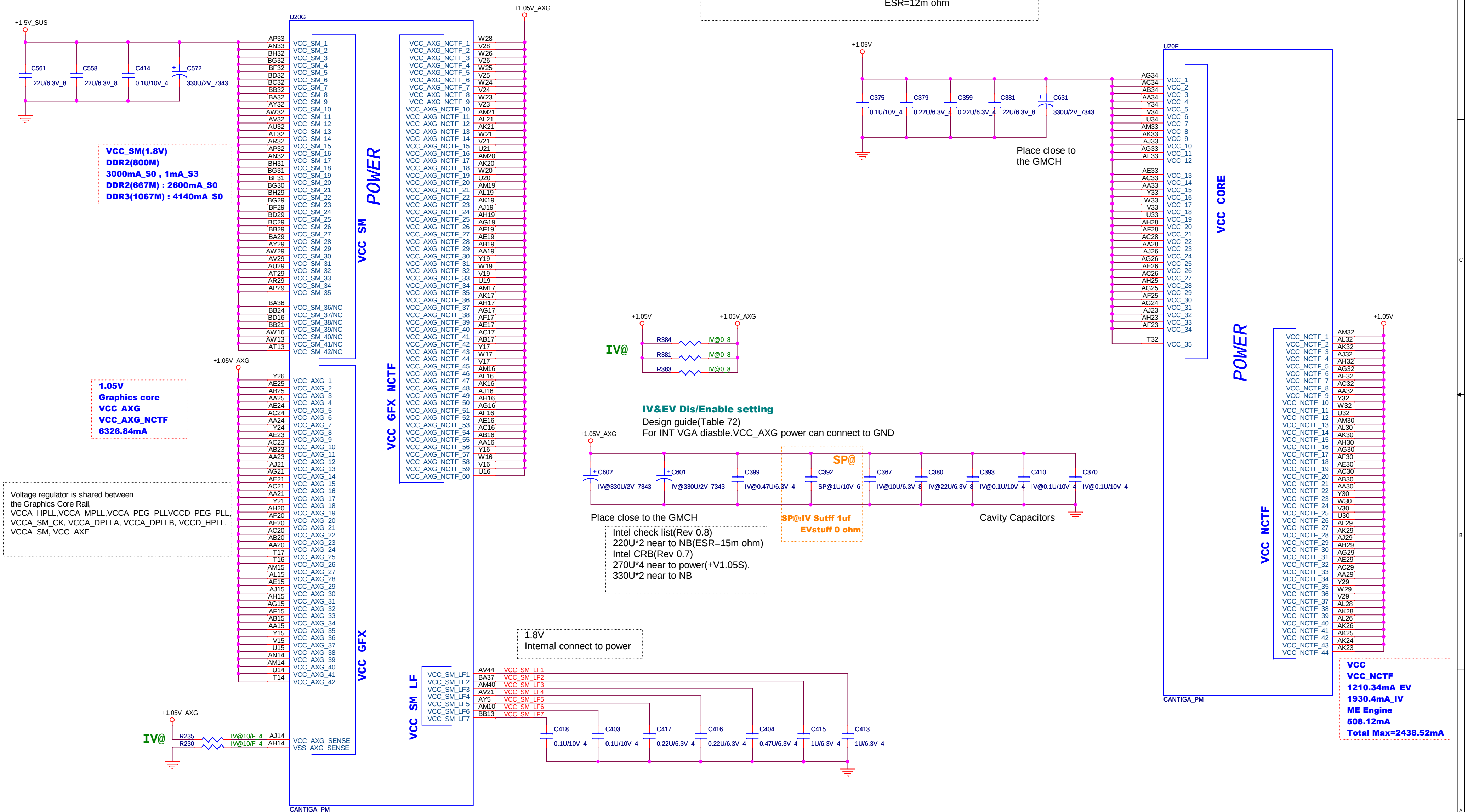
SP@

Power consumption reference to Intel 644135 Cantiga chipset EDS Volume1. Section 10

GM TDP 10.5~12W
GS TDP 7~8W
PM TDP 7W

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm



Place close to the GMCH

VCC_SM(1.8V)
DDR2(800M)
3000mA_S0 , 1mA_S3
DDR2(667M) : 2600mA_S0
DDR3(1067M) : 4140mA_S0

IV@

IV&EV Dis/Enable setting
Design guide(Table 72)
For INT VGA diasble.VCC_AXG power can connect to GND

1.05V
Graphics core
VCC_AXG
VCC_AXG_NCTF
6326.84mA

Voltage regulator is shared between the Graphics Core Rail, VCCA_HPLL,VCCA_MPLL,VCCA_PEG_PLLVCCD_PEG_PLL, VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL, VCCA_SM, VCC_AXF

SP@

Place close to the GMCH

SP@:IV Sutff 1uf
EVstuff 0 ohm

Cavity Capacitors

Intel check list(Rev 0.8)
220U*2 near to NB(ESR=15m ohm)
Intel CRB(Rev 0.7)
270U*4 near to power(+V1.05S).
330U*2 near to NB

1.8V
Internal connect to power

IV@

VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

GMCH (CANTIGA)

PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH VCC,NCTF	1A
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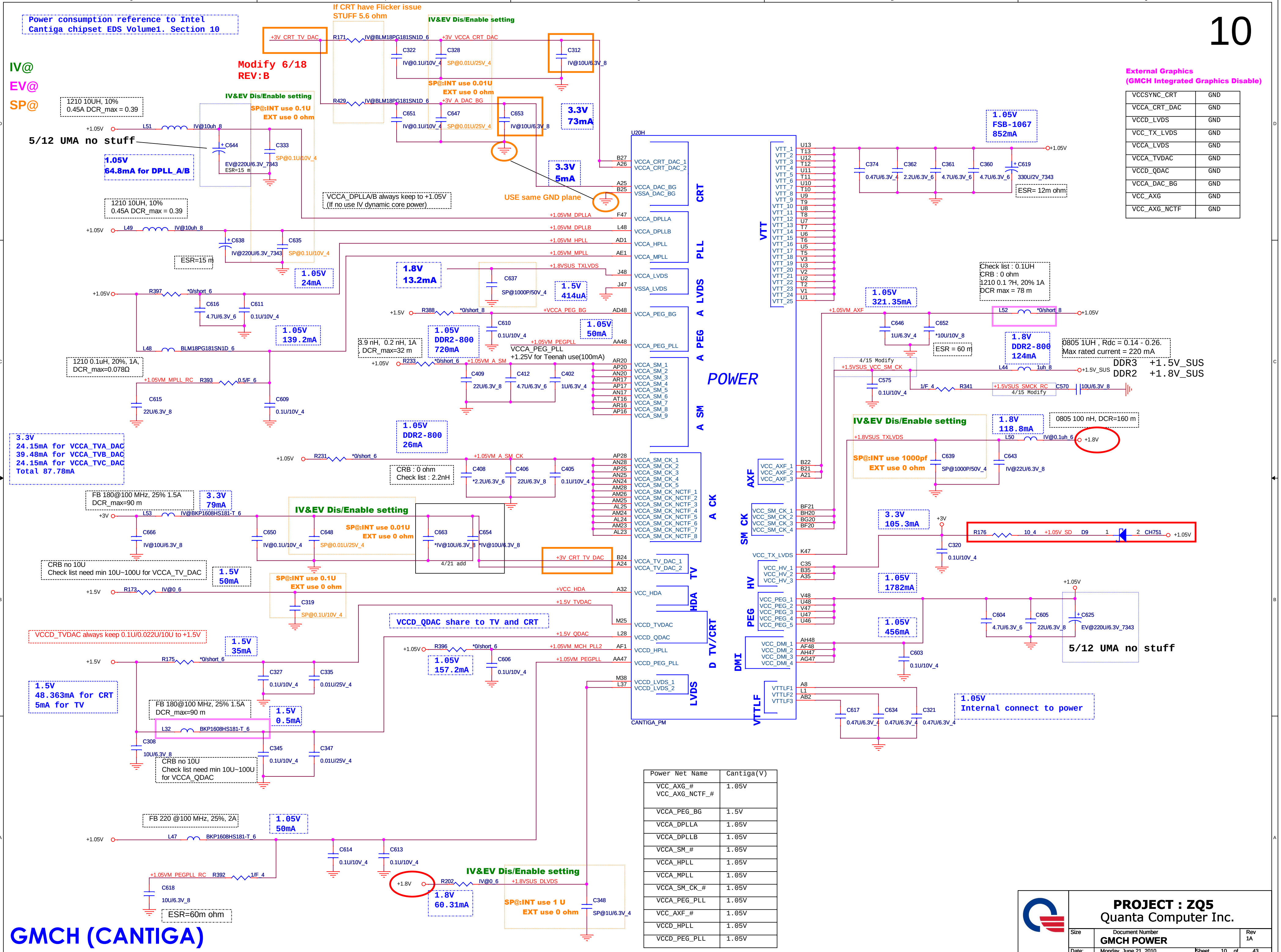

GMCH (CANTIGA)

External Graphics
(GMCH Integrated Graphics Disable)

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TVDAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

Power Net Name	Cantiga(V)
VCC_AXG_# VCC_AXG_NCTF_#	1.05V
VCCA_PEG_BG	1.5V
VCCA_DPLLA	1.05V
VCCA_DPLLB	1.05V
VCCA_SM_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCCA_SM_CK_#	1.05V
VCCA_PEG_PLL	1.05V
VCC_AXF_#	1.05V
VCCD_HPLL	1.05V
VCCD_PEG_PLL	1.05V

PROJECT : ZQ5
Quanta Computer Inc.

Size | Document Number: GMCH POWER | Rev 1A
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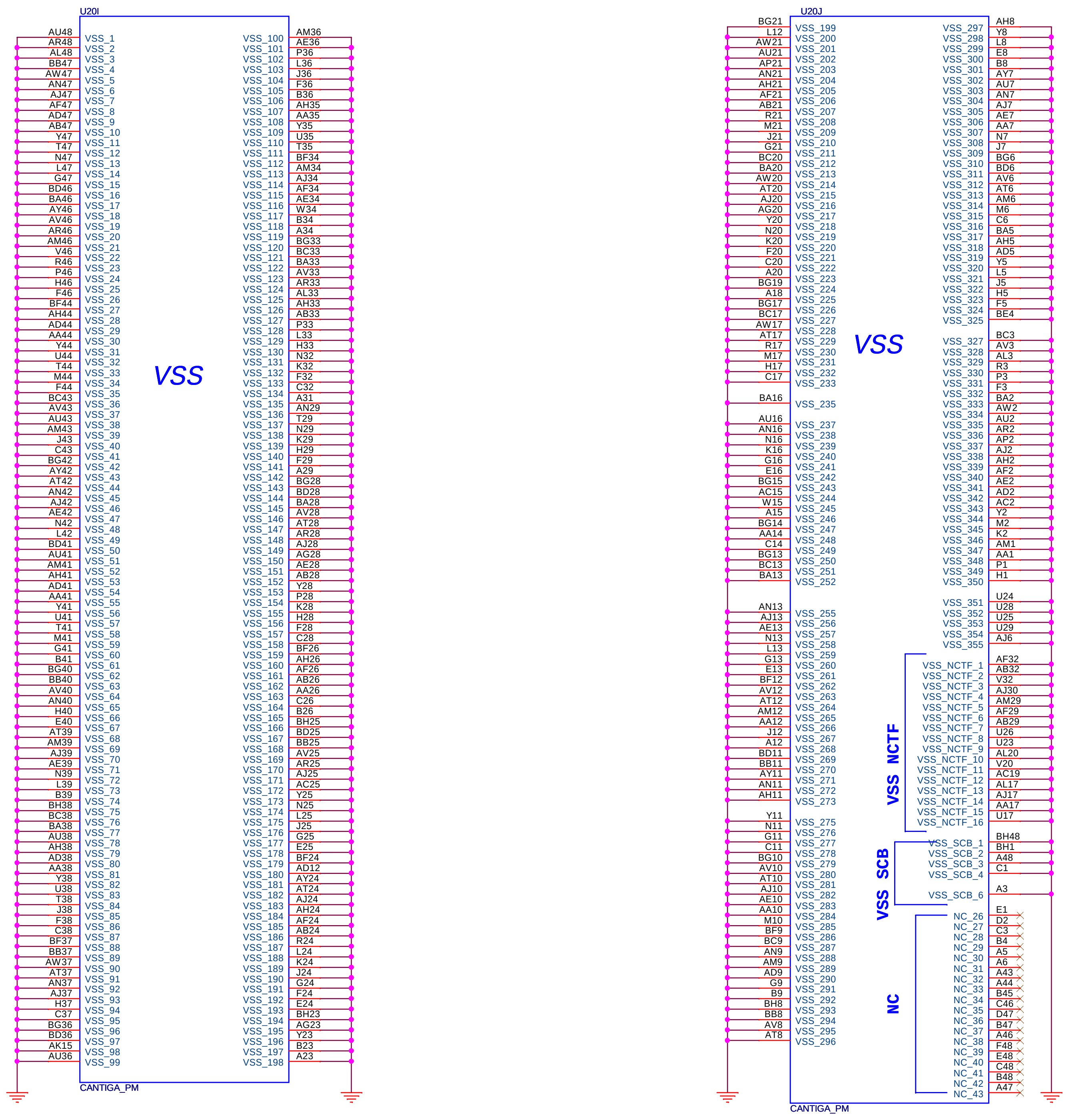

GMCH (CANTIGA)

PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH VSS	1A
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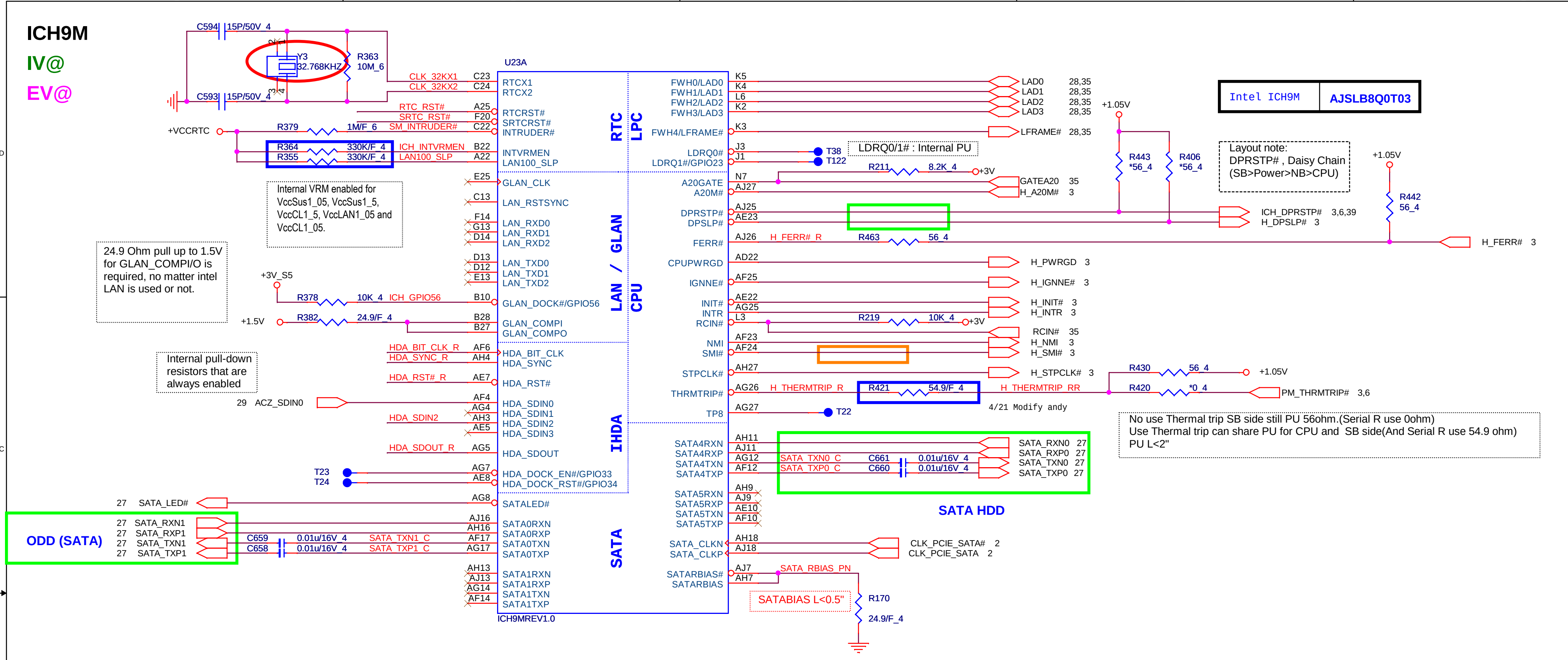
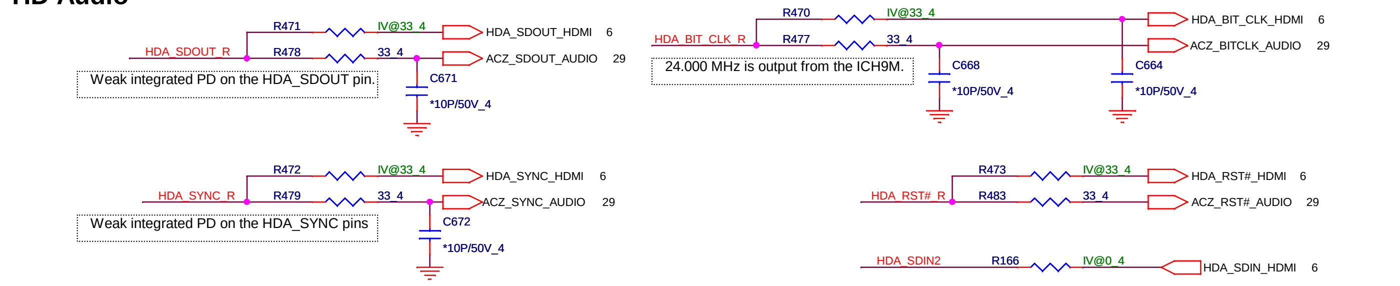
ICH9M

IV@

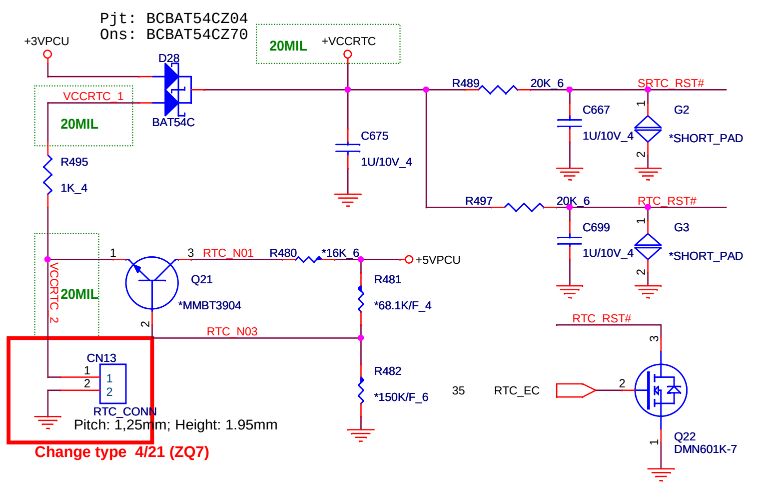
EV@



HD Audio



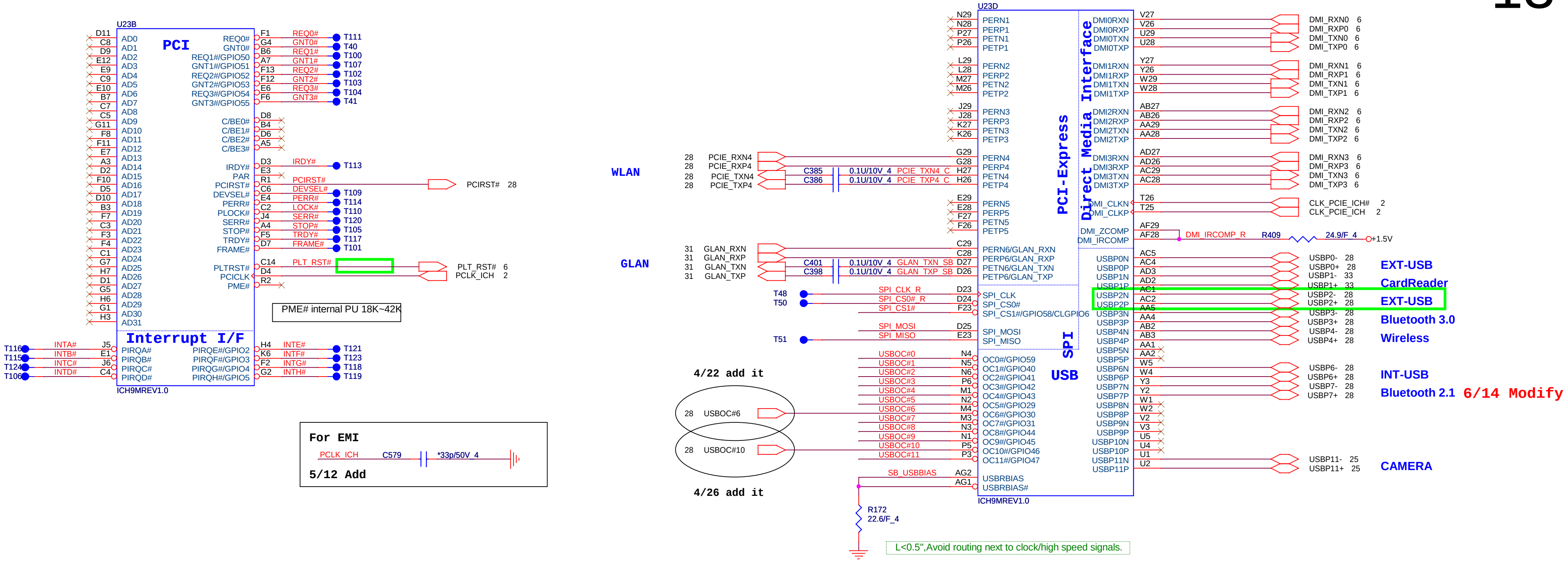
RTC

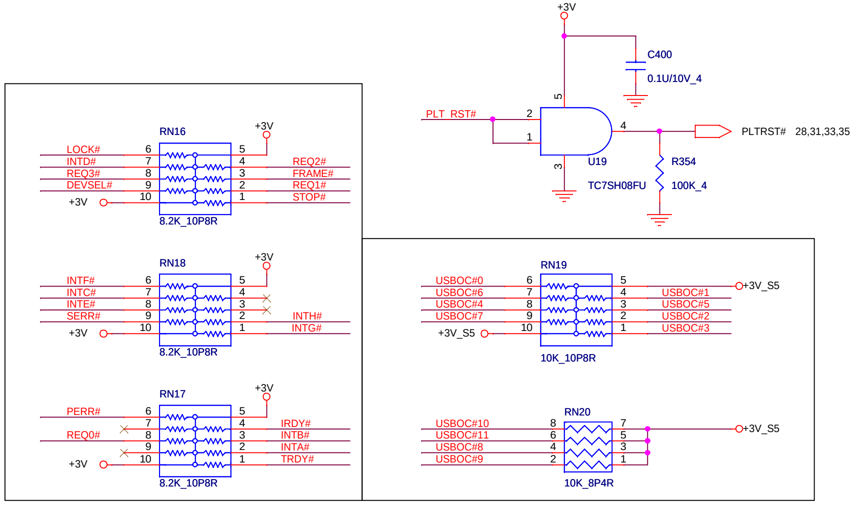


South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	see table below	14 ICH_TP3 — ICH_TP3 R370 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	see table below	HDA_SDOUT_R R440 *1K_4 +3V

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1



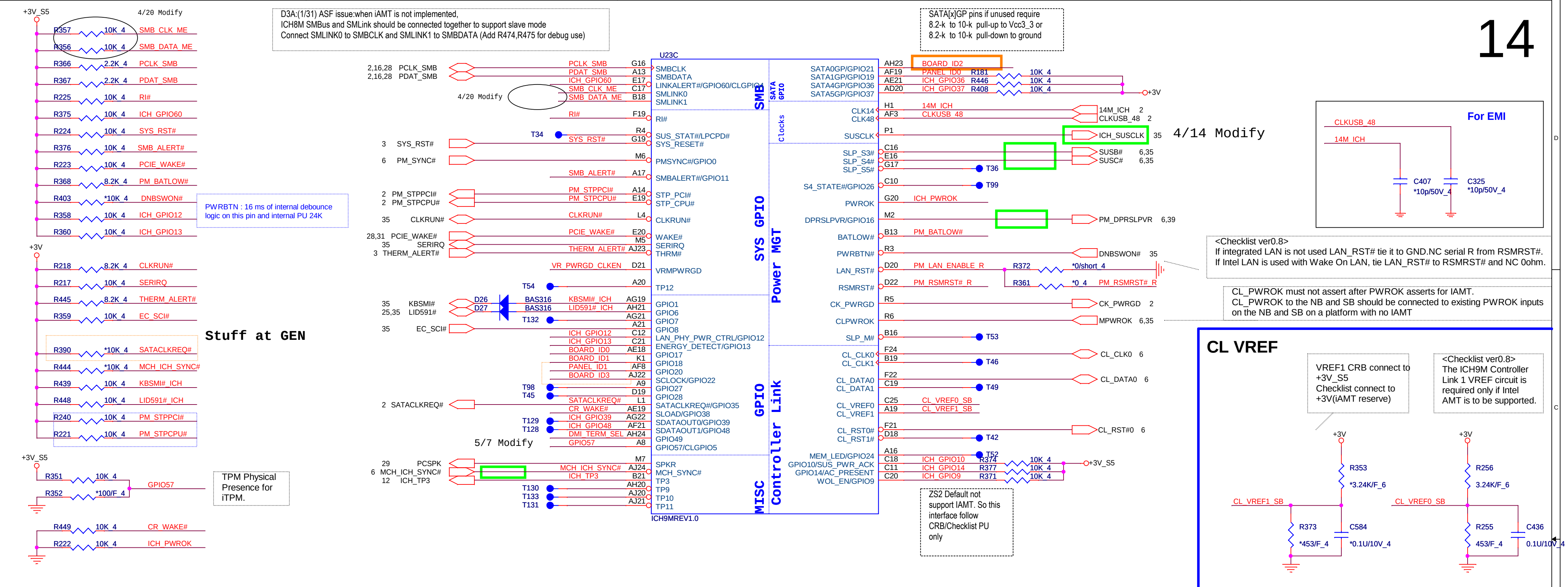


5/11 Swap

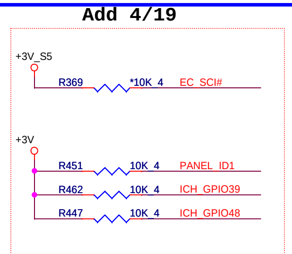
5/11 Swap

South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R237 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI R380 *10K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI	GNT0# R236 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1 / 0 / PCI 1 / 1 / LPC(Default)	SPI_CS1# R234 *1K_4

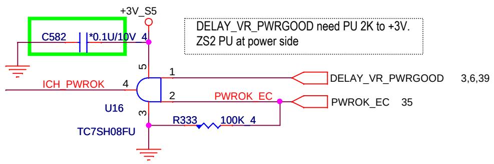


Add 4/19

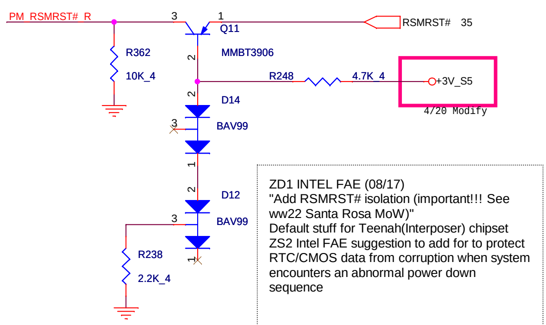


Follow CHECK LIST V1.5

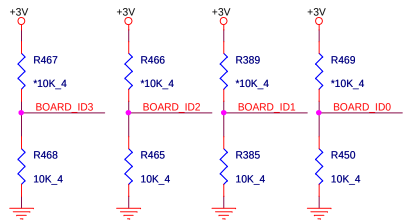
ICH PWROK



Resume RST



M/B ID

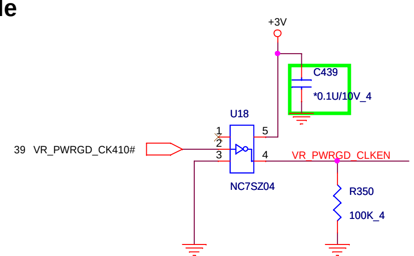


Board ID	ID3	ID2	ID1	ID0
default	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R216 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R464 *1K_4

CLK Enable

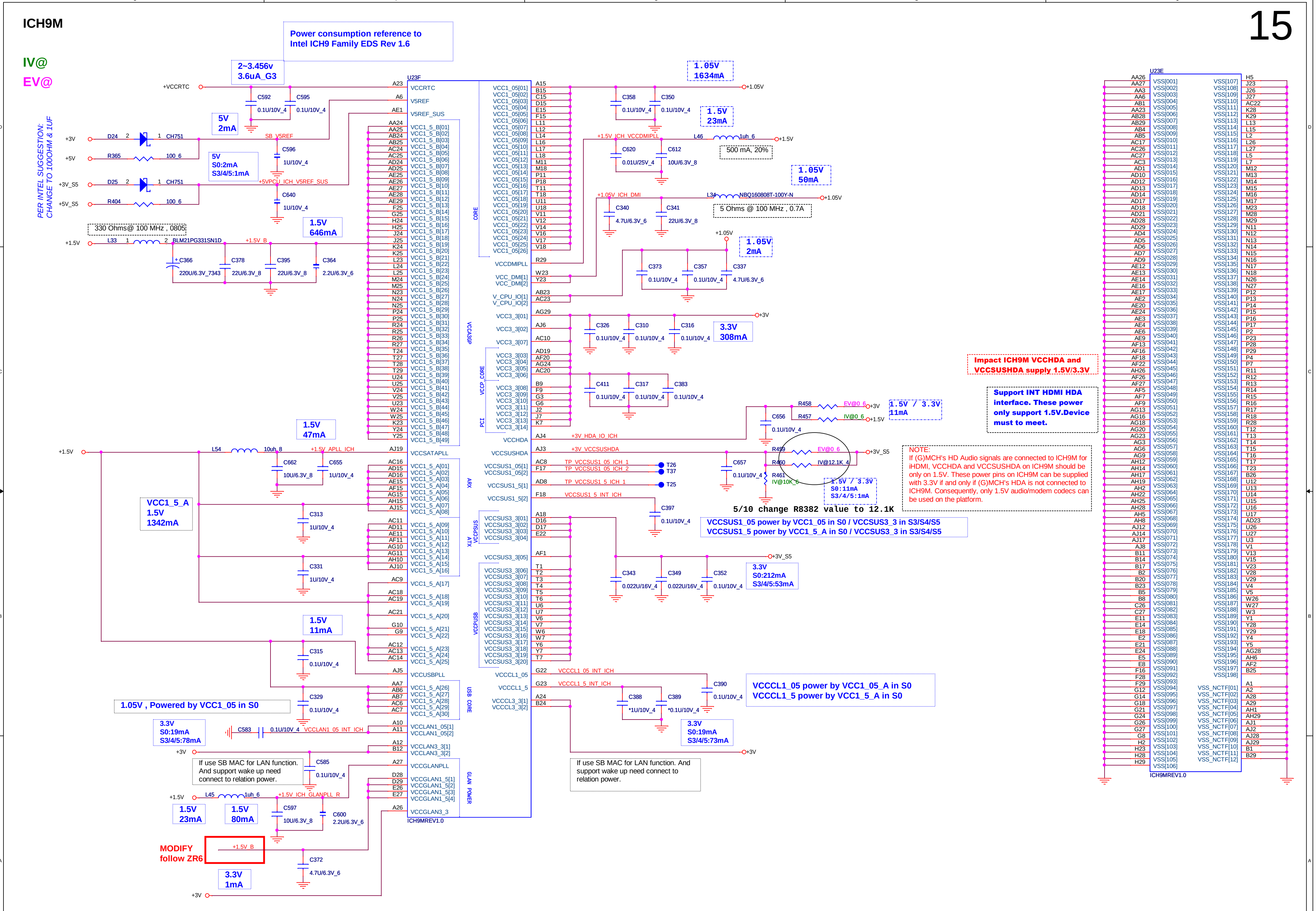


PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	ICH9M GPIO	1A

Date: Monday, June 21, 2010 Sheet 14 of 43

ICH9M



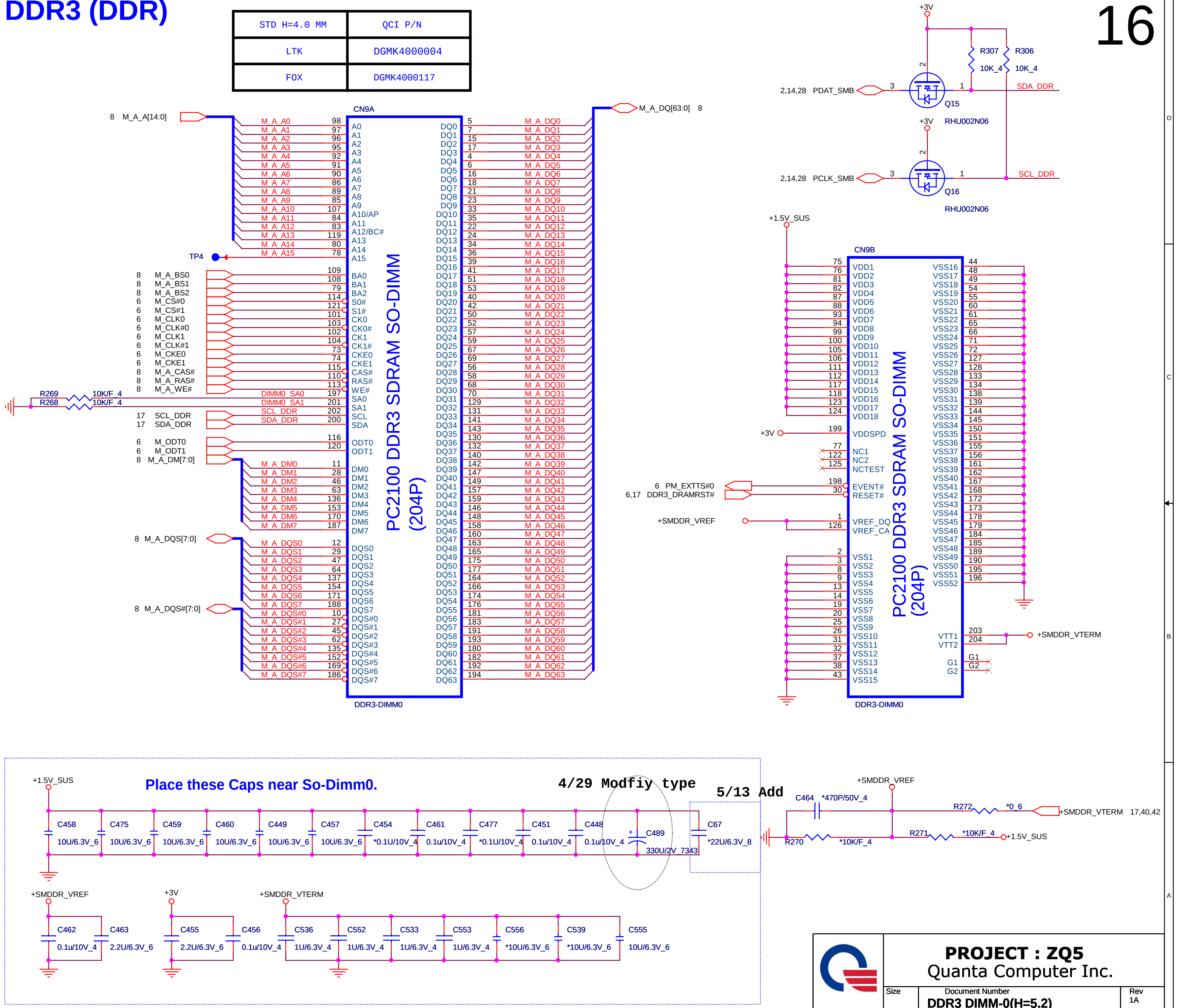
PROJECT : ZQ5

Quanta Computer Inc.

Size	Document Number	Rev
	ICH9 POWER	1A
Date: Monday, June 21, 2010	Sheet 15 of 43	

DDR3 (DDR)

STD H=4.0 MM	QCI P/N
LTK	DGMK4000004
FOX	DGMK4000117



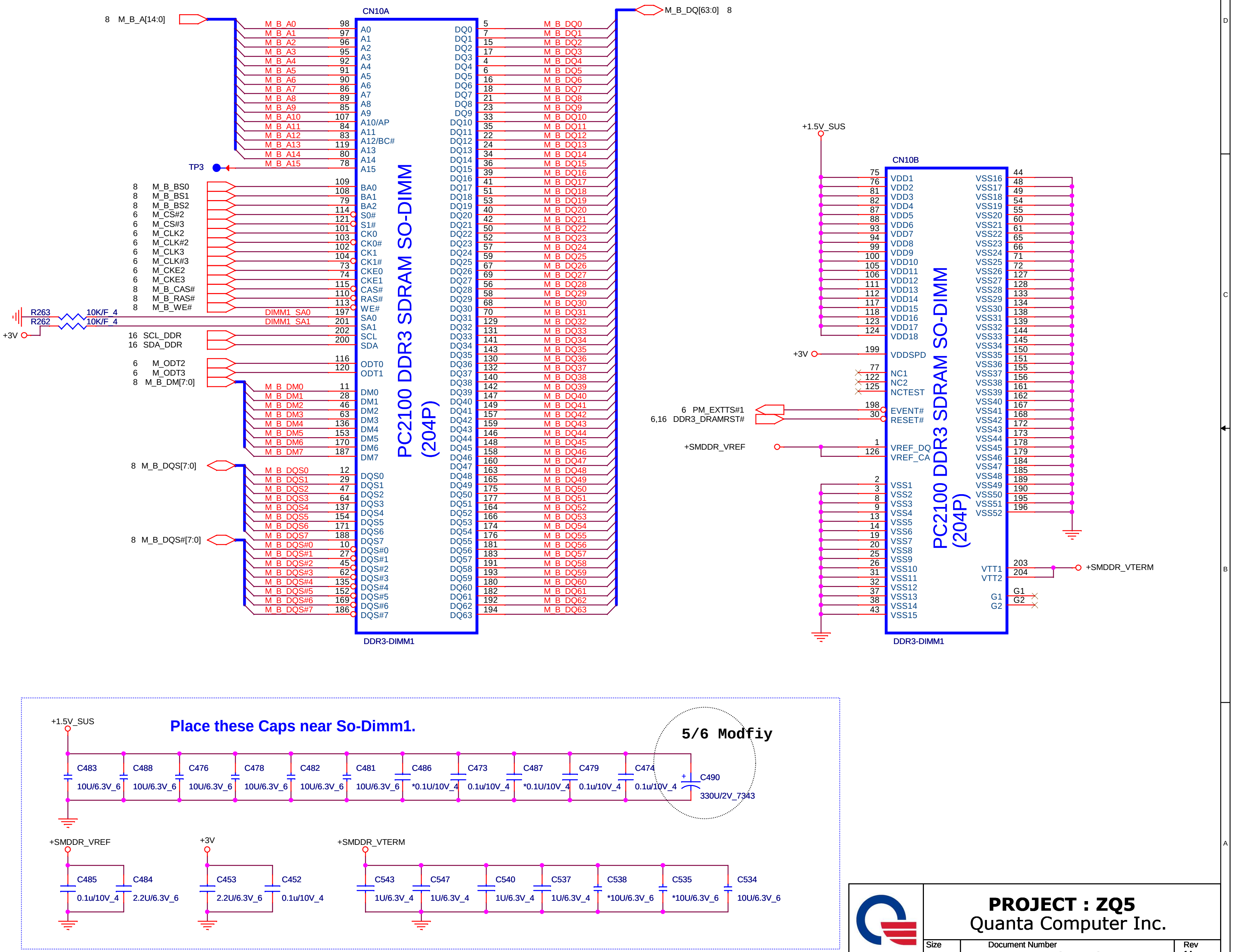
PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	DDR3 DIMM-0(H=5.2)	1A

Date: Monday, June 21, 2010 Sheet 16 of 43

DDR3 (DDR)

STD H=8.0 MM	QCI P/N
LTK	DGMK4000097
FOX	DGMK4000130



PROJECT : ZQ5

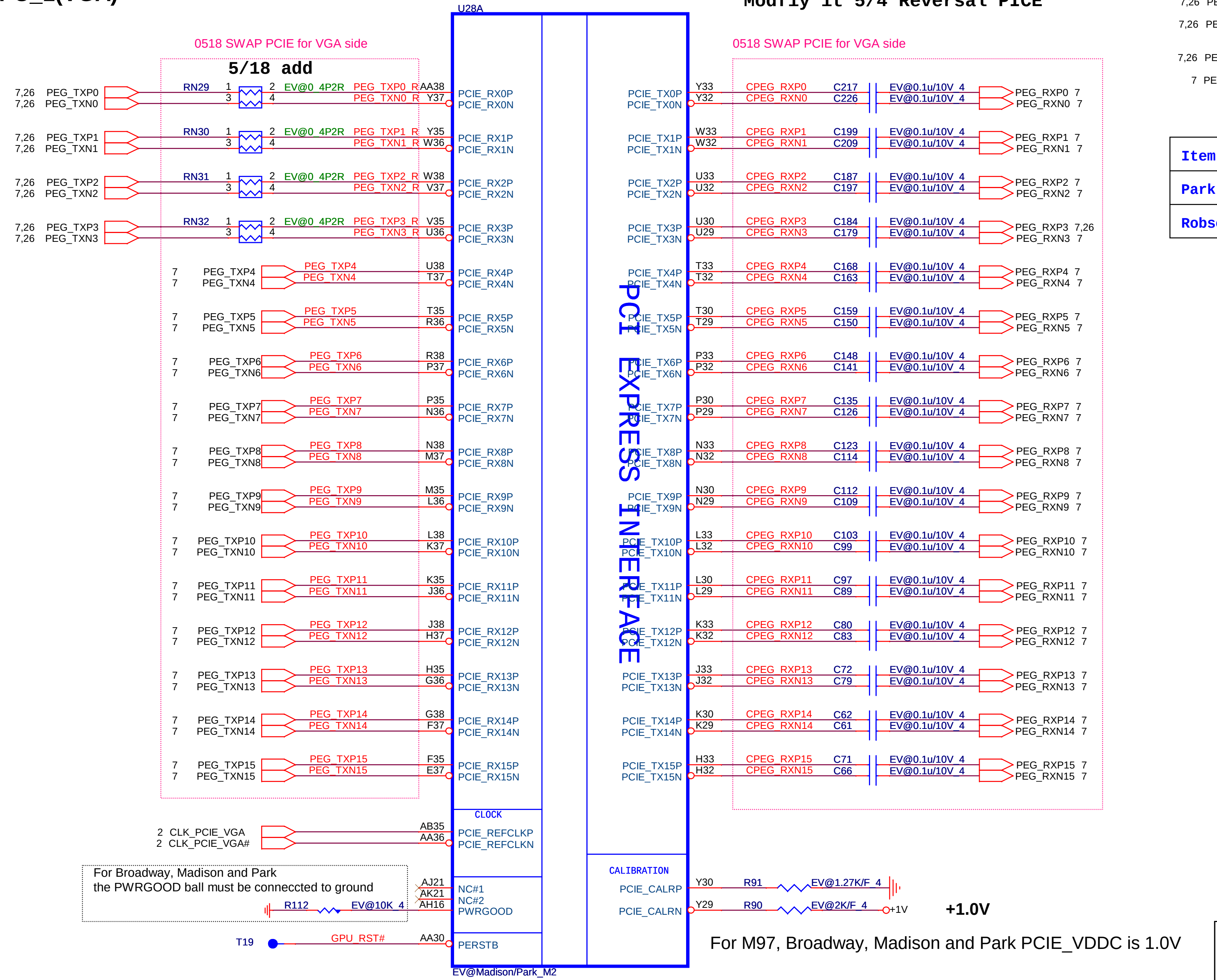
Quanta Computer Inc.

Size	Document Number	Rev
	DDR3 DIMM-1(H=9.2)	1A

Date: Monday, June 21, 2010 Sheet 17 of 43

GPU_1(VGA)

Modfiy it 5/4 Reversal PICE



7,26 PEG_TXP[0..15] — PEG_TXP[0..15]
7,26 PEG_TXN[0..15] — PEG_TXN[0..15]
7,26 PEG_RXP[0..15] — PEG_RXP[0..15]
7 PEG_RXN[0..15] — PEG_RXN[0..15]

Item	Quanta P/N
Park	AJ077400T08
Robson	AJ007740T02

For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

Quanta Computer Inc.

PROJECT : ZQ5

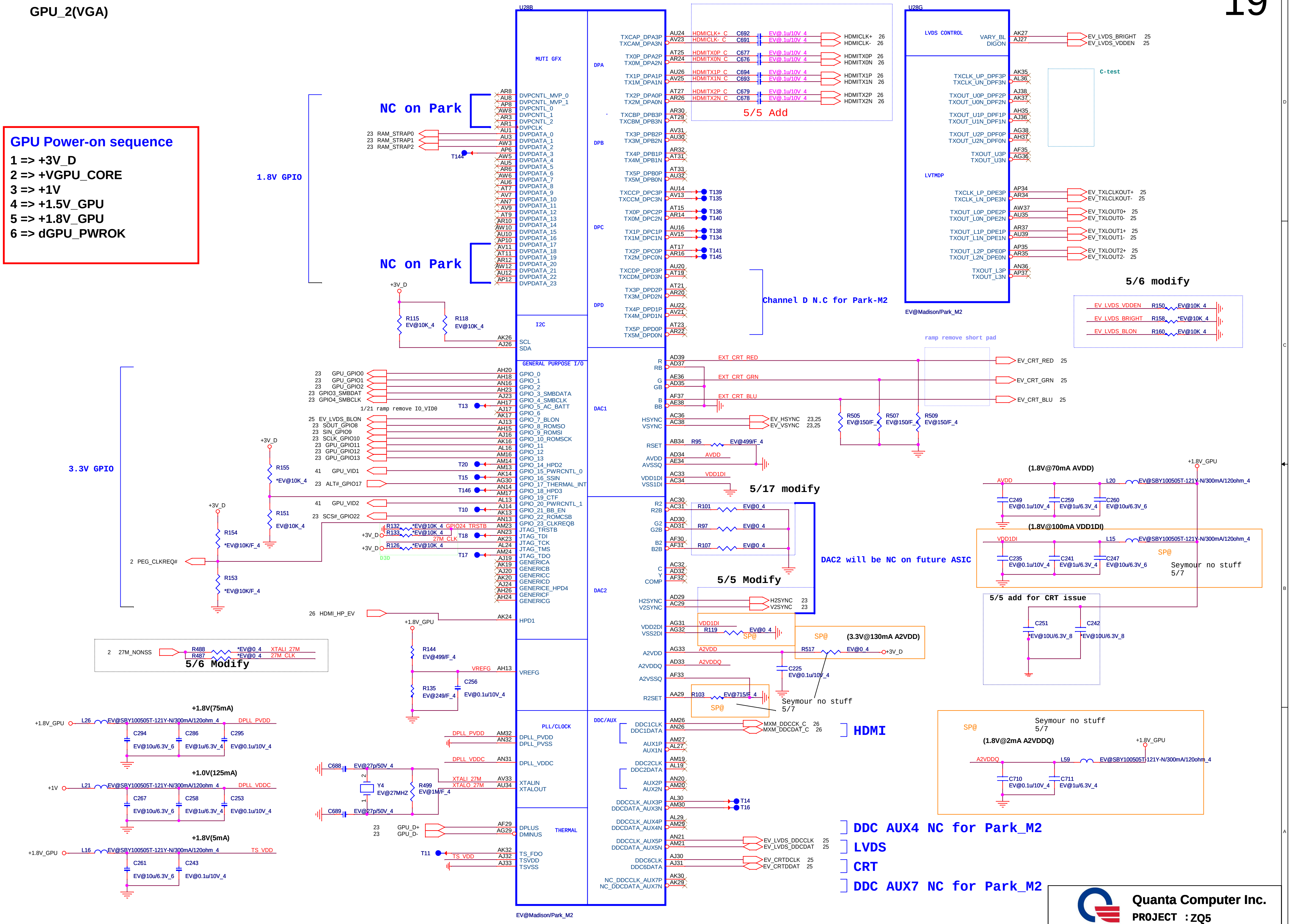
Size	Document Number	Rev
	Madison/Park M2-PCIE I/F	1A

Date: Monday, June 21, 2010 Sheet 18 of 45

GPU_2(VGA)

GPU Power-on sequence

1 => +3V_D
2 => +VGPU_CORE
3 => +1V
4 => +1.5V_GPU
5 => +1.8V_GPU
6 => dGPU_PWROK



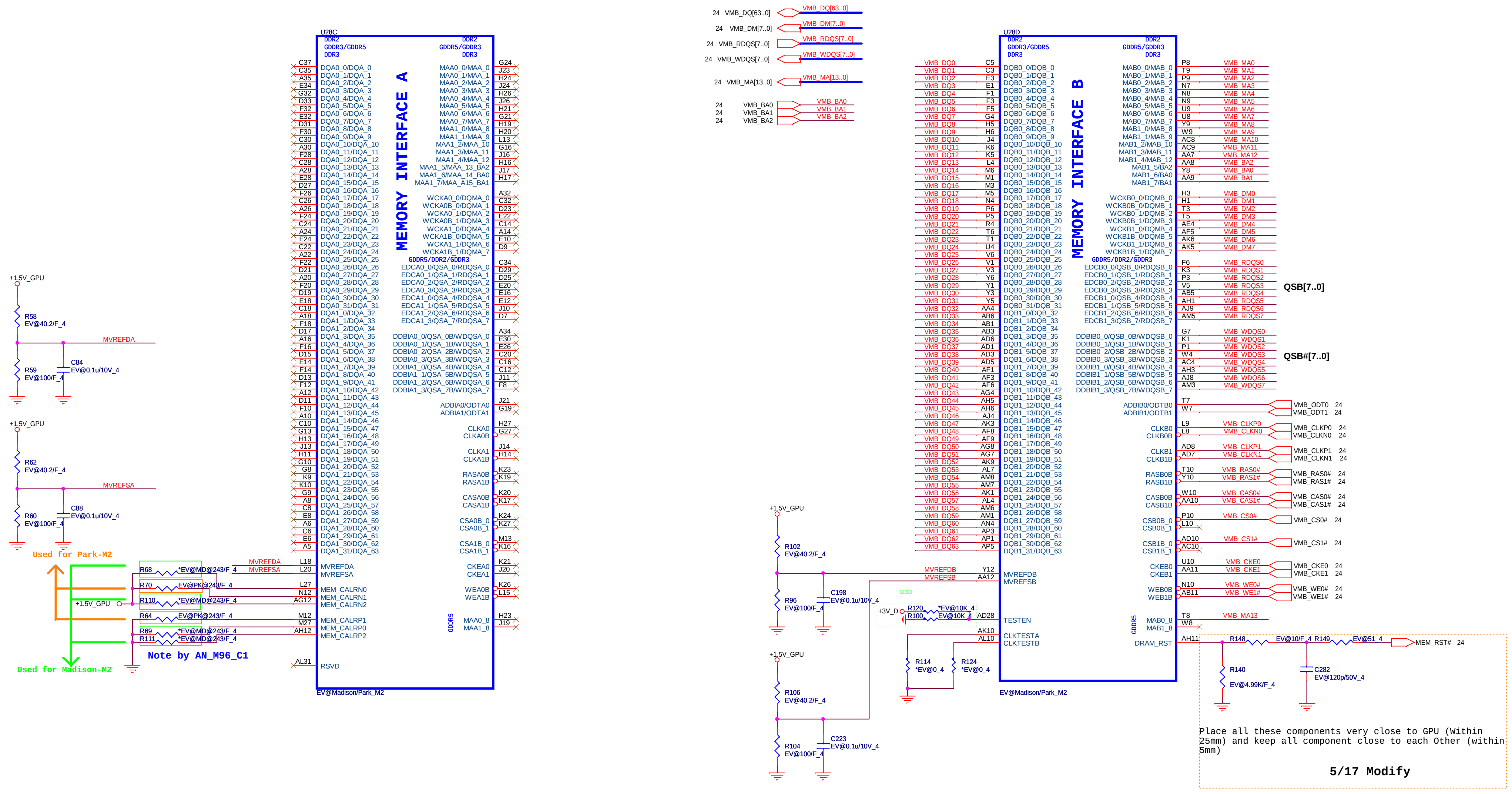
Quanta Computer Inc.

PROJECT : ZQ5

Size	Document Number	Rev
	Madison/Park M2-HOST I/F	1A

Date: Monday, June 21, 2010 Sheet 19 of 45

Park M2-channel B used(S3 package use Channel A)



Quanta Computer Inc.

PROJECT : ZQ5

Size	Document Number	Rev
	Madison/Park M2-MEM I/F	1A

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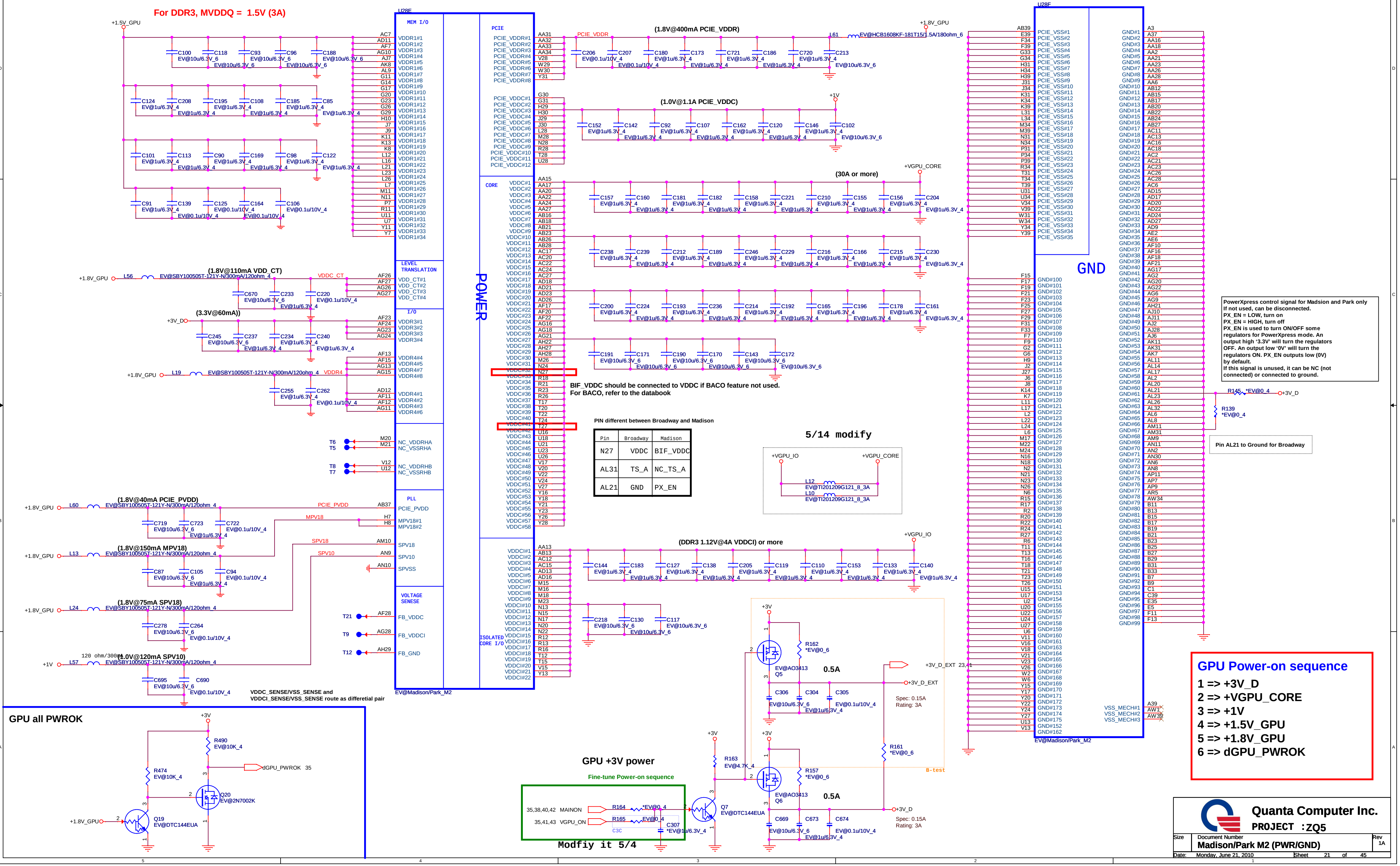
GPU_4(VGA)



PIN different between Broadway and Madison

Pin	Broadway	Madison
N27	VDDC	BIF_VDDC
AL31	TS_A	NC_TS_A
AL21	GND	PX_EN

PowerXpress control signal for Madsion and Park only
If not used, can be disconnected.
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
PX_EN is used to turn ON/OFF some regulators for PowerXpress mode. An output high '3.3V' will turn the regulators OFF. An output low '0V' will turn the regulators ON. PX_EN outputs low (0V) by default.
If this signal is unused, it can be NC (not connected) or connected to ground.

GPU Power-on sequence

1 => +3V_D
2 => +VGPU_CORE
3 => +1V
4 => +1.5V_GPU
5 => +1.8V_GPU
6 => dGPU_PWROK

Quanta Computer Inc.
PROJECT : ZQ5

Size	Document Number	Rev
	Madison/Park M2 (PWR/GND)	1A

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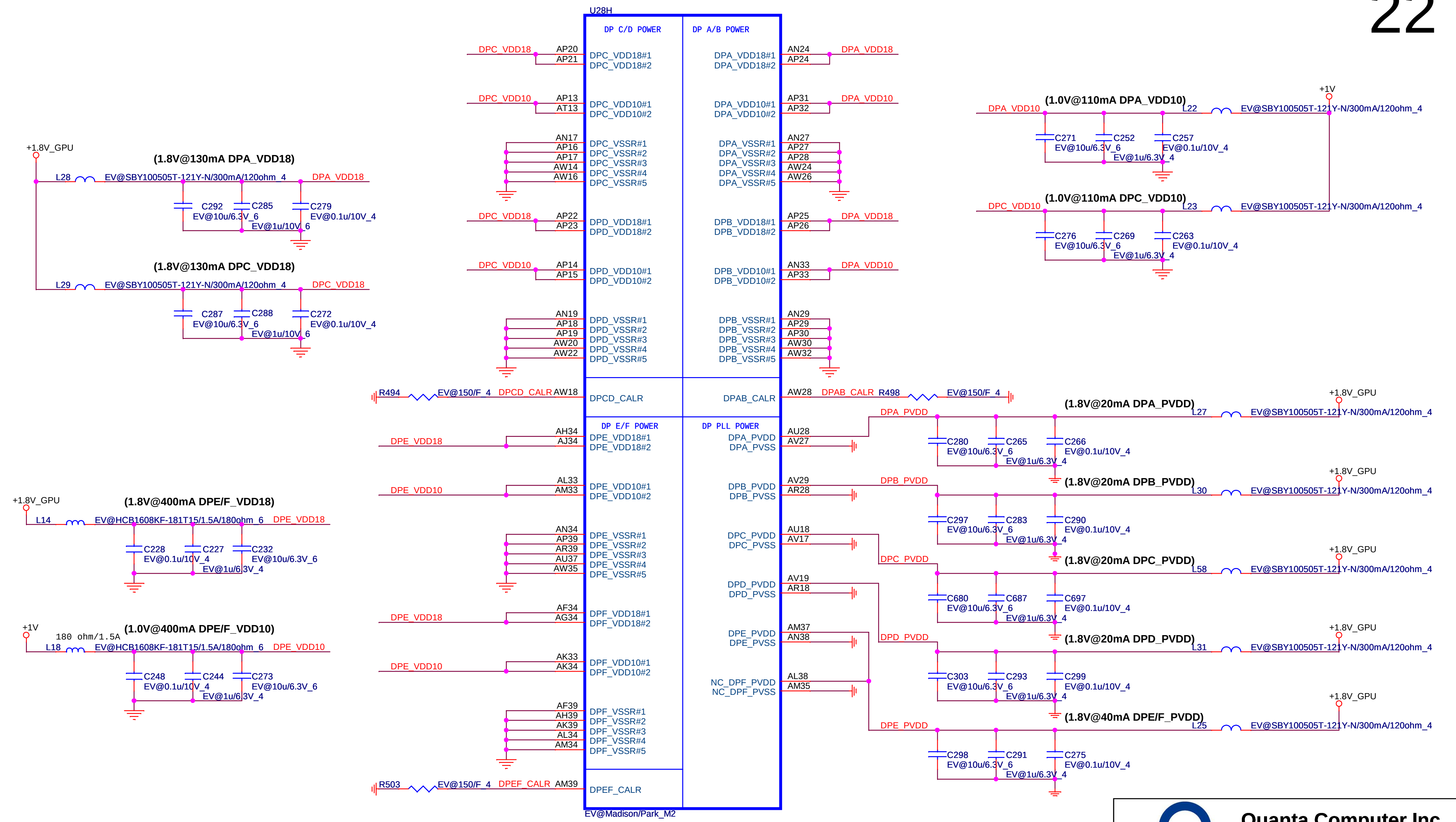
GPU_5(VGA)



Quanta Computer Inc.

PROJECT : ZQ5

Size	Document Number	Rev
	Madison/Park M2 (DP_PWR/GND)	1A
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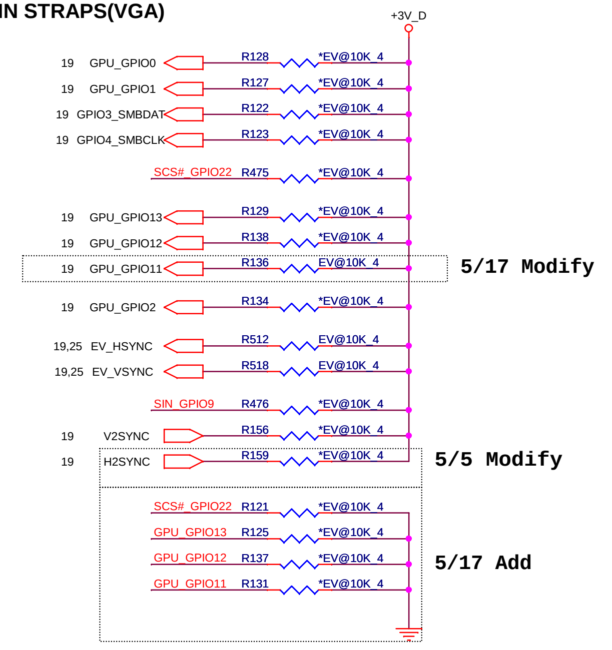
PIN STRAPS(VGA)



ROM Table	
Size of the primary memory apertures	CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
32 MB	011

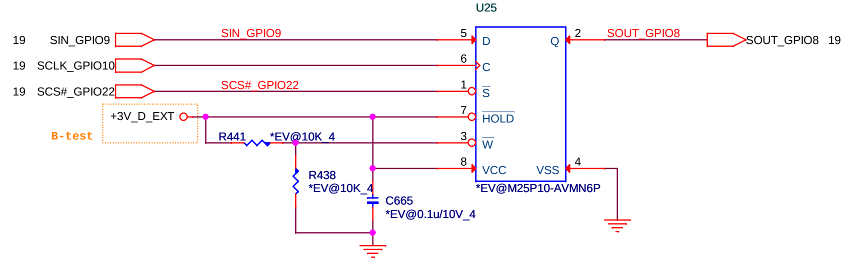
ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	1	
ROMIDCFG(2:0)	GPIO[13:11]	Primary Memory Aperture size requested at PCI Configuration	001	table 3-35
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM(VGA)

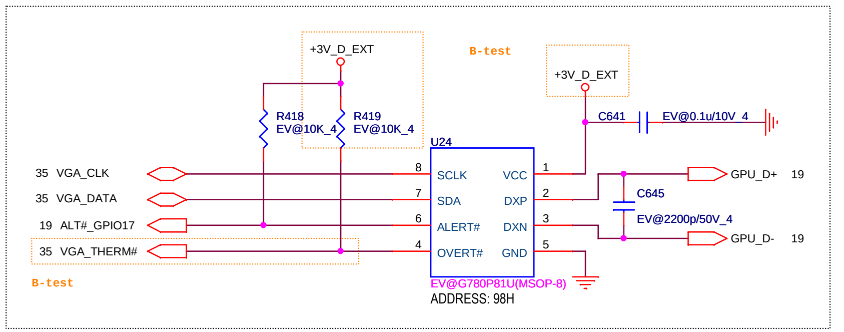


Thermal Sensor(VGA)

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

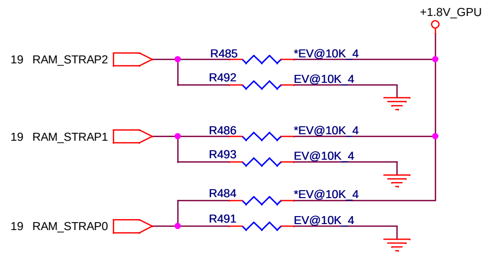
USD0.16

5/6 modify



DDR3 Memory Aperture size(GPU)

DDR3 Memory Aperture size					
Vendor	Vendor P/N	STN B/S P/N	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1	0	0
			1	0	1
Samsung					
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500 (128M*16)	0	0	1



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

Quanta Computer Inc.

PROJECT : ZQ5

Size	Document Number	Rev
	Strip/Thermal	1A

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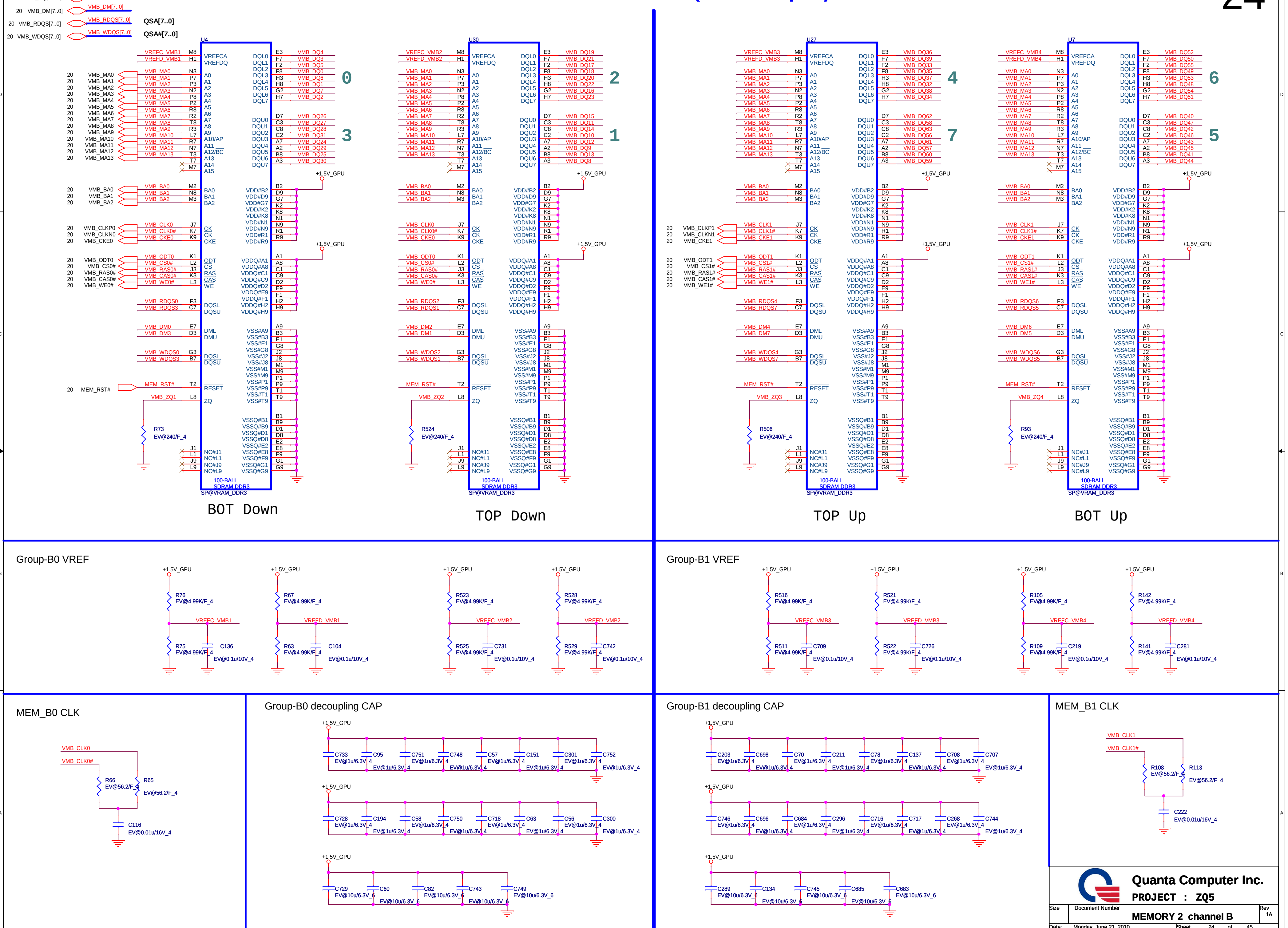
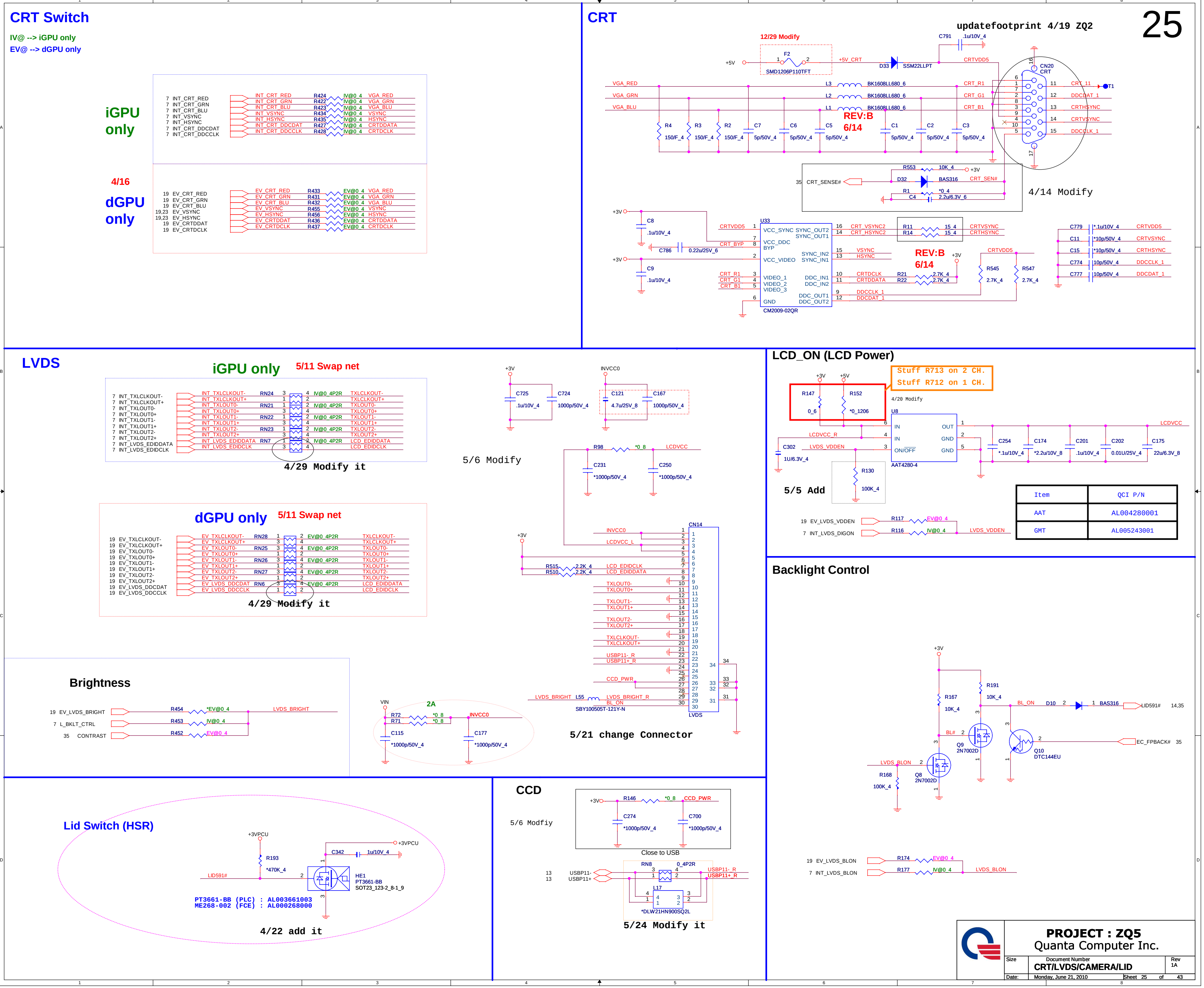
CHANNEL B: 512MB DDR3 (16*64M*4pcs)



Quanta Computer Inc.		
PROJECT : ZQ5		
Size	Document Number: MEMORY 2 channel B	Rev 1A
Date: Monday, June 21, 2010	Sheet 24 of 45	

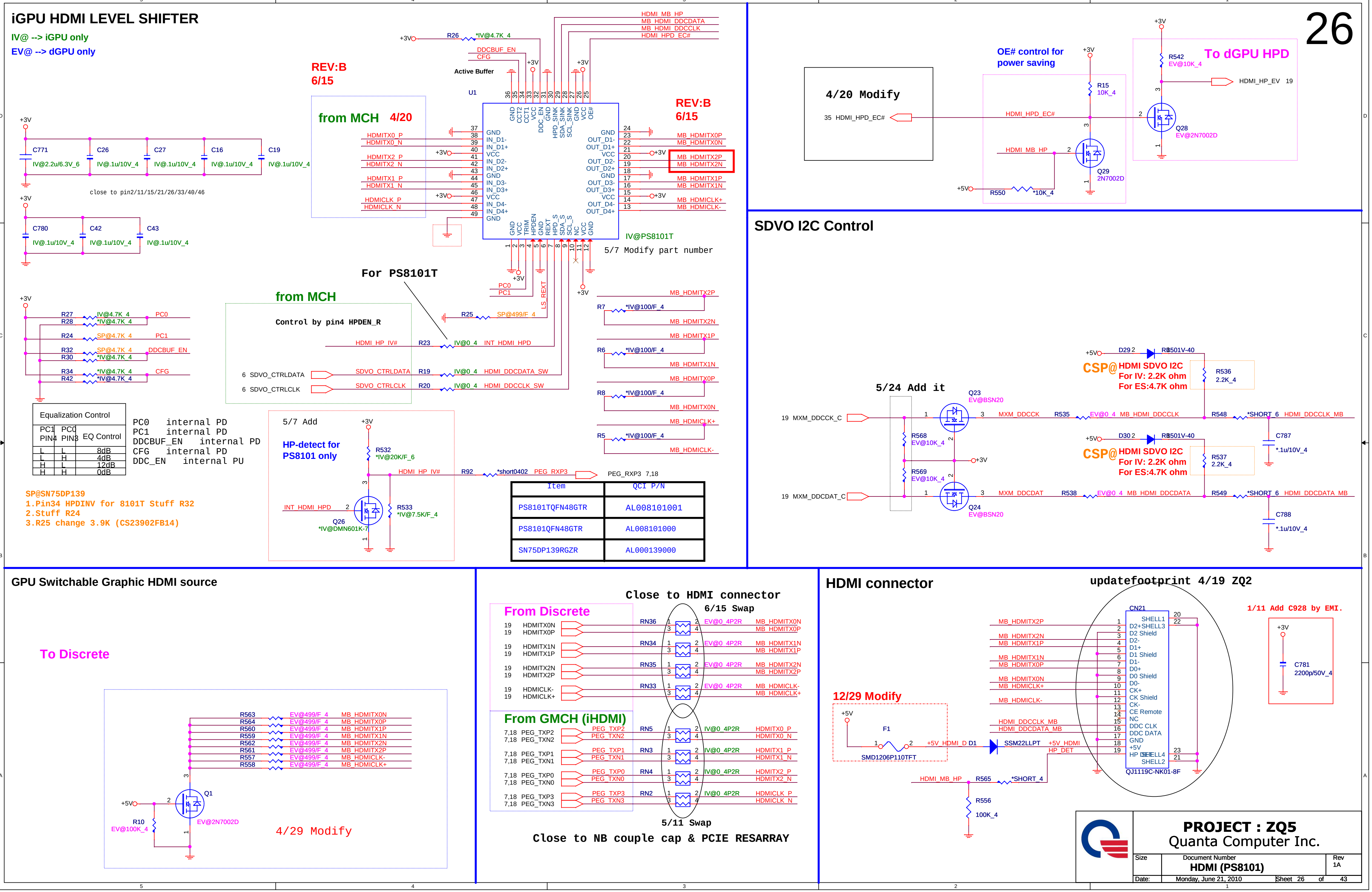


PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1A

Date: Monday, June 21, 2010 — Sheet 25 of 43

iGPU HDMI LEVEL SHIFTER



Item	QCI P/N
PS8101TQFN48GTR	AL008101001
PS8101QFN48GTR	AL008101000
SN75DP139RGZR	AL000139000

PROJECT : ZQ5

Quanta Computer Inc.

Size	Document Number	Rev
	HDMI (PS8101)	1A
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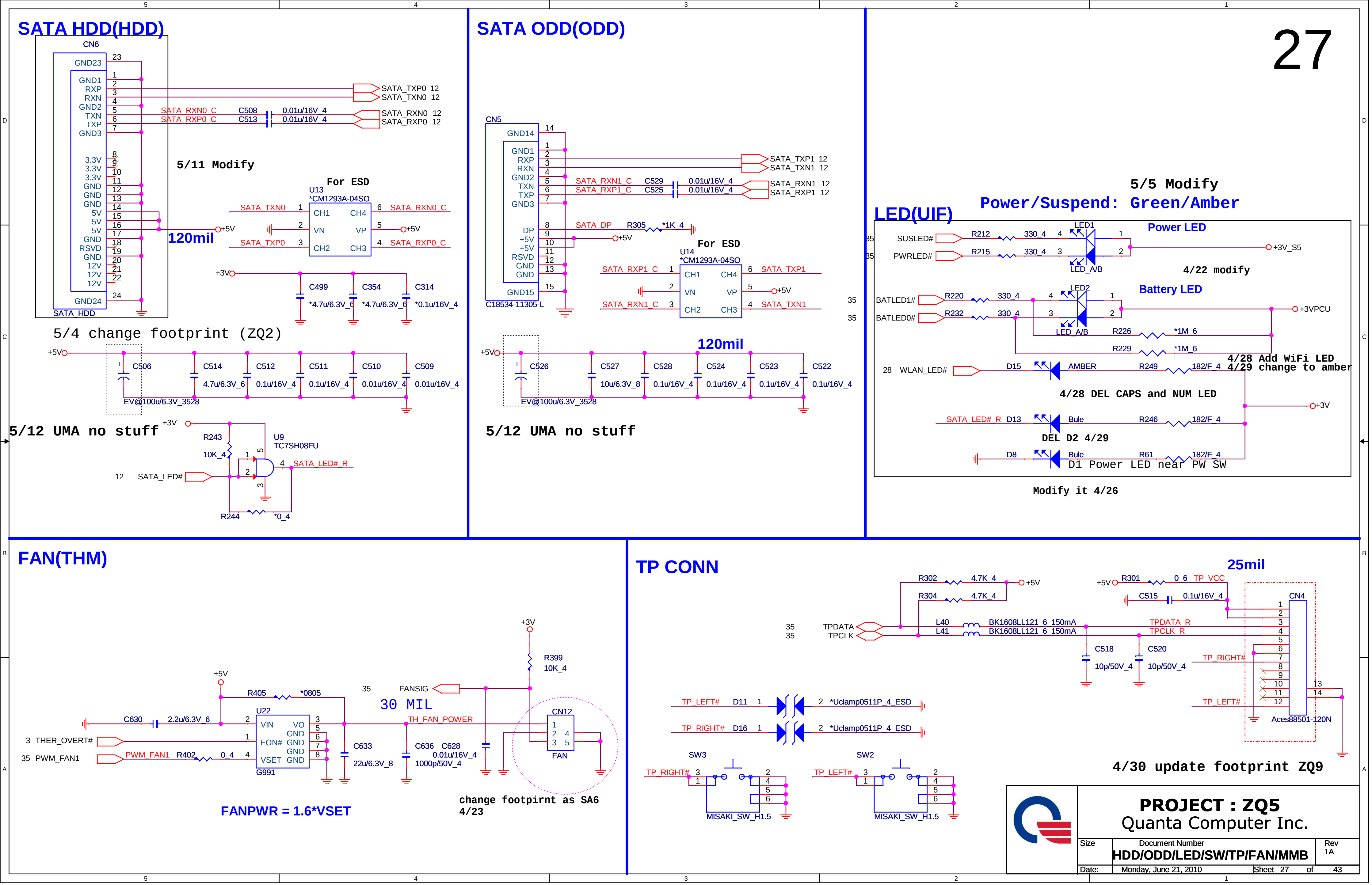
SATA HDD(HDD)
CN6
SATA_HDD
SATA_TXP0 12
SATA_TXN0 12
SATA_RXN0 12
SATA_RXP0 12
SATA_RXN0_C
SATA_RXP0_C
C508
C513
0.01u/16V_4
5/11 Modify
For ESD
U13
*CM1293A-04SO
120mil
5/4 change footprint (ZQ2)
C499 C354 C314
*4.7u/6.3V_6
*0.1u/16V_4
C506 C514 C512 C511 C510 C509
EV@100u/6.3V_3528
5/12 UMA no stuff
R243
10K_4
U9
TC7SH08FU
SATA_LED#
SATA_LED#_R
R244
*0_4
SATA ODD(ODD)
CN5
C18534-11305-L
SATA_TXP1 12
SATA_TXN1 12
SATA_RXN1 12
SATA_RXP1 12
SATA_RXN1_C
SATA_RXP1_C
C529
C525
SATA_DP
R305
*1K_4
For ESD
U14
*CM1293A-04SO
120mil
C526 C527 C528 C524 C523 C522
10u/6.3V_8
5/12 UMA no stuff
27
5/5 Modify
Power/Suspend: Green/Amber
LED(UIF)
Power LED
SUSLED#
PWRLED#
R212
R215
330_4
LED1
LED_A/B
+3V_S5
4/22 modify
Battery LED
BATLED1#
BATLED0#
R220
R232
LED2
+3VPCU
R226
R229
*1M_6
4/28 Add WiFi LED
4/29 change to amber
WLAN_LED#
D15
AMBER
R249
182/F_4
4/28 DEL CAPS and NUM LED
SATA_LED#_R
D13
Bule
R246
DEL D2 4/29
D8
R61
D1 Power LED near PW SW
Modify it 4/26
FAN(THM)
R399
10K_4
FANSIG
30 MIL
TH_FAN_POWER
R405
*0805
U22
G991
C630
2.2u/6.3V_6
THER_OVERT#
PWM_FAN1
R402
0_4
C633
22u/6.3V_8
C636 C628
0.01u/16V_4
1000p/50V_4
CN12
FAN
FANPWR = 1.6*VSET
change footprint as SA6
4/23
TP CONN
R302
R304
4.7K_4
R301
0_6
TP_VCC
25mil
C515
0.1u/16V_4
CN4
TPDATA
TPCLK
L40
L41
BK1608LL121_6_150mA
TPDATA_R
TPCLK_R
C518
C520
10p/50V_4
TP_RIGHT#
TP_LEFT#
Aces88501-120N
D11
D16
*Uclamp0511P_4_ESD
SW3
SW2
MISAKI_SW_H1.5
4/30 update footprint ZQ9
PROJECT : ZQ5
Quanta Computer Inc.
Size
Document Number
HDD/ODD/LED/SW/TP/FAN/MMB
Rev
1A
Date:
Monday, June 21, 2010
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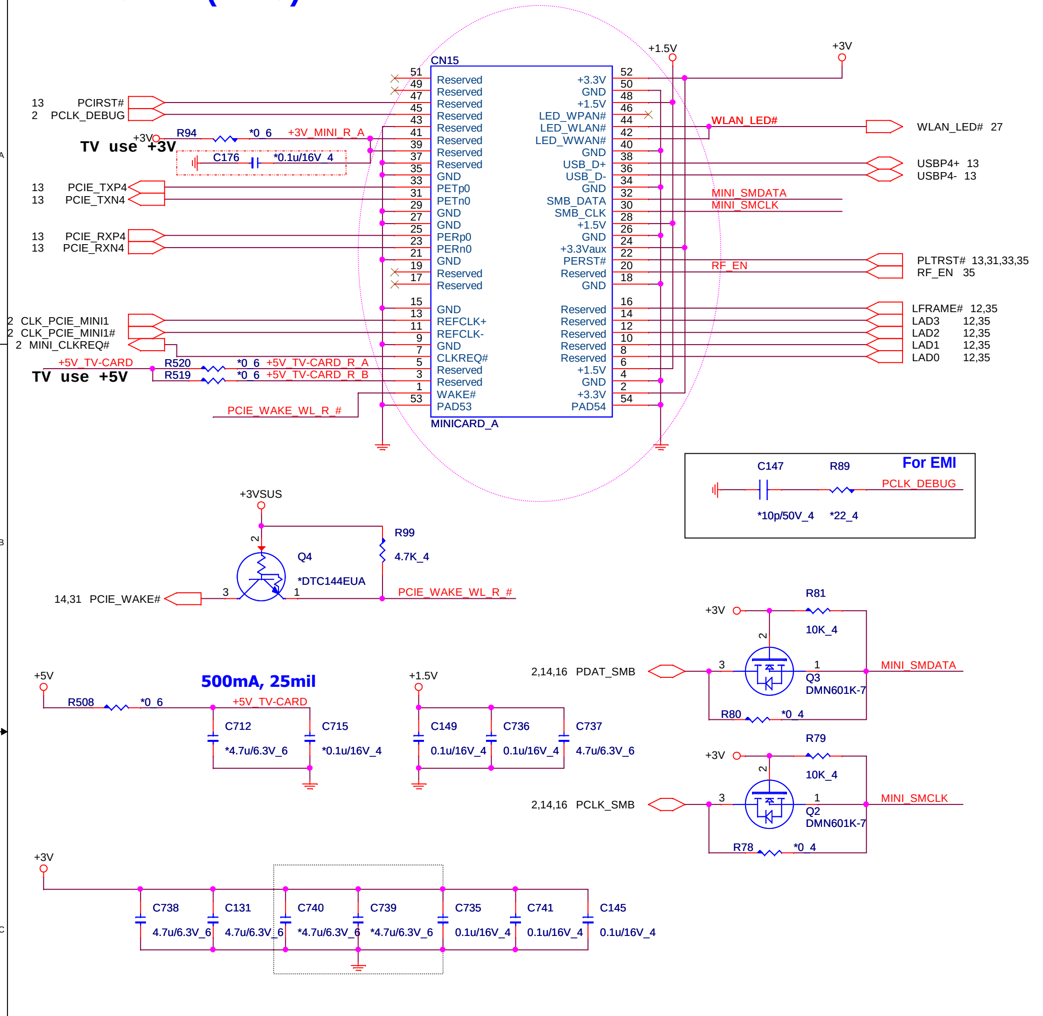
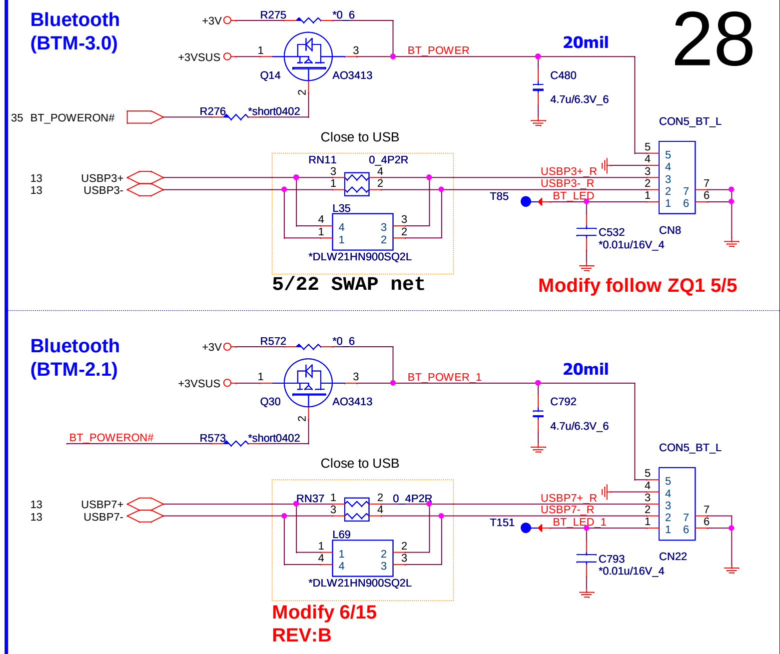
MINI-CARD(MPC)

4/21 change footprint andy(ZYD) H=7.0

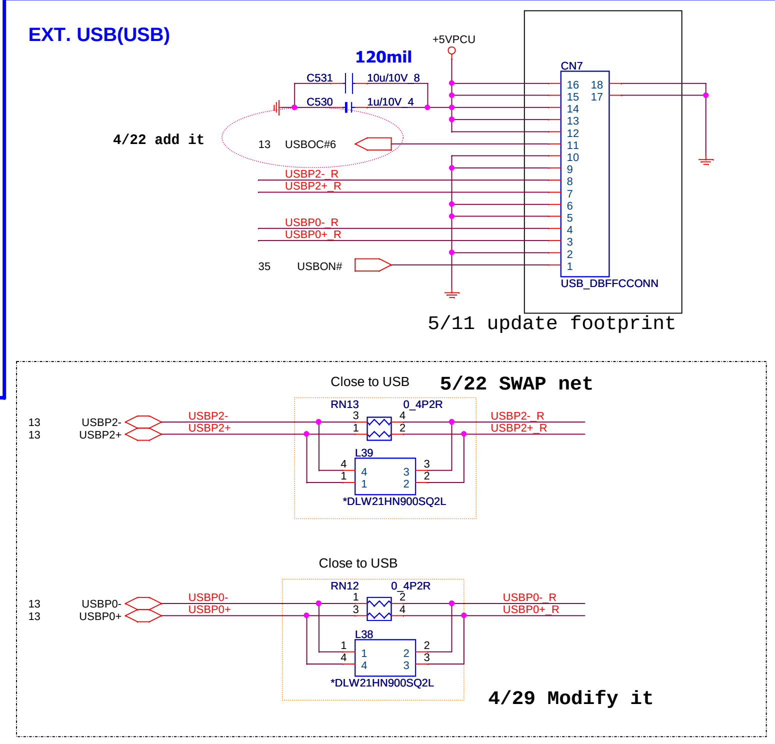


Bluetooth (BTM-3.0)

Bluetooth (BTM-2.1)

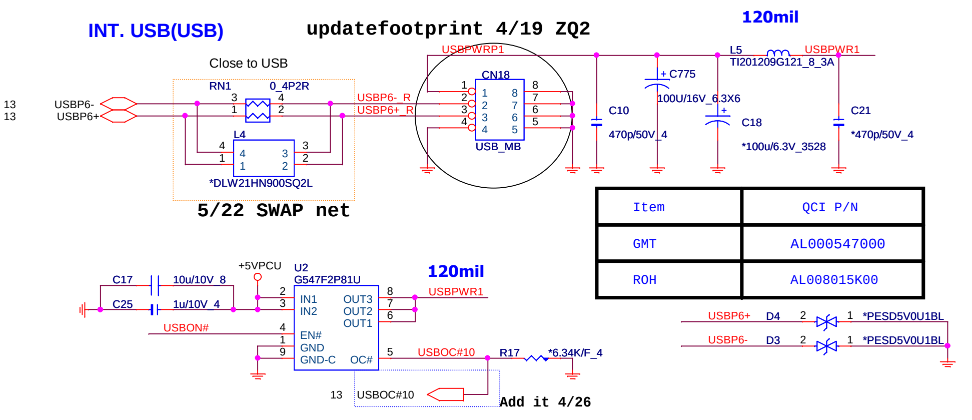


EXT. USB(USB)



INT. USB(USB)

updatefootprint 4/19 ZQ2



Item	QCI P/N
GMT	AL000547000
ROH	AL008015K00

PROJECT : ZQ5

Quanta Computer Inc.

Size	Document Number	Rev
	MINI/USB/BT/HOLE	1A

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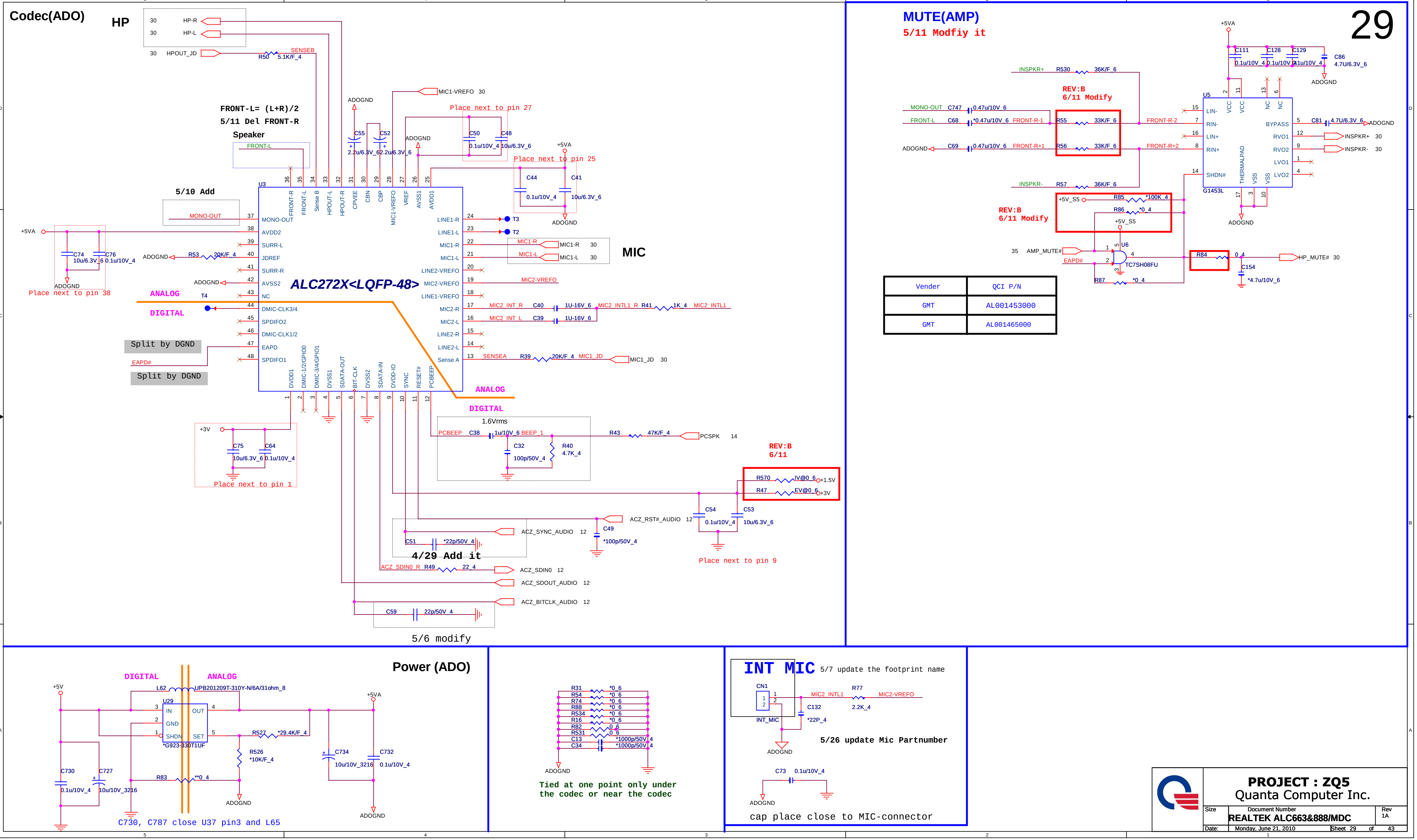
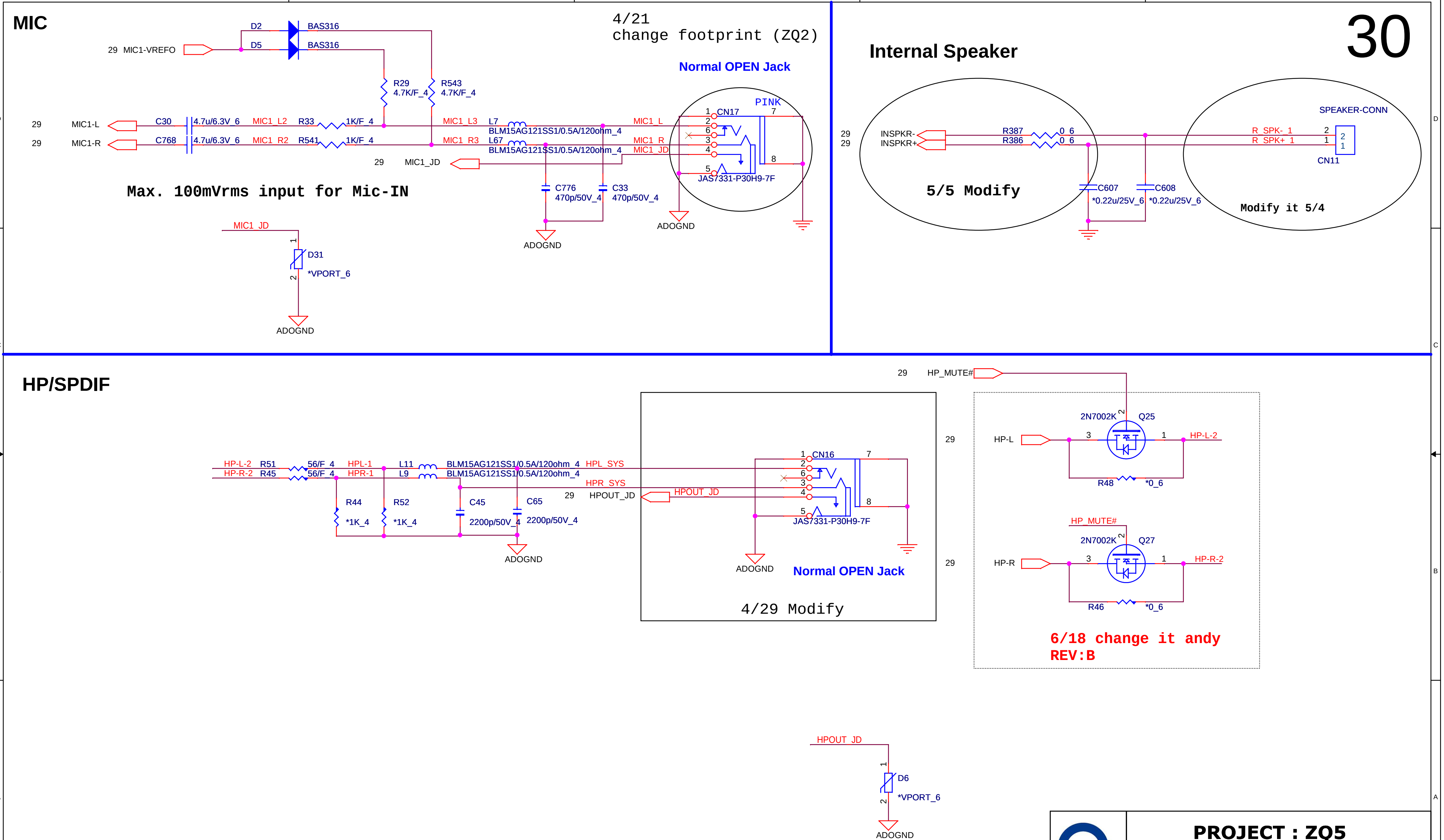


Vender	QCI P/N
GMT	AL001453000
GMT	AL001465000

PROJECT : ZQ5
Quanta Computer Inc.

Size | Document Number: REALTEK ALC663&888/MDC | Rev 1A
Date: Monday, June 21, 2010 | Sheet 29 of 43



PROJECT : ZQ5

Quanta Computer Inc.

Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A
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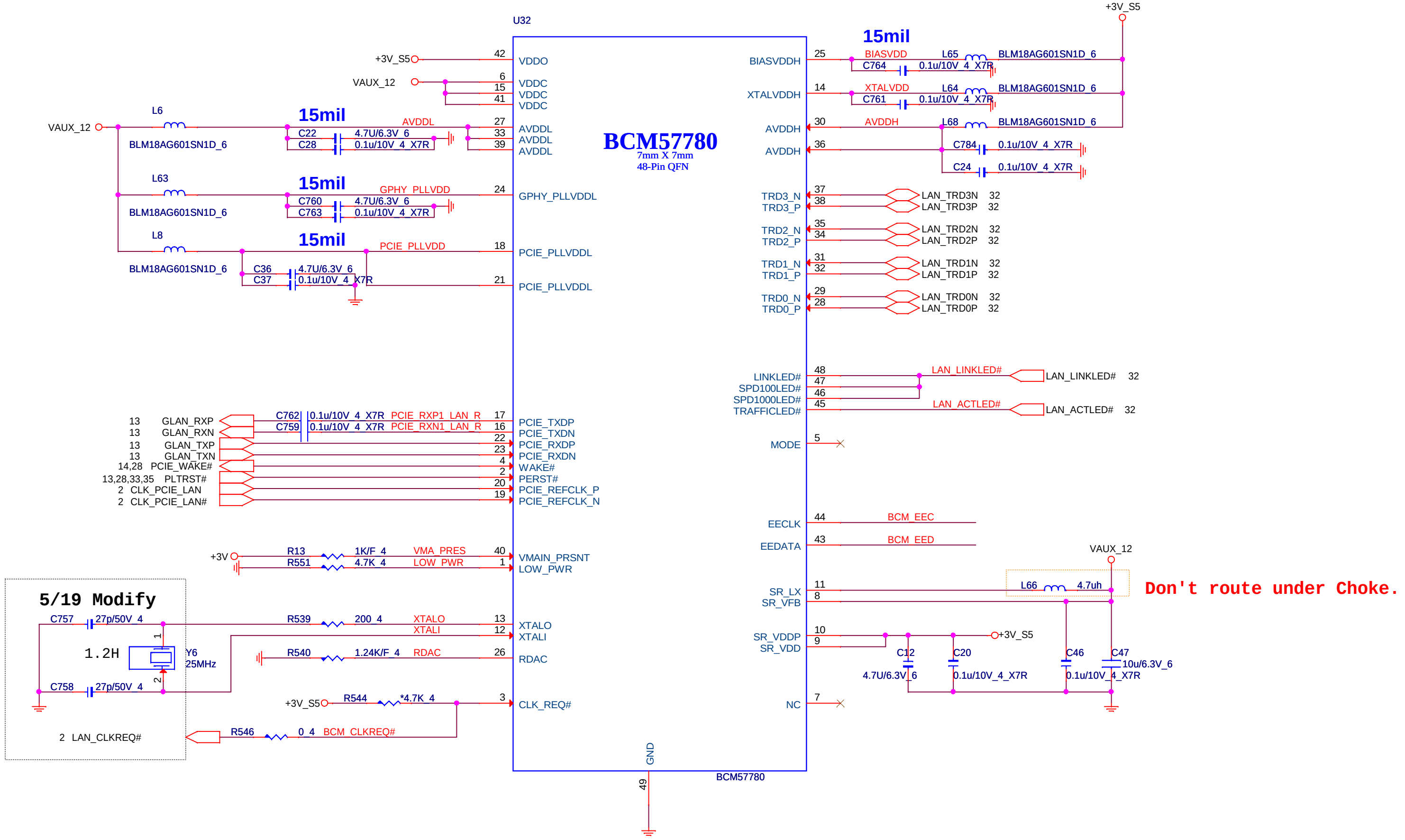
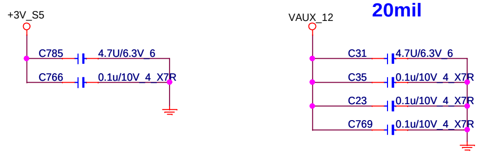
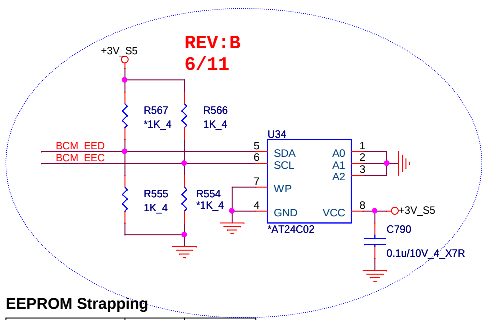
Giga-LAN BCM57780



LAN POWER



EEPROM



EEPROM Strapping

EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

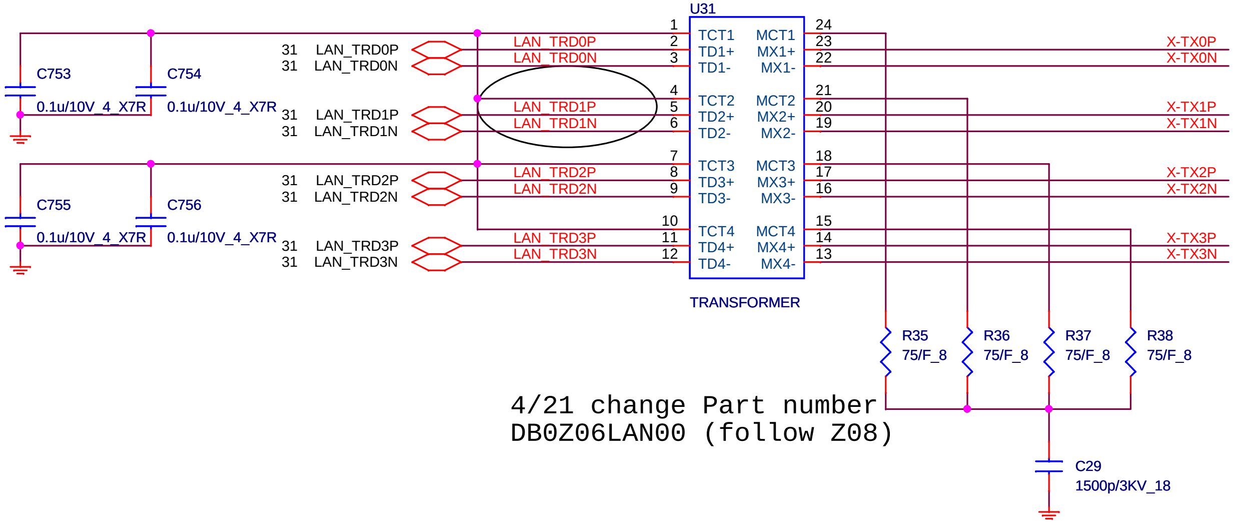
PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	GLAN BCM57780	1A

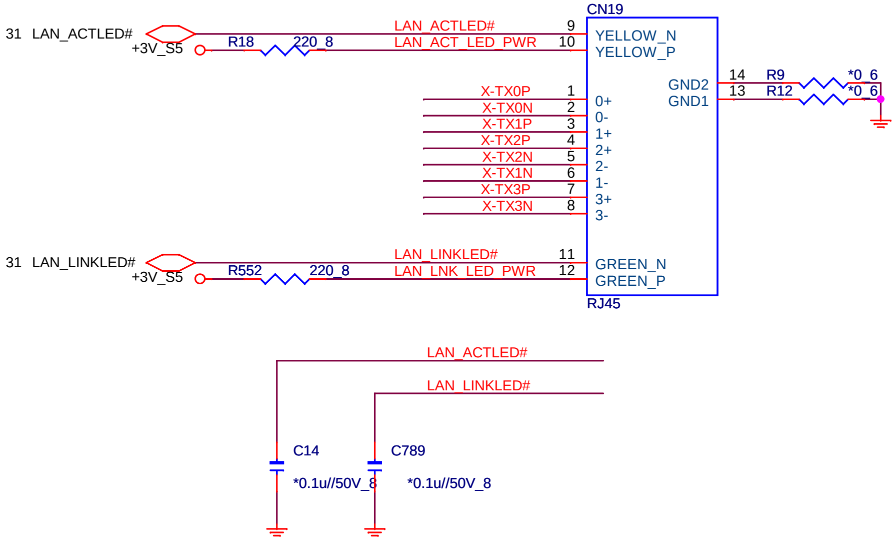
Date: Monday, June 21, 2010 Sheet 31 of 43

TRANSFORMER

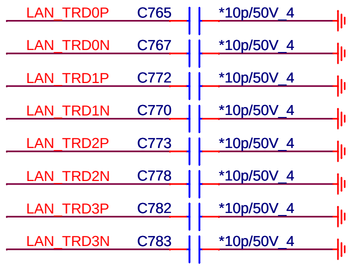
4/27 modify it



RJ45 Conn



For EMI



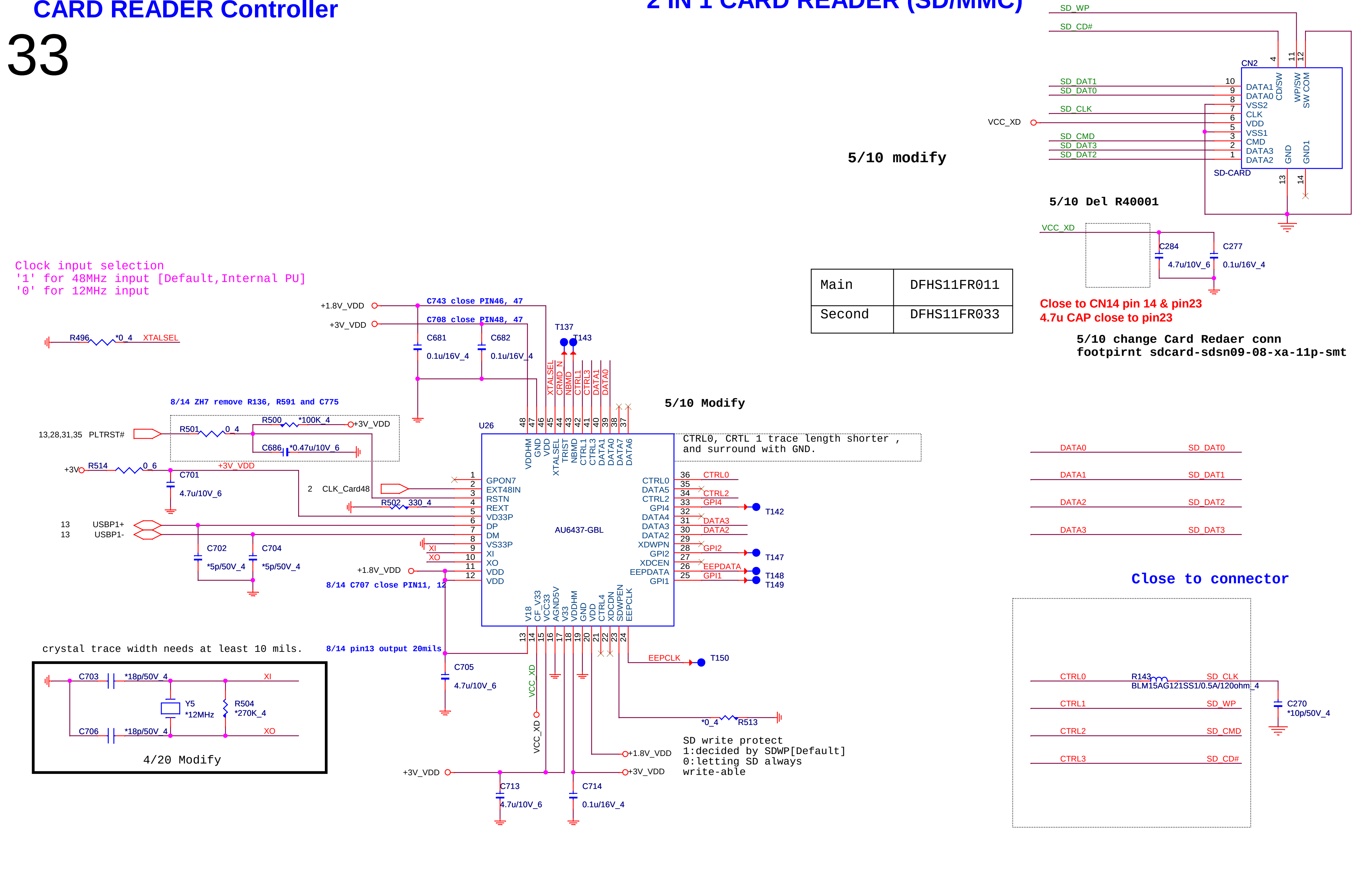
PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	LAN Transformer and RJ45	1A
Date:	Monday, June 21, 2010	Sheet 32 of 43

CARD READER Controller

33

2 IN 1 CARD READER (SD/MMC)



Main	DFHS11FR011
Second	DFHS11FR033

PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	AU6433 CardReader	1A

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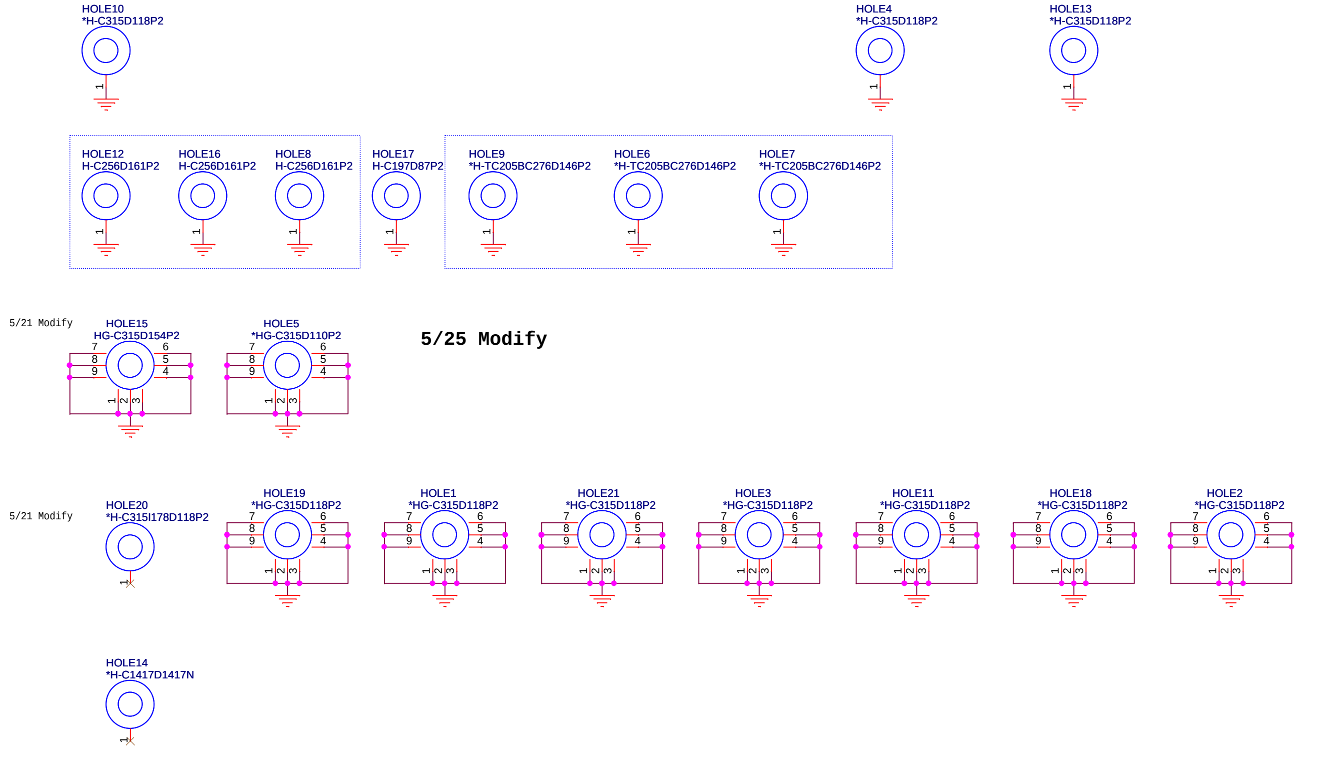
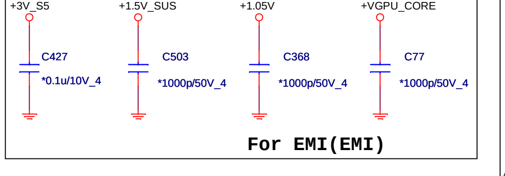
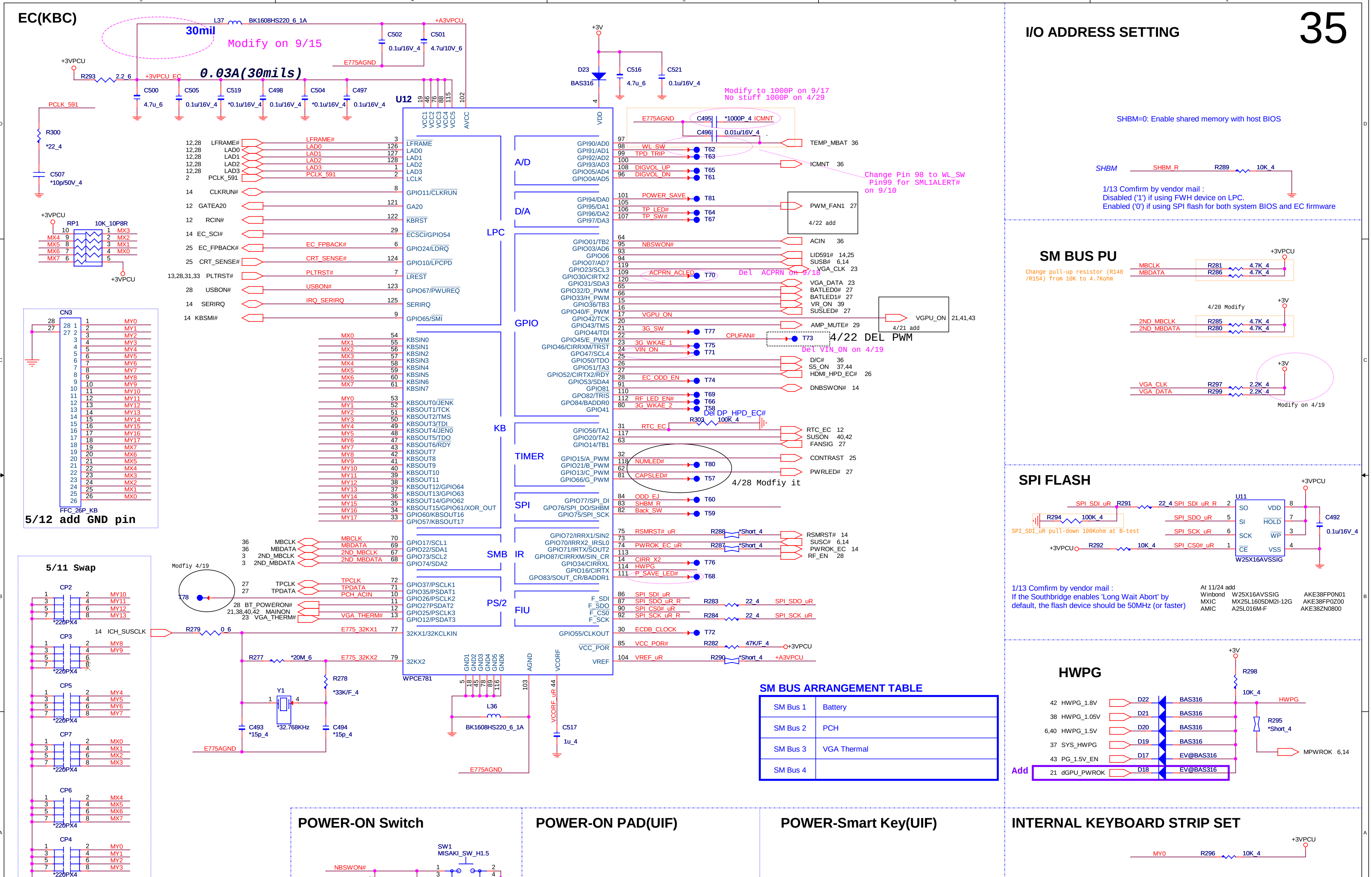
(OTH)





PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	MINI/USB/BT/HOLE	1A
Date: Monday, June 21, 2010	Sheet 34 of 43	



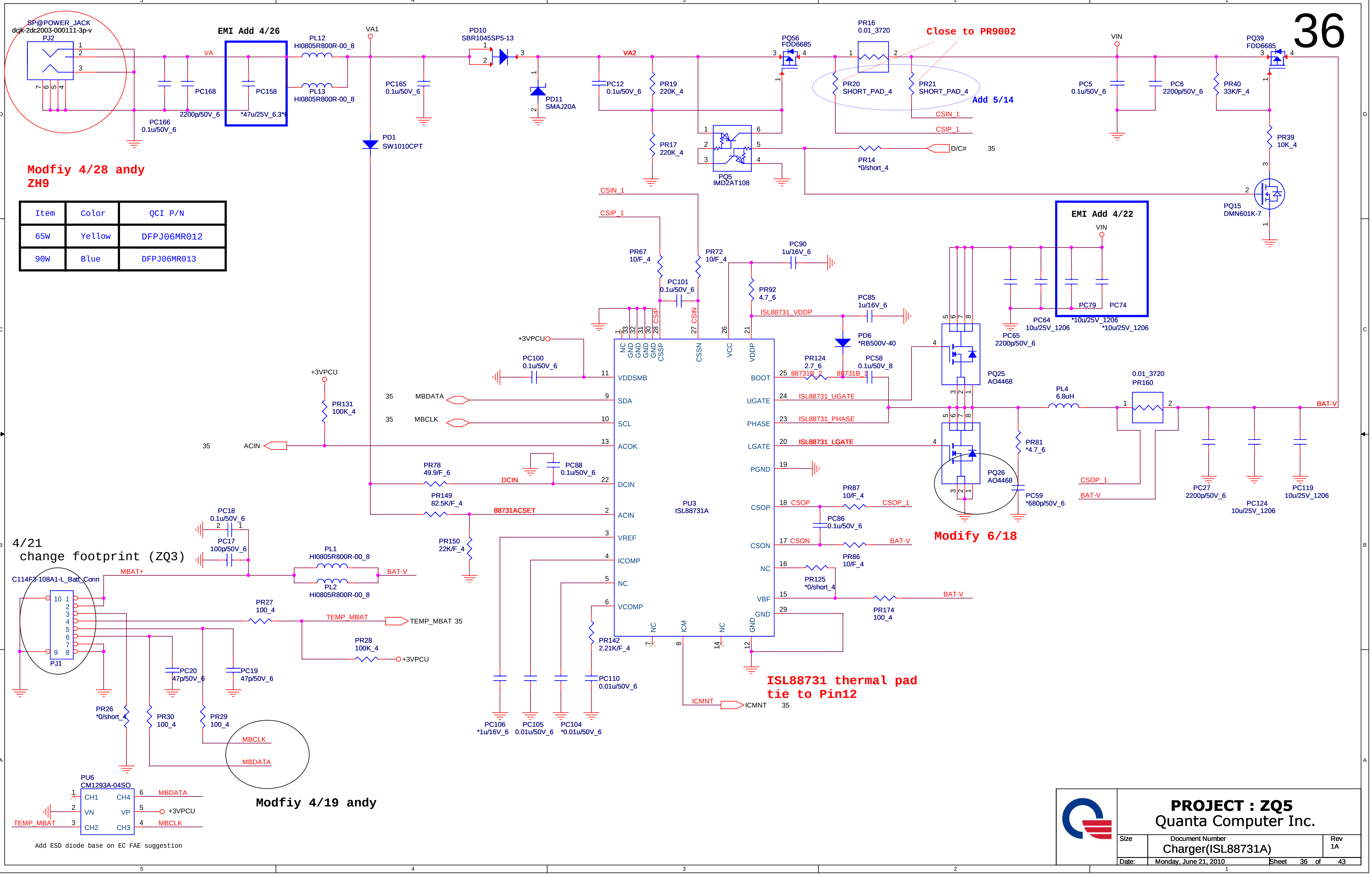
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA Thermal
SM Bus 4	

PROJECT : ZQ5

Quanta Computer Inc.

Size	Document Number	Rev
	WPCE81 & FLASH	1A
Date: Monday, June 21, 2010	Sheet 35 of 43	



Item	Color	QCI P/N
65W	Yellow	DFPJ06MR012
90W	Blue	DFPJ06MR013

PROJECT : ZQ5

Quanta Computer Inc.

Size	Document Number	Rev
	Charger(ISL88731A)	1A
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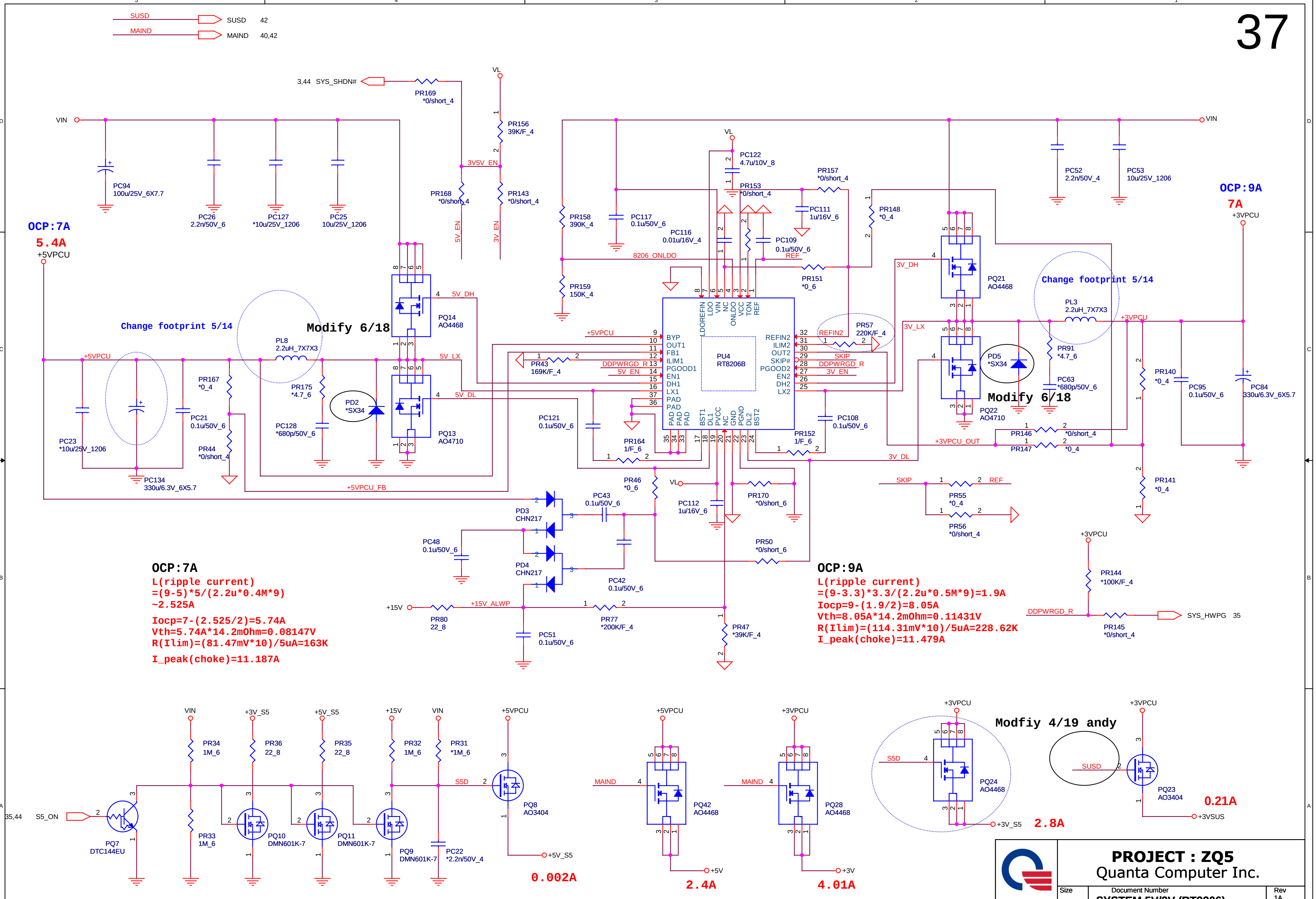
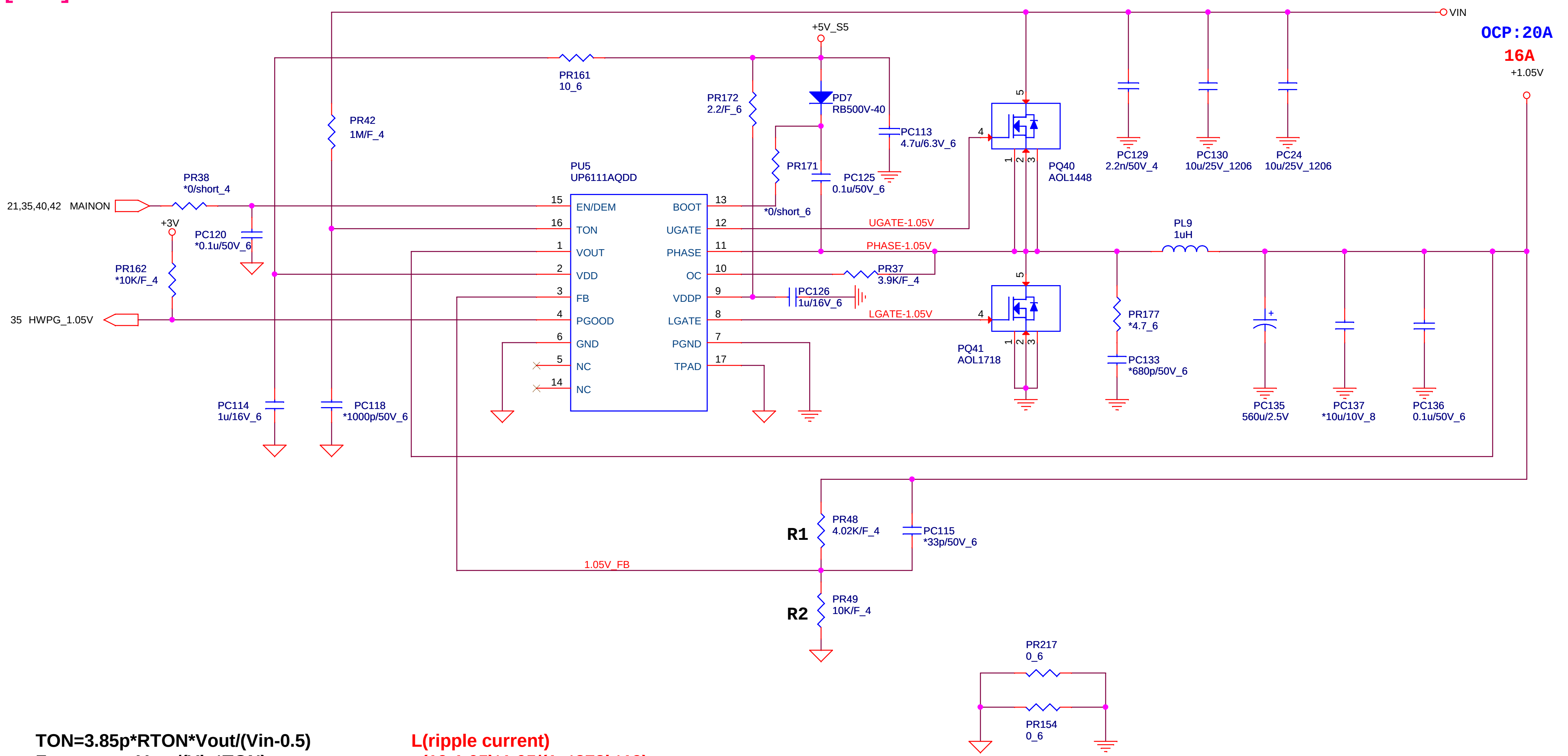


PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	SYSTEM 5V/3V (RT8206)	1A
Date:	Monday, June 21, 2010	Sheet 37 of 43

[PWM]



TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.647A

RILIM=4.3mohm*20-1.823/20uA=3.907Kohm
I(choke)peak=23.647A

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Size	Document Number	Rev
	+1.05V (UP6111A)	1A
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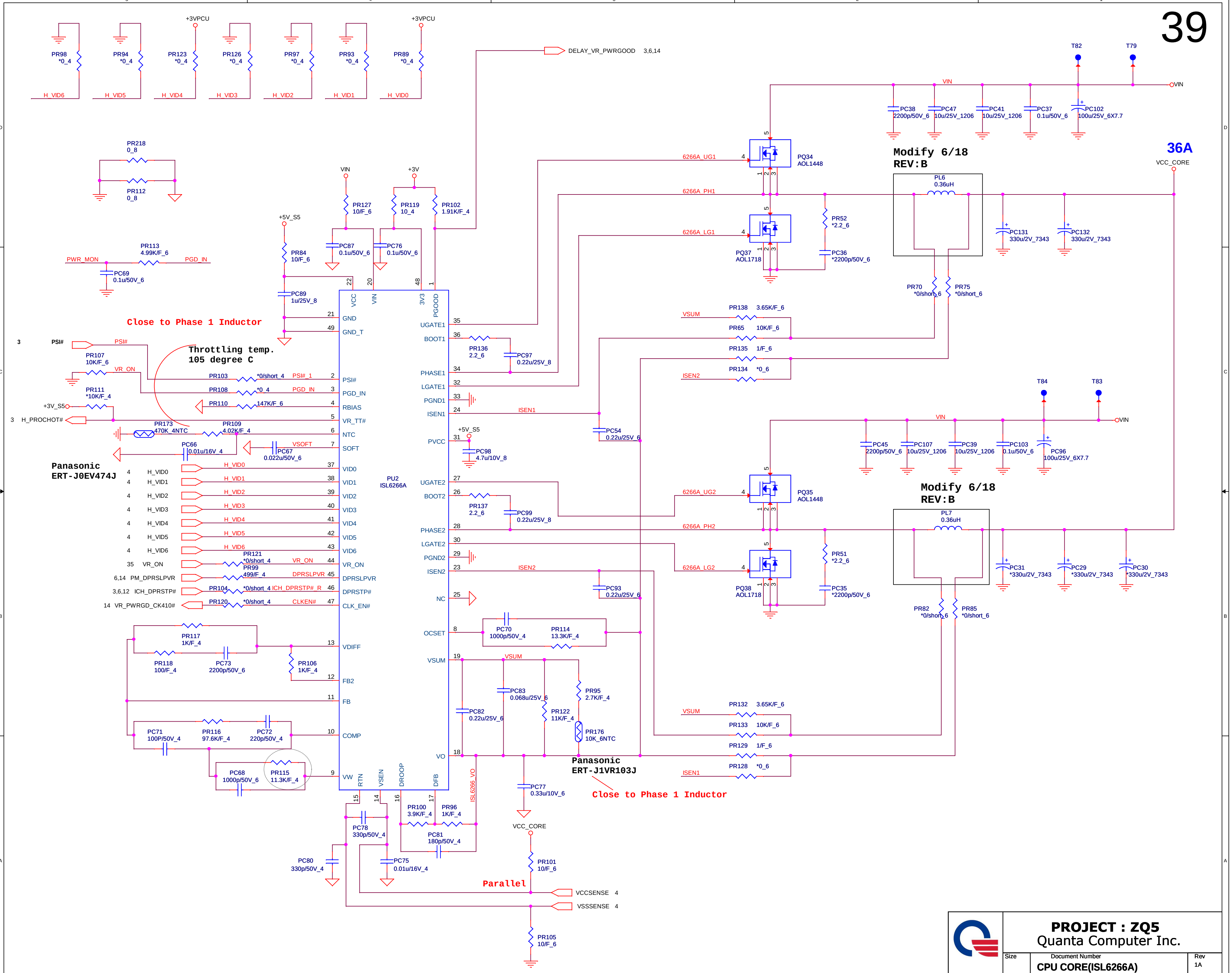

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Quanta Computer Inc.			
Size	Document Number		Rev
	CPU CORE(ISL6266A)		1A
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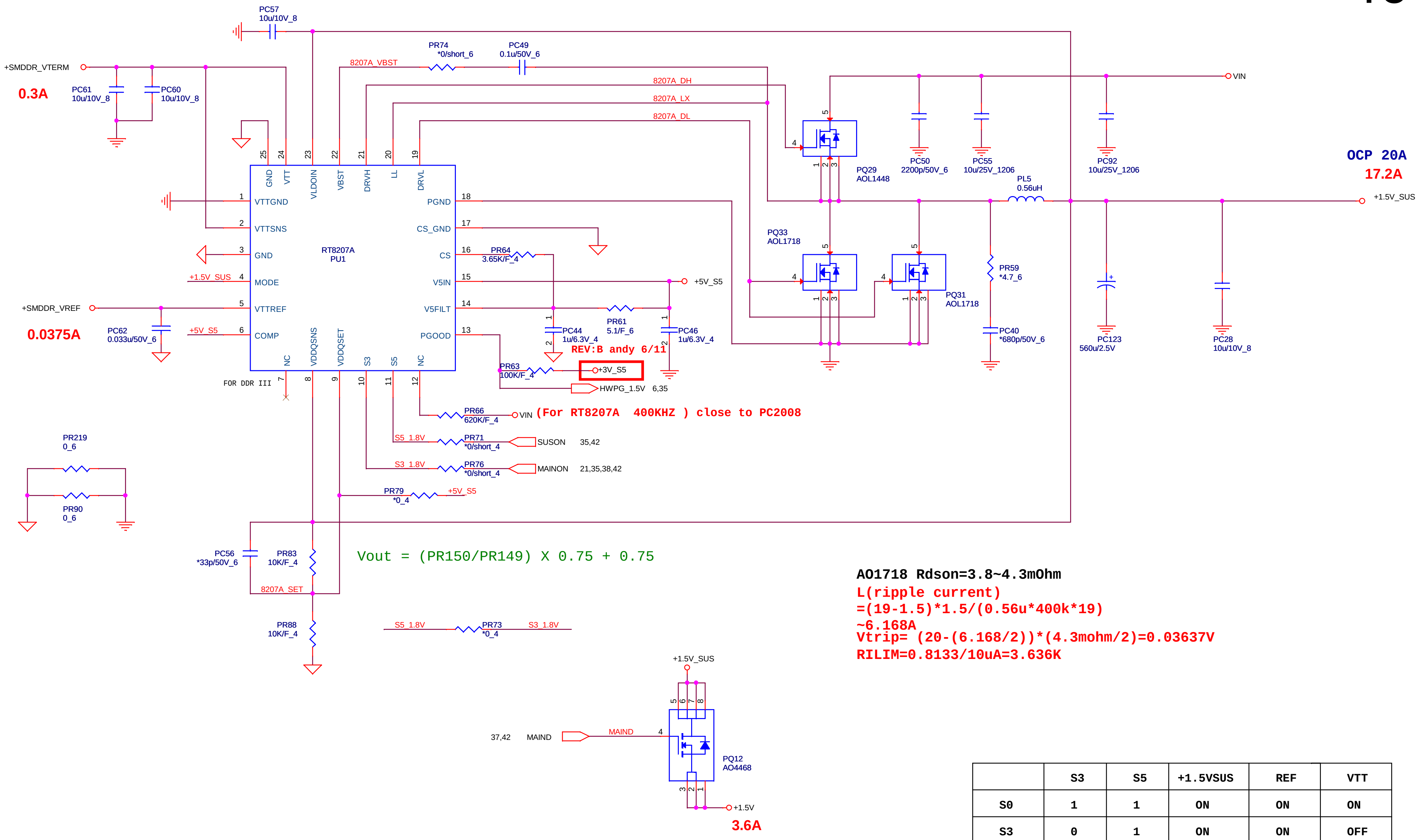


AO1718 Rdson=3.8~4.3mOhm

L(ripple current)

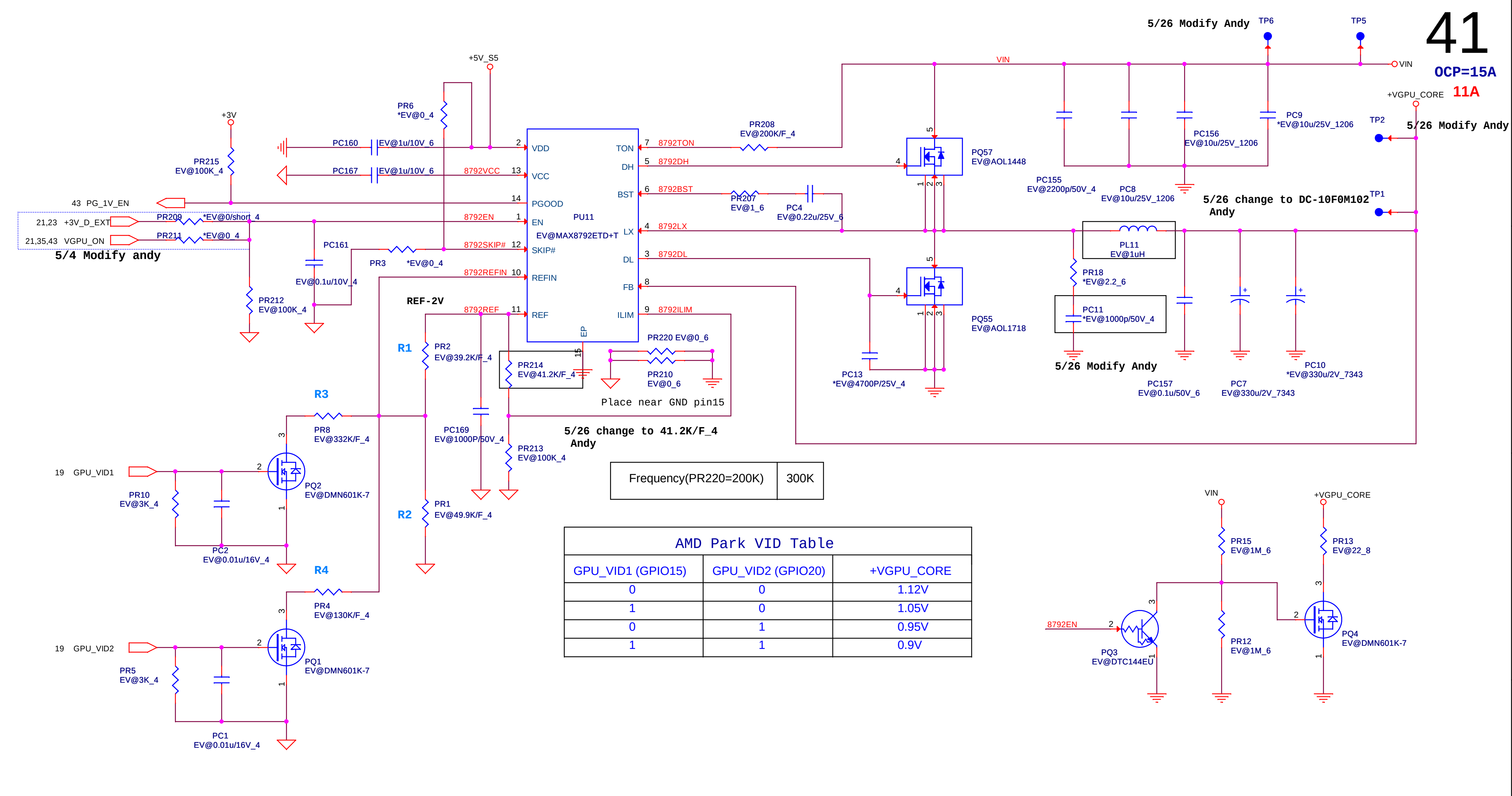
=(19-1.5)*1.5/(0.56u*400k*19)

~6.168A

Vtrip= (20-(6.168/2))*(4.3mohm/2)=0.03637V

RILIM=0.8133/10uA=3.636K

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



Frequency(PR220=200K)	300K

AMD Park VID Table

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

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Size	Document Number	Rev
	GPU CORE(MAX8792)	1A
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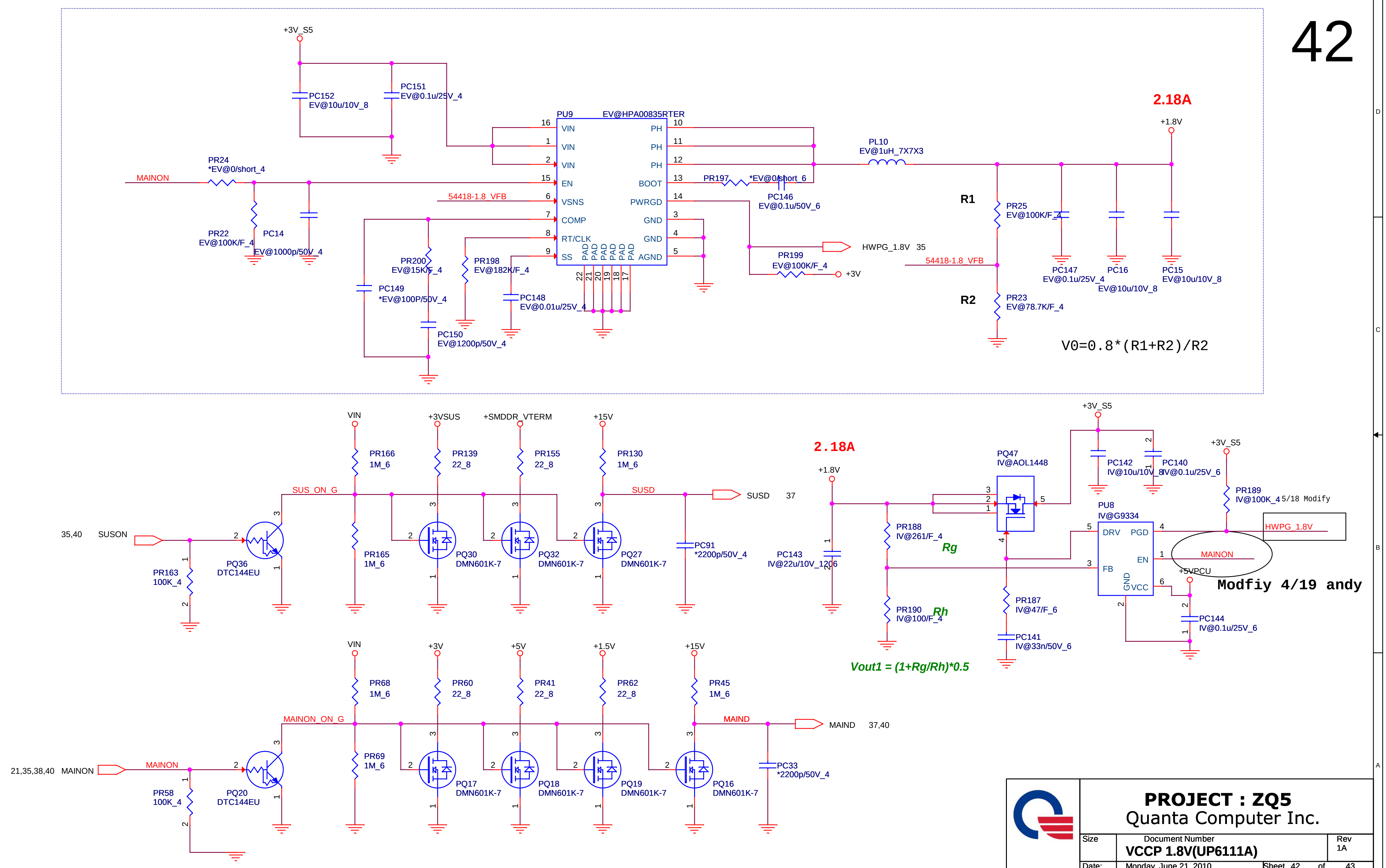

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Quanta Computer Inc.

Size	Document Number	Rev
	VCCP 1.8V(UP6111A)	1A
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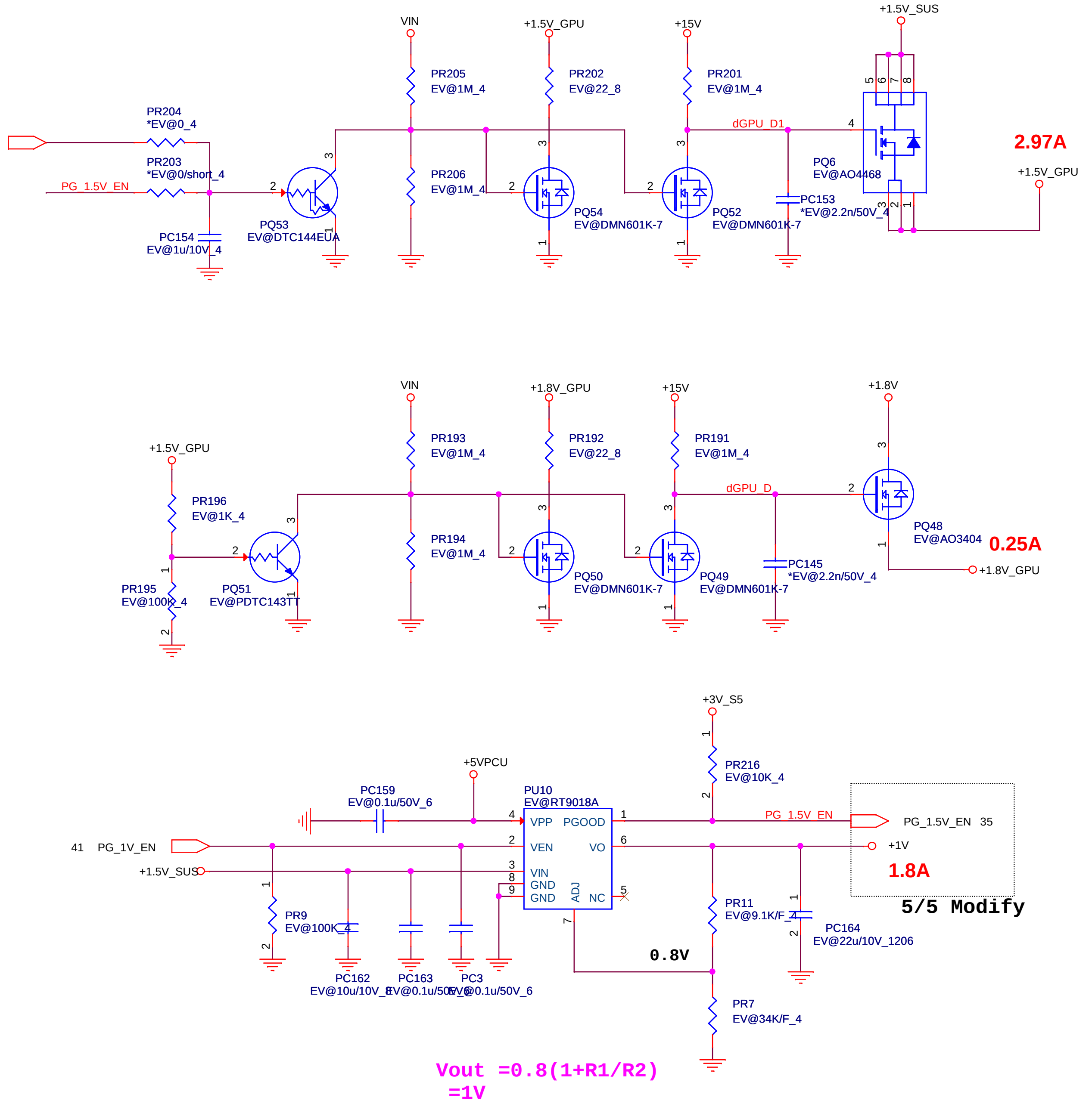

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Size	Document Number GPU_POWER	Rev 1A
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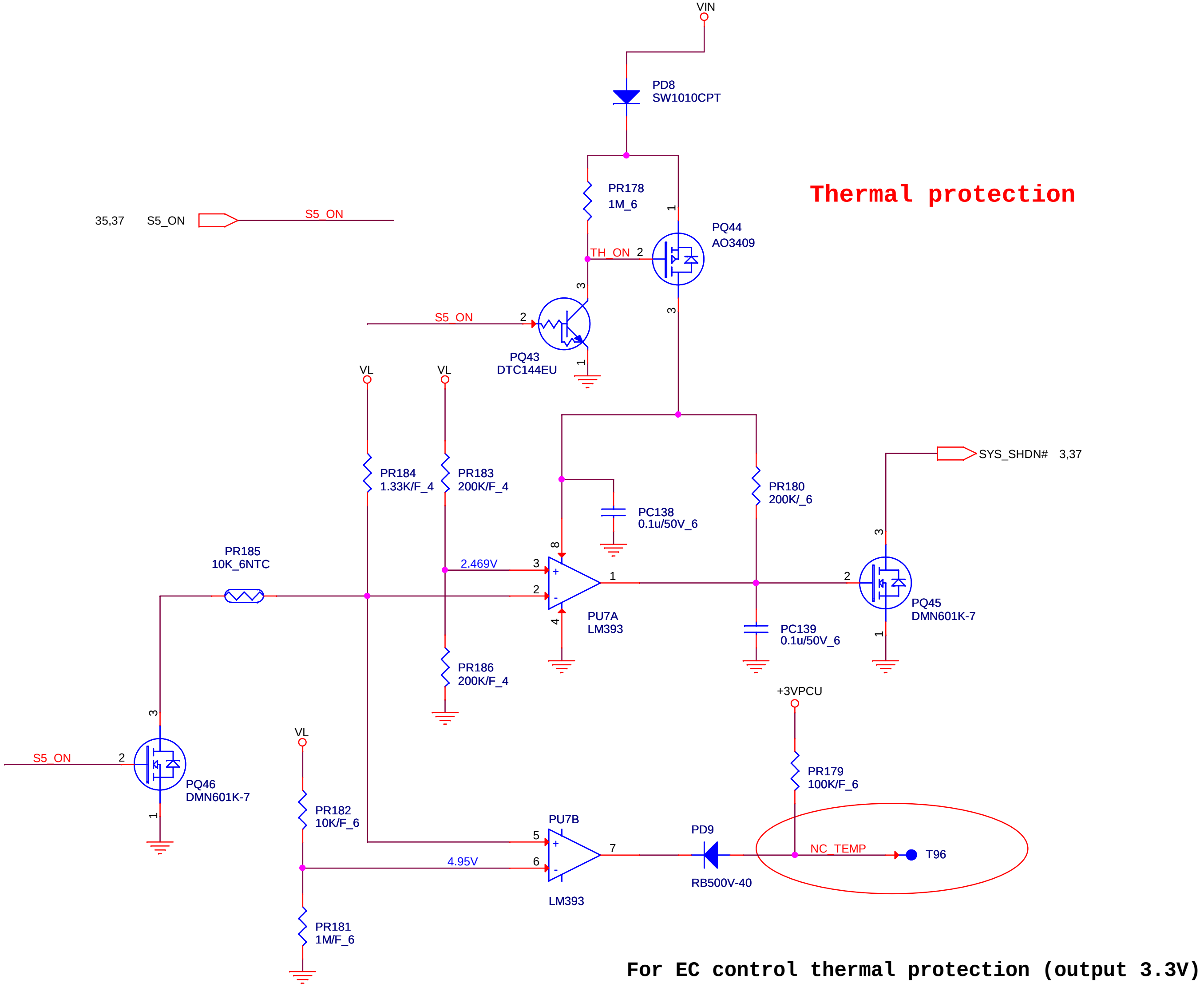

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	Thermal Protection	1A
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MODEL:	REV	CHANGE LIST
ZQ5 MB	A	***First release***
	C	1.Page40:change HWPG_1.5V pull up to +3V_S5 for S3 issue 2.Page29:Add R570 pull up +1.5V for uma Audio I/O 3.Page26:Swap HDMI Lane2 for HDMI issue 4.Page31:U34 and R567 no stuff ,R555 stuff it for LAN ID issue 5.Page02:Q12 and Q13 change Part number from BAM700200F6 to BAM700200H2 6.Page29:R55 and R56 change Part number to CS33303F911(33K) for Audio 7.Page29:change R86 and U6 Pin5 pull up to +5V_S5 8.Page29:change R84 value to 0 ohm 9.Page30:change Q25 and Q27 Part number to BAM70020002 as ZYB 10.Page25:L1,L2,L3 change to CX8LL680001 11.Page25:C1,C2,C3,C5,C6,C7 change to CH-5006JBD4 12.Page25:R11,R14 change to CS01502JB12 13.Page28:Add another BT circuit (USB port5),Add Q30,RN37,C792,CN22 14.Page07:Change R425,R426 to CS02492FB29 for CRT issue 15.Page13:Change BT 2.1 to USB port 7 16.Page28:Change BT 2.1 to USB port 7 17.Page25:chage 0805 to SHORT Pad R71,R72,R98,R146 18.Page29:Stuff R84 U6 and no stuff R86 for Audio bobo noise 19.Page10:change R171 and R429 to bead CX8PG181001 20.Page30:stuff Q25 and Q27 and no stuff R46 R48 for Audio bobo noise 21.Page40:Add PR219 22.Page38:Add PR217 23.Page41:Add PR220 24.Page39:Add PR218 25.Page36: Change PR16 (0.01/F_7520) to CS+0108GL13 (0.01_3720) 26.Page41: DEL JP1 and JP4 27.Page39: DEL JP2 and JP3 28.Page38:change PR171,PR38 to short Pad 29.Page36:change PR125,PR14,PR26 to short Pad 30.Page37:change PR143,PR145,PR146,PR153,PR157,PR168,PR169,PR170,PR50,PR44,PR56 to short Pad 31.Page39:change PR120,PR121,PR104,PR103,PR70,PR75,PR82,PR85 to short Pad 32.Page40:change PR71,PR76,PR74 to short Pad 33.Page41:change PR209 to short Pad (EV@) 34.Page42:change PR24,PR197 to short Pad (EV@) 35.Page43:change PR203 to short Pad (EV@) 36.Page36:Change PQ26 to AO4468（P/N：BAM44680003） 37.Page37:PD2 and PD5 no stuff 38.Page39:PC29 and PC31 no stuff 39.Page36:PJ1 change Part number to DFHD08MR140

PAGE \ MODEL	ZR6 MB FROM	TO
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	
31	1A	
32	1A	
33	1A	
34	1A	
35	1A	
36	1A	
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38	1A	
39	1A	
40	1A	
41	1A	
42	1A	
43	1A	
44	1A	
45	1A	

MB Assy' P/N: 31ZQ5MB0000	Project :ZQ5 MB	Document No.:
Approved by : Andy_Lin	Drawing by :Andy Chen	DATE: 2009/03/04

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	Thermal Protection	1A
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