IPMIP-GS

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51	RSMRST CIRCUIT / EMI
52	CPU ITP / LPC DEBUG CONN
53	RTL8111DL LAN
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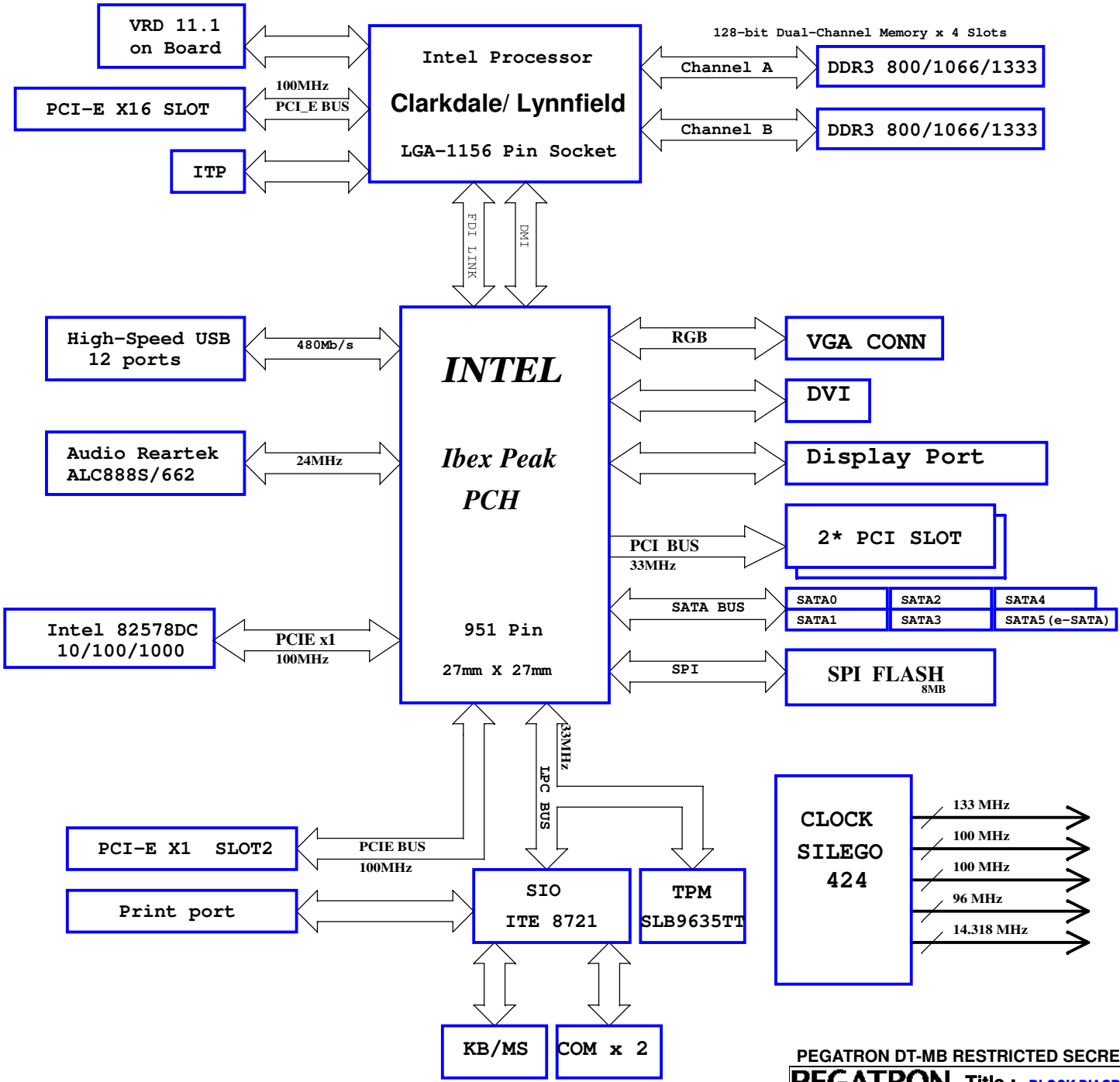
55	LPT
56	ATX POWER CONNECTOR
57	VCORE CONTROLLER
58	VCORE DRIVER1
59	VCORE DRIVER2
60	VAGX CONTROLLER
61	VAGX DRIVER
62	+1P1V_VTT
63	+1P5V_DUAL
64	+1P05V_PCH / +1P05V_ME
65	+5V_DUAL / +3P3V_ME
66	+SM_VTT / +1P8V_SFR



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : BLOCK DIAGRAM

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Friday, April 23, 2010 Sheet 1 of 68

Schematics Change History

Version	Date	Comments

CAD Note:

Default component footprint is SMD 0402, Y5V, 5% type. Difference footprint show on schematics.

Property: BOM

I = Installed Part.

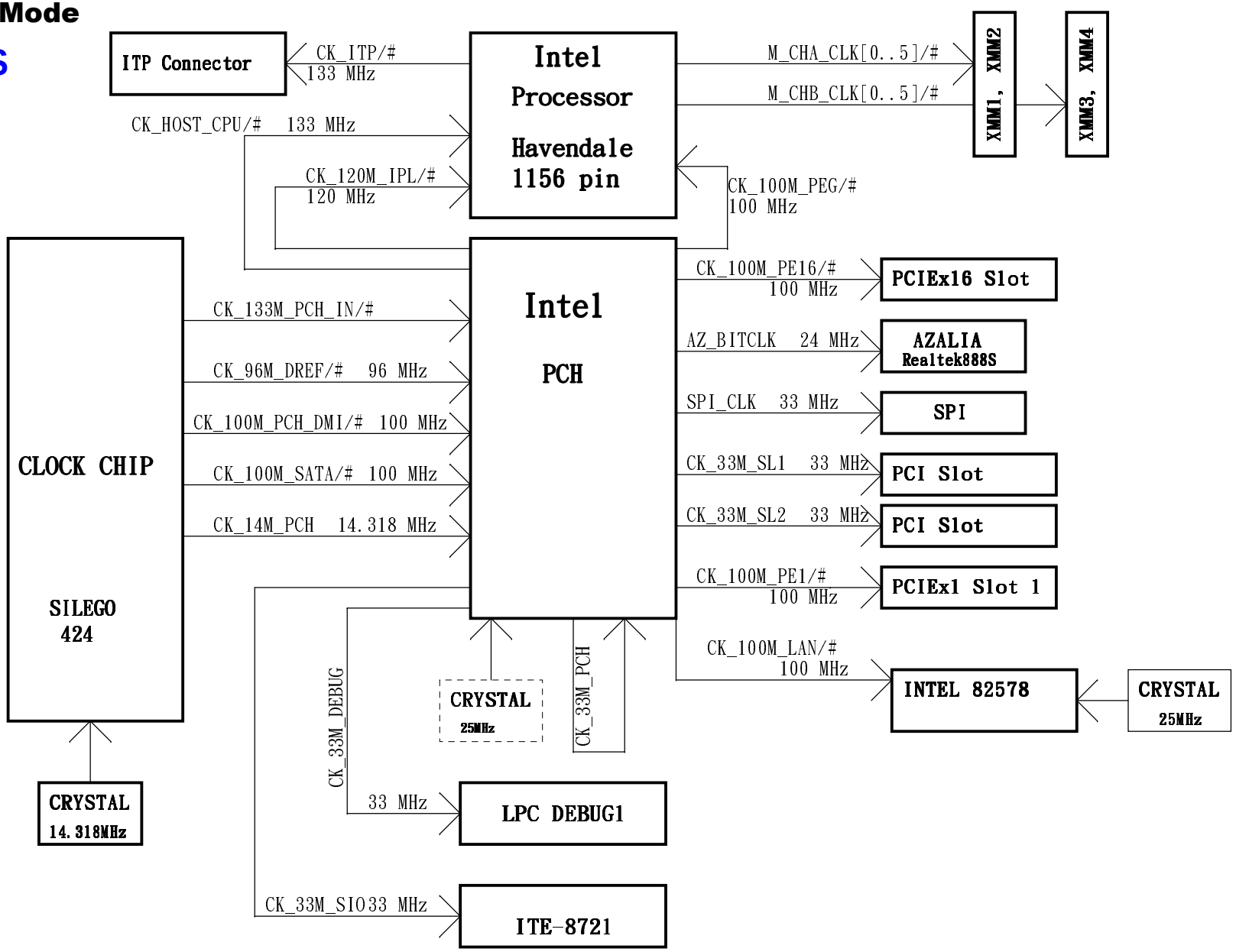
NI = Not Installed Part.

PROTO = PROTO Phase Only.

VP = Virtual Part.

PCH Buffer Mode

IPMIP-GS



PEGATRON DT-MB RESTRICTED SECRET

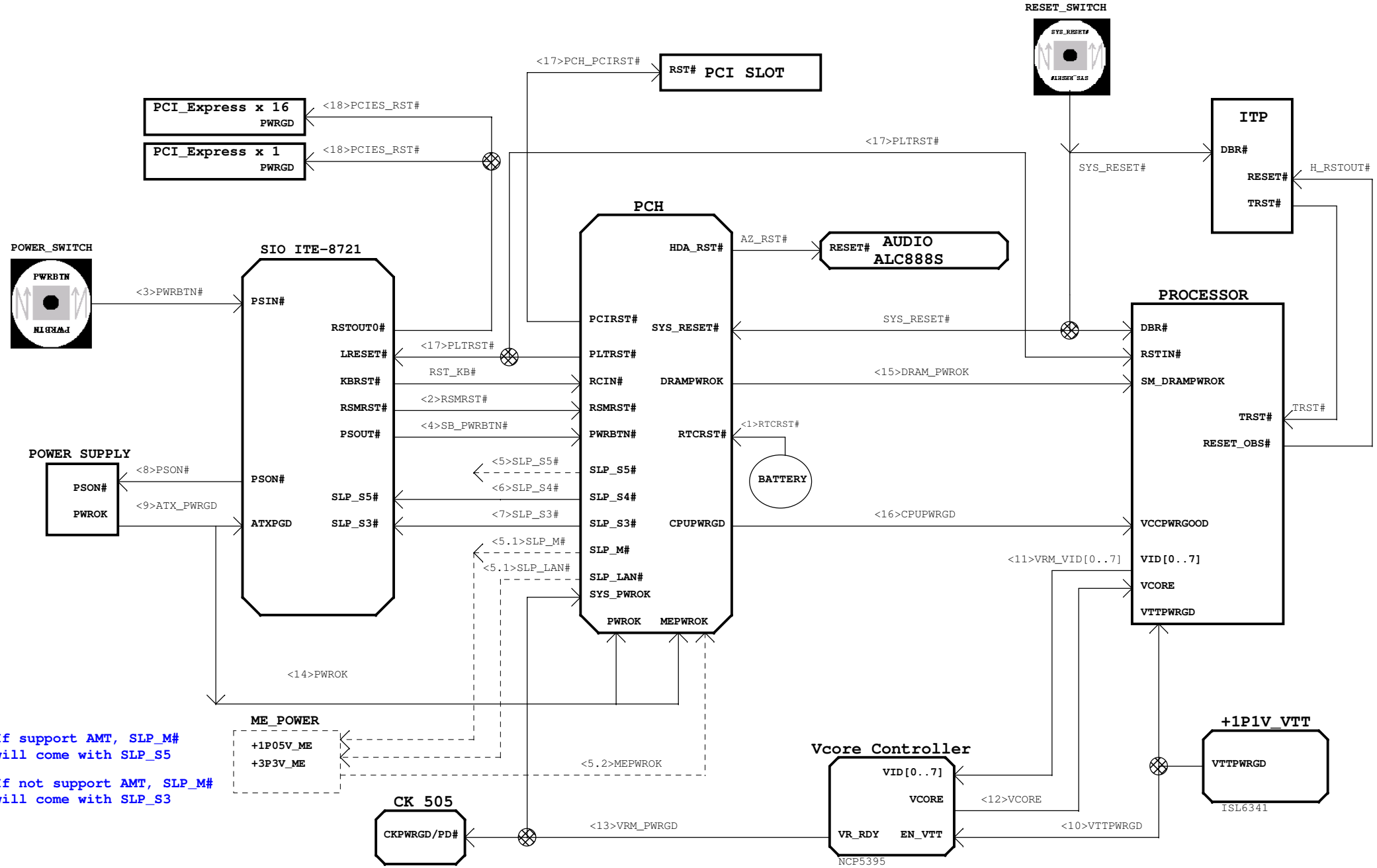
PEGATRON Title : CLOCK DISTRIBUTION

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

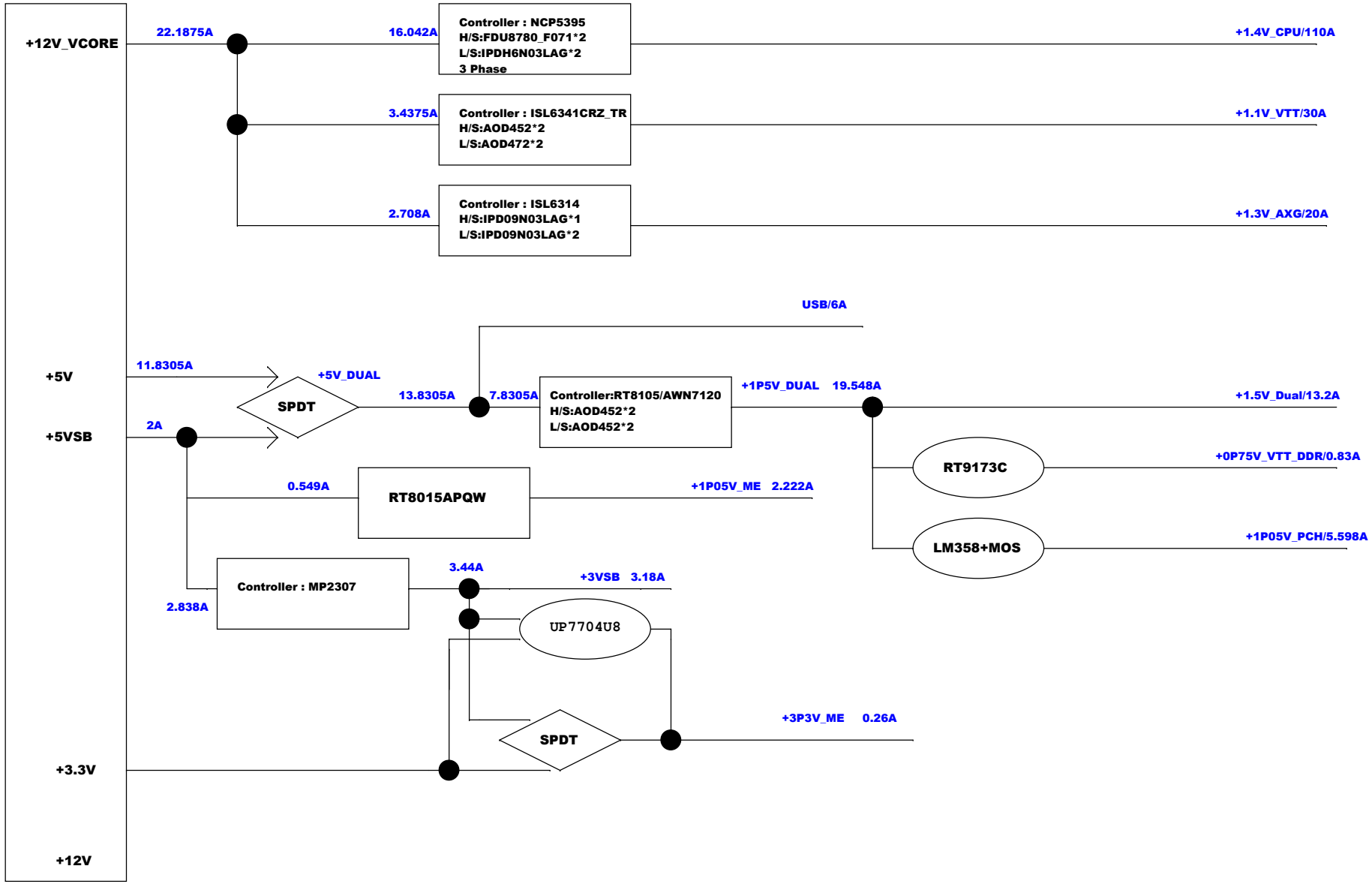
Date: Tuesday, March 23, 2010 Sheet 3 of 68

IPMIP-GS



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : SIGNAL & RESET MAP	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-GS	Rev: 1.01
Date: Tuesday, March 23, 2010	Sheet 4 of 68	



SWITCHING

LINEAR

SWITCH ON/OFF

<Variant Name>

PEGATRON Title : POWER FLOW

PEGATRON CORPOATION Engineer: Michael Lee

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Tuesday, March 23, 2010 Sheet 5 of 68

Lynnfield/Clarkdale

VCORE
+1.1V_VTT
+1.5V
+1.8V

-> 90A - 95(TBD)W
-> 30A(TBD) - 33W
Vddq -> 6A - 9W
Vccpll -> 1.35A - 2.43W

Intel Ibex Peak

V_CPU_IO
+5V
+5V
+3.3V
+1.1V
+1.05V
+1.8V
+3P3V
+3P3VSB

-> <1mA - 1.1mW
V5REF -> <1mA - 5mW
V5REF_Sus -> <1mA - 5mW

Vcc3_3 -> 0.357A - 1.178W
VccDAC -> 0.069A - 0.228W

VccDMI -> 0.065A - 0.07W

VccADPLLA -> 0.075A - 0.079W
VccADPLLB-> 0.075A - 0.079W
VccCORE -> 1.629A - 1.71W
VccIO -> 3.251A - 3.414W
VccLAN -> 0.372A - 0.39W
VccME -> 2.222A - 2.333W

VccqNAND -> 0.156A - 0.281W
VccVRM -> 0.196A - 0.353W
VccTX_LVDS -> 0.059A - 0.106W

VccALVDS -> <1mA - 3.3mW

VccRTC -> 2mA - 6.6mW
VccSus3_3 -> 0.168A - 0.554W
VccSusHDA -> 0.006A - 0.02W
VccME3_3-> 0.086A - 0.284W

CLOCK- CK505

+3P3V
+VDD_IO (0.8V)

-> 250mA - 0.825W
-> 80mA - 64mW

DDR3 DIMM (4) & Termination

+1.5V_DAUL
SM_VTT(0.75V)

VDD (S0, S1) -> 7.2 A - 10.8W
VDD (S3) -> 712mA - 1.07W

SM VTT (S0, S1) -> 0.83A - 0.623W

PCI Express x 1

+12V
+3P3V
+3P3V_PCI

-> 0.5A - 6W
-> 3.0A - 9.9W
WAKE -> 0.375A - 1.24W
No WAKE-> 20mA - 66mW

PCI Express x 16

+12V
+3P3V
+3P3V_PCI

-> 5.5A - 66W
-> 3.0A - 9.9W
WAKE -> 0.375A - 1.24W
No WAKE-> 20mA - 66mW

PCI SLOTS

+12V
-12V
+5V
+3P3V
+3P3V_PCI

-> 0.5A - 6W
-> 0.1A - 1.2W
-> 5.0A - 25W
-> 7.6A - 25.08W
WAKE -> 0.375A - 1.24W
No WAKE-> 20mA - 66mW

INTEL 82578

+3P3V_CL
+1P8VSB_LAN
VCC_LAN(1.05V)

-> 15.5mA(TBD) - 51.15mW
-> 300mA - 540mW
-> 300mA -315mW

SIO ITE-8721

+5V
+3.3VSB
+3.3V

-> 1mA - 5mW
-> 2.4uA - 7.92uW
-> 2mA - 6.6mW

ALC888S Azalia Codec

+5VSB
+3P3V

-> 0.6A - 3W
-> 0.4A - 1.32W

USB 12 PORTS

+5V_DUAL

(S0, S1) -> 8.4A - 42W
(S3) -> 0.336A - 1.68W

1394A

+3P3V

-> mA - W

HDMI

+3P3V
+2P5V_DVI

-> mA - mW
-> mA - mW

SATA 6 PORTS

+5V
+12V

-> 0.975A - 4.875W
-> 0.9A - 10.8W

FAN

+12V

-> 0.6A - 7.2W

PS2 KB/MS

+5V_DUAL

(S0, S1) -> 0.345A - 1.73W
(S3) -> 2mA - 10mW

SPI

+3V

-> 30mA - 99mW

HDD

+12V
+5V

-> 0.75A - 9.0W
-> 0.75A - 3.75W

CD ROM

+12V
+5V

-> 0.75A - 9.0W
-> 0.75A - 3.75W

PEGATRON DT-MB RESTRICTED SECRET

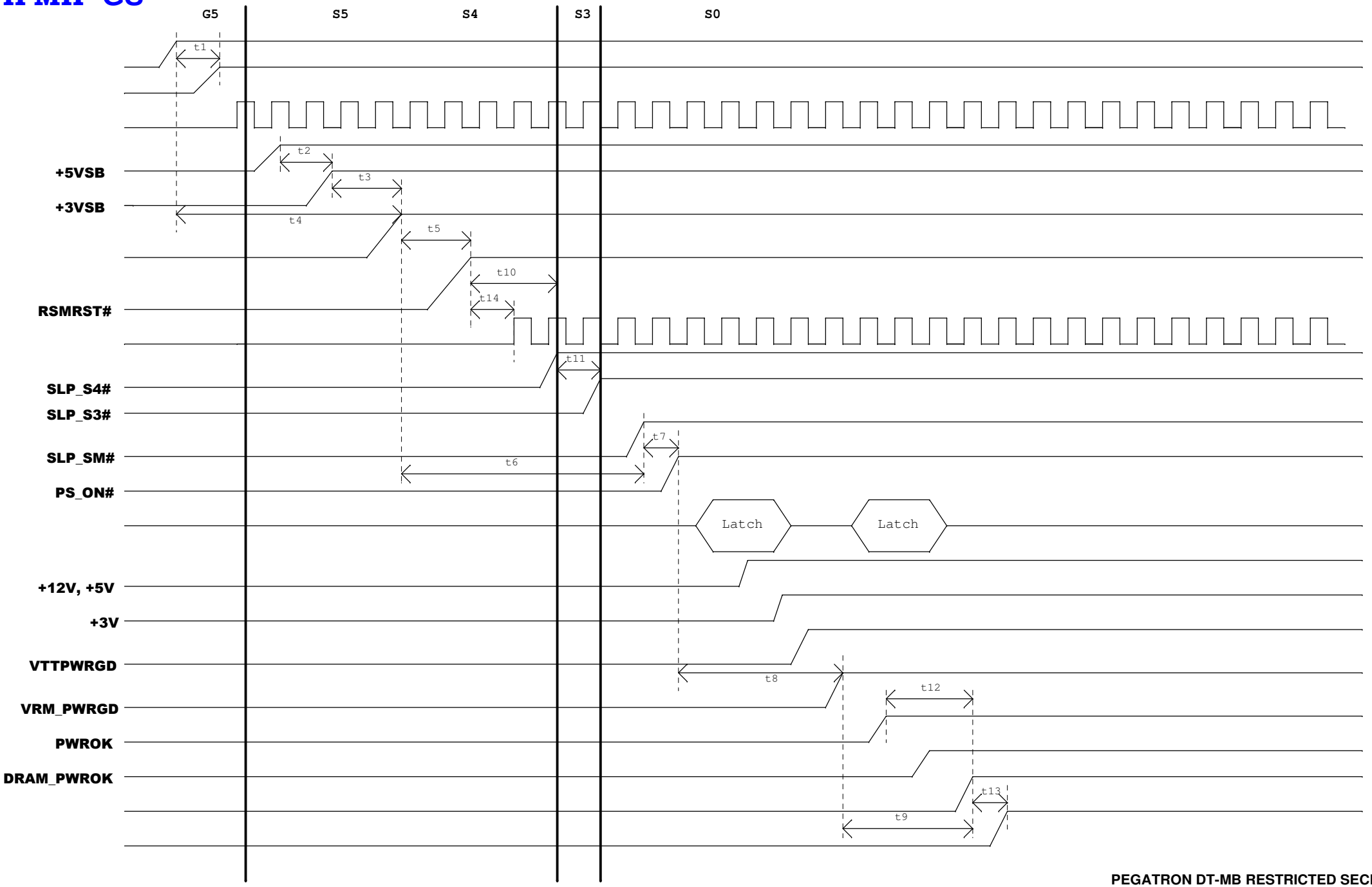
PEGATRON Title : POWER DISTRIBUTION

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Tuesday, March 23, 2010 Sheet 6 of 68

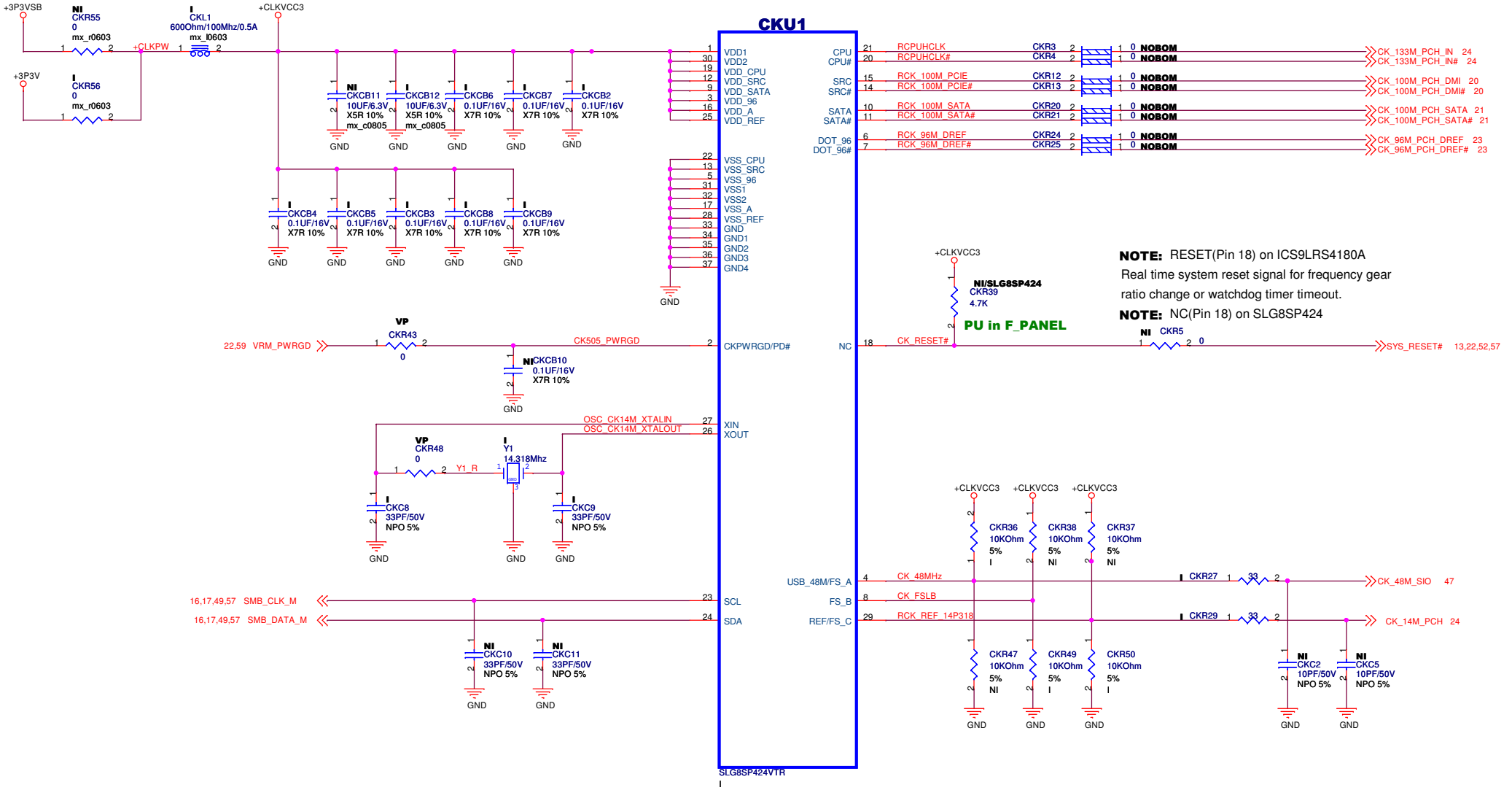
IPMIP-GS



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : POWER SEQUENCE	
Pegatron Corp.	Engineer: Michael Lee	
Size: A3	Project Name: IPMIP-GS	Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 7 of 68	

ICS9LRS4180AKLFT: 0610-0038000
SLG8SP424VTR: 0610-007D000



NOTE: RESET(Pin 18) on ICS9LRS4180A
Real time system reset signal for frequency gear ratio change or watchdog timer timeout.

NOTE: NC(Pin 18) on SLG8SP424

NOTE:

FSLC	FSLB	FSLA	CPU FREQ
0	0	1	133MHz
1	0	1	100MHz

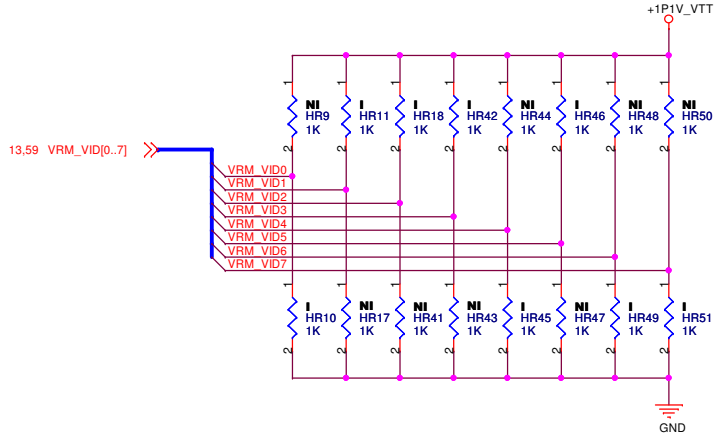
PEGATRON DT-MB RESTRICTED SECRET

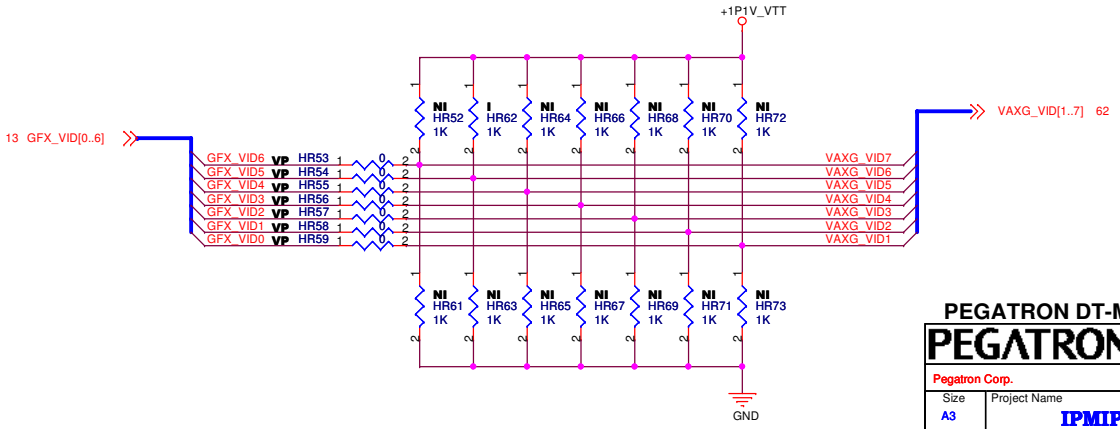
PEGATRON Title : ICS 4180/SLG 424

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 8 of 68





POWER ON CONFIGURATION (POC) TABLE

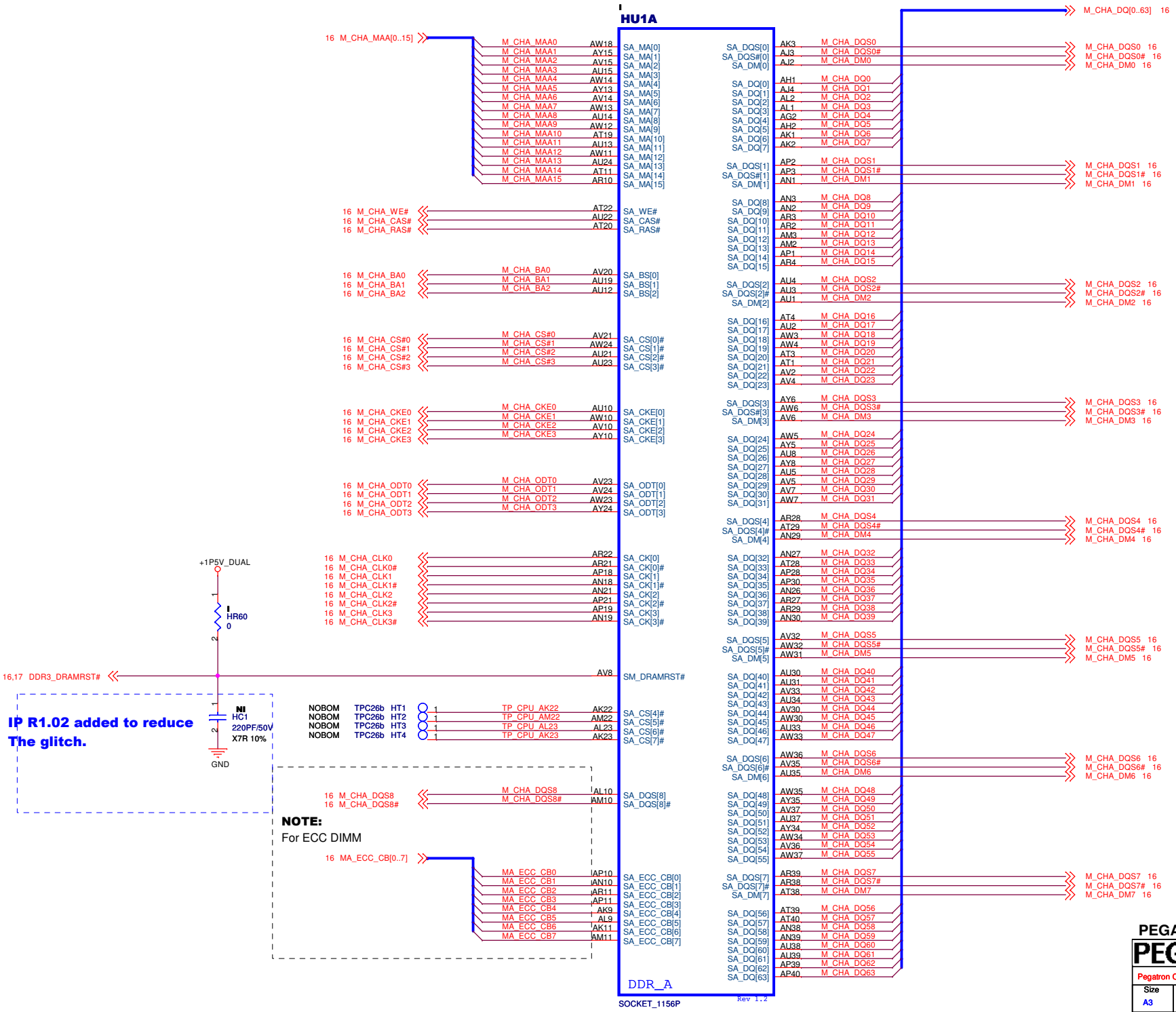
	FUNCTION	DEFAULT
VID0	MSI0	0
VID1	MSI1	1
VID2	MSI2	1
VID3	IMON CONFIG0	1
VID4	IMON CONFIG1	0
VID5	IMON CONFIG3	1
VID6	RESERVED	
VID7	VRD SELECT	LOW
PSI#	RESERVED	LOW

PEGATRON Title : VID RES

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.0.101

Date: Wednesday, April 07, 2010 Sheet 9 of 68



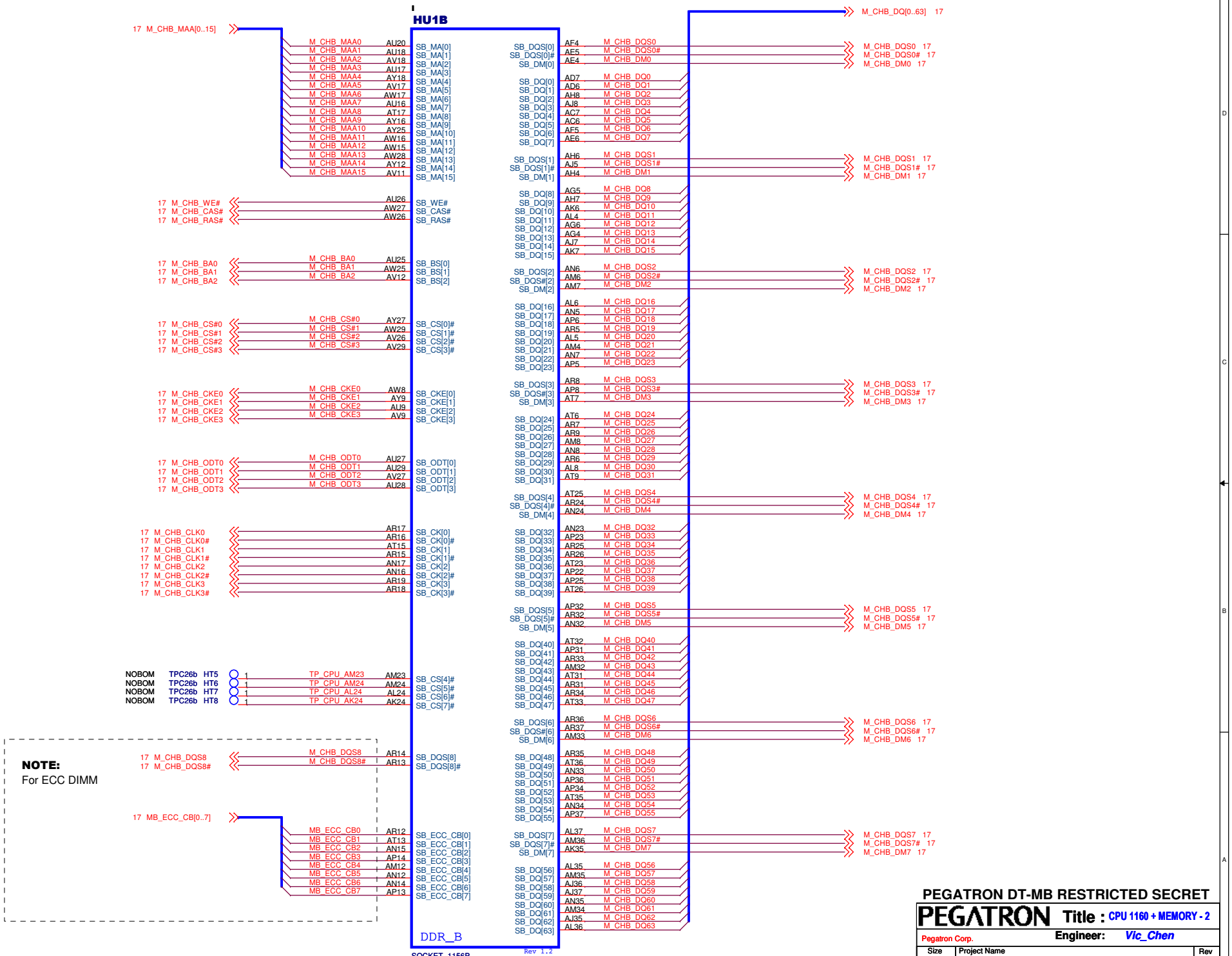
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU 1160 + MEMORY - 1

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 10 of 68



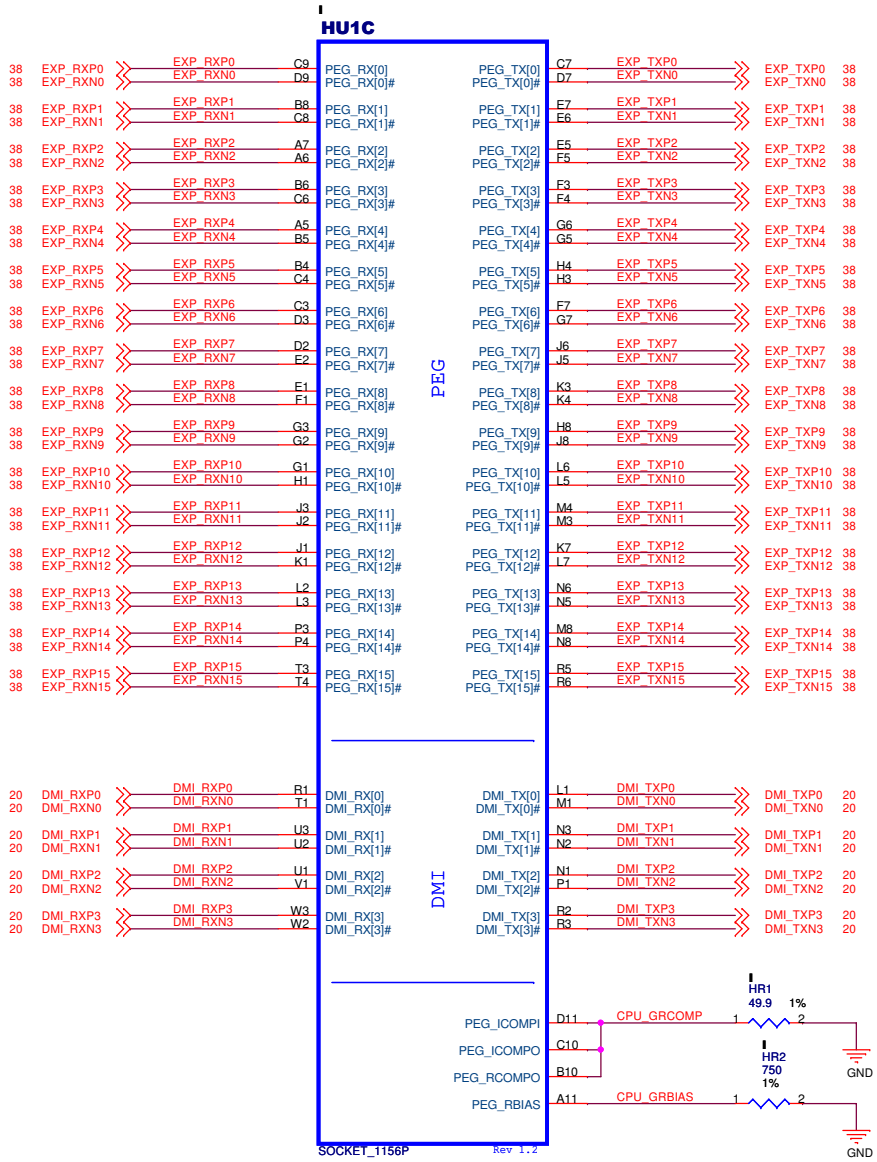
PEGATRON DT-MB RESTRICTED SECRET

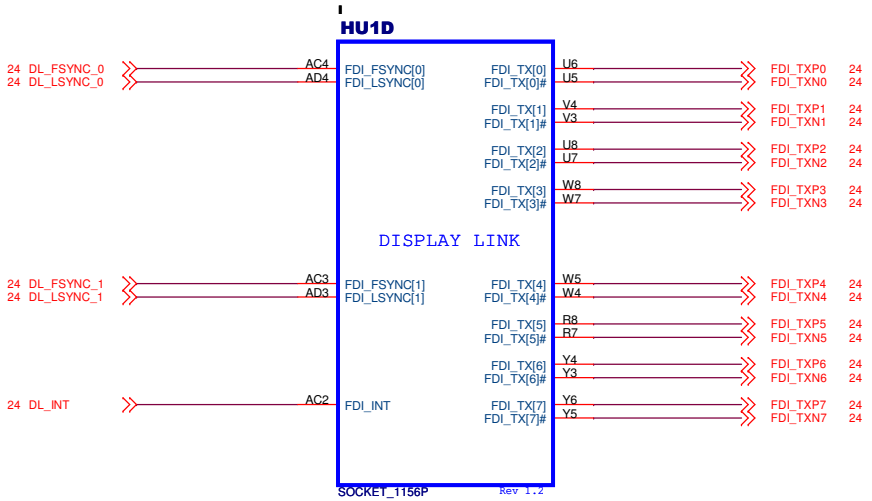
PEGATRON Title : CPU 1160 + MEMORY - 2

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 11 of 68





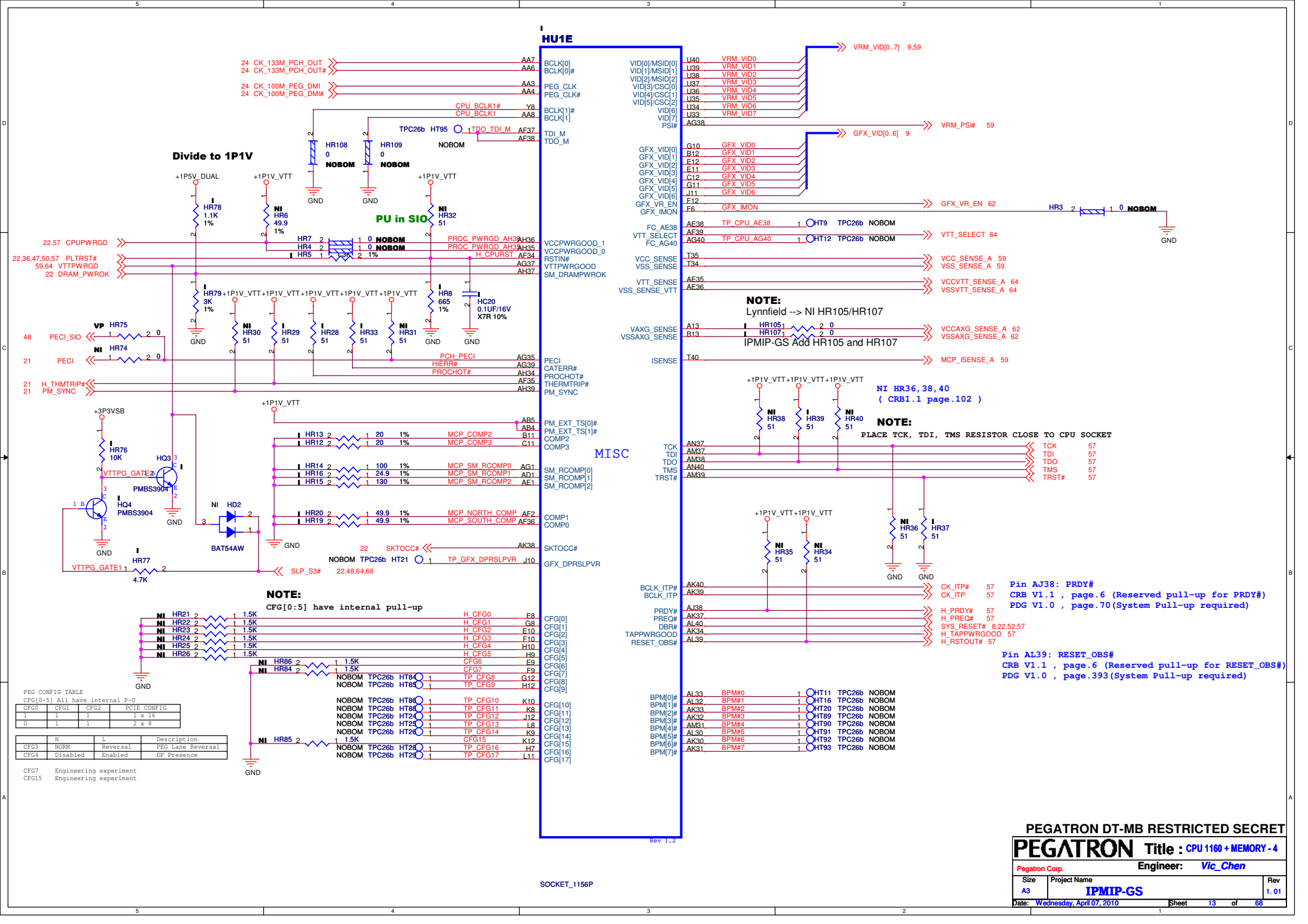
PEGATRON DT-MB RESTRICTED SECRET

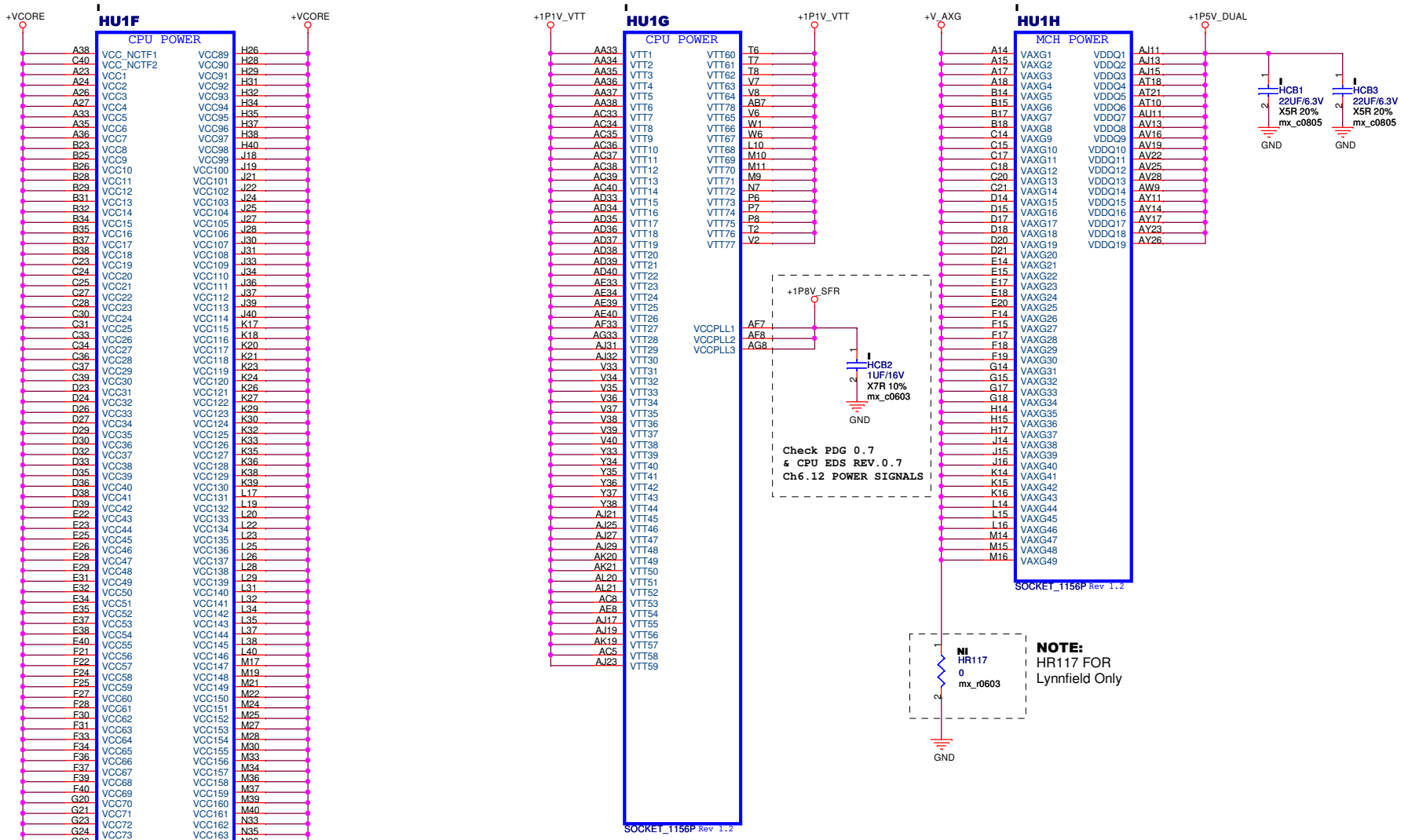
PEGATRON Title : CPU 1160 + MEMORY - 3

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 12 of 68


HU1E
Divide to 1P1V
PU in SIO
NOTE:
Lynnfield --> NI HR105/HR107
IPMIP-GS Add HR105 and HR107
NI HR36,38,40
(CRB1.1 page.102)
NOTE:
PLACE TCK, TDI, TMS RESISTOR CLOSE TO CPU SOCKET
NOTE:
CFG[0:5] have internal pull-up
MISC
Pin AJ38: PRDY#
CRB V1.1 , page.6 (Reserved pull-up for PRDY#)
PDG V1.0 , page.70(System Pull-up required)
Pin AL39: RESET_OBS#
CRB V1.1 , page.6 (Reserved pull-up for RESET_OBS#)
PDG V1.0 , page.393(System Pull-up required)
PEG CONFIG TABLE
CFG[0-5] All have internal P-U
CFG7 Engineering experiment
CFG15 Engineering experiment
SOCKET_1156P
Rev 1.2
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : CPU 1160 + MEMORY - 4
Pegatron Corp.
Engineer: Vic_Chen
Size A3
Project Name IPMIP-GS
Rev 1.01
Date: Wednesday, April 07, 2010
Sheet 13 of 68



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU 1160 + MEMORY - 5

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Tuesday, March 23, 2010 Sheet 14 of 68

HU1I

SOCKET_1156P Rev 1.2

HU1J

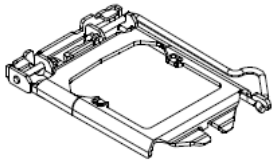
SOCKET_1156P Rev 1.2

IHR27 HR80 Change to I for QS CPU

NOTE:

Lynnfield	ES2	QS	Production
HR27	NI	I	I
HR80	NI	I	I

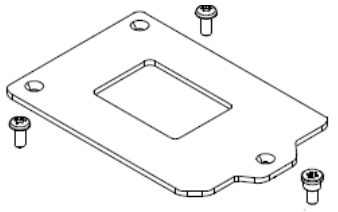
ILM1



INTEL LGA1156 SOCKET ILM

SOCKET1156_ILM

BACKPLATE1



INTEL LGA 1156P BACK PLATE,3 SCREW

PT44P11-6401

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU 1160 + MEMORY - 6

Pegatron Corp. Engineer: Vic_Chen

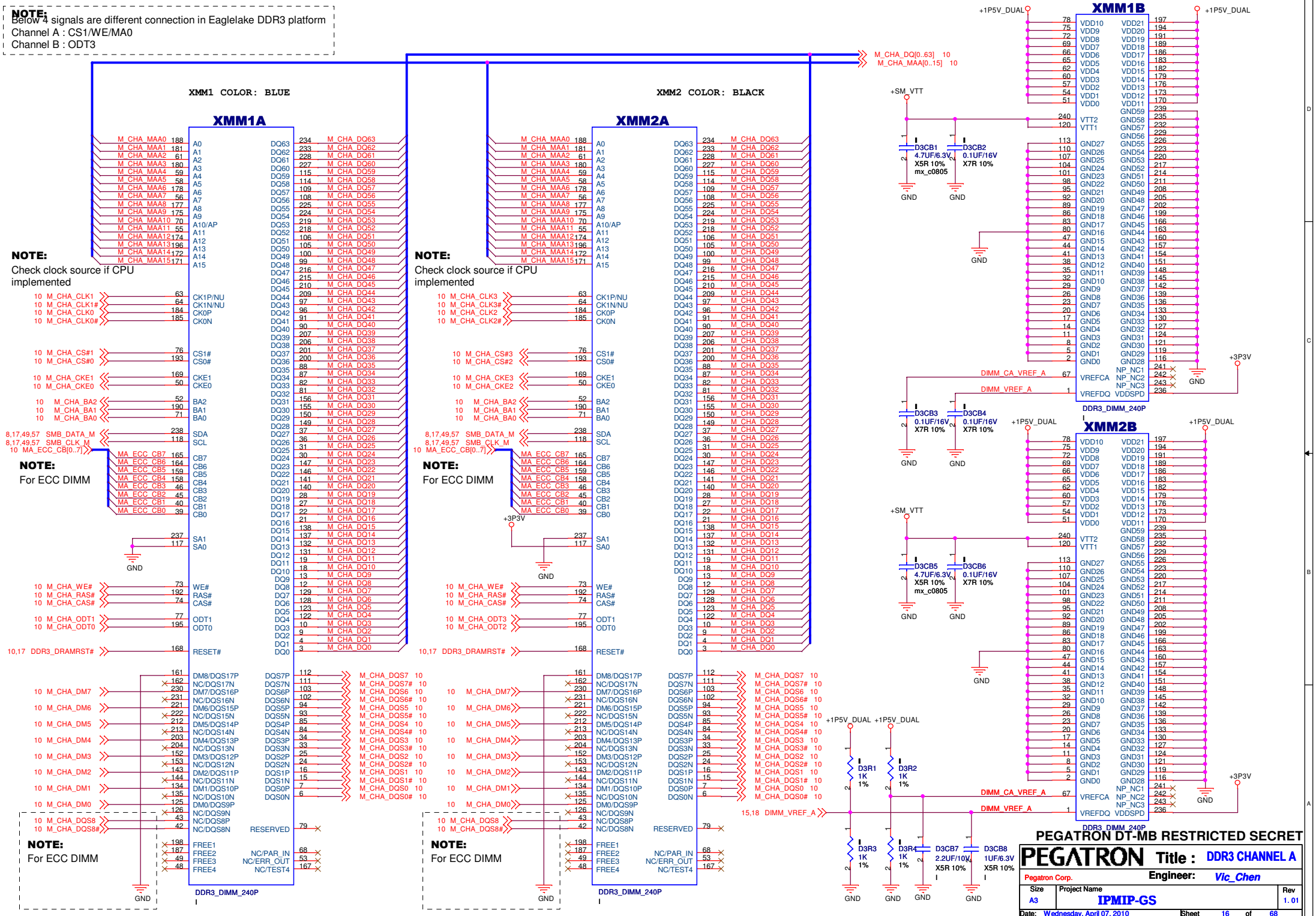
Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 15 of 68

NOTE:
Below 4 signals are different connection in Eaglelake DDR3 platform
Channel A : CS1/WE/MA0
Channel B : ODT3

XMM1 COLOR: BLUE

XMM2 COLOR: BLACK



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR3 CHANNEL A

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1. 01

Date: Wednesday, April 07, 2010 Sheet 16 of 68

XMM3 COLOR: BLUE

XMM4 COLOR: BLACK

XMM3A

XMM4A

XMM3B

XMM4B

NOTE:
Check clock source if CPU implemented

NOTE:
For ECC DIMM

DDR3_DIMM_240P

+1P5V_DUAL

+3P3V

+SM_VTT

GND

D3CB9 4.7UF/6.3V X5R 10% mx_c0805

D3CB10 0.1UF/16V X7R 10%

D3CB11 0.1UF/16V X7R 10%

D3CB12 0.1UF/16V X7R 10%

D3CB13 4.7UF/6.3V X5R 10% mx_c0805

D3CB14 0.1UF/16V X7R 10%

D3CB15 2.2UF/10V X5R 10%

D3CB16 1UF/6.3V X5R 10%

D3R5 1K 1%

D3R6 1K 1%

D3R7 1K 1%

D3R8 1K 1%

DIMM_CA_VREF_B

DIMM_VREF_B

15,18 DIMM_VREF_B

M_CHB_DQ[0..63] 11

M_CHB_MAA[0..15] 11

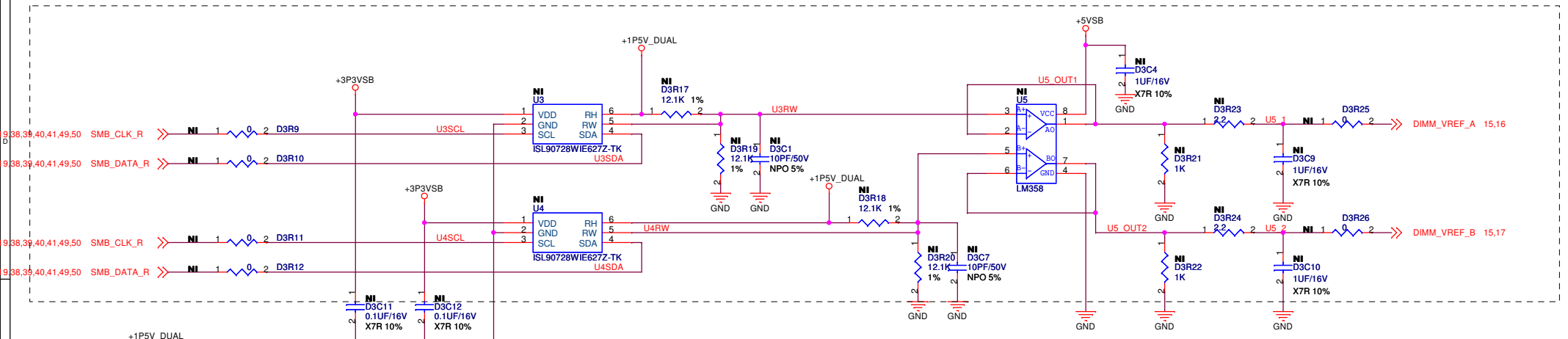
PEGATRON DT-MB RESTRICTED SECRET

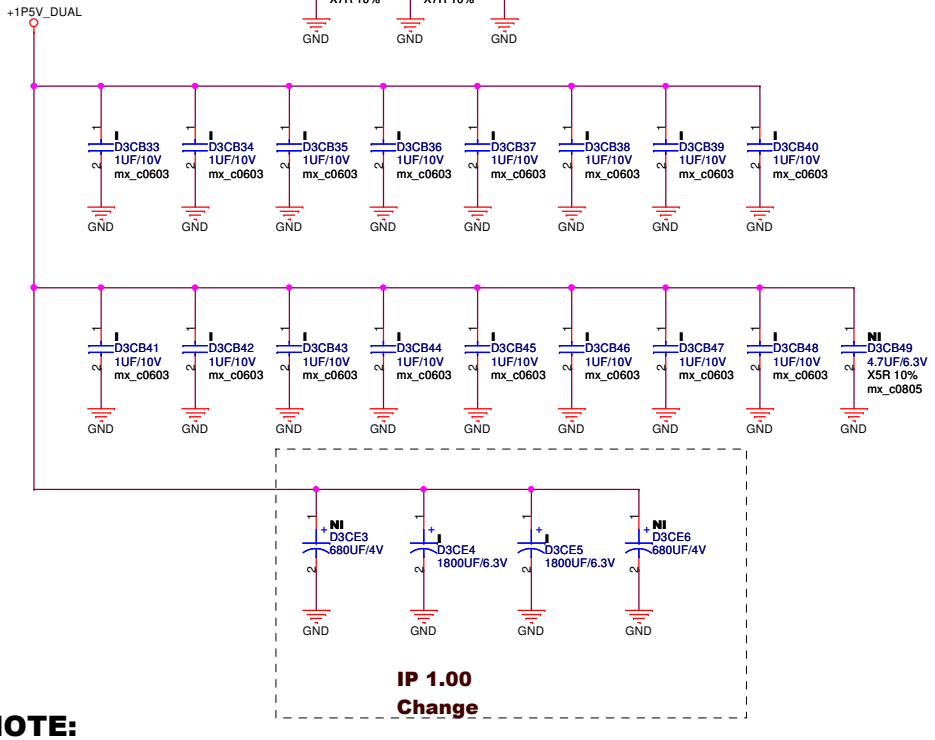
PEGATRON Title : DDR3 CHANNEL B

Pegatron Corp. Engineer: Vic_Chen

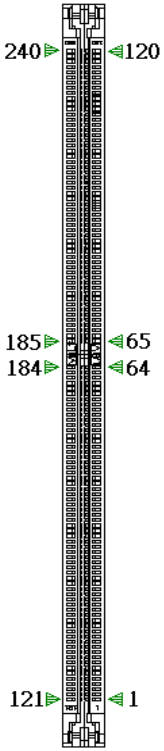
Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 17 of 68

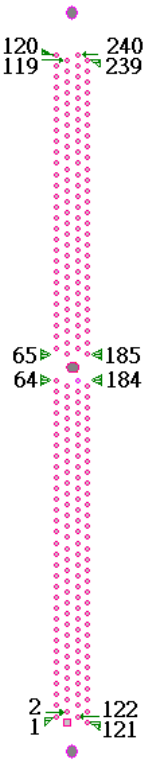




IP 1.00
Change



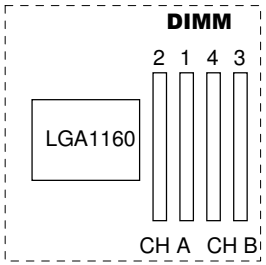
TOP SIDE VIEW

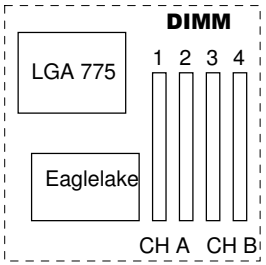


BOTTOM SIDE VIEW

NOTE:

DIMM Placement for different platform





PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DDR3 DECOUPLING	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-GS	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 18 of 68	

P55 ES2: 0200-006T000

Strap
(GNT0#~GNT3# have IPU)

GNT3#	0	TOP Block SWAP
	1	Normal(Default)

GNT2#	0	ESI mode (Server Only)
	1	DMI(Default)

GNT1#	GNT0#	BOOT BIOS
1	0	RESERVED
0	1	PCI
1	1	SPI
0	0	LPC

U1A

PCI: PCIRST#, PME#, PAR, DEVSEL#, CLKIN_PCILOOPBACK, IRDY#, SERR#, STOP#, PLOCK#, TRDY#, PERR#, FRAME#, C/BE0#, C/BE1#, C/BE2#, C/BE3#, GNT3#/GPIO55, GNT2#/GPIO53, GNT1#/GPIO51, GNT0#, AD0–AD31, REQ3#/GPIO54, REQ2#/GPIO52, REQ1#/GPIO50, REQ0#, PIRQA#, PIRQB#, PIRQC#, PIRQD#, PIRQE#/GPIO2, PIRQF#/GPIO3, PIRQG#/GPIO4, PIRQH#/GPIO5

SMBUS: SMBCLK, SMBDATA, SMBALERT#/GPIO11, SML0CLK, SML0DATA, SML0ALERT#/GPIO60, SML1ALERT#/GPIO74, SML1CLK/GPIO58, SML1DATA/GPIO75

RTC: RTCRST#, SRTCRST#, RTCX1, RTCX2

SPI: SPI_CS1#, SPI_CS0#, SPI_MOSI, SPI_MISO, SPI_CLK

IBEXPEAK Rev 1.0

Strap

SPI_MOSI (IPD)	0	Disable ITPM (Default)
	1	Enable ITPM

CRB R1.0 (page.39) suggests that don't change it to 0402 package type

XY5 Crystal Holder

Y5 32.768Khz

SR13 MX_R0603 10MOhm

NOBOM SR15

SC1 15PF/50V NPO 5%

SC2 15PF/50V NPO 5%

SC6 SC7 SC25 SC26 SC4 SC5 150PF/50V NPO 5%

SR154 SR155 SR152 SR153 SR131 SR132 2.2K

SR1 SR2 SR9 SR40 1K

SR3 SR4 SR5 10K

SR8 SR14 1K

ST26 TPC26b NOBOM

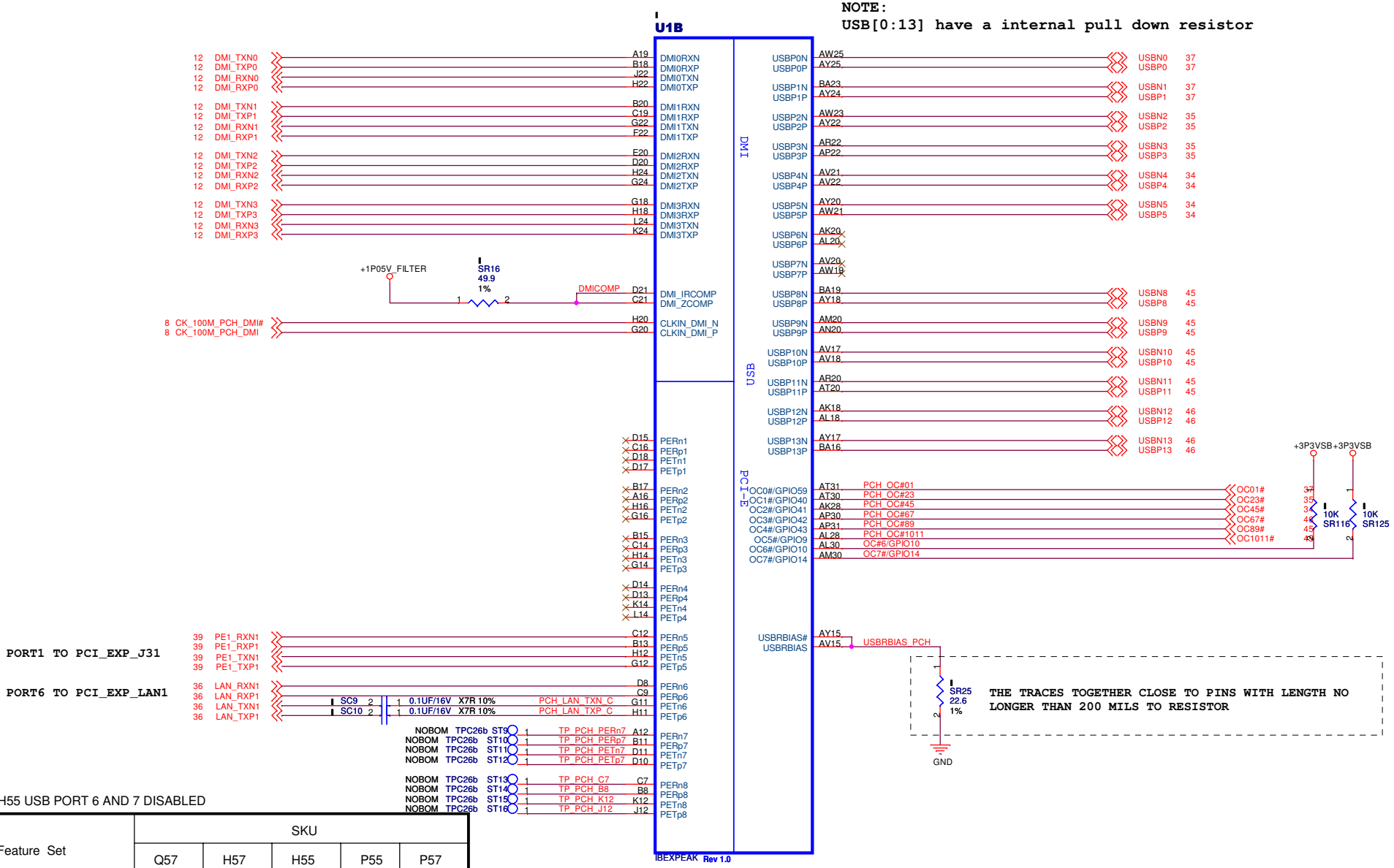
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : INTEL_PCH-1

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Thursday, April 08, 2010 Sheet 19 of 68



NOTE: FOR H55 USB PORT 6 AND 7 DISABLED

Feature Set	SKU				
	Q57	H57	H55	P55	P57
PCI Express 2.0	8	8	6	8	8
USB 2.0	14	14	12	14	14
SATA	6	6	6	6	6
HDMI/DVI/VGA/SDVO/DisplayPort	YES	YES	YES	NO	NO

PEGATRON DT-MB RESTRICTED SECRET

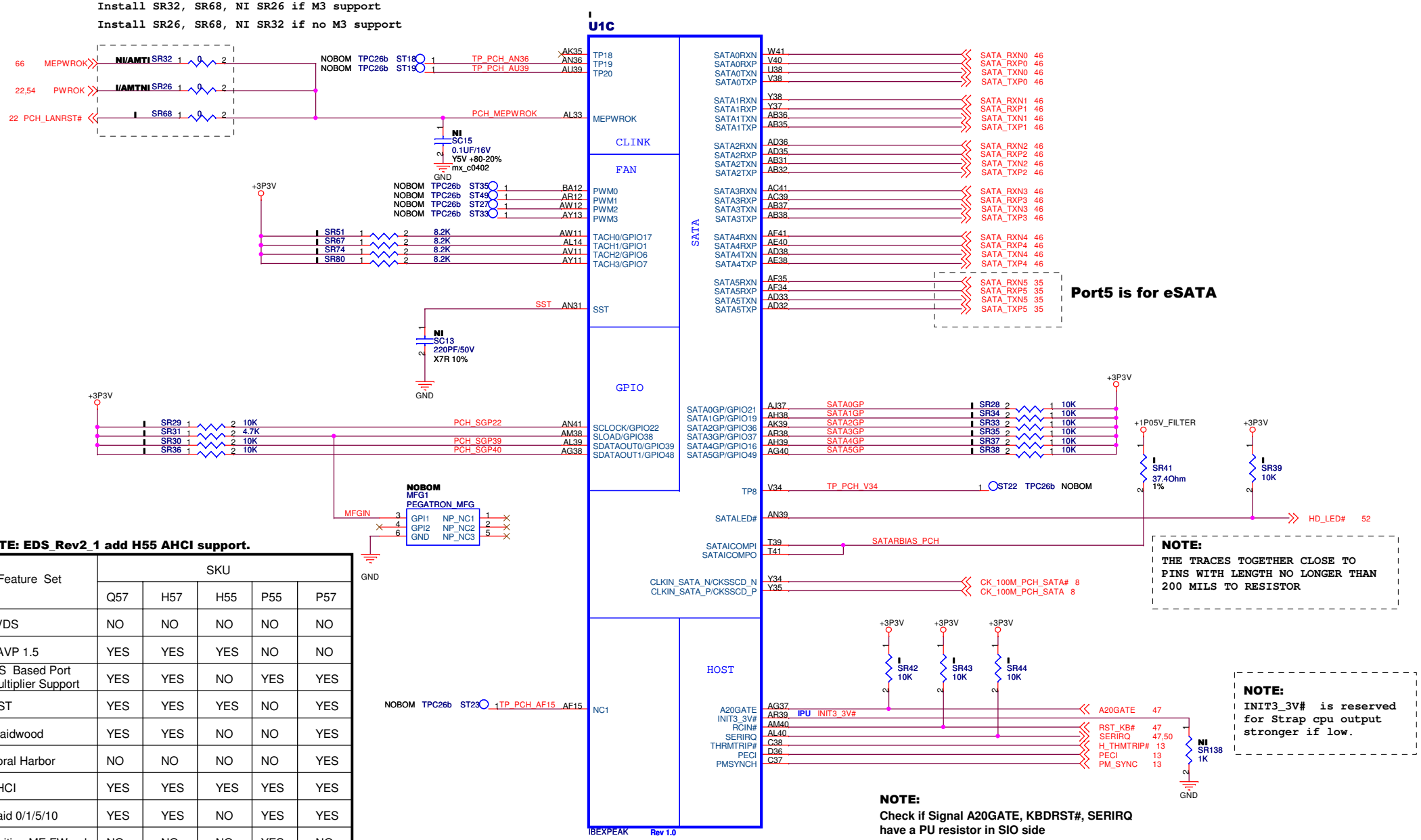
PEGATRON Title : INTEL_PCH - 2

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 20 of 68

NOTE:
Install SR32, SR68, NI SR26 if M3 support
Install SR26, SR68, NI SR32 if no M3 support



Port5 is for eSATA

NOTE:
THE TRACES TOGETHER CLOSE TO PINS WITH LENGTH NO LONGER THAN 200 MILS TO RESISTOR

NOTE:
INIT3_3V# is reserved for Strap cpu output stronger if low.

NOTE:
Check if Signal A20GATE, KBDRST#, SERIRQ have a PU resistor in SIO side

NOTE: EDS_Rev2_1 add H55 AHCI support.

Feature Set	SKU				
	Q57	H57	H55	P55	P57
LVDS	NO	NO	NO	NO	NO
PAVP 1.5	YES	YES	YES	NO	NO
FIS Based Port Multiplier Support	YES	YES	NO	YES	YES
QST	YES	YES	YES	NO	YES
Braidwood	YES	YES	NO	NO	YES
Coral Harbor	NO	NO	NO	NO	YES
AHCI	YES	YES	YES	YES	YES
Raid 0/1/5/10	YES	YES	NO	YES	YES
Ignition ME FW only	NO	NO	NO	YES	NO
AT-p	YES	NO	NO	NO	NO
iAMT 6.0	YES	NO	NO	NO	NO
IRPA for Business	YES	NO	NO	NO	NO
IRPA for Consumer	NO	YES	NO	NO	NO
IRWT	NO	YES	YES	NO	NO

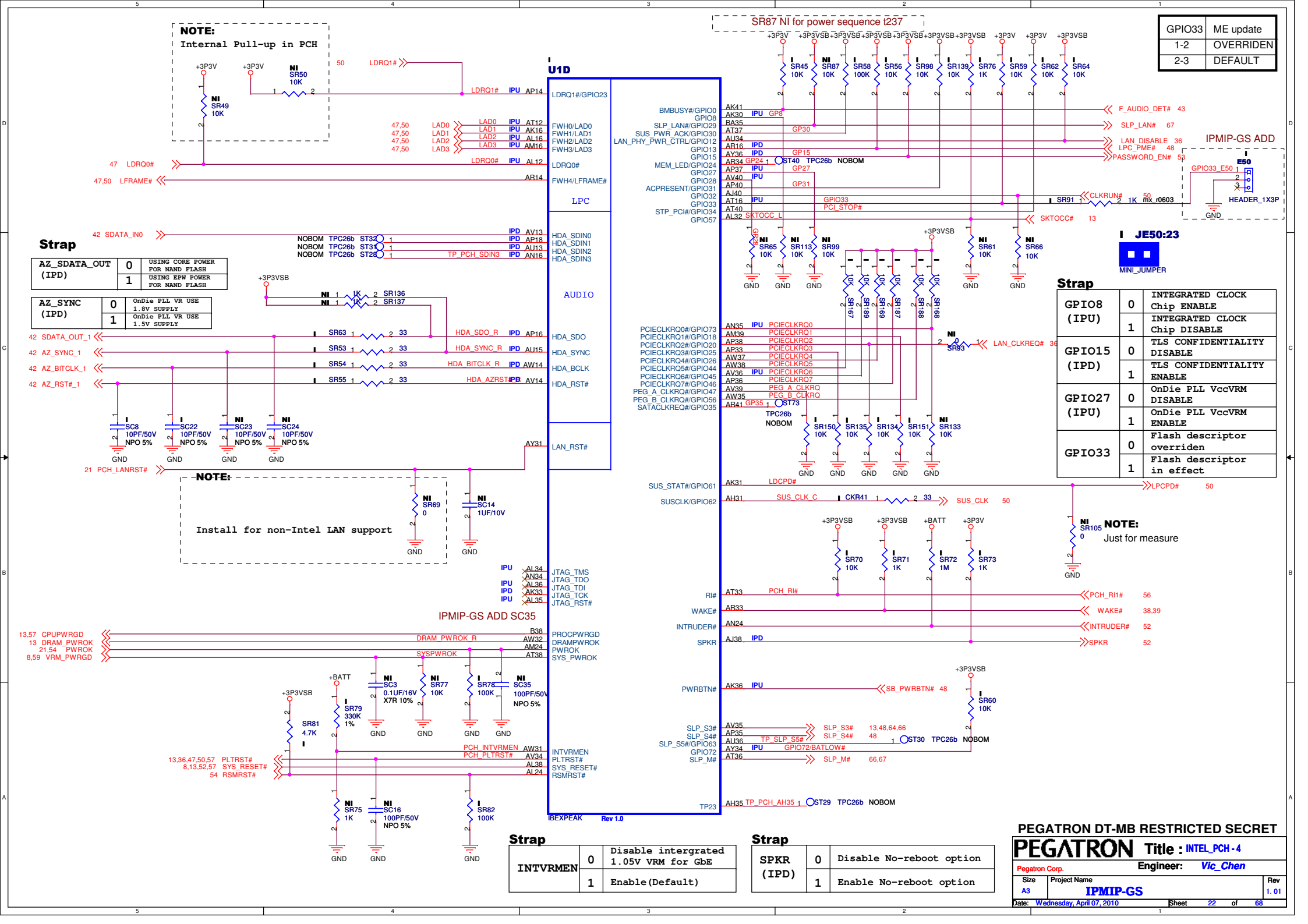
PEGATRON DT-MB RESTRICTED SECRET

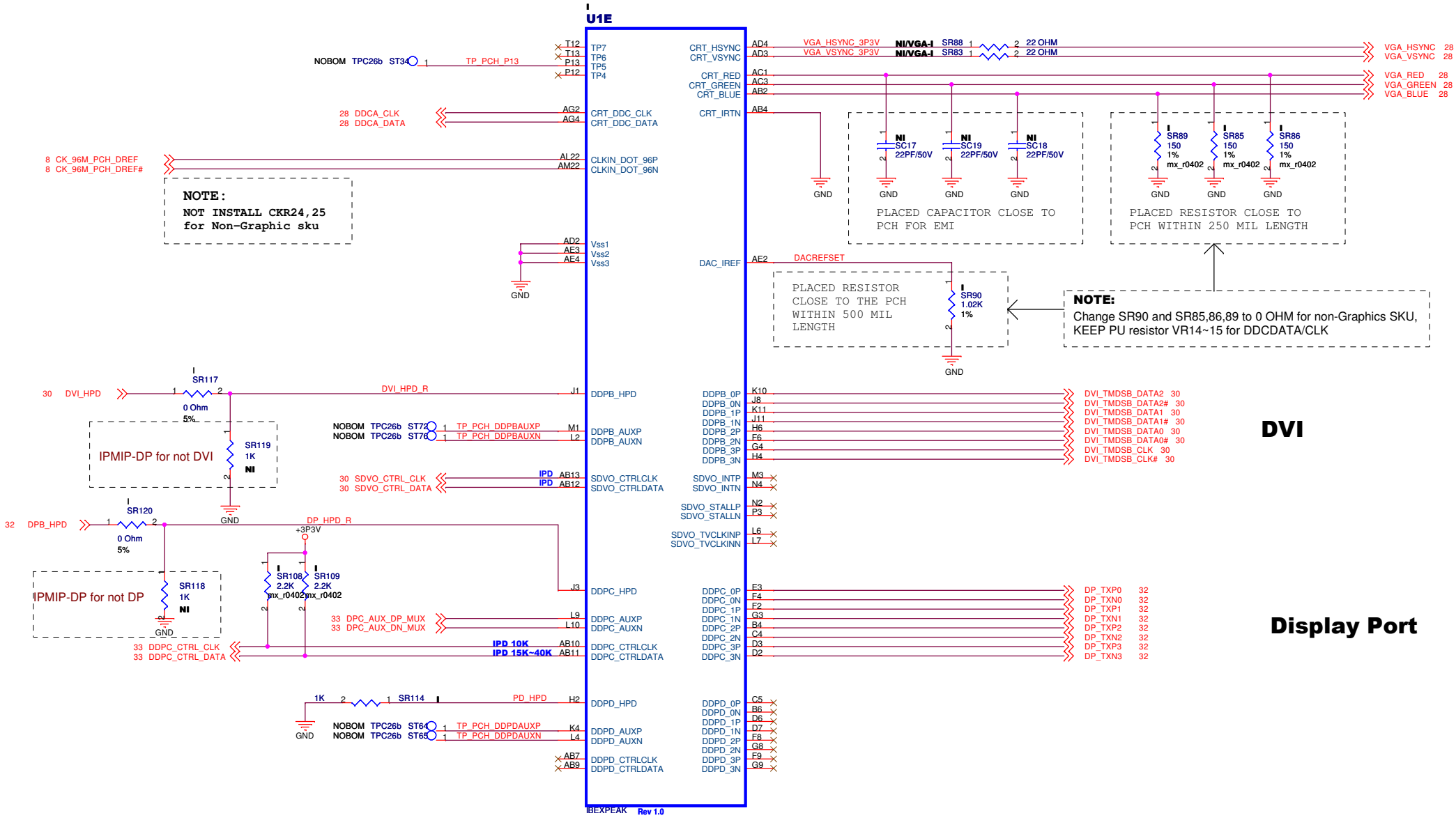
PEGATRON Title : INTEL_PCH - 3

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 21 of 68


NOTE:
Internal Pull-up in PCH
SR87 NI for power sequence t237
GPIO33 | ME update
1-2 | OVERRIDEN
2-3 | DEFAULT
U1D
IBEXPEAK Rev 1.0
LPC
AUDIO
LAN_RST#
Strap
AZ_SDATA_OUT (IPD)
0 USING CORE POWER FOR NAND FLASH
1 USING EPW POWER FOR NAND FLASH
AZ_SYNC (IPD)
0 OnDie PLL VR USE 1.8V SUPPLY
1 OnDie PLL VR USE 1.5V SUPPLY
NOTE:
Install for non-Intel LAN support
IPMIP-GS ADD SC35
IPMIP-GS ADD
JE50:23
MINI_JUMPER
Strap
GPIO8 (IPU)
0 INTEGRATED CLOCK Chip ENABLE
1 INTEGRATED CLOCK Chip DISABLE
GPIO15 (IPD)
0 TLS CONFIDENTIALITY DISABLE
1 TLS CONFIDENTIALITY ENABLE
GPIO27 (IPU)
0 OnDie PLL VccVRM DISABLE
1 OnDie PLL VccVRM ENABLE
GPIO33
0 Flash descriptor overriden
1 Flash descriptor in effect
NOTE:
Just for measure
Strap
INTVRMEN
0 Disable intergrated 1.05V VRM for GbE
1 Enable(Default)
Strap
SPKR (IPD)
0 Disable No-reboot option
1 Enable No-reboot option
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : INTEL_PCH - 4
Pegatron Corp. Engineer: Vic_Chen
Size A3 Project Name IPMIP-GS Rev 1.01
Date: Wednesday, April 07, 2010 Sheet 22 of 68



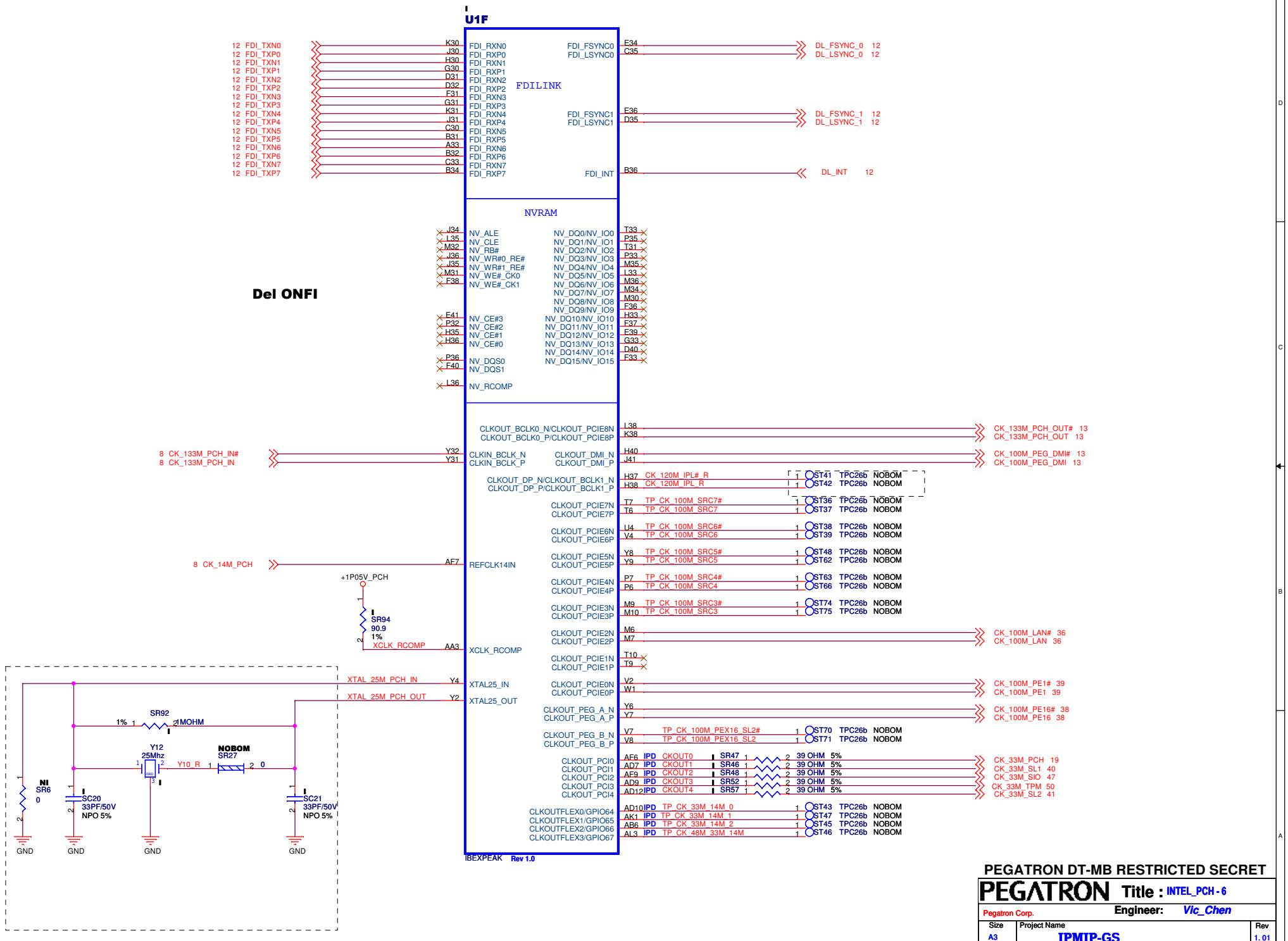
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : INTEL_PCH - 5

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 23 of 68



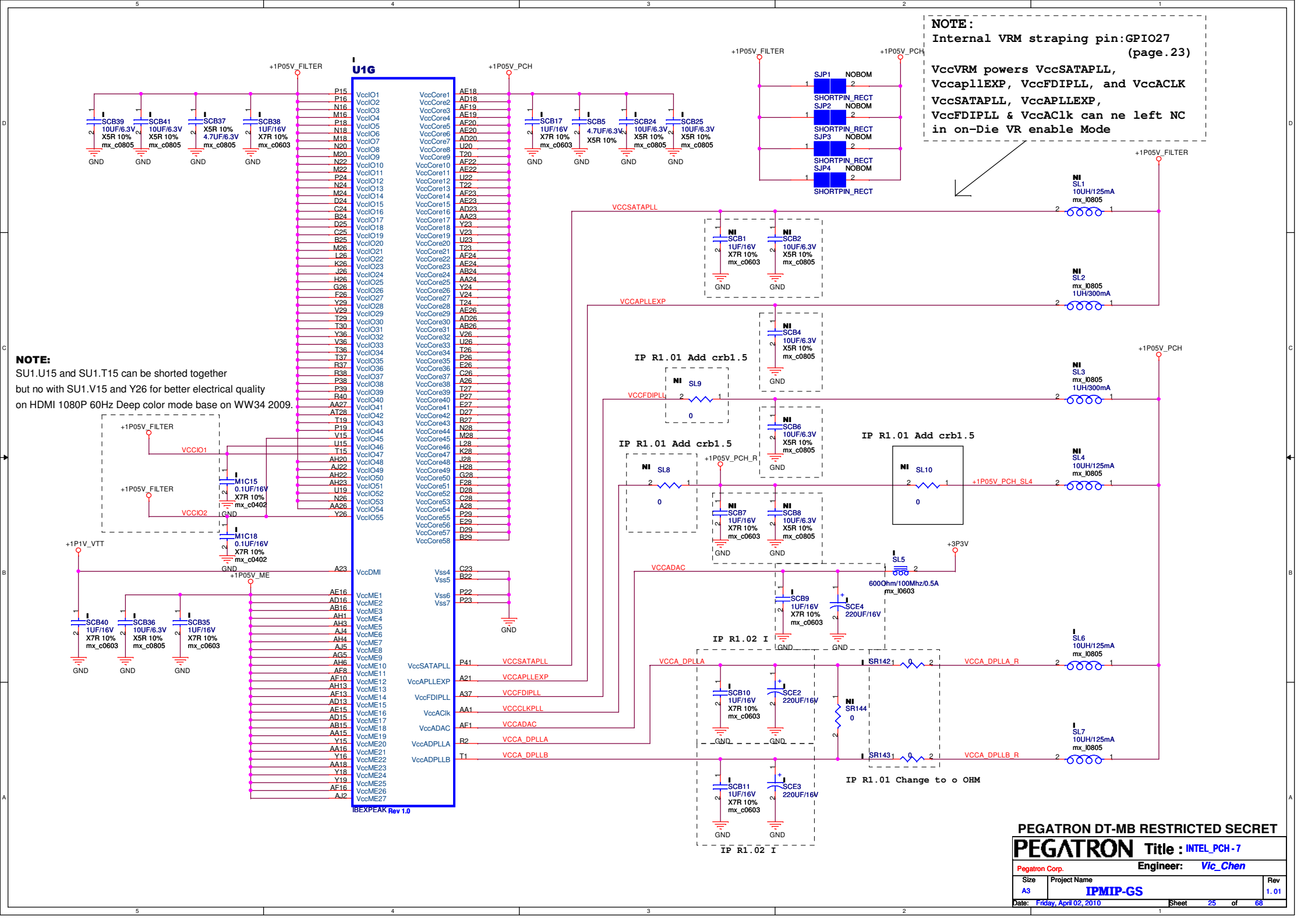
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : INTEL_PCH - 6

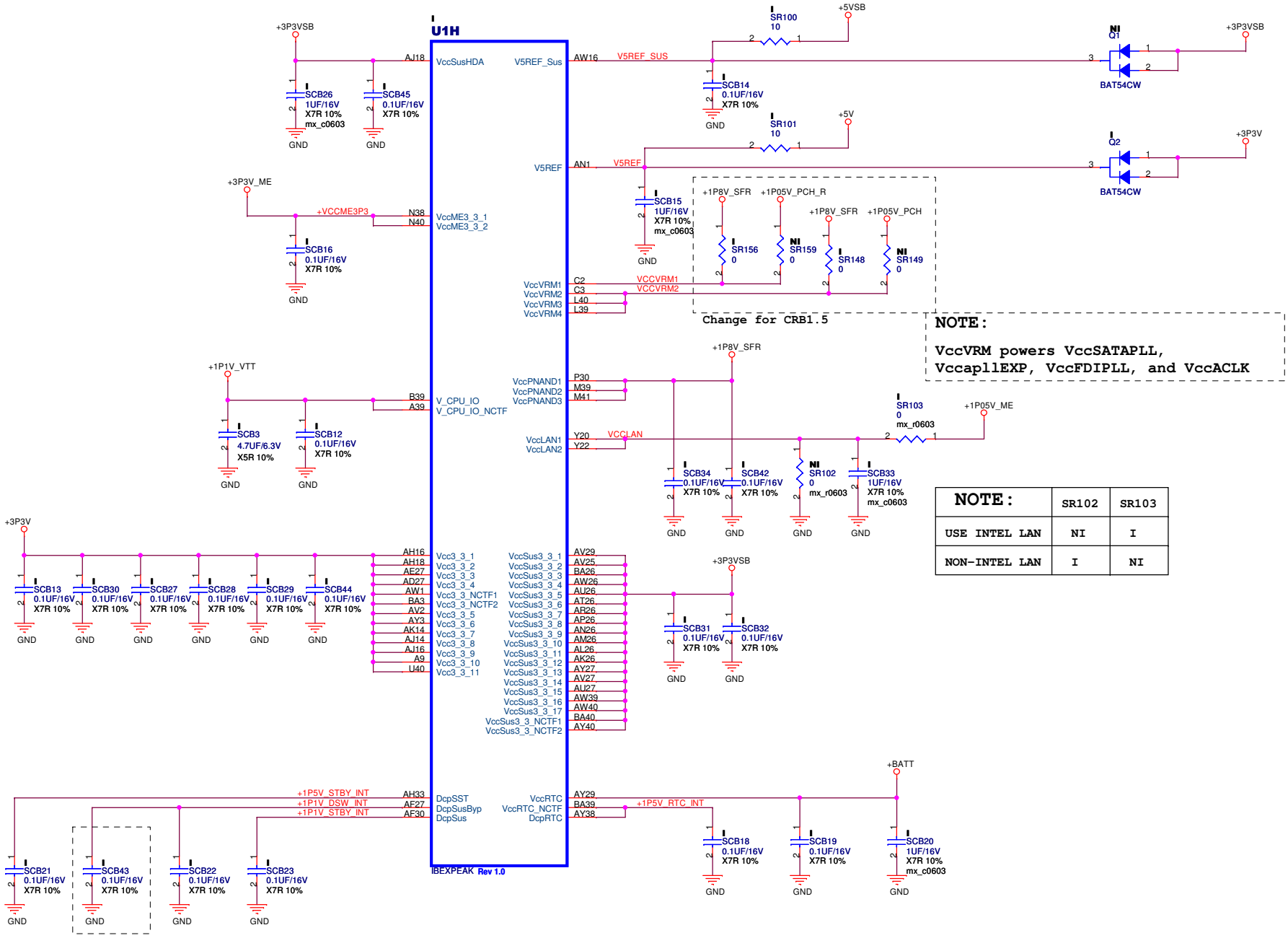
Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1. 01

Date: Wednesday, April 07, 2010 Sheet 24 of 68


NOTE:
Internal VRM straping pin:GPIO27
(page.23)
VccVRM powers VccSATAPLL,
VccapllEXP, VccFDIPLL, and VccACLK
VccSATAPLL, VccAPLLEXP,
VccFDIPLL & VccAClk can ne left NC
in on-Die VR enable Mode
NOTE:
SU1.U15 and SU1.T15 can be shorted together
but no with SU1.V15 and Y26 for better electrical quality
on HDMI 1080P 60Hz Deep color mode base on WW34 2009.
U1G
IBEXPEAK Rev 1.0
IP R1.01 Add crb1.5
IP R1.01 Add crb1.5
IP R1.01 Add crb1.5
IP R1.02 I
IP R1.02 I
IP R1.01 Change to o OHM
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : INTEL_PCH-7
Pegatron Corp.
Engineer: Vic_Chen
Size A3
Project Name IPMIP-GS
Rev 1.01
Date: Friday, April 02, 2010
Sheet 25 of 68

Note
Place SCB45 close to
SU1.AJ18 for EMI issue



Change for CRB1.5

NOTE:
VccVRM powers VccSATAPLL, VccapllEXP, VccFDIPLL, and VccACLK

NOTE:	SR102	SR103
USE INTEL LAN	NI	I
NON-INTEL LAN	I	NI

NOTE:
MOW WW08 recommand to reserved SCB43.

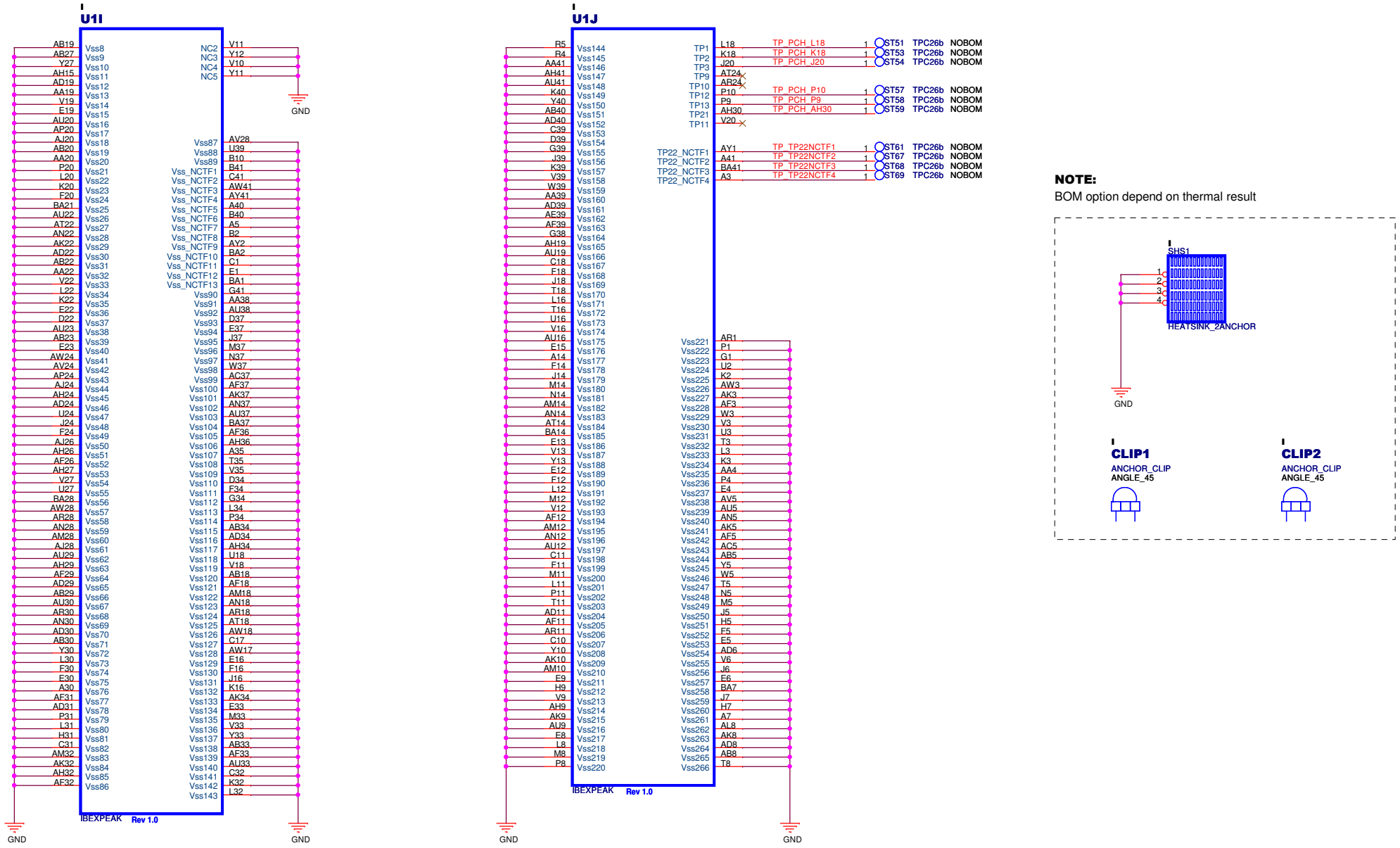
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : INTEL_PCH-8

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Tuesday, March 23, 2010 Sheet 26 of 68



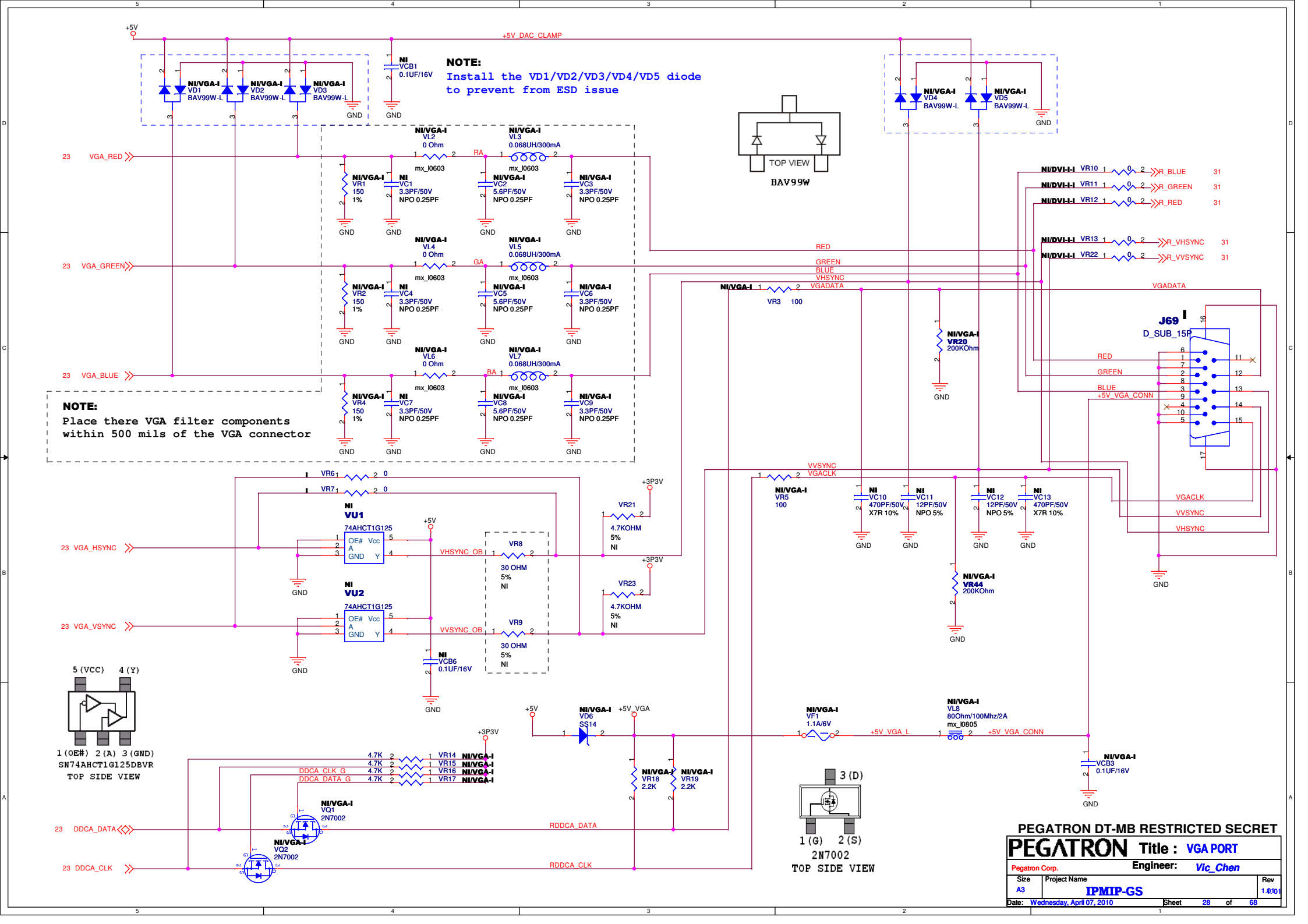
PEGATRON DT-MB RESTRICTED SECRET

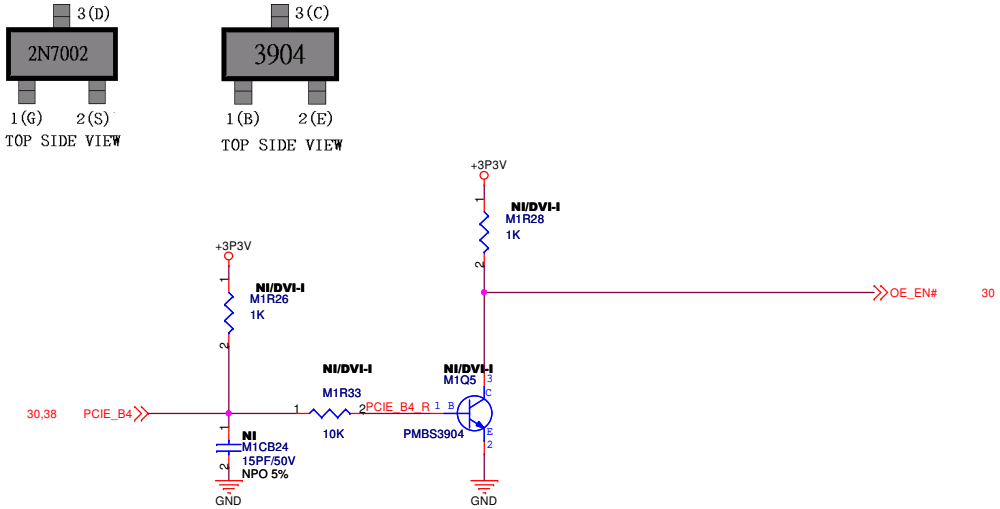
PEGATRON Title : INTEL_PCH - 9

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Tuesday, March 23, 2010 Sheet 27 of 68


NOTE:
Install the VD1/VD2/VD3/VD4/VD5 diode
to prevent from ESD issue
TOP VIEW
BAV99W
NOTE:
Place there VGA filter components
within 500 mils of the VGA connector
1(OE#) 2(A) 3(GND)
SN74AHCT1G125DBVR
TOP SIDE VIEW
5(VCC) 4(Y)
3(D)
1(G) 2(S)
2N7002
TOP SIDE VIEW
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : VGA PORT
Pegatron Corp.
Engineer: Vic_Chen
Size A3
Project Name IPMIP-GS
Rev 1.0.101
Date: Wednesday, April 07, 2010
Sheet 28 of 68



NOTE:

PCIE X16	PCIE_B4	SEL (MUX)	DDC_EN# (Level Shifter)	OE_EN# (Level Shifter)	Function
Plugged	LOW	LOW	LOW	HI	PCIE x16
Unplugged	HI	HI	HI	LOW	DVI , HDMI

PEGATRON DT-MB RESTRICTED SECRET

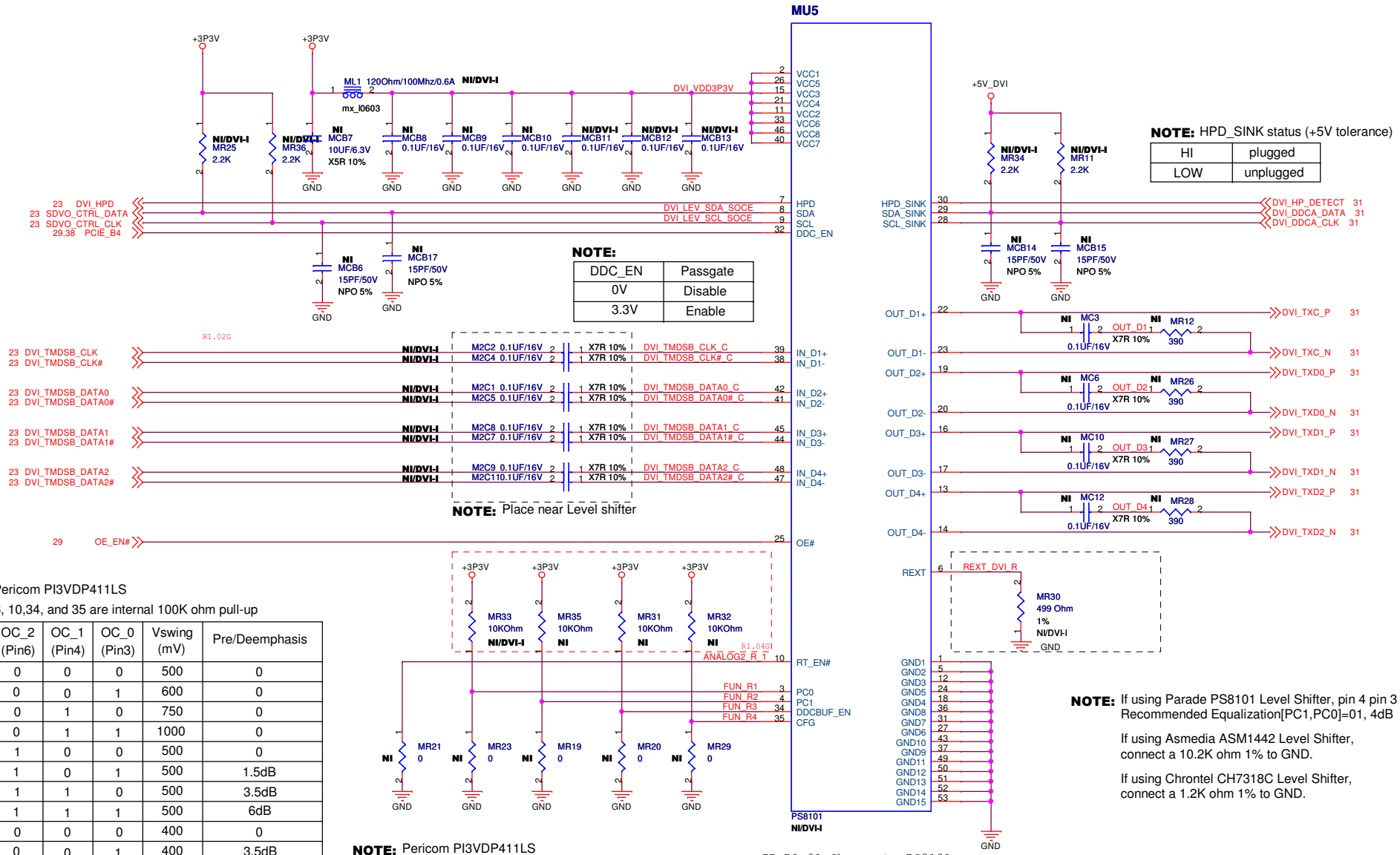
PEGATRON Title : DVI Control

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 29 of 68

CH7318: 02G480001000
ASM1442: 022U-0004000



NOTE: HPD_SINK status (+5V tolerance)

HI	plugged
LOW	unplugged

NOTE:

DDC_EN	Passgate
0V	Disable
3.3V	Enable

NOTE: Place near Level shifter

NOTE: Pericom PI3VDP411LS

Pin 3, 4, 6, 10,34, and 35 are internal 100K ohm pull-up

OC_3 (Pin10)	OC_2 (Pin6)	OC_1 (Pin4)	OC_0 (Pin3)	Vswing (mV)	Pre/Deemphasis
0	0	0	0	500	0
0	0	0	1	600	0
0	0	1	0	750	0
0	0	1	1	1000	0
0	1	0	0	500	0
0	1	0	1	500	1.5dB
0	1	1	0	500	3.5dB
0	1	1	1	500	6dB
1	0	0	0	400	0
1	0	0	1	400	3.5dB
1	0	1	0	400	6dB
1	0	1	1	400	9dB
1	1	0	0	1000	0
1	1	0	1	1000	-3.5dB
1	1	1	0	1000	-6dB
1	1	1	1	1000	-9dB

NOTE: Pericom PI3VDP411LS

EQ0 (Pin34)	EQ1 (Pin35)	Equalization (dB)
0	0	3
0	1	7.2
1	0	10
1	1	12

NOTE:

OE*	IN_D Termination	OUT_D Outputs
1	Hi-Z	Hi-Z
0	50ohm	Active

IP R1.01 Change to PS8101

NOTE: If using Parade PS8101 Level Shifter, pin 4 pin 3 Recommended Equalization[PC1,PC0]=01, 4dB

If using Asmedia ASM1442 Level Shifter, connect a 10.2K ohm 1% to GND.

If using Chrontel CH7318C Level Shifter, connect a 1.2K ohm 1% to GND.

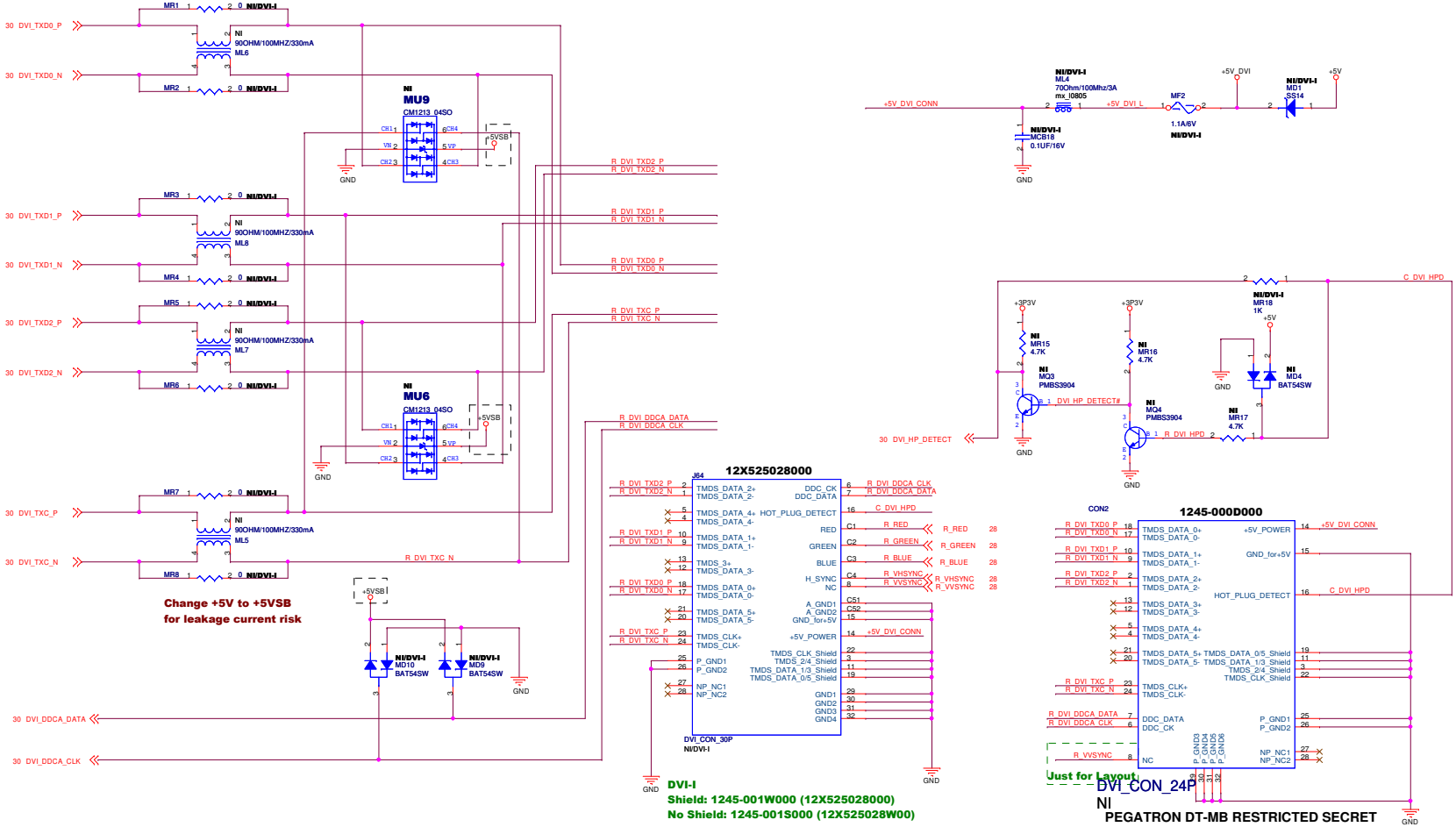
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DVI Level shifter

Pegatron Corp. Engineer: Vic_Chen

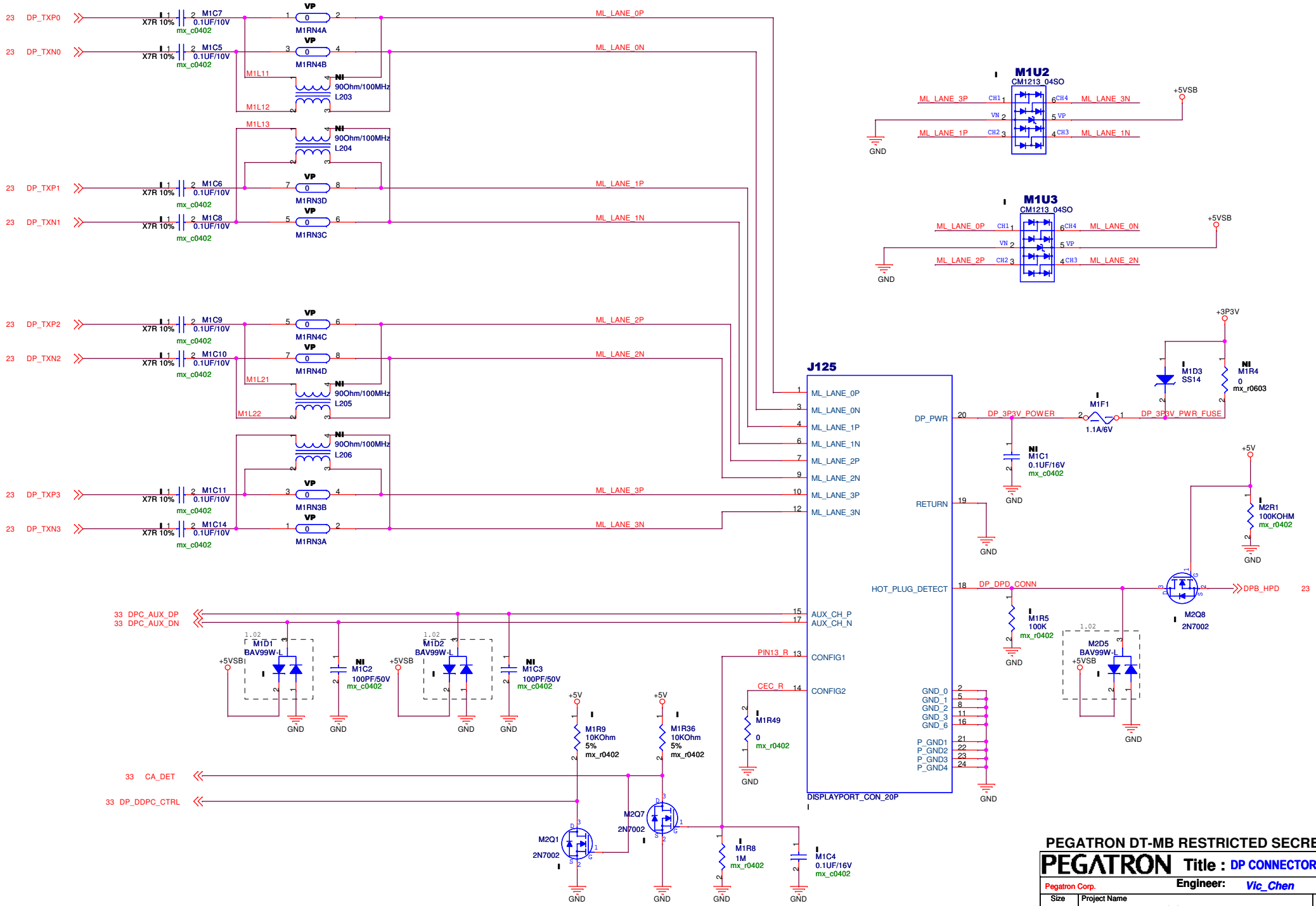
Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 30 of 68



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DVI-I Connector		
Pegatron Corp.	Engineer: Vic_Chen		
Size: A2	Project Name: IPMIP-GS		Rev
Date: Wednesday, April 07, 2010	Sheet 31 of 68		



PEGATRON DT-MB RESTRICTED SECRET

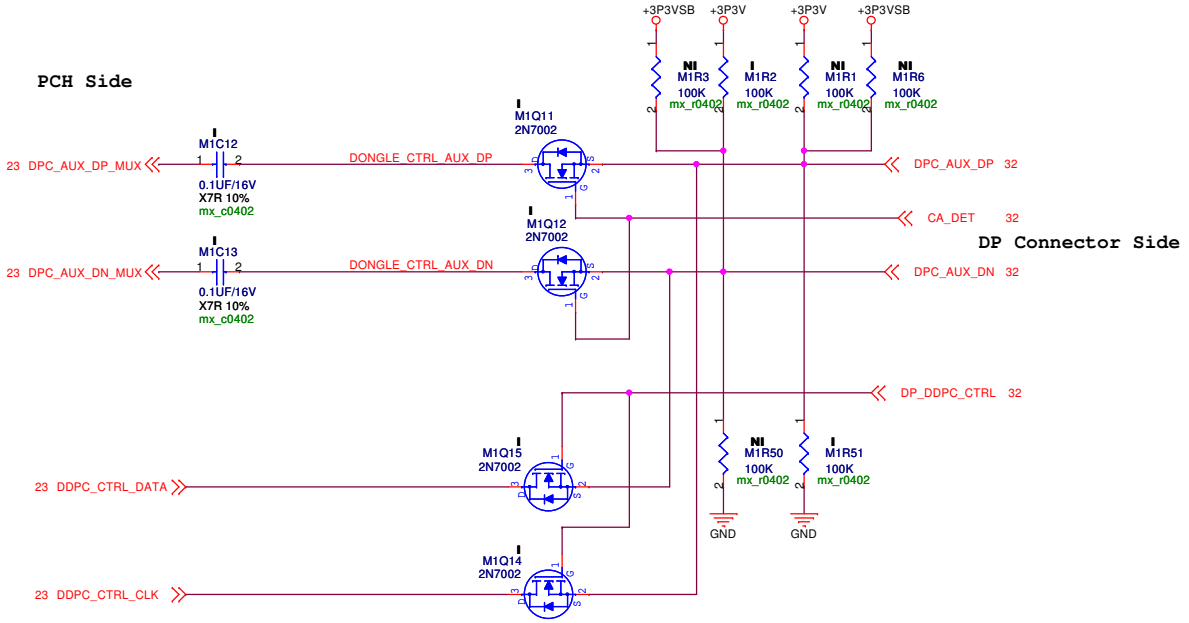
PEGATRON Title : DP CONNECTOR

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

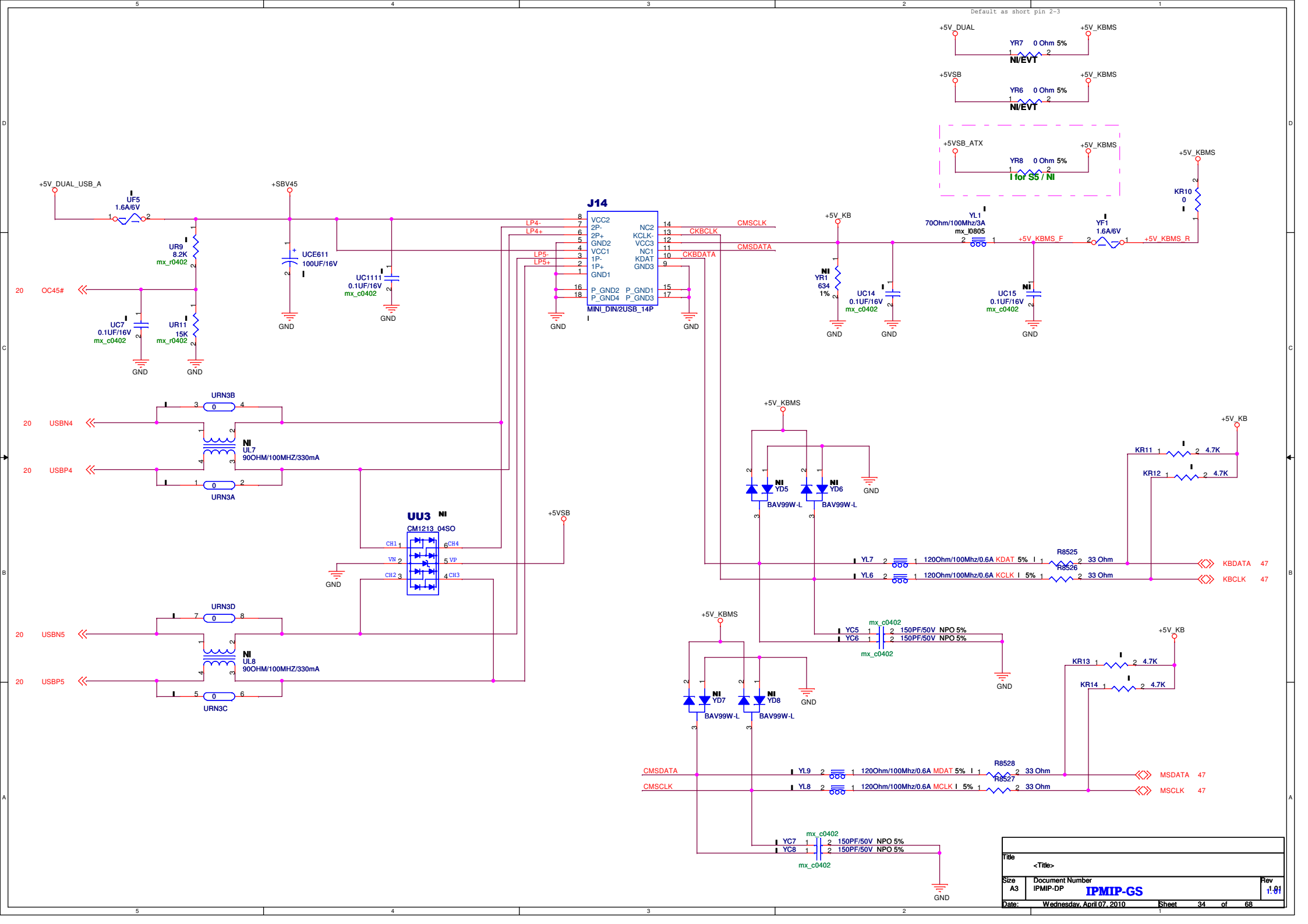
Date: Wednesday, April 07, 2010 Sheet 32 of 68

Display Port to HDMI/DVI Dongle control

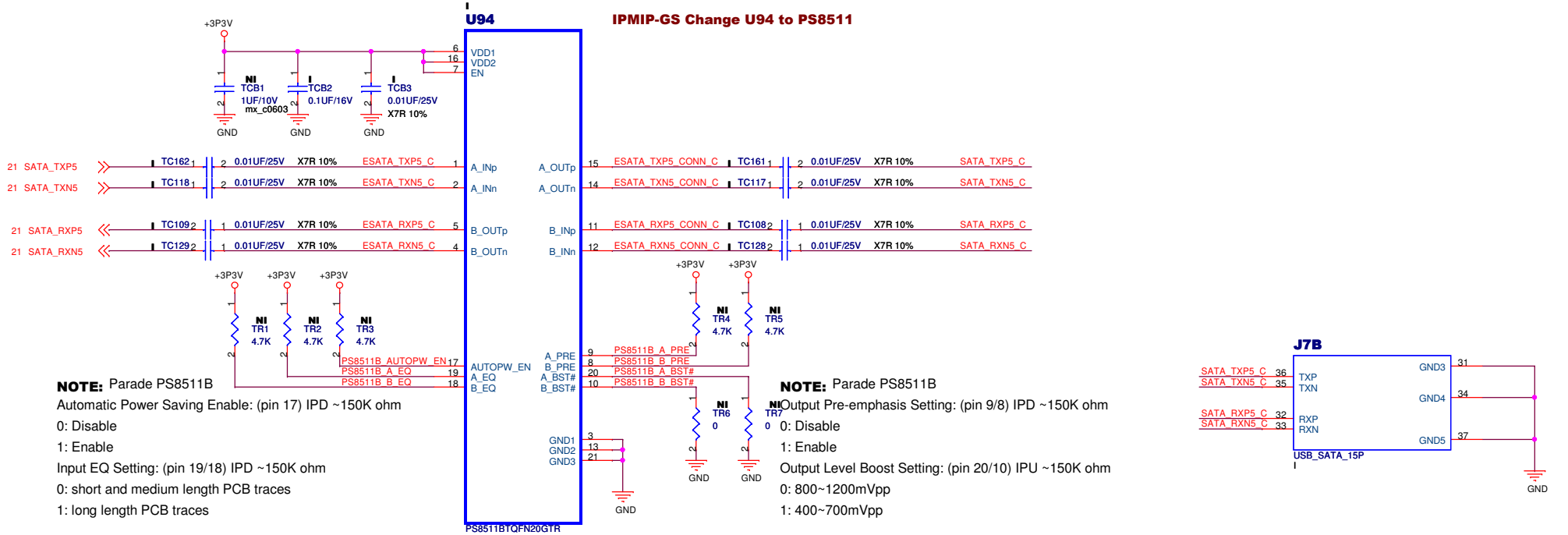


PEGATRON DT-MB RESTRICTED SECRET

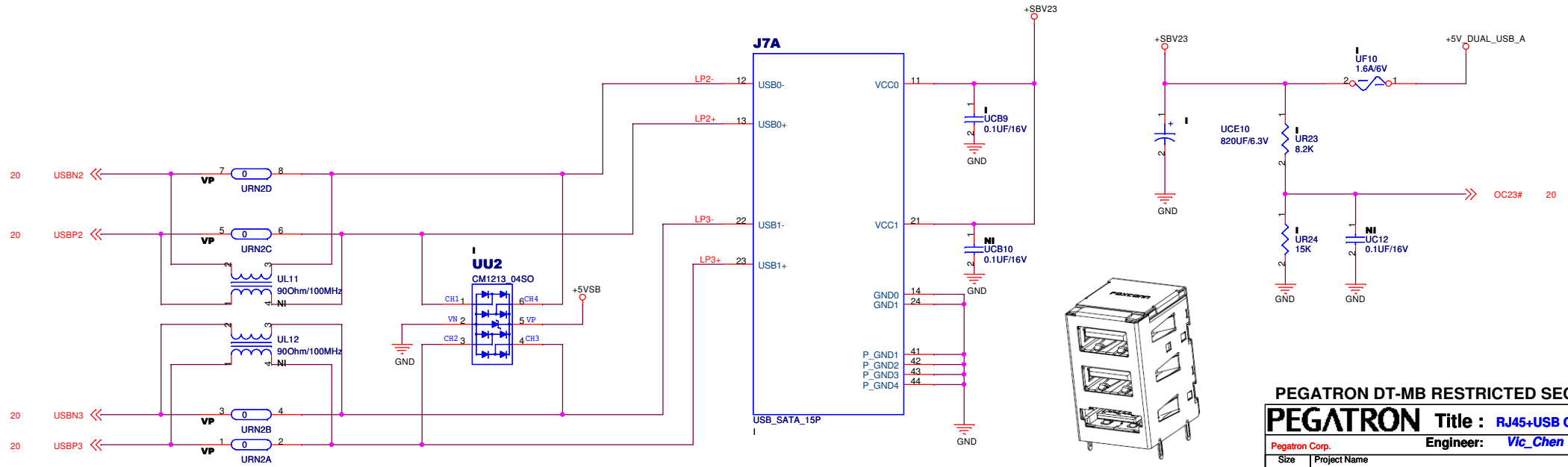
PEGATRON	Title : DP DONGLE	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-GS	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 33 of 68	



Title	<Title>	
Size A3	Document Number IPMIP-DP	Rev 1.01
Date: Wednesday, April 07, 2010	Sheet 34 of 68	IPMIP-GS



E-SATA + Dual USB CONNECTOR



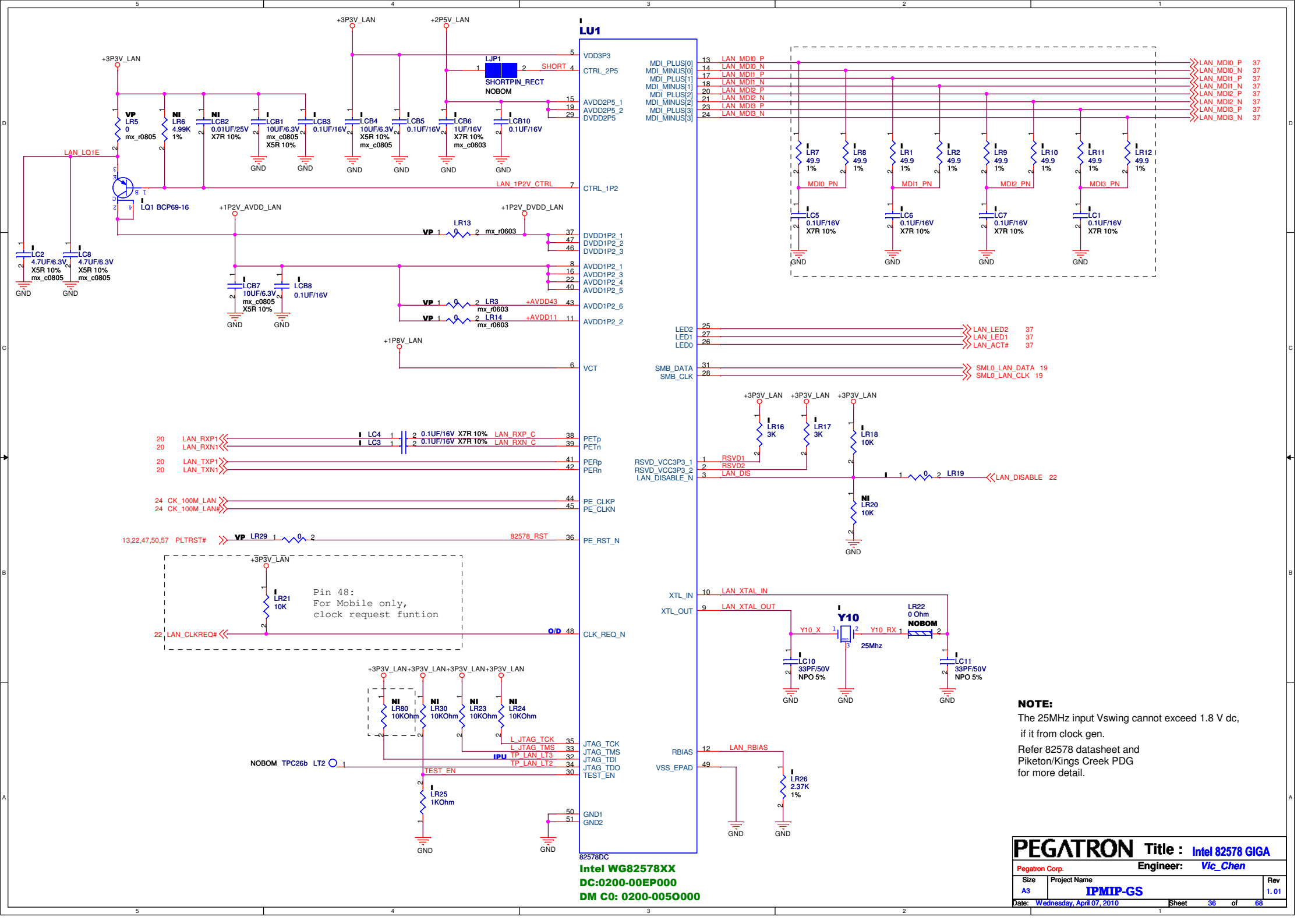
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : RJ45+USB CONN.2

Pegatron Corp. Engineer: Vic_Chen

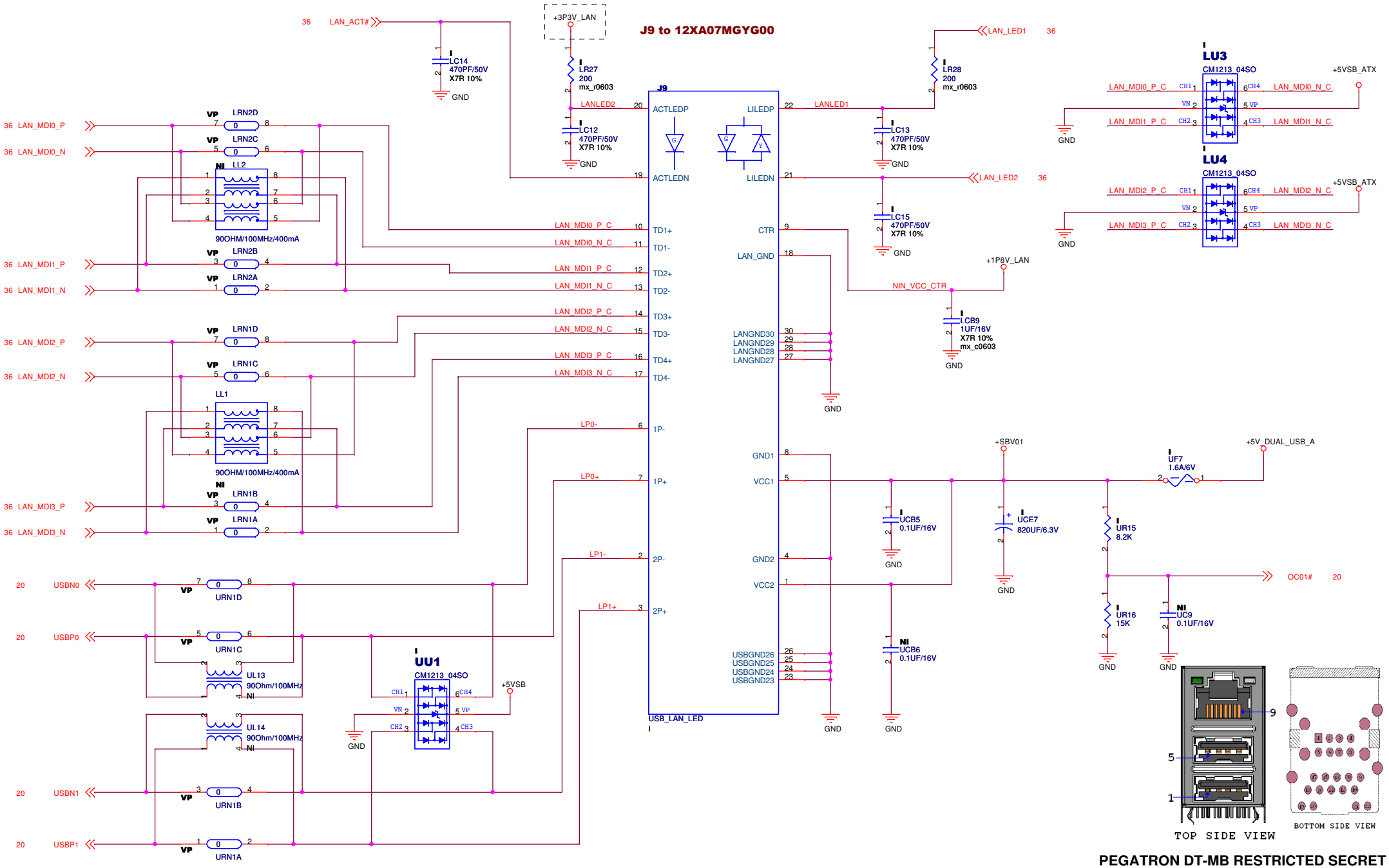
Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 35 of 68


LU1
82578DC
Intel WG82578XX
DC:0200-00EP000
DM C0: 0200-005O000
Pin 48:
For Mobile only,
clock request funtion
NOTE:
The 25MHz input Vswing cannot exceed 1.8 V dc,
if it from clock gen.
Refer 82578 datasheet and
Piketon/Kings Creek PDG
for more detail.
PEGATRON
Title : Intel 82578 GIGA
Pegatron Corp.
Engineer: Vic_Chen
Size A3
Project Name IPMIP-GS
Rev 1.01
Date: Wednesday, April 07, 2010
Sheet 36 of 68

Change +3p3V to +3P3V_LAN

J9 to 12XA07MGYG00



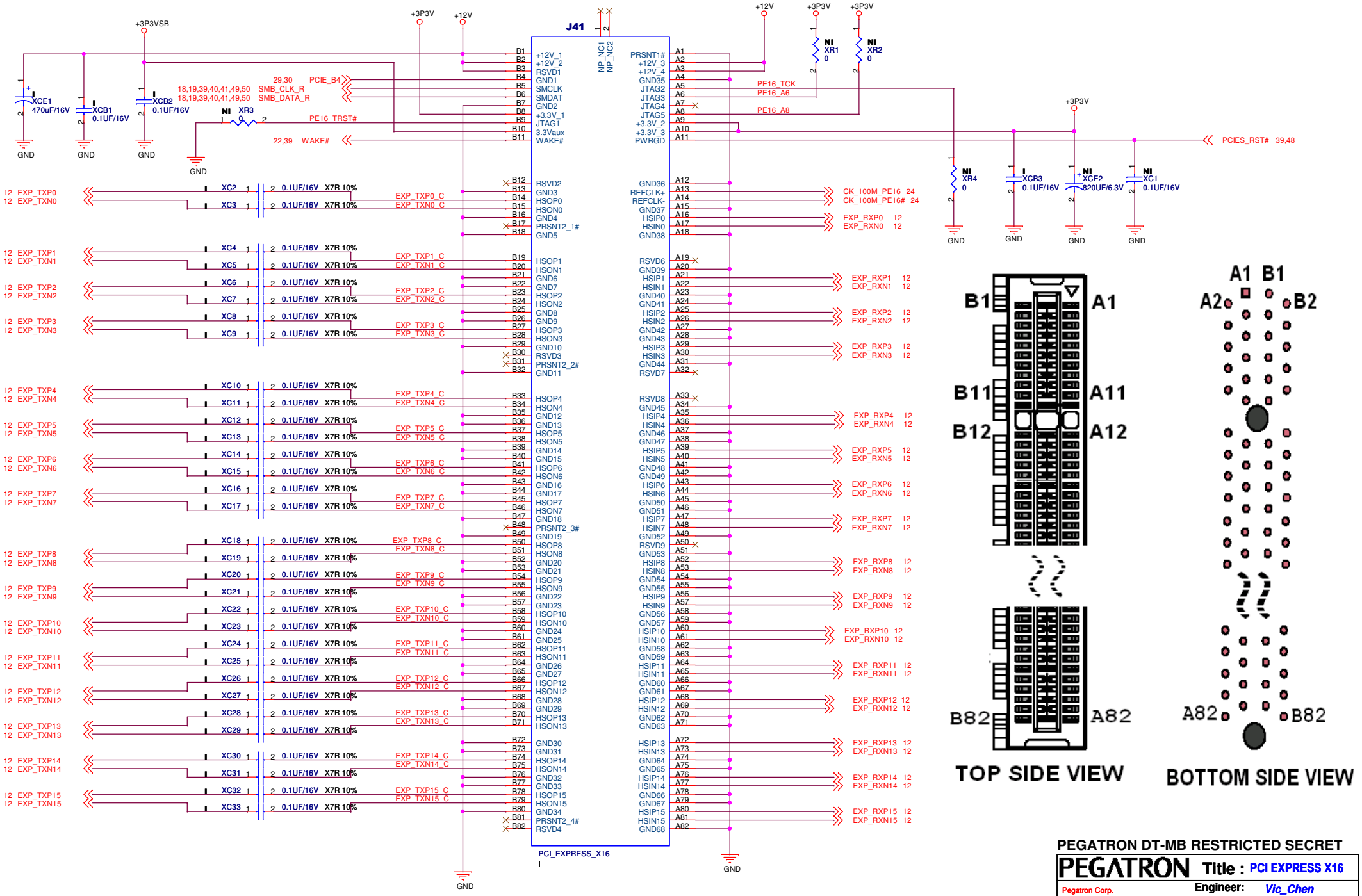
TOP SIDE VIEW

BOTTOM SIDE VIEW

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title :	RJ45+USB CONN.1
Pegatron Corp.	Engineer:	Vic_Chen
Size: A3	Project Name: IPMIP-GS	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 37 of 68	

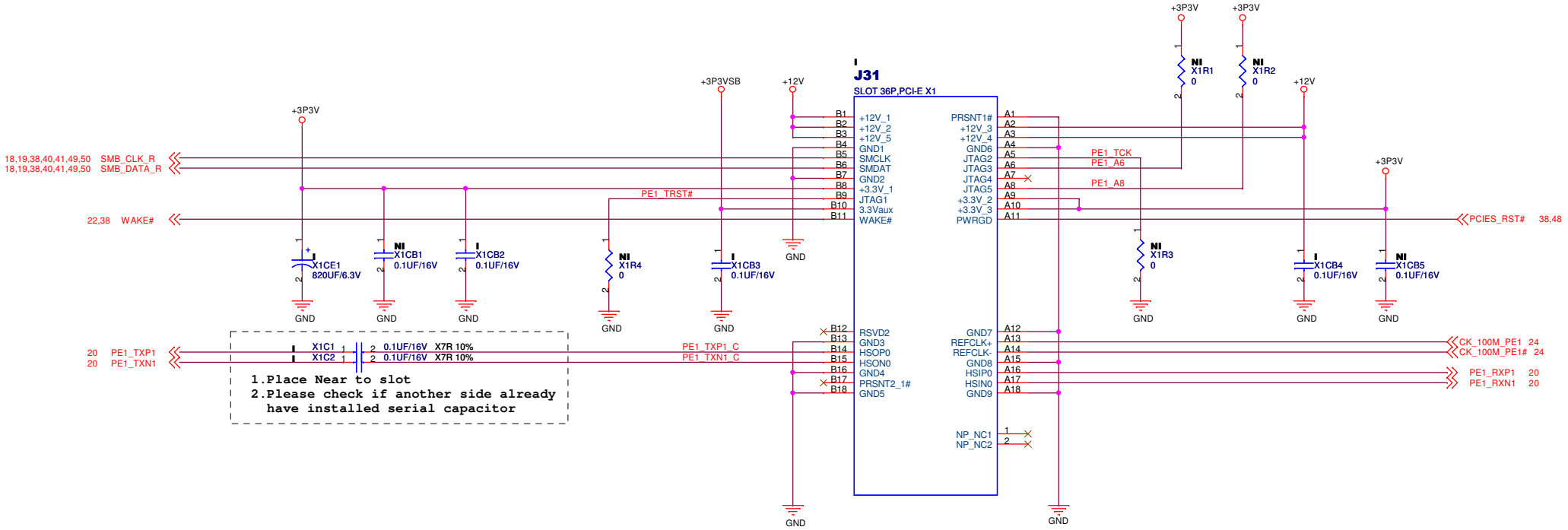
PCI EXPRESS X16 Graphics Card Slot

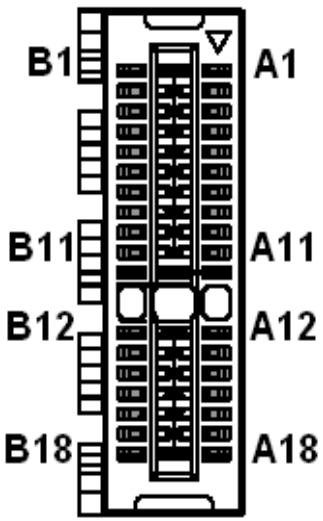


PEGATRON DT-MB RESTRICTED SECRET

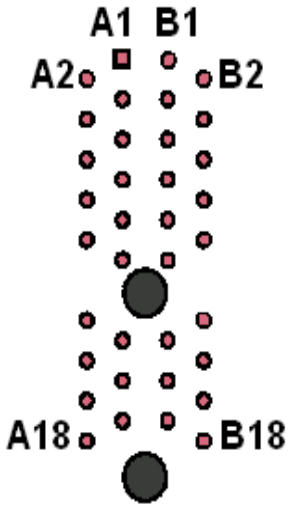
PEGATRON	Title : PCI EXPRESS X16	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-GS	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 38 of 68	

PCI Express x1 SLOT





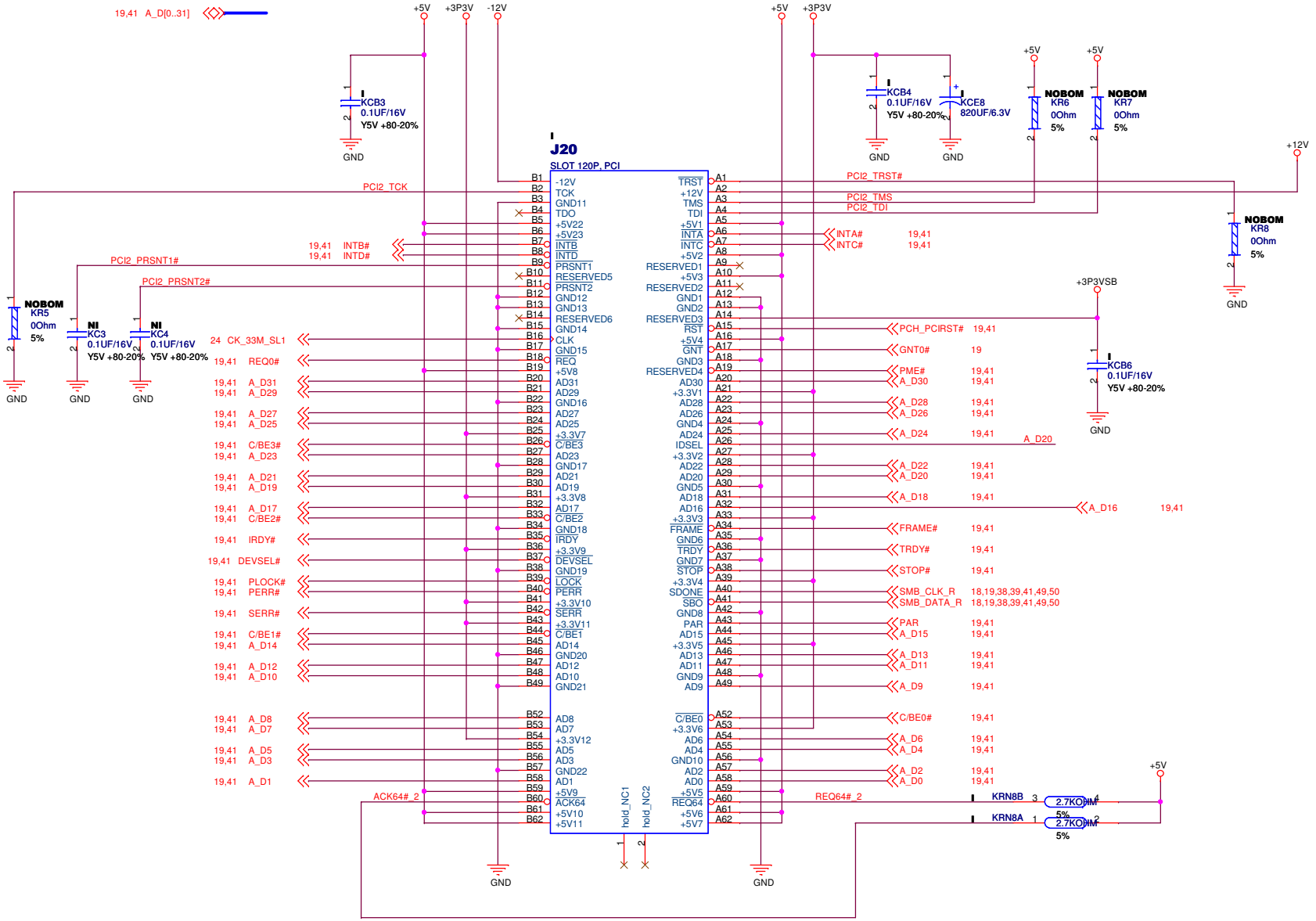
TOP SIDE VIEW



BOTTOM SIDE VIEW

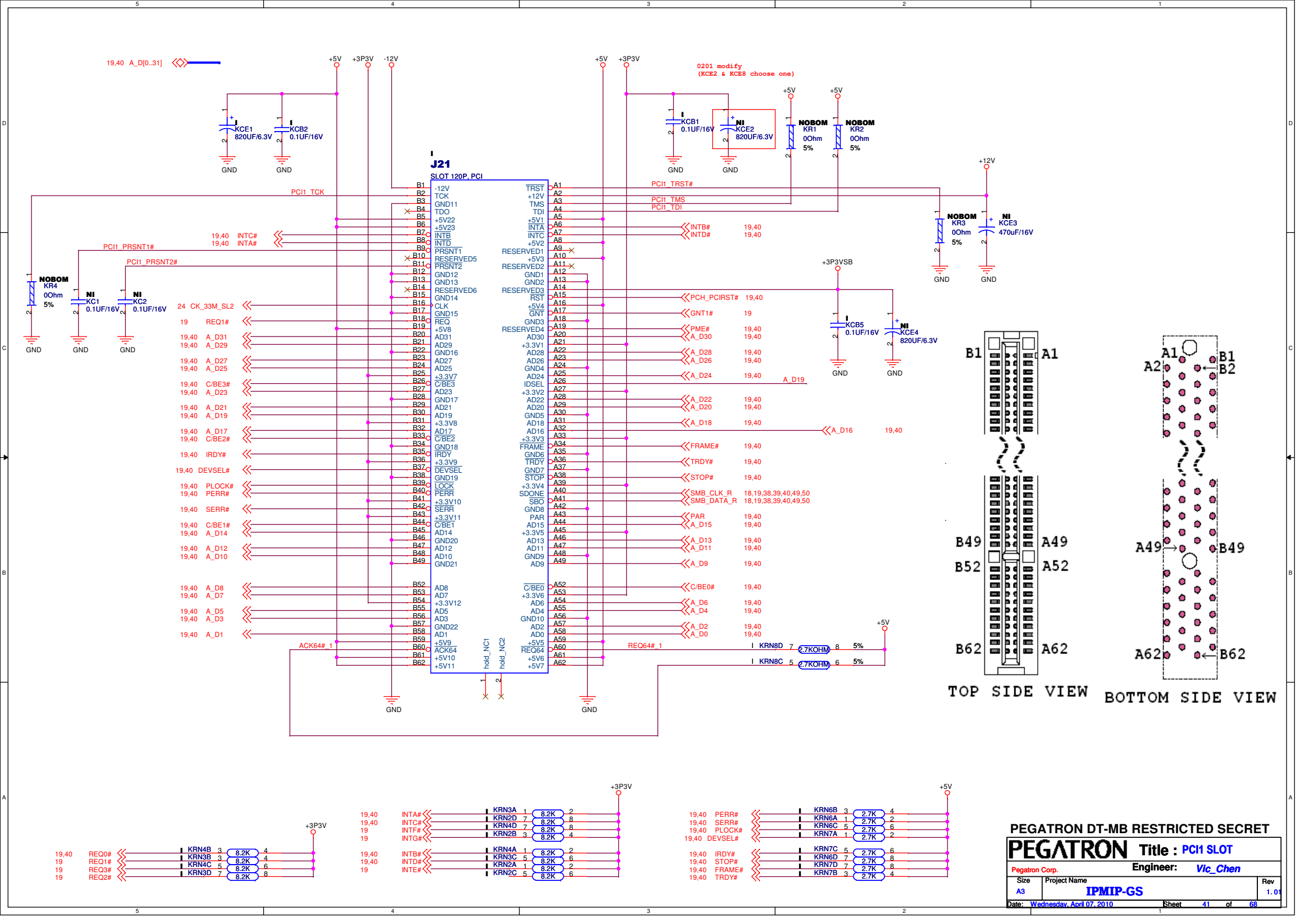
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : PCI EXPRESS X1	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-GS	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 39 of 68	



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : PCI EXPRESS X4	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-GS	Rev: 1. 01
Date: Wednesday, April 07, 2010	Sheet 40 of 68	


J21
SLOT 120P, PCI
0201 modify
(KCE2 & KCE8 choose one)
TOP SIDE VIEW
BOTTOM SIDE VIEW
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : PCI1 SLOT
Pegatron Corp.
Engineer: Vic_Chen
Size A3
Project Name IPMIP-GS
Rev 1.01
Date: Wednesday, April 07, 2010
Sheet 41 of 68

Note : (AD48)

For some power supply , +5VSB drop before +12V when AC power out (S0 --> G3) , +12V will current back to +5VSB If your power supply has this sequence issue , please install AD48 instead of AQ1

Please noite: AZ_BITCLK need add a serial res(22 ohm) near SB side

Digital Region

Provision AR23 for ALC888S-VC codec

PLACE NEAR front audio CODEC FOR EMI

ALC888S Rev. A

ALC888S_GR

ALC662 02X611003200

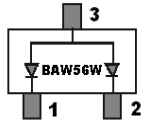
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : AUDIO CODEC

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1. 01

Date: Wednesday, April 07, 2010 Sheet 42 of 68



TOP SIDE VIEW

NI
AC30
100PF/50V
NPO 5%
AR78
0
AGND
GND

PLACE NEAR front audio header FOR EMI

J100
HEADER_1X4P_K2
+5V
AC38
0.1UF/16V
AR52
200
NI
AC42
100PF/50V
NPO 5%
GND
SPDIF_O1_L
AL8
120Ohm/100Mhz/0.6A
SPDIF_OUT1
AR77
0 mx_r0603
SPDIF_OUT1 42

But for other customers (ex, Intel, EPSON, FSC, Dell.....etc), they might don't need 6+3 configuration, just general 6+2 type. If so, please change LINE1 (Pin 23/24) to Rear Line-In port instead of CD-IN, because CD-IN (Pin 18/19/20) port is only dedicated input port and can't retasking

Front Audio Header

42 MIC2_VREF
AD4
BAW56WPT
MIC2_VREF_R
MIC2_VREF_L
5%
4.7KOHM
ARN15A
ARN15B

42 LIN2_VREF
AD5
BAW56WPT
LIN2_VREF_R
LIN2_VREF_L
5%
4.7KOHM
ARN15C
ARN15D

42 MIC2_L_C
42 MIC2_R_C
42 LIN2_R_C
42 LIN2_L_C
AL4 120Ohm/100Mhz/0.6A
AL3 120Ohm/100Mhz/0.6A
AR80 0 mx_r0603
AR81 0 mx_r0603

AR47 22KOHM 5% NI
AR48 22KOHM 5% NI
AR49 22KOHM 5% NI
AR50 22KOHM 5% NI
AGND

AC28 100PF/50V NPO 5%
AC29 100PF/50V NPO 5%
AC31 100PF/50V NPO 5%
AC43 100PF/50V NPO 5%

Color = Green
P23
HEADER_2X5P_K8
MIC2_L
MIC2_R
LIN2_R
LIN2_L
MIC2_RTU
LIN2_RTU

AR53
42,44 SENSE_B
47 Ohm 5%
AC32 100PF/50V NPO 5% NI

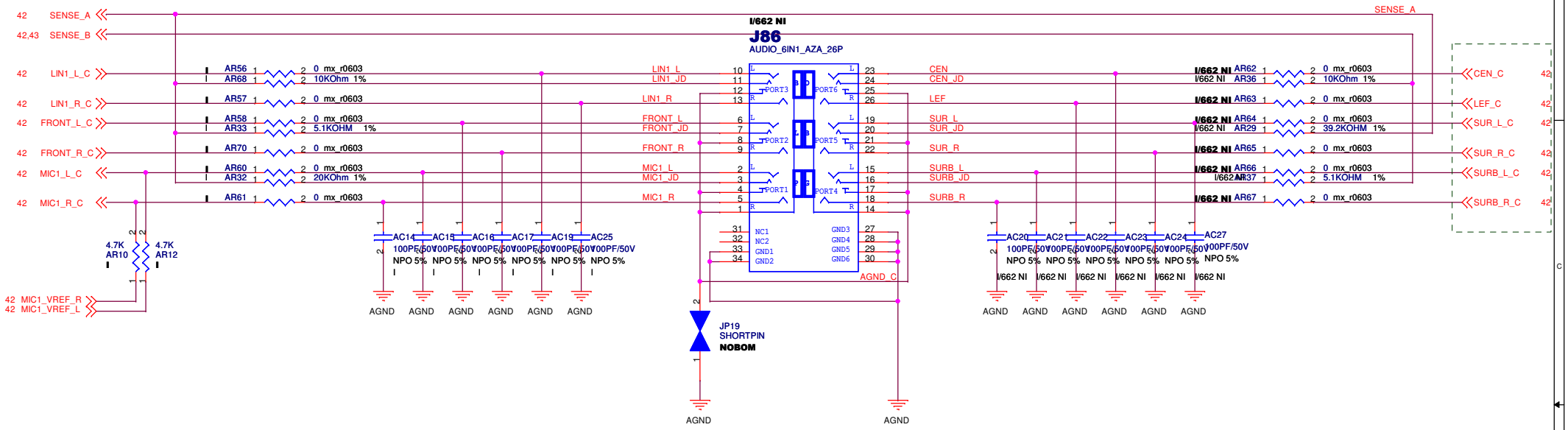
AR39 39.2KOHM 1%
AR51 20KOhm 1%

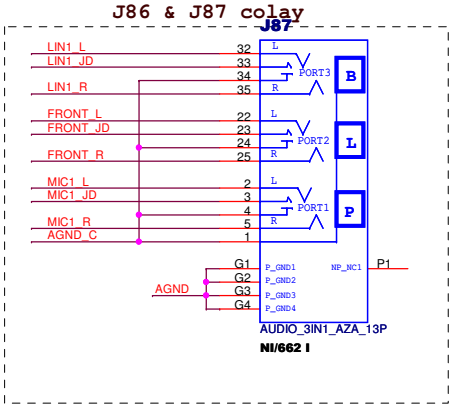
+3P3V
AR38 4.7KOHM 5%
ACB10 0.1UF/16V Y5V +80-20% NI
F_AUDIO_DET# 22

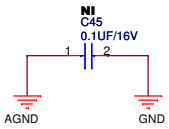
PEGATRON Title : FORNT AUDIO CONN.
Pegatron Corp. Engineer: Vic_Chen
Size A3 | Project Name IPMIP-GS | Rev 1. 01
Date: Wednesday, April 07, 2010 | Sheet 43 of 68

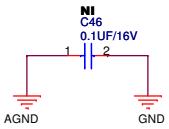
Azalia Rear Audio Connector

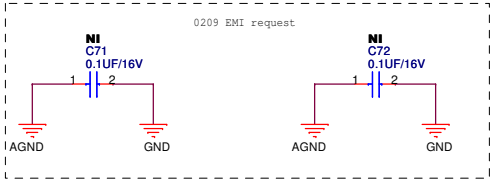
IPMIP-GS R1.01 Change port











PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : REAR AUDIO CONN.

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 44 of 68

NOTE:
Check USB cable internal whether had capacity
NI:BPC
I: CPC

+SBV89
UCB7 0.1UF/16V
UCE8 470uF/6.3V
UF8 1.6A/6V
+5V_DUAL_USB_B
UR17 8.2K
UR19 15K
NI UC10 0.1UF/16V
OC89# 20

P151 HEADER_2X5P_K9
LP8- LP8 LP9- LP9+

20 USBN8 URN5B
20 USBP8 URN5A
20 USBN9 URN5D
20 USBP9 URN5C
VP 0
NI 90Ohm/100MHz UL3
NI 90Ohm/100MHz UL4

UU5 CM1213_04SO
CH1 VN CH2 CH4 VP CH3
+5VSB

SRV05 4
TOP SIDE VIEW

NOTE:
Check USB cable internal whether had capacity
NI: BPC
I: CPC

+SBV1011
UCB8 0.1UF/16V
UCE9 470uF/6.3V
UF9 1.6A/6V
+5V_DUAL_USB_B
UR20 8.2K
UR22 15K
NI UC11 0.1UF/16V
OC1011# 20

P152 HEADER_2X5P_K9
LP10- LP10+ LP11- LP11+

20 USBN10 URN6B
20 USBP10 URN6A
20 USBN11 URN6D
20 USBP11 URN6C
VP 0
NI 90Ohm/100MHz UL5
NI 90Ohm/100MHz UL6

UU6 CM1213_04SO
CH1 VN CH2 CH4 VP CH3
+5VSB

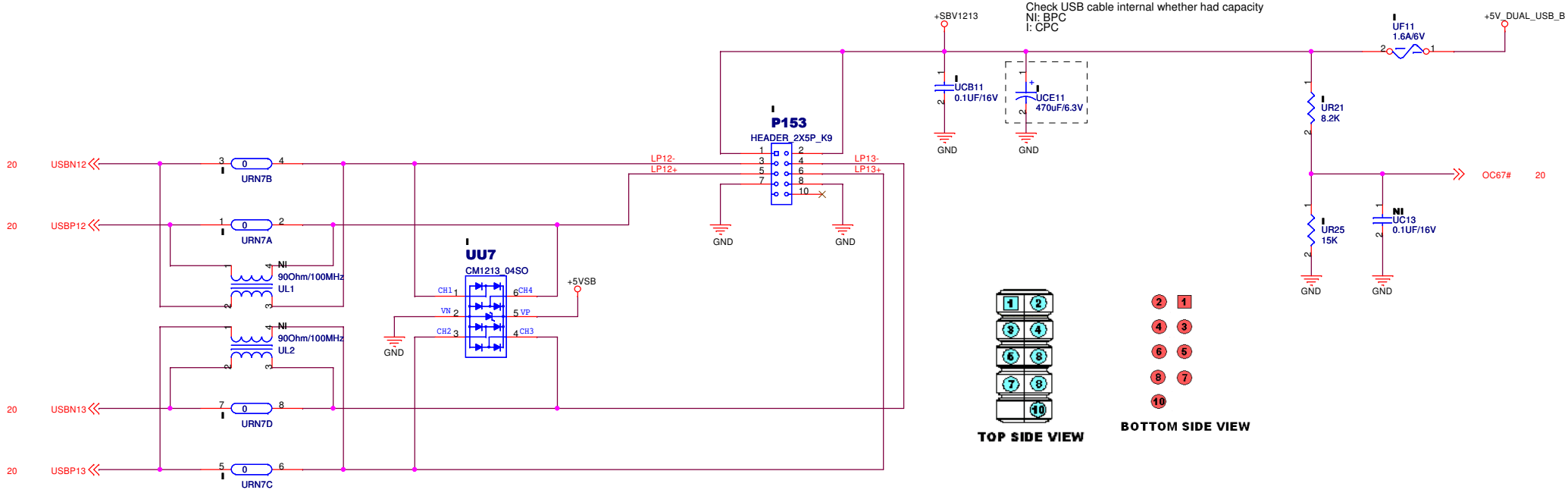
TOP SIDE VIEW

BOTTOM SIDE VIEW

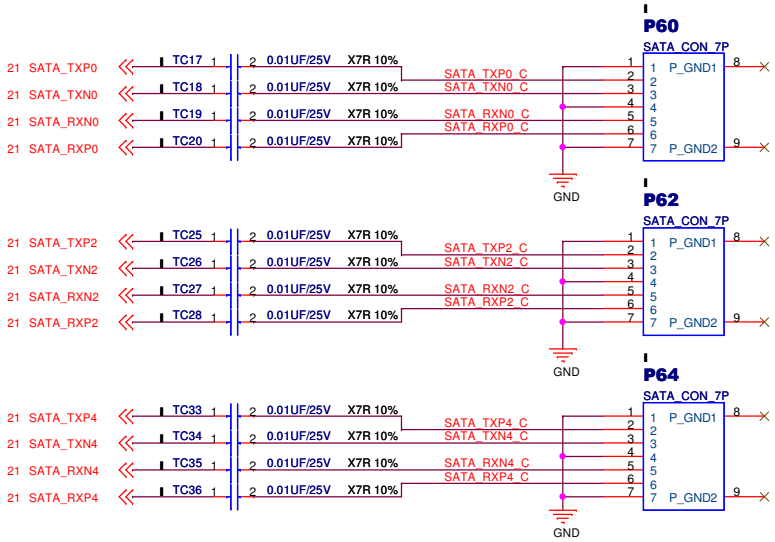
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : USB HEADER CON.	
Pegatron Corp.	Engineer: Vic_Chen	
Size A3	Project Name IPMIP-GS	Rev 1.01
Date: Wednesday, April 07, 2010	Sheet 45 of 68	

NOTE:
Check USB cable internal whether had capacity
NI: BPC
I: CPC



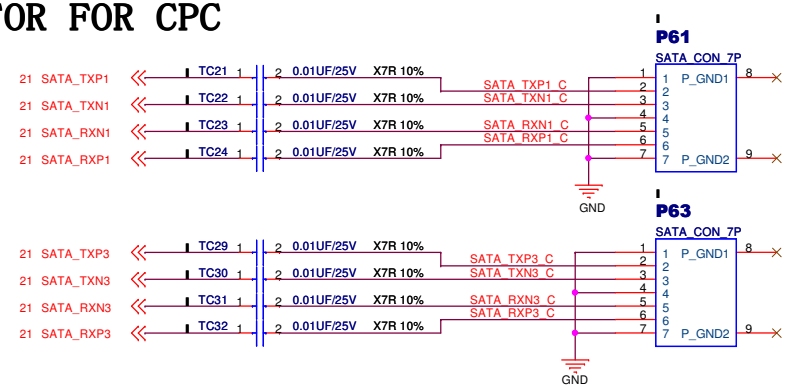
SATA CONNECTOR FOR CPC



SATA CONTROLLER #1
(PRIMARY MASTER)
COLOR = RED

SATA CONTROLLER #1
(PRIMARY MASTER)
COLOR = RED

SATA CONTROLLER #2
(PRIMARY MASTER)
COLOR = RED

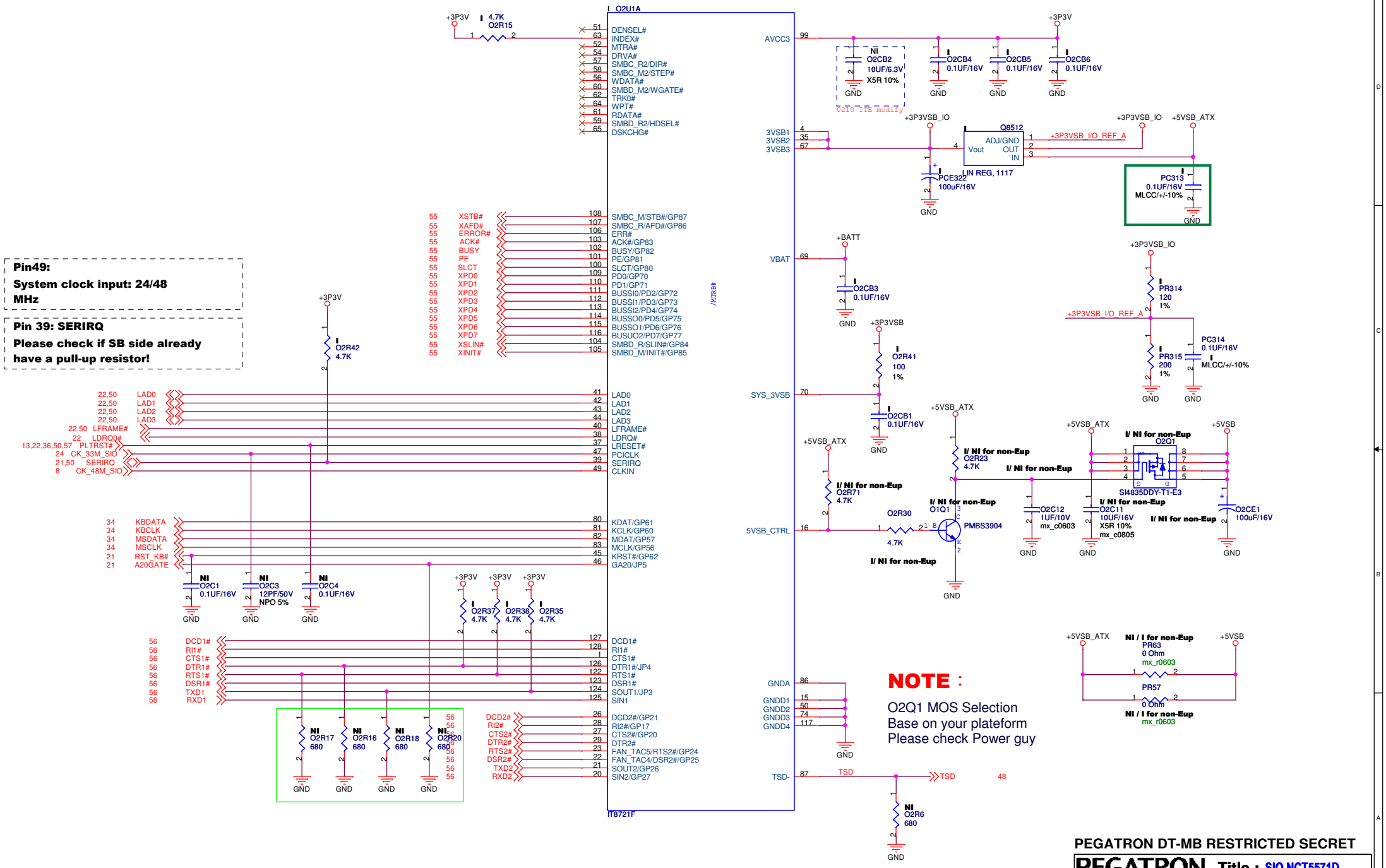


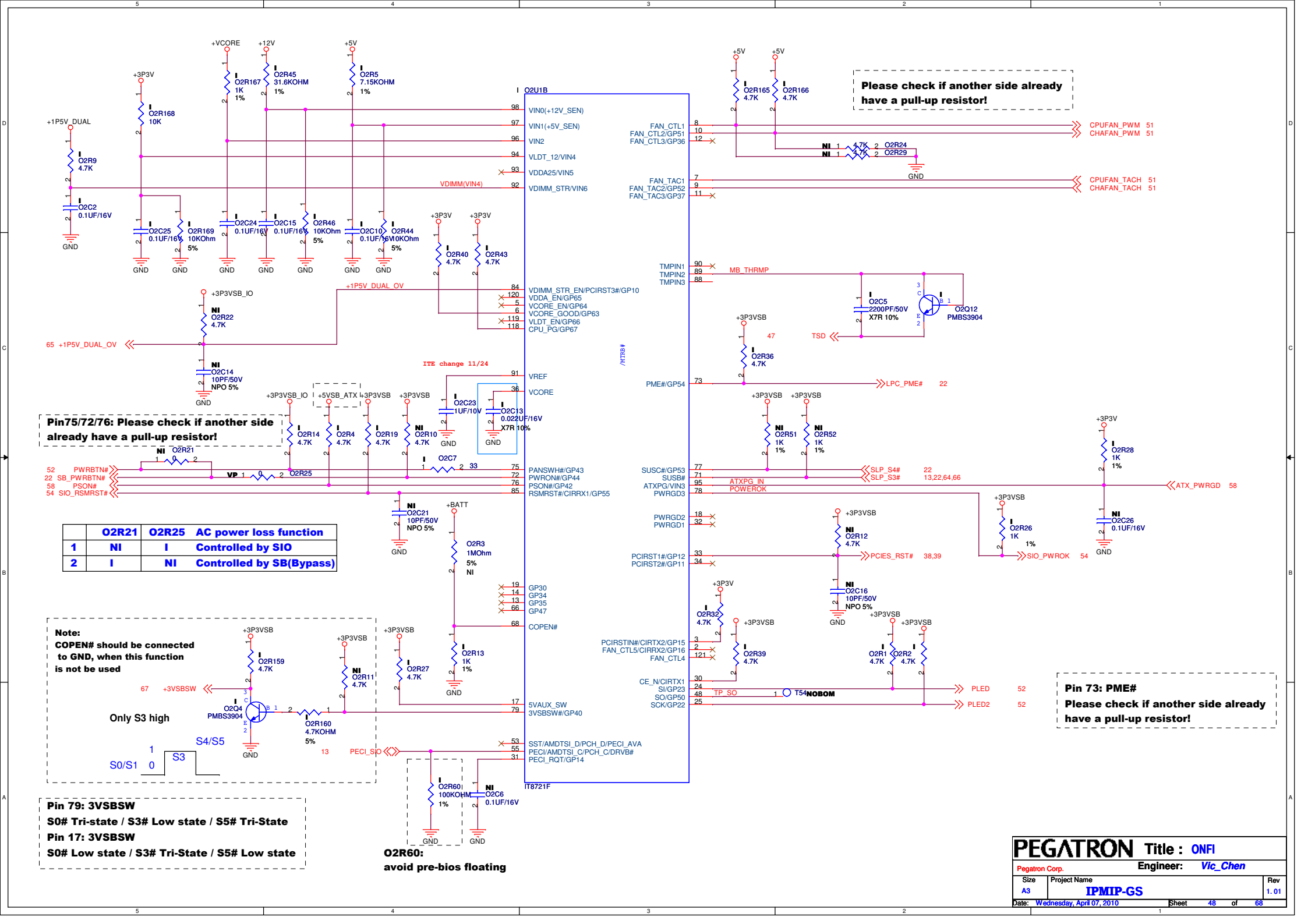
SATA CONTROLLER #1
(SECONDARY MASTER)
COLOR = RED

SATA CONTROLLER #1
(SECONDARY MASTER)
COLOR = RED

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : USB HEADER CON.	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-GS	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 46 of 68	


O2U1A
IT8721F
Pin49:
System clock input: 24/48 MHz
Pin 39: SERIRQ
Please check if SB side already have a pull-up resistor!
NOTE :
O2Q1 MOS Selection
Base on your plateform
Please check Power guy
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : SIO NCT5571D
Pegatron Corp. Engineer: Vic_Chen
Size A3
Project Name IPMIP-GS
Rev 1.01
Date: Wednesday, April 07, 2010
Sheet 47 of 68



	O2R21	O2R25	AC power loss function
1	NI	I	Controlled by SIO
2	I	NI	Controlled by SB(Bypass)

SM BUS Control

To PCH, PCI, and PCIE Slot

18,19,38,39,40,41,50 SMB_DATA_R

18,19,38,39,40,41,50 SMB_CLK_R

To Clock Gen, DIMMs, and ITP Debug Port

SMB_DATA_M 8,16,17,57

SMB_CLK_M 8,16,17,57

+3P3V

VP R14 0

NI R18 2.7K

NI R19 2.7K

NI Q7 2N7002

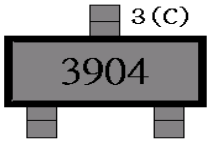
VP R39 0

NI Q14 2N7002

+12V

NI R15 8.2K

PWROK_R_Q



TOP SIDE VIEW

SPI BIOS ROM - 64Mbit

19 SPI_CS#

19 SPI_MISO

19 SPI_MOSI

19 SPI_CLK

E16 HEADER_2X4P_K4

NI F3R1 0

GND

+3P3V_ME

F3R5 8.2K

U14 SOCKET_8P NI

SPI_CS# E16

SPI_MISO

FWH_WP#

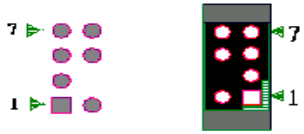
SPI_HOLD#

F3R6 8.2K

F3CB1 0.1UF/16V

JE16:12

MINI_JUMPER



BOTTOM SIDE VIEW

TOP SIDE VIEW

IPMIP-GS Change SPI 64Mb

64Mb: 05X00Z2GE330

U96 W25Q64BVSSIG

SPI_CS# E16

SPI_MISO

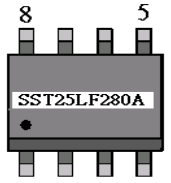
FWH_WP#

SPI_HOLD#

SPI_CLK

SPI_MOSI

GND



TOP SIDE VIEW

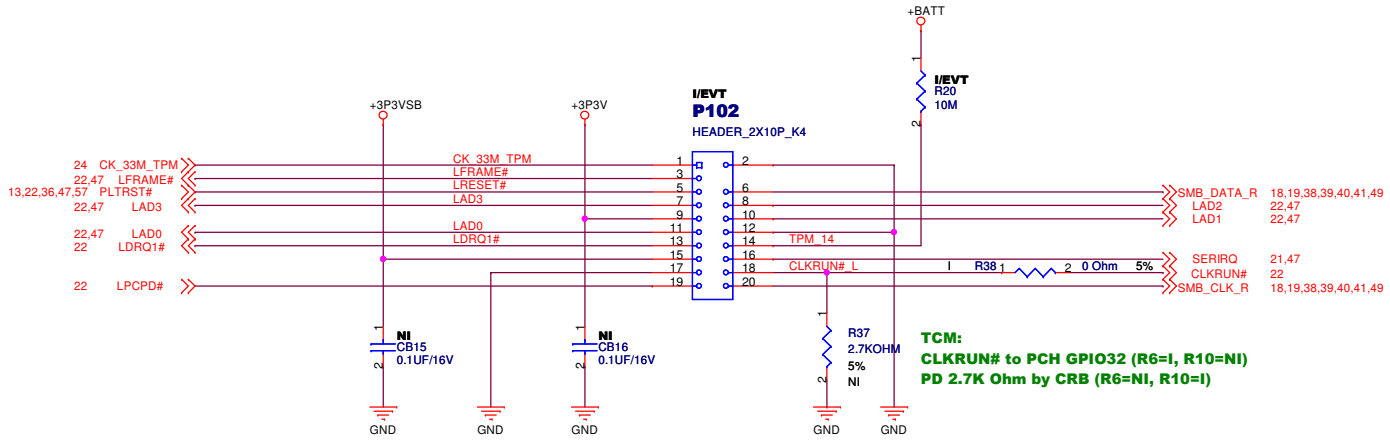
PEGATRON DT-MB RESTRICTED SECRET

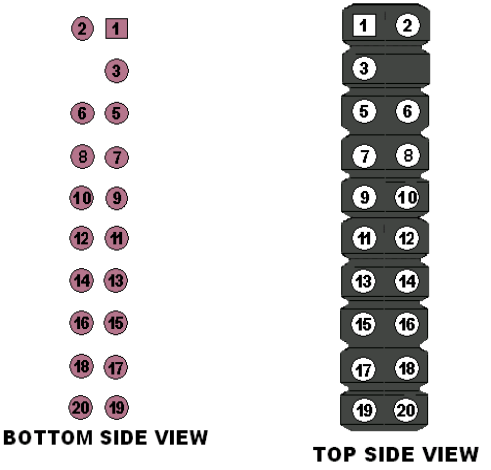
PEGATRON Title : SPI FLASH - 8M

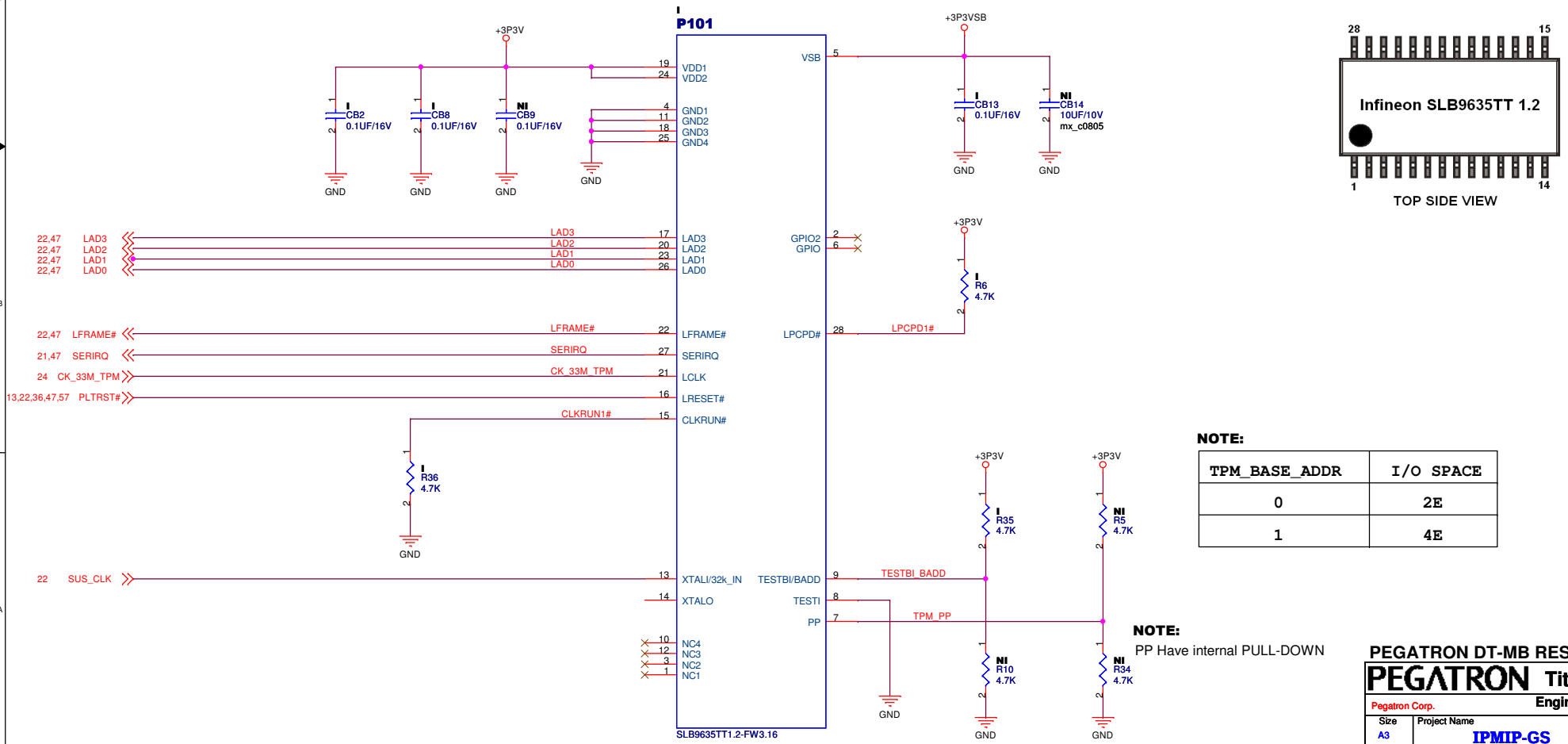
Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 49 of 68







NOTE:

TPM_BASE_ADDR	I/O SPACE
0	2E
1	4E

NOTE:
PP Have internal PULL-DOWN

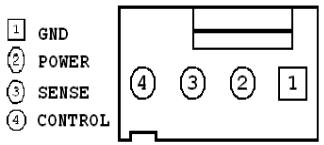
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SATA2 & TPM/TCM

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

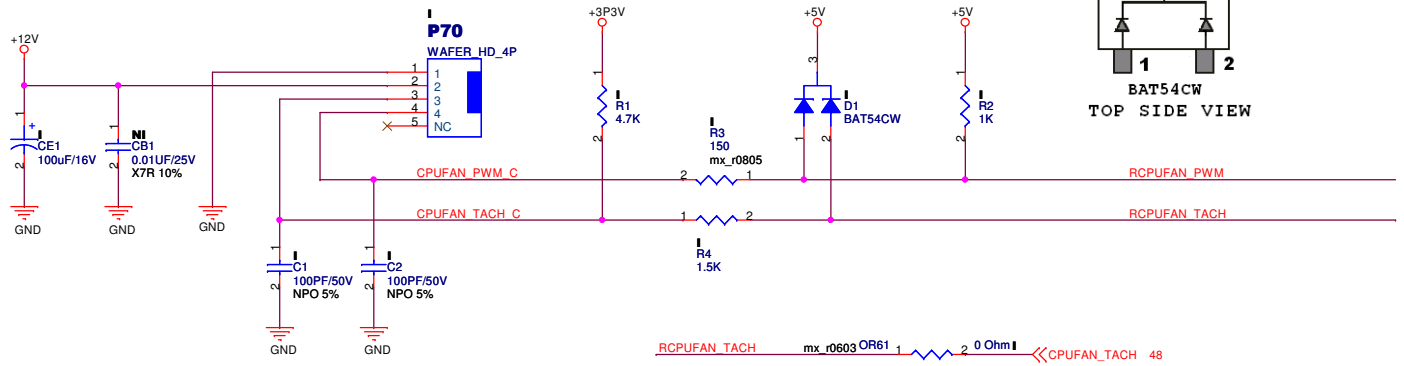
Date: Wednesday, April 07, 2010 Sheet 50 of 68



TOP SIDE VIEW

BOTTOM SIDE VIEW

CPU FAN
COLOR: WHITE
W/POST

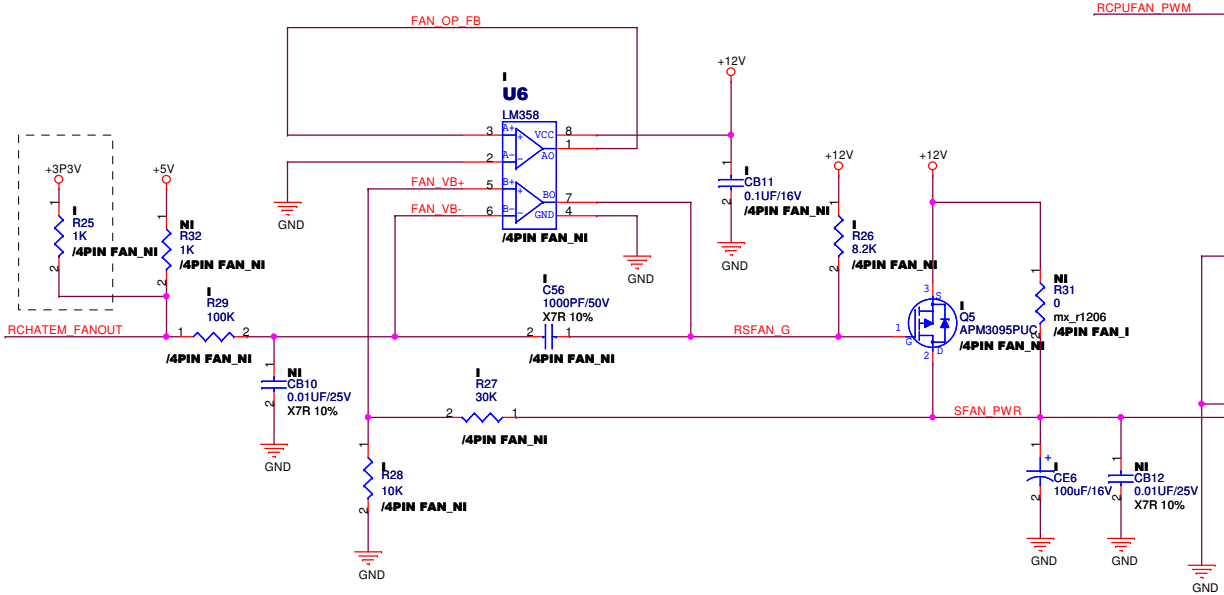


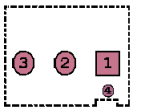
BAT54CW
TOP SIDE VIEW

RCPUFAN_TACH mx_r0603 OR61 0 Ohm CPUFAN_TACH 48

RCPUFAN_PWM mx_r0603 OR64 /SFSC 0 Ohm CPUFAN_PWM 48

3 & 4 PIN CO-LAYOUT Circuit (Default 3 pin fan)

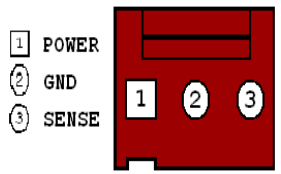




BOTTOM SIDE VIEW

RCHAFANIN OR52 0 Ohm mx_r0603 /NB_FAN/AFSC CHAFAN_TACH 48

RCHATEM_FANOUT OR56 0 Ohm mx_r0603 /NB_FAN/AFSC CHAFAN_PWM 48

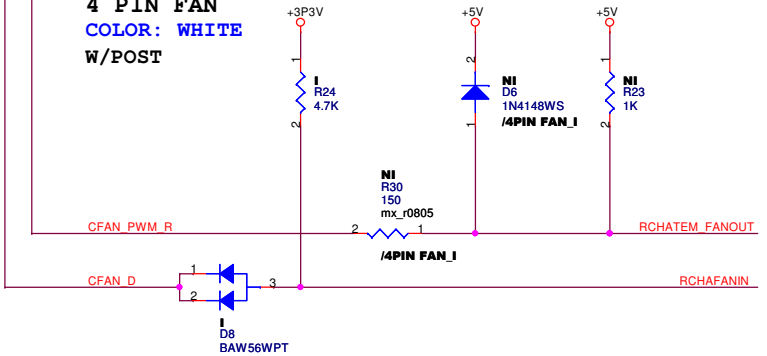


TOP SIDE VIEW

3 PIN FAN
COLOR: RED
W/POST

3 PIN FAN
COLOR: RED
W/POST

4 PIN FAN
COLOR: WHITE
W/POST

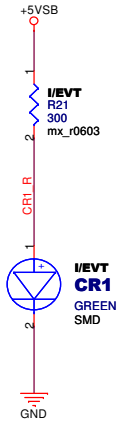


R1.03G

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : 4-PIN FAN CONN	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-GS	Rev: 1.01
Date: Thursday, April 08, 2010	Sheet 51 of 68	

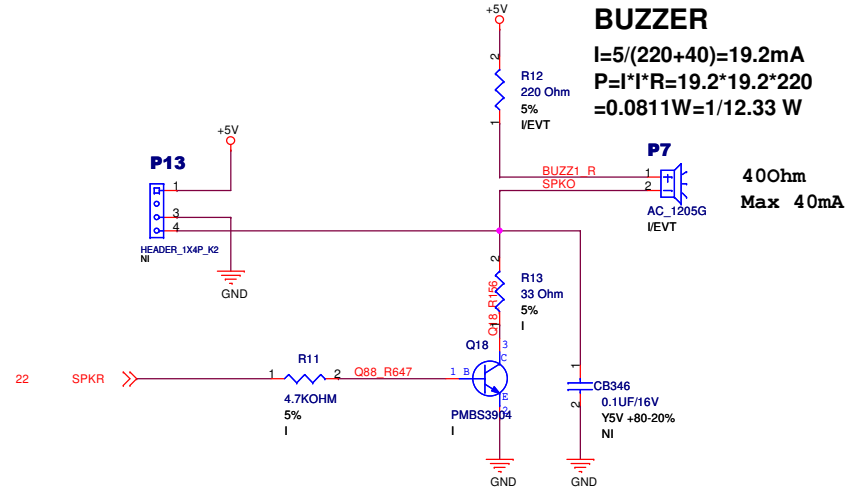
+5VSB : GREEN



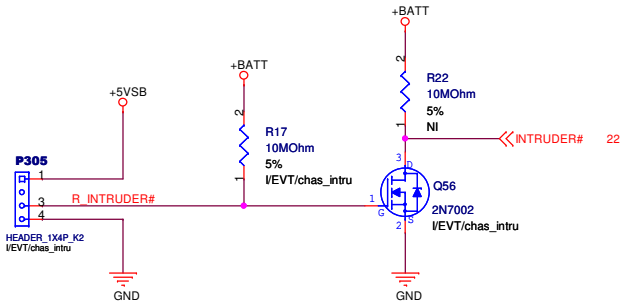
BUZZER

I=5/(220+40)=19.2mA
P=I*I*R=19.2*19.2*220
=0.0811W=1/12.33 W

40Ohm
Max 40mA



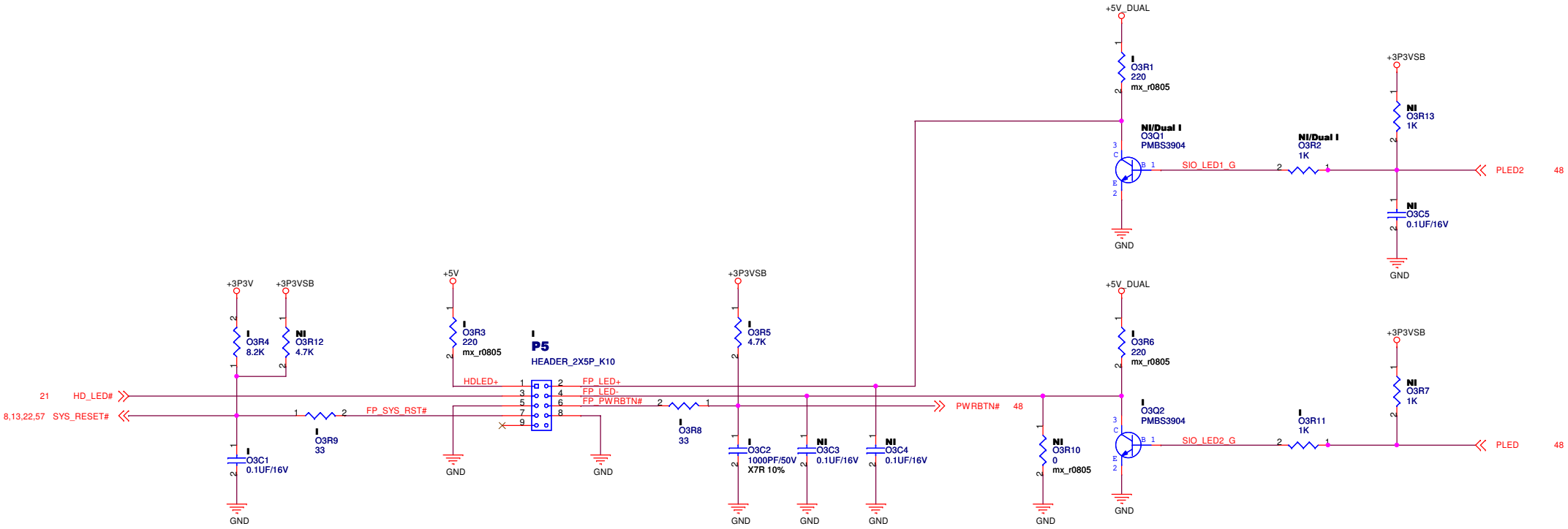
INTRUDER



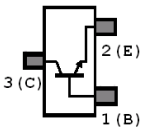
JP305:34

MINI_JUMPER
I/EVT

HPD CONTROL PANEL / LED CIRCUITRY



FRONT POWER LED COLOR SUPPORT	O3Q1	O3R2			
SINGLE COLOR	NI	NI			
DUAL COLOR	I	I			



PMBS3904
TOP SIDE VIEW

PEGATRON DT-MB RESTRICTED SECRET

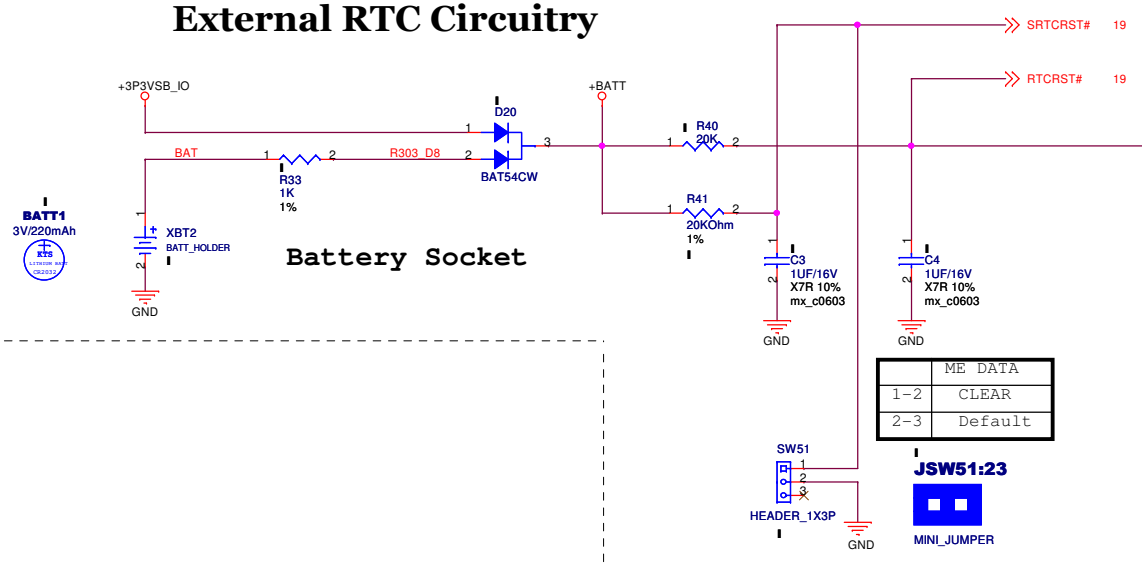
PEGATRON Title : FRONT PANEL

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.01

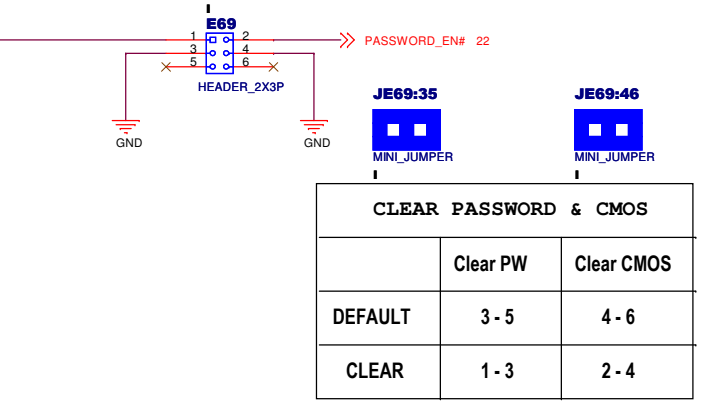
Date: Wednesday, April 07, 2010 Sheet 52 of 68

External RTC Circuitry

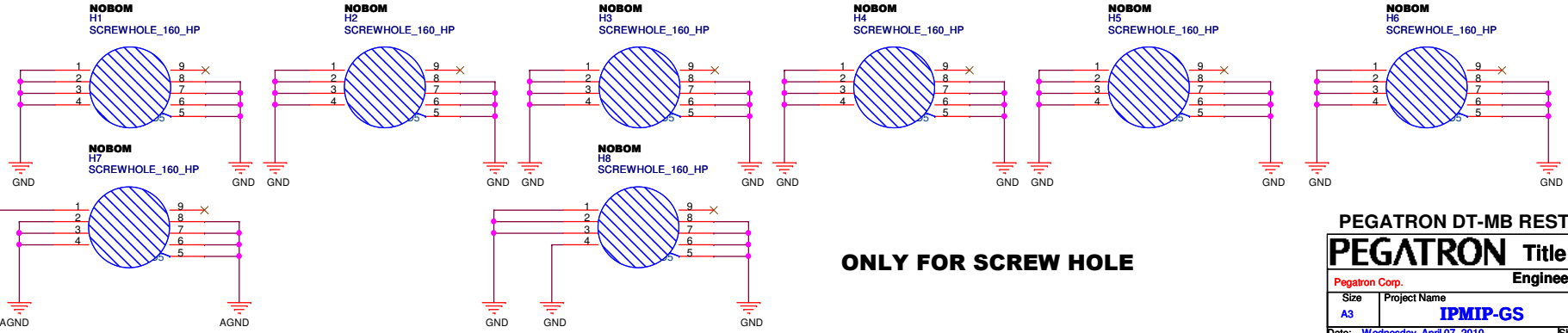


	ME DATA
1-2	CLEAR
2-3	Default

CLEAR CMOS & PASSWORD



CLEAR PASSWORD & CMOS		
	Clear PW	Clear CMOS
DEFAULT	3 - 5	4 - 6
CLEAR	1 - 3	2 - 4



ONLY FOR SCREW HOLE

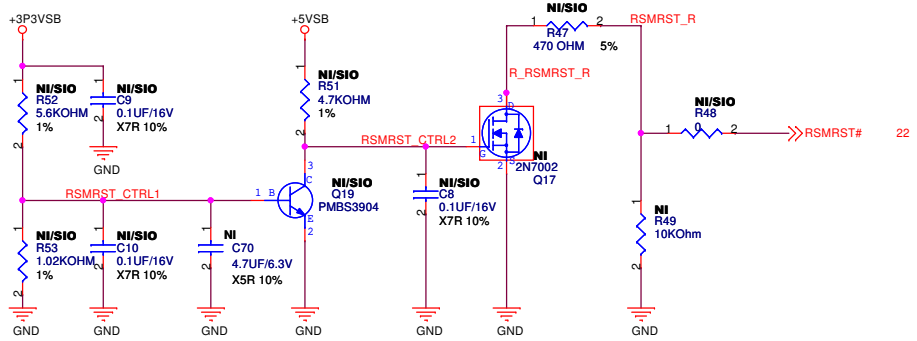
PEGATRON Title : RTC / CMOS / KBMS

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-GS	1.0G1

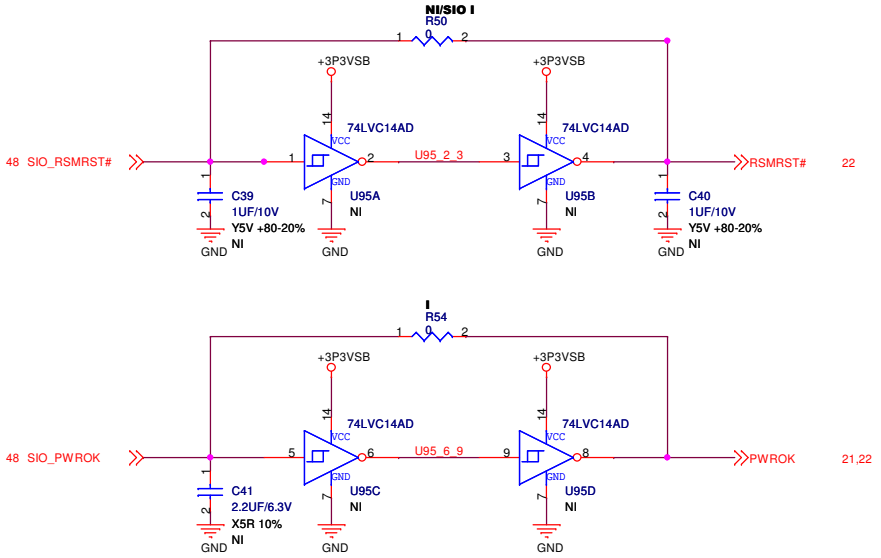
Date: Wednesday, April 07, 2010 Sheet 53 of 68

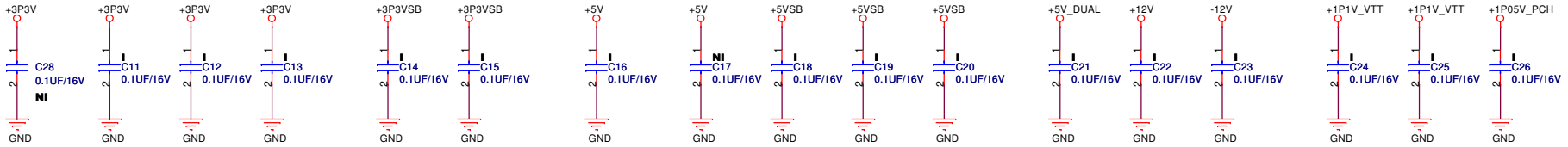
RSMRST CIRCUIT

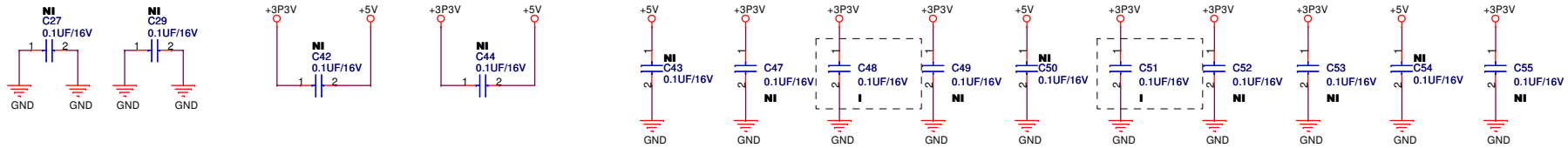


10/02/01 Modify
1.Q17,3904 to 2N7002 (0201change)
2.R52,pull high form +5VSB to +3P3VSB
3.R51,pull high from +3P3VSB to +5VSB
4.Add,C70

Schmitt-trigger for RTC issue

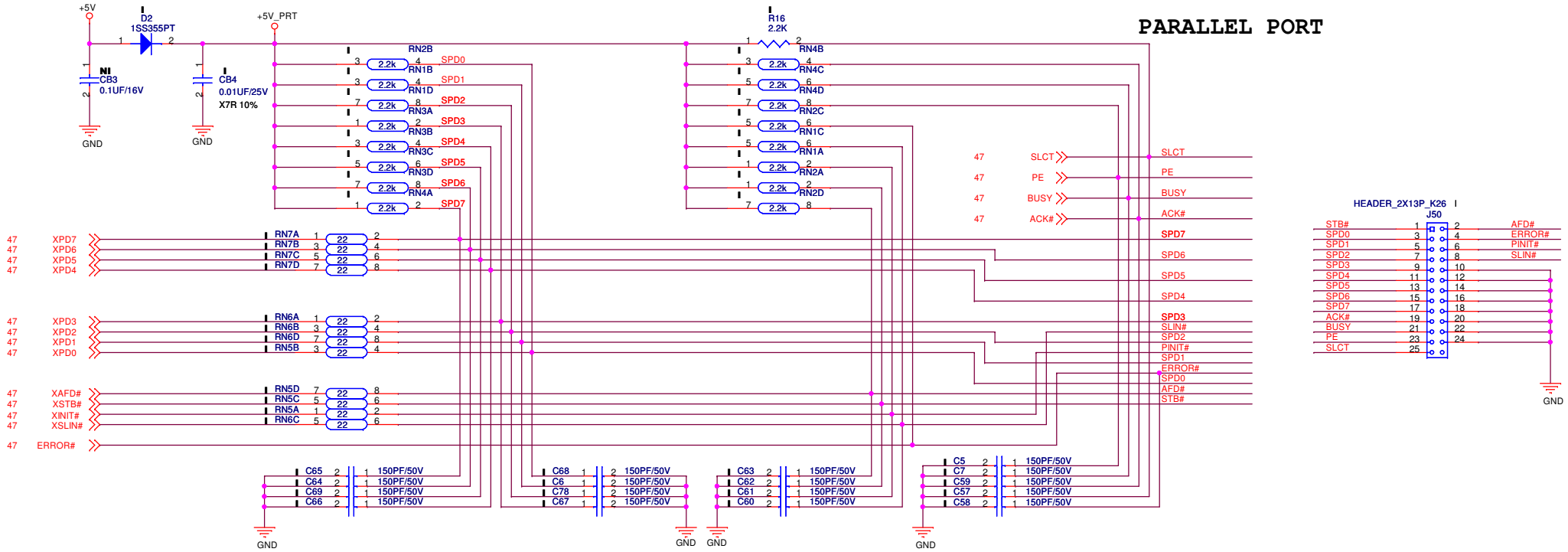






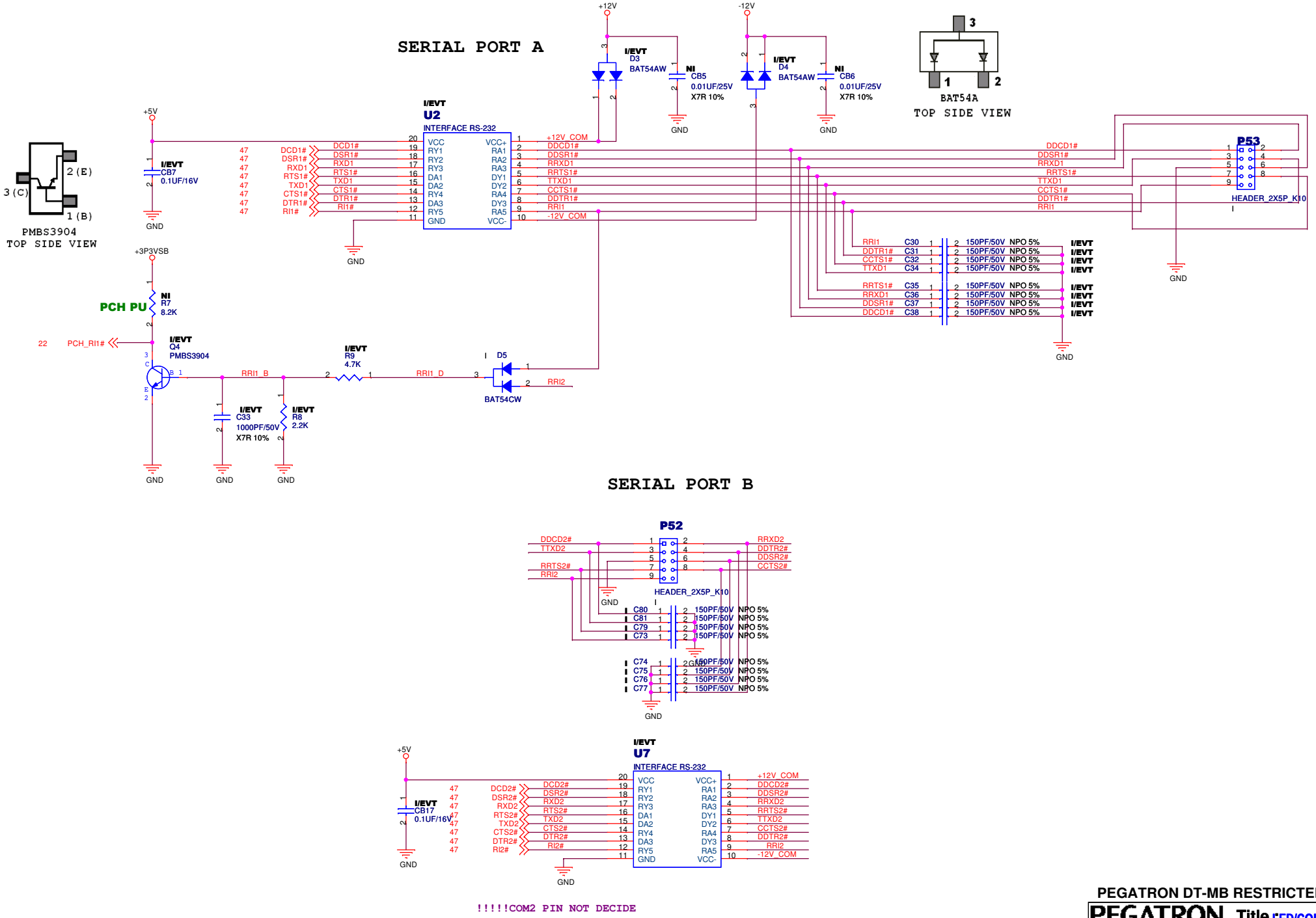
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : RSMRST CIRCUIT	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-GS	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 54 of 68	



PEGATRON DT-MB RESTRICTED SECRET

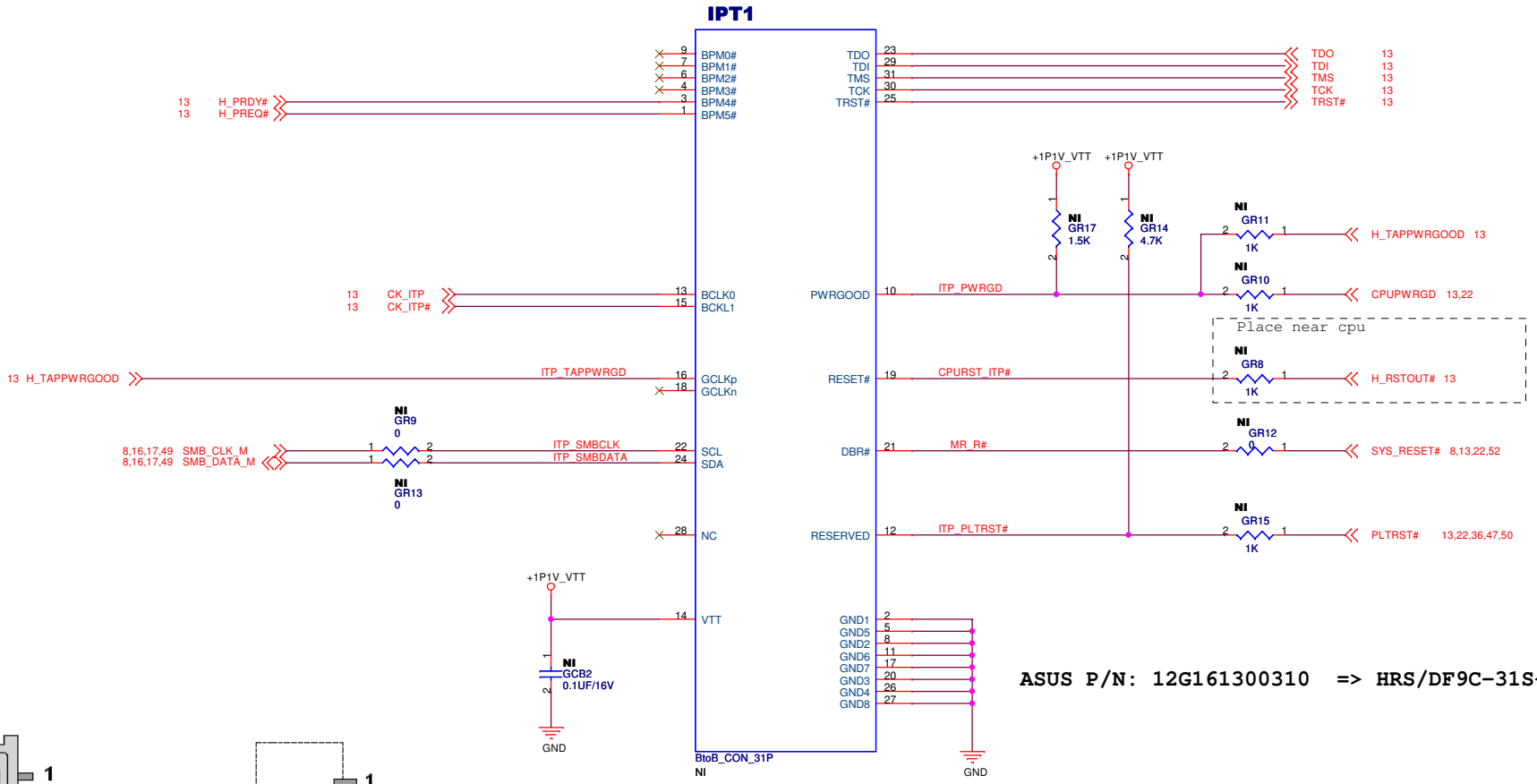
PEGATRON	Title : HDMI Connector	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-GS	Rev: 1. 01
Date: Wednesday, April 07, 2010	Sheet 55 of 68	



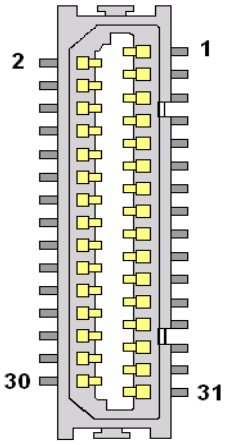
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title: LED/COM/SPKR/INTRU	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-GS	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 56 of 68	

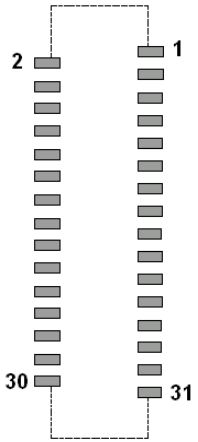
INTEL LGA-775 PROCESSOR ITP DEBUG PORT



ASUS P/N: 12G161300310 => HRS/DF9C-31S-1V(22)



HRS/DF9C-31S-1V(22)
TOP SIDE VIEW



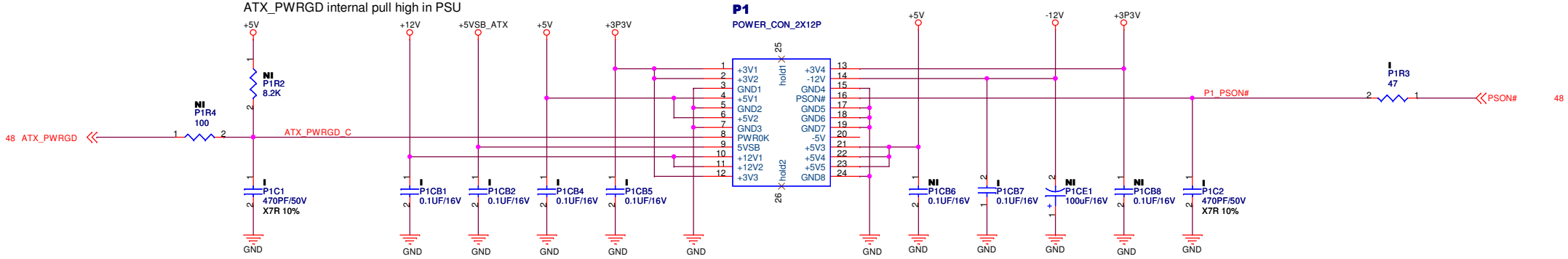
HRS/DF9C-31S-1V(22)
PCB FOOTPRINT

PEGATRON DT-MB RESTRICTED SECRET

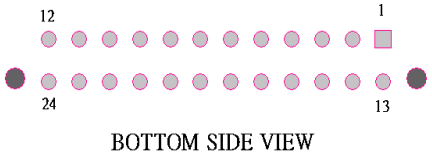
PEGATRON	Title : CPU ITP Debug CONN	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-GS	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 57 of 68	

ATX POWER_24P SUPPLY CONNECTOR

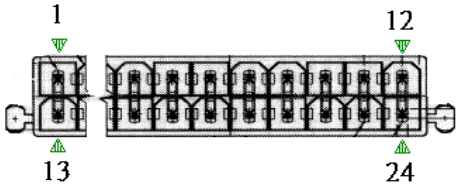
NOTE:
ATX_PWRGD internal pull high in PSU



All of the Caps Around the ATX Power Connector



BOTTOM SIDE VIEW



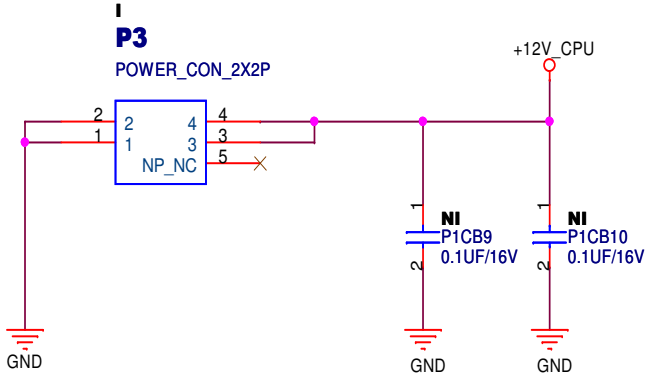
TOP SIDE VIEW

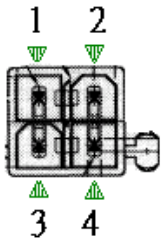
PCB

PCB38

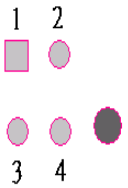
IPMIP-GS R1.00 RED
08M1-0UX0200

VRM POWER_4P SUPPLY CONNECTOR





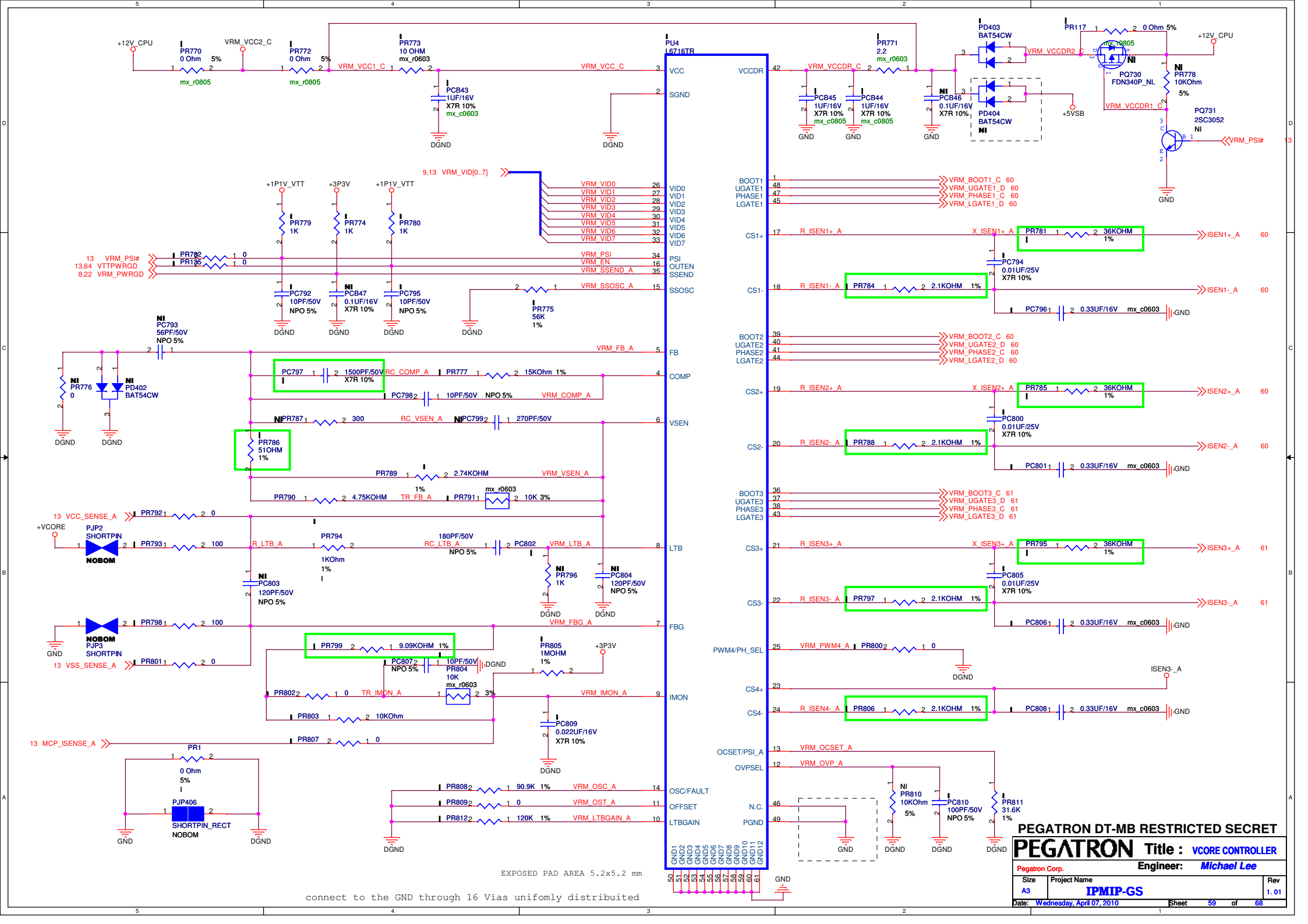
TOP SIDE VIEW

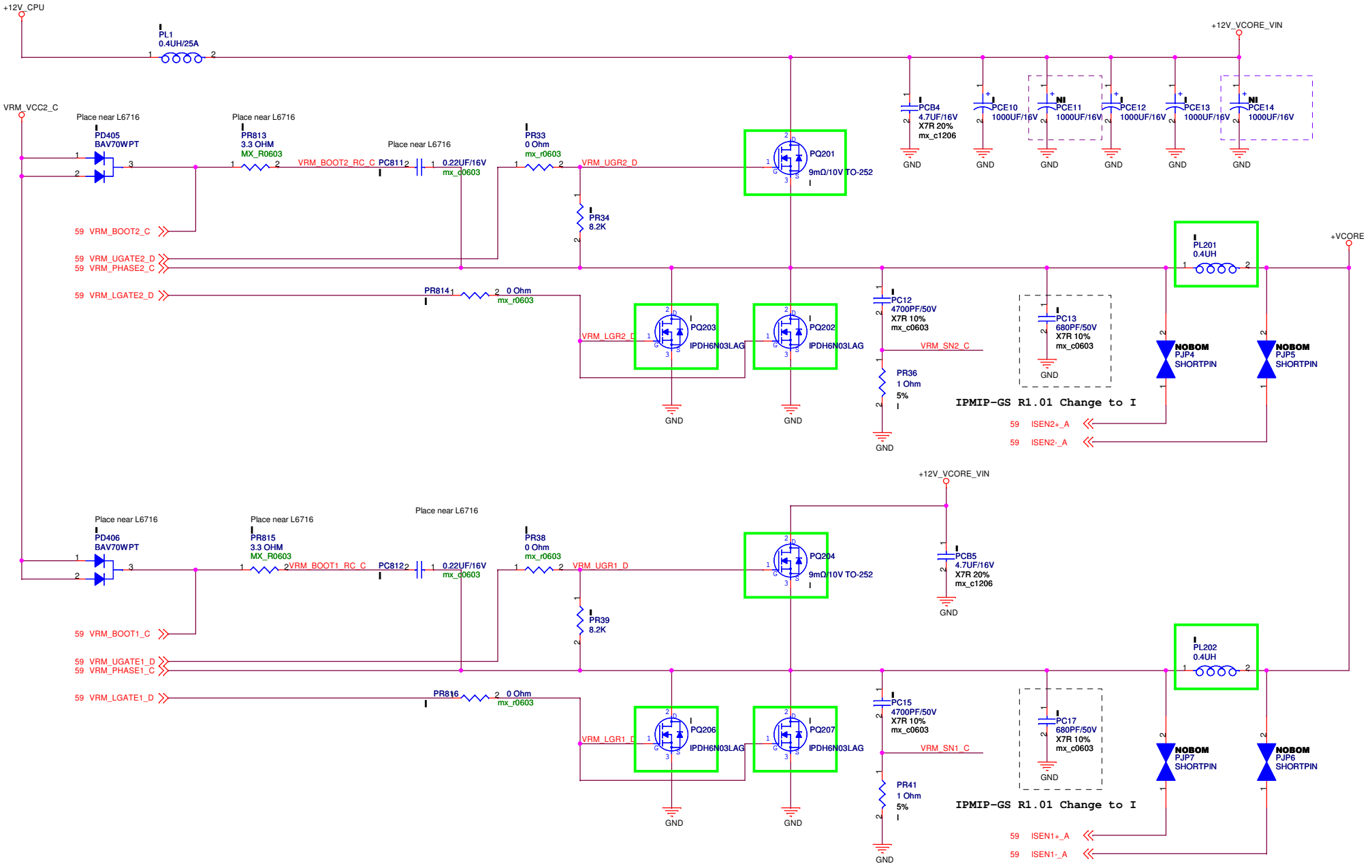


BOTTOM SIDE VIEW

PEGATRON DT-MB RESTRICTED SECRET

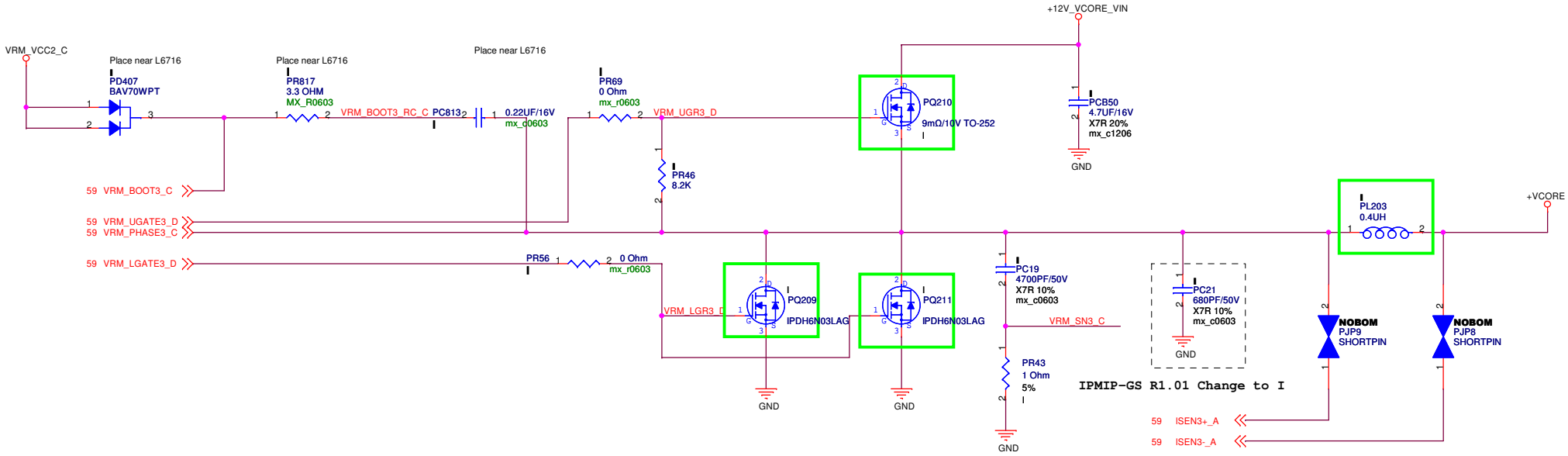
PEGATRON	Title : ATX POWER	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-GS	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 58 of 68	

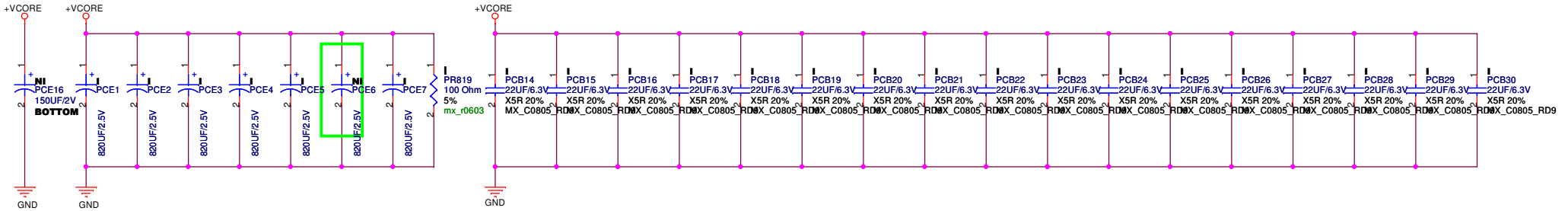

+12V_CPU
VRM_VCC2_C
PR770 0 Ohm 5% mx_r0805
PR772 0 Ohm 5% mx_r0805
VRM_VCC1_C
PR773 10 OHM mx_r0603
VRM_VCC_C
PCB43 1UF/16V X7R 10% mx_c0603
DGND
PU4 L6716TR
VCC
SGND
PR771 2.2 mx_r0603
VRM_VCCDR_C
PD403 BAT54CW
PD404 BAT54CW NI
VRM_VCCDR2_C
PR117 0 Ohm 5%
PQ730 FDN340P_NL NI
PR778 10KOhm 5%
VRM_VCCDR1_C
PQ731 2SC3052 NI
VRM_PSI#
+5VSB
PCB45 1UF/16V X7R 10% mx_c0805
PCB44 1UF/16V X7R 10% mx_c0805
PCB46 0.1UF/16V X7R 10%
GND
VCCDR
9,13 VRM_VID[0..7]
VRM_VID0
VRM_VID1
VRM_VID2
VRM_VID3
VRM_VID4
VRM_VID5
VRM_VID6
VRM_VID7
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VID7
+1P1V_VTT
+3P3V
PR779 1K
PR774 1K
PR780 1K
13 VRM_PSI#
13,64 VTTPWRGD
8,22 VRM_PWRGD
PR782 0
PR135 0
VRM_PSI
VRM_EN
VRM_SSEND_A
PSI
OUTEN
SSEND
PC792 10PF/50V NPO 5%
PCB47 0.1UF/16V X7R 10%
PC795 10PF/50V NPO 5%
VRM_SSOSC_A
SSOSC
PR775 56K 1%
PC793 56PF/50V NPO 5%
NI PR776 0
NI PD402 BAT54CW
VRM_FB_A
FB
PC797 1500PF/50V X7R 10%
RC_COMP_A
PR777 15KOhm 1%
COMP
PC798 10PF/50V NPO 5%
VRM_COMP_A
NI PR787 300
RC_VSEN_A
NI PC799 270PF/50V
VSEN
PR786 51OHM 1%
PR789 2.74KOHM 1%
VRM_VSEN_A
PR790 4.75KOHM
TR_FB_A
PR791 10K 3%
mx_r0603
13 VCC_SENSE_A
PR792 0
+VCORE
PJP2 SHORTPIN NOBOM
PR793 100
R_LTB_A
PR794 1KOhm 1%
180PF/50V NPO 5%
RC_LTB_A
PC802
VRM_LTB_A
LTB
NI PC803 120PF/50V NPO 5%
NI PR796 1K
NI PC804 120PF/50V NPO 5%
NOBOM PJP3 SHORTPIN
PR798 100
VRM_FBG_A
FBG
13 VSS_SENSE_A
PR801 0
PR799 9.09KOHM 1%
PC807 10PF/50V NPO 5%
PR804 10K mx_r0603
PR805 1MOHM 1%
+3P3V
PR802 0
TR_IMON_A
VRM_IMON_A
IMON
PR803 10KOhm
PC809 0.022UF/16V X7R 10%
13 MCP_ISENSE_A
PR807 0
PR1 0 Ohm 5%
PJP406 SHORTPIN_RECT NOBOM
GND
PR808 90.9K 1%
VRM_OSC_A
OSC/FAULT
PR809 0
VRM_OST_A
OFFSET
PR812 120K 1%
VRM_LTBGAIN_A
LTBGAIN
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12
BOOT1
UGATE1
PHASE1
LGATE1
VRM_BOOT1_C 60
VRM_UGATE1_D 60
VRM_PHASE1_C 60
VRM_LGATE1_D 60
CS1+
R_ISEN1+_A
X_ISEN1+_A
PR781 36KOHM 1%
ISEN1+_A 60
PC794 0.01UF/25V X7R 10%
CS1-
R_ISEN1-_A
PR784 2.1KOHM 1%
ISEN1-_A 60
PC796 0.33UF/16V mx_c0603
BOOT2
UGATE2
PHASE2
LGATE2
VRM_BOOT2_C 60
VRM_UGATE2_D 60
VRM_PHASE2_C 60
VRM_LGATE2_D 60
CS2+
R_ISEN2+_A
X_ISEN2+_A
PR785 36KOHM 1%
ISEN2+_A 60
PC800 0.01UF/25V X7R 10%
CS2-
R_ISEN2-_A
PR788 2.1KOHM 1%
ISEN2-_A 60
PC801 0.33UF/16V mx_c0603
BOOT3
UGATE3
PHASE3
LGATE3
VRM_BOOT3_C 61
VRM_UGATE3_D 61
VRM_PHASE3_C 61
VRM_LGATE3_D 61
CS3+
R_ISEN3+_A
X_ISEN3+_A
PR795 36KOHM 1%
ISEN3+_A 61
PC805 0.01UF/25V X7R 10%
CS3-
R_ISEN3-_A
PR797 2.1KOHM 1%
ISEN3-_A 61
PC806 0.33UF/16V mx_c0603
PWM4/PH_SEL
VRM_PWM4_A
PR800 0
CS4+
CS4-
R_ISEN4-_A
PR806 2.1KOHM 1%
PC808 0.33UF/16V mx_c0603
OCSET/PSI_A
VRM_OCSET_A
OVPSEL
VRM_OVP_A
N.C.
PGND
NI PR810 10KOhm 5%
PC810 100PF/50V NPO 5%
PR811 31.6K 1%
EXPOSED PAD AREA 5.2x5.2 mm
connect to the GND through 16 Vias unifomly distribuited
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : VCORE CONTROLLER
Pegatron Corp.
Engineer: Michael Lee
Size A3
Project Name IPMIP-GS
Rev 1.01
Date: Wednesday, April 07, 2010
Sheet 59 of 68



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : VCORE DRIVER-1	
Pegatron Corp.	Engineer: Michael Lee	
Size: A3	Project Name: IPMIP-GS	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 60 of 68	





+CPU VCORE OUTPUT CAPs

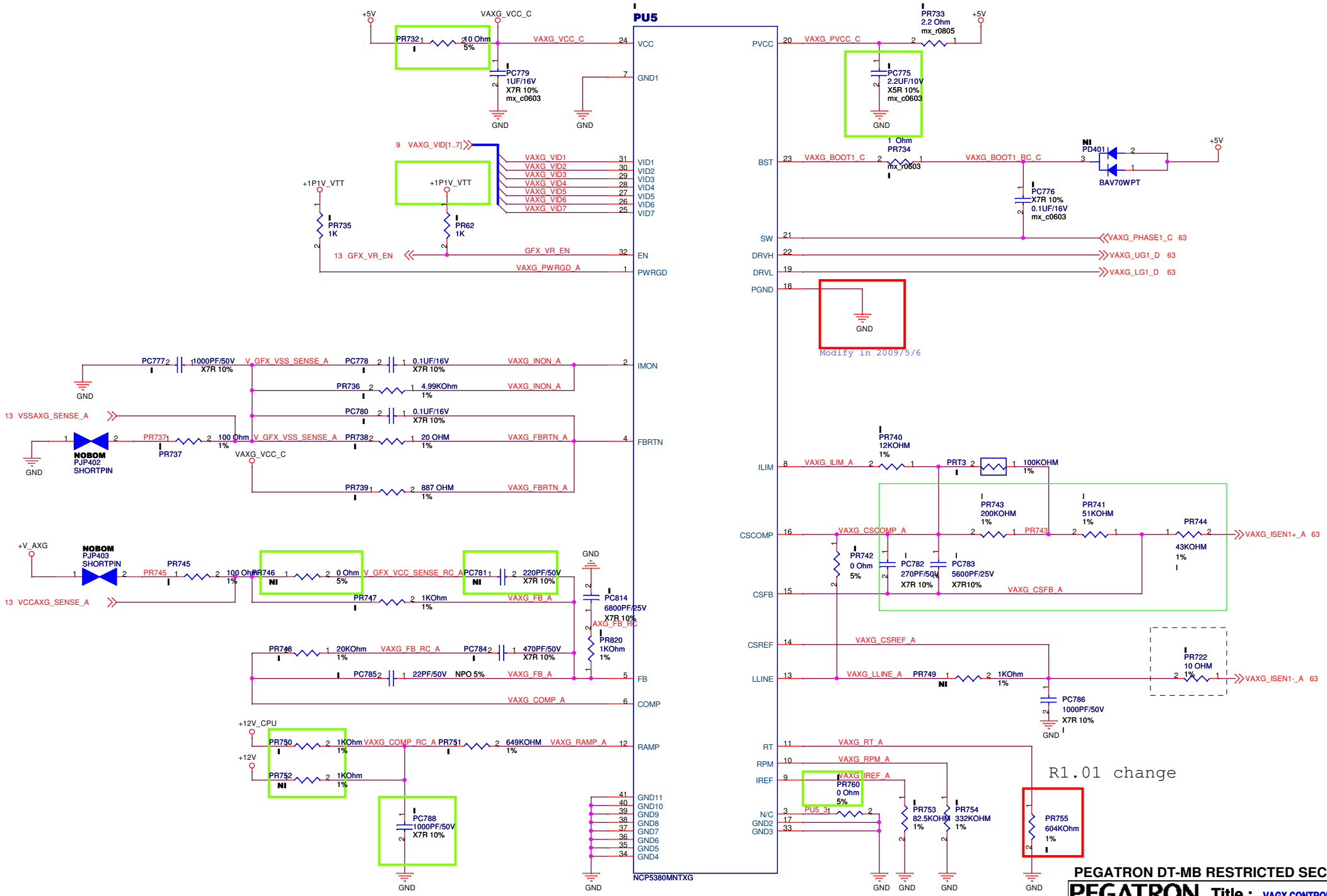
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VCORE DRIVER-2

Pegatron Corp. Engineer: Michael Lee

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 61 of 68



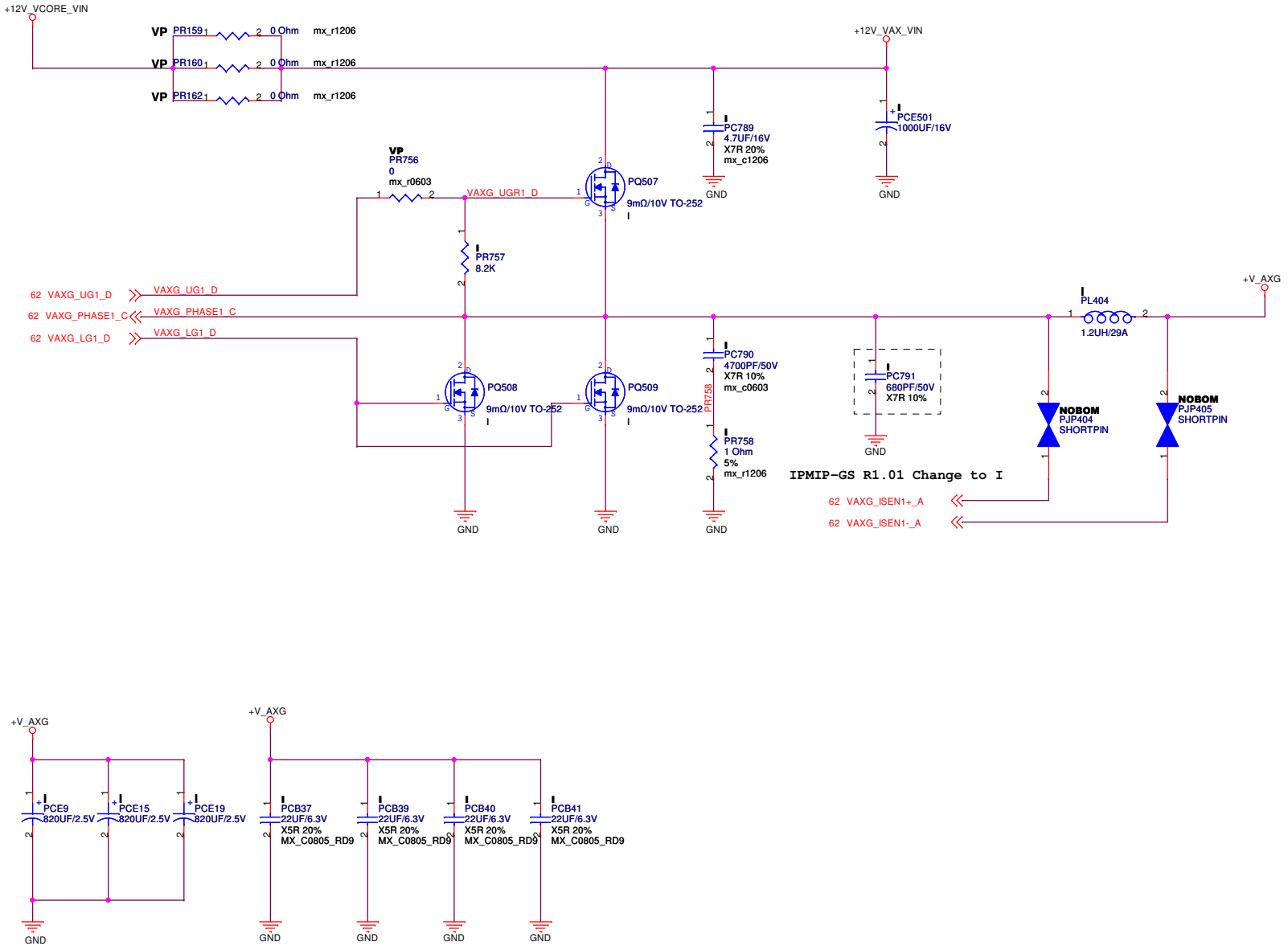
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VAGX CONTROLLER

Pegatron Corp. Engineer: Michael Lee

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 62 of 68



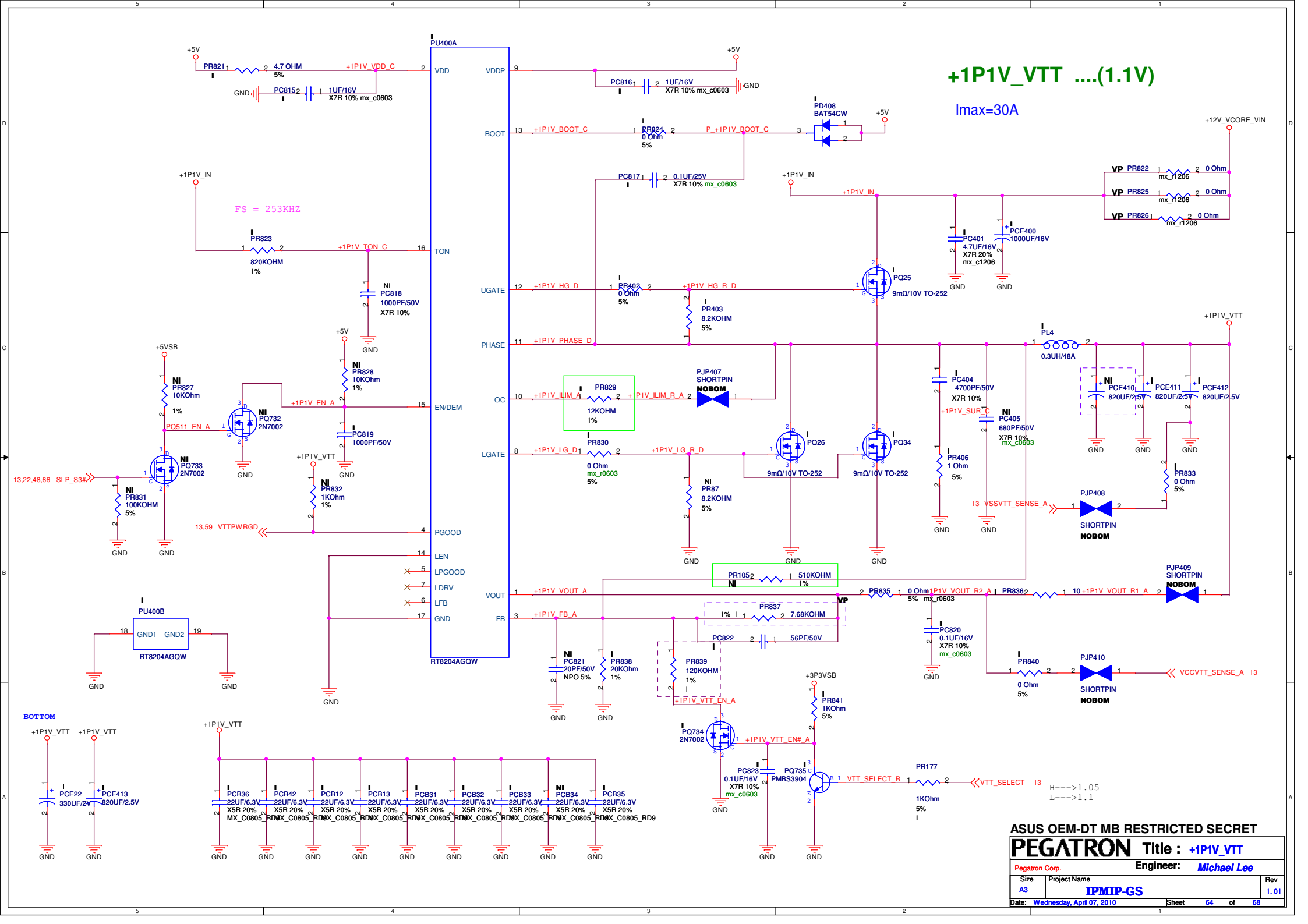
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VAGX DRIVER

Pegatron Corp. Engineer: Michael Lee

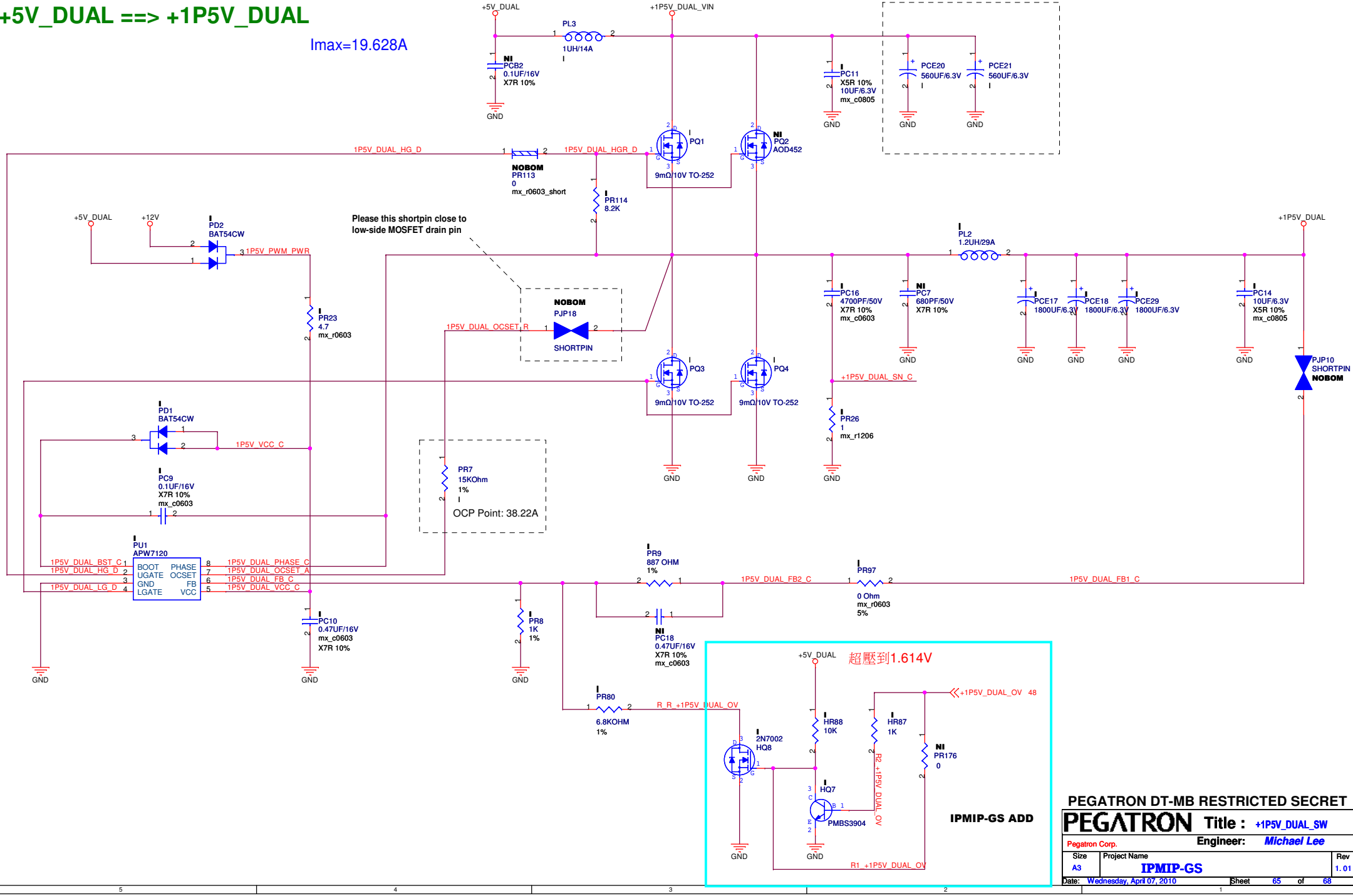
Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 63 of 68


+1P1V_VTT ....(1.1V)
Imax=30A
PU400A
RT8204AGQW
FS = 253KHZ
+1P1V_IN
+12V_VCORE_IN
+1P1V_VTT
+5V
+5VSB
+3P3VSB
GND
VDD
VDDP
BOOT
UGATE
PHASE
OC
LGATE
PGOOD
EN/DEM
TON
LEN
LPGOOD
LDRV
LFB
VOUT
FB
PU400B
GND1
GND2
PR821 4.7 OHM 5%
PC815 1UF/16V X7R 10% mx_c0603
PC816 1UF/16V X7R 10% mx_c0603
PD408 BAT54CW
PR824 0 Ohm 5%
PC817 0.1UF/25V X7R 10% mx_c0603
PR823 820KOHM 1%
PC818 1000PF/50V X7R 10%
PR828 10KOhm 1%
PC819 1000PF/50V
PR827 10KOhm 1%
PQ732 2N7002
PQ733 2N7002
PR831 100KOHM 5%
PR832 1KOhm 1%
PQ511_EN_A
+1P1V_EN_A
13,22,48,66 SLP_S3#
13,59 VTTPWRGD
PR402 0 Ohm 5%
PR403 8.2KOHM 5%
PQ25 9mΩ/10V TO-252
PC401 4.7UF/16V X7R 20% mx_c1206
PCE400 1000UF/16V
VP PR822 0 Ohm mx_r1206
VP PR825 0 Ohm mx_r1206
VP PR826 0 Ohm mx_r1206
PL4 0.3UH/48A
PJP407 SHORTPIN NOBOM
PR829 12KOHM 1%
PR830 0 Ohm mx_r0603 5%
PR87 8.2KOHM 5%
PQ26 9mΩ/10V TO-252
PQ34 9mΩ/10V TO-252
PC404 4700PF/50V X7R 10%
PC405 680PF/50V X7R 10% mx_c0603
PR406 1 Ohm 5%
PCE410 820UF/2.5V
PCE411 820UF/2.5V
PCE412 820UF/2.5V
PR833 0 Ohm 5%
PJP408 SHORTPIN NOBOM
13 VSSVTT_SENSE_A
PR105 510KOHM 1%
PR835 0 Ohm 5% mx_r0603
PR836 10
PJP409 SHORTPIN NOBOM
PR837 7.68KOHM 1%
PC822 56PF/50V
PC820 0.1UF/16V X7R 10% mx_c0603
PR840 0 Ohm 5%
PJP410 SHORTPIN NOBOM
VCCVTT_SENSE_A 13
PC821 20PF/50V NPO 5%
PR838 20KOhm 1%
PR839 120KOHM 1%
+1P1V_VTT_EN_A
PR841 1KOhm 5%
PQ734 2N7002
+1P1V_VTT_EN#_A
PC823 0.1UF/16V X7R 10% mx_c0603
PQ735 PMBS3904
VTT_SELECT_R
PR177 1KOhm 5%
VTT_SELECT 13
H--->1.05
L--->1.1
BOTTOM
PCE22 330UF/2V
PCE413 820UF/2.5V
PCB36 22UF/6.3V X5R 20% MX_C0805_RD0
PCB42 22UF/6.3V X5R 20% MX_C0805_RD0
PCB12 22UF/6.3V X5R 20% MX_C0805_RD0
PCB13 22UF/6.3V X5R 20% MX_C0805_RD0
PCB31 22UF/6.3V X5R 20% MX_C0805_RD0
PCB32 22UF/6.3V X5R 20% MX_C0805_RD0
PCB33 22UF/6.3V X5R 20% MX_C0805_RD0
PCB34 22UF/6.3V X5R 20% MX_C0805_RD0
PCB35 22UF/6.3V X5R 20% MX_C0805_RD9
ASUS OEM-DT MB RESTRICTED SECRET
PEGATRON
Title : +1P1V_VTT
Pegatron Corp.
Engineer: Michael Lee
Size A3
Project Name IPMIP-GS
Rev 1.01
Date: Wednesday, April 07, 2010
Sheet 64 of 68

+5V_DUAL ==> +1P5V_DUAL

Imax=19.628A



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +1P5V_DUAL_SW

Pegatron Corp. Engineer: Michael Lee

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 65 of 68

R1.01 add for PCH CORE LVR CONTROL

+1P05V_PCH

Imax=5.598A

+1P05V_DUAL

PR508 20K 1%

PR509 20K 1%

PQ22 IPDH6N03LAG

PQ23 IPDH6N03LAG

OP1_VG_C

PC501 470PF/50V X7R 10%

PC503 3900PF/50V X7R 10%

PR506 1K

PR124 4.7K

OP1_REF_A

PR179 1K

PR131 1K

PR128 0

PQ17_D

PQ18 2N7002

PC520 0.1UF/16V

PR505 9.31K 1%

PQ28 PMBS3904

PC522 0.1UF/16V

PR511 20K 1%

PR521 0.1UF/16V

PR507 24K 1%

PQ18_B

OP1_FB_A

OP2_REF_A

PU3 LM358

+12V

PC561 0.1UF/25V mx_c0603

+1P05V_PCH

PCE8 820UF/2.5V

PC554 0.1UF/25V mx_c0603

+3P3V

OP2_VG_C

PQ32 P3055LDG

PR178 100K 1%

PC502 470PF/50V X7R 10%

PR129 4.7K

PC69_PR80

PC71 3300PF/25V X7R 10%

PR512 1K

OP2_FB_A

PJP21 SHORTPIN NOBOM

+1P8V_SFR

PCE36 820UF/6.3V

R1.01 ADD OP2

PR180 1K

SLP_S3# 13,22,48,64

R1.01 add for PCH CORE LVR CONTROL

Imax=1.84A

Install for AMT support

+1P05V_ME

I/AMTNI PR47 0 mx_r1206

+1P05V_PCH

PR52 30.1KOHM 1%

PR53 301K 1%

PC29 0.47UF/16V X7R 10%

PQ14B PMBS3904

PQ1415

+3P3VSB

+3P3V_ME

R43 0 Ohm

R42R43

PR127 0 Ohm

PR54 33KOHM

PR55 5.6KOHM

PD3 BAT54CW

SLP_M# 22,67

MEPWROK 21

PC30 0.1UF/16V X7R 10%

PQ15 PMBS3904

IP R1.01 CRB1.5

PC31 100PF/50V NPO 5%

Install for AMT support

Fsw = 500KHz

+1P05V_ME

Imax=2.222A

+5VSB

PR73 1MOhm 5%

PR731 750KOhm

1P05VME_EN_A

1P05VME_FSW

PR74 100K

PQ17 2N7002

22,67 SLP_M#

PU763 RT8015APQW

SHDN/RT GND1 LX1 LX2 PGND GND2 COMP FB VDD PVDD2 PVDD1

1P05MELX

1P05MECOM_A

1P05MEFB_A

PR728 13KOHM 1%

PC771 1000PF/50V X7R 10%

PR728_A

PR729 154KOHM 1%

PR730 49.9KOHM

PC42 22PF/50V

1P05MEFB1_A

PR78 0 Ohm 5%

PL402 4.7UH

1P05MELX_R

PC722 22UF/6.3V X5R 10%

PC723 22UF/6.3V X5R 10%

PC724 22UF/6.3V X5R 10%

+1P05V_ME

+5VSB

PR76 8.2K

PQ13_G

PR13 4.7K

PQ37 PMBS3904

22,67 SLP_M#

+1P05V_ME

+1P05V_PCH

PR45 0 mx_r1206

FDN340P_NL PQ13

+1P05V_PCH_PR45

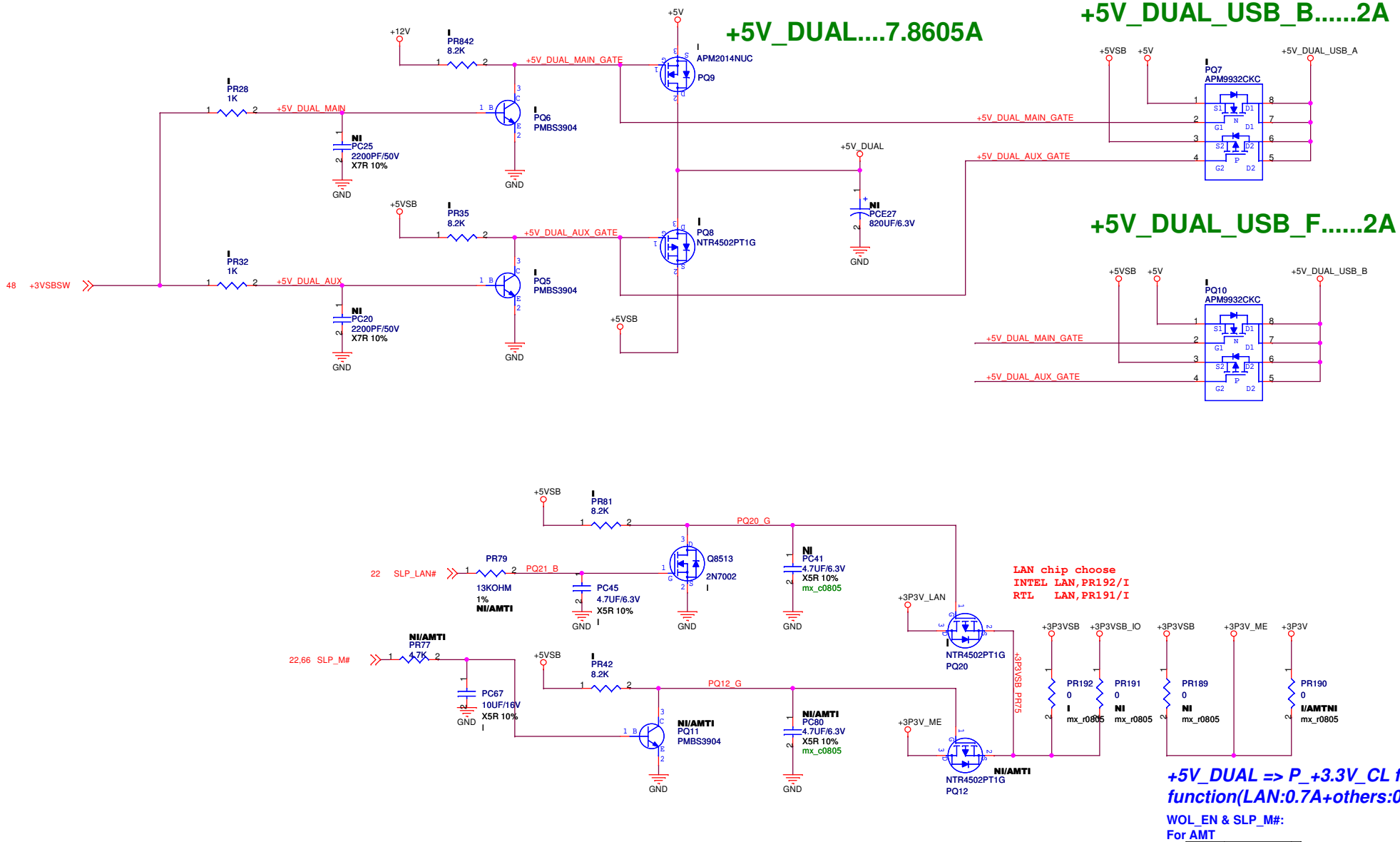
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title :+1P05V_PCH & +1P05V_ME

Pegatron Corp. Engineer: Michael Lee

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Wednesday, April 07, 2010 Sheet 66 of 68

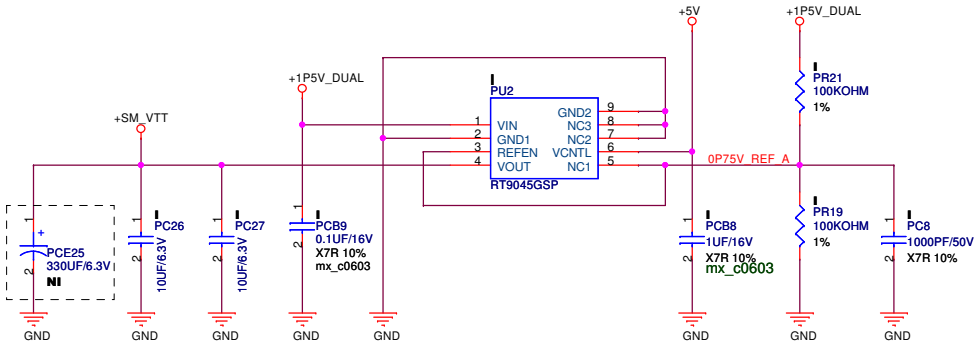


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : +5V_DUAL & +3P3V_ME	
Pegatron Corp.	Engineer: Michael Lee	
Size: A3	Project Name: IPMIP-GS	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 67 of 68	

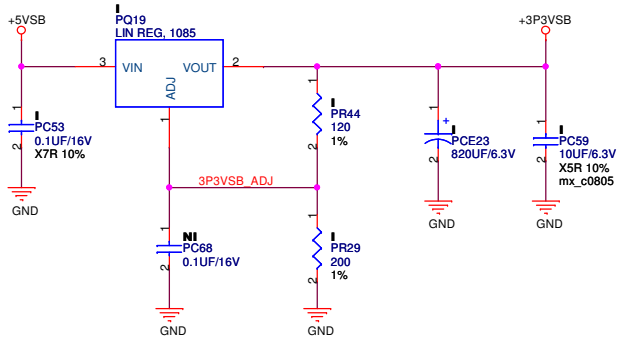
+1P5V_DUAL ==> +0P75V_VTT_DDR

Imax=0.83A



4/28 MODIFY

+5VSB ==> +3P3VSB....3.44A



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title +0P75V_VTT_ & +1P8V_SFR

Pegatron Corp. Engineer: Michael Lee

Size	Project Name	Rev
A3	IPMIP-GS	1.01

Date: Thursday, April 01, 2010 Sheet 68 of 68