2016 Apollo Lake Ironhide_APL"

Schematics Document

EMMC

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

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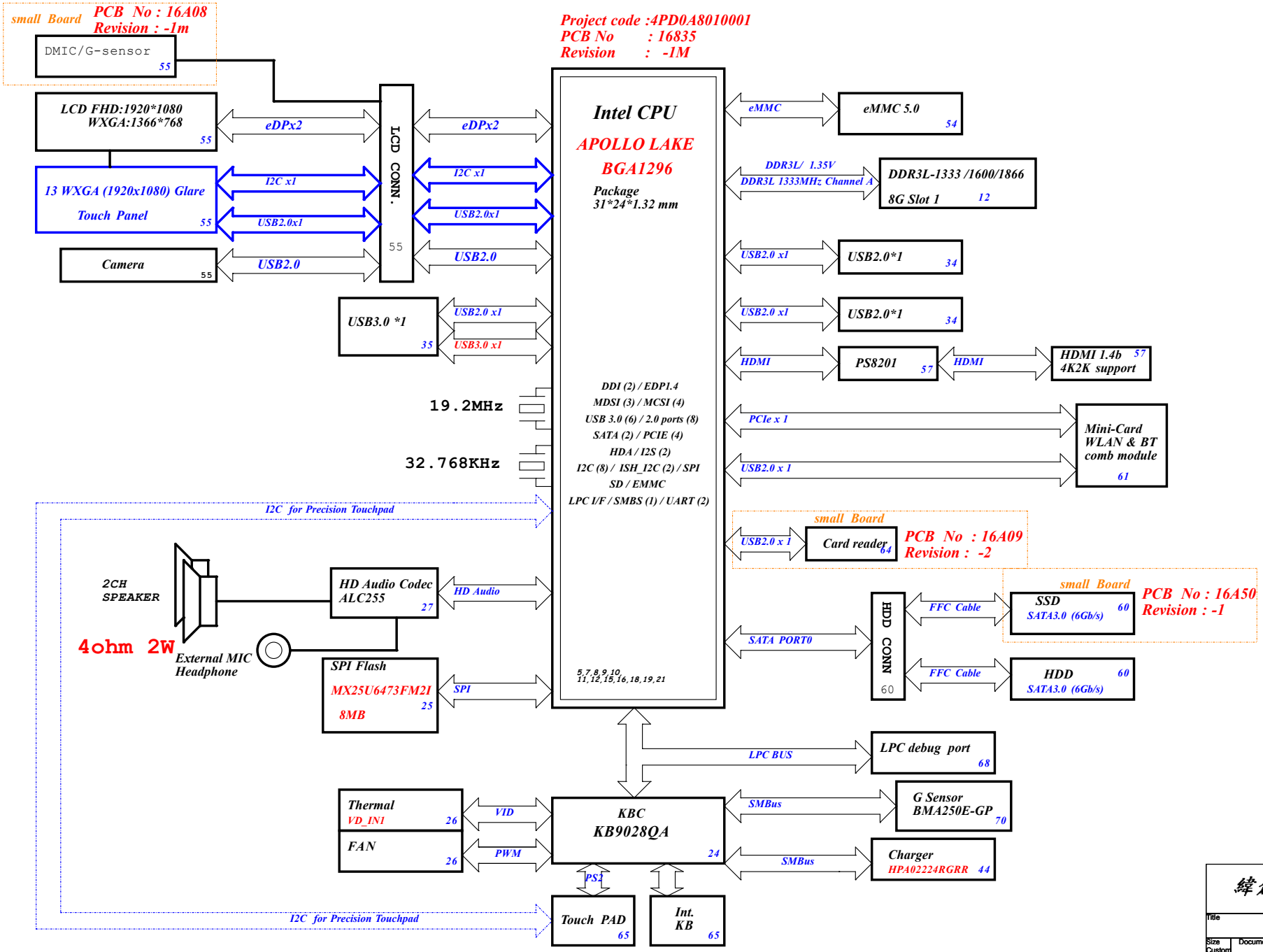
Ironhide_APL Board Block Diagram

small Board PCB No : 16A08
Revision : -1m

Project code :4PD0A8010001
PCB No : 16835
Revision : -1M



CHARGER HPA02224	44
INPUTS	OUTPUTS
19V_DCBATOUT	BT+

SYSTEM DC/DC RT6575DGQW	45
INPUTS	OUTPUTS
19V_DCBATOUT	5V_S5 3D3V_S5

CPU DC/DC RT5073AGQW-GP	46
INPUTS	OUTPUTS
19V_DCBATOUT	1D8V_S5 1D24V_S5 1D05V_S0
PWR_VDDQ	PWR_VTT

SYSTEM DC/DC RT9610BZQW-GP	47
INPUTS	OUTPUTS
5V_S5	1V_CPU_VCGI

CPU DC/DC RT9610BZQW-GP	50
INPUTS	OUTPUTS
5V_S5	1V_CPU_VNN

CPU DC/DC RT9610BZQW-GP	51
INPUTS	OUTPUTS
5V_S5	PWR_VDDQ

SYSTEM Load switch APE8910	40
INPUTS	OUTPUTS
5V_S5	5V_S0
3D3V_S5	3V_S0
1D8V_S5	1D8V_S0

SYSTEM DC/DC TL70215	53
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

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SSID = CPU

Blanking

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Title: *(Reserved)*

Size	Document Number	Rev
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SSID = CPU

Blanking

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Size	Document Number	Rev
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SSID = CPU

12 M_A_DQ[63:0]

M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14 M_A_A15 → M_A_A[15:0] 12

M_A_DQS_DN0 M_A_DQS_DN1 M_A_DQS_DN2 M_A_DQS_DN3 M_A_DQS_DN4 M_A_DQS_DN5 M_A_DQS_DN6 M_A_DQS_DN7 → M_A_DQS_DN[7:0] 12

M_A_DQS_DP0 M_A_DQS_DP1 M_A_DQS_DP2 M_A_DQS_DP3 M_A_DQS_DP4 M_A_DQS_DP5 M_A_DQS_DP6 M_A_DQS_DP7 → M_A_DQS_DP[7:0] 12

12 M_A_BS0
12 M_A_BS1
12 M_A_BS2
12 M_A_ODT0
12 M_A_ODT1
12 M_A_CAS#
12 M_A_WE#
12 M_A_RAS#

12 M_A_CS#1
12 M_A_CS#0
12 M_A_CLK1
12 M_A_CLK#1
12 M_A_CLK0
12 M_A_CLK#0
12 M_A_CKE0
12 M_A_CKE1

12 DDR3_DRAMRST#

CPU1A — 1 OF 23 — APL_SOC

M_A_DQ0	AY62	MEM_CH0_DQ0/MEM_CH0_DQA0	
M_A_DQ1	AY61	MEM_CH0_DQ1/MEM_CH0_DQA1	
M_A_DQ2	BE62	MEM_CH0_DQ2/MEM_CH0_DQA2	
M_A_DQ3	BG62	MEM_CH0_DQ3/MEM_CH0_DQA3	
M_A_DQ4	BD63	MEM_CH0_DQ4/MEM_CH0_DQA4	
M_A_DQ5	AW62	MEM_CH0_DQ5/MEM_CH0_DQA5	
M_A_DQ6	AW63	MEM_CH0_DQ6/MEM_CH0_DQA6	
M_A_DQ7	BD62	MEM_CH0_DQ7/MEM_CH0_DQA7	
M_A_DQ8	AV59	MEM_CH0_DQ8/MEM_CH0_DQA8	
M_A_DQ9	AU63	MEM_CH0_DQ9/MEM_CH0_DQA9	
M_A_DQ10	AU62	MEM_CH0_DQ10/MEM_CH0_DQA10	
M_A_DQ11	AV58	MEM_CH0_DQ11/MEM_CH0_DQA11	
M_A_DQ12	AV57	MEM_CH0_DQ12/MEM_CH0_DQA12	
M_A_DQ13	AT55	MEM_CH0_DQ13/MEM_CH0_DQA13	
M_A_DQ14	AT54	MEM_CH0_DQ14/MEM_CH0_DQA14	
M_A_DQ15	AY59	MEM_CH0_DQ15/MEM_CH0_DQA15	
M_A_DQ16	AY57	MEM_CH0_DQ16/MEM_CH0_DQA16	
M_A_DQ17	BB57	MEM_CH0_DQ17/MEM_CH0_DQA17	
M_A_DQ18	BD59	MEM_CH0_DQ18/MEM_CH0_DQA18	
M_A_DQ19	BF59	MEM_CH0_DQ19/MEM_CH0_DQA19	
M_A_DQ20	AV54	MEM_CH0_DQ20/MEM_CH0_DQA20	
M_A_DQ21	AY55	MEM_CH0_DQ21/MEM_CH0_DQA21	
M_A_DQ22	AV52	MEM_CH0_DQ22/MEM_CH0_DQA22	
M_A_DQ23	BD58	MEM_CH0_DQ23/MEM_CH0_DQA23	
M_A_DQ24	BE56	MEM_CH0_DQ24/MEM_CH0_DQA24	
M_A_DQ25	BD54	MEM_CH0_DQ25/MEM_CH0_DQA25	
M_A_DQ26	BF58	MEM_CH0_DQ26/MEM_CH0_DQA26	
M_A_DQ27	BE50	MEM_CH0_DQ27/MEM_CH0_DQA27	
M_A_DQ29	BB50	MEM_CH0_DQ29/MEM_CH0_DQA29	
M_A_DQ28	BD50	MEM_CH0_DQ28/MEM_CH0_DQA28	
M_A_DQ30	BA50	MEM_CH0_DQ30/MEM_CH0_DQA30	
M_A_DQ31	BB54	MEM_CH0_DQ31/MEM_CH0_DQA31	
		MEM_CH0_DQ32/MEM_CH0_DQB0	AR39 M_A_DQ32
		MEM_CH0_DQ33/MEM_CH0_DQB1	AV37 M_A_DQ33
		MEM_CH0_DQ34/MEM_CH0_DQB2	AW37 M_A_DQ34
		MEM_CH0_DQ35/MEM_CH0_DQB3	AR37 M_A_DQ35
		MEM_CH0_DQ36/MEM_CH0_DQB4	AT37 M_A_DQ36
		MEM_CH0_DQ37/MEM_CH0_DQB5	AT41 M_A_DQ37
		MEM_CH0_DQ38/MEM_CH0_DQB6	AR41 M_A_DQ38
		MEM_CH0_DQ39/MEM_CH0_DQB7	AW35 M_A_DQ39
		MEM_CH0_DQ40/MEM_CH0_DQB8	BJ44 M_A_DQ40
		MEM_CH0_DQ41/MEM_CH0_DQB9	BG39 M_A_DQ41
		MEM_CH0_DQ42/MEM_CH0_DQB10	BG40 M_A_DQ42
		MEM_CH0_DQ43/MEM_CH0_DQB11	BJ40 M_A_DQ43
		MEM_CH0_DQ44/MEM_CH0_DQB12	BG43 M_A_DQ44
		MEM_CH0_DQ45/MEM_CH0_DQB13	BG44 M_A_DQ45
		MEM_CH0_DQ46/MEM_CH0_DQB14	BH45 M_A_DQ46
		MEM_CH0_DQ47/MEM_CH0_DQB15	BH41 M_A_DQ47
		MEM_CH0_DQ48/MEM_CH0_DQB16	BA34 M_A_DQ48
		MEM_CH0_DQ49/MEM_CH0_DQB17	BE34 M_A_DQ49
		MEM_CH0_DQ50/MEM_CH0_DQB18	BD34 M_A_DQ50
		MEM_CH0_DQ51/MEM_CH0_DQB19	BD37 M_A_DQ51
		MEM_CH0_DQ52/MEM_CH0_DQB20	BB37 M_A_DQ52
		MEM_CH0_DQ53/MEM_CH0_DQB21	BE39 M_A_DQ53
		MEM_CH0_DQ54/MEM_CH0_DQB22	BD39 M_A_DQ54
		MEM_CH0_DQ55/MEM_CH0_DQB23	BB34 M_A_DQ55
		MEM_CH0_DQ56/MEM_CH0_DQB24	BJ38 M_A_DQ56
		MEM_CH0_DQ57/MEM_CH0_DQB25	BG34 M_A_DQ57
		MEM_CH0_DQ58/MEM_CH0_DQB26	BG33 M_A_DQ58
		MEM_CH0_DQ59/MEM_CH0_DQB27	BH33 M_A_DQ59
		MEM_CH0_DQ60/MEM_CH0_DQB28	BG38 M_A_DQ60
		MEM_CH0_DQ61/MEM_CH0_DQB29	BH37 M_A_DQ61
		MEM_CH0_DQ62/MEM_CH0_DQB30	BG37 M_A_DQ62
		MEM_CH0_DQ63/MEM_CH0_DQB31	BJ34 M_A_DQ63

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CPU1B — 2 OF 23 — APL_SOC

M_A_DQS_DP0	BB63	MEM_CH0_DQSP0/MEM_CH0_DQSPA0	
M_A_DQS_DN0	BC62	MEM_CH0_DQSN0/MEM_CH0_DQSNA0	
M_A_DQS_DP1	AT59	MEM_CH0_DQSP1/MEM_CH0_DQSPA1	
M_A_DQS_DN1	AT58	MEM_CH0_DQSN1/MEM_CH0_DQSNA1	
M_A_DQS_DP2	BB59	MEM_CH0_DQSP2/MEM_CH0_DQSPA2	
M_A_DQS_DN2	BB58	MEM_CH0_DQSN2/MEM_CH0_DQSNA2	
M_A_DQS_DP3	BD52	MEM_CH0_DQSP3/MEM_CH0_DQSPA3	
M_A_DQS_DN3	BB52	MEM_CH0_DQSN3/MEM_CH0_DQSNA3	
M_A_DQS_DP4	AV39	MEM_CH0_DQSP4/MEM_CH0_DQSPB0	
M_A_DQS_DN4	AW39	MEM_CH0_DQSN4/MEM_CH0_DQSNB0	
M_A_DQS_DP5	BJ42	MEM_CH0_DQSP5/MEM_CH0_DQSPB1	
M_A_DQS_DN5	BG42	MEM_CH0_DQSN5/MEM_CH0_DQSNB1	
M_A_DQS_DP6	BB35	MEM_CH0_DQSP6/MEM_CH0_DQSPB2	
M_A_DQS_DN6	BD35	MEM_CH0_DQSN6/MEM_CH0_DQSNB2	
M_A_DQS_DP7	BG36	MEM_CH0_DQSP7/MEM_CH0_DQSPB3	
M_A_DQS_DN7	BH35	MEM_CH0_DQSN7/MEM_CH0_DQSNB3	
M_A_A0	BG50	MEM_CH0_MA0/MEM_CH0_CAB7	
M_A_A1	BG51	MEM_CH0_MA1/MEM_CH0_CAB9	
M_A_A2	BH51	MEM_CH0_MA2/MEM_CH0_CAB5	
M_A_A3	BD41	MEM_CH0_MA3/NCTF_22	
M_A_A4	BE41	MEM_CH0_MA4/NCTF_23	
M_A_A5	BJ52	MEM_CH0_MA5/MEM_CH0_CAA2	
M_A_A6	BG53	MEM_CH0_MA6/MEM_CH0_CAA0	
M_A_A7	BG55	MEM_CH0_MA7/MEM_CH0_CAA3	
M_A_A8	BH53	MEM_CH0_MA8/MEM_CH0_CAA1	
M_A_A9	BG52	MEM_CH0_MA9/MEM_CH0_CAA4	
M_A_A10	BH49	MEM_CH0_MA10/MEM_CH0_CAB6	
M_A_A11	BH55	MEM_CH0_MA11/MEM_CH0_CAA6	
M_A_A12	BG54	MEM_CH0_MA12/MEM_CH0_CAA5	
M_A_A13	BG46	MEM_CH0_MA13/MEM_CH0_CAB0	
M_A_A14	BG56	MEM_CH0_MA14/MEM_CH0_CAA8	
M_A_A15	BG57	MEM_CH0_MA15/MEM_CH0_CAA9	
		MEM_CH0_VREFCA	AR35
		MEM_CH0_VREFDQ	AT34
		MEM_CH0_BA0/MEM_CH0_CAB2	BJ48 M_A_BS0
		MEM_CH0_BA1/MEM_CH0_CAB8	BG49 M_A_BS1
		MEM_CH0_BA2/MEM_CH0_CAA7	BH57 M_A_BS2
		MEM_CH0_ODT0/MEM_CH0_ODTA	AW43 M_A_ODT0
		MEM_CH0_ODT1/MEM_CH0_ODTB	AW41 M_A_ODT1
		MEM_CH0_CAS#/MEM_CH0_CAB1	BH47 M_A_CAS#
		MEM_CH0_WE#/MEM_CH0_CAB4	BG48 M_A_WE#
		MEM_CH0_RAS#/MEM_CH0_CAB3	BG47 M_A_RAS#
		NCTF/MEM_CH0_CS1A#	AT43
		NCTF/MEM_CH0_CS0B#	BB41
		MEM_CH0_CS1#/MEM_CH0_CS1B#	BA41 M_A_CS#1
		MEM_CH0_CS0#/MEM_CH0_CS0A#	AR43 M_A_CS#0
		MEM_CH0_CLKP1/MEM_CH0_CLKP_A	BB48 M_A_CLK1
		MEM_CH0_CLKN1/MEM_CH0_CLKN_A	BD48 M_A_CLK#1
		MEM_CH0_CLKP0/MEM_CH0_CLKP_B	BD45 M_A_CLK0
		MEM_CH0_CLKN0/MEM_CH0_CLKN_B	BE45 M_A_CLK#0
		MEM_CH0_CKE0/MEM_CH0_CKE0A	BH61 M_A_CKE0
		MEM_CH0_CKE1/MEM_CH0_CKE1A	BH60 M_A_CKE1
		NCTF/MEM_CH0_CKE0B	BH58
		NCTF/MEM_CH0_CKE1B	BJ58
		MEM_CH1_RESET#/NCTF_31	AR30
		MEM_CH0_RESET#/NCTF_33	AR34 DDR3_DRAMRST#
		MEM_CH0_DQSP8/NCTF_28	BD47
		MEM_CH0_DQSN8/NCTF_30	BB47
		MEM_CH0_CB7/NCTF_35	BA45
		MEM_CH0_CB6/NCTF_34	BD43
		MEM_CH0_CB5/NCTF_32	AV47
		MEM_CH0_CB4/NCTF_29	AV48
		MEM_CH0_CB3/NCTF_27	AW49
		MEM_CH0_CB2/NCTF_26	BB43
		MEM_CH0_CB1/NCTF_25	AW47
		MEM_CH0_CB0/NCTF_24	AW48

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DY ED501 Do Not Stuff — close to CPU — EMC solution

CPU1C — 3 OF 23 — APL_SOC

BJ26	MEM_CH1_DQ0/MEM_CH1_DQA0		
BG30	MEM_CH1_DQ1/MEM_CH1_DQA1		
BH31	MEM_CH1_DQ2/MEM_CH1_DQA2		
BG31	MEM_CH1_DQ3/MEM_CH1_DQA3		
BH27	MEM_CH1_DQ4/MEM_CH1_DQA4		
BG27	MEM_CH1_DQ5/MEM_CH1_DQA5		
BG26	MEM_CH1_DQ6/MEM_CH1_DQA6		
BJ30	MEM_CH1_DQ7/MEM_CH1_DQA7		
BA30	MEM_CH1_DQ8/MEM_CH1_DQA8		
BB30	MEM_CH1_DQ9/MEM_CH1_DQA9		
BE30	MEM_CH1_DQ10/MEM_CH1_DQA10		
BD30	MEM_CH1_DQ11/MEM_CH1_DQA11		
BE25	MEM_CH1_DQ12/MEM_CH1_DQA12		
BB27	MEM_CH1_DQ13/MEM_CH1_DQA13		
BD25	MEM_CH1_DQ14/MEM_CH1_DQA14		
BD27	MEM_CH1_DQ15/MEM_CH1_DQA15		
BG24	MEM_CH1_DQ16/MEM_CH1_DQA16		
BJ20	MEM_CH1_DQ17/MEM_CH1_DQA17		
BH23	MEM_CH1_DQ18/MEM_CH1_DQA18		
BJ24	MEM_CH1_DQ19/MEM_CH1_DQA19		
BG20	MEM_CH1_DQ20/MEM_CH1_DQA20		
BG21	MEM_CH1_DQ21/MEM_CH1_DQA21		
BH19	MEM_CH1_DQ22/MEM_CH1_DQA22		
BG25	MEM_CH1_DQ23/MEM_CH1_DQA23		
AT27	MEM_CH1_DQ24/MEM_CH1_DQA24		
AW29	MEM_CH1_DQ25/MEM_CH1_DQA25		
AR27	MEM_CH1_DQ26/MEM_CH1_DQA26		
AT23	MEM_CH1_DQ27/MEM_CH1_DQA27		
AV27	MEM_CH1_DQ28/MEM_CH1_DQA28		
AR25	MEM_CH1_DQ29/MEM_CH1_DQA29		
AR23	MEM_CH1_DQ30/MEM_CH1_DQA30		
AW27	MEM_CH1_DQ31/MEM_CH1_DQA31		
		MEM_CH1_DQ32/MEM_CH1_DQB0	BF6
		MEM_CH1_DQ33/MEM_CH1_DQB1	BD10
		MEM_CH1_DQ34/MEM_CH1_DQB2	BE14
		MEM_CH1_DQ35/MEM_CH1_DQB3	BB10
		MEM_CH1_DQ36/MEM_CH1_DQB4	BA14
		MEM_CH1_DQ37/MEM_CH1_DQB5	BB14
		MEM_CH1_DQ38/MEM_CH1_DQB6	BD14
		MEM_CH1_DQ39/MEM_CH1_DQB7	BE8
		MEM_CH1_DQ40/MEM_CH1_DQB8	AV12
		MEM_CH1_DQ41/MEM_CH1_DQB9	BD6
		MEM_CH1_DQ42/MEM_CH1_DQB10	BD5
		MEM_CH1_DQ43/MEM_CH1_DQB11	BB7
		MEM_CH1_DQ44/MEM_CH1_DQB12	AV10
		MEM_CH1_DQ45/MEM_CH1_DQB13	AY9
		MEM_CH1_DQ46/MEM_CH1_DQB14	AY7
		MEM_CH1_DQ47/MEM_CH1_DQB15	BF5
		MEM_CH1_DQ48/MEM_CH1_DQB16	AU2
		MEM_CH1_DQ49/MEM_CH1_DQB17	AT10
		MEM_CH1_DQ50/MEM_CH1_DQB18	AT9
		MEM_CH1_DQ51/MEM_CH1_DQB19	AU1
		MEM_CH1_DQ52/MEM_CH1_DQB20	AY5
		MEM_CH1_DQ53/MEM_CH1_DQB21	AV5
		MEM_CH1_DQ54/MEM_CH1_DQB22	AV6
		MEM_CH1_DQ55/MEM_CH1_DQB23	AV7
		MEM_CH1_DQ56/MEM_CH1_DQB24	AY2
		MEM_CH1_DQ57/MEM_CH1_DQB25	BD2
		MEM_CH1_DQ58/MEM_CH1_DQB26	BD1
		MEM_CH1_DQ59/MEM_CH1_DQB27	BE2
		MEM_CH1_DQ60/MEM_CH1_DQB28	AW1
		MEM_CH1_DQ61/MEM_CH1_DQB29	AW2
		MEM_CH1_DQ62/MEM_CH1_DQB30	AY3
		MEM_CH1_DQ63/MEM_CH1_DQB31	BG2

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CPU1D — 4 OF 23 — APL_SOC

BG28	MEM_CH1_DQSP0/MEM_CH1_DQSPA0		
BH29	MEM_CH1_DQSN0/MEM_CH1_DQSNA0		
BD29	MEM_CH1_DQSP1/MEM_CH1_DQSPA1		
BB29	MEM_CH1_DQSN1/MEM_CH1_DQSNA1		
BJ22	MEM_CH1_DQSP2/MEM_CH1_DQSPA2		
BG22	MEM_CH1_DQSN2/MEM_CH1_DQSNA2		
AV25	MEM_CH1_DQSP3/MEM_CH1_DQSPA3		
AW25	MEM_CH1_DQSN3/MEM_CH1_DQSNA3		
BB12	MEM_CH1_DQSP4/MEM_CH1_DQSPB0		
BD12	MEM_CH1_DQSN4/MEM_CH1_DQSNB0		
BB5	MEM_CH1_DQSP5/MEM_CH1_DQSPB1		
BB6	MEM_CH1_DQSN5/MEM_CH1_DQSNB1		
AT5	MEM_CH1_DQSP6/MEM_CH1_DQSPB2		
AT6	MEM_CH1_DQSN6/MEM_CH1_DQSNB2		
BC2	MEM_CH1_DQSP7/MEM_CH1_DQSPB3		
BB1	MEM_CH1_DQSN7/MEM_CH1_DQSNB3		
BG9	MEM_CH1_MA0/MEM_CH1_CAB7		
BG10	MEM_CH1_MA1/MEM_CH1_CAB9		
BH9	MEM_CH1_MA2/MEM_CH1_CAB5		
BD16	MEM_CH1_MA3/NCTF_1		
BB16	MEM_CH1_MA4/NCTF_2		
BG11	MEM_CH1_MA5/MEM_CH1_CAA2		
BJ12	MEM_CH1_MA6/MEM_CH1_CAA0		
BG14	MEM_CH1_MA7/MEM_CH1_CAA3		
BG12	MEM_CH1_MA8/MEM_CH1_CAA1		
BH11	MEM_CH1_MA9/MEM_CH1_CAA4		
BG7	MEM_CH1_MA10/MEM_CH1_CAB6		
BH13	MEM_CH1_MA11/MEM_CH1_CAA6		
BG13	MEM_CH1_MA12/MEM_CH1_CAA5		
BH3	MEM_CH1_MA13/MEM_CH1_CAB0		
BG15	MEM_CH1_MA14/MEM_CH1_CAA8		
BG16	MEM_CH1_MA15/MEM_CH1_CAA9		
		MEM_CH1_VREFDQ	AT30
		MEM_CH1_VREFCA	AR29
		MEM_CH1_BA0/MEM_CH1_CAB2	BH6
		MEM_CH1_BA1/MEM_CH1_CAB8	BG8
		MEM_CH1_BA2/MEM_CH1_CAA7	BH15
		MEM_CH1_RAS#/MEM_CH1_CAB3	BJ6
		MEM_CH1_CAS#/MEM_CH1_CAB1	BH4
		MEM_CH1_WE#/MEM_CH1_CAB4	BH7
		MEM_CH1_ODT0/MEM_CH1_ODTA	AW19
		MEM_CH1_ODT1/MEM_CH1_ODTB	AV16
		MEM_CH1_CLKP1/MEM_CH1_CLKP_A	BB21
		MEM_CH1_CLKN1/MEM_CH1_CLKN_A	BD21
		MEM_CH1_CLKP0/MEM_CH1_CLKP_B	BD19
		MEM_CH1_CLKN0/MEM_CH1_CLKN_B	BE19
		MEM_CH1_CKE0/MEM_CH1_CKE0A	BG18
		MEM_CH1_CKE1/MEM_CH1_CKE1A	BG17
		NCTF/MEM_CH1_CKE0B	BH17
		NCTF/MEM_CH1_CKE1B	BJ16
		MEM_CH1_CS0#/MEM_CH1_CS0A#	BD17
		MEM_CH1_CS1#/MEM_CH1_CS1B#	AW17
		NCTF/MEM_CH1_CS0B#	AV17
		NCTF/MEM_CH1_CS1A#	BB17
		MEM_CH1_DQSN8/NCTF_9	BE23
		MEM_CH1_DQSP8/NCTF_5	BD23
		MEM_CH1_CB0/NCTF_3	AR21
		MEM_CH1_CB1/NCTF_4	AT21
		MEM_CH1_CB6/NCTF_11	BA23
		MEM_CH1_CB3/NCTF_7	AW23
		MEM_CH1_CB4/NCTF_8	BA19
		MEM_CH1_CB5/NCTF_10	AW19
		MEM_CH1_CB7/NCTF_12	BB23
		MEM_CH1_CB2/NCTF_6	AW22

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDR)

Size	Document Number	Rev
Custom	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 5 of 109

SSID = CPU PDG P54

CPU1V

APL_SOC

22 OF 23

APOLLO-LAKE-GP-U

3D3V_USB
1D24V_USB2
1V_CPU_VNN
3D3V_S5
1D24V_AUD_ISH_PLL
1D24V_MPHY
1D24V_GLML
1D05V_S0
1D05V_IO_3PHASEIO
1D05V_FHV1
1D05V_FHV0
1D05V_FUSE

PG601 Do Not Stuff
PG602 Do Not Stuff
PG603 Do Not Stuff
PG604 Do Not Stuff
PG605 Do Not Stuff
PG607 Do Not Stuff
PG608 Do Not Stuff
PG609 Do Not Stuff
PG610 Do Not Stuff

AJ25	VCC_3P3V_A_6	
AK25	VCC_3P3V_A_5	
AG20	VDD2_1P24_USB2	
AJ37	VNN_SVID	
AJ39	VNN_SVID	
AJ41	VNN_SVID	
AJ42	VNN_SVID	
AJ46	VNN_SVID	
AK37	VNN_SVID	
AK39	VNN_SVID	
AK41	VNN_SVID	
AK42	VNN_SVID	
AK44	VNN_SVID	
AK46	VNN_SVID	
AM44	VNN_SVID	
AJ44	RSVD_11	
AA42	VCC_3P3V_A_4	
Y44	VCC_3P3V_A_1	
V46	VCC_3P3V_A_2	
V44	VCC_3P3V_A_3	
AC41	VCC_3P3V_A_7	
AJ20	VDD2_1P24_AUD_ISH_PLL	
AJ22	VDD2_1P24_AUD_ISH_PLL	
AE18	VDD2_1P24_MPHY	
AE20	VDD2_1P24_MPHY	
AE22	VDD2_1P24_MPHY	
AG22	VDD2_1P24_MPHY	
BJ61	RSVD_7	
AK20	VDD2_1P24_GLM	
AC20	RSVD_10	
AC22	RSVD_9	
AA18	VDD2_1P24_DSI_CSI1	
AA20	VDD2_1P24_DSI_CSI2	
AK22	VDD2_1P24_AUD_ISH_PLL	
AA22	VCCRAM_1P05_IO	
AC23	VCCRAM_1P05_IO	
V18	VCCRAM_1P05_IO	
Y18	VCCRAM_1P05_IO	
Y20	VCCRAM_1P05_IO	
P16	VCC_1P05V	
T15	VCC_1P05V	
T13	VCC_1P05V	
AA23	VCCRAM_1P05_IO	

VNN Max 3.3A

3D3V_S5 Max 0.15A

VCCIOA Max 1.5A
Tie to VNN for LPDDR3/DDR3L
Tie to VDDQ for for LPDDR4.

D4	NCTF_18	
T51	NCTF_19	
L14	NCTF_17	
E3	NCTF_21	
AM37	VDD2_1P24_GLM	1D24V_GLML
AM20	VDD2_1P24_GLM	
AM28	VDD2_1P24_GLM	
AA28	VCC_VCGI_43	
AA30	VCC_VCGI_41	
AA32	VCC_VCGI_40	
AC28	VCC_VCGI_39	
AC30	VCC_VCGI_38	
AC32	VCC_VCGI_37	
AE28	VCC_VCGI_36	
AE30	VCC_VCGI_34	
AE32	VCC_VCGI_62	
AG28	VCC_VCGI_60	1V_CPU_VCGI
AG30	VCC_VCGI_58	
AG32	VCC_VCGI_56	
AJ28	VCC_VCGI_54	
AJ30	VCC_VCGI_52	
AJ32	VCC_VCGI_50	
AK28	VCC_VCGI_48	
AK30	VCC_VCGI_46	
AK32	VCC_VCGI_44	
AM30	VCC_VCGI_42	
E29	VCC_VCGI_63	
E37	VCC_VCGI_61	
U28	VCC_VCGI_59	
U30	VCC_VCGI_57	
U32	VCC_VCGI_55	
V28	VCC_VCGI_53	
V30	VCC_VCGI_51	
V32	VCC_VCGI_49	
Y28	VCC_VCGI_47	
Y30	VCC_VCGI_45	
Y32	VCC_VCGI_35	
E50	VCC_VCGI_64	
R19	NCTF_20	
AA44	VCCRTC_3P3V	3D3V_RTC_AUX
AM23	VCCIOA	1V_CPU_VNN
AM25	VCCIOA	
AM41	VCCIOA	
AM42	VCCIOA	
BJ62	RSVD_8	
V49	RSVD_12	

C601 1 SC1U10V2KX-1GP

C602 2 SC1U10V2KX-1GP

AM28 IS INTERNAL SHORTED ON APL PACKAGE TO VDD2

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5.5.1 Voltage and Current Specifications

Table 5-3. Apollo Lake SoC Power Rail DC Specification and Iccmax

Power Type	Voltage Range (V)	Voltage Tolerance (AC+DC+Ripple)	Power Well Description	Iccmax (A)
VCC_VCGI	0V, 0.45~1.3	**With AVP[1]:** DC Load Line (DCLL) = 6 mOhms Ripple at Iccmax = +/-15mV TOB[2] Iccmax = +/-20mV Overshoot voltage (max) = 100mV Overshoot duration (max) = 50 µs **Without AVP[1]:** Voltage Tolerance = +35mV/-16mV Overshoot voltage (max) = 100mV Overshoot duration (max) = 50 µs	Variable voltage supply to CPU and Graphics Core and ISP logic. SVID and I2C VID are voltage control interface supported.	21
VNN_SVID	0V, 0.45~1.3	+/-50mV	Variable voltage supply to other (non core) logic	3.3
VCCIOA	0V, 0.45~1.3	+/-50mV	***Notes:*** 1. Please tie VCCIOA to VNN_SVID for DDR3L and LPDDR3 designs 2. Please tie VCCIOA to VDDQ for LPDDR4 designs	1.5
VCCRAM_V1P05	1.05	+/-5%	Fixed voltage rail for SRAM and I/O Logic	2.7
VCCRAM_1P05	1.05	+/-5%	Fixed voltage rail for SRAM and I/O Logic	
VCCRAM_1P05_IO	1.05	+/-5%	Fixed voltage rail for SRAM and I/O Logic	
VCCRAM_1P05_INT	1.05	+/-5%	Fixed voltage rail for SRAM and I/O Logic	
VCC_V1P24_1P35_A	1.24V or 1.35V	+/- 5%	Fixed voltage rail for SoC L2, I/O Logic and PLLs	1.8
VCC_V1P24_A	1.24	+/-5%	Fixed voltage rail for MIPI* I/Os	0.13
VCC_V1P8V_A	1.8	+/-5%	Fixed voltage rail for all GPIOs	0.4
VDDQ	1.35 (DDR3L)	+/-5%	Fixed voltage rail for DDR3L PHY	2.8 (excluding DRAM)
	1.2 (LPDDR3)	+8.3%/-5%	Fixed voltage rail for LPDDR3 PHY	
	1.1 (LPDDR4)	+6/-4%[3]	Fixed voltage rail for LPDDR4 PHY	
VCC_3P3V_A	3.3	+/-5%	Fixed voltage rail for GPIO, I/O logic and USB 2 PHY	0.15
VCC_RTC_3P3V	2~3.47	N/A	Fixed Voltage rail for RTC (Real Time Clock)	7 µA

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Title: **CPU (CFG)**
Size: Custom
Document Number: **Ironhide_APL**
Rev: **-1M**
Date: Wednesday, September 21, 2016
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SSID = CPU

CPU1W

APL_SOC

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1D05V_S0

1D8V_S5

1D8V_S5
Max 0.4A

1D05V_S0
Max 2.7A

VDDQ
Max 2.8A

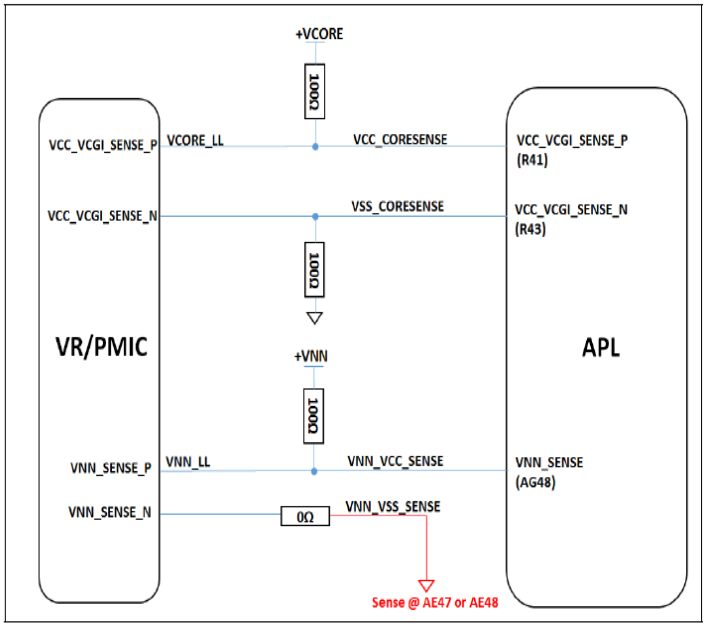
46 VSSGI_SENSE
46 VCCGI_SENSE
46 VNNCORE_SENSE

E6	NCTF_16	
AA25	VCCRAM_1P05	
AC25	VCCRAM_1P05	
AE25	VCCRAM_1P05	
U22	VCCRAM_1P05	
U23	VCCRAM_1P05	
V22	VCCRAM_1P05	
V23	VCCRAM_1P05	
V25	VCCRAM_1P05	
Y23	VCCRAM_1P05	
U20	VCCRAM_1P05	
U25	VCCRAM_1P05	
Y25	VCCRAM_1P05	
AM32	RSVD_4	
AN32	RSVD_6	
D1	RSVD_2	
BG63	RSVD_1	
V48	RSVD_3	
VSSGI_SENSE R43	VCC_VCGI_SENSE_N	
VCCGI_SENSE R41	VCC_VCGI_SENSE_P	
VNNCORE_SENSE AG48	VNN_SENSE	
AN18	VDDQ_15	
AN20	VDDQ_14	
AN22	VDDQ_13	
1D35V_S3 AN23	VDDQ_12	
AN41	VDDQ_11	
AN42	VDDQ_10	
AN44	VDDQ_9	
AN46	VDDQ_8	
AR17	VDDQ_6	
AR47	VDDQ_7	
AT13	VDDQ_5	
AT17	VDDQ_4	
AT47	VDDQ_3	
AT51	VDDQ_2	
AV14	VDDQ_1	
AV50	VDDQ_16	
F23	NCTF_14	
E23	NCTF_15	
BJ3	RSVD_5	

AE42	VCC_1P8V_A_1	
AE44	VCC_1P8V_A_2	
AA46	VCC_1P8V_A_3	1D8V_S5
AC42	VCC_1P8V_A_4	
AC44	VCC_1P8V_A_5	
AC46	VCC_1P8V_A_6	
AE46	VCC_1P8V_A_7	
AG25	VCC_1P8V_A_8	
R17	NCTF_13	
F29	VCC_VCGI_32	1V_CPU_VCGI
E35	VCC_VCGI_31	
AK34	VCC_VCGI_33	
E45	VCC_VCGI_30	
AC37	VCC_VCGI_27	
AE36	VCC_VCGI_24	
AE37	VCC_VCGI_21	
AG36	VCC_VCGI_18	
E43	VCC_VCGI_15	
E48	VCC_VCGI_12	
R45	VCC_VCGI_9	
R47	VCC_VCGI_7	
U36	VCC_VCGI_6	
U37	VCC_VCGI_3	
U39	VCC_VCGI_1	
U41	VCC_VCGI_28	
U42	VCC_VCGI_25	
U44	VCC_VCGI_22	
U46	VCC_VCGI_19	
U47	VCC_VCGI_16	
U48	VCC_VCGI_13	
V36	VCC_VCGI_10	
V37	VCC_VCGI_8	
V39	VCC_VCGI_5	
V41	VCC_VCGI_4	
Y36	VCC_VCGI_2	
Y37	VCC_VCGI_29	
Y39	VCC_VCGI_26	
Y41	VCC_VCGI_23	
AC36	VCC_VCGI_20	
AA36	VCC_VCGI_17	
AA37	VCC_VCGI_14	
AA39	VCC_VCGI_11	

APOLLO-LAKE-GP-U

Figure 3-4. VCGI, VSS, VNN Sense Guideline



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Title: CPU (VCC_CORE)

Size: Custom | Document Number: Ironhide_APL | Rev: -1M

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SSID = CPU

HDMI

57 HDMI_CLK_CPU
57 HDMI_DATA_CPU
57 HDMI_DATA_CPU_P2
57 HDMI_DATA_CPU_N2
57 HDMI_DATA_CPU_P1
57 HDMI_DATA_CPU_N1
57 HDMI_DATA_CPU_P0
57 HDMI_DATA_CPU_N0
57 HDMI_DATA_CPU_P3
57 HDMI_DATA_CPU_N3
57 HDMI_DET_CPU

eDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_P1
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
24 eDP_BLEN_CPU
55 eDP_BLCTRL_CPU
55 eDP_VDDEN_CPU
18,55 eDP_HPD_CPU

HDMI

1D8V_S0 — RN888 — DY — Do Not Stuff

Vth(max)=1.1V

Q804 — PJT138KA-GP — 075.00138.0A7C

HDMI_CLK_CPU → HDMI_CLK_CPU_R → B49 DDI0_DDC_SCL
HDMI_DATA_CPU → HDMI_DATA_CPU_R → C49 DDI0_DDC_SDA
A54 DDI1_DDC_SCL
C54 DDI1_DDC_SDA

1.8V

RN801 — SRN2K2J-1-GP — 3D3V_S0

eDP_AUX_CPU_P → AH10 EDP_AUXP
eDP_AUX_CPU_N → AH9 EDP_AUXN
R802 — 402R2F-GP
EDP_RCOMP_N → AG5 EDP_RCOMP_N
EDP_RCOMP_P → AG6 EDP_RCOMP_P

eDP_TX_CPU_P0 → AG7 EDP_TXP_0
eDP_TX_CPU_N0 → AG9 EDP_TXN_0
eDP_TX_CPU_P1 → AG12 EDP_TXP_1
eDP_TX_CPU_N1 → AG10 EDP_TXN_1
AC6 EDP_TXP_2
AC5 EDP_TXN_2
AC7 EDP_TXP_3
AC9 EDP_TXN_3

1.05V

EDP

CPU1E — APL_SOC — 5 OF 23 — APOLLO-LAKE-GP-U

DDI0_TXP_0 AK3 HDMI_DATA_CPU_P2
DDI0_TXN_0 AK2 HDMI_DATA_CPU_N2
DDI0_TXP_1 AM3 HDMI_DATA_CPU_P1
DDI0_TXN_1 AM2 HDMI_DATA_CPU_N1
DDI0_TXP_2 AH3 HDMI_DATA_CPU_P0
DDI0_TXN_2 AH2 HDMI_DATA_CPU_N0
DDI0_TXP_3 AL2 HDMI_DATA_CPU_P3
DDI0_TXN_3 AL1 HDMI_DATA_CPU_N3
DDI0_RCOMP_P AG1 DDI0_RCOMP_P — R801 — DY — Do Not Stuff
DDI0_RCOMP_N AG2 DDI0_RCOMP_N
DDI0_AUXP AM16
DDI0_AUXN AM15

only for DP

DDI1_AUXP AK16
DDI1_AUXN AK15
DDI1_TXP_0 AF2
DDI1_TXN_0 AF3
DDI1_TXP_1 AD3
DDI1_TXN_1 AD2
DDI1_TXP_2 AC1
DDI1_TXN_2 AC2
DDI1_TXP_3 AB3
DDI1_TXN_3 AB2

1.05V

(1)Notice: AB2/AB3

eDP® Channel

EDP_TXP_[3:0] EDP_TXN_[3:0] AG7, AG9, AG12, AG10 AC6, AC5, AC7, AC9
EDP_AUXP EDP_AUXN AH9, AH10
PNL0_VDDEN C47 — Panel Power Control Circuit
PNL0_BKLTEN B47 — Panel Backlight Power Control Circuit
PNL0_BKLTCTL C46 — Panel Backlight Control Circuit
HV_DDI2_HPD P48 — HPD Circuit
EDP_RCOMP_P AG6
EDP_RCOMP_N AG5 — 402 ohm/1%
ATL SoC

eDP Connector

CPU1F — APL_SOC — 6 OF 23 — APOLLO-LAKE-GP-U

MDSI_A_DP_0 AP12
MDSI_A_DN_0 AP10
MDSI_A_DP_1 AR2
MDSI_A_DN_1 AR1
MDSI_A_DP_2 AP15
MDSI_A_DN_2 AP13
MDSI_A_DP_3 AP6
MDSI_A_DN_3 AP5
MDSI_A_CLKP AP2
MDSI_A_CLKN AP3

1.24V

MDSI_C_DP_0 AK7
MDSI_C_DN_0 AK6
MDSI_C_DP_1 AM5
MDSI_C_DN_1 AM6
MDSI_C_DP_2 AM12
MDSI_C_DN_2 AM10
MDSI_C_DP_3 AK13
MDSI_C_DN_3 AM13
MDSI_C_CLKP AM9
MDSI_C_CLKN AM7

1.24V

MIPI_I2C_SDA B51
MIPI_I2C_SCL C51
GPIO_199/HV_DDI1_HPD A50
GPIO_200/HV_DDI0_HPD C50
MDSI_A_TE M45
MDSI_C_TE M43

1.8V

PNL0_VDDEN C47 → eDP_VDDEN_CPU
PNL0_BKLTEN B47 → eDP_BLEN_CPU
PNL0_BKLTCTL C46
PNL1_VDDEN C52
PNL1_BKLTEN B53
PNL1_BKLTCTL C53

1.8V

close to connector

HDMI_DET_CPU → R815 100KR2J-4-GP
Q803 — 2N7002K-2-GP — 84.2N702.J31 — 2ND = 084.27002.0L31 — 3rd = 084.06587.0031
R844 10KR2J-L-GP → HDMI_DET_CPU_RR

1D8V_S0 — R804 Do Not Stuff — DY
R803 1MR2J-L3-GP

1D8V_S0 — R805 Do Not Stuff — DY
R827 Do Not Stuff — DY

1D8V_S0 3D3V_S0 — RN827 SRN2K2J-1-GP
L_BKLT_CTRL_B
eDP_BLCTRL_CPU_RR → Q801 LMBT3904LT1G-GP → eDP_BLCTRL_CPU
84.T3904.H11 — 2nd = 84.T3904.K11 — 3rd = 84.T3904.C11

DDI0_RCOMP_P/N	O	V1P05	Display PHY	Port 0/1: This signal is used for pre-driver slew rate compensation. **Note:** The SoC will use the eDP_RCOMP value for DDI Port 0/1 as well. Please ensure that the eDP_RCOMP pin is populated with the correct value. There is no need to have this DDI0_RCOMP on the platform.

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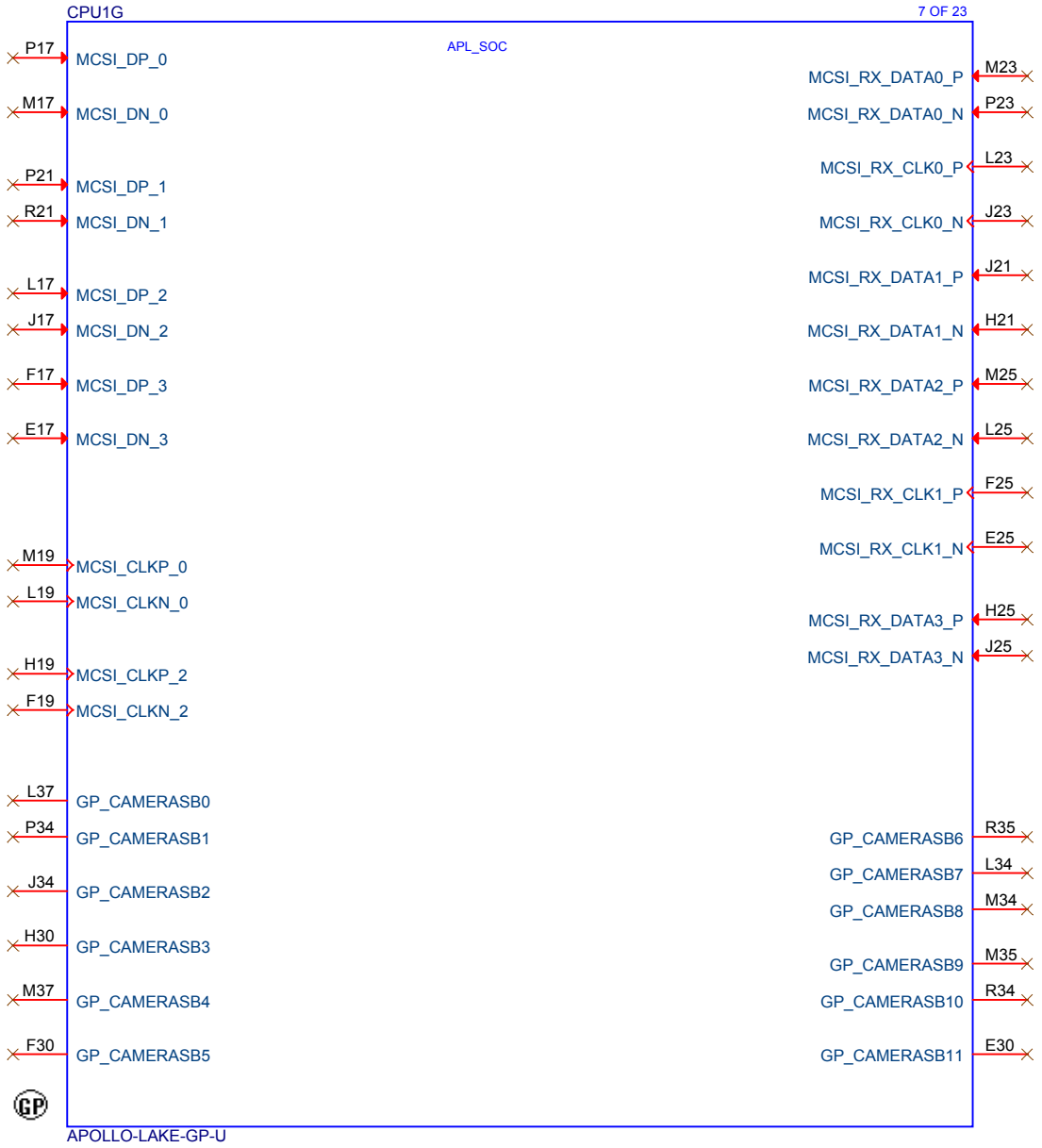
Title: CPU (DDI/EDP/GPIO)
Size: A2 — Document Number: Ironhide_APL — Rev: -1M
Date: Wednesday, September 21, 2016 — Sheet 8 of 106

SSID = CPU



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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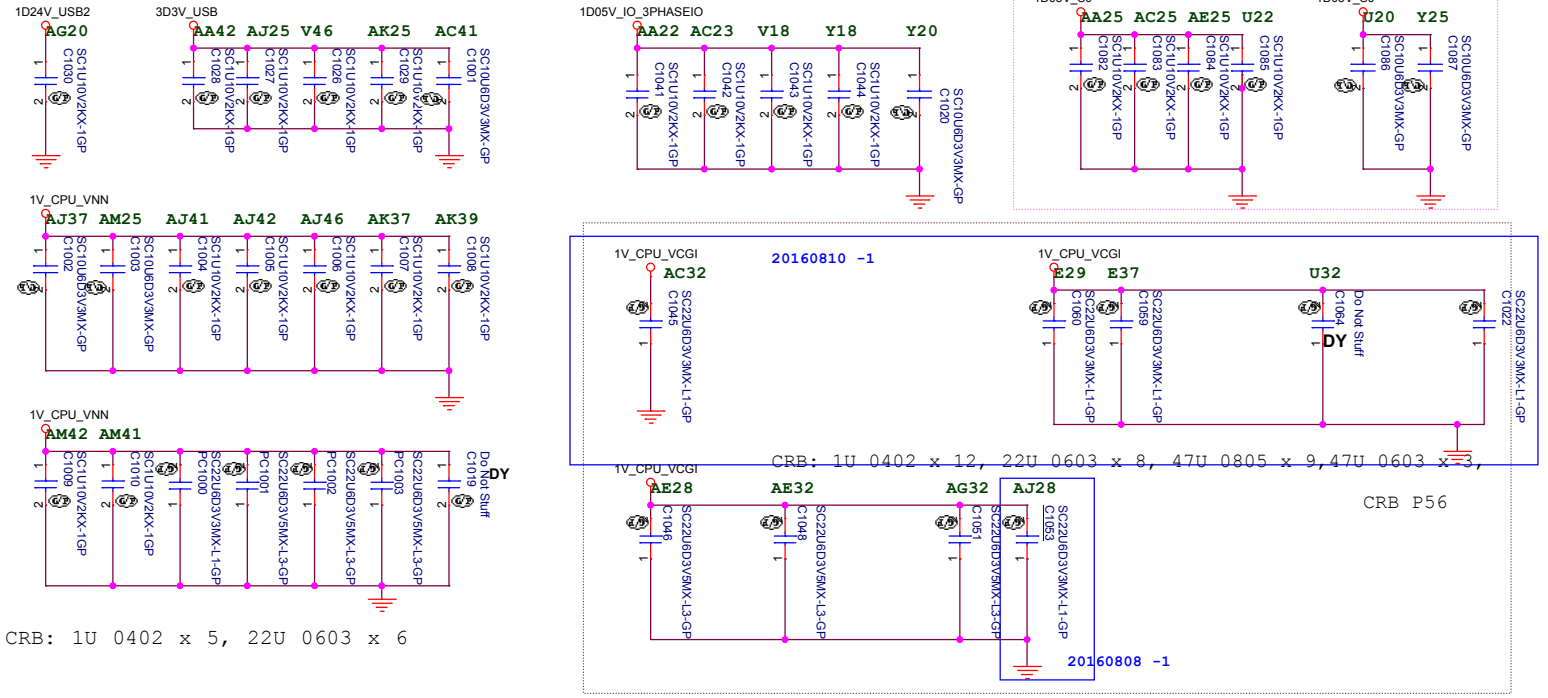
Title: **CPU (VSS)**

Size	Document Number	Rev
A4	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 9 of 106

SSID = CPU



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Power CAP1)

Size: Custom | Document Number: Ironhide_APL | Rev: -1M

Date: Wednesday, September 21, 2016 | Sheet 10 of 106

SSID = CPU

Blanking

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Title: CPU (Power CAP2)

Size	Document Number	Rev
A4	Ironhide_APL	-1M

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SSID = MEMORY

Reverse type

For Intel Recommend Close to DM1

5 M_A_A[15:0]
5 M_A_DQ[63:0]
5 M_A_DQS_DN[7:0]
5 M_A_DQS_DP[7:0]
5 M_A_ODT0
5 M_A_ODT1
5 M_A_BS0
5 M_A_BS1
5 M_A_BS2
5 M_A_RAS#
5 M_A_WE#
5 M_A_CAS#
5 M_A_CS#0
5 M_A_CS#1
5 M_A_CKE0
5 M_A_CKE1
5 M_A_CLK0
5 M_A_CLK#0
5 M_A_CLK1
5 M_A_CLK#1
17,69 PCH_SMB_DATA
17,69 PCH_SMB_CLK
5 DDR3_DRAMRST#

1D35V_S3
R1255 3K65R2F-1-GP
M_VREFCA_DM0
R1245 3K65R2F-1-GP
C1226 SCD1U16V2KX-L-GP

1D35V_S3
R1210 3K65R2F-1-GP
M_VREFDQ_DM0
R1213 3K65R2F-1-GP
C1203 SCD1U16V2KX-L-GP

0D675V_VREF_S0
Layout Note:
Place these capsclose to VTT1 and VTT2.
C1268 DY Do Not Stuff
C1270 DY Do Not Stuff
C1266 SC10U6D3V3MX-L-GP

1D35V_S3
RN1207
DDR3_DRAMRST#
M_A_DRAMRST#_R
SRN1KJ-7-GP
0D675V_VREF_S0
close to DM1
ED1201 DY Do Not Stuff
EMC solution

DM1
DDR3-204P-262-GP-U
SKT_DDR_204P_SMD

M_A_A0	98	A0	
M_A_A1	97	A1	
M_A_A2	96	A2	
M_A_A3	95	A3	
M_A_A4	92	A4	
M_A_A5	91	A5	
M_A_A6	90	A6	
M_A_A7	86	A7	
M_A_A8	89	A8	
M_A_A9	85	A9	
M_A_A10	107	A10/AP	
M_A_A11	84	A11	
M_A_A12	83	A12	
M_A_A13	119	A13	
M_A_A14	80	A14	
M_A_A15	78	A15	
M_A_BS2	79	A16/BA2	
M_A_BS0	109	BA0	
M_A_BS1	108	BA1	
NP1		NP1	
NP2		NP2	
M_A_RAS#	110	RAS#	
M_A_WE#	113	WE#	
M_A_CAS#	115	CAS#	
M_A_CS#0	114	CS0#	
M_A_CS#1	121	CS1#	
M_A_CKE0	73	CKE0	
M_A_CKE1	74	CKE1	
M_A_CLK0	101	CK0	
M_A_CLK#0	103	CK0#	
M_A_CLK1	102	CK1	
M_A_CLK#1	104	CK1#	
PCH_SMB_DATA	200	SDA	
PCH_SMB_CLK	202	SCL	
DIMM1_EVENT#	198	EVENT#	
	199	VDDSPD	
DIMM1_SA0	197	SA0	
DIMM1_SA1	201	SA1	
	77	NC#1	
	122	NC#2	
	125	NC#TEST	
M_A_DQ14	5	DQ0	DQ1
M_A_DQ13	7	DQ1	
M_A_DQ12	15	DQ2	
M_A_DQ11	17	DQ3	
M_A_DQ10	4	DQ4	
M_A_DQ9	6	DQ5	
M_A_DQ15	16	DQ6	
M_A_DQ8	18	DQ7	
M_A_DQ1	21	DQ8	DQ0
M_A_DQ6	23	DQ9	
M_A_DQ4	33	DQ10	
M_A_DQ7	35	DQ11	
M_A_DQ5	22	DQ12	
M_A_DQ0	24	DQ13	
M_A_DQ2	34	DQ14	
M_A_DQ3	36	DQ15	
M_A_DQ21	39	DQ16	DQ2
M_A_DQ16	41	DQ17	
M_A_DQ17	51	DQ18	
M_A_DQ19	53	DQ19	
M_A_DQ22	40	DQ20	
M_A_DQ20	42	DQ21	
M_A_DQ18	50	DQ22	
M_A_DQ23	52	DQ23	
M_A_DQ31	57	DQ24	DQ3
M_A_DQ25	59	DQ25	
M_A_DQ27	67	DQ26	
M_A_DQ28	69	DQ27	
M_A_DQ24	56	DQ28	
M_A_DQ26	58	DQ29	
M_A_DQ29	68	DQ30	
M_A_DQ30	70	DQ31	
M_A_DQ46	129	DQ32	DQ5
M_A_DQ45	131	DQ33	
M_A_DQ47	141	DQ34	
M_A_DQ42	143	DQ35	
M_A_DQ40	130	DQ36	
M_A_DQ44	132	DQ37	
M_A_DQ43	140	DQ38	
M_A_DQ41	142	DQ39	
M_A_DQ60	147	DQ40	DQ4
M_A_DQ56	149	DQ41	
M_A_DQ57	157	DQ42	
M_A_DQ63	159	DQ43	
M_A_DQ61	146	DQ44	
M_A_DQ62	148	DQ45	
M_A_DQ58	158	DQ46	
M_A_DQ59	160	DQ47	DQ7
M_A_DQ51	163	DQ48	
M_A_DQ52	165	DQ49	
M_A_DQ50	175	DQ50	
M_A_DQ49	177	DQ51	
M_A_DQ54	164	DQ52	
M_A_DQ53	166	DQ53	
M_A_DQ55	174	DQ54	
M_A_DQ48	176	DQ55	DQ6
M_A_DQ39	181	DQ56	
M_A_DQ37	183	DQ57	
M_A_DQ32	191	DQ58	
M_A_DQ36	193	DQ59	
M_A_DQ34	180	DQ60	
M_A_DQ33	182	DQ61	
M_A_DQ35	192	DQ62	
M_A_DQ38	194	DQ63	
M_A_DQS_DN1	10	DQS0#	
M_A_DQS_DN0	27	DQS1#	
M_A_DQS_DN2	45	DQS2#	
M_A_DQS_DN3	63	DQS3#	
M_A_DQS_DN5	135	DQS4#	
M_A_DQS_DN7	152	DQS5#	
M_A_DQS_DN6	169	DQS6#	
M_A_DQS_DN4	186	DQS7#	
M_A_DQS_DP1	12	DQS0	
M_A_DQS_DP0	29	DQS1	
M_A_DQS_DP2	47	DQS2	
M_A_DQS_DP3	64	DQS3	
M_A_DQS_DP5	137	DQS4	
M_A_DQS_DP7	154	DQS5	
M_A_DQS_DP6	171	DQS6	
M_A_DQS_DP4	188	DQS7	
M_A_ODT0	116	ODT0	
M_A_ODT1	120	ODT1	
M_VREFCA_DM0	126	VREF_CA	
M_VREFDQ_DM0	1	VREF_DQ	
M_A_DRAMRST#_R	30	RESET#	
0D675V_VREF_S0	203	VTT1	
	204	VTT2	
VDD1	75		
VDD2	76		
VDD3	81		
VDD4	82		
VDD5	87		
VDD6	88		
VDD7	93		
VDD8	94		
VDD9	99		
VDD10	100		
VDD11	105		
VDD12	106		
VDD13	111		
VDD14	112		
VDD15	117		
VDD16	118		
VDD17	123		
VDD18	124		
VSS	2		
VSS	3		
VSS	8		
VSS	9		
VSS	13		
VSS	14		
VSS	19		
VSS	20		
VSS	25		
VSS	26		
VSS	31		
VSS	32		
VSS	37		
VSS	38		
VSS	43		
VSS	44		
VSS	48		
VSS	49		
VSS	54		
VSS	55		
VSS	60		
VSS	61		
VSS	65		
VSS	66		
VSS	71		
VSS	72		
VSS	127		
VSS	128		
VSS	133		
VSS	134		
VSS	138		
VSS	139		
VSS	144		
VSS	145		
VSS	150		
VSS	151		
VSS	155		
VSS	156		
VSS	161		
VSS	162		
VSS	167		
VSS	168		
VSS	172		
VSS	173		
VSS	176		
VSS	179		
VSS	184		
VSS	185		
VSS	189		
VSS	190		
VSS	195		
VSS	196		
VSS	205		
VSS	206		

62.10024.S21
2nd = 62.10024.M31
3rd = 62.10024.Q61
4th = 62.10017.X41

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

1D35V_S3
R1215 Do Not Stuff
R1214 Do Not Stuff
3D3V_S0
C1208 DY Do Not Stuff
C1207 SCD1U16V2KX-L-GP
Temperature event pin
TP1203 Do Not Stuff

Layout Note:
Place these Caps near SO-DIMMA.

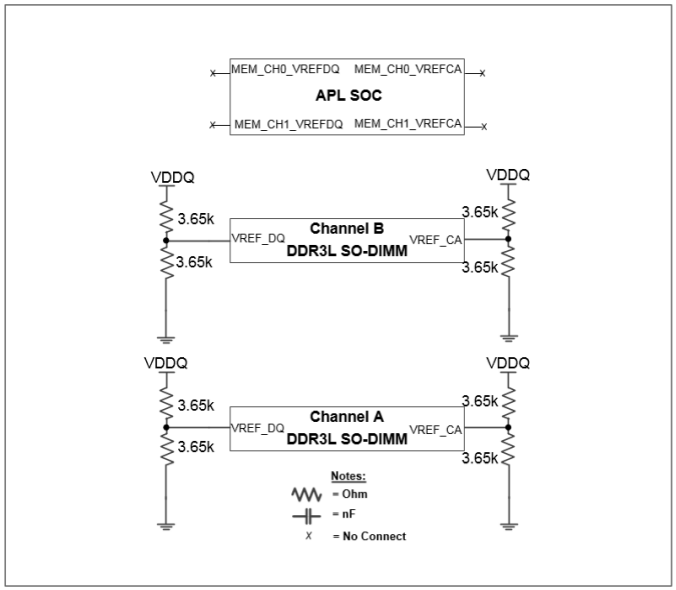
SODIMM A DECOUPLING
1D35V_S3
C1277 C1262 C1263 C1264 C1265 C1275 C1278 C1243
SC10U6D3V3MX-L-GP
DY Do Not Stuff
C1272 C1269 C1273 C1267
SC1U10V2KX-1GP

CRB p201
VTT: 1U 0402 x 4, 10U 0603 x 2
VDD: 0.1U 0402 x 8, 10U 0603 x 8, 330U 0805 x 1

DDR3L Decoupling Recommendation for SODIMM

Memory Configuration	Power Domain	Decoupling Location	Quantity X uF (Size)	Notes
DDR3L SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
			16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	2x - 4x 0.1µF (0402)	
	VTT	On the Vtt island	1x 22µF (0603) or 2x 10µF (0603)	3
				3

SODIMM DRAM_VREF Generation Example Circuit



NOTE: APL SoC VREF outputs can be left No Connect for DDR3L SODIMM

EMMC

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LPDDR3-RAM1 & 2
Size: A2
Document Number: Ironhide_APL
Rev: -1M
Date: Wednesday, September 21, 2016
Sheet 12 of 106

SSID = MEMORY

Blanking

EMMC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LPDDR3-RAM1 & 2*

Size: Custom | Document Number: Ironhide_APL | Rev: -1M

Date: Wednesday, September 21, 2016 | Sheet 13 of 106

SSID = CPU

Blanking

EMMC

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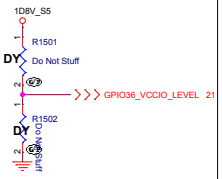
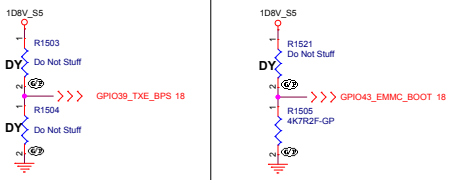
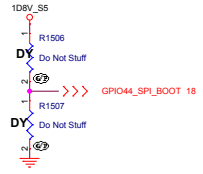
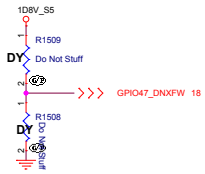
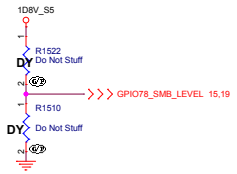
Taipei Hsien 221, Taiwan, R.O.C.

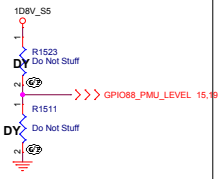
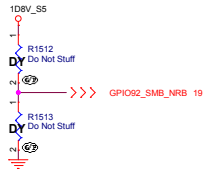
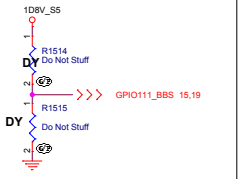
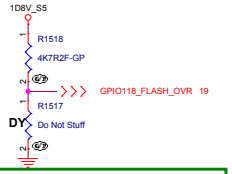
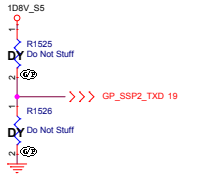
Title: *(Reserved)*

Size	Document Number	Rev
A4	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 14 of 106

SSID = STRAP

GPIO	GPIO_36	GPIO_39	GPIO_43	GPIO_44	GPIO_47	GPIO_78
Schematic						
High	VCCIO used for B-step	enable CSE ROM bypass	enable EMMC Boot Weak internal pull-up	default (allow SPI as a boot source) Weak internal pull-up	force DNX FW Load	Weak internal pull-up SMBus 1.8V mode select
Low	default (A-step) Weak internal pull-down	default (disable bypass) Weak internal pull-down	Not allow eMMC as a boot source	disable	default (don't force DNX FW Load) Weak internal pull-down	SMBus 3.3V mode select

GPIO	GPIO_88	GPIO_92	GPIO_111	GPIO_110	GPIO_118	GPIO_120	GPIO_123
Schematic							
High	Weak internal pull-up PMU 1.8V mode select	SMBS No-reboot enable	Do not boot from SPI Weak internal pull-up	Weak internal pull-up LPC 1.8V mode select	Flash Descriptor Override	Two SWAP override enable	RSVD (Internal 20K PU)
Low	PMU 3.3V mode select	default (SMBus No Re-Boot Disable) Weak internal pull-down	boot from SPI	LPC 3.3V mode select	No Override (Normal Operat i on) Weak internal pull-down	default (Disable top swap override) Weak internal pull-down	RSVD

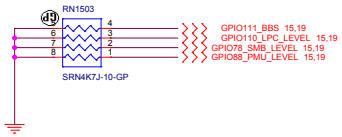
0921

Table 2-36. Hardware Straps

GPIO #	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_34	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_35	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_36	VCC_1P24V_1P35V_A voltage selection	20K PD	1 = 1.35V 0 = 1.24V (default) ***Note:*** This strap will only be used for B-step. For A-step this rails should only be set at 1.24V
GPIO_39	Enable CSE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) ***Note:*** Apollo Lake supports TXE3.0 (this is also called CSE) ***Note:*** This strap tells CSE (TXE3.0) to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of CSE (TXE3.0) before the first patch point this strap enabled the platform tell CSE (TXE3.0) to bypass the ROM causing the issue and go to the patch space instead.
GPIO_40	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_43	Allow eMMC as a boot source	20K PU	1=enable (default) 0=disable
GPIO_44	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable
GPIO_47	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) ***Note:*** DnX: Download and Execute ***Note:*** This strap is a recovery strap for corrupted FW image. This strap will force CSE (TXE3.0) to execute a "Download and Execute" (DnX) flow, where it would fetch firmware from a USB stick and re-flash a USB. CSE (TXE3.0) can do it for BIOS part of FW, but if CSE FW itself is corrupted we need this strap.
GPIO_48	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_78	SMBus 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_82	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_88	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_92	SMBus No Re-Boot	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Platforms should strap this LOW. Functionality is handled by the PMC.

GPIO #	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_104	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_105	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_106	RSVD	20K PU	Please ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_111	Boot BIOS Strap (BBS)	20K PU	1 = Do not boot from SPI (default) 0 = Boot from SPI
GPIO_118	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override ***Note:*** This strap enables the platform to override security features in the SPI.
GPIO_110	LPC 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_117	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_123	RSVD	20K PU	Please ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_112	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_113	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_120	Top swap override	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_121	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

Note: All the straps are sampled at Rising Edge of RSM_RST_N



EMMC

緯創資通 Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)

Size: A2 | Document Number: Ironhide_APL | Rev: -1M

Date: Wednesday, September 21, 2016 | Sheet 15 of 106

SSID = PCH

Apollo Lake		2016 Ironhide
SATA P0		HDD/SSD
SATA P1	USB3 Port5	
PCIe Port 0		
PCIe Port 1		
PCIe Port 2		
PCIe Port 3	USB3 Port4	WIFI
PCIe Port 4	USB3 Port3	
PCIe Port 5	USB3 Port2	
USB3	USB3 Port1	
USB3	USB3 Port0 (OTG)	USB 3 I/O
USB2	USB2 Port0	USB 3 I/O
USB2	USB2 Port1	
USB2	USB2 Port2	USB 2 I/O
USB2	USB2 Port3	USB 2 I/O
USB2	USB2 Port4	BT
USB2	USB2 Port5	TS
USB2	USB2 Port6	CCD
USB2	USB2 Port7	CR
USB3	USB SSIC	
eMMC	eMMC	eMMC
SDIO	SDIO	

USB3.0 port1

35 USB1_USB30_TX_P
35 USB1_USB30_TX_N
35 USB1_USB30_RX_P
35 USB1_USB30_RX_N

HDD

60 HDD_SATA_TX_N
60 HDD_SATA_TX_P
60 HDD_SATA_RX_N
60 HDD_SATA_RX_P

WLAN

61,89 WLAN_PCIE_TX_P
61,89 WLAN_PCIE_TX_N
61,89 WLAN_PCIE_RX_N
61,89 WLAN_PCIE_RX_P
61,89 WLAN_CLK_CPU
61,89 WLAN_CLK_CPU#
61,89 WLAN_CLKREQ_CPU#

18,24,61,89 PCIE_WAKE#

CPU1I 9 OF 23 APL_SOC

WLAN

WLAN_PCIE_TX_P — C1616 SCD1U16V2KX-L-GP — WLAN_CPU_TX_P — P3
WLAN_PCIE_TX_N — C1617 SCD1U16V2KX-L-GP — WLAN_CPU_TX_N — P2
WLAN_PCIE_RX_P — P12
WLAN_PCIE_RX_N — P10

PCIE_P5_USB3_P2_TXP L2
PCIE_P5_USB3_P2_TXN L1
PCIE_P5_USB3_P2_RXP K7
PCIE_P5_USB3_P2_RXN M7
PCIE_P4_USB3_P3_TXP N2
PCIE_P4_USB3_P3_TXN M2
PCIE_P4_USB3_P3_RXP H5
PCIE_P4_USB3_P3_RXN H6
PCIE_P3_USB3_P4_TXP
PCIE_P3_USB3_P4_TXN
PCIE_P3_USB3_P4_RXP
PCIE_P3_USB3_P4_RXN

1.24V

R1601 1 — 402R2F-GP
PCIE_OBSP_CPU F6
PCIE_OBSN_CPU F5
PCIE2_USB3_SATA3_RCOMP_P
PCIE2_USB3_SATA3_RCOMP_N
1.24V

PCIE_P2_TXP T2
PCIE_P2_TXN T3
PCIE_P2_RXP M5
PCIE_P2_RXN M6
PCIE_P1_TXP R1
PCIE_P1_TXN R2
PCIE_P1_RXP T10
PCIE_P1_RXN T12
PCIE_P0_TXP V3
PCIE_P0_TXN V2
PCIE_P0_RXP P7
PCIE_P0_RXN P6

1.24V

PCIE_WAKE3# N62 — PCIE_WAKE3_CPU — R1602 1 — Do Not Stuff — 2 — PCIE_WAKE#
PCIE_WAKE2# P61 — PCIE_WAKE2_CPU
PCIE_WAKE1# P62 — PCIE_WAKE1_CPU
PCIE_WAKE0# R62 — PCIE_WAKE0_CPU

1.8V

1D8V_S5

RN1655
PCIE_WAKE3_CPU 1 8
PCIE_WAKE2_CPU 2 7
PCIE_WAKE1_CPU 3 6
PCIE_WAKE0_CPU 4 5
SRN10KJ-12-GP

APOLLO-LAKE-GP-U

CPU1J 10 OF 23 APL_SOC

USB3.0 port1

USB1_USB30_TX_P J1
USB1_USB30_TX_N J2
USB1_USB30_RX_P K9
USB1_USB30_RX_N K10
USB3_P1_TXP K3
USB3_P1_TXN K2
USB3_P1_RXP F2
USB3_P1_RXN G2
USB3_P0_TXP
USB3_P0_TXN
USB3_P0_RXP
USB3_P0_RXN

1.24V

SATA_P1_USB3_P5_TXP W1
SATA_P1_USB3_P5_TXN W2
SATA_P1_USB3_P5_RXP T5
SATA_P1_USB3_P5_RXN T6

HDD

HDD_SATA_TX_P Y3
HDD_SATA_TX_N Y2
HDD_SATA_RX_P T9
HDD_SATA_RX_N T7
SATA_P0_TXP
SATA_P0_TXN
SATA_P0_RXP
SATA_P0_RXN

PCIE_CLKOUT3P B7 — WLAN_CLK_CPU
PCIE_CLKOUT3N B5 — WLAN_CLK_CPU#
PCIE_CLKOUT2P A7
PCIE_CLKOUT2N B8
PCIE_CLKOUT1P C10
PCIE_CLKOUT1N A10
PCIE_CLKOUT0P C11
PCIE_CLKOUT0N B11

1.05V

PCIE_CLKREQ3# AJ62 — WLAN_CLKREQ_CPU#
PCIE_CLKREQ2# AH61 — PCIE_CLKREQ2#
PCIE_CLKREQ1# AH62 — PCIE_CLKREQ1#
PCIE_CLKREQ0# AK62 — PCIE_CLKREQ0#

1.8V

USB_SSIC_0_TX_P AH13
USB_SSIC_0_TX_N AH12
USB_SSIC_0_RX_P AG16
USB_SSIC_0_RX_N AG15

1.05V

1D8V_S5

RN1601
PCIE_CLKREQ2# 1 8
PCIE_CLKREQ1# 2 7
WLAN_CLKREQ_CPU# 3 6
PCIE_CLKREQ0# 4 5
SRN10KJ-12-GP

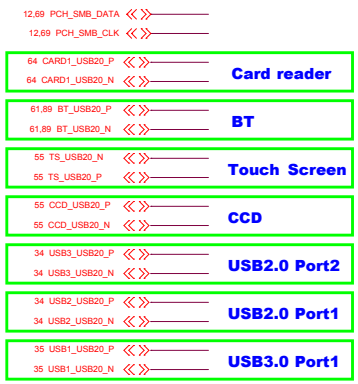
APOLLO-LAKE-GP-U

EMMC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (USB/LPC/GPIO)
Size: Custom | Document Number: Ironhide_APL | Rev: -1M
Date: Wednesday, September 21, 2016 | Sheet 16 of 106

SSID = CPU



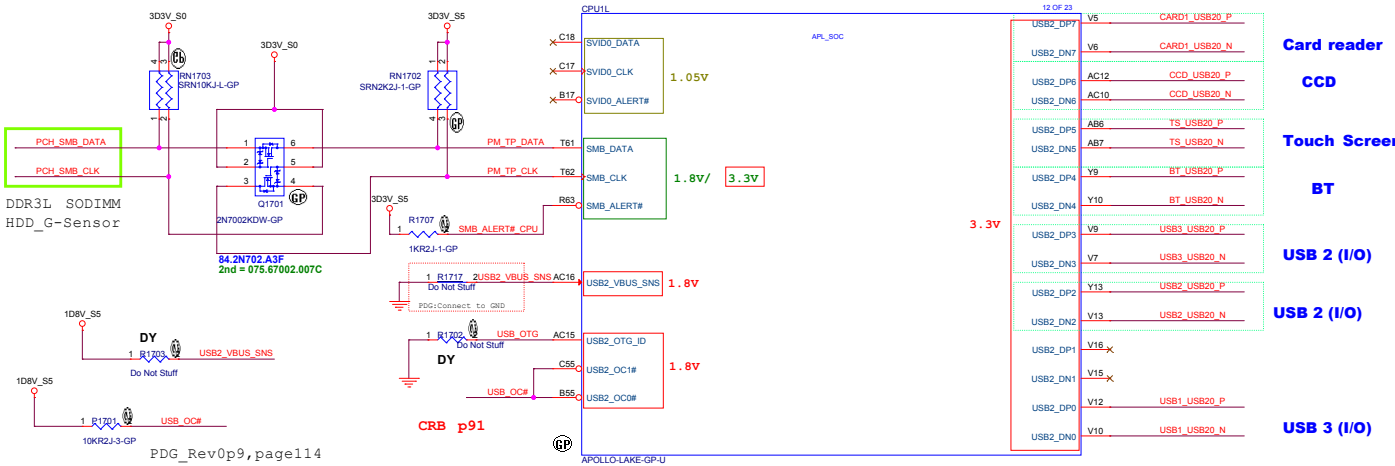


Table 61. Over current Pin Default Usage

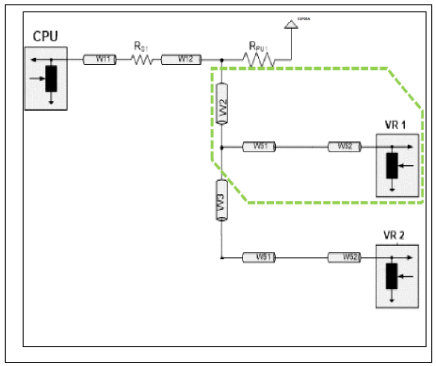
Pin	Default Port Mapping
OC0#	Port 0
OC1#	Port 1-7

Table 62. Over current Pin Example Configuration

Location	Number of USB Ports	USB Ports Number	OC Pins Used
External Topology	1	0	OC0#
External Topology	4	1,2,3,4	OC1#

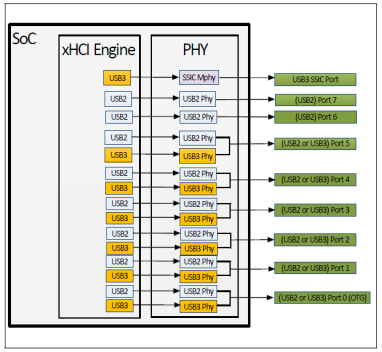
NOTE: All USB ports routed out of the package must have over current protection. It is the system BIOS responsibility to ensure all used ports have OC protection.

Routing Illustration for SVID0_ALERT_N



NOTE: If less than 2 VR is used, remove the first device from the topology.Example:If 1 VR is used, remove from W2 to VR1 from the topology (as illustrated by dotted line).

Figure 3-3. USB2 and USB3 Port Mapping



Notes: There are 8x USB Ports supported on Apollo Lake. USB Ports [5:0] can be used as USB2 and USB3 and are mutually exclusive. USB Port 6 and Port 7 can only be used as USB2.

Apollo Lake		2016 Ironhide
SATA P0		HDD/SSD
SATA P1	USB3 Port5	
PCIe Port 0		
PCIe Port 1		
PCIe Port 2		
PCIe Port 3	USB3 Port4	WIFI
PCIe Port 4	USB3 Port3	
PCIe Port 5	USB3 Port2	
USB3	USB3 Port1	
USB3	USB3 Port0 (OTG)	USB 3 I/O
USB2	USB2 Port0	USB 3 I/O
USB2	USB2 Port1	
USB2	USB2 Port2	USB 2 I/O
USB2	USB2 Port3	USB 2 I/O
USB2	USB2 Port4	BT
USB2	USB2 Port5	TS
USB2	USB2 Port6	CCD
USB2	USB2 Port7	CR
USB3	USB SSIC	
eMMC	eMMC	eMMC
SDIO	SDIO	

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Size	Document Number	Rev
Custom	Ironhide_APL	-1M
Date: Wednesday, September 21, 2016	Sheet 17 of 105	

SSID = PCH

N/A	PMC_SPI_FS1	1.8V	20K PU	LSMV	CMOS	PMC_SPI_FS1/ Out	Func2: HV_DDI2_HPD/Input

SUSPWRDNACK[1]	CMOS	O	**Sus Power Down Ack:** Indicator from SoC that "always on" rails can be shut down.

Table 2-30. Apollo Lake PM Interface Signals (Sheet 1 of 2)

Note: These signals are part of the GPIO. Please refer to Table 2-37 for more details.

Signal Name	Dir.	I/O Voltage	Type	Description
PMU_BATLOW_N	I/O	V1P8/V3P3	GPIO	**Battery Low:** This signal indicates that there is insufficient power to boot the system. Assertion will prevent wake from S3-S5 state. This signal can also be enabled to cause an SMI# when asserted.
PMU_PLTRST_N	I/O	V1P8/V3P3	GPIO	**Platform Reset:** This signal is used to reset devices on the platform (such as SIO, LAN, processor, and so forth.). This signal is asserted during power-up and when S/W initates a hard reset sequence through the Reset Control register (I/O port CF9h). The SoC drives PLTRST# active a minimum of 1 ms when initiated through the Reset Control register (I/O port CF9h)
PMU_PWRBTN_N	I/O	V1P8/V3P3	GPIO	**Power Button:** Power button input signal. Used to wake the SoC from power button press. The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S3–S4 states. This signal has an internal 16 ms de-bounce on the input.
PMU_RSTBTN_N	I/O	V1P8/V3P3	GPIO	**Reset Button:** Reset button input signal.
PMU_SLP_S0_N	I/O	V1P8/V3P3	GPIO	**S0 Sleep Control:** Controls power delivery subsystem. Asserted low in S0ix and G3 state.
PMU_SLP_S3_N	I/O	V1P8/V3P3	GPIO	**S3 Sleep Control:** Controls power delivery subsystem. Asserted low in S3 and lower
PMU_SLP_S4_N	I/O	V1P8/V3P3	GPIO	**S4 Sleep Control:** Controls power delivery subsystem. Asserted low in S4 and lower

Table 2-30. Apollo Lake PM Interface Signals (Sheet 2 of 2)

Note: These signals are part of the GPIO. Please refer to Table 2-37 for more details.

Signal Name	Dir.	I/O Voltage	Type	Description
PMU_SUSCLK	I/O	V1P8/V3P3	GPIO	**Suspend Clock:** Primary RTC clock output.
SUS_STAT_N		V1P8/V3P3	GPIO	**Suspend Status:** Asserted to indicate that the system will be entering a Sx state.
SUSPWRDNACK		V1P8/V3P3	GPIO	**Sus Power Down Ack:** Indicator from SoC that "always on" rails can be shut down.
SOC_PWROK	I	V1P8/V3P3	RTC	**SoC Power OK:** When asserted, this signal is an indication to the SoC that all of its core power rails have been stable for at least 5 ms. This signal can be driven asynchronously. Then this signal is negated, the SOC asserts PLTRST#.

Note: The I/O voltage selection is done by using Hardware Strap GPIO_88

Vth(max)=1.1V

APS debug port

Do Not Stuff APS1801 PM_SLP_S3#
Do Not Stuff APS1802 PM_SLP_S4#
Do Not Stuff APS1803 RTC_RST#
Do Not Stuff APS1804 KBC_PWRBTN# 24,64,89
Do Not Stuff APS1806 PM_SLP_S0#

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Title: CPU (CLK/SPI/SIDEBAND/JTAG)

Size: Custom | Document Number: Ironhide APL | Rev: -1M

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SSID = PCH

SPI ROM
24,25 SPI_SI_ROM
24,25 SPI_SO_ROM
25 SPI_WP_ROM
25 SPI_HOLD_ROM
24,25 SPI_CS_CPU_N0
24,25,90 SPI_CLK_ROM

OTHER
90 HDA_RST#_CPU
24,68 INT_SERIRQ
24,68 LPC_FRAME#_CPU
24 PM_CLKRUN#_EC
24,90 LPC_CLK_KBC
68,90 LPC_CLK_DBG
24,68 LPC_AD_CPU_P3
24,68 LPC_AD_CPU_P2
24,68 LPC_AD_CPU_P1
24,68 LPC_AD_CPU_P0
27 HDA_RST#_CODEC
24 ME_UNLOCK

STRAP
15 GPIO92_SMB_NRB
15 GPIO111_BBS
15 GPIO118_FLASH_OVR
15 GPIO120_BIOS_SWAP
15 GPIO110_LPC_LEVEL
15 GPIO88_PMU_LEVEL
15 GPIO78_SMB_LEVEL

24 GS_I2C5_SDA_KBC
24 GS_I2C5_SCL_KBC
65 TP_I2C4_SDA
65 TP_I2C4_SCL
55 TS_I2C3_SDA
55 TS_I2C3_SCL

15 GP_SSP2_TXD

CPU1K — APL_SOC — 11 OF 23 — APOLLO-LAKE-GP-U

Strap GPIO_82
Strap pin
1.8V
3.3V /1.8V
1.8V

M52 AVS_DMIC_DATA_2
M54 AVS_DMIC_DATA_1
P52 AVS_DMIC_CLK_B1
M55 AVS_DMIC_CLK_AB2
P54 AVS_DMIC_CLK_A1
M61 AVS_I2S3_WS_SYNC
GPIO92_SMB_NRB L63 AVS_I2S3_SDO
L62 AVS_I2S3_SDI
M62 AVS_I2S3_BCLK
M57 AVS_I2S2_WS_SYNC
GPIO88_PMU_LEVEL M58 AVS_I2S2_SDO
K59 AVS_I2S2_SDI
HDA_RST#_CODEC R1901 33R2J-2-GP HDA_RST#_CPU K58 AVS_I2S2_MCLK/AVS_HDA_RST#
C1903 Do Not Stuff DY
H59 AVS_I2S2_BCLK
J62 AVS_I2S1_WS_SYNC
GPIO78_SMB_LEVEL K62 AVS_I2S1_SDO
K61 AVS_I2S1_SDI
G62 AVS_I2S1_MCLK
H63 AVS_I2S1_BCLK

LPC_SERIRQ AB62 INT_SERIRQ
LPC_FRAME# V61 LPC_FRAME#_CPU
LPC_CLKRUN# V62 PM_CLKRUN#_EC
LPC_CLKOUT1 AA62
LPC_CLKOUT0 AB61 LPC_CLK_CPU_P0
LPC_AD3 W63 LPC_AD_CPU_P3
LPC_AD2 W62 LPC_AD_CPU_P2
LPC_AD1 Y62 LPC_AD_CPU_P1
LPC_AD0 Y61 LPC_AD_CPU_P0

R1905 33R2J-2-GP LPC_CLK_KBC
R1904 Do Not Stuff LPC_CLK_DBG
Debug

OSCOUT P29 XTL_19D2M_X1_CPU
OSCIN R27 XTL_19D2M_X2_CPU
OSC_CLK_OUT_4 AF62
OSC_CLK_OUT_3 AE60
OSC_CLK_OUT_2 AG63
OSC_CLK_OUT_1 AF61
OSC_CLK_OUT_0 AG62

C1901 SC3D9P50V2CN-1GP
X1901 SPEC CL=7pF,10PPM
R1912 200KR2F-L-GP
XTAL-48D2MHZ-21-GP 082.30001.0061
2nd = 82.30071.131
C1902 SC3D9P50V2CN-1GP

RN1901 SRN2K2J-1-GP GSENSOR_1
3D3V_S5
Vth(max)=1.1V
RN1902 SRN2K2J-1-GP GSENSOR_1
1D8V_S5
Q1901 PJT138KA-GP 075.00138.0A7C
GS_I2C5_SDA_KBC
GS_I2C5_SCL
GS_I2C5_SDA
GS_I2C5_SCL_KBC

R put near ROM side

CPU1M — APL_SOC — 13 OF 23 — APOLLO-LAKE-GP-U

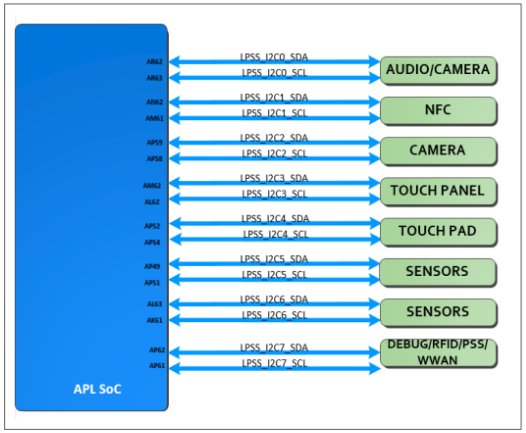
SPI_SI_ROM A58 FST_SPI_MOSI_IO0
SPI_SO_ROM B58 FST_SPI_MISO_IO1
SPI_WP_ROM B60 FST_SPI_IO2
SPI_HOLD_ROM B61 FST_SPI_IO3
C57 FST_SPI_CS1#
SPI_CS_CPU_N0 B57 FST_SPI_CS0#
SPI_CLK_ROM C56 FST_SPI_CLK
GP_SSP2_TXD E62 SIO_SPI_2_TXD Strap pin
C62 SIO_SPI_2_RXD
D59 SIO_SPI_2_FS2 Strap GPIO_121
GPIO120_BIOS_SWAP E56 SIO_SPI_2_FS1 Strap pin
D61 SIO_SPI_2_FS0
GPIO118_FLASH_OVR F62 SIO_SPI_2_CLK Strap pin
ME_UNLOCK 2 R1913 1 Do Not Stuff
H58 SIO_SPI_1_TXD Strap GPIO_117
H57 SIO_SPI_1_RXD Strap GPIO_116
F61 SIO_SPI_1_FS1 Strap GPIO_113
K55 SIO_SPI_1_FS0 Strap GPIO_112
GPIO111_BBS F58 SIO_SPI_1_CLK Strap pin
GPIO110_LPC_LEVEL J52 SIO_SPI_0_TXD Strap pin
H54 SIO_SPI_0_RXD
H52 SIO_SPI_0_FS1 Strap GPIO_106
F52 SIO_SPI_0_FS0 Strap GPIO_105
F54 SIO_SPI_0_CLK Strap GPIO_104

1.8V
1.8V

LPSS_I2C7_SDA/ISH_I2C2_SDA AP62
LPSS_I2C7_SCL/ISH_I2C2_SCL AP61
LPSS_I2C6_SDA/ISH_I2C1_SDA AL63
LPSS_I2C6_SCL/ISH_I2C1_SCL AK61
LPSS_I2C5_SDA/ISH_I2C0_SDA AP49 GS_I2C5_SDA
LPSS_I2C5_SCL/ISH_I2C0_SCL AP51 GS_I2C5_SCL
LPSS_I2C4_SDA AP52 TP_I2C4_SDA
LPSS_I2C4_SCL AP54 TP_I2C4_SCL
LPSS_I2C3_SDA AM62 TS_I2C3_SDA
LPSS_I2C3_SCL AL62 TS_I2C3_SCL
LPSS_I2C2_SDA AP59
LPSS_I2C2_SCL AP58
LPSS_I2C1_SDA AN62
LPSS_I2C1_SCL AM61
LPSS_I2C0_SDA AR62
LPSS_I2C0_SCL AR63

Rotate G_Sensor
Touch Pad
Touch Panel

Figure 203. I²C Interface Topology



To configure the I²C ports, follow the pin muxing options listed out in the Apollo Lake SoC – External Design Specification (EDS) Volume 1 of 4 [CDI#: 557555].

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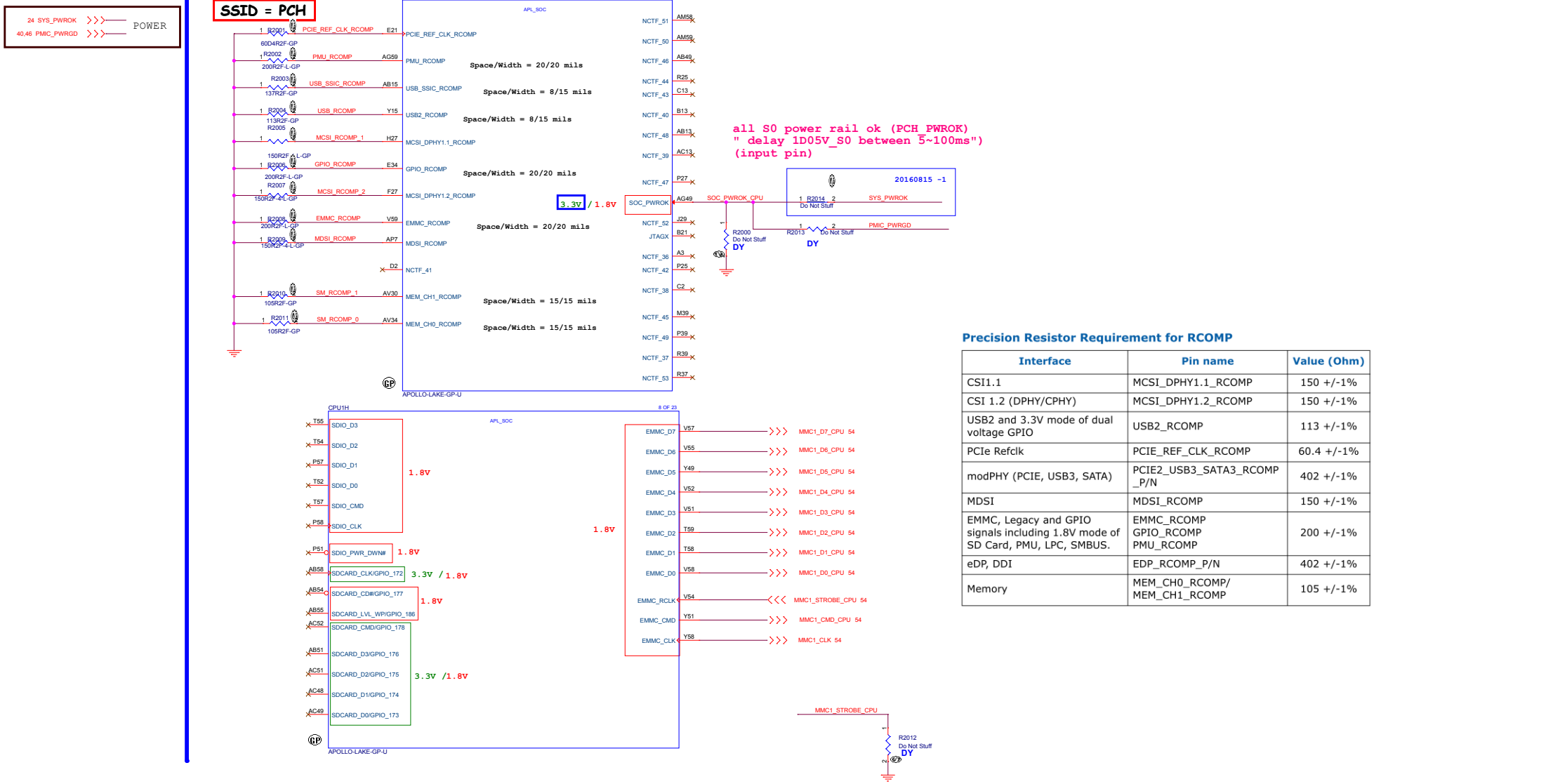

Precision Resistor Requirement for RCOMP

Interface	Pin name	Value (Ohm)
CSI1.1	MCSI_DPHY1.1_RCOMP	150 +/-1%
CSI 1.2 (DPHY/CPHY)	MCSI_DPHY1.2_RCOMP	150 +/-1%
USB2 and 3.3V mode of dual voltage GPIO	USB2_RCOMP	113 +/-1%
PCIe Refclk	PCIE_REF_CLK_RCOMP	60.4 +/-1%
modPHY (PCIE, USB3, SATA)	PCIE2_USB3_SATA3_RCOMP _P/N	402 +/-1%
MDSI	MDSI_RCOMP	150 +/-1%
EMMC, Legacy and GPIO signals including 1.8V mode of SD Card, PMU, LPC, SMBUS.	EMMC_RCOMP GPIO_RCOMP PMU_RCOMP	200 +/-1%
eDP, DDI	EDP_RCOMP_P/N	402 +/-1%
Memory	MEM_CH0_RCOMP/ MEM_CH1_RCOMP	105 +/-1%

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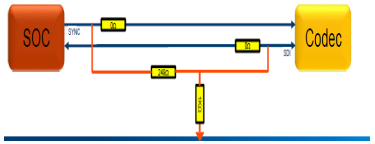
SSID = CPU

AUDIO
27 HDA_SPKR
27 HDA_SDIN0_CODEC
27,90 HDA_SDOUT_CODEC
27,90 HDA_SDIN0_CPU
27 HDA_SYNC_CODEC
27,90 HDA_BITCLK_CODEC

46 PMIC_IRQ#
15 GPIO36_VCCIO_LEVEL
65 TP_IN#
68 LPSS_UART2_TXD
68 LPSS_UART2_RXD
69 GSR_HDD_INT1
24 EC_SCI#
24 SH_INT#
55 TOUCH_DET#
55 TOUCH_RST#_CPU
55 TOUCH_INT#_CPU
25 RTC_DET#



CPU1O
APL_SOC
15 OF 23
APOLLO-LAKE-GP-U

HDA_SPKR — AK57 ISH_GPIO_9/SPKR
AM52 ISH_GPIO_8/MEMHOT#
AM55 ISH_GPIO_7/AVS_I2S5_SDO/LPSS_UART2_CTS#
AM57 ISH_GPIO_6/AVS_I2S5_SDI/LPSS_UART2_RTS#
LPSS_UART2_TXD — AM49 ISH_GPIO_5/AVS_I2S5_WS_SYNC/LPSS_UART2_TXD
LPSS_UART2_RXD — AM51 ISH_GPIO_4/AVS_I2S5_BCLK/LPSS_UART2_RXD
AM54 ISH_GPIO_3/AVS_I2S6_SDO/AVS_HDA_SDO
AK51 ISH_GPIO_2/AVS_I2S6_SDI/AVS_HDA_SDI
AK58 ISH_GPIO_1/AVS_I2S6_WS_SYNC/AVS_HDA_WS_SYNC
AM48 ISH_GPIO_0/AVS_I2S6_BCLK/AVS_HDA_BCLK
1.8V

F34 GPIO_33/ISH_GPIO_15/SUS_CLK3
F35 GPIO_32/ISH_GPIO_14/SUS_CLK2
H34 GPIO_31/ISH_GPIO_13/SUS_CLK1
C37 GPIO_30/ISH_GPIO_12
H35 GPIO_29/ISH_GPIO_11
B37 GPIO_28/ISH_GPIO_10
C29 GPIO_27
C31 GPIO_26/SATA_LED#
C27 GPIO_25/SATA_DEVSLP1
1.8V

J39 GPIO_18 — TP_IN#
C25 GPIO_24/SATA_DEVSLP0
B25 GPIO_23/SATA_GP1
A26 GPIO_22/SATA_GP0
C26 GPIO_21
B27 GPIO_20
C33 GPIO_19 — SH_INT#
A30 GPIO_9
C35 GPIO_17 — TOUCH_INT#_CPU
C36 GPIO_16 — GSR_HDD_INT1
F39 GPIO_15 — TOUCH_DET_CPU
C38 GPIO_14 — TOUCH_RST#_CPU
C30 GPIO_13
E39 GPIO_12 — SOC_WAKE_SCI#
C34 GPIO_11 — EC_SCI#
L39 GPIO_10
A38 GPIO_0
B29 GPIO_8
H39 GPIO_7
B31 GPIO_6
A34 GPIO_5
B35 GPIO_4
B39 GPIO_3
C39 GPIO_2
B33 GPIO_1
1.8V

HDA_SDIN0_CPU
HDA_SDIN0_CODEC — R2103 — ES-CPU
R2106 Do Not Stuff — ES-CPU
Doc#560733-HD audio SDI pin issue
HDA_SYNC_CODEC — HDA_SYNC_CPU
HDA_BITCLK_CODEC — HDA_BITCLK_CPU
HDA_SDOUT_CODEC — HDA_SDOUT_CPU
RN2102 SRN33J-1-GP
1D8V_S5
R2101 Do Not Stuff DY
PMIC_IRQ# — R2102 Do Not Stuff — PMIC_IRQ#_CPU

20160804 -1
1D8V_S5
TP_IN# — R2104 10KR2F-L1-GP
1D8V_S5
SH_INT# — R2108 10KR2F-L1-GP

3D3V_S0
1D8V_S0
R2105 10KR2F-L1-GP TS
R2107 Do Not Stuff DY
TOUCH_DET_CPU — Q2102 — TOUCH_DET#
Do Not Stuff
Do Not Stuff
2nd = 084.27002.0L31
3rd = 084.06587.0031

1D8V_S5
EC_SCI# — RN2101 — SOC_WAKE_SCI#
SRN10KJ-L-GP

CPU1Q
APL_SOC
17 OF 23
APOLLO-LAKE-GP-U

M16 NCTF_59
L16 NCTF_60
F16 NCTF_63
E16 NCTF_54
J16 NCTF_66
H16 NCTF_58
H12 NCTF_68
F12 NCTF_56
M12 NCTF_65
M10 NCTF_62
F14 NCTF_57
H14 NCTF_55

L30 GPIO_219
M30 GPIO_218
M29 GPIO_217
P30 GPIO_216
AP57 NCTF_67
E41 PWM3
F41 PWM2 — GPIO36_VCCIO_LEVEL
C41 PWM1
B41 PWM0
C63 NCTF_64
E63 NCTF_61
1.8V

Strap pin
Strap GPIO_35
Strap GPIO_34

20160715 -1
RTC_DET#
PSW_CLR#
G2101 Do Not Stuff
20160728 -1

20160728 -1
RTC_DET# — RN2103 — PSW_CLR#
SRN10KJ-L-GP
1D8V_S5

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Title: CPU (POWER1)
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Blanking

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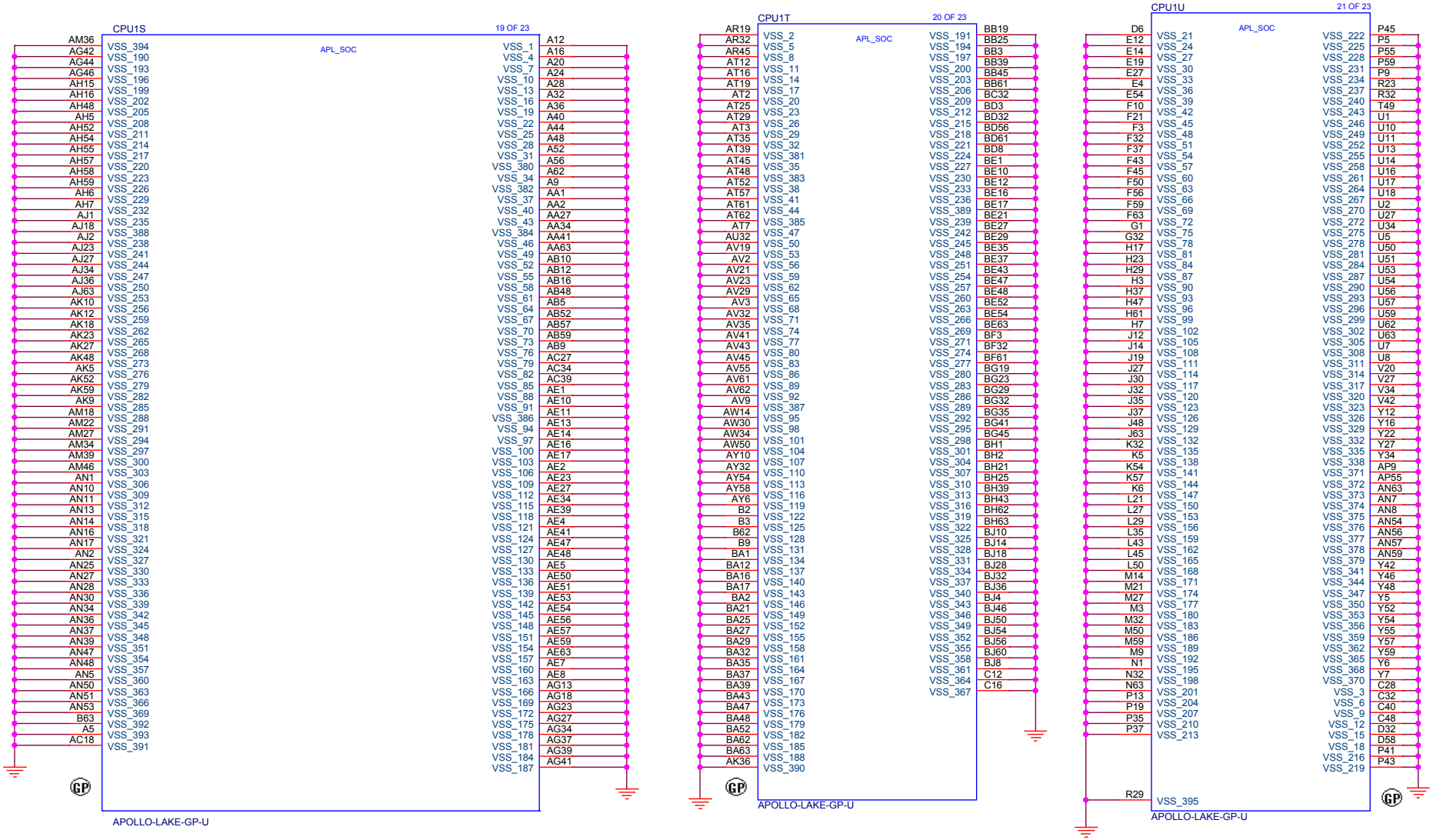
Size	Document Number	Rev
A4	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 22 of 106

SSID = CPU



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Title: VSS

Size: Custom | Document Number: Ironhide_APL | Rev: -1M

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SSID = KBC

Power

3D3V_AUX_S5
3D3V_S0
3D3V_RTC_AUX

Signal

EC_CAP_LED 65
FUN_OFF# 65,89
LPC_FRAME#_CPU 19,68
LPC_AD_CPU_P3 19,68
LPC_AD_CPU_P2 19,68
LPC_AD_CPU_P1 19,68
LPC_AD_CPU_P0 19,68
LPC_CLK_KBC 19,90
PLT_RST# 18,26,54,61,68,89
WLAN_PCIE_WAKE# 24,61
TOUCH_EN 24,55
LID_CLOSE# 64,89
LID_CLOSE# 64,89
FTP_PWR_EN# 65
PURE_HW_SHUTDOWN# 26,40
PM_CLKRUN#_EC 19
ES1_TXD 61,68
ES1_RXD 68
EC_TP_IN# 24,65
KBC_BEEP 27
KB_BL_DET 65
FAN1_PWM 26,89
FAN_TACH1 26,89
Value= 64
Value= 64
KSO0 65,89
KSO1 65,89
KSO2 65,89
KSO3 65,89
KSO4 65,89
KSO5 65,89
KSO6 65,89
KSO7 65,89
KSO0 65,89
KSO1 65,89
KSO2 65,89
KSO3 65,89
KSO4 65,89
KSO5 65,89
KSO6 65,89
KSO7 65,89
KSO8 65,89
KSO9 65,89
KSO10 65,89
KSO11 65,89
KSO12 65,89
KSO13 65,89
KSO14 65,89
KSO15 65,89
AC_IN# 44
KBC_PWRBTN# 18,64,89
BAT_IN# 43
AD_IA 44
ALL_SYS_PWRGD 40
MODEL_ID_AD 55
STOBY_LED 64
3V_EN 40
PMC_RSMRST# 18,46
SML1_CLK 18,55,70
SML1_DATA 18,55,70
BAT_SCL 43,44
BAT_SDA 43,44
SPI_WP_ROM 19,25
TOUCH_EN 24,55
EC_TPCLK 65
EC_TPDATA 65
ME_UNLOCK 19
EC_TP_IN# 24,65
GSENSOR_INT 55,70
RTCRST_ON 18
BLON_OUT 55
AD_OFF 43
VID_IN1 26
VID_OUT1 26
PROCHOT#_CPU 18,44
CHARGE_LED 64
DC_BATFULL 64
RSMRST#_KBC 18
AMP_MUTE# 27
SS_ENABLE 40
KB_BL_PWM 65
GS_I2CS_SDA_KBC 19
GS_I2CS_SCL_KBC 19
SYS_PWROK 20
POWER_LED 64
SPI_SO_ROM 19,25
SPI_SI_ROM 19,25
SPI_CLK_ROM 19,25,90
SPI_CS_CPU_N0 19,25
WIFI_RF_EN 61,89
BLUETOOTH_EN 61,89
USB_PWR_EN# 34,35
WLAN_PCIE_WAKE# 24,61
CHG_ON# 44
NMI_SMI_DBG# 18
WLAN_PERST# 61
WLAN_PWR_EN# 61
BUS_PWRDN_ACK 18
SH_INT# 21

SOC need 1.8V

AC_PRESENT 18
eDP_BLEN_CPU 8
PM_PWRBTN# 18
PCIE_WAKE# 16,18,61,89

SOC need level shift

EC_SCI# 21

Apollo 9028: VCC_LPC 3.3V
Braswell 9029: VCC_IO2 1.8V

INT_SERIRQ 19,68

3.3V

PM_SLP_S3# 18,40,46,53
PM_SLP_S4# 18,46

LPC BUS=>3.3V
SPI BUS=>3.3V/1.8V (VCC_IO2 PIN:124 OPTION)

Close to the EC

PLT_RST#
R2460 47KR2J-L2-GP

1D8V_S0
R2458 10KR2F-L1-GP PI_RCIN#
3D3V_S0
RN2410 FAN_TACH1 FUN_OFF# SRN10KJ-GP
3D3V_S5
GSENSOR_1
RN2402 SML1_CLK SML1_DATA SRN2KJ-1-GP
EC_SCI# R2465 Do Not Stuff ECSCI#_KBC
3D3V_AUX_S5
R2441 330KR2J-L-GP
KBC_PWRBTN# R2442 470R2F-GP KBC_PWRBTN#_R
G2402 Do Not Stuff

D2401 RB520SM-30T2R-GP
83.1R003.N8F
2nd = 83.R2003.0EF
ECRST#
PURE_HW_SHUTDOWN#
RN2407 Do Not Stuff
ECRST#_Q
3D3V_AUX_S5
Q2403 Do Not Stuff
DY
2nd = 84.03906.F11
3rd = 84.T3906.E11
C2426 SC1U10V2KX-L1-GP

For EC power consumption reserver

3D3V_AUX_KBC
R2406 Do Not Stuff
3D3V_AUX_S5

VCC_LPC(Pin9)

3D3V_AUX_KBC
R2435 Do Not Stuff
VCC_LPC

U2401
LPC_CLK_KBC
LPC_FRAME#_CPU
LPC_AD_CPU_P3
LPC_AD_CPU_P2
LPC_AD_CPU_P1
LPC_AD_CPU_P0
INT_SERIRQ
SH_INT#
H_RCIN#
PLT_RST#
ECSCI#_KBC
PM_CLKRUN#_EC
ECRST#
KBC_BEEP
KB_BL_PWM
DC_BATFULL
FAN1_PWM
FAN_TACH1
CHG_ON#
KSO0 KSO1 KSO2 KSO3 KSO4 KSO5 KSO6 KSO7 KSO8 KSO9 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15
KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7
SML1_DATA
SML1_CLK
BAT_SDA
BAT_SCL
GS_I2CS_SCL_KBC
GS_I2CS_SDA_KBC
LID_CLOSE#
PMC_RSMRST#
STOBY_LED
ES1_TXD
ES1_RXD
WL_OFF#_CLOCK
CHARGE_LED
WIFI_RF_EN
GSENSOR_INT
LPC_CLK_KBC
LPC_FRAME#_CPU
LPC_AD_CPU_P3
LPC_AD_CPU_P2
LPC_AD_CPU_P1
LPC_AD_CPU_P0
INT_SERIRQ
PLT_RST#
SCI#
CLKRUN#
ECRST#
PWM0
PWM1
PWM2
FANPWM0
FANPWM1
FANFB0
FANFB1
3.3V
1.8V
071.09028.000G
CPU/G-sensor --->
BATTER /CHARGER --->
CPU <---
Touch Pad

3D3V_AUX_KBC 3D3V_RTC_AUX
VCC_LPC
VCC_IO2
AVCC
EC_AGND
1D8V_S5
C2429 CD1U16V2KX-L-GP
AMP_MUTE#
TOUCH_EN
PM_SLP_S3#
WLAN_PCIE_WAKE#
AD_IA
PCB_VER_AD
ADT_TYPE_AD
EC_TP_INT
VID_IN1
VID_OUT1
WLAN_PERST#
KB_BL_DET
BLON_OUT
AD_OFF
SS_ENABLE
FUN_OFF#
WL_OFF#_KBC
RSMRST#_KBC
VID_OUT1
USB_PWR_EN#
SYS_PWROK
RTCRST_ON
EC_CAP_LED
VID_IN1
PC_INT
KBC_PWRBTN#_R
ALL_SYS_PWRGD
5V_EN
TP2401 Do Not Stuff
PECI
WLAN_PWR_EN#
BAT_INH
POWER_LED
eDP_BLEN_CPU
PM_PWRBTN#
IOAC
R2451 Do Not Stuff
PCIE_WAKE#_R
PCIE_WAKE#
AC_PRESENT
YellowP
PSIP_PWR_EN#
PROCHOT_EC
BLUETOOTH_EN
PM_SLP_S3#
SPI_CS_KBC_N0 R2412 Do Not Stuff SPI_CS_CPU_N0
SPI_SI_KBC R2410 Do Not Stuff SPI_SI_ROM
SPI_SO_KBC R2413 Do Not Stuff SPI_SO_ROM
SPI_CLK_KBC R2411 Do Not Stuff SPI_CLK_ROM

SYS_PWROK(S0_PWR_GOOD) ==DELAY 99ms

3D3V_AUX_KBC_AVCC
L2407 BLM15AG121SN-1GP
C2421 C2424 C2425 C2426 C2420 C2416 C2422 C2427 CD1U16V2KX-L-GP
EC_AGND

3D3V_S0
DY
TOUCH_EN R2401 Do Not Stuff
Pull-high 102B

3D3V_AUX_KBC
BAT_SCL BAT_SDA RN2406 100KR2J-4-GP
ECRST# R2404 100KR2J-2-GP
USB_PWR_EN# R2405 Do Not Stuff DY

GPIO0 High Active
PROCHOT_EC Q2404 2N7002K-2-GP PROCHOT#_CPU
R2409 100KR2F-L3-GP
84.2N702.J31
2ND = 084.27002.0L31
3rd = 084.06587.0031

L2401 BLM15AG121SN-1GP EC_AGND
AD_OFF R2453 100KR2J-3-GP DY
SS_ENABLE R2452 100KR2J-3-GP DY
3D3V_AUX_KBC
BAT_INH RN2405 SRN100KJ-GP

20160920 -1M

3D3V_AUX_KBC
R2428 64KR2F-1-GP
PCB_VER_AD
R2427 100KR2F-L3-GP
EC_AGND

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
Reserved for project use -1M	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.756 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.524 V	< 1.756 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.374 V	>= 1.281 V	< 1.524 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.062 V	>= 0.524 V	< 1.126 V

Model_ID
3D3V_AUX_KBC
R2434 10KR2F-L1-GP
MODEL_ID_AD

Model_ID	High	Low
Ironhide_APL_11	V	
Drift_APL_13		V

3D3V_AUX_KBC
R2425 100KR2F-L3-GP 45W
ADT_TYPE_AD
R2430 20KR2F-L3-GP 45W
EC_AGND

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	NA	100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K	NA	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.305 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.559 V	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.831 V	>= 0.684 V	< 0.937 V
135W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.937 V	< 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.315 V	>= 1.177 V	< 1.366 V
Reserved	76.8 K	100.0 K	1.433 V	1.450 V	>= 1.366 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.542 V	< 1.842 V

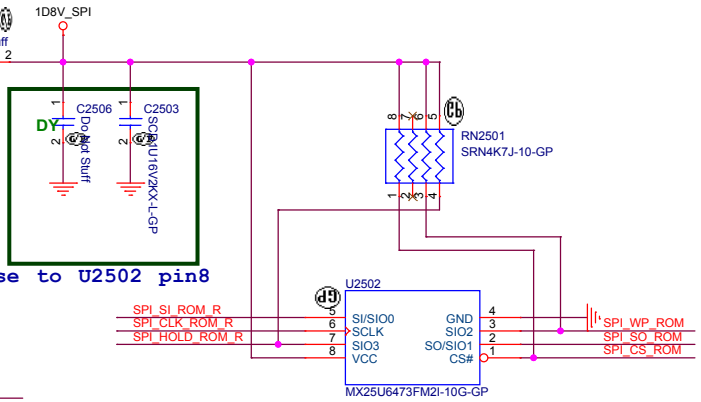
EMMC

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC_KB9028
Size: Custom
Document Number: Ironhide_APL
Rev: -1M
Date: Thursday, September 22, 2016
Sheet 24 of 106

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

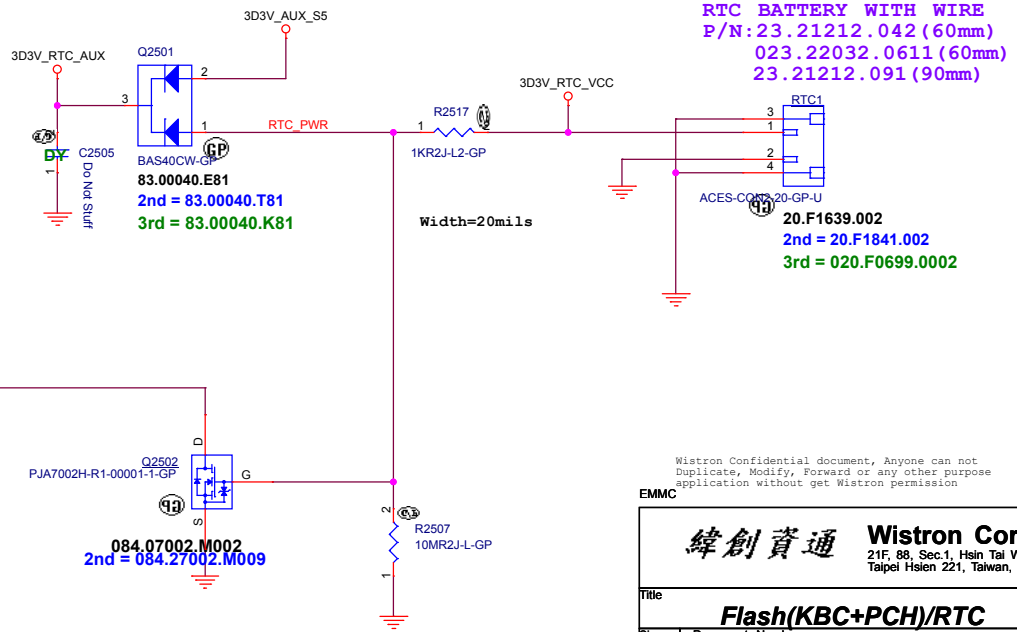


19,24 SPI_SO_ROM
19,24 SPI_SI_ROM
19,24 SPI_CS_CPU_N0
19,24,90 SPI_CLK_ROM
19 SPI_HOLD_ROM
19 SPI_WP_ROM

SPI_SI_ROM	R2511	Do Not Stuff	SPI_SI_ROM_R
SPI_CS_CPU_N0	R2513	Do Not Stuff	SPI_CS_ROM
SPI_CLK_ROM	R2514	Do Not Stuff	SPI_CLK_ROM_R
SPI_HOLD_ROM	R2515	Do Not Stuff	SPI_HOLD_ROM_R

BOM use MX25U6473FM2I-10G-GP
1st = 072.25647.0001
2nd = 072.25Q64.0E01 1.8V
3rd = 072.02564.0A01

SSID = RBAT



21 RTC_DET#

EMMC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash(KBC+PCH)/RTC

Size	Document Number	Rev
Custom	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 25 of 106

24 VD_IN1

24,89 FAN1_PWM

24,89 FAN_TACH1

24,40 PURE_HW_SHUTDOWN#

24 VD_OUT1

40 IMVP_PWRGD

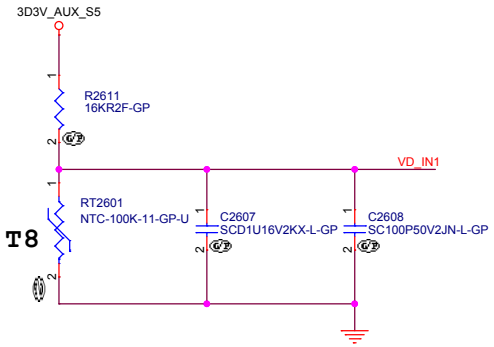
89 FAN_TACH1_C

18,46 PMIC_THERMTRIP#

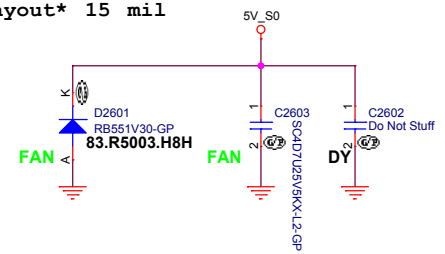
18,24,54,61,68,89 PLT_RST#

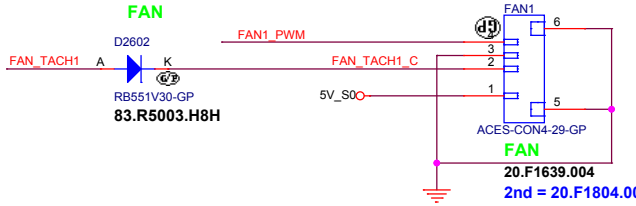
SSID = Thermal

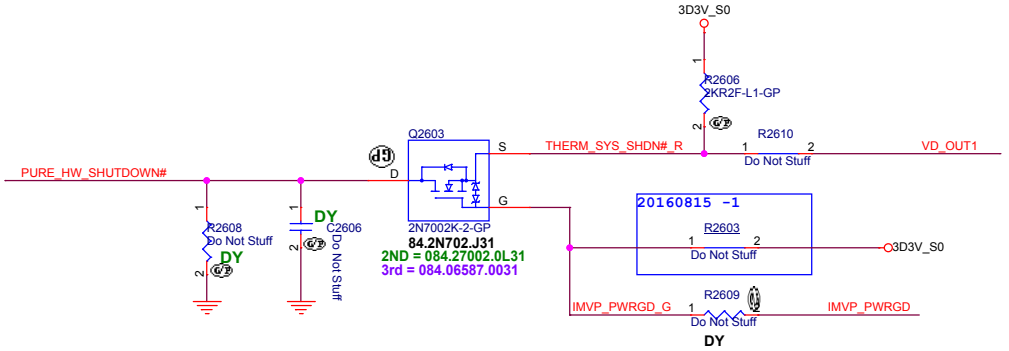
Layout 15 mil

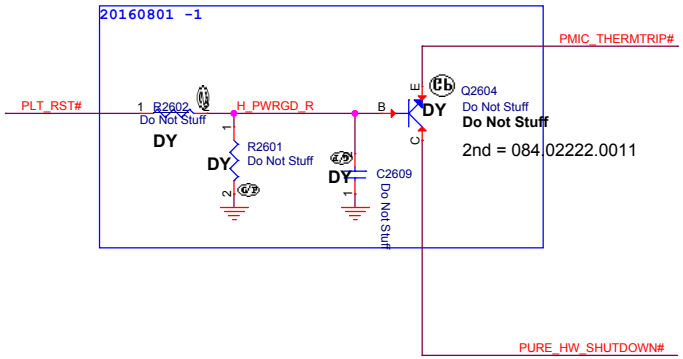


RT2601 close CPU and Vcore chock









EMMC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal 7718/Fan Controllor P2793

Size	Document Number	Rev
A3	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 26 of 106

SSID = AUDIO

29 AUD_HP1_JACK_L2
29 AUD_HP1_JACK_R2
24 AMP_MUTE#
29 AUD_SPK_L+
29 AUD_SPK_L-
29 AUD_SPK_R-
29 AUD_SPK_R+
55 DMIC_DATA_CON
55 DMIC_CLK_CON
21,90 HDA_SDOUT_CODEC
21,90 HDA_BITCLK_CODEC
21,90 HDA_SDIN0_CPU
21 HDA_SYNC_CODEC
19 HDA_RST#_CODEC
29 AUD_HP1_JD#
27,29,89 SELEEVE
27,29,89 RING2
24 KBC_BEEP
21 HDA_SPKR
21 HDA_SDIN0_CODEC

EC2701 1DY Do Not Stuff
EC2702 1DY Do Not Stuff
AUD_AGND

G2703 G2701 G2702 Do Not Stuff
AUD_AGND close to codec IC

placed nearby codec PIN12

C2725 SCD1U16V2KX-L-GP
AUDIO_PC_BEEP KBC_BEEP_C
RN2704 SRN47K-2-GP-U
KBC_BEEP HDA_SPKR
R2730 10KR2F-L1-GP

3D3V_S0 C2701 SC4D7U6D3V3KX-L-GP Close pin36
1D5V_S0 R2766 Do Not Stuff
1D5V_AVDD_S0 C2715 SC4D7U6D3V3KX-L-GP Close pin40
AUD_AGND

AUD_HP1_JACK_L2
AUD_HP1_JACK_R2
3V_MIC2V
AUD_AGND
C2704 SC2D2U6D3V3KX-L-GP
R2711 100KR2F-L3-GP
C2705 SC10U6D3V3MX-L-GP
C2702
R2748 Do Not Stuff
3D3V_S0 C2714
C2703 SC10U6D3V3MX-L-GP
5V_PVDD2 R2755 Do Not Stuff 5V_S0
AUD_AGND

5V_PVDD2 C2711 SC10U6D3V3MX-L-GP
C2710 SCD1U16V2KX-L-GP
Layout Note: Place close to Pin 26

RN2703 SRN4K7J-8-GP
LINE1_VREFO_L LINE1_VREFO_R
3V_MIC2V
RN2702 SRN2K2J-5-GP
3D3V_S5

U2701
CBP C2712 SC10U6D3V3MX-L-GP AUD_AGND
LDO2_CAP
1D5V_AVDD_S0
5V_PVDD
AUD_SPK_L+ AUD_SPK_L- AUD_SPK_R- AUD_SPK_R+
SPK-OUT-L+ SPK-OUT-L- SPK-OUT-R- SPK-OUT-R+
PVDD1 PVDD2 PDB SPDIF-OUT/GPIO2 GND
AMP_MUTE# R2754 Do Not Stuff 5V_PVDD
EAPD#
071.00255.0003
ALC255-CG-GP-U

LINE1_L C2723 SC4D7U6D3V3KX-L-GP AUD_HP1_JACK_L2
LINE1_R C2724 AUD_HP1_JACK_R2
R2712 Do Not Stuff
V33_STB
MIC_CAP C2713 SC10U6D3V3MX-L-GP
AUD_AGND
3D3V_S5

R2708 is need to connect.To prvent the beep sound

AUD_SENSE_A R2713 200KR2F-L3-GP AUD_HP1_JD#
Layout Note: Place close to Pin 13

SELEEVE 27,29,89
RING2 27,29,89
Layout Note:
Width>40mil, to improve Headpohone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.

3D3V_AUDIO_DVDD C2717 SC10U6D3V3MX-L-GP C2716 SCD1U16V2KX-L-GP
Close to Pin1

3D3V_S0 R2720 Do Not Stuff 3D3V_AUDIO_DVDD
DVDD_IO R2714 Do Not Stuff 1D8V_S0
20160801 -1
C2720 SC10U6D3V3MX-L-GP

AUD_SENSE_A R2722 100KR2F-L3-GP 3D3V_S0

ED2701 AZ5125-02S-R7G-GP
75.05125.07D
2nd = 075.08212.007D

EMC solution
DMIC_DATA_CON
DMIC_CLK_CON EL2701 MCB1005S601FBP-GP-U DMIC_CLK_AUD
close to CODEC
AUDIO_PC_BEEP
HDA_SDOUT_CODEC
HDA_BITCLK_CODEC
HDA_SDIN0_CPU R2718 33R2J-L1-GP HDA_SDIN0_CODEC
HDA_SYNC_CODEC
HDA_RST#_CODEC

AUD_HP1_JACK_L2
AUD_HP1_JACK_R2
ED2702 AZ5125-02S-R7G-GP
75.05125.07D
2nd = 075.08212.007D

5V_S0 R2719 Do Not Stuff 5V_PVDD
C2709 C2708 SCD1U16V2KX-L-GP SC10U6D3V3MX-L-GP
Close to Pin46

C2707 C2706 SCD1U16V2KX-L-GP SC10U6D3V3MX-L-GP
Close to Pin41

EMMC

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC255
Size: A2
Document Number: Ironhide_APL
Rev: -1M
Date: Wednesday, September 21, 2016
Sheet 27 of 106

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EMMC

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 28 of 106

89 AUD_SPK1_L-_CON
89 AUD_SPK1_L+_CON
89 AUD_SPK1_R-_CON
89 AUD_SPK1_R+_CON

89 AUD_HP1_JD#_R
89 AUD_HP1_JACK_R1
89 AUD_HP1_JACK_L1
89 AUD_HP1_JD#_TYPE

27 AUD_SPK_L-
27 AUD_SPK_L+
27 AUD_SPK_R-
27 AUD_SPK_R+

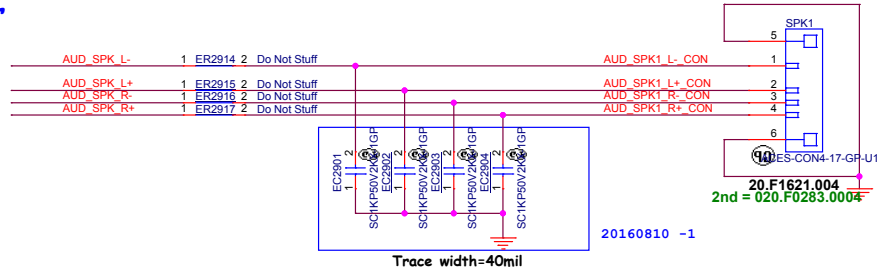
27 AUD_HP1_JD#

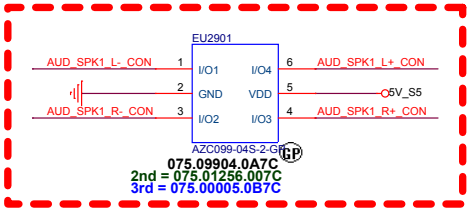
27,89 RING2
27 AUD_HP1_JACK_L2

27 AUD_HP1_JACK_R2
27,89 SELEEVE

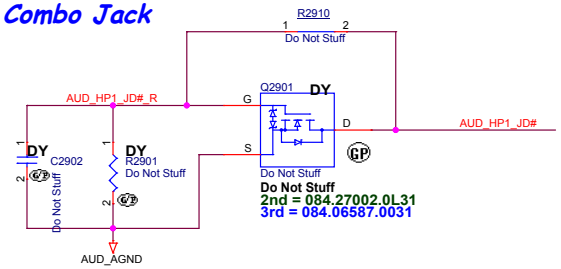
SSID = AUDIO

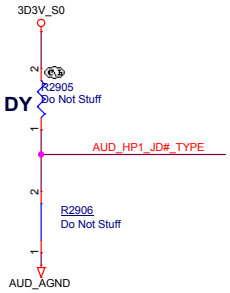
Speaker

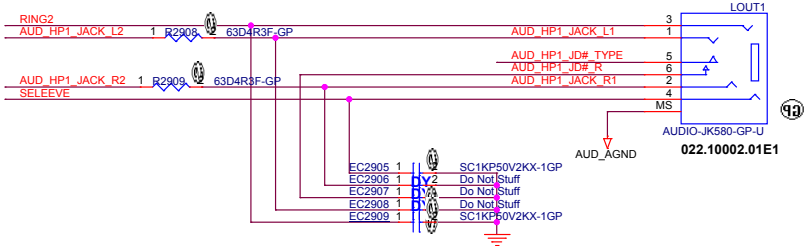




Combo Jack







EMMC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Speaker/HPMIC**

Size: Custom | Document Number: **Ironhide_APL** | Rev: **-1M**

Date: Wednesday, September 21, 2016 | Sheet 29 of 106

Blanking

EMMC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
LAN(RTL8111)

Size	Document Number	Rev
A	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 30 of 106

Blanking

EMMC

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(LAN+VGA) CONNECTOR

Size	Document Number	Rev
A	Ironhide_APL	-1M
Date: Wednesday, September 21, 2016	Sheet 31 of 106	

Blanking

EMMC

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RTS5170(CARD READER)

Size	Document Number	Rev
A4	**Ironhide_APL**	**-1M**

Date: Wednesday, September 21, 2016 Sheet 32 of 106

SSID = SDIO

SD//MS Card Reader

Blanking

EMMC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN

Size	Document Number	Rev
A4	Ironhide_APL	-1M

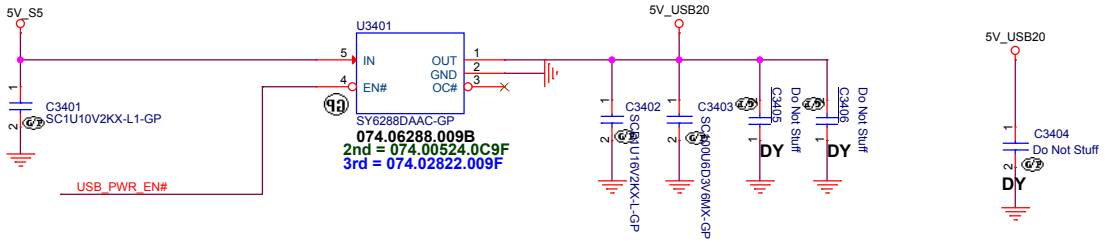
Date: Wednesday, September 21, 2016 Sheet 33 of 106

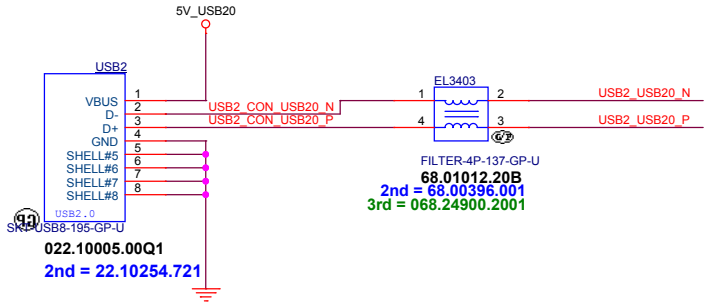
24,35 USB_PWR_EN#

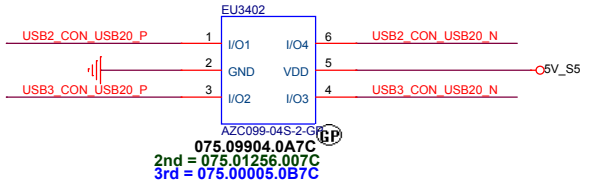
17 USB2_USB20_N
17 USB2_USB20_P
17 USB3_USB20_N
17 USB3_USB20_P

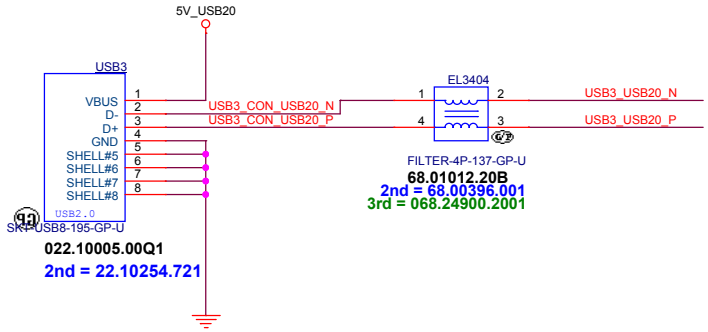
89 USB2_CON_USB20_N
89 USB2_CON_USB20_P
89 USB3_CON_USB20_N
89 USB3_CON_USB20_P

Low Active 2A









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Title: ***USB2.0***

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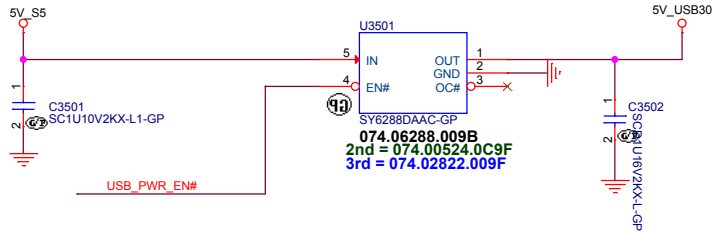
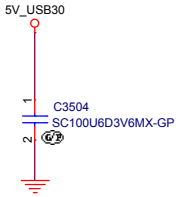
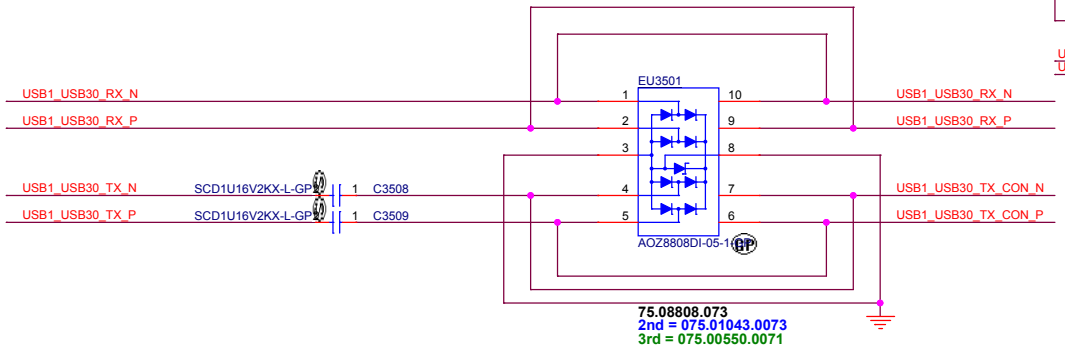
24,34 USB_PWR_EN#
17 USB1_USB20_N
17 USB1_USB20_P
16 USB1_USB30_RX_N
16 USB1_USB30_RX_P
16 USB1_USB30_TX_N
16 USB1_USB30_TX_P
89 USB1_CON_USB20_N
89 USB1_CON_USB20_P

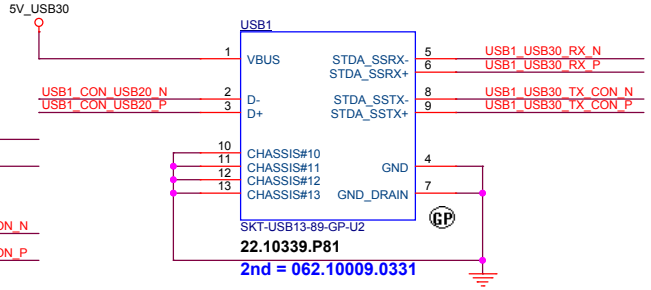
Low Active 2A

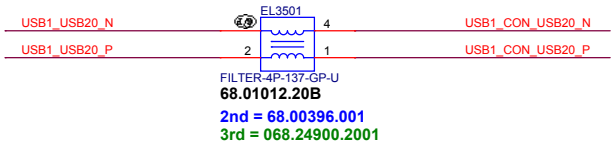


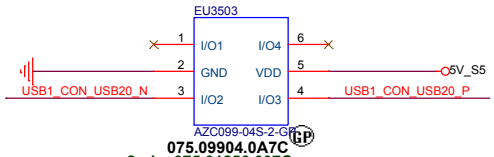


USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+









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Title: USB 3.0

Size: A3 | Document Number: Ironhide_APL | Rev: -1M

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Title	***Reserved***	
Size: A	Document Number: **Ironhide_APL**	Rev: **-1M**
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Title
ADAPTER OCP / S3 reduction

Size	Document Number	Rev
A4	Ironhide_APL	-1M
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Title: *USB HUB*

Size	Document Number	Rev
Custom	Ironhide_APL	-1M

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Title

Reserved

Size	Document Number	Rev
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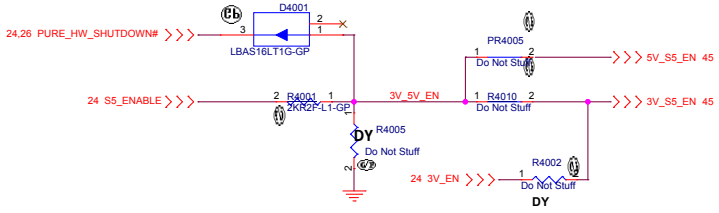
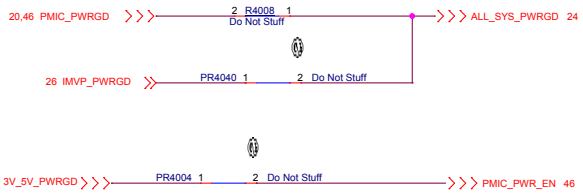
SSID = Reset.Suspend

Power Sequence



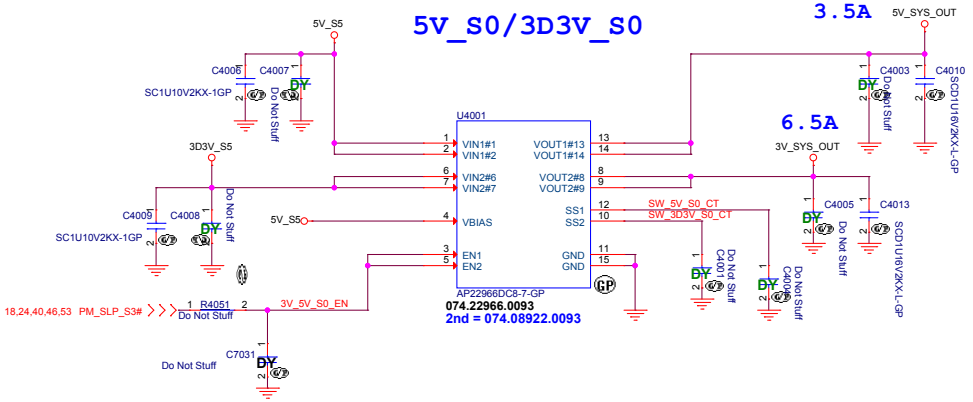
ALL_SYS_PWRGD

To EC

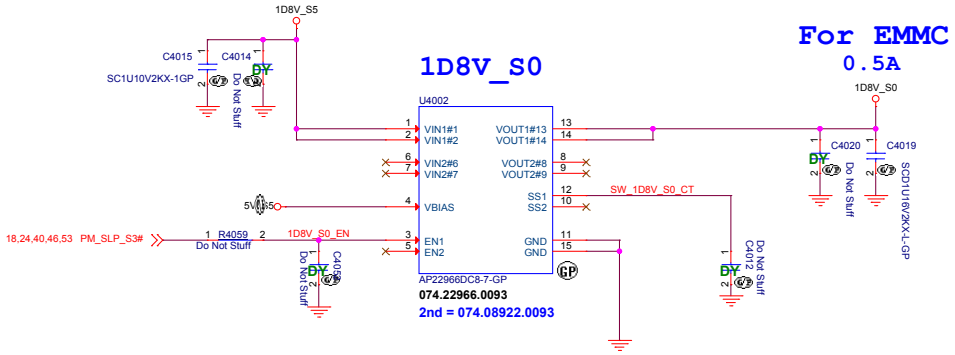


RUN Power

5V_S0/3D3V_S0

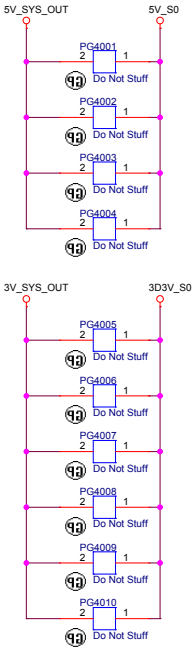


1D8V_S0



For EMMC

0.5A



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Title: Power Plane Enable & SEQUENCE		
Size: Custom	Document Number: Ironhide_APL	Rev: -1M
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Title	***Reserved***	
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ANNIE solution

Blanking

EMMC

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Title: ***Reserved***

Size	Document Number	Rev
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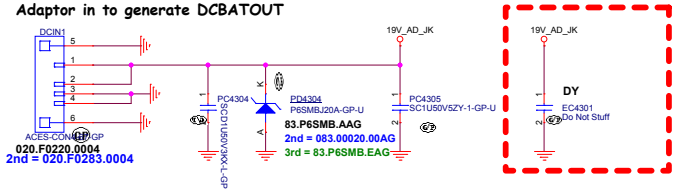
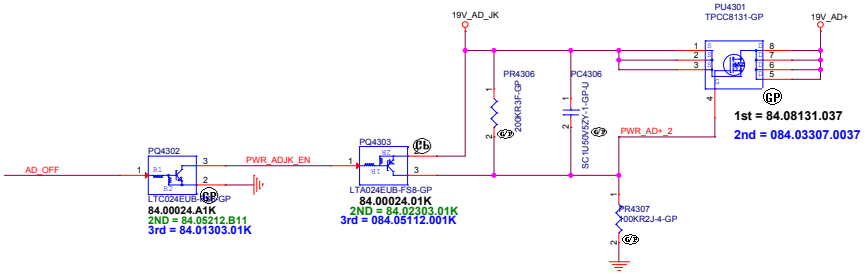
ANNIE solution

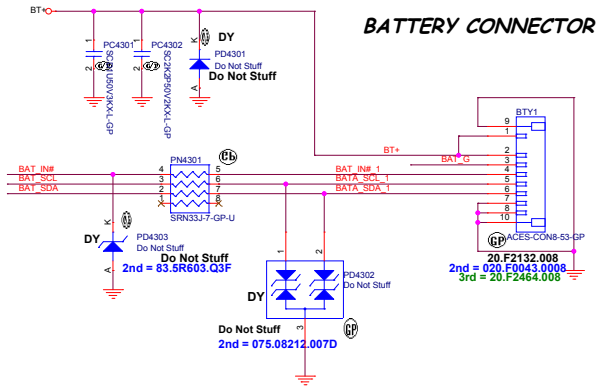
Adaptor in to generate DCBATOUT

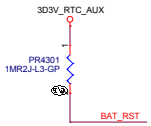




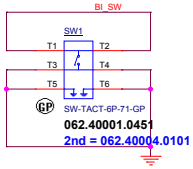
24 AD_OFF

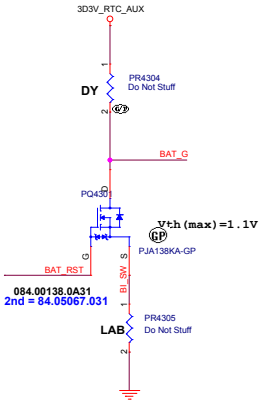
BATTERY CONNECTOR





Battery Insert





24 BAT_IN#
24,44 BAT_SCL
24,44 BAT_SDA
89 BAT_G
89 BAT_IN#_1
89 BATA_SCL_1
89 BATA_SDA_1
64 BAT_RST

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Title: BATT CONN		
Size: A2	Document Number: Ironhide_APL	Rev: -1M
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SSID = Charger

CHARGER ENABLE CONTROL

24,44 CHG_ON#

Others

24,43 BAT_SCL
24,43 BAT_SDA
24,44 AC_IN#
24,44 AD_IA
18,24,44 PROCHOT#_CPU

Id= -10A
Qg= -22nC
Rdson=14~22mohm

PU4407 TPCC8131-GP
1st = 84.08131.037
2nd = 084.03307.0037

PR4403 100KR2J-1-GP
PR4404 10KR2F-2-GP
PR4405 49K9R2F-L-GP
PQ4402 2N7002KDW-GP
84.2N702.A3F
2nd = 075.67002.007C

PG4402 Do Not Stuff
PG4401 Do Not Stuff
PC4402 SCD1U50V3KX-L-GP
PC4403 SCD1U50V3KX-L-GP
PC4404 SCD1U50V3KX-L-GP

PU4408 TPCC8131-GP
1st = 84.08131.037
2nd = 084.03307.0037
Id= -10A
Qg= -22nC
Rdson=14~22mohm
PC4419 is close to PU4401 PIN#4
PR4406 470KR2J-2-GP
SC1KP50V2KX-L-1-GP

PR4414 20R5F-1GP
PR4407 20R5F-1GP
PC4408 SC1U50V5ZY-1-GP-U

PU4404 HPA02224RGRR-1-GP
74.02224.073

PR4408 324KR2F-GP
PR4412 49K9R2F-L-GP
PC4411 SCD01U50V2KX-L-GP
PR4425 100KR2J-4-GP
PR4410 60K4R2F-GP
PR4416 3D3M2J-GP
PR4413 100KR2F-L1-GP
PR4411 Do Not Stuff
PR4415 Do Not Stuff

PD4401 RB520SM-30T2R-GP
PR4409 1D5R2F-GP
PC4410 SCD1U50V3KX-L-GP
PC4409 SC1U10V2KX-L1-GP

PU4403 AON7410-GP
PU4409 AON7410-GP
84.07410.A37
2nd = 84.08067.A37

PC4405 SCD1U25V2KX-L-GP
PC4406 SC10U25V6KX-GP
PC4407 Do Not Stuff

Charger Current=1.4~3.6A

PL4401 IND-4DYUH-173-GP-U
68.4R71C.10K
2nd = 68.4R71A.20H
PR4417 D01R3721F-GP-U
PG4403 Do Not Stuff
PG4404 Do Not Stuff
PC4412 SC10U25V5KX-GP
PC4413 Do Not Stuff
PC4421 SC10U25V5KX-GP
PC4422 Do Not Stuff
PC4414 SCD1U25V2KX-L-GP

PR4418 10R2F-L-GP
PR4420 7D5R2F-GP
PR4422 Do Not Stuff
PC4415 Do Not Stuff
PC4416 SCD1U50V3KX-L-GP
PC4417 SCD1U16V2KX-L-GP
PC4418 SCD1U25V2KX-L-GP

PR4419 100KR2J-1-GP
PR4423 Do Not Stuff
PQ4401 2N7002K-2-GP
84.2N702.J31
2nd = 084.27002.0L31
3rd = 084.06587.0031
PR4424 100KR2J-1-GP
PR4421 Do Not Stuff
PR4427 100KR2J-1-GP
PR4428 100KR2J-1-GP
PQ4404 2N7002K-2-GP
84.2N702.J31
2nd = 084.27002.0L31
3rd = 084.06587.0031

	Stat	FM_SLP_A#	Adaptor Current	AC_Protect.prsent (85% x 120%)	AC_Protect Current	PR4404 Sense resistor	Current to Volta...	R1 PR4407	R2 PR4401
40W	AC + Battery	High	2.1	102%	2.142	20 mOhm	0.8568	41.2	100
45W	AC + Battery	High	2.37	102%	2.4174	20 mOhm	0.96696	50.4	100
60W	AC + Battery	High	3.42	102%	3.4884	10 mOhm	0.69768	34.2	100
90W	AC + Battery	High	4.74	102%	4.8348	10 mOhm	0.96696	50.4	100
120W	AC + Battery	High	6.31	102%	6.4362	10 mOhm	1.28724	113	100
150W	AC + Battery	High	7.1	102%	7.242	10 mOhm	1.4484	180	100

AC_Protect
PQ4408 2N7002KDW-GP
84.2N702.A3F
2nd = 075.67002.007C
PR4446 Do Not Stuff
PR4442 Do Not Stuff
PC4426 Do Not Stuff
AC_Protect_R1
AC_Protect_R
18,24,44 PROCHOT#_CPU

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Title: Charger HPA02224RGRR
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5V/3V ENABLE CONTROL

40,45 5V_S5_EN

40,45 3V_S5_EN

5V/3V POWER GOOD

40 3V_5V_PWRGD

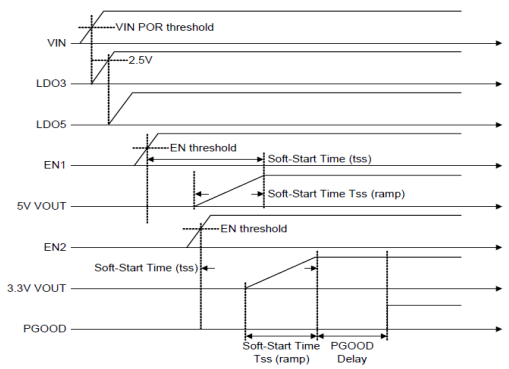

Figure 6. RT6575B Timing

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Title: RT6575D_5V/3D3V

Size: Custom | Document Number | Rev

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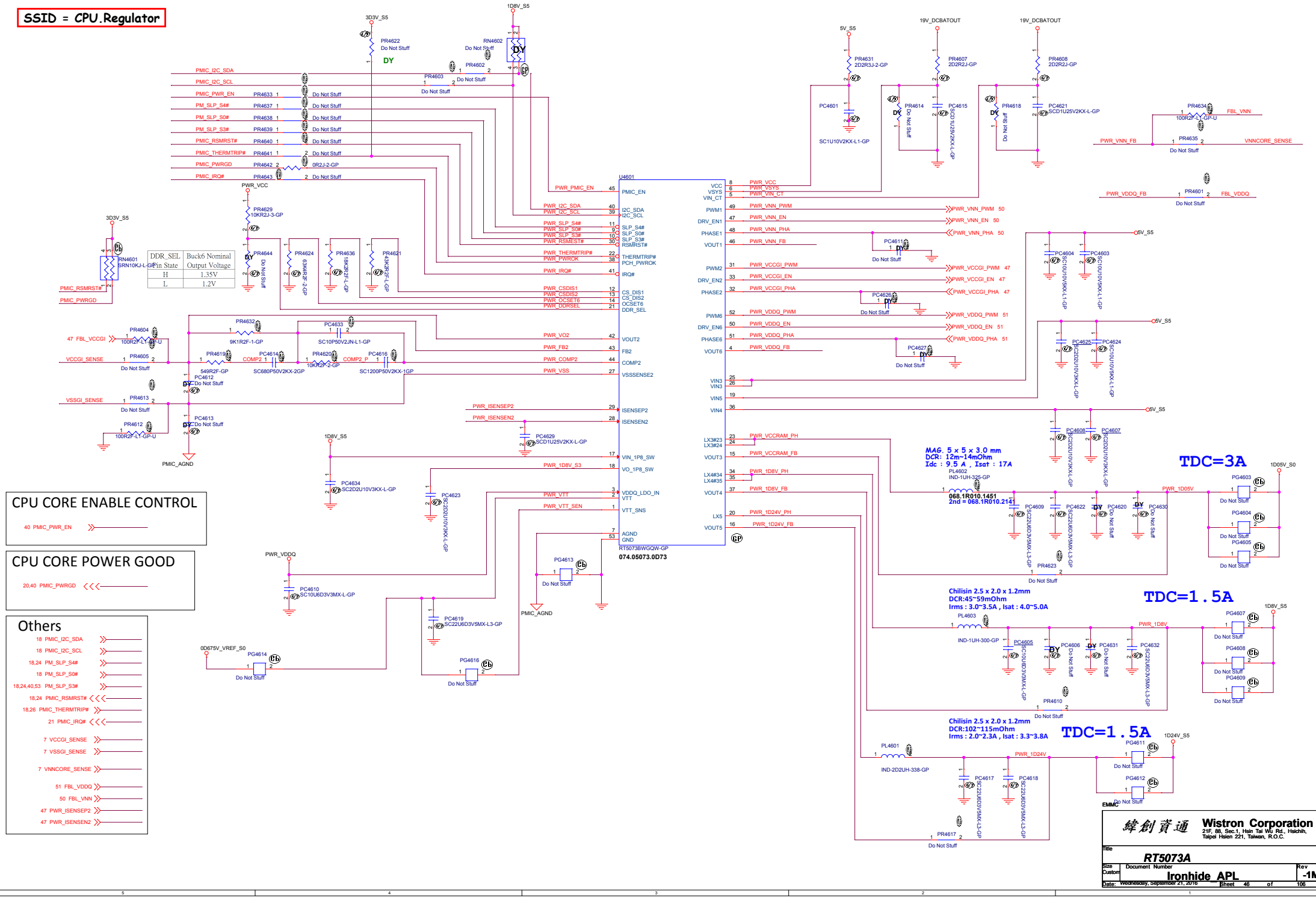
SSID = CPU.Regulator



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Title: RT5073A	
Size: Custom	Document Number: Ironhide_APL	Rev: -1M
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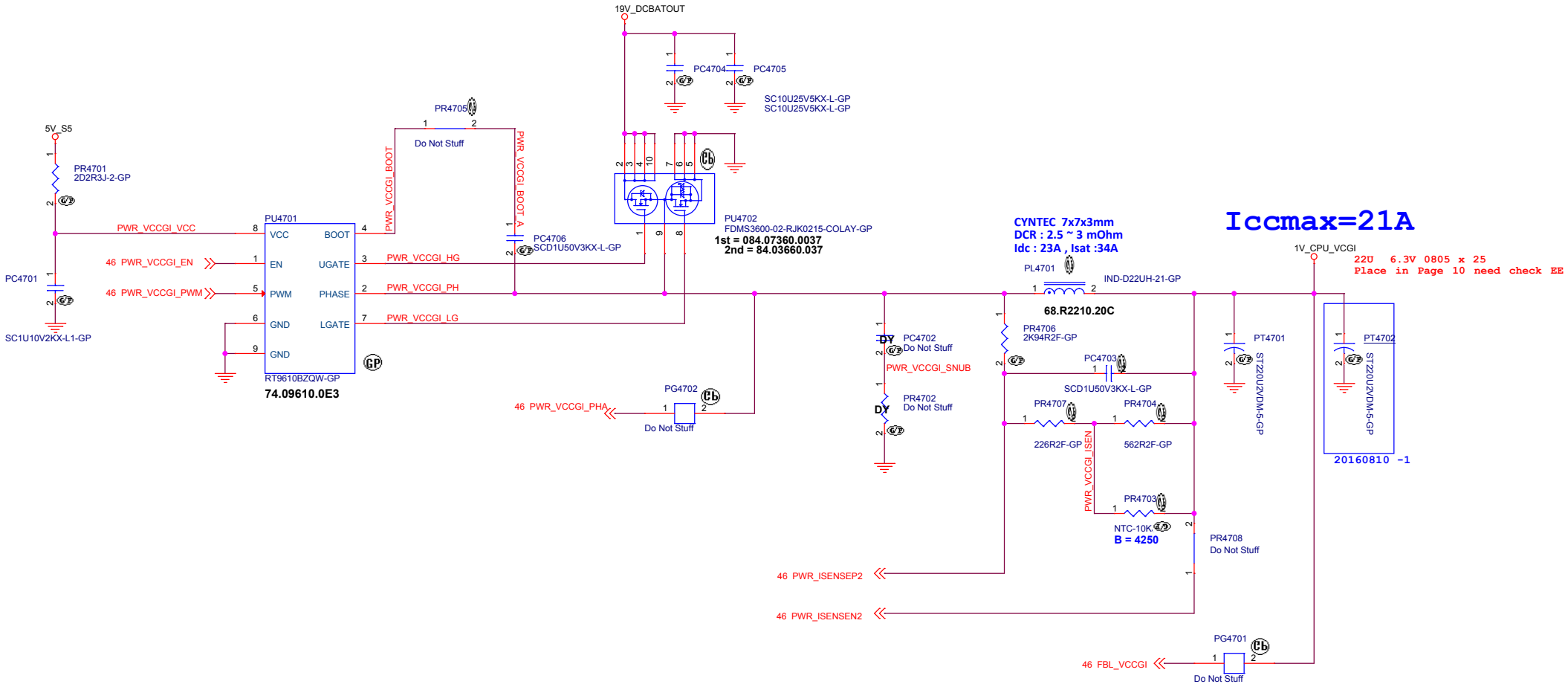

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Title: ***RT5073A_VCCGI***

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Title: RT8171B_CPUCORE(2/3)

Size: Custom | Document Number: Ironhide_APL | Rev: -1M

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Title: *Reserved*

Size: A3 | Document Number: Ironhide_APL | Rev: -1M

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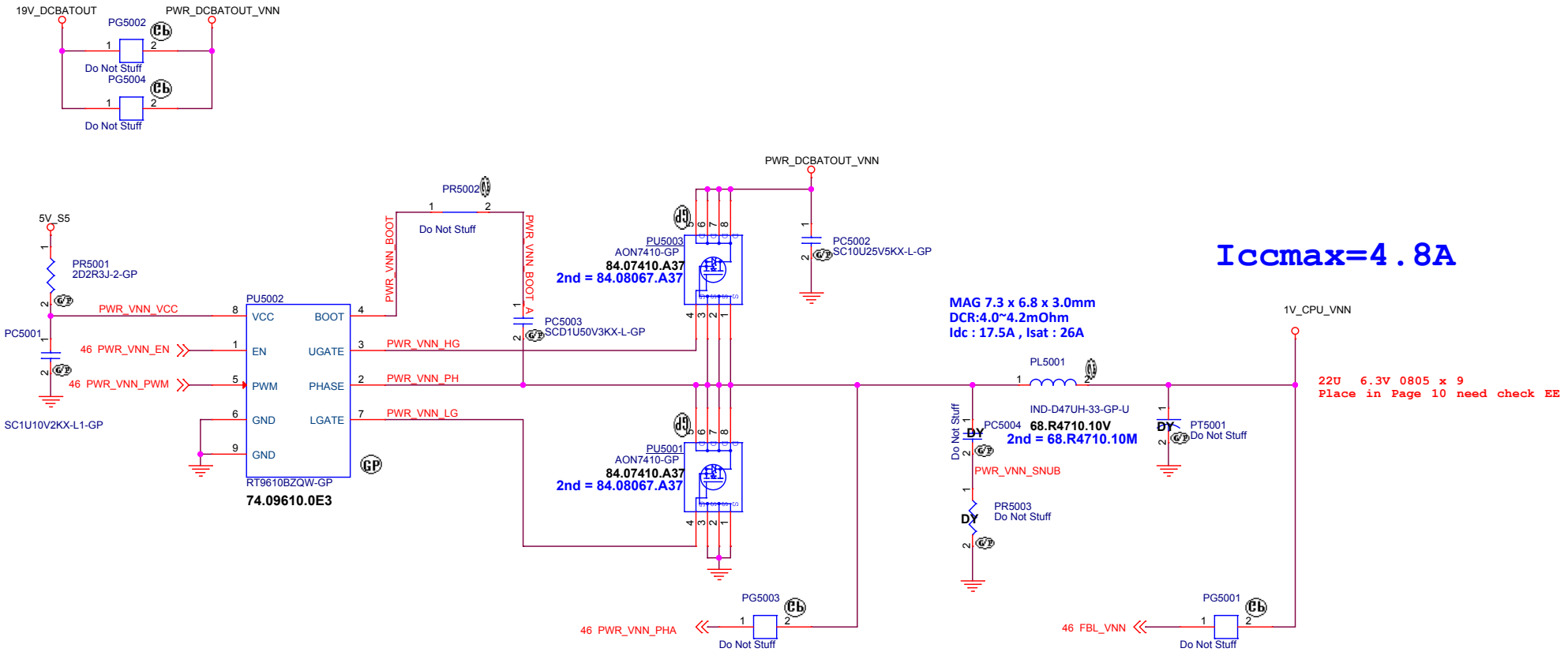

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Title: RT5073A_VNN

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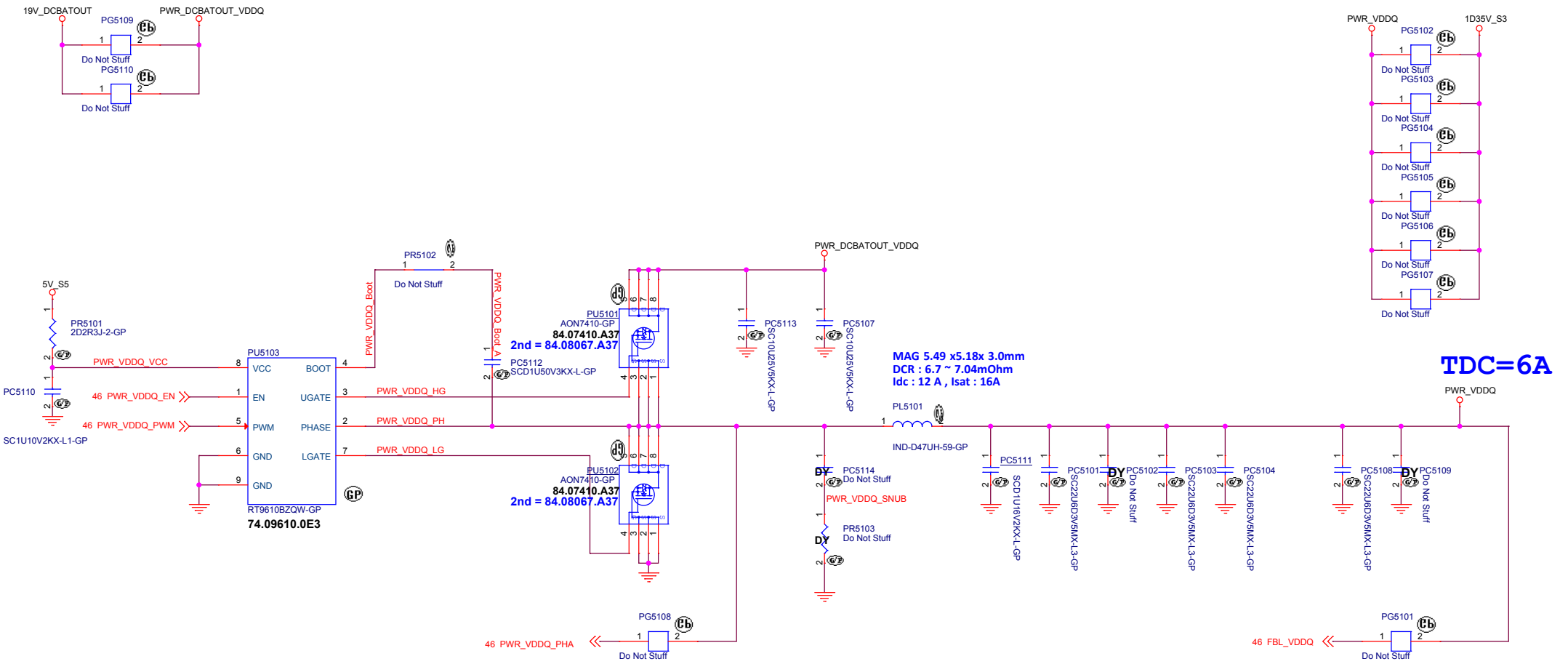

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Title: ***RT5073A_VDDQ***

Size	Document Number	Rev
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Title: *(Reserved)*

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B	Ironhide_APL	-1M

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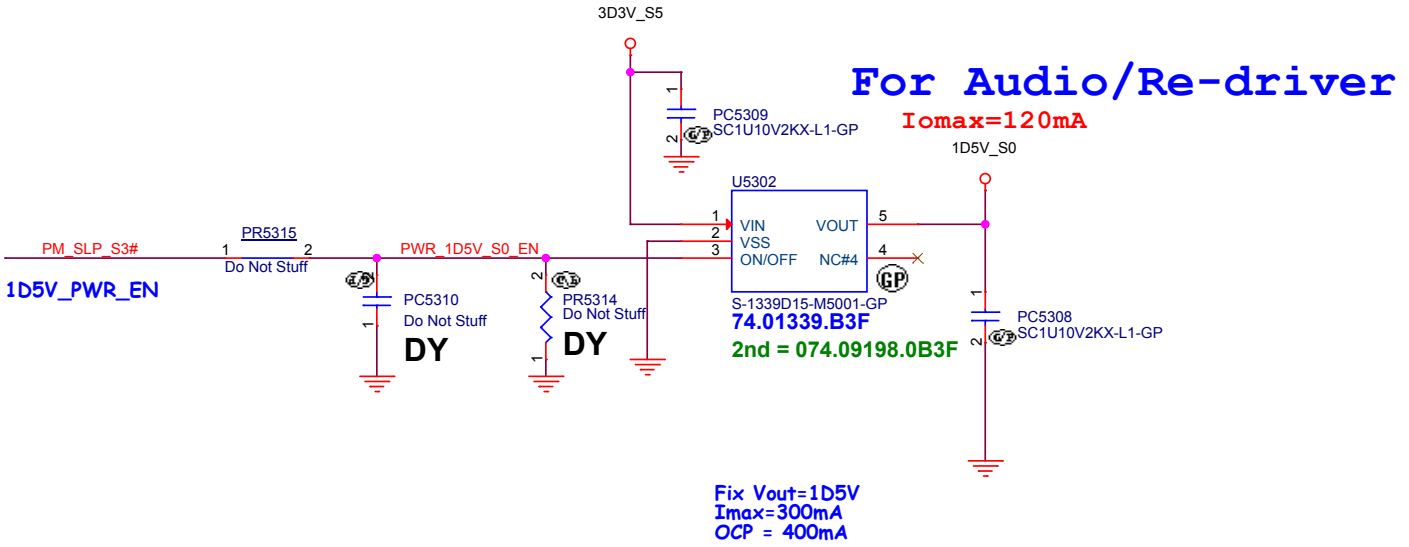
TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V

For HDMI re-driver and audio codec

18,24,40,46 PM_SLP_S3#



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Title: 1D5V_S0		
Size: Custom	Document Number: Ironhide_APL	Rev: -1M
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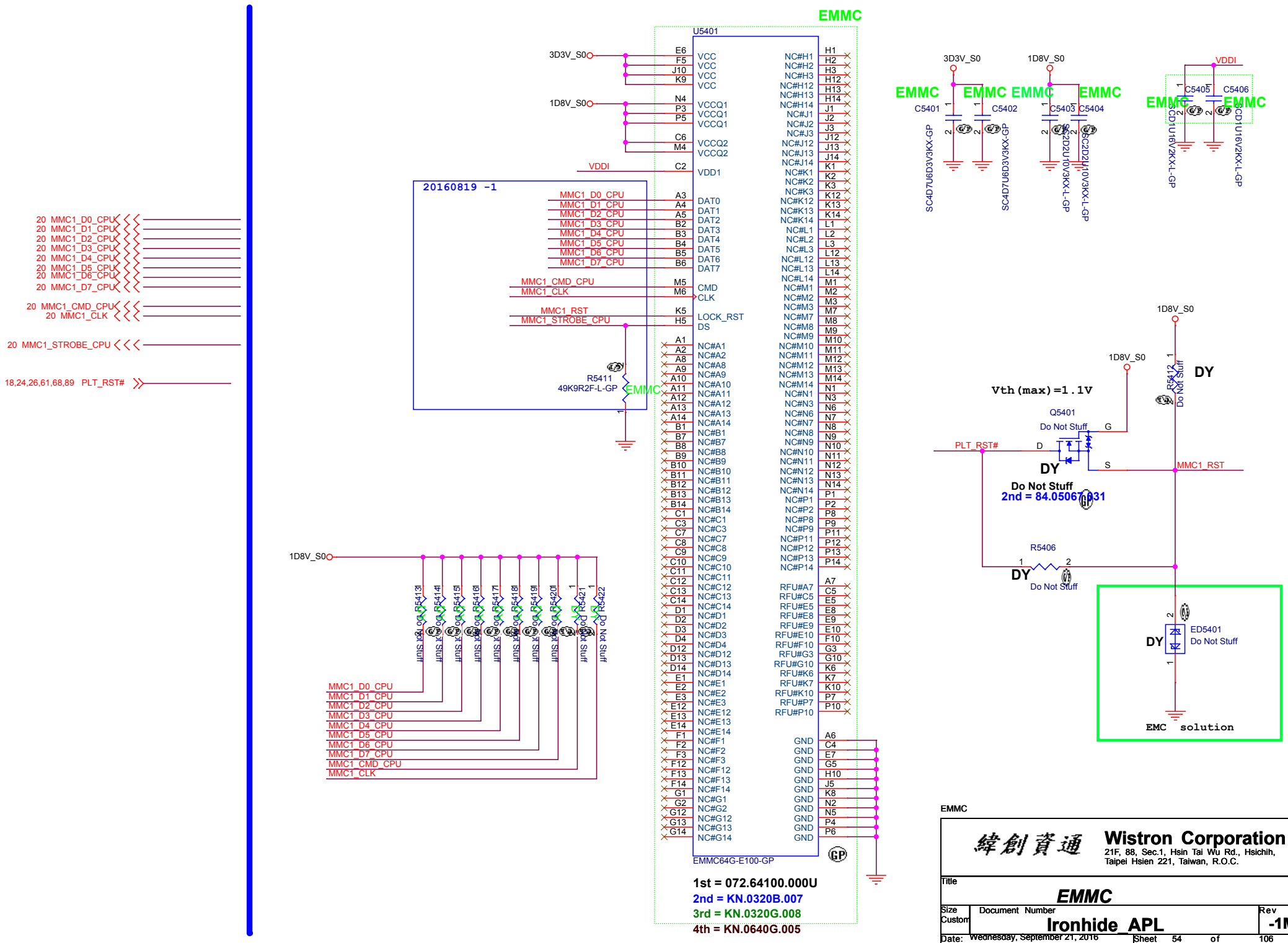

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Title: EMMC

Size	Document Number	Rev
Custom	Ironhide_APL	-1M

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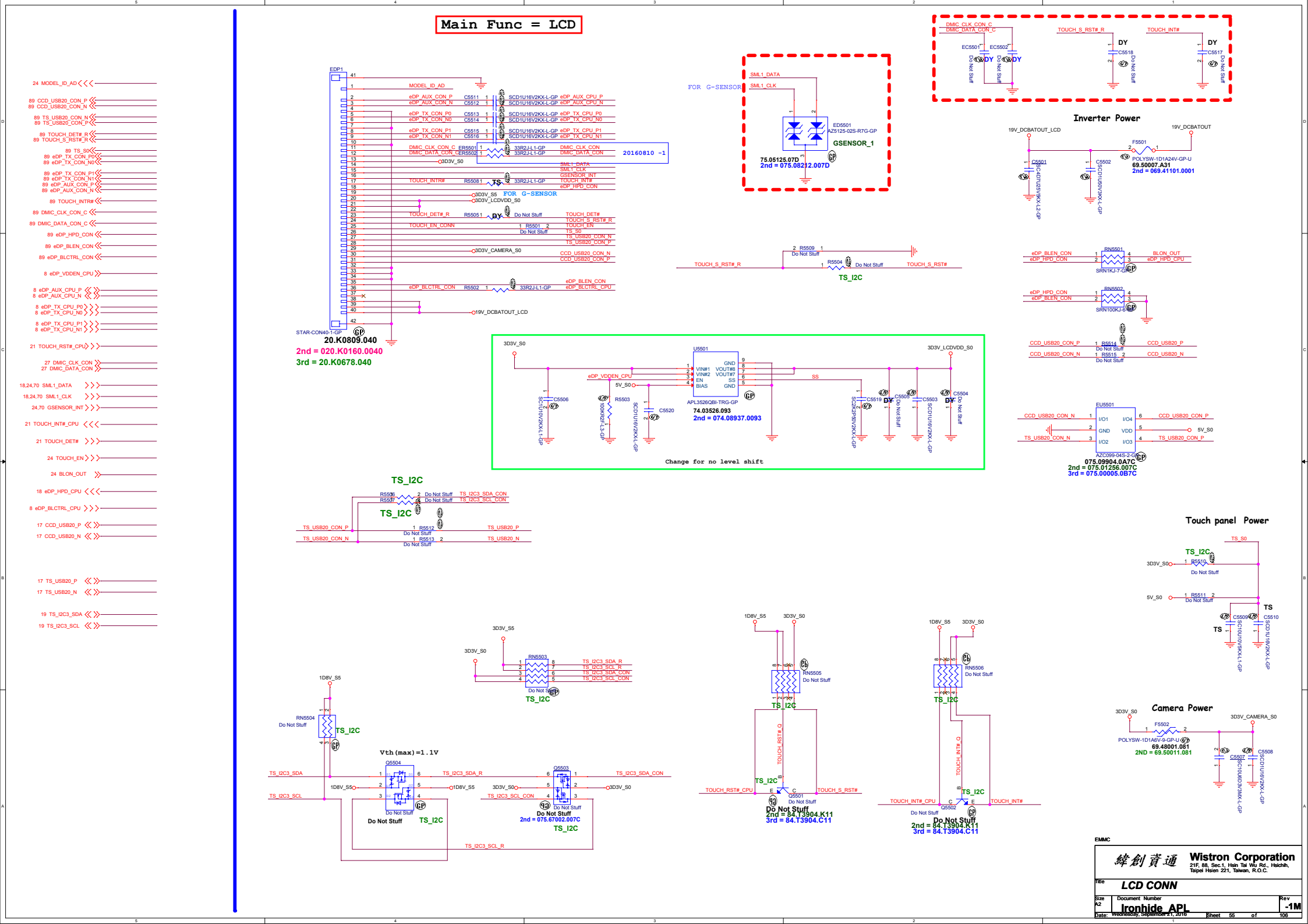
Main Func = LCD



SSID = mSATA

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EMMC

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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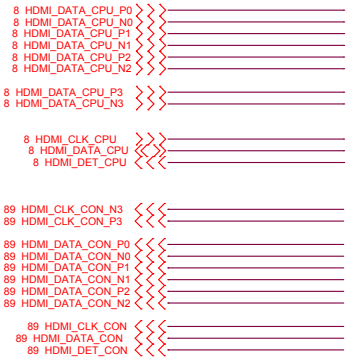
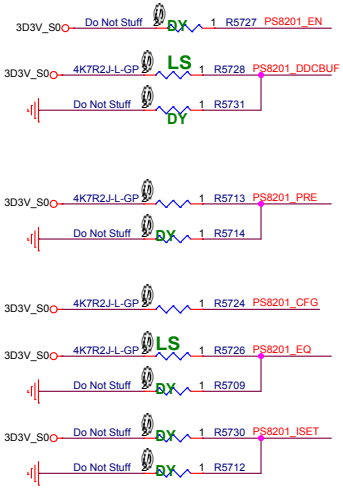
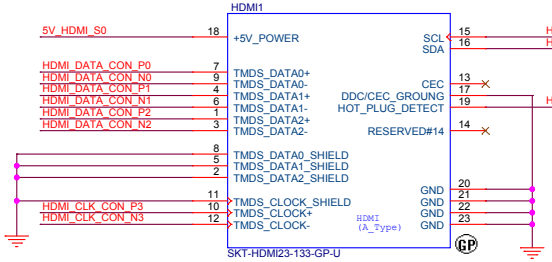
SSID = VIDEO

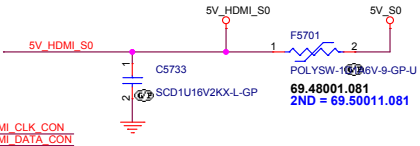
HDMI Level Shifter & CONNECTOR

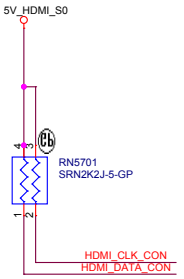
HDMI CONN

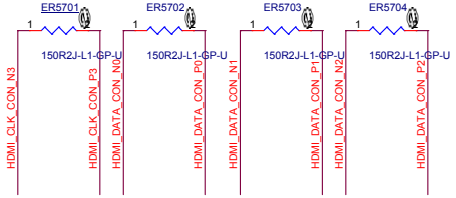


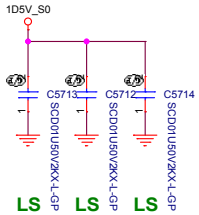


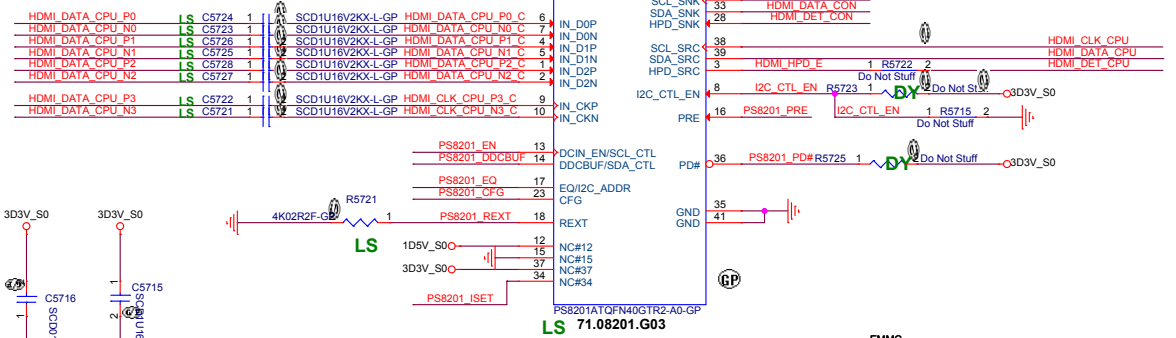


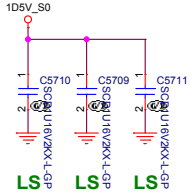












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Title: HDMI Level Shifter/Connector		
Size: Custom	Document Number: Ironhide_APL	Rev: -1M
Date: Wednesday, September 21, 2016	Sheet 57 of 106	

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Title

Hall Sensor

Size	Document Number	Rev
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Date: Wednesday, September 21, 2016 Sheet 58 of 106

SSID = 3G

Mini Card Connector(WWAN)

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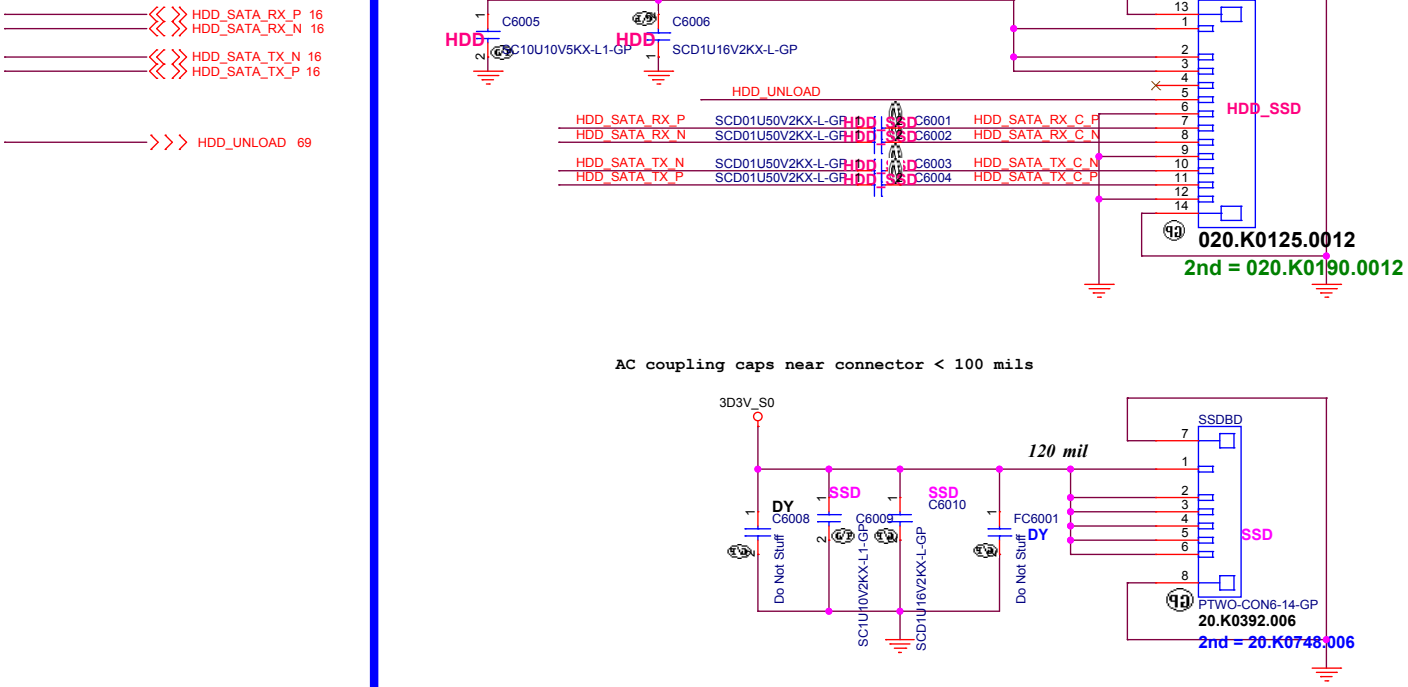
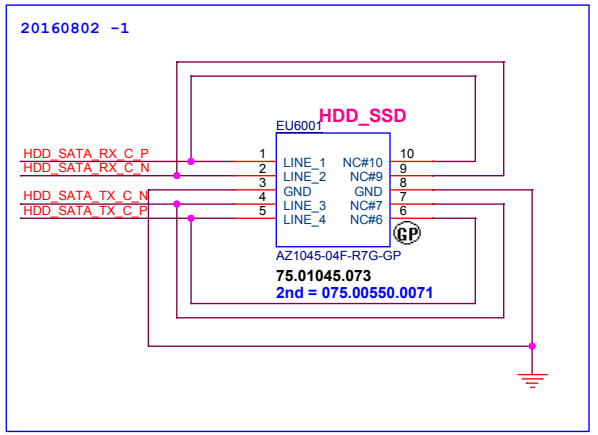
Title: WWAN CONN

Size	Document Number	Rev
A4	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 59 of 106

SSID = SATA SATA HDD Connector





AC coupling caps near connector < 100 mils

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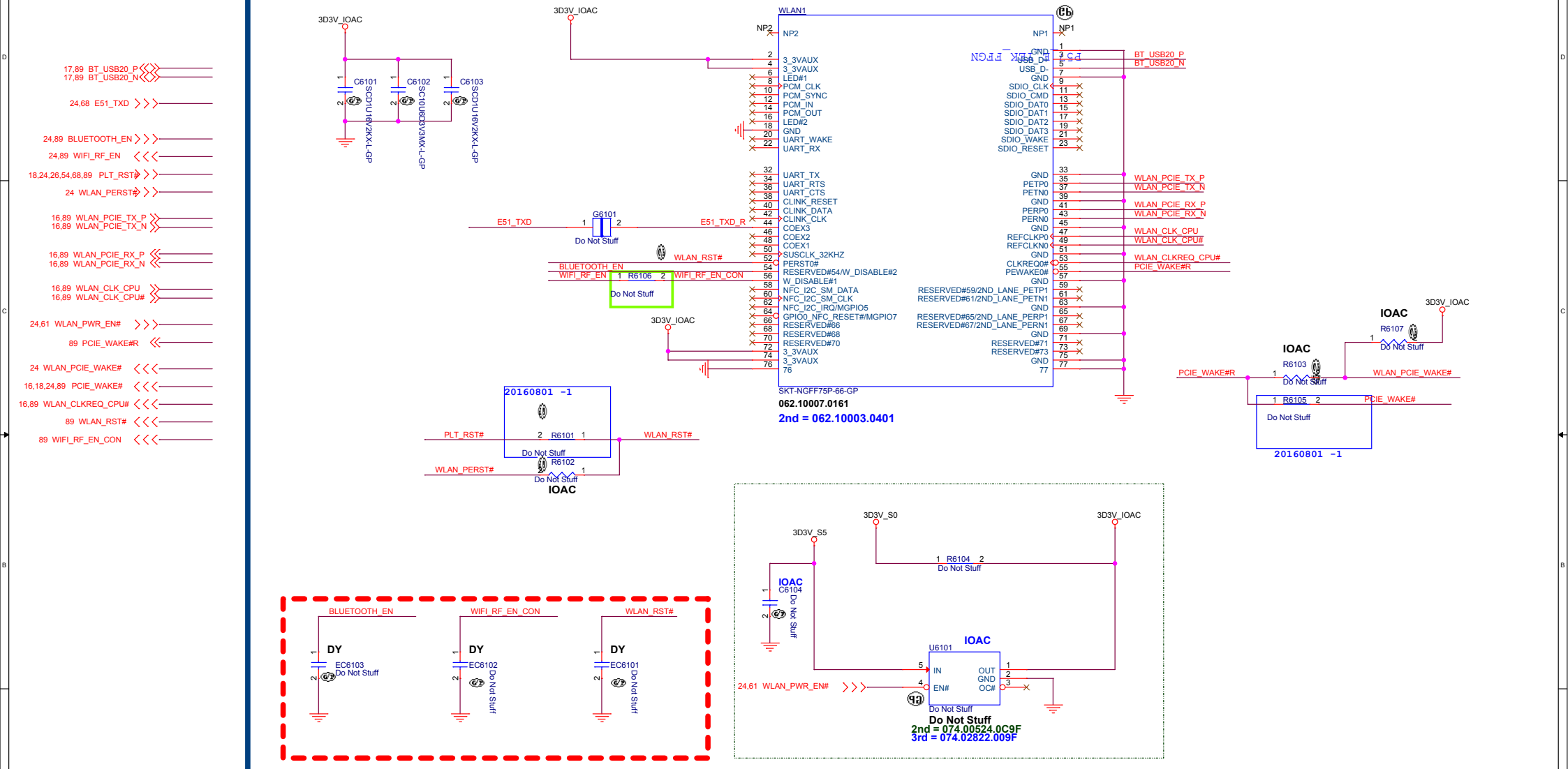
Title: HDD/SSD

Size: Custom | Document Number: Ironhide_APL | Rev: -1M

Date: Wednesday, September 21, 2016 | Sheet 60 of 106

SSID = Wireless Mini Card Connector(802.11a/b/g/n)



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Title	Mini Card-WLAN	
Size: Custom	Document Number: Ironhide_APL	Rev: -1M
Date: Wednesday, September 21, 2016	Sheet 61 of 106	

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Title: ***Audio Jack***

Size	Document Number	Rev
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Title: SSD

Size: A3 | Document Number: Ironhide_APL | Rev: -1M

Date: Wednesday, September 21, 2016 | Sheet 63 of 106

SSID = User.Interface

17 CARD1_USB20_P
17 CARD1_USB20_N
24 STDBY_LED
24 POWER_LED
24 CHARGE_LED
24 DC_BATFULL
24,89 LID_CLOSE#
24,89 LID_CLOSE2#
89 STDBY_LED#_R
89 FRONT_PWRLED#_R
89 CHARGE_LED#_R
89 DC_BATFULL#_R
18,24,89 KBC_PWRBTN#
24 Value+
24 Value-
89 Value+_R
89 Value-_R
89 CARD1_CON_USB20_P
89 CARD1_CON_USB20_N
43 BAT_RST

20160818 -1

STDBY_LED# Q — R6401 820R2F-GP — STDBY_LED#_R
FRONT_PWRLED# Q — R6402 200R2F-L-GP — FRONT_PWRLED#_R
CHARGE_LED# Q — R6403 820R2F-GP — CHARGE_LED#_R
DC_BATFULL# Q — R6405 200R2F-L-GP — DC_BATFULL#_R

Power button LED

Q6401
FRONT_PWRLED# Q — 3
STDBY_LED — 2
1 — 6 — STDBY_LED#_Q
5 — POWER_LED
Vth(max)=2.5V 2N7002KDW-GP
84.2N702.A3F
2nd = 075.67002.007C

Power STDBY_LED

RN6412
Value+ 2 — 1 Value-
4
SRN2K2J-5-GP

CARD1_USB20_P — 1 R6411 Do Not Stuff
CARD1_USB20_N — 1 R6412 2 Do Not Stuff

SMB1
STDBY_LED# R
FRONT_PWRLED# R
CHARGE_LED# R
DC_BATFULL# R
KBC_PWRBTN#
Value+_R
Value-_R
CARD1_CON_USB20_P
CARD1_CON_USB20_N
3D3V_S0
BAT_RST
5V_S5
5V_AUX_S5
ACES-CON20-29-GP-U
20.K0637.020
2nd = 020.K0190.0020

Battery LED2(DC_BATFULL)

Q6404
DC_BATFULL# Q — 3
CHARGE_LED — 2
1 — 6 — CHARGE_LED#_Q
5 — DC_BATFULL
Vth(max)=2.5V 2N7002KDW-GP
84.2N702.A3F
2nd = 075.67002.007C

LAB
PWRBT1
T1 — T2 — KBC_PWRBTN#
T5 — T6
T3 — T4
Do Not Stuff

Do Not Stuff

3D3V_S5
RN6401
Value+ 1 — 4
Value- 2 — 3
SRN100K5-4-GP

Battery LED1(CHARGE)

EU6404
1 I/O1 — I/O4 6
2 GND — VDD 5 — 5V_S5
CARD1_CON_USB20_P — 3 I/O2 — I/O3 4 — CARD1_CON_USB20_N
AZC099-04S-2-GP
075.09904.0A7C
2nd = 075.01256.007C
3rd = 075.00005.0B7C

3D3V_AUX_S5
SCD1U16V2KX-L-GP
C6401
LID1
LID_CLOSE2# — 1 — 2 OUT2 GND — OUT1 VDD — 4 — 3 — LID_CLOSE#
HGDEDM013A-GP
074.00013.00BJ
DY C6402 Do Not Stuff
DY C6403 Do Not Stuff

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Title: LED Bard/Power Button
Size: A3
Document Number: Ironhide_APL
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SSID = KBC

Internal KeyBoard Connector

24,89 KSI[0..7]
24,89 KSO[0..15]
24 EC_TPCLK
24 EC_TPDATA
24,89 FUN_OFF#
89 EC_TP_CLK_C
89 EC_TP_DATA_C
89 TP_IN#_R
24 PTP_PWR_EN#
21 TP_IN#
24 EC_TP_IN#
24 KB_BL_PWM
24 KB_BL_DET
24 EC_CAP_LED
19 TP_I2C4_SDA
19 TP_I2C4_SCL
89 TP_I2C4_SDA_CON
89 TP_I2C4_SCL_CON

KB_BL_DET_R — EC6506 DY Do Not Stuff

KB1 ACES-CON28-10-GP 020.K0173.0028

KB_BL1 PSC-CON4-GP 20.K0788.004

R6504 100KR2F-L3-GP KB_BL
R6502 200KR2F-L-3-GP KB_BL
R6521 200R2F-L-GP KB_BL
KB_LED_PWM_D
Q6501 2N7002K-2-GP 84.2N702.J31
2nd = 084.27002.0L31
3rd = 084.06587.0031
KB_BL_PWM
C6502 DY Do Not Stuff

5V_S0
C6501 DY Do Not Stuff
R6520 1KR2J-L2-GP
3D3V_S0
CAP_LED#_R
CAP_LED#2
Q6504 2N7002K-2-GP 84.2N702.J31
2nd = 084.27002.0L31
3rd = 084.06587.0031
EC_CAP_LED
R6523 Do Not Stuff
R6524 Do Not Stuff
20160816 -1

KSO0 KSO1 KSO2 KSO3 KSO4 KSO5 KSO6 KSO7 KSO8 KSO9 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15
KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7
KSI1_R KSI_R

VCC Pin 1
VCC Pin 2
GND Pin 3
GND Pin 4

KB_LED_PWM_R — R6522 Do Not Stuff DY — 5V_S0

TOUCH PAD

3D3V_TP_S3
RN6503 SRN4K7J-8-GP
RN6502 SRN33J-5-GP-U
EC_TPCLK
EC_TPDATA
EC6502 Do Not Stuff DY
EC_TP_CLK_C
EC_TP_DATA_C
TP_I2C4_SDA_CON
TP_I2C4_SCL_CON
TP_IN#_R
FUN_OFF#
TPAD1 ETY-CON-22-GP-U1 20.K0665.008
2nd = 20.K0667.008
Source have swap
To use 20.K0665.008 footprint, but BOM use : main source is 20.K0667.008
TP_IN#_R EC6507 DY Do Not Stuff
EC6501 DY Do Not Stuff
EC6503 DY Do Not Stuff

3D3V_S5
U6502 SY6288DAAC-GP 074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F
IN EN# OUT GND OC#
PTP_PWR_EN#
C6509 SC4D7U6D3V3KX-L-GP
C6504 SC4D7U6D3V3KX-L-GP

20160920 -1M

R6525 100KR2J-4-GP
R6506 100KR2J-4-GP
BTP_IN#_B
TP_IN# TP_IN#_R
Q6502 LMBT3904LT1G-GP 84.T3904.H11
2nd = 84.T3904.K11
3rd = 84.T3904.C11
EC_TP_IN# R6512 Do Not Stuff

1D8V_S5
RN6504 SRN2K2J-1-GP TP_I2C
Vth(max)=1.1V
Q6505 PJT138KA-GP 075.00138.0A7C TP_I2C
TP_I2C4_SCL
TP_I2C4_SDA

3D3V_S5
RN6505 SRN2K2J-GP TP_I2C
TP_I2C4_SCL_R
TP_I2C4_SDA_R
TP_I2C4_SDA_CON
TP_I2C4_SCL_CON
Q6503 2N7002KDW-GP 84.2N702.A3F
2nd = 075.67002.007C TP_I2C
TP_I2C4_SCL_CON — EC6504 DY Do Not Stuff
TP_I2C4_SDA_CON — EC6505 DY Do Not Stuff
TP_I2C4_SDA_R

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Title: Key Board/Touch Pad
Size: Custom
Document Number: Ironhide_APL
Rev: -1M
Date: Wednesday, September 21, 2016
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Title: ***IO/POWER BOARD CONN***

Size	Document Number	Rev
A	Ironhide_APL	-1M

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Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

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Title: G Sensor

Size	Document Number	Rev
A	Ironhide_APL	-1M

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19,24 INT_SERIRQ
19,90 LPC_CLK_DBG

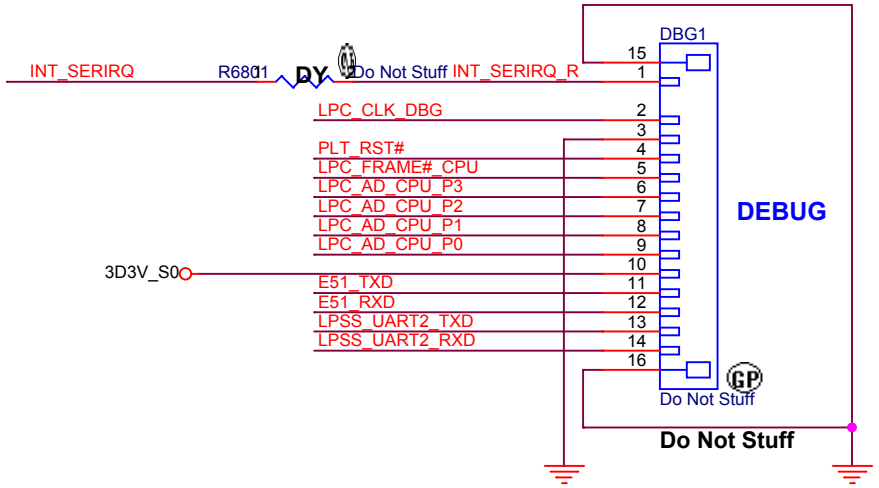
18,24,26,54,61,89 PLT_RST#
19,24 LPC_FRAME#_CPU

19,24 LPC_AD_CPU_P3
19,24 LPC_AD_CPU_P2

19,24 LPC_AD_CPU_P1
19,24 LPC_AD_CPU_P0

24,61 E51_TXD
24 E51_RXD

21 LPSS_UART2_TXD
21 LPSS_UART2_RXD



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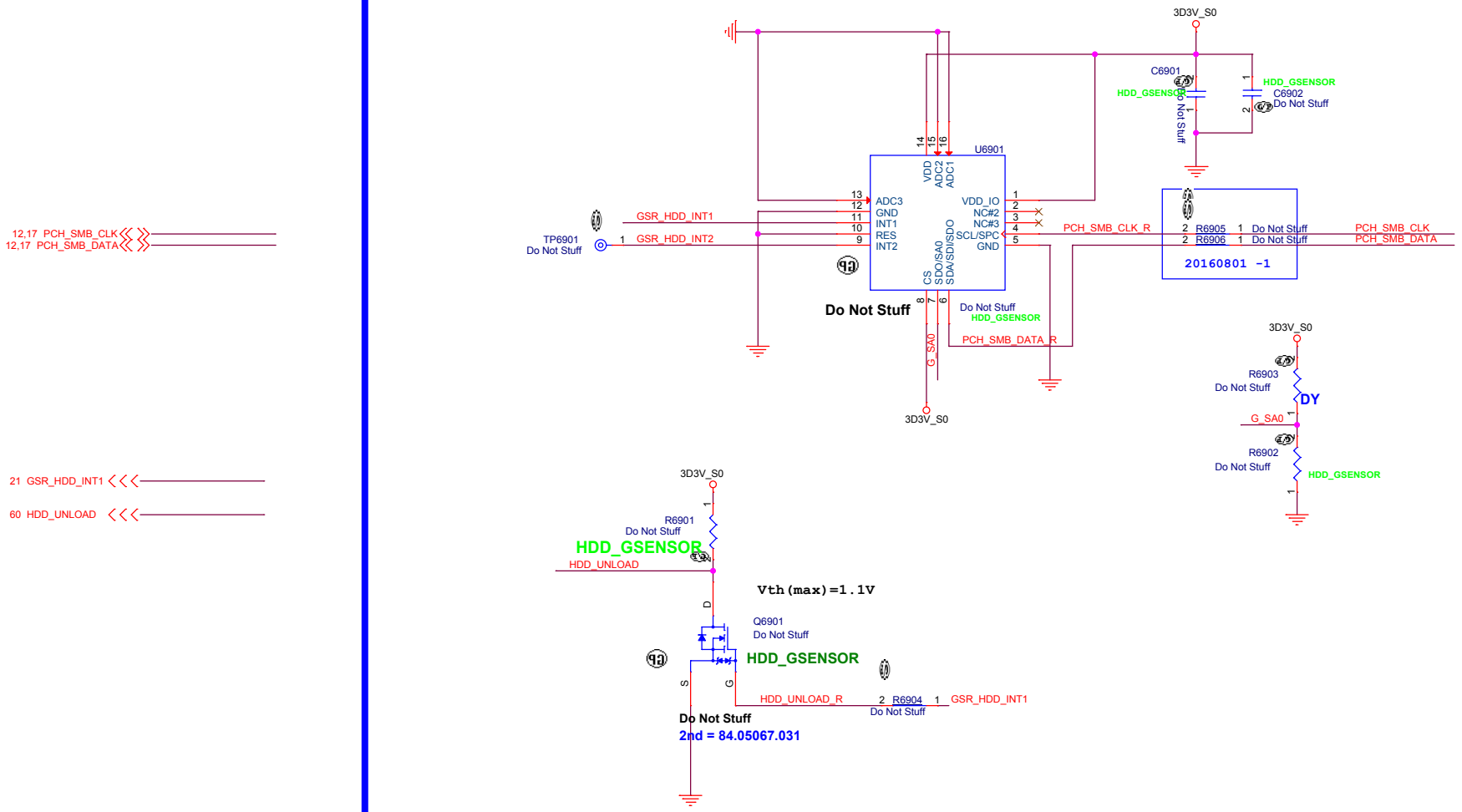
Title: ***Dubug connector***

Size	Document Number	Rev
A4	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 68 of 106



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Title: *HDD_G_Sensor*		
Size: A3	Document Number: Ironhide_APL	Rev: -1M
Date: Wednesday, September 21, 2016	Sheet 69 of 106	

SSID = User.Interface

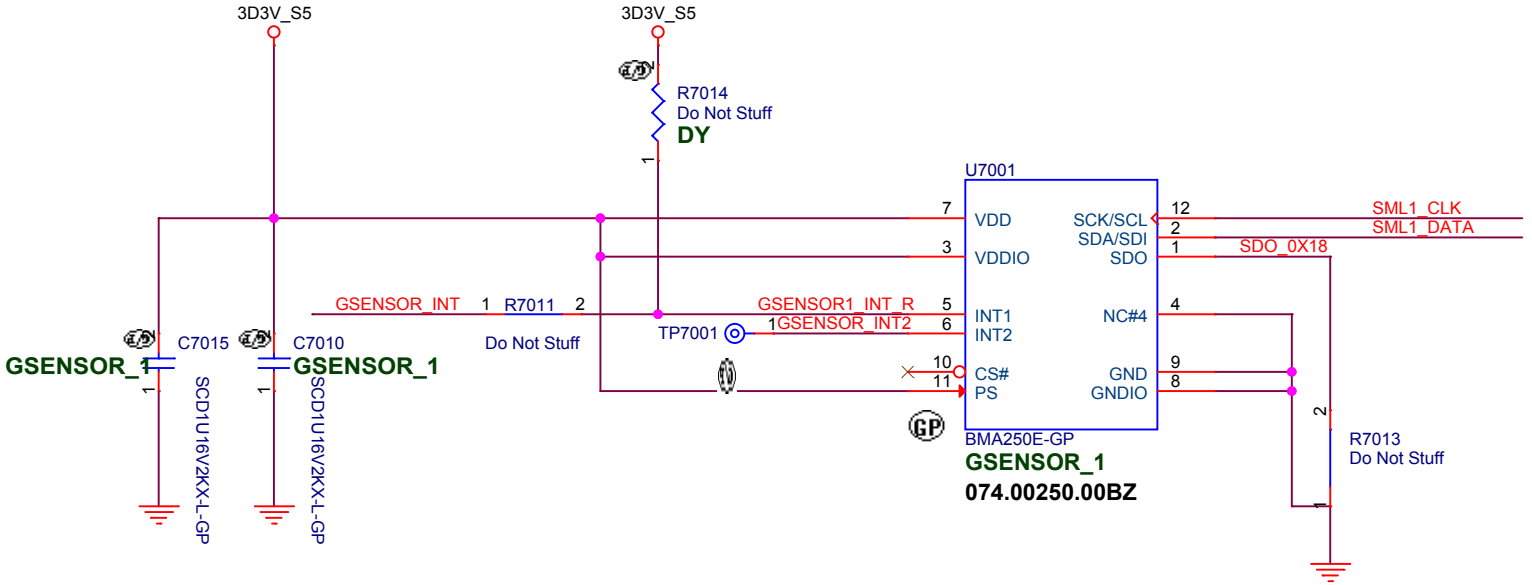
G Sensor

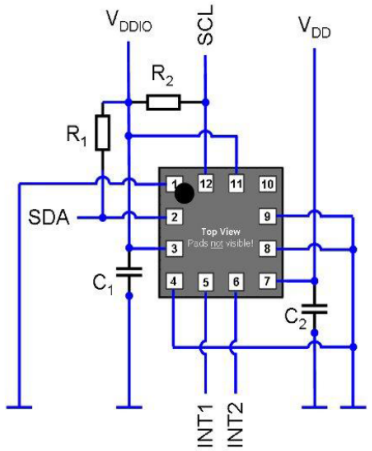
Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

The default I²C address of the device is 0011000b (0x18). It is used if the SDO pin is pulled to ´GND´. The alternative address 0011001b (0x19) is selected by pulling the SDO pin to ´V_{DDIO}´.

24,55 GSENSOR_INT

18,24,55 SML1_CLK
18,24,55 SML1_DATA





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Title: G SENSOR

Size: A4 | Document Number: Ironhide_APL | Rev: -1M

Date: Wednesday, September 21, 2016 | Sheet 70 of 106

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Title

H_Sensor

Size	Document Number	Rev
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Title: *Thunderbolt (5/5)*

Size	Document Number	Rev
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Title: GPU(PEG)

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A2	Ironhide_APL	-1M

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Title: *GPU (DIGITALOUT)*

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Title

GPU (VRAM I/F)

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Custom	Ironhide_APL	-1M

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Title: *GPU (GPIO/STRAP)*

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Title
GPU (POWER/GND)

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A4	Ironhide_APL	-1M
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Title
GPU-VRAM1,2 (1/4)

Size	Document Number	Rev
A4	Ironhide_APL	-1M
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
A4	Ironhide_APL	-1M
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM5,6 (3/4)*

Size	Document Number	Rev
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Date: Wednesday, September 21, 2016	Sheet 80 of 106	

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Taipei Hsien 221, Taiwan, R.O.C.

Title
GPU-VRAM7,8 (4/4)

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Date: Wednesday, September 21, 2016	Sheet 81 of 106	

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Title
RT8812A_VGA_CORE

Size	Document Number	Rev
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
Custom	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 83 of 106

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
A2	Ironhide_APL	-1M

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Title

Switchable GFX LCD(2/2)

Size	Document Number	Rev
A4	**Ironhide_APL**	**-1M**
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Title: ***Audio Jack***

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H1 Do Not Stuff — Do Not Stuff

H2 Do Not Stuff — Do Not Stuff

Screw PAD

H3 Do Not Stuff — Do Not Stuff

H4 Do Not Stuff — Do Not Stuff

H5 Do Not Stuff — Do Not Stuff

H6 Do Not Stuff — Do Not Stuff

SP9 SUL-1315A1M-GP

SP10 SUL-1315A1M-GP

SP11 SUL-1315A1M-GP

20160817 -1

HS1 STF237R128H34-4-GP — 34.4YP25.001 / 2nd = 34.4YP25.301

HS2 STF237R128H34-4-GP — 34.4YP25.001 / 2nd = 34.4YP25.301

HS3 STFT236B142R128H43-2-GP — 34.4EO02.101

To use 34.4EO02.101 footprint, but BOM use :
main source is 34.4EO02.201
second source is 34.4EO02.301

SP1 SPRING-112-GP

SP2 SPRING-112-GP

SP3 SPRING-112-GP

SP4 SPRING-112-GP

SP5 SPRING-112-GP

SP6 SPRING-112-GP

SP7 SPRING-112-GP

SP8 SPRING-112-GP

Check test point

3D3V_S0 — AFTP1

3D3V_AUX_S5 — TP7

3D3V_S5 — TP8

5V_S5 — AFTP9

Top side

DCIN

19V_AD_JK — TP2

19V_AD_JK — AFTP3

AFTP4

AFTP5

Touch PAD

65 EC_TP_CLK_C — TP56

65 EC_TP_DATA_C — TP57

65 TP_I2C4_SDA_CON — AFTP58

65 TP_I2C4_SCL_CON — TP59

65 TP_IN#_R — AFTP90

3D3V_TP_S3 — TP91

24,65 FUN_OFF# — AFTP85

Speaker

29 AUD_SPK1_L-_CON — AFTP16

29 AUD_SPK1_L+_CON — TP18

29 AUD_SPK1_R-_CON — TP19

29 AUD_SPK1_R+_CON — AFTP20

KB

KSO0 — TP24 — KSI0 — AFTP48

KSO1 — AFTP26 — KSI1 — TP50

KSO2 — AFTP25 — KSI2 — TP49

KSO3 — TP27 — KSI3 — TP51

KSO4 — TP28 — KSI4 — AFTP53

KSO5 — AFTP30 — KSI5 — TP52

KSO6 — TP29 — KSI6 — TP54

KSO7 — TP32 — KSI7 — AFTP55

KSO8 — TP33

KSO9 — TP40

KSO10 — TP39

KSO11 — AFTP41

KSO12 — AFTP42

KSO13 — TP44

KSO14 — TP43

KSO15 — AFTP45

KSI[0..7] 24,65

KSO[0..15] 24,65

Battery

BT+ — AFTP6

BT+ — AFTP11

AFTP13

AFTP14

43 BAT_G — AFTP21

43 BAT_IN#_1 — TP22

43 BATA_SCL_1 — TP23

43 BATA_SDA_1 — AFTP36

Daughter BD

24,64 LID_CLOSE2# — TP100

64 CARD1_CON_USB20_P — AFTP71

64 CARD1_CON_USB20_N — TP72

18,24,64 KBC_PWRBTN# — TP31

24,64 LID_CLOSE# — TP99

64 STDBY_LED#_R — AFTP35

64 FRONT_PWRLED#_R — TP46

64 CHARGE_LED#_R — AFTP47

64 DC_BATFULL#_R — TP67

64 Value+_R — TP68

64 Value-_R — AFTP75

5V_AUX_S5 — TP34

3D3V_S0 — TP96

5V_S5 — TP97

AFTP98

WLAN

16,18,24,61 PCIE_WAKE# — TP76

17,61 BT_USB20_P — AFTP77

17,61 BT_USB20_N — TP78

24,61 WIFI_RF_EN — TP79

61 WLAN_RST# — AFTP80

16,61 WLAN_CLKREQ_CPU# — TPA4

16,61 WLAN_CLK_CPU# — TPA5

16,61 WLAN_CLK_CPU — TPA6

16,61 WLAN_PCIE_TX_P — TPA7

16,61 WLAN_PCIE_TX_N — TPA8

16,61 WLAN_PCIE_RX_P — TPA9

16,61 WLAN_PCIE_RX_N — TPB1

24,61 BLUETOOTH_EN — TPB3

61 PCIE_WAKE#R — TPB4

61 WIFI_RF_EN_CON — TPB5

3D3V_IOAC — TP82 / AFTP84

USB2.0

34 USB2_CON_USB20_N — AFTP106

34 USB2_CON_USB20_P — AFTP107

5V_USB20 — AFTP117

5V_USB20 — TP133

34 USB3_CON_USB20_N — AFTP108

34 USB3_CON_USB20_P — AFTP109

EDP

55 eDP_TX_CON_P0 — AFTP37

55 eDP_TX_CON_N0 — AFTP38

55 eDP_TX_CON_P1 — TP73

55 eDP_TX_CON_N1 — TP74

55 eDP_AUX_CON_P — TP86

55 eDP_AUX_CON_N — TP87

55 eDP_BLCTRL_CON — AFTP89

55 eDP_HPD_CON — TP83

55 eDP_BLEN_CON — AFTP92

55 TOUCH_INTR# — TP94

55 TS_USB20_CON_N — TP112

55 TS_USB20_CON_P — TP113

55 TOUCH_DET#_R — AFTP114

55 TOUCH_S_RST#_R — TP115

55 TS_S0 — TP116

3D3V_CAMERA_S0 — TP93

3D3V_LCDVDD_S0 — AFTP81

19V_DCBATOUT_LCD — TP15

AFTP17

FAN

24,26 FAN1_PWM — TP60

24,26 FAN_TACH1 — AFTP61

5V_S0 — TPA1

26 FAN_TACH1_C — AFTPA2

LOUT

27,29 SELEEVE — AFTP62

29 AUD_HP1_JACK_R1 — TP63

29 AUD_HP1_JD#_TYPE — AFTP64

29 AUD_HP1_JACK_L1 — TP65

27,29 RING2 — TP66

29 AUD_HP1_JD#_R — AFTPB2

USB3.0

5V_USB30 — TP118

35 USB1_CON_USB20_N — TP119

35 USB1_CON_USB20_P — AFTP120

CCD

3D3V_S0 — TP88

55 CCD_USB20_CON_P — TP69

55 CCD_USB20_CON_N — AFTP70

55 DMIC_CLK_CON_C — TP95

55 DMIC_DATA_CON_C — TP110

18,24,26,54,61,68 PLT_RST# — AFTP111

HDMI

57 HDMI_CLK_CON_N3 — TP121

57 HDMI_CLK_CON_P3 — TP122

57 HDMI_DATA_CON_P0 — TP124

57 HDMI_DATA_CON_N0 — AFTP123

57 HDMI_DATA_CON_P1 — TP126

57 HDMI_DATA_CON_N1 — TP125

57 HDMI_DATA_CON_P2 — TP128

57 HDMI_DATA_CON_N2 — AFTP127

57 HDMI_CLK_CON — TP130

57 HDMI_DATA_CON — TP129

57 HDMI_DET_CON — TP132

5V_HDMI_S0 — AFTP131

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Title: UNUSED PARTS/EMI Capacitors

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let the cap close to PR4417

BT+ — EC9001 1 — Do Not Stuff

let the cap close to PU4504

PWR_DCBATOUT_5V — EC9003 1 — Do Not Stuff; EC9004 1 — Do Not Stuff

let the cap close to PU4502

PWR_DCBATOUT_3D3V — EC9007 1 — Do Not Stuff; EC9008 1 — Do Not Stuff

let the cap close to PU4403

19V_DCBATOUT — EC9023 1 — Do Not Stuff; EC9024 1 — Do Not Stuff

let the cap close to PU5101

PWR_DCBATOUT_VDDQ — EC9019 1 — Do Not Stuff; EC9020 1 — Do Not Stuff

let the cap close to PU4601.

19V_DCBATOUT — EC9011 1 — Do Not Stuff; EC9012 1 — Do Not Stuff

let the cap close to PU4702.

19V_DCBATOUT — EC9015 1 — Do Not Stuff; EC9016 1 — Do Not Stuff

let the cap close to PU5003

PWR_DCBATOUT_VNN — EC9071 1 — Do Not Stuff; EC9072 1 — Do Not Stuff

let the cap close to EDP1

19V_DCBATOUT_LCD — EC9053 1 — Do Not Stuff; EC9054 1 — Do Not Stuff

let the cap close to U2401

19,24,90 LPC_CLK_KBC — EC9041 1 — Do Not Stuff

let the cap close to U2701

21,27 HDA_BITCLK_CODEC — EC9042 1 — Do Not Stuff

let the cap close to CPU.

21,27 HDA_SDOUT_CODEC — EC9059 1 — Do Not Stuff

let the cap close to CPU.

19 HDA_RST#_CPU — EC9060 1 — Do Not Stuff

19V_DCBATOUT — EC9073 1 — SCD1U25V2KX-L-GP; EC9074 1 — SCD1U25V2KX-L-GP; EC9075 1 — SCD1U25V2KX-L-GP; EC9076 1 — SCD1U25V2KX-L-GP; EC9077 1 — SCD1U25V2KX-L-GP; EC9078 1 — SCD1U25V2KX-L-GP; EC9079 1 — SCD1U25V2KX-L-GP

19V_DCBATOUT — EC9080 1 — Do Not Stuff — DY

For Acoustic Noise

let the cap close to PU4403

19V_DCBATOUT — FC9001 1 — Do Not Stuff; FC9002 1 — Do Not Stuff

let the cap close to PR4417

BT+ — FC9003 1 — Do Not Stuff; FC9004 1 — Do Not Stuff

let the cap close to PU4504

PWR_DCBATOUT_5V — FC9005 1 — Do Not Stuff; FC9006 1 — Do Not Stuff

let the cap close to PL4502

PWR_5V — FC9007 1 — Do Not Stuff; FC9008 1 — Do Not Stuff

let the cap close to PU4502

PWR_DCBATOUT_3D3V — FC909 1 — Do Not Stuff; FC9010 1 — Do Not Stuff

let the cap close to PL4501

PWR_3D3V — FC9011 1 — Do Not Stuff; FC9012 1 — Do Not Stuff

let the cap close to PU4601

19V_DCBATOUT — FC9013 1 — Do Not Stuff; FC9014 1 — Do Not Stuff

let the cap close to PL4603

1D8V_S5 — FC9015 1 — Do Not Stuff; FC9016 1 — Do Not Stuff

let the cap close to PL4601

1D24V_S5 — FC9017 1 — Do Not Stuff; FC9018 1 — Do Not Stuff

let the cap close to PL4602

1D05V_S0 — FC9019 1 — Do Not Stuff; FC9020 1 — Do Not Stuff

let the cap close to PU4601

0D675V_VREF_S0 — FC9021 1 — Do Not Stuff; FC9022 1 — Do Not Stuff

let the cap close to PU4601

PWR_VDDQ — FC9023 1 — Do Not Stuff; FC9024 1 — Do Not Stuff

let the cap close to U4001

5V_S5 — FC9025 1 — Do Not Stuff; FC9026 1 — Do Not Stuff

let the cap close to U4001

3D3V_S5 — FC9027 1 — Do Not Stuff; FC9028 1 — Do Not Stuff

let the cap close to U4001

5V_SYS_OUT — FC9029 1 — Do Not Stuff; FC9030 1 — Do Not Stuff

let the cap close to U4001

3V_SYS_OUT — FC9031 1 — Do Not Stuff; FC9032 1 — Do Not Stuff

let the cap close to U4002

1D8V_S5 — FC9034 1 — Do Not Stuff; FC9033 1 — Do Not Stuff

let the cap close to U4002

1D8V_S0 — FC9035 1 — Do Not Stuff; FC9036 1 — Do Not Stuff

let the cap close to U5302

3D3V_S5 — FC9037 1 — Do Not Stuff; FC9038 1 — Do Not Stuff

let the cap close to U5302

1D5V_S0 — FC9039 1 — Do Not Stuff; FC9040 1 — Do Not Stuff

let the cap close to PU4701

5V_S5 — FC9041 1 — Do Not Stuff; FC9042 1 — Do Not Stuff

let the cap close to PU4702

19V_DCBATOUT — FC9043 1 — Do Not Stuff; FC9044 1 — Do Not Stuff

let the cap close to PL4701

1V_CPU_VCGI — FC9045 1 — Do Not Stuff; FC9046 1 — Do Not Stuff

let the cap close to CPU1

1D35V_S3 — FC9047 1 — Do Not Stuff; FC9048 1 — 2 SCD1U16V2KX-L-GP; FC9095 1 — 2 Do Not Stuff; FC9096 1 — 2 SC2D2U16V2KX-GP

let the cap close to CPU1

1D05V_S0 — FC9049 1 — 2 SCD1U16V2KX-L-GP; FC9050 1 — 2 SC2D2U16V2KX-GP; FC9097 1 — Do Not Stuff; FC9098 1 — 2 SCD1U16V2KX-L-GP

let the cap close to CPU1

1D8V_S5 — FC9051 1 — 2 SCD1U16V2KX-L-GP; FC9052 1 — 2 SC2D2U16V2KX-GP; FC9099 1 — Do Not Stuff; FC9100 1 — Do Not Stuff

let the cap close to CPU1

1V_CPU_VCGI — FC9053 1 — 2 SCD1U16V2KX-L-GP; FC9054 1 — 2 SC2D2U16V2KX-GP; FC9102 1 — Do Not Stuff; FC9101 1 — Do Not Stuff

let the cap close to PU5002

5V_S5 — FC9056 1 — Do Not Stuff; FC9055 1 — Do Not Stuff

let the cap close to PU5003

PWR_DCBATOUT_VNN — FC9058 1 — Do Not Stuff; FC9057 1 — Do Not Stuff

let the cap close to PL5001

1V_CPU_VNN — FC9060 1 — Do Not Stuff; FC9059 1 — Do Not Stuff

let the cap close to PU5103

5V_S5 — FC9062 1 — Do Not Stuff; FC9061 1 — Do Not Stuff

let the cap close to PU5101

PWR_DCBATOUT_VDDQ — FC9064 1 — Do Not Stuff; FC9063 1 — Do Not Stuff

let the cap close to PL5101

PWR_VDDQ — FC9066 1 — Do Not Stuff; FC9065 1 — Do Not Stuff

let the cap close to RN1207

1D35V_S3 — FC9068 1 — 2 Do Not Stuff — DY; FC9067 1 — 2 SC2D2U16V2KX-GP

let the cap close to DM1

3D3V_S0 — FC9070 1 — 2 SC2D2U16V2KX-GP; FC9069 1 — 2 SCD1U16V2KX-L-GP

let the cap close to DM1

1D35V_S3 — FC9071 1 — 2 SC2D2U16V2KX-GP; FC9072 1 — 2 SCD1U16V2KX-L-GP; FC9104 1 — 2 SCD1U16V2KX-L-GP; FC9103 1 — 2 SCD1U16V2KX-L-GP; FC9105 1 — 2 Do Not Stuff — DY; FC9106 1 — 2 Do Not Stuff — DY

let the cap close to WLAN1

3D3V_IOAC — FC9073 1 — Do Not Stuff

let the cap close to EDP1

3D3V_S0 — FC9075 1 — Do Not Stuff

let the cap close to EDP1

3D3V_S5 — FC9077 1 — Do Not Stuff

let the cap close to EDP1

3D3V_LCDVDD_S0 — FC9079 1 — Do Not Stuff

let the cap close to EDP1

19V_DCBATOUT_LCD — FC9081 1 — Do Not Stuff

let the cap close to HDMI1

5V_HDMI_S0 — FC9083 1 — Do Not Stuff

let the cap close to HDD1

5V_S0 — FC9085 1 — EC4D7U10V3KX-GP; HDD 20160803 -1

let the cap close to SSDBD

3D3V_S0 — FC9087 1 — Do Not Stuff; FC9088 1 — Do Not Stuff

let the cap close to U7001

3D3V_S5 — FC9089 1 — Do Not Stuff

let the cap close to R1905

19,24,90 LPC_CLK_KBC — FC9091 1 — Do Not Stuff

let the cap close to R1904

19,68 LPC_CLK_DBG — FC9092 1 — Do Not Stuff

let the cap close to CPU1

19,24,25 SPI_CLK_ROM — FC9093 1 — Do Not Stuff

let the cap close to CPU1

21,27 HDA_SDIN0_CPU — FC9094 1 — Do Not Stuff

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SSID = Docking

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SSID = Intel LAN

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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0[1]	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST#[1]	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4[1]	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST#[1]	0	System	18	HOOK7	DBR#[1]	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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Title

PCH_XDP

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Title

Audio Jack

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Title

Audio Jack

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Main Func = Debug

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Title: CPU_XDP

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Title: *table of content*

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Title

Change History

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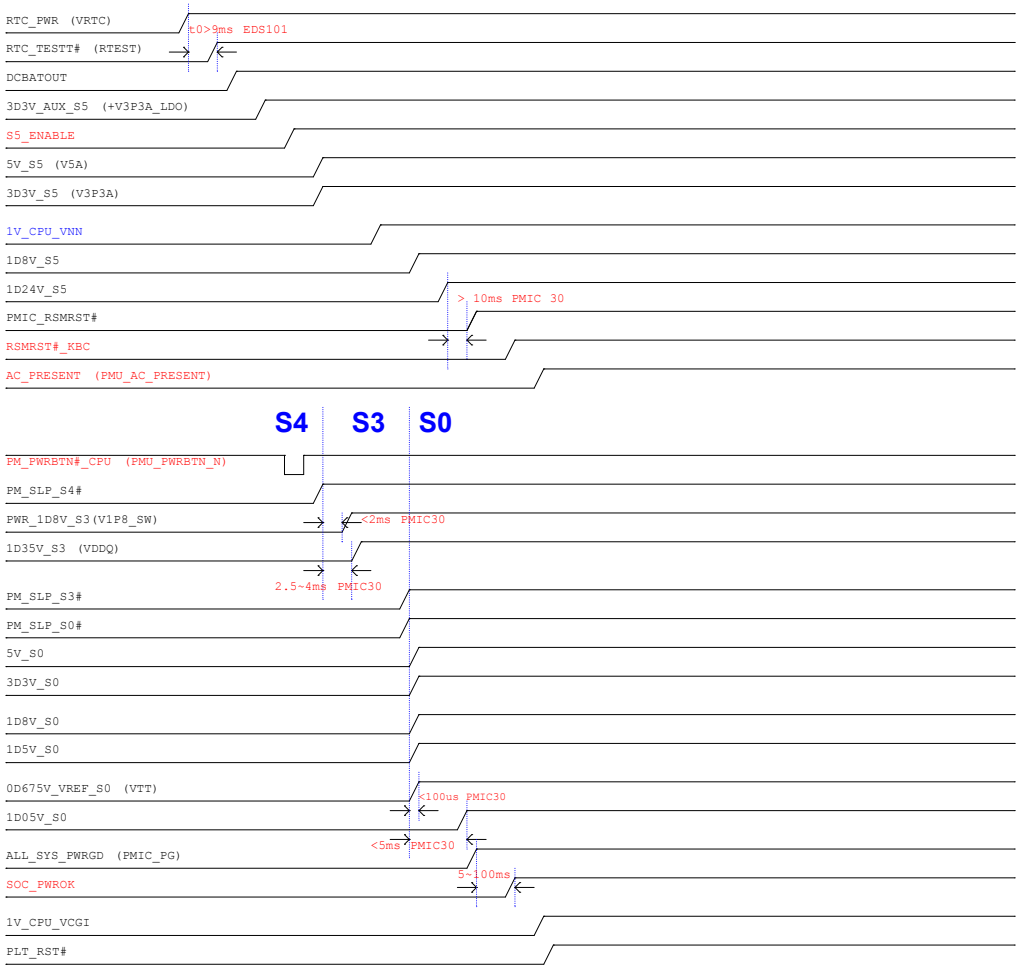
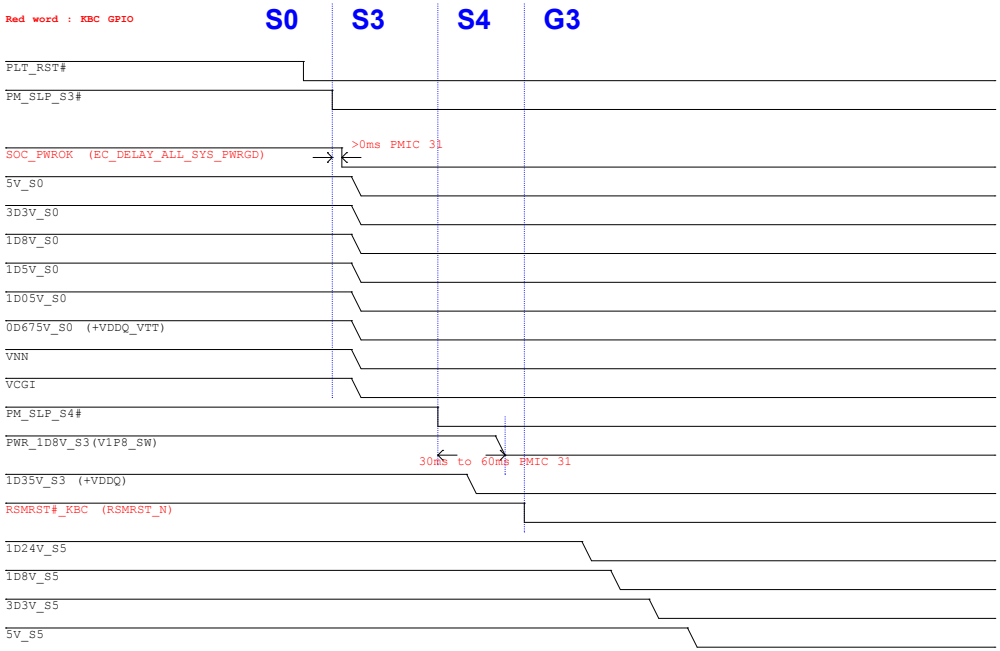
Intel-Power Up Sequence

G3 to S5/S4

Red word : KBC GPIO



Intel-Power Down Sequence



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Title: *Power Sequence*		
Size: A2	Document Number: Ironhide_APL	Rev: -1M
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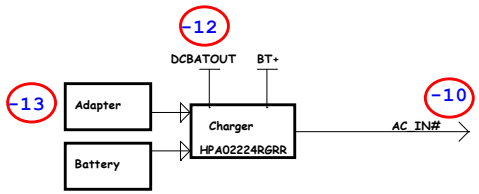
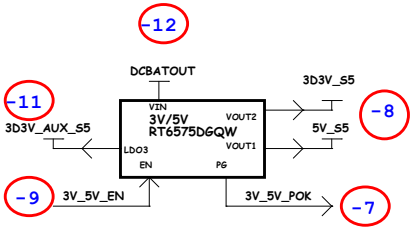
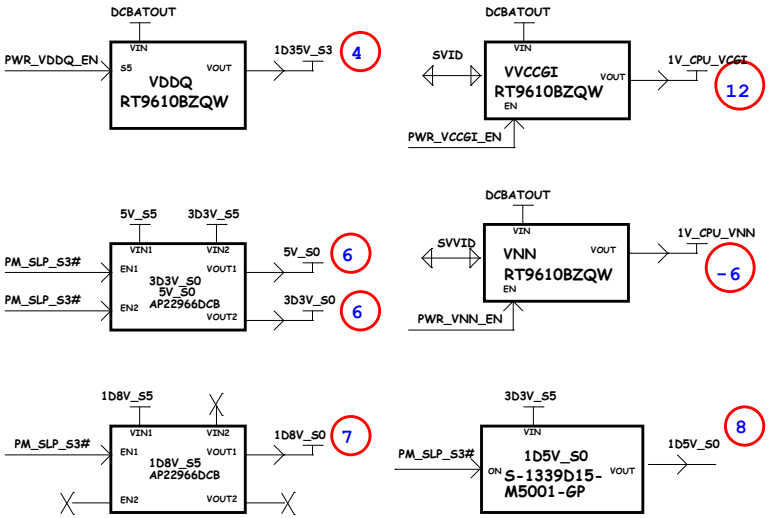
APOLLO LAKE SEQUENCE & BLOCK DIAGRAM

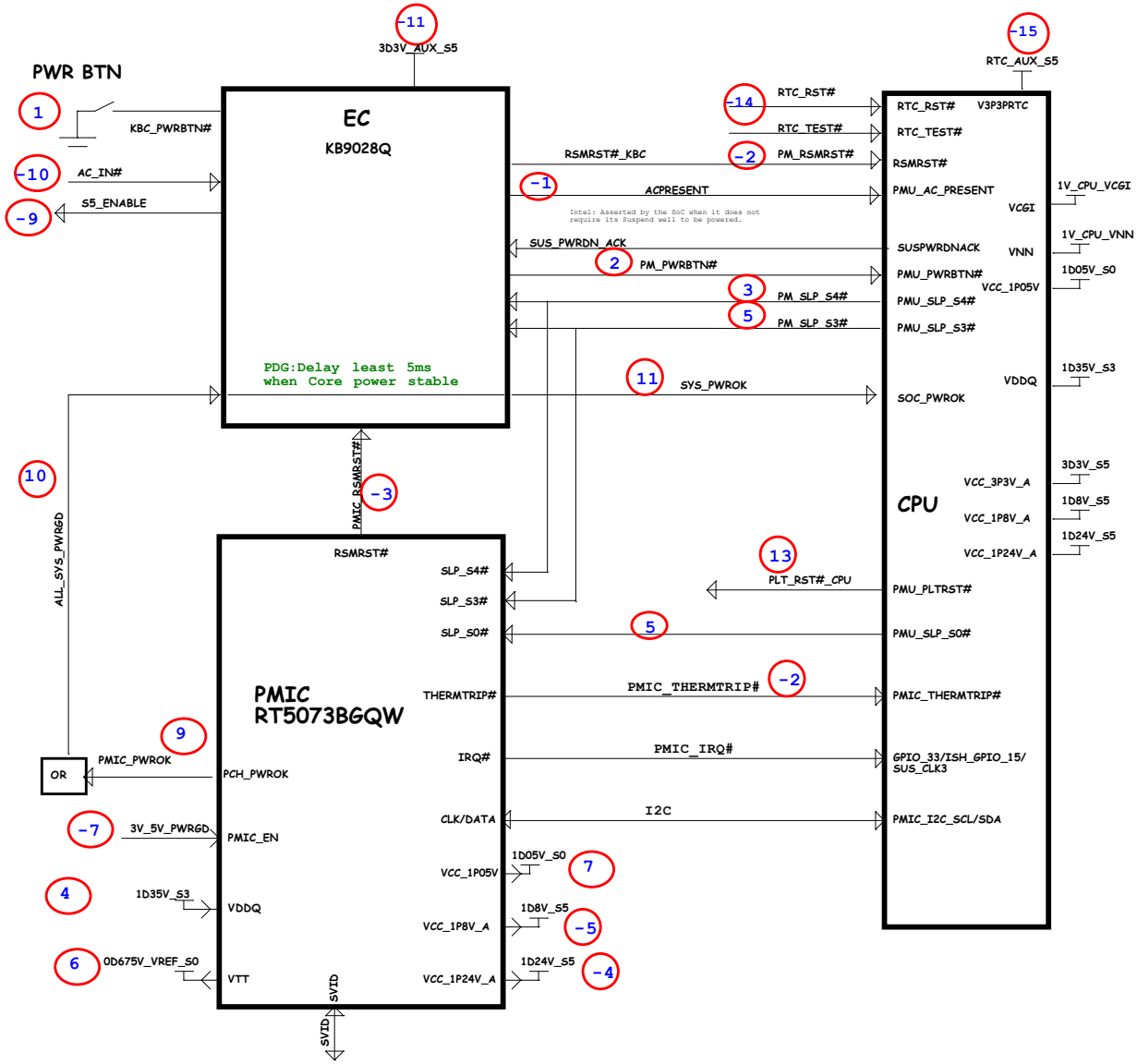


S5 PWR



S3-S0 PWR





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Title: Power Block Diagram

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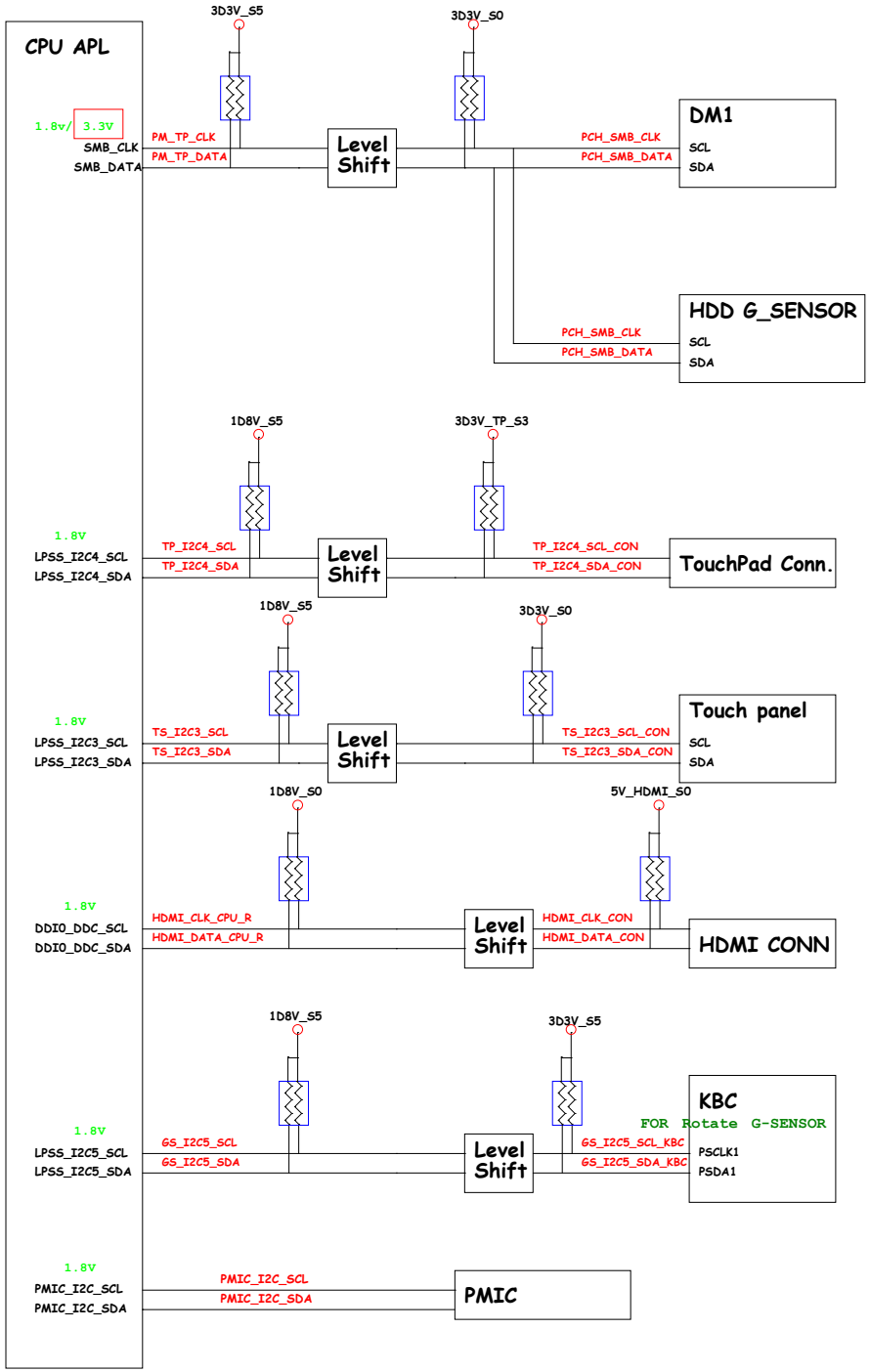
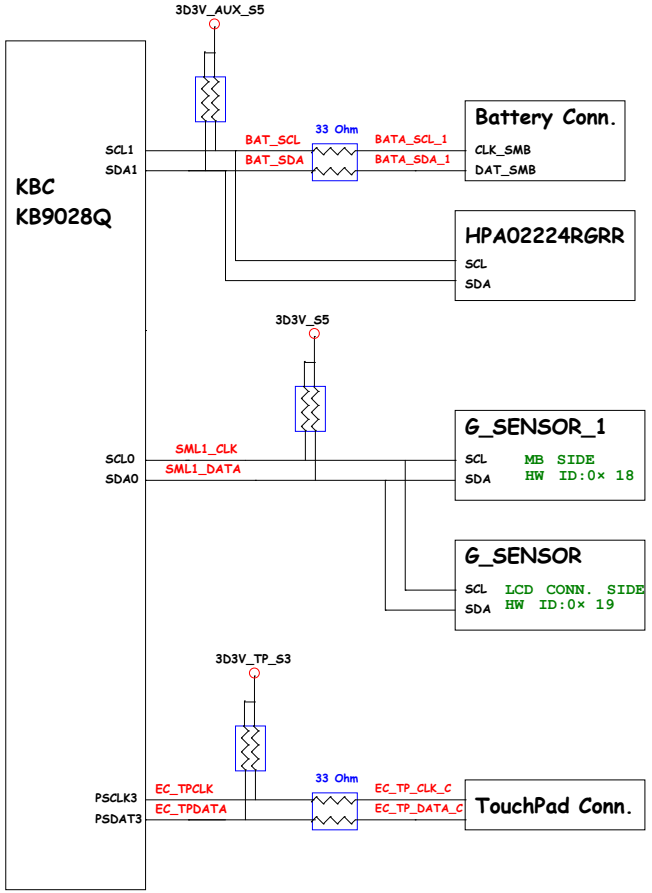
PCH SMBus/I2C Block Diagram



KBC SMBus/I2C Block Diagram



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Title: SMBUS/I2C BLOCK DIAGRAM

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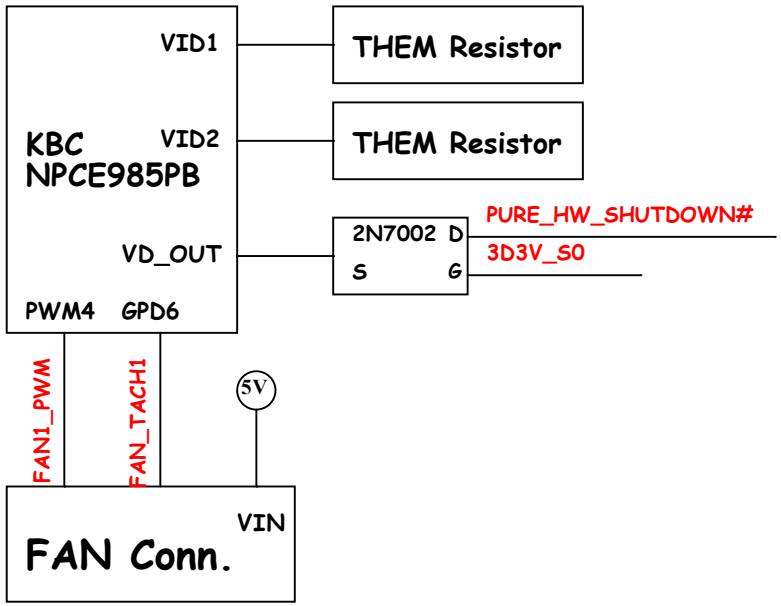
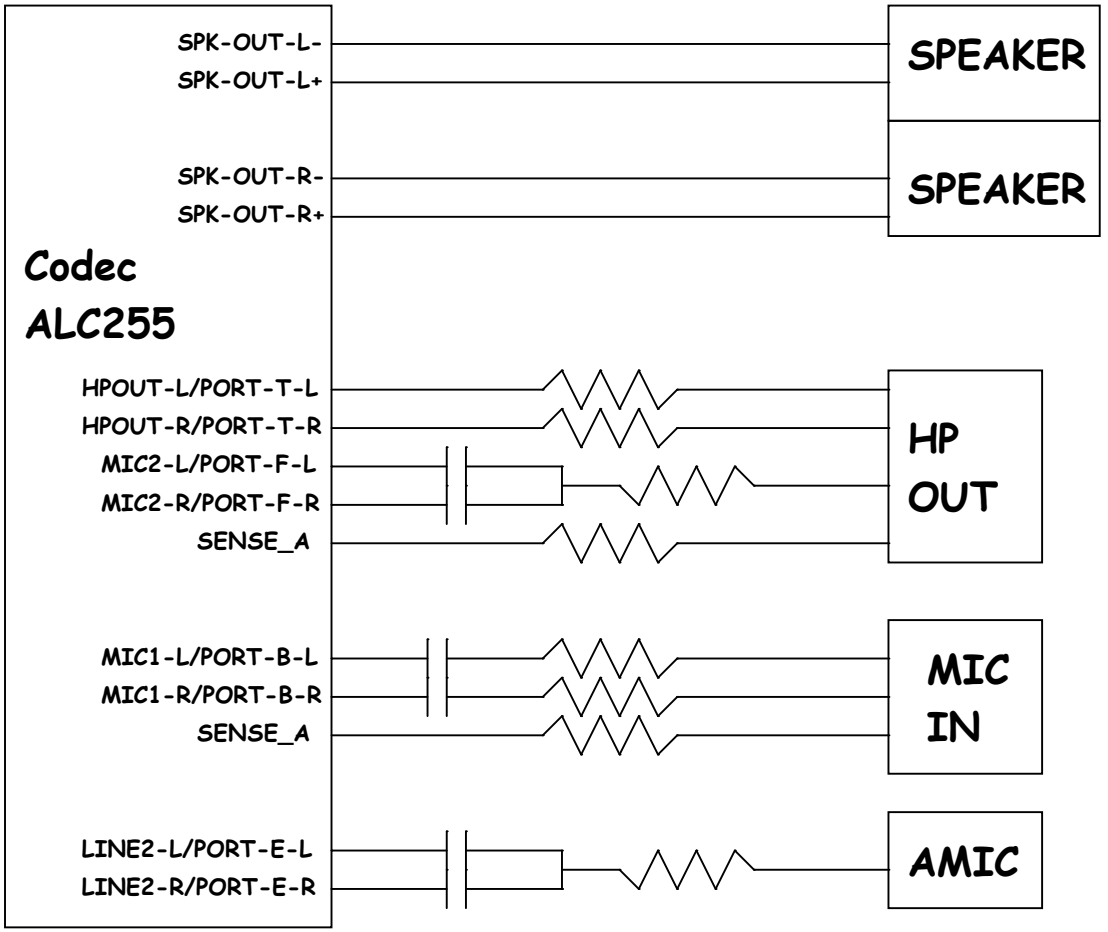
Thermal Block Diagram



Audio Block Diagram



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Blanking

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Title: ***LAN Switch***

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