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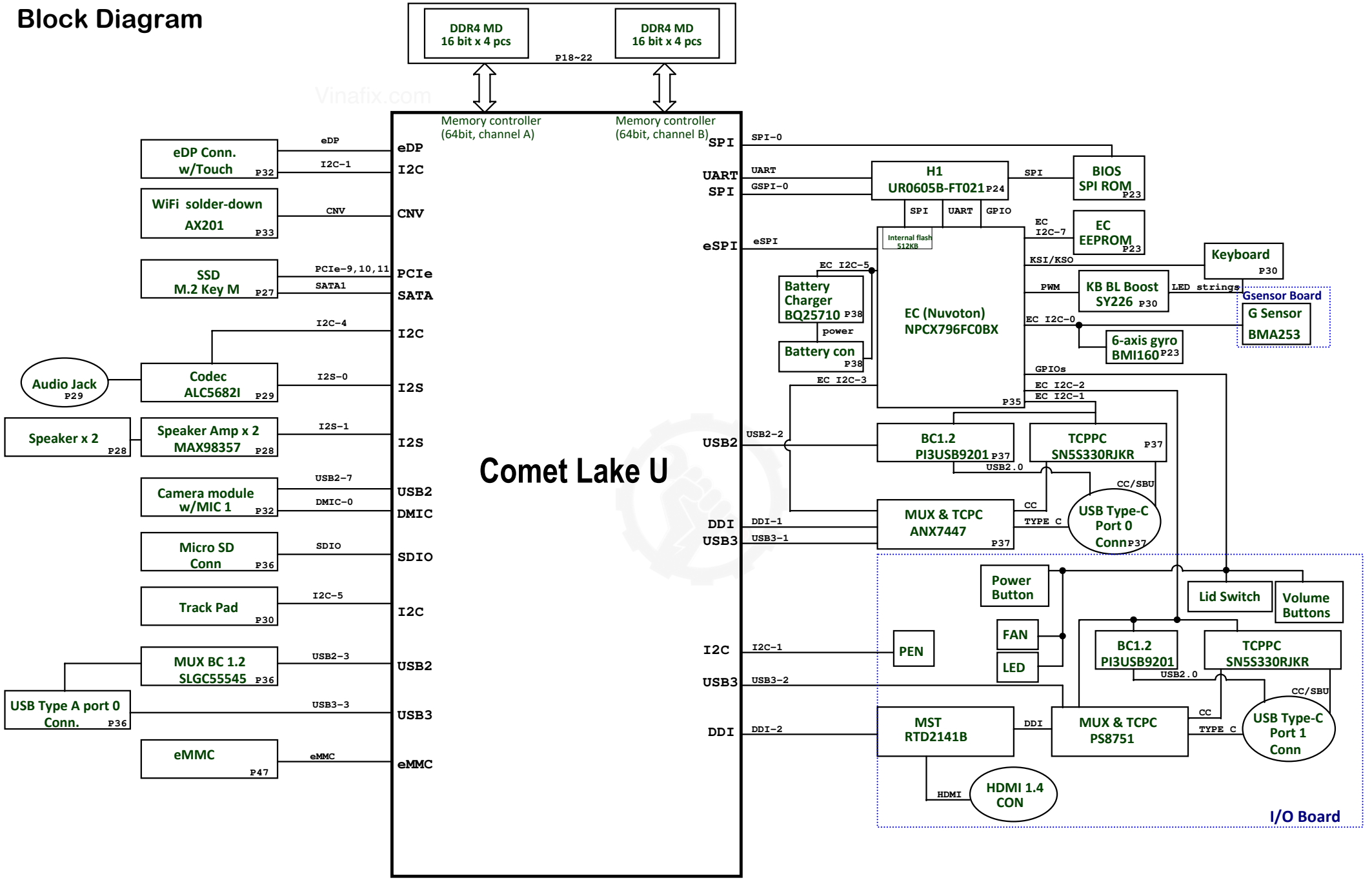

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SYSTEM BLOCK DIAGRAM
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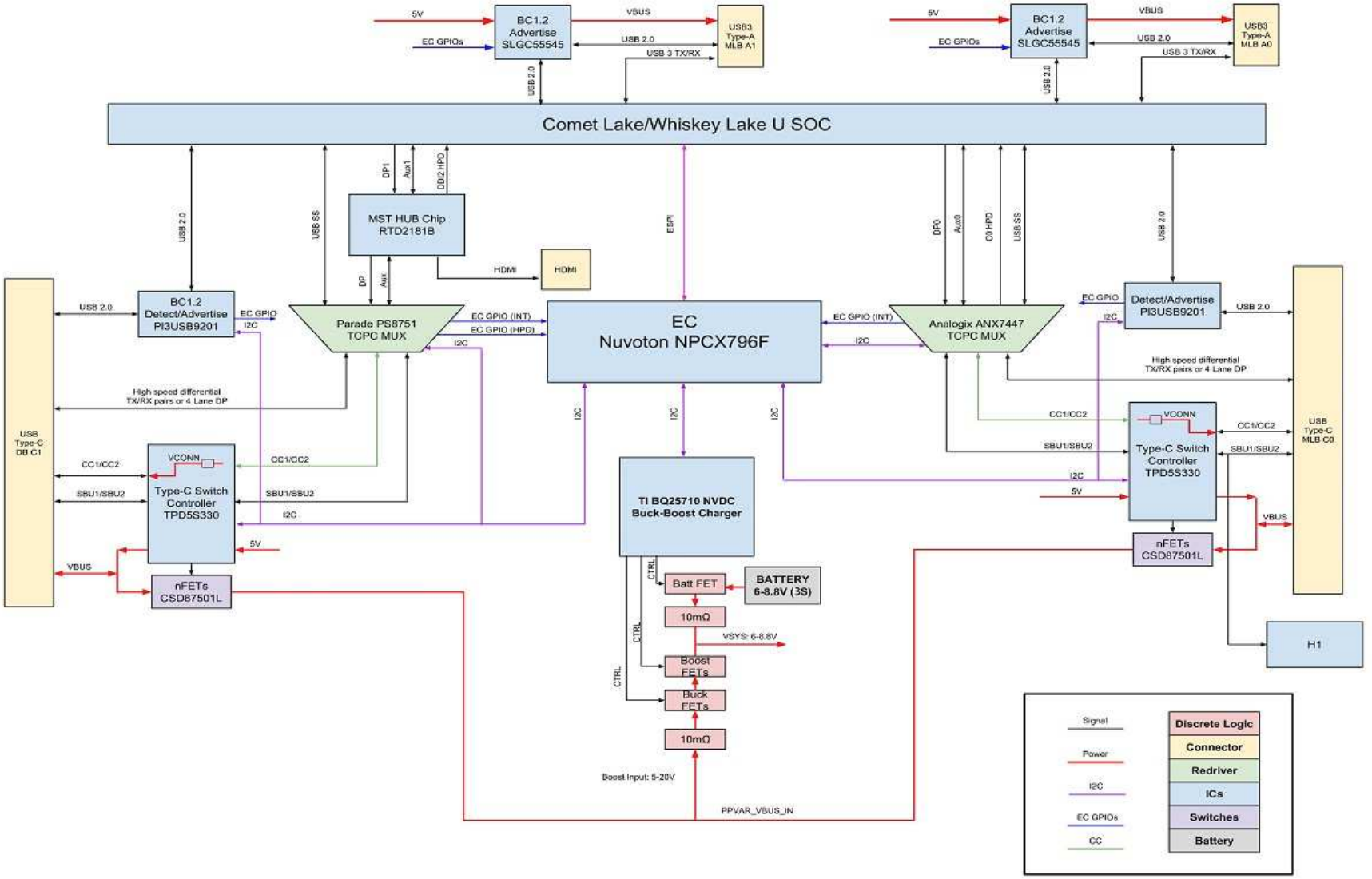
Hatch USB Block Diagram

Updated: 11/19/2018



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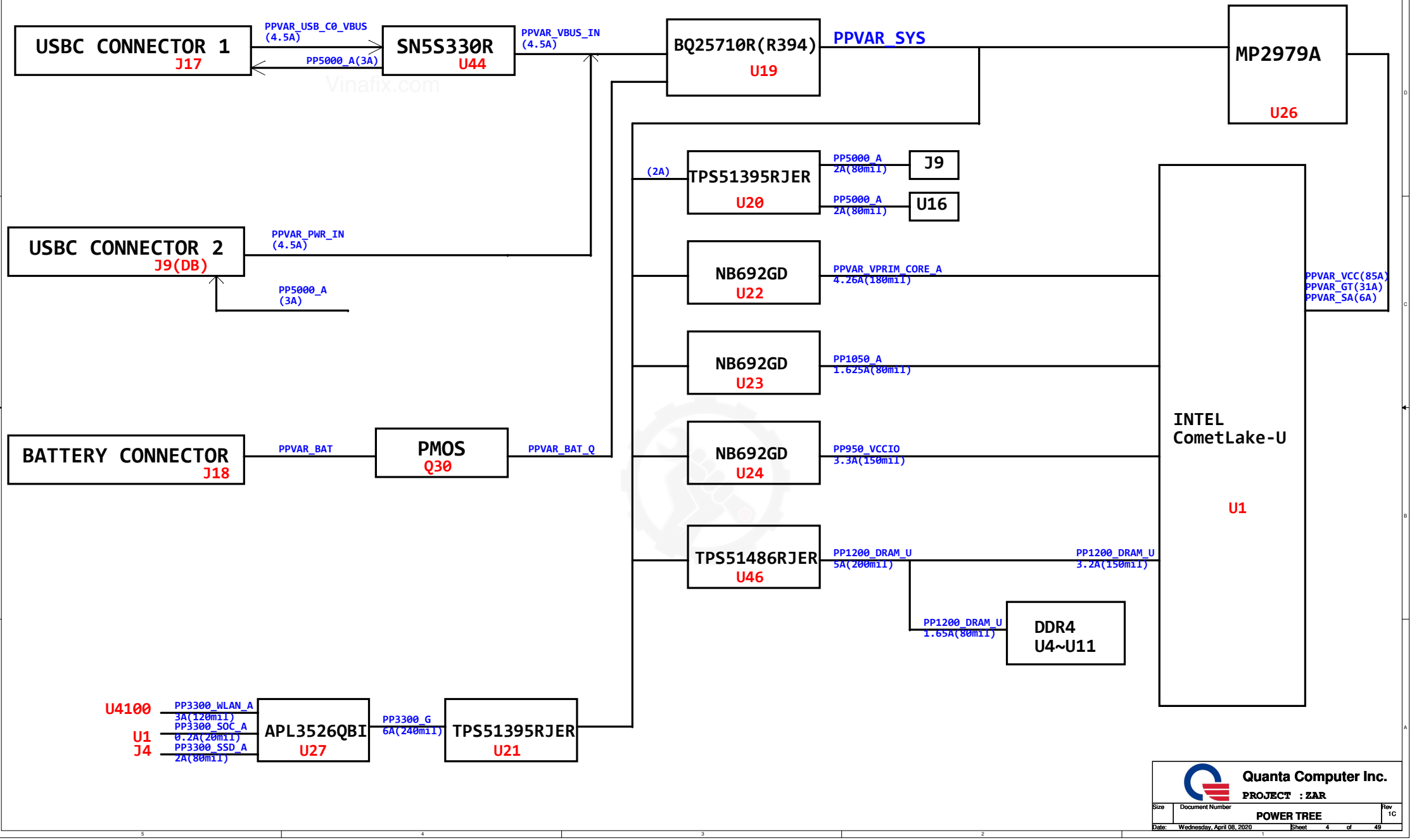

Quanta Computer Inc.

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Size	Document Number	Rev
	POWER TREE	1C

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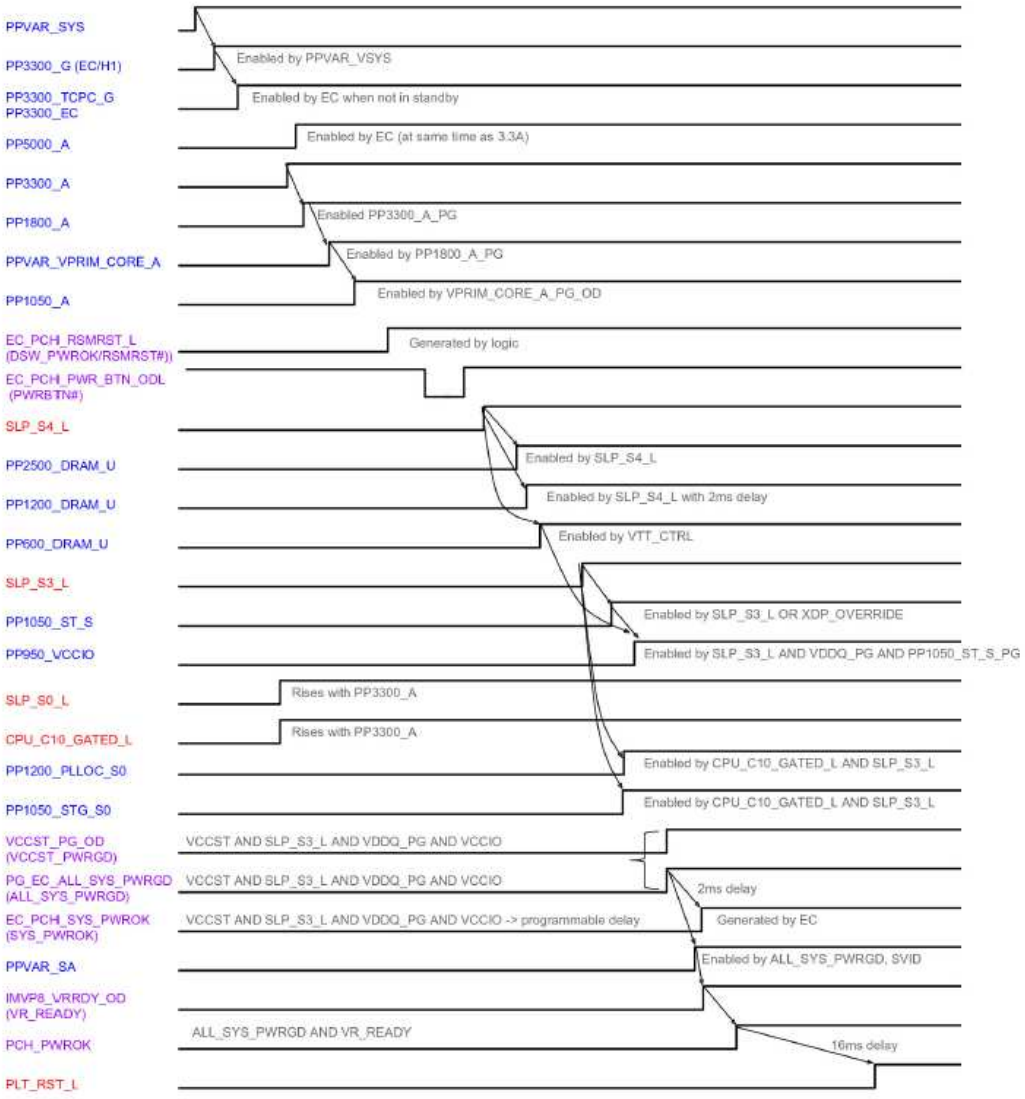

Power Rail
Signal from PCH
Signal from Platform

Hatch Power Sequencing

Updated: 11/29/2018

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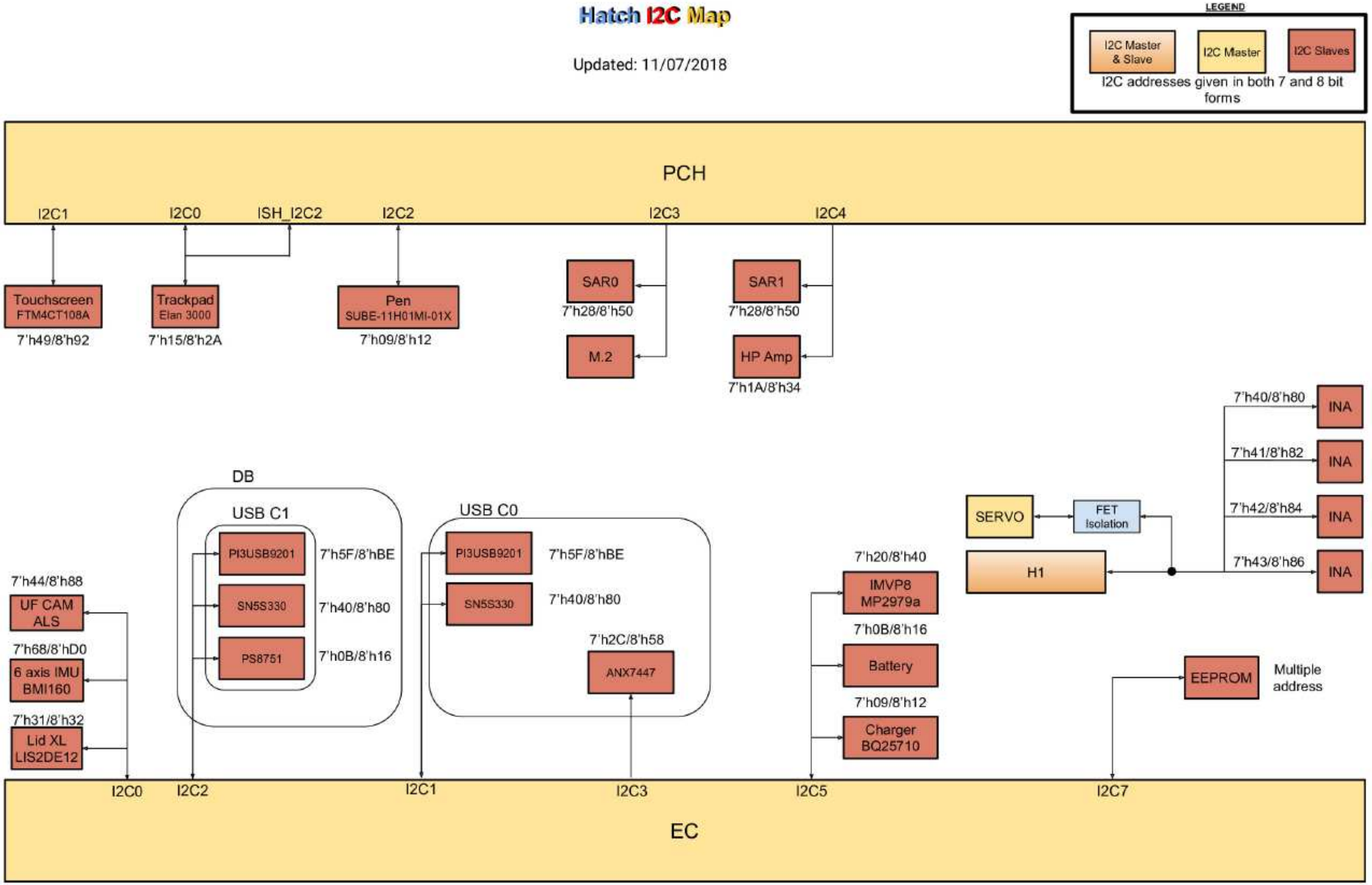
Hatch I2C Map

Updated: 11/07/2018



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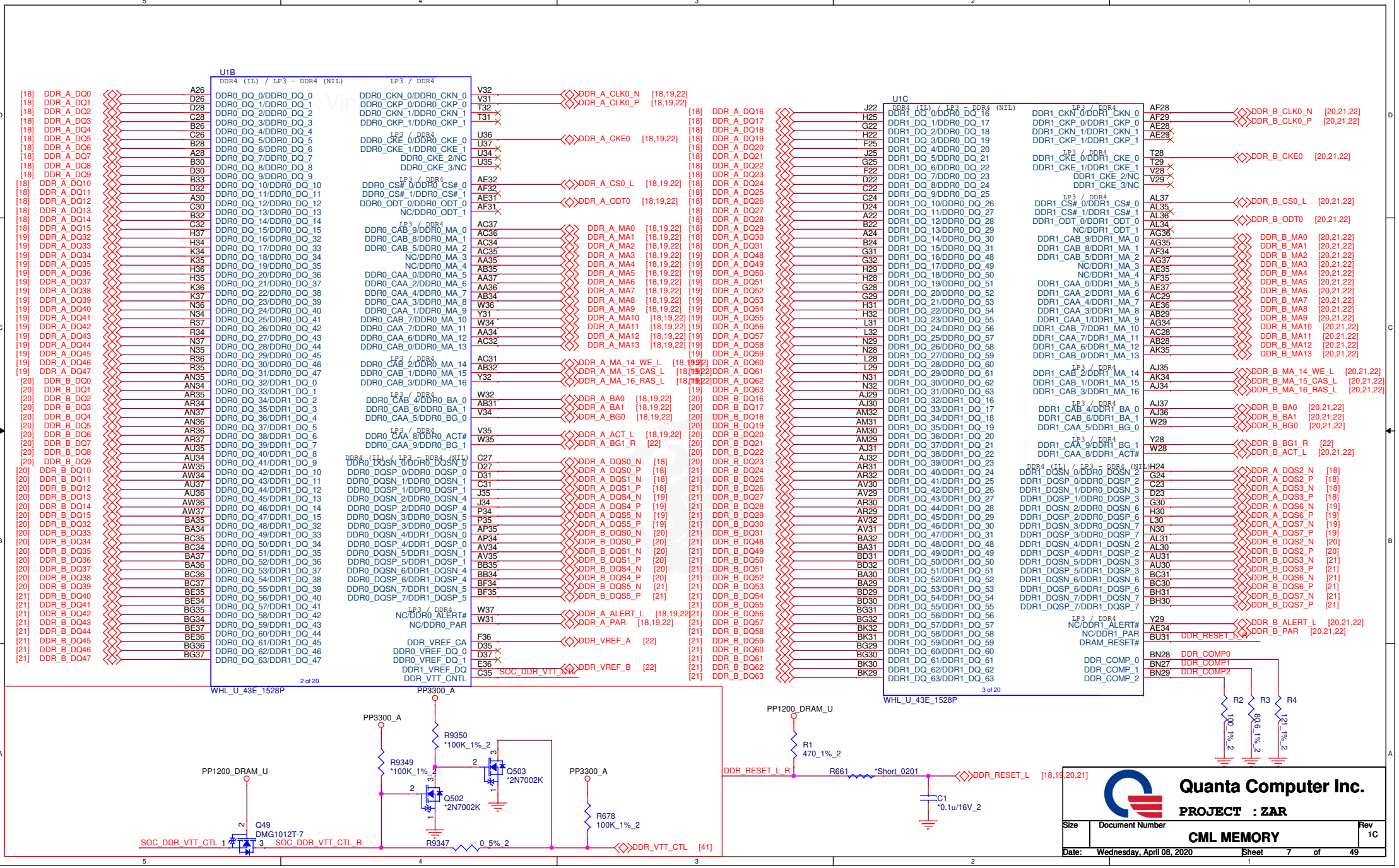
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DDR0_DQ_3/DDR0_DQ_3
DDR0_DQ_4/DDR0_DQ_4
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NC/DDR0_PAR
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DDR1_DQ_17/DDR0_DQ_49
DDR1_DQ_18/DDR0_DQ_50
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DDR1_DQ_27/DDR0_DQ_59
DDR1_DQ_28/DDR0_DQ_60
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DDR1_DQ_30/DDR0_DQ_62
DDR1_DQ_31/DDR0_DQ_63
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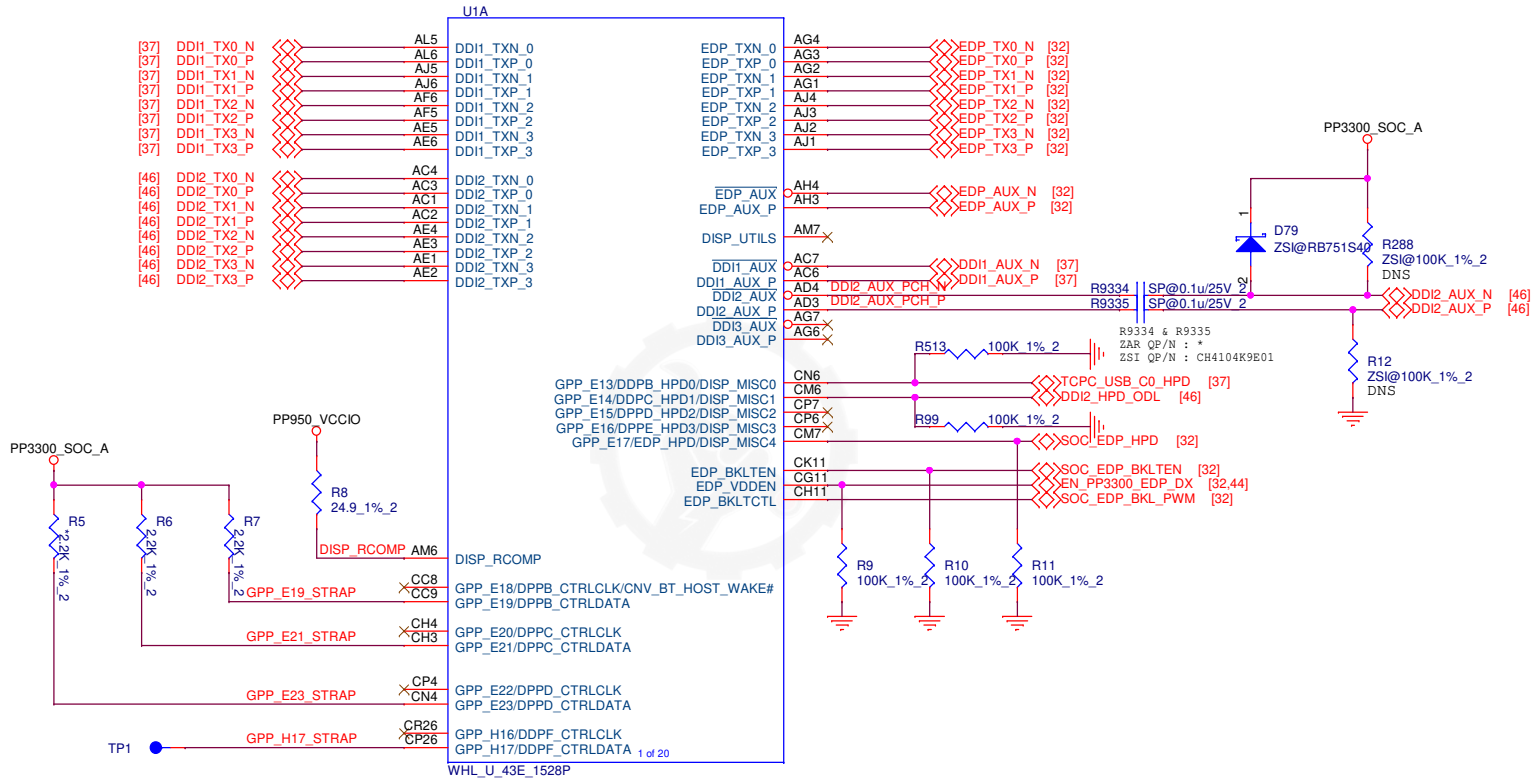
DDR_RESET_L [18,19,20,21]
C1
*0.1u/16V_2
Quanta Computer Inc.
PROJECT : ZAR
Size
Document Number
CML MEMORY
Rev
1C
Date: Wednesday, April 08, 2020
Sheet 7 of 49



[9,10,11,12,14,25,44,45] PP3300_SOC_A
[13,17,40,45] PP950_VCCIO

Quanta Computer Inc.

PROJECT : ZAR

Size	Document Number	Rev
	CML DISPLAY	1C
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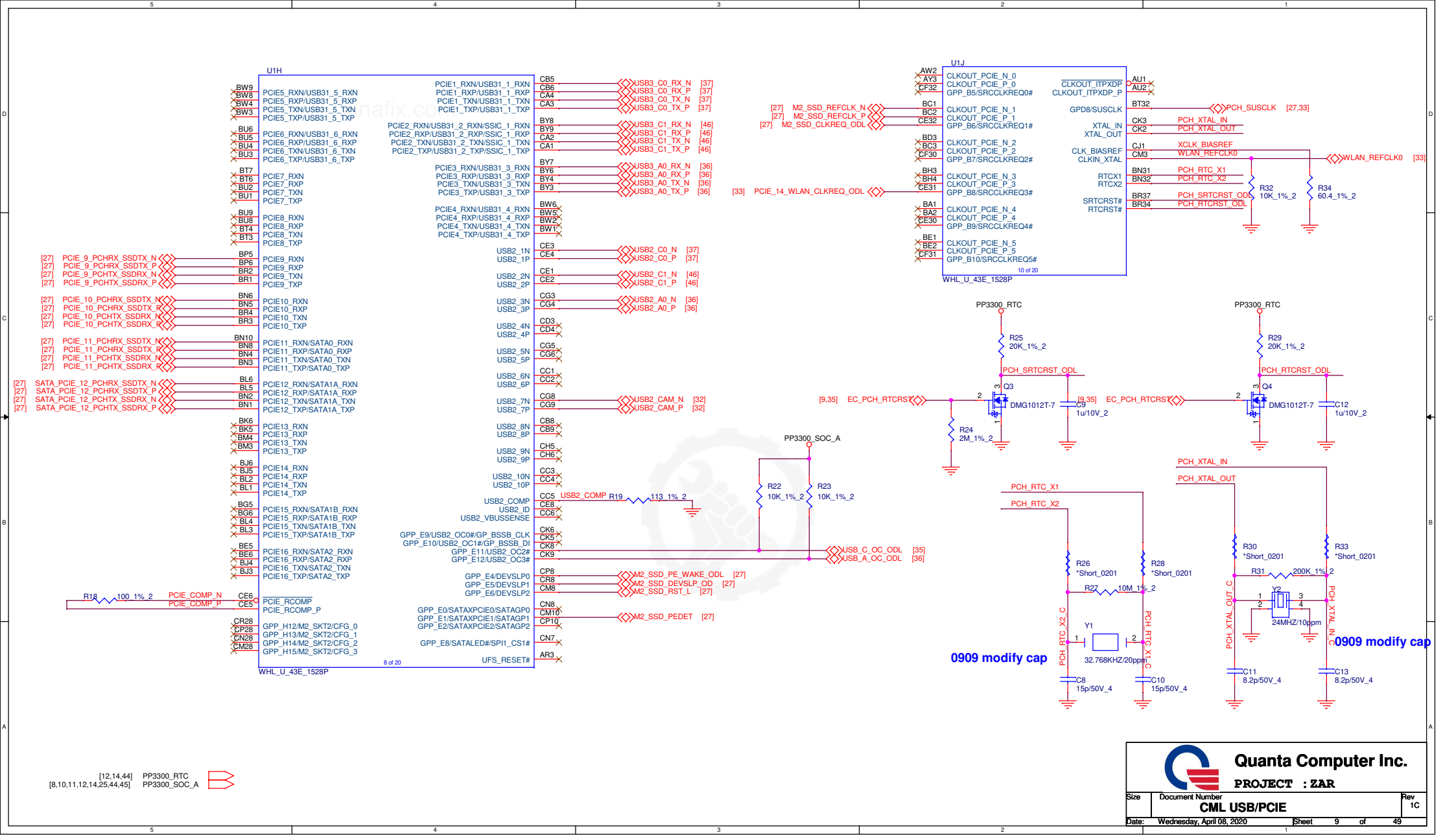
U1H
PCIE5_RXN/USB31_5_RXN
PCIE5_RXP/USB31_5_RXP
PCIE5_TXN/USB31_5_TXN
PCIE5_TXP/USB31_5_TXP
PCIE6_RXN/USB31_6_RXN
PCIE6_RXP/USB31_6_RXP
PCIE6_TXN/USB31_6_TXN
PCIE6_TXP/USB31_6_TXP
PCIE7_RXN
PCIE7_RXP
PCIE7_TXN
PCIE7_TXP
PCIE8_RXN
PCIE8_RXP
PCIE8_TXN
PCIE8_TXP
PCIE9_RXN
PCIE9_RXP
PCIE9_TXN
PCIE9_TXP
PCIE10_RXN
PCIE10_RXP
PCIE10_TXN
PCIE10_TXP
PCIE11_RXN/SATA0_RXN
PCIE11_RXP/SATA0_RXP
PCIE11_TXN/SATA0_TXN
PCIE11_TXP/SATA0_TXP
PCIE12_RXN/SATA1A_RXN
PCIE12_RXP/SATA1A_RXP
PCIE12_TXN/SATA1A_TXN
PCIE12_TXP/SATA1A_TXP
PCIE13_RXN
PCIE13_RXP
PCIE13_TXN
PCIE13_TXP
PCIE14_RXN
PCIE14_RXP
PCIE14_TXN
PCIE14_TXP
PCIE15_RXN/SATA1B_RXN
PCIE15_RXP/SATA1B_RXP
PCIE15_TXN/SATA1B_TXN
PCIE15_TXP/SATA1B_TXP
PCIE16_RXN/SATA2_RXN
PCIE16_RXP/SATA2_RXP
PCIE16_TXN/SATA2_TXN
PCIE16_TXP/SATA2_TXP
PCIE_RCOMP
PCIE_RCOMP_P
GPP_H12/M2_SKT2/CFG_0
GPP_H13/M2_SKT2/CFG_1
GPP_H14/M2_SKT2/CFG_2
GPP_H15/M2_SKT2/CFG_3
8 of 20
WHL_U_43E_1528P
PCIE1_RXN/USB31_1_RXN
PCIE1_RXP/USB31_1_RXP
PCIE1_TXN/USB31_1_TXN
PCIE1_TXP/USB31_1_TXP
PCIE2_RXN/USB31_2_RXN/SSIC_1_RXN
PCIE2_RXP/USB31_2_RXP/SSIC_1_RXP
PCIE2_TXN/USB31_2_TXN/SSIC_1_TXN
PCIE2_TXP/USB31_2_TXP/SSIC_1_TXP
PCIE3_RXN/USB31_3_RXN
PCIE3_RXP/USB31_3_RXP
PCIE3_TXN/USB31_3_TXN
PCIE3_TXP/USB31_3_TXP
PCIE4_RXN/USB31_4_RXN
PCIE4_RXP/USB31_4_RXP
PCIE4_TXN/USB31_4_TXN
PCIE4_TXP/USB31_4_TXP
USB2_1N
USB2_1P
USB2_2N
USB2_2P
USB2_3N
USB2_3P
USB2_4N
USB2_4P
USB2_5N
USB2_5P
USB2_6N
USB2_6P
USB2_7N
USB2_7P
USB2_8N
USB2_8P
USB2_9N
USB2_9P
USB2_10N
USB2_10P
USB2_COMP
USB2_ID
USB2_VBUSSENSE
GPP_E9/USB2_OC0#/GP_BSSB_CLK
GPP_E10/USB2_OC1#/GP_BSSB_DI
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#
GPP_E4/DEVSLP0
GPP_E5/DEVSLP1
GPP_E6/DEVSLP2
GPP_E0/SATAXPCIE0/SATAGP0
GPP_E1/SATAXPCIE1/SATAGP1
GPP_E2/SATAXPCIE2/SATAGP2
GPP_E8/SATALED#/SPI1_CS1#
UFS_RESET#
USB3_C0_RX_N
USB3_C0_RX_P
USB3_C0_TX_N
USB3_C0_TX_P
USB3_C1_RX_N
USB3_C1_RX_P
USB3_C1_TX_N
USB3_C1_TX_P
USB3_A0_RX_N
USB3_A0_RX_P
USB3_A0_TX_N
USB3_A0_TX_P
USB2_C0_N
USB2_C0_P
USB2_C1_N
USB2_C1_P
USB2_A0_N
USB2_A0_P
USB2_CAM_N
USB2_CAM_P
USB2_COMP
R19
113_1%_2
M2_SSD_PE_WAKE_ODL
M2_SSD_DEVSLP_OD
M2_SSD_RST_L
M2_SSD_PEDET
R18
100_1%_2
PCIE_COMP_N
PCIE_COMP_P
U1J
CLKOUT_PCIE_N_0
CLKOUT_PCIE_P_0
GPP_B5/SRCCLKREQ0#
CLKOUT_PCIE_N_1
CLKOUT_PCIE_P_1
GPP_B6/SRCCLKREQ1#
CLKOUT_PCIE_N_2
CLKOUT_PCIE_P_2
GPP_B7/SRCCLKREQ2#
CLKOUT_PCIE_N_3
CLKOUT_PCIE_P_3
GPP_B8/SRCCLKREQ3#
CLKOUT_PCIE_N_4
CLKOUT_PCIE_P_4
GPP_B9/SRCCLKREQ4#
CLKOUT_PCIE_N_5
CLKOUT_PCIE_P_5
GPP_B10/SRCCLKREQ5#
10 of 20
WHL_U_43E_1528P
M2_SSD_REFCLK_N
M2_SSD_REFCLK_P
M2_SSD_CLKREQ_ODL
PCIE_14_WLAN_CLKREQ_ODL
CLKOUT_ITPXDP
CLKOUT_ITPXDP_P
GPD8/SUSCLK
XTAL_IN
XTAL_OUT
CLK_BIASREF
CLKIN_XTAL
RTCX1
RTCX2
SRTCRST#
RTCRST#
PCH_SUSCLK
PCH_XTAL_IN
PCH_XTAL_OUT
XCLK_BIASREF
WLAN_REFCLK0
PCH_RTC_X1
PCH_RTC_X2
PCH_SRTCRST_ODL
PCH_RTCRST_ODL
R32
10K_1%_2
R34
60.4_1%_2
PP3300_RTC
R25
20K_1%_2
R29
20K_1%_2
Q3
Q4
DMG1012T-7
R24
2M_1%_2
C9
1u/10V_2
C12
1u/10V_2
EC_PCH_RTCRST
PP3300_SOC_A
R22
10K_1%_2
R23
10K_1%_2
USB_C_OC_ODL
USB_A_OC_ODL
R26
*Short_0201
R27
10M_1%_2
R28
*Short_0201
Y1
32.768KHZ/20ppm
C8
15p/50V_4
C10
15p/50V_4
R30
*Short_0201
R31
200K_1%_2
R33
*Short_0201
Y2
24MHZ/10ppm
C11
8.2p/50V_4
C13
8.2p/50V_4
0909 modify cap
0909 modify cap
[12,14,44] PP3300_RTC
[8,10,11,12,14,25,44,45] PP3300_SOC_A
Quanta Computer Inc.
PROJECT : ZAR
Size
Document Number
CML USB/PCIE
Rev
1C
Date: Wednesday, April 08, 2020
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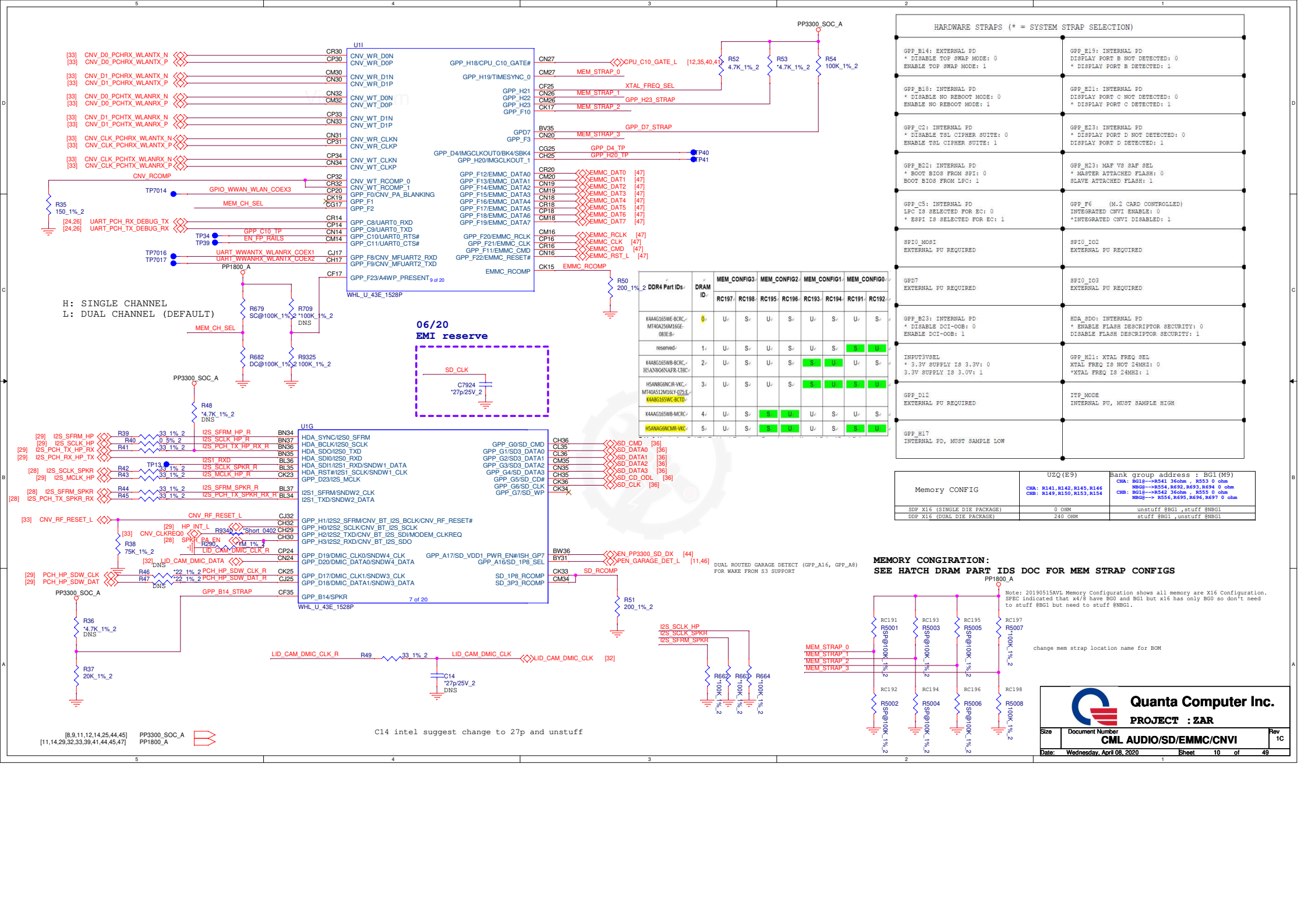
U1I
U1G
PP3300_SOC_A
PP1800_A
H: SINGLE CHANNEL
L: DUAL CHANNEL (DEFAULT)
06/20
EMI reserve
HARDWARE STRAPS (* = SYSTEM STRAP SELECTION)
GPP_B14: EXTERNAL PD
* DISABLE TOP SWAP MODE: 0
ENABLE TOP SWAP MODE: 1
GPP_E19: INTERNAL PD
DISPLAY PORT B NOT DETECTED: 0
* DISPLAY PORT B DETECTED: 1
GPP_B18: INTERNAL PD
* DISABLE NO REBOOT MODE: 0
ENABLE NO REBOOT MODE: 1
GPP_E21: INTERNAL PD
DISPLAY PORT C NOT DETECTED: 0
* DISPLAY PORT C DETECTED: 1
GPP_C2: INTERNAL PD
* DISABLE TSL CIPHER SUITE: 0
ENABLE TSL CIPHER SUITE: 1
GPP_E23: INTERNAL PD
* DISPLAY PORT D NOT DETECTED: 0
DISPLAY PORT D DETECTED: 1
GPP_B22: INTERNAL PD
* BOOT BIOS FROM SPI: 0
BOOT BIOS FROM LPC: 1
GPP_H23: MAF VS SAF SEL
* MASTER ATTACHED FLASH: 0
SLAVE ATTACHED FLASH: 1
GPP_C5: INTERNAL PD
LPC IS SELECTED FOR EC: 0
* ESPI IS SELECTED FOR EC: 1
GPP_F6 (M.2 CARD CONTROLLED)
INTEGRATED CNVI ENABLE: 0
*INTEGRATED CNVI DISABLED: 1
SPI0_MOSI
EXTERNAL PU REQUIRED
SPI0_IO2
EXTERNAL PU REQUIRED
GPD7
EXTERNAL PU REQUIRED
SPI0_IO3
EXTERNAL PU REQUIRED
GPP_B23: INTERNAL PD
* DISABLE DCI-OOB: 0
ENABLE DCI-OOB: 1
HDA_SDO: INTERNAL PD
* ENABLE FLASH DESCRIPTOR SECURITY: 0
DISABLE FLASH DESCRIPTOR SECURITY: 1
INPUT3VSEL
* 3.3V SUPPLY IS 3.3V: 0
3.3V SUPPLY IS 3.0V: 1
GPP_H21: XTAL FREQ SEL
XTAL FREQ IS NOT 24MHZ: 0
*XTAL FREQ IS 24MHZ: 1
GPP_D12
EXTERNAL PU REQUIRED
ITP_MODE
INTERNAL PU, MUST SAMPLE HIGH
GPP_H17
INTERNAL PD, MUST SAMPLE LOW
DDR4 Part IDs
DRAM ID
MEM_CONFIG3
MEM_CONFIG2
MEM_CONFIG1
MEM_CONFIG0
RC197
RC198
RC195
RC196
RC193
RC194
RC191
RC192
K4A4G165WE-BCRC, MT40A256M16GE-083E:B
reserved
K4A8G165WB-BCRC, H5AN8G6NAFR-UHC
H5AN8G6NCJR-VKC, MT40A512M16LY-075:E, K4A8G165WC-BCTD
K4AAG165WB-MCRC
H5ANAG6NCMR-VKC
Memory CONFIG
UZQ(E9)
CHA: R141,R142,R145,R146
CHB: R149,R150,R153,R154
Bank group address : BG1(M9)
CHA: BG1@-->R541 36ohm , R553 0 ohm
NBG@-->R554,R692,R693,R694 0 ohm
CHB: BG1@-->R542 36ohm , R555 0 ohm
NBG@--> R556,R695,R696,R697 0 ohm
SDP X16 (SINGLE DIE PACKAGE)
0 OHM
unstuff @BG1 ,stuff @NBG1
DDP X16 (DUAL DIE PACKAGE)
240 OHM
stuff @BG1 ,unstuff @NBG1
MEMORY CONGIRATION:
SEE HATCH DRAM PART IDS DOC FOR MEM STRAP CONFIGS
DUAL ROUTED GARAGE DETECT (GPP_A16, GPP_A8) FOR WAKE FROM S3 SUPPORT
Note: 20190515AVL Memory Configuration shows all memory are X16 Configuration. SPEC indicated that x4/8 have BG0 and BG1 but x16 has only BG0 so don't need to stuff @BG1 but need to stuff @NBG1.
change mem strap location name for BOM
C14 intel suggest change to 27p and unstuff
Quanta Computer Inc.
PROJECT : ZAR
Size
Document Number
CML AUDIO/SD/EMMC/CNVI
Rev
1C
Date: Wednesday, April 08, 2020
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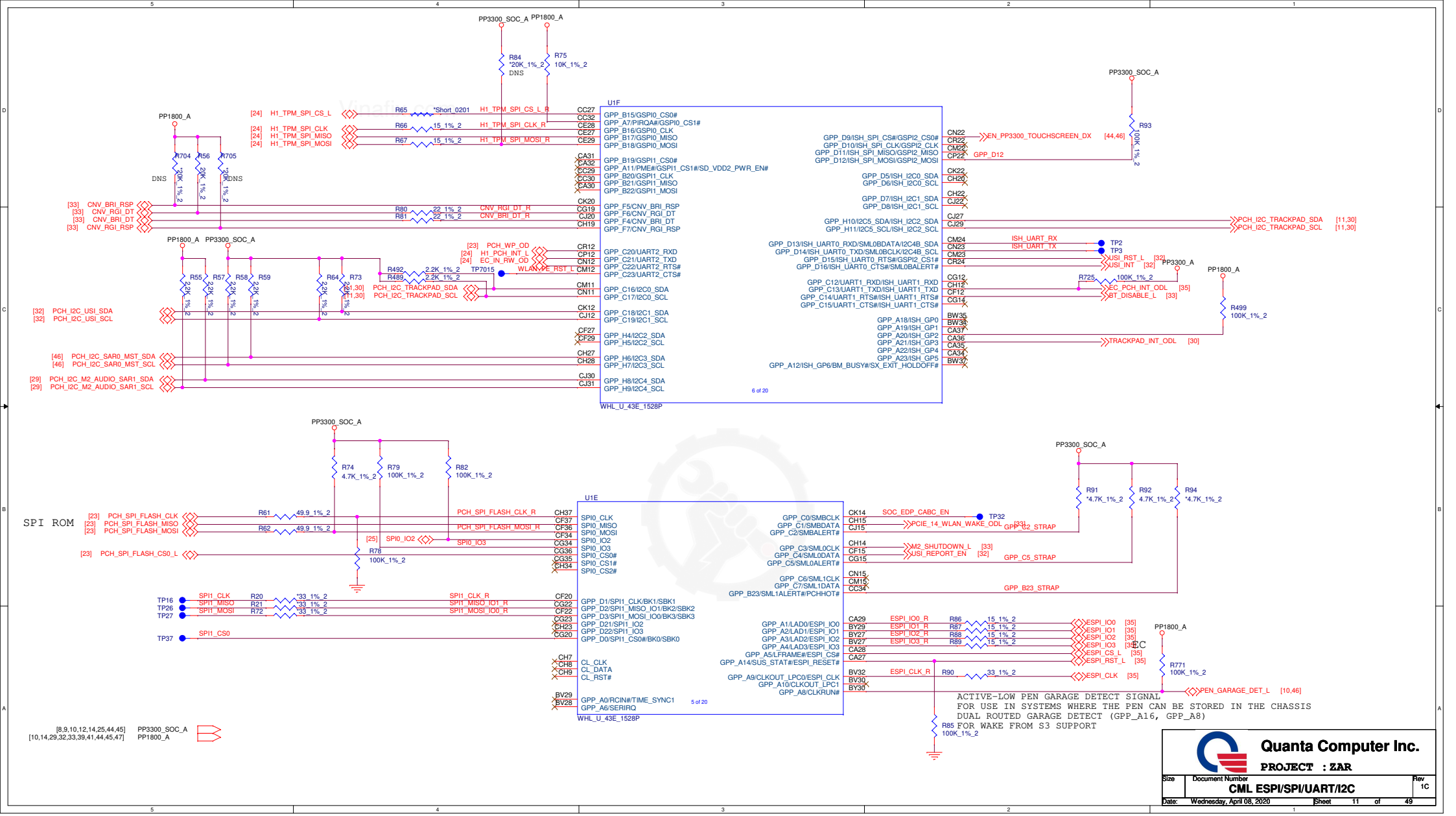
PP3300_SOC_A
PP1800_A
R84 *20K_1%_2 DNS
R75 10K_1%_2
U1F
GPP_B15/GSPI0_CS0#
GPP_A7/PIRQA#/GSPI0_CS1#
GPP_B16/GSPI0_CLK
GPP_B17/GSPI0_MISO
GPP_B18/GSPI0_MOSI
GPP_B19/GSPI1_CS0#
GPP_A11/PME#/GSPI1_CS1#/SD_VDD2_PWR_EN#
GPP_B20/GSPI1_CLK
GPP_B21/GSPI1_MISO
GPP_B22/GSPI1_MOSI
GPP_F5/CNV_BRI_RSP
GPP_F6/CNV_RGI_DT
GPP_F4/CNV_BRI_DT
GPP_F7/CNV_RGI_RSP
GPP_C20/UART2_RXD
GPP_C21/UART2_TXD
GPP_C22/UART2_RTS#
GPP_C23/UART2_CTS#
GPP_C16/I2C0_SDA
GPP_C17/I2C0_SCL
GPP_C18/I2C1_SDA
GPP_C19/I2C1_SCL
GPP_H4/I2C2_SDA
GPP_H5/I2C2_SCL
GPP_H6/I2C3_SDA
GPP_H7/I2C3_SCL
GPP_H8/I2C4_SDA
GPP_H9/I2C4_SCL
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WHL_U_43E_1528P
GPP_D9/ISH_SPI_CS#/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/GSPI2_CLK
GPP_D11/ISH_SPI_MISO/GSPI2_MISO
GPP_D12/ISH_SPI_MOSI/GSPI2_MOSI
GPP_D5/ISH_I2C0_SDA
GPP_D6/ISH_I2C0_SCL
GPP_D7/ISH_I2C1_SDA
GPP_D8/ISH_I2C1_SCL
GPP_H10/I2C5_SDA/ISH_I2C2_SDA
GPP_H11/I2C5_SCL/ISH_I2C2_SCL
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#
GPP_D16/ISH_UART0_CTS#/SML0BALERT#
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_A18/ISH_GP0
GPP_A19/ISH_GP1
GPP_A20/ISH_GP2
GPP_A21/ISH_GP3
GPP_A22/ISH_GP4
GPP_A23/ISH_GP5
GPP_A12/ISH_GP6/BM_BUSY#/SX_EXIT_HOLDOFF#
R704 20K_1%_2 DNS
R56 20K_1%_2
R705 20K_1%_2 DNS
R65 *Short_0201
R66 15_1%_2
R67 15_1%_2
R80 22_1%_2
R81 22_1%_2
R93 100K_1%_2
R55 2.2K_1%_2
R57 2.2K_1%_2
R58 2.2K_1%_2
R59 2.2K_1%_2
R64 2.2K_1%_2
R73 2.2K_1%_2
R492 2.2K_1%_2
R489 2.2K_1%_2
TP7015
R725 100K_1%_2
R499 100K_1%_2
TP2
TP3
R74 4.7K_1%_2
R79 100K_1%_2
R82 100K_1%_2
R61 49.9_1%_2
R62 49.9_1%_2
R78 100K_1%_2
SPI ROM
U1E
SPI0_CLK
SPI0_MISO
SPI0_MOSI
SPI0_IO2
SPI0_IO3
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_C5/SML0ALERT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#
GPP_D1/SPI1_CLK/BK1/SBK1
GPP_D2/SPI1_MISO_IO1/BK2/SBK2
GPP_D3/SPI1_MOSI_IO0/BK3/SBK3
GPP_D21/SPI1_IO2
GPP_D22/SPI1_IO3
GPP_D0/SPI1_CS0#/BK0/SBK0
CL_CLK
CL_DATA
CL_RST#
GPP_A0/RCIN#/TIME_SYNC1
GPP_A6/SERIRQ
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WHL_U_43E_1528P
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A8/CLKRUN#
R91 *4.7K_1%_2
R92 4.7K_1%_2
R94 *4.7K_1%_2
R20 *33_1%_2
R21 *33_1%_2
R72 *33_1%_2
R86 15_1%_2
R87 15_1%_2
R88 15_1%_2
R89 15_1%_2
R90 33_1%_2
R771 100K_1%_2
R85 100K_1%_2
EC
ACTIVE-LOW PEN GARAGE DETECT SIGNAL
FOR USE IN SYSTEMS WHERE THE PEN CAN BE STORED IN THE CHASSIS
DUAL ROUTED GARAGE DETECT (GPP_A16, GPP_A8)
FOR WAKE FROM S3 SUPPORT
Quanta Computer Inc.
PROJECT : ZAR
CML ESPI/SPI/UART/I2C
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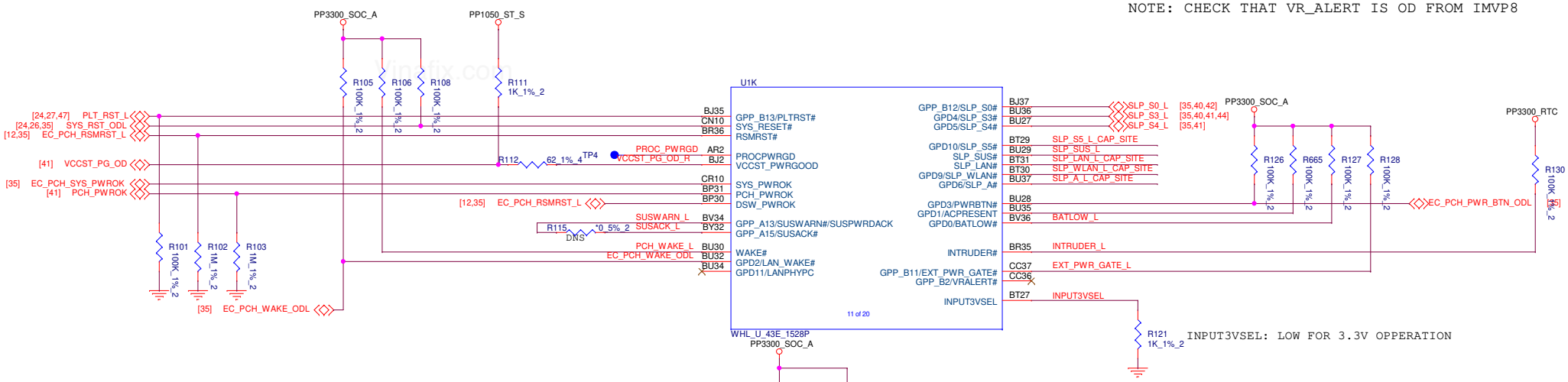
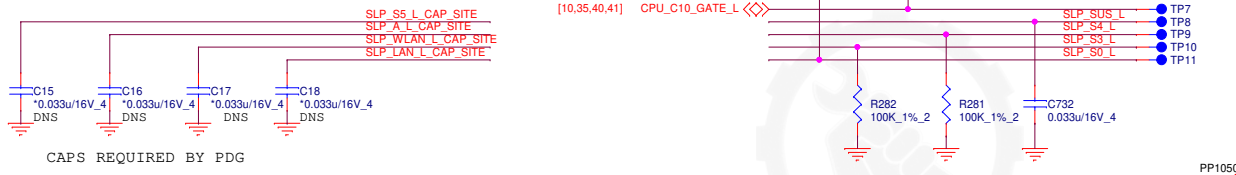
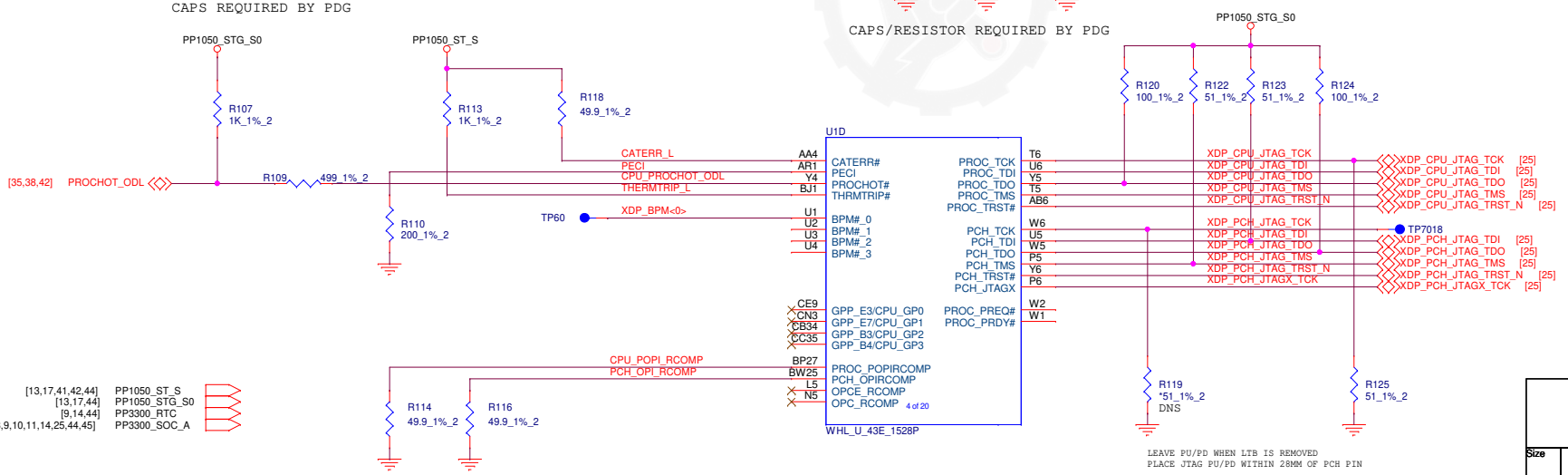
NOTE: CHECK THAT VR_ALERT IS OD FROM IMVP8





CAPS REQUIRED BY PDG

CAPS/RESISTOR REQUIRED BY PDG



[13,17,41,42,44] PP1050_ST_S
[13,17,44] PP1050_STG_S0
[9,14,44] PP3300_RTC
[8,9,10,11,14,25,44,45] PP3300_SOC_A

LEAVE PU/PD WHEN LTB IS REMOVED
PLACE JTAG PU/PD WITHIN 28MM OF PCH PIN

Quanta Computer Inc.
PROJECT : ZAR

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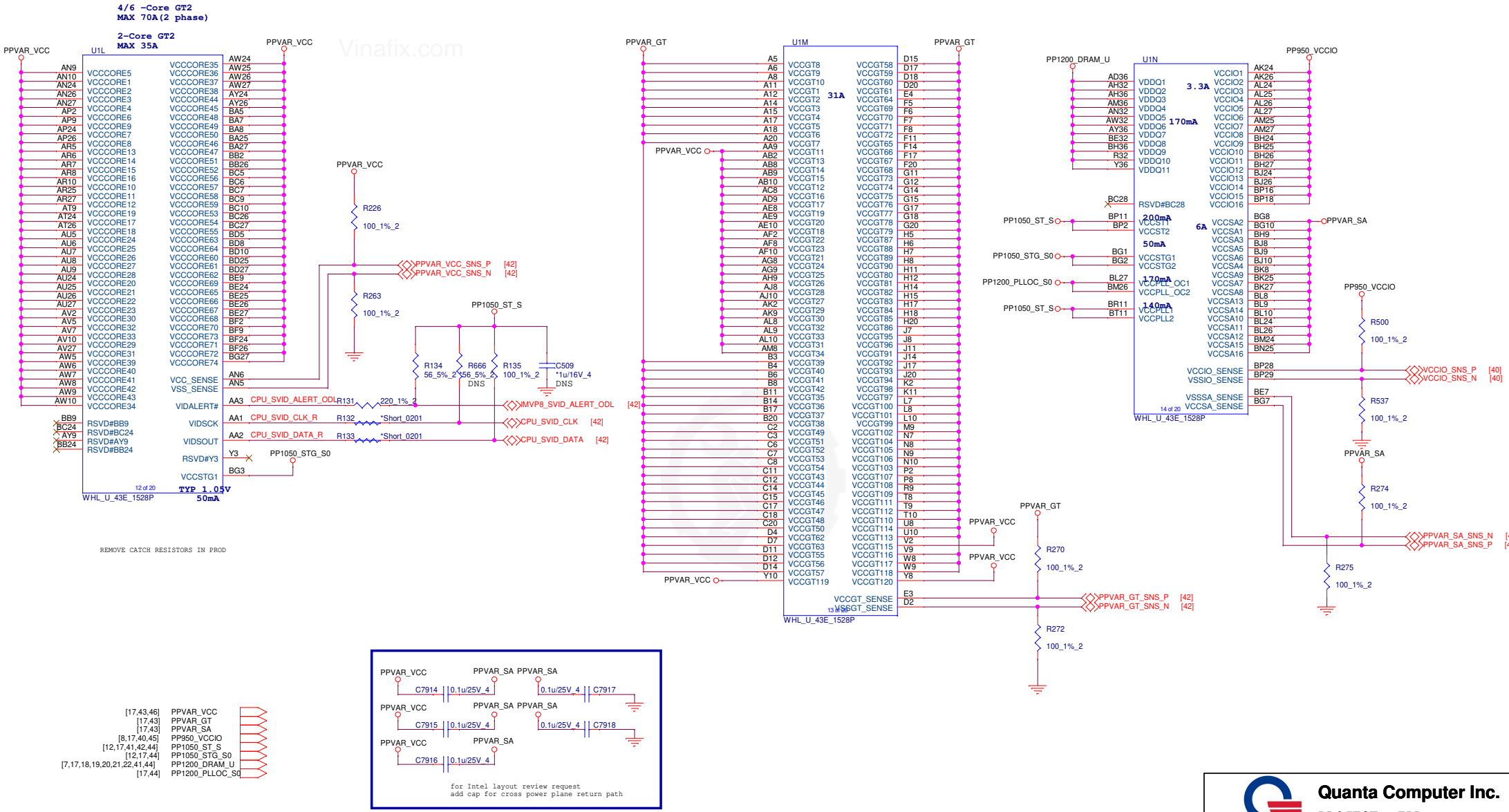
4/6 -Core GT2
MAX 70A(2 phase)
2-Core GT2
MAX 35A
U1L
U1M
U1N
PPVAR_VCC
PPVAR_GT
PP1050_ST_S
PP1050_STG_S0
PP1200_PLLOC_S0
PP1200_DRAM_U
PP950_VCCIO
PPVAR_SA
R226
R263
R134
R666
R135
C509
R131
R132
R133
R270
R272
R500
R537
R274
R275
CPU_SVID_ALERT_ODL
CPU_SVID_CLK_R
CPU_SVID_DATA_R
IMVP8_SVID_ALERT_ODL
CPU_SVID_CLK
CPU_SVID_DATA
PPVAR_VCC_SNS_P
PPVAR_VCC_SNS_N
PPVAR_GT_SNS_P
PPVAR_GT_SNS_N
VCCIO_SNS_P
VCCIO_SNS_N
PPVAR_SA_SNS_N
PPVAR_SA_SNS_P
WHL_U_43E_1528P
TYP 1.05V
50mA
3.3A
170mA
200mA
6A
50mA
170mA
140mA
REMOVE CATCH RESISTORS IN PROD
for Intel layout review request
add cap for cross power plane return path
C7914
C7915
C7916
C7917
C7918
0.1u/25V_4
[17,43,46] PPVAR_VCC
[17,43] PPVAR_GT
[17,43] PPVAR_SA
[8,17,40,45] PP950_VCCIO
[12,17,41,42,44] PP1050_ST_S
[12,17,44] PP1050_STG_S0
[7,17,18,19,20,21,22,41,44] PP1200_DRAM_U
[17,44] PP1200_PLLOC_S0
Quanta Computer Inc.
PROJECT : ZAR
Size
Document Number
CML CORE POWER
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1C
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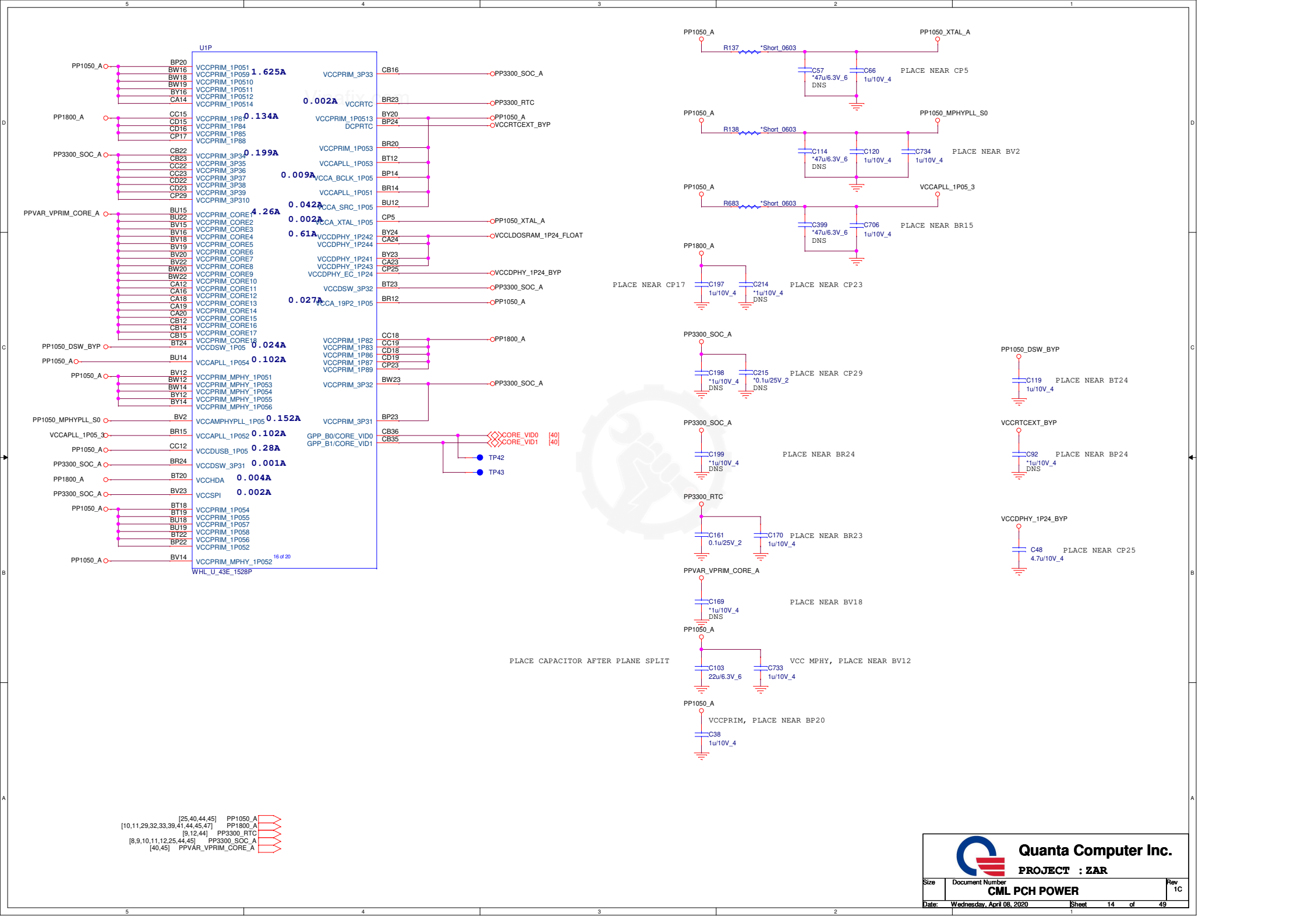
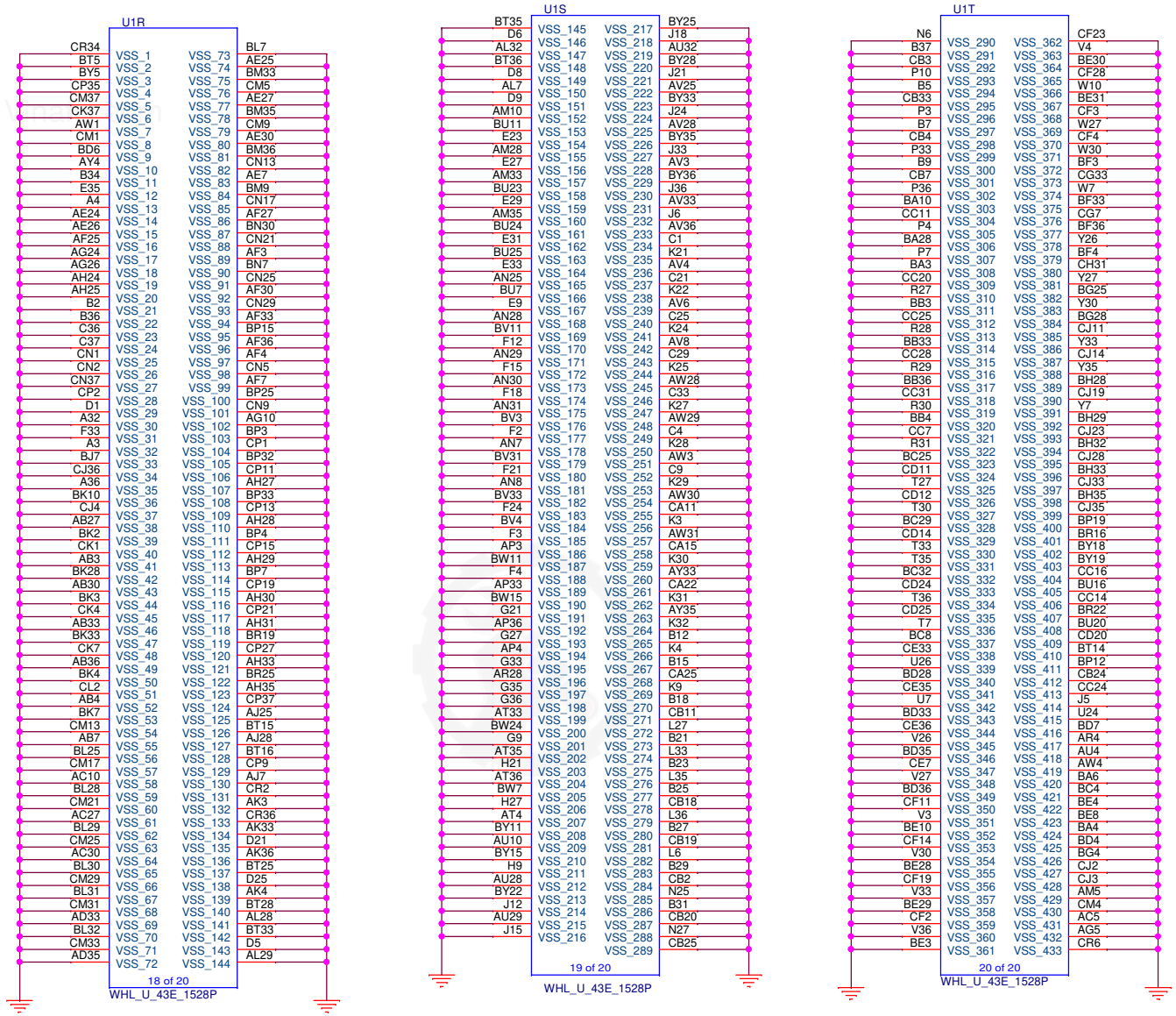

U1P
WHL_U_43E_1528P
16 of 20
PP1050_A
PP1800_A
PP3300_SOC_A
PPVAR_VPRIM_CORE_A
PP1050_DSW_BYP
PP1050_MPHYPLL_S0
VCCAPLL_1P05_3
PP3300_RTC
VCCRTCEXT_BYP
VCCDPHY_1P24_BYP
PP1050_XTAL_A
VCCAPLL_1P05_3
PP1050_MPHYPLL_S0
VCCCLDOSRAM_1P24_FLOAT
VCCDPHY_1P24_BYP
CORE_VID0 [40]
CORE_VID1 [40]
TP42
TP43
1.625A
0.134A
0.199A
0.009A
4.26A
0.002A
0.61A
0.027A
0.024A
0.102A
0.152A
0.28A
0.001A
0.004A
0.002A
R137 *Short_0603
C57 *47u/6.3V_6 DNS
C66 1u/10V_4
PLACE NEAR CP5
R138 *Short_0603
C114 *47u/6.3V_6 DNS
C120 1u/10V_4
C734 1u/10V_4
PLACE NEAR BV2
R683 *Short_0603
C399 *47u/6.3V_6 DNS
C706 1u/10V_4
PLACE NEAR BR15
PLACE NEAR CP17
C197 1u/10V_4
C214 *1u/10V_4 DNS
PLACE NEAR CP23
C198 *1u/10V_4 DNS
C215 *0.1u/25V_2 DNS
PLACE NEAR CP29
C119 1u/10V_4
PLACE NEAR BT24
C199 *1u/10V_4 DNS
PLACE NEAR BR24
C92 *1u/10V_4 DNS
PLACE NEAR BP24
C161 0.1u/25V_2
C170 1u/10V_4
PLACE NEAR BR23
C48 4.7u/10V_4
PLACE NEAR CP25
C169 *1u/10V_4 DNS
PLACE NEAR BV18
PLACE CAPACITOR AFTER PLANE SPLIT
C103 22u/6.3V_6
C733 1u/10V_4
VCC MPHY, PLACE NEAR BV12
VCCPRIM, PLACE NEAR BP20
C38 1u/10V_4
[25,40,44,45] PP1050_A
[10,11,29,32,33,39,41,44,45,47] PP1800_A
[9,12,44] PP3300_RTC
[8,9,10,11,12,25,44,45] PP3300_SOC_A
[40,45] PPVAR_VPRIM_CORE_A
Quanta Computer Inc.
PROJECT : ZAR
Size
Document Number
CML PCH POWER
Rev
1C
Date: Wednesday, April 08, 2020
Sheet 14 of 49

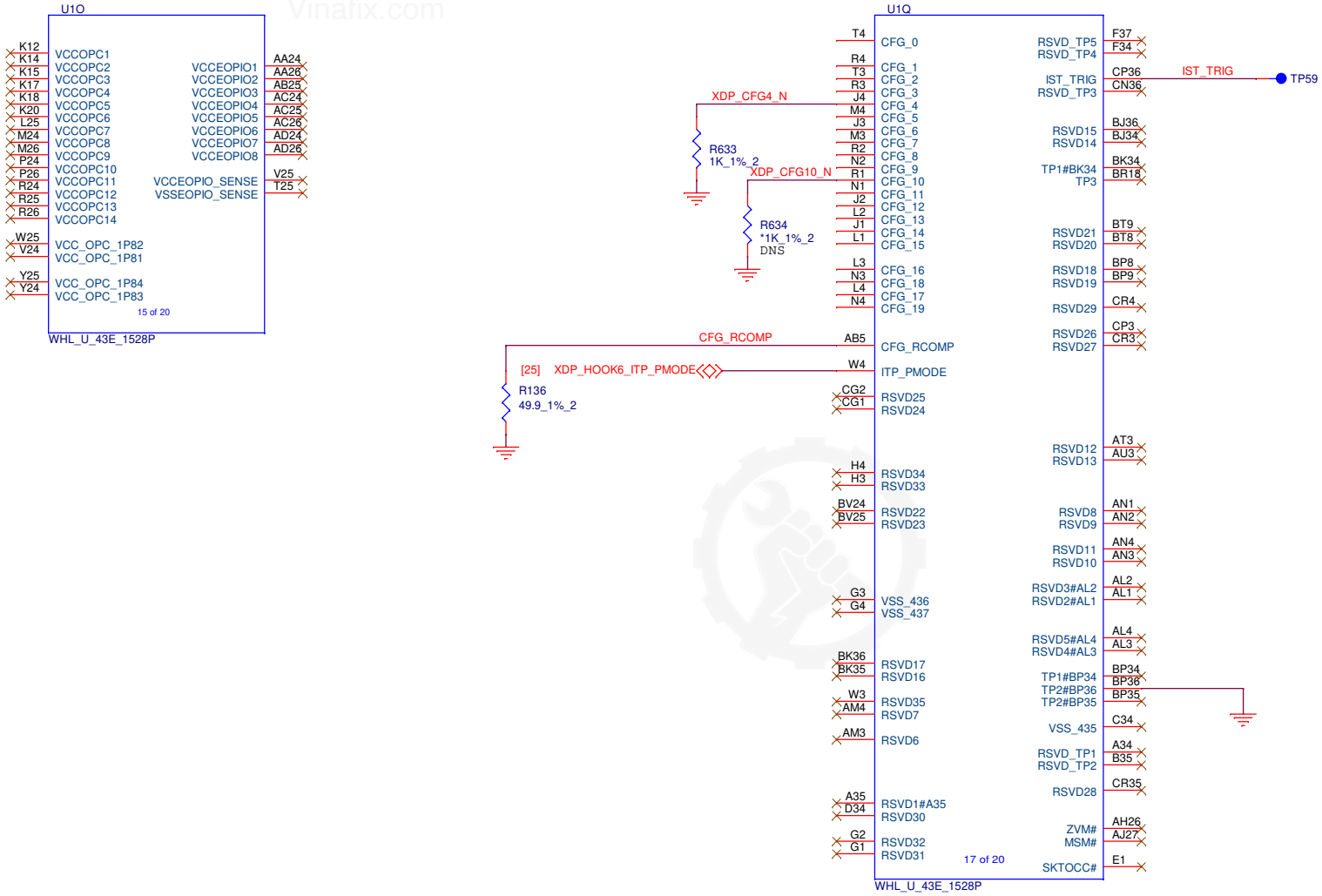


Quanta Computer Inc.

PROJECT : ZAR

Size	Document Number	Rev
	CML GND	1C

Date: Wednesday, April 08, 2020 Sheet 15 of 49



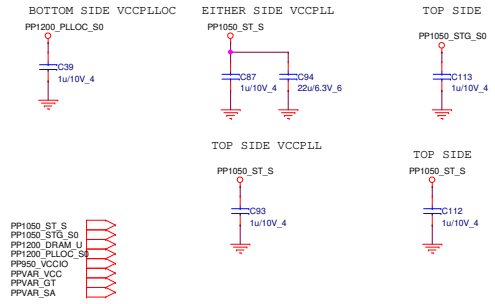
Quanta Computer Inc.		
PROJECT : ZAR		
Size	Document Number: CML DEBUG/RSVD	Rev: 1C
Date: Wednesday, April 08, 2020	Sheet 16 of 49	

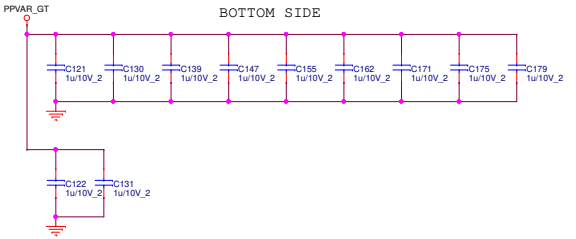
CPU DECOUPLING

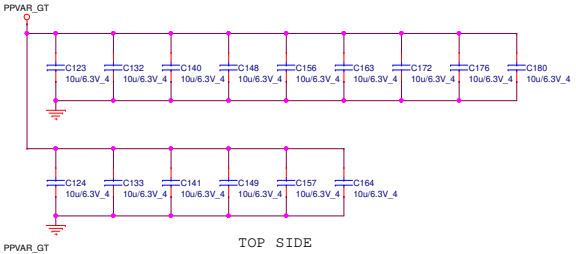
CH5223MEB00
CAP CHIP 2.2U 16V(+-20%,X6S,0402)

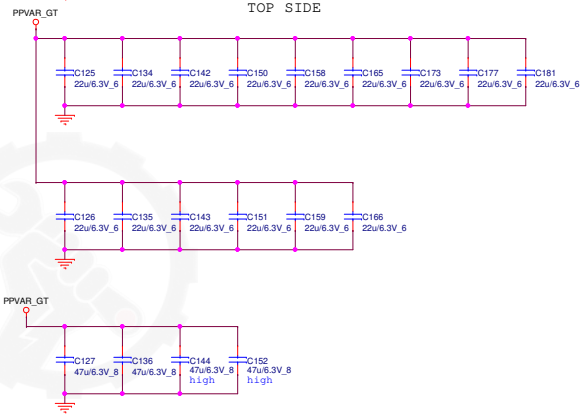
CH6101MEB01
CAP CHIP 10UF 6.3V(+-20%,X6S,0402)

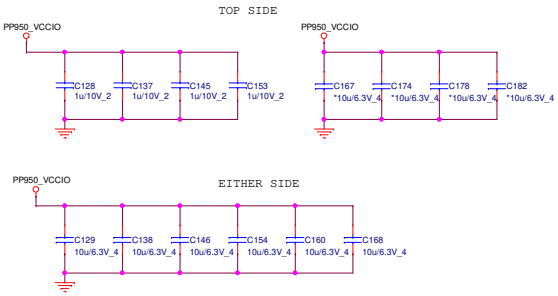
CH6221ME900
CAP CHIP 22U 6.3V(+-20%,X6S,0603)

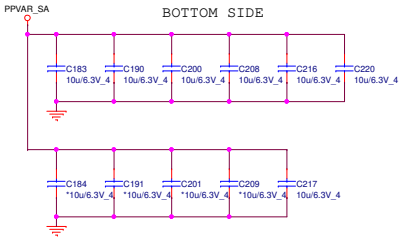


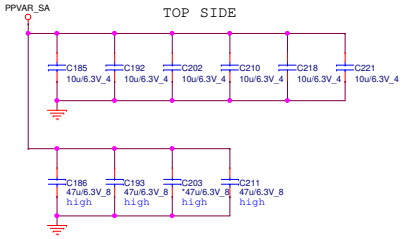


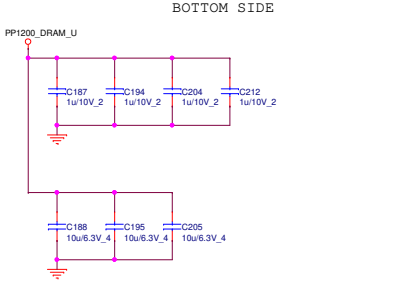






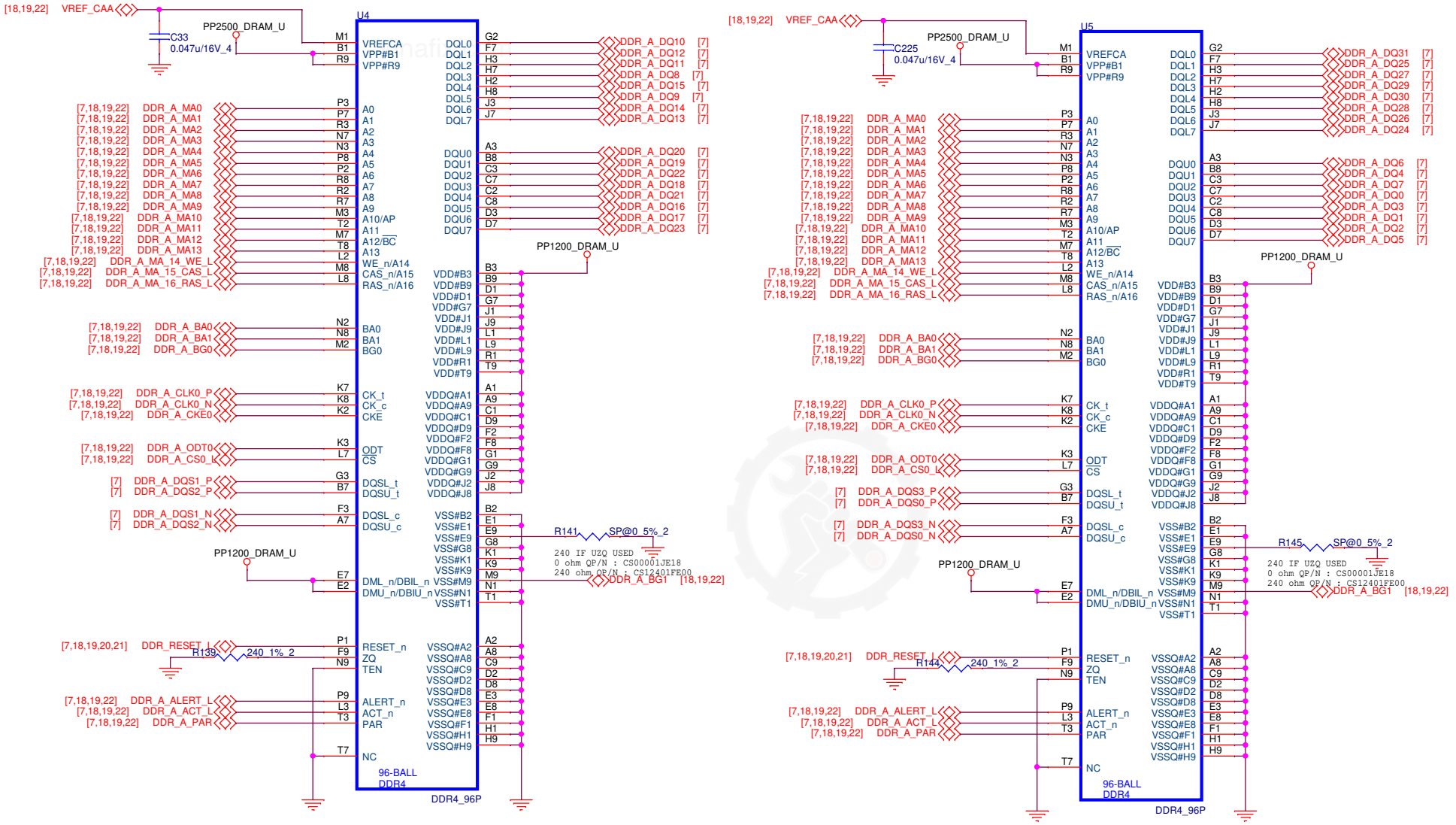




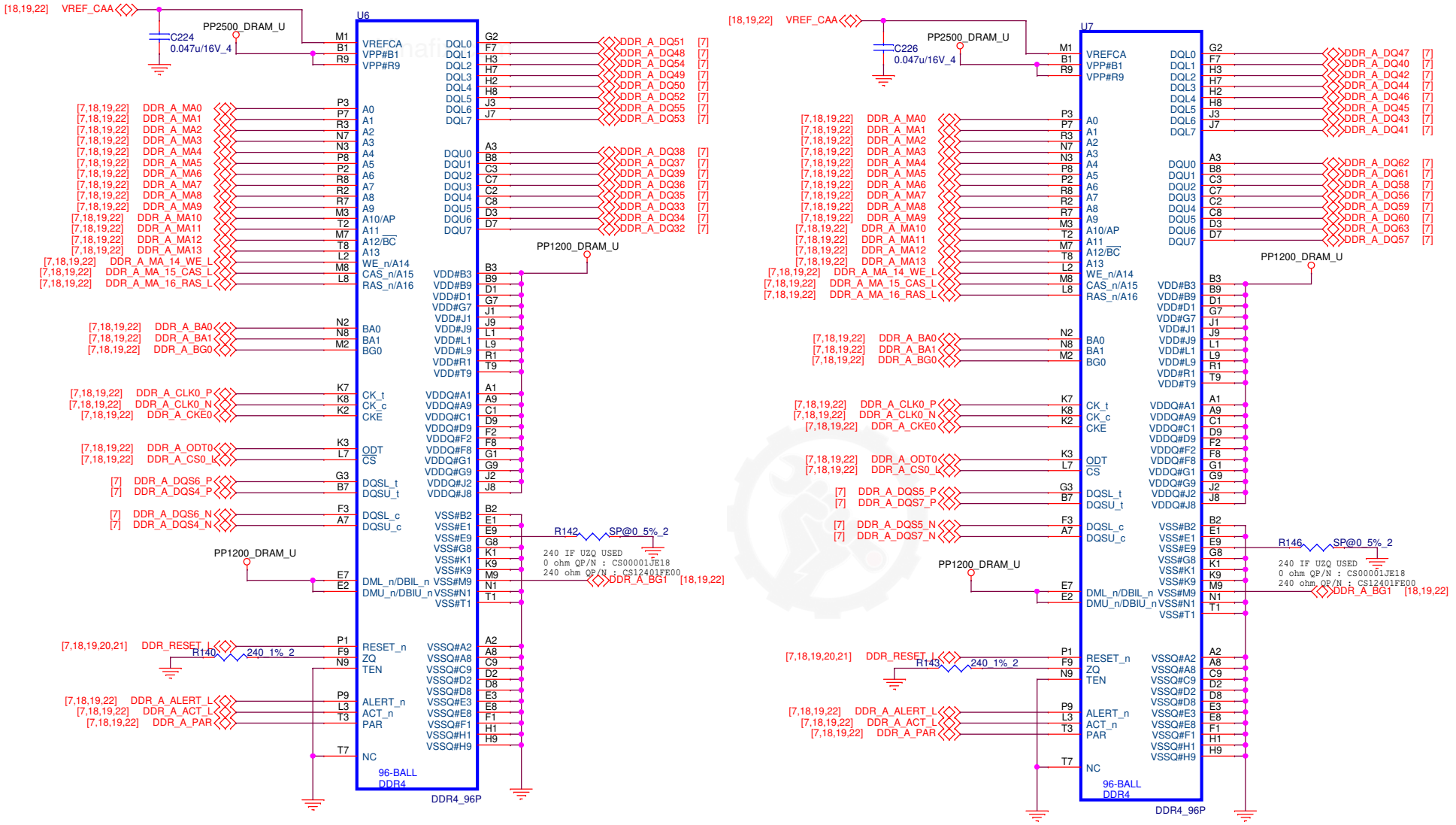


Quanta Computer Inc.
PROJECT : ZAR

Size	Document Number	Rev
	CML POWER RAIL DECOUPLING	1C
Date: Wednesday, April 08, 2020	Sheet 17 of 49	



Quanta Computer Inc.		
PROJECT : ZAR		
Size	Document Number: MEMORY CH A-1 DDR4	Rev: 1C
Date: Wednesday, April 08, 2020	Sheet 18 of 49	

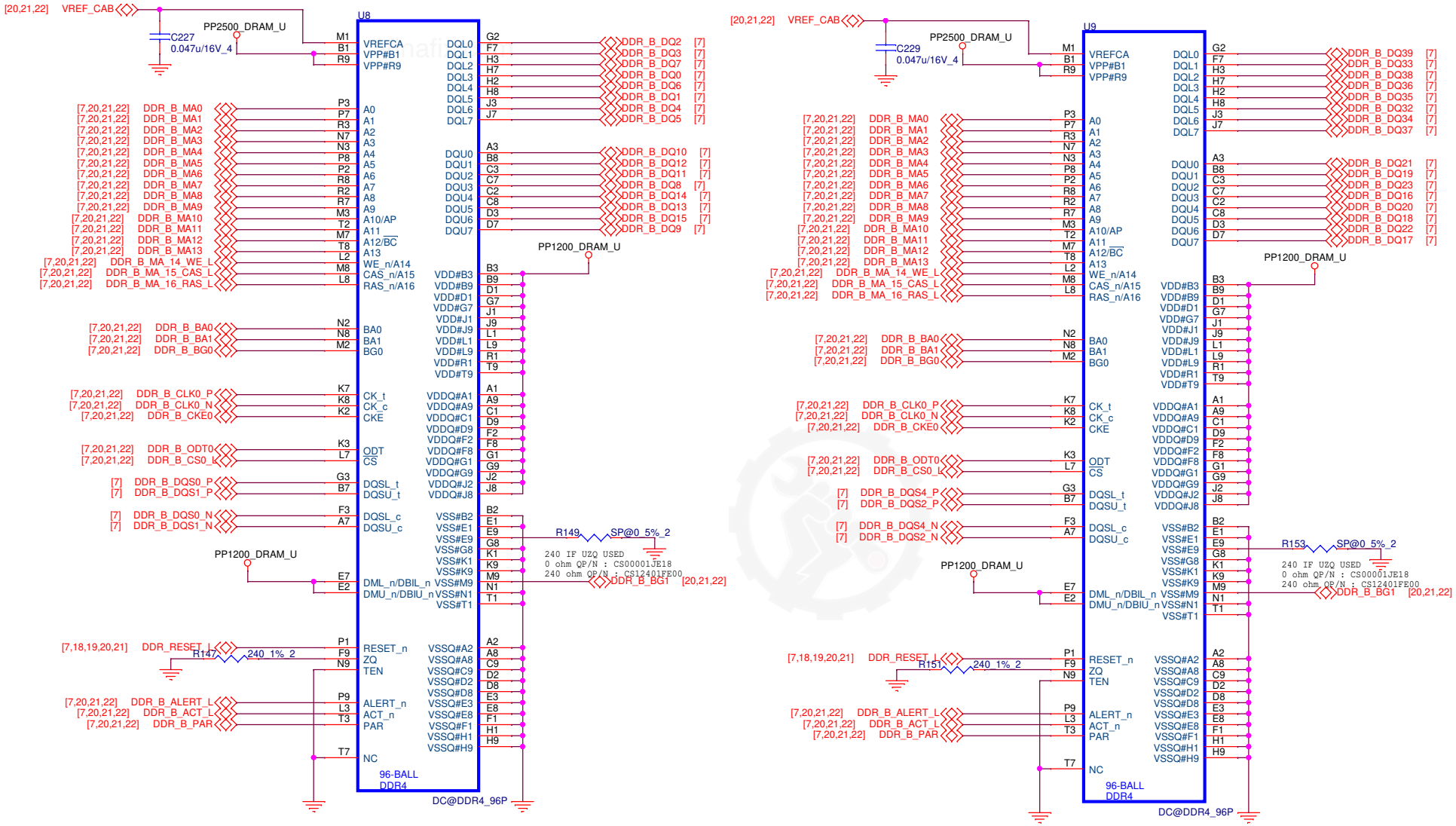


Quanta Computer Inc.

PROJECT : ZAR

Size	Document Number	Rev
	MEMORY CH A-2 DDR4	1C

Date: Wednesday, April 08, 2020 Sheet 19 of 49

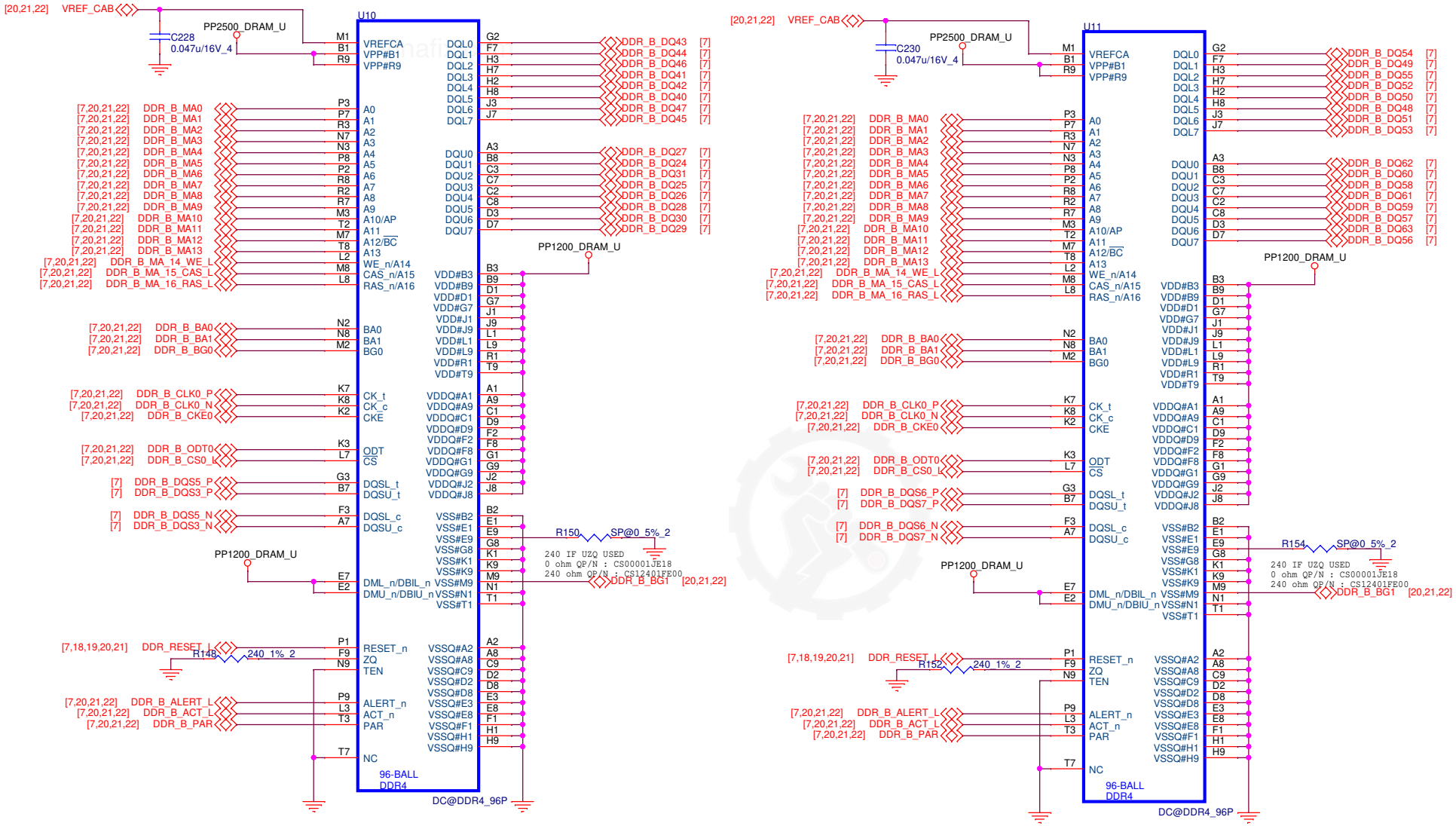


[7,13,17,18,19,21,22,41,44] PP1200_DRAM_U
[18,19,21,22,41,45] PP2500_DRAM_U

Quanta Computer Inc.

PROJECT : ZAR

Size	Document Number	Rev
	MEMORY CH B-1 DDR4	1C
Date: Wednesday, April 08, 2020	Sheet 20 of 49	



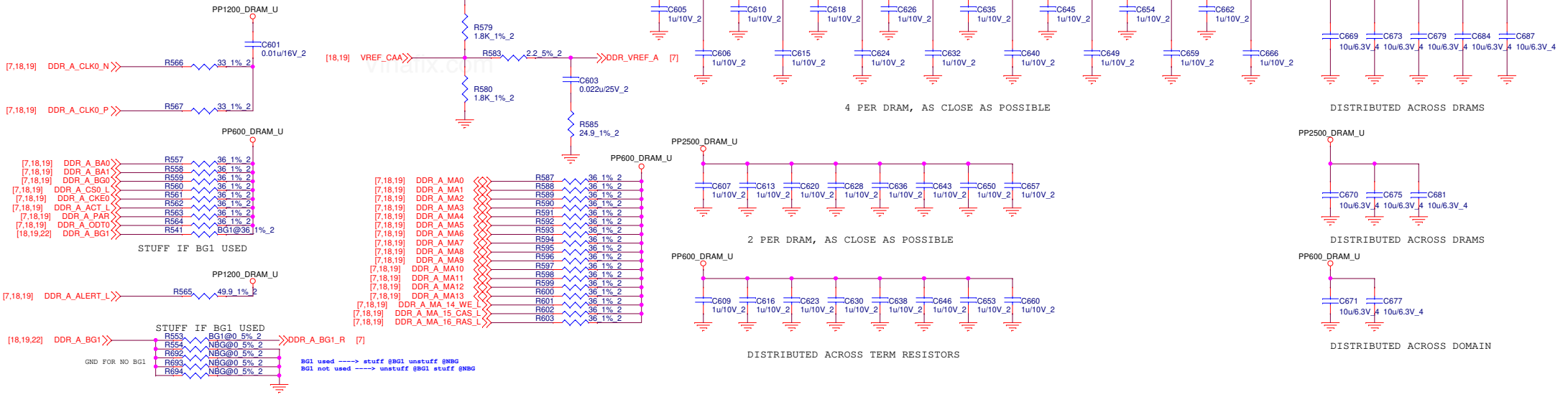
Quanta Computer Inc.

PROJECT : ZAR

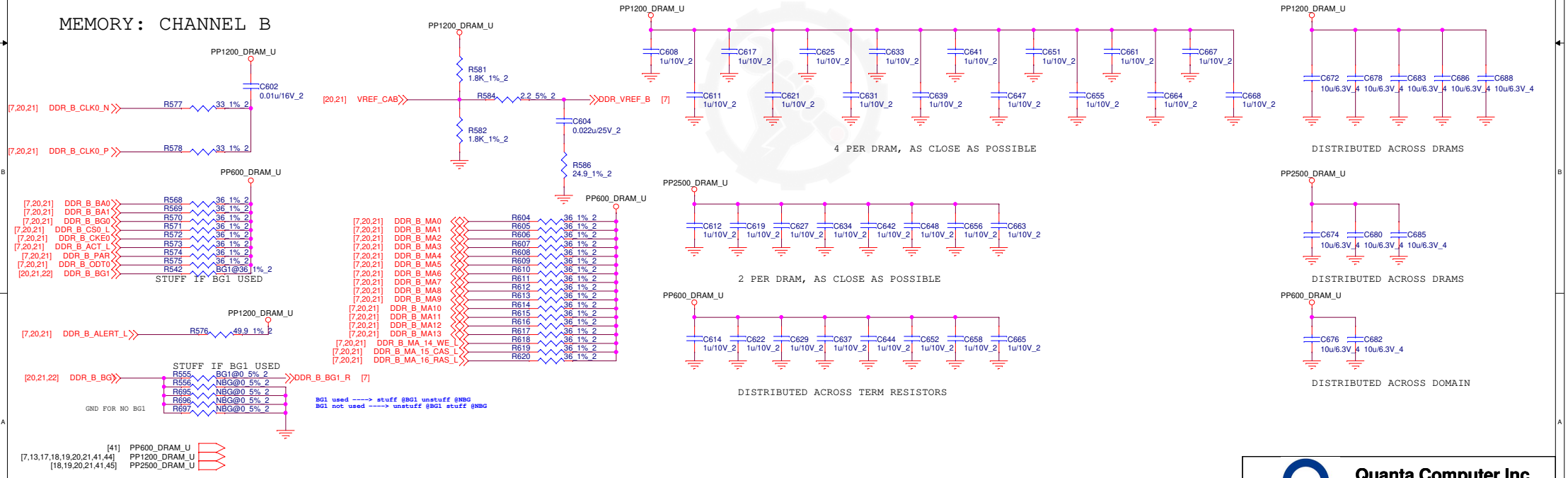
Size	Document Number	Rev
	MEMORY CH B-2 DDR4	1C

Date: Wednesday, April 08, 2020 Sheet 21 of 49

MEMORY: CHANNEL A



MEMORY: CHANNEL B

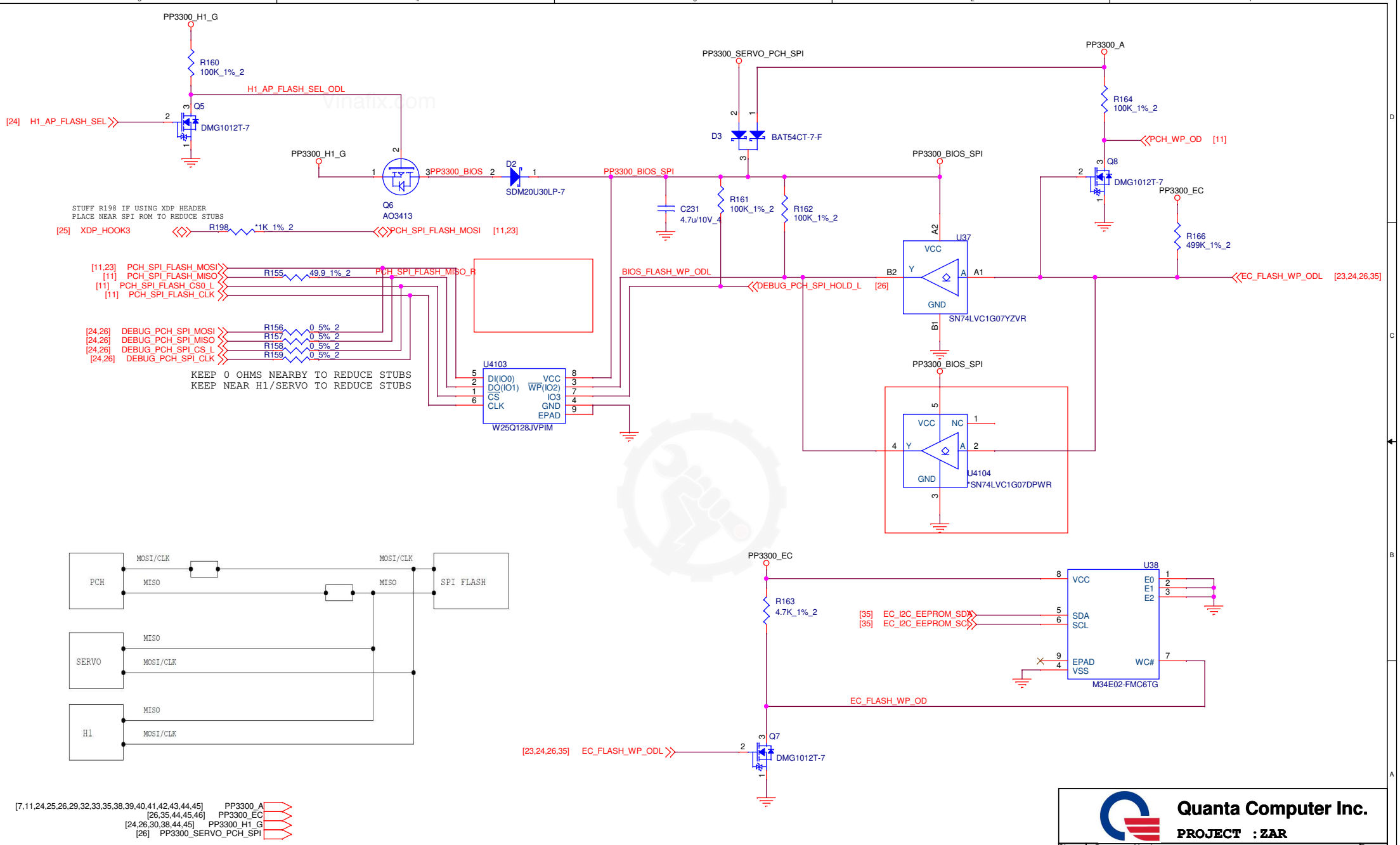


Quanta Computer Inc.

PROJECT : ZAR

Size	Document Number	Rev
	MEMORY DECOUPLING/TERM	1C

Date: Wednesday, April 08, 2020 Sheet 22 of 49

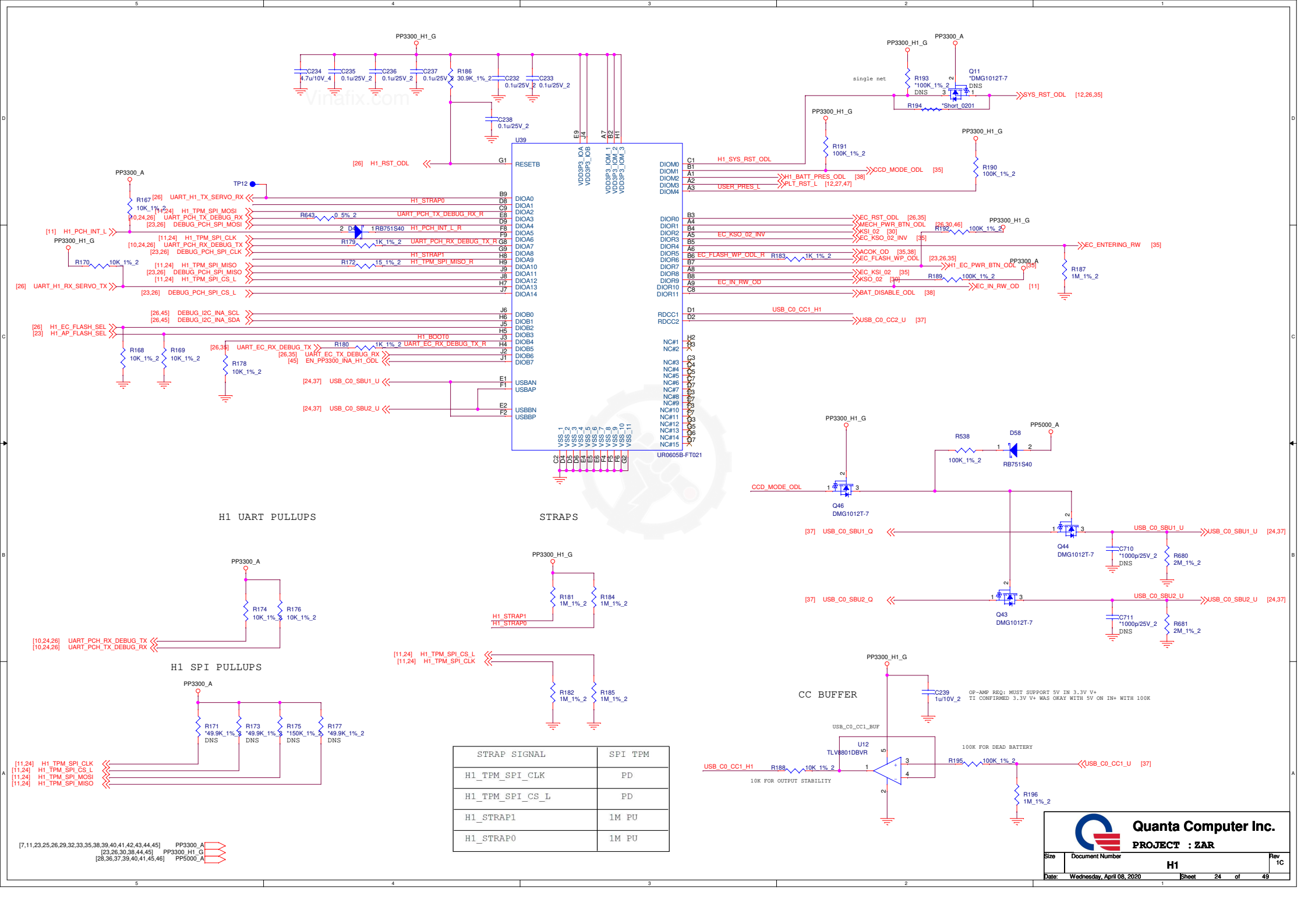


Quanta Computer Inc.

PROJECT : ZAR

Size	Document Number	Rev
	SPI ROM	1C

Date: Wednesday, April 08, 2020 Sheet 23 of 49



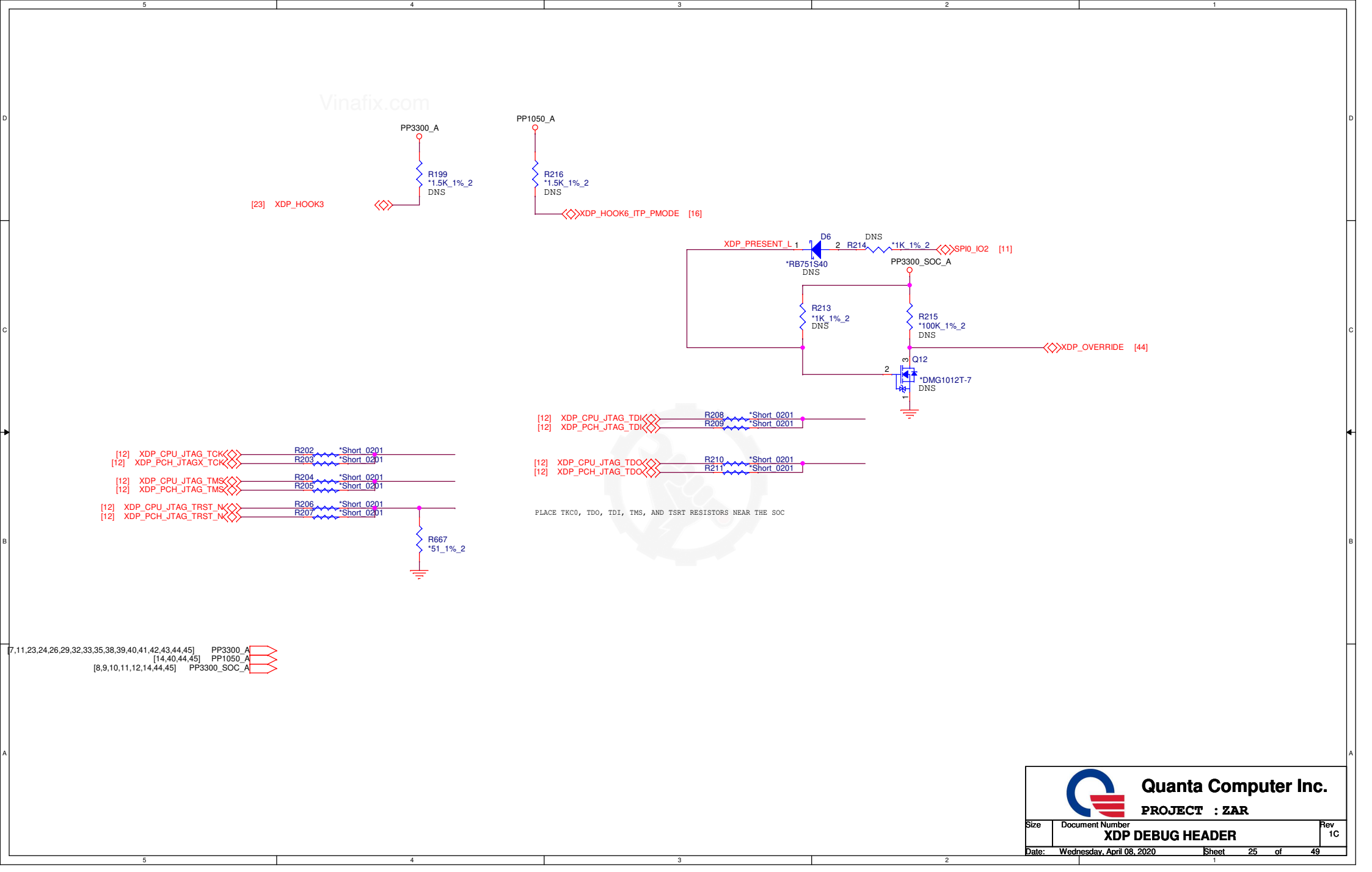
STRAP SIGNAL	SPI TPM
H1_TPM_SPI_CLK	PD
H1_TPM_SPI_CS_L	PD
H1_STRAP1	1M PU
H1_STRAP0	1M PU

[7,11,23,25,26,29,32,33,35,38,39,40,41,42,43,44,45] PP3300_A
[23,26,30,38,44,45] PP3300_H1_G
[28,36,37,39,40,41,45,46] PP5000_A

Quanta Computer Inc.
PROJECT : ZAR

Size	Document Number	Rev
	H1	1C

Date: Wednesday, April 08, 2020 Sheet 24 of 49



Quanta Computer Inc.

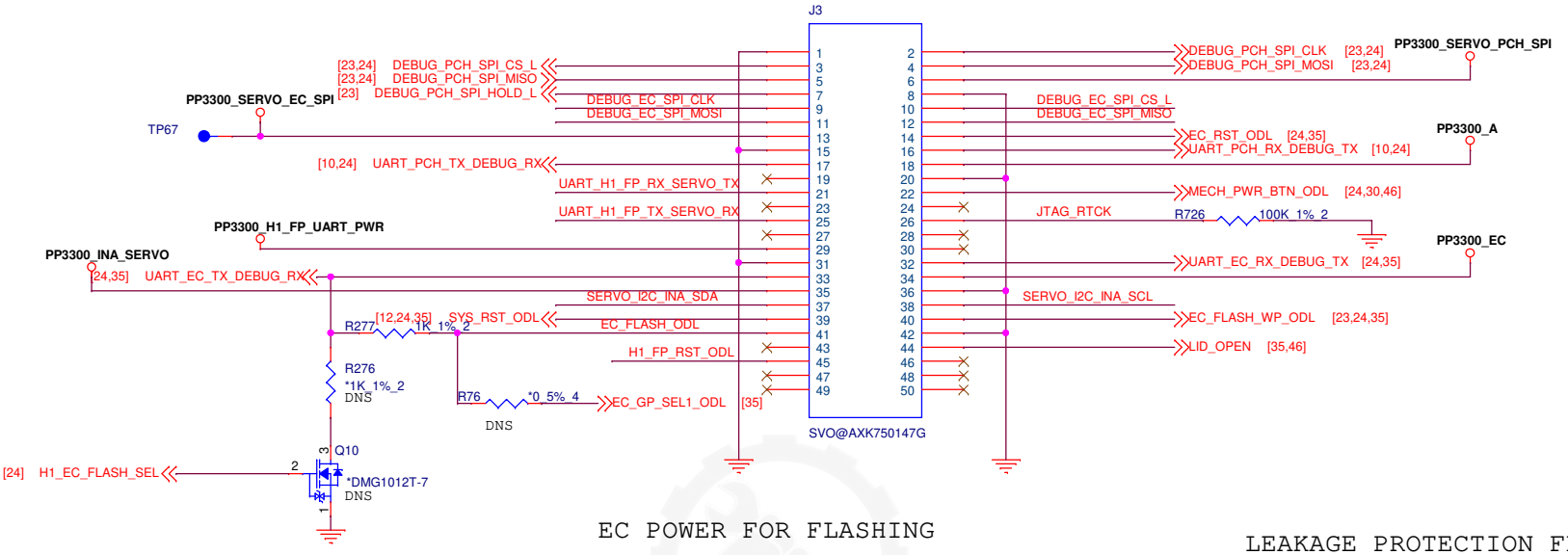
PROJECT : ZAR

Size	Document Number	Rev
	XDP DEBUG HEADER	1C

Date: Wednesday, April 08, 2020 Sheet 25 of 49

[35] KSI_04_EC_SPI_FLASH_CLK — R221 33_1%_2 — DEBUG_EC_SPI_CLK
[35] KSI_00_EC_SPI_FLASH_MOSI — R222 33_1%_2 — DEBUG_EC_SPI_MOSI
[35] KSI_05_EC_SPI_FLASH_MISO — R223 *Short_0201 — DEBUG_EC_SPI_MISO
[35] KSI_01_EC_SPI_FLASH_CS_L — R224 33_1%_2 — DEBUG_EC_SPI_CS_L

SERVO HEADER

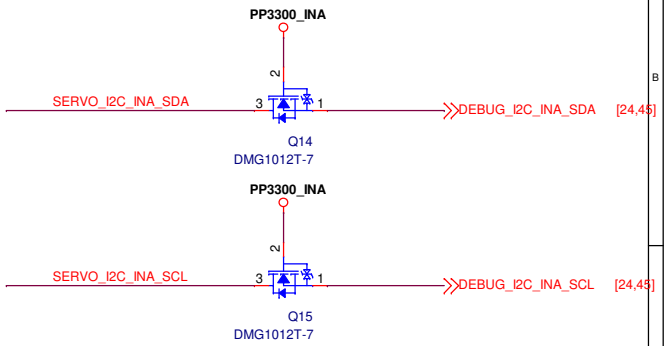


EC POWER FOR FLASHING

[24] UART_H1_TX_SERVO_RX — R744 *Short_0402 — UART_H1_FP_TX_SERVO_RX
[24] UART_H1_RX_SERVO_TX — R746 *Short_0402 — UART_H1_FP_RX_SERVO_TX
[24] H1_RST_ODL — R748 *Short_0402 — H1_FP_RST_ODL

PP3300_H1_G — R225 *Short_0402 — PP3300_H1_FP_UART_PWR

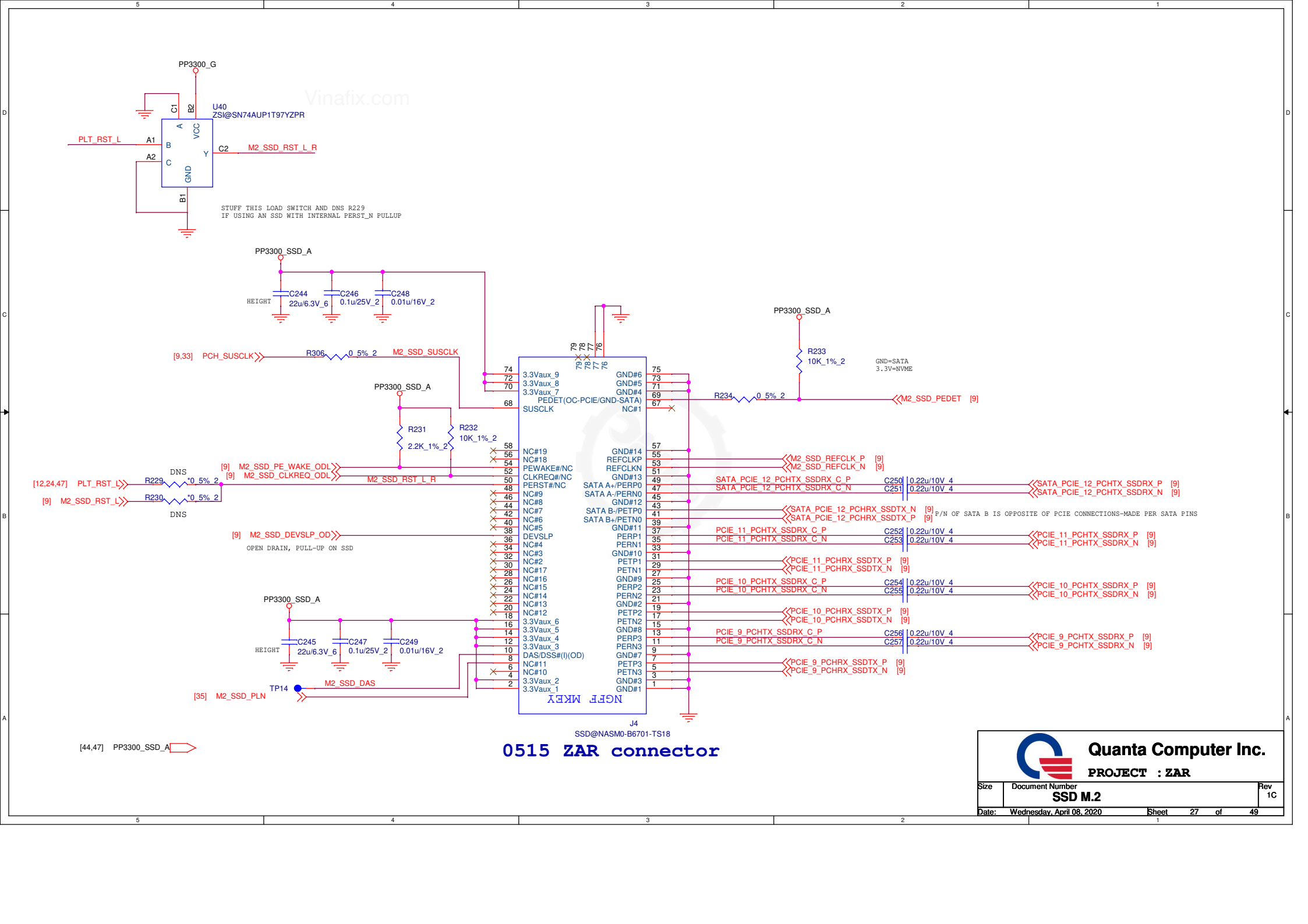
LEAKAGE PROTECTION FROM SERVO



[7,11,23,24,25,29,32,33,35,38,39,40,41,42,43,44,45] PP3300_A
[23,35,44,45,46] PP3300_EC
[27,29,35,39,44,45,46] PP3300_G
[23,24,30,38,44,45] PP3300_H1_G
[45] PP3300_INA
[45] PP3300_INA_SERVO
[23] PP3300_SERVO_PCH_SPI
[30,32,38,39,40,41,42,43] PPVAR_SYS

Quanta Computer Inc.
PROJECT : ZAR

Size	Document Number	Rev
	SERVO DEBUG	1C
Date: Wednesday, April 08, 2020	Sheet 26 of 49	


PP3300_G
U40
ZSI@SN74AUP1T97YZPR
PLT_RST_L
M2_SSD_RST_L_R
STUFF THIS LOAD SWITCH AND DNS R229
IF USING AN SSD WITH INTERNAL PERST_N PULLUP
PP3300_SSD_A
C244 22u/6.3V_6
C246 0.1u/25V_2
C248 0.01u/16V_2
HEIGHT
[9,33] PCH_SUSCLK
R306 0_5%_2
M2_SSD_SUSCLK
R231 2.2K_1%_2
R232 10K_1%_2
R233 10K_1%_2
GND=SATA
3.3V=NVME
R234 0_5%_2
M2_SSD_PEDET [9]
M2_SSD_REFCLK_P [9]
M2_SSD_REFCLK_N [9]
[9] M2_SSD_PE_WAKE_ODL
[9] M2_SSD_CLKREQ_ODL
M2_SSD_RST_L_R
DNS
[12,24,47] PLT_RST_L
R229 *0_5%_2
[9] M2_SSD_RST_L
R230 *0_5%_2
[9] M2_SSD_DEVSLP_OD
OPEN DRAIN, PULL-UP ON SSD
C245 22u/6.3V_6
C247 0.1u/25V_2
C249 0.01u/16V_2
TP14
M2_SSD_DAS
[35] M2_SSD_PLN
3.3Vaux_9
3.3Vaux_8
3.3Vaux_7
PEDET(OC-PCIE/GND-SATA)
SUSCLK
NC#19
NC#18
PEWAKE#/NC
CLKREQ#/NC
PERST#/NC
NC#9
NC#8
NC#7
NC#6
NC#5
DEVSLP
NC#4
NC#3
NC#2
NC#17
NC#16
NC#15
NC#14
NC#13
NC#12
3.3Vaux_6
3.3Vaux_5
3.3Vaux_4
3.3Vaux_3
DAS/DSS#(I)(OD)
NC#11
NC#10
3.3Vaux_2
3.3Vaux_1
GND#6
GND#5
GND#4
NC#1
GND#14
REFCLKP
REFCLKN
GND#13
SATA A+/PERP0
SATA A-/PERN0
GND#12
SATA B-/PETP0
SATA B+/PETN0
GND#11
PERP1
PERN1
GND#10
PETP1
PETN1
GND#9
PERP2
PERN2
GND#2
PETP2
PETN2
GND#8
PERP3
PERN3
GND#7
PETP3
PETN3
GND#3
GND#1
NGFF MKEY
J4
SSD@NASM0-B6701-TS18
SATA_PCIE_12_PCHTX_SSDRX_C_P
SATA_PCIE_12_PCHTX_SSDRX_C_N
C250 0.22u/10V_4
C251 0.22u/10V_4
SATA_PCIE_12_PCHTX_SSDRX_P [9]
SATA_PCIE_12_PCHTX_SSDRX_N [9]
SATA_PCIE_12_PCHRX_SSDTX_N [9]
SATA_PCIE_12_PCHRX_SSDTX_P [9]
P/N OF SATA B IS OPPOSITE OF PCIE CONNECTIONS-MADE PER SATA PINS
PCIE_11_PCHTX_SSDRX_C_P
PCIE_11_PCHTX_SSDRX_C_N
C252 0.22u/10V_4
C253 0.22u/10V_4
PCIE_11_PCHTX_SSDRX_P [9]
PCIE_11_PCHTX_SSDRX_N [9]
PCIE_11_PCHRX_SSDTX_P [9]
PCIE_11_PCHRX_SSDTX_N [9]
PCIE_10_PCHTX_SSDRX_C_P
PCIE_10_PCHTX_SSDRX_C_N
C254 0.22u/10V_4
C255 0.22u/10V_4
PCIE_10_PCHTX_SSDRX_P [9]
PCIE_10_PCHTX_SSDRX_N [9]
PCIE_10_PCHRX_SSDTX_P [9]
PCIE_10_PCHRX_SSDTX_N [9]
PCIE_9_PCHTX_SSDRX_C_P
PCIE_9_PCHTX_SSDRX_C_N
C256 0.22u/10V_4
C257 0.22u/10V_4
PCIE_9_PCHTX_SSDRX_P [9]
PCIE_9_PCHTX_SSDRX_N [9]
PCIE_9_PCHRX_SSDTX_P [9]
PCIE_9_PCHRX_SSDTX_N [9]
[44,47] PP3300_SSD_A
0515 ZAR connector
Quanta Computer Inc.
PROJECT : ZAR
Size
Document Number
SSD M.2
Rev
1C
Date: Wednesday, April 08, 2020
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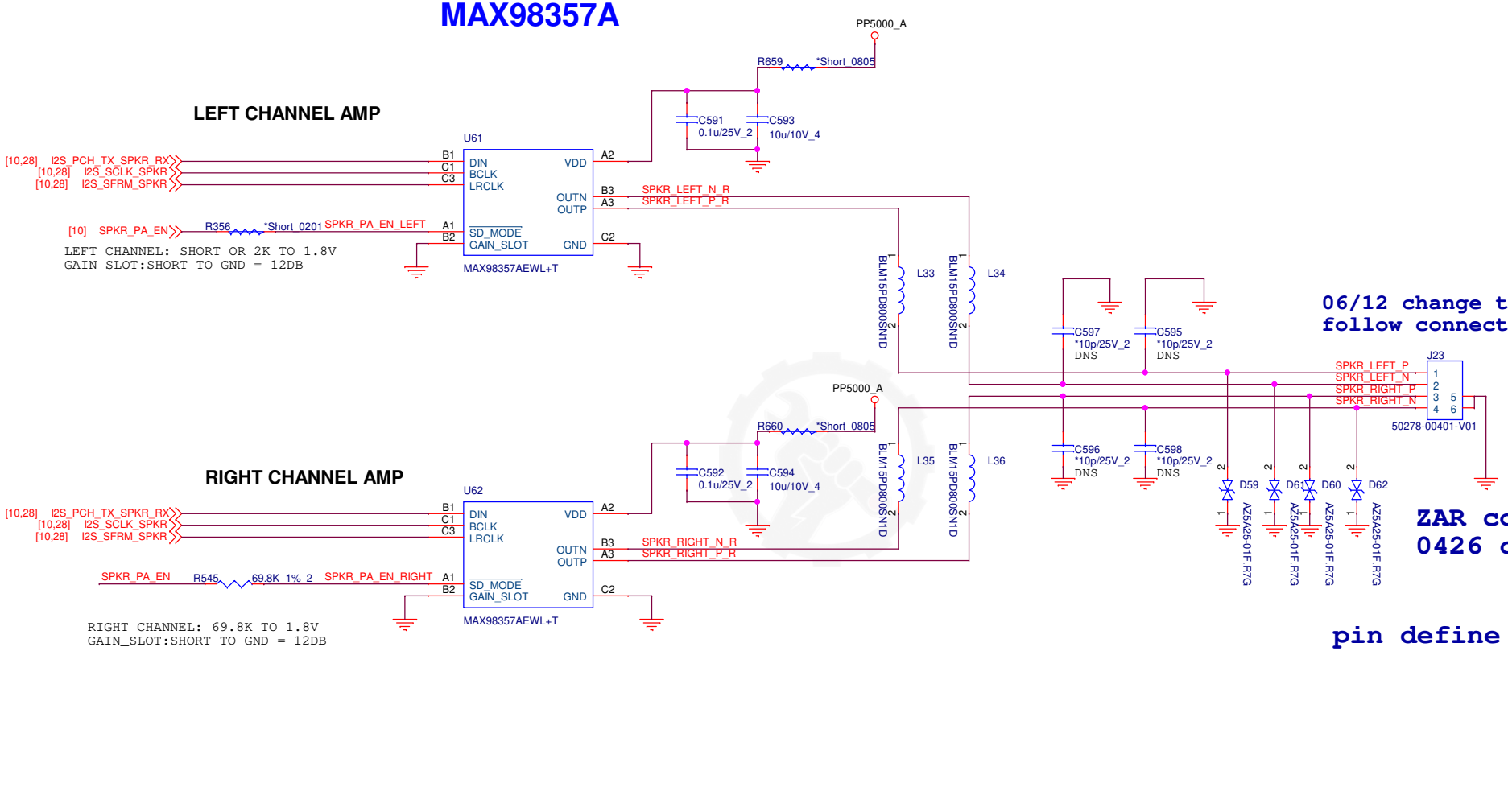
MAX98357A



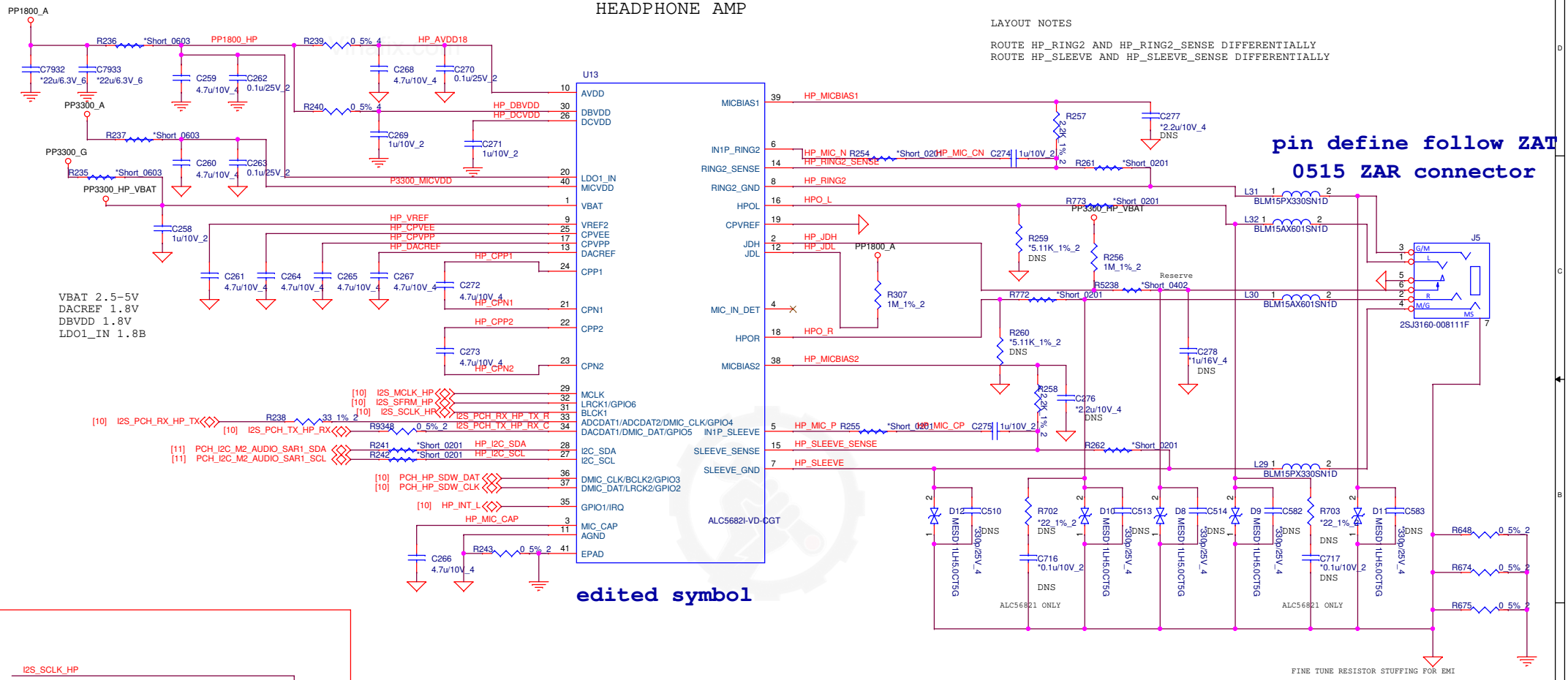
Quanta Computer Inc.		
PROJECT : ZAR		
Size	Document Number: AUDIO SPEAER AMPS	Rev: 1C
Date: Wednesday, April 08, 2020	Sheet 28 of 49	

VBAT ON EC RAIL TO REDUCE 60HZ
POWERED SPEAKER NOISE
OTHER POWER ON SOC RAILS TO PREVENT LEAKEGE

HEADPHONE AMP

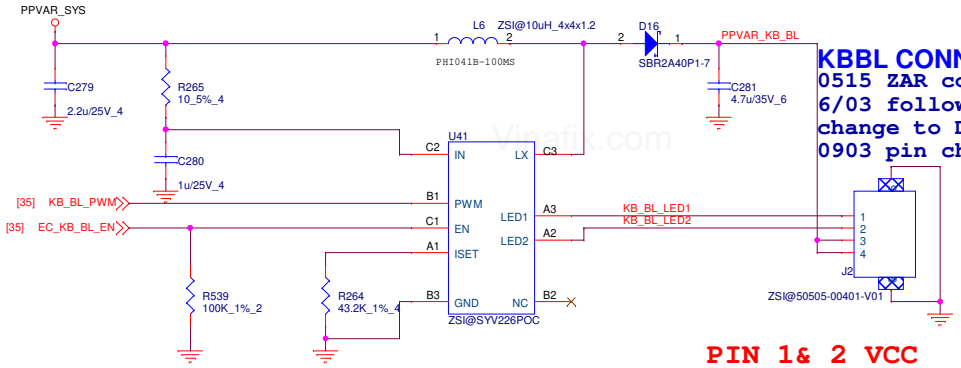
LAYOUT NOTES

ROUTE HP_RING2 AND HP_RING2_SENSE DIFFERENTIALLY
ROUTE HP_SLEEVE AND HP_SLEEVE_SENSE DIFFERENTIALLY

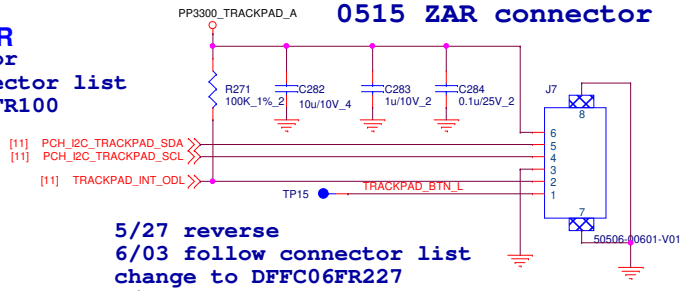


[10,11,14,32,33,39,41,44,45,47] PP1800_A
[7,11,23,24,25,26,32,33,35,38,39,40,41,42,43,44,45] PP3300_A
[27,35,39,44,45,46] PP3300_G

Quanta Computer Inc.			
PROJECT : ZAR			
Size	Document Number		Rev
	AUDIO HEADPHONE AMP		1C
Date: Wednesday, April 08, 2020		Sheet 29 of 49	



KBBL CONNECTOR
0515 ZAR connector
6/03 follow connector list
change to DFFC04FR100
0903 pin changed



TRACKPAD CONNECTOR
0515 ZAR connector

5/27 reverse
6/03 follow connector list
change to DFFC06FR227
6/17 follow connector list
change to DFFC06FR050

4.4 Pin Assignment

Pin Assignment and Description

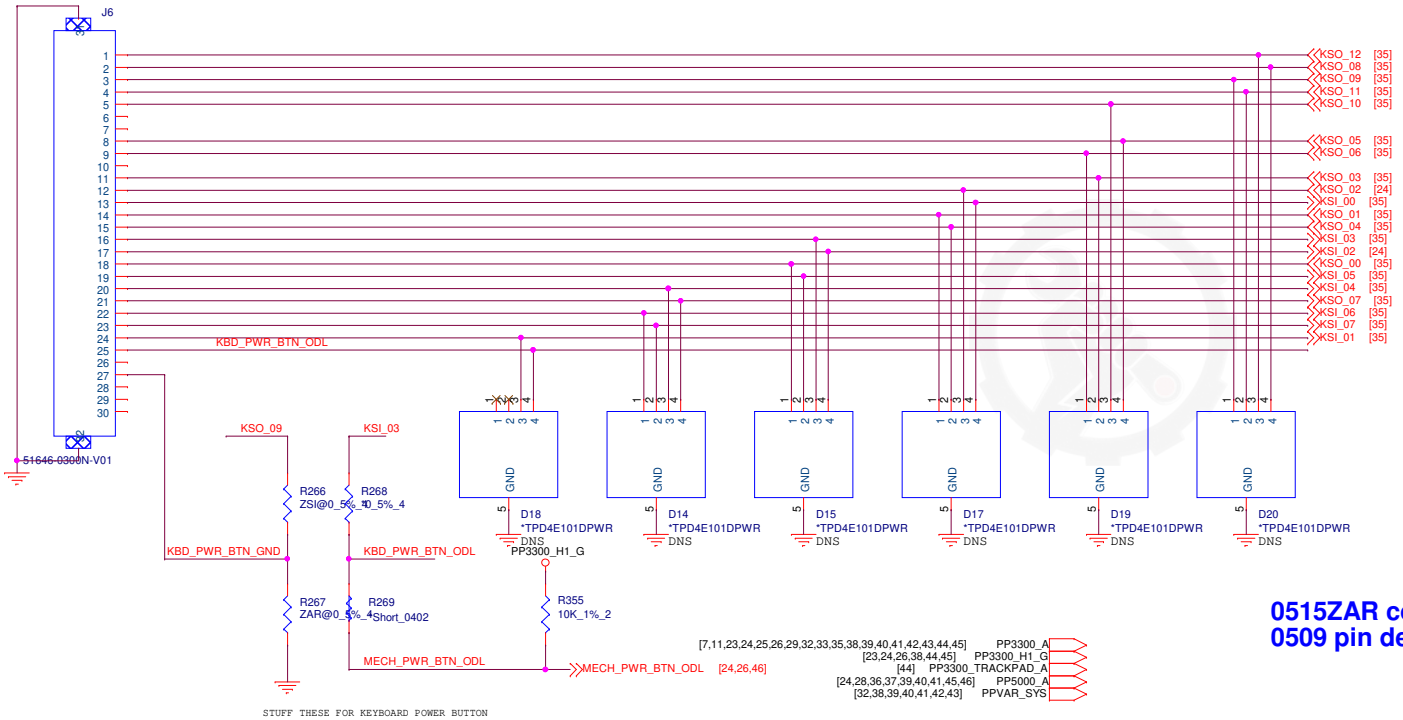
Pin#	Signal	I/O	Description
1	NC		Not connected
2	/INT	O	Slave interrupt, low active Indicates touchpad likes to send data to system (host) when low.
3	GND	GND	Ground
4	I^2C_CLK	I/O	I^2C clock I_{Drive} or I_{Sink}: 8 mA max.
5	I^2C_DATA	I/O	I^2C data. I_{Drive} or I_{Sink}: 8 mA max.
6	VDD_3.3V	Power	3.3V +/-5%. Power ripple: 100 mVpp max. Power sequence: See section 4.6.

pin define follow 0509 AVL ADLB577C009

LED = (1.229V * 1030)/R_ISET(43.2K) = 29.3mA
FSW = 1MHZ
ZSA = 29.127mA

PIN 1& 2 VCC
connector is under contact

5/27 reverse



STUFF THESE FOR KEYBOARD POWER BUTTON

KEYBOARD CONNECTOR

1030 follow connector list, change to DFFC30FR199
0603 follow connector list, change to DFFC30FR165
0515 ZAR connector
0509 pin define follow ZSA
0426 change P/N

0515ZAR connector
0509 pin define follow ZSA

	16"
1	KSO12
2	KSO8
3	KSO9
4	KSO11
5	KSO10
6	NC
7	NC
8	KSO5
9	KSO6
10	NC
11	KSO3
12	KSO2
13	KSI0
14	KSO1
15	KSO4
16	KSI3
17	KSI2
18	KSO0
19	KSI5
20	KSI4
21	KSO7
22	KSI6
23	KSI7
24	KSI1
25	POWER_DET
26	NC
27	GND
28	NC
29	NC
30	NC

12" AD1G_C80B

Mem-PIN	Define
1	KSO12
2	KSO8
3	KSO9
4	KSO11
5	KSO 0
6	N.C
7	N.C
8	KSO5
9	KSO6
10	N.C
11	KSO3
12	KSO2
13	KSI0
14	KSO1
15	KSO4
16	KSI3
17	KSI2
18	KSO0
19	KSI5
20	KSI4
21	KSO7
22	KSI6
23	KS I
24	KSI1
25	N.C
26	N.C
27	N.C
28	N.C
29	N.C
30	N.C

13" AL1G_C18BWL

Quanta Computer Inc.
PROJECT : ZAR

Size	Document Number	Rev
	KB/TP/FAN	1C

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Quanta Computer Inc.

PROJECT : ZAR

Size	Document Number	Rev
	FINGER PRINT SENSOR(none)	1C

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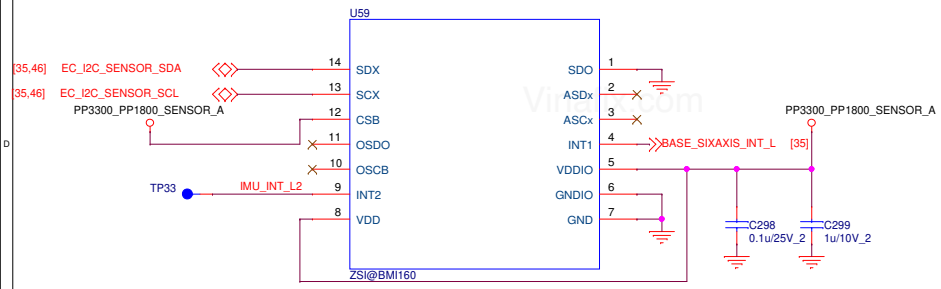
6 AXIS IMU (MLB)

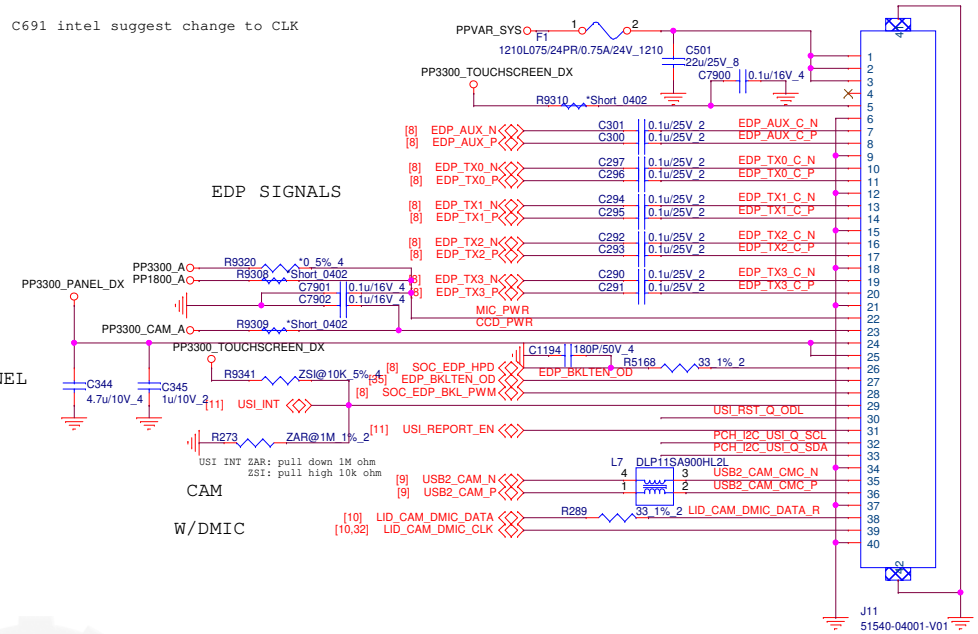


8 BIT ADDRESS: 0XD0

STUFF FOR DMIC TUNING

C691 intel suggest change to CLK

EDP SIGNALS

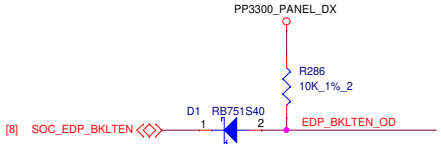


USI TOUCH PANEL

CAM

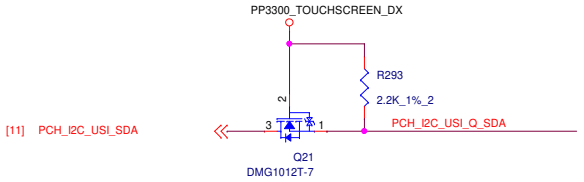
W/DMIC

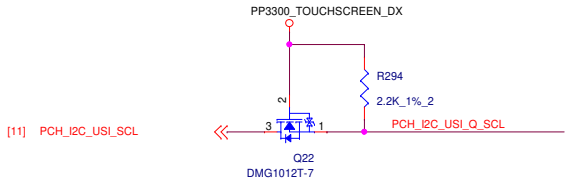
BACKLIGHT ENABLE CONTROL

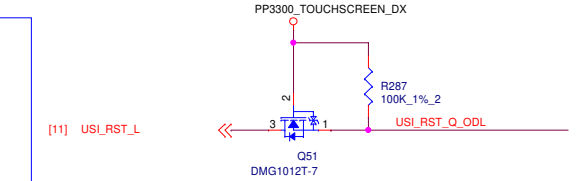


RESERVE GMR

0515 ZAR connector pin define follow ZSA

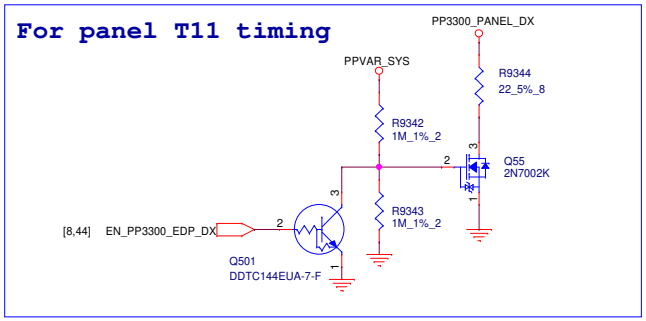






[7,11,23,24,25,26,29,33,35,38,39,40,41,42,43,44,45] PP3300_A
[10,11,14,29,33,39,41,44,45,47] PP1800_A
[44] PP3300_CAM_A
[44,45] PP3300_PANEL_DX
[30,38,39,40,41,42,43] PPVAR_SYS

For panel T11 timing



Quanta Computer Inc.		
PROJECT : ZAR		
Size	Document Number: LID, EDP, CAM, TOUCH, PEN	Rev: 1C
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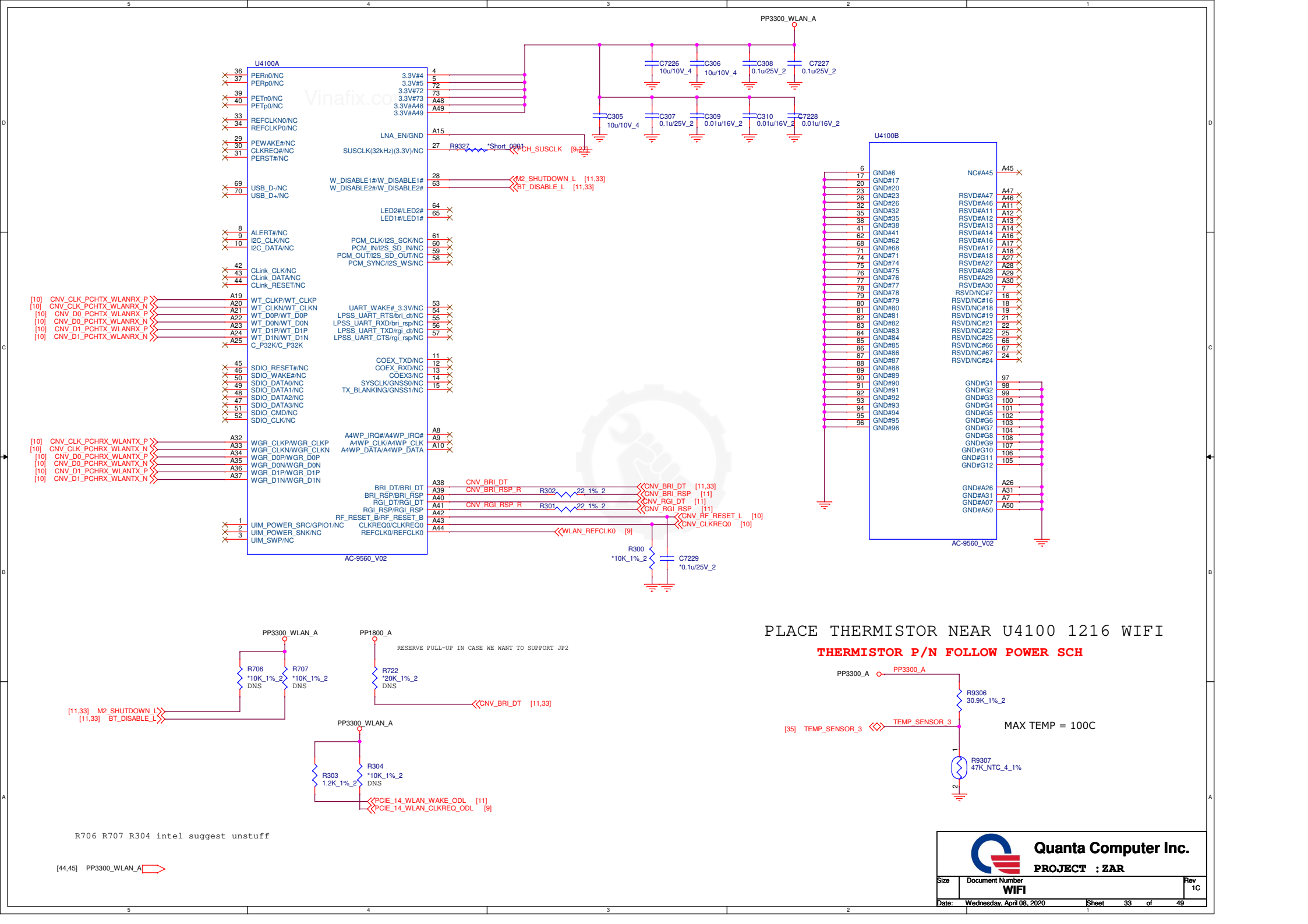
PP3300_WLAN_A
U4100A
C7226 10u/10V_4
C306 10u/10V_4
C308 0.1u/25V_2
C7227 0.1u/25V_2
C305 10u/10V_4
C307 0.1u/25V_2
C309 0.01u/16V_2
C310 0.01u/16V_2
C7228 0.01u/16V_2
R9327 *Short_0201
PCH_SUSCLK [9,27]
M2_SHUTDOWN_L [11,33]
BT_DISABLE_L [11,33]
U4100B
AC-9560_V02
CNV_BRI_DT
CNV_BRI_RSP_R
R302 22_1%_2
CNV_RGI_RSP_R
R301 22_1%_2
CNV_BRI_DT [11,33]
CNV_BRI_RSP [11]
CNV_RGI_DT [11]
CNV_RGI_RSP [11]
CNV_RF_RESET_L [10]
CNV_CLKREQ0 [10]
WLAN_REFCLK0 [9]
R300 *10K_1%_2
C7229 *0.1u/25V_2
PP3300_WLAN_A
PP1800_A
RESERVE PULL-UP IN CASE WE WANT TO SUPPORT JP2
R706 *10K_1%_2 DNS
R707 *10K_1%_2 DNS
R722 *20K_1%_2 DNS
[11,33] M2_SHUTDOWN_L
[11,33] BT_DISABLE_L
CNV_BRI_DT [11,33]
PP3300_WLAN_A
R303 1.2K_1%_2
R304 *10K_1%_2 DNS
PCIE_14_WLAN_WAKE_ODL [11]
PCIE_14_WLAN_CLKREQ_ODL [9]
PLACE THERMISTOR NEAR U4100 1216 WIFI
THERMISTOR P/N FOLLOW POWER SCH
PP3300_A
PP3300_A
R9306 30.9K_1%_2
[35] TEMP_SENSOR_3
TEMP_SENSOR_3
MAX TEMP = 100C
R9307 47K_NTC_4_1%
R706 R707 R304 intel suggest unstuff
[44,45] PP3300_WLAN_A
Quanta Computer Inc.
PROJECT : ZAR
Size
Document Number
WIFI
Rev
1C
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Quanta Computer Inc.			
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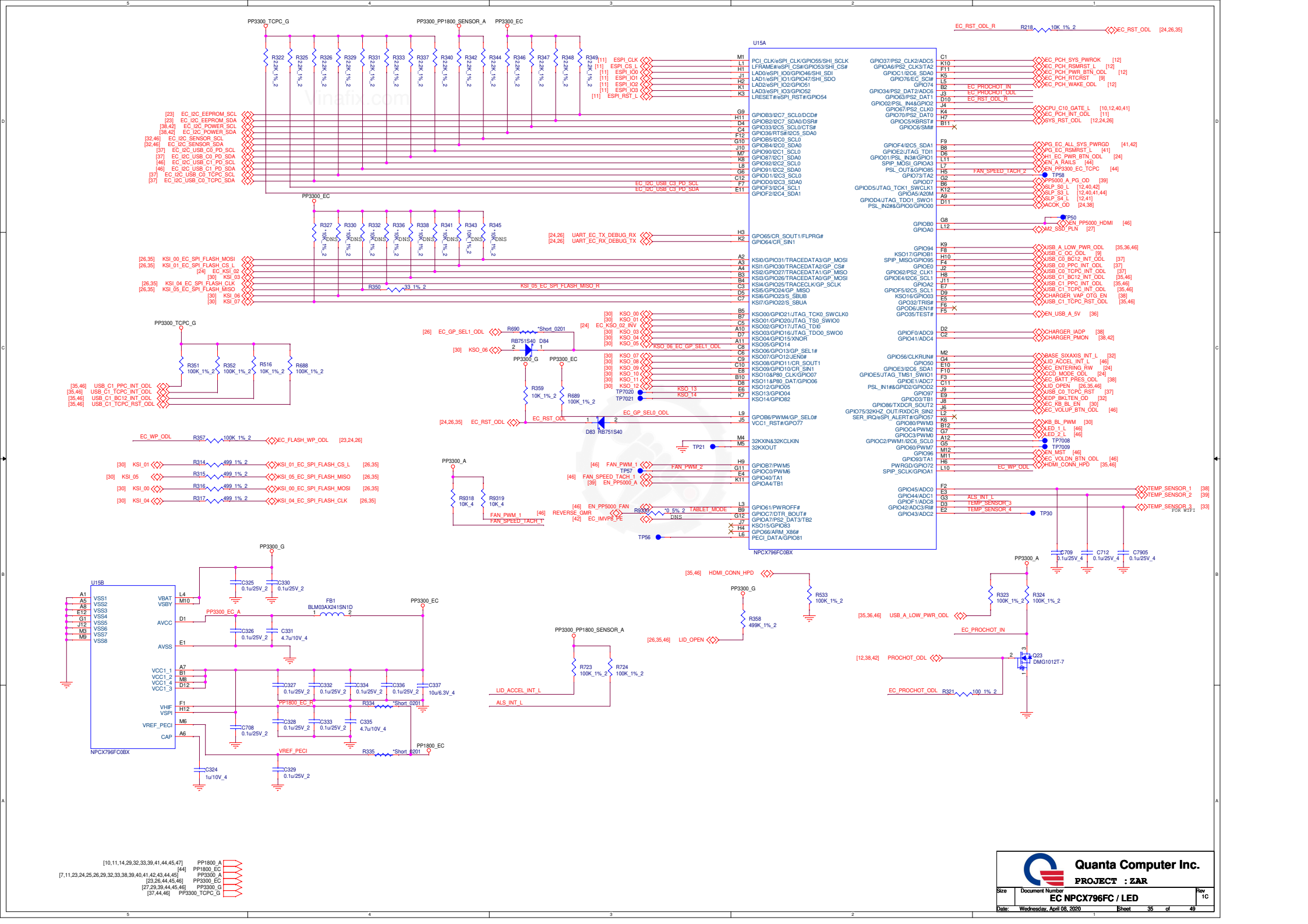
PP3300_TCPC_G
PP3300_PP1800_SENSOR_A
PP3300_EC
U15A
NPCX796FC0BX
EC_RST_ODL_R
R218
10K_1%_2
EC_RST_ODL
[24,26,35]
ESPI_CLK
ESPI_CS_L
ESPI_IO0
ESPI_IO1
ESPI_IO2
ESPI_IO3
ESPI_RST_L
PCI_CLK/eSPI_CLK/GPIO55/SHI_SCLK
LFRAME#/eSPI_CS#/GPIO53/SHI_CS#
LAD0/eSPI_IO0/GPIO46/SHI_SDI
LAD1/eSPI_IO1/GPIO47/SHI_SDO
LAD2/eSPI_IO2/GPIO51
LAD3/eSPI_IO3/GPIO52
LRESET#/eSPI_RST#/GPIO54
GPIO37/PS2_CLK2/ADC5
GPIO6A/PS2_CLK3/TA2
GPIOC1/I2C6_SDA0
GPIO76/EC_SCI#
GPIO74
GPIO34/PS2_DAT2/ADC6
GPIO63/PS2_DAT1
GPIO02/PSL_IN4&GPIO2
GPIO67/PS2_CLK0
GPIO70/PS2_DAT0
GPIOC5/KBRST#
GPIO6C/SMI#
EC_PCH_SYS_PWROK
EC_PCH_RSMRST_L
EC_PCH_PWR_BTN_ODL
EC_PCH_RTCRST
EC_PCH_WAKE_ODL
EC_PROCHOT_IN
EC_PROCHOT_ODL
EC_RST_ODL_R
CPU_C10_GATE_L
EC_PCH_INT_ODL
SYS_RST_ODL
GPIOF4/I2C5_SDA1
GPIOE2/JTAG_TDI1
GPIO01/PSL_IN3#/GPIO1
SPIP_MOSI_GPIOA3
PSL_OUT&GPIO85
GPIO73/TA2
GPIOD7
GPIOD5/JTAG_TCK1_SWCLK1
GPIOA5/A20M
GPIOD4/JTAG_TDO1_SWO1
PSL_IN2#&GPIO0/GPIO00
PG_EC_ALL_SYS_PWRGD
PG_EC_RSMRST_L
PH1_EC_PWR_BTN_ODL
EN_A_RAILS
EN_PP3300_EC_TCPC
FAN_SPEED_TACH_2
TP58
PP5000_A_PG_OD
SLP_S0_L
SLP_S3_L
SLP_S4_L
ACOK_OD
P50
EN_PP5000_HDMI
M2_SSD_PLN
GPIOB0
GPIOA0
GPIO94
KSO17/GPIOB1
SPIP_MISO/GPIO96
GPIOE0
GPIO62/PS2_CLK1
GPIOE4/I2C6_SCL1
GPIO5/I2C5_SCL1
KSO16/GPIO03
GPO32/TRIS#
GPIOD6/JEN1#
GPO35/TEST#
USB_A_LOW_PWR_ODL
USB_C_OC_ODL
USB_C0_BC12_INT_ODL
USB_C0_PPC_INT_ODL
USB_C0_TCPC_INT_ODL
USB_C1_BC12_INT_ODL
USB_C1_PPC_INT_ODL
USB_C1_TCPC_INT_ODL
CHARGER_VAP_OTG_EN
USB_C1_TCPC_RST_ODL
EN_USB_A_5V
GPIOF0/ADC9
GPIOA1/ADC4
CHARGER_IADP
CHARGER_PMON
GPIO56/CLKRUN#
GPIO50
GPIOE3/I2C6_SDA1
GPIOE5/JTAG_TMS1_SWIO1
GPIOE1/ADC7
PSL_IN1#&GPIO2/GPIOD2
GPIO97
GPIOD3/TB1
GPIO86/TXDCR_SOUT2
GPIO75/32KHZ_OUT/RXDCR_SIN2
SER_IRQ/eSPI_ALERT#/GPIO57
GPIO80/PWM3
GPIOC4/PWM2
GPIOC3/PWM1
GPIOC2/PWM1/I2C6_SCL0
GPIO60/PWM7
GPIO96
GPIO93/TA1
PWRGD/GPIO72
SPIP_SCLK/GPIOA1
BASE_SIXAXIS_INT_L
LID_ACCEL_INT_L
EC_ENTERING_RW
VCCD_MODE_ODL
EC_BATT_PRES_ODL
LID_OPEN
USB_C0_TCPC_RST
EDP_BKLTEN_OD
EC_KB_BL_EN
EC_VOLUP_BTN_ODL
KB_BL_PWM
LED_1_L
LED_2_L
TP7008
TP7009
EN_MST
EC_VOLDN_BTN_ODL
HDMI_CONN_HPD
EC_WP_ODL
GPIO45/ADC0
GPIO44/ADC1
GPIOF1/ADC8
GPIO42/ADC3/RI#
GPIO43/ADC2
TEMP_SENSOR_1
TEMP_SENSOR_2
TEMP_SENSOR_3
TEMP_SENSOR_4
TP30
FOR WIFI
GPIOE6/PWM4/GP_SEL0#
VCC1_RST#/GPO77
32KXIN&32KCLKIN
32KXOUT
TP21
GPIOB7/PWM5
GPIOC0/PWM6
GPIO40/TA1
GPIOA4/TB1
FAN_PWM_1
FAN_PWM_2
FAN_SPEED_TACH_1
EN_PP5000_A
GPIO61/PWROFF#
GPIOC7/DTR_BOUT#
GPIOA7/PS2_DAT3/TB2
KSO15/GPIO83
GPO66/ARM_X86#
PECI_DATA/GPIO81
EN_PP5000_FAN
TABLET_MODE
REVERSE_GMR
EC_IMVP8_PE
TP56
KSI0/GPIO31/TRACEDATA3/GP_MOSI
KSI1/GPIO30/TRACEDATA2/GP_CS#
KSI2/GPIO27/TRACEDATA1/GP_MISO
KSI3/GPIO26/TRACEDATA0/GP_MOSI
KSI4/GPIO25/TRACECLK/GP_SCLK
KSI5/GPIO24/GP_MISO
KSI6/GPIO23/S_SBUB
KSI7/GPIO22/S_SBUA
KSO00/GPIO21/JTAG_TCK0_SWCLK0
KSO01/GPIO20/JTAG_TS0_SWIO0
KSO02/GPIO17/JTAG_TDI0
KSO03/GPIO16/JTAG_TDO0_SWO0
KSO04/GPIO15/XNOR
KSO05/GPIO14
KSO06/GPIO13/GP_SEL1#
KSO07/GPIO12/JEN0#
KSO08/GPIO11/CR_SOUT1
KSO09/GPIO10/CR_SIN1
KSO10&P80_CLK/GPIO07
KSO11&P80_DAT/GPIO06
KSO12/GPIO05
KSO13/GPIO04
KSO14/GPIO82
KSO_13
KSO_14
KSO_06_EC_GP_SEL1_ODL
EC_GP_SEL0_ODL
UART_EC_TX_DEBUG_RX
UART_EC_RX_DEBUG_TX
GPIO65/CR_SOUT1/FLPRG#
GPIO64/CR_SIN1
EC_I2C_USB_C3_PD_SCL
EC_I2C_USB_C3_PD_SDA
EC_I2C_EEPROM_SCL
EC_I2C_EEPROM_SDA
EC_I2C_POWER_SCL
EC_I2C_POWER_SDA
EC_I2C_SENSOR_SCL
EC_I2C_SENSOR_SDA
EC_I2C_USB_C0_PD_SCL
EC_I2C_USB_C0_PD_SDA
EC_I2C_USB_C1_PD_SCL
EC_I2C_USB_C1_PD_SDA
EC_I2C_USB_C0_TCPC_SCL
EC_I2C_USB_C0_TCPC_SDA
KSI_00_EC_SPI_FLASH_MOSI
KSI_01_EC_SPI_FLASH_CS_L
KSI_02
KSI_03
KSI_04_EC_SPI_FLASH_CLK
KSI_05_EC_SPI_FLASH_MISO
KSI_06
KSI_07
KSI_05_EC_SPI_FLASH_MISO_R
R350
33_1%_2
KSO_00
KSO_01
KSO_02_INV
KSO_03
KSO_04
KSO_05
KSO_06
KSO_07
KSO_08
KSO_09
KSO_10
KSO_11
KSO_12
EC_GP_SEL1_ODL
R690
*Short_0201
RB751S40_D84
R359
10K_1%_2
R689
100K_1%_2
TP7020
TP7021
EC_RST_ODL
D83 RB751S40
EC_WP_ODL
R357
100K_1%_2
EC_FLASH_WP_ODL
[23,24,26]
KSI_01_EC_SPI_FLASH_CS_L
KSI_05_EC_SPI_FLASH_MISO
KSI_00_EC_SPI_FLASH_MOSI
KSI_04_EC_SPI_FLASH_CLK
R314
R315
R316
R317
499_1%_2
R9318
10K_4
R9319
10K_4
R9330
*0_5%_2
DNS
FAN_PWM_1
FAN_SPEED_TACH_1
R351
100K_1%_2
R352
100K_1%_2
R516
10K_1%_2
R688
100K_1%_2
USB_C1_PPC_INT_ODL
USB_C1_TCPC_INT_ODL
USB_C1_BC12_INT_ODL
USB_C1_TCPC_RST_ODL
R327
R330
R332
R336
R338
R341
R343
R345
10K_1%_2
DNS
R533
100K_1%_2
R358
499K_1%_2
LID_OPEN
R323
R324
100K_1%_2
USB_A_LOW_PWR_ODL
EC_PROCHOT_IN
PROCHOT_ODL
Q23
DMG1012T-7
EC_PROCHOT_ODL
R321
100_1%_2
R723
R724
100K_1%_2
LID_ACCEL_INT_L
ALS_INT_L
C709
C712
C7905
0.1u/25V_4
U15B
NPCX796FC0BX
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VBAT
VSBY
AVCC
AVSS
VCC1_1
VCC1_2
VCC1_4
VCC1_3
VHIF
VSPI
VREF_PECI
CAP
FB1
BLM03AX241SN1D
PP3300_EC_A
PP1800_EC_R
VREF_PECI
C325
C330
C326
C331
4.7u/10V_4
C327
C332
C334
C336
C337
10u/6.3V_4
C328
C333
C335
C708
C324
1u/10V_4
C329
R334
R335
*Short_0201
[10,11,14,29,32,33,39,41,44,45,47] PP1800_A
[44] PP1800_EC
[7,11,23,24,25,26,29,32,33,38,39,40,41,42,43,44,45] PP3300_A
[23,26,44,45,46] PP3300_EG
[27,29,39,44,45,46] PP3300_G
[37,44,46] PP3300_TCPC_G
Quanta Computer Inc.
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TYPE-A: PORT 0

0527
follow connector list

PP5000_A

PP5000_USB_A0_VBUS

U16
SLGC55545VTR

C338 22u/10V_6

R361 100K_1%_2

[9] USB2_A0_N
[9] USB2_A0_P

USB2_A0_U_N
USB2_A0_U_P

[35] EN_USB_A_5V

USB_A0_ILIM_SEL

USB_A0_ILIM_LO
USB_A0_ILIM_HI

[35,46] USB_A_LOW_PWR_ODL

Q24 PJA138K

R362 48.7K_1%_2

R363 29.4K_1%_2

USB_A0_STATUS_L [46]

USB_A_OC_ODL [9]

IF USING TPS2546, R362=51.1K, R363=30.9K
LO LIMIT: 912-1055 MA
HI LIMIT: 1516-1737MA

[9] USB3_A0_RX_N
[9] USB3_A0_RX_P

L4 NFP0QHB542HS2D

L3 NFP0QHB542HS2D

L5 NFP0QHB542HS2D

C340 0.22u/10V_2
C339 0.22u/10V_2

[9] USB3_A0_TX_N
[9] USB3_A0_TX_P

C343 150u/6.3V_3528H1.9

CN1
2UB4024-002111F

0827 modify SMT footprint

D28
AZ1043-04F.R7G

D89 PESD5V0H1BSF
D90 PESD5V0H1BSF

MICRO SD CARD
*IF NOT ON MLB, USB TO SD INTERFACE MUST BE USED

PP3300_SD_DX

C341 4.7u/10V_4

C342 0.1u/25V_2

0527 follow connector list

J16 158-1000902625

[10] SD_DATA3
[10] SD_CMD
[10] SD_CLK
[10] SD_DATA0
[10] SD_DATA1
[10] SD_DATA2
[10] SD_CD_ODL

R367 22_1%_2
R368 22_1%_2
R635 *Short_0201
R364 22_1%_2
R365 22_1%_2
R366 22_1%_2
R5237 *Short_0201

SD_DATA3_R
SD_CMD_R
SD_CLK_R
SD_DATA0_R
SD_DATA1_R
SD_DATA2_R

Reserve for NC or NO

D25 D26 D27 D22 D23 D24 D63
TPD1E6B06DPLR

[44] PP3300_SD_DX
[24,28,37,39,40,41,45,46] PP5000_A

Quanta Computer Inc.
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PP5000_A
C358 0.1u/25V_2
C360 1u/10V_2
PP3300_TCPC_G
R373 10K_1%_2
U17
VDD
USB+
USB-
SCL
SDA
INTB
GND
NC
D+
D-
ADDR
ENB
PI5USB9201ZTAEX
[9] USB2_C0_P
[9] USB2_C0_N
USB2_C0_U_P
USB2_C0_U_N
[35] EC_I2C_USB_C0_PD_SCL
[35] EC_I2C_USB_C0_PD_SDA
BC12_C0_ADDR
BC12_C0_EN_L
[35] USB_C0_BC12_INT_ODL
R371 *Short_0201
R676 *Short_0201
ADDRESS (HEX, 8 BIT): 0XBE

PORT 0:TCPPC

CSD87501L --> MOQ 3K
CSD87501LT --> MOQ 250
CSD87501L = CSD87501LT

Q27
CSD87501L
PPVAR_VBUS_IN
PPVAR_USB_C0_VBUS
C1
C2
PP5000_A
C366 150u/6.3V_3528H1.9
U44
SN5S330RJKR
PP1_INT
PP2_SENSEP
PP2_SENSEN
PP2_GATE1
PP2_GATE2
VBUS
VBUS_IN
VIN_3V3
VANA_3V3
VDIG_1V8
PP_CABLE
CC1
CC2
SBU1
SBU2
EPAD2
EPAD1
GND#4
GND#5
GND#3
GND#2
GND#1
NC#2
NC#1
VBIAS#1
VBIAS#2
C_CC1
C_CC2
C_SBU1
C_SBU2
VDDIO
I2C_SCL
I2C_SDA
INT
ADDR_0
ADDR_1
MODE
ALT
USB_C0_CC1
USB_C0_CC2
USB_C0_SBU1
USB_C0_SBU2
USB_C0_CC1_U
USB_C0_CC2_U
USB_C0_SBU1_Q
USB_C0_SBU2_Q
TP7023
THERM_PAD1_C0
THERM PAD 1 MUST BE CONNECTED TO ISOLATED THERMAL PAD
R383 3.3_5%_4
D42 RB751S40
C367 1u/50V_6
C368 4.7u/50V_8
VANA_3V3_C0
VDIG_1V8_C0
VBIAS_C0
C369 0.1u/25V_4
C370 4.7u/10V_4
C371 10u/10V_4
C372 1u/10V_4
PP3300_TCPC_G
R385 10K_1%_2
EC_I2C_USB_C0_PD_SCL
EC_I2C_USB_C0_PD_SDA
I2C IN FAST PLUS MODE
USB_C0_PPC_INT_ODL [35]
I2C_SPEED_MODE_C0
R384 *Short_0201
ADDRESS (HEX, 8 BIT): 0X80

06/20
EMI reserve
PPVAR_USB_C0_VBUS
C7923 1000p/50V_2

PPVAR_USB_C0_VBUS
R320 348K_1%_4
VBUS_SENSE_C0
R372 49.9K_1%_2
IF TCPC IS NOT ANALOGIX, MUST STUFF
PULL-UP/PULL-DOWN RESISTORS ON
DDI1_AUX_P AND DDI_AUX_N

PP3300_TCPC_G
FB4 BLM03AX241SN1D
PP3300_TCPC_AVDD
C346 1u/10V_2
C347 0.1u/25V_2
C348 1000p/25V_2
AVDD33 SHOULD TURN ON FIRST
DVDD_IO SHOULD TURN ON WITHIN 2MS OF AVDD33
R775 0_5%_4
PP3300_TCPC_DVDD
C764 1000p/25V_2
C765 0.1u/25V_2
C766 1u/10V_2

PORT 0:TCPC

U60
ANX3447QN-A
DP_LN_0P
DP_LN_0N
DP_LN_1P
DP_LN_1N
DP_LN_2P
DP_LN_2N
DP_LN_3P
DP_LN_3N
AUXP
AUXN
SSTX_P
SSTX_N
SSRX_P
SSRX_N
HPD
ROLE_SEL
TEST_R
TEST_EN
CFG_SCL
CFG_SDA
I2C_ADR_0
I2C_ADR_1
INTP_OUT
AVDD33_1
AVDD33_2
DVDD_IO
SSTXP1
SSTXN1
SSRXP1
SSRXN1
SSTXP2
SSTXN2
SSRXP2
SSRXN2
CC1
CC2
SBU1
SBU2
SOURCE_CTRL
DISCH_CTRL
SINK_CTRL
FF0
FF1
VBUS_SENSE
VBUS_OCP
VCONN_PWR
NC_1
NC_2
EP_GND
[8] DDI1_TX0_P
[8] DDI1_TX0_N
[8] DDI1_TX1_P
[8] DDI1_TX1_N
[8] DDI1_TX2_P
[8] DDI1_TX2_N
[8] DDI1_TX3_P
[8] DDI1_TX3_N
[8] DDI1_AUX_P
[8] DDI1_AUX_N
DDI1_AUX_P_C
DDI1_AUX_N_C
C698 0.1u/25V_2
C699 0.1u/25V_2
[9] USB3_C0_TX_P
[9] USB3_C0_TX_N
[9] USB3_C0_RX_P
[9] USB3_C0_RX_N
USB3_C0_TX1_P
USB3_C0_TX1_N
USB3_C0_RX1_P
USB3_C0_RX1_N
USB3_C0_TX2_P
USB3_C0_TX2_N
USB3_C0_RX2_P
USB3_C0_RX2_N
USB_C0_CC1
USB_C0_CC2
USB_C0_SBU1
USB_C0_SBU2
TCPC_USB_C0_HPD
USB_C0_TCPC_RST
EC_I2C_USB_C0_TCPC_SCL
EC_I2C_USB_C0_TCPC_SDA
USB_C0_ADDR0
USB_C0_ADDR1
USB_C0_TCPC_INT_ODL
[35] USB_C0_TCPC_INT_ODL
R319 4.7K_1%_2
R297 4.7K_1%_2
R370 *4.7K_1%_2
R369 *4.7K_1%_2
R636 *100K_1%_2
R637 *100K_1%_2
D80 RB751S40
DNS
TP35
TP36
VBUS_SENSE_C0
R711 *0_5%_4
PP5000_A
C349 *1u/10V_2
C3 *200p/16V_2
C19 *200p/16V_2

DEFAULT I2C ADDRESSES (HEX, 8-BIT)

TCPC: 0X58
SPI: 0X7E
EMTB: 0X7A
EMRB: 0X84
DEBUG1: 0X72
DEBUG2: 0X70

ESD DIODES TO PROTECT H1
D13
GND
TPD4E101DPWR
USB_C0_CC1_U
USB_C0_CC2_U
USB_C0_SBU1_U
USB_C0_SBU2_U

USB3_C0_TX1_P C363 0.22u/10V_2
USB3_C0_TX1_N C362 0.22u/10V_2
USB3_C0_TX2_P C365 0.22u/10V_2
USB3_C0_TX2_N C364 0.22u/10V_2
L11 NFP0QHB542HS2D
L10 NFP0QHB542HS2D
L13 NFP0QHB542HS2D
L12 NFP0QHB542HS2D
L9 NFP0QHB542HS2D
USB3_C0_TX1_C_P
USB3_C0_TX1_C_N
USB3_C0_RX1_P
USB3_C0_RX1_N
USB3_C0_TX2_C_P
USB3_C0_TX2_C_N
USB3_C0_RX2_P
USB3_C0_RX2_N
USB2_C0_U_P
USB2_C0_U_N
USB3_C0_TX1_L_P
USB3_C0_TX1_L_N
USB3_C0_RX1_L_P
USB3_C0_RX1_L_N
USB3_C0_TX2_L_P
USB3_C0_TX2_L_N
USB3_C0_RX2_L_P
USB3_C0_RX2_L_N
USB2_C0_L_P
USB2_C0_L_N
[24] USB_C0_CC1_U
[24] USB_C0_CC2_U
[24] USB_C0_SBU1_U
[24] USB_C0_SBU2_U

J17
UCF3M-01N01-0P53
SSTXp1
SSTXn1
SSRXp1
SSRXn1
SSTXp2
SSTXn2
SSRXp2
SSRXn2
Dp1
Dn1
Dp2
Dn2
CC1
CC2
SBU1
SBU2
VBUS_1
VBUS_3
VBUS_2
VBUS_4
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
NC_1
NC_2
PPVAR_USB_C0_VBUS
EC2 PE3620M1Q

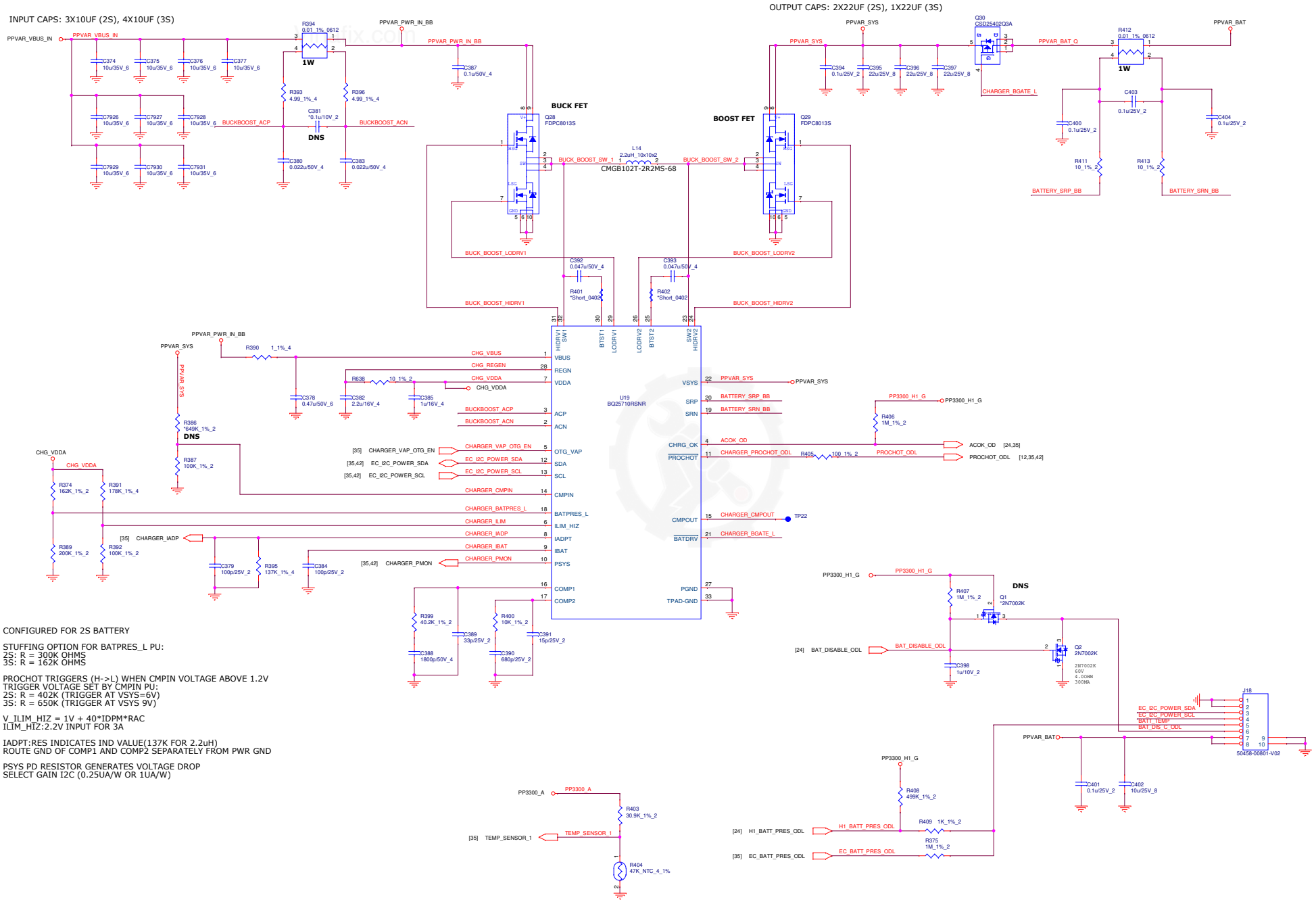
D66 PESD5V0H1BSF
D88 PESD5V0H1BSF
USB2_C0_L_N
USB2_C0_L_P

D840
AZ1043-04F.R7G
D85
AZ1043-04F.R7G
Line-1
Line-2
Line-3
Line-4
GND#1
NC#4
NC#3
NC#2
NC#1

DFHS24FR477
8/27 EVT changed

[35,44,46] PP3300_TCPC_G
[24,28,36,39,40,41,45,46] PP5000_A
[38,46] PPVAR_VBUS_IN

Quanta Computer Inc.
PROJECT : ZAR
Size
Document Number
USB C0
Rev
1C
Date: Wednesday, April 08, 2020
Sheet 37 of 49



CONFIGURED FOR 2S BATTERY

STUFFING OPTION FOR BATPRES_L PU:
2S: R = 300K OHMS
3S: R = 162K OHMS

PROCHOT TRIGGERS (H->L) WHEN CMPIN VOLTAGE ABOVE 1.2V
TRIGGER VOLTAGE SET BY CMPIN PU:
2S: R = 402K (TRIGGER AT VSYS=6V)
3S: R = 650K (TRIGGER AT VSYS 9V)

V_ILIM_HIZ = 1V + 40*IDPM*RAC
ILIM_HIZ:2.2V INPUT FOR 3A

IADPT:RES INDICATES IND VALUE(137K FOR 2.2uH)
ROUTE GND OF COMP1 AND COMP2 SEPARATELY FROM PWR GND

PSYS PD RESISTOR GENERATES VOLTAGE DROP
SELECT GAIN I2C (0.25UA/W OR 1UA/W)

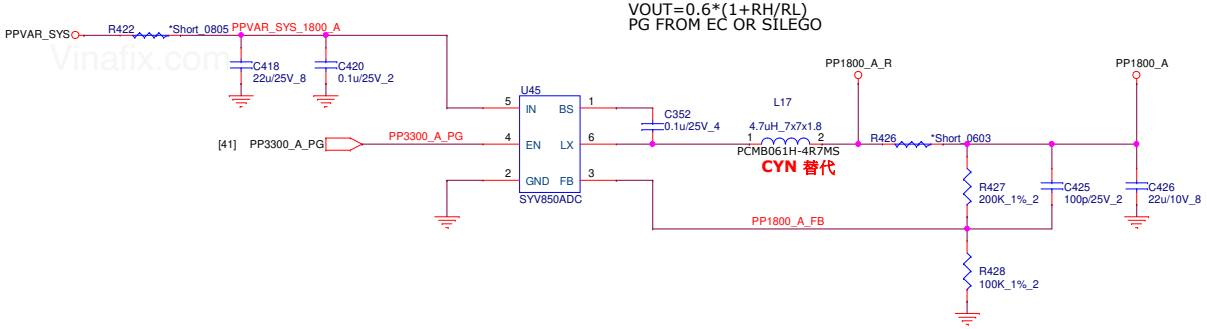
MAX TEMP = 100C
PLACE THERMISTOR NEAR CHARGING INDUCTOR

Quanta Computer Inc.	
PROJECT :	
Size	Document Number: POWER: BATTERY CHARGER — Rev: 1C
Date: Wednesday, April 08, 2020	Sheet 36 of 51

PP1800_A

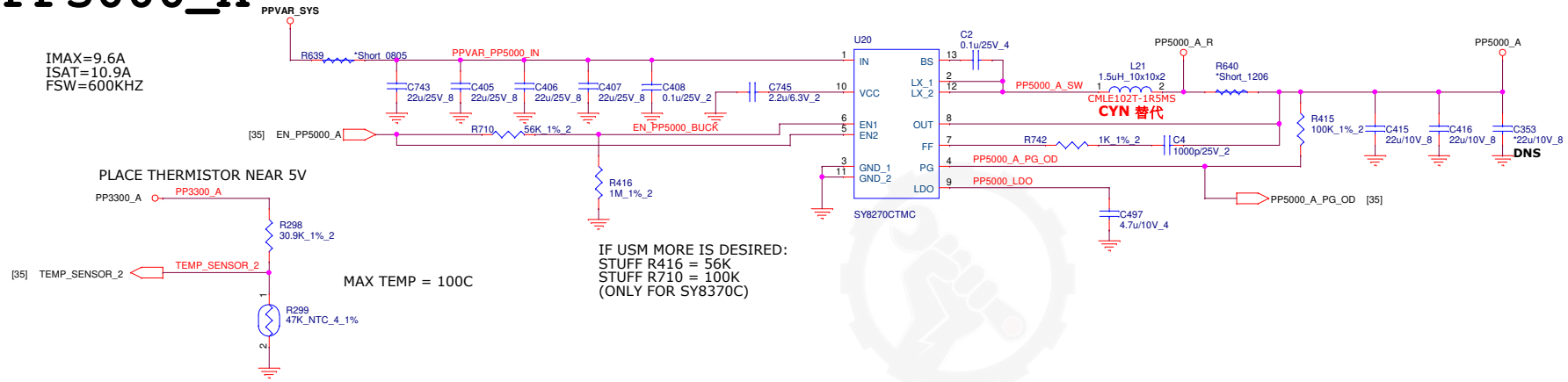
IMAX = 0.2A
ISAT = 0.2A
FSW = 500KHZ

VOUT=0.6*(1+RH/RL)
PG FROM EC OR SILEGO



PP5000_A

IMAX=9.6A
ISAT=10.9A
FSW=600KHZ



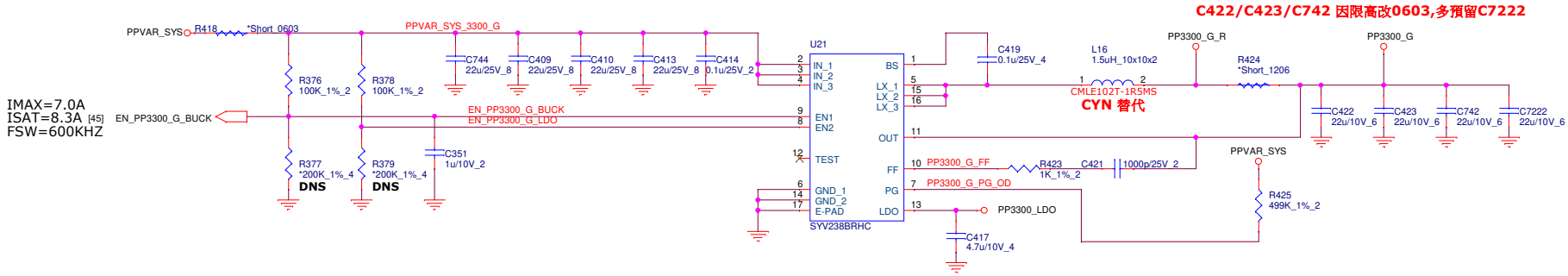
PLACE THERMISTOR NEAR 5V

MAX TEMP = 100C

IF USM MORE IS DESIRED:
STUFF R416 = 56K
STUFF R710 = 100K
(ONLY FOR SY8370C)

PP3300_G

C422/C423/C742 因限高改0603,多預留C7222

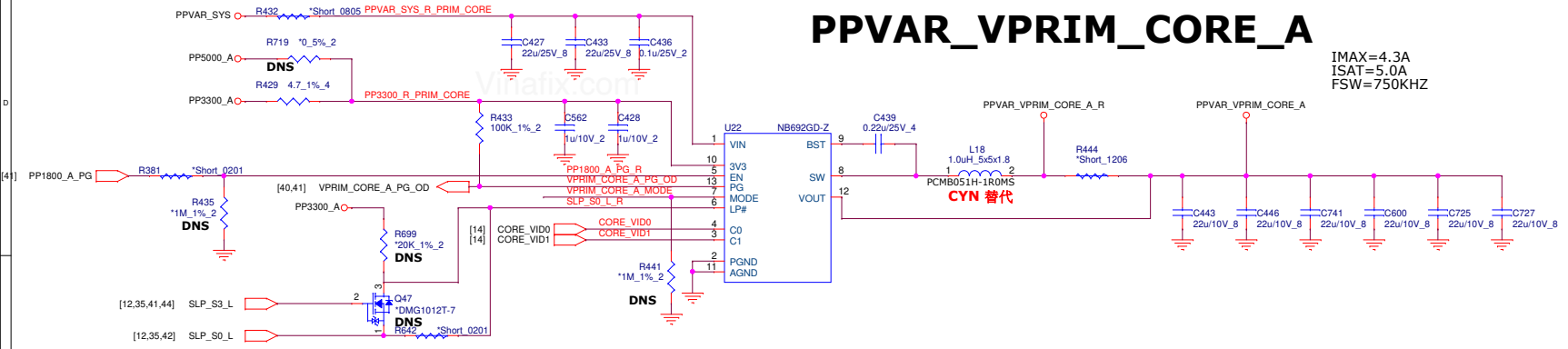


Quanta Computer Inc.
PROJECT :
POWER: 5V, 3.3V, 1.8V
Size | Document Number | Rev 1C
Date: Wednesday, April 08, 2020 | Sheet 39 of 49

SETTINGS

PPVAR_VPRIM_CORE_A

IMAX=4.3A
ISAT=5.0A
FSW=750KHZ

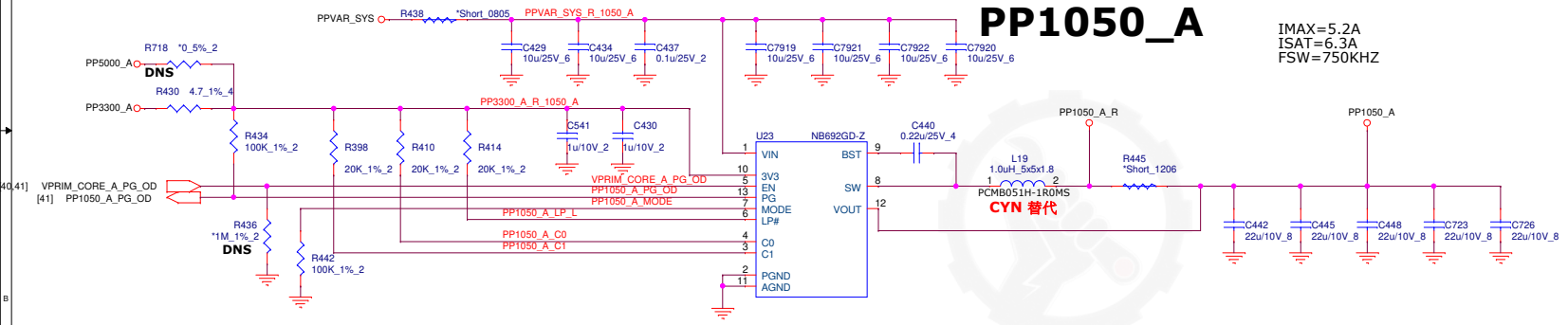


	VOUT	LP_L	C0	C1
PPVAR_VPRIM_CORE_A	0.75	0	x	x
	0.9	1	0	0
	0.95	1	0	1
	1.00	1	1	1
	1.05	1	1	1
PP1050_A	1.05	1	1	1
PP950_VCCIO	0.95	1	0	1

*LP_L, C0, C1 PULLED HIGH INTERNALLY

PP1050_A

IMAX=5.2A
ISAT=6.3A
FSW=750KHZ

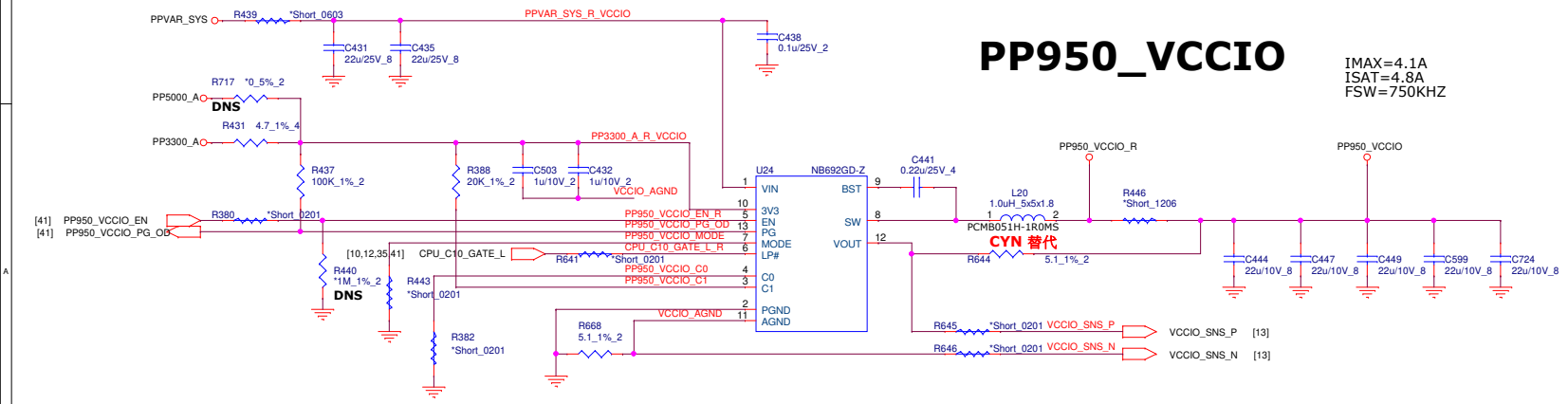


OPERATING MODE	EN PIN VOLTAGE [V]
ULTRASONIC (USM)	1.3 - 1.7
NORMAL	> 2.3

*EN PIN HAS 800K INTERNAL PU

PP950_VCCIO

IMAX=4.1A
ISAT=4.8A
FSW=750KHZ



RAIL	MODE PIN PD RES
PPVAR_VPRIM_CORE_A	FLOAT OR >230K
VCCOPC/V1.0A/EOPIO	100K
VCCIO	0

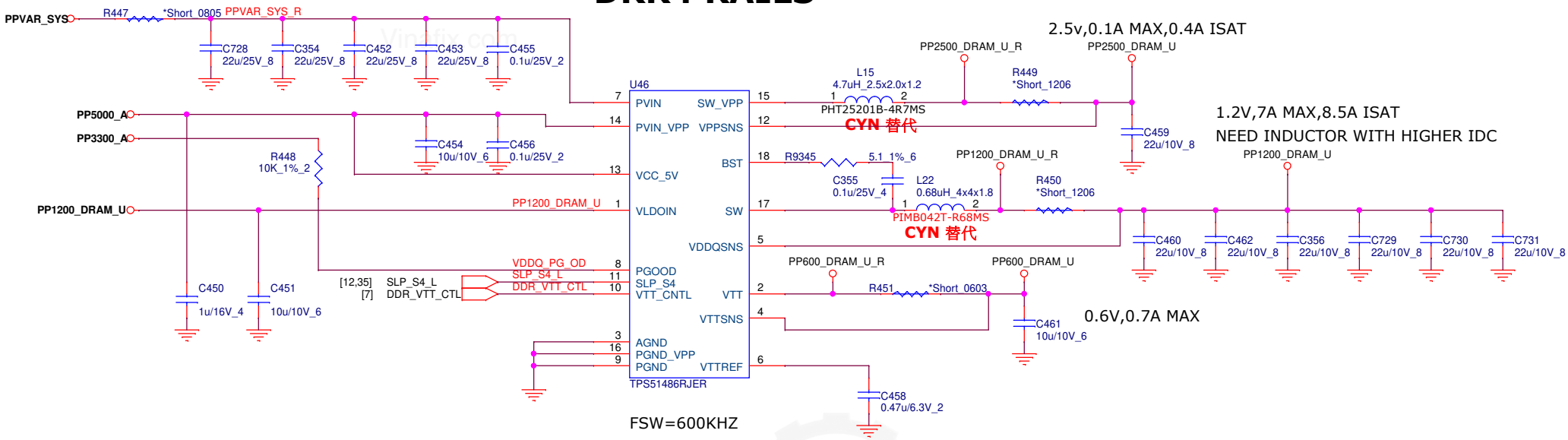
Quanta Computer Inc.

PROJECT :

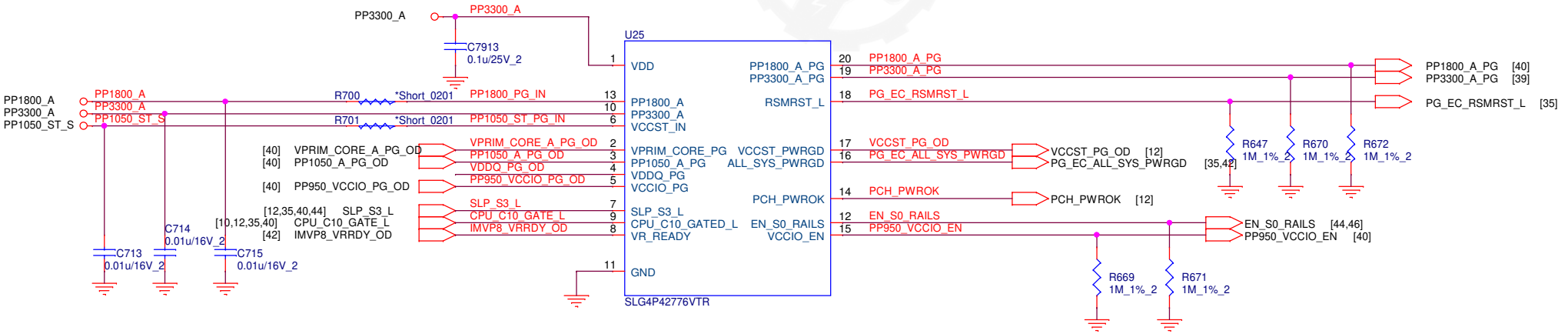
Size	Document Number	Rev
	VCCPRIM_CORE, 1.05, VCCIO	1C

Date: Wednesday, April 08, 2020 Sheet 40 of 49

DRR4 RAILS



POWER GOOD GENERATION

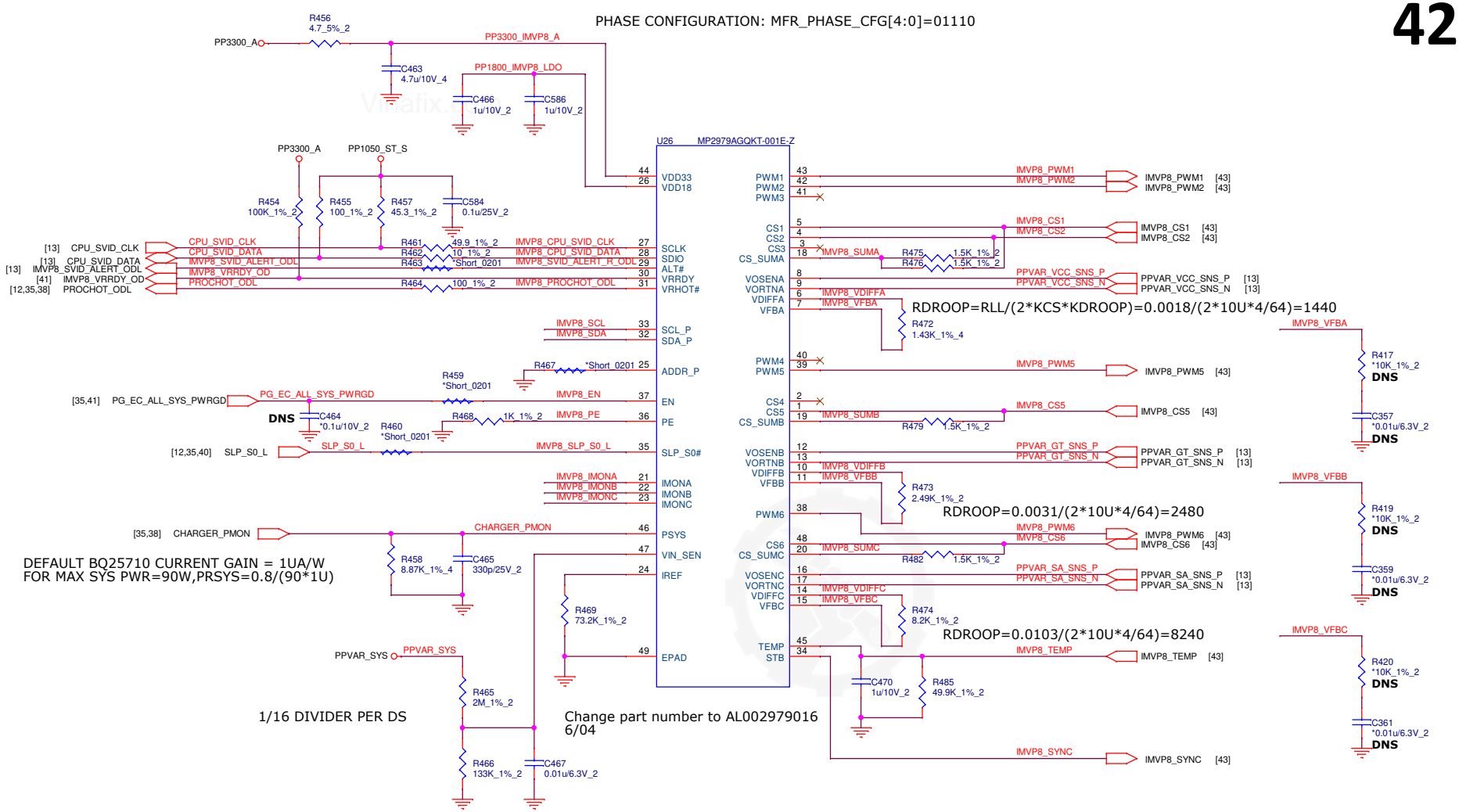


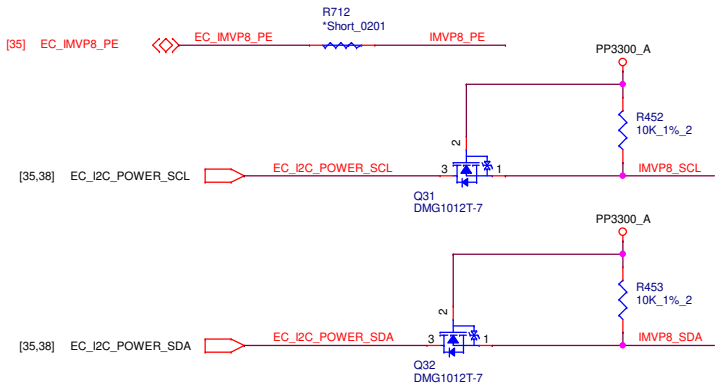
Quanta Computer Inc.

PROJECT :

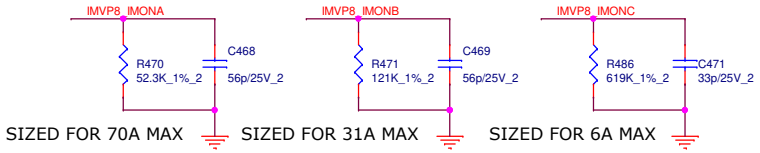
Size	Document Number	Rev
	POWER: VDDQ, PG CHIP	1C
Date: Wednesday, April 08, 2020	Sheet 41 of 49	

PHASE CONFIGURATION: MFR_PHASE_CFG[4:0]=01110





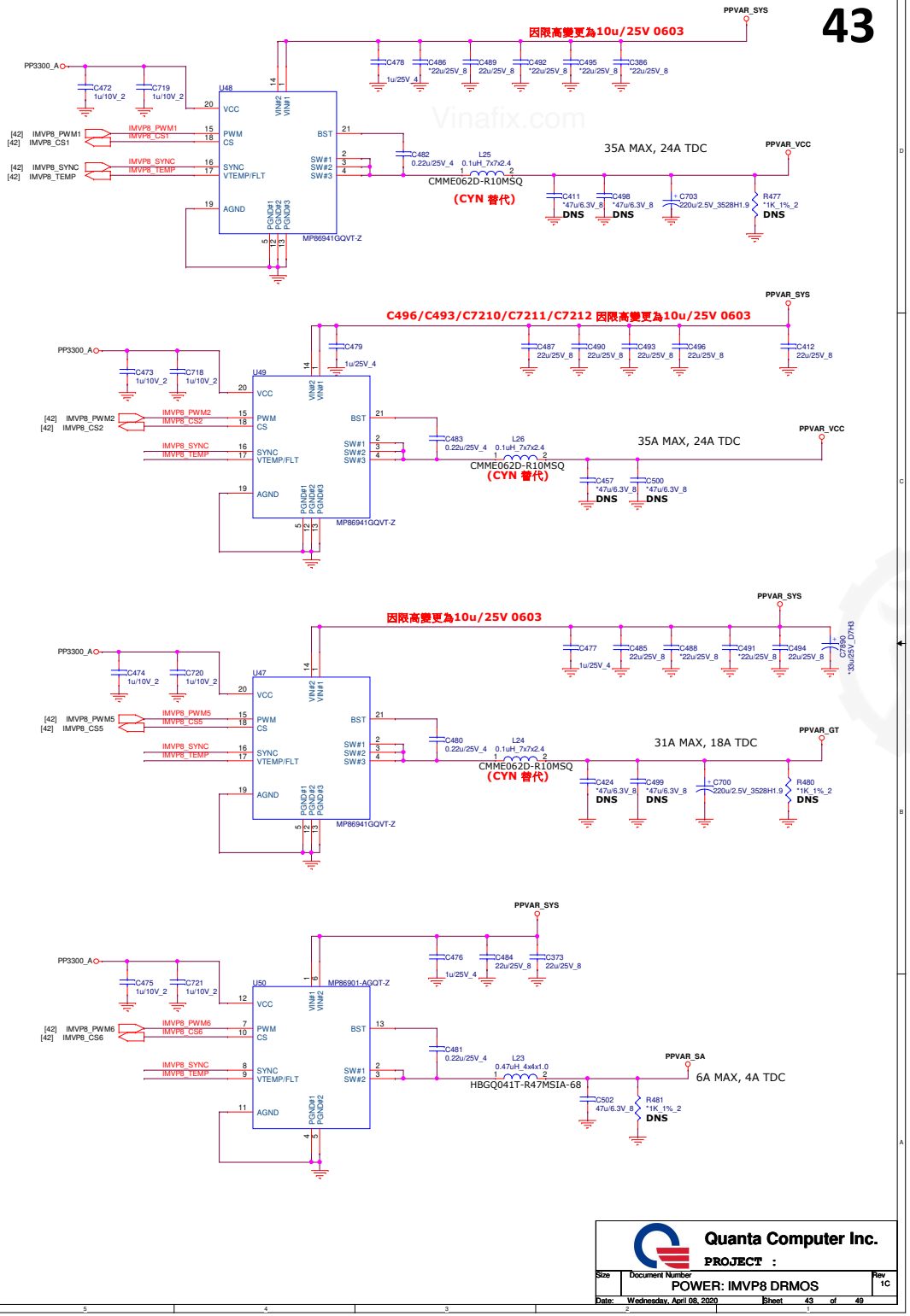
RIMON=32*VIMON_MAX/(ICCMAX*KCS), WHERE VIMON_MAX=1.1636, KCS=10U



Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
	POWER: IMVP8	1C
Date: Wednesday, April 08, 2020	Sheet 42 of 49	



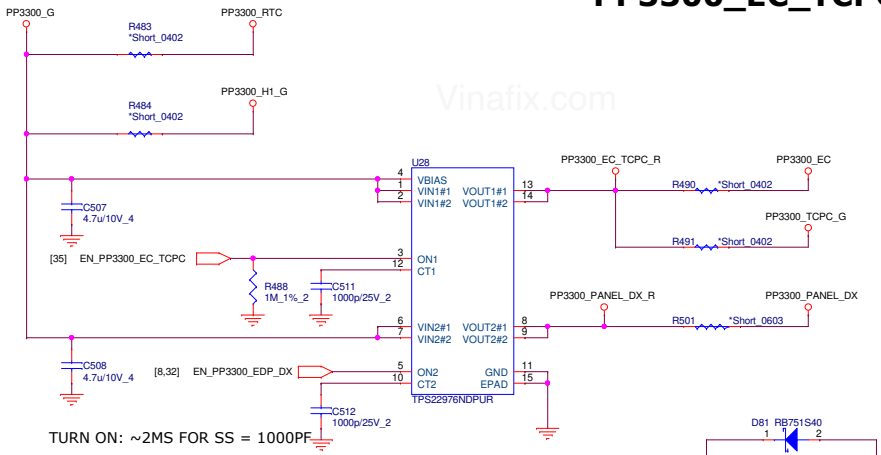
Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
	POWER: IMVP8 DRMOS	1C

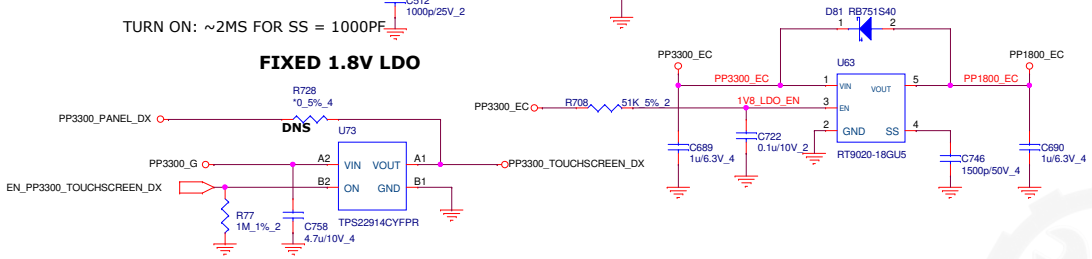
Date: Wednesday, April 08, 2020 Sheet 43 of 49

PP3300_EC_TCPC

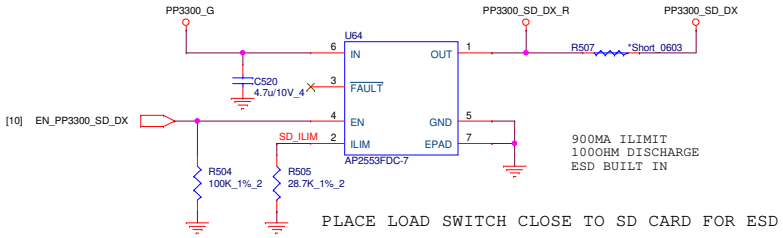


TURN ON: ~2MS FOR SS = 1000PF

FIXED 1.8V LDO



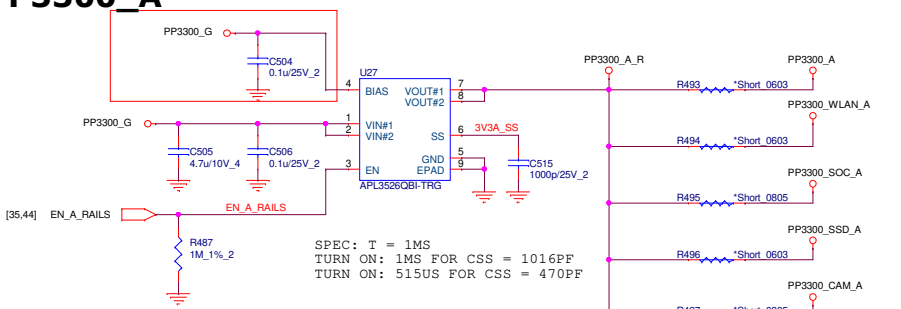
PP3300_SD_DX



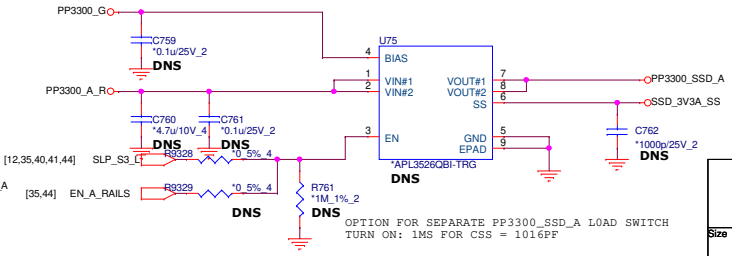
900MA ILIMIT
100OHM DISCHARGE
ESD BUILT IN

PLACE LOAD SWITCH CLOSE TO SD CARD FOR ESD

PP3300_A

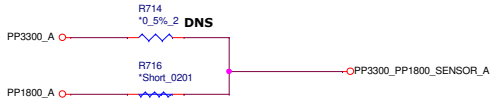


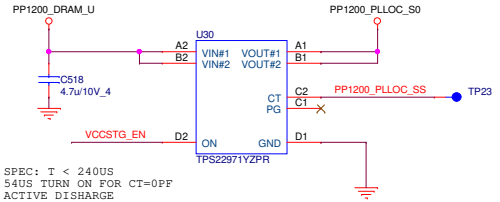
SPEC: T = 1MS
TURN ON: 1MS FOR CSS = 1016PF
TURN ON: 515US FOR CSS = 470PF



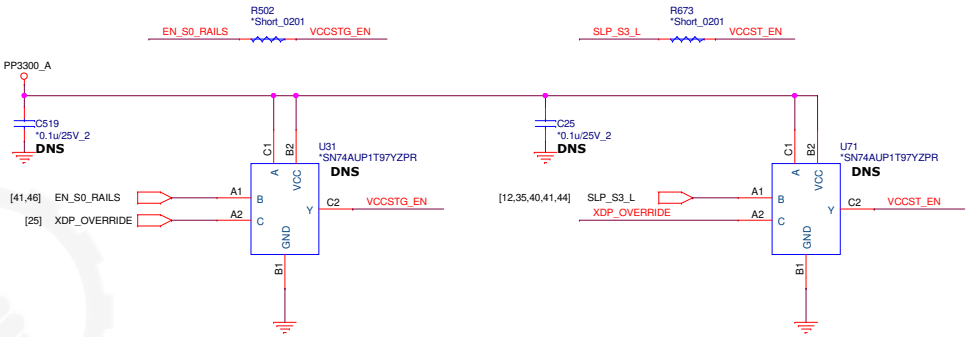
OPTION FOR SEPARATE PP3300_SSD_A LOAD SWITCH
TURN ON: 1MS FOR CSS = 1016PF

PP1200

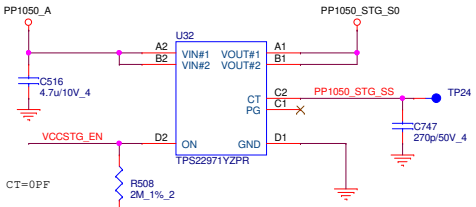




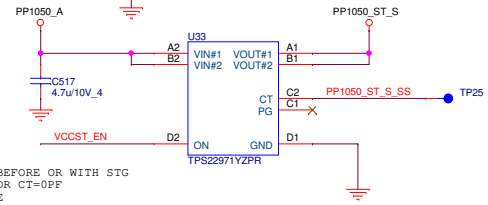
SPEC: T < 240US
54US TURN ON FOR CT=0PF
ACTIVE DISHARGE



PP1050



SPEC: T < 65US
54US TURN ON FOR CT=0PF
ACTIVE DISHARGE

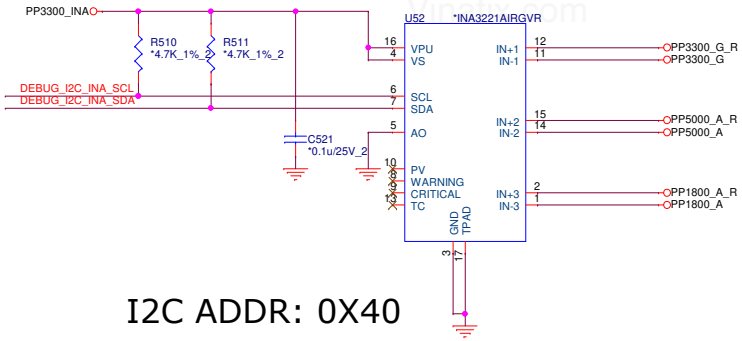


SPEC: COME UP BEFORE OR WITH STG
54US TURN ON FOR CT=0PF
ACTIVE DISHARGE

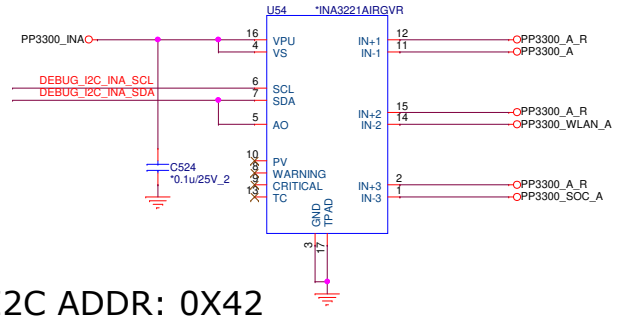
Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	POWER: LOAD SWITCH	1C
Date: Wednesday, April 08, 2020	Sheet 44 of 49	

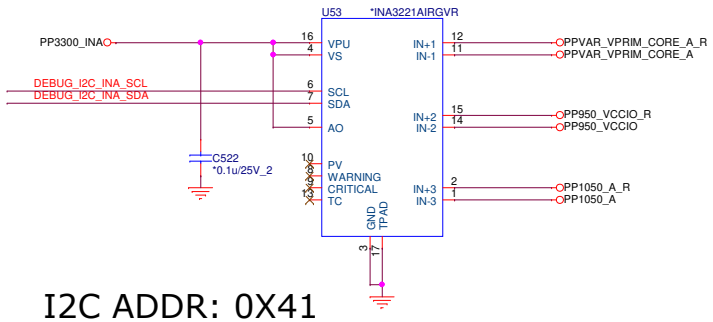
[24,26] DEBUG_I2C_INA_SCL
[24,26] DEBUG_I2C_INA_SDA



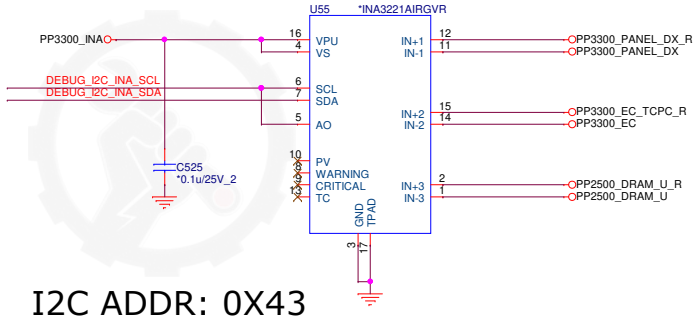
I2C ADDR: 0X40



I2C ADDR: 0X42



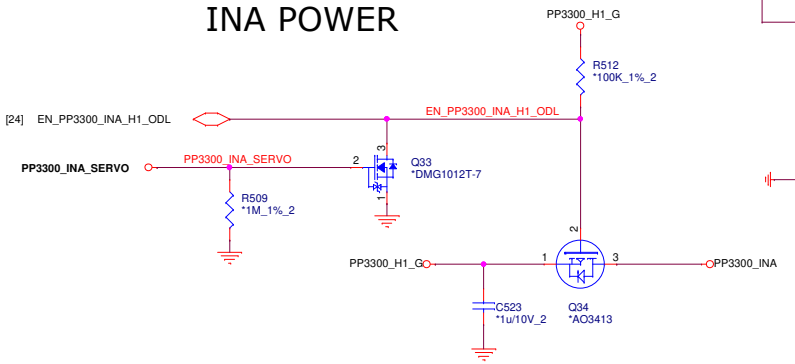
I2C ADDR: 0X41

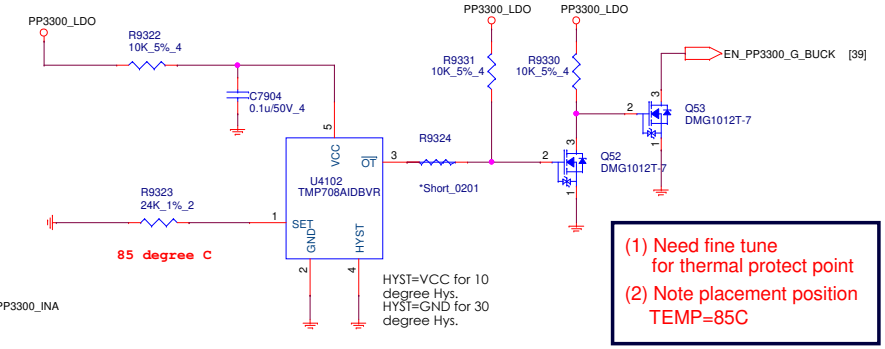


I2C ADDR: 0X43

Thermal protection

INA POWER



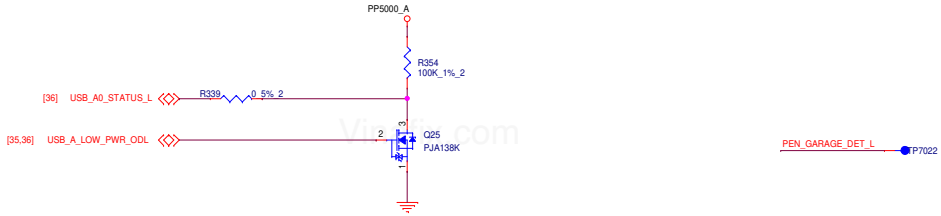


(1) Need fine tune for thermal protect point
(2) Note placement position TEMP=85C

Quanta Computer Inc.
PROJECT :

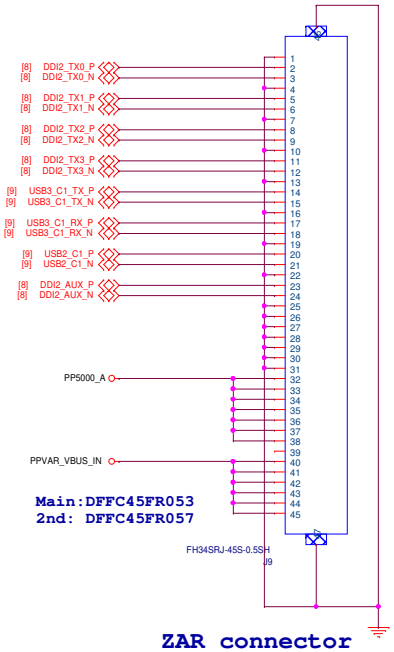
Size	Document Number	Rev
	INAS / Thermal	1C

Date: Wednesday, April 08, 2020 Sheet 45 of 51



PEN_GARAGE_DET_L — TP7022

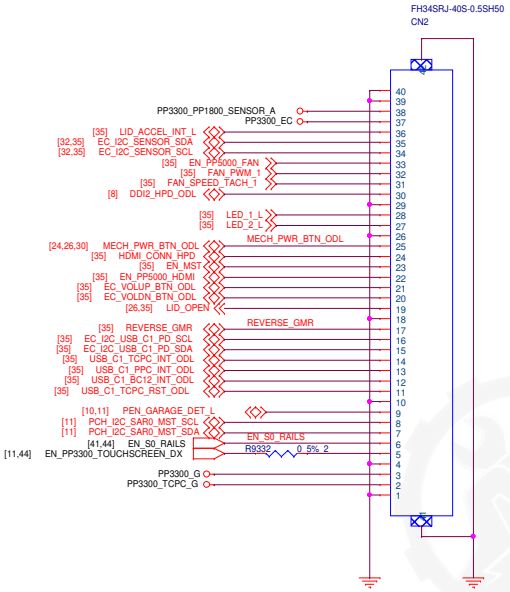
5/27 reverse



Main:DFFC45FR053
2nd: DFFC45FR057

ZAR connector
0426 change P/N

5/27 reverse



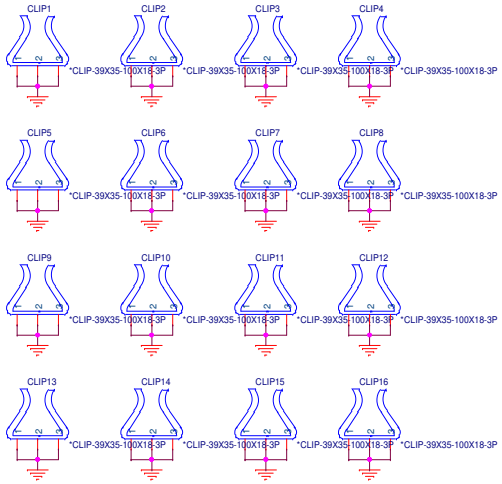
ZAR connector
0426 P/N check OK

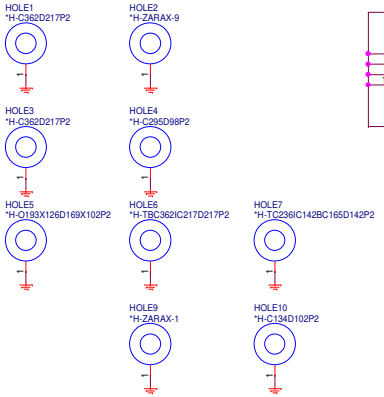
[27,29,35,39,44,45] PP3300_G
[35,37,44] PP3300_TCPC_G
[24,28,36,37,39,40,41,45] PP5000_A
[37,38] PPVAR_VBUS_IN

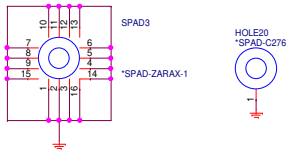
For unuse Board ID

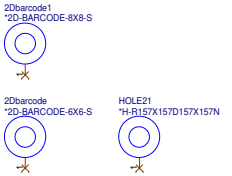
TP7024 — Board_ID — R7500 — ZAR@1K_1%_2

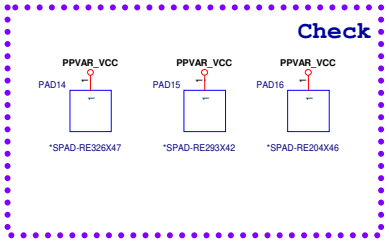
[CLIP]

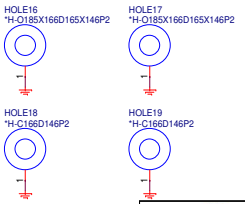












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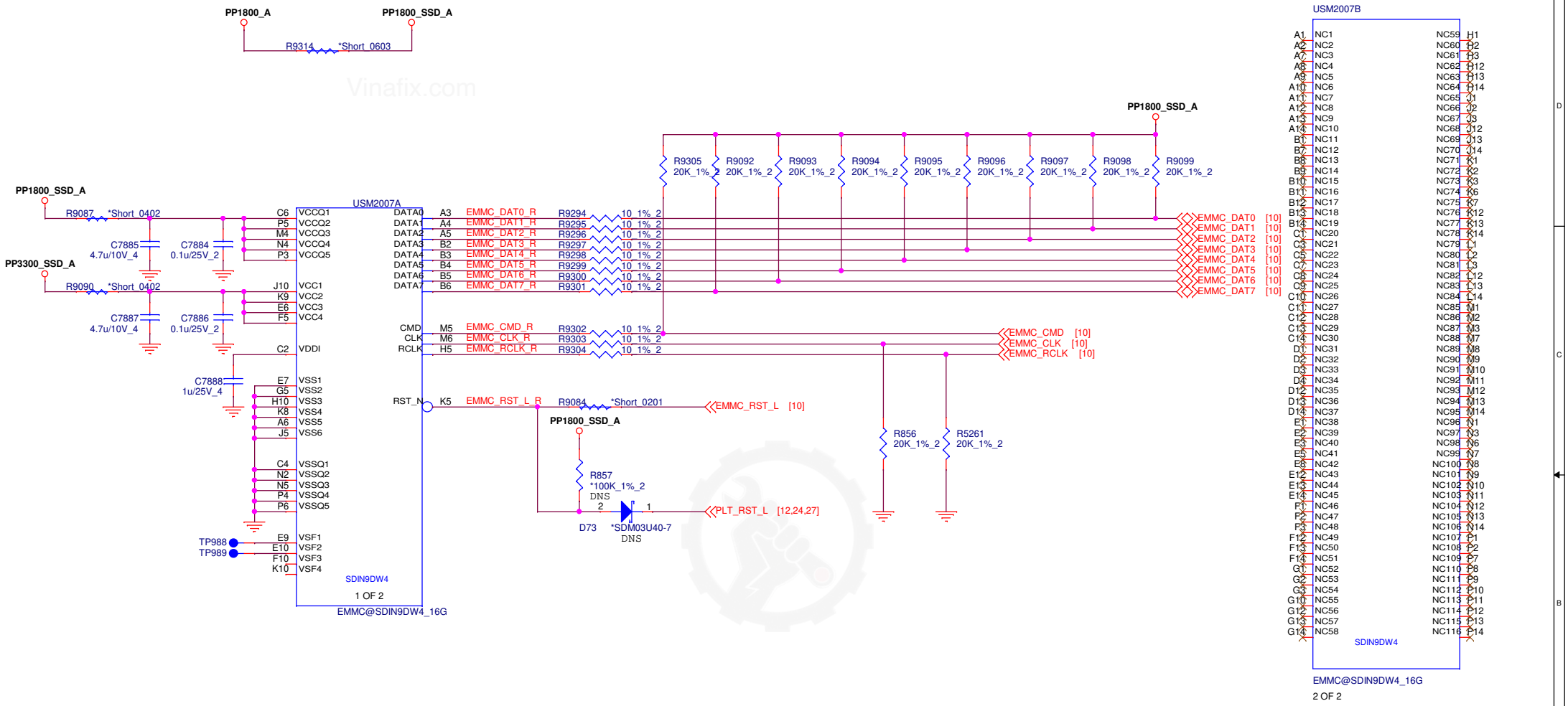

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Model	Version	CHANGE LIST
	1A	1. First release
	1B	1. page 22: Delete C599,C600 on DDR CLK lines, these are being removed from CML PDG 2. page 35: Move PD resistors on HDMI_CONN_HPD R533 to MLB EC page 3. page 33: Add 10k PU R706,R707 to PP3300_WLAN_A on M2_SHUTDOWN_L and also BT_DISABLE_L 4. page 11: Change PU on R499 to 1.8V 5. page 10: Move MEM_CH_SEL to GPP_F2 6. page 9: Move WiFi M.2 USB from SoC port 5 to port 10 7. page 41: U25, Use Silego part with new firmware with adjusted tolerances (BOM change) 8. page 35: USB_C0_TCPC_RST_ODL to USB_C0_TCPC_RST and remove R687 9. page 35: Remove TCPC_USB_C1_HPD from EC 10. page 35: Move EC_VOLDN_BTN_ODL to GPIO93 on EC 11. page 35: swap FAN_SPEED_TACH_2 on GPIOA4 with EN_PP5000_A on GPIO73 12. page 30,35: Moved DS1, DS2, R629, R630, R631, R632, D21 (power LED) from EC page to Base page 13. page 44: VIN of U63 change to PP3300_G. Add a 10K/0.1uF RC delay (R708, C722) to the enable of U63 and have it enabled by PP3300_EC 14. page 39: Changed PU on R415 to PP5000_A 15. page 10: Add a 100K PU R709 on GPP_F23 to 1.8V 16. page 24: Q44,Q43 bodydiode pointed to the wrong way should be towards USB_C0_SBU1_U and USB_C0_SBU2_U 17. page 39: U21+Others, Replace PU2 (SYV886) with NB690 to allow for higher current output. 18. page 40: U22, Add 4 22uF output caps (6 output caps total) 19. page 40: U23, Add 2 22uF output caps (5 output caps total) 20. page 40: U24, Add 3 22uF output caps (5 output caps total) 21. page 41: U46, Add 3 22uF output caps (6 output caps total) and Add another 22uF input cap (4 input caps total). Change inductor to 0.68uH instead of 1uH. Need Isat > 8.5A and Idc>7A 22. page 45: Q33 set to STUFF 23. page 42: Change R468 to 1K ohms. Add a 0 ohm resistor between the PE signal (Pin 36) and GPIOA7 of the EC. Name the net EC_IMVP8_PE on the EC side and IMVP8_PE on the MPS side 24. page 11: Remove R60, R63 25. page 32: Remove Q19, Q20, R291, R292. Remove PCH_I2C_PEN_SDA/SCL_Q nets from J25 connector 26. page 37: DNS resistors R637, R636 27. page 11,32: PCH_I2C_TOUCHSCREEN_SDA/SCL change to PCH_I2C_USI_SDA/SCL. Change on both sides of FETs. 28. page 11,32: TOUCHSCREEN_RST_L rename as USI_RSL_L. Change on both sides of FET 29. page 11,32: TOUCHSCREEN_INT_L rename as USI_INT_H. Remove PU and add 1M pull-down 30. page 11,32: TOUCHSCREEN_DIS_L rename as USI_REPORT_EN 31. page 39: Ignore line items 36-40. Replace U20 with SY8270C. There should be 4x22uF input caps and 2x22uF output caps. Inductor should be 1.5uH with Idc > 9.6A and Isat > 10.9A. Add a voltage divider to the EN signal. Divider is just a place holder for now. When SY8370C is used R1 = 100K, R2 = 56K (refer to google schematic) 32. page 39: Replace U21 with SYV238B. There should be 4x22uF input caps and 3x22uF output caps. The inductor should be 1.5uH with Idc > 7A and Isat > 8.3A 33. page 44: Replace U63 with RT9020 34. page 44: Add 270pF C747 cap to GND 35. page 17: Reduce to C94 22uF instead of 47uF 36. page 27: Add control circuit for PLT_RST_L with EC_PCH_RSMRST_L control. Follow Google's schematic 37. page 2(on USB DB): Add schottky diode D79 clamps the AUX line to the 3.3V rail to limit overshoot problems: DP_MST_AUX_C_N to PP3300_TCPC 38. page 35: Reduce C335 from 10uF to 4.7UF 39. page 37: Add schottky diode D80 clamps the AUX line to the 3.3V rail to limit overshoot problems:DDI1_AUX_N_C to PP3300_TCPC 40. page 37, 2(on USB DB): Add a 0 ohm resistor between PP5000_A from VCONN Power and DNS it on both U60 and U65 41. page 44: R708 should be ~51K. C746 should be at least 1500pF. Input to LDO should be PP3300_EC 42. page 42: Change R469 to 73.2kOhm 43. page 14: Added C734 - a 1uF cap to be placed near BV2. Added C733 - a 1uFcap to be placed near BV12 44. page 27,35: Added M2_SSD_PLN net to pin 8 of the SSD connector and connected this to GPIOA0 on the EC 45. page 11,34: Changed the name WWAN_RADIO_DISABLE_1V8_ODL to WWAN_RADIO_DISABLE_1V8. Change the name WWAN_RADIO_DISABLE_1V8_Q_ODL to WWAN_RADIO_DISABLE_1V8_ODL. Replaced fet Q52 with diode D82 46. page 12: Add a test point to XDP_BPM<0> 47. page 33: Add a DNS PU R722 to 1.8V on CNV_BRI_DT 48. page 32: Added ALS_INT_L on page 32 49. page 44: Created PP3300_PP1800_SENSOR_A (default to PP1800_A) so that we can switch the sensor power rail to 3.3V if desired 50. page 32, 35, 1(on G sensor DB): Changed PP1800_A to PP3300_PP1800_SENSOR_A EC_I2C_SENSOR_1V8_SCL to EC_I2C_SENSOR_SCL EC_I2C_SENSOR_1V8_SDA to EC_I2C_SENSOR_SDA 51. page 35: Added R723, R724 100K pullups to PP3300_PP1800_SENSOR_A on LID_ACCEL_INT_L and ALS_INT_L 52. page 39: Changed inductor L16 and L21 to CMME102T-1R5MS
	rev 2_1	1. page 11,35: Add a PU R725 to EC_PCH_INT_L and change name to _ODL 2. page 32: On all the touchscreen and pen devices, pull them up(PP3300_PANEL_DXPCH_I2C_USI_SDA/SCL, USI_RST_L) to PP3300_TOUCHSCREEN_DX instead 3. page 11,32: Rename USI_INT_H to USI_INT 4. page 11, 34: Rename WWAN_RADIO_DISABLE_1V8 to WWAN_RADIO_DISABLE_1V8_L 5. page 11: Rename EMR_GARAGE_DET to PEN_GARAGE_DET_L on BY30 6. page 11: Change BV30 from unused PEN_RESET_L to FPMCU_BOOT1 7. page 16: Remove TP38, TP44-TP49 8. page 26: Add 100K R726 PD to Pins 26 on servo(J3) 9. page 31: Remove SLP_S4_L and SLP_SUS_L going to FP connector 10. page 23: Change the SPI ROM to a 16MB part 11. page 35: Pull up R359 to PP3300_G, Connect EC_RST_ODL to PSL4 , Move SYS_RST_ODL to pin GPIOC5/KBRST_L 12. page 35: Add a diode D83 with annode connected to GPIO77 and cathode connected to EC_RST_ODL before R359 13. page 23: Move R198 closer to the SPI ROM and DNS it with a note that the resistor should be close to the SPI ROM to reduce the stub 14. page 26: Remove U40 and related components, ADD R744~R751 15. page 4(on USB DB): Move D79 to be in parallel with R506 16. page 31: Add straps, PUs, and PDs to MCU signals 17. page 31: Option for PDs on SPI CS signals 18. page 46, 1(USB DB): move power button switch (SW1)to USB DB 19. page 47: add eMMC page 20. page 33: change WIFI from M.2 type to solder down type 21. page 30, 5(USB DB): move LED and Fan to DB 22. page 31: remove finger print function 22. page 34: remove LTE function 23. page 10: Move MEM_STRAPs to match eMMC schematic 24. page 2,3: update block diagram 25. page 32: update edp pin define 26. page 46: add pen detect circuit and pen charge circuit. 27. page 9: delete TP7010-7013, TP7018-7019, TP7022-7029, TP7036-TP7041 28. page 34: delete R311,R627,R628(LTE) 29. page 11: delete TP7030-7035,TP7020, TP7021 30. page 31: delete finger print circuit 31. page 11, 46: delete PEN_PDCT_ODL, PEN_RESET_ODL,PEN_INT_ODL NET 32. page 33: M2_SHUTDOWN_L connect to wifi pin 28 ,BT_DISABLE_L connect to wifi pin 63 33. page 12: stuff R101 33. page 25: delete TP128~TP133, delete R201,R203,R205,R207,R209,R9282 34. page 23: delete R165,Q9, U38 PIN 9 change to NC. 35. page 47: stuff 49084, unstuff R857 , add R9314
	rev 2_2	1. page 11: Removed TRACKPAD_INT_ODL from GPP_D21 2. page 11: Change R74 to 4.7K 3. page 25: DNSed all XDP components 4. page 11: Removed WWAN_CONFIG_0/1/2/3 and R95/R96/R97/R98 5. page 11: Removed TP16,TP26,TP27,TP37 and R20,R21,R72 6. page 10: Added R9325 100k ohm to GPP_F23 and stuff, DNS R709

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	1C	1.Down size of some cap and res footprint.(C1205,C7835,C7836,R857,R721,R720,R46,R47,R680,R681,R5118,R5168,R9058,R9059,R9316, C290,C291,C292,C293,C294,c295,C296,C297,C300,C301). To optimize routing. 2.Del J24. (colay keyboard connector no use in future) . 3.Adjust PPVAR_SYS Cap quantity and value of U47,U48 and U49. New placement without high limit, we change back to follow CRB design. 4.Del pen function (J25,J26,U4101 relative sch).Customer remove this function form feature list. 5.Change CN1,J16,J17 connector type for new ID. 6.Colay SPI ROM socket 7.Reverse J6,J7,J9,CN2,pin define for placement 8.Change to EC_PROCHOT_IN_OD to EC_PROCHOT_IN(Clarity for firmware) 9.R303 Change to 1.2k (Reduce rise time < 100ns on WAKE signal) 10.R231 Change to 2.2k (Reduce rise time < 100ns on WAKE signal) 11.Q46 Gate of this transistor should be connected to PP3300_H1_G 12.Change connector PN follow connector list.(J17,J6,J2,Page30,37) 13. Adjust PPVAR_SYS_R_VCCIO CAP (2x 22U -->6x10u, due to layout high limit,Page 40) 14. Change this circuit to match Nami CCD circuit (Q46, Q18, R538,Page 24) 15. Adjust cap of PPVAR_VPRIM_CORE_A and PP1050_A (due to high limit, Page40) 16. Del reserve GMR function on MB (Page32) 17. Add power net name between D2 and U37 (Page23) 18. R5237 chnage to 0201 size (Page36) 19. Down size of res and cap (EMMC)(Page47).To optimize routing. 20. Modify sch of thermal detected.(Page45) 21. Change J23 PN follow connector list .(Page28) 22. Down size of cap (TX/RX cap)(Page37).To optimize routing. 23. Change ESD solution (Page37).To optimize routing. 24. Add screw hole (Page46) 25. Swap L10,L3,L4,L5,L9 pin connection.(Page36) To optimize routing. 26. Change USB typeA ESD solution D28,D87 (Page36) 27. Add screw hole (Page46) 28. Change U63 PN to RT9020-18GU5. Output Voltage should be 1.8V not 3.3V (Page44) 29. Change J7 PN follow connector list (Page30) 30. Swap L4,L5 pin connection.(Page36) To optimize routing. 31. Add EMI solution. C7923,C7924,C7925,L29,L30,L31,L32,L33,L34,L35,L36(Page10,Page28,Page29,Page37) For EMI reserve. 32. Add connection to CN2 for PEN.(Page46) 33. Del TP103,TP105,TP113,TP111,TP114,TP115,TP104,TP112,TP118,TP106,TP110,TP116,TP109,TP108,TP135,TP134,TP120,TP107.(Page16) 34. Change USB typeA / typeC ESD solution add D66,D88,D89,D90 & Del D86,D87(page 36,37) for Intel Feedback add F2 for safety request(page 36) 35. Change hole9/hole10 footprint and add 2 clip (Page46) 36. DNS R711, C349 (Page37) VCONN for Port 0 is sourced from U44 37. Add DNS buffer powered from PP3300_G to isolate PLT_RST_L from M2_SSD_RST_L_R (in parallel with R229). Add note that it is only needed for SSDs that have an internal pull-up. (Page27) Internal pull-up on some SSDs can cause glitch on PLT_RST_L after the AP stops driving it, causing CR50 to think that AP is still on. 38. Change R362 to 48.7k, and add note that if using TI BC1.2 part, value should be 51.1k, Change R363 to 29.4k, and add note that if using TI BC1.2 part, value should be 30.9k (Page36) 39. Add a schematic note next to this signal that describes when this signal is needed.Need to make this clear to OEMs(Page11) 40.Add DNS 200pF caps near TCPC.May need to add capacitance in order to meet USB PD cReceiver minimum spec(Page37) 41.Add TABLET_MODE signal to GPIOC7 pin on EC.This will be used in systems that have GMR sensor instead of hall effect (Page35) 42.Change C302, C303 to 0 ohm(Page8).we mount cap on USB board. 43.Modify Hole2 Hole3 Hole4 footprint. (Page46) 44.Modify J4 J5 footprint. (Page27,29). Follow connector list. 45.Modify XDP connection. (Page12,25). To optimize routing. 46.Modify PAD footprint. (Page46). 47. Change C55,C98,C86,C91,C73,C118,C29,C37,C193,C144,C186,C211,C203,C152 PN(Page17). Without high limitation, change to another one. 48. Change R490 to 0.1 ohm (Page44). 49. Change clip PN for ME request (Page46). 50. Change Hole7,Hole8 footprint (Page46). 51. Change D66,D88,D89,D90 PN (Page36,37). USB+- should use ESD component with 5v tolerance.

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Model	Version	CHANGE LIST
	1D	1.Page 12,25 : Modify XDP connection. For intel issue tracker JTAG connection. Stuff these resistors R202, R203, R204 R205, R206, R207, R208, R209, R210, R211. 2. page 30 : J2 pin define upside down(JIM) 3. page 36 : remove F2 on PP3300_SD_DX. Due to U64 already had safety function. 4. page 11 : Change R75 pull up to be PP1800_A. GPP_A8 Dual-route signal to GPP_A16 5. page 32: Remove "USI INT IS ACTIVE HIGH" note. 6. page 11: Change R771 pull up to be PP1800_A. GPP_A8 Dual-route signal to GPP_A16 7. page 8, USB D/B page 4: Move diode D79 to DDI2_AUX_N on page 8 (cathode connected to PP3300_SOC_A) 8. page 25 : reserved R667 for DCI. 9. page 10 : unstuff C7924 for SD_CLK EMI suggestion, after EMI test, we can remove it and signal will be more positive. 10. page 10 : Add R9340 damping R for CNV_CLKREQ 11. page 29 : Add R773,R772 option for output crosstalk tuning 12. page 11 : DNS series resistors R20, R21 and R72 on unused PCH SPI1 interface 13. page 35 : Put diode D84 in series with signal KSO_06, cathode connecting to EC and anode connecting to the keyboard connector. Remove R691 499 ohm series resistor.
	ZAR DVT ZSI EVT	1.Page 37(Follow Hatch change list) : add FB4 between AVDD and DVDD rails of ANX3447. add C764, C765, C766 for DVDD rails. 2.Page 32: add Q55,Q501,R9342,R9343,R9344 for panel T11 timing tuning. 3.USB D/B : modify R629 to 3.3k and modify R630 to 1.8k for LED current setting 4.USB D/B : R9390 change from 1k to 620 ohm to prevent OCP (Fan Iset up to 0.9A) 5.MLB : add layout test point for factory request 6.Page 37(Follow Hatch change list): Connect DVDD_IO to PP3300_TCPC_AVDD through a 0 ohm resistor R775 7.Page 37(Follow Hatch change list): connect pull-up R319 to PP3300_TCPC_AVDD because ROLE_SEL needs to be pulled up to AVDD33 8.Page 37(Follow Hatch change list): add note stating that 100K pull-up / pull-down is 'no-stuff' only for ANX3447 because of bug b:/124410548 9.Page 37(Follow Hatch change list): add 10K series resistor R218 at output of GPIO2/PSL_IN4 to Improper isolation of EC_RST_ODL on some NPCX79nx designs 9.Page 29: add C7932, C7933 for PP1800_A power rail
	V3.0	1.Page 23(Follow Hatch change list) : R163 change from 100k to 4.7k because Input impedance on EC EEPROM WC# pin is too low, so pullup is too large. Static "high" voltage only reaches 1.15V when it should be ~3.3V, resulting in unprotected EC EEPROM
	V3.1	1. Page X : Change to shortpad : Location : 0201 : R132,R133,R194,R202,R203,R204,R205,R206,R207,R208,R209,R210,R211,R223,R241,R242,R254,R255,R26,R261,R262,R28,R30,R33,R334,R335,R356,R371,R384,R5237, R635,R65,R661,R676,R690,R772,R773,R9084,R9327,R9334,R9335 0402 : R225,R5238,R744,R746,R748,R9087,R9090,R9308,R9309,R9310,R9340 0603 : R137,R138,R235,R236,R237,R683 0805 : R659,R660 2.Page 23 : (1) Remove U3 (BIOS socket) (2) Reserved U4104 for shortage issue. (3) Add R9348 for realtek recommend . (3) Remove soundwires straps : R244,R245,R246,R247,R248,R249,R250,R251,R252,R253 for realtek recommend . 3.Page 10 : (1) Remove C7925 for realtek recommend (2) Change R40 from 33 ohm to 0ohm for realtek recommend 4.Page 7 : Add. R9347 ,Reserved Q502 ,Q503 & Del. Q49 for reduce glitch 5.Page 29 : (1) Add C7934 for realtek recommend (2) Unstuff C7932,C7933 5.Page 44 : Change U27.4 BIAS pin from PP5000_A to PP3300_G for PP5000_A glitch
	V3.2	1.Page 35 & 46 : Connect U15.G8 to CN2.6,and change net name to EN_PP5000_HDMI 2.Page 44 : Change U75.4 BIAS pin from PP5000_A to PP3300_G. U75 is DNS SSD load switch 3.Page 8 : 1. U9334 & R9335 BOM (1) For PCB REV: G SHORT PAD (*) For PCB REV: I change to 0_2 (2)For ZAR Stuff CS00001JE18 (0_2) For ZSI Stuff CH4104K9E01(0.1U_2) 2. Change R288 ,R12 ,& D79 to ZSI@

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