Compal Confidential

FH7AT/FH5AT/FH4AT
MB Schematic Document

LA-K092P
Rev: 2A

2020.12.29

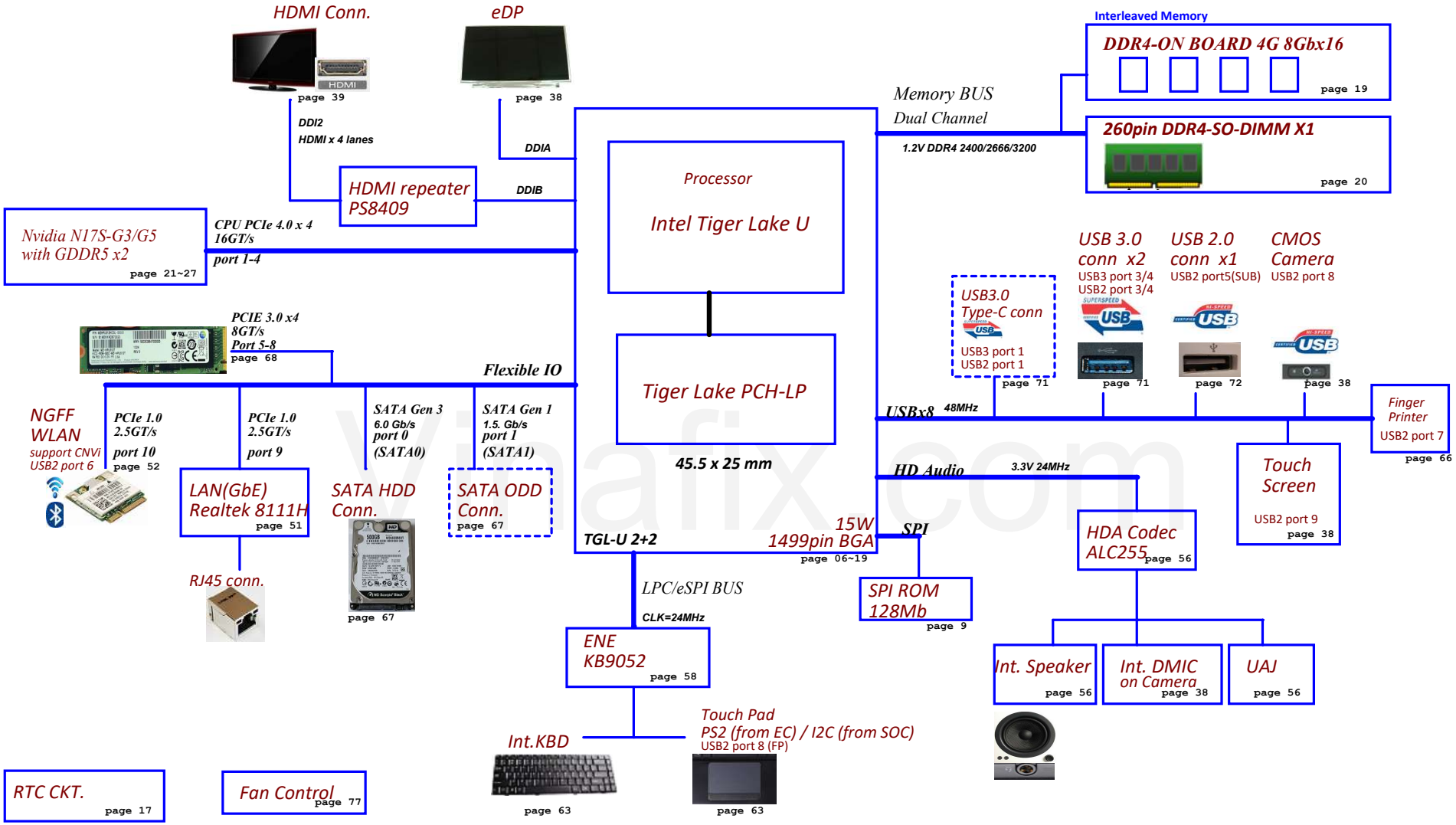
Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.		
Title: Cover Sheet		
Size	Document Number: LA-K092P	Rev: 0.1
Date: Thursday, May 06, 2021	Sheet 1 of 102	

Compal Confidential

Model Name: TGL-UP3

Project Name: LA-K092P



Compal Electronics, Inc.

Title: **TGL-UP3 Block Diagrams**

Size: | Document Number: **LA-K092P** | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 2 of 102

Vcc	3.3V +/- 5%	EC Board ID Table for AD channel				
Ra	100K +/- 1%					
Board ID	Rb	Vmin	Vtyp	Vmax	EC AD	
0 --> 0.1	0		0.000 V	0.300 V	0x00 - 0x13	SD034120280
1 --> 0.2	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E	SD034150280
2 --> 0.3	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25	SD034200280
3 --> 1.0	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30	SD034270280
4 --> 1A	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A	SD034330280
5 --> 1B / 2.0	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45	SD034430280
*6 --> 2A	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54	SD034560280
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64	SD034750280
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76	SD034100380
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87	SD034130380
10 --> K094 0.1	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96	SD034160380
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4	SD034200380
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF	SD000001B80
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7	SD00000G280
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF	SD034330380
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9	SD00000WM80
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4	SD034560380
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD	SD00000AL80
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0	
19	NC	3.000 V	3.000 V		0xF1 - 0xFF	

HSIO Port Table (PCH)

HSIO Port	Capable	Port Allocation	PCIE CLK	NOTE
0	USB3.1 #1 / PCIe #1	USB3.1 Type C	NA	USB3.1 interface
1	USB3.1 #2 / PCIe #2	NA	NA	NA
2	USB3.1 #3 / PCIe #3	USB3.1 Type A	NA	USB3.1 interface
3	USB3.1 #4 / PCIe #4	USB3.1 Type A	NA	USB3.1 interface
4	PCIe #5	SSD (NGFF Key M)	CLK1 & CLKREQ#1	PCIe interface
5	PCIe #6			
6	PCIe #7 /GbE			
7	PCIe #8 /GbE			
8	PCIe #9 /GbE	GLAN	CLK2 & CLKREQ#2	PCIe interface
9	PCIe #10	WLAN+CNVio (NGFF_KeyE)	CLK3 & CLKREQ#3	PCIe interface
10	PCIe #11 /SATA0	HDD	NA	SATA interface
11	PCIe #12 /SATA1	ODD	NA	SATA interface

Load BOM Option Table

	BOM Number	Load BOM Option
1.0	431AMYBOL06	VGA@/CHG@/MEM@/CNVi@/CMC@/GLITCH@/3S@/255@/MP@/I2CTS@/PREM@/i7@/G5@/N17S@/FP@/FP3V@
1.0	431AMYBOL55	VGA@/CHG@/MEM@/CNVi@/CMC@/GLITCH@/3S@/255@/MP@/I2CTS@/PREM@/i7@/G5@/N17S@/FP@/FP3V@
1A	431AMYBOL59	VGA@/CHG@/MEM@/CNVi@/CMC@/GLITCH@/3S@/255@/MP@/I2CTS@/PREM@/i7@/G5@/N17S@/FP@/FP3V@
1A	431AMYBOL60	VGA@/CHG@/MEM@/CNVi@/CMC@/GLITCH@/3S@/255@/MP@/I2CTS@/PREM@/i7@/G5@/N17S@/FP@/FP3V@
1A	431AMYBOL61	VGA@/CHG@/MEM@/CNVi@/CMC@/GLITCH@/3S@/255@/MP@/I2CTS@/PREM@/i7@/G5@/N17S@/FP@/FP3V@
1A	431AMYBOL07	VGA@/CHG@/MEM@/CNVi@/CMC@/GLITCH@/3S@/255@/MP@/I2CTS@/PREM@/i7@/G5@/N17S@/FP@/FP3V@
1A	431AMYBOL08	VGA@/CHG@/MEM@/CNVi@/CMC@/GLITCH@/3S@/255@/MP@/I2CTS@/PREM@/i7@/G5@/N17S@/FP@/FP3V@
1A	431AMYBOL09	VGA@/CHG@/MEM@/CNVi@/CMC@/GLITCH@/3S@/255@/MP@/I2CTS@/PREM@/i7@/G5@/N17S@/FP@/FP3V@

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
CMC	CMC@
UMA STRAP	UMA@
DIS circuit	VGA@
TPM	TPM@
PRIM Design	PREM@
Volume Design	VOL@
USB charger	CHG@
Intel CNVi	CNVI@
Intel design request	GLITCH@
G-Sensor	GSEN@
for SW debug board	UART@
EMI/ESD UNPOP	XEMC@
EMI/ESD requirement	EMC@
EMI requirement	EMI@
ESD requirement	ESD@
EMI/ESD require reserve	XEMC@
ODD SKU	ODD@
RF RESERVE	@RF@
3S BATTERY	3S@
VRAM BOM Select	X76@
ON BOARD RAM circuit	MEM@
SINGLE DIE OB RAM	SDP@
DUAL DIE OB RAM	DDP@
DIMM only sku	NODX76@
Finger Print	FP@
Finger Print (3V module)	FP3V@
Finger Print (5V module)	FP5V@
FP ESD requirement	FPEMC@
NV N17S-G3/G5	N17S@
NV N18S-G5	N18S@
NV N17S-G3 CHIP	G3@
NV N17S-G5 CHIP	G5@
I2C touch screen	I2CTS@
USB touch screen	USBTS@
ALC 255 Codec	255@
ALC 255M Codec	255M@
ALC 256 Codec	256@

Power State

STATE \ SIGNAL	SLP_S0#	CPU_C10_GATE#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	HIGH	HIGH	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	HIGH	HIGH	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	HIGH	HIGH	LOW	LOW	LOW	ON	OFF	OFF	OFF
S0IX	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	ON	ON

PCI-e 4 (CPU)

HSIO Port	Capable	Port Allocation	PCIE CLK	NOTE
0	PCIe4 #1	dGPU	CLK0 & CLKREQ#0	PCIe interface
1	PCIe4 #2			
2	PCIe4 #3			
3	PCIe4 #4			

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)
EC_SMB_CK1 EC_SMB_DA1	+3VLP_EC	BAT	0x16
		CHGR	0x12
EC_SML1CLK EC_SML1DATA	+3VALW_PRIM	GPU	0x9E

I2C Address Table

I2C Port	Power Rail	Device	Address (7 bit)
I2C 3	+3VALW_PRIM	Track Pad	0x2CH
I2C 5	+3VS	eDP Touch screen	TBC

USB2.0 Port Table

USB2.0 Port	Device
1	USB Type-C (MB)
2	NA
3	USB Type-A (MB)
4	USB Type-A (MB)
5	USB Type-C (IO Board)
6	NA
7	Finger print
8	Camera
9	eDP Touch Panel
10	NGFF WLAN+BT (KEY E)

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5
+20V_ADP_IN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+VCCIN	Core voltage for CPU	ON	OFF	OFF	OFF
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.05V_VCCST	Sustain voltage for CPU standby modes	ON	ON	ON	OFF
+1.05VS_VCCSTG	Gated sustain voltage for CPU standby modes	ON	OFF	OFF	OFF
		ON	OFF	ON	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.2V_VDDQ	DDR4/L-RS +1.2V power rail & CPU digital PLL	ON	ON	ON	OFF
+2.5V	DDR4/L-RS +2.5V power rail	ON	ON	ON	OFF
+1.8V_PRIM_SOC	TCSS/AGSH TypeC sub system / CPU analog power supply	ON	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*
+3V_PRIM	+3VALW power for PCH suspend rails	ON	ON	ON	ON*
+3VS	System +3VS power rail	ON	ON	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU	ON	OFF	OFF	OFF
+VGA_CORE	Power rail for GPU	ON	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*
+5VS	System +5VS power rail	ON	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

Compal Electronics, Inc.

Title: Notes List

Size: | Document Number: LA-K092P | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 3 of 102

Power Source name	Net Name	Location	power plane	Current (mA)
+19VB	+VCCIN	PQZ1、PQZ2		62000
	+VCCIN_AUX	PUG1		27000
	+VGA_CORE	PUV1		35000
	+1.35VSDGPU	PUW1		7500
	+1.2VP	PUM1		6920
	+0.6VSP	PUM1		1200
	+5VALWP	PU501		17000
	+3VALWP	PU301		10000
	+INVPWR_B+	LV1		2000
+0.6VSP	+0.6VS_VTT	PJ502		1200
+1.2V_VDDQ	+1.2V_VDDQ	PJM3		6920
+5VALWP	+5VALW	PJ501		17000
+5VALW	+USB3_VCC (TypeC)	UT6		3000
	+5VALW_USBA (USB3.0 port1)	UT10		2000
	+5VALW_USBB (USB3.0 port2)	US12		2000
	+5VALW (sub USB2.0)	JIO1		2000
	+5VS	UQ1		5200
	+FP_VCC	UK6		50
+5VS	+5VS_BL	U1		200
	+5VS_DISP	UV17		1000
	+5VS_HDD	RO3		1500
	+5VS_ODD	RO26		1400
	+VDDA (Codec)	JPA1		1500
	+VCC_FAN1	RF1		500
+3VALWP	+3VALW	PU301		10000
+3VALW	+3VS	UQ1		5136
	+3V_LAN	UL1		1500
	+3VALW_TPM	RW1		500
	+3VALW_PRIM	JPC7		500
	+3VALW_DSW	RC173		500
	+3V_PTP	UK1		500
	+3VS_WLAN	UM1		2000
	+1.8VALWP	PU1801		3000
	+FP_VCC	UK6		100
	+2.5V (DDR4)	PUM2		400
+3VS	+LCDVDD	UX1		1500
	+3VS_DVDD	RA5		60
	+3VS_SSD_NGFF (SSD)	RM9		2790
	+3VS_TPM	RW2		5
	+3VS_DVDDIO (Codec)	RA2		60
	+3VS(Camera)	JEDP1.35		200
+1.8VALWP	+1.8VALW_PRIM	PU1801		2000
+1.8VALW_PRIM	+1.8VSDGPU_AON	UV16		1000
	+1.8VSDGPU_MAIN	UV16		1000
	+1.8VALW_PRIM (CPU)			930
	+1.8VS	UC5		500
+1.8VS	+1.8VS_VDDA (Codec)	RA6		30
+1.0V5ALW	+1.05VO_OUT_FET (VCCST & VCCSTG)			3000

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2019/09/20	Deciphered Date 2020/12/31	Title: Power MAP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Document Number: LA-K092P; Rev: 0.1
			Date: Thursday, May 06, 2021; Sheet 4 of 102

[FH5AT-PWR Sequence_TGL-UP3_DDR4_Volume_S0iX] BIOS / EC : 016

G3 > S0 > S5 OK, S0iX what for BIOS update

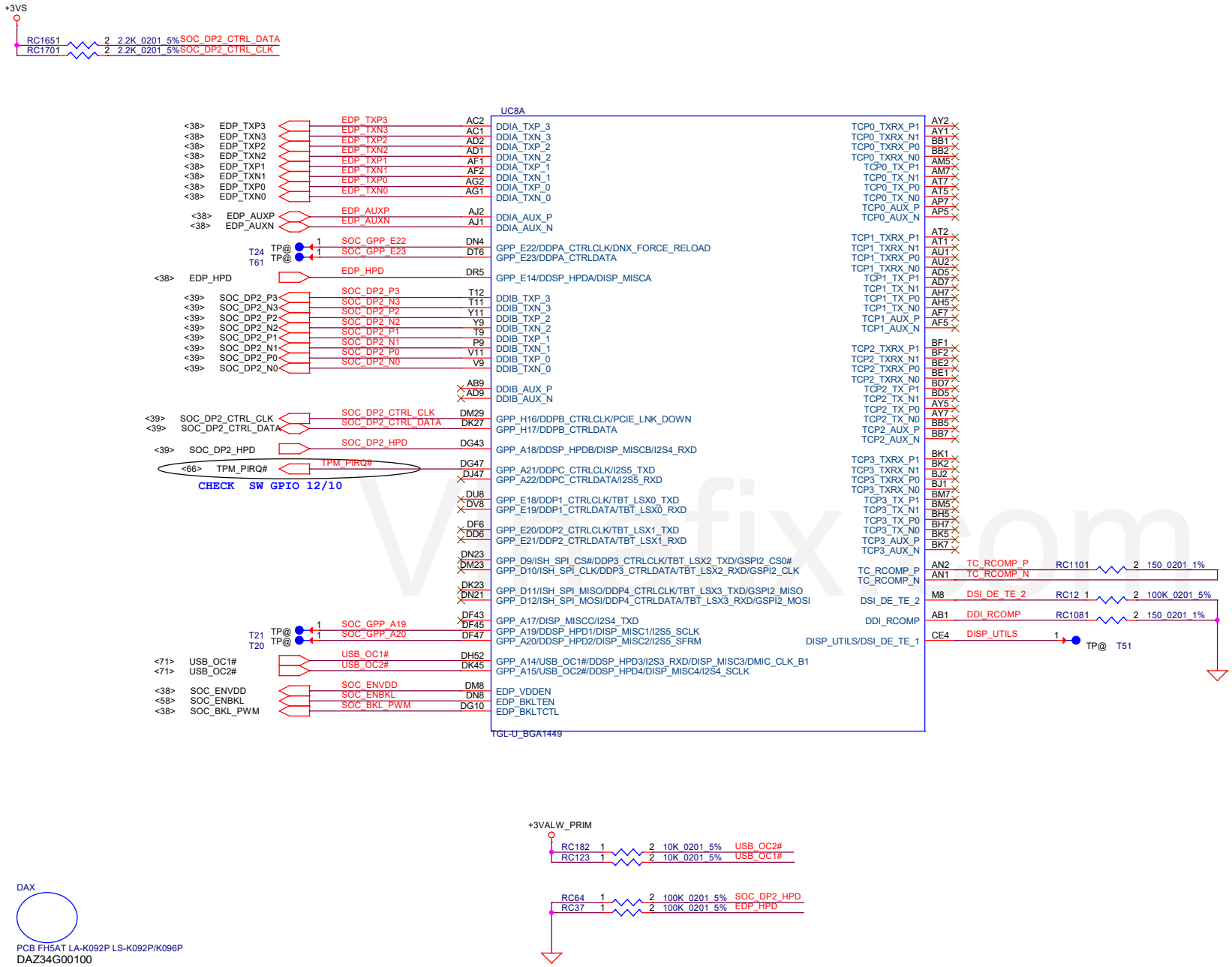
G3->S0 | S0-> S0iX | S0iX ->S0 | S0->S5

Compal Electronics, Inc.

Title: Power Sequence

Size | Document Number: LA-K092P | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 5 of 102

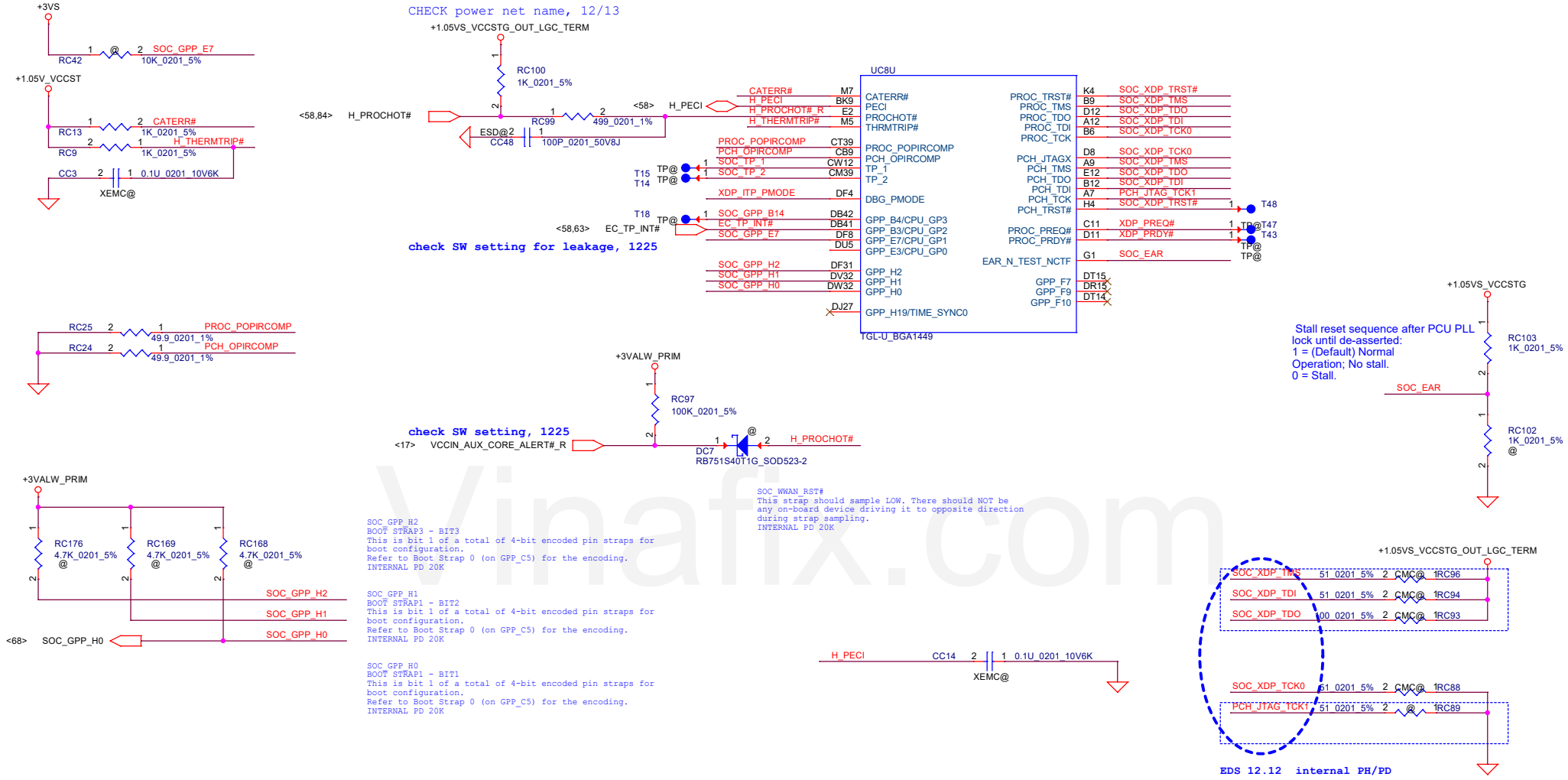


Compal Electronics, Inc.

Title: TGL-UP3(1/14)DDI,EDP

Size: | Document Number: LA-K092P | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 6 of 102

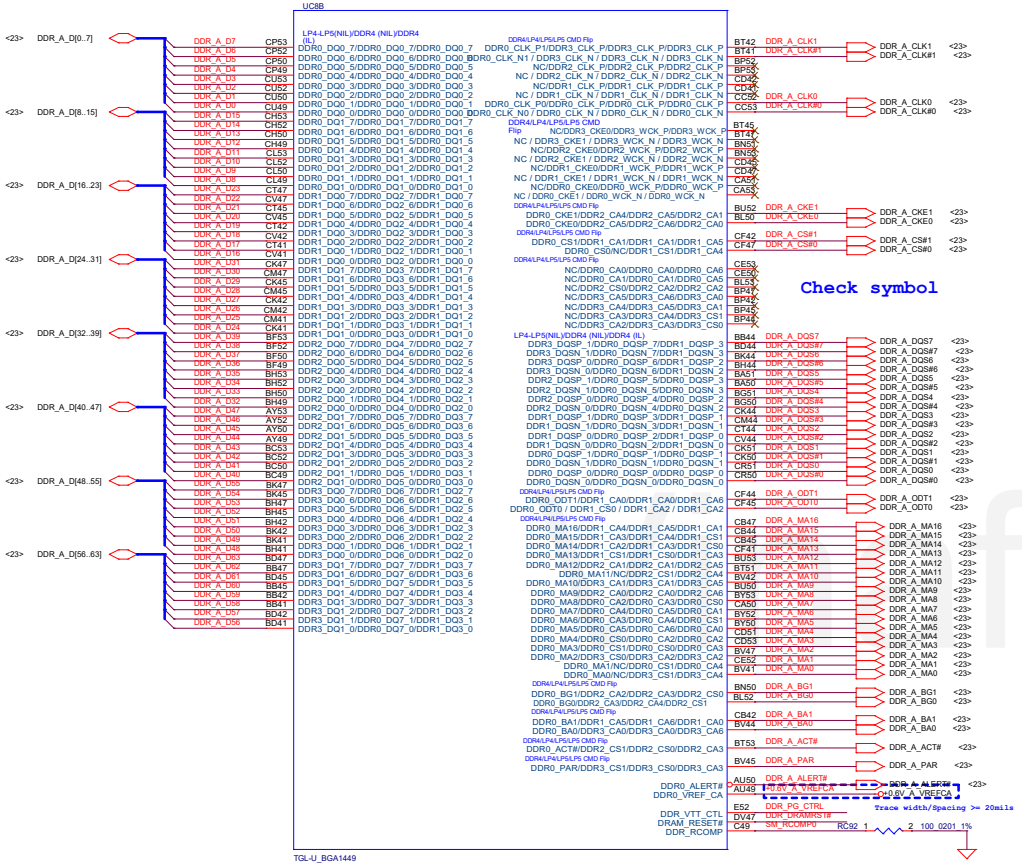


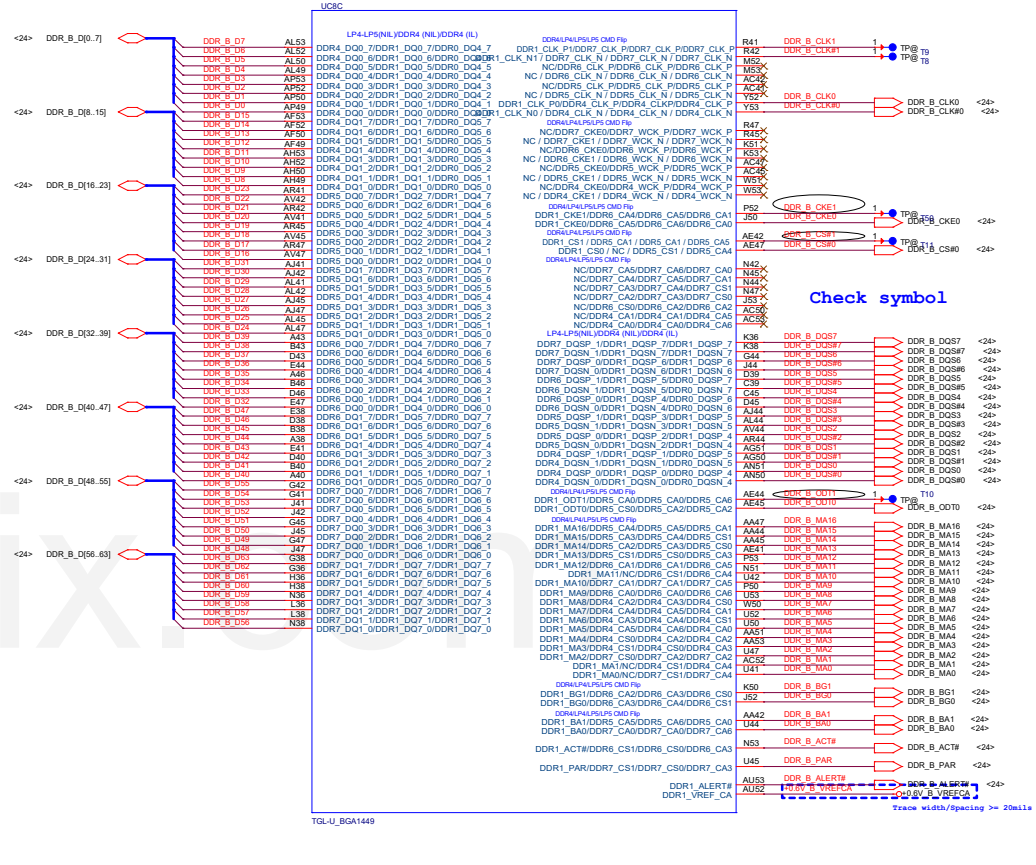
Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

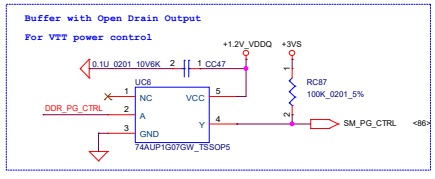
Compal Electronics, Inc.			
Title	TGL-UP3(1/14)DDI,MSIC,XDP		
Size	Document Number LA-K092P		Rev 0.1
Date: Thursday, May 06, 2021	Sheet 7 of 102		

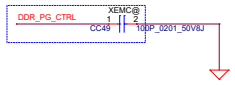
Follow Intel DDR4 NIL

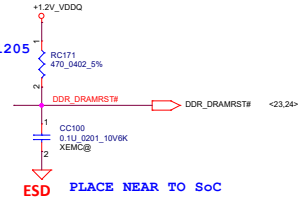
DDR4: Refer to 609003_TGL_U_DDR4_SODIMM_RVP_SCH_REV0p5











Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

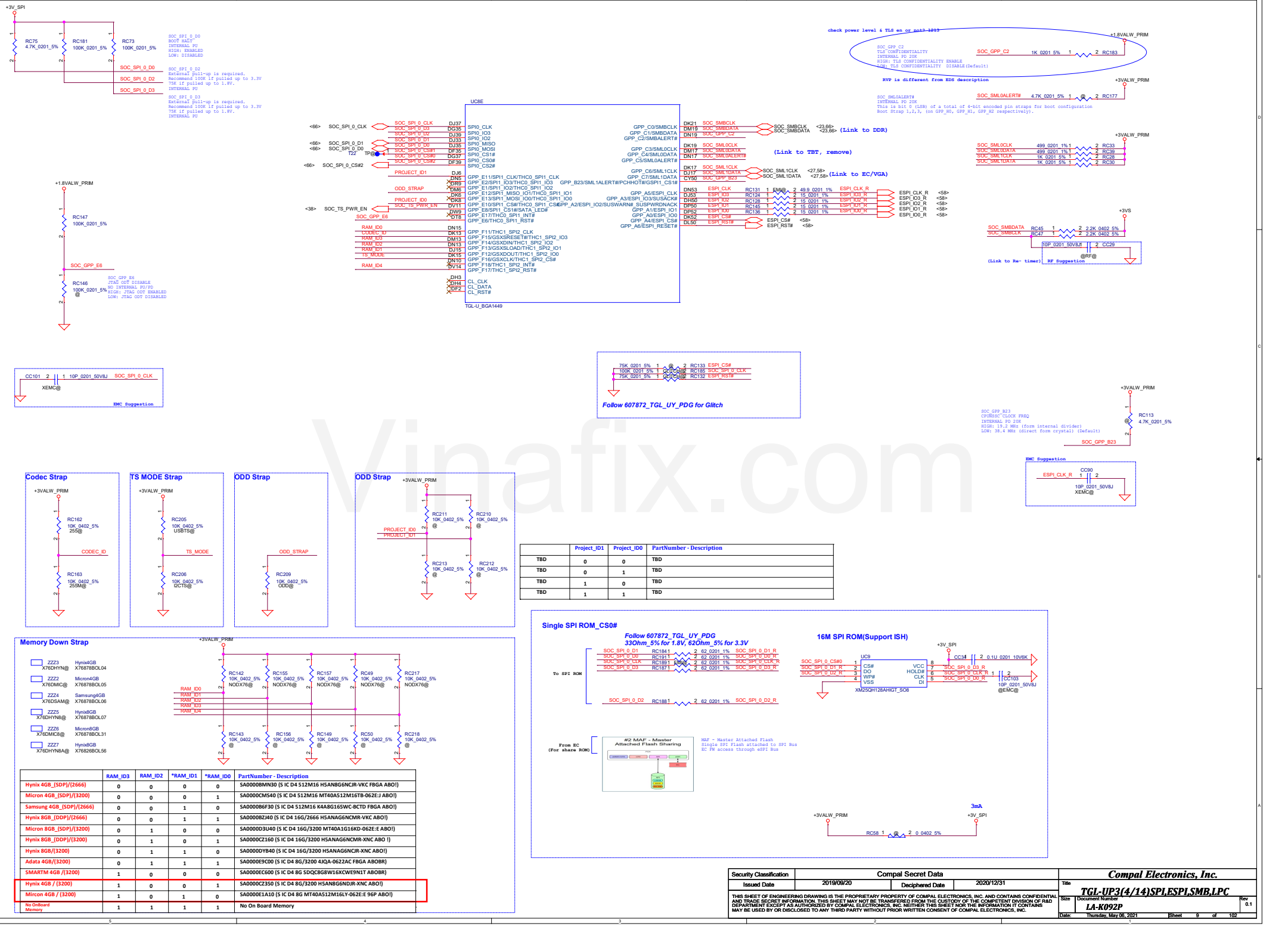
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: **TGL-UP3(3/14)DDR4**

Size: | Document Number: **LA-K092P** | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 8 of 102

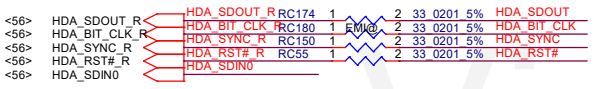


	Project_ID1	Project_ID0	PartNumber - Description
TBD	0	0	TBD
TBD	0	1	TBD
TBD	1	0	TBD
TBD	1	1	TBD

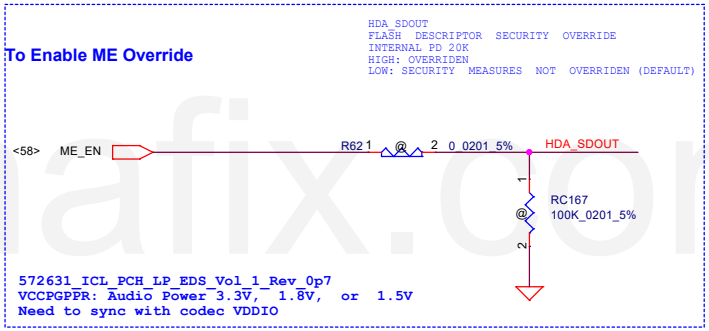
	RAM_ID3	RAM_ID2	*RAM_ID1	*RAM_ID0	PartNumber - Description
Hynix 4GB_(SDP)/(2666)	0	0	0	0	SA0000BMN30 (S IC D4 512M16 H5AN8G6NCJR-VKC FBGA ABO!)
Micron 4GB_(SDP)/(3200)	0	0	0	1	SA0000CMS40 (S IC D4 512M16 MT40A512M16TB-062E:J ABO!)
Samsung 4GB_(SDP)/(2666)	0	0	1	0	SA0000B6F30 (S IC D4 512M16 K4A8G165WC-BCTD FBGA ABO!)
Hynix 8GB_(DDP)/(2666)	0	0	1	1	SA0000BZJ40 (S IC D4 16G/2666 H5ANAG6NCMR-VKC ABO!)
Micron 8GB_(SDP)/(3200)	0	1	0	0	SA0000D3U40 (S IC D4 16G/3200 MT40A1G16KD-062E:E ABO!)
Hynix 8GB_(DDP)/(3200)	0	1	0	1	SA0000CZ160 (S IC D4 16G/3200 H5ANAG6NCMR-XNC ABO !)
Hynix 8GB/(3200)	0	1	1	0	SA0000DYB40 (S IC D4 16G/3200 H5ANAG6NCJR-XNC ABO!)
Adata 4GB/(3200)	0	1	1	1	SA0000E9C00 (S IC D4 8G/3200 4JQA-0622AC FBGA ABOBR)
SMARTM 4GB /(3200)	1	0	0	0	SA0000EC600 (S IC D4 8G SDQC8G8W16XCWE9N1T ABOBR)
Hynix 4GB / (3200)	1	0	0	1	SA0000CZ350 (S IC D4 8G/3200 H5AN8G6NDJR-XNC ABO!)
Mircon 4GB / (3200)	1	0	1	0	SA0000E1A10 (S IC D4 8G MT40A512M16LY-062E:E 96P ABO!)
No OnBoard Memory	1	1	1	1	No On Board Memory

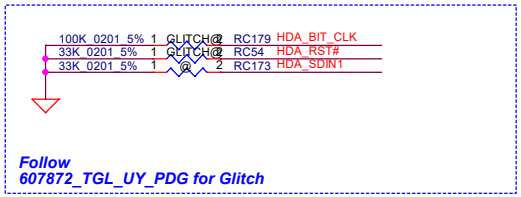
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2019/09/20	Deciphered Date 2020/12/31	Title: TGL-UP3(4/14)SPI,ESPI,SMB,LPC
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Document Number: LA-K092P Rev: 0.1
			Date: Thursday, May 06, 2021 Sheet 9 of 102

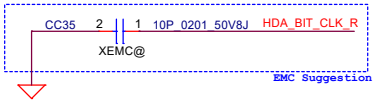
HDA for AUDIO



To Enable ME Override







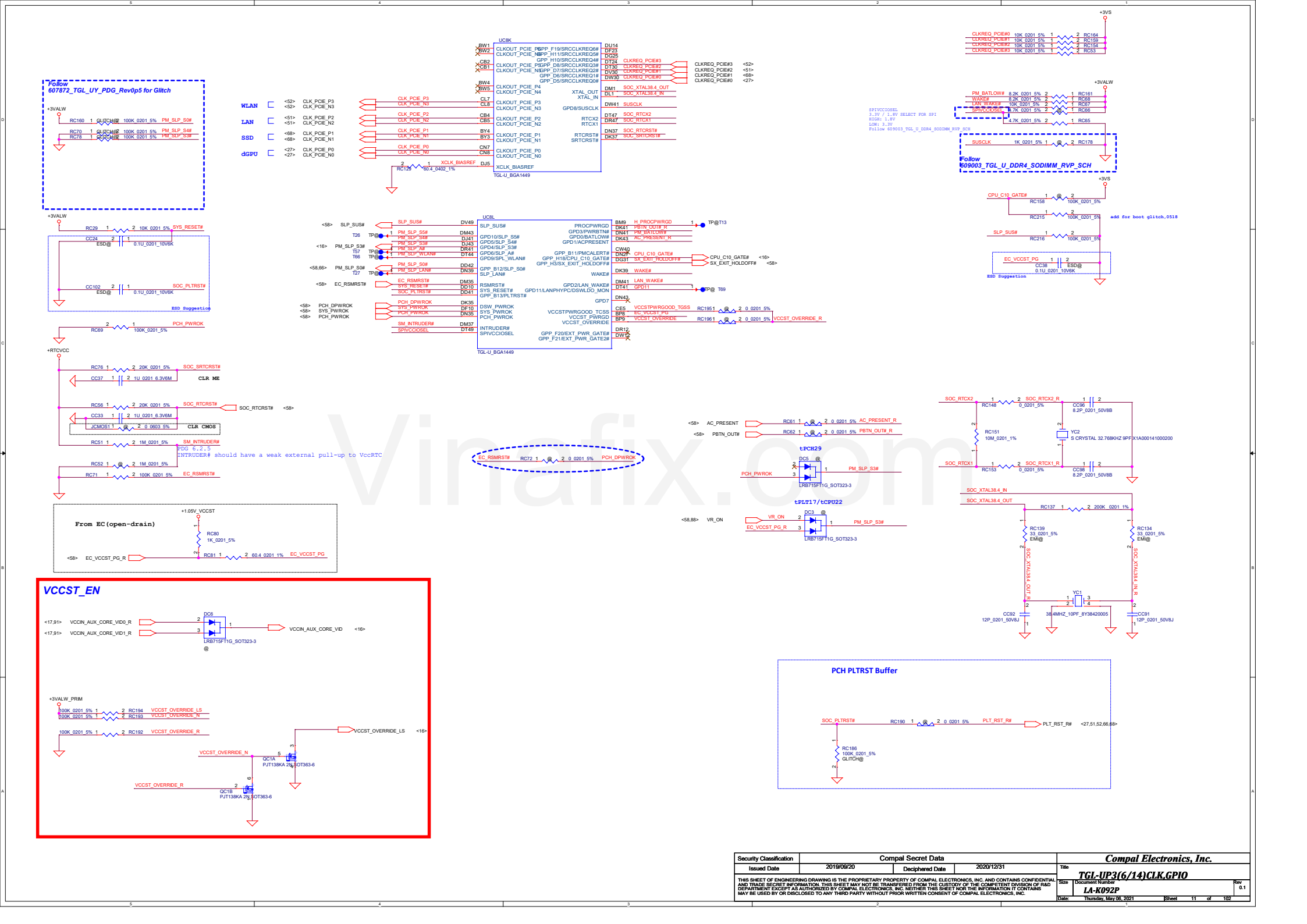
Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: TGL-UP3(5/14)HDA,SNDW

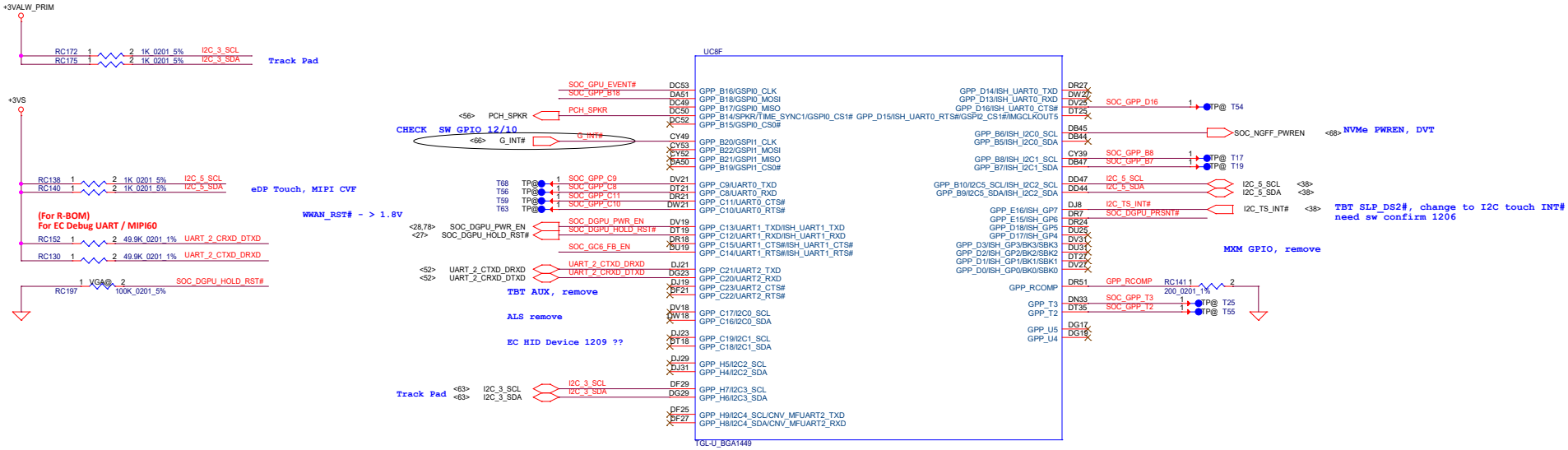
Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 Sheet 10 of 102

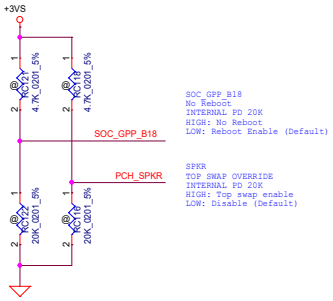


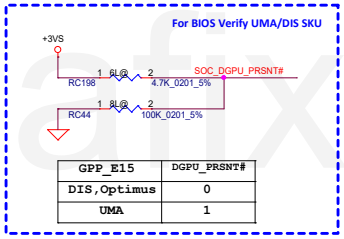
Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.	
Title	TGL-UP3(6/14)CLK,GPIO
Size	Document Number: LA-K092P
Rev	0.1
Date:	Thursday, May 06, 2021
Sheet	11 of 102



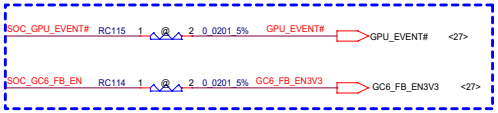
Strap Pin





GPP_E15	DGPU_PRSNT#
DIS,Optimus	0
UMA	1

to dGPU Connect to SOC GPIO



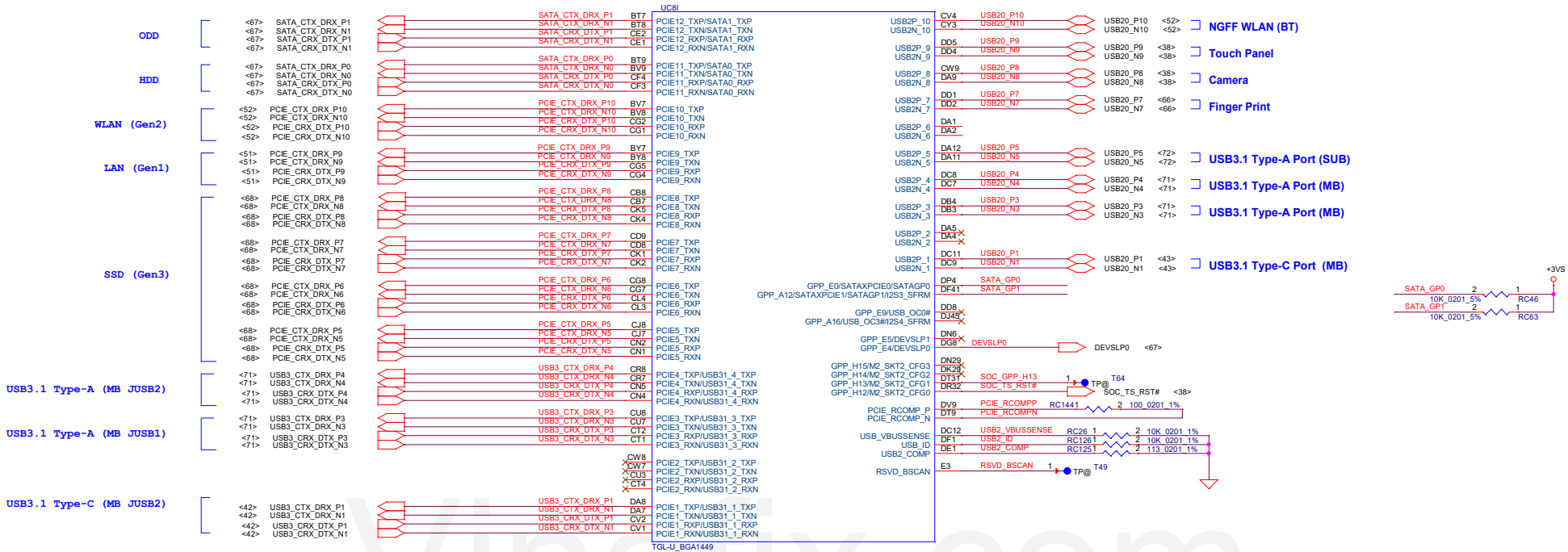
Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: TGL-UP3(7/14)GPIO

Size: C | Document Number: LA-K092P | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 12 of 102



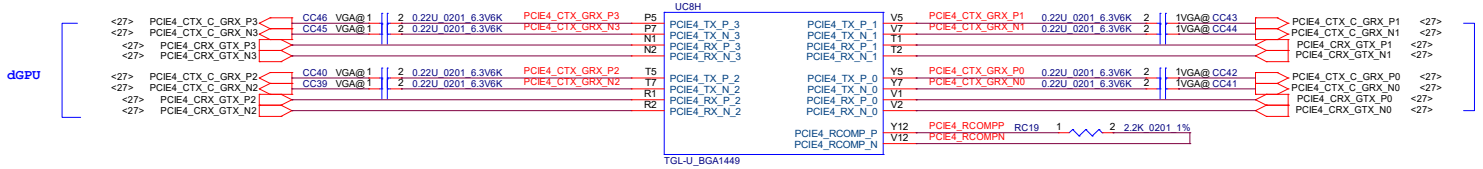
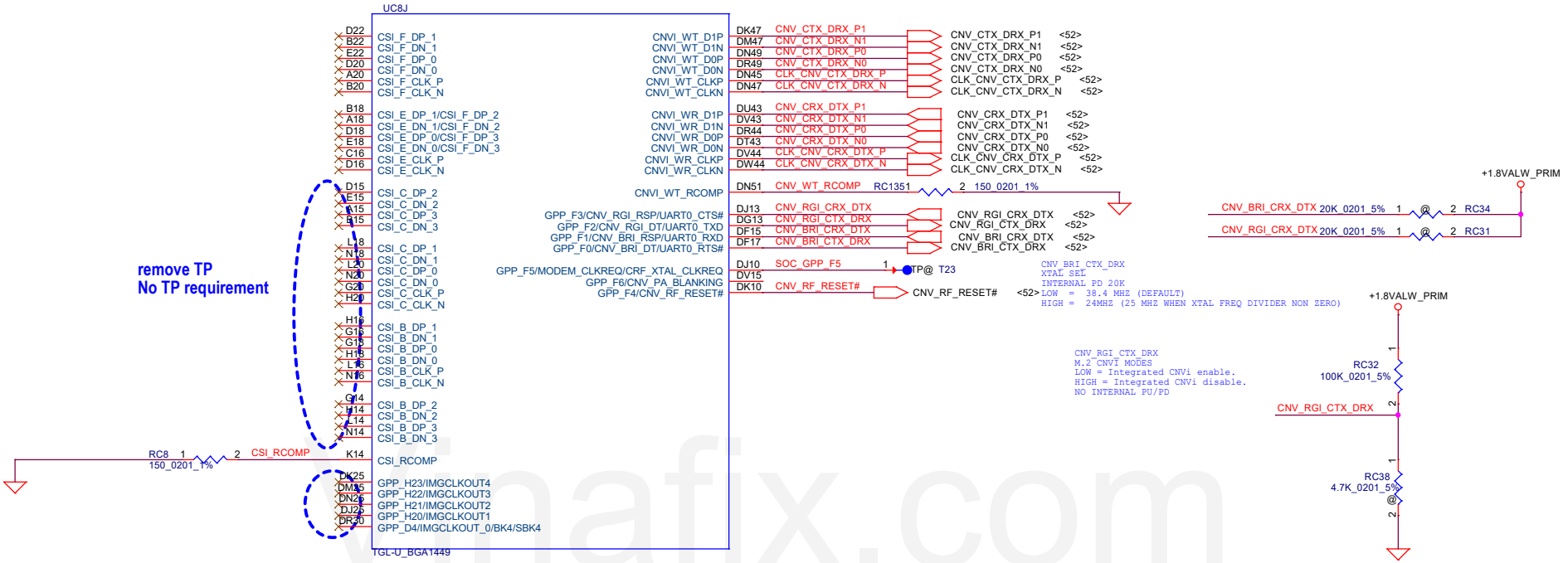


Table 58. Signal Descriptions

Name	Type	SSC Capable	Description
PCH-LP (U): • CLKOUT_PCIE_P[6:0] • CLKOUT_PCIE_N[6:0] PCH-LP (Y): • CLKOUT_PCIE_P[6:1] • CLKOUT_PCIE_N[6:1]	O	Yes	**PCI Express* Clock Output**: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices • CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1/2/3 support • CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2019/09/20	Deciphered Date 2020/12/31	Title: TGL-UP3(8/14)PCIE,USB,SATA
			Size: LA-K092P; Document Number; Rev 0.1
			Date: Thursday, May 06, 2021; Sheet 13 of 102



Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

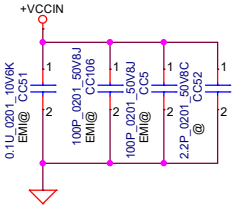
Title: TGL-UP3(9/14)CSI,CNV

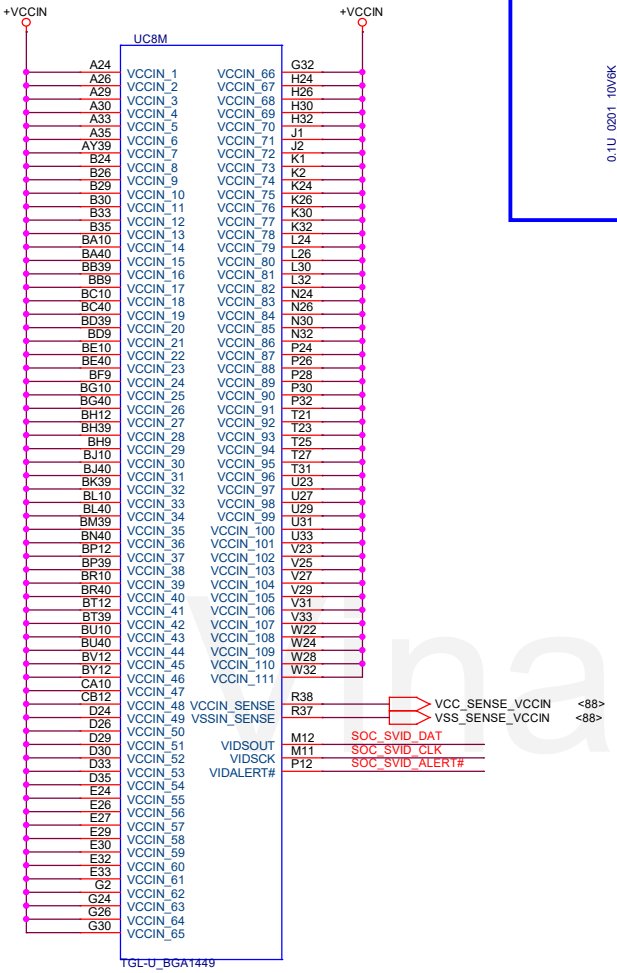
Size | Document Number: LA-K092P | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 14 of 102

Package size?

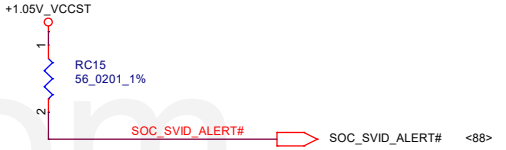
EMC CAPS-PLACE
< 5mm from SOC VCCIN



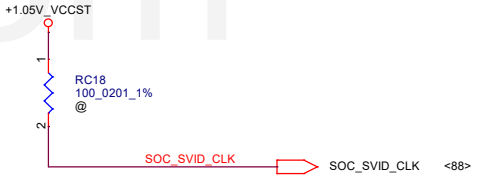


SVID DATA

SVID ALERT



SVID CLOCK

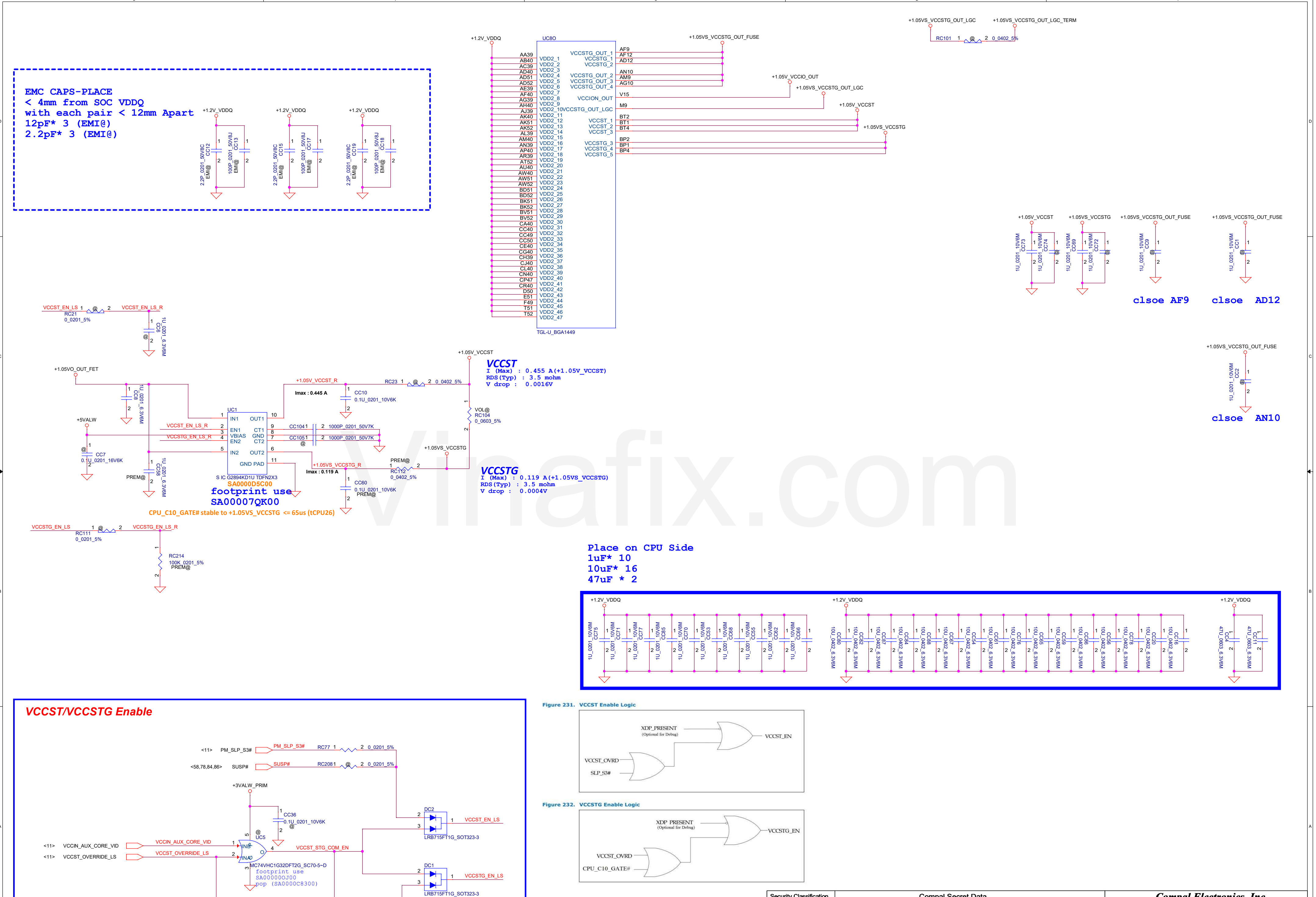


Compal Electronics, Inc.

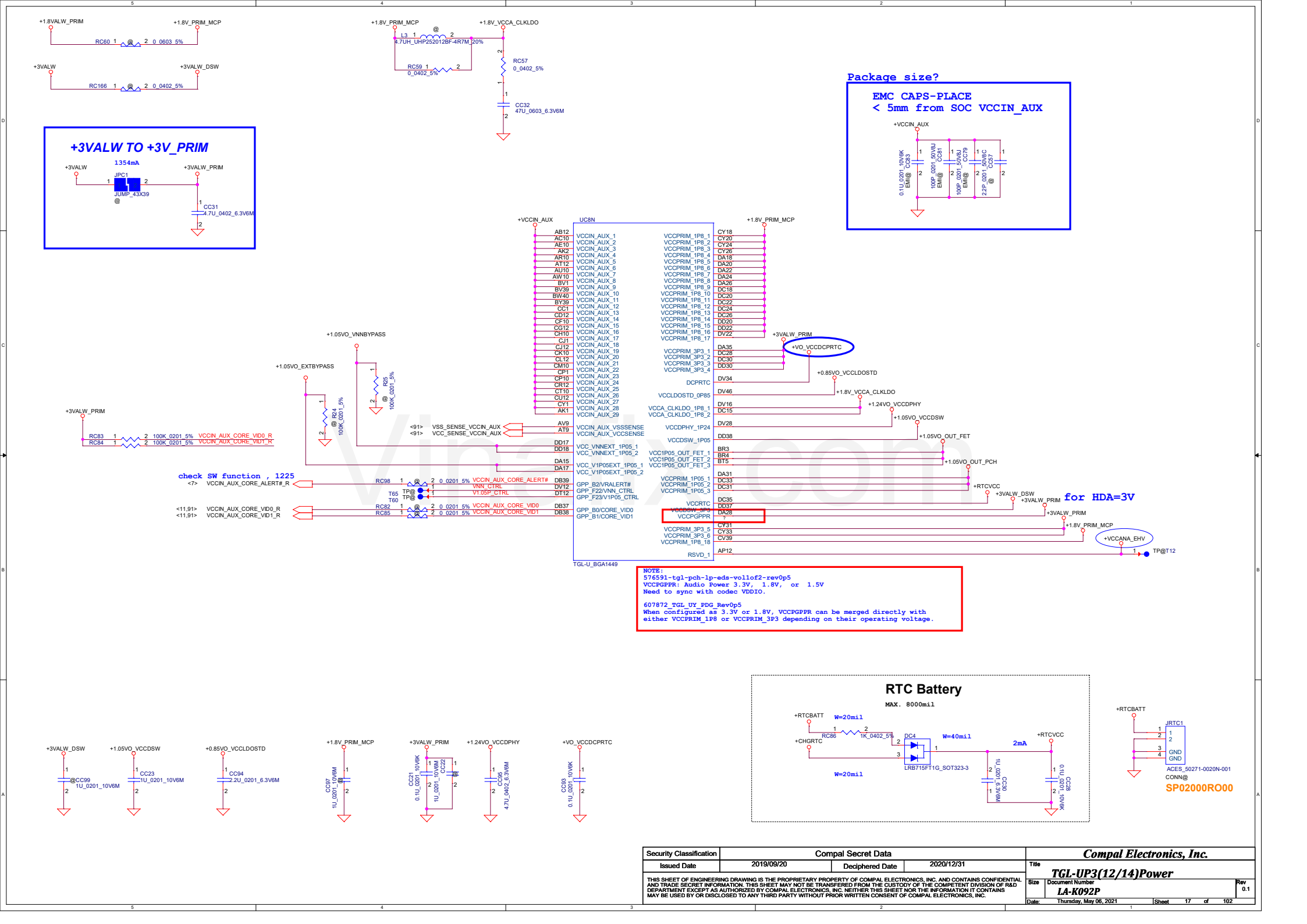
Title: TGL-UP3(10/14)Power, SVID

Size | Document Number: LA-K092P | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 15 of 102



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2019/09/20	Deciphered Date	2020/12/31	Title: TGL-UP3(11/14)Power
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number: LA-K092P; Rev 0.1
				Date: Thursday, May 06, 2021; Sheet 16 of 102



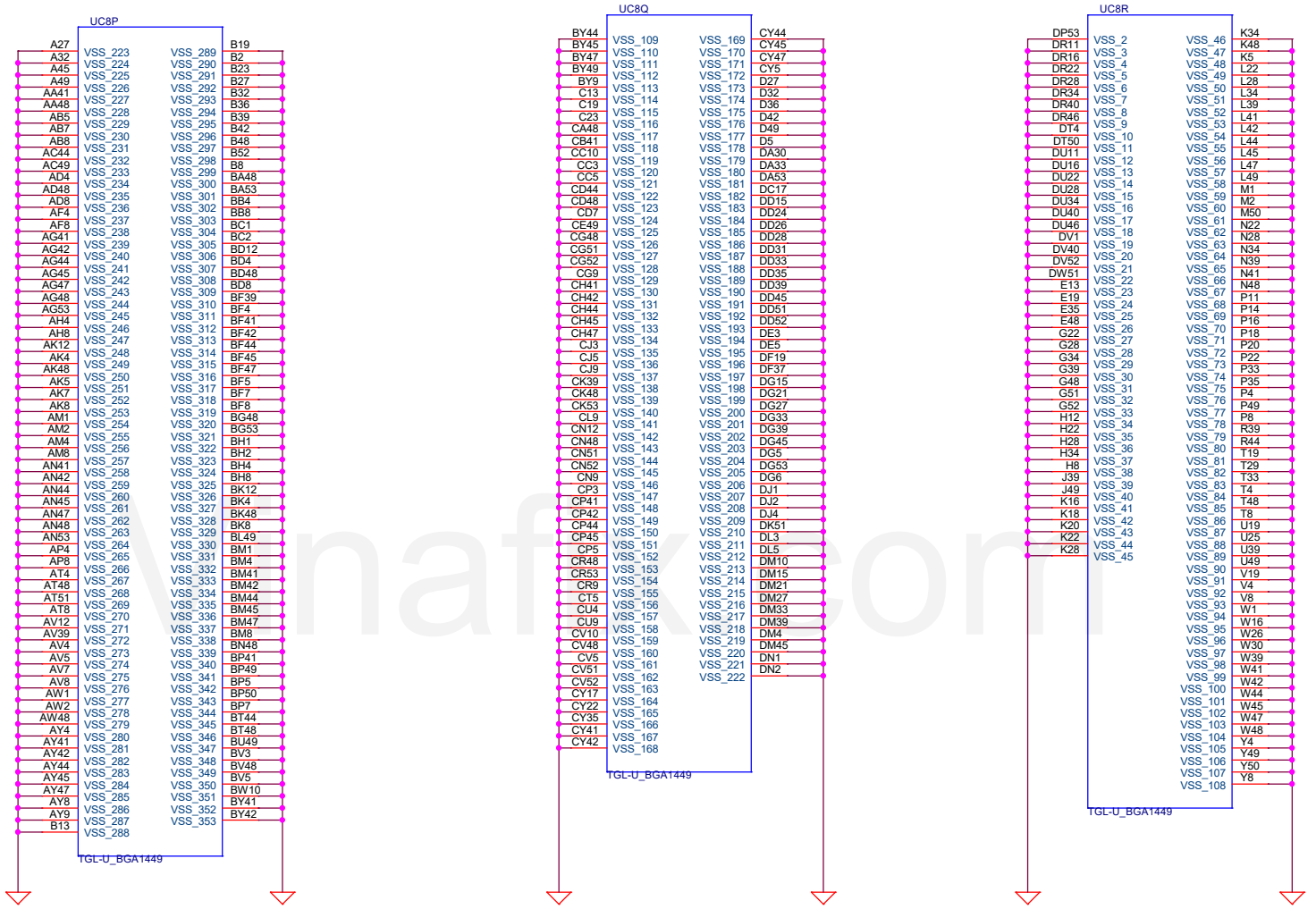
Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **TGL-UP3(12/14)Power**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 Sheet 17 of 102



Compal Electronics, Inc.

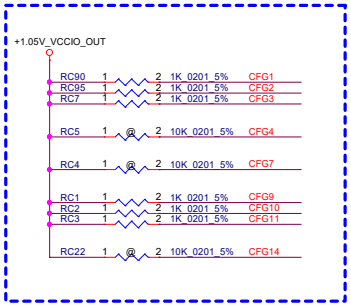
Title: TGL-UP3(13/14)GND

Size | Document Number: LA-K092P | Rev: 0.1

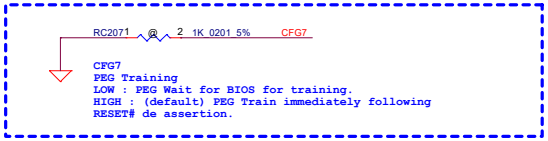
Date: Thursday, May 06, 2021 | Sheet 18 of 102

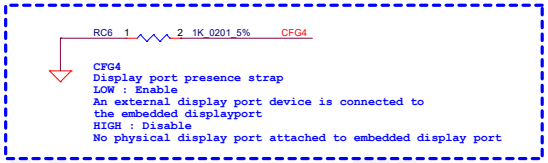
CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

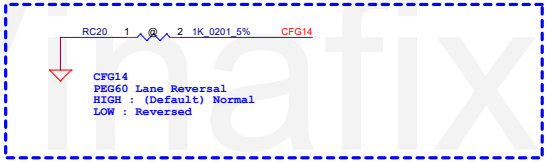
CFG Signals have int. PH 3K ohm.

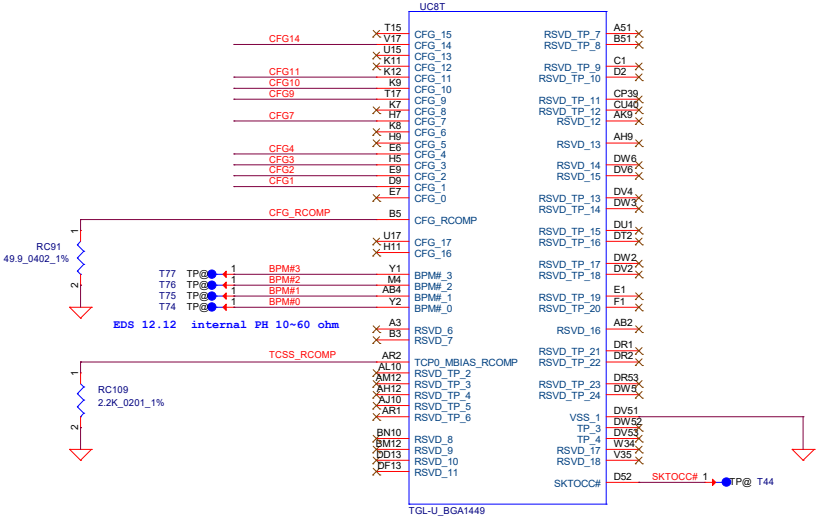


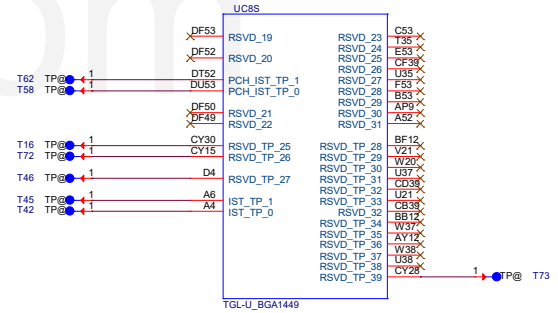
CFG Signals
(For Strap & XDP)











Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: TGL-UP3(14/14)RSVD,CFG

Size | Document Number: LA-K092P | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 19 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for SOC/PCH/FCH**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 20 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for SOC/PCH/FCH**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 21 of 102

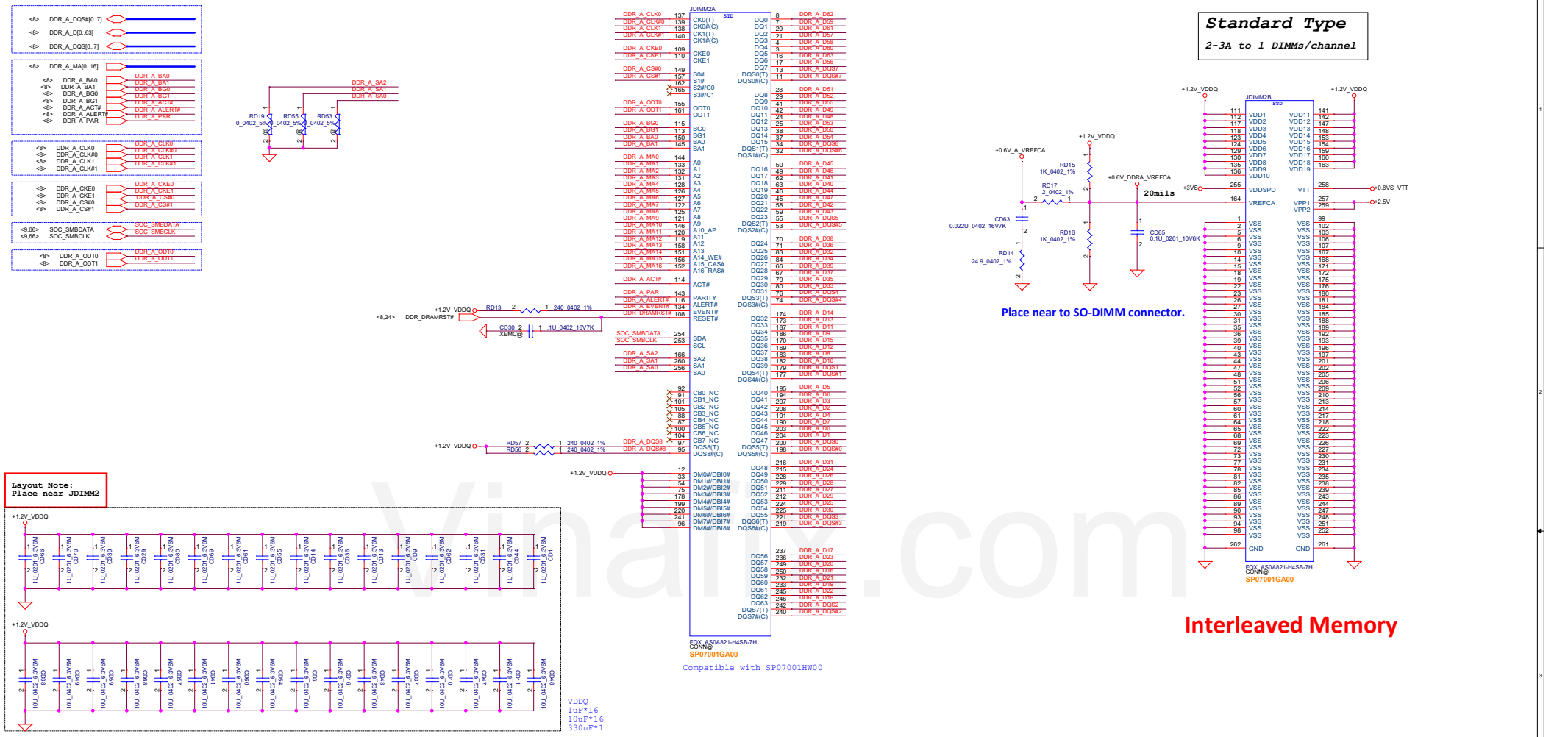
Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for SOC/PCH/FCH**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 22 of 102



Refer for DDR4 SO-DIMM Decoupling Caps
607872_TGL_UY_PDG_Rev0p5

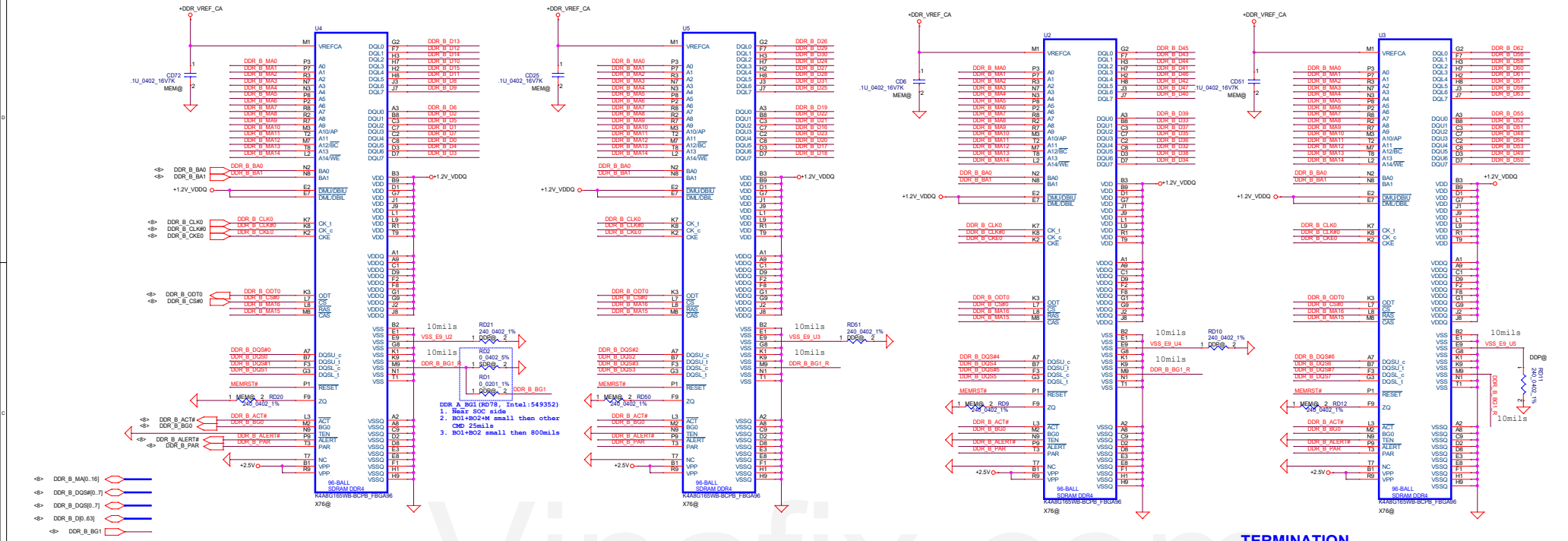
Table 50. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 SODIMM 1DPC	VDDQ/VDD	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)
		placeholder	1x 330µF (7343)
	VTT	Place on VTT plane close to DIMM 1 cap stuffed, 1 placeholder	2x 10µF (0603)
		Place on VTT plane close to DIMM	4x 1µF (0402)
	VPP	DIMM pin side, 1 per DIMM	2x 10µF (0603)
		DIMM pin side, 1 per DIMM	2x 1µF (0402)
	VDDSPD	1 cap per DIMM. Place close to DIMM	2x 0.1µF (0402)
		1 cap per DIMM. Place close to DIMM	2x 2.2µF (0402)

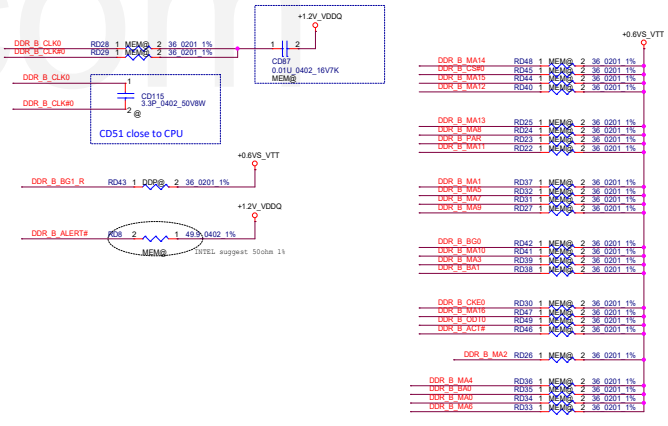
Note: 1. Total quantity is referring to 2 channels.

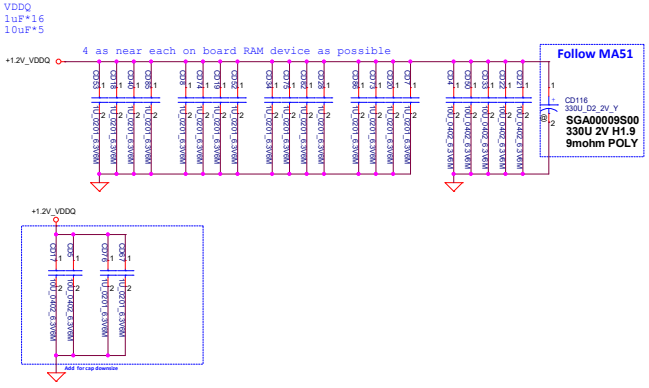
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/12/27	Deciphered Date 2019/12/27	Title: DDR4 DIMMB
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Custom; Document Number: LA-K092P; Rev: 0.1
			Date: Thursday, May 06, 2021; Sheet 23 of 102

change SDP footprint

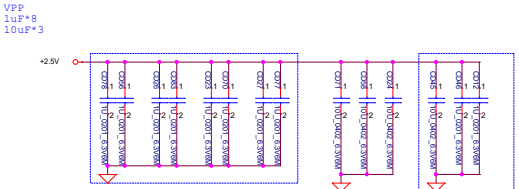


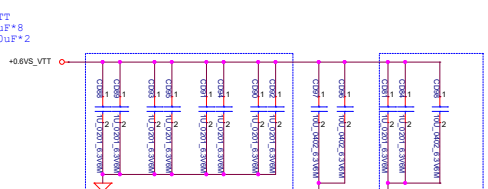
TERMINATION





DDR4 mapping	SDP	DDP
E9	VSS	UZQ
M9	VSS	BG1
T7	NC	VSS
RCOMP[0] (SOC side)	200_1%	121_1%





Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.	
Title	DDR4 ON BOARD CHIPS
Size / Document Number	FH5LI M/B LA-H801P
Rev	0.1
Date: Thursday, May 06, 2021	Sheet 24 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for DDR2**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 25 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for DDR3**

Size | Document Number: **LA-K092P** | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 26 of 102

N17 GPU		
GPIO	I/O	USAGE
GPIO0	O	PWM_VID
GPIO1	O	GC6_FB_EN
GPIO2	I	GPU_EVENT#
GPIO3	I/O	NVVDDS_PWM
GPIO4	O	1V8_MAIN_EN
GPIO5	I	FRAME_LOCK#
GPIO6	O	PSI
GPIO7	O	LCD_BL_PWM
GPIO8	O	MEM_VDD_CTL
GPIO9	I/O	THERM_ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	LCD_VDD
GPIO12	I	PWR_LEVEL
GPIO13	O	LCD_BLEN
GPIO14	I	HPD_IFPA
GPIO15	I	HPD_IFPB
GPIO16		Reserved
GPIO17	I	HPD_IFPD
GPIO18	I	HPD_IFPE
GPIO19	O	3D_VISION
GPIO20		Reserved
GPIO21		Reserved (OC_WARN)
GPIO22		Reserved
GPIO23		Reserved

UGPU1A

Part 1 of 6

PCI EXPRESS

GPIO

DACs

I2C

CLK

N18S-G5-A1_FCBGA603

change to N18S footprint

DA-08329-001_V02

Table 8. Other PLLs Power Decoupling and Filtering

GPU	Type	Footprint	Population N16	Population N17	Location
PLLVDD (N17: XS_PLLVDD) Supply Rail					
GB2B-64, GB2C-64	0.1 µF X7R	0402	1	1	Under GPU
	22 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L2=30 Ω (ESR=0.05 Ω)	0402	1	0	Near GPU
SP_PLLVDD and VID_PLLVDD Combined Supply Rails					
GB2B-64, GB2C-64	0.1 µF X7R	0402	2	2	Under GPU
	10 µF X5R	0603	1	0	Near GPU
	47 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L2=300 Ω (ESR=0.2 Ω)	0603	1	0	Near GPU

2016/11/10
C2007 change to 22uF
1. NV reference design
2. Top side only 1.2mm high

SM010008A00
3000ma 30ohm@100mhz DCR 0.03

CO-LAY N18S

under GPU

GC6 2.0 function

Table 15-8. I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

Crystals must have a max ESR of 80 ohm

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

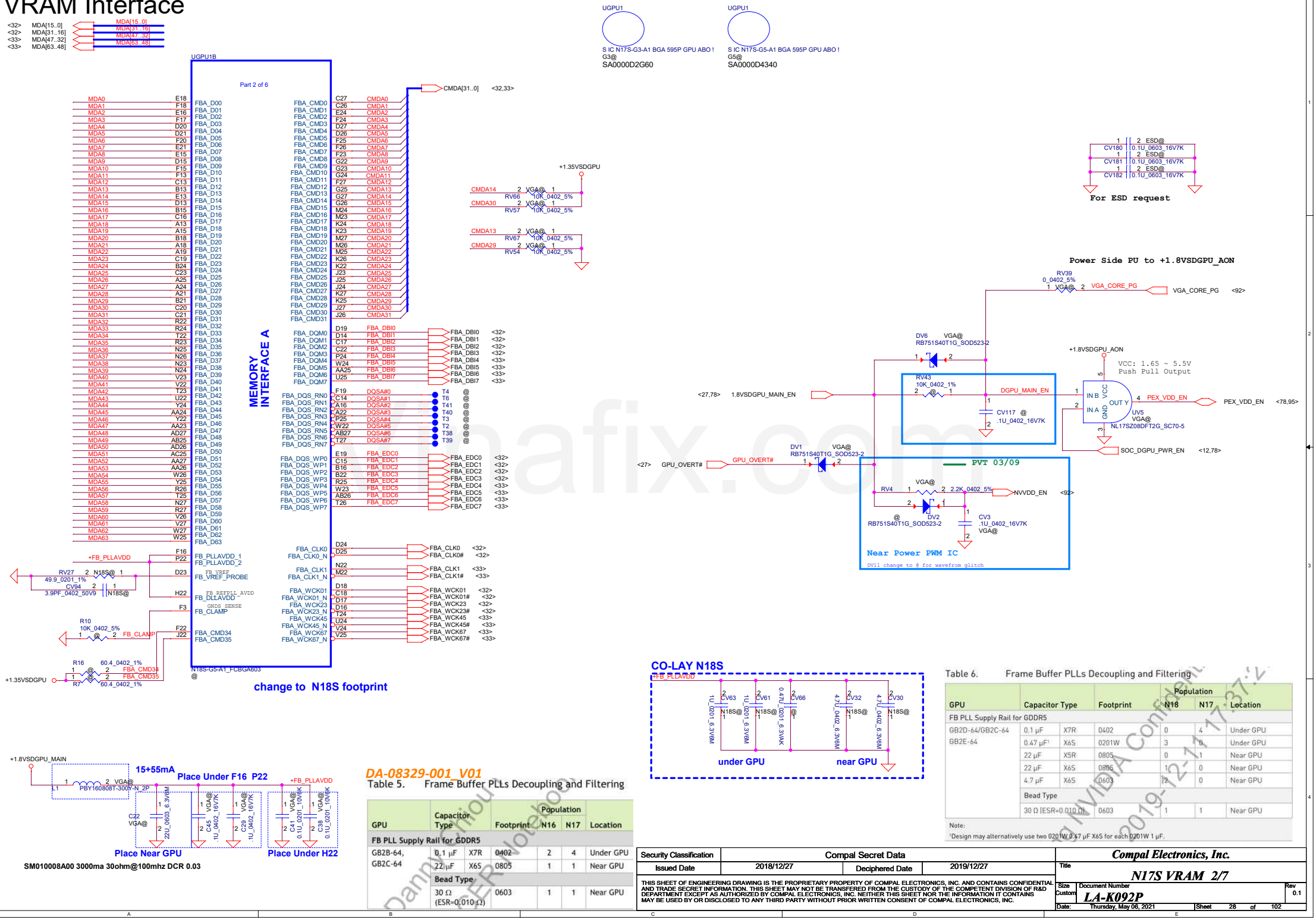
Compal Electronics, Inc.

Title: N17S PEG 1/7

Size: Custom | Document Number: LA-K092P | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 27 of 102

VRAM Interface



DA-08329-001_V01

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
Bead Type						
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

Table 6. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N18	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2D-64/GB2C-64	0.1 µF	X7R	0402	0	4	Under GPU
GB2E-64	0.47 µF[1]	X6S	0201W	3	0	Under GPU
	22 µF	X5R	0805	0	1	Near GPU
	22 µF	X6S	0805	1	0	Near GPU
	4.7 µF	X6S	0603	2	0	Near GPU
	Bead Type					
	30 Ω [ESR=0.010 Ω]		0603	1	1	Near GPU

Note:
[1]Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

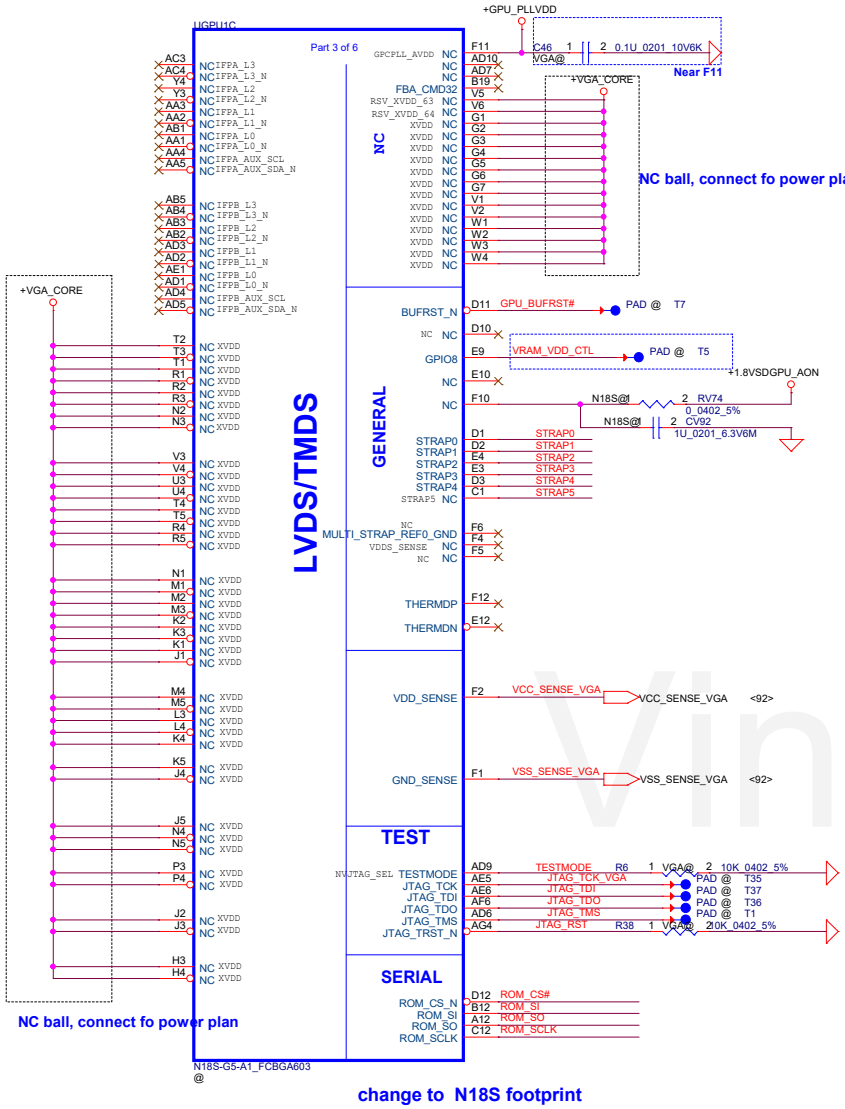
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

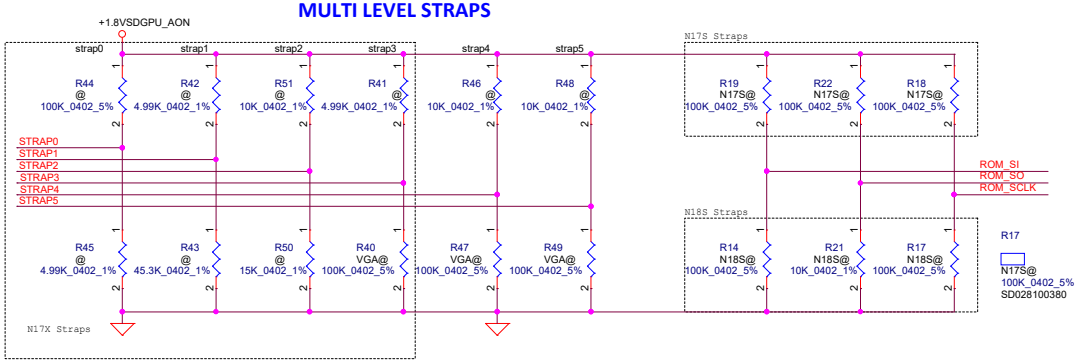
Title: N17S VRAM 2/7

Size: Custom | Document Number: LA-K092P | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 28 of 102



MULTI LEVEL STRAPS



Multi strap table — **MX330/350 Decive ID : N17S-G3/G5-A1 0x1D16/0x1C94**

GPU	VRAM Voltage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	strap5	ROM_SI	ROM_SO	ROM_SCLK
N17S-G3	+1.35V	SR	X76878BOL02	3.5GHz	256Mx32x2 2G	0x9 (SA00009TI60) Micron MT51J256M32HF-80:B	PD 100K	PU 100K PD 100K	PD 100K						
			X76878BOL01			0xA (SA0000C1700) Hynix H5GC8H24AJR-R2C	PU 100K	PU 100K PD 100K	PD 100K						
			X76878BOL03			0x3 (SA00009TA40) Samsung K4G80325FC-HC25	PU 100K	PU 100K	PD 100K						
N17S-G5	+1.35V	SR	X76878BOL02	3.5GHz	256Mx32x2 2G	0x9 (SA00009TI60) Micron MT51J256M32HF-80:B	PD 100K	PU 100K PD 100K	PD 100K						
			X76878BOL01			0xA (SA0000C1700) Hynix H5GC8H24AJR-R2C	PU 100K	PU 100K PD 100K	PD 100K						
			X76826BOLA1			0xB (SA00009TA40) Samsung K4G80325FC-HC25	PU 100K PD 100K	PU 100K	PD 100K						
N18S-G5	+1.35V	SR	X76878BOL09	3.5GHz	256Mx32x2 2G	0x1 (SA00009TI60) Micron MT51J256M32HF-80:B	PU 100K	PD 100K PU 100K	PD 100K PD 100K						
			X76878BOL08			0x2 (SA0000C1700) Hynix H5GC8H24AJR-R2C	PD 100K	PD 100K	PD 100K						
			X76878BOL10			0x4 (SA00009TA40) Samsung K4G80325FC-HC25	PD 100K	PD 100K	PU 100K						

PD 100K | PU 100K | PU 100K | PU 100K PD 100K | PD 100K | PD 10K | PD 100K

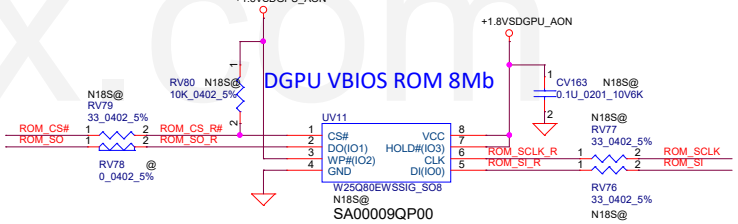


Table 12.3 RAMCFG

Strap Pins (see Note)			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 13. N18S-G5 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x1	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0x2	8 Gbps	N/A	Full	Production candidate
			Samsung	K4G80325FC-HC25	C-die	0x4	8 Gbps	N/A	Full	Production candidate

Table 6. N17S-G0/G2/G3/G4 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FC-HC25	C-die	0x3	8 Gbps	N/A	Full	Post-production ready

Table 4. N17S-G5/LP GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production candidate
			Samsung	K4G80325FC-HC25	C-die	0xB	8 Gbps	N/A	Full	Production candidate

DA-08329-001_V02

Table 8. Other PLLs Power Decoupling and Filtering

GPU	Type	Footprint	Population N16	Population N17	Location
PLLVDD (N17: XS_PLLVDD) Supply Rail					
GB2B-64, GB2C-64	0.1 µF X7R	0402	1	1	Under GPU
	22 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L=30 Ω (ESR=0.05 Ω)	0402	1	0	Near GPU
SP_PLLVDD and VID_PLLVDD Combined Supply Rails					
GB2B-64, GB2C-64	0.1 µF X7R	0402	2	2	Under GPU
	10 µF X5R	0603	1	0	Near GPU
	47 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L=300 Ω (ESR=0.2 Ω)	0603	1	0	Near GPU
NC (N17: GPCPLL_AVDD) Supply Rail					
GB2C-64	0.1 µF X7R	0402	N/A	1	Under GPU
	4.7 µF X6S	0603	N/A	1	Near GPU
	22 µF X6S	0805	N/A	1	Near GPU
	Bead Type				
	L=30 Ω (ESR=0.010 Ω)	0603	N/A	1	Near GPU

NV 17S DG-07785-001_V07

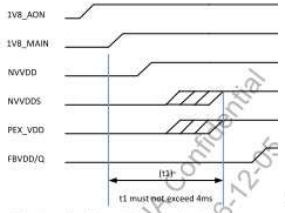


Figure 7.5 Example of Power-Up Sequencing Order

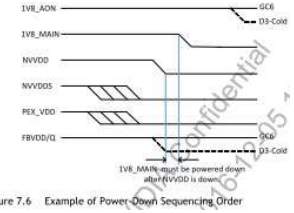


Figure 7.6 Example of Power-Down Sequencing Order

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: N17S LVDS 3/7

Size: Custom | Document Number: LA-K092P | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 29 of 102

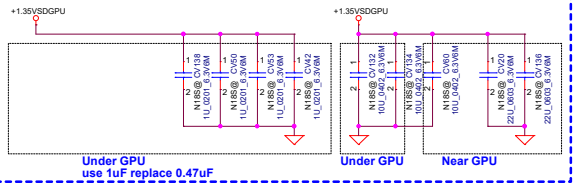
Table 5. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N18	Population N17	Location
FBVDD/Q Supply Rail for GDDR5						
GB2D-64/GB2C-64 GB2E-64	0.47 µF[1]	X6S	0201W	24	0	Under GPU
	1 µF[1]	X6S	0402 or 0201W	0	8	Under GPU
	10 µF	X6S	0603	4	2	Under GPU
	10 µF	X6S	0603	2	1	Near GPU
	22 µF	X6S	0603	5	3	Near GPU

PEX_HVDD Supply Rail						
GB2D-64/GB2C-64 GB2E-64	1.0 µF[1]	X6S	0402 or 0201W	0	4	Under GPU
	0.47 µF[1]	X6S	0201W	13	0	Under GPU
	4.7 µF	X6S	0603	0	2	Near GPU
	4.7 µF	X6S	0603	3	0	Under GPU
	10 µF	X6S	0805	0	2	Midway between GPU and power supply
	10 µF	X6S	0805	3	0	Near GPU
	22 µF	X6S	0805	0	1	Midway between GPU and power supply
	22 µF	X6S	0805	2	0	Near GPU

Note:
[1] Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

CO-LAY N18S



CO-LAY N18S

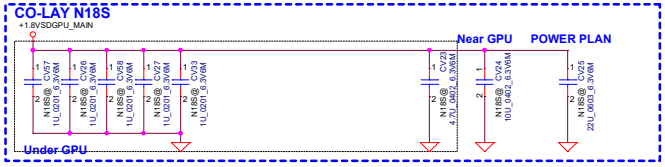
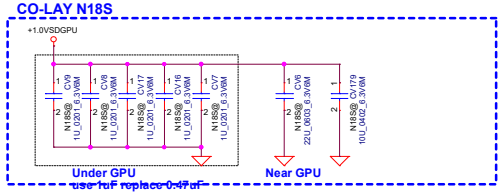


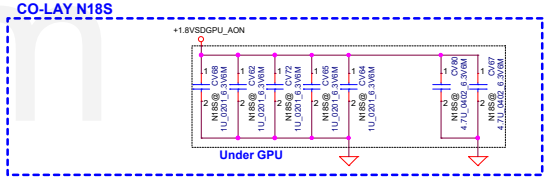
Table 7. N17 and N18 PEX Core and IO Supply Decoupling and Filtering

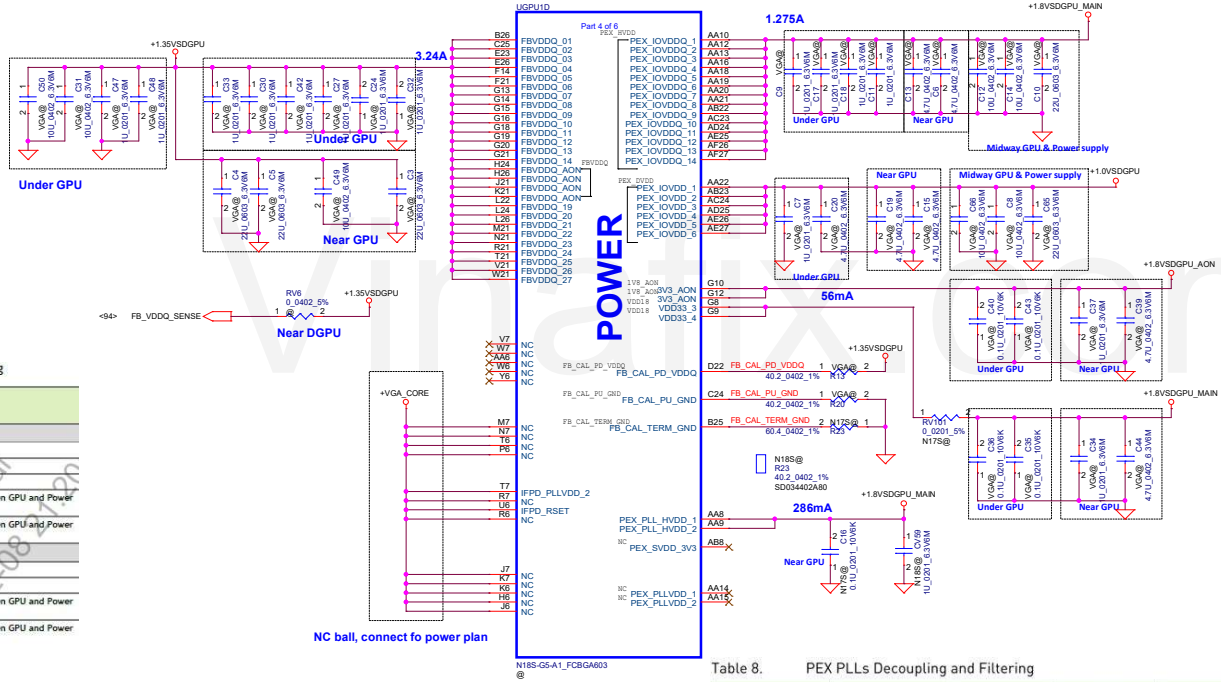
GPU	Capacitor Type		Footprint	Population N18	Population N17	Location
PEX_DVDD Supply Rail						
GB2D-64/GB2C-64 GB2E-64	1.0 µF[1]	X6S	0402 or 0201W	0	1	Under GPU
	0.47 µF[1]	X6S	0201W	12	0	Under GPU
	4.7 µF	X6S	0603	0	2	Near GPU
	4.7 µF	X6S	0603	3	1	Under GPU
	10 µF	X6S	0805	0	2	Midway between GPU and power supply
	10 µF	X6S	0805	3	0	Near GPU
	22 µF	X6S	0805	0	2	Midway between GPU and power supply
	22 µF	X6S	0805	2	0	Near GPU

CO-LAY N18S



CO-LAY N18S





DA-08329-001_V02

Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

Table 7. PEX PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
PEX_PLLVDD Supply Rail						
GB2B-64	0.1 µF	X7R	0402	1	N/A	Under GPU
	1.0 µF	X5R	0603	1	N/A	Near GPU
	4.7 µF	X5R	0805	1	N/A	Near GPU
PEX_SVDD_3V3 Supply Rail						
GB2B-64	4.7 µF	X5R	0603	2	N/A	Near GPU
PEX_PLL_HVDD Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU

Table 8. PEX PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N18	Population N17	Location
PEX_PLL_HVDD Supply Rail						
GB2D-64/GB2C-64	0.1 µF	X7R	0402	0	1	Under GPU
GB2E-64	0.47 µF[1]	X6S	0201W	1	0	Under GPU

Note:
[1] Decoupling for PEX_PLL_HVDD is merged with PEX_HVDD, and Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

Table 10. VDD_AON and VDD_MAIN Decoupling

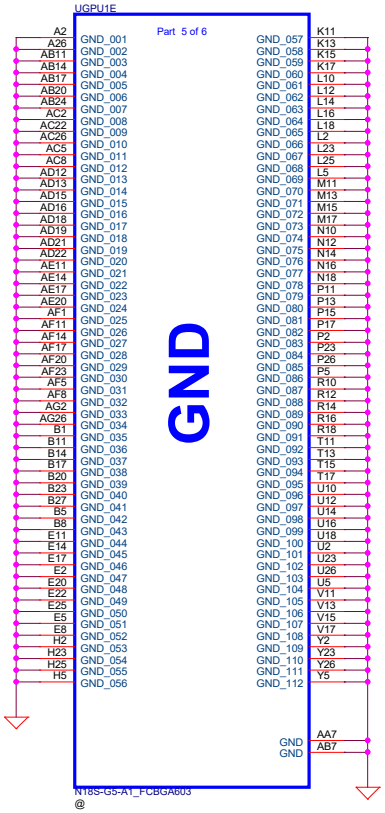
GPU	Capacitor Type		Footprint	Population N18	Population N17	Location
N17 VDD18 (N18 NC) Supply Rail						
GB2D-64/GB2C-64	0.1 µF	X7R	0402	N/A	2	Under GPU
GB2E-64	1.0 µF	X6S	0603	N/A	1	Near GPU
	4.7 µF	X6S	0603	N/A	1	Near GPU
1V8_AON Supply Rail						
GB2D-64/GB2C-64	0.1 µF	X7R	0402	0	2	Under GPU
GB2E-64	0.47 µF[1]	X6S	0201W	4	0	Under GPU
	1.0 µF[1]	X6S	0402 or 0201W	0	1	Near GPU
	0.47 µF[1]	X6S	0201W	6	0	Near GPU

Compal Electronics, Inc.

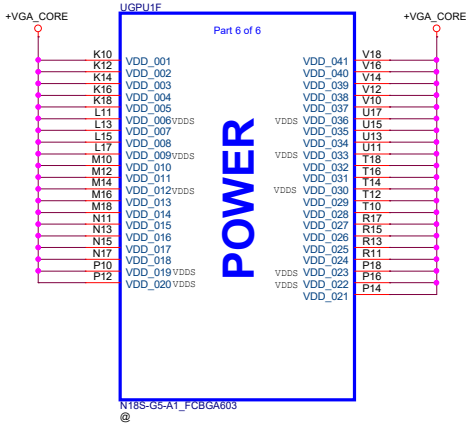
Title: N17S POWER & GND 4/7

Size: Custom | Document Number: LA-K092P | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 30 of 102



change to N18S footprint



change to N18S footprint

NV 16x DG-07158-V05

Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64 / GB2-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

DA-08329-001_V01

Table 3. NVVDD and NVVDDS Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
NVVDD Supply Net						
GB2B-64, GB2C-64	4.7 µF	X6S	0603	10	8	Under GPU
	1 µF	X6S	0402	4	3	Under GPU
	47 µF	X5R	0805	1	-	Near GPU
	10 µF	X7R	0805	-	4	Near GPU
	22 µF	X5R	0805	1	3	Near GPU
	4.7 µF	X5R	0805	1	4	Near GPU
	330 µF	POS	7343	1	1	Near GPU
NVVDDS Supply Net						
GB2C-64 Only	4.7 µF	X6S	0603	N/A	4	Under GPU
	1 µF	X6S	0402	N/A	2	Under GPU
	10 µF	X6S	0805	N/A	7	Near GPU
	22 µF	X6S	0805LP	N/A	1	Near GPU
	330 µF	POS	7343	N/A	1	Near GPU

DA-07750-000-V02

Table 6. EDP-Continuous [3]

Products	VRAM Type	GPU Core – (A)	GPU FBIO 1.5V [4] (A)	GPU FBIO 1.35V [4] (A)	FB Total [1,5] 1.5V [4] (A)	FB Total [1,5] 1.35V [4] (A)	1.05V Total [2] 1.05V [4] (A)	3.3V Total 3.3V [4] (A)
N16S-GMR	GDDR5	19.0	–	2.0	–	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GTR	GDDR5 @ 2.0 GHz	26.5	–	2.0	–	4.2	0.80	0.06
	GDDR5 @ 2.5 GHz	26.5	–	2.0	–	4.7	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06

Table 7. EDP-Peak [3]

Products	VRAM Type	GPU Core – (A)	GPU FBIO 1.5V [4] (A)	GPU FBIO 1.35V [4] (A)	FB Total [1,5] 1.5V [4] (A)	FB Total [1,5] 1.35V [4] (A)	1.05V Total [2] 1.05V [4] (A)
N16S-GMR	GDDR5	34.0	–	2.9	–	6.8	2.1
	DDR3/L	39.5	2.6	2.3	4.1	3.9	2.1
N16S-GTR	GDDR5 @ 2.0 GHz	53.0	–	2.9	–	6.8	2.1
	GDDR5 @ 2.5 GHz	53.0	–	3.1	–	7.2	2.1
	DDR3/L	51.0	2.6	2.3	4.1	3.9	2.1

SP-08318-001_V03

Table 7. Output EDP-Continuous

Product	NVVDD – (A)	GPU FBIO 1.35V[4] (A)	FB Total[5] 1.35V[4] (A)	1.0V Total[1] 1.0V[4] (A)	1.8V Total[2] 1.8V[4] (A)
N17S-G1	30.0	2.0	3.4	0.1	0.3

Table 8. Output EDP-Peak

Product	NVVDD – (A)	GPU FBIO 1.35V[3] (A)	FB TOTAL[4] 1.35V[3] (A)	1.0V Total[1] 1.0V[3] (A)
N17S-G1	60.1	3.2	6.6	0.2

DA-07751-000-V02

Table 5. EDP-Continuous [3]

Product	VRAM Type	GPU Core – (A)	GPU FBIO 1.5V [4] (A)	GPU FBIO 1.35V[4] (A)	FB Total [1,5] 1.5V [4] (A)	FB Total [1,5] 1.35V [4] (A)	1.05V Total [2] 1.05V [4] (A)	3.3V Total 3.3V [4] (A)
N16V-GMR1	GDDR5 @ 2.0 GHz	18.5	–	2.0	–	4.2	0.8	0.06
	GDDR5 @ 2.5 GHz	18.5	–	2.0	–	4.7	0.8	0.06
	DDR3/L	19.0	1.4	1.4	2.4	2.3	0.8	0.06

Table 6. EDP-Peak [3]

Products	VRAM Type	GPU Core – (A)	GPU FBIO 1.5V [4] (A)	GPU FBIO 1.35V [4] (A)	FB Total [1,5] 1.5V [4] (A)	FB Total [1,5] 1.35V [4] (A)	1.05V Total [2] 1.05V [4] (A)
N16V-GMR1	GDDR5 @ 2.0 GHz	30.0	–	2.9	–	6.8	2.1
	GDDR5 @ 2.5 GHz	31.0	–	3.1	–	7.2	2.1
	DDR3/L	28.5	2.6	2.3	4.1	3.9	2.1

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: **N17S POWER & GND 5/7**

Size	Document Number	Rev
Custom	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 31 of 102

VRAM GDDR5 chips

<28,33> MDA[63..0] → MDA[63..0]
<28,33> CMDA[31..0] → CMDA[31..0]

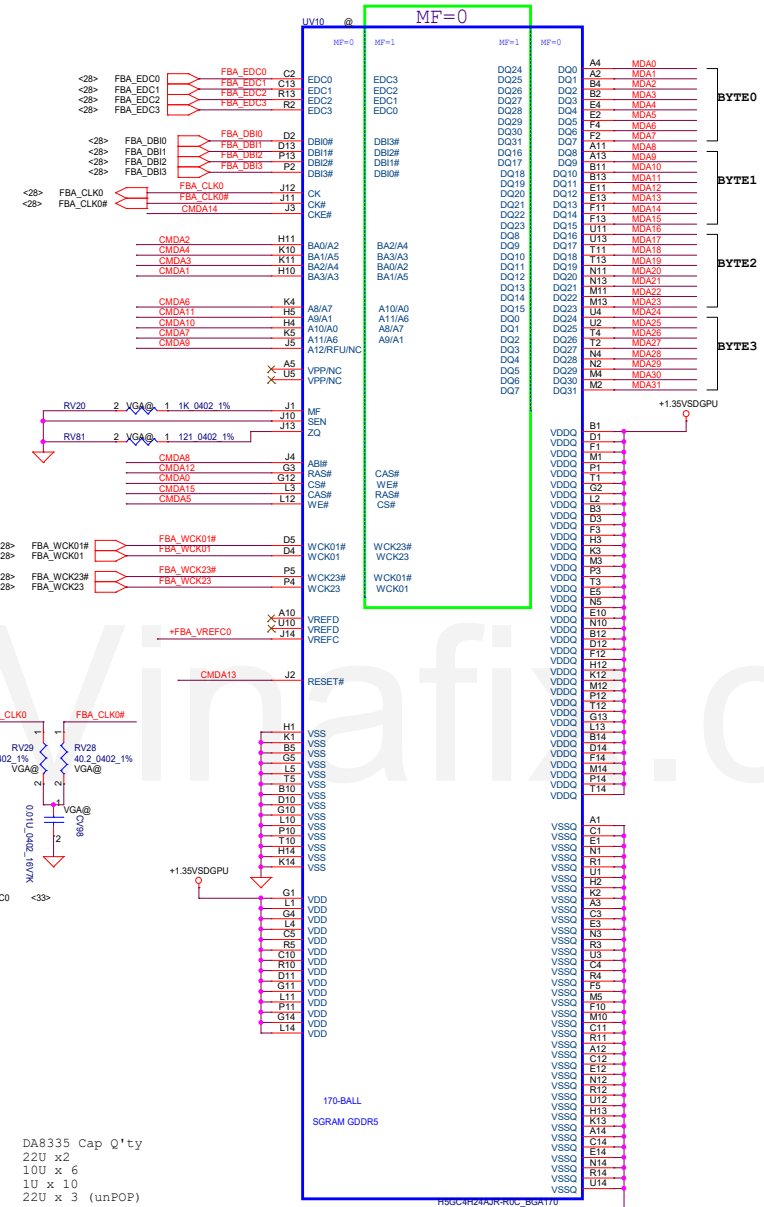
X76 for N17S 2G VRAM

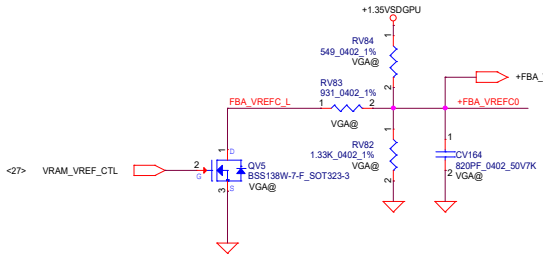
ZZZ X76VSAM@ — Samsung_256Mx32x2 X76829BOL03
ZZZ X76VHYN@ — Hynix_256Mx32x2 X76829BOL01
ZZZ X76VMIC@ — Micron_256Mx32x2 X76829BOL02

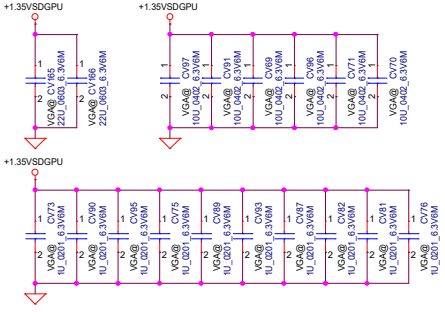
GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

Channel 0 BOT SIDE







DA8335 Cap Q'ty
22U x2
10U x 6
1U x 10
22U x 3 (unPOP)

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: N17S Lower Rank0 6/7

Size: Custom | Document Number: LA-K092P | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 32 of 102

VRAM GDDR5 chips

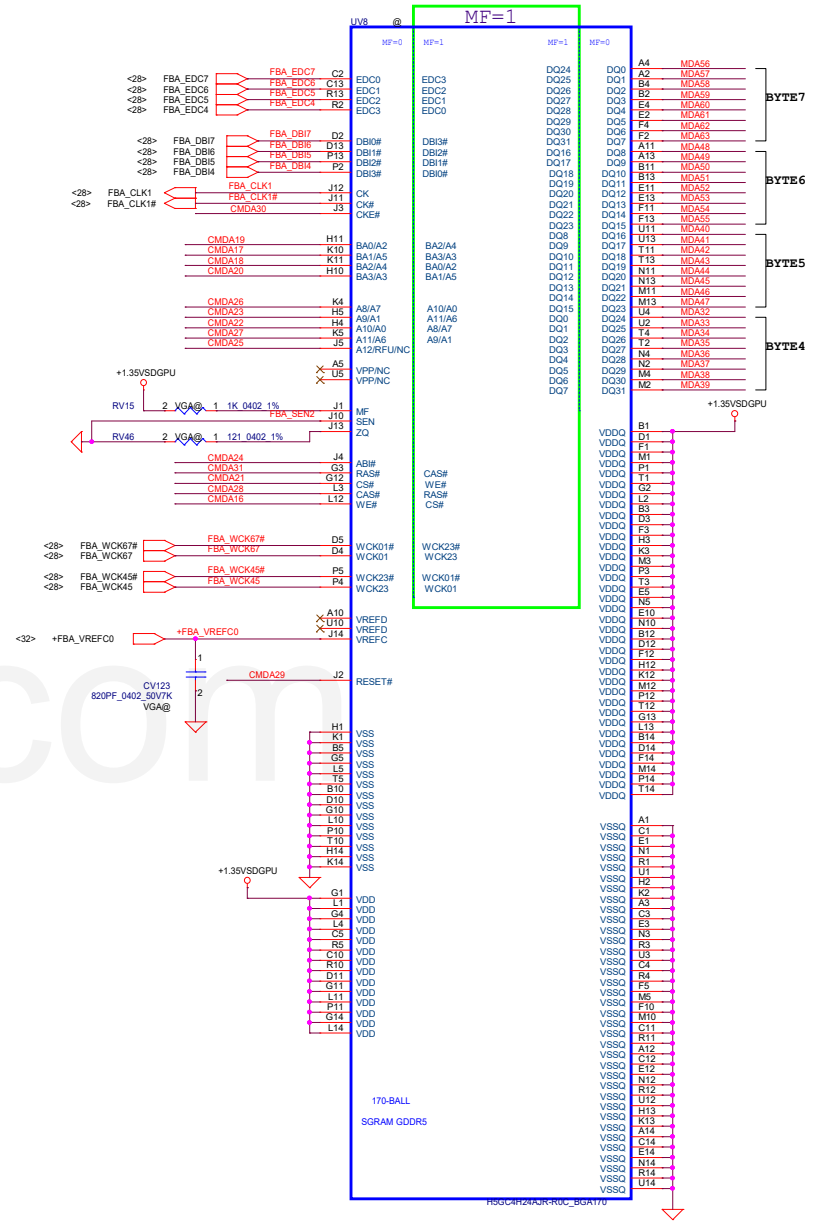
<28,32> MDA[63..0] → MDA[63..0]

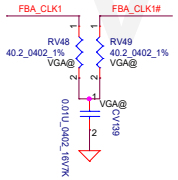
<28,32> CMDA[31..0] → CMDA[31..0]

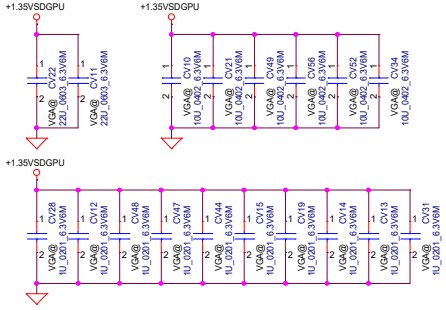
GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

Channel 1 BOT SIDE







DA8335 Cap Q'ty
22U x2
10U x 6
1U x 10
22U x 3 (unPOP)

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: N17S Lower Rank1 7/7

Size: Custom | Document Number: LA-K092P | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 33 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for DGPU**

Size | Document Number: **LA-K092P** | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 34 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **N16P GDDR5 A**

Size: | Document Number: **LA-K092P** | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 35 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for N16P_GDDR5_A**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 36 of 102

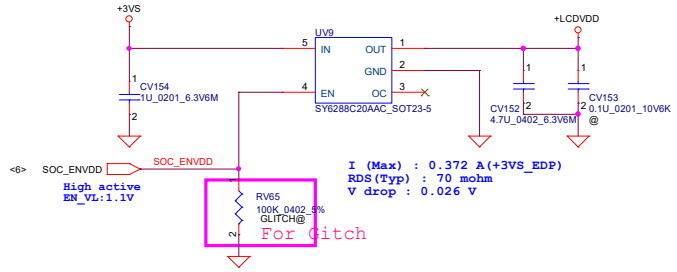
Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

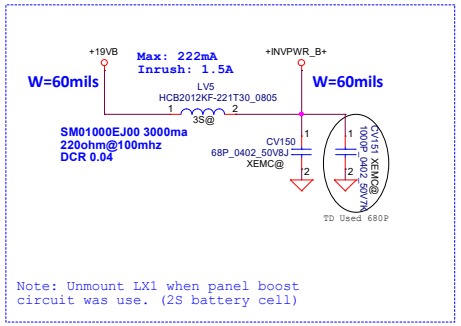
Compal Electronics, Inc.

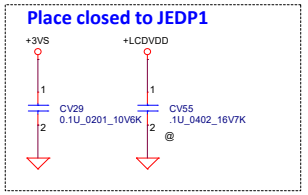
Title: **DGPU_DC/DC Interface**

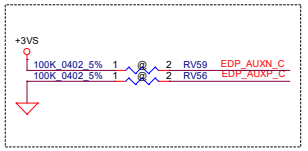
Size	Document Number	Rev
	LA-K092P	0.1

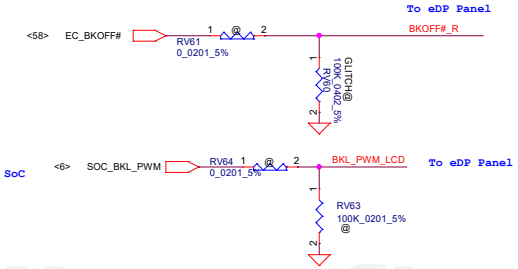
Date: Thursday, May 06, 2021 Sheet 37 of 102

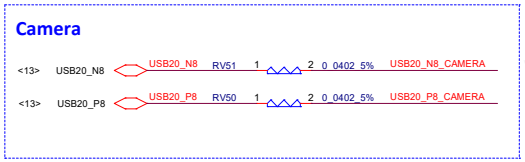


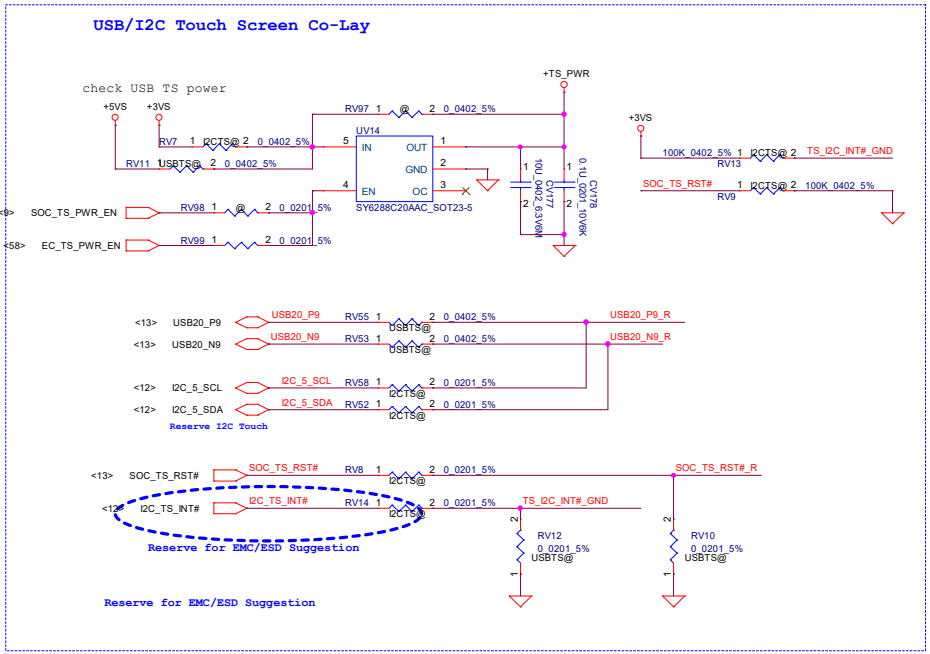


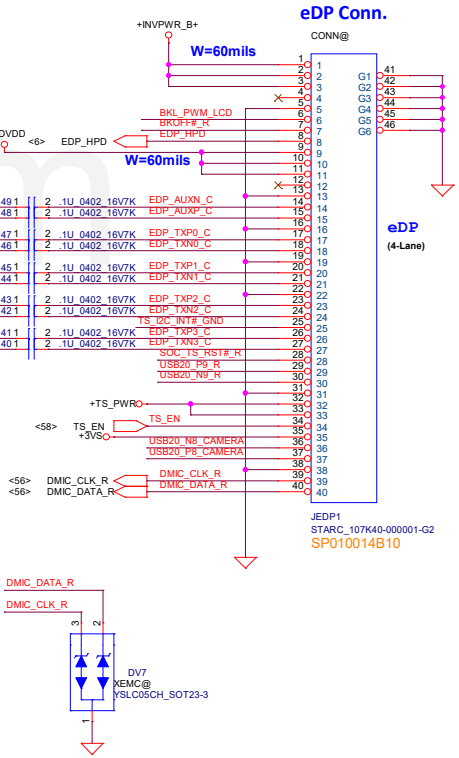












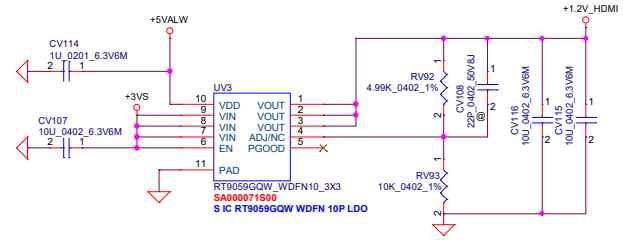
Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

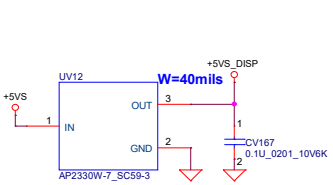
Compal Electronics, Inc.

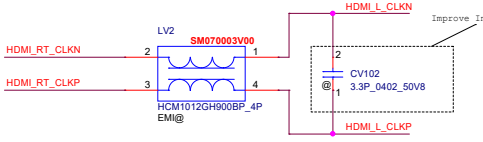
Title: eDP / DMIC / IR Camera / Touch

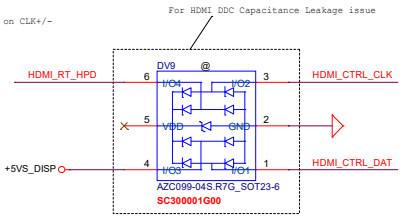
Size	Document Number	Rev
	LA-K092P	0.1

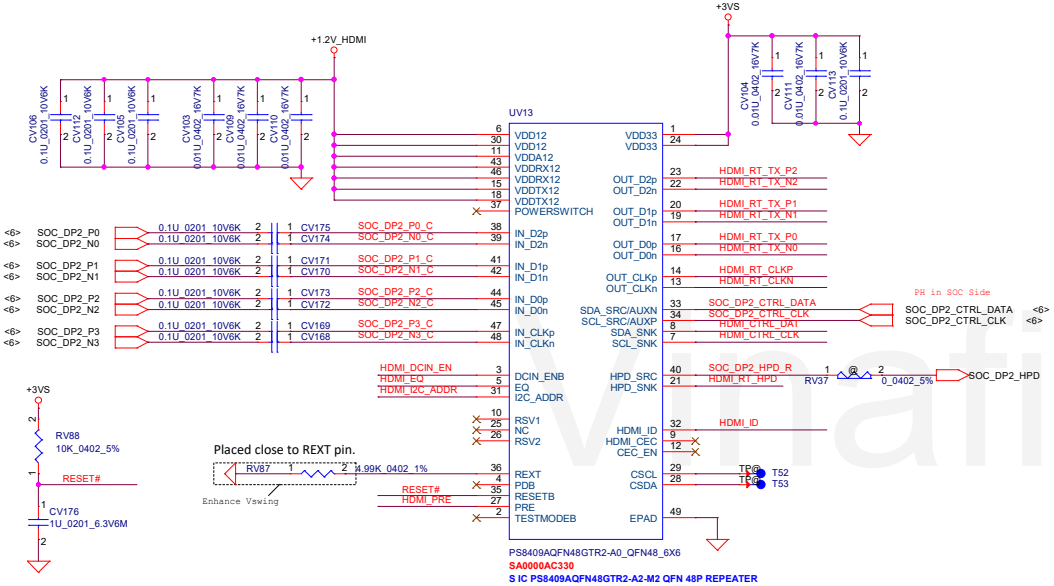
Date: Thursday, May 06, 2021 | Sheet 38 of 102

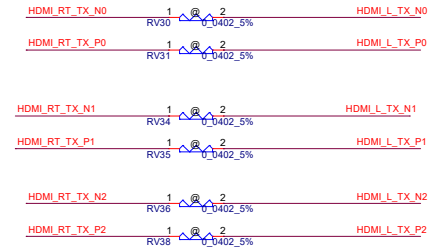


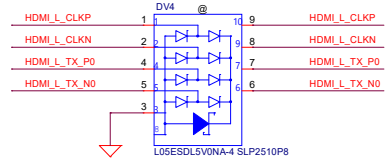


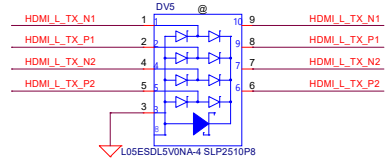


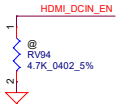




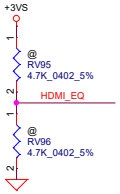




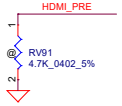




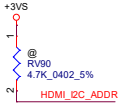
DC coupling enable; Internal pull up, 3.3V I/O.
L: DC coupling input
H: Default,AC coupling input



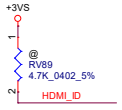
Receiver equalization setting(Internal 150K PD)
(*) L: programmable EQ for channel loss up to 5.3dB
( ) H: programmable EQ for channel loss up to 10dB
( ) M: programmable EQ for channel loss up to 14dB



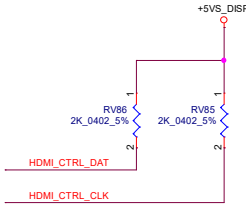
Output pre-emphasis setting;Internal pull-up 3.3V I/O
L: Pre-emphasis =2.5dB
H: Default, No Pre-emphasis



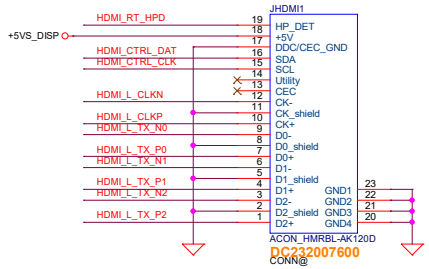
I2C Slave Address selection; Internal pull down;3.3V I/O
L: Default, Slave address 0x10-0x2F.
H: Alternative salve address 0x90-0x9F, 0xD0-0xDF.



HDMI_ID enable ; Internal pull down;3.3V I/O
L: Default, HDMI ID enable
H: HDMI ID disable



HDMI connector



Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **HDMI REDRIVER (PS8409)**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 Sheet 39 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **CloverFalls Conn**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 40 of 102

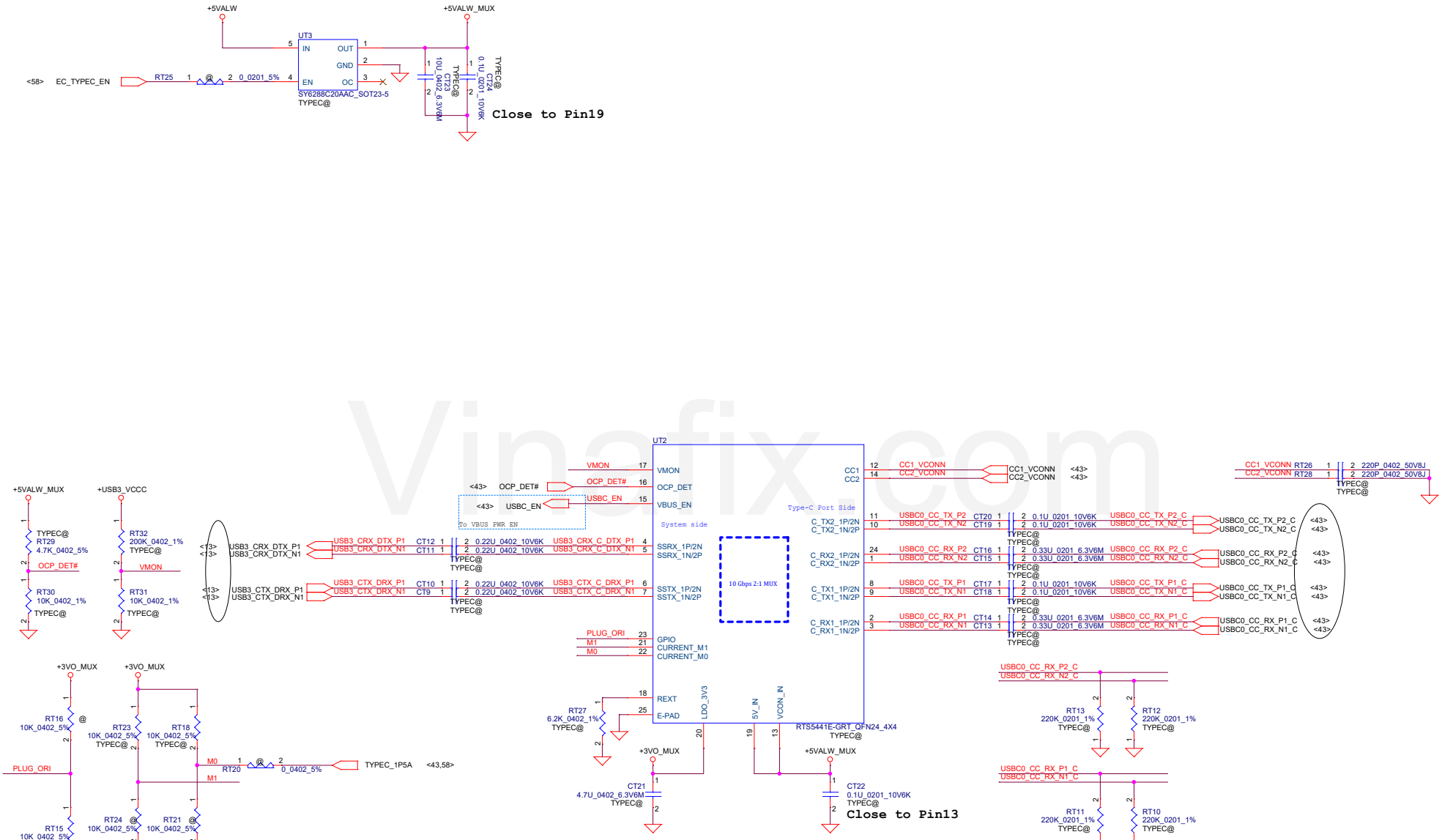
Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for CRT**

Size | Document Number: **LA-K092P** | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 41 of 102



5441E Current Limit		
M1	M0	MODE
L	H	0.9A
H	L	1.5A
H	H	3A

confirm realtek hand-shake

RTS5441 M0 truth table by 2018 BIOS spec			
TYPEC_1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery >30%
L	1.5A	1.92A	Battery <30% when DC mode

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

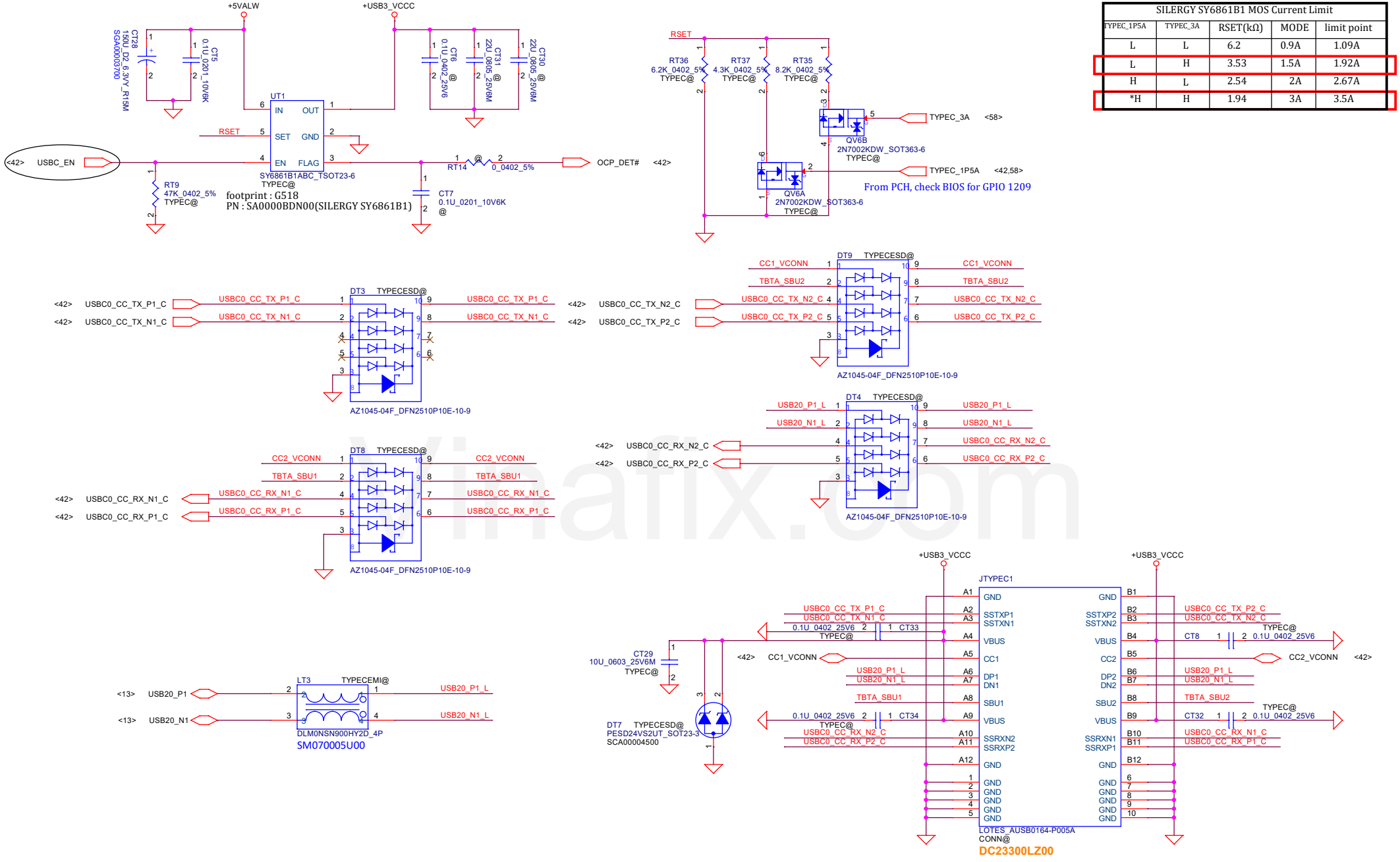
Compal Electronics, Inc.

Title: TBT TYPE-C Port0 (1/2)

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 Sheet 42 of 102

SILERGY SY6861B1 MOS Current Limit				
TYPEC_1P5A	TYPEC_3A	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A



CC1_VCONN & CC2_VCONN need 20miil trace width.

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **TBT_TYPE-C_Port0 (2/2)**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 Sheet 43 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **TBT TYPE-C Port1 (1/2)**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 Sheet 44 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **TBT_TYPE-C_Port1 (2/2)**

Size | Document Number: **LA-K092P** | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 45 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **TBT_TYPE-C_Port2 (1/2)**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 46 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **TBT TYPE-C Port2 (2/2)**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 Sheet 47 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **TBT TYPE-C Port3 (1/2)**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 Sheet 48 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for TBT_TYPE-C_Port3 (2/2)**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 49 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

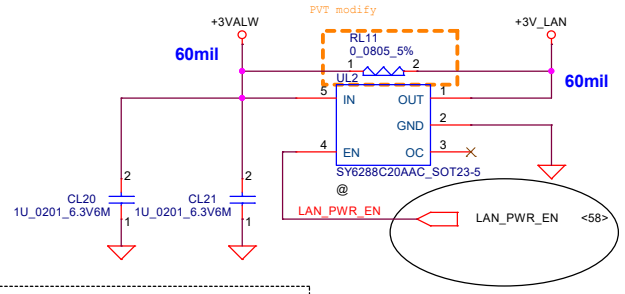
Compal Electronics, Inc.

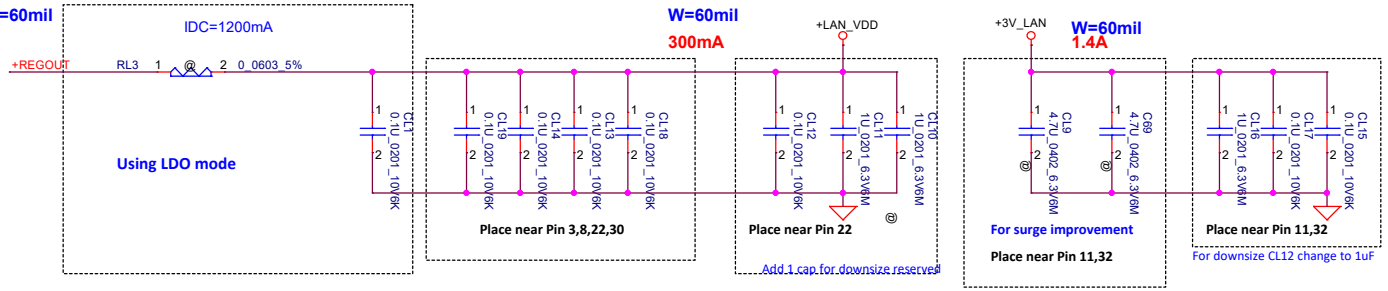
Title: **TYPE-C Power Path**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 Sheet 50 of 102

LAN-RTL8111H

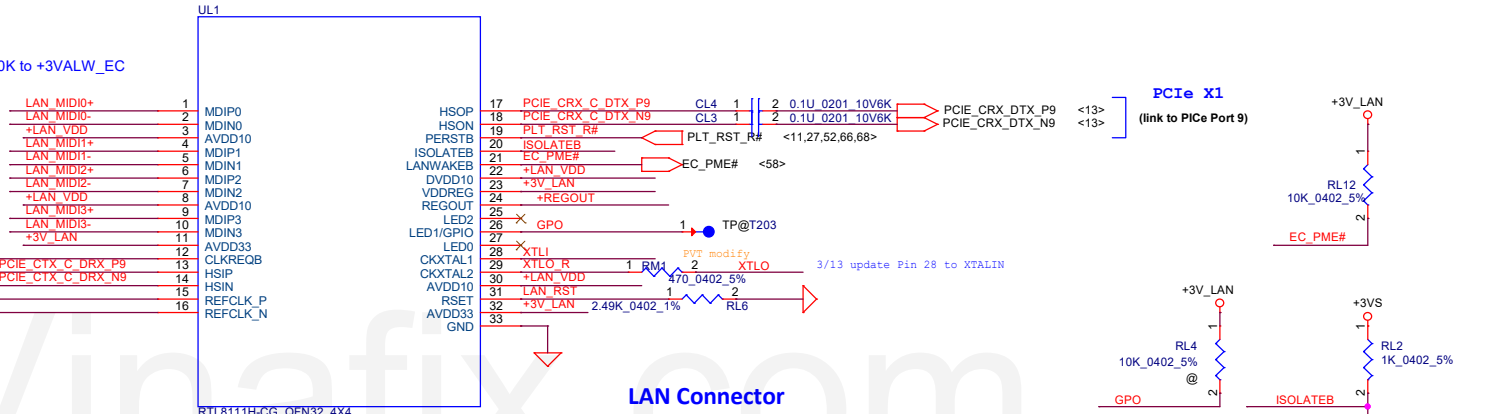




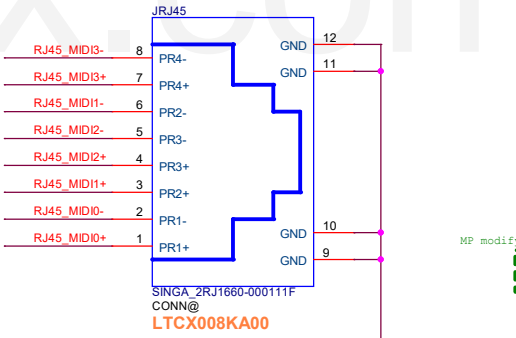
From EC

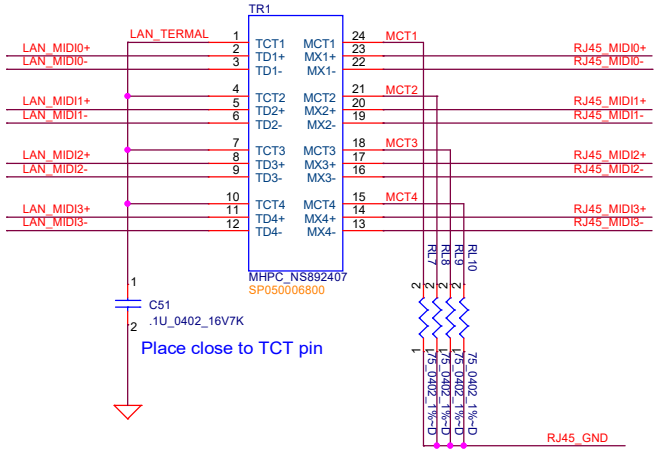
High active.
EN threshold voltage min:1.2V typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A

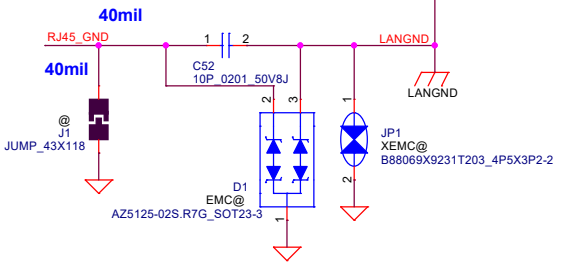
reserve EC_PME# pull high 100K to +3VALW_EC

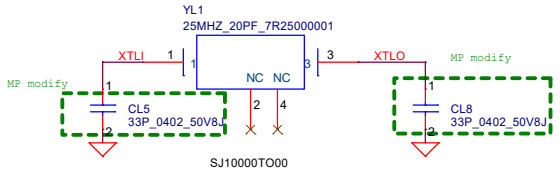


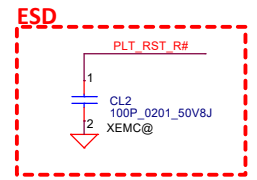
LAN Connector









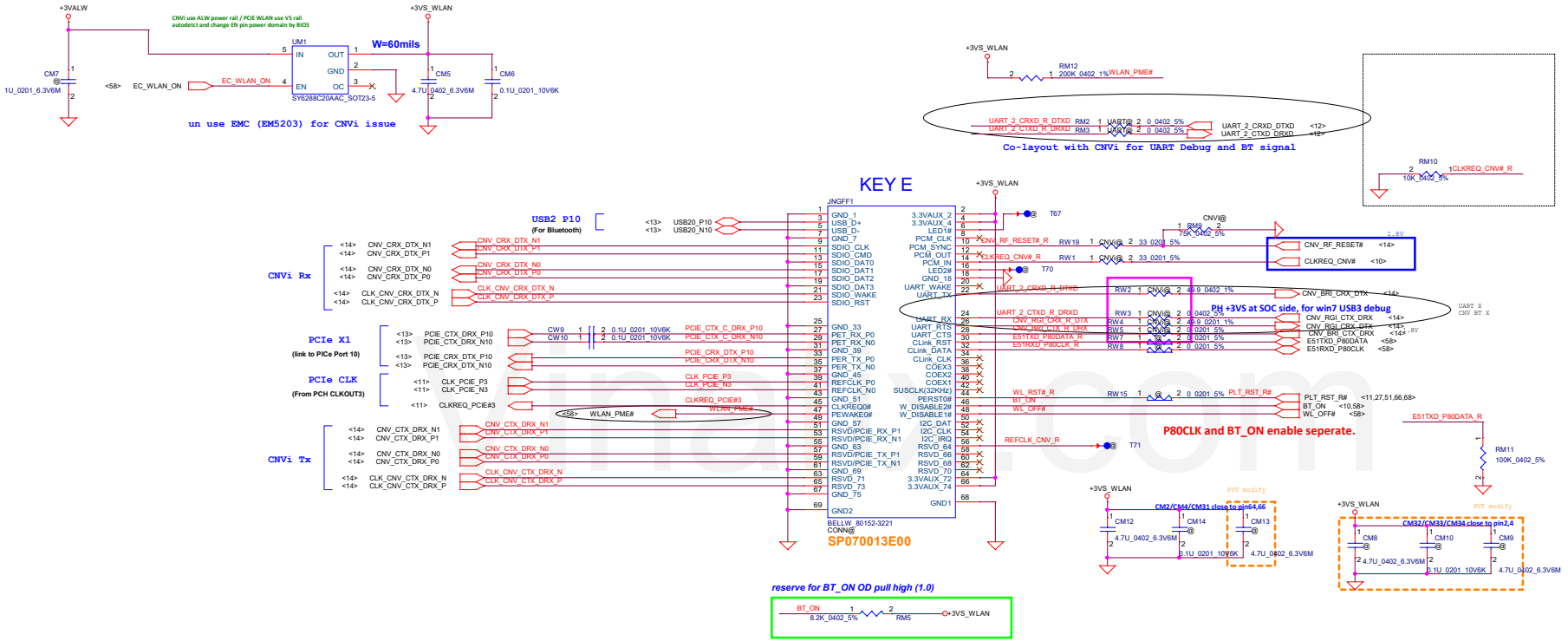


Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: LAN-RTL8111H
Size: Document Number: LA-K092P
Rev: 0.1
Date: Thursday, May 06, 2021
Sheet: 51 of 102

NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]



Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.			
Title	NGFF WL(KEY E) / WWAN(KRY B)		
Size	Document Number		Rev
	LA-K092P		0.1
Date:	Thursday, May 06, 2021	Sheet	52 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for WIGIG/WIDI**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 53 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for PCIE Device**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 54 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

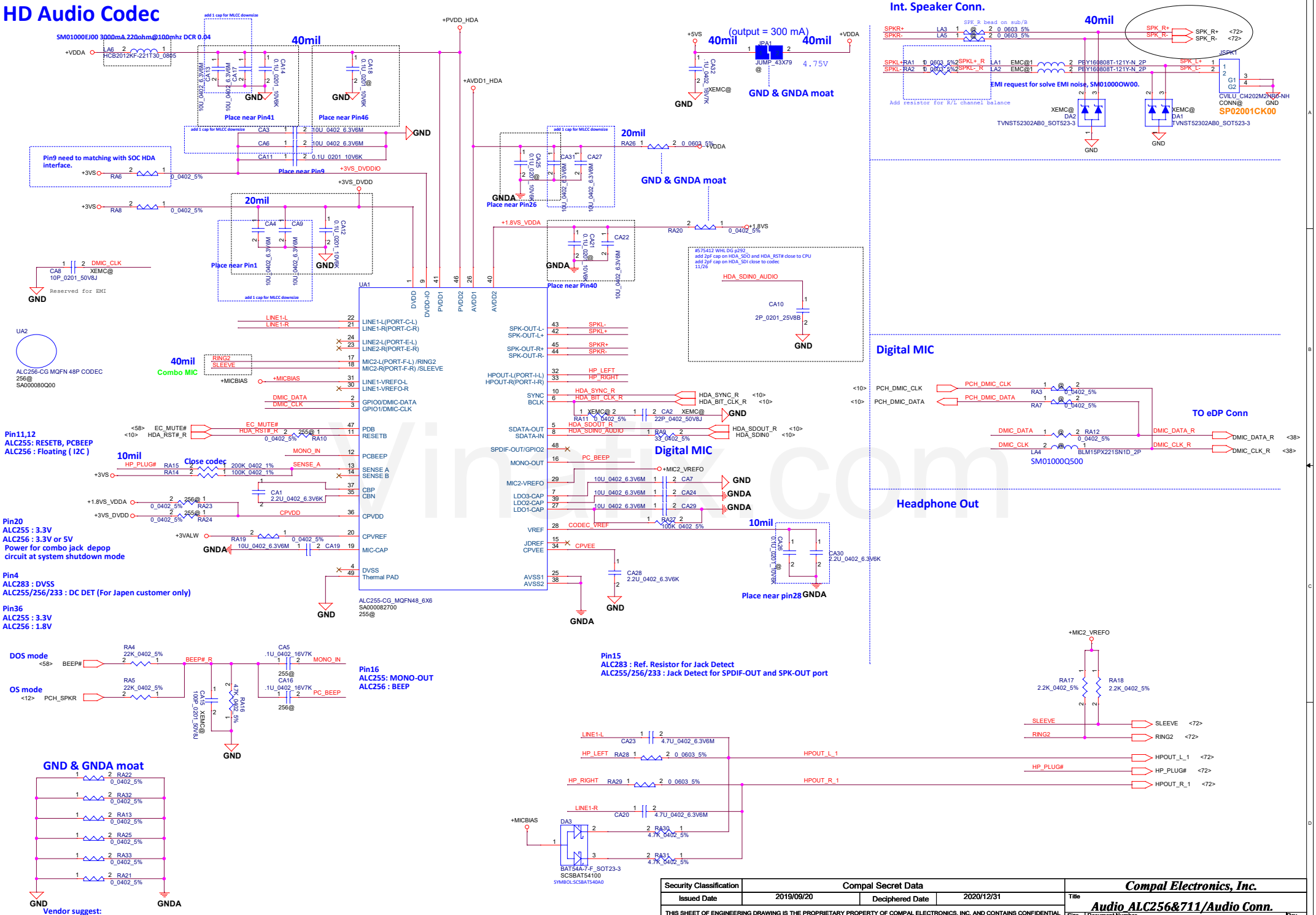
Compal Electronics, Inc.

Title: **Reserve for PCIE Device**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 55 of 102

HD Audio Codec



Compal Electronics, Inc.	
Title	Audio_ALC256&711/Audio Conn.
Size	Document Number: LA-K092P
Rev	0.1
Date:	Thursday, May 06, 2021
Sheet	56 of 102

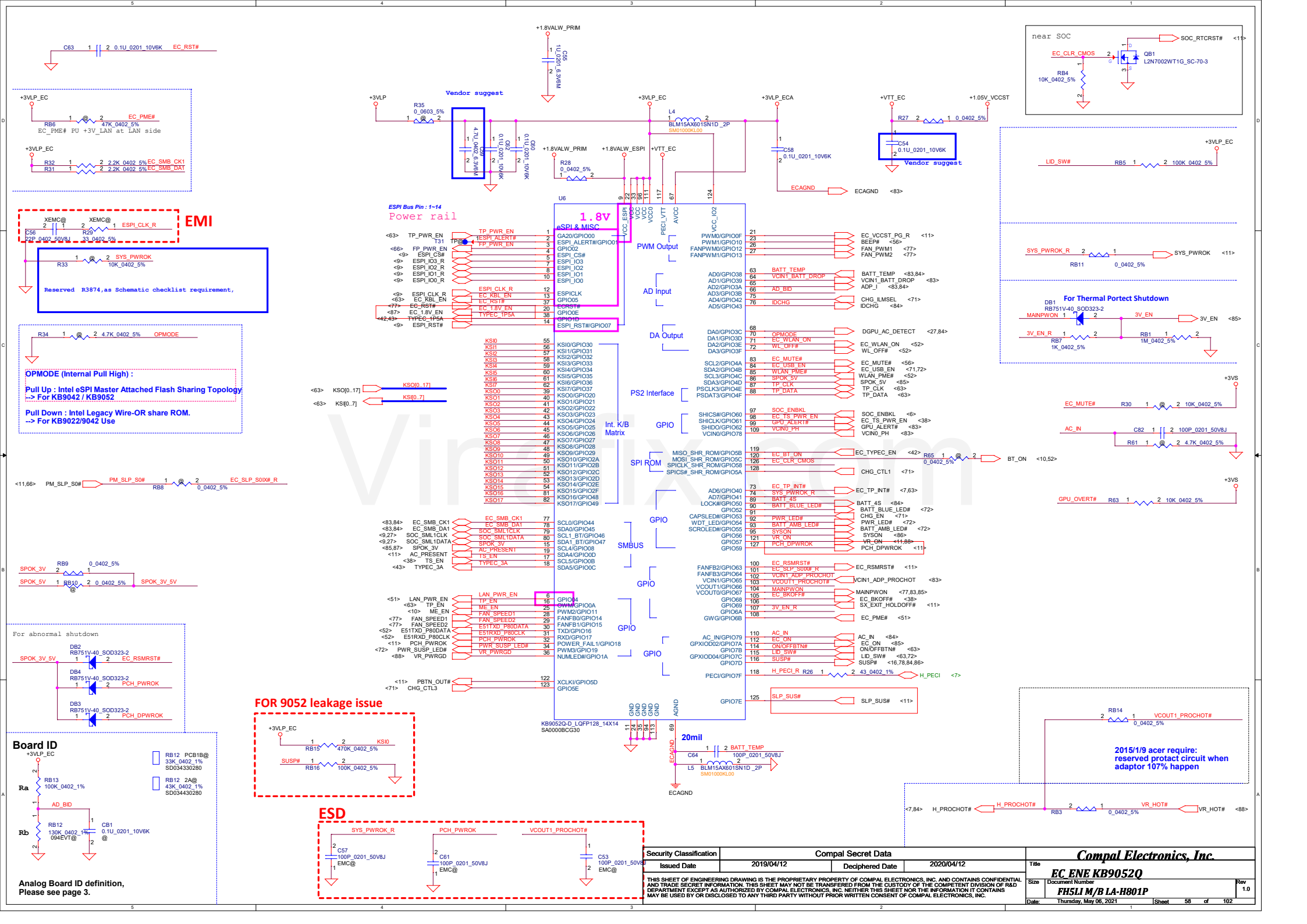
Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for Audio Ampfilper**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 57 of 102


EMI
Reserved R3874,as Schematic checklist requirement,
OPMODE (Internal Pull High) :
Pull Up : Intel eSPI Master Attached Flash Sharing Topology
--> For KB9042 / KB9052
Pull Down : Intel Legacy Wire-OR share ROM.
--> For KB9022/9042 Use
For abnormal shutdown
Board ID
Analog Board ID definition,
Please see page 3.
FOR 9052 leakage issue
ESD
Vendor suggest
ESPI Bus Pin : 1~14
Power rail
1.8V
eSPI & MISC
PWM Output
AD Input
DA Output
PS2 Interface
GPIO
Int. K/B Matrix
SPI ROM
SMBUS
KB9052Q-D_LQFP128_14X14
SA0000BCG30
20mil
near SOC
For Thermal Portect Shutdown
2015/1/9 acer require:
reserved protact circuit when
adaptor 107% happen
Security Classification
Compal Secret Data
Issued Date
2019/04/12
Deciphered Date
2020/04/12
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
EC ENE KB9052Q
Size
Document Number
FH5LI M/B LA-H801P
Rev
1.0
Date:
Thursday, May 06, 2021
Sheet
58
of
102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for KBC&SIO**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 59 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for Secure & Reset IC**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 60 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for SMB/I2C Block Diagrams**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 61 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

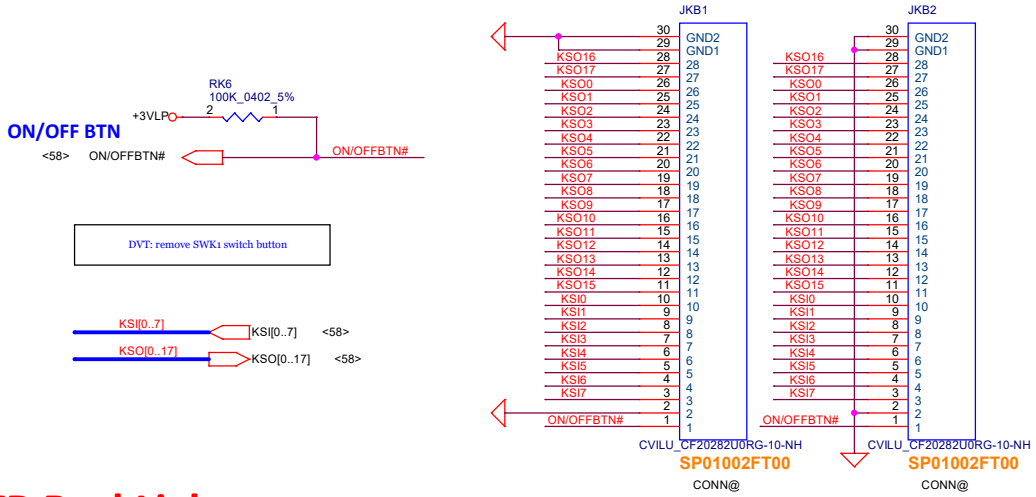
Compal Electronics, Inc.

Title: **Reserve for LEDs Controller**

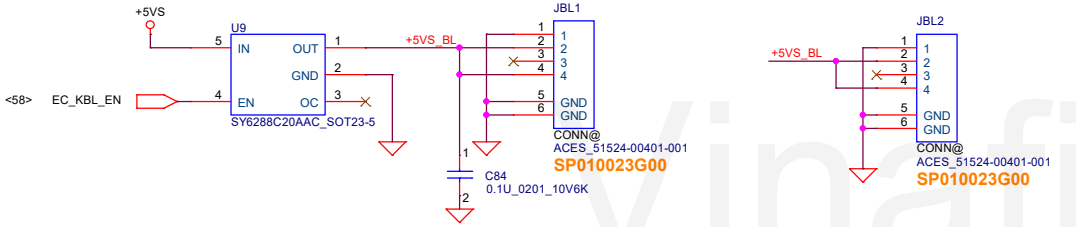
Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 62 of 102

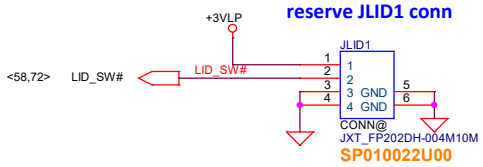
KB Conn.



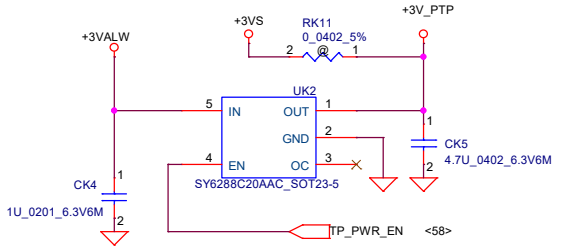
KB BackLight



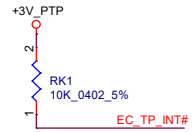
Lid Switch

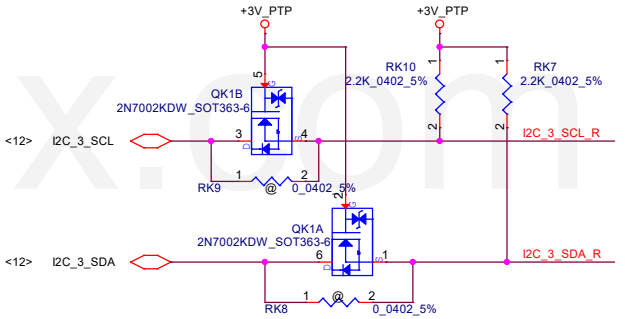


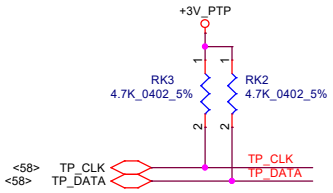
TP/B Conn.

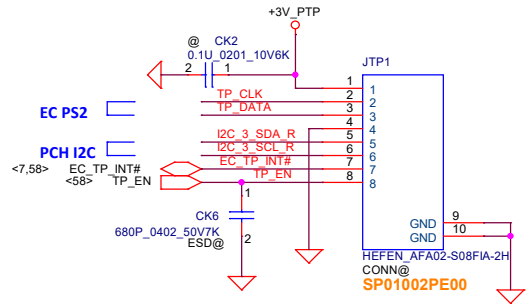


TP_PWR_EN follow SYSON behavior









Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

Compal Electronics, Inc.

Title: *KB/TP*

Size	Document Number	Rev
Custom	*FH5LI M/B LA-H801P*	1.0

Date: Thursday, May 06, 2021 Sheet 63 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for KB/TP/LED/LID**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 64 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

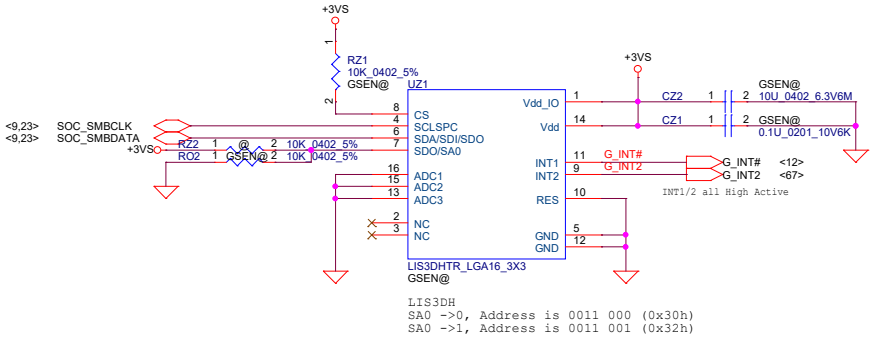
Compal Electronics, Inc.

Title: **Reserve for KB/TP/LED/LID**

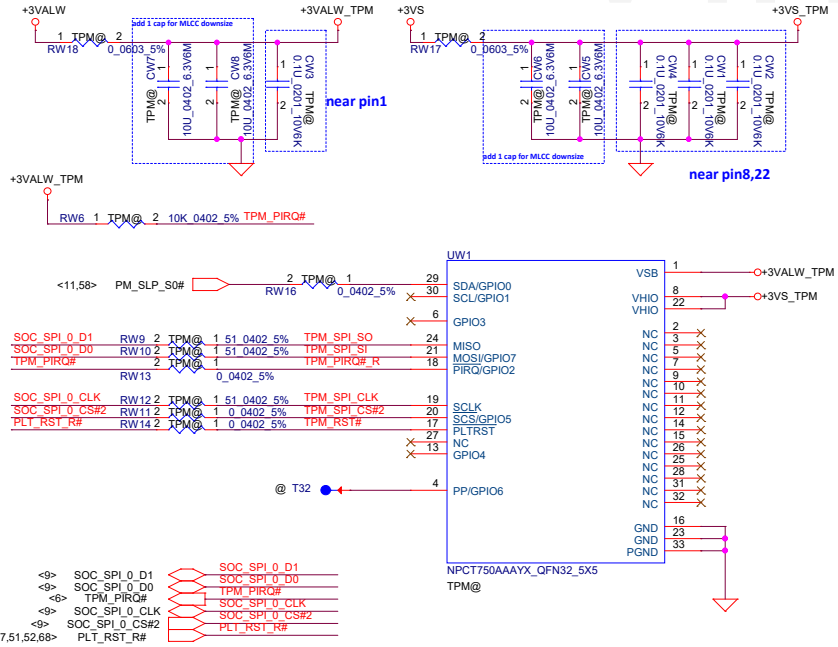
Size | Document Number: **LA-K092P** | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 65 of 102

G-Sensor reserved for BA serial



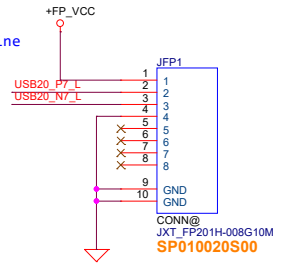
TPM 2.0

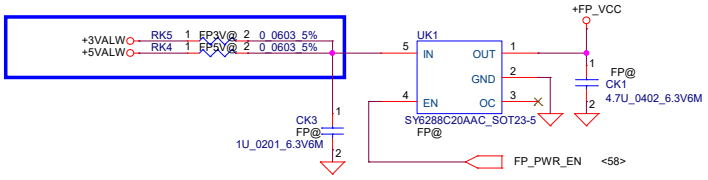


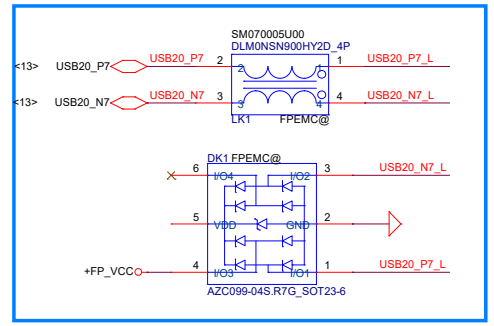
Finger Print

Power Souce Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V

DVT:update JFP1 define







Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

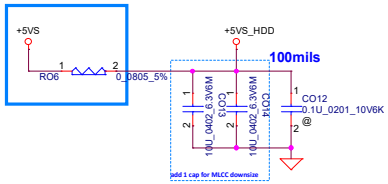
Compal Electronics, Inc.

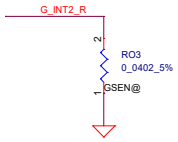
Title: KB & TP & TPM & FP

Size: Custom | Document Number: FH5LI M/B LA-H801P | Rev: 1.0

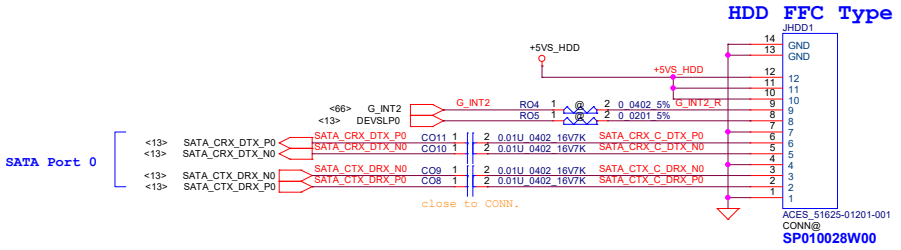
Date: Thursday, May 06, 2021 | Sheet 66 of 102

SATA HDD

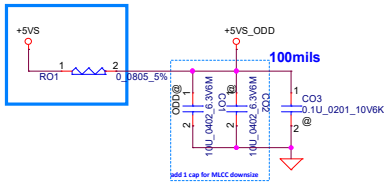




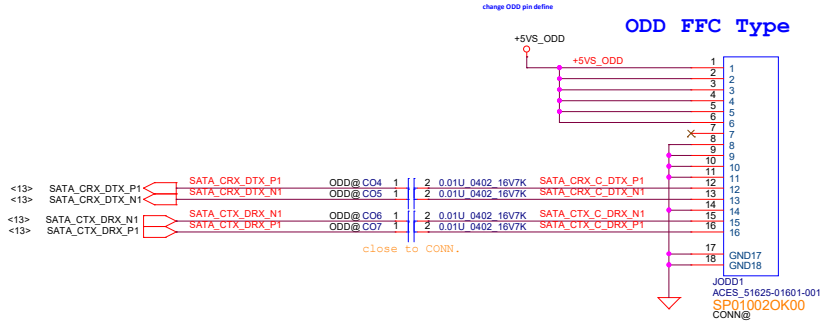
HDD FFC Type



SATA ODD



ODD FFC Type



Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

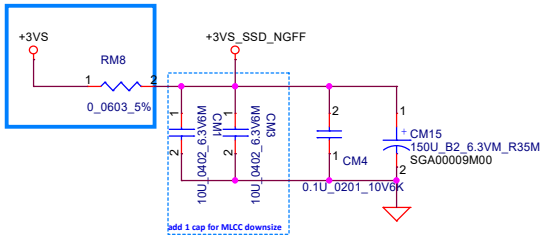
Compal Electronics, Inc.

Title: **HDD/ODD Connector**

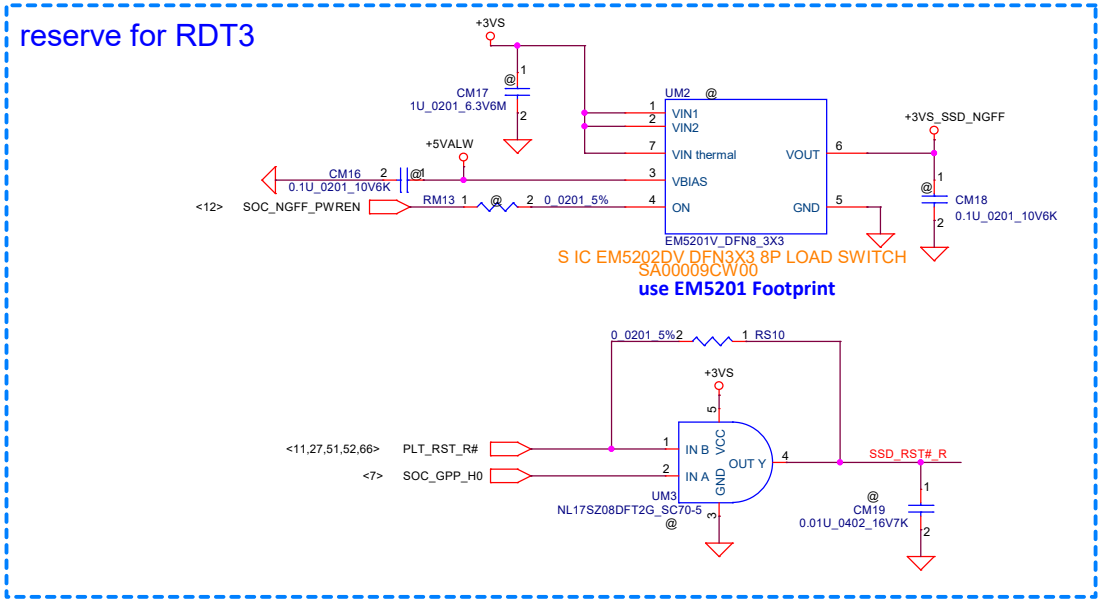
Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 Sheet 67 of 102

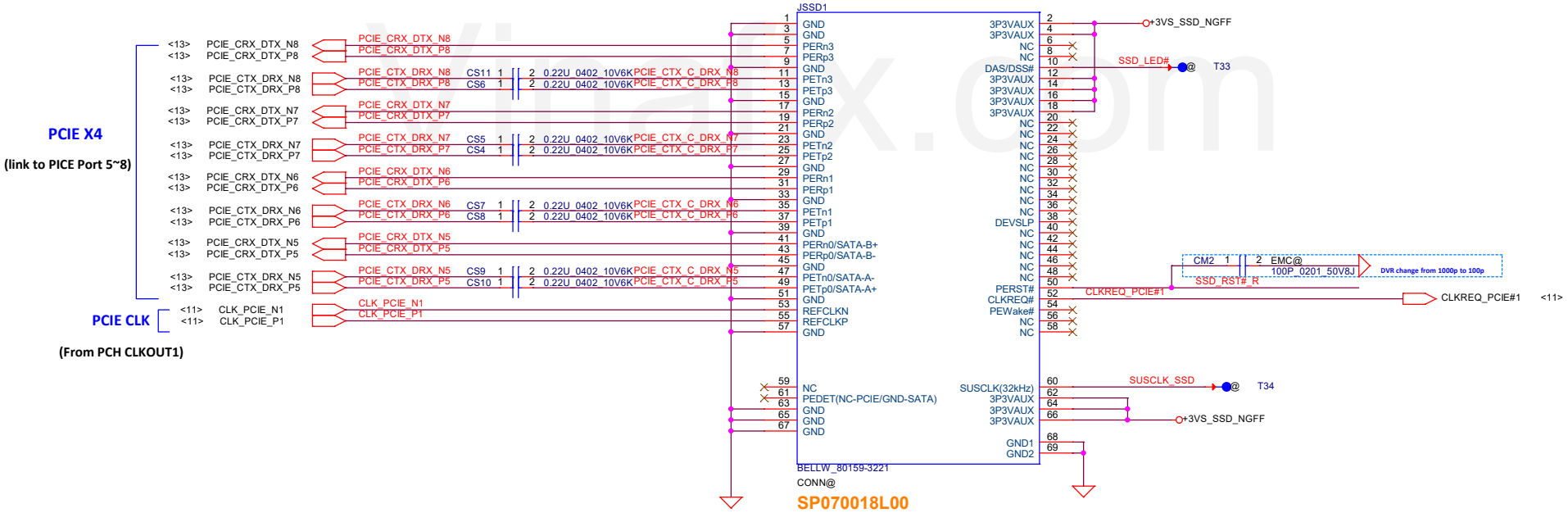
mSATA/SSD



reserve for RDT3



KEY M



Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.			
Title: NGFF SSD(KEY M)			
Size	Document Number: LA-K092P		Rev: 0.1
Date: Thursday, May 06, 2021	Sheet 68 of 102		

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve eMMC**

Size | Document Number: **LA-K092P** | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 69 of 102

+3VS TO +3VS_CARD

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

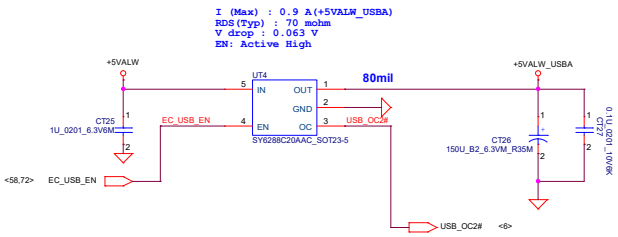
Compal Electronics, Inc.

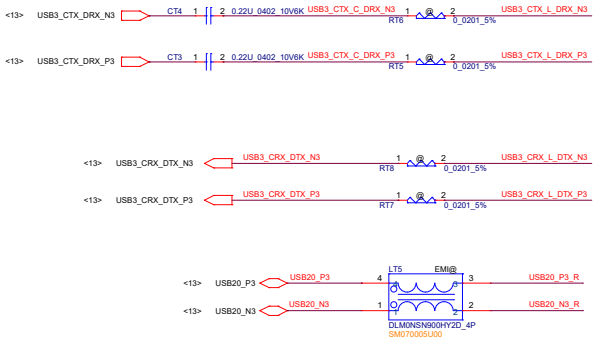
Title: **Card Reader RTS5227S**

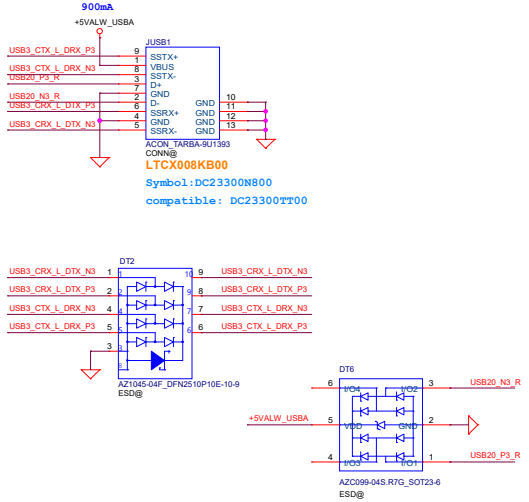
Size: | Document Number: **LA-K092P** | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 70 of 102

MB_USB3.1 Type-A Conn.

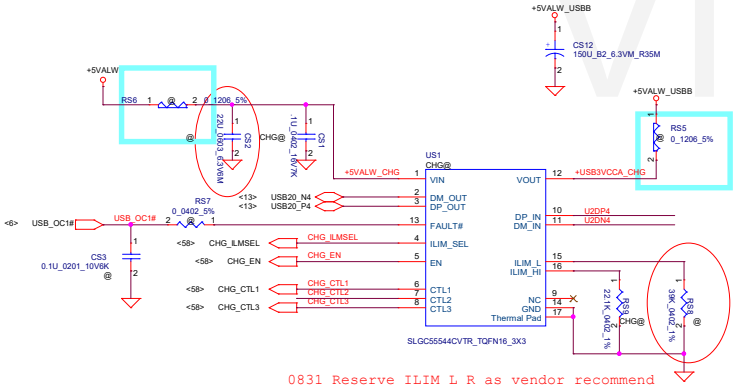






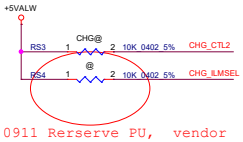
MB_USB3.1 Type-A Conn. (Charge Port)

USB Host Charger



0831 Reserve ILIM_L R as vendor recommend

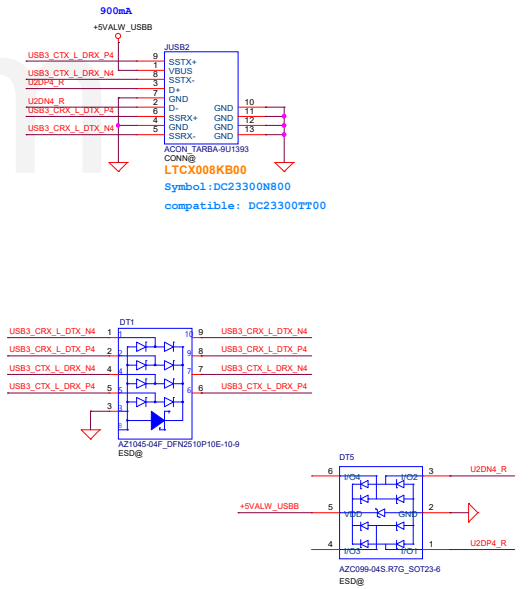
ILM R vaule
Ios(mA)=50250/R(Kohm)
ILIM_Hi=2273mA
ILIM_L=1288mA(reserve)



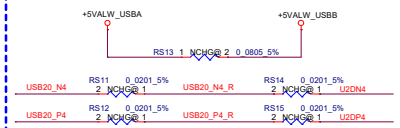
0911 Rerserve PU, vendor suggest to EC control if future need support SDP2

USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected



W/O Charger



Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

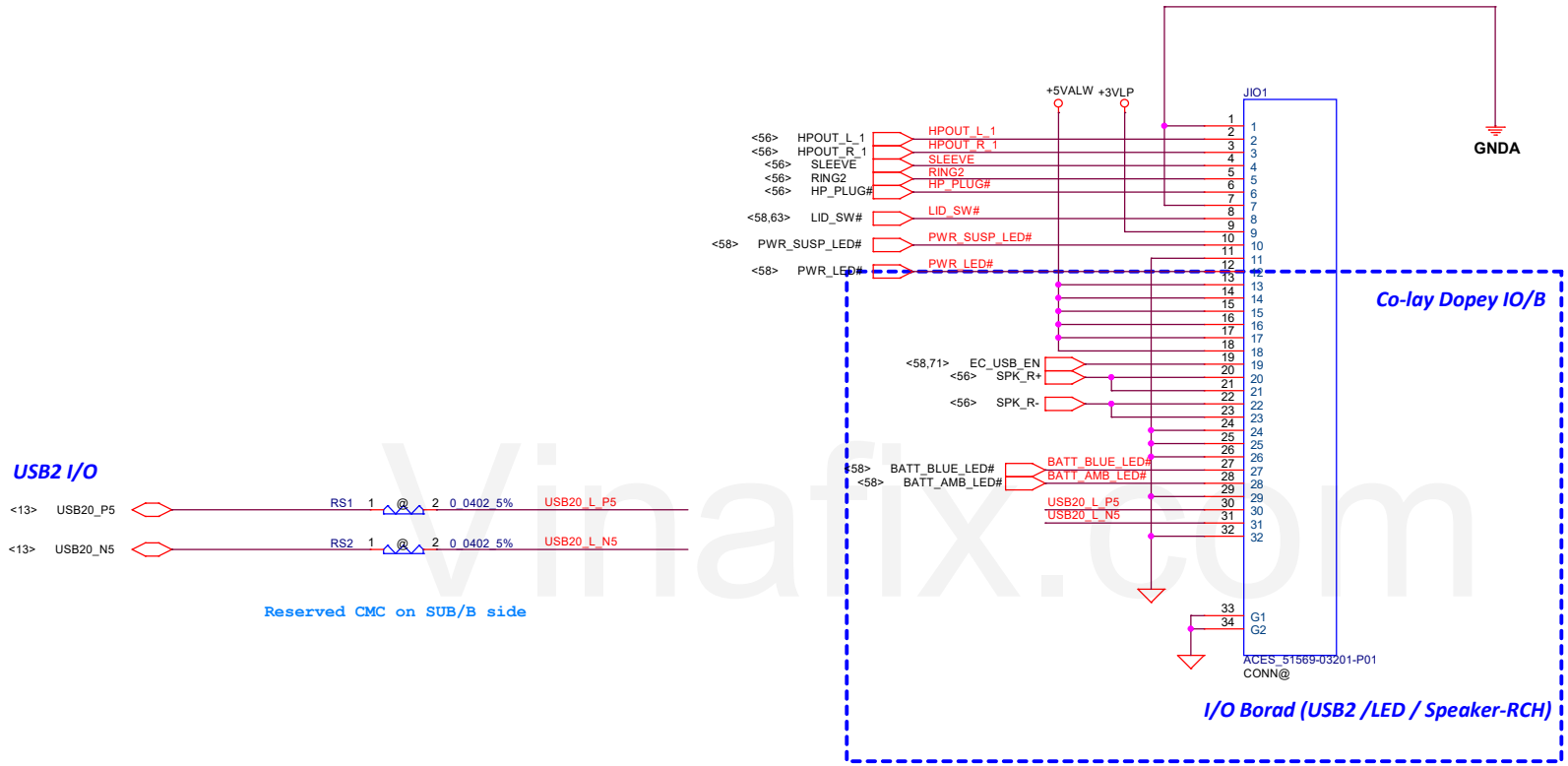
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: USB2/USB3 TYPEA1&2

Size: | Document Number: LA-K092P | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 71 of 102



Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.			
Title: Reserve USB2/USB3 TYPEA			
Size	Document Number: LA-K092P		Rev: 0.1
Date: Thursday, May 06, 2021		Sheet 72 of 102	

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve USB2/USB3 DB**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 73 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for Dock**

Size | Document Number: **LA-K092P** | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 74 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Reserve for USB**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 75 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

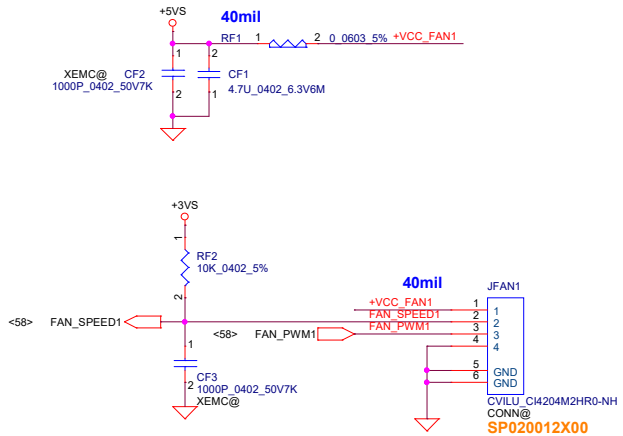
Compal Electronics, Inc.

Title: **Reserve for USB**

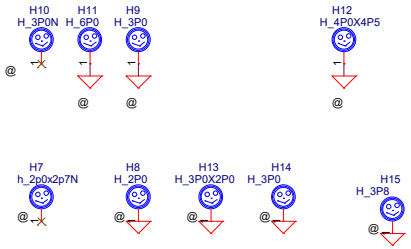
Size	Document Number	Rev
	LA-K092P	0.1

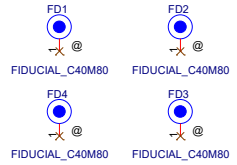
Date: Thursday, May 06, 2021 | Sheet 76 of 102

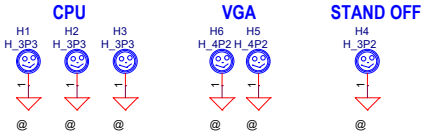
FAN1 Conn



Screw Hole

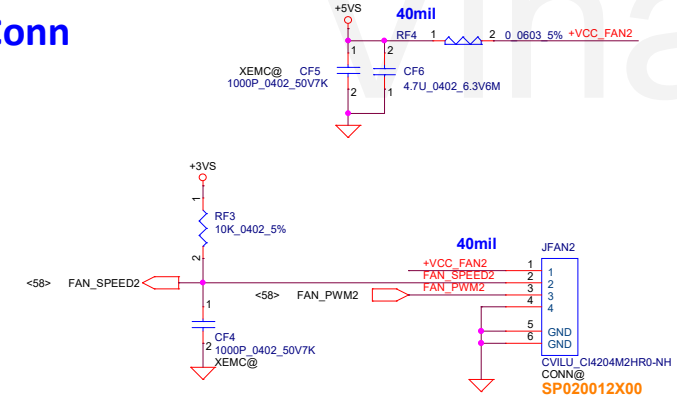




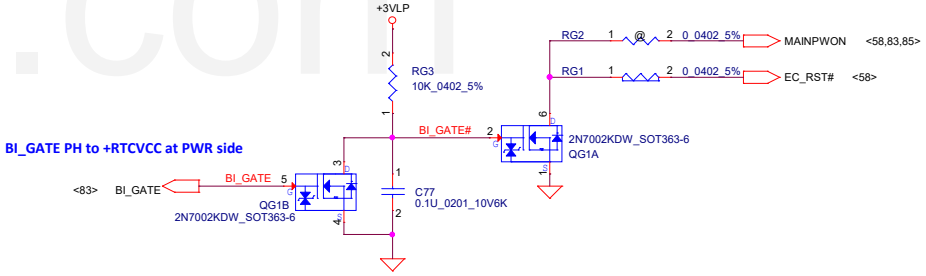


Clips

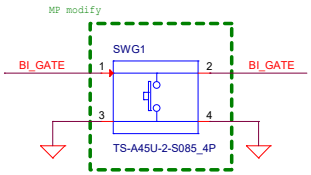
FAN2 Conn



Reset Circuit



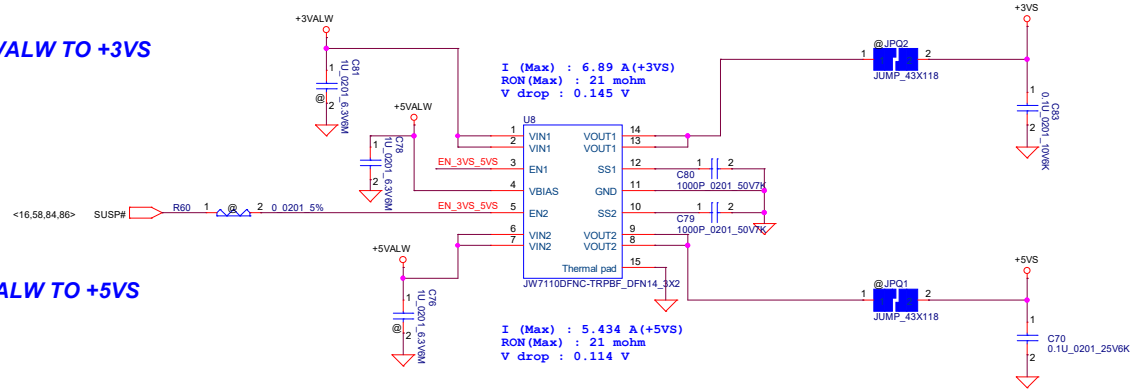
Reset Button



Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

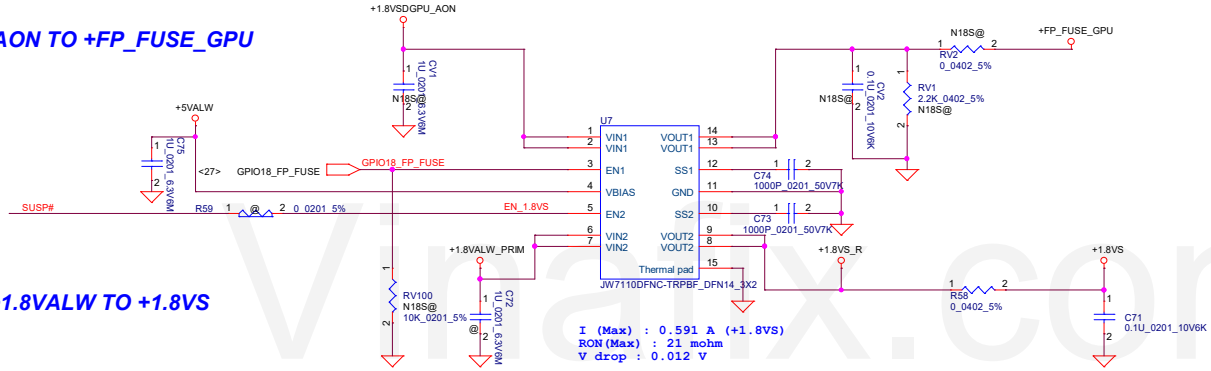
Compal Electronics, Inc.			
Title: FAN & Screw Hole & Reset			
Size: Custom	Document Number: FH5LI M/B LA-H801P		Rev: 1.0
Date: Thursday, May 06, 2021	Sheet 77 of 102		

+3VALW TO +3VS



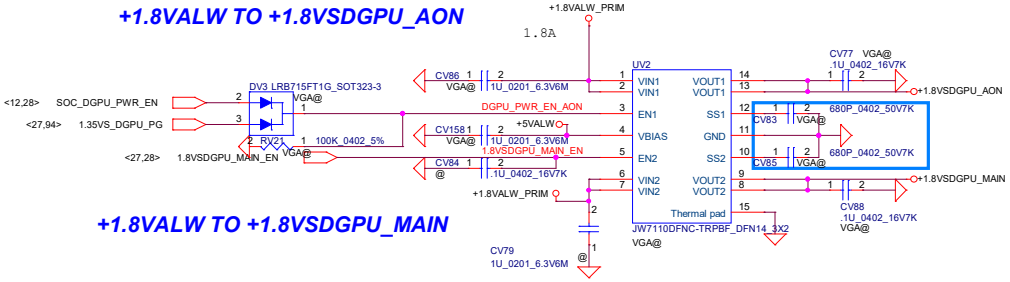
+5VALW TO +5VS

FOR N18S
+1.8VSDGPU_AON TO +FP_FUSE_GPU

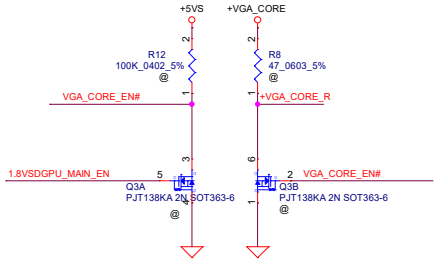


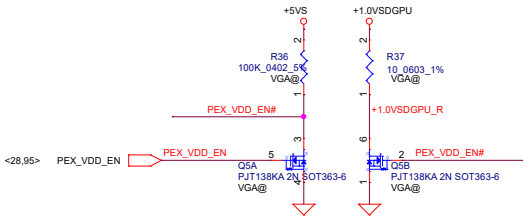
+1.8VALW TO +1.8VS

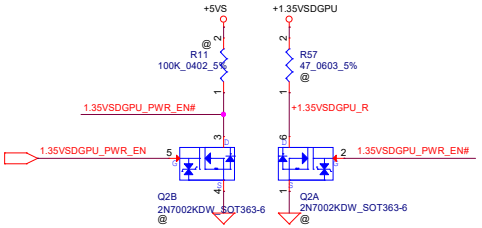
+1.8VALW TO +1.8VSDGPU_AON



+1.8VALW TO +1.8VSDGPU_MAIN







Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **DC Interface & Sequence Logic**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 Sheet 78 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **XDP/CMC/APS Debug Conn**

Size	Document Number	Rev
	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 79 of 102

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/12/31

Compal Electronics, Inc.

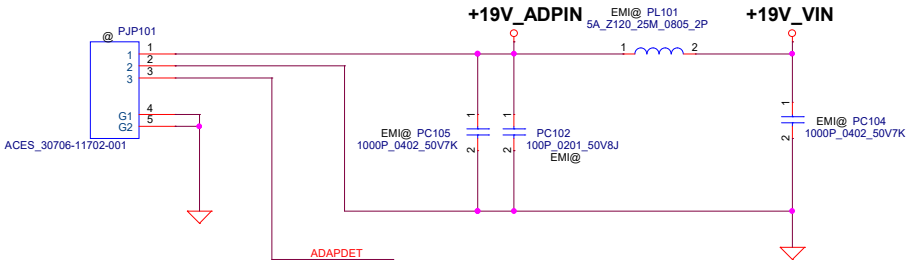
Title: **FIP Conn**

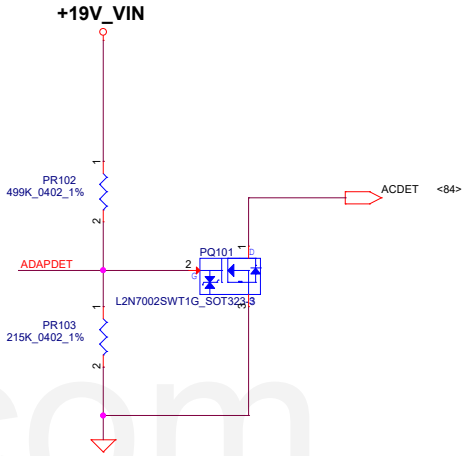
Size	Document Number	Rev
	LA-K092P	0.1

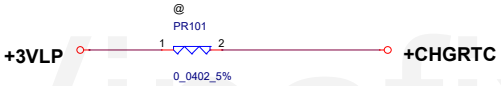
Date: Thursday, May 06, 2021 | Sheet 80 of 102

PWR-Reserve Page

Title	<Title>	
Size: A	Document Number: LA-K092P	Rev: 0.1
Date: Thursday, May 06, 2021	Sheet 81 of 102	







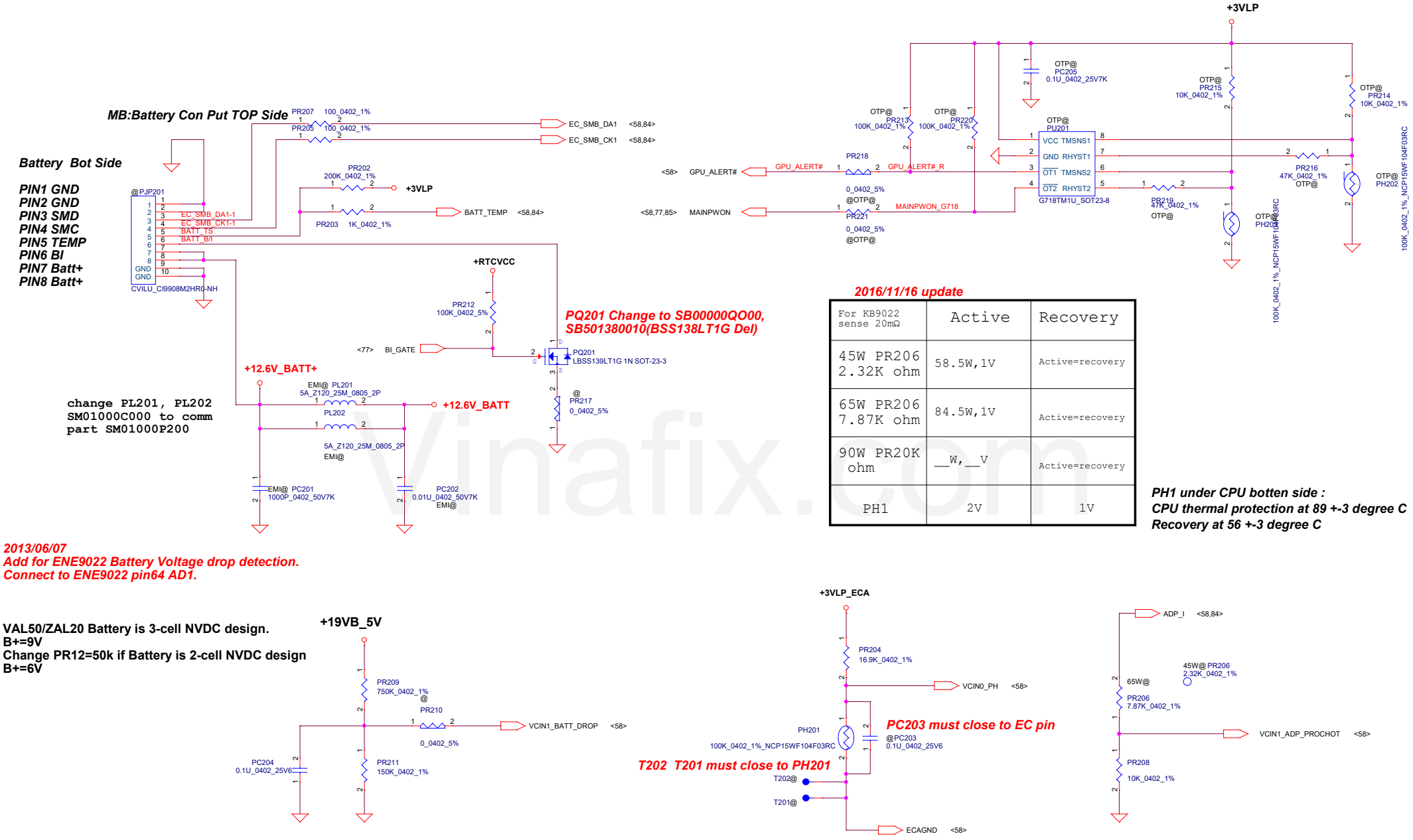
Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: **PWR DCIN / Pre-charge**

Size: Custom | Document Number: **LA-K092P** | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 82 of 102



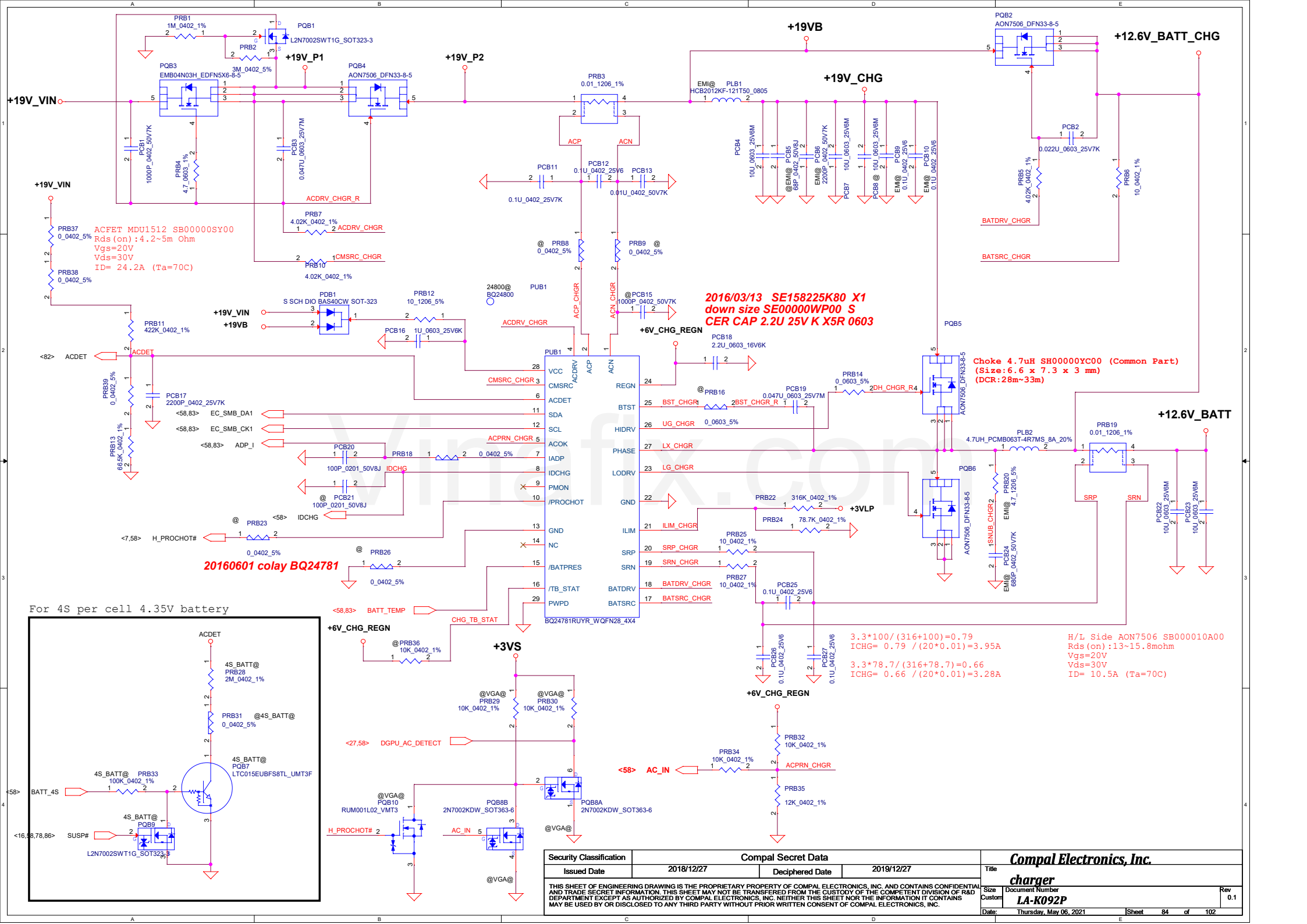
Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

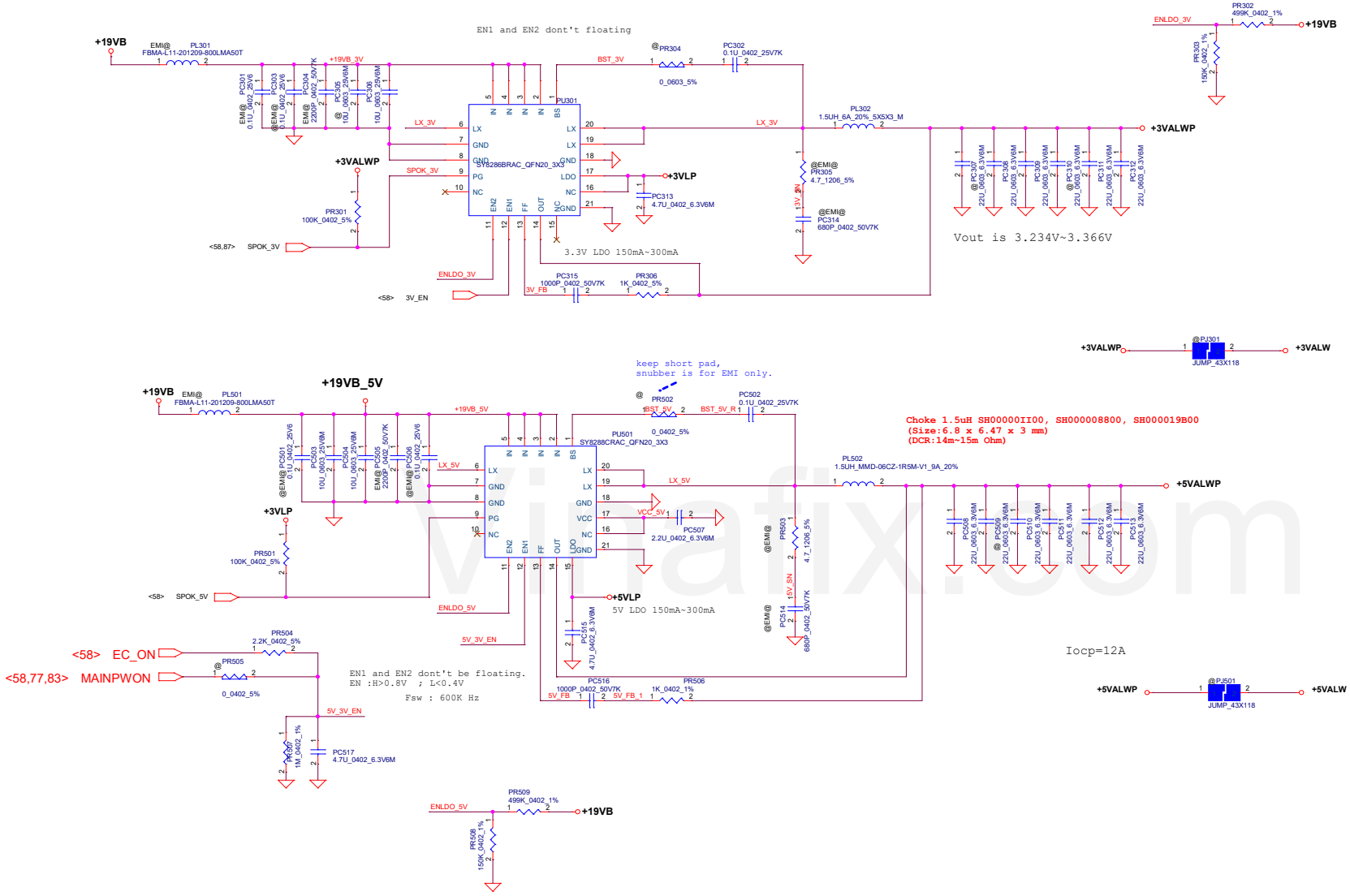
Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: LA-K092P | Rev: 0.1

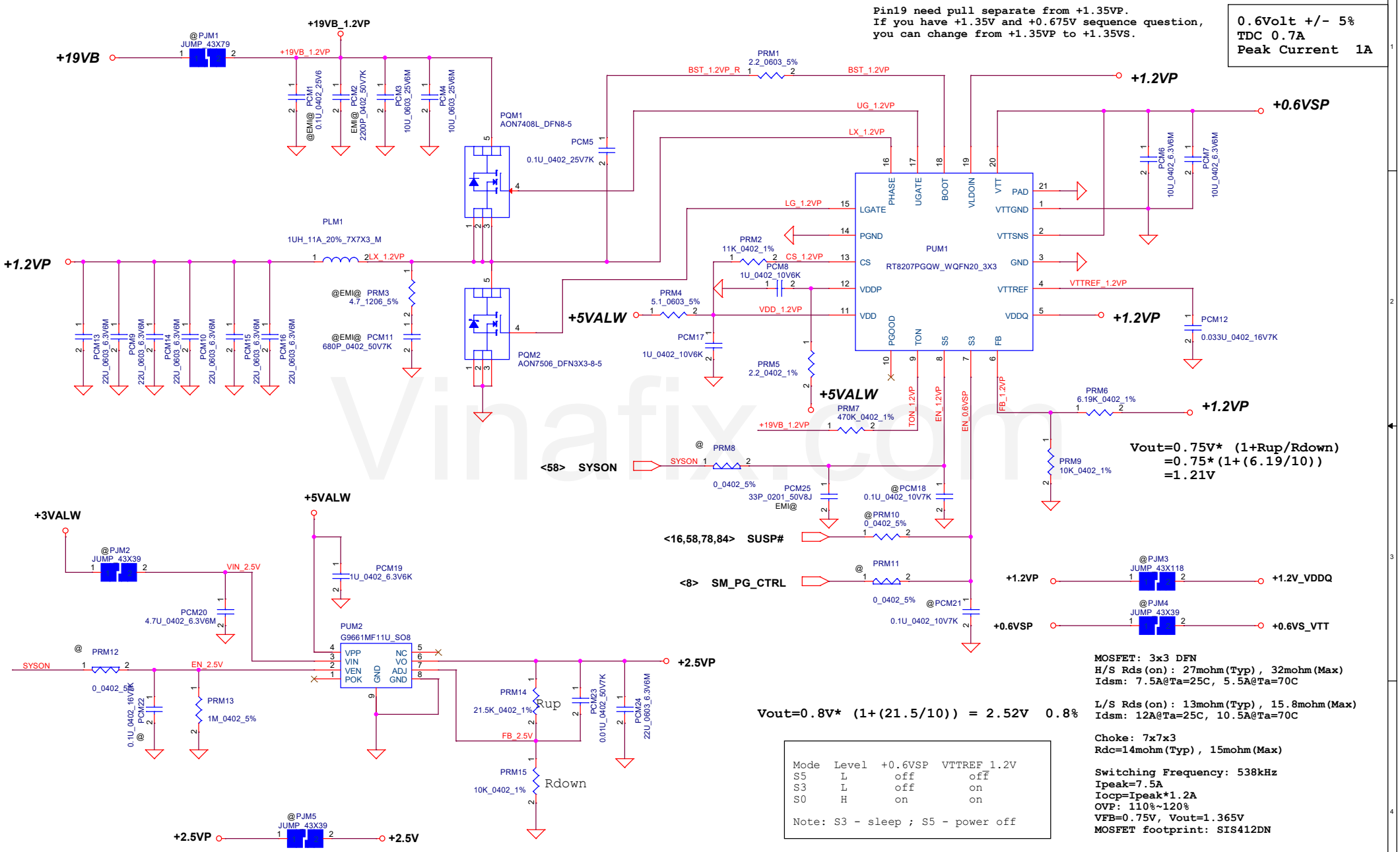
Date: Thursday, May 06, 2021 | Sheet 83 of 102





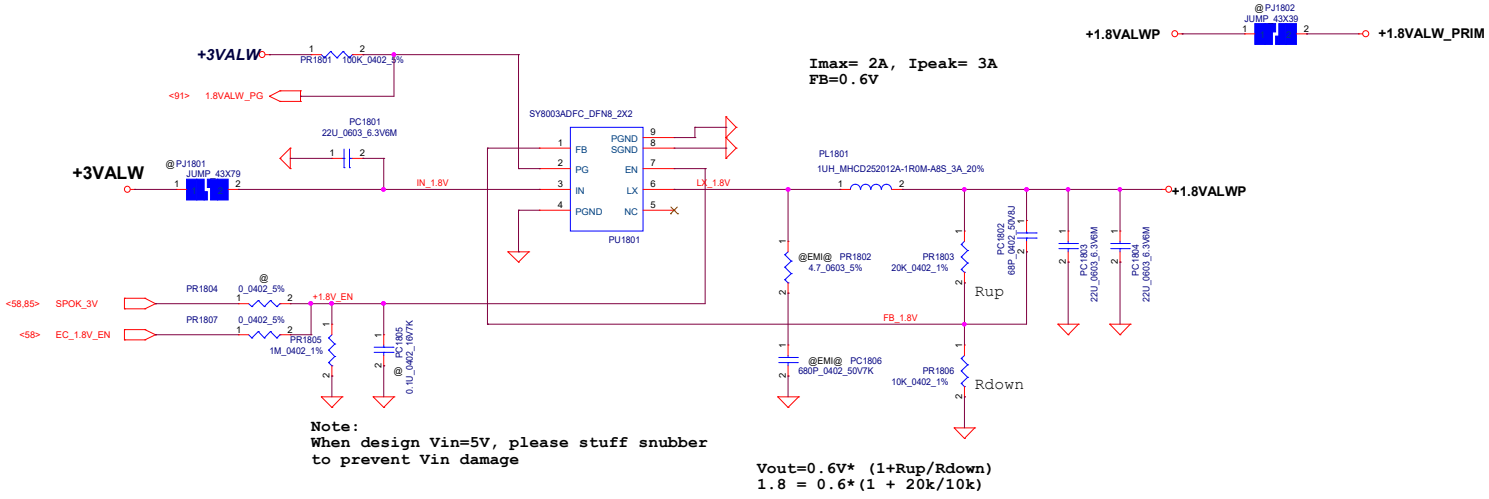
Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.			
Title	+3VALW/+5VALW		
Size: Custom	Document Number: LA-K092P		Rev: 0.1
Date: Thursday, May 06, 2021	Sheet 85 of 102		



Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.			
Title: RT8207P			
Size: Custom	Document Number: LA-K092P		Rev: 0.1
Date: Thursday, May 06, 2021	Sheet 86 of 102		



Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: SY8032

Size	Document Number	Rev
C	LA-K092P	0.1

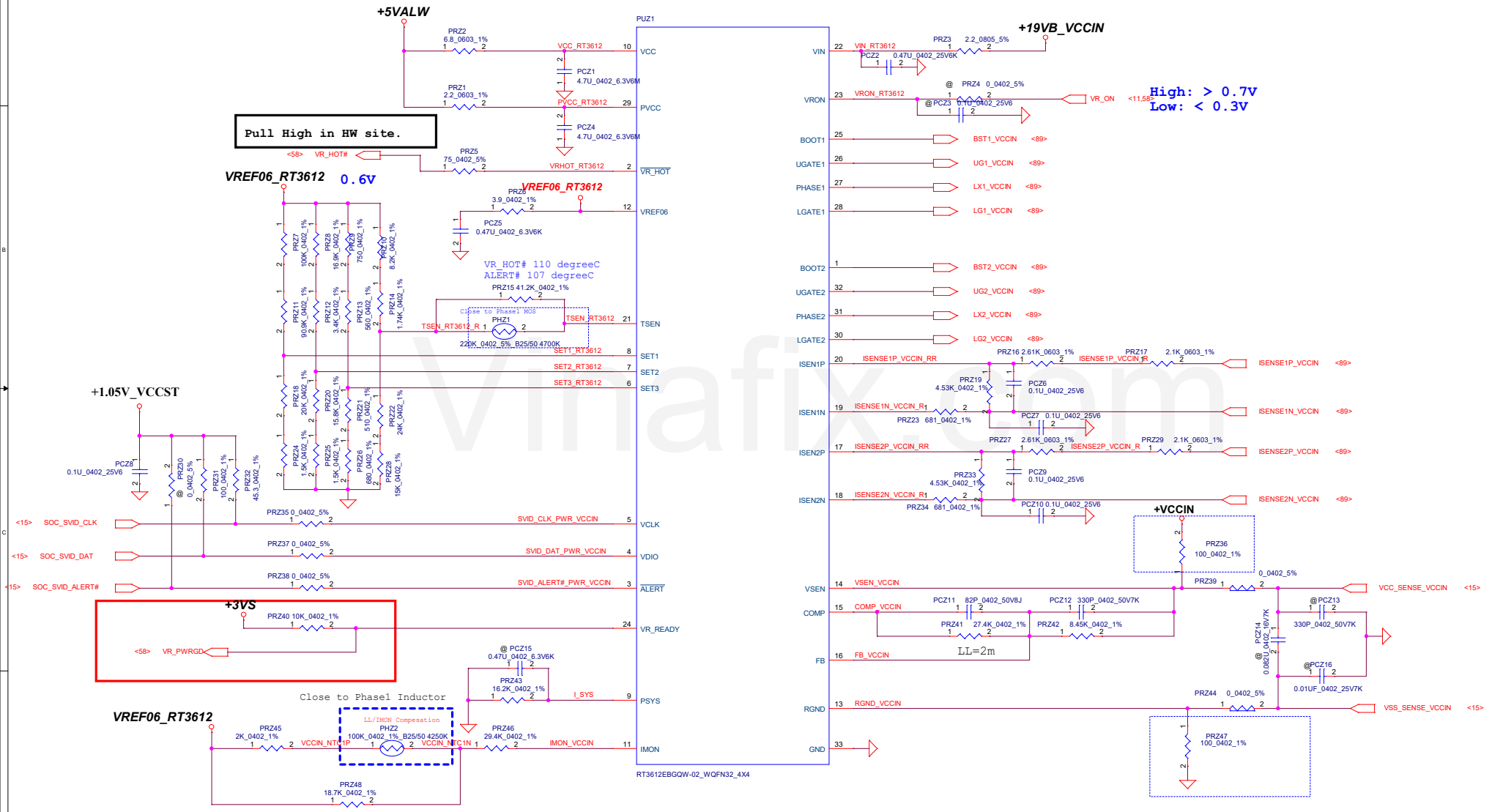
Date: Thursday, May 06, 2021 Sheet 87 of 102

Module model information

RT3612EB_2Phase_V1A.mdd for IC portion

RT3612EB_2Phase_V1B.mdd for SW portion

RT3612EBGQW-02 is not MP part



Security Classification	Compal Secret Data		
Issued Date	2019/05/15	Deciphered Date	2020/05/15

Compal Electronics, Inc.

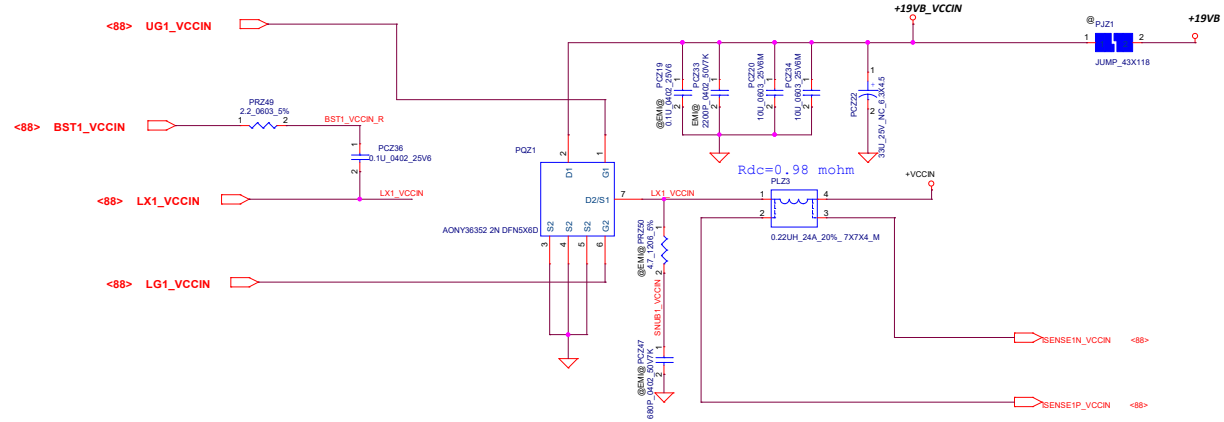
Title: +VCORE(RT3612EB)

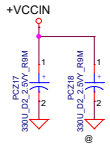
Size: Custom | Document Number | Rev: 0.1

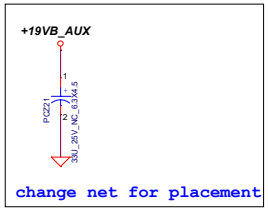
Date: Thursday, May 06, 2021 | Sheet 88 of 102

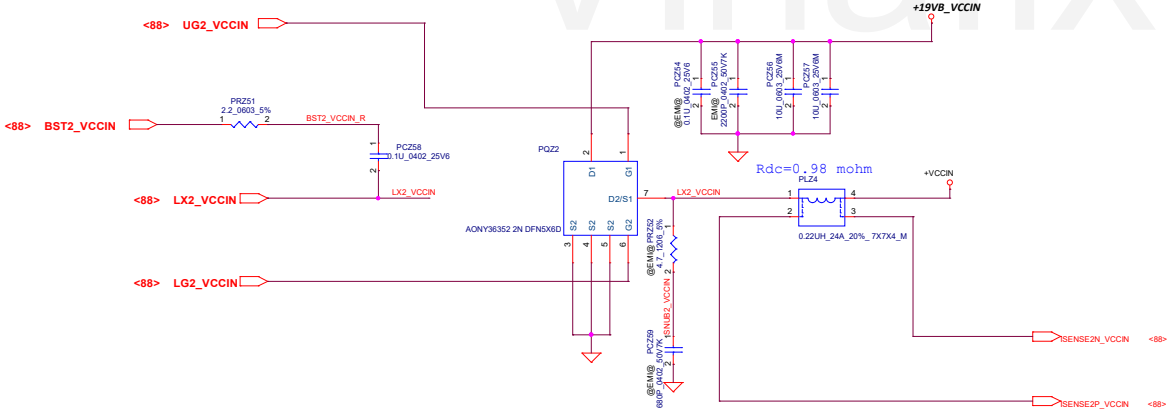
ICCMAX=47A
TDC=30A
OCP=61.1A
OVP=VID+0.35V=2.24V

Frequency 600KHz









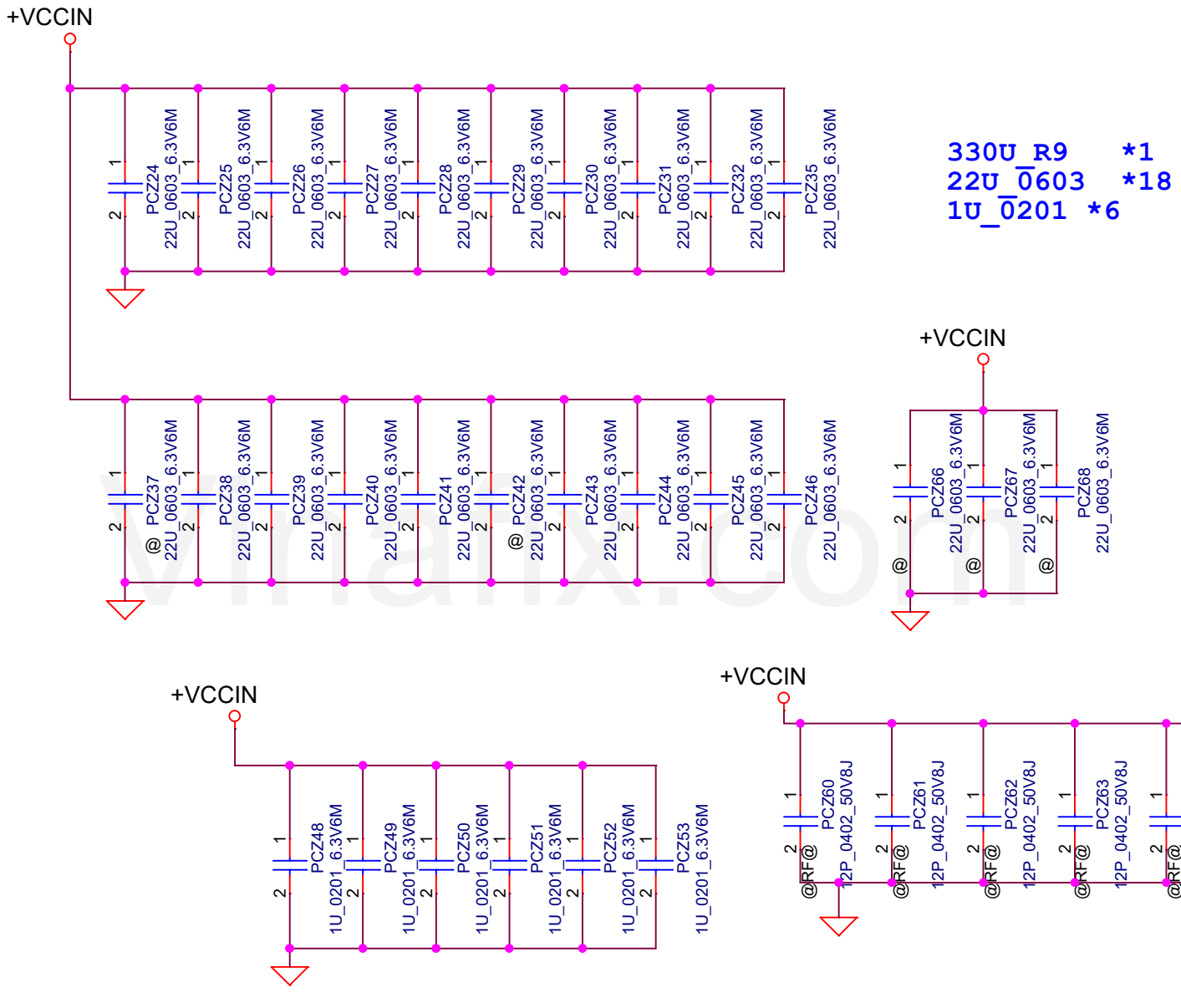
Security Classification	Compal Secret Data		
Issued Date	2019/05/15	Deciphered Date	2020/05/15

Compal Electronics, Inc.

Title: Power stage-VCCIN

Size: Custom | Document Number | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 89 of 102



Title	<Title>	
Size A	Document Number LA-K092P	Rev 0.1
Date: Thursday, May 06, 2021	Sheet 90 of 102	

Module model information

RT6543A_V1A.mdd for IC portion

RT6543A_V1B.mdd for SW portion

OCP is Lowside MOSFET Rdson sense

226K x1.2
255K x1.4

High > 1V
Low <0.4V

5V: 800KHz
Float: 600KHz
GND: 400KHz

AUX input cap need place 5pcs

ICCMAX=27A
TDC=14A

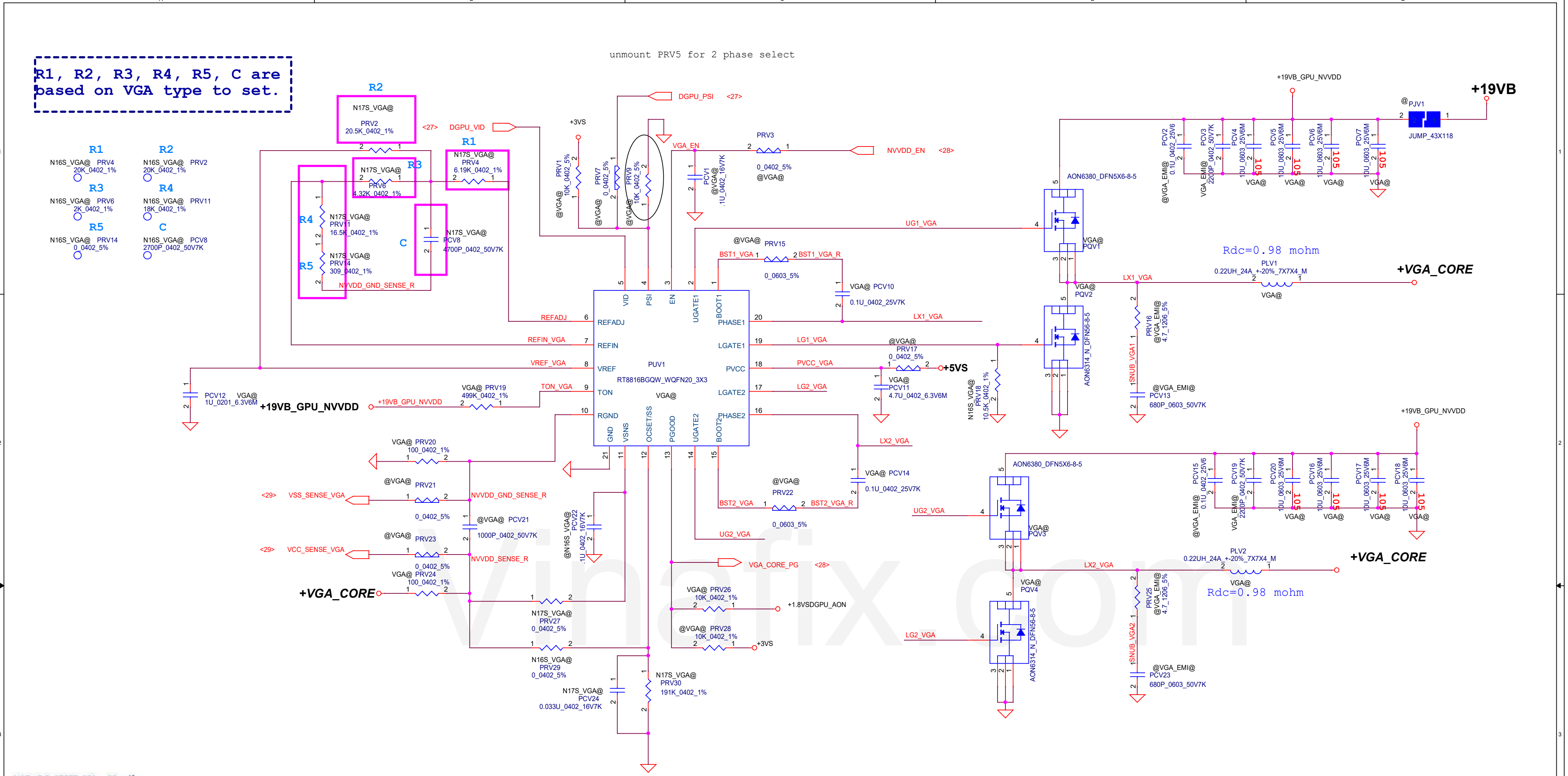
Rdc=0.98 mohm

330U_R9 *1
22U_0603 *13

VCCIN_AUX VID Follow Intel PDG Rev0.71

VID1	VID0	+VCCIN_AUX Voltage
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2019/05/15	Deciphered Date 2020/05/15	Title +VCCIN_AUX
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size Custom / Document Number / Rev 0.1
			Date: Thursday, May 06, 2021 Sheet 91 of 102



N17x DG-07875-001_v08.pdf:

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification	Unit	Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Vstep	mV	6.25

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.309
C	nF	4.7

Table 10. Output EDP-Continuous

Product	NVVDD – (A)	GPU FBIO 1.35V[4] (A)	FB Total[5] 1.35V[4] (A)	1.0V Total[1] 1.0V[4] (A)	1.8V Total[2] 1.8V[4] (A)
N17S-LG (0x1D12)	15.4	2.5	5.0	0.1	0.2
N17S-LG (0x1D52)	15.6	2.7	5.3	0.1	0.2
N17S-LP	19.6	3.1	7.1	0.3	0.5
N17S-G1	30.0	3.0	5.6	0.1	0.3
N17S-G0[6]	27.8	3.2	5.8	0.2	0.5
N17S-G2[6]	28.6	3.2	5.8	0.2	0.5
N17S-G3[6]	29.8	3.2	5.8	0.2	0.5
N17S-G4[6]	29.0	3.2	5.8	0.2	0.5
N17S-G5[6]	35.0	3.1	7.1	0.3	0.5

Table 11. Output EDP-Peak

Product	NVVDD – (A)	GPU FBIO 1.35V[3] (A)	FB TOTAL[4] 1.35V[3] (A)	1.0V Total[1] 1.0V[3] (A)
N17S-LG (0x1D12)	48.3	2.8	5.8	0.2
N17S-LG (0x1D52)	48.6	3.0	6.2	0.2
N17S-LP	69.9	3.1	7.6	0.4
N17S-G1	60.1	3.4	6.9	0.2
N17S-G0[5]	42.0	3.9	7.4	0.3
N17S-G2[5]	60.3	3.9	7.4	0.3
N17S-G3[5]	58.7	3.9	7.4	0.3
N17S-G4[5]	56.8	3.9	7.4	0.3
N17S-G5[5]	69.9	3.1	7.6	0.4

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

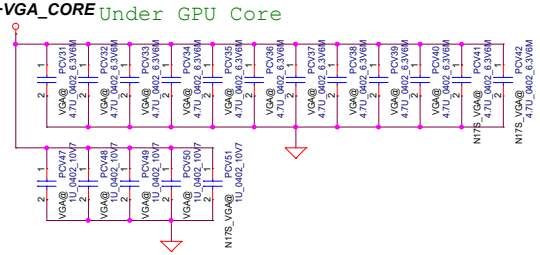
Compal Electronics, Inc.

Title: Power Train

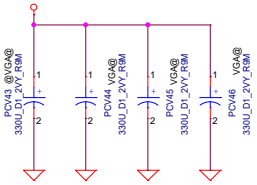
Size: C | Document Number: LA-K092P | Rev: 0.1

GB4-128 package

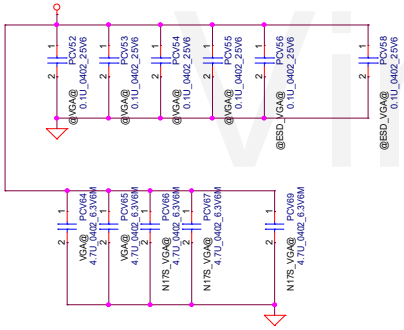
+VGA_CORE Under GPU Core



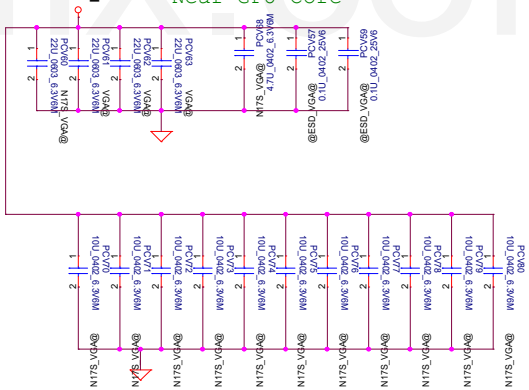
+VGA_CORE



+VGA_CORE



+VGA_CORE Near GPU Core



Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

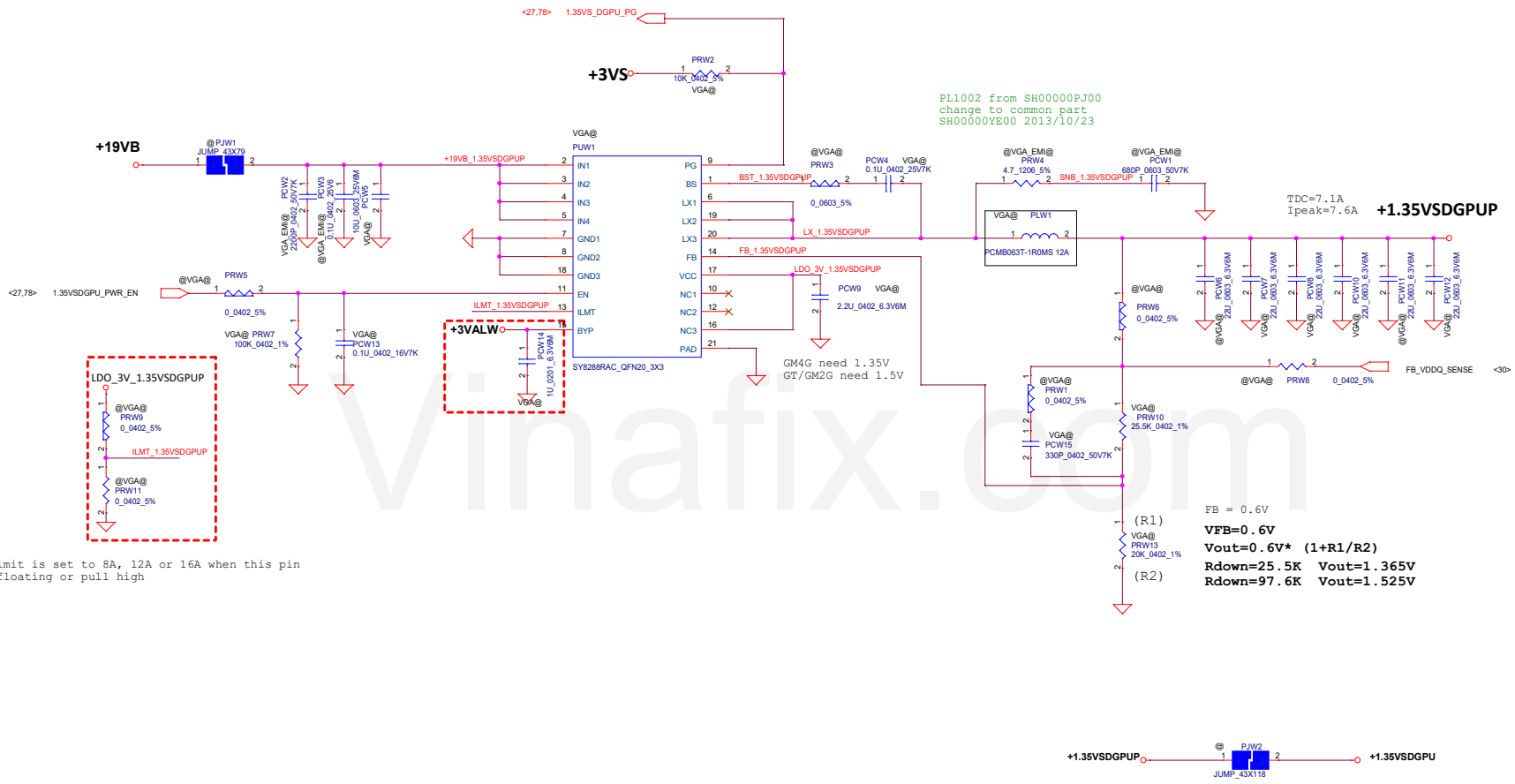
Title: Power Train

Size	Document Number	Rev
C	LA-K092P	0.1

Date: Thursday, May 06, 2021 | Sheet 93 of 102

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

PL1002 from SH00000PJ00
change to common part
SH00000YE00 2013/10/23



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

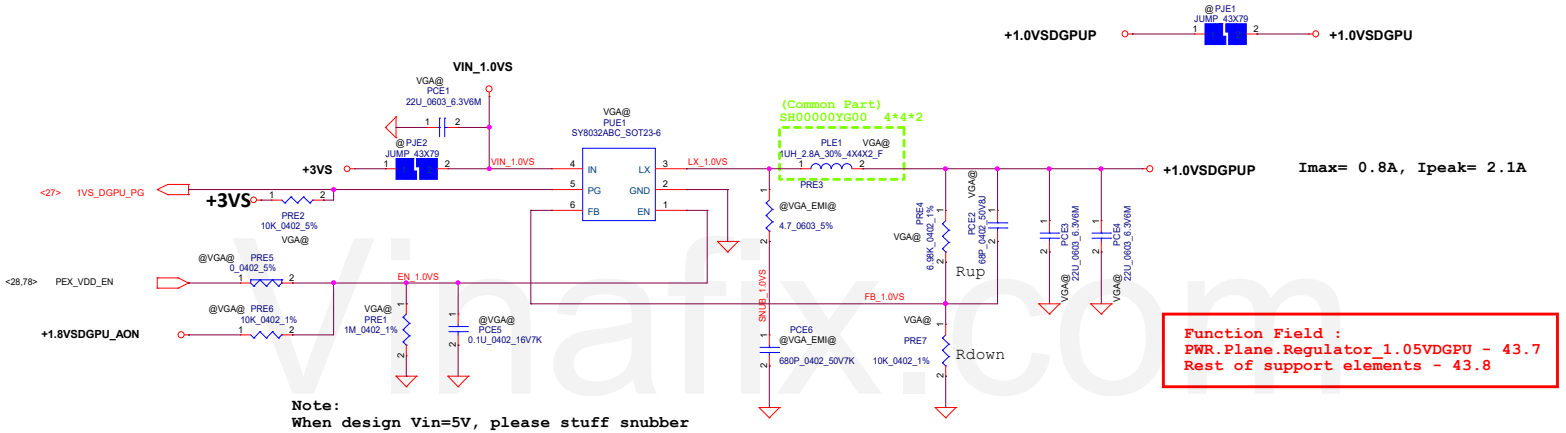
Title: Power Train

Size	Document Number	Rev
C	LA-K092P	0.1

Date: Thursday, May 06, 2021 Sheet 94 of 102

Module model information

SY8032_V2.mdd



Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: Power Train

Size	Document Number	Rev
C	LA-K092P	0.1

Date: Thursday, May 06, 2021 Sheet 95 of 102

PWR-Reserve Page

Title	<Title>	
Size: A	Document Number: LA-K092P	Rev: 0.1
Date: Thursday, May 06, 2021	Sheet 96 of 102	

PWR-Reserve Page

Title	<Title>	
Size: A	Document Number: LA-K092P	Rev: 0.1
Date: Thursday, May 06, 2021	Sheet 97 of 102	

PWR-Reserve Page

Title	<Title>	
Size: A	Document Number: LA-K092P	Rev: 0.1
Date: Thursday, May 06, 2021	Sheet 98 of 102	

PWR-Reserve Page

Title	<Title>	
Size: A	Document Number: LA-K092P	Rev: 0.1
Date: Thursday, May 06, 2021	Sheet 99 of 102	

PWR-Reserve Page

Title	<Title>	
Size: A	Document Number: LA-K092P	Rev: 0.1
Date: Thursday, May 06, 2021	Sheet 100 of 102	

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Change PRZ46 value for CPU transient test	Change PRZ46 value for CPU transient test		P.88	Change PRZ46 to 29.4K(SD034294280)	20/03/19	EVT
02	Change PU1801 solution for N18S-G5	Change PU1801 solution for N18S-G5		P.87	Change PU1801 to SY8003A (SA00007QP00)	20/03/19	EVT
03	Skin temperture over spec 5-7C	Skin temperture over spec 5-7C		P.92	Change PQV1-4 change to AONY36352 (SB00001P000)	20/03/19	EVT
04		change PN avoid material shortage		P.82,84, 86,91	Change PCG12 to SE000003W00 Change PCB18 to SE000006S80 Change PC102,PCB20 to SE00000SE00 Change PCM25 to SE00000TB00 Change PC202,PCB13,PCM23 to SE074103K80	20/03/25	EVT
05		Avoid MOS over working temperture		P.83	Pop PR218	20/03/30	EVT
06		change VGA mosfet for cost		P.92	Change PQV1 to SB00001GP00,add PQV3 SB00001GP00 Change PQV2 to SB00001GK00,add PQV4 SB00001GK00	20/04/17	DVT
07		change 0 ohm to R-short		P.83~95	PRB8,PRB9,PRB23,PRB31,PRE5,PRG9,PRM8,PRM11, PRM12,PRV3,PRV7,PRW5,PRZ4,PR218	20/05/28	DVT
08							
09							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: PIR

Size: Custom | Document Number: LA-K092P | Rev: 0.1

Date: Thursday, May 06, 2021 | Sheet 101 of 102

Title	<Title>	
Size: A	Document Number: LA-K092P	Rev: 0.1
Date: Thursday, May 06, 2021	Sheet 102 of 102	