Kylo-2 (LKL-2)
Whiskeylake-U Schematics

Project Code: 4PD0FC010001
PCB(Raw Card): 18724-1M

2018-10-17

LKL-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***COVER PAGE***		
Size: A4	Document Number: **Kylo-2**	Rev: **1M**
Date: Wednesday, October 17, 2018	Sheet 1 of 99	

Kylo-2 Whiskeylake Block Diagram

Project Code: 4PD0FC010001
PCB(Raw Card): 18724-1M

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating	Size
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

0402=> 1/16W, 25V
0603 => 1/16W, 75V
0805 => 1/10W, 100V

2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

DESCRIPTION

BOM control parts :
TEXT with PURPLE color near part reference

BOM control name
Part reference
Symbol name

PCB Layer Stackup

8 Layers FR4
L1:Component
L2:GND
L3:Signal 1
L4:VCC
L5:Signal 2
L6:Signal 3
L7:VCC
L8:Component

Battery Charger/Selector BQ25710ARSNR 44
VINT20_IN | 19V_DCBATOUT BT+

System DC/DC TPS51225BRUKR 45
19V_DCBATOUT | 5V_S5 3D3V_S5

IMVP8 Controller NCP81218MNTXG 46

DC/DC VCCCPUCORE NCP302045MNTXG 47
19V_DCBATOUT | 1V_CPU_CORE

DC/DC VCCGT NCP302035MNTXG 48
19V_DCBATOUT | 1V_VCCGT

DC/DC VCCSA NCP81253MNTBG 50
19V_DCBATOUT | 1V_VCCSA

DC/DC DDR4 VDDQ RT8231AGQW 51
19V_DCBATOUT | 1D2V_S3

DC/DC DDR4 VTT RT8231AGQW 51
1D2V_S3 | 0D6V_VREF_S0

DC/DC DDR4 VPP RT5797ALGQW 51
3D3V_S5 | 2D5V_S5

DC/DC 1D05V_S5 RT8231AGQW 52
19V_DCBATOUT | 1D0V_S5

DC/DC 1D8V_SUS RT5797ALGQW 53
3D3V_S5 | 1D8V_SUS

LCD
13.3" FHD/HD
Touch Panel (Yoga Only) 55
eDP 1.3 (2 Lanes)
Port 6 USB 2.0 480Mb/s

HDMI 29
DP/HDMI DEMUX PS8337B 56
DDI 5.4GT/s
DP
Type-C Port2 39
DP/USB MUX PS8747B 58
Port 2 USB3.0
Type-C Port1 39
DP/USB MUX PS8747B 37
DDI 5.4GT/s
Port 1 USB3.0

DDR4-SODIMM1 12
DDR4-SODIMM2 13
DDR4*2 2400MT/s

Wireless LAN Antenna
WLAN Card (Support CNVi) Bluetooth 61
Type-E M.2 2230
USB 2.0 Port 10 (BT)
Port 1 (1x) (Gen 2) (WLAN)

Type-C Port1 39 — Port 1
Type-C Port2 39 — Port 2
USB3.0 System Port (With AOU) 36 — Port 3
USB3.0 System Port 36 — Port 4
RGB Camera 66 — Port 5
Touch Screen (Yoga Only) 55 — Port 6
FingerPrint 92 — Port 7
IR Camera 66 — Port 8
World Facing Camera 66 — Port 9
BT in M.2 WLAN (Support CNVi) 61 — Port 10
USB2.0 x10 Ports
USB3.0 x4 Ports

CPU
Intel Whiskeylake-U Series
WHL PCH-LP
vPro / Non-vPro
ISH
ME
Clock Generator
3~11, 15~23

I2C (PCH_I2C0)
SM Bus_3B
I2C (ISH_I2C0)
C-Link 66MHz(Vpro only)
PCI Express x4 Ports
SATA 6Gb/s x1
IHDA
Port 4 (4x) (Gen 3) (SSD)
Port 2 (1x) (Gen 2) (GbE)
Port 3 (1x) (Gen 2) (Card)

SPI Flash 16MB (non-vPro) 32MB (vPro) 25
SPI
TPM 2.0 91
G-sensor (Yoga Only) LIS2DH12TR Angle Calculate 70
I2C (ISH_I2C0)
G-sensor KX022-1020 Thermal control 70
I2C
NFC 55
I2C

24MHz (X1801)
PECI 3.0
LPC Bus 24MHz
32.768KHz (X1802)

Type M.M.2 2242
SSD 63

GbE PHY Intel 219LM/V 31
25MHz (X3101)
MiniRJ45 32
Card Reader RTS5232S-GR 33
Micro SD Slot 33

HDA CODEC Realtek ALC3287-CG 27
Internal Mic
DMIC Module 66
Stereo Speaker 29
HP/MIC
30 Audio Jack (Microphone /Headphone)

Embedded Controller NPCE288 24
Hall Sensor HGDEDM013A 69
KBC_PWRBTN#
SMBus
Thermal Sensor NCT7717U NCT7718W 26
FAN 26

SM Bus_3B
ClickPad 65
Keyboard/Backlight TrackPoint 65

RTC Battery 25
Active Pen (Yoga Only)
Power Button 64
Power (3.3V)
KBC_PWRBTN#

USB Type-C Adapter
Battery Charger 44
I2C
Main Battery 43
DC/DC Converter 45

External Connector/Socket
Internal Connector/Socket
Internal Switch

LKL-2
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Title: BLOCK DIAGRAM
Size: A2 | Document Number: Kylo-2 | Rev: 1M
Date: Wednesday, October 17, 2018 | Sheet 2 of 99

Main Func = CPU

24 PECI_CPU
24,44,46 PROCHOT#_CPU

40 THERMTRIP#_CPU

99 PROC_TCK
99 PROC_TDI
99 PROC_TMS
99 PROC_TRST#
99 PCH_JTAG_TCK

99 PROC_PREQ#
99 PROC_PRDY#
99 PROC_TDO

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

1V_VCCSTG = 1.05 V

R301 1KR2J-1-GP
R302 499R2F-2-GP
R303 49D9R2F-GP
R304 49D9R2F-GP
R305 49D9R2F-GP
R308 1KR2J-1-GP
TP307 TPAD14-OP-GP

CPU1D 4 OF 20

CATERR# CPU
PECI CPU
PROCHOT# CPU R
THERMTRIP# CPU
CPU POPIRCOMP
PCH POPIRCOMP
GPP B4

CATERR# AA4
PECI AR1
PROCHOT# Y4
THRMTRIP# BJ1
BPM#0 U1
BPM#1 U2
BPM#2 U3
BPM#3 U4
GPP_E3/CPU_GP0 CE9
GPP_E7/CPU_GP1 CN3
GPP_B3/CPU_GP2 CB34
GPP_B4/CPU_GP3 CC35
PROC_POPIRCOMP BP27
PCH_OPIRCOMP BW25

PROC_TCK T6
PROC_TDI U6
PROC_TDO Y5
PROC_TMS T5
PROC_TRST# AB6
PCH_TCK W6
PCH_TDI U5
PCH_TDO W5
PCH_TMS P5
PCH_TRST# Y6
PCH_JTAGX P6
PROC_PREQ# W2
PROC_PRDY# W1

PROC_TCK
PROC_TDI
PROC_TDO
PROC_TMS
PROC_TRST#
PCH_JTAG_TCK

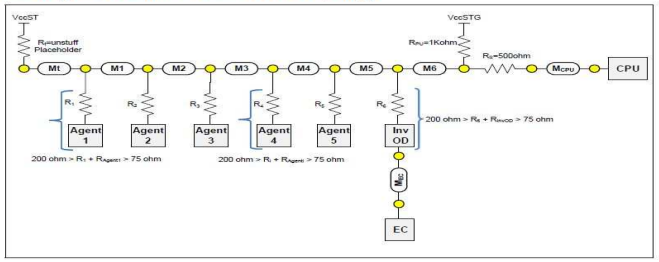
PROC_TDO R327 51R2J-2-GP
PROC_TCK R322 51R2J-2-GP
PCH_JTAG_TCK R326 51R2J-2-GP
DY

WHISKEY-LAKE-GP

ZZ.00CPU.271
CPU1 will use BOM control to Whiskeylake-U

(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

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Title: CPU (THML/JTAG)
Size: A3 | Document Number: Kylo-2 | Rev: 1M
Date: Wednesday, October 17, 2018 | Sheet 3 of 99

Main Func = CPU

USBC

37 DP1_DDI_TX_N0
37 DP1_DDI_TX_P0
37 DP1_DDI_TX_N1
37 DP1_DDI_TX_P1
37 DP1_DDI_TX_N2
37 DP1_DDI_TX_P2
37 DP1_DDI_TX_N3
37 DP1_DDI_TX_P3
37 DP1_AUX_CPU_N
37 DP1_AUX_CPU_P
37,38 USBC_HPD_MUX1

USBC

56 DP2_DDI_TX_N0
56 DP2_DDI_TX_P0
56 DP2_DDI_TX_N1
56 DP2_DDI_TX_P1
56 DP2_DDI_TX_N2
56 DP2_DDI_TX_P2
56 DP2_DDI_TX_N3
56 DP2_DDI_TX_P3
56 DP2_AUX_CPU_N
56 DP2_AUX_CPU_P
56 DP2_HPD_CPU

56 DP2_SCL_CPU
56 DP2_SDA_CPU

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1

55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
55 eDP_HPD_CPU

24 L_BKLT_EN
55 L_BKLT_CTRL
55 EDP_VDD_EN

15 GPP_H17_STRAP

24 EC_SCI#

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

1V_VCCIO
CHECK WHL design guide: DISP_RCOMP
R401
24D9R2F-L-GP
eDP_RCOMP_CPU
AM6 DISP_RCOMP

3D3V_S0
RN401
SRN2K2J-1-GP
DP1_SDA_CPU
RN402
SRN2K2J-1-GP
DP2_SCL_CPU
DP2_SDA_CPU

CPU1A
1 OF 20

DP1_DDI_TX_N0 AL5 DDI1_TXN0
DP1_DDI_TX_P0 AL6 DDI1_TXP0
DP1_DDI_TX_N1 AJ5 DDI1_TXN1
DP1_DDI_TX_P1 AJ6 DDI1_TXP1
DP1_DDI_TX_N2 AF6 DDI1_TXN2
DP1_DDI_TX_P2 AF5 DDI1_TXP2
DP1_DDI_TX_N3 AE5 DDI1_TXN3
DP1_DDI_TX_P3 AE6 DDI1_TXP3

DP2_DDI_TX_N0 AC4 DDI2_TXN0
DP2_DDI_TX_P0 AC3 DDI2_TXP0
DP2_DDI_TX_N1 AC1 DDI2_TXN1
DP2_DDI_TX_P1 AC2 DDI2_TXP1
DP2_DDI_TX_N2 AE4 DDI2_TXN2
DP2_DDI_TX_P2 AE3 DDI2_TXP2
DP2_DDI_TX_N3 AE1 DDI2_TXN3
DP2_DDI_TX_P3 AE2 DDI2_TXP3

AG4 EDP_TXN0 eDP_TX_CPU_N0
AG3 EDP_TXP0 eDP_TX_CPU_P0
AG2 EDP_TXN1 eDP_TX_CPU_N1
AG1 EDP_TXP1 eDP_TX_CPU_P1
AJ4 EDP_TXN2
AJ3 EDP_TXP2
AJ2 EDP_TXN3
AJ1 EDP_TXP3

AH4 EDP_AUX_N eDP_AUX_CPU_N
AH3 EDP_AUX_P eDP_AUX_CPU_P
AM7 DISP_UTILS
AC7 DDI1_AUX_N DP1_AUX_CPU_N
AC6 DDI1_AUX_P DP1_AUX_CPU_P
AD4 DDI2_AUX_N DP2_AUX_CPU_N
AD3 DDI2_AUX_P DP2_AUX_CPU_P
AG7 DDI3_AUX_N
AG6 DDI3_AUX_P

CN6 GPP_E13/DDPB_HPD0/DISP_MISC0 USBC_HPD_MUX1
CM6 GPP_E14/DDPC_HPD1/DISP_MISC1 DP2_HPD_CPU
CP7 GPP_E15/DPPD_HPD2/DISP_MISC2 EC_SCI#
CP6 GPP_E16/DPPE_HPD3/DISP_MISC3
CM7 GPP_E17/EDP_HPD/DISP_MISC4 eDP_HPD_CPU

CK11 EDP_BKLTEN L_BKLT_EN
CG11 EDP_VDDEN EDP_VDD_EN
CH11 EDP_BKLTCTL L_BKLT_CTRL

DP1_SDA_CPU CC5 GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
CC6 GPP_E19/DPPB_CTRLDATA
DP2_SCL_CPU CH4 GPP_E20/DPPC_CTRLCLK
DP2_SDA_CPU CH3 GPP_E21/DPPC_CTRLDATA
CP4 GPP_E22/DPPD_CTRLCLK
CN4 GPP_E23/DPPD_CTRLDATA
GPP_H17_STRAP CR26 GPP_H16/DDPF_CTRLCLK
reserved for strap CP26 GPP_H17/DDPF_CTRLDATA

WHISKEY-LAKE-GP
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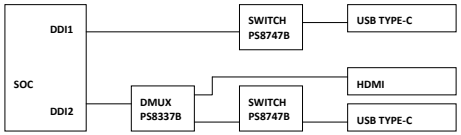
CPU1 will use BOM control to Whiskeylake-U

R404 10KR2J-1-GP
R403 10KR2J-1-GP
R402 10KR2J-1-GP

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

TABLE: Functional Strap

DDPB_CTRLDATA **HIGH Port B is detected.** **LOW Port B is not detected.**
DDPC_CTRLDATA **HIGH Port C is detected.** **LOW Port C is not detected.**



Vinafix.com

LKL-2

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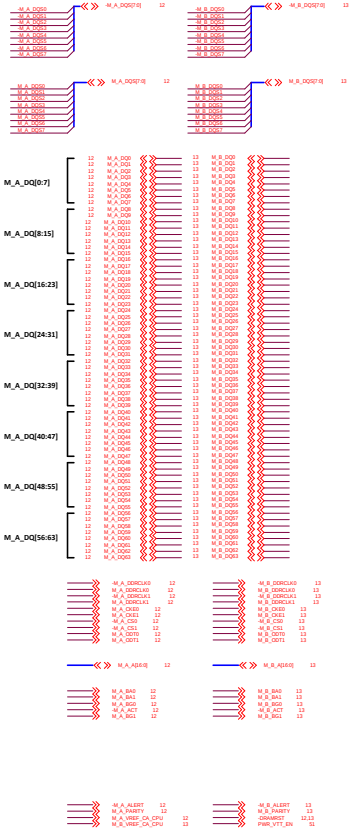
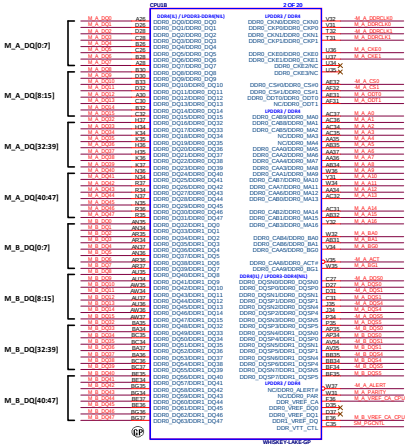
Title: CPU (DDI/EDP)
Size: A2 | Document Number: Kylo-2 | Rev: 1M
Date: Wednesday, October 17, 2018 | Sheet 4 of 99

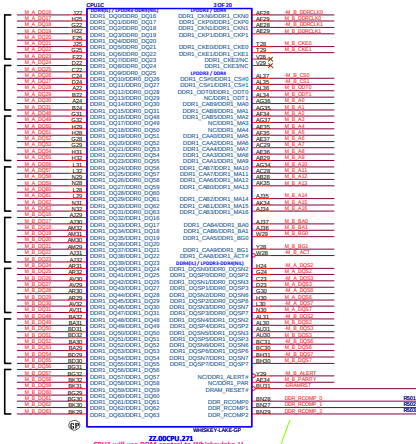
Main Func = CPU

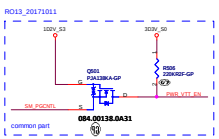
DDR4 ball type: Non-Interleaved Type

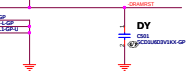




DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.







DDP: 121 ohm (64.12105.6DL)
SDP: 200 ohm (64.20005.6DL)

Layout Note:

#575412
Table 4-3. WHL U DDR4 SODIMM Signal Routing Guidelines (mils)
Design Guideline:
SM_RCOMP_0/1/2 keep routing length less than 500 mils.

#575412
Table 3-1. RCOMP Recommendation for WHL and CFL
DDR - DDR4 SODIMM
DDR_RCOMP[0]: 121Ω ±1% on pkg to VSS
DDR_RCOMP[1]: 80.6Ω ±1% on pkg to VSS
DDR_RCOMP[2]: 100Ω ±1% on pkg to VSS

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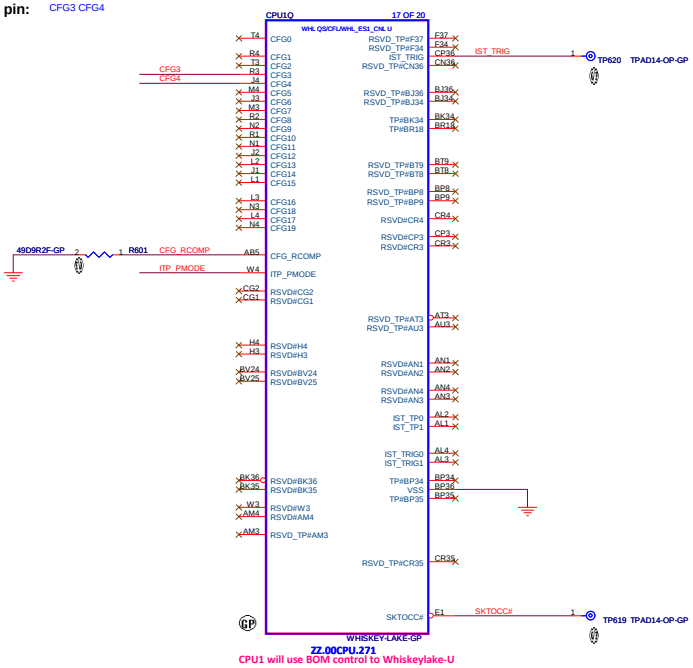
Title: CPU(CFG/IST)
Size: A3 | Document Number: Kylo-2 | Rev: 1M
Date: Wednesday, October 17, 2018 | Sheet 5 of 59

Main Func = CPU

15,99 CFG3
15 CFG4

99 ITP_PMODE

PCH strap pin: CFG3 CFG4



ZZ.00CPU.271

CPU1 will use BOM control to Whiskeylake-U

LKL-2

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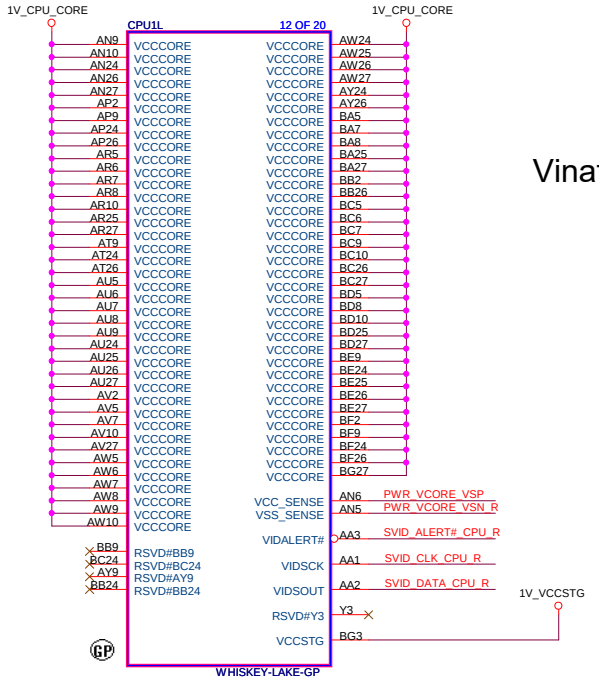
Title: CPU(CFG/IST)		
Size: A2	Document Number: Kylo-2	Rev: 1M
Date: Wednesday, October 17, 2018	Sheet 6 of 99	

Main Func = CPU

46 PWR_VCORE_VSP
46 PWR_VCORE_VSN_R
46 PWR_VCORE_ALERT#
46 VIDSCK_CPU_R
46 VIDSOUT_CPU_R



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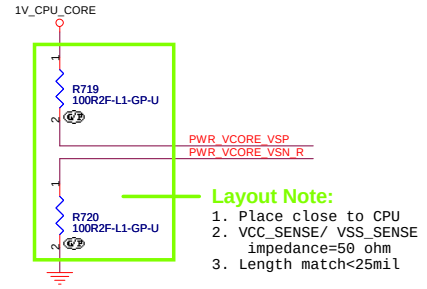
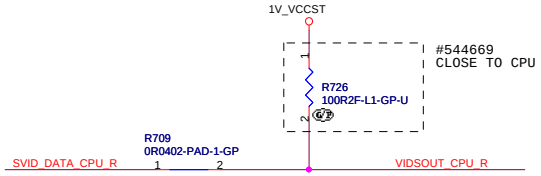
CPU1 will use BOM control to Whiskeylake-U

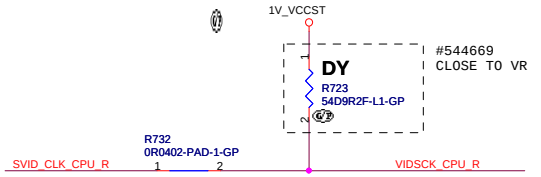


Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID DATA



SVID CLOCK



SVID ALERT

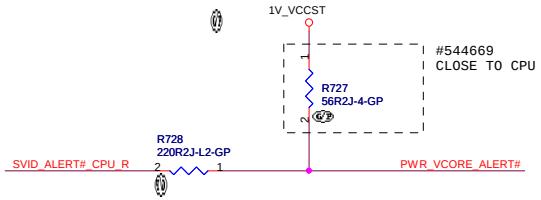


Figure 10-7. Routing Illustration for SVID Topology

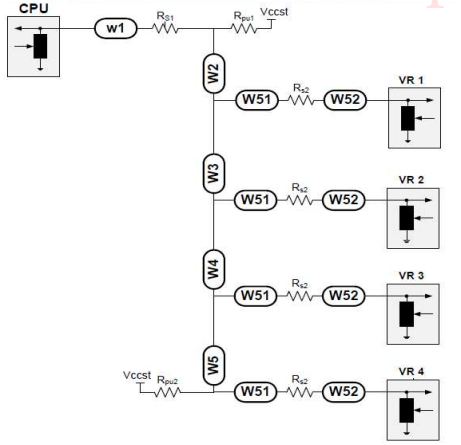


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

LKL-2

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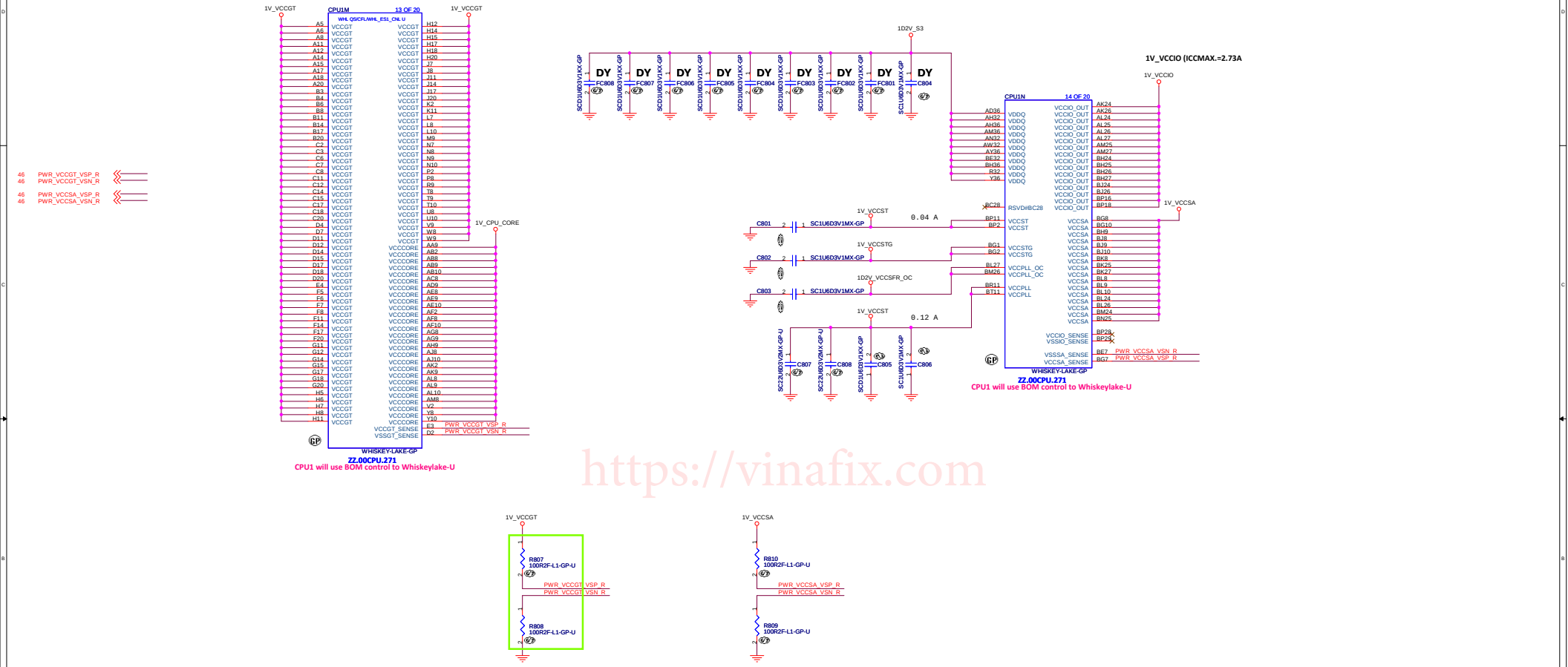
Title: CPU (VCC_CORE)
Size: A3 | Document Number: Kylo-2 | Rev: 1M
Date: Wednesday, October 17, 2018 | Sheet 7 of 99

Main Func = CPU

KL2_SIT_MB_W006
KL2_SIT_MB_W029
KL2_SOVP_MB_W002



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Title: CPU (VDDQ/VCC/VCCST/VCCSTG)

Size	Document Number	Rev
A2	Kylo-2	1M

Date: Wednesday, October 17, 2018 Sheet 8 of 99

BLANK

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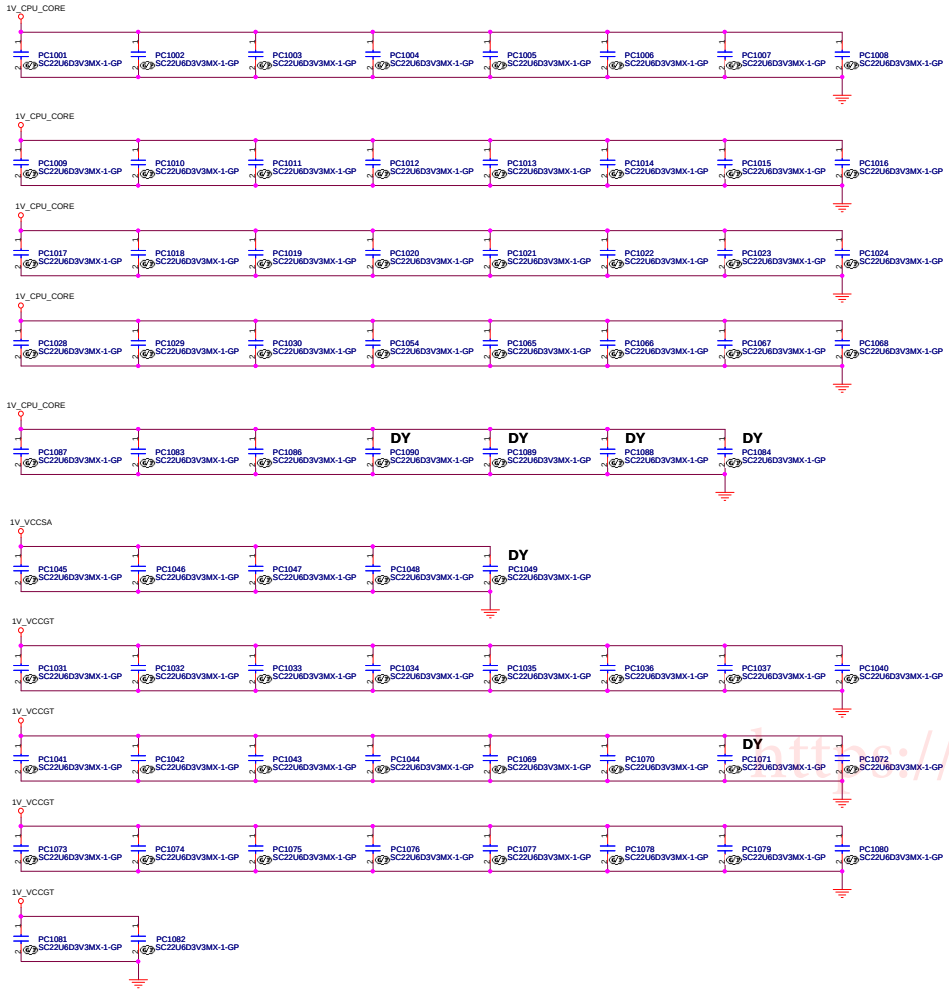
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (RSVD)***

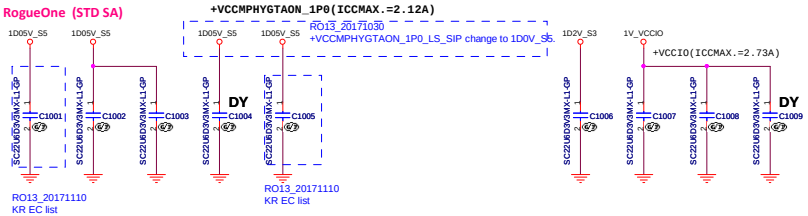
Size	Document Number	Rev
A4	Kylo-2	1M

Date: Wednesday, October 17, 2018 Sheet 9 of 99

Main Func = CPU



RogueOne (STD SA)



RO13_20171110
KR EC list

RO13_20171110
KR EC list

LKL-2

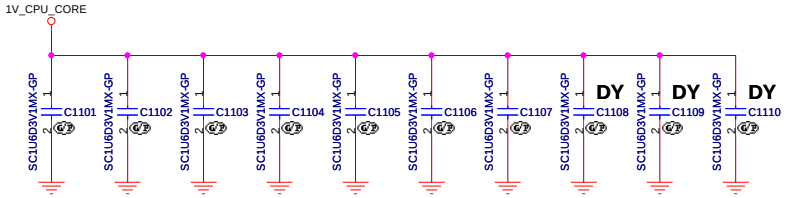
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (POWER CAP1)

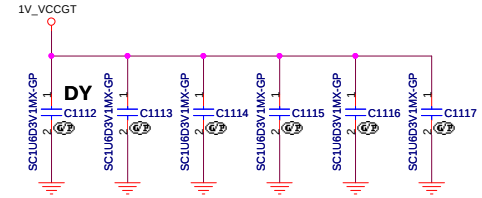
Size: A2 | Document Number: Kylo-2 | Rev: 1M

Date: Wednesday, October 17, 2018 | Sheet 10 of 99

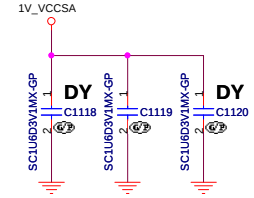
VCORE WHL U42



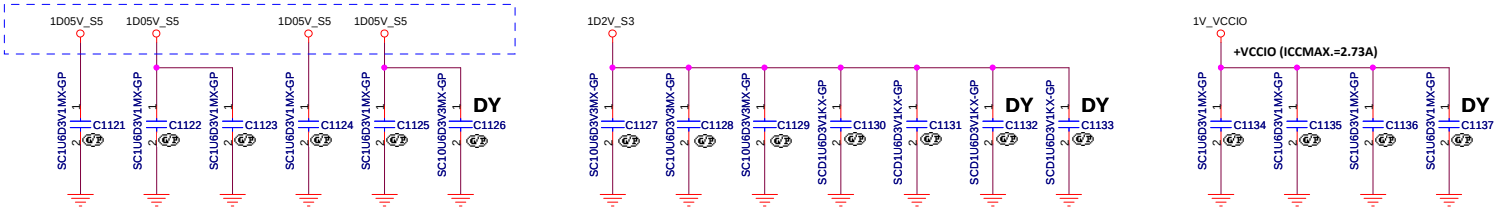
VCCGT WHL U42



VCCSA WHL U42



RO13_20171030
+VCCMPHYGTAON_1P0_LS_SIP change to 1D0V_S5.

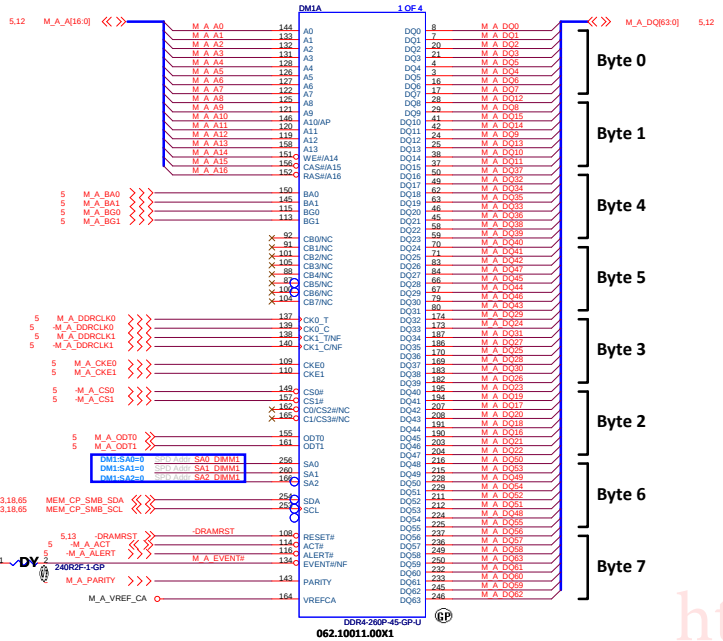


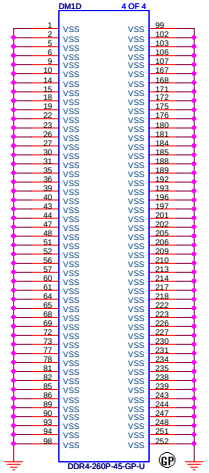
LKL-2

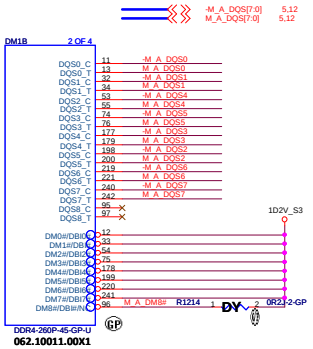
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU (POWER CAP2)		
Size: A3	Document Number: Kylo-2	Rev: 1M
Date: Wednesday, October 17, 2018	Sheet 11 of 99	

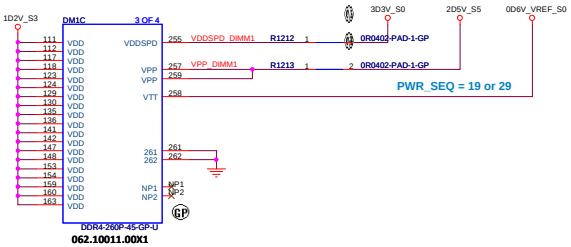
KL2_SIT_MB_W006

CHANNEL-A XMM1, A0, H=4.0mm

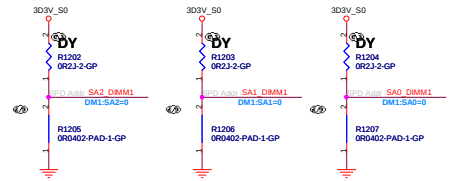








SPD Address of DM1



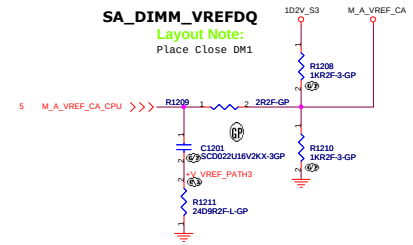
SPD SA2	0
SPD SA1	0
SPD SA0	0

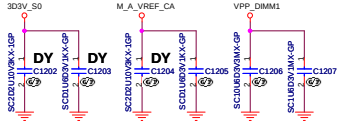
Note:
SA0 DM1 = 0, SA1_DM1 = 0
SA2 DM1 = 0
SO-DIMMA SPD Address is 0xA0

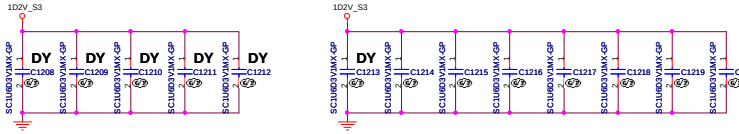
VREF CIRCUITRY

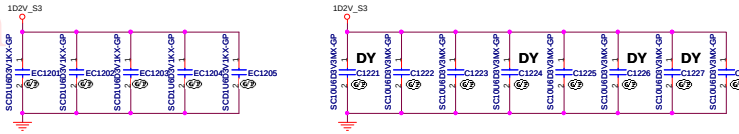
SA_DIMM_VREFDQ

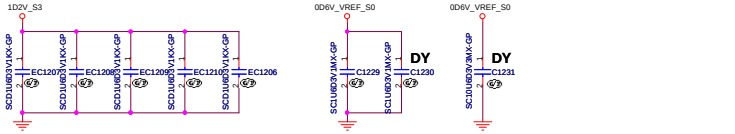
Layout Note:
Place Close DM1











LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-CHA SODIMM)

Size: A2 | Document Number: Kylo-2 | Rev: 1M

Date: Wednesday, October 17, 2018 | Sheet 12 of 99

CHANNEL-B XMM1, A0, H=4.0mm

5,13 M_B_A[16:0]
5,13 M_B_DQ[63:0]
5,13 -M_B_DQS[7:0]
5,13 M_B_DQS[7:0]

SPD Address of DM2

SPD SA2	0
SPD SA1	0
SPD SA0	1

3D3V_S0
R1302 0R2J-2-GP — SPD Addr: SA2_DIMM2 — DM2:SA2=0
R1303 0R2J-2-GP — SPD Addr: SA1_DIMM2 — DM2:SA1=0
R1304 0R0402-PAD-1-GP — SPD Addr: SA0_DIMM2 — DM2:SA0=1
R1305 0R0402-PAD-1-GP
R1306 0R0402-PAD-1-GP
R1307 0R2J-2-GP

Note:
SA0 DM2 = 1, SA1_DM2 = 0
SA2 DM2 = 0
SO-DIMMB SPD Address is 0xA2

VREF CIRCUITRY

SA_DIMM_VREFDQ
Layout Note:
Place Close DM2

1D2V_S3 — R1308 1KR2F-3-GP — M_B_VREF_CA
5 M_B_VREF_CA_CPU — R1309 2R2F-GP — C1301 SCD022U16V2KX-3GP — 1V_VREF_PATH4 — R1311 24D9R2F-L-GP — R1310 1KR2F-3-GP

3D3V_S0: C1302 SC2ZDU10V0KX-1GP, C1303 SCDU0B3V1KX-GP
M_B_VREF_CA: C1304 SC2ZDU10V0KX-1GP, C1305 SCDU0B3V1KX-GP
VPP_DIMM2: C1306 SCU0U0B3V0GMX-GP, C1307 SC1U16D3V1MX-GP

1D2V_S3: C1308–C1312 SCU0U0B3V1MX-GP
C1313–C1320 SCU0U0B3V1MX-GP
C1321–C1328 SCU0U0B3V0MX-GP
0D6V_VREF_S0: C1329 SCU0U0B3V3MX-GP, C1330, C1331

DM2A — 1 OF 4

DDR4-260P-45-GP-U
062.10011.00X1

Pin	Net	Pin	Net
144	M_B_A0	8	M_B_DQ4
133	M_B_A1	7	M_B_DQ1
132	M_B_A2	20	M_B_DQ2
131	M_B_A3	21	M_B_DQ3
128	M_B_A4	4	M_B_DQ0
126	M_B_A5	3	M_B_DQ5
127	M_B_A6	16	M_B_DQ6
122	M_B_A7	17	M_B_DQ7
125	M_B_A8	28	M_B_DQ8
121	M_B_A9	29	M_B_DQ11
146	M_B_A10	41	M_B_DQ12
120	M_B_A11	42	M_B_DQ14
119	M_B_A12	24	M_B_DQ9
158	M_B_A13	25	M_B_DQ13
161	M_B_A14	38	M_B_DQ15
156	M_B_A15	37	M_B_DQ10
152	M_B_A16	50	M_B_DQ36
		49	M_B_DQ32
		62	M_B_DQ33
		63	M_B_DQ34
		46	M_B_DQ35
		45	M_B_DQ37
		58	M_B_DQ39
		59	M_B_DQ38
		70	M_B_DQ41
		71	M_B_DQ44
		83	M_B_DQ42
		84	M_B_DQ46
		66	M_B_DQ40
		67	M_B_DQ45
		79	M_B_DQ43
		80	M_B_DQ47
		174	M_B_DQ22
		173	M_B_DQ23
		187	M_B_DQ21
		186	M_B_DQ18
		170	M_B_DQ16
		169	M_B_DQ17
		183	M_B_DQ20
		182	M_B_DQ19
		195	M_B_DQ24
		194	M_B_DQ28
		207	M_B_DQ30
		208	M_B_DQ26
		191	M_B_DQ25
		190	M_B_DQ29
		203	M_B_DQ31
		204	M_B_DQ27
		216	M_B_DQ52
		215	M_B_DQ48
		228	M_B_DQ51
		229	M_B_DQ54
		211	M_B_DQ49
		212	M_B_DQ53
		224	M_B_DQ55
		225	M_B_DQ50
		237	M_B_DQ58
		236	M_B_DQ56
		249	M_B_DQ62
		250	M_B_DQ59
		232	M_B_DQ57
		233	M_B_DQ61
		245	M_B_DQ63
		246	M_B_DQ60

Byte 0 | Byte 1 | Byte 4 | Byte 5 | Byte 3 | Byte 2 | Byte 6 | Byte 7

Pin	Net
150	M_B_BA0
145	M_B_BA1
115	M_B_BG0
113	M_B_BG1
92	CB0/NC
91	CB1/NC
101	CB2/NC
102	CB3/NC
88	CB4/NC
87	CB5/NC
103	CB6/NC
104	CB7/NC
137	M_B_DDRCLK0
139	-M_B_DDRCLK0
138	M_B_DDRCLK1
140	-M_B_DDRCLK1
109	M_B_CKE0
110	M_B_CKE1
149	-M_B_CS0
157	-M_B_CS1
162	C0/CS2#/NC
163	C1/CS3#/NC
155	M_B_ODT0
161	M_B_ODT1
256	SA0
260	SA1
164	SA2
254	SDA
253	SCL
106	-DRAMRST
114	-M_B_ACT
116	-M_B_ALERT
134	M_B_EVENT#
143	M_B_PARITY
164	M_B_VREF_CA

DM2:SA0=1 SPD Addr: SA0_DIMM2
DM2:SA1=0 SPD Addr: SA1_DIMM2
DM2:SA2=0 SPD Addr: SA2_DIMM2

12,18,65 MEM_CP_SMB_SDA
12,18,65 MEM_CP_SMB_SCL
5,12 -DRAMRST
5 -M_B_ACT
5 -M_B_ALERT

1D2V_S3 — R1301 240R2F-1-GP — -DRAMRST

DM2D — 4 OF 4

DDR4-260P-45-GP-U
062.10011.00X1

Pin	Net	Pin	Net
1	VSS	99	VSS
2	VSS	102	VSS
5	VSS	103	VSS
6	VSS	106	VSS
9	VSS	107	VSS
10	VSS	167	VSS
14	VSS	168	VSS
15	VSS	171	VSS
18	VSS	172	VSS
19	VSS	175	VSS
22	VSS	176	VSS
23	VSS	180	VSS
26	VSS	181	VSS
27	VSS	184	VSS
30	VSS	185	VSS
31	VSS	188	VSS
35	VSS	189	VSS
36	VSS	192	VSS
39	VSS	193	VSS
40	VSS	196	VSS
43	VSS	197	VSS
44	VSS	201	VSS
47	VSS	202	VSS
48	VSS	205	VSS
51	VSS	206	VSS
52	VSS	209	VSS
56	VSS	210	VSS
57	VSS	213	VSS
60	VSS	214	VSS
61	VSS	217	VSS
64	VSS	218	VSS
65	VSS	222	VSS
68	VSS	223	VSS
69	VSS	226	VSS
72	VSS	227	VSS
73	VSS	230	VSS
77	VSS	231	VSS
78	VSS	234	VSS
81	VSS	235	VSS
82	VSS	238	VSS
85	VSS	239	VSS
86	VSS	243	VSS
89	VSS	244	VSS
90	VSS	247	VSS
93	VSS	248	VSS
94	VSS	251	VSS
98	VSS	252	VSS

-M_B_DQS[7:0] 5,13
M_B_DQS[7:0] 5,13

DM2B — 2 OF 4

DDR4-260P-45-GP-U
062.10011.00X1

Pin	Net
11	-M_B_DQS0
13	M_B_DQS0
32	-M_B_DQS1
34	M_B_DQS1
53	-M_B_DQS4
54	M_B_DQS4
74	-M_B_DQS5
76	M_B_DQS5
177	-M_B_DQS2
179	M_B_DQS2
198	-M_B_DQS3
200	M_B_DQS3
219	-M_B_DQS6
221	M_B_DQS6
240	-M_B_DQS7
242	M_B_DQS7
95	
97	
12	
33	
54	
75	
178	
199	
220	
241	
96	M_B_DM8#

1D2V_S3 — R1314 — DY — 0R2J-2-GP

DM2C — 3 OF 4

DDR4-260P-45-GP-U
062.10011.00X1

Pin	Net
111	VDD
112	VDD
117	VDD
118	VDD
123	VDD
124	VDD
129	VDD
130	VDD
135	VDD
136	VDD
141	VDD
142	VDD
147	VDD
148	VDD
153	VDD
154	VDD
159	VDD
160	VDD
163	VDD
255	VDDSPD_DIMM2
257	VPP_DIMM2
259	VPP
258	VTT
261	
262	
NP1	NP1
NP2	NP2

1D2V_S3 — R1312 0R0402-PAD-1-GP — 3D3V_S0
R1313 0R0402-PAD-1-GP — 2D6V_S5
0D6V_VREF_S0

PWR_SEQ = 19 or 29

LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-CHB SODIMM)
Size: A2 | Document Number: Kylo-2 | Rev: 1M
Date: Wednesday, October 17, 2018 | Sheet 13 of 99

BLANK

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LKL-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***DDR (RSVD)***

Size	Document Number	Rev
A4	**Kylo-2**	**1M**

Date: Wednesday, October 17, 2018 Sheet 14 of 99

Main Func = PCH

HW Strap

GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (See SPI Flash Programming Guide). ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.

GPP_B14

R1501 DY 20KR2J-L2-GP SPKR

GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_B18

GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_C2

GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). **Bit 6** / **Boot BIOS Destination** 0 / SPI (Default) 1 / LPC ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.

GPP_B22

GPP_B22_GSPI1_MOSI DY R1553 20KR2J-L2-GP

GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **If this strap is configured to '0' (eSPI is disabled), the *eSPI Flash Sharing Mode* strap must be configured to '0' as well (SAFS is disabled)**

GPP_C5

LKL-2 uses LPC interface

SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_MOSI

GPP_D12 / ISH_SPI_MOSI / GSPI2_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_D12

RVP 20K PH; #566439 EDS 100K

GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.

GPP_B23

SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO2

SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO3

HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_R2 / HDA_SDO / I2S0_TXD / HDACPU_SDO

GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

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GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

on page 4

GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

RO13_CFLU_20180130 follow RO13 no GPP_E23 strap (remove R1528)

GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

RO13_CFLU_20180108 reserve for strap (intel review)

GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_H21

RO13_CFLU_20180105

GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.

GPP_F2 / CNV_RGI_DT / UART0_TXD

Close to WLAN1

INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% ***Note:*** This strap should only be used for specific targeted 1S battery systems.

GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**

[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)

CFG[3]: 0 — ENABLED: SET DFX ENABLED BIT IN DEBUG INTERFACE MSR; 1 — DISABLED

PDG datasheet, #575418

(#543016)

DISPLAY PORT PRESENCE STRAP

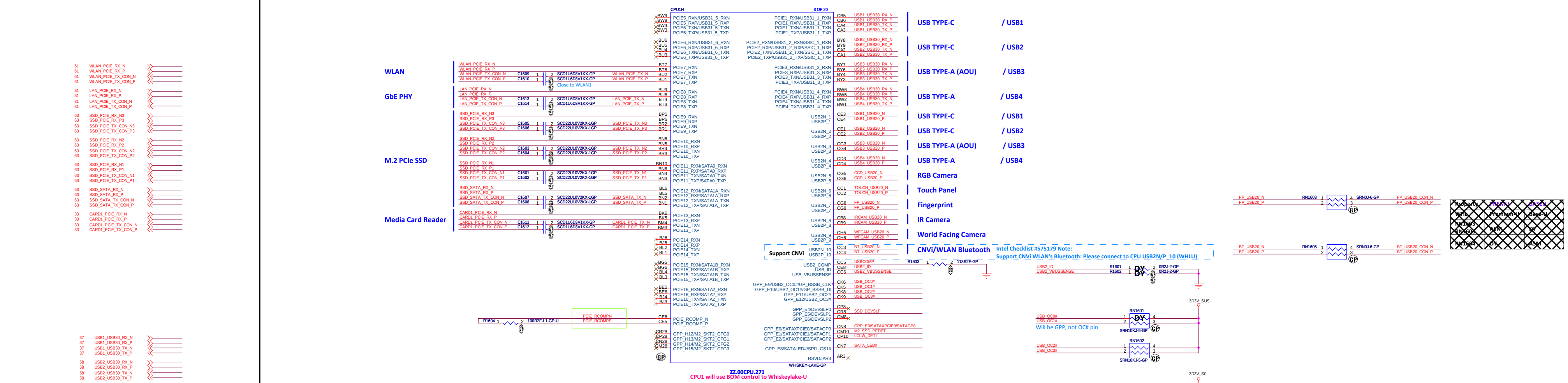
CFG[4]: 0 — ENABLED: An external Display Port device is connected to the Embedded Display Port. 1 — DISABLED (Default): No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

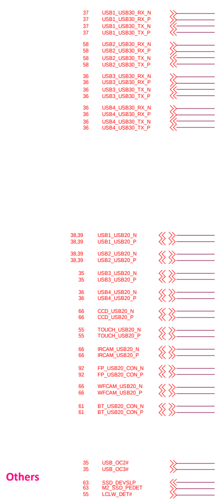
PCH strap pin:

LKL-2

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **CPU(STRAP)**		
Size: A0	Document Number: **Kylo-2**	Rev: **1M**
Date: Wednesday, October 17, 2018	Sheet 15 of 99	

KL2_SIT_MB_W006
KL2_SVT_MB_W005





Layout Note:

1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

PCIe Configuration

Pair	Device
1	NC
2	NC
3	NC
4	NC
5	NC
6	NC
7	WLAN
8	GbE
9	M.2 PCIe SSD
10	M.2 PCIe SSD
11	M.2 PCIe SSD
12	M.2 PCIe SSD
13	Media Card Reader
14	NC
15	NC
16	NC

USB3.0 Configuration

Pair	Device
1	USB3 Type-C Port1
2	USB3 Type-C Port2
3	USB3 Type-A Port3
4	USB3 Type-A Port4
5	NC
6	NC

Premium-WHL-U

USB2.0 Configuration

Pair	Device
1	USB3 Type-C Port1
2	USB3 Type-C Port2
3	USB3 Type-A Port3
4	USB3 Type-A Port4
5	RGB
6	Touch Screen
7	Fingerprint
8	IR Camera
9	World Facing Camera
10	Bluetooth (CNVi)

Base-WHL-U

USB2.0 Configuration

Pair	Device
1	USB3 Type-C Port1
2	USB3 Type-C Port2
3	USB3 Type-A Port3
4	USB3 Type-A Port4
5	RGB
6	Touch Screen
7	Bluetooth (WLAN)
8	IR Camera

LKL-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (PCIE/SATA/USB)**

Size: A1 | Document Number: Kylo-2 | Rev: 1M

Main Func = PCH

KL2_SVT_MB_W009

KL2_SIT_MB_W011
KL2_SIT_MB_W012
KL2_SIT_MB_W036
KL2_SIT_MB_W040
KL2_SVT_MB_W009

Follow Checklist #575412, v0.9, p.34: 1K PU and 10K-ohm is used on the CRB

#575412, v0.9, p.30: 1M-ohm PU and 330K-ohm is used on the CRB

CPU1 will use BOM control to Whiskeylake-U

Reserve Kylo-1 Solution

R1722 & EC1708 modify to 100k and 0.01uF at DVT1

#543816 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

BATLOW#: Pull-up required even if not implemented.

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PCH (PMU)

Kylo-2

1M

Main Func = PCH

KL2_SIT_MB_W001
KL2_SIT_MB_W030
KL2_SIT_MB_W037
KL2_SIT_MB_W040
KL2_SVT_MB_W009

PCH strap pin: SPI_SO_CPU

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

PCH strap pin: CPU_SMB_ALERT#_P0

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

This signal has a weak internal pull-down.

RCIN#: Frequency to Avoid: 33 MHz

SERIRQ Prt:
PDG: 8.2k
CRB: 10k

ZZ.00CPU.271
CPU1 will use BOM control to Whiskeylake-U

Follow Checklist #575412, v0.9, p.23

R1843: LPC Debug Port for Security (Page 68)

Close CPU1

WLAN
SSD
GbE PHY
Media Card Reader

24MHz (X1801)
TXC 7V24000023 082.30006.0571
HARMONY X3G024000BC1HA-HU 082.30006.0531

32.768KHz (X1802)
EPSON EP.FC-135R 32.768K12.5+-20 (X1A000141000300) 082.30003.0191
SEIKO Q-SC32P0320CSAAAF 082.30003.0301
TXC 9H03200042 082.30003.0231

LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(SPI/ESPI/SMBUS/XTAL/CLK)
Size: A3 | Document Number: Kylo-2 | Rev: 1M
Date: Wednesday, October 17, 2018 | Sheet 18 of 99

Main Func = PCH

27 HDA_SDIN0_CPU
27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
27 HDA_SDOUT_CODEC
15 HDA_SDOUT_CPU
25 RTC_TEST

24 ME_FWP_EC

61 BT_PCMOUT_CLKREQ0
61 BT_PCMFRM_RSTN

15,27 SPKR

61 BLUETOOTH_EN
55 TOUCH_RESET#
66 YOGA_DET#
61 CNV_EN#

PCH strap pin: HDA_SDOUT_CPU

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin: SPKR

TOP SWAP OVERRIDE	
HDA_SPKR	* High = TOP SWAP ENABLED Low = DISABLED (WEAK INTERNAL PD)

The internal pull-up

CPU1G — 7 OF 20 — WHISKEY-LAKE-GP

HDA_SYNC_CPU BN34 HDA_SYNC/I2S0_SFRM
HDA_BITCLK_CPU BN37 HDA_BCLK/I2S0_SCLK
HDA_SDOUT_CPU BN36 HDA_SDO/I2S0_TXD /strap
HDA_SDIN0_CPU BN35 HDA_SDI0/I2S0_RXD
BL36 HDA_SDI1/I2S1_RXD/SNDW1_DATA
BL35 HDA_RST#/I2S1_SCLK/SNDW1_CLK
CK23 GPP_D23/I2S_MCLK
BL37 I2S1_SFRM/SNDW2_CLK
BL34 I2S1_TXD/SNDW2_DATA

GPP_G0/SD_CMD CH36 BLUETOOTH_EN
GPP_G1/SD_DATA0 CL35
GPP_G2/SD_DATA1 CL36 RTC_TEST
GPP_G3/SD_DATA2 CM35
GPP_G4/SD_DATA3 CN35 YOGA_DET#
GPP_G5/SD_CD# CH35
GPP_G6/SD_CLK CK36
GPP_G7/SD_WP CK34 CNV_EN#

TPAD14-OP-GP TP1903 1 HDA_RST_N_CPU

BT_PCMFRM_RSTN R1913 1 2 33R2J-2-GP GPP_H1_SFRM C32 GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#
BT_PCMOUT_CLKREQ0 R1912 1 2 33R2J-2-GP GPP_H2_CLKREQ0 CH32 GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK
CH29 GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ
CH30 GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO

3D3V_S0 R1902 1 2 10KR2J-3-GP TOUCH_RESET#

TOUCH_RESET# CP24 GPP_A17/SD_VDD1_PWR_En#/ISH_GP7
CN24 GPP_D19/DMIC_CLK0/SNDW4_CLK
GPP_D20/DMIC_DATA0/SNDW4_DATA
CK25 GPP_D17/DMIC_CLK1/SNDW3_CLK
CJ25 GPP_D18/DMIC_DATA1/SNDW3_DATA

GPP_A18/SD_1P8_SEL BW36
BY31
SD_1P8_RCOMP
SD_3P3_RCOMP
CK33 SD_RCOMP R1901 1 2 200R2F-L-GP
CM34

SPKR CF35 GPP_B14/SPKR /strap

ZZ.00CPU.271
CPU1 will use BOM control to Whiskeylake-U

3D3V_S5 YOGA_DET# R1903 1 2 100KR2J-1-GP

HDA_SYNC_CODEC R1908 1 2 33R2J-2-GP HDA_SYNC_CPU

HDA_BITCLK_CODEC R1920 1 2 33R2J-2-GP HDA_BITCLK_CPU
HDA_SDOUT_CODEC R1921 1 2 33R2J-2-GP HDA_SDOUT_CPU

ME_FWP_EC R1909 1 2 1KR2J-1-GP

LKL-2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(HDA/I2S/SD/DMIC)
Size: A2 | Document Number: Kylo-2 | Rev: 1M
Date: Wednesday, October 17, 2018 | Sheet 19 of 99

Main Func = PCH

KL2_SIT_MB_W016

CNVi
- 61 CNV_BRI_DT_R
- 61 CNV_RGI_RSP
- 15,61 CNV_RGI_DT_R
- 61 CNV_BRI_RSP
- 61 CNV_UART_WAKE

NFC
- 90 CPU_I2C_SDA_P0
- 90 CPU_I2C_SCL_P0

TOUCH PANEL
- 55 CPU_I2C_SDA_P1
- 55 CPU_I2C_SCL_P1

PD
- 38 PD_I2C_SDA_P2
- 38 PD_I2C_SCL_P2

SENSOR
- 66,68,70 CPU_I2C_SDA_ISH0
- 66,68,70 CPU_I2C_SCL_ISH0

EC
- 24,68 EC_I2C_SDA_ISH1
- 24,68 EC_I2C_SCL_ISH1

- 90 NFC_DLREQ
- 91 PIRQA#
- 90 NFC_INT
- 15 NRB_BIT
- 26,88 FAN_ID
- 15 GPP_B22_GSPI1_MOSI
- 90 NFC_DTCT
- 90 NFC_ON
- 56 SW
- 17,61 PCIE_WAKE#_CPU_R
- 25 RTC_DET#
- 15 GPP_D12
- 68 -ISH_ALS_INT
- 68 -ISH_GSENSOR_INT
- 66,68,70 -ISH_ANGLE_INT
- 24,67 LID_CLOSE#
- 24,67 SENSOR_LID_OPEN#
- 68 SENSOR_BRD_ID
- 68 LID_CLOSE#_D
- 68 SENSOR_LID_OPEN#_D
- 55 TOUCH_PANEL_INTR#
- 55 TOUCH_EN

PDG #575412 p128

3D3V_SUS
- R2053 10KR2J-3-GP PIRQA#
- R2012 10KR2J-3-GP CNV_UART_WAKE

3D3V_S0
- R2003 10KR2J-3-GP FAN_ID

1D8V_SUS
- RN2001 SRN20KJ-1-GP CNV_RGI_RSP / CNV_BRI_RSP

CNV_RGI_DT_R / CNV_BRI_DT_R — RN2002 SRN33J-5-GP-U

3D3V_S5
- R2014 4K7R2J-2-GP PCIE_WAKE#_GPP_H9

PCIE_WAKE#_CPU_R — R2013 0R2J-2-GP — PCIE_WAKE#_GPP_H9

KBLR:GPP_F4~F9: 1.8V only
WHL:GPP_H4~H9: ?V

CPU1F — 6 OF 20

NFC_DLREQ	CC27	GPP_B15/GSPI0_CS0#
PIRQA#	CC32	GPP_A7/PIRQA#/GSPI0_CS1#
NFC_INT	CE28	GPP_B16/GSPI0_CLK
TOUCH_EN	CE27	GPP_B17/GSPI0_MISO
NRB_BIT	CE29	GPP_B18/GSPI0_MOSI /strap
CNV_UART_WAKE	CA31	GPP_B19/GSPI1_CS0#
	CA32	GPP_A11/PME#/GSPI1_CS1#/SD_VDD2_PWR_EN#
FAN_ID	CC29	GPP_B20/GSPI1_CLK
GPP_B22_GSPI1_MOSI	CA30	GPP_B21/GSPI1_MISO
		GPP_B22/GSPI1_MOSI /strap
CNV_BRI_RSP	CK20	GPP_F5/CNV_BRI_RSP
CNV_RGI_DT	CG19	GPP_F6/CNV_RGI_DT
CNV_BRI_DT	CJ20	GPP_F4/CNV_BRI_DT
CNV_RGI_RSP	CH19	GPP_F7/CNV_RGI_RSP
NFC_DTCT	CR12	GPP_C20/UART2_RXD
NFC_ON	CP12	GPP_C21/UART2_TXD
TOUCH_PANEL_INTR#	CN12	GPP_C22/UART2_RTS#
SW	CM12	GPP_C23/UART2_CTS#
CPU_I2C_SDA_P0	CM11	GPP_C16/I2C0_SDA
CPU_I2C_SCL_P0	CN11	GPP_C17/I2C0_SCL
CPU_I2C_SDA_P1	CK12	GPP_C18/I2C1_SDA
CPU_I2C_SCL_P1	CJ12	GPP_C19/I2C1_SCL
PD_I2C_SDA_P2	CF27	GPP_H4/I2C2_SDA
PD_I2C_SCL_P2	CF28	GPP_H5/I2C2_SCL
	CH27	GPP_H6/I2C3_SDA
	CH28	GPP_H7/I2C3_SCL
	CJ30	GPP_H8/I2C4_SDA
	CJ31	GPP_H9/I2C4_SCL

NFC
TOUCH PANEL
PD

	CC22	GPP_D9/ISH_SPI_CS#/GSPI2_CS0#
	CR22	GPP_D10/ISH_SPI_CLK/GSPI2_CLK
RTC_DET#	CM22	GPP_D11/ISH_SPI_MISO/GSPI2_MISO
GPP_D12	CP22	GPP_D12/ISH_SPI_MOSI/GSPI2_MOSI
CPU_I2C_SDA_ISH0	CK22	GPP_D5/ISH_I2C0_SDA
CPU_I2C_SCL_ISH0	CH20	GPP_D6/ISH_I2C0_SCL
CPU_I2C_SDA_ISH1	CH22	GPP_D7/ISH_I2C1_SDA
CPU_I2C_SCL_ISH1	CJ22	GPP_D8/ISH_I2C1_SCL
	CJ23	GPP_H10/I2C5_SDA/ISH_I2C2_SDA
	CJ25	GPP_H11/I2C5_SCL/ISH_I2C2_SCL
	CM24	GPP_D13/ISH_UART0_RXD
	CN24	GPP_D14/ISH_UART0_TXD
	CM25	GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#
	CR24	GPP_D16/ISH_UART0_CTS#/SML0BALERT#
	CG12	GPP_C12/UART1_RXD/ISH_UART1_RXD
	CH12	GPP_C13/UART1_TXD/ISH_UART1_TXD
	CF12	GPP_C14/UART1_RTS#/ISH_UART1_RTS#
	CG13	GPP_C15/UART1_CTS#/ISH_UART1_CTS#
-ISH_ALS_INT	BW35	GPP_A18/ISH_GP0
-ISH_GSENSOR_INT	BW34	GPP_A19/ISH_GP1
-ISH_ANGLE_INT	CA37	GPP_A20/ISH_GP2
LID_CLOSE#_D	CA36	GPP_A21/ISH_GP3
SENSOR_LID_OPEN#_D	CA35	GPP_A22/ISH_GP4
SENSOR_BRD_ID	CA34	GPP_A23/ISH_GP5
ISH_GP6	BW37	GPP_A12/ISH_GP6/BM_BUSY#/SX_EXIT_HOLDOFF#

SENSOR
EC

KBLR:GPP_F10~F11: 1.8V only
WHLU:GPP_H10~H11: ?V

WHISKEY-LAKE-GP

ZZ.00CPU.271
CPU1 will use BOM control to Whiskeylake-U

D2001 D2002 RB530SM-30T2R-GP-U
LID_CLOSE#
SENSOR_LID_OPEN#

3D3V_S0
- RN2007 SRN1KJ-7-GP — CPU_I2C_SDA_ISH0 / CPU_I2C_SCL_ISH0
- RN2008 SRN1KJ-7-GP — CPU_I2C_SDA_ISH1 / CPU_I2C_SCL_ISH1

(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

3D3V_S0
- RN2010 SRN10KJ-5-GP — -ISH_ALS_INT / -ISH_GSENSOR_INT
- RN2011 SRN10KJ-5-GP — -ISH_ANGLE_INT
- RN2012 SRN10KJ-5-GP — LID_CLOSE#_D / SENSOR_LID_OPEN#_D
- R2004 R2005 10KR2J-3-GP — SENSOR_BRD_ID / ISH_GP6
- R2006 R2007 10KR2J-3-GP — SENSOR_BRD_ID / ISH_GP6

3D3V_S0 — Q2001 SSM6N7002KFU-GP
- CPU_I2C_SDA_ISH1 ↔ EC_I2C_SDA_ISH1
- EC_I2C_SCL_ISH1 ↔ CPU_I2C_SCL_ISH1

PCH strap pin: NRB_BIT

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

LKL-2

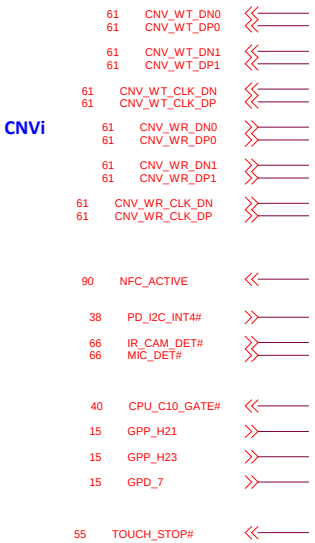
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

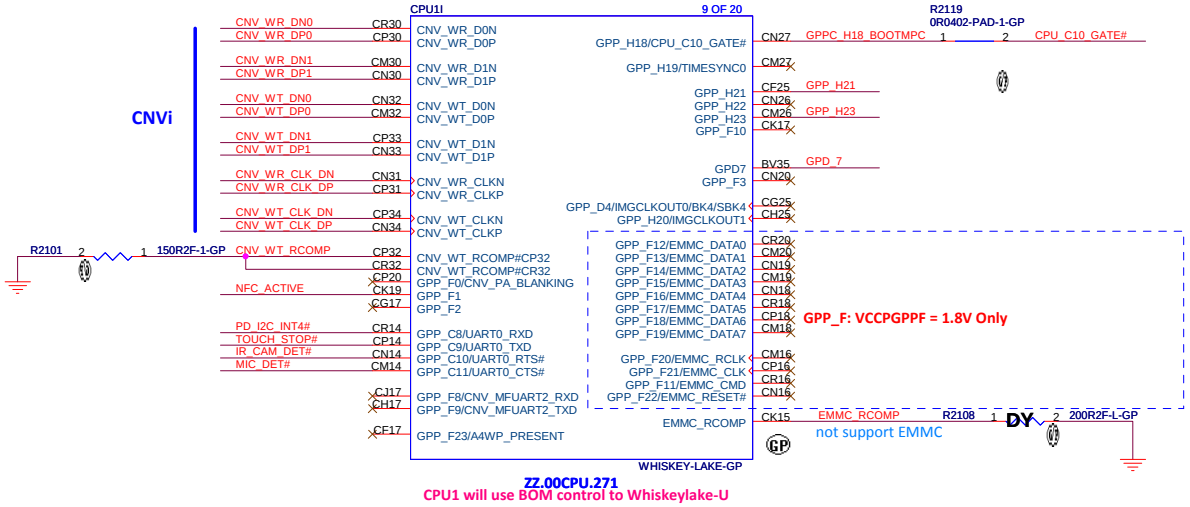
Title: CPU_(UART/I2C/ISH)

Size: A2 | Document Number: Kylo-2 | Rev: 1M

Date: Wednesday, October 17, 2018 | Sheet 20 of 99

Main Func = PCH





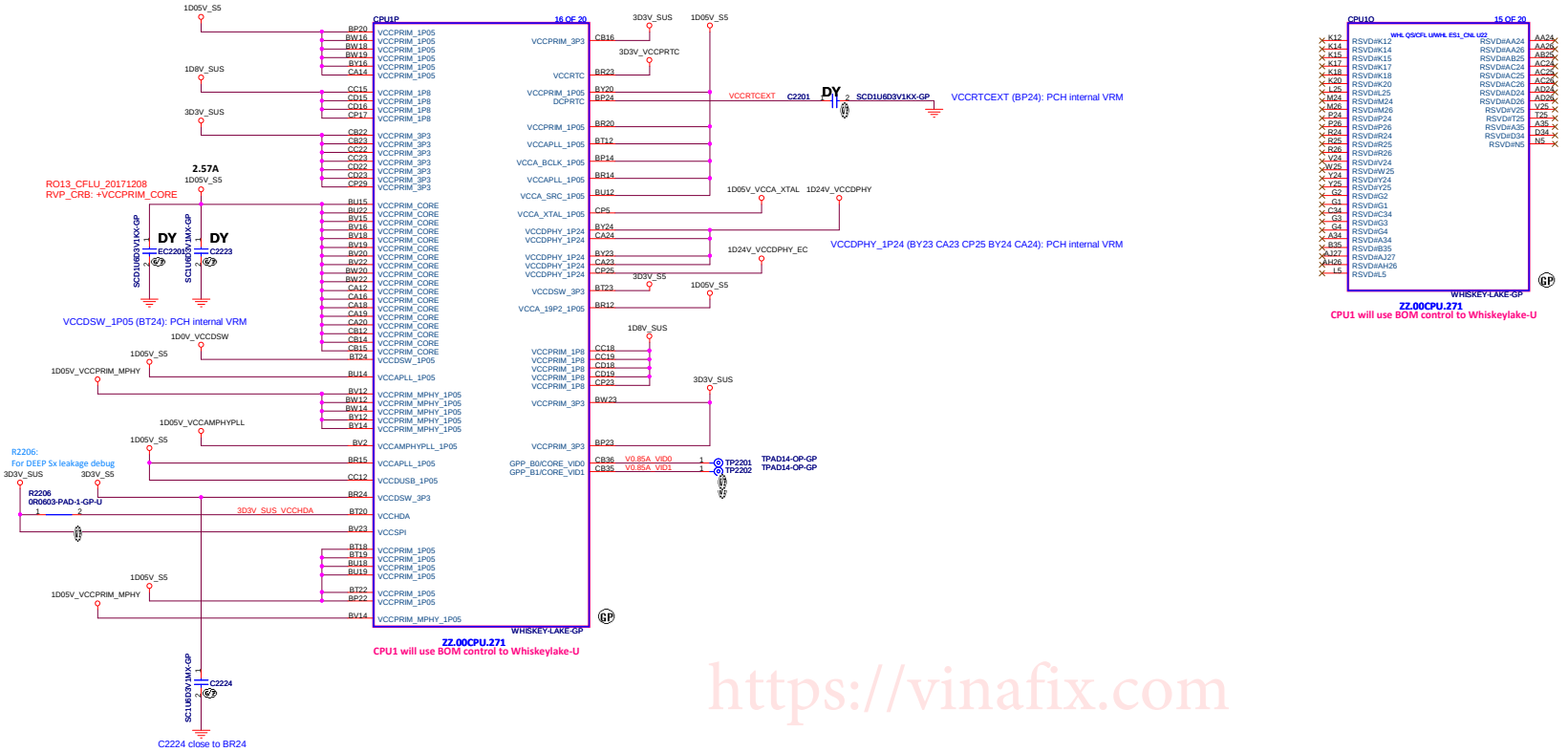
KL2_SVT_MB_W009

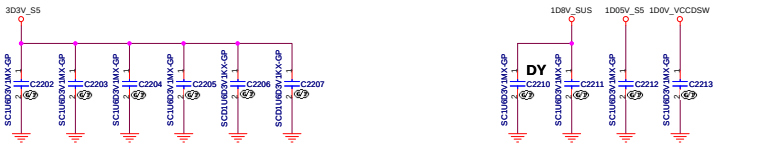
LKL-2

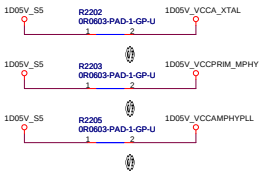
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU_(CSI/EMMC/CNVI)		
Size: A3	Document Number: Kylo-2	Rev: 1M
Date: Wednesday, October 17, 2018	Sheet 21 of 99	

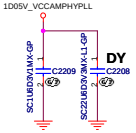
Main Func = PCH

KL2_SIT_MB_W006
KL2_SIT_MB_W028
KL2_SIT_MB_W033
KL2_SIT_MB_W040
KL2_SVT_MB_W009

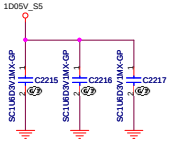


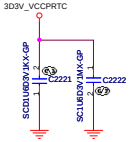






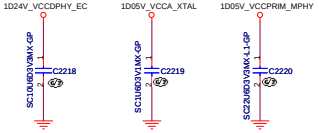
Layout Note:
C2208 near BV2
C2209 near BV2





Layout Note:
C2221 near BR23
C2222 near BR23

Layout Note:
C2218 near CP25



LKL-2

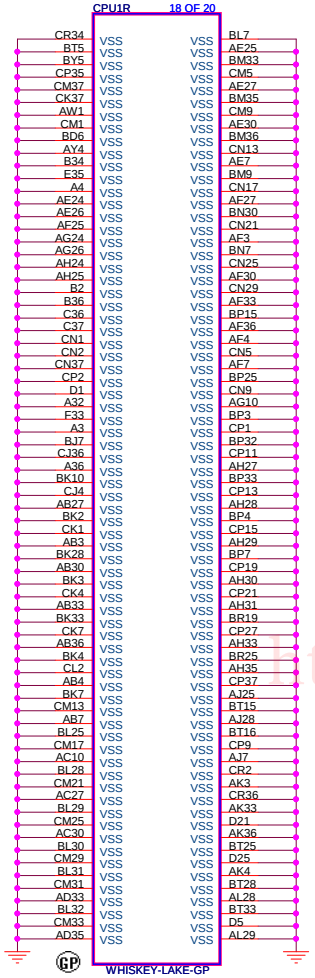
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(PCH-LP PWR&CAPS)

Size: A2 | Document Number: Kylo-2 | Rev: 1M

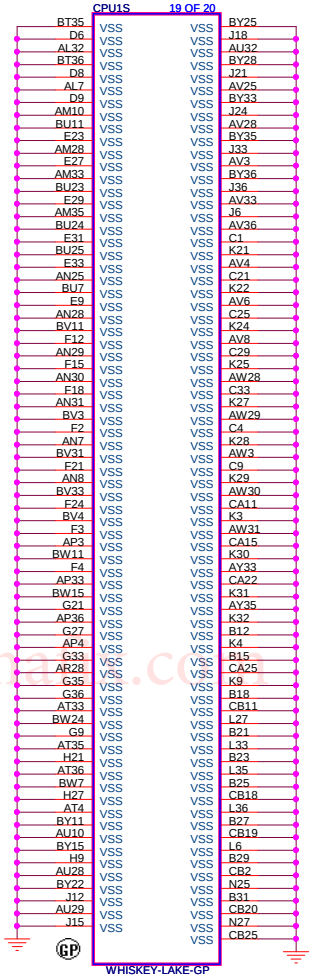
Date: Wednesday, October 17, 2018 | Sheet 22 of 99

Main Func = PCH



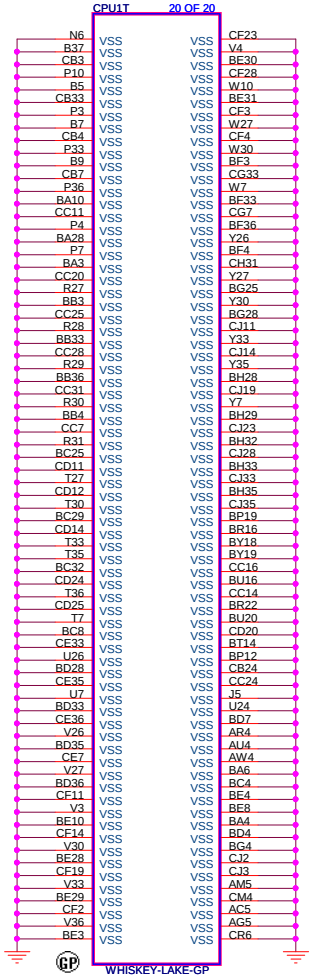
ZZ.00CPU.271

CPU1 will use BOM control to Whiskeylake-U



ZZ.00CPU.271

CPU1 will use BOM control to Whiskeylake-U



ZZ.00CPU.271

CPU1 will use BOM control to Whiskeylake-U

LKL-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_(VSS)***

Size	Document Number	Rev
A3	**Kylo-2**	1M

Date: Wednesday, October 17, 2018 Sheet 23 of 99

Main Func = KBC

KL2_SIT_MB_W006
KL2_SIT_MB_W014
KL2_SIT_MB_W017
KL2_SIT_MB_W019
KL2_SIT_MB_W025
KL2_SIT_MB_W033
KL2_SVT_MB_W001
KL2_SVT_MB_W002
KL2_SVT_MB_W009
KL2_SOVP_MB_W001

SKU_ID (PIN 96)		Pull Down (R2449)	Pull High (R2448)	Voltage
LKL-2	vPro	100.0K	64.9K	2.001V
	non-vPro		76.8K	1.867V
	vPro	100.0K	100.0K	1.650V
	non-vPro		143.0K	1.358V

LOGIC

PCB_ID (PIN 98)	Pull Down (R2419)	Pull High (R2418)	Voltage
17821-SD	100.0K	10.0K	3V
18724-SB	100.0K	20.0K	2.75V
18724-1	100.0K	33.0K	2.481V
18724-1M	100.0K	47.0K	2.245V
	100.0K	64.9K	2.001V
	100.0K	76.8K	1.867V
	100.0K	100.0K	1.650V
	100.0K	143.0K	1.358V
	100.0K	191.0K	1.134V
	100.0K	267.0K	0.89V

LOGIC

NOTE:
EXT_RST# has 110K internal pull-up, however an additional external pull-up may be required to meet 60u sec timing requiremen...

NOTE:
Please be aware that the SPI interface trace length between PCH and EC should not exceed 6500mils,. The mismatch of SPI interface signals between EC and SPI flash should not exceed 500mils.

NOTE:
Locate resistors R2415 and R2417 close to the KBC1.

NOTE:
place all the ADC input capacitors close to the ADC pins.

NOTE:
E51_RxD for debug card detestion
When using debug card,ASM R2453 and flash KBC code

NOTE:
Please place R2410 close to AGND pin.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

NOTE:
C2412 must place close to VCORF pin.

NOTE:
PWM Signal :
1. If unused, select altrnative GPIO function and enable internal pull-down.
2. Please measure and make sure that the rise time of VCC_BOB is less than 10us.

NOTE:
EXT_PURST# has a 110K internal PU to Vcc power plane. Thus R2403 can be eliminated.

Nuvoton KBC PSL Power Switched Logic

#1 Enter PSL Mode (Entry S5 after 10sec) :
3D3V_AUX_KBC : OFF (KBC PWR supply)

#2 At PSL Mode (SPEC: S5<10mW)

	EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
PSL Mode (AC or DC)	HIGH	LOW	OFF
PSL Wake (AC or DC):	LOW	HIGH	ON

GPIO42	LID_CLOSE#: NB Lid function
GPIO80	SENSOR_LID_OPEN#: Tablet detect function

EC_GPIO47 High Active

BATTERY / CHARGER ---->
PCH / Thermal / G-sensor (Thermal)---->
Intel Sensor Hub ---->
PD 65988 /MUX PS8742 **2 ---->
Click PAD---->

KBC1 NPCE288GA0DX-1-GP 071.00288.0A0G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ECIO (NUVOTON NPCE288)
Size: Custom | Document Number: Kylo-2 | Rev: 1M
Date: Wednesday, October 17, 2018 | Sheet 24 of 99

Main Func = SPI Flash

KL2_SIT_MB_W006
KL2_SIT_MB_W013
KL2_SIT_MB_W014
KL2_SIT_MB_W031
KL2_SIT_MB_W035
KL2_SIT_MB_W040
KL2_SVT_MB_W009

18,24 SPI_CS_CPU_N0
18,24,91 SPI_CLK_CPU
15,18,24,91 SPI_SI_CPU
18,24,91 SPI_SO_CPU
15,18 SPI_WP_CPU
15,18 SPI_HOLD_CPU

3D3V_SUS
3D3V_SPI
3D3V_SPI
R2510 0R0603-PAD-1-GP-U
R2519 4K7R2J-2-GP

SPI ROM (BIOS1)

BIOS1
SPI_CS_CPU_N0
SPI_SO_CPU R2506 0R0402-PAD-1-GP SPI_SO_ROM
SPI_WP_CPU R2507 33R2J-2-GP SPI_WP_ROM
S# GND
DQ1 VCC
W#/VPP HOLD#
VSS C
DQ0
SPI_HOLD_ROM R2503 33R2J-2-GP SPI_HOLD_CPU
SPI_CLK_ROM R2508 33R2J-2-GP SPI_CLK_CPU
SPI_SI_ROM R2509 0R0402-PAD-1-GP SPI_SI_CPU
LILY-BIOS-COLAY-GP-U
ZZ.00PAD.M41

208MIL SOIC8 (BIOS1):		16MB (128Mb)	non-vPro
WINBOND	W25Q128JVSIQ	072.25128.0B51	
MACRONIX	MX25L12873FM2I-10G	072.25128.0B11	
MICRON	MT25QL128ABA1ESE-0SIT	072.25128.000N	
MACRONIX	MX25L12872FM2I-10G	072.25128.0D61	
208MIL SOIC8 (BIOS1):		32MB (256Mb)	vPro
WINBOND	W25Q256JVEIQ	072.25256.0N01	(WSON8)
MACRONIX	MX25L25673GM2I-08G	072.25673.0001	(SOP8)

SPI ROM Socket (SSKT1)

3D3V_SPI
SSKT1
SPI_CS_CPU_N0
SPI_SO_ROM
SPI_WP_ROM
SPI_HOLD_ROM
SPI_CLK_ROM
SPI_SI_ROM
SKT-50960-0084L-001-GP
62.10076.051
Co-Layout Design on BIOS1
SPI socket mount in SA stage

3D3V_SPI
SCD1U6D3V1KX-GP
C2502

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Main Func = RTC

18,99 RTC_RST#
18 SRTC_RST#
20 RTC_DET#
19 RTC_TEST

3D3V_AUX_S5
R2514 0R0402-PAD-1-GP
3D3V_AUX_R
D2502 RB530SM-30T2R-GP-U

RTC CONN

RTCVCC_CONN
RTCVCC_D
RTC_AUX_S5
RTC1
R2501 1KR2J-1-GP
D2501 RB530SM-30T2R-GP-U
ACES-CON2-20-GP-U
20.F1639.002
DY
C2504 SC1U6D3V1MX-GP
RN2501
SRN20KJ-1-GP
RTC_RST#
SRTC_RST#
C2501 SC1U6D3V1MX-GP
C2503 SC1U6D3V1MX-GP

RTCVCC_D
Q2502 T2N7002BK-2-GP
Detect Low
RTC_DET#
R2513 100KR2J-1-GP
3D3V_S0
5V_S0
R2512 100KR2J-1-GP
Test High
RTC_TEST
RTC_DET#_G
R2511 10KR2J-L-GP
Q2501 T2N7002BK-2-GP

https://vinafix.com

LKL-2

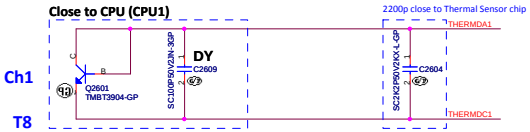
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FLASH/RTC
Size: A3
Document Number: Kylo-2
Rev: 1M
Date: Wednesday, October 17, 2018
Sheet 25 of 99

Main Func = Thermal Sensor

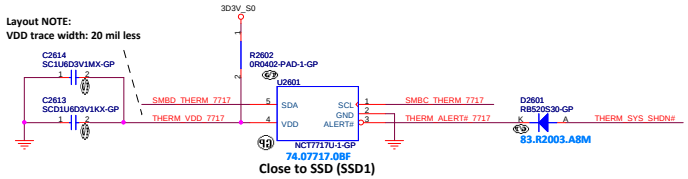
Thermal Sensor

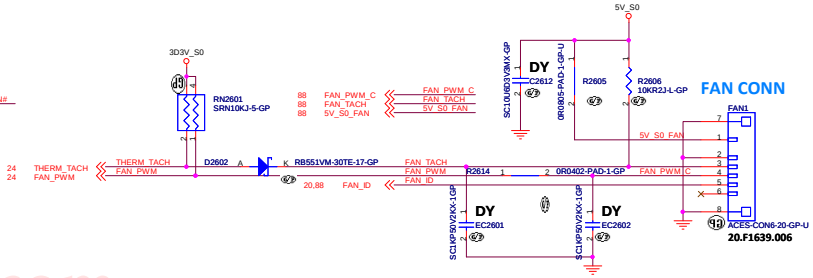
KL2_SIT_MB_W006
KL2_SIT_MB_W033
KL2_SVT_MB_W009

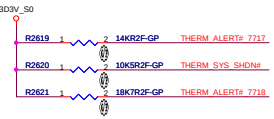


CPU backside or inside the socket

CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.







ALERT# /T_CRIT# Pull-up Resistor v.s. Alert temperature (℃)

NCT7717U Table:

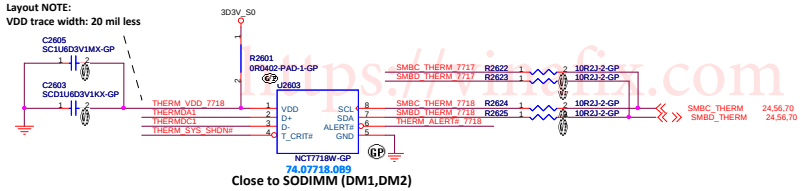
R2619	
2.0K	75
7.5K	90
10.5K	~~100~~
14.0K	105
~~18.7K~~	110

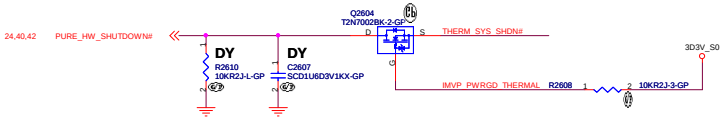
NCT7718W Table:

R2621 \ R2620	2.0K	7.5K	10.5K	14.0K	18.7K
2.0K	77	87	97	107	117
7.5K	79	89	99	109	119
10.5K	81	91	101	111	121
14.0K	83	93	103	113	123
~~18.7K~~	85	95	105	115	125

FAN Controller

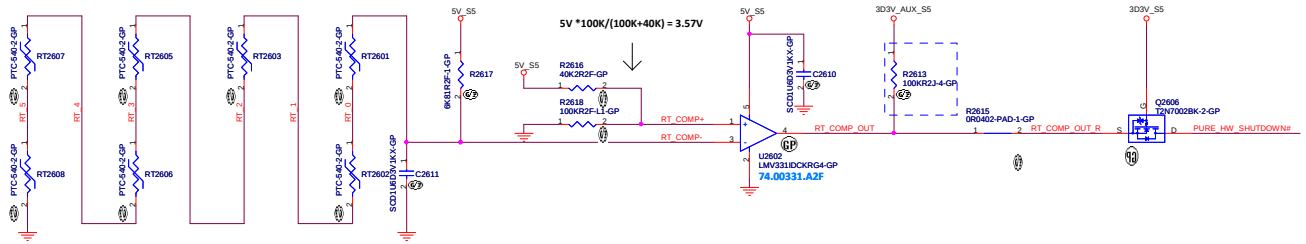
NCT7717U 's maximum power consumption can be xxx mA (TBD)
NCT7718W 's maximum power consumption can be xxx mA (TBD)





PURE_HW_SHUTDOWN# logic table

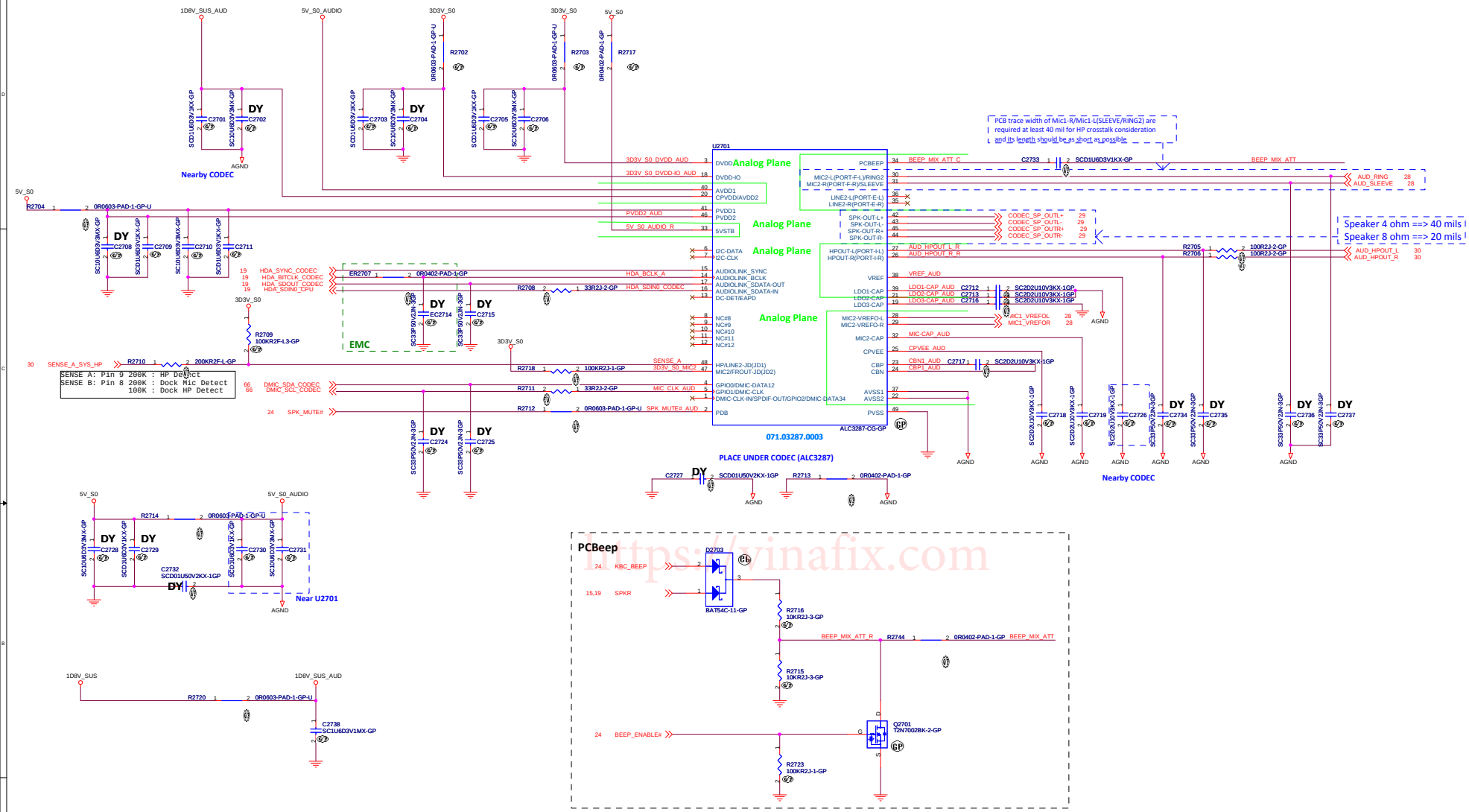
signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low



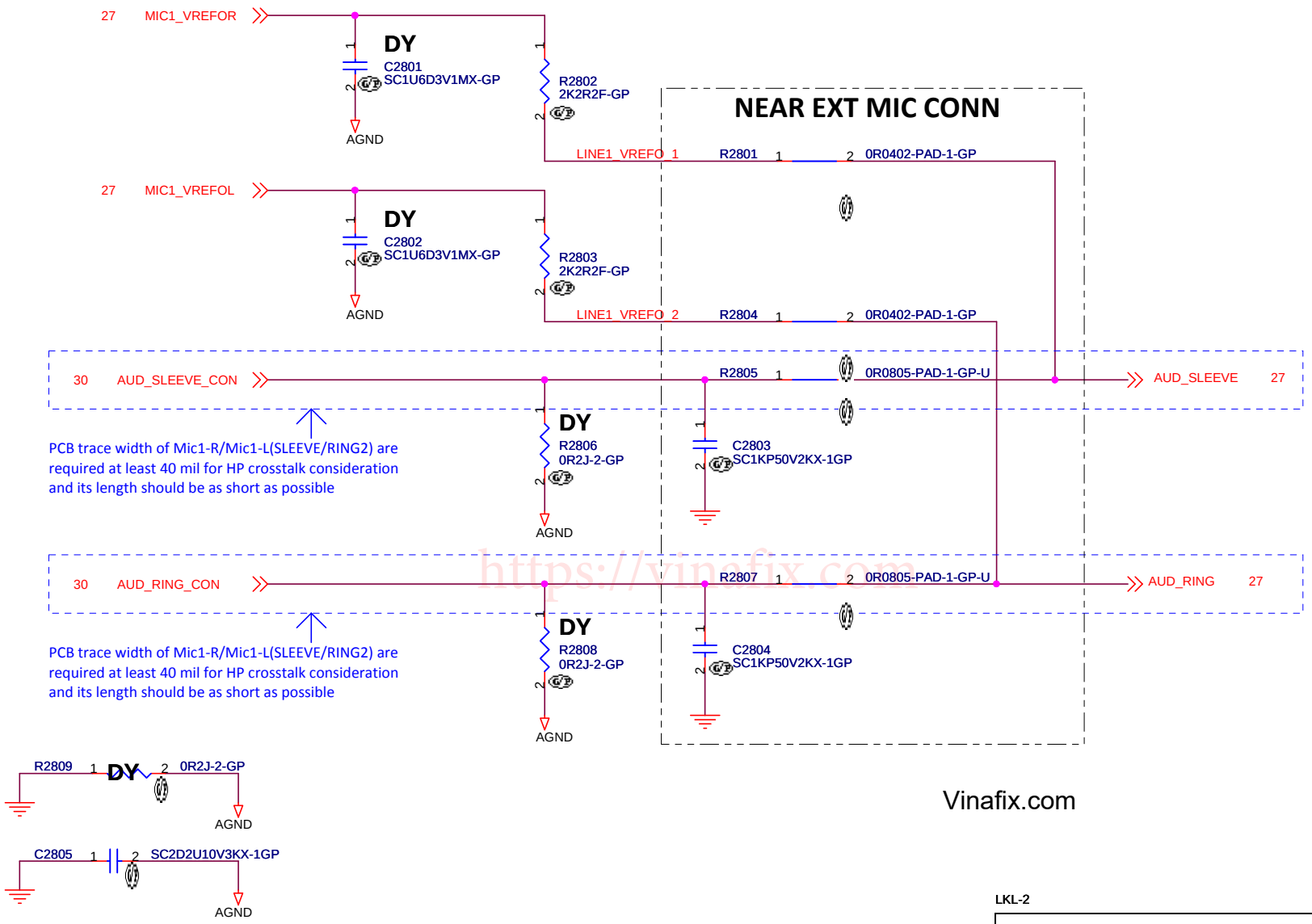
LKL-2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (THERMAL/FAN)
Size: A2
Document Number: Kylo-2
Rev: 1M
Date: Wednesday, October 17, 2018
Sheet 28 of 99



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	AUDIO (CODEC ALC3287)
Size	A2
Document Number	Kylo-2
Rev	1M
Date	Wednesday, October 17, 2018
Sheet	27 of 99



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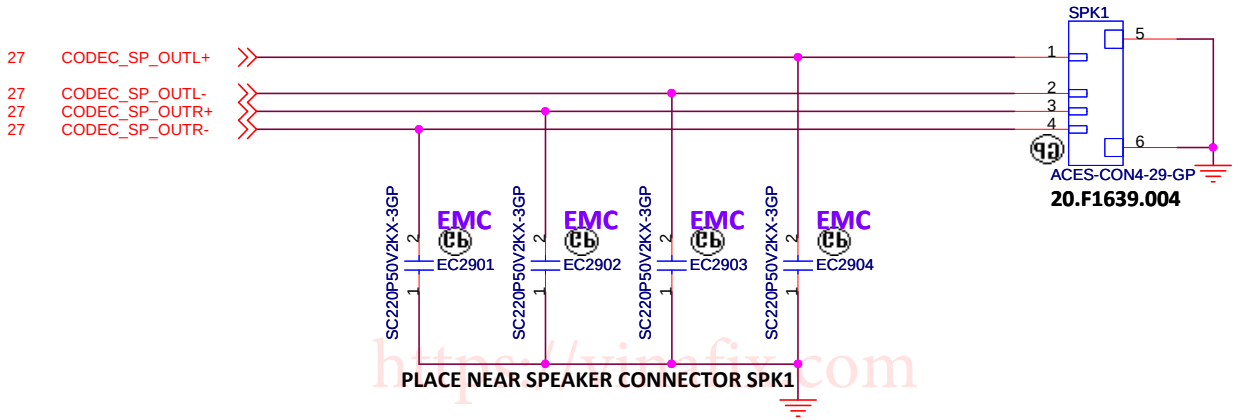
LKL-2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO (MIC I/F)		
Size: A4	Document Number: Kylo-2	Rev: 1M
Date: Wednesday, October 17, 2018	Sheet 28 of 99	

Main Func = AUDIO

Speaker Connector



LKL-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***AUDIO (SPEAKER)***	
Size A4	Document Number **Kylo-2**	Rev **1M**
Date: Wednesday, October 17, 2018	Sheet 29 of 99	

KL2_SIT_MB_W006
KL2_SIT_MB_W031
KL2_SVT_MB_W009
KL2_SVT_MB_W012

27 AUD_HPOUT_L — R3007 1 2 0R0402-PAD-1-GP
27 AUD_HPOUT_R — R3008 1 0R0402-PAD-1-GP
DY C3002 SC100P50V2JN-L-GP
DY C3003 SC100P50V2JN-L-GP
Moat

NEAR AUDIO JACK CONN

3D3V_S0
R3001 10KR2J-3-GP

Combo Jack
AUD1
AUD_RING_CON
AUD_HPOUT_L_CON
AUD_HPJD_N
HP_JACK_SYS
AUD_HPOUT_R_CON
AUD_SLEEVE_CON
Audio(IP/NK comb)
AUDIO-JK628-GP
022.10002.01U1

AUDIO JACK SENSE
CLOSE TO CODEC
6-10 mil trace recommend

HGNDA/HGNDB trace width >70mil,
changed to sharp will be better.

AUD_RING_CON
AUD_HPOUT_L_CON
HP_JACK_SYS
AUD_HPOUT_R_CON
AUD_SLEEVE_CON
R3005 1 2 0R0402-PAD-1-GP

AUD_RING_CON 28
HP_JACK_IN 24
AUD_SLEEVE_CON 28

EMC ED3001 AZ5125-02S-R7G-GP 75.05125.07D
EMC ED3002 AZ5125-02S-R7G-GP 75.05125.07D
EMC ED3003 AZ5125-02S-R7G-GP 75.05125.07D
SC1KP50V2KX-1GP EC3006
SC1KP50V2KX-1GP EC3007
Close to AUD1
Close to AUD1
Close to AUD1
Moat

R3006 1 2 0R0402-PAD-1-GP
AGND
EC3005 1 2 SCD1U6D3V1KX-GP
AGND
Moat

AUDIO JACK SENSE

SENSE_A_SYS_HP 27
HP_JACK_SYS
R3002 22KR2J-GP
HP_JACK_SYS_R
Q3001 T2N7002BK-2-GP
R3010 100KR2J-1-GP
C3001 SC2D2U10V3KX-1GP
AGND
AGND

LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

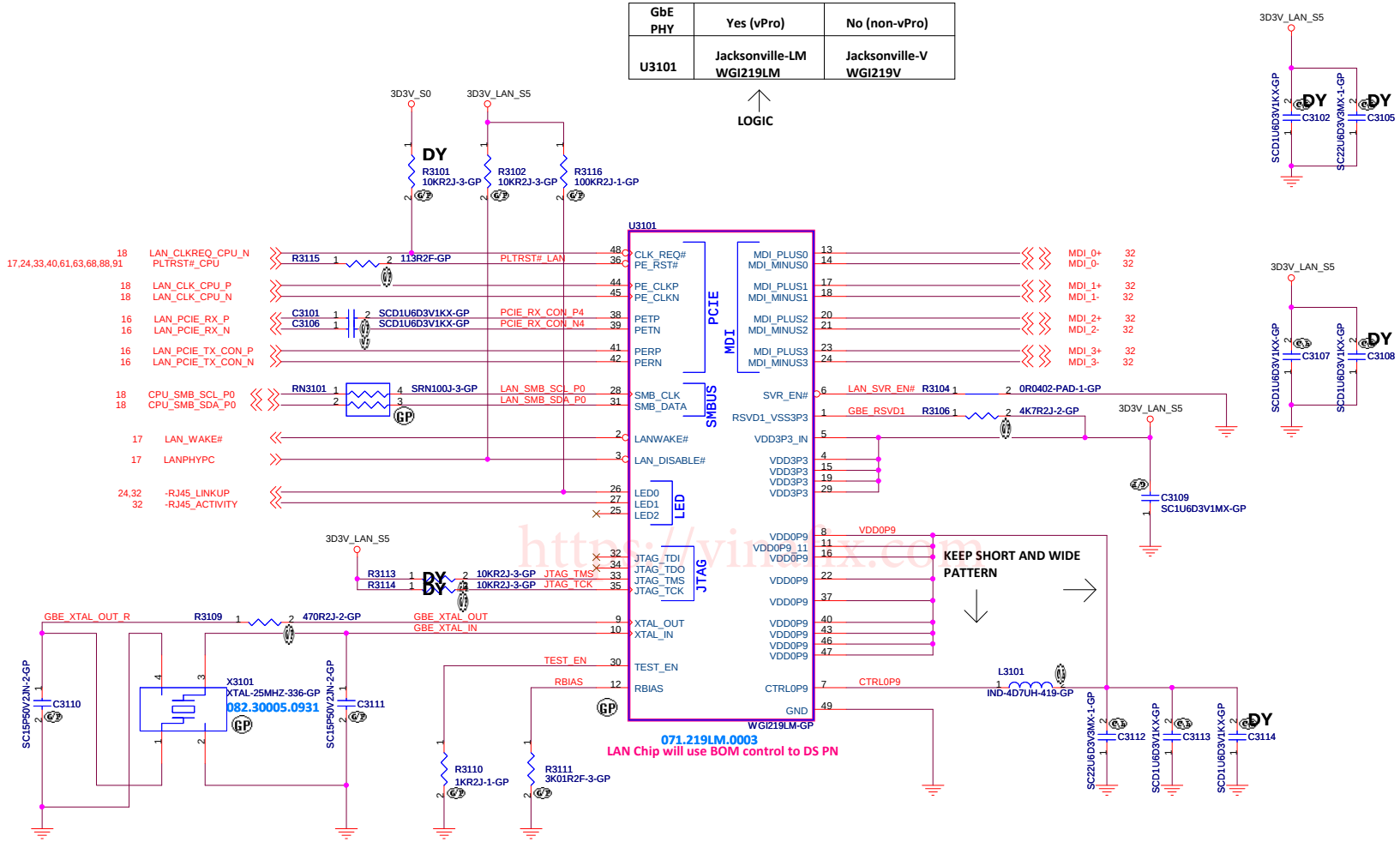
Title: AUDIO (AUDIO JACK)
Size: A3
Document Number: Kylo-2 teknisi indonesia
Rev: 1M
Date: Wednesday, October 17, 2018
Sheet 30 of 99

KL2_SIT_MB_W006
KL2_SIT_MB_W026
KL2_SVT_MB_W003
KL2_SVT_MB_W009

vPro Capability Need BOM control vPro/non-vPro

GbE PHY	Yes (vPro)	No (non-vPro)
U3101	Jacksonville-LM WGI219LM	Jacksonville-V WGI219V

LOGIC



25MHz (X3101)

TXC	7R25000008	082.30005.0931
HARMONY	X2V025000DC1H-HU	082.30005.0A81

LKL-2

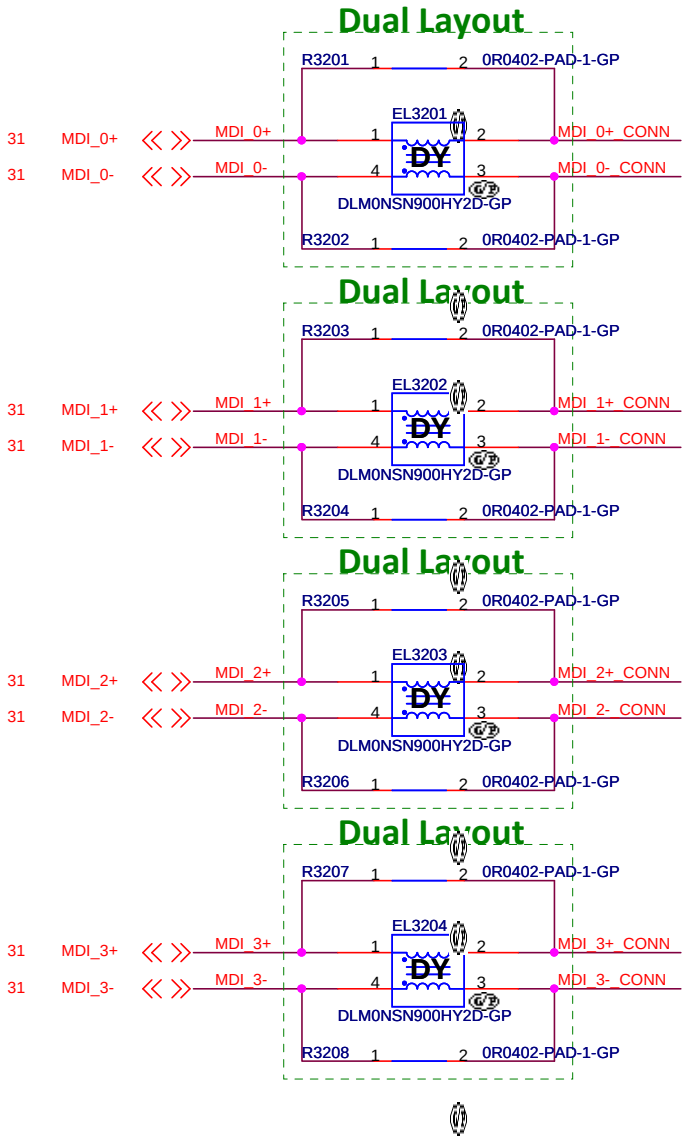
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

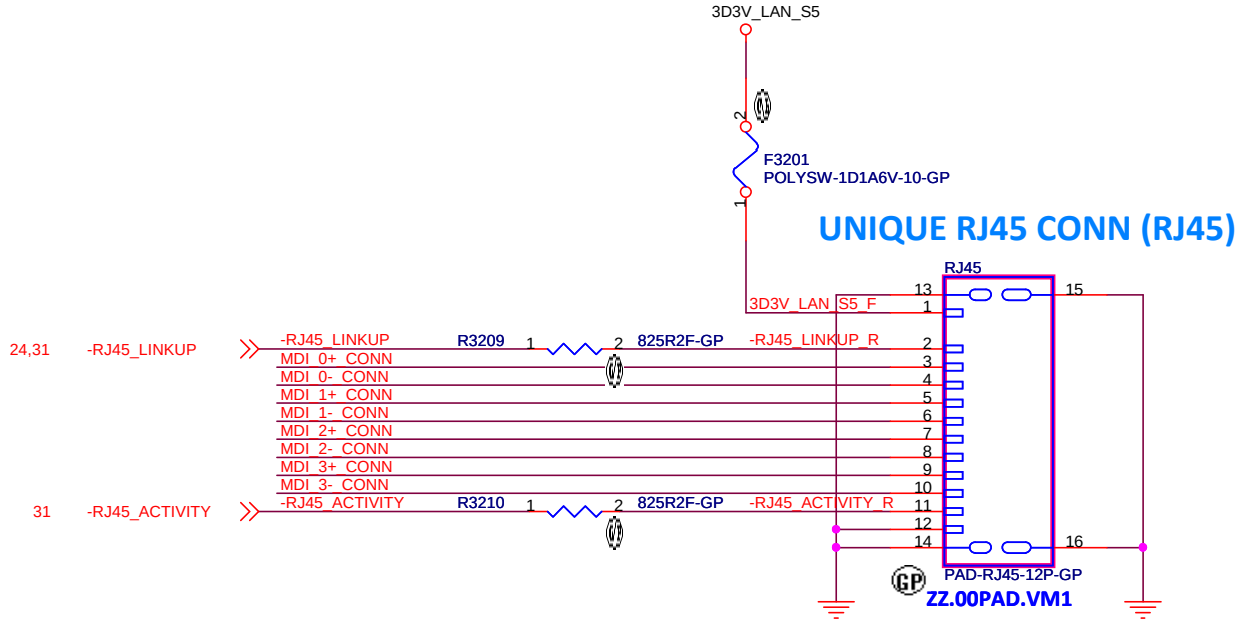
Title: LAN (GIGA_WGI219LM)

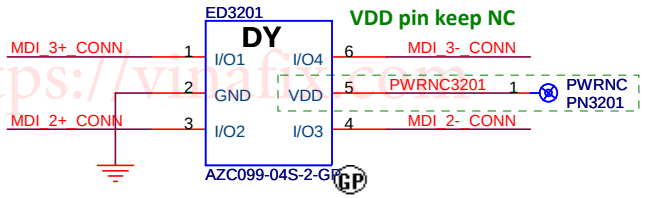
Size	Document Number	Rev
A3	Kylo-2	1M

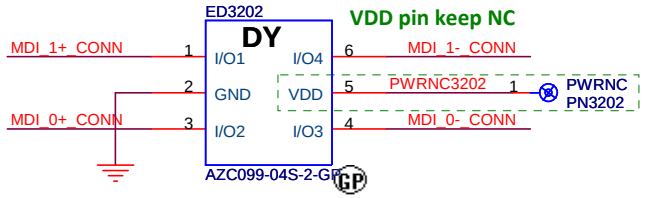
Date: Wednesday, October 17, 2018 Sheet 31 of 99

Dual Layout









LKL-2

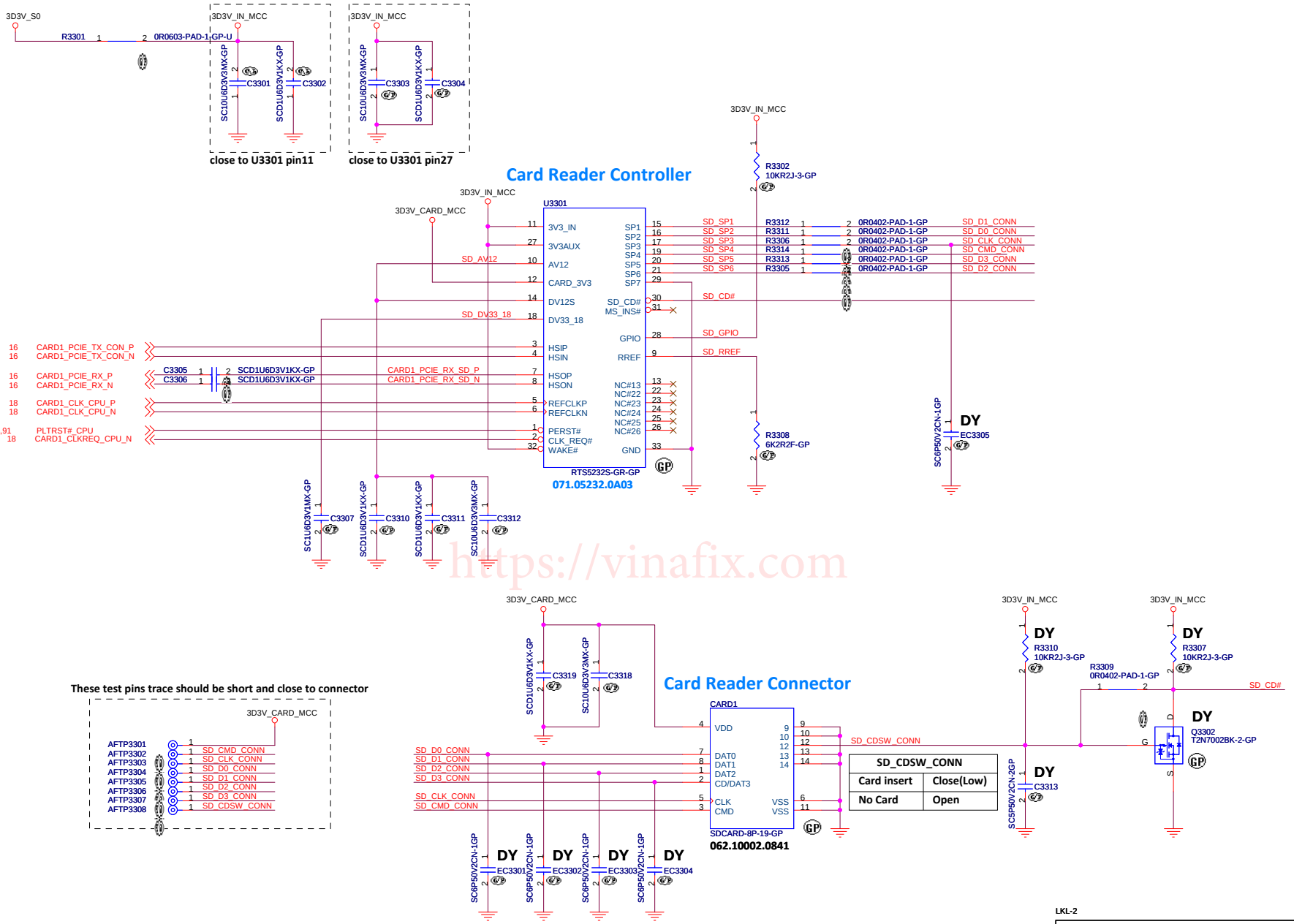
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN (GBE DONGLE I/F)***

Size	Document Number	Rev
A4	**Kylo-2**	**1M**

Date: Wednesday, October 17, 2018 Sheet 32 of 99

KL2_SIT_MB_W006
KL2_SIT_MB_W033
KL2_SVT_MB_W009



SD_CDSW_CONN	
Card insert	Close(Low)
No Card	Open

LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARDREADER (SDIO/SD CONN)

Size	Document Number	Rev
A3	Kylo-2	1M

Date: Wednesday, October 17, 2018 Sheet 33 of 99

BLANK

LKL-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

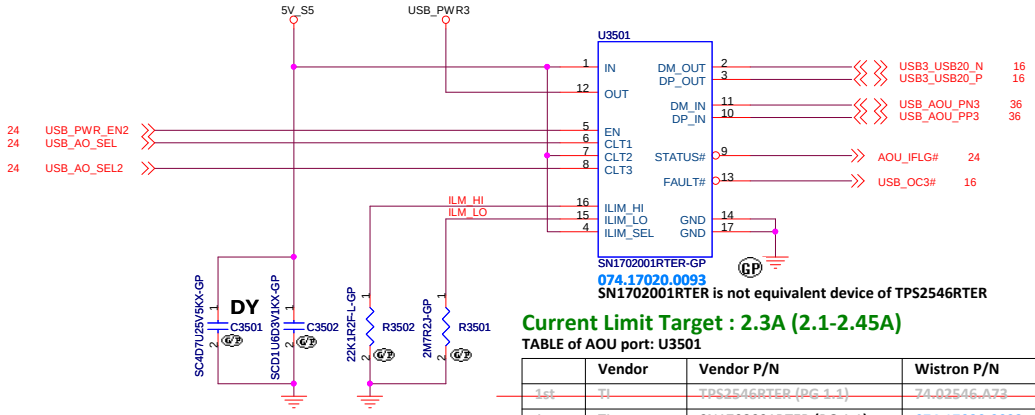
Title: ***USB (RSVD)***

Size	Document Number	Rev
A4	Kylo-2	1M

Date: Wednesday, October 17, 2018 Sheet 34 of 99

Main Func = USB Charger

For USB3.0 System Port3 (For AOU)



074.17020.0093

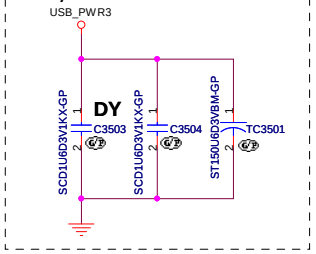
SN1702001RTER is not equivalent device of TPS2546RTER

Current Limit Target : 2.3A (2.1-2.45A)

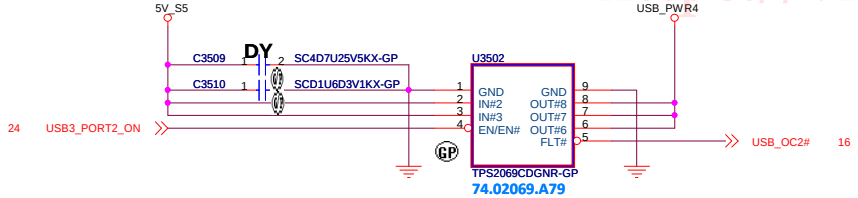
TABLE of AOU port: U3501

	Vendor	Vendor P/N	Wistron P/N	
~~1st~~	~~TI~~	~~TPS2546RTER (PG 1.1)~~	~~74.02546.A73~~	(had iPhone 6/7 charging issue)
1st	TI	SN1702001RTER (PG 1.1)	074.17020.0093	
~~2nd~~	~~Pericom~~	~~PI5USB2546ZHEX REV.X~~	~~074.52546.0A73~~	(had iPhone 6/7 charging issue)
2nd	DIODES	PI5USB2546HZHEX	074.52546.0D73	

Layout Note: Close USB3.0 Port3



For USB3.0 System Port4



74.02069.A79

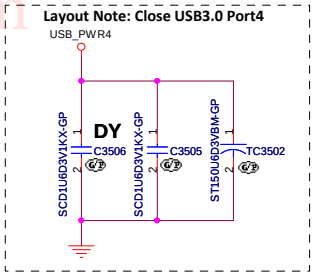
Continous Current Limit 1.5A

Non-Common Part

TABLE of USB 3.0 port: U3502

	Vendor	Vendor P/N	Wistron P/N
1st	TI	TPS2069CDGNR	74.02069.A79
2nd	ROHM	BD82032FVJ-GE2	74.82032.07G

Layout Note: Close USB3.0 Port4



LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

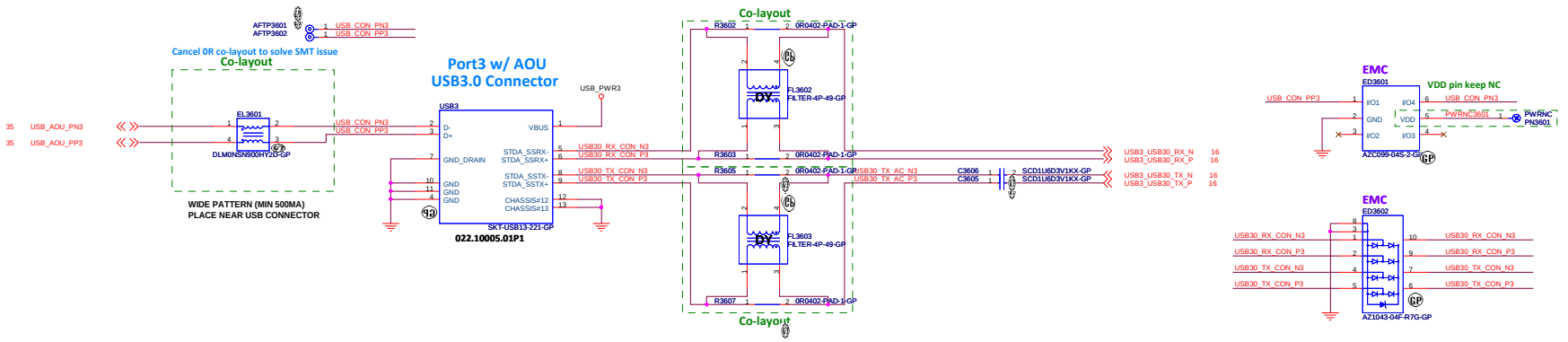
Title: USB (CHARGER/SWITCH)

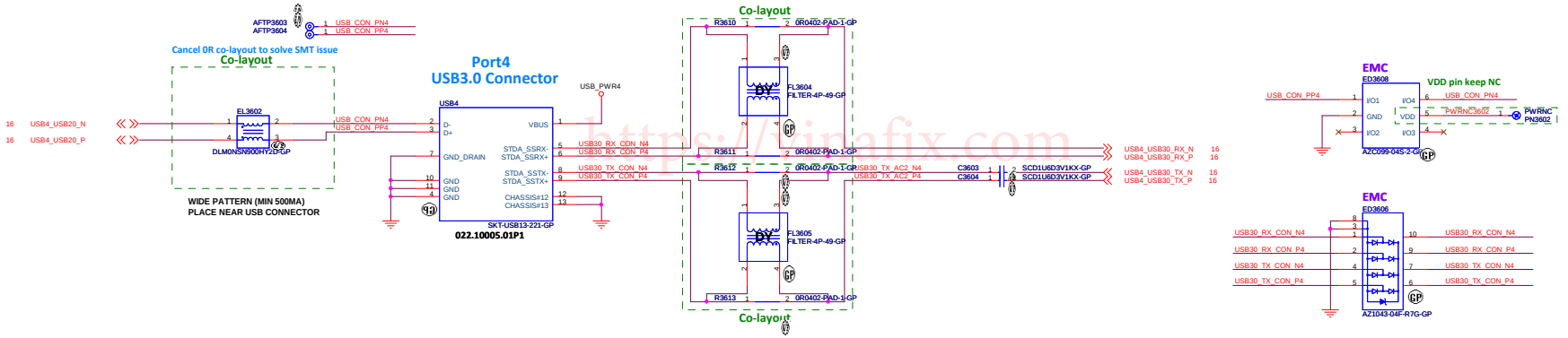
Size: A3 | Document Number: Kylo-2 | Rev: 1M

Date: Wednesday, October 17, 2018 | Sheet 35 of 99

Main Func = USB3.0 Port3 w/ AOU
Main Func = USB3.0 Port4

KL2_SIT_MB_W006
KL2_SIT_MB_W022
KL2_SVT_MB_W009
KL2_SVT_MB_W010





Vinafix.com

LKL-2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (USB3.0 CONN)

Size: A2 | Document Number: Kylo-2 | Rev: 1M

Date: Wednesday, October 17, 2018 | Sheet 38 of 99

KL2_SIT_MB_W006
KL2_SVT_MB_W009

3D3V_SUS — R3701 0R0603-PAD-1-GP-U — 3D3V_PS8747B

3D3V_PS8747B

R3733 2 — 1 4K7R2J-2-GP PS8747_CEQ_SDA1

R3706 2 — DY — 1 4K7R2J-2-GP PS8747_I2C_CTL1 R3707 2 — 1 4K7R2J-2-GP

R3708 2 — DY — 1 4K7R2J-2-GP PS8747_DCICFG_ADDR1 R3709 2 — DY — 1 4K7R2J-2-GP

PS8747_I2C_CTL1 =		
L: Pin Control is selected	R3706: DY, R3707: ASM	<-- LOGIC
H: I2C Control is selected	R3706: ASM, R3707: DY	

PS8747_DCICFG_ADDR1 =		
(Pin Control mode only) =		
L: DCI mode disabled	R3708: DY, R3709: ASM	
H: DCI mode enabled	R3708: ASM, R3709: DY	
M: Automatic DCI mode entering enabled	R3708: DY, R3709: DY	<-- LOGIC
(I2C Control mode only) =		
L: 0x20/0x21 (Default)	R3708: DY, R3709: ASM	
H: 0x22/0x23	R3708: ASM, R3709: DY	

3D3V_PS8747B

C3701 DY SCD1U6D3V1KX-GP
C3702 DY SCD1U6D3V1KX-GP
C3703 SCD1U6D3V1KX-GP
C3705 SCD1U6D3V1KX-GP
C3706 DY SCD01U50V2KX-1GP
C3707 DY SCD01U50V2KX-1GP
C3708 SCD01U50V2KX-1GP
C3704 SCD01U50V2KX-1GP

C3709 SC2D2U10V3KX-1GP

U3701

EPAD VDD33 VDD33 VDD33_CEXT VDD_DCI

ML0P ML0N ML3P ML3N

SSDE/DCI_DATA CDE/DCI_CLK SSRXP SSRXN SSTXP SSTXN

RX1P RX1N RX2P RX2N TX1P TX1N TX2P TX2N

ML2P ML2N ML1P ML1N AUXP AUXN

CE_DP CE_USB FLIP SBU1 SBU2 IN_HPD

I2C_EN DCICFG DPEQ CEQ REXT

1 Port USB + 2 Lanes DP

PS8747BQFN40GTR-B1-GP
071.08747.0003
Lenovo P/N:PS8747B

4	DP1_DDI_TX_P0	C3710	SCD1U6D3V1KX-GP	USBC_DP0P_C	R3726	5D1R2J-1-GP	USBC_DP0P_C_R
4	DP1_DDI_TX_N0	C3711	SCD1U6D3V1KX-GP	USBC_DP0N_C	R3727	5D1R2J-1-GP	USBC_DP0N_C_R
4	DP1_DDI_TX_P3	C3712	SCD1U6D3V1KX-GP	USBC_DP3P_C	R3718	5D1R2J-1-GP	USBC_DP3P_C_R
4	DP1_DDI_TX_N3	C3713	SCD1U6D3V1KX-GP	USBC_DP3N_C	R3719	5D1R2J-1-GP	USBC_DP3N_C_R
16	USB1_USB30_RX_P	C3714	SCD1U6D3V1KX-GP	USB30_RX_CPU_P1_C			
16	USB1_USB30_RX_N	C3715	SCD1U6D3V1KX-GP	USB30_RX_CPU_N1_C			
16	USB1_USB30_TX_P	C3716	SCD1U6D3V1KX-GP	USB30_TX_CPU_P1_C			
16	USB1_USB30_TX_N	C3717	SCD1U6D3V1KX-GP	USB30_TX_CPU_N1_C			
4	DP1_DDI_TX_P2	C3718	SCD1U6D3V1KX-GP	USBC_DP2P_C	R3720	5D1R2J-1-GP	USBC_DP2P_C_R
4	DP1_DDI_TX_N2	C3719	SCD1U6D3V1KX-GP	USBC_DP2N_C	R3721	5D1R2J-1-GP	USBC_DP2N_C_R
4	DP1_DDI_TX_P1	C3720	SCD1U6D3V1KX-GP	USBC_DP1P_C	R3722	5D1R2J-1-GP	USBC_DP1P_C_R
4	DP1_DDI_TX_N1	C3721	SCD1U6D3V1KX-GP	USBC_DP1N_C	R3723	5D1R2J-1-GP	USBC_DP1N_C_R
4	DP1_AUX_CPU_P	C3722	SCD1U6D3V1KX-GP	USBC_AUXP_C	R3724	0R0402-PAD-1-GP	USBC_AUXP_C_R
4	DP1_AUX_CPU_N	C3723	SCD1U6D3V1KX-GP	USBC_AUXN_C	R3725	0R0402-PAD-1-GP	USBC_AUXN_C_R

USBC_RX1P_CONN1	39	USBC_RX1P
USBC_RX1N_CONN1	39	USBC_RX1N
USBC_RX2P_CONN1	39	USBC_RX2P
USBC_RX2N_CONN1	39	USBC_RX2N
USBC_TX1P_CONN1	39	USBC_TX1P
USBC_TX1N_CONN1	39	USBC_TX1N
USBC_TX2P_CONN1	39	USBC_TX2P
USBC_TX2N_CONN1	39	USBC_TX2N

3D3V_PS8747B

USBC_DP_MODE_R R3710 — DY — 10KR2J-3-GP
USBC_USB_MODE_R R3712 — DY — 10KR2J-3-GP
USBC_POL_R R3730 — DY — 10KR2J-3-GP

USBC_DP_MODE_R R3717 — 0R0402-PAD-1-GP — USBC_DP_MODE 38
USBC_USB_MODE_R R3728 — 0R0402-PAD-1-GP — USBC_USB_MODE 38
USBC_POL_R R3729 — 0R0402-PAD-1-GP — USBC_POL 38

To 65988

USBC1_SBU1 39
USBC1_SBU2 39
USBC_HPD_MUX1 4,38

3D3V_PS8747B

RN3701 SRN100KJ-6-GP
USBC_AUXN_C
USBC_AUXP_C

24,38,58 I2C_CLK_PD
24,38,58 I2C_DATA_PD

R3715 DY 0R2J-2-GP PS8747_I2C_CTL1
R3716 DY 0R2J-2-GP PS8747_DCICFG_ADDR1 PS8747_DPEQ_SCL1 PS8747_CEQ_SDA1

R3714 4K99R2F-L-GP
R3731 2MR2-GP
R3732 2MR2-GP

LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (TYPEC MUX PS8747B)

Size	Document Number	Rev
A3	Kylo-2	1M

Date: Wednesday, October 17, 2018 Sheet 37 of 99

TABLE BUSPOWER Configuration (PD_ADCIN1 Resister Divider)

DIV = R3804 / (R3802 + R3804)		Configuration
DIV MIN	DIV MAX	
0.00	0.18	BP_NoRespones
0.20	0.38	BP_WaitForV3_Internal
0.40	0.58	BP_WaitForV3_External
0.60	1.00	BP_NoWait

LOGIC

DIV = R2 / (R1 + R2)

BUSPOWER Config.
BP_NoWait

TABLE I2C Addrssing (TBD)

I2C1 (to EC)	USB1 PORT	0X23
	USB2 PORT	0X27
I2C2 (to AR)	USB1 PORT	0X38
	USB2 PORT	0X3F

PLACE NEAR U3801

Non-Common Part
D3801,D3802
ONSEMI NSR20F30NXT5G 083.20F30.008H
VISHAY VSKY20301608 083.20301.008F

(Split-pad)
SN1701012RJTR
TPS65988CE RJTR Symbol

(with split-pad)
SN1701012 is equivalent device of TPS65988
Need to BOM control by co-lay symbol issue

1MB (8Mb) 150MIL SOIC8 (BIOS2):
WINBOND W25Q80DVSNIG 072.25Q80.0C01
MACRONIX MX25L8006EM1I-12G 072.25806.0A01

LKL-2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (TYPEC PD TPS65988)
Size: Custom | Document Number: Kylo-2 | Rev: 1M
Date: Wednesday, October 17, 2018 | Sheet 38 of 99

KL2_SIT_MB_W006
KL2_SIT_MB_W007
KL2_SVT_MB_W008
KL2_SVT_MB_W010

CC PROTECTION

U3901 SN1710033RUKR-1-GP
074.17100.0073
MP version

TS3USB31E is placed for security reason.
When unknown USB Type-C power adapter is attached, utility in OS shuts down USB 2.0 signal from USB Type-C port to avoid computer virus.

VOLTAGE MONITOR

The VBIAS pin requires a minimum 35-VDC rated capacitor, and a 50-VDC rated capacitor is recommended.

Place on BOTTOM side

Cancel 0R co-layout to solve SMT issue
Co-layout

Port1
USB TYPE-C CONN

USB2 SKT-USB30-46-GP
062.10009.00D1

EMC ED3901 AZ1043-04F-R7G-GP

EMC ED3902 AZ1043-04F-R7G-GP

VDD pin keep NC
ED3903 AZC099-04S-2-GP

EL3901 DLM0NSN900HY2D-GP

CC PROTECTION

U3904 SN1710033RUKR-1-GP
074.17100.0073
MP version

TS3USB31E is placed for security reason.
When unknown USB Type-C power adapter is attached, utility in OS shuts down USB 2.0 signal from USB Type-C port to avoid computer virus.

VOLTAGE MONITOR

The VBIAS pin requires a minimum 35-VDC rated capacitor, and a 50-VDC rated capacitor is recommended.

Place on BOTTOM side

Cancel 0R co-layout to solve SMT issue
Co-layout

Port2
USB TYPE-C CONN

USB1 SKT-USB30-46-GP
062.10009.00D1

EMC ED3905 AZ1043-04F-R7G-GP

EMC ED3907 AZ1043-04F-R7G-GP

VDD pin keep NC
ED3906 AZC099-04S-2-GP

EL3902 DLM0NSN900HY2D-GP

LKL-2

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Title: USB (TYPEC CONN)
Size: Custom | Document Number: Kylo-2 | Rev: 1M
Date: Wednesday, October 17, 2018 | Sheet 39 of 99

Main Func = Power Plane & Sequence

KL2_SIT_MB_W006
KL2_SIT_MB_W029
KL2_SIT_MB_W038
KL2_SVT_MB_W009
KL2_SVT_MB_W018

Run Power

5V_S0 — 5V_S0 Consumption Peak current 5A

3D3V_S0 — 3D3V_S0 Consumption Peak current 2.5A

1V_VCCIO

1V_VCCSTG

1V_VCCST

For Deep Sx Configured Systrem (Support Energy Star 7.0)

3D3V_SUS — 3D3V_SUS Consumption Peak current x.xA

NON_DEEP

NON_DEEP function for bring up

CPU C10 Function Reserved (For Power Saving)

1D2V_VCCSFR_OC

Non-Common Part

Power Good

[#543016] Optional, Added for addition system robustness

Title	SEQUENCE (POWER PLANE EN)
Size	A3
Document Number	Kylo-2
Rev	1M
Date	Thursday, November 06, 2014
Sheet	60 of 69

Wistron Corporation
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BLANK

LKL-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

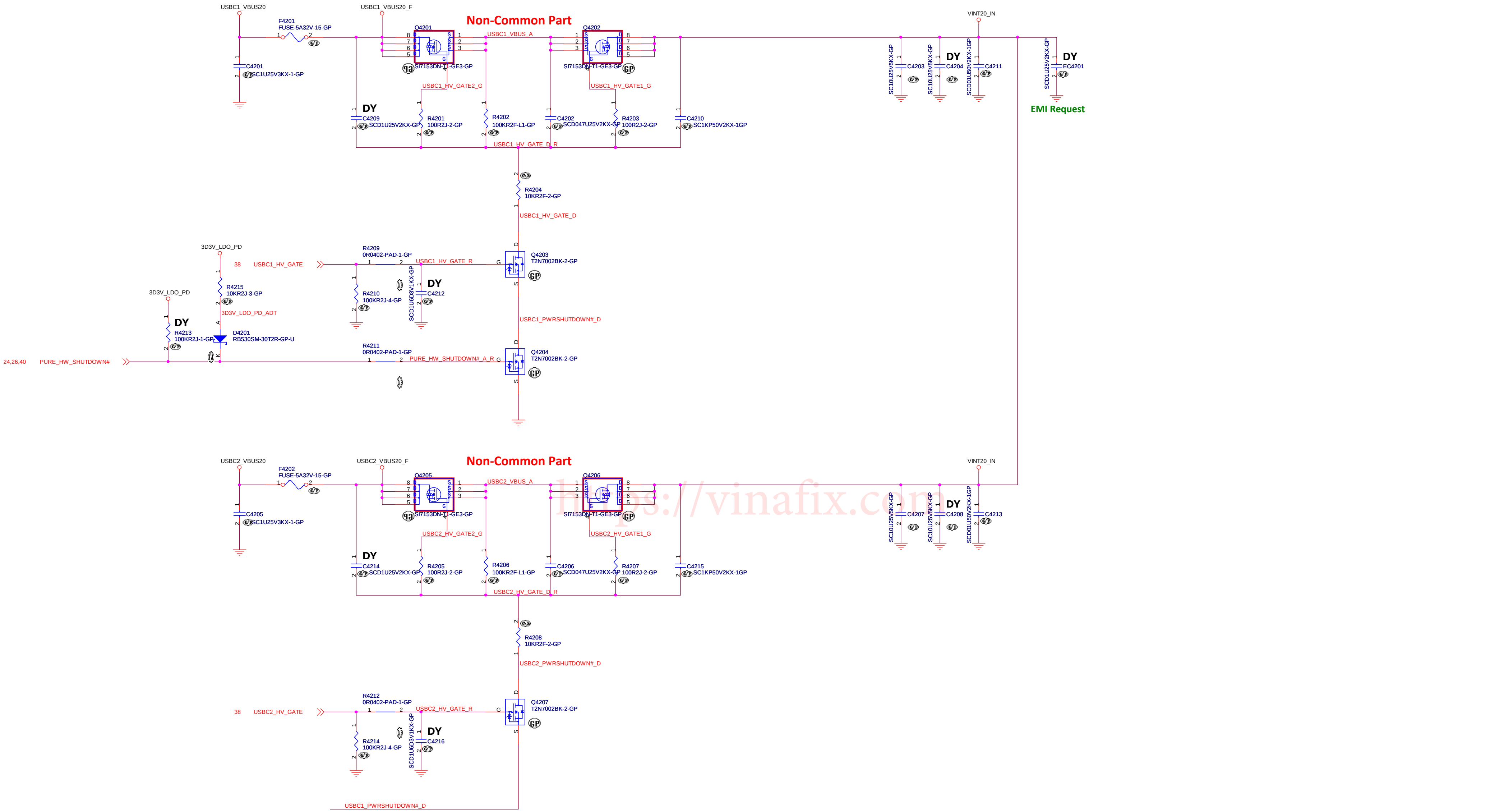
Title: ***SEQUENCE (RSVD)***

Size	Document Number	Rev
A4	Kylo-2	1M

Date: Wednesday, October 17, 2018 Sheet 41 of 99

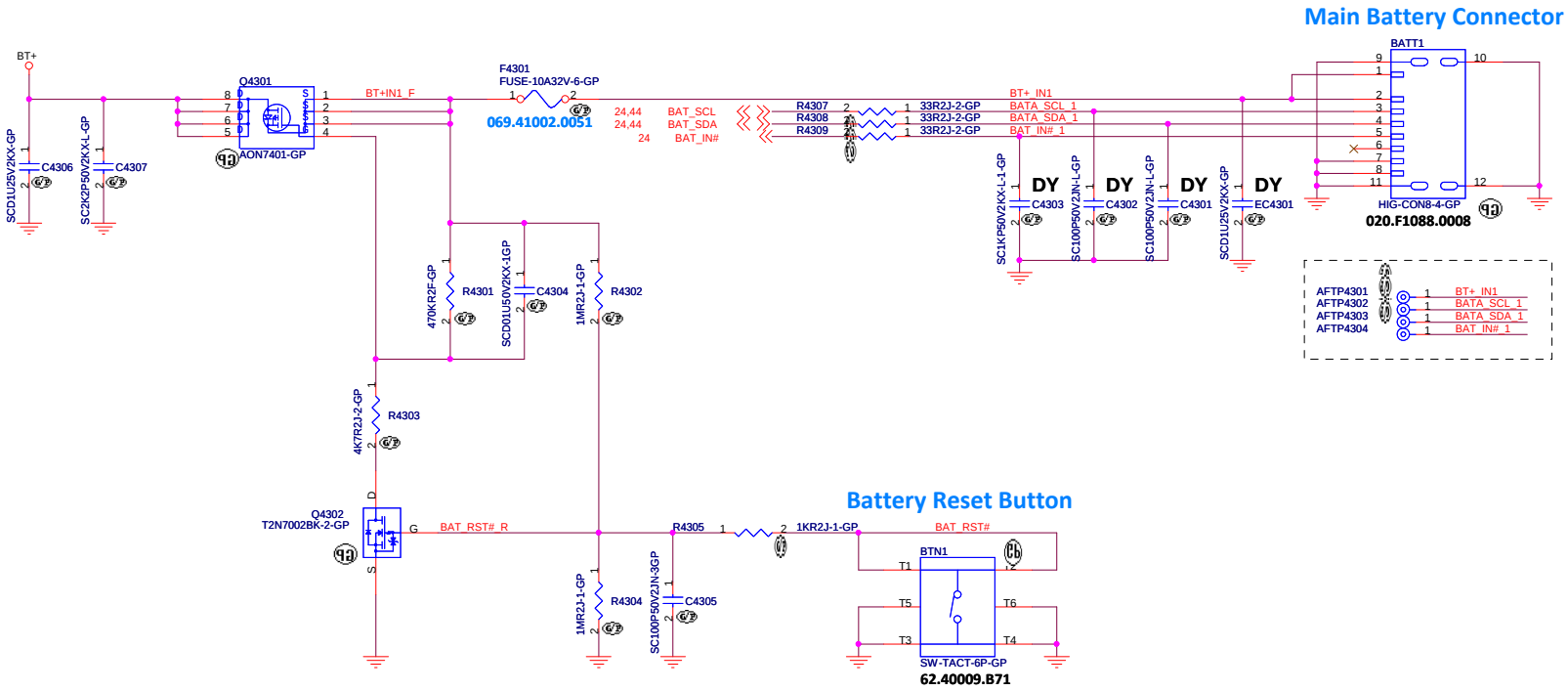
Q4201, Q4202, Q4205, Q4206

	1st	VISHAY	SI7153DN-T1-GE3	084.07153.0037
OBS	2nd	FAIRCHILD	FDMC6679AZ	084.06679.M001


USBC1_VBUS20
USBC1_VBUS20_F
F4201
FUSE-5A32V-15-GP
C4201
SC1U25V3KX-1-GP
Non-Common Part
Q4201
SI7153DN-T1-GE3-GP
USBC1_VBUS_A
Q4202
SI7153DN-T1-GE3-GP
USBC1_HV_GATE2_G
USBC1_HV_GATE1_G
DY
C4209
SCD1U25V2KX-GP
R4201
100R2J-2-GP
R4202
100KR2F-L1-GP
C4202
SCD047U25V2KX-GP
R4203
100R2J-2-GP
C4210
SC1KP50V2KX-1GP
USBC1_HV_GATE_D_R
VINT20_IN
SC10U25V5KX-GP
C4203
C4204
C4211
SCD01U50V2KX-1GP
SCD1U25V2KX-GP
EC4201
EMI Request
R4204
10KR2F-2-GP
USBC1_HV_GATE_D
3D3V_LDO_PD
38 USBC1_HV_GATE
R4209
0R0402-PAD-1-GP
USBC1_HV_GATE_R
Q4203
T2N7002BK-2-GP
R4215
10KR2J-3-GP
R4210
100KR2J-4-GP
SCD1U6D3V1KX-GP
C4212
3D3V_LDO_PD_ADT
R4213
100KR2J-1-GP
D4201
RB530SM-30T2R-GP-U
USBC1_PWRSHUTDOWN#_D
R4211
0R0402-PAD-1-GP
Q4204
T2N7002BK-2-GP
24,26,40 PURE_HW_SHUTDOWN#
PURE_HW_SHUTDOWN#_A_R
USBC2_VBUS20
USBC2_VBUS20_F
F4202
FUSE-5A32V-15-GP
C4205
SC1U25V3KX-1-GP
Non-Common Part
Q4205
SI7153DN-T1-GE3-GP
USBC2_VBUS_A
Q4206
SI7153DN-T1-GE3-GP
C4207
C4208
C4213
USBC2_HV_GATE2_G
USBC2_HV_GATE1_G
C4214
SCD1U25V2KX-GP
R4205
100R2J-2-GP
R4206
100KR2F-L1-GP
C4206
SCD047U25V2KX-GP
R4207
100R2J-2-GP
C4215
SC1KP50V2KX-1GP
USBC2_HV_GATE_D_R
R4208
10KR2F-2-GP
USBC2_PWRSHUTDOWN#_D
38 USBC2_HV_GATE
R4212
0R0402-PAD-1-GP
USBC2_HV_GATE_R
Q4207
T2N7002BK-2-GP
R4214
100KR2J-4-GP
C4216
USBC1_PWRSHUTDOWN#_D

LKL-2

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*INT IO (DC-IN)*
Size A2 · Document Number	Kylo-2 · Rev 1M
Date: Wednesday, October 17, 2018	Sheet 42 of 99



LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (BATT CONN)

Size: A3 | Document Number: Kylo-2 | Rev: 1M

Date: Wednesday, October 17, 2018 | Sheet 43 of 99

OFFPAGE

PH on EE Side

24,43 BAT_SCL → BAT_SCL

24,43 BAT_SDA → BAT_SDA

PH on EE Side

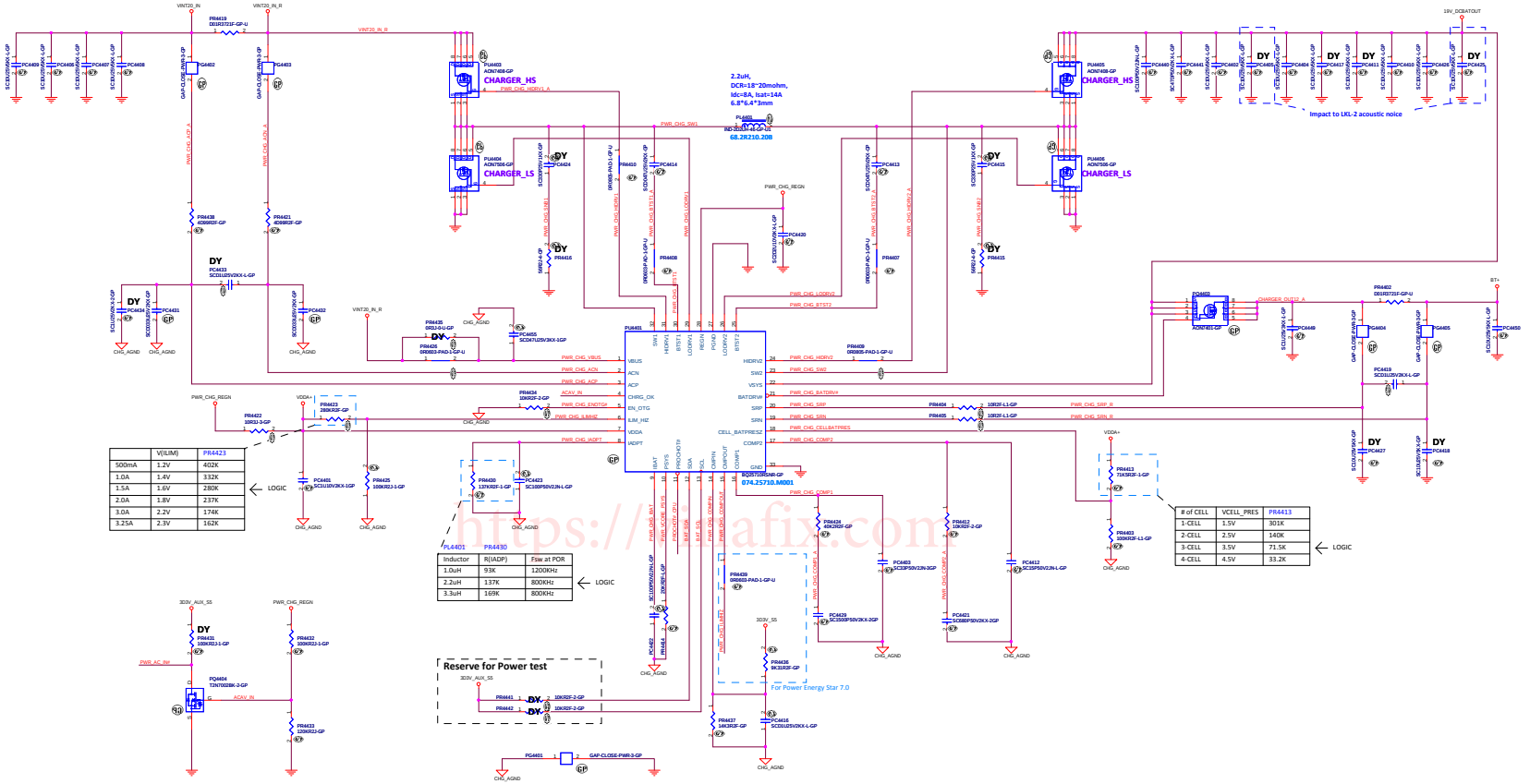
3,24,46 PROCHOTH_CPU → PROCHOTH_CPU

46 PWR_VCORE_PSYS → PWR_VCORE_PSYS

24 PWR_AC_IN# → PWR_AC_IN#

24 ACAV_IN → ACAV_IN

24 PWR_CHG_IADPT → PWR_CHG_IADPT



	V(ILIM)	PR4423
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

PL4401 PR4430

Inductor	R(IADP)	Fsw at POR
1.0uH	93K	1200KHz
2.2uH	137K	800KHz
3.3uH	169K	800KHz

# of CELL	VCELL_PRES	PR4413
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (CHARGER_BQ25710RSNR)

Size	Document Number	Rev
A3	Kylo-2	1M

Date: Wednesday, October 27, 2010 Sheet 44 of 59

KL2_SIT_MB_W009
KL2_SIT_MB_W021
KL2_SVT_MB_W004
KL2_SVT_MB_W007

OFFPAGE-Signal

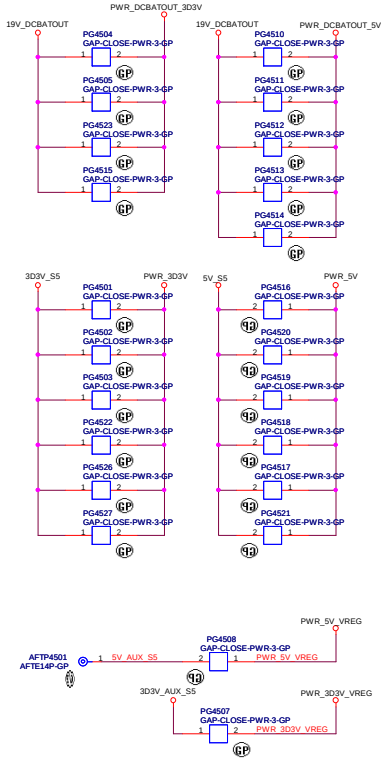
40 PWR_5V_EN >> PWR_5V_EN

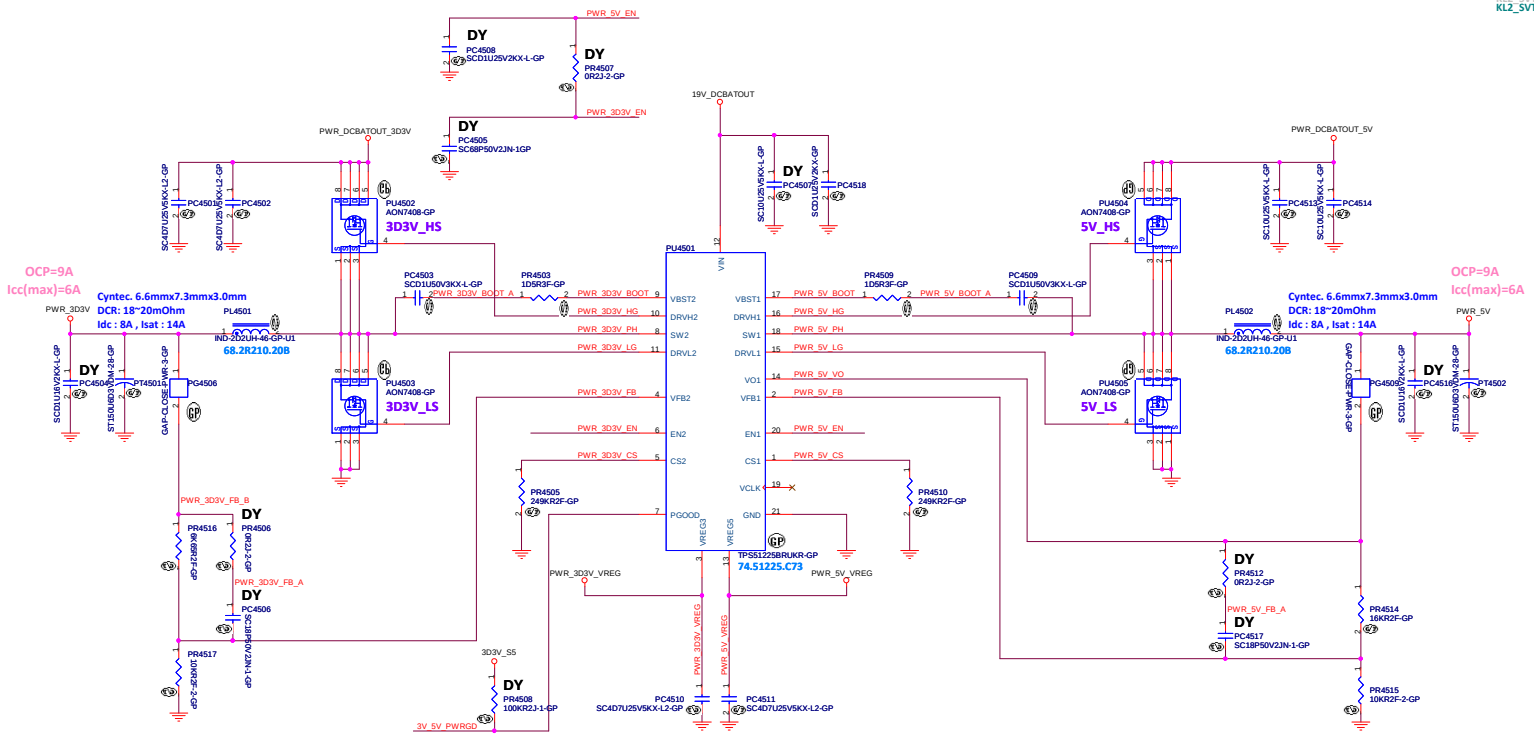
40 PWR_3D3V_EN >> PWR_3D3V_EN

PH on EE Side

17,40 3V_5V_PWRGD << 3V_5V_PWRGD

OFFPAGE-GAP





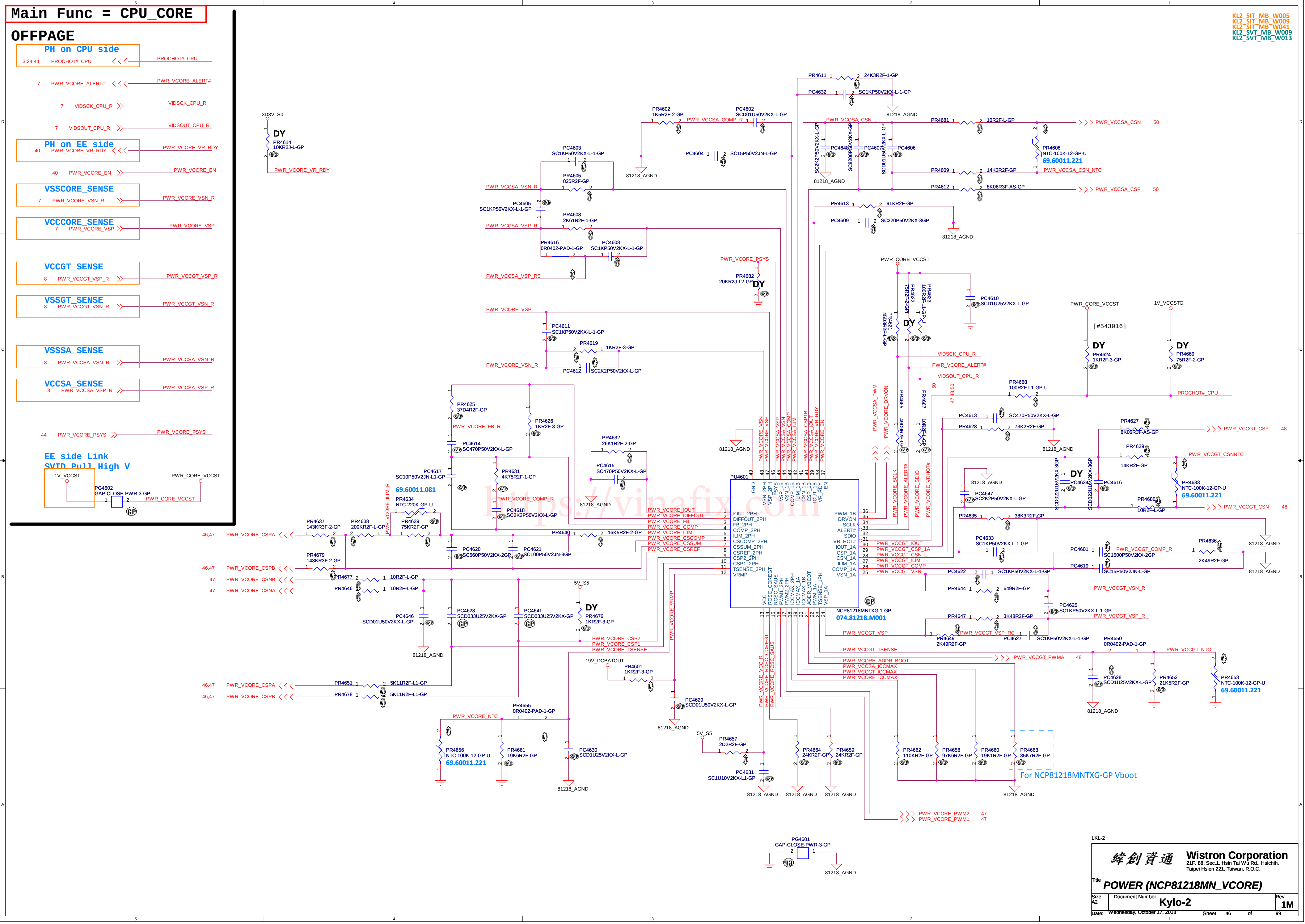
LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (TPS51225B_5V/3D3V)

Size: A2 | Document Number: Kylo-2 | Rev: 1M

Date: Wednesday, October 17, 2018 | Sheet 45 of 99



Main Func = CPU_CORE
OFFPAGE
PH on CPU side
PROCHOT#_CPU
PWR_VCORE_ALERT#
VIDSCK_CPU_R
VIDSOUT_CPU_R
PH on EE side
PWR_VCORE_VR_RDY
PWR_VCORE_EN
VSSCORE_SENSE
PWR_VCORE_VSN_R
VCCCORE_SENSE
PWR_VCORE_VSP
VCCGT_SENSE
PWR_VCCGT_VSP_R
VSSGT_SENSE
PWR_VCCGT_VSN_R
VSSSA_SENSE
PWR_VCCSA_VSN_R
VCCSA_SENSE
PWR_VCCSA_VSP_R
PWR_VCORE_PSYS
EE side Link
SVID Pull High V
1V_VCCST
PWR_CORE_VCCST
PG4602
GAP-CLOSE-PWR-3-GP
PU4601
NCP81218MNTXG-1-GP
074.81218.M001
For NCP81218MNTXG-GP Vboot
PG4601
GAP-CLOSE-PWR-3-GP
81218_AGND
PWR_VCCSA_CSN
PWR_VCCSA_CSP
PWR_VCCGT_CSP
PWR_VCCGT_CSN
PWR_VCCGT_PWMA
PWR_VCORE_PWM2
PWR_VCORE_PWM1
PWR_VCORE_CSPA
PWR_VCORE_CSPB
PWR_VCORE_CSNB
PWR_VCORE_CSNA
KL2_SIT_MB_W005
KL2_SIT_MB_W009
KL2_SIT_MB_W041
KL2_SVT_MB_W009
KL2_SVT_MB_W013
LKL-2
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
POWER (NCP81218MN_VCORE)
Size A2
Document Number
Kylo-2
Rev 1M
Date: Wednesday, October 17, 2018
Sheet 46 of 99

Main Func = CPU_CORE

OFFPAGE

KL2_SIT_MB_W024
KL2_SVT_MB_W004
KL2_SVT_MB_W007
KL2_SVT_MB_W009
KL2_SVT_MB_W011
KL2_SVT_MB_W014
KL2_SVT_MB_W016
KL2_SVT_MB_W017

For acoustic noice

19V_DCBATOUT

PT4704 ST15U25VDM-1-GP

PT4703 ST15U25VDM-1-GP

5V_S5

PR4702 2D2R2F-GP

PWR_VCORE_VCC1

PC4707 SC220U10V3KX-L-GP

PC4708 SC1U10V2KX-L1-GP

PR4701 3D9R3-GP

PWR_VCORE_BOOT_RC1

PWR_VCORE_BOOT1

PC4706 SCD22U25V3KX-GP

PWR_VCORE_PHASED1

PU4701

19V_DCBATOUT

PC4702 SC10U25V5KX-L-GP DY

PC4703 SC10U25V5KX-L-GP DY

PC4704 SC10U25V5KX-L-GP DY

PC4705 SC10U25V5KX-L-GP DY

Impact to LKL-2 acoustic noice

VIN VIN VIN VIN PHASE BOOT VCC VCCD

PWM DISB# THWN SMOD#

PR4704 0R0402-PAD-1-GP

PWR_VCORE_DISB#1

PWR_VCORE_PWM1 46

PWR_VCORE_DRVON 46,47,48,50

PGND PGND PGND PGND PGND

GL#27 GL#33 NC#6 AGND COND

VSW#16 VSW#17 VSW#18 VSW#19 VSW#20 VSW#21 VSW#22

VSW#26 VSW#25 VSW#24 VSW#23

NCP302045LMNTWG-GP

074.30204.M002

PWR_VCORE_GL1

PWR_VCORE_SW1

Cyntec. 7.45 x 6.8 x 4 mm

DCR: 0.66 mOhm

Idc : 36A , Isat : 46A

PL4701 IND-D15UH-33-GP

068.R1510.1171

1V_CPU_CORE

DY PR4703 2D2R5F-2-GP

PG4707 GAP-CLOSE-PWR-3-GP

PG4708 GAP-CLOSE-PWR-3-GP

PT4702 SE470U2VDM-GP

470uF / 2V,

ESR = 6m ohm,

Ripple current = 3500mA

PWR_VCORE_SNUB1

DY PC4709 SC2K2P50V2KX-L-GP

Confirm with EE:

22uF/0603 total 40pcs

46 PWR_VCORE_CSPA

46 PWR_VCORE_CSNA

5V_S5

PR4712 2D2R2F-GP

PWR_VCORE_VCC2

PC4721 SC220U10V3KX-L-GP

PC4728 SC1U10V2KX-L1-GP

PR4711 3D9R3-GP

PWR_VCORE_BOOT_RC2

PWR_VCORE_BOOT2

PC4722 SCD22U25V3KX-GP

PWR_VCORE_PHASED2

PU4702

19V_DCBATOUT

PC4725 SC10U25V5KX-L-GP

PC4724 SC10U25V5KX-L-GP

PC4723 SC10U25V5KX-L-GP DY

PC4729 SC10U25V5KX-L-GP DY

PC4726 SC10U25V5KX-L-GP DY

VIN VIN VIN VIN PHASE BOOT VCC VCCD

PWM DISB# THWN SMOD#

PR4714 0R0402-PAD-1-GP

PWR_VCORE_DISB#2

PWR_VCORE_PWM2 46

PWR_VCORE_DRVON 46,47,48,50

PGND PGND PGND PGND PGND

GL#27 GL#33 NC#6 AGND COND

VSW#16 VSW#17 VSW#18 VSW#19 VSW#20 VSW#21 VSW#22

VSW#26 VSW#25 VSW#24 VSW#23

NCP302045LMNTWG-GP

074.30204.M002

PWR_VCORE_GL2

PWR_VCORE_SW2

TDC=42A

Iomax=64A

OCP>80A

Cyntec. 7.45 x 6.8 x 4 mm

DCR: 0.66 mOhm

Idc : 36A , Isat : 46A

PL4702 IND-D15UH-33-GP

068.R1510.1171

1V_CPU_CORE

DY PR4713 2D2R5F-2-GP

PG4712 GAP-CLOSE-PWR-3-GP

PG4711 GAP-CLOSE-PWR-3-GP

DY PT4705 SE330U2VDM-4-GP

330uF / 2V,

ESR = 9m ohm,

Ripple current = 3000mA

PWR_VCORE_SNUB2

DY PC4727 SC2K2P50V2KX-L-GP

46 PWR_VCORE_CSPB

46 PWR_VCORE_CSNB

LKL-2

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (NCP302045M_VCORE)

Size: A2 | Document Number: Kylo-2 | Rev: 1M

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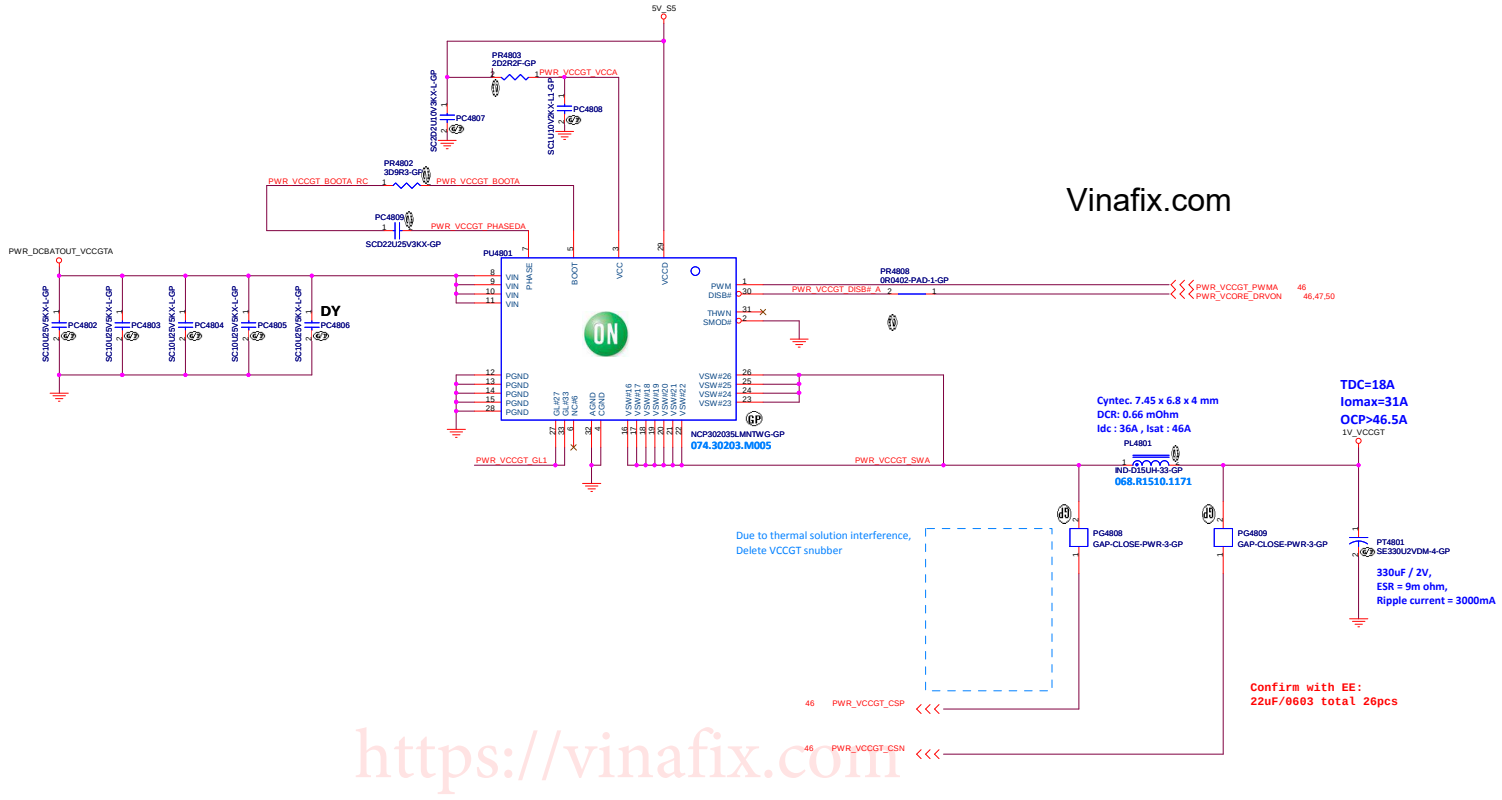
Main Func = VCCGT

OFFPAGE

19V_DCBATOUT
PWR_DCBATOUT_VCCGTA
PG4802 GAP-CLOSE-PWR-GP
PG4803 GAP-CLOSE-PWR-GP
PG4804 GAP-CLOSE-PWR-GP
PG4801 GAP-CLOSE-PWR-GP
PG4805 GAP-CLOSE-PWR-GP
PG4806 GAP-CLOSE-PWR-GP

KL2_SIT_MB_W024
KL2_SIT_MB_W039
KL2_SVT_MB_W005
KL2_SVT_MB_W007
KL2_SVT_MB_W009
KL2_SVT_MB_W014



LKL-2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: POWER (NCP302035M_VCCGT)		
Size: A2	Document Number: Kylo-2	Rev: 1M
Date: Wednesday, October 17, 2018	Sheet 48 of 99	

Main Func = CPU_CORE

BLANK

LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (RSVD)

Size	Document Number	Rev
A4	Kylo-2	1M

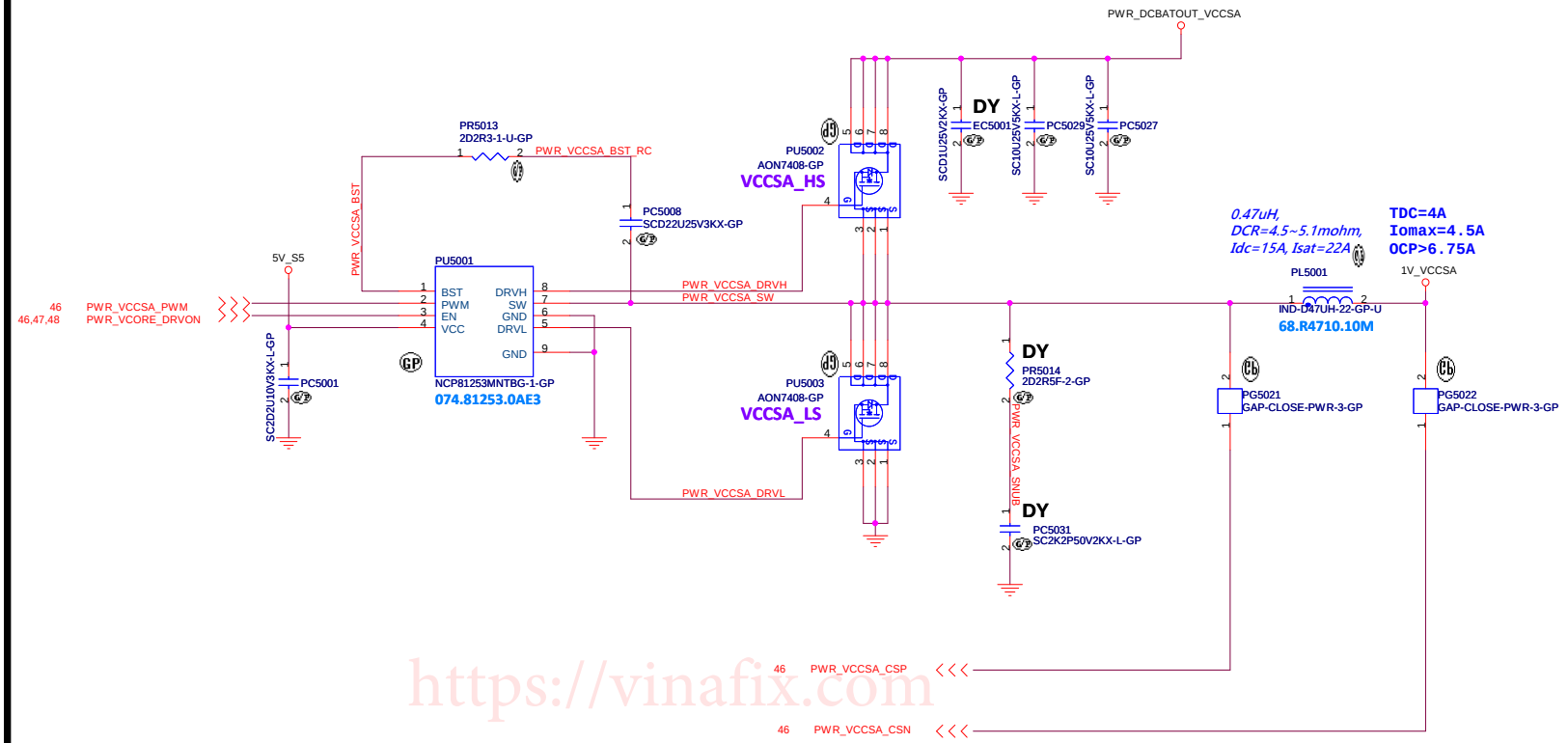
Date: Wednesday, October 17, 2018 Sheet 49 of 99

Main Func = VCCSA

KL2_SVT_MB_W004
KL2_SVT_MB_W007

OFFPAGE

19V_DCBATOUT — PG5002 GAP-CLOSE-PWR-3-GP — PWR_DCBATOUT_VCCSA
PG5003 GAP-CLOSE-PWR-3-GP



LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (NCP81253MN_VCCSA)

Size	Document Number	Rev
A3	Kylo-2	1M

Date: Wednesday, October 17, 2018 Sheet 50 of 99

OFFPAGE

S5
40 PWR_VDDQ_EN → PWR_VDDQ_EN

S3
5 PWR_VTT_EN → PWR_VTT_EN

PH on EE Side
40 PWR_VDDQ_PG → PWR_VDDQ_PG

PH on EE Side
40 PWR_2D5V_PG → PWR_2D5V_PG

17 PWR_2D5V_EN → PWR_2D5V_EN

OFFPAGE_GAP

19V_DCBATOUT → PWR_DCBATOUT_VDDQ
PG5117 GAP-CLOSE-PWR-3-GP
PG5118 GAP-CLOSE-PWR-3-GP

1D2V_S3 → PWR_1D2V
PG5119 PG5120 PG5121 PG5122 PG5123 PG5124 GAP-CLOSE-PWR-3-GP

1D2V_S3 → PWR_VDDQ_VLDOIN
PG5115 PG5116 GAP-CLOSE-PWR-3-GP

0D6V_VREF_S0 → PWR_VDDQ_VTT
PG5113 PG5114 GAP-CLOSE-PWR-3-GP

3D3V_S5 → PWR_2D5V_VIN
PG5125 PG5126 GAP-CLOSE-PWR-3-GP

2D5V_S5 → PWR_2D5V
PG5127 PG5128 PG5129 GAP-CLOSE-PWR-3-GP

VTT

Table 1. VID and Reference Voltage Setting

VID	Reference Voltage (V)
High	0.675
Low	0.75

PWR_VDDQ_VID → PR5107 5D1R2F-GP → 5V_S5
PC5102 SC1U10V2KX-L1-GP
PWR_VDDQ_VDD → PR5109 0R0402-PAD-1-GP → 5V_S5
PC5107 SC1U10V2KX-L1-GP

OCP setting
PWR_VDDQ_CS → PR5114 681KR2F-GP

3D3V_S5 → DY PR5111 10KR2F-L1-GP

PWR_DCBATOUT_VDDQ → PR5113 750KR2F-L-GP
Freq. setting
750K -> 350K Hz

PU5101 RT8231CGQW-GP-U
074.08231.0A73

Pin	Name
10	PGOOD
9	TON
8	S5
7	S3
19	VLDOIN
1	VTTGND
20	VTT
2	VTTSNS
21	GND
3	GND
13	CS
11	VID
12	VDD
18	BOOT
17	UGATE
16	PHASE
15	LGATE
14	PGND
5	VDDQ
6	FB
4	VTTREF

PWR_VDDQ_PG
PWR_VDDQ_TON
PWR_VDDQ_EN
PWR_VTT_EN
PWR_VDDQ_VLDOIN
PWR_VDDQ_VTT
PWR_VDDQ_EN → DY PC5106 SCD1U16V2KX-L-GP
PC5109 SC10U6D3V3MX-L-GP
PWR_VDDQ_BOOT → PR5112 2D2R3F-L-GP → PWR_VDDQ_BOOT_A → PC5108 SCD1U50V3KX-L-GP
PWR_VDDQ_HG
PWR_VDDQ_PH
PWR_VDDQ_LG
PWR_VDDQ_VDDQ
PWR_VDDQ_FB
PWR_VDDQ_VTTREF → PC5116 SCD047U25V2KX-GP

VDDQ_HS PU5102 AON7408-GP
VDDQ_LS PU5103 AON7408-GP

PWR_DCBATOUT_VDDQ → PC5103 SC470U25VSKX-L2-GP, PC5104 SC470U25VSKX-L2-GP

Cyntec. 6.6mmx7.3mmx3.0 mm
DCR: 9~10mOhm
Idc : 11A , Isat : 22A
PL5101 COIL-1UH-34-GP-U1
Icc(max)=6A

PWR_1D2V → PC5113 PC5110 PC5111 PC5112 PC5114 PC5119 SC22U6D3V3MX-L1-GP

Close to output cap pin1, not inside of the output cap
PC5101 GAP-CLOSE-PWR-3-GP → PWR_1D2V

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

R1 PR5116 15K8R2F-GP
DY PC5115 SC18P50V2JN-1-GP
R2 PR5117 20KR2F-L3-GP

Vout Setting
Vout = Vref * (1 + R1/R2)
= 0.675 * (1 + 15.8K / 20K)
= 1.2V

VID vs Vref Table
VID Logic-High => Vref = 0.675 V
VID Logic-Low => Vref = 0.75 V
note. Vref can only be changed form 0.675v to 0.75v after power-on

Vout = 0.6V
Iomax = 1.2A

PWR_VDDQ_VTT
DY PC5117 SC10U6D3V3MX-L-GP
DY PC5118 SC10U6D3V3MX-L-GP

TDC=2A
Imax= 3A

PWR_2D5V_VIN
PU5104 RT5797ALGQW-GP
074.05797.0073
PGND NC#5 LX EN SGND VIN PG FB
PWR_2D5V_PH
PWR_2D5V_EN
PWR_2D5V_FB
PWR_2D5V_PG

TOKO. 2.5mmx2.0mmX1.2mm
DCR: 59m Ohm
Idc : 3 A , Isat : 3A
PL5102 IND-1UH-382-GP

PC5121 SC22U6D3V3MX-L1-GP
3D3V_S5 → DY PR5103 100KR2F-L1-GP
PR5104 150KR2F-L-GP
PR5105 47KR2F-GP
DY PC5122 SC22P25V2NX-L-GP
PWR_2D5V → PC5123 PC5124 SC22U6D3V3MX-L1-GP

PWR_2D5V_EN → DY PC5120 SC1U10V2KX-L1-GP

Vout Setting
Vout = Vref * (1 + R1/R2)
= 0.6 * (1 + 150K / 47K)
= 2.515V

LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (RT8231_VDDQ/VTT/VPP)
Size: A2 | Document Number: Kylo-2 | Rev: 1M
Date: Wednesday, October 17, 2018 | Sheet 51 of 99

KL2_SIT_MB_W021
KL2_SIT_MB_W024
KL2_SVT_MB_W007

OFFPAGE

PH on EE Side

40 PWR_1D0V_PG → PWR_1D0V_PG

40,53 PWR_1D8V_PG → PWR_1D8V_PG

OFFPAGE_GAP

19V_DCBATOUT → PWR_DCBATOUT_1D0V

PG5202 GAP-CLOSE-PWR-3-GP
PG5203 GAP-CLOSE-PWR-3-GP
PG5204 GAP-CLOSE-PWR-3-GP
PG5205 GAP-CLOSE-PWR-3-GP

1D05V_S5 → PWR_1D0V

PG5206 GAP-CLOSE-PWR-3-GP
PG5207 GAP-CLOSE-PWR-3-GP
PG5208 GAP-CLOSE-PWR-3-GP
PG5209 GAP-CLOSE-PWR-3-GP
PG5210 GAP-CLOSE-PWR-3-GP
PG5211 GAP-CLOSE-PWR-3-GP
PG5214 GAP-CLOSE-PWR-3-GP
PG5215 GAP-CLOSE-PWR-3-GP
PG5212 GAP-CLOSE-PWR-3-GP
PG5213 GAP-CLOSE-PWR-3-GP

PR5203 5D1R2F-GP 5V_S5
PWR_1D0V_VID
PC5206 SC1U10V2KX-L1-GP

PR5206 0R0402-PAD-1-GP 5V_S5
PWR_1D0V_VDD
PC5208 SC1U10V2KX-L1-GP

PWR_1D0V_CS
OCP setting
COP:12A
PR5204 316KR2F-GP

3D3V_S5
DY PR5202 10KR2J-3-GP

PWR_DCBATOUT_1D0V

PR5210 470KR2F-GP
PWR_1D0V_PG
PWR_1D0V_TON
PWR_1D8V_PG
PWR_1D0V_S3
PWR_1D0V_VLDOIN

DY UFTP5201
PC5207 SC1P50V2KX-1-GP

PR5207 0R0402-PAD-1-GP
PWR_1D0V_S3

PU5201 RT8231CGQW-GP-U 074.08231.0A73

Pin	Name
10	PGOOD
9	TON
8	S5
7	S3
19	VLDOIN
1	VTTGND
20	VTT
2	VTTSNS
21	GND
3	GND
13	CS
11	VID
12	VDD
18	BOOT
17	UGATE
16	PHASE
15	LGATE
14	PGND
5	VDDQ
6	FB
4	VTREF

PWR_1D0V_BOOT
PWR_1D0V_HG
PWR_1D0V_PH
PWR_1D0V_LG
PWR_1D0V_FB_A
PWR_1D0V_FB
PWR_1D0V_VTREF

PR5201 2D2R3-1-U-GP
PWR_1D0V_BOOT_A
PC5205 SCD1U50V3KX-L-GP

PU5202 AON7408-GP 1D05V_HS
PU5203 AON7506-GP 1D05V_LS

PC5202 SCD47U25V3KX-L2-GP
PC5203 SCD47U25V3KX-L2-GP

PL5201 COIL-1UH-57-GP 68.1R010.20G
Cyntec. 6.5 x 6.9 x 3.0 mm
DCR: 18 mOhm
Idc : 8A, Isat : 14A
Icc(max)=6.5A

PG5201 GAP-CLOSE-PWR-3-GP

PR5208 2K2R2F-GP
DY PC5209 SC1P50V2KX-1-GP
PR5209 41K2R2F-GP

PWR_1D0V
PC5210 PC5211 PC5212 PC5213 PC5214 PC5215 SC22U6D3V3MX-1-GP

DY PC5217 DY PC5218 DY PC5219 SC22U6D3V3MX-1-GP

LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (RT8231_1D05V)

Size	Document Number	Rev
A2	Kylo-2	1M

Date: Wednesday, October 17, 2018 Sheet 52 of 99

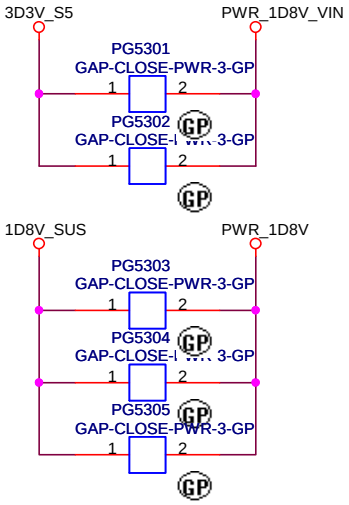
OFFPAGE

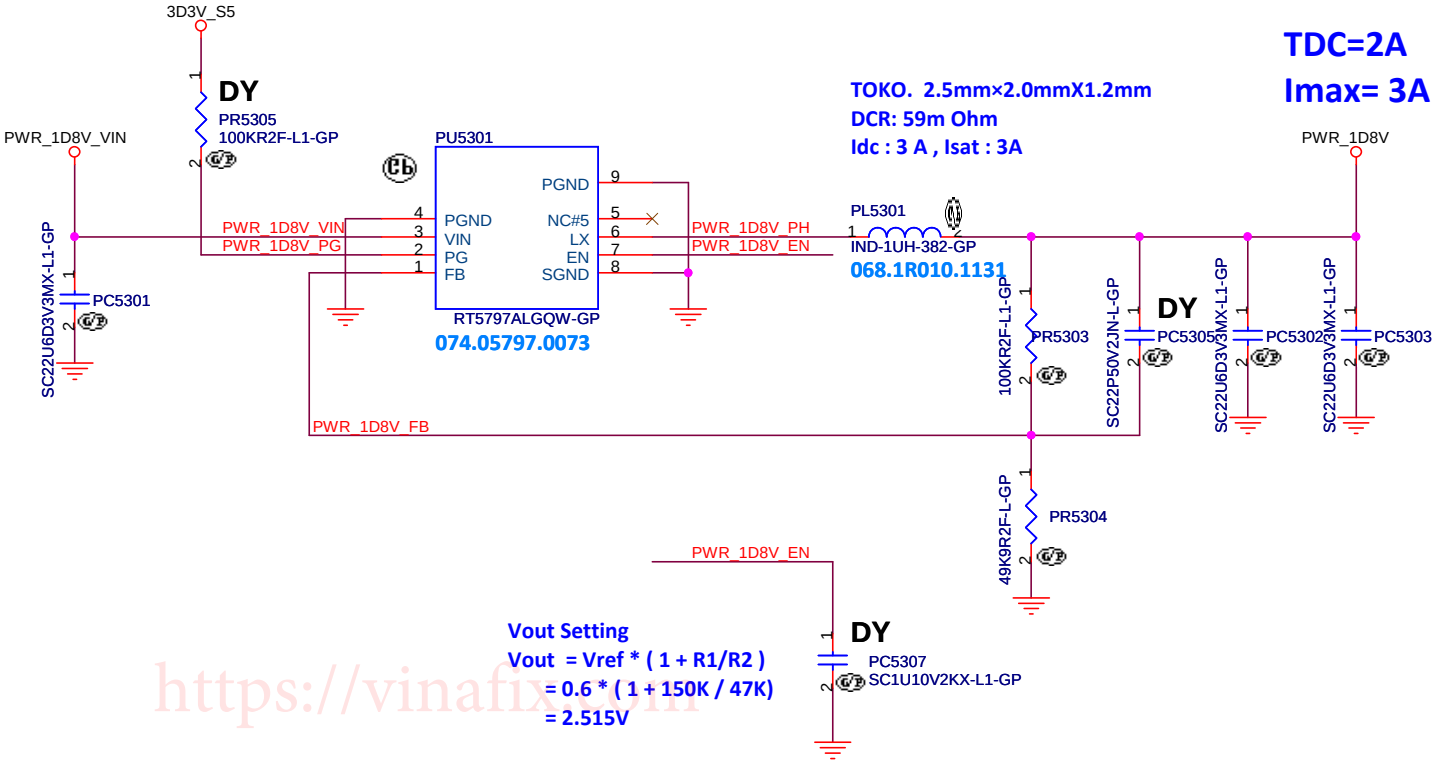
PH on EE Side

40,52 PWR_1D8V_PG

17 PWR_1D8V_EN

OFFPAGE-GAP





LKL-2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: POWER (RT5797_1D8V)		
Size: A4	Document Number: Kylo-2	Rev: 1M
Date: Wednesday, October 17, 2018	Sheet 53 of 99	

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LKL-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **POWER (RSVD)**

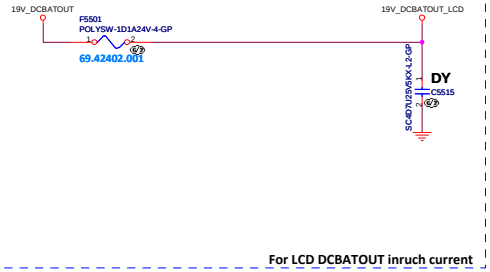
Size	Document Number	Rev
A4	Kylo-2	1M

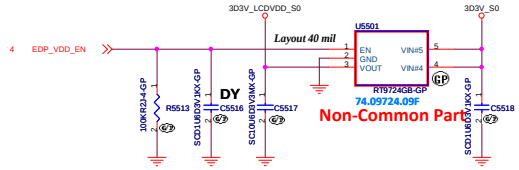
Date: Wednesday, October 17, 2018 Sheet 54 of 99

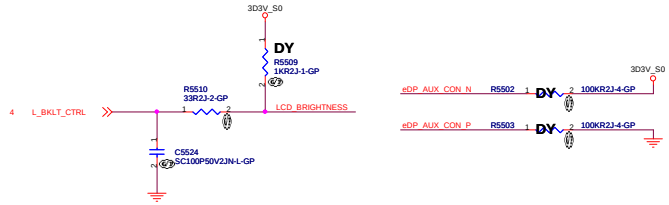
Main Func = LCD

KL2_SIT_MB_W006
KL2_SIT_MB_W032
KL2_SIT_MB_W033
KL2_SVT_MB_W009

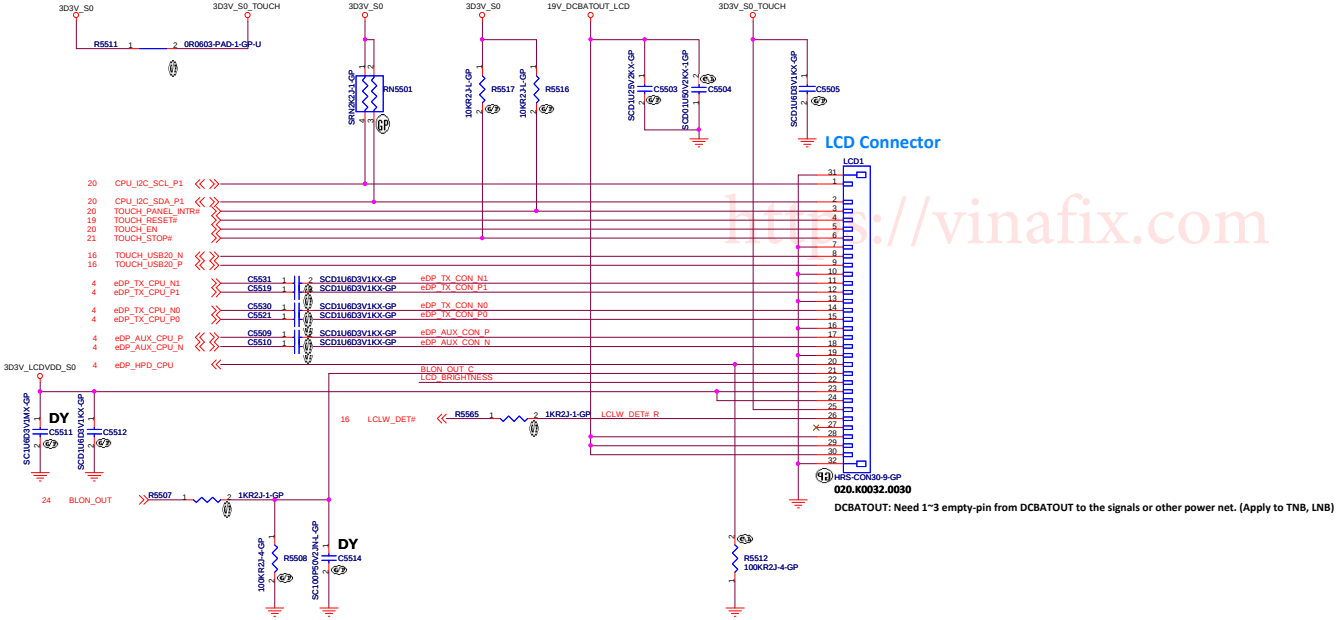
LCD Backlight Power







LCD Connector



DCBATOUT: Need 1~3 empty-pin from DCBATOUT to the signals or other power net. (Apply to TNB, LNB)

LKL-2

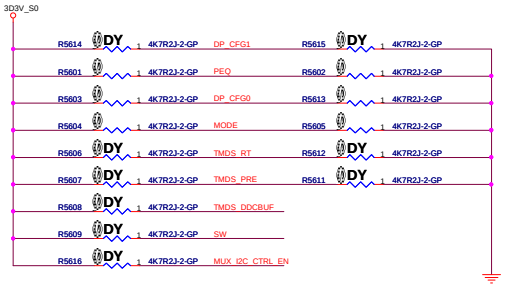
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

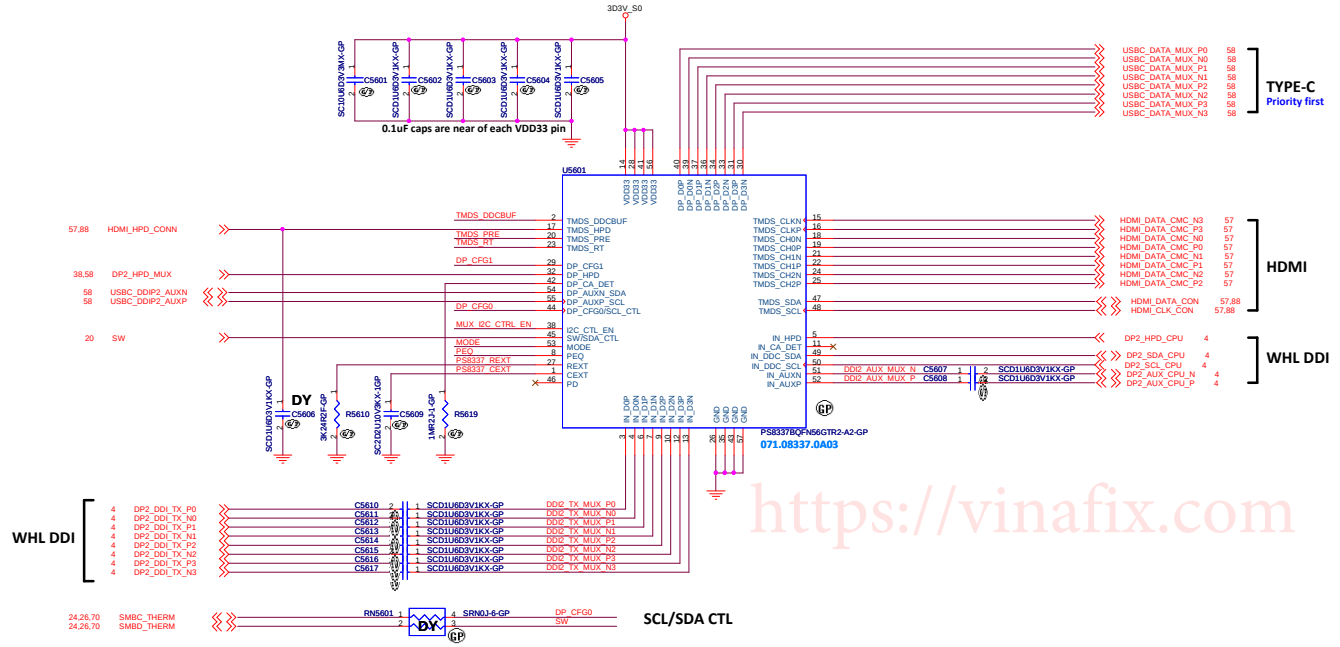
Title: DISPLAY (LCD/CAM/TOUCH)

Size: A2 | Document Number: Kylo-2 | Rev: 1M

Date: Wednesday, October 17, 2018 | Sheet 55 of 99

H: 4.7K-ohm
M: 150K-ohm
L: DY





TMDS_PRE1 = L: no pre-emphasis
= H: 1.5dB pre-emphasis
= M: 3.0dB pre-emphasis
The pin Internal pull down at ~150K, 3.3V I/O.

TMDS_RT1 = L: Standard open drain driver
= H: Open drain driver with termination resistors
The pin Internal pull down at ~150K, 3.3V I/O.

TMDS_DDCBUF1 = L: DDC pass through
= H: DDC active buffer
= M: DDC pass through with 40 kohm pull up resistor
The pin Internal pull down at ~150K, 3.3V I/O.

PEQ1 = L: default, LEQ, compensate channel loss up to 12dB @ HBR2
= H: HEQ, compensate channel loss up to 15dB @ HBR2
= M: LLEQ, compensate channel loss up to 5dB @ HBR2
The pin Internal pull down at ~150K, 3.3V I/O.

DP1_CFG1 = L: default, auto test disable & input offset cancellation enable
= H: auto test enable & input offset cancellation enable
= M: auto test disable & input offset cancellation disable
The pin Internal pull down at ~150K, 3.3V I/O.

DP1_CFG0 = L: default, automatic EQ enable & AUX interception enable
= H: automatic EQ disable & AUX interception enable
= M: automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing
The pin Internal pull down at ~150K, 3.3V I/O.

MODE1 = L: Control Switching Mode, HDMI ID disable
= H: Automatic Switching Mode, HDMI ID disable
= M: Automatic Switching Mode, HDMI ID enable
The pin Internal pull down at ~150K, 3.3V I/O.

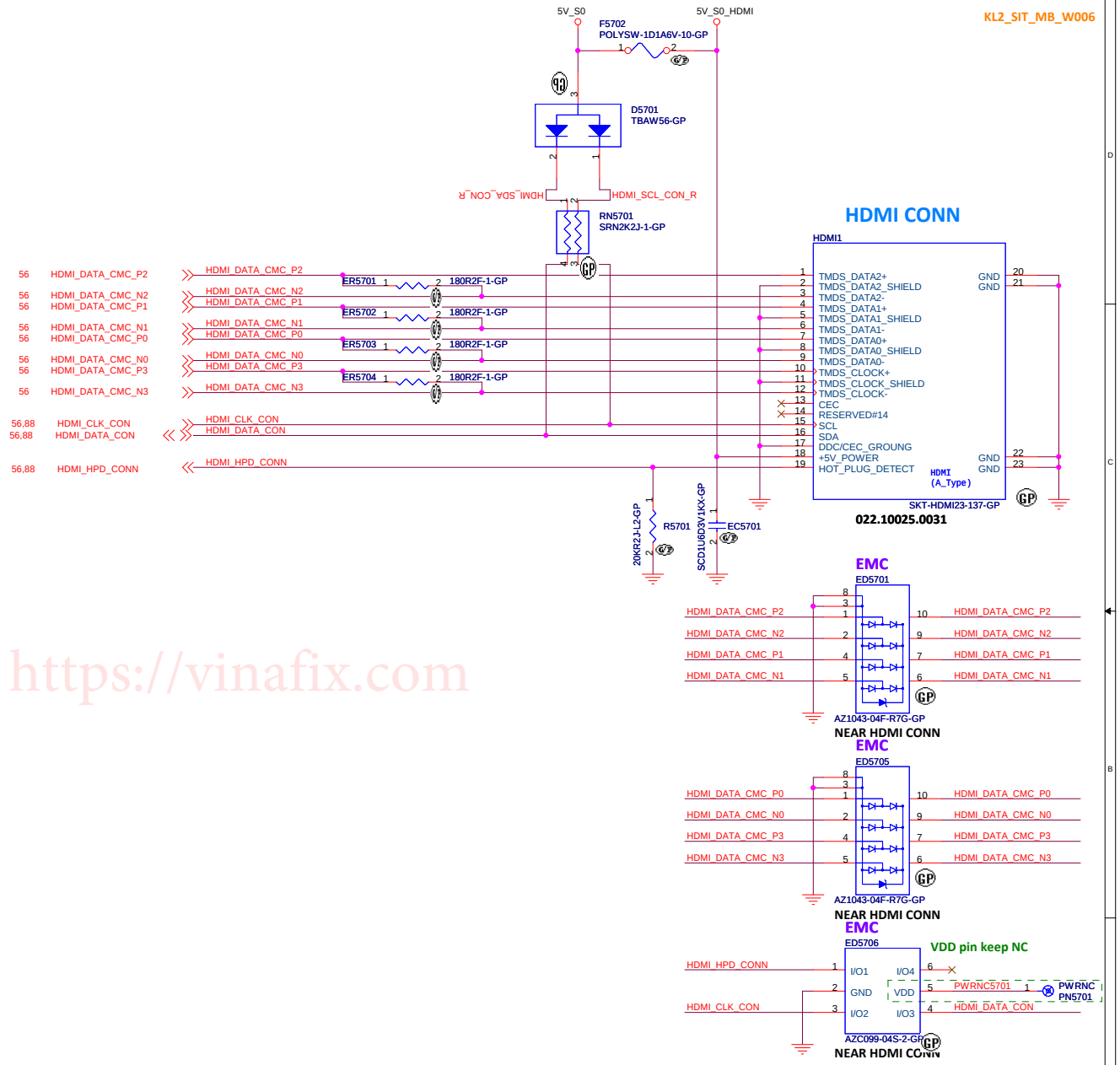
For Control Switching:
SW 1= L: DP output is selected
SW 1= H: TMDS output is selected

For Automatic Switching:
SW 1 = L: DP output has higher priority .
The pin Internal pull down at ~150K, 3.3V I/O.
SW 1 = H:TMDS output has higher priority.

LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISPLAY (DDI DEMUX PS8337B)
Size: A2 | Document Number: Kylo-2 | Rev: 1M
Date: Wednesday, October 17, 2018 | Sheet 58 of 99



LKL-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DISPLAY (HDMI CONN)	
Size A3	Document Number Kylo-2	Rev 1M
Date: Wednesday, October 17, 2018	Sheet 57 of 99	

KL2_SIT_MB_W006
KL2_SVT_MB_W009

3D3V_SUS — R5801 0R0603-PAD-1-GP-U — 3D3V_PS8747B_2

3D3V_PS8747B_2

R5834 4K7R2J-2-GP PS8747_CEQ_SDA2
R5806 DY 4K7R2J-2-GP PS8747_I2C_CTL2 R5807 4K7R2J-2-GP
R5808 DY 4K7R2J-2-GP PS8747_DCICFG_ADDR2 R5809 DY 4K7R2J-2-GP

PS8747_I2C_CTL2 =		
L: Pin Control is selected	R5806: DY, R5807: ASM	<-- LOGIC
H: I2C Control is selected	R5806: ASM, R5807: DY	

PS8747_DCICFG_ADDR2 =		
(Pin Control mode only) =		
L: DCI mode disabled	R5808: DY, R5809: ASM	
H: DCI mode enabled	R5808: ASM, R5809: DY	
M: Automatic DCI mode entering enabled	R5808: DY, R5809: DY	<-- LOGIC
(I2C Control mode only) =		
L: 0x20/0x21	R5808: DY, R5809: ASM	
H: 0x22/0x23 (Default)	R5808: ASM, R5809: DY	

3D3V_PS8747B_2

C5801 DY SCD1U6D3V1KX-GP
C5807 DY SCD1U6D3V1KX-GP
C5808 SCD1U6D3V1KX-GP
C5802 SCD1U6D3V1KX-GP
C5803 DY SCD01U50V2KX-1GP
C5804 DY SCD01U50V2KX-1GP
C5805 SCD01U50V2KX-1GP
C5806 SCD01U50V2KX-1GP

C5809 SC2D2U10V3KX-1GP

U5801

Pin	Signal	Pin	Signal
41	EPAD	6	VDD33
28	VDD33	20	VDD33
1	CEXT	17	VDD_DCI
9	ML0P	10	ML0N
18	ML3P	19	ML3N
11	SSDE/DCI_DATA	14	CDE/DCI_CLK
5	SSRXP	4	SSRXN
8	SSTXP	7	SSTXN
15	ML2P	16	ML2N
12	ML1P	13	ML1N
24	AUXP	25	AUXN
30	RX1P	31	RX1N
40	RX2P	39	RX2N
33	TX1P	34	TX1N
37	TX2P	36	TX2N
23	CE_DP	35	CE_USB
38	FLIP	27	SBU1
26	SBU2	32	IN_HPD
29	I2C_EN	3	DCICFG
21	DPEQ	22	CEQ
2	REXT		

1 Port USB + 2 Lanes DP

PS8747BQFN40GTR-B1-GP
071.08747.0003
Lenovo P/N:PS8747B

56	USBC_DATA_MUX_P0	C5810	SCD1U6D3V1KX-GP	USBC_DDIP2_0P_C — R5817 5D1R2J-1-GP — USBC_DDIP2_0P_C_R
56	USBC_DATA_MUX_N0	C5813	SCD1U6D3V1KX-GP	USBC_DDIP2_0N_C — R5818 5D1R2J-1-GP — USBC_DDIP2_0N_C_R
56	USBC_DATA_MUX_P3	C5811	SCD1U6D3V1KX-GP	USBC_DDIP2_3P_C — R5819 5D1R2J-1-GP — USBC_DDIP2_3P_C_R
56	USBC_DATA_MUX_N3	C5812	SCD1U6D3V1KX-GP	USBC_DDIP2_3N_C — R5820 5D1R2J-1-GP — USBC_DDIP2_3N_C_R
16	USB2_USB30_RX_P	C5814	SCD1U6D3V1KX-GP	USB30_RX_CPU_P2_C
16	USB2_USB30_RX_N	C5815	SCD1U6D3V1KX-GP	USB30_RX_CPU_N2_C
16	USB2_USB30_TX_P	C5816	SCD1U6D3V1KX-GP	USB30_TX_CPU_P2_C
16	USB2_USB30_TX_N	C5817	SCD1U6D3V1KX-GP	USB30_TX_CPU_N2_C
56	USBC_DATA_MUX_P2	C5818	SCD1U6D3V1KX-GP	USBC_DDIP2_2P_C — R5821 5D1R2J-1-GP — USBC_DDIP2_2P_C_R
56	USBC_DATA_MUX_N2	C5819	SCD1U6D3V1KX-GP	USBC_DDIP2_2N_C — R5822 5D1R2J-1-GP — USBC_DDIP2_2N_C_R
56	USBC_DATA_MUX_P1	C5820	SCD1U6D3V1KX-GP	USBC_DDIP2_1P_C — R5823 5D1R2J-1-GP — USBC_DDIP2_1P_C_R
56	USBC_DATA_MUX_N1	C5821	SCD1U6D3V1KX-GP	USBC_DDIP2_1N_C — R5824 5D1R2J-1-GP — USBC_DDIP2_1N_C_R
56	USBC_DDIP2_AUXP	R5810	0R0402-PAD-1-GP	USBC_DDIP2_AUXP_R
56	USBC_DDIP2_AUXN	R5812	0R0402-PAD-1-GP	USBC_DDIP2_AUXN_R

USBC2_RX1P	39	USBC2_RX1P	39
USBC2_RX1N	39	USBC2_RX1N	39
USBC2_RX2P	39	USBC2_RX2P	39
USBC2_RX2N	39	USBC2_RX2N	39
USBC2_TX1P	39	USBC2_TX1P	39
USBC2_TX1N	39	USBC2_TX1N	39
USBC2_TX2P	39	USBC2_TX2P	39
USBC2_TX2N	39	USBC2_TX2N	39

3D3V_PS8747B_2

USBC2_DP_MODE_R	R5829	DY	10KR2J-3-GP
USBC2_USB_MODE_R	R5830	DY	10KR2J-3-GP
USBC2_POL_R	R5831	DY	10KR2J-3-GP
USBC2_DP_MODE_R	R5825		0R0402-PAD-1-GP
USBC2_USB_MODE_R	R5826		0R0402-PAD-1-GP
USBC2_POL_R	R5827		0R0402-PAD-1-GP

USBC2_DP_MODE	38	USBC2_DP_MODE	38
USBC2_USB_MODE	38	USBC2_USB_MODE	38
USBC2_POL	38	USBC2_POL	38
USBC2_SBU1	39	USBC2_SBU1	39
USBC2_SBU2	39	USBC2_SBU2	39
DP2_HPD_MUX	38,56		

3D3V_PS8747B_2

RN5801 SRN100KJ-6-GP
USBC_DDIP2_AUXN_R
USBC_DDIP2_AUXP_R

24,37,38	I2C_CLK_PD	R5815	DY	0R2J-2-GP — PS8747_I2C_CTL2
24,37,38	I2C_DATA_PD	R5816	DY	0R2J-2-GP — PS8747_DCICFG_ADDR2 / PS8747_DPEQ_SCL2 / PS8747_CEQ_SDA2

R5814 4K99R2F-L-GP
R5832 2MR2-GP
R5833 2MR2-GP

LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (DP MUX PS8747B)
Size: A3 | Document Number: Kylo-2 | Rev: 1M
Date: Wednesday, October 17, 2018 | Sheet 58 of 99

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LKL-2

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DISPLAY (RSVD)***

Size	Document Number	Rev
A4	Kylo-2	1M

Date: Wednesday, October 17, 2018 Sheet 59 of 99

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LKL-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *INT IO (RSVD)*

Size	Document Number	Rev
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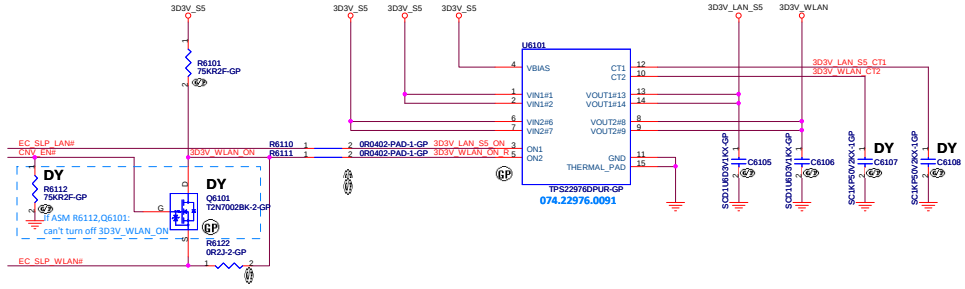
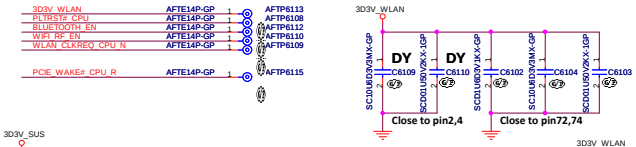
Main Func = WLAN

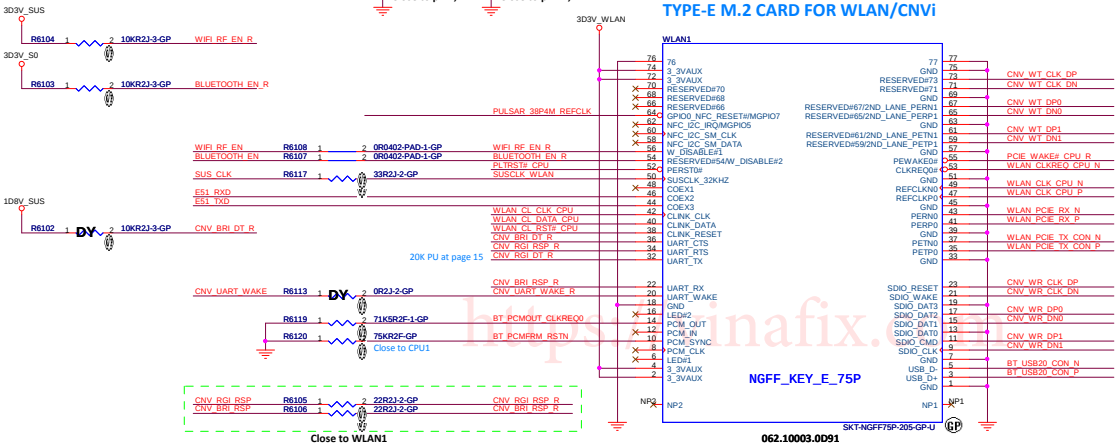
KL2_SIT_MB_W006
KL2_SIT_MB_W016
KL2_SIT_MB_W020
KL2_SIT_MB_W034
KL2_SVT_MB_W009
KL2_SVT_MB_W015

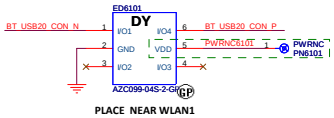
3D3V_LAN_S5 3D3V_WLAN





TYPE-E M.2 CARD FOR WLAN/CNVi





Vinafix.com

LKL-2

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (WLAN M.2/CNVi)

Size: A2 | Document Number: Kylo-2 | Rev: 1M

Date: Thursday, November 08, 2018 | Sheet 61 of 99

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LKL-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***INT IO (RSVD)***

Size	Document Number	Rev
A4	Kylo-2	1M

Date: Wednesday, October 17, 2018 Sheet 62 of 99

TYPE-M M.2 CARD FOR SSD

3D3V_S0

SC10U6D3V3MX-GP C6301 DY

0R0805-PAD-1-GP-U R6301 DY

SSD1

NGFF_KEY_M 75P

		GND	1		
16	SSD_PCIE_RX_N3	GND	3	3_3VAUX	2
16	SSD_PCIE_RX_P3	PETP3 PETN3	5	3_3VAUX	4
		PETN3 PETP3	7	NC#6	6
16	SSD_PCIE_TX_CON_N3	GND	9	NC#8	8
16	SSD_PCIE_TX_CON_P3	PERN3	11	DAS/DSS#	10
		PERP3	13	3_3VAUX	12
16	SSD_PCIE_RX_N2	GND	15	3_3VAUX	14
16	SSD_PCIE_RX_P2	PETP2 PETN2	17	3_3VAUX	16
24	SSD_DTCT#	PETN2 PETP2	19	3_3VAUX	18
16	SSD_PCIE_TX_CON_N2	GND	21	NC#20	20
16	SSD_PCIE_TX_CON_P2	PERN2	23	NC#22	22
		PERP2	25	NC#24	24
16	SSD_PCIE_RX_N1	GND	27	NC#26	26
16	SSD_PCIE_RX_P1	PETN1	29	NC#28	28
		PETP1	31	NC#30	30
16	SSD_PCIE_TX_CON_N1	GND	33	NC#32	32
16	SSD_PCIE_TX_CON_P1	PERN1	35	NC#34	34
		PERP1	37	NC#36	36
16	SSD_SATA_RX_P	GND	39	DEVSLP	38
16	SSD_SATA_RX_N	PETN0/SATA_B+	41	NC#40	40
		PETP0/SATA_B-	43	NC#42	42
16	SSD_SATA_TX_CON_N	GND	45	NC#44	44
16	SSD_SATA_TX_CON_P	PERN0/SATA_A-	47	NC#46	46
		PERP0/SATA_A+	49	NC#48	48
18	SSD_CLK_CPU_N	GND	51	PERST#/NC#50	50
18	SSD_CLK_CPU_P	REFCLKN	53	CLKREQ#/NC#52	52
		REFCLKP	55	PEWAKE#/NC#54	54
		GND	57	NC#56	56
		NC#67	67	NC#58	58
16	M2_SSD_PEDET	PEDET(OC_PCIE/GND_SATA)	69	SUSCLK_32KHZ	68
		GND	71	3_3VAUX	70
		GND	73	3_3VAUX	72
		GND	75	3_3VAUX	74
		77	77	76	76
		NP1	NP1	NP2	NP2

SKT-NGFF75P-77-GP

062.10003.0511

PEDET (M2_SSD_PEDET)
SATA Device GND
PCIe Device Open

3D3V_S0_SSD

SSD_DEVSLP 16

R6302 33R2J-2-GP

PLTRST#_SSD

PLTRST#_CPU 17,24,31,33,40,61,68,88,91

SSD_CLKREQ_CPU_N 18

3D3V_S0_SSD

SC10U6D3V3MX-GP C6310

SCD01U50V2KX-1GP C6311 DY

LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (SSD M.2)

Size	Document Number	Rev
A4	Kylo-2	1M

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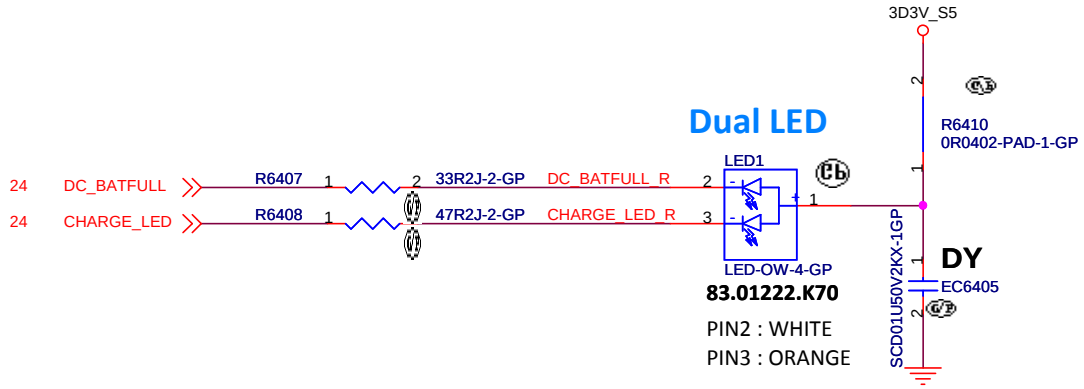
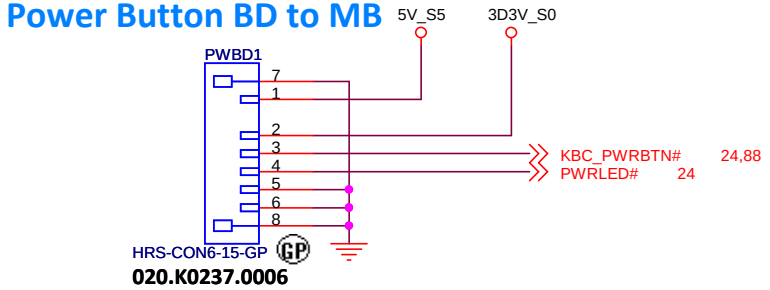




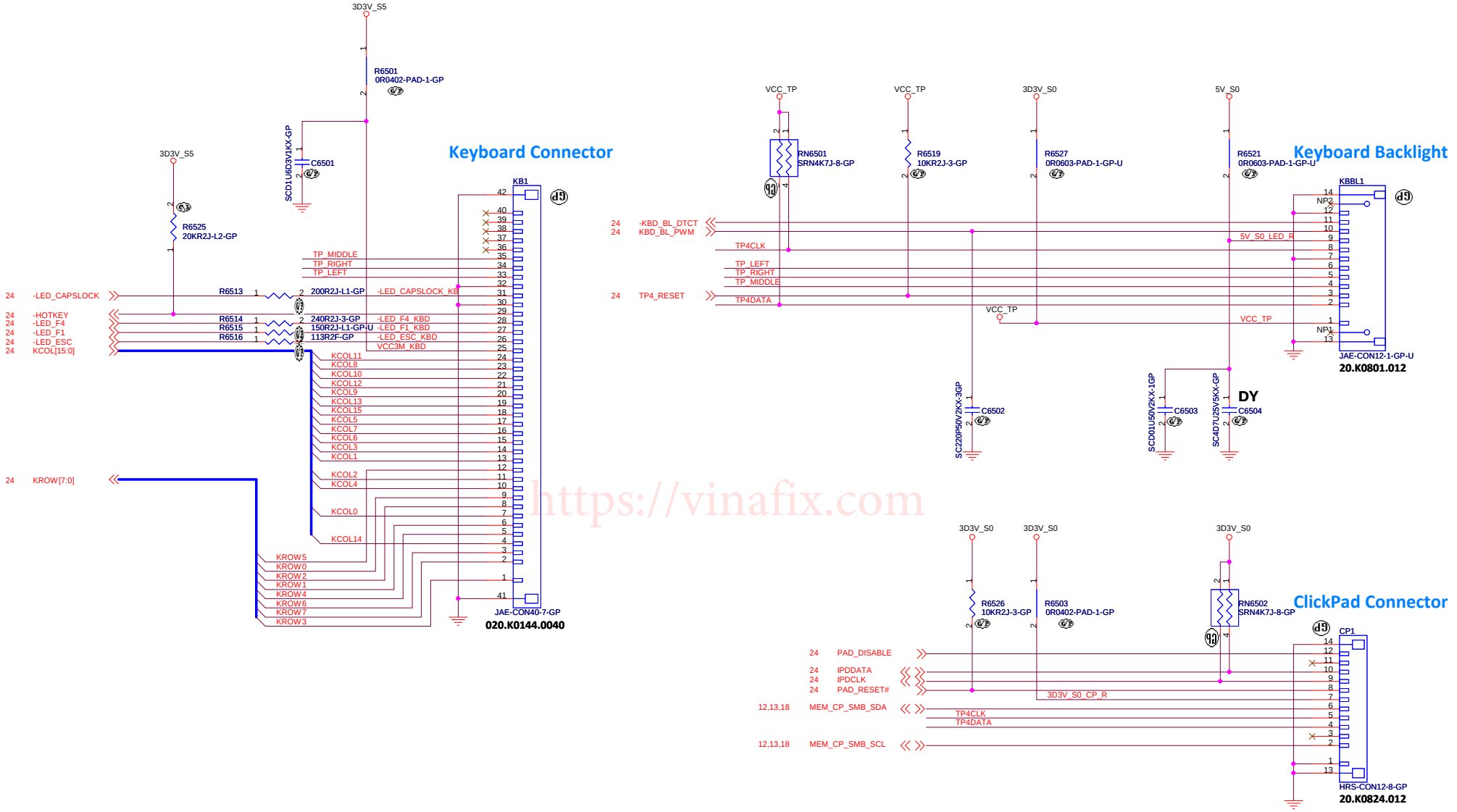
LKL-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LED / BUTTON / POWER BUTTON***

Size	Document Number	Rev
A4	**Kylo-2**	**1M**

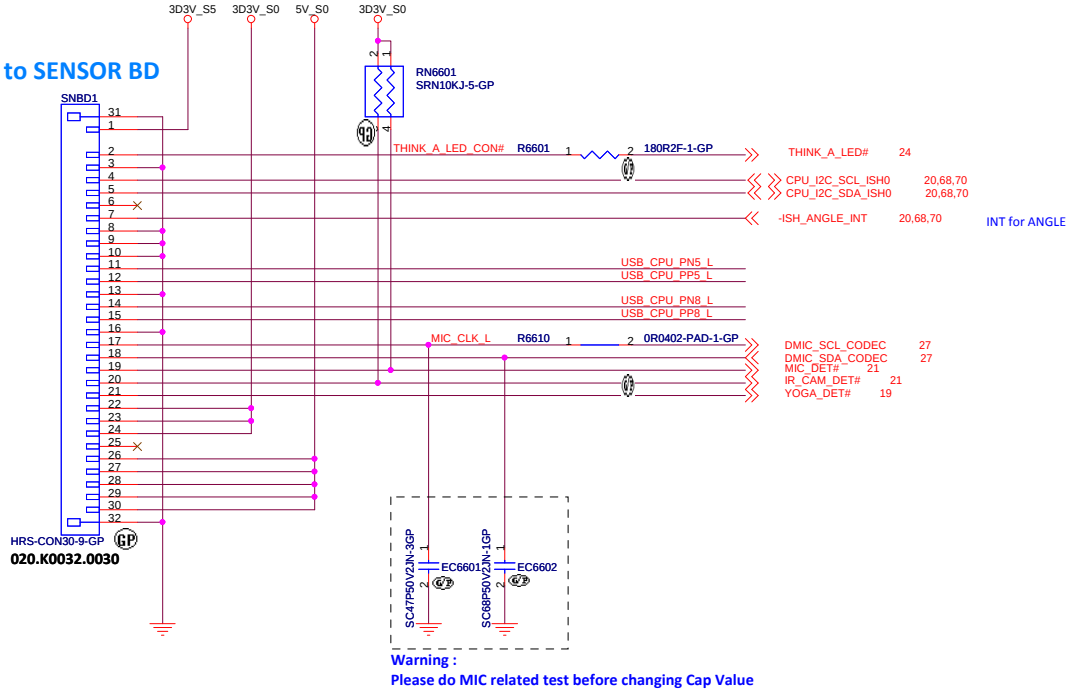
Date: Wednesday, October 17, 2018 Sheet 64 of 99



LKL-2

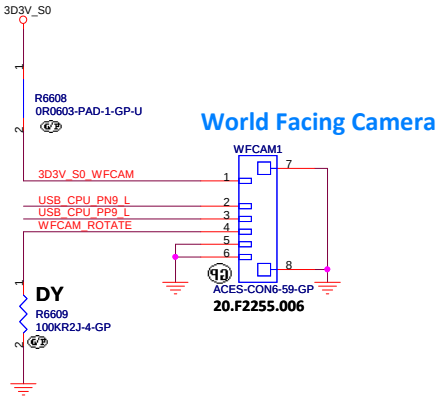
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***INT IO (KB/CP/TP)***
Size A3 / Document Number	**Kylo-2** / Rev **1M**
Date: Wednesday, October 17, 2018	Sheet 65 of 99

MB to SENSOR BD



Warning :
Please do MIC related test before changing Cap Value

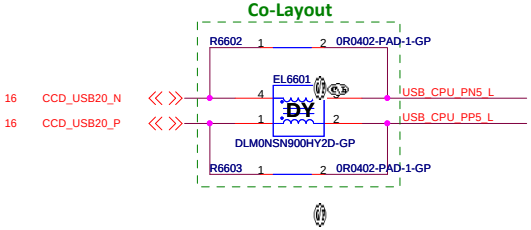
World Facing Camera



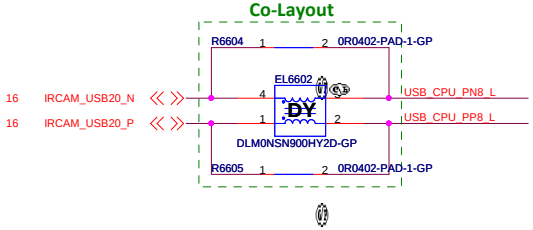
Default camera direction is, LED on the right side of Lens/CMOS.

Pin4 supply = High : Normal image (default, and if this pin not be connected = normal image)
Pin4 supply = Low : Upside down image (means if we can rotate camera module 180 degree = LED on left side, use this mode)

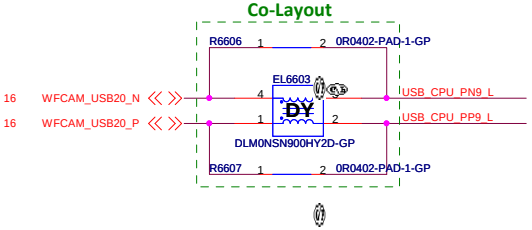
Co-Layout



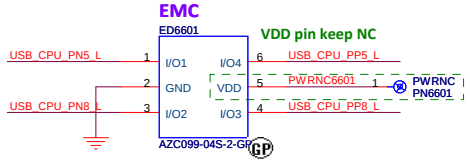
Co-Layout



Co-Layout

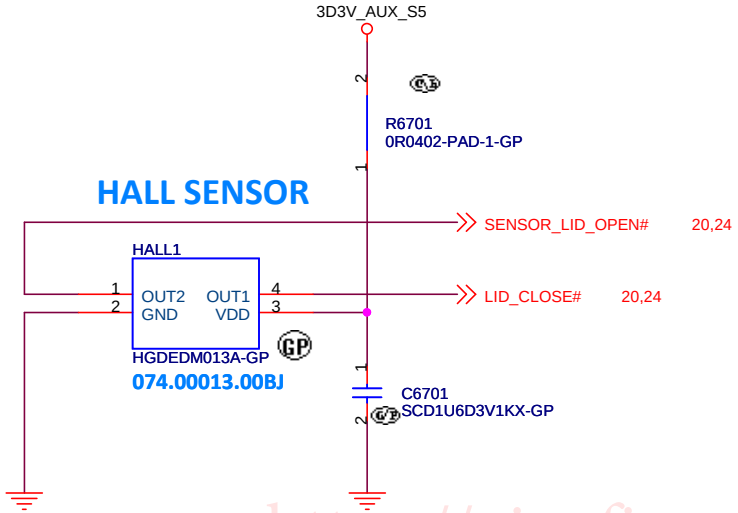


EMC



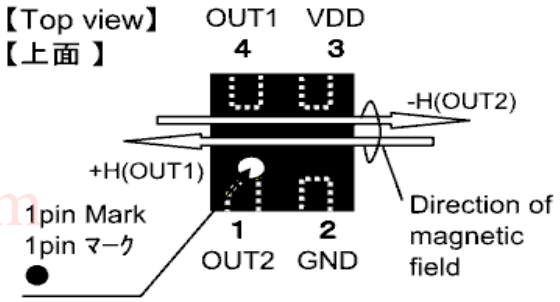
LKL-2

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	IO BOARD CONN (SNBD/WFCAM)	
Size A3	Document Number Kylo-2	Rev 1M
Date: Wednesday, October 17, 2018	Sheet 66 of 99	



Pin1 need place at "Upper Right Corner"

LID_CLOSE# : NB Lid function
SENSOR_LID_OPEN#: Tablet detect function



LKL-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SENSOR (HALL-SENSOR)***

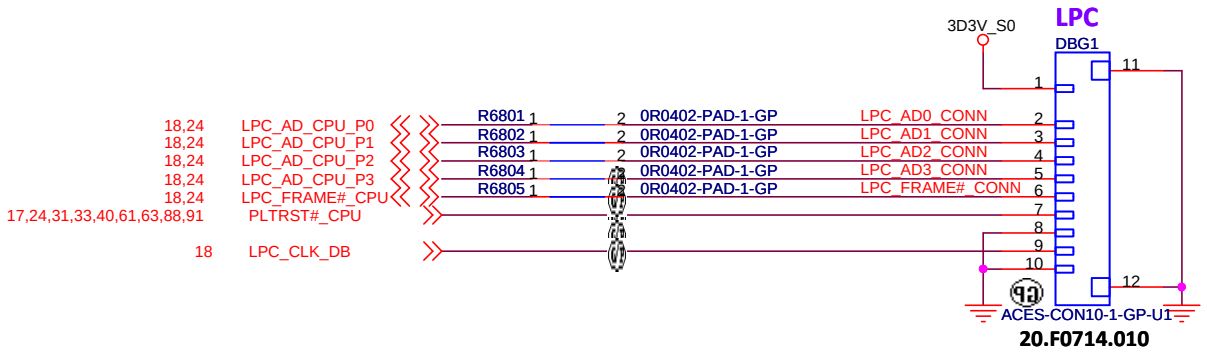
Size	Document Number	Rev
A4	Kylo-2	1M

Date: Wednesday, October 17, 2018 Sheet 67 of 99

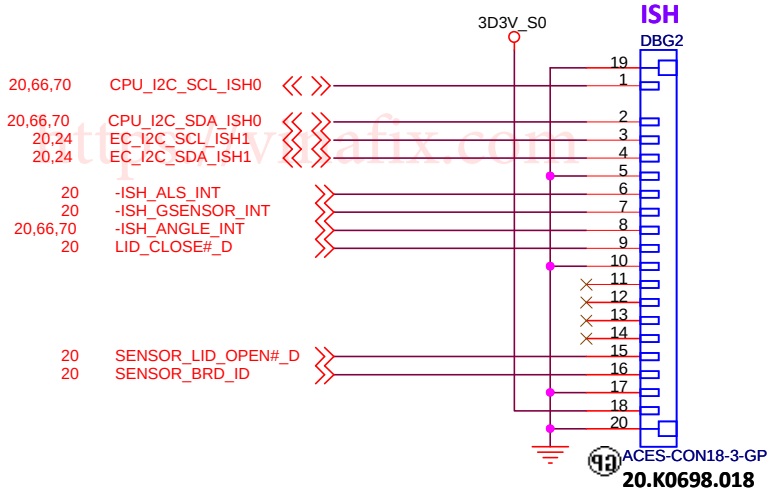
Main Func = Debug

KL2_SVT_MB_W002

LPC Connector



Sensors Debug Hooks



LKL-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***DEBUG (LPC DEBUG)***	
Size A4	Document Number **Kylo-2**	Rev **1M**
Date: Wednesday, October 17, 2018	Sheet 68 of 99	

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LKL-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SENSOR (RSVD)

Size	Document Number	Rev
A4	Kylo-2	1M

Date: Wednesday, October 17, 2018 Sheet 69 of 99

Angle Calculation (ISH_I2C)

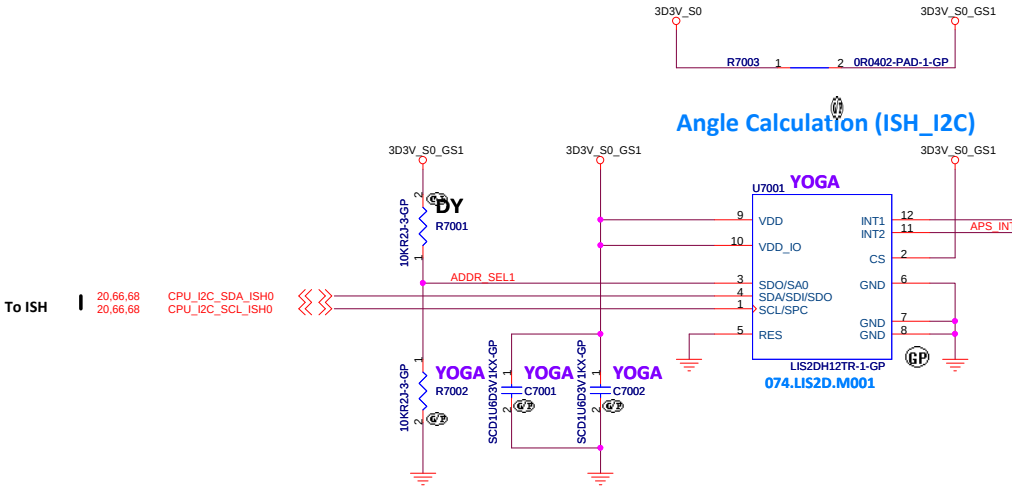

TABLE for Angle Detection (U7001): Tri-axis Digital Accelerometer

P/N	ADDR_SEL1	Address (7bit)	
ST LIS2DH12TR 074.LIS2D.M001	H	19h (7bit)	(SENSOR BD)
	L	18h (7bit)	LOGIC (MB)

TABLE

CS	Mode Selection	
H	I2C Mode	LOGIC
L	SPI Mode	

Thermal Control (I2C)

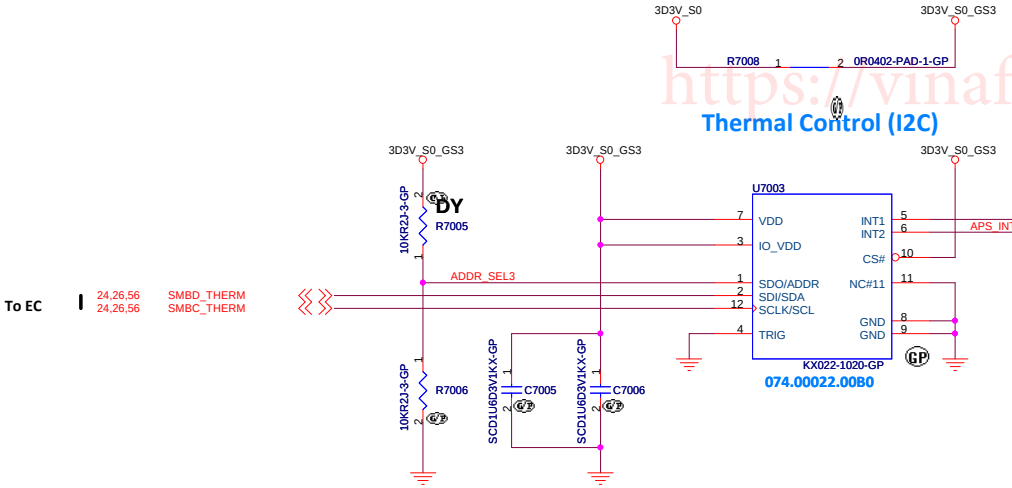

TABLE for ITS Detection (U7003): Tri-axis Digital Accelerometer

P/N	ADDR_SEL3	Address (8bit)	
ROHM KX022-1020 074.00022.00B0	H	3Eh (W) & 3Fh (R)	LOGIC
	L	3Ch (W) & 3Dh (R)	
ST LIS2DWLTR 074.LIS2D.00B0	H	32h (W) & 33h (R)	
	L	30h (W) & 31h (R)	

TABLE

CS#	Mode Selection	
H	I2C Mode	LOGIC
L	SPI Mode	

LKL-2

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Title: SENSOR (G-SENSOR)
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Title: ***EXT IO (RSVD)***

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Title: *EXT IO (RSVD)*

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Title: EXT IO (RSVD)		
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Title: ***EXT IO (RSVD)***

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Title: ***GPU (RSVD)***

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Title: ***GPU (RSVD)***

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Title: ***GPU (RSVD)***

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Title: GPU (RSVD)

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Title: ***GPU (RSVD)***

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Title: GPU (RSVD)

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Title: ***GPU (RSVD)***

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Title: ***GPU (RSVD)***

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Title: GPU (RSVD)

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Title: GPU (RSVD)

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Title: GPU (RSVD)

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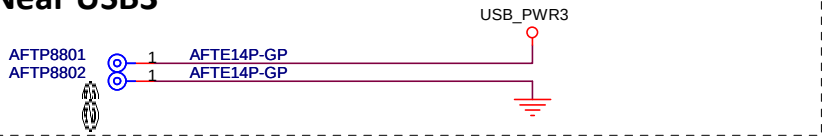
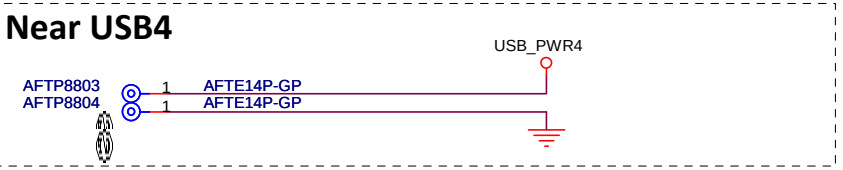
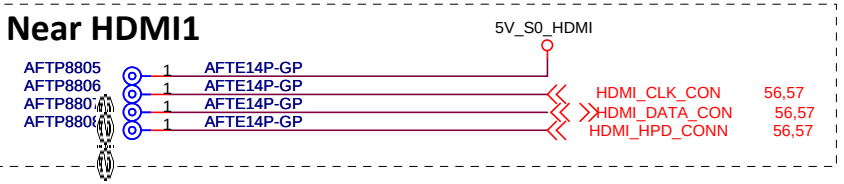
Near USB3



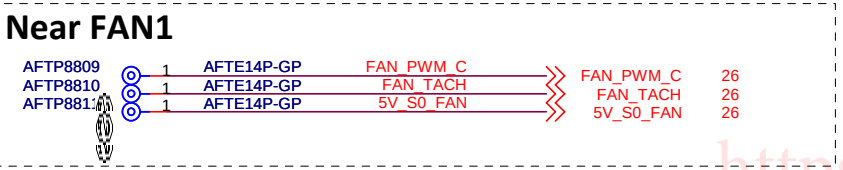
Near USB4



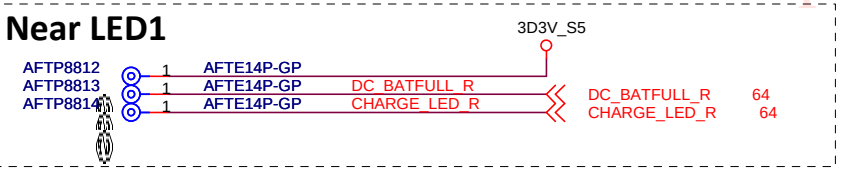
Near HDMI1



Near FAN1



Near LED1



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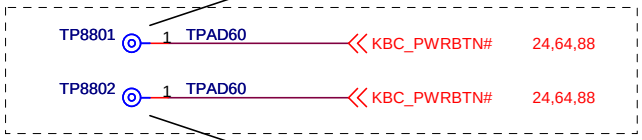

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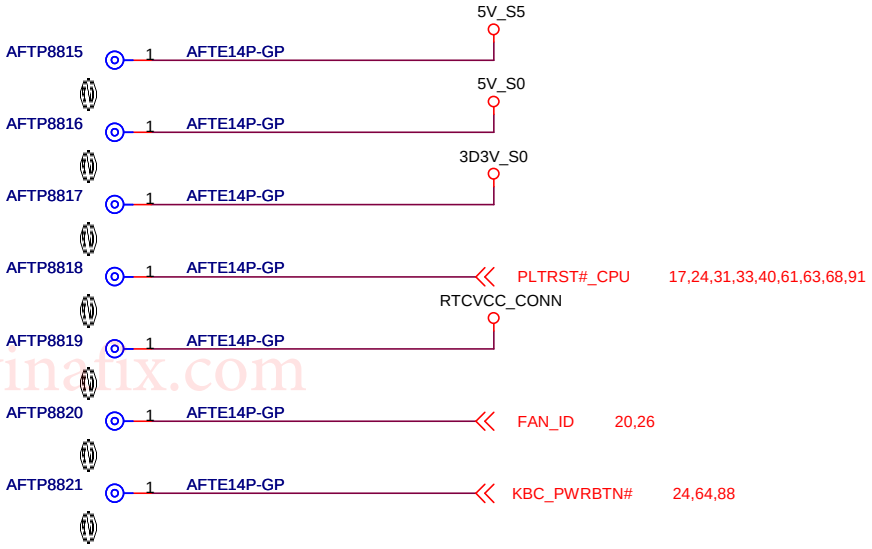

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Title: ***UNUSED PARTS (TEST POINT)***

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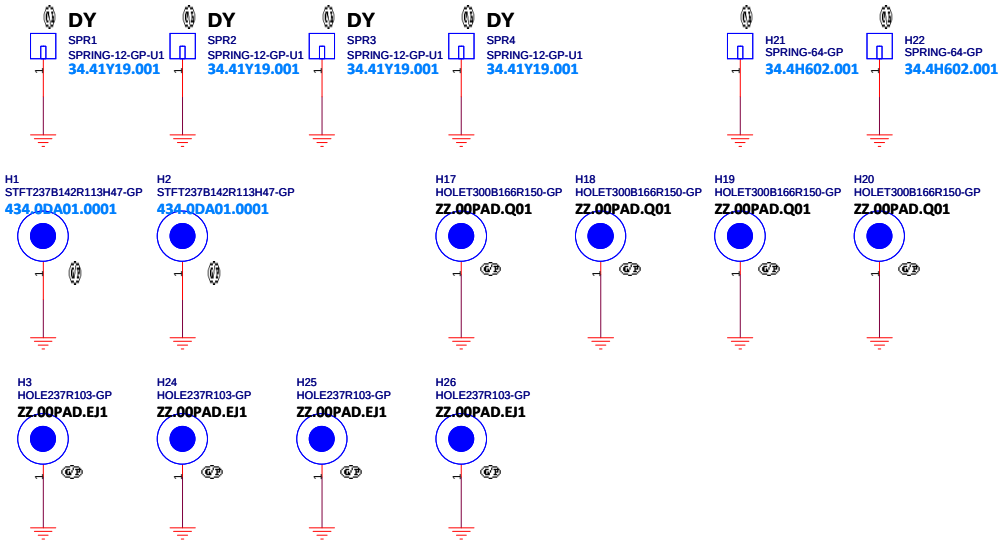
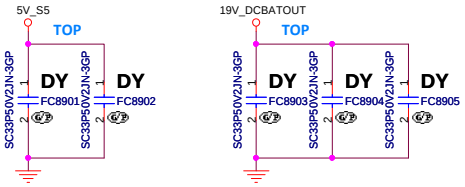
KL2_SIT_MB_W027
KL2_SVT_MB_W007
KL2_SVT_MB_W019

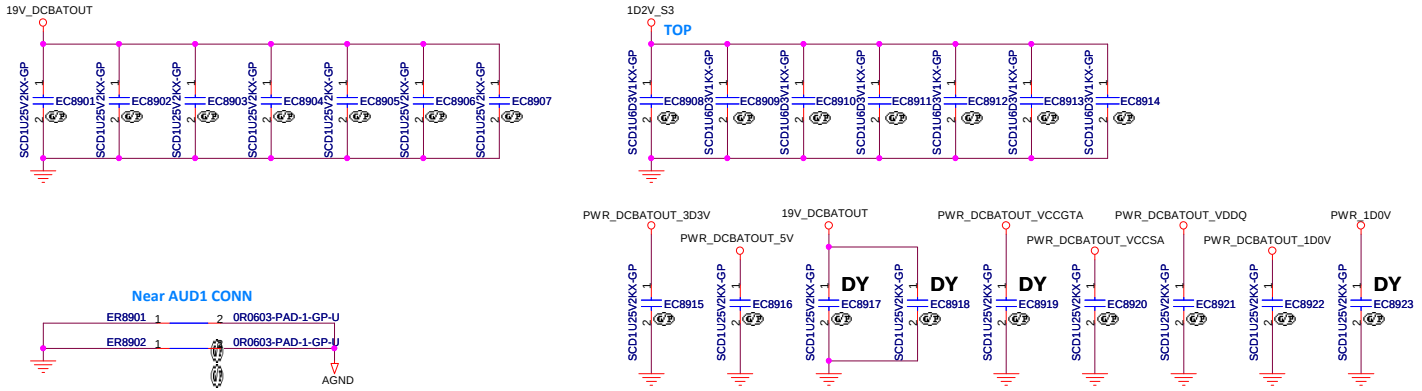
EMI Clip



RF Capacitors



EMI Capacitors



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Title: UNUSED PARTS (ME/RF/EMI)

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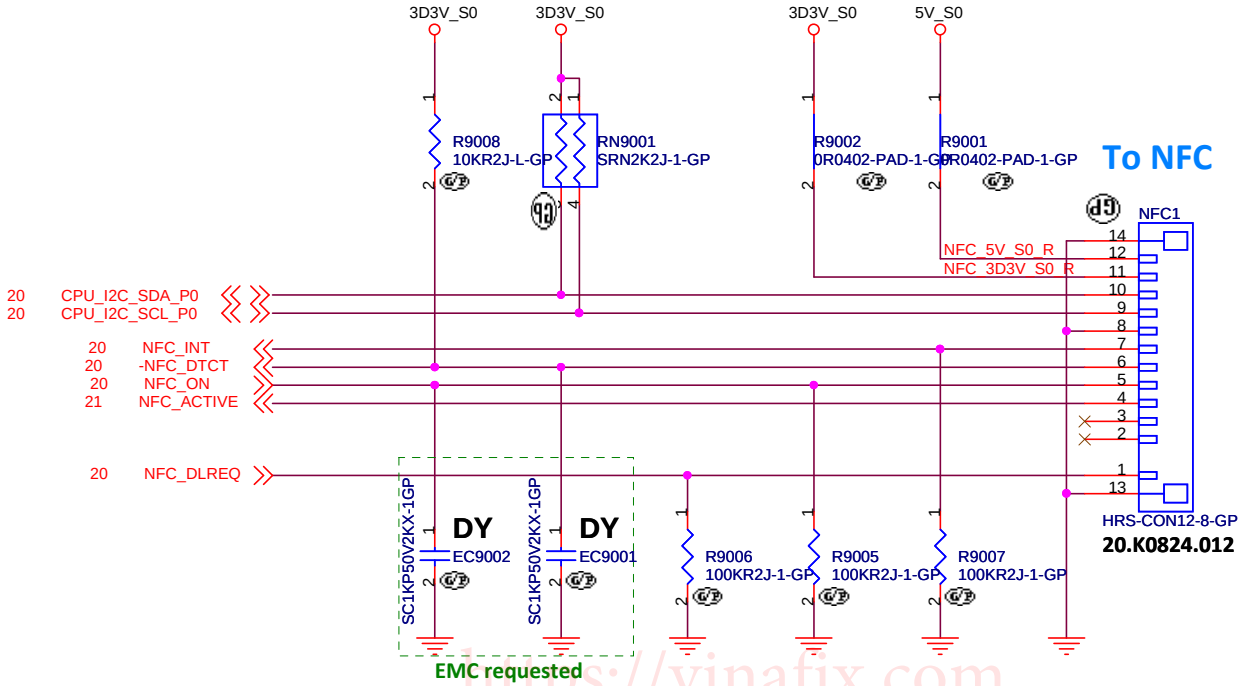

Pin	Symbol	Pin Type	Refer	Description
1	VBAT	Input Power	N/A	Power supply from system (4.5V - 5.5V)
2	PVDD	Input Power	N/A	Power supply to I/O (3.0V – 3.6V)
3	I2C_SDA	I/O	PVDD	I2C data
4	I2C_SCL	I	PVDD	I2C clock
5	GND	G	N/A	Ground
6	IRQ	O	PVDD	Interrupt from NFC module to the host (Host_Wake)
7	NFC_Presence	G	N/A	Connect to ground for NFC module presence bit (Low active)
8	VEN	I	VBAT	Reset pin. Set the device in Hard Power Down
9	TX_PWR_REQ	O	VDD	(External TX power supply request) (Active high 1.8V level output) Indicates NFC busy state during NFC communication to touchpad.
10	PMUVCC	Input Power	N/A	Power supply to UICC(1.78V~3.3V)
11	SWIO_UICC	I/O	VDD(SIM)	SWP data connection to SIM
12	DWL_REQ	I	PVDD	Firmware download control pin
S1	GND	G	N/A	Ground
S2	GND	G	N/A	Ground

Remark: P – power supply, G – ground, I – input, O – output, I/O – input/output

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Title: ***INT IO (NFC)***

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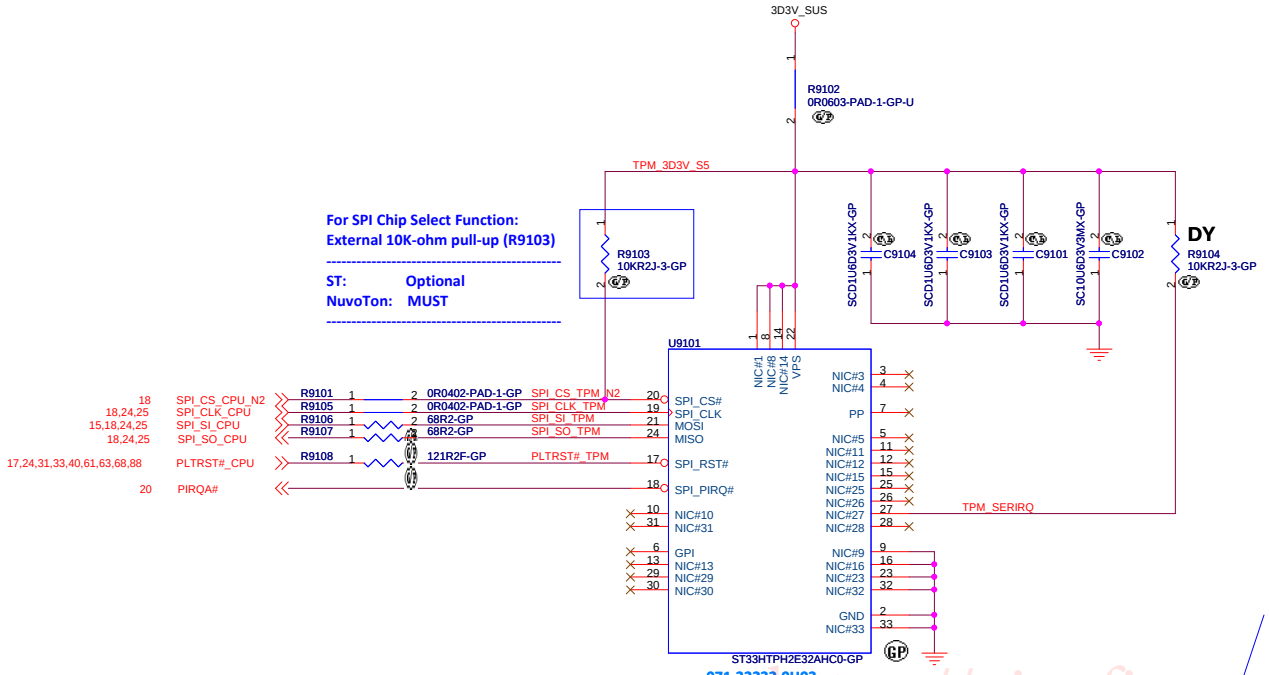
KL2_SIT_MB_W006
KL2_SIT_MB_W014
KL2_SIT_MB_W025
KL2_SIT_MB_W040
KL2_SVT_MB_W009



SPI Chip Select Pin:
ST (SPI_CS#) Internal pull-up
NuvoTon (SCS#) Internal pull-up is disabled if the pin is part of the recognized host interface

TABLE 071.33232.0H03 071.00750.0D03 ~~071.09670.0I03~~

Pin No	TCG PTP Spec	ST ST33HTPH2E32AHC0	NuvoTon NPCT750LABYX	Infineon SLB9670VQ2.0-EW7.63
1	VDD	NC	VSB	VDD
2	GND	GND	NC	GND
3	GPIO	NC	NC	NC
4	GPIO	NC	PP/GPIO6	NC
5	NC	NC	NC	NC
6	NC/GPIO	GPIO	GPIO3	GPIO
7	GPIO/VDD	PP	NC	PP
8	VDD	NC	VHIO	VDD
9	GND	NC	NC	GND
10	NC/GPIO	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	NC
13	NC/GPIO	NC	GPIO4	NC
14	VDD	NC	NC	NC
15	NC	NC	NC	NC
16	GND	NC	GND	NC
17	SPI_RST#	SPI_RST#	PLTRST#	RST#
18	SPI_PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2	PIRQ#
19	SPI_CLK	SPI_CLK	SCLK	SCLK
20	SPI_CS#	SPI_CS#	SCS#/GPIO5	CS#
21	MOSI	MOSI	MOSI/GPIO7	MOSI
22	VDD	VPS	VHIO	VDD
23	GND	NC	GND	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	NC
28	NC	NC	NC	NC
29	NC/GPIO	NC	SDA/GPIO0	NC
30	NC/GPIO	NC	SCL/GPIO1	NC
31	NC	NC	NC	NC
32	GND	NC	NC	GND

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Title: INT IO (TPM 2.0)

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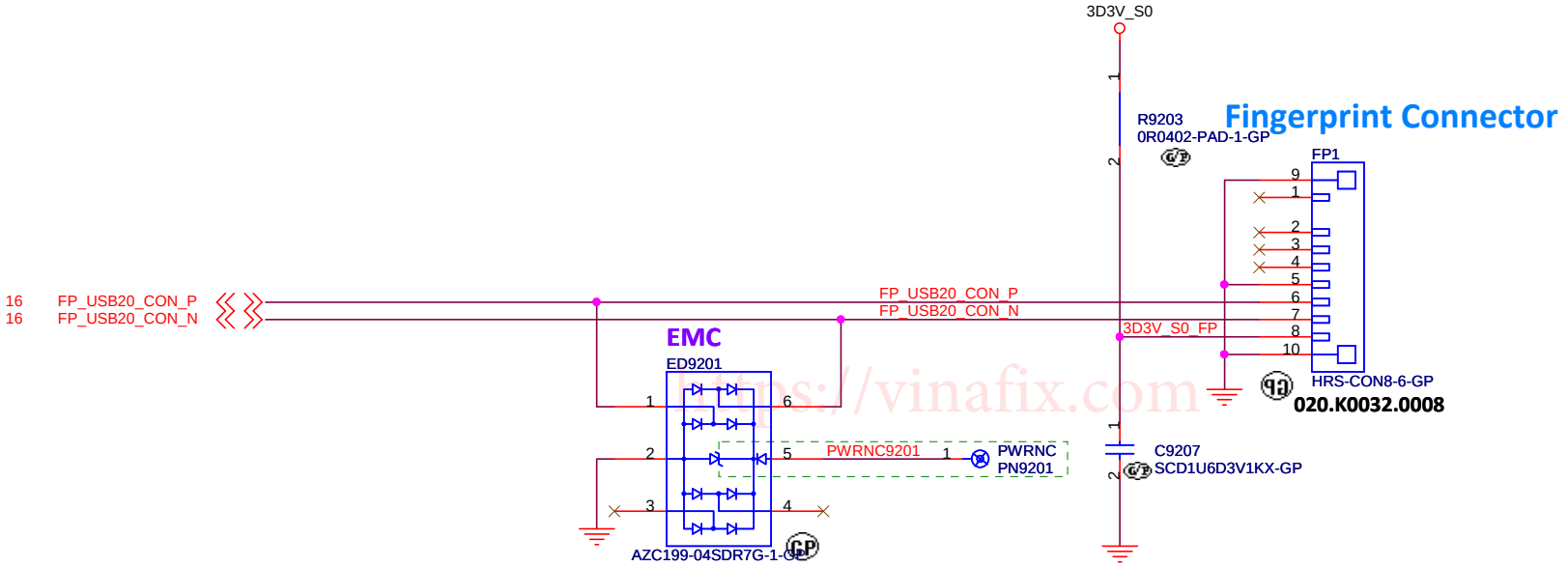
KL2_SIT_MB_W006
KL2_SVT_MB_W009



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Title: ***INT IO (FINGERPRINT)***

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Title: ***EXT IO (RSVD)***

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Title: ***EXT IO (RSVD)***

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Title: EXT IO (RSVD)

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Title: ***COMMERCIAL (RSVD)***

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Title: ***COMMERCIAL (RSVD)***

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Title: ***COMMERCIAL (RSVD)***

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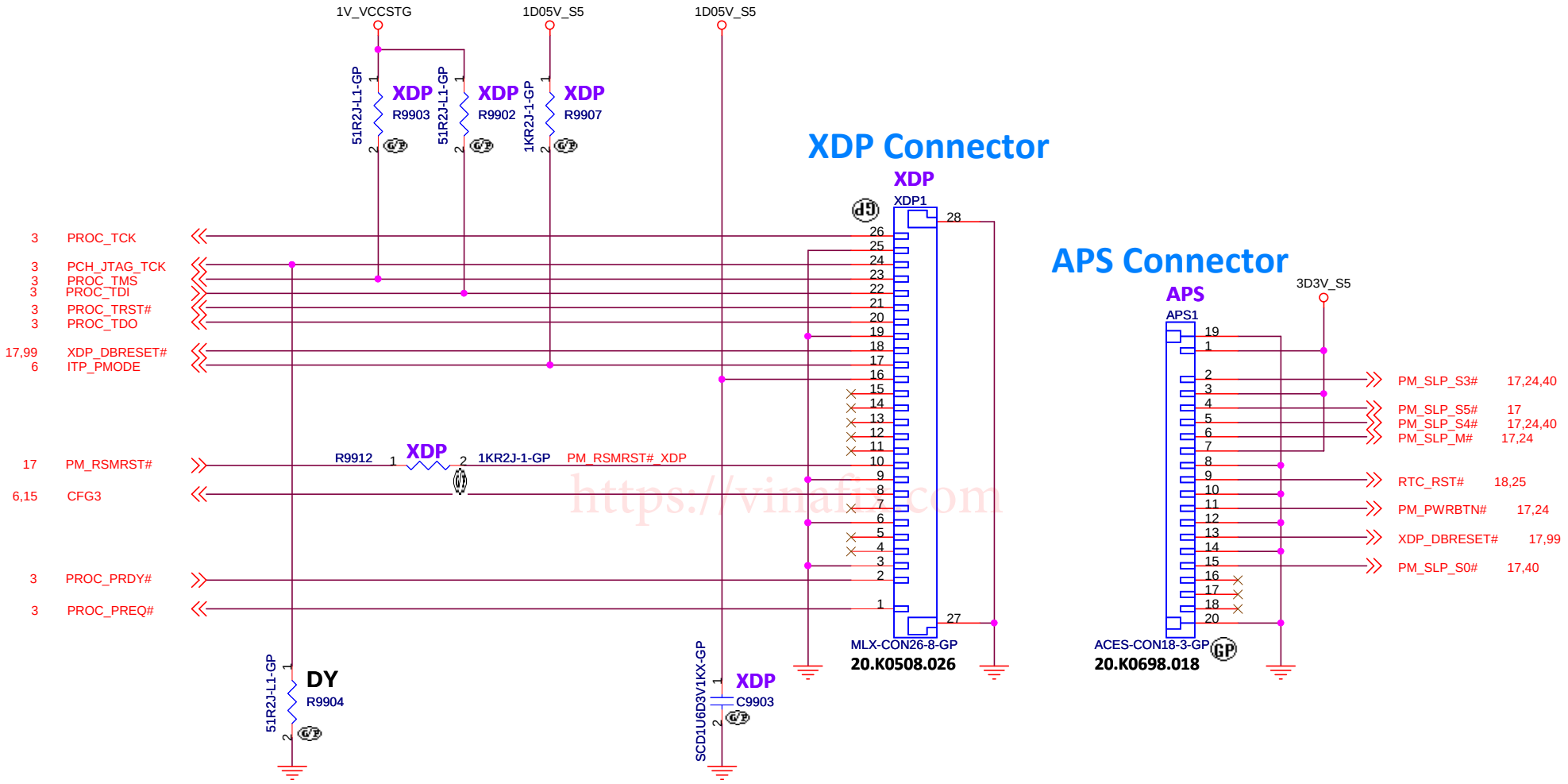
Main Func = Debug

KL2_SIT_MB_W002
KL2_SIT_MB_W006



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Title: ***DEBUG (XDP/APS)***

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