PWWAA

Marseille LC

L-A6841P REV 0.1 Schematic

Intel Penryn/ Cantiga/ ICH9M

2010-07-22 Rev. 0.1

Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

Compal Electronics, Inc.		
Title: Cover Page		
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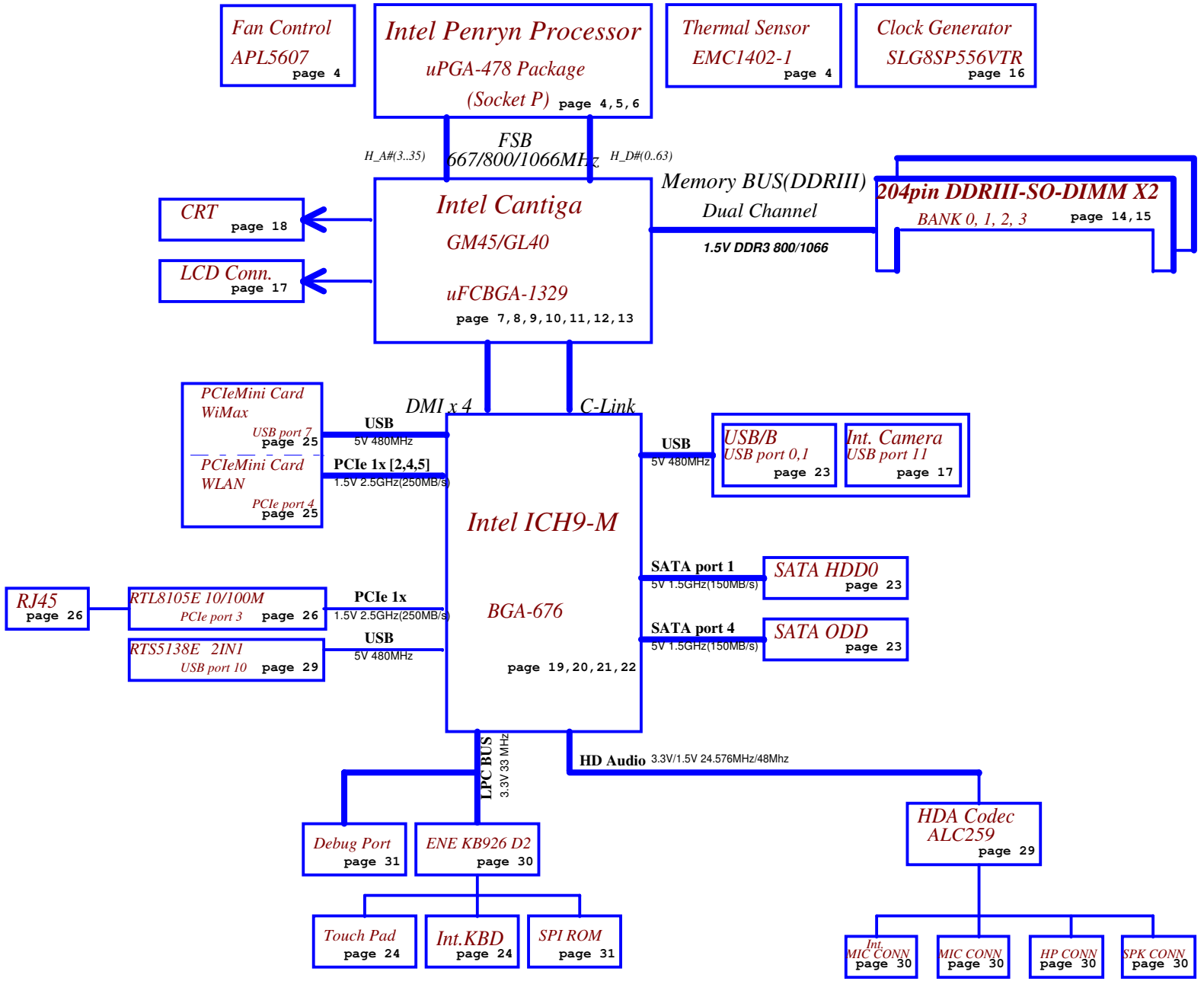
Compal Confidential

Model Name : PWWAA
File Name : LA-6841P



Power/B page 24

RTC CKT. page 20

DC/DC Interface CKT. page 33

Power Circuit DC/DC page 34,35,36,37,38,39,40

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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5 power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8V power rail	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for SB	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

BTO Option Table

Function	Card Reader		Camera	WLAN	Energy Star
description			(X)	Always	Always
explain			Camera	WLAN	Energy Star
BTO			CAM@	WLAN@	

External PCI Devices

DEVICE	PCI DEVICE ID	IDSEL#	REQ/GNT#	PIRQ

EC SM Bus1 address

Power	Device	Address
+3VL	EC KB926 D2	
+3VL	Smart Battery	**0001 011X b**

EC SM Bus2 address

Power	Device	Address
+3VS	EC KB926 D2	
+3VS	CPU THM Sen SMSC SMC1402	**1001 101Xb**

ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
+3VS	Clock Generator (SLG8SP556V)	**1101 001Xb**
+3VS	DDR DIMM0	**1001 000Xb**
+3VS	DDR DIMM1	**1001 010Xb**

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Title: Notes List

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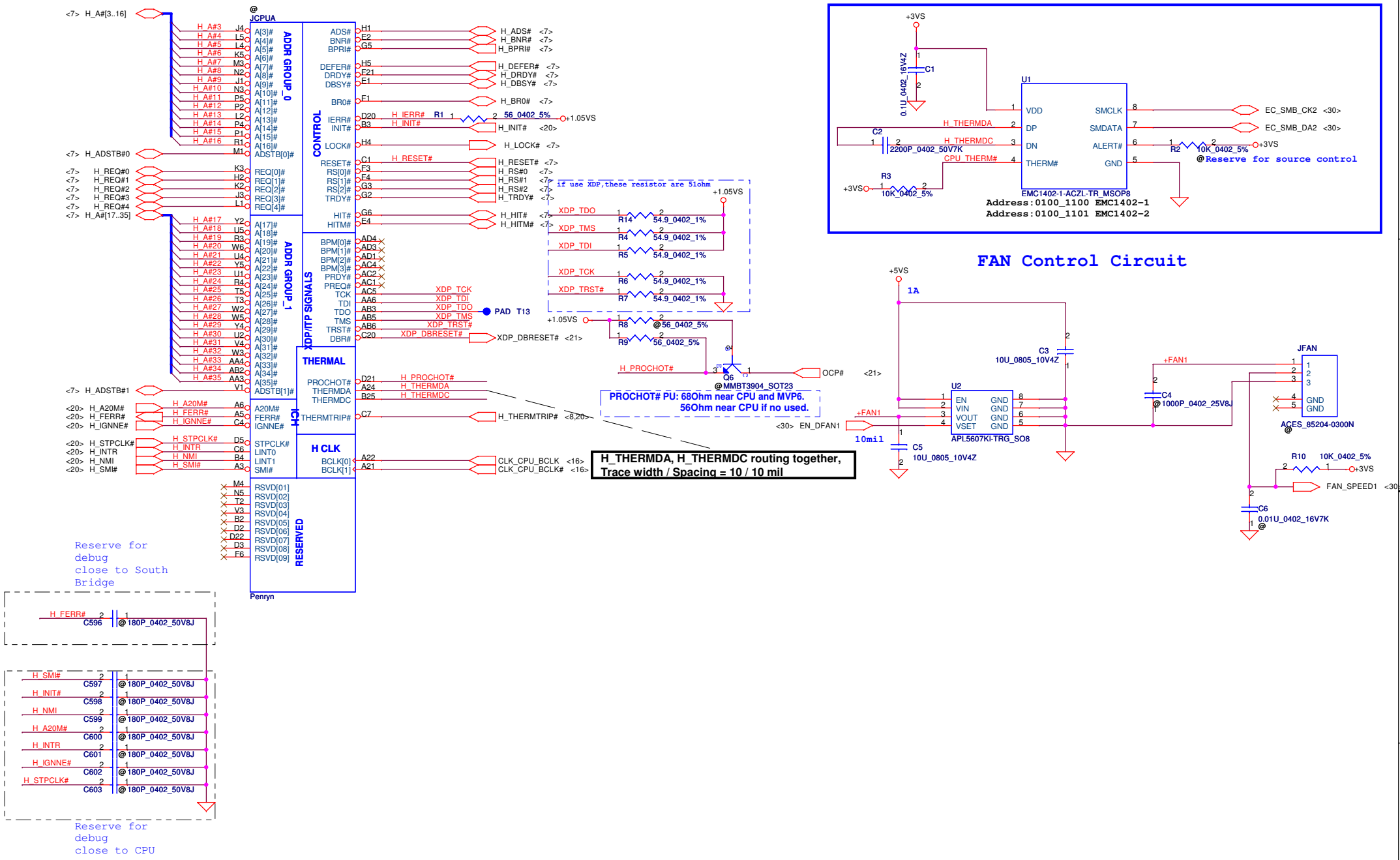

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Compal Electronics, Inc.	
Title	Penryn(1/3)-AGTL+/THM/FAN
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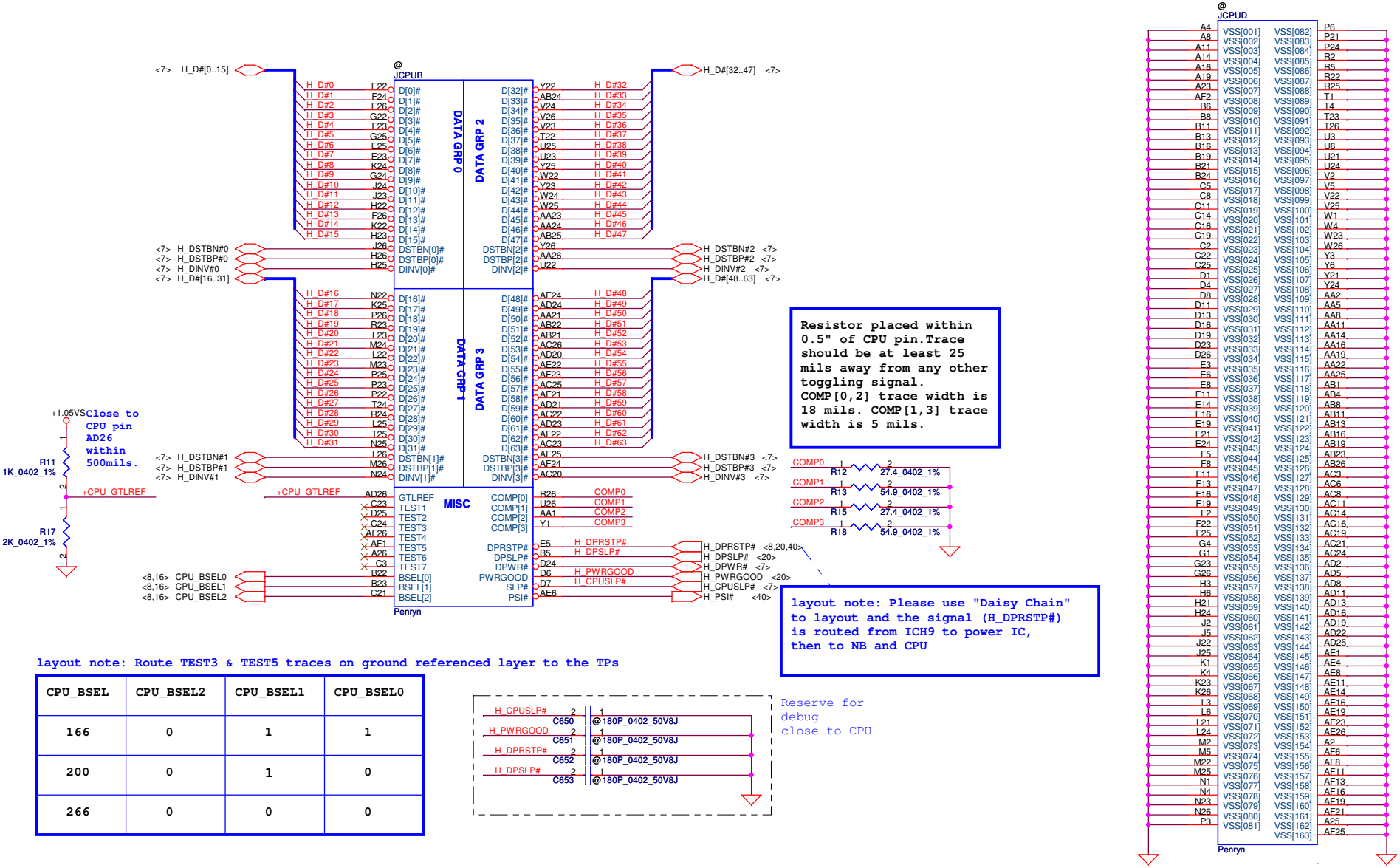

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

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Title: Penryn(2/3)-AGTL+/GND

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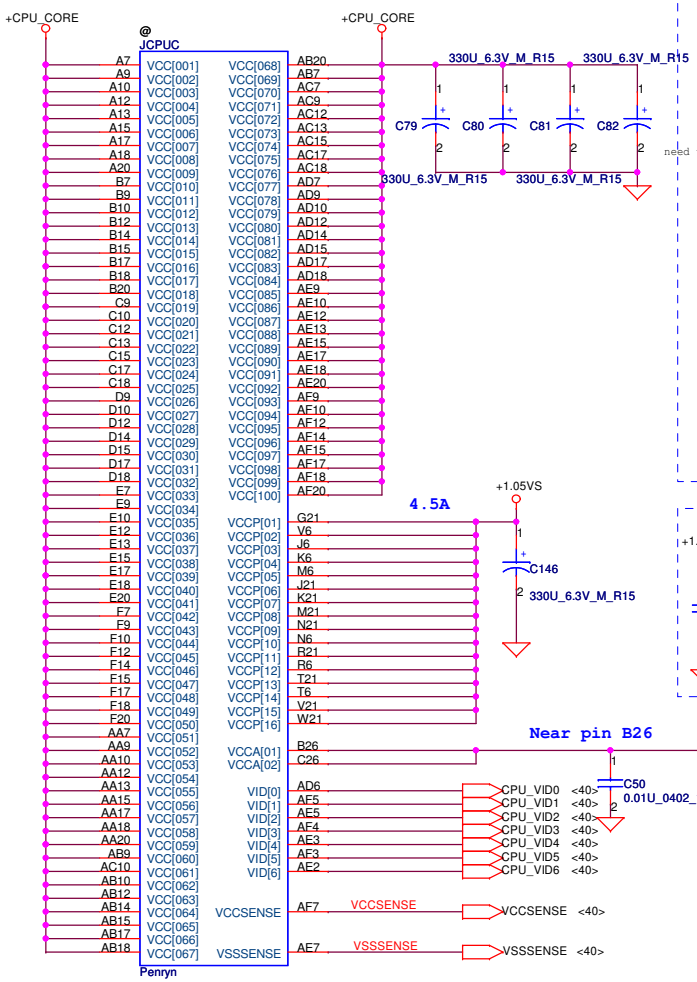
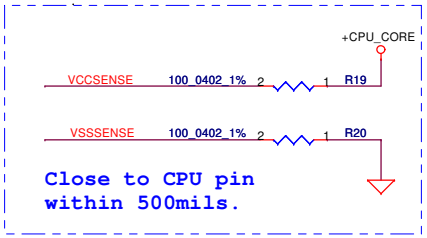
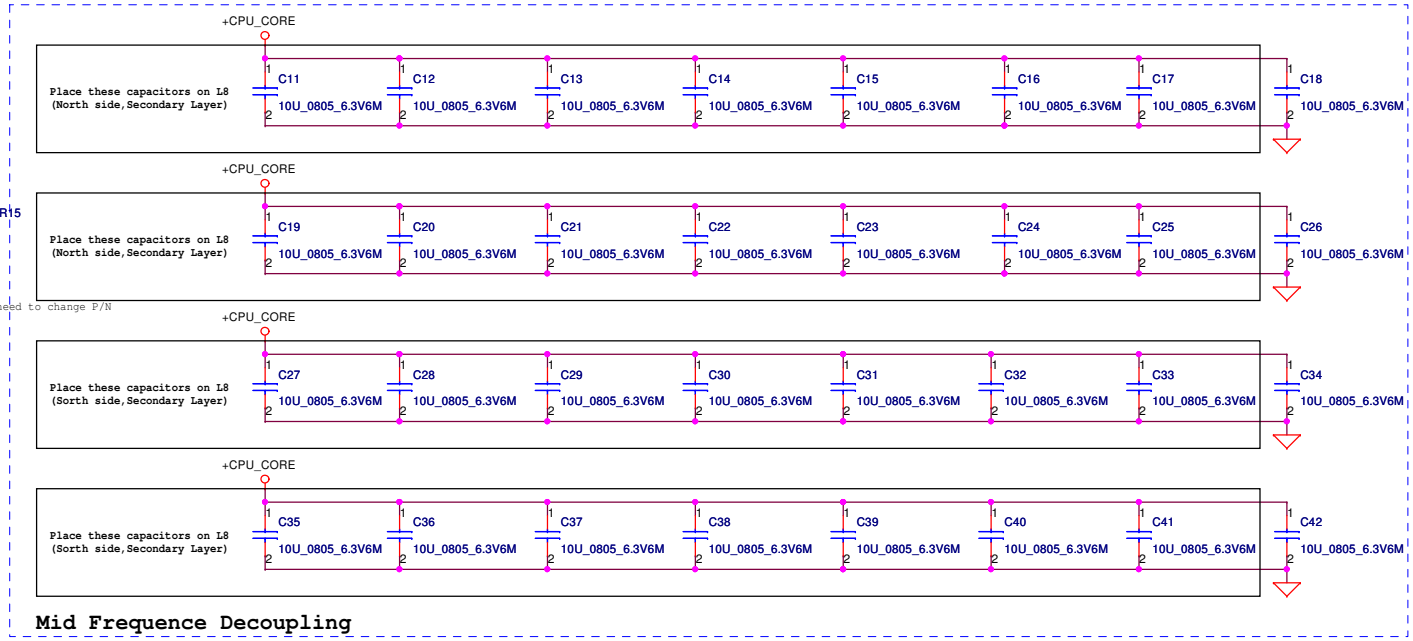
Near CPU CORE regulator

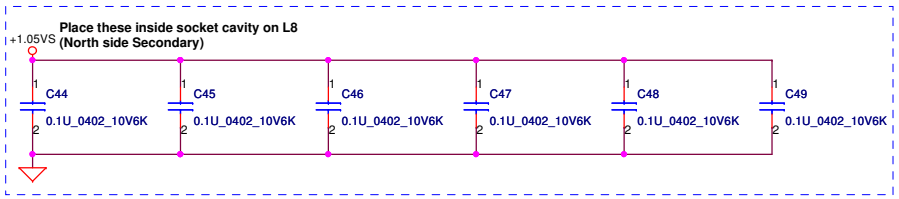
ESR <= 1.5m ohm
Capacitor > 1980uF





Length match within 25 mils.
The trace width/space/other is 14/7/25.





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Compal Electronics, Inc.

Title: Penryn(3/3)-PWR/Bypass

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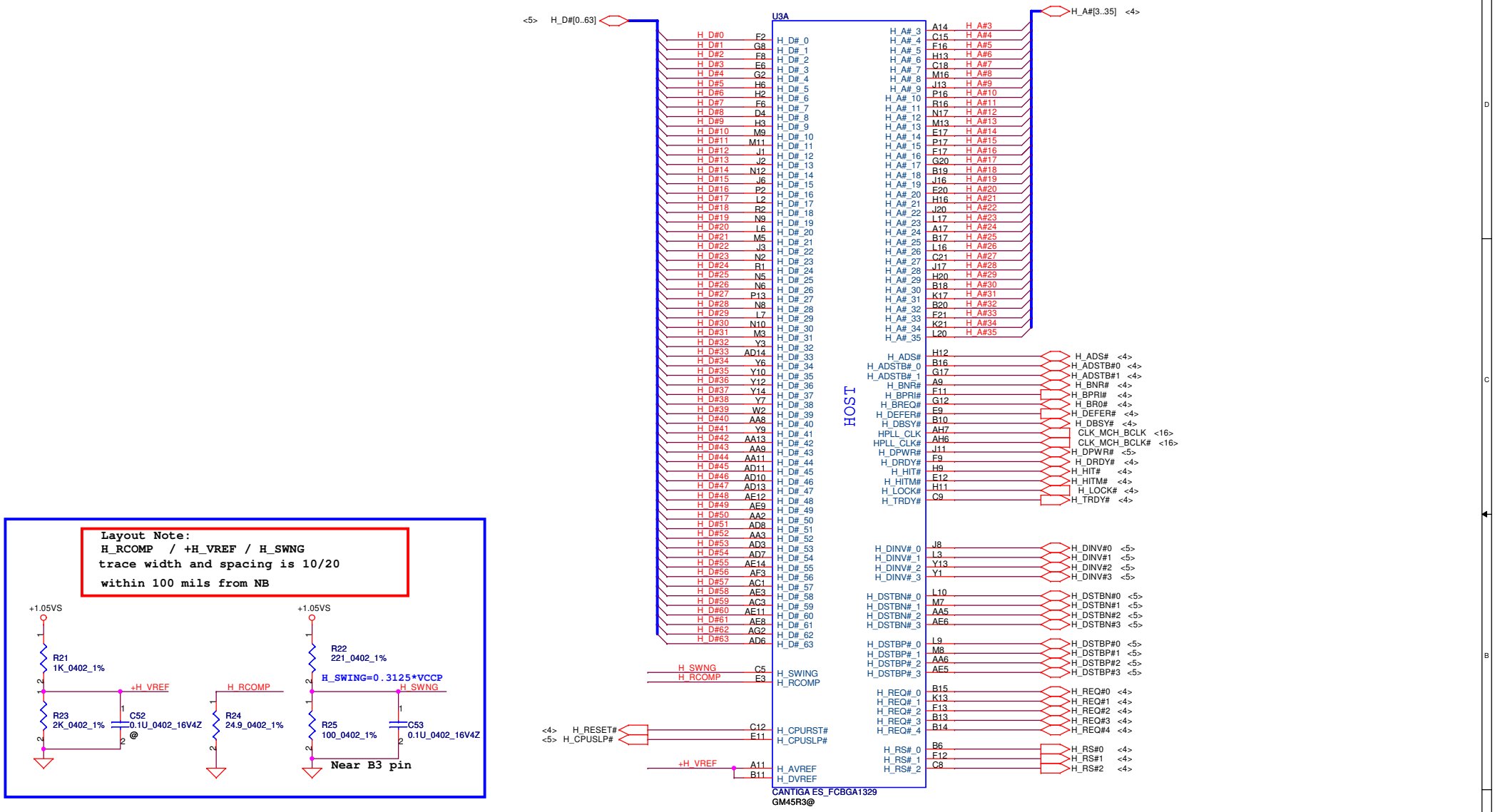

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Cantiga GMCH(1/7)-GTL

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Strap Pin Table

CFG[2:0]		011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6	Internal pull-up	0 = iTPM Host Interface is enabled can support disble by SW. 1 = iTPM Host Interface is Disabled *(Default)
CFG7	Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9	Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10	Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12]	Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation*(Default)
CFG16	Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19	Internal pull-down	0 = Normal Operation 1 = DMI Lane Reversal Enable *(Default)
CFG20 (PCIE/SDVO select)	Internal pull-down	0 = Only PCIE or [SDVO/DP/HDMI] is operational. * (Default) 1 = PCIE/[SDVO/DP/HDMI] are operating simu.

Strap Pin Table

SDVO_CTRLDATA (Internal pull-down)	0 = SDVO interface disabled *(Default) 1 = SDVO interface enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (iHDMI/DP) interface disabled *(Default) 1 = Digital display (iHDMI/DP) interface enabled

Use VGATE for GMCH_PWROK

<21,30,40> VGATE — R58 @0_0402_5%
<21,30> ICH_PWROK — R59 0_0402_5%
→ GMCH_PWROK

CANTIGA ES_FCBGA1329
GM45R3@

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Title: Cantiga GMCH(2/7)-GTL

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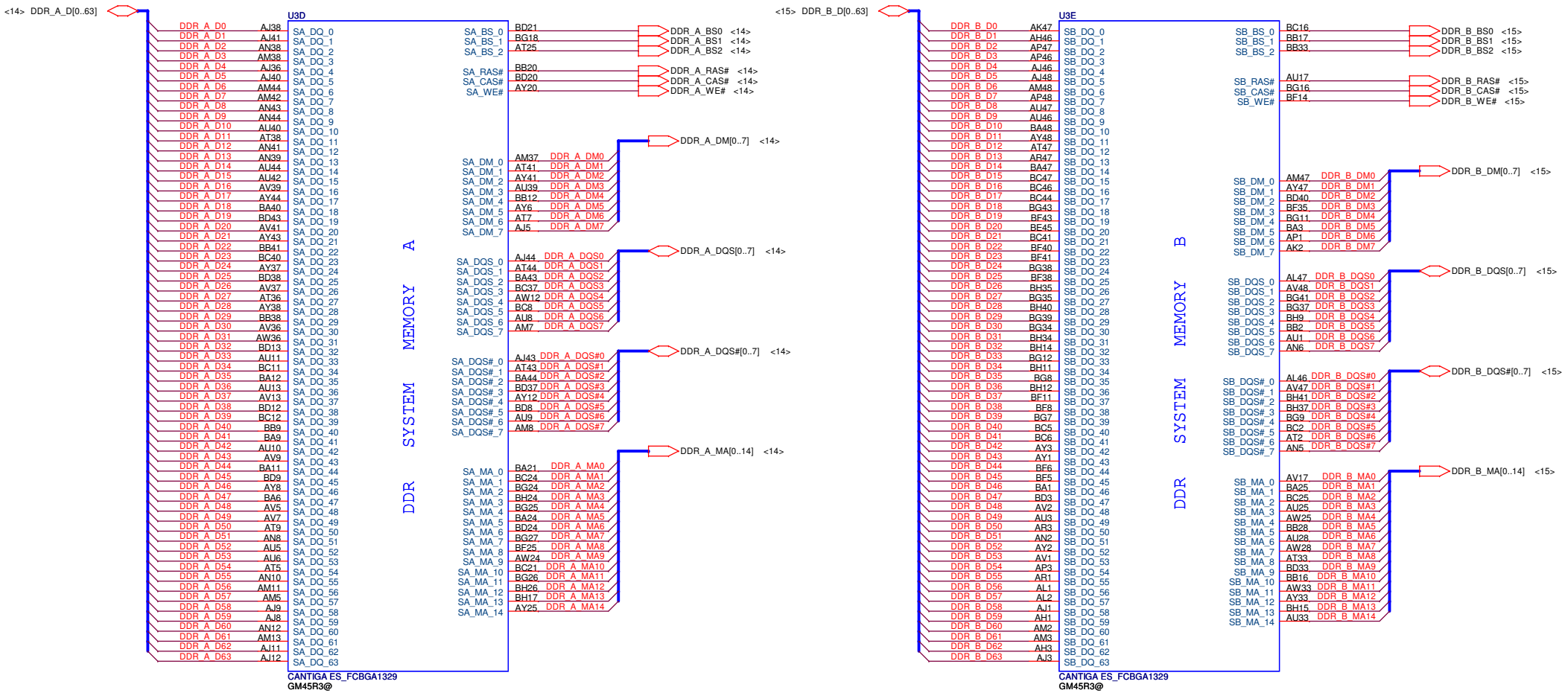

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Title: Cantiga GMCH(3/7)-GTL

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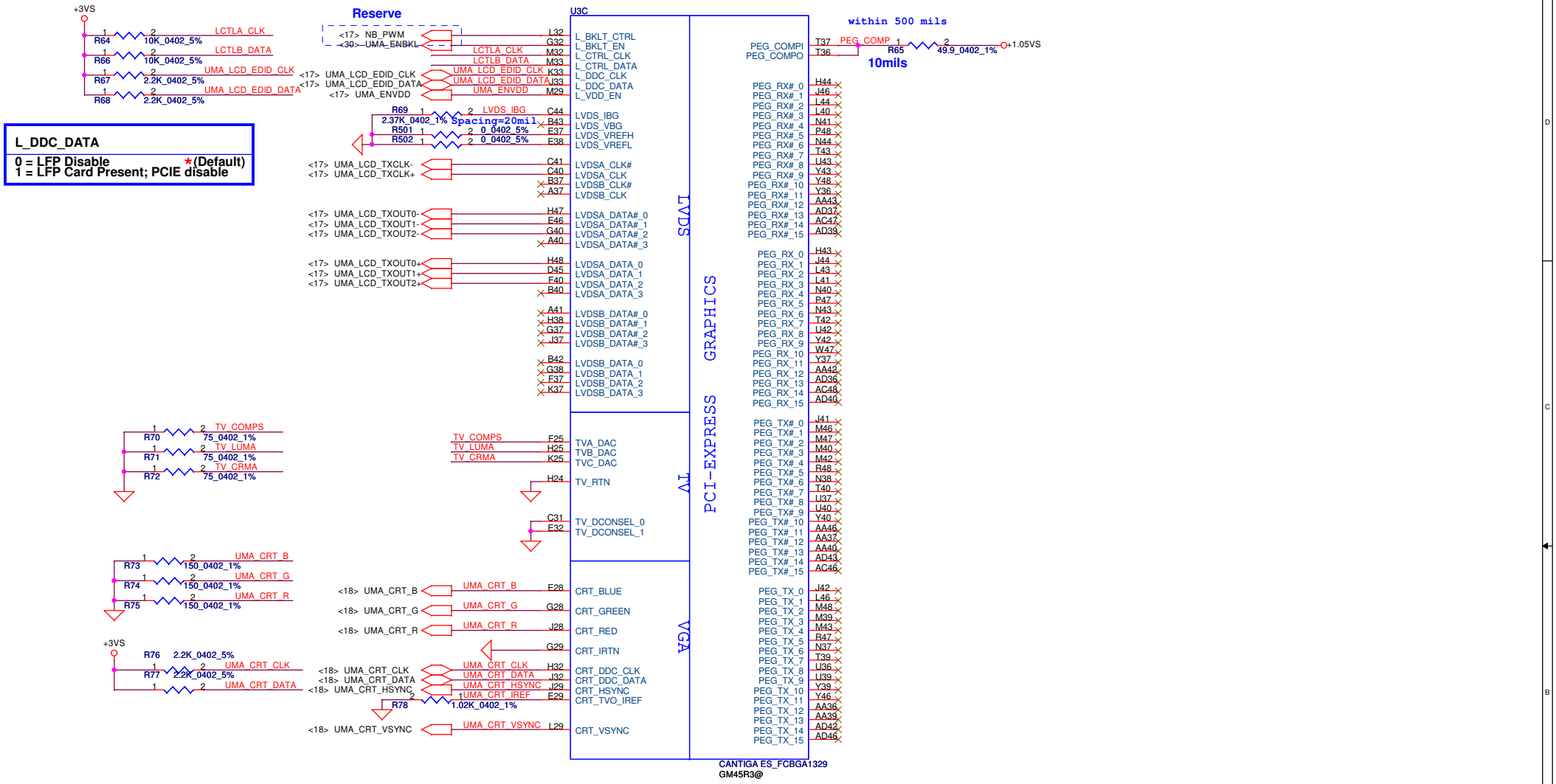

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Title: Cantiga GMCH(4/7)-GTL

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	PWWAA LA6841P M/B	0.1

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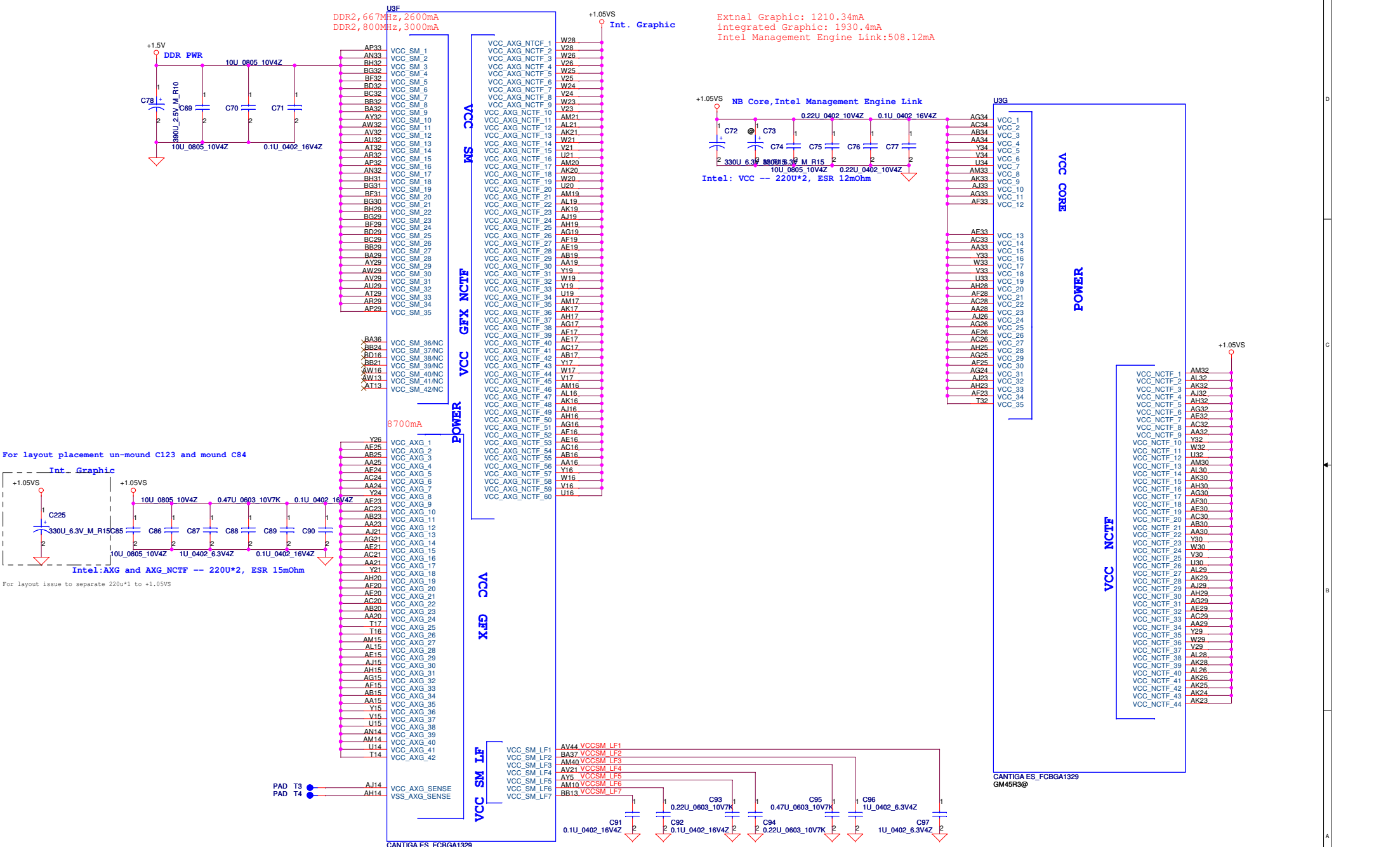

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Title	Cantiga GMCH(5/7)-GTL	
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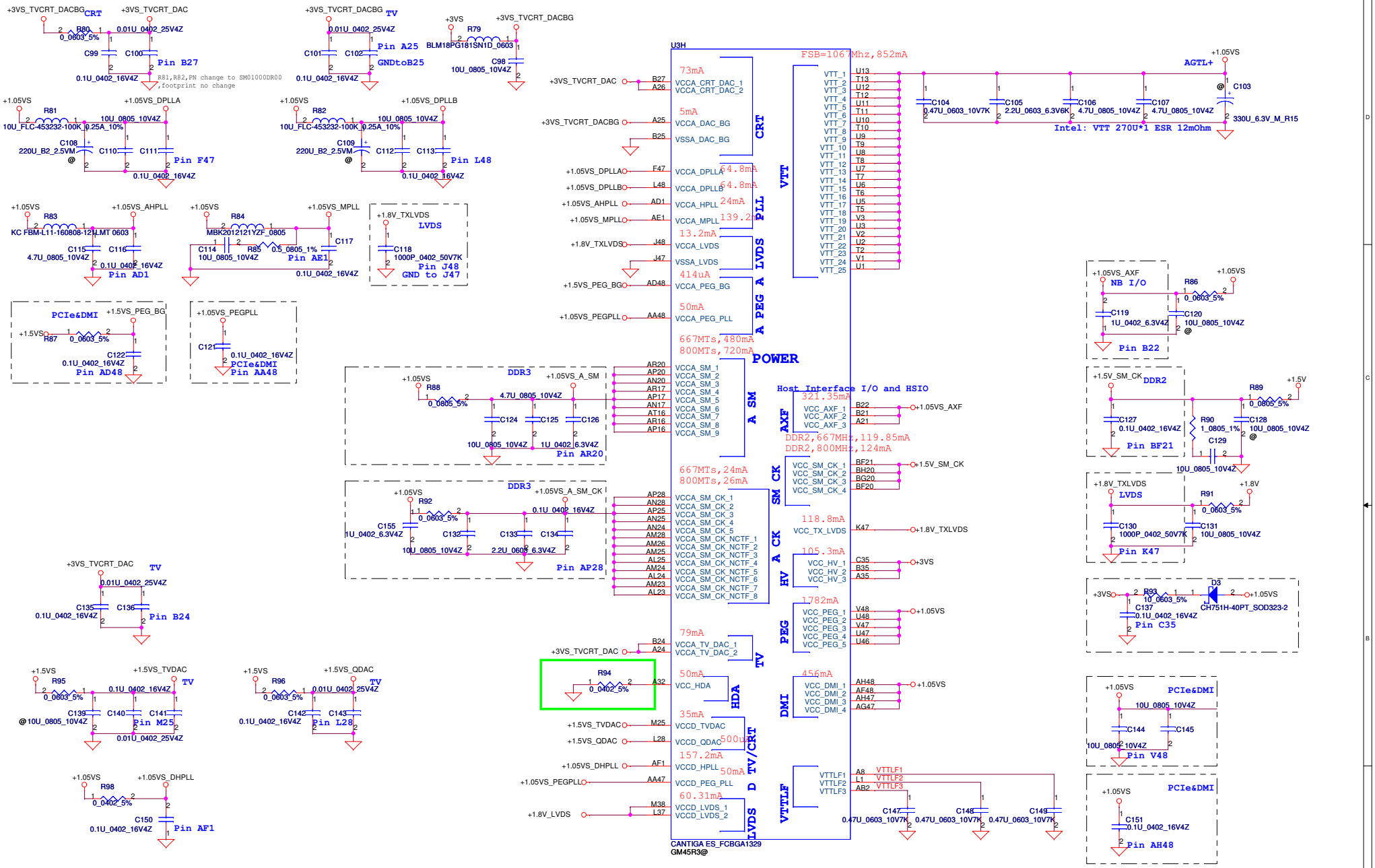

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Compal Electronics, Inc.

Title: Crestline GMCH (6/7)-VCC

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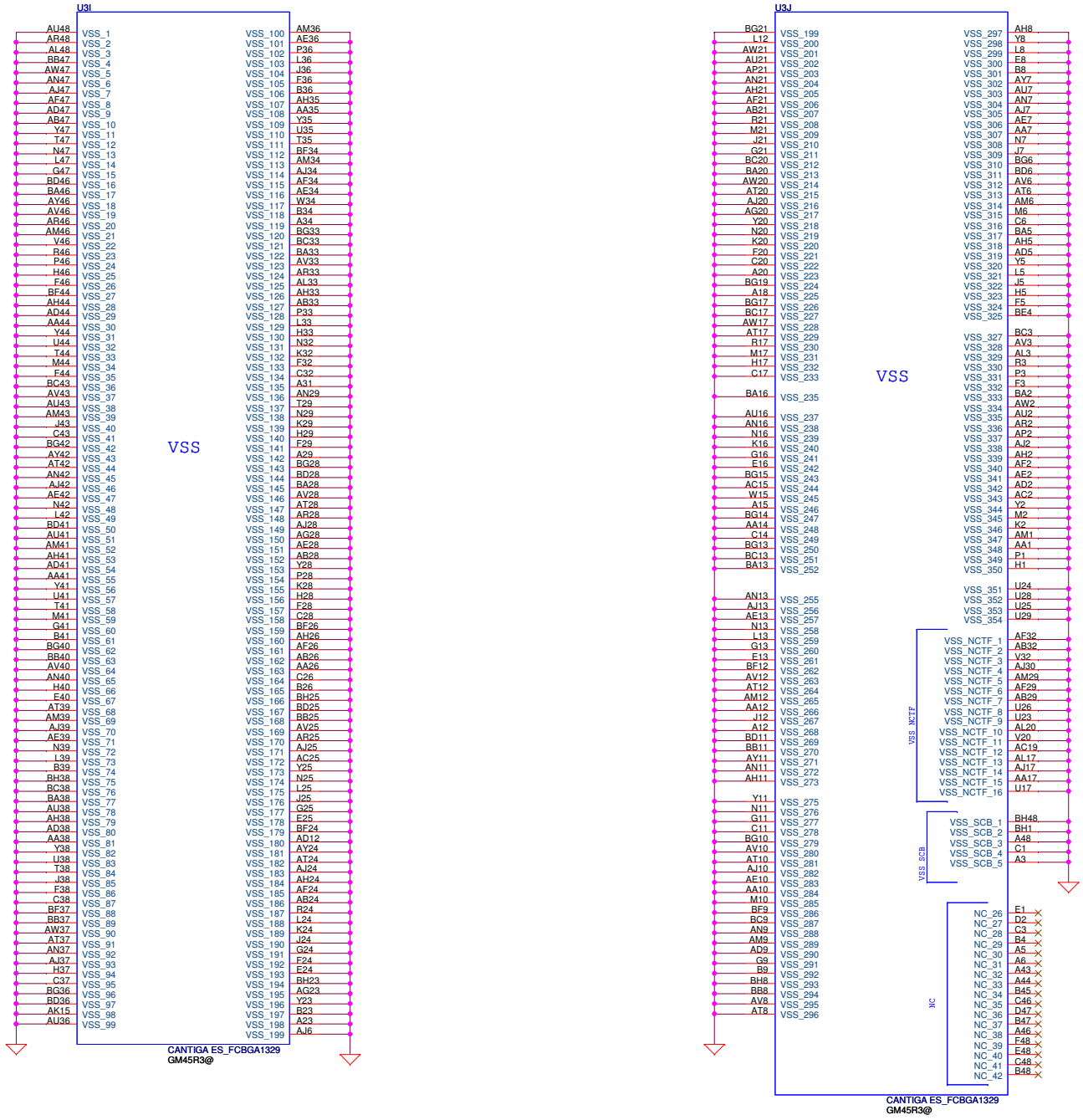

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Title: Cantiga GMCH(1/7)-GTL

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DDR3 SO-DIMM A
REVERSE TYPE

DDR_A_DQS[0..7] <9>
DDR_A_DQS#[0..7] <9>
DDR_A_D[0..63] <9>
DDR_A_DM[0..7] <9>
DDR_A_MA[0..14] <9>

+V_DDR3_DIMM_REF
JDDRH
close to JDDRH.1
CONN@
LOTES_AAA-DDR-111-K01
SM_DRAMRST# <8,15>
DDRA_CKE0 <8>
DDRA_CKE1 <8>
DDRA_CLK0 <8>
DDRA_CLK0# <8>
DDRA_CLK1 <8>
DDRA_CLK1# <8>
DDR_A_BS0 <9>
DDR_A_BS1 <9>
DDR_A_WE# <9>
DDR_A_CAS# <9>
DDR_A_RAS# <9>
DDRA_SCS0# <8>
DDRA_SCS1# <8>
DDRA_ODT0 <8>
DDRA_ODT1 <8>
+DDR_VREF_CA_DIMMA
close to JDDRH.126
PM_EXTTS# <8,15>
PM_SMBDATA <15,16,21,25>
PM_SMBCLK <15,16,21,25>

RD1 1K_0402_1%
RD2 1K_0402_1%
<BOM Structure>

Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

CD45 @ 330U_6.3V_M_R15

Layout Note:
Place near JDDRH.203 & JDDRH.204

RD3 10K_0402_5%
RD4 0_0402_5%
RD5 10K_0402_5%
RD6 @0_0402_5%

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Compal Electronics, Inc.

Title: DDRII-SODIMM0

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DDR3 SO-DIMM B
REVERSE TYPE

DDR_B_DQS[0..7] <9>
DDR_B_DQS#[0..7] <9>
DDR_B_D[0..63] <9>
DDR_B_DM[0..7] <9>
DDR_B_MA[0..14] <9>

+V_DDR3_DIMM_REF

CD23 0.1U_0402_16V4Z
CD24 2.2U_0603_6.3V4Z
close to JDDRL.1

JDDRL

1	VREF_DQ	VSS1	2		
3	VSS2	DQ4	4	DDR_B_D4	
5	DQ0	DQ5	6	DDR_B_D5	
7	DQ1	VSS3	8		
9	VSS4	DQS#0	10	DDR_B_DQS#0	
11	DM0	DQS0	12	DDR_B_DQS0	
13	VSS5	VSS6	14		
15	DQ2	DQ6	16	DDR_B_D6	
17	DQ3	DQ7	18	DDR_B_D7	
19	VSS7	VSS8	20		
21	DQ8	DQ12	22	DDR_B_D12	
23	DQ9	DQ13	24	DDR_B_D13	
25	VSS9	VSS10	26		
27	DQS#1	DM1	28	DDR_B_DM1	
29	DQS1	RESET#	30	SM_DRAMRST# <8,14>	
31	VSS11	VSS12	32		
33	DQ10	DQ14	34	DDR_B_D14	
35	DQ11	DQ15	36	DDR_B_D15	
37	VSS13	VSS14	38		
39	DQ16	DQ20	40	DDR_B_D20	
41	DQ17	DQ21	42	DDR_B_D21	
43	VSS15	VSS16	44		
45	DQS#2	DM2	46	DDR_B_DM2	
47	DQS2	VSS17	48		
49	VSS18	DQ22	50	DDR_B_D22	
51	DQ18	DQ23	52	DDR_B_D23	
53	DQ19	VSS19	54		
55	VSS20	DQ28	56	DDR_B_D28	
57	DQ24	DQ29	58	DDR_B_D29	
59	DQ25	VSS21	60		
61	VSS22	DQS#3	62	DDR_B_DQS#3	
63	DM3	DQS3	64	DDR_B_DQS3	
65	VSS23	VSS24	66		
67	DQ26	DQ30	68	DDR_B_D30	
69	DQ27	DQ31	70	DDR_B_D31	
71	VSS25	VSS26	72		
73	CKE0	CKE1	74	DDRB_CKE1 <8>	
75	VDD1	VDD2	76		
77	NC1	A15	78	DDR_B_MA14	
79	BA2	A14	80		
81	VDD3	VDD4	82		
83	A12/BC#	A11	84	DDR_B_MA11	
85	A9	A7	86	DDR_B_MA7	
87	VDD5	VDD6	88		
89	A8	A6	90	DDR_B_MA6	
91	A5	A4	92	DDR_B_MA4	
93	VDD7	VDD8	94		
95	A3	A2	96	DDR_B_MA2	
97	A1	A0	98	DDR_B_MA0	
99	VDD9	VDD10	100		
101	CK0	CK1	102	DDRB_CLK1 <8>	
103	CK0#	CK1#	104	DDRB_CLK1# <8>	
105	VDD11	VDD12	106		
107	A10/AP	BA1	108	DDR_B_BS1 <9>	
109	BA0	RAS#	110	DDR_B_RAS# <9>	
111	VDD13	VDD14	112		
113	WE#	S0#	114	DDRB_SCS0# <8>	
115	CAS#	ODT0	116	DDRB_ODT0 <8>	
117	VDD15	VDD16	118		
119	A13	ODT1	120	DDRB_ODT1 <8>	
121	S1#	NC2	122		
123	VDD17	VDD18	124		
125	NCTEST	VREF_CA	126	+DDR_VREF_CA_DIMMB	
127	VSS27	VSS28	128		
129	DQ32	DQ36	130	DDR_B_D36	
131	DQ33	DQ37	132	DDR_B_D37	
133	VSS29	VSS30	134		
135	DQS#4	DM4	136	DDR_B_DM4	
137	DQS4	VSS31	138		
139	VSS32	DQ38	140	DDR_B_D38	
141	DQ34	DQ39	142	DDR_B_D39	
143	DQ35	VSS33	144		
145	VSS34	DQ44	146	DDR_B_D44	
147	DQ40	DQ45	148	DDR_B_D45	
149	DQ41	VSS35	150		
151	VSS36	DQS#5	152	DDR_B_DQS#5	
153	DM5	DQS5	154	DDR_B_DQS5	
155	VSS37	VSS38	156		
157	DQ42	DQ46	158	DDR_B_D46	
159	DQ43	DQ47	160	DDR_B_D47	
161	VSS39	VSS40	162		
163	DQ48	DQ52	164	DDR_B_D52	
165	DQ49	DQ53	166	DDR_B_D53	
167	VSS41	VSS42	168		
169	DQS#6	DM6	170	DDR_B_DM6	
171	DQS6	VSS43	172		
173	VSS44	DQ54	174	DDR_B_D54	
175	DQ50	DQ55	176	DDR_B_D55	
177	DQ51	VSS45	178		
179	VSS46	DQ60	180	DDR_B_D60	
181	DQ56	DQ61	182	DDR_B_D61	
183	DQ57	VSS47	184		
185	VSS48	DQS#7	186	DDR_B_DQS#7	
187	DM7	DQS7	188	DDR_B_DQS7	
189	VSS49	VSS50	190		
191	DQ58	DQ62	192	DDR_B_D62	
193	DQ59	DQ63	194	DDR_B_D63	
195	VSS51	VSS52	196		
197	SA0	EVENT#	198	PM_EXTTS# <8,14>	
199	VDDSPD	SDA	200	PM_SMBDATA <14,16,21,25>	
201	SA1	SCL	202	PM_SMBCLK <14,16,21,25>	
203	VTT1	VTT2	204	+0.75VS	
205	G1	G2	206		

TYCO_2-2013289-1
CONN@

<8> DDRB_CKE0
+1.5V
<9> DDR_B_BS2
<8> DDRB_CLK0
<8> DDRB_CLK0#
<9> DDR_B_BS0
<9> DDR_B_WE#
<9> DDR_B_CAS#
<8> DDRB_SCS1#

RD10 1 2 @0_0402_5%
RD7 1 2 0_0402_5%
+V_DDR3_DIMM_REF
CD28 2.2U_0603_6.3V4Z
CD27 0.1U_0402_16V4Z
close to JDDRL.126

RD8 1 2 10K_0402_5%
RD9 1 2 10K_0402_5%
+3VS
+0.75VS
CD26 2.2U_0603_6.3V4Z
CD25 0.1U_0402_16V4Z

Layout Note:
Place near JDDRL

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB

+1.5V
22U_0805_6.3V6M CD29
CD30 @ 10U_0805_6.3V6M
CD31 @ 10U_0805_6.3V6M
CD32 @ 10U_0805_6.3V6M
22U_0805_6.3V6M CD33
CD34 @ 10U_0805_6.3V6M
0.1U_0402_16V4Z CD38
0.1U_0402_16V4Z CD37
0.1U_0402_16V4Z CD36
0.1U_0402_16V4Z CD35

Layout Note:
Place near JDDRL.203 & JDDRL.204

+0.75VS
CD40 1U_0402_6.3V4Z
CD42 1U_0402_6.3V4Z
CD41 1U_0402_6.3V4Z
CD43 1U_0402_6.3V4Z
CD44 @ 10U_0805_6.3V6M

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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

Routing the trace at least 10mil

place 22ohm for damping resistor when loading is two device,If one device use 33ohm

close to U4 befor R115
EMI request 6/25

CLK_ICH	0 = SRC8/SRC8# (100MHz) 1 = ITP/ITP# (266MHz)
CLK_EC	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)

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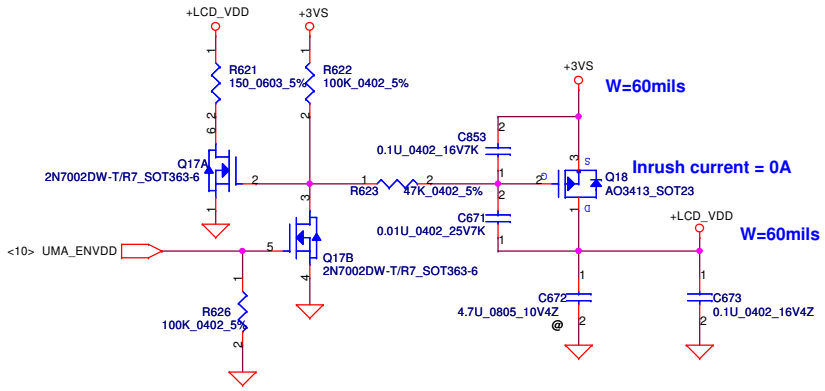
Compal Electronics, Inc.

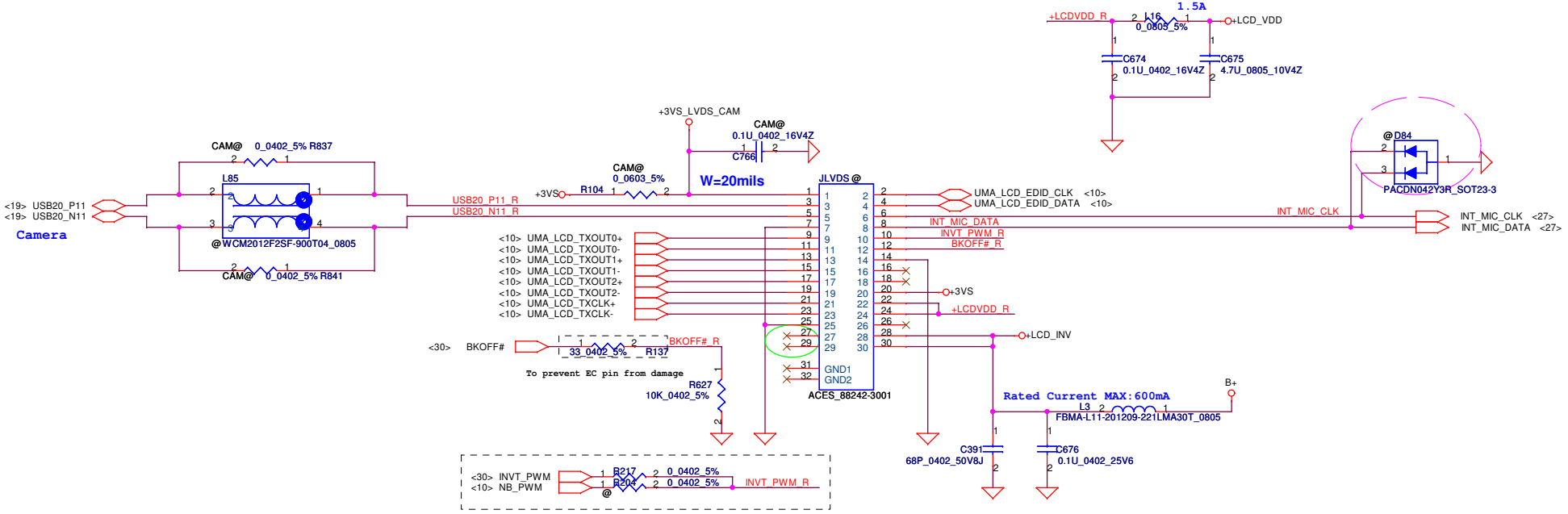
Title: Clock Generator

Size | Document Number: PWWAA LA6841P M/B | Rev: 0.1

Date: Monday, August 16, 2010 | Sheet 16 of 44

LCD/PANEL BD. Conn.





Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

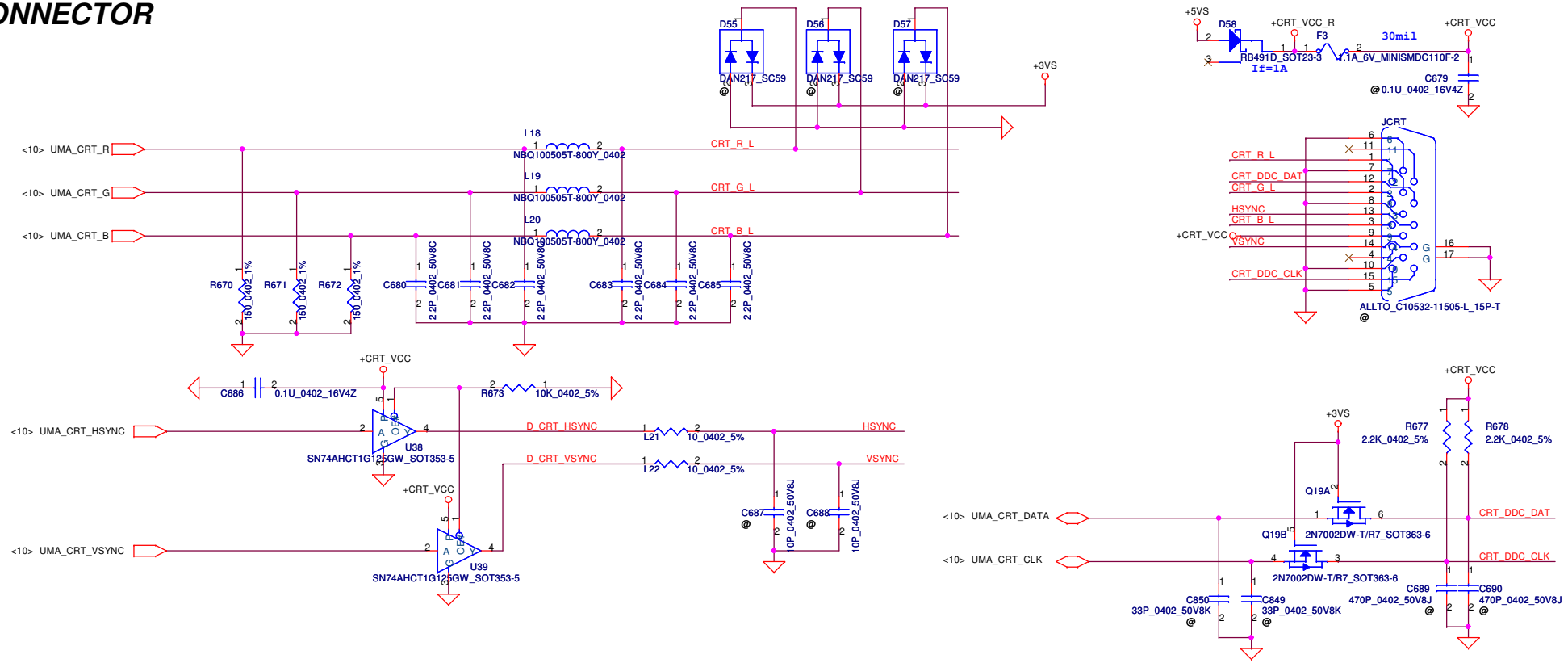
Compal Electronics, Inc.

Title: NB9M GDDR2A

Size | Document Number: PWWAA LA6841P M/B | Rev: 0.1

Date: Monday, August 16, 2010 | Sheet 17 of 44

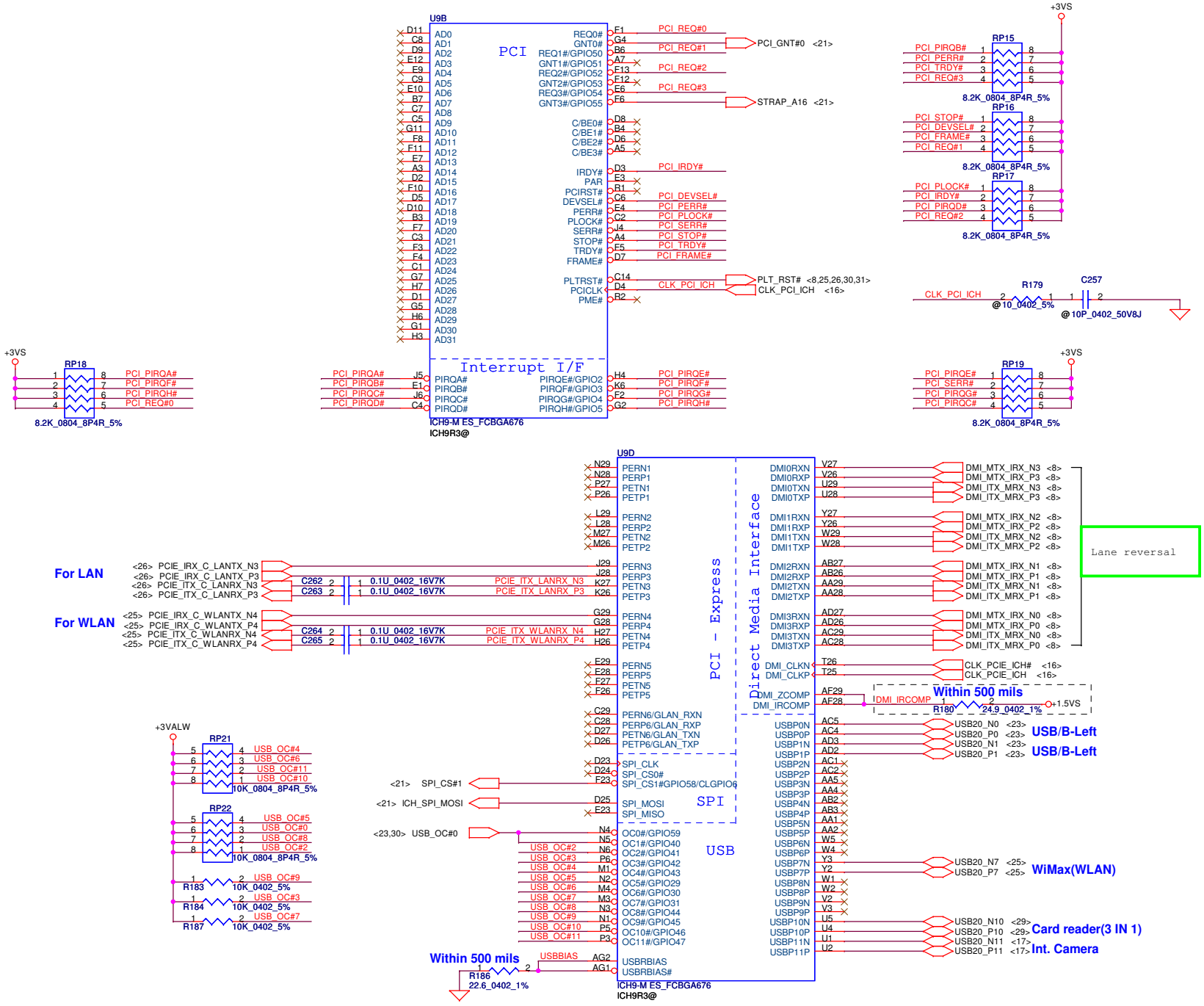
CRT CONNECTOR



Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

Compal Electronics, Inc.

Title	CRT\TV\LVDS	
Size	Document Number: PWWAA LA6841P M/B	Rev: 0.1
Date: Monday, August 16, 2010	Sheet 18 of 44	



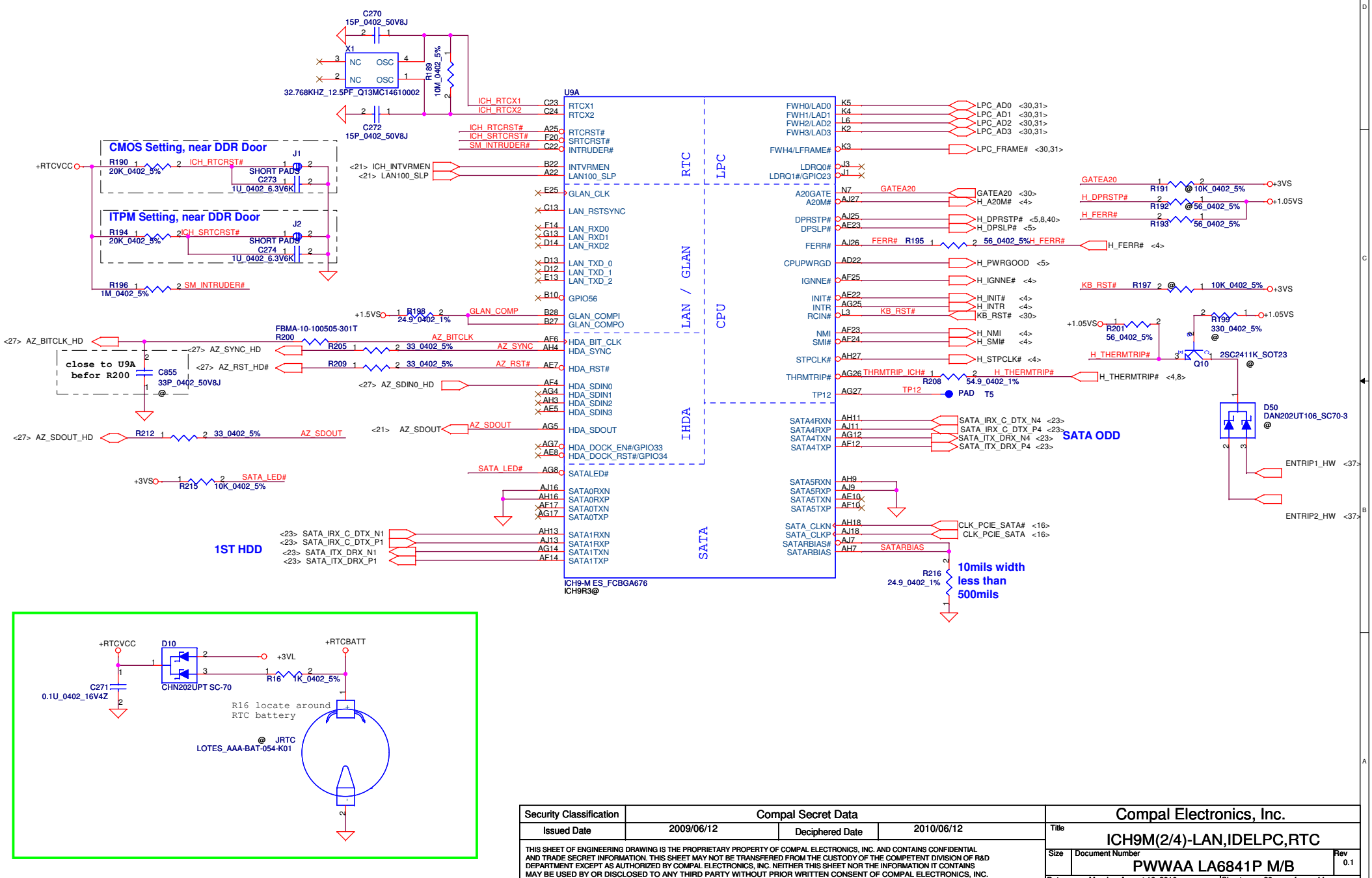
Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

Compal Electronics, Inc.

Title: ICH9M(1/4)-PCI

Size	Document Number	Rev
	PWWAA LA6841P M/B	0.1

Date: Monday, August 16, 2010 Sheet 19 of 44



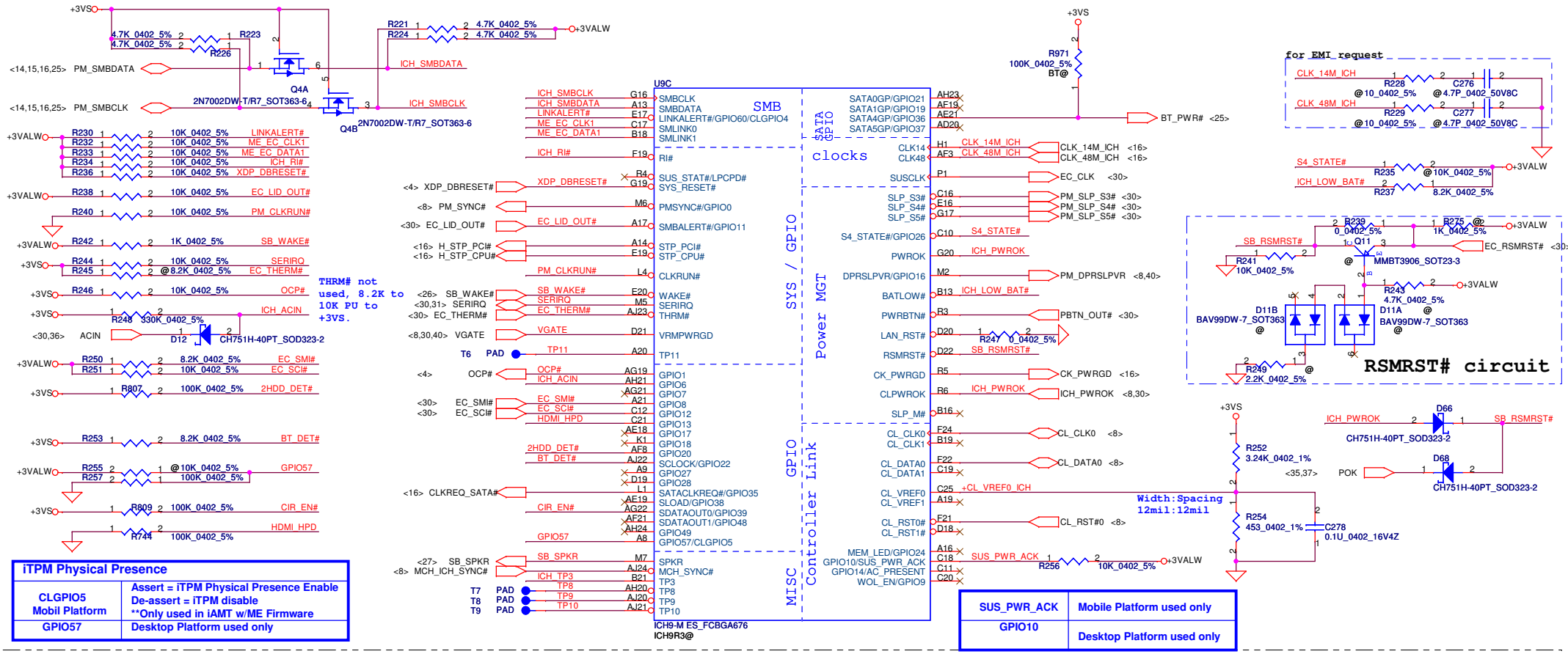
Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size	Document Number	Rev
	PWWAA LA6841P M/B	0.1

Date: Monday, August 16, 2010 Sheet 20 of 44



iTPM Physical Presence	
CLGPIO5 Mobil Platform	Assert = iTPM Physical Presence Enable De-assert = iTPM disable **Only used in iAMT w/ME Firmware
GPIO57	Desktop Platform used only

SUS_PWR_ACK	Mobile Platform used only
GPIO10	Desktop Platform used only

ICH9M Strap Pin

Internal TPM Strap(Internal pull-down)	
SPI_MOSI	Low= Disable High= iTPM enable by MCH strap*

No Reboot Strap (Internal pull-up)	
SB_SPKR	Low= *Default High= "No Reboot"

Boot BIOS Strap (Internal pull-up)		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	0	RESERVED
0	1	SPI
1	0	PCI
1	1	LPC* (Default)

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default* (Internal pull-up)

Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

XOR Chain Entrance Strap		
ICH_TP3 (Internal pull-up)	HDA_SDOUT (Internal pull-down)	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

Flash Descriptor Security Override Strap	
GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

DMI Termination Voltage	
GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)

Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

Compal Electronics, Inc.

Title: ICH9M(3/4)-USB,GPIO,PCIE

Size | Document Number: PWWAA LA6841P M/B | Rev: 0.1

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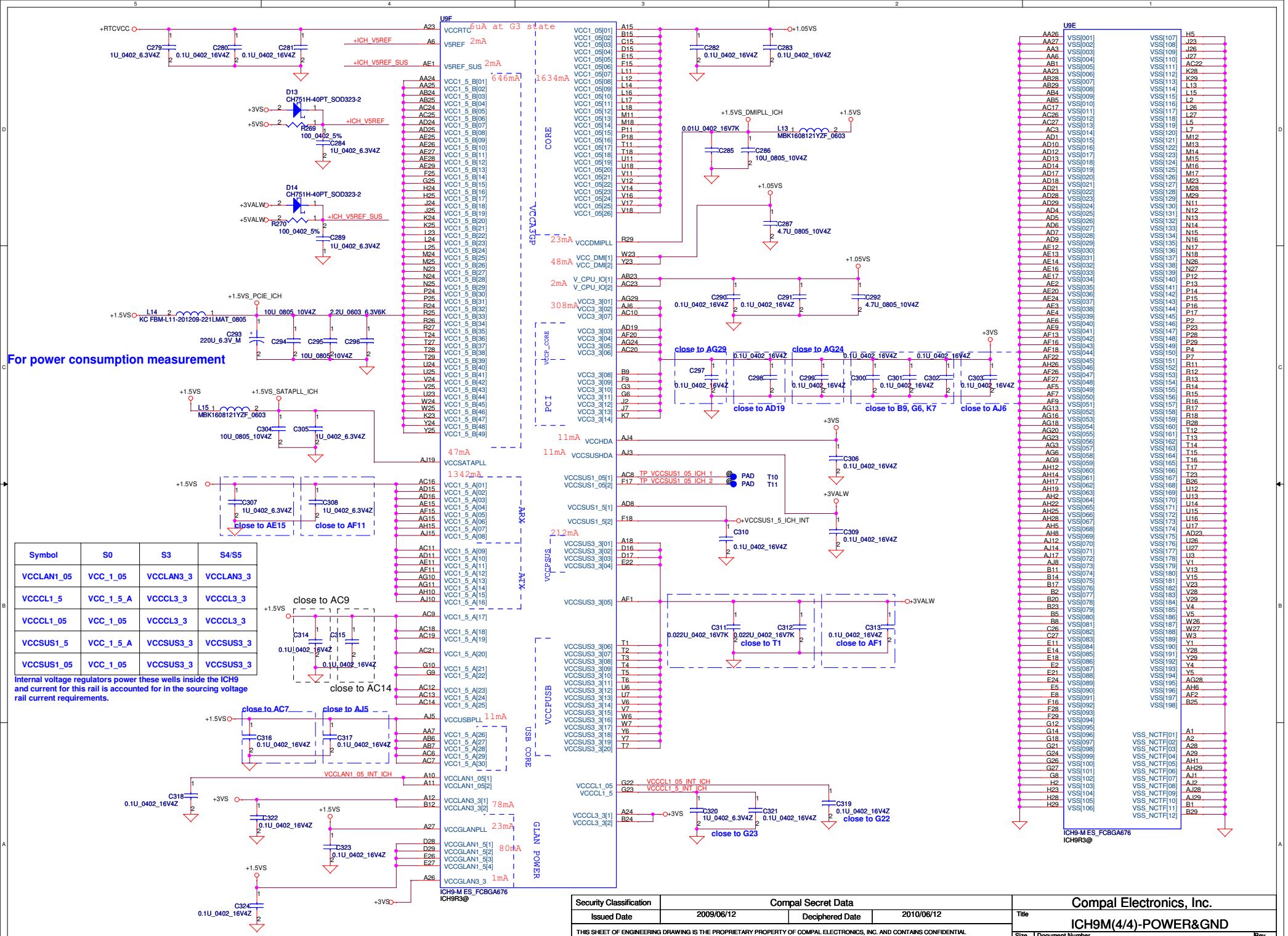

Symbol	S0	S3	S4/S5
VCCLAN1_05	VCC_1_05	VCCLAN3_3	VCCLAN3_3
VCCCL1_5	VCC_1_5_A	VCCCL3_3	VCCCL3_3
VCCCL1_05	VCC_1_05	VCCCL3_3	VCCCL3_3
VCCSUS1_5	VCC_1_5_A	VCCSUS3_3	VCCSUS3_3
VCCSUS1_05	VCC_1_05	VCCSUS3_3	VCCSUS3_3

Internal voltage regulators power these wells inside the ICH9 and current for this rail is accounted for in the sourcing voltage rail current requirements.

Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

Compal Electronics, Inc.

Title: ICH9M(4/4)-POWER&GND

Size: | Document Number: PWWAA LA6841P M/B | Rev: 0.1

Date: Monday, August 16, 2010 | Sheet 22 of 44

SATA HDD Conn.

Place closely JHDD SATA CONN.

+5VS 1.2A

C697 10U_0805_10V4Z
C698 0.1U_0402_16V4Z
C699 0.1U_0402_16V4Z
C700 0.1U_0402_16V4Z

JHDD

GND 1
A+ 2
A- 3
GND 4
B- 5
B+ 6
GND 7
V33 8
V33 9
V33 10
GND 11
GND 12
GND 13
V5 14
V5 15
V5 16
GND 17
Reserved 18
GND 19
V12 20
V12 21
V12 22
GND 23
GND 24

SATA_ITX_C_DRX_P1 C713 0.01U_0402_25V7K → SATA_ITX_DRX_P1 <20>
SATA_ITX_C_DRX_N1 C715 0.01U_0402_25V7K → SATA_ITX_DRX_N1 <20>
SATA_IRX_DTX_N1 C717 0.01U_0402_25V7K → SATA_IRX_C_DTX_N1 <20>
SATA_IRX_DTX_P1 C719 0.01U_0402_25V7K → SATA_IRX_C_DTX_P1 <20>

+3VS
+5VS

SANTA_191201-1
CONN@
this is temp. footprint

SATA ODD Conn

Place components close to ODD CONN.

+5VS 1.1A

C721 10U_0805_10V4Z
C722 10U_0805_10V4Z
C723 @ 1U_0402_6.3V4Z
C724 0.1U_0402_16V4Z
C725 0.1U_0402_16V4Z

JODD

GND 1
A+ 2
A- 3
GND 4
B- 5
B+ 6
GND 7
DP 8
+5V 9
+5V 10
MD 11
GND 12
GND 13
GND 14
GND 15

SATA_ITX_C_DRX_P4_ODD
SATA_ITX_C_DRX_N4_ODD
SATA_IRX_DTX_N4_ODD
SATA_IRX_DTX_P4_ODD
+5VS

SANTA_206401-1_RV
CONN@

SATA_ITX_C_DRX_P4_ODD C733 0.01U_0402_25V7K → SATA_ITX_DRX_P4 <20>
SATA_ITX_C_DRX_N4_ODD C734 0.01U_0402_25V7K → SATA_ITX_DRX_N4 <20>
SATA_IRX_DTX_N4_ODD C735 0.01U_0402_25V7K → SATA_IRX_C_DTX_N4 <20>
SATA_IRX_DTX_P4_ODD C736 0.01U_0402_25V7K → SATA_IRX_C_DTX_P4 <20>

W=60mils

+5VALW 1.4A +USB_VCCA

U42
GND OUT
IN OUT
IN OUT
EN# FLG

<30> USB_EN#
USB_OC#0 <19,30>

C693 1000P_0402_50V7K For EMI request
C752 4.7U_0805_10V4Z @

G528_SO8

USB Conn

+USB_VCCA

C84 220U_6.3V_M
C63 0.1U_0402_16V4Z
C64 1000P_0402_50V7K

W=60mils

<BOM Structure> 10K_0402_5%

@WCM2012F2SF-900T04_0805

<19> USB20_N0
<19> USB20_P0

L87

USB20_N0_R
USB20_P0_R

JUSB1 @

VCC GND
D- GND
D+ GND
GND GND

ALLTOP C107L8-10405-L

D65 @ PJDLC05_SOT23-3

<19> USB20_N1
<19> USB20_P1

L86

USB20_N1_R
USB20_P1_R

JUSB2 @

ALLTOP C107L8-10405-L

D62 @ PJDLC05_SOT23-3

C60 0.1U_0402_16V4Z
C61 1000P_0402_50V7K

W=60mils

Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

Compal Electronics, Inc.

Title: SATA-HDD/ODD/USB

Size | Document Number: PWWAA LA6841P M/B | Rev: 0.1

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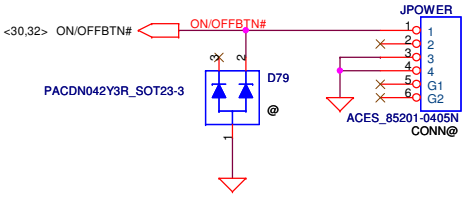
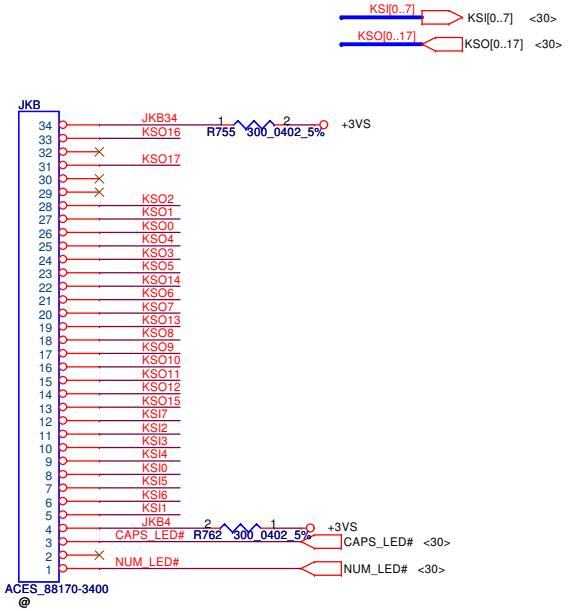
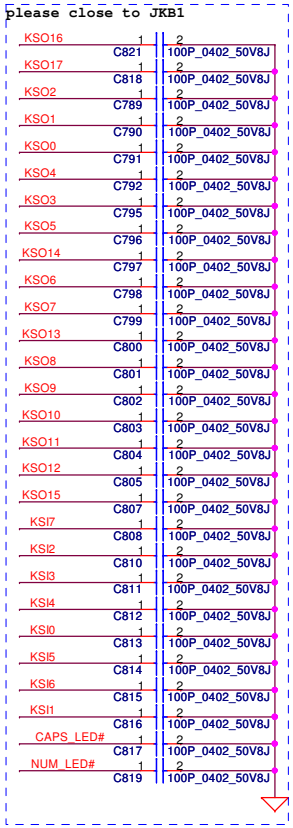
POWER/B Connector

Check footprint and pin define

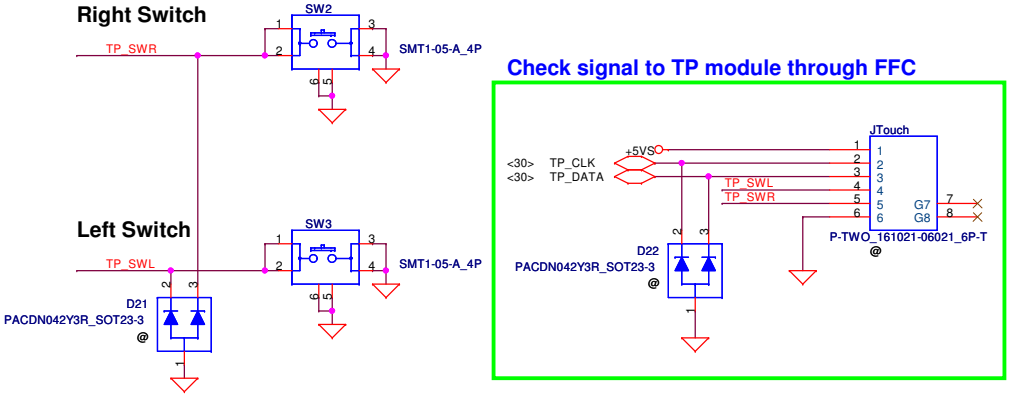


KEYBOARD CONN





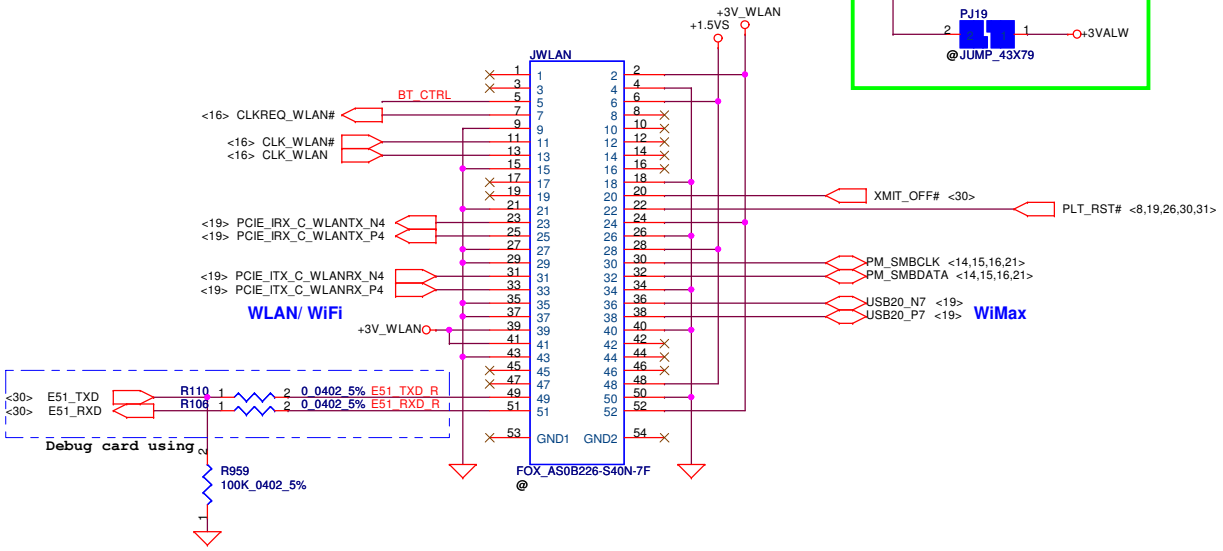
Touch/B Connector

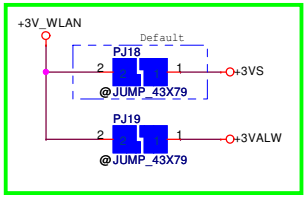


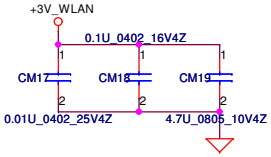
Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

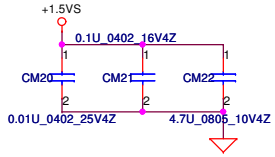
Compal Electronics, Inc.			
Title	USB/BT/FP/Int. Cam		
Size	Document Number	PWWAA LA6841P M/B	Rev 0.1
Date: Monday, August 16, 2010	Sheet 24 of 44		

PCIe Mini Card-WLAN/WiMax





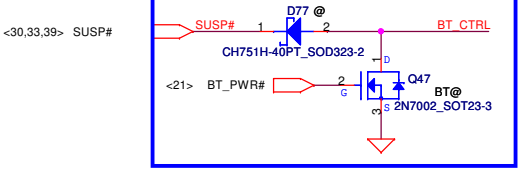




WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	H	L
BT_PWR#	L	H

**If +3V_WLAN is +3VS, please remove D77



<30,33,39> SUSP#

Add BT_CTRL for WLAN & BT Combo module at DVT

Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

Compal Electronics, Inc.

Title: PCIe-WLAN/HDDVD/NAND/NEW

Size	Document Number	Rev
	PWWAA LA6841P M/B	0.1

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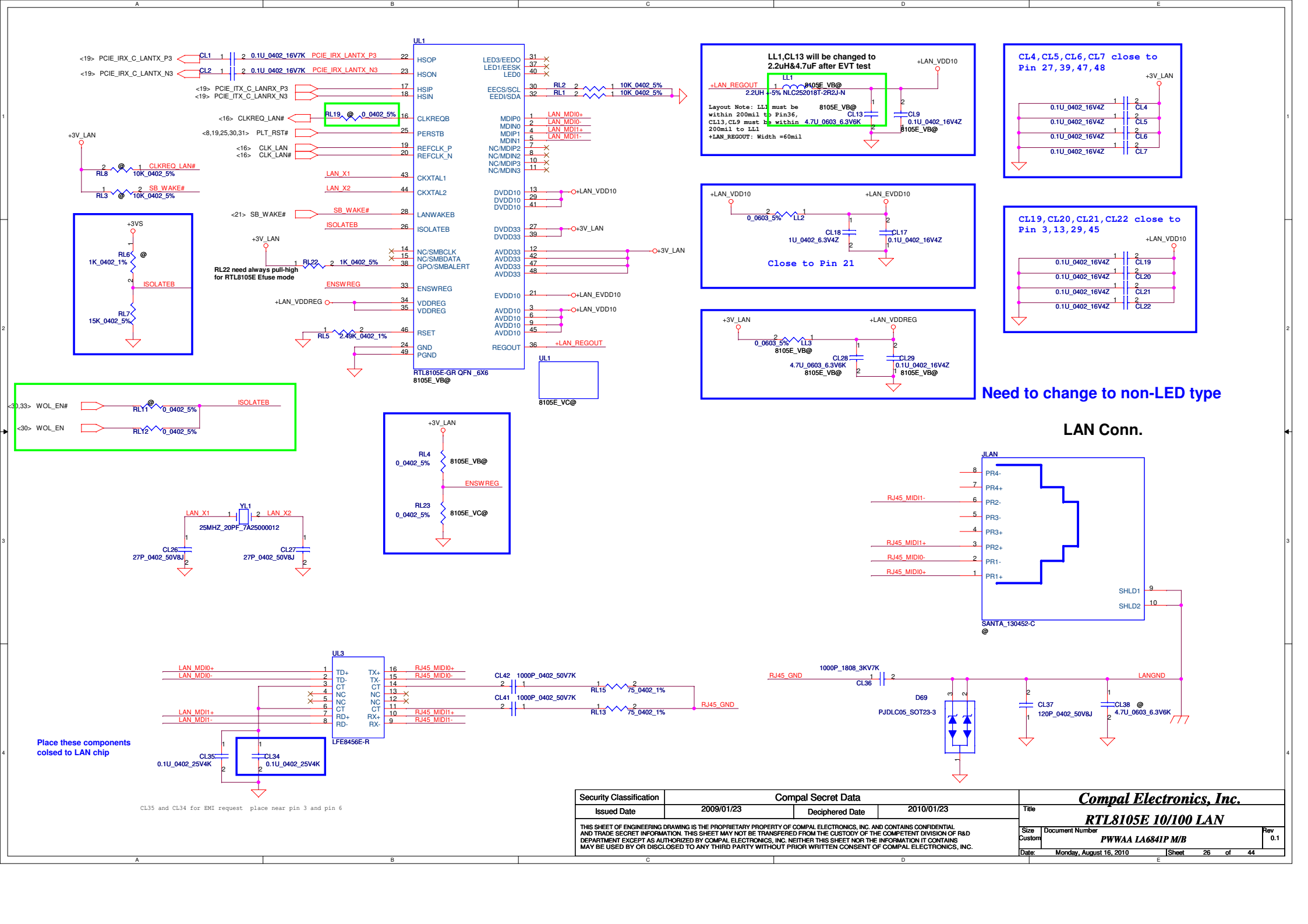
UL1
RTL8105E-GR QFN_6X6
8105E_VB@
8105E_VC@
LL1,CL13 will be changed to 2.2uH&4.7uF after EVT test
CL4,CL5,CL6,CL7 close to Pin 27,39,47,48
CL19,CL20,CL21,CL22 close to Pin 3,13,29,45
Close to Pin 21
RL22 need always pull-high for RTL8105E Efuse mode
Need to change to non-LED type
LAN Conn.
JLAN
SANTA_130452-C
@
YL1
25MHZ_20PF_7A25000012
UL3
LFE8456E-R
Place these components colsed to LAN chip
CL35 and CL34 for EMI request place near pin 3 and pin 6
Security Classification
Compal Secret Data
Issued Date
2009/01/23
Deciphered Date
2010/01/23
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Compal Electronics, Inc.
Title
RTL8105E 10/100 LAN
Size
Custom
Document Number
PWWAA LA6841P M/B
Rev
0.1
Date: Monday, August 16, 2010
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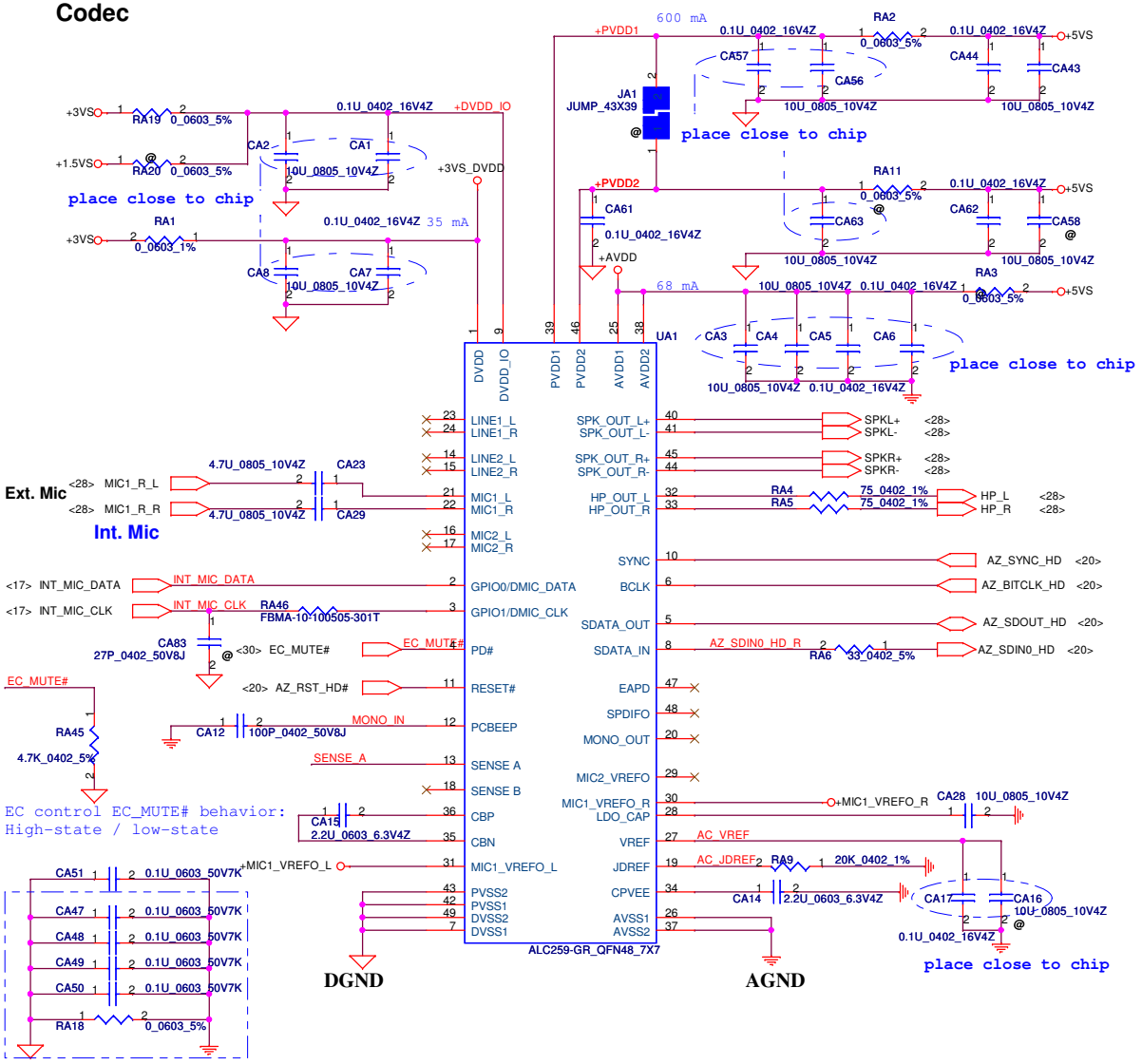
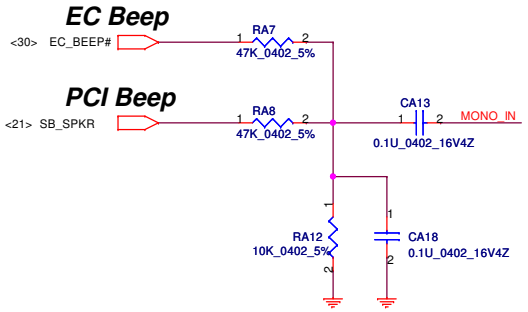
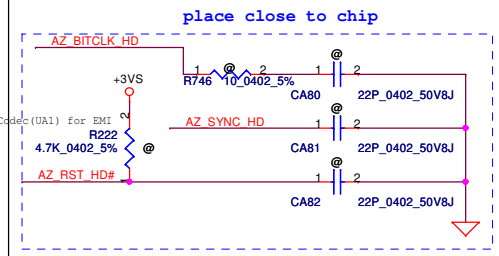
Codec

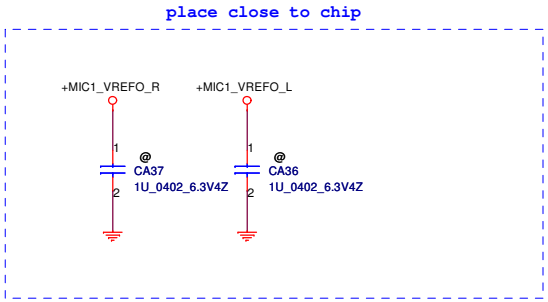


Beep sound

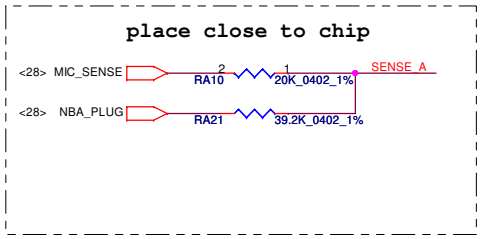


close to Audio Codec(UA1) for EMI





Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 20)	



Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

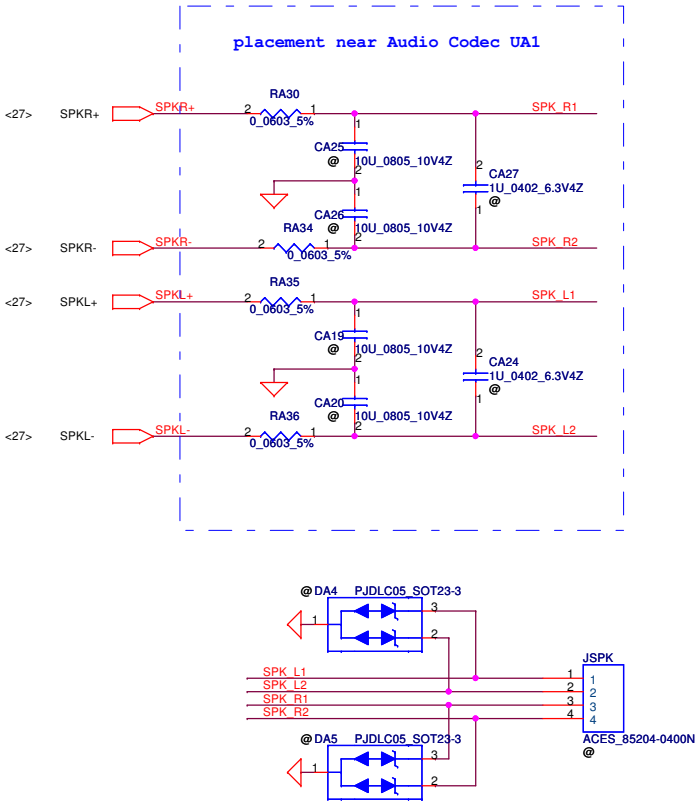
Compal Electronics, Inc.

Title: HD CODEC ALC272

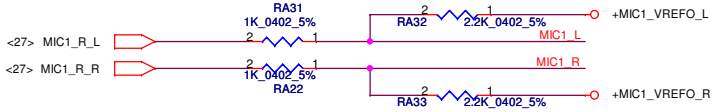
Size | Document Number: PWWAA LA6841P M/B | Rev: 0.1

Date: Monday, August 16, 2010 | Sheet 27 of 44

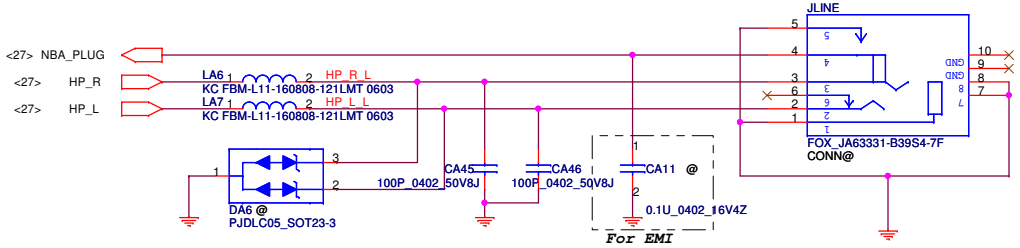
Speaker Connector



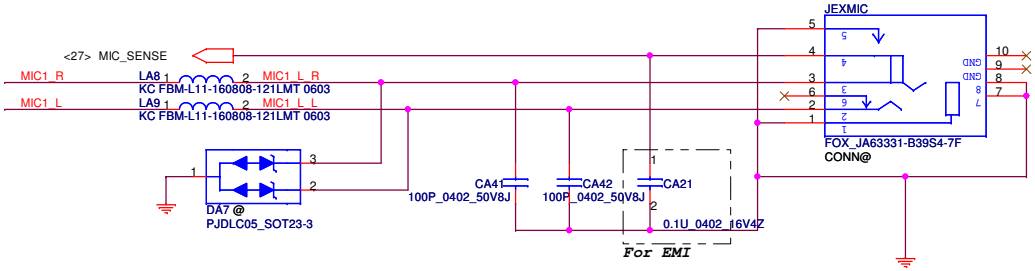
Ext. Mic



HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK



Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

Compal Electronics, Inc.

Title: AUDIO AMP/MIC/SPK/VR

Size	Document Number	Rev
	PWWAA LA6841P M/B	0.1

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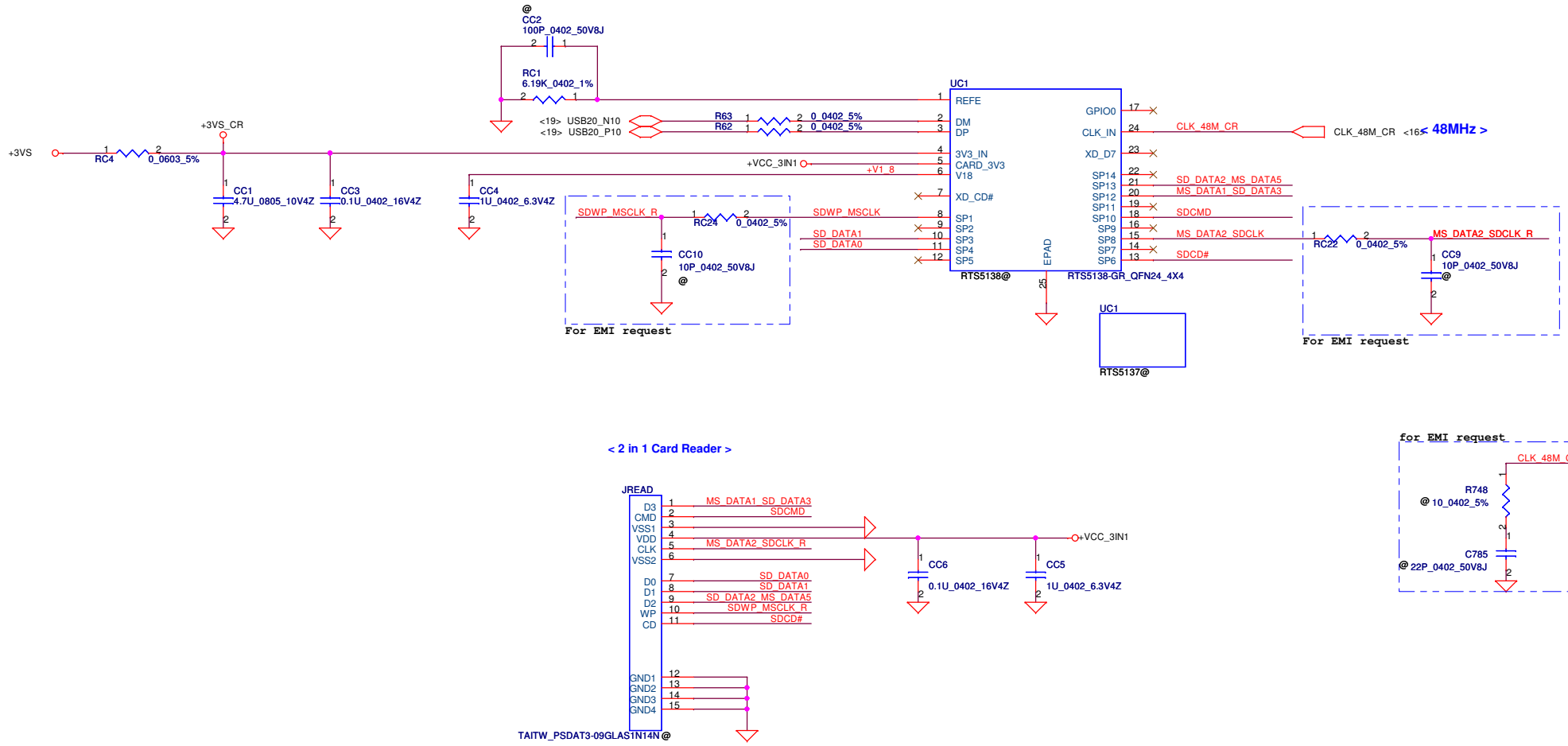

Security Classification	Compal Secret Data		
Issued Date	2009/10/01	Deciphered Date	2010/10/01

Compal Electronics, Inc.

Title: RTS5138 Card Reader

Size	Document Number	Rev
Custom	PWWAA LA6841P M/B	0.1

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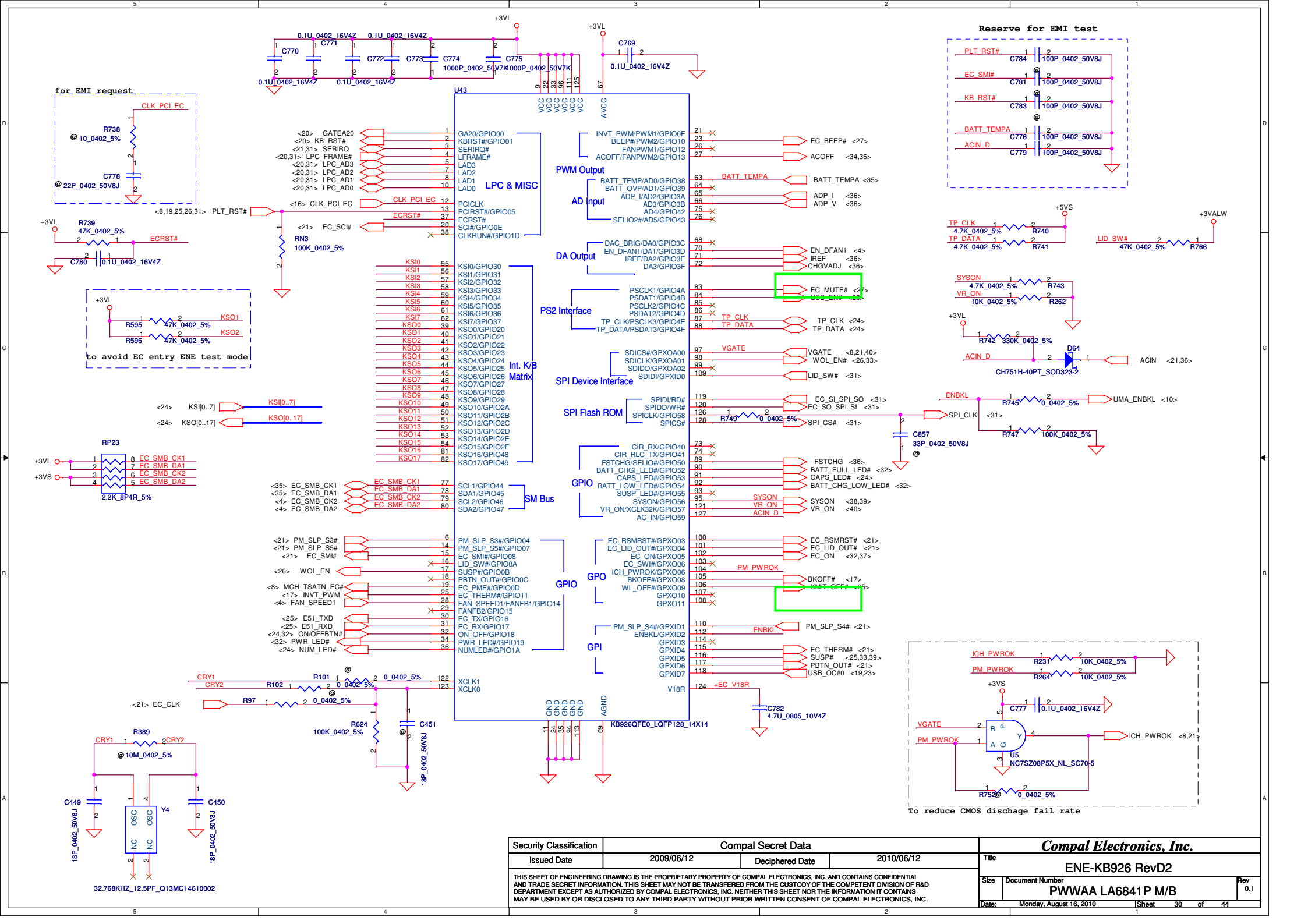
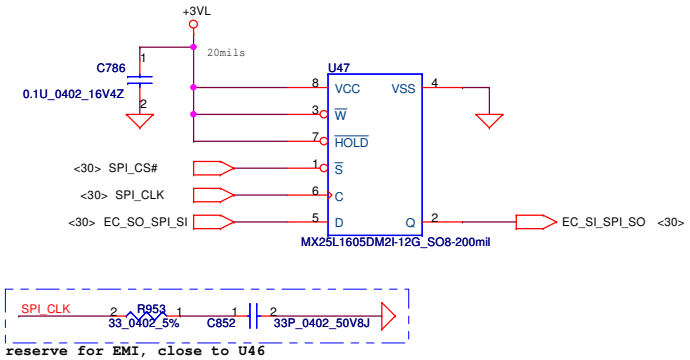


Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

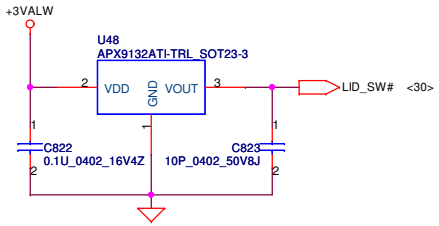
Compal Electronics, Inc.

Title	ENE-KB926 RevD2	
Size	Document Number: PWWAA LA6841P M/B	Rev: 0.1
Date: Monday, August 16, 2010	Sheet 30 of 44	

SPI Flash (16Mb*1)

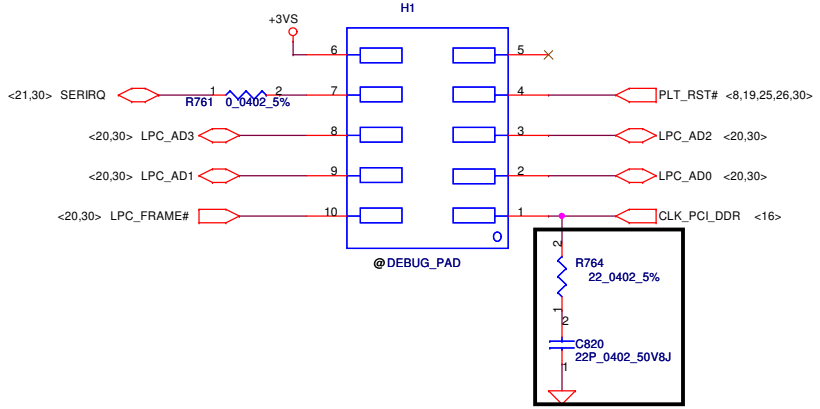


Lid SW

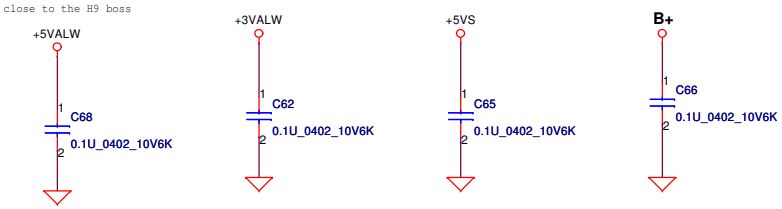


LPC Debug Port

Please place the PAD under DDR DIMM.



for EMI



Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

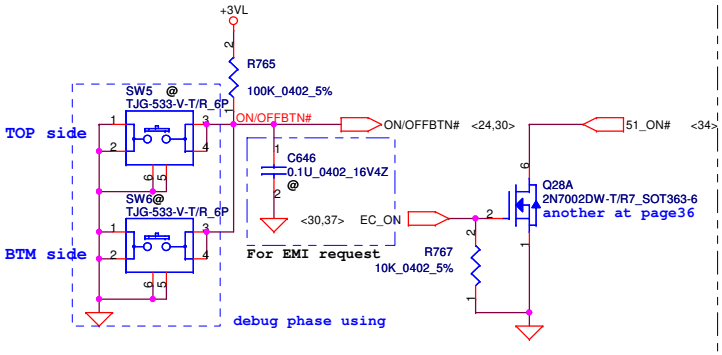
Compal Electronics, Inc.

Title: SPI ROM/TP/KB/Debug

Size	Document Number	Rev
	PWWAA LA6841P M/B	0.1

Date: Monday, August 16, 2010 Sheet 31 of 44

Power Button



ISPD

PCB

ZZZ

DAZ0HE00100

DC-IN

PJP1

PJP1

45@

NB_GL40_R3

U3

CANTIGA GL40

GL40R3@

NB_GL40_R1

U3

CANTIGA GL40

GL40R1@

NB_GM45_R1

U3

CANTIGA GM45

GM45R1@

SB_R1

U9

ICH9-M ES

ICH9R1@

DC-IN LED

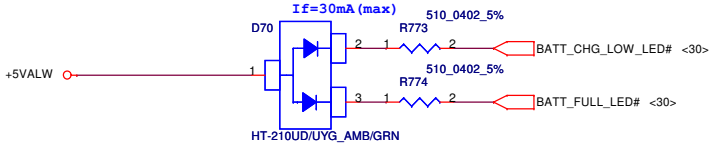
Vf=2.0V(typ),2.4V(max)
If=30mA(max)

footprint is SC510UYG000

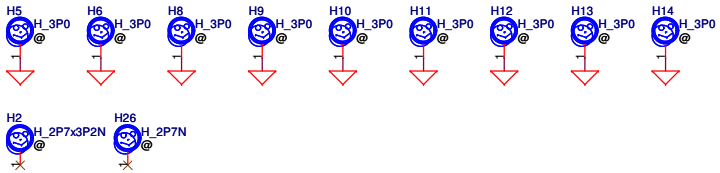
BATT CHARGE/FULL LED

Vf=1.9V(typ),2.4V(max) for amber
Vf=2.0V(typ),2.4V(max) for green
If=30mA(max)

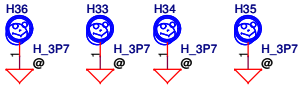
footprint is SC510UDG000



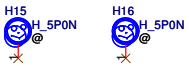
Screw Hole



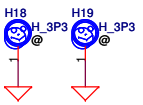
CPU



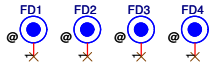
SB



MINI CARD



PCB Fedical Mark PAD



Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

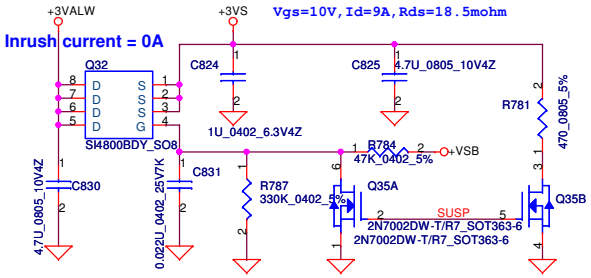
Compal Electronics, Inc.

Title: Comm. SW/ Sub Conn./LEDS

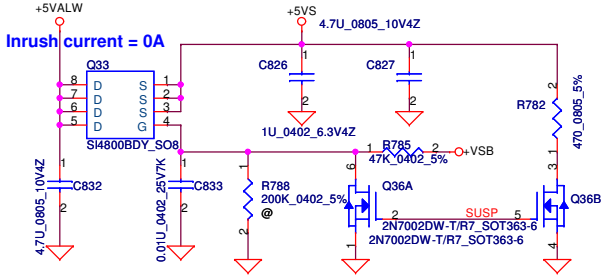
Size | Document Number: PWWAA LA6841P M/B | Rev: 0.1

Date: Monday, August 16, 2010 | Sheet 32 of 44

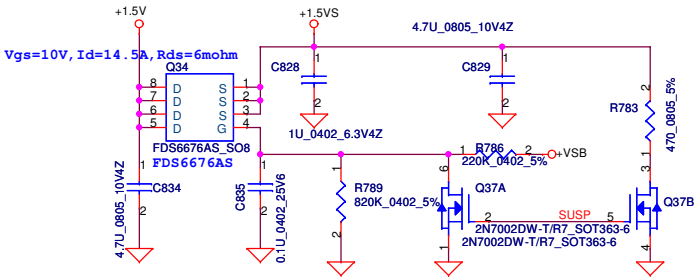
+3VALW TO +3VS



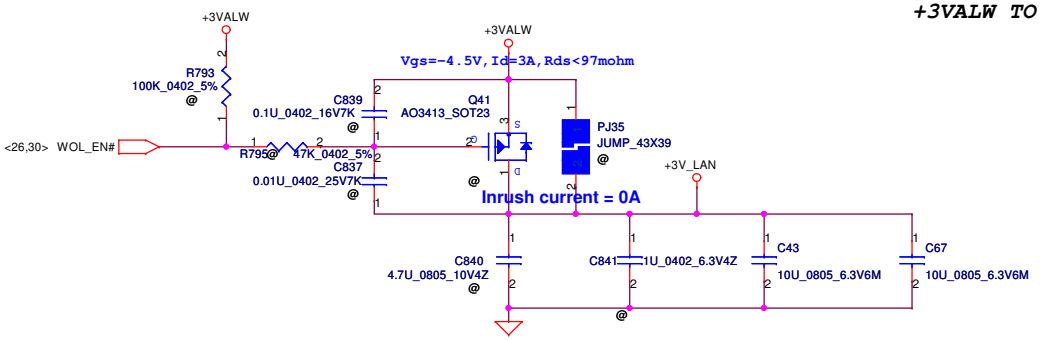
+5VALW TO +5VS



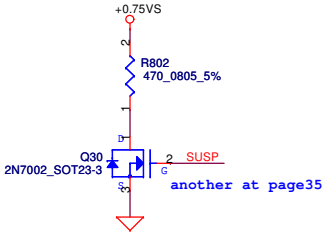
+1.5V to +1.5VS

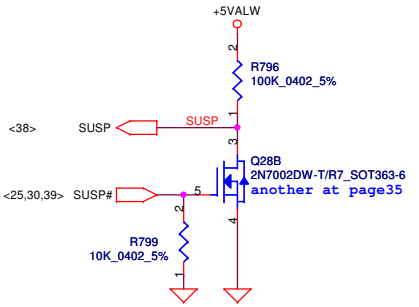


+3VALW TO +3V_LAN



+3VALW TO +3V_SB





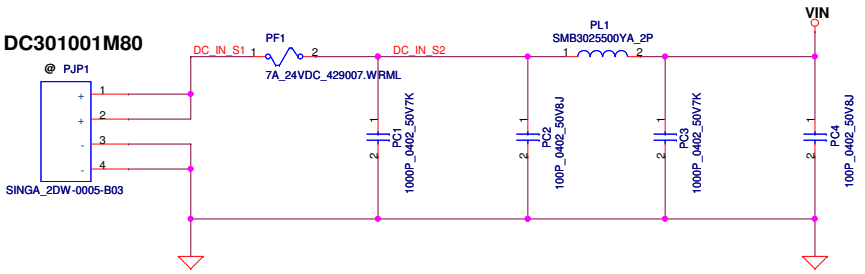
Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

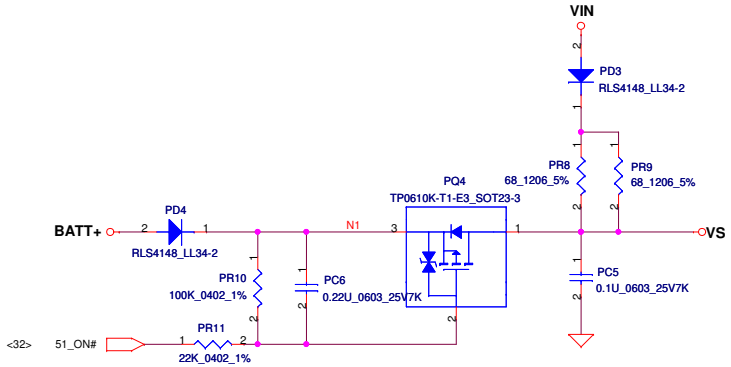
Compal Electronics, Inc.

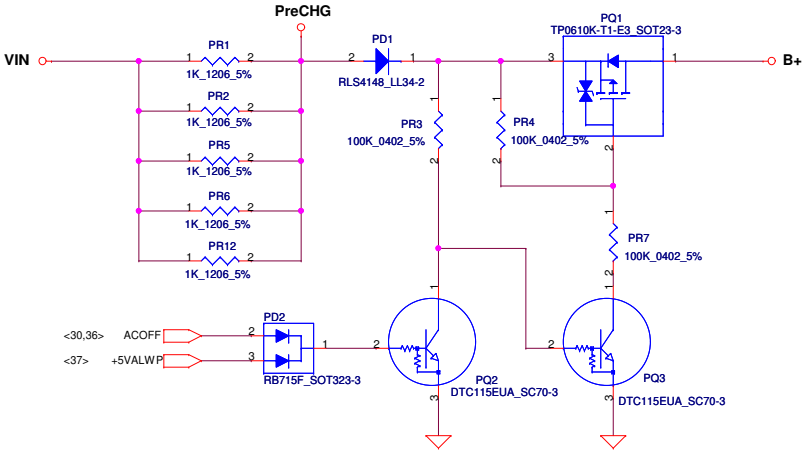
Title: DC-DC INTERFACE

Size | Document Number: PSWAA LA6511P M/B | Rev: 0.1

Date: Monday, August 16, 2010 | Sheet 33 of 44





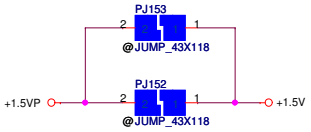


(100mA,40mils ,Via NO.= 2)

(5A,200mils ,Via NO.= 10)
OCP=7.7A

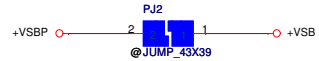
(0.98A,40mils ,Via NO.= 2)

(5A,200mils ,Via NO.= 10)
OCP=7.9A

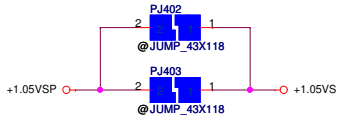


(7.5A,300mils ,Via NO.= 15)
OCP=8.87A

(1.46A,60mils ,Via NO.= 3)



(120mA,40mils ,Via NO.= 1)



(7.5A,300mils ,Via NO.=15)
OCP=8.41A

ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

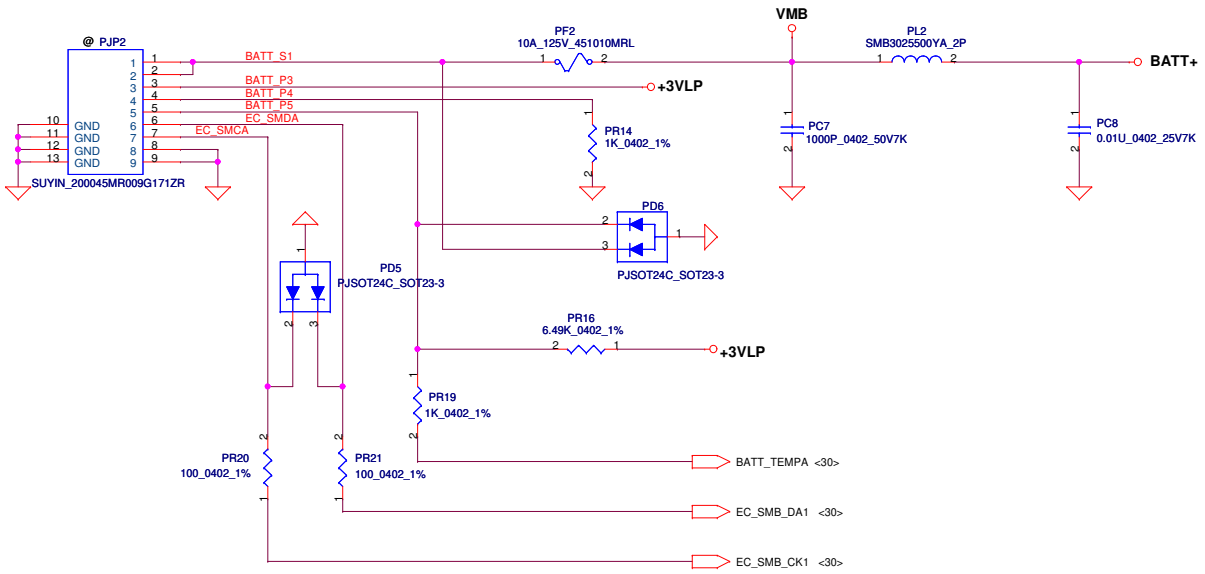
Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size | Document Number: KSWAA | Rev: 0.1

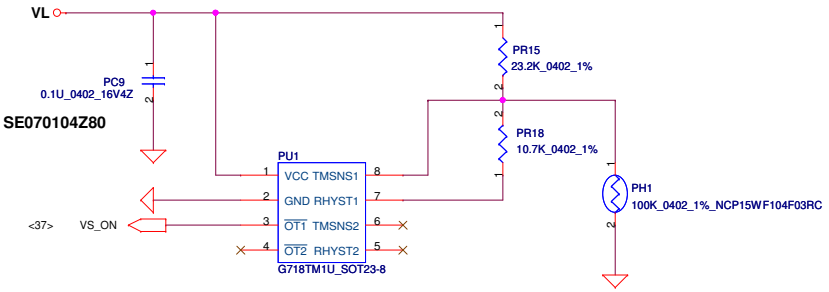
Date: Monday, August 16, 2010 | Sheet 34 of 44



PH1 under CPU botten side :

CPU thermal protection at 90 degree C

Recovery at 56 degree C



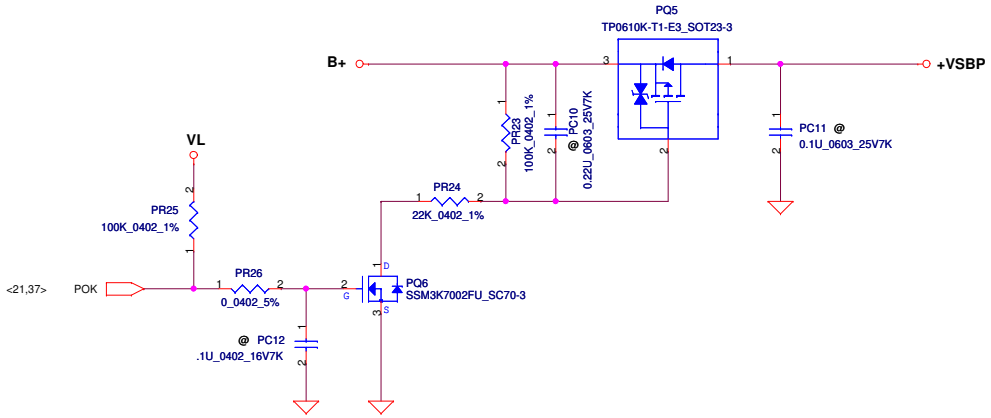
Rset = 3 * Rtmh

Rhyst = (Rset* Rtml) / (3*Rtml - Rset)

Rtmh at 90C = 7.79K, Rtml at 56C = 26.1K

Rset = 3 * 7.79K = 23.37K ==> 23.2K

Rhyst = (23.2K * 26.1K) / (3 * 26.1K - 23.2K) = 10.99K ==> 10.7K



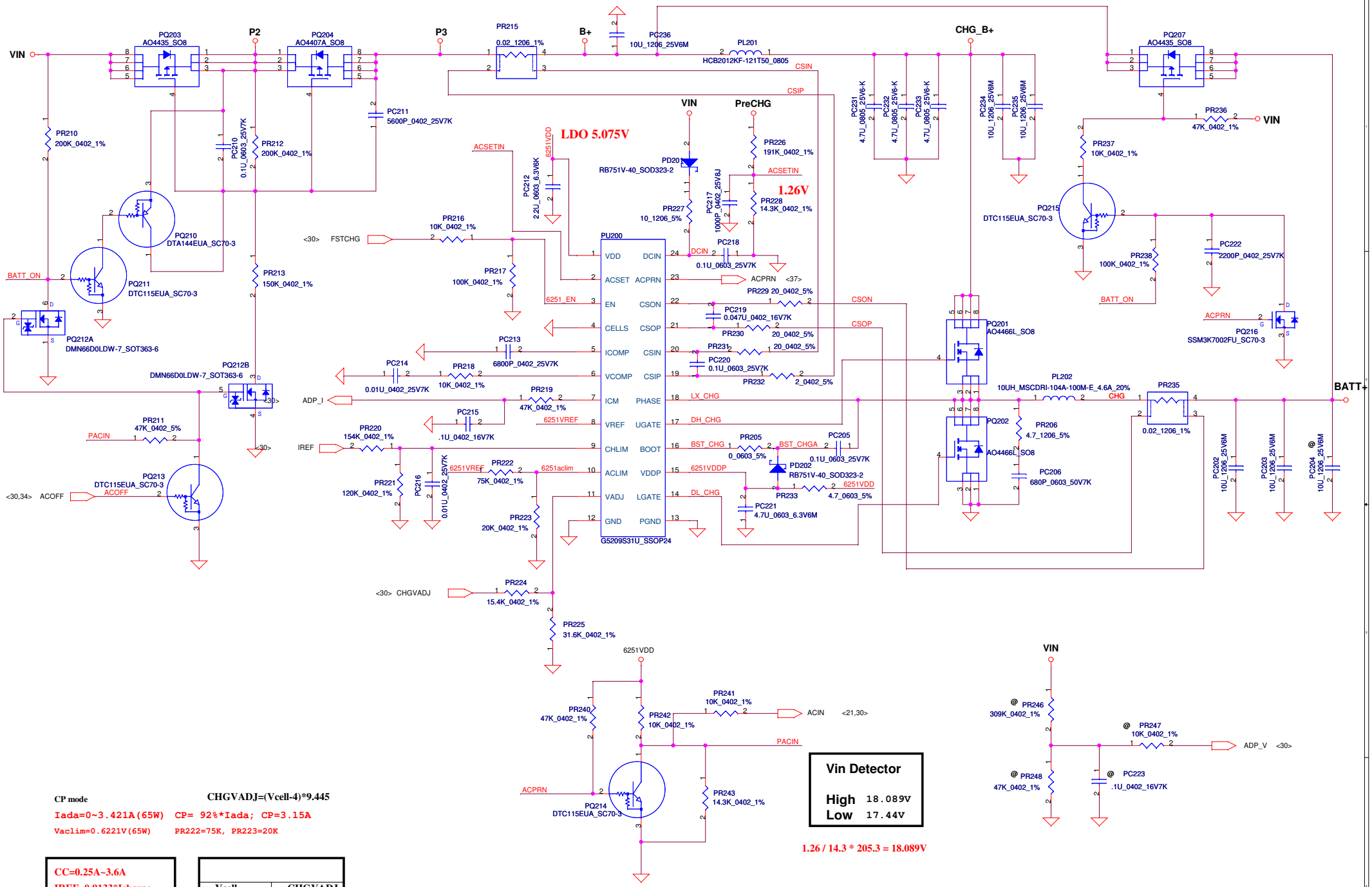
Security Classification	Compal Secret Data		
Issued Date	2008/10/09	Deciphered Date	2009/10/09

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
	KSWAA	0.1

Date: Monday, August 16, 2010 | Sheet 35 of 44



CP mode

Iada=0~3.421A(65W) CP= 92%*Iada; CP=3.15A

Vaclim=0.6221V(65W) PR222=75K, PR223=20K

CHGVADJ=(Vcell-4)*9.445

Vcell	CHGVADJ
4V	0V
4.2V	1.889V
4.35V	3.30575V

CC=0.25A~3.6A
IREF=0.9133*Icharge
IREF=0.228V~3.29V
VCHLIM need over 95mV

Vin Detector

High 18.089V
Low 17.44V

1.26 / 14.3 * 205.3 = 18.089V

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

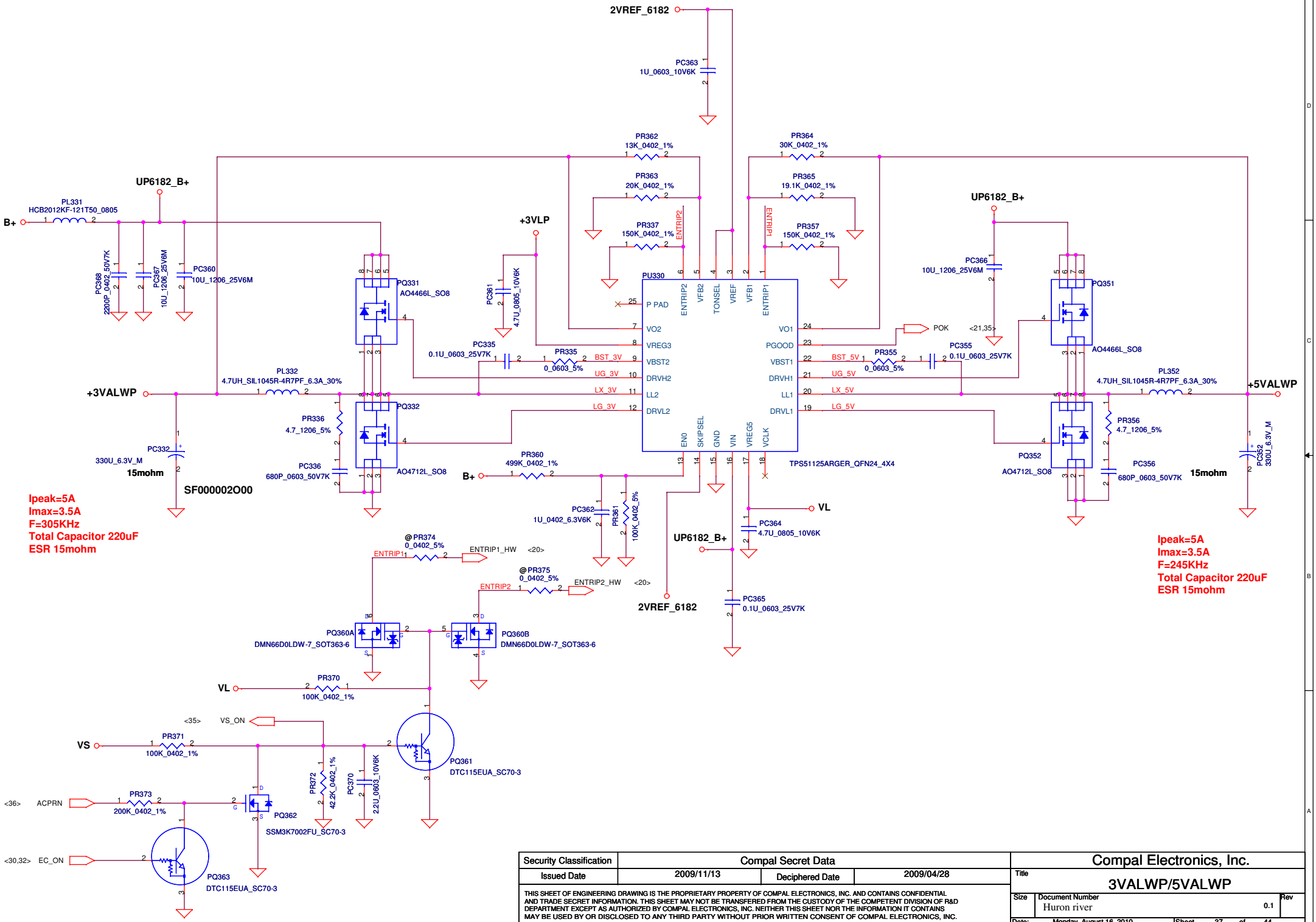
Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number | Rev: 0.1

Date: Monday, August 16, 2010 | Sheet 36 of 44

Huron river



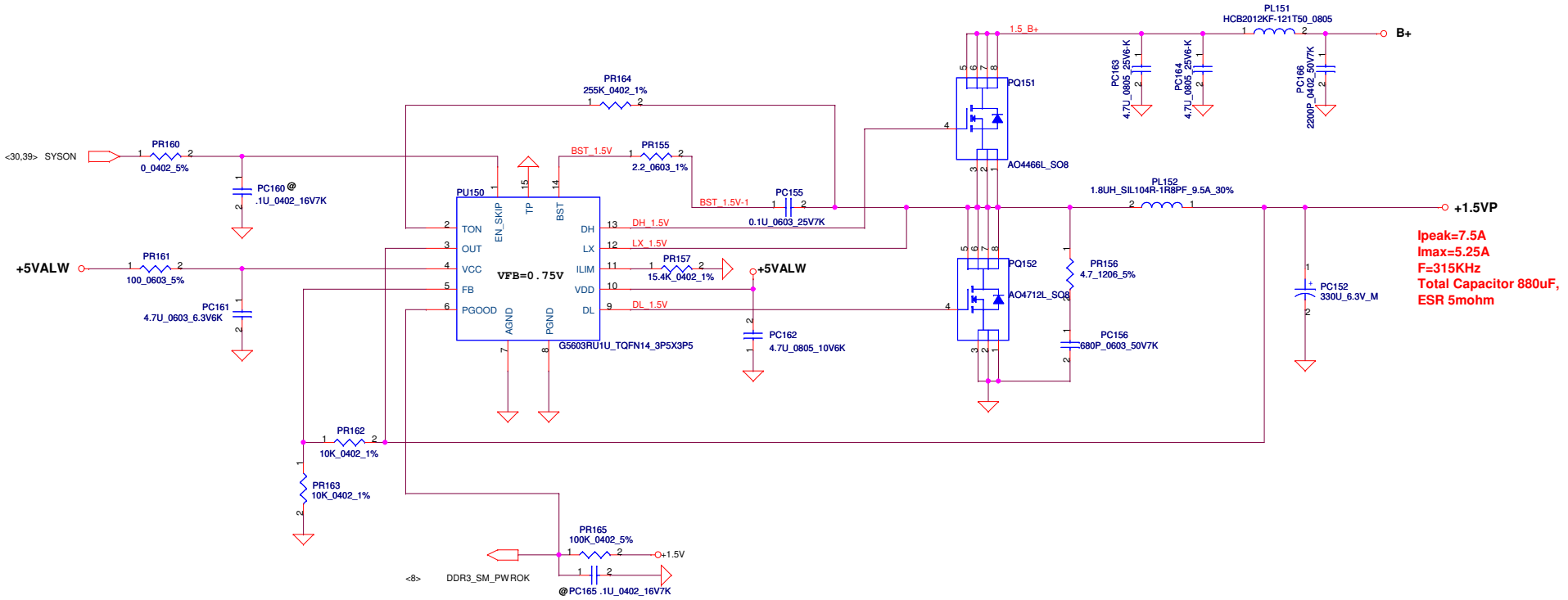
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2009/04/28

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size | Document Number: Huron river | Rev: 0.1

Date: Monday, August 16, 2010 | Sheet 37 of 44



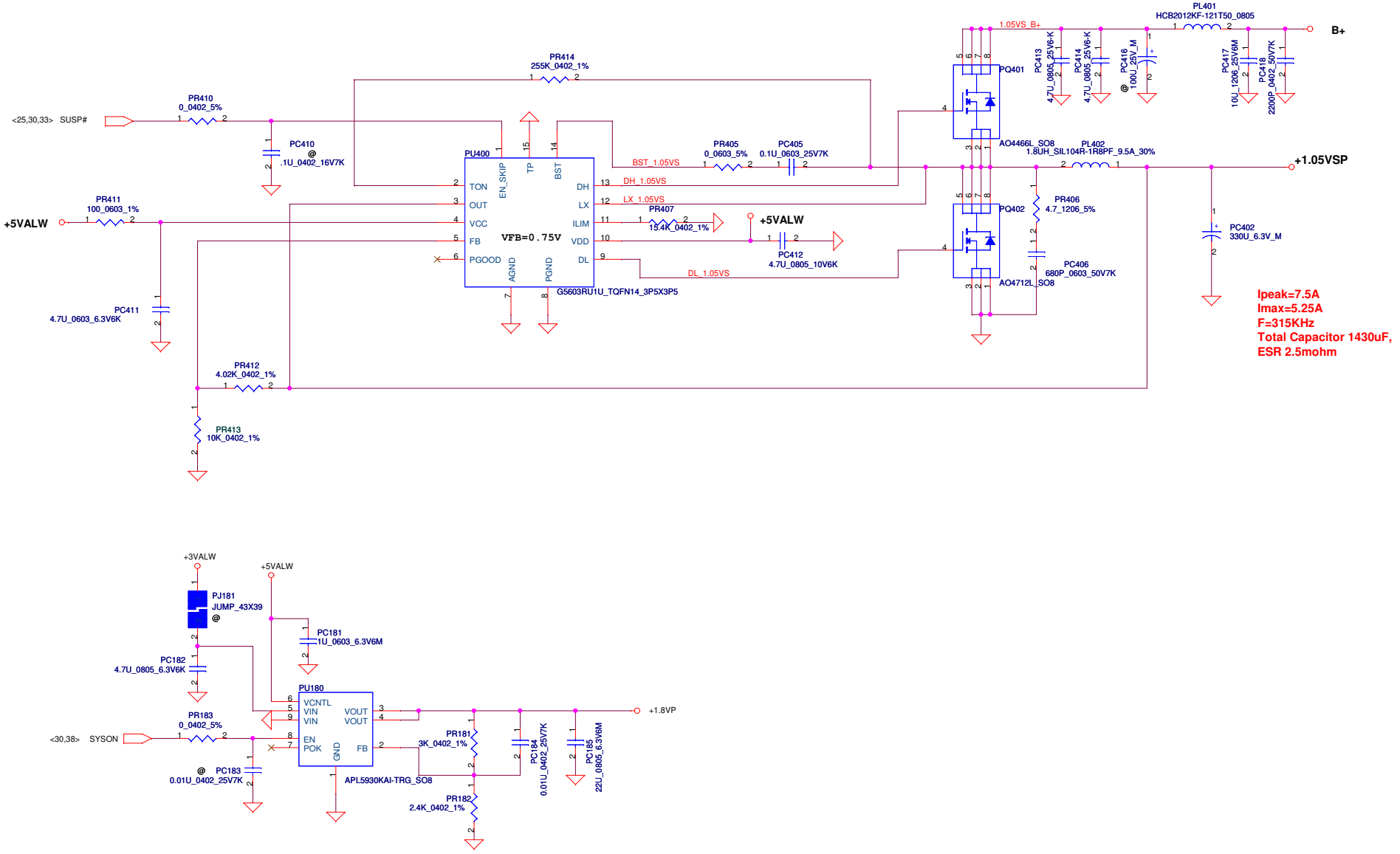
Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

Compal Electronics, Inc.

Title: 1.8V / 1.5V / 0.75V

Size	Document Number	Rev
	KSWAA	0.1

Date: Monday, August 16, 2010 | Sheet 38 of 44



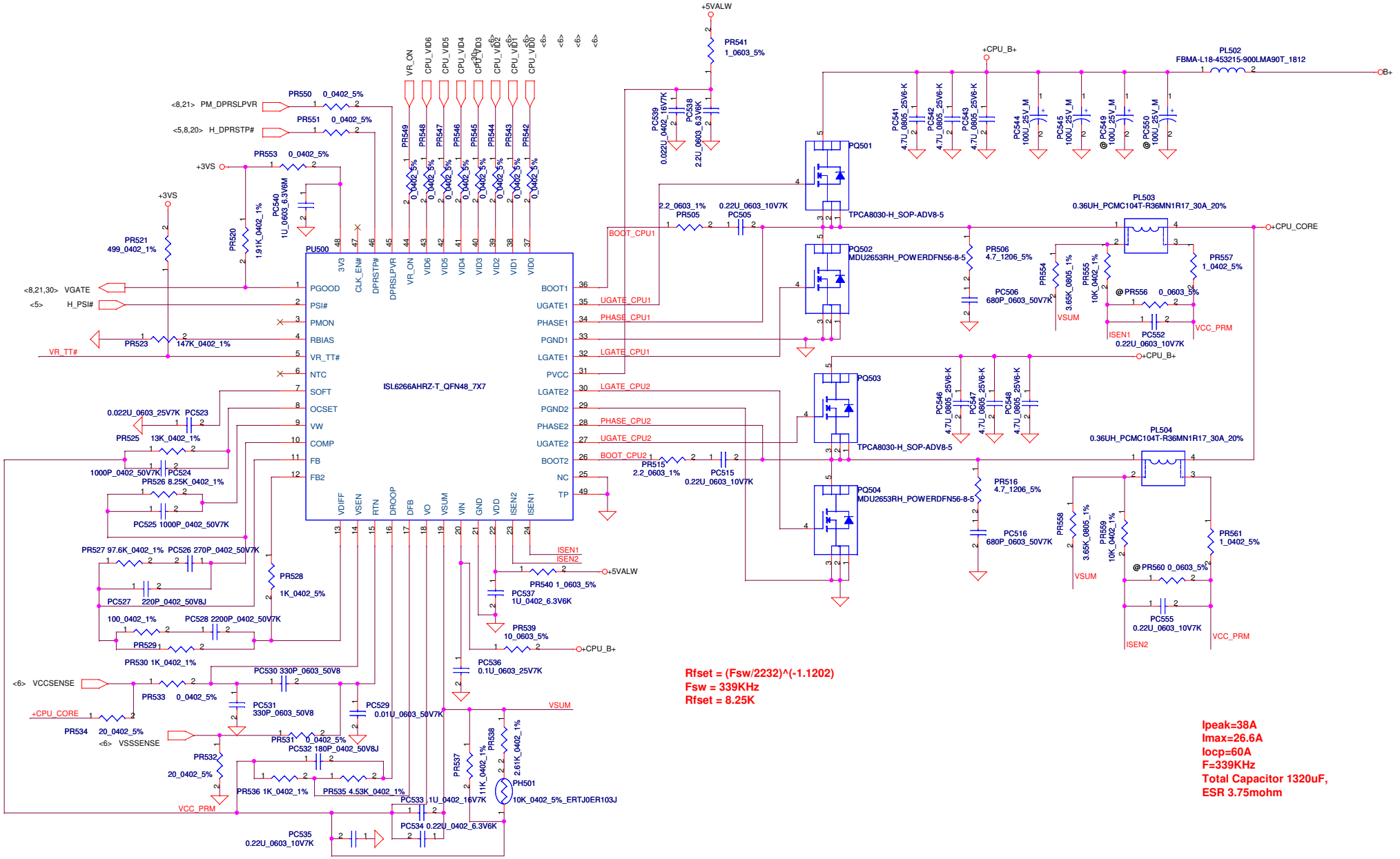
Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

Compal Electronics, Inc.

Title: 1.05V / 1.8V

Size	Document Number	Rev
	KSWAA	0.1

Date: Monday, August 16, 2010 | Sheet 39 of 44



Security Classification	Compal Secret Data		
Issued Date	2007/11/12	Deciphered Date	2008/11/12

Compal Electronics, Inc.

Title: +CPU_CORE

Size	Document Number	Rev
Custom	KSWAA	0.1

Date: Monday, August 16, 2010 | Sheet 40 of 44

PIR (Product Improve Record)

REVISION CHANGE: 0.1 TO 0.2 PVT

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	07/23	32	Change R768,R773 from 120 ohm to 510 ohm	for changed 5mA LED
2.	07/23	32	Chage LED power rail from +3valw to +5valw	for changed 5mA LED
3.	07/23	23	del. L86,L87 EMI component	for EMI request
4.	07/23	31	Add 1PCS(C62) 0.1uF_0402 on +3Valw-->GND	for EMI request
5.	07/23	31	Add 1PCS(C65) 0.1uF_0402 on +5Vs-->GND	for EMI request
6.	07/23	31	Add 0.1uF_0402(C66) on B+-->GND close to H8	for EMI request
7.	07/23	28	JLINE and JEXMIC change from DC2300006300 to DC230004L00	for SMT DFx request
8.	07/27	30	change R742 from +3VALW to +3VL	for LED no function issue
9.	07/27	8	add test pad ON U3.E36,U3.AK34	for ATE request
10.	07/27	33	change part number of Q30 (SB770020010)	for Reduce BOM part type
11.	07/27	32	Change D67(power on LED) from SC510UYG000 to SC500009D00	for changed 5mA LED
12.	07/27	32	Change D70(DC in LED) from SC510UDG000 to SC500009800	for changed 5mA LED
13.	07/29	14	un-mount CD7,CD8,CD9,CD10,CD11,CD12,CD30,CD31,CD32,CD34,and mount(22uF) CD29,CD33	for design change
14.	07/29	11	For +1.5V ,C78 from 330uF to 390u (SF000002O00)	for design change
15.	07/29	12	Change R82 and R81 from inductor to Bead	for design change
16.	07/29	15	+0.75VS filter un-mount CD22 and CD44	for design change
17.	08/03	25	un-mount D77	for If +3V_WLAN is +3VS, please un-mount D77

Compal Electronics, Inc.		
Title: PIR		
Size	Document Number: PWWAA LA6841P M/B	Rev: 0.1
Date: Monday, August 16, 2010	Sheet 41 of 44	

PIR (Product Improve Record)

REVISION CHANGE: 0.2 TO 0.3 Pre-MP

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	08/09	29	Change net V1_8 to +v1_8	for power trace
2.	08/09	32	add R774	for LED control
3.	08/12	32	un-mount SW5 and SW6	for Pre-MP do need power SW
4.	08/12	20	add R16 (for RTC battery)	for design change
5.	08/13	26	add D69 and un-mount CL38	for EMI request
6.	08/13	26	CL37 from 0.1uF to 120pF	for EMI request
7.	08/13	26	add CL35	for EMI request
8.	08/13	27	add CA51	for EMI request
9.	08/13	33	add C67 and C43	for EMI request

Compal Electronics, Inc.

Title: PIR

Size | Document Number: PWWAA LA6841P M/B | Rev: 0.1

Date: Monday, August 16, 2010 | Sheet 42 of 44

PIR (Product Improve Record)

REVISION CHANGE: 0.1 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE

Compal Electronics, Inc.

Title	PIR		
Size	Document Number		Rev
	PWWAA LA6841P M/B		0.1
Date: Monday, August 16, 2010		Sheet 43 of 44	

Version Change List (P. I. R. List) for Power Circuit

Page #	Item Title	Solution Description
PVT : modification from EVT		
P35	mount ESD diode	mount PD5, PD6
P36	EMI request	add PC236 10uF
P37	EMI request	add PC367 10uF, PC368 2200pF
P37	change 3/5V IC main source	change PU330 to UP6182
P38	EMI request	add PC166 2200pF
P39	EMI request	add PC417 10uF, PC418 2200pF
P40	adjust loadine	change PR535 to 3.09K
P34	unify source	change PD1 to SC11N414880
P36	unify source	change PQ216 to SB000009610
P37	unify source	change PQ362 to SB000009610
P40	unify source	change PL502 to SM010020720
P40	turn on speed too quick	change PQ502, PQ504 to MDU2653RH
P37	change cap to 330uF with same price	change PC332, PC352 to SF000002000
P38	change cap to 330uF with same price	change PC152 to SF000002000
P39	change cap to 330uF with same price	change PC402 to SF000002000
P36	EMI request to mount snubber circuit, ISN caps	add PR206, PC206; PC234, PC235
P37	EMI request to mount snubber circuit	add PR336, PC336; PR356, PC356
P38	EMI request to mount snubber circuit & boost resistor	add PR156, PC156; change PR155 to 2.2ohm
P39	EMI request to mount snubber circuit	add PR406, PC406
P40	EMI request to mount snubber circuit	add PR506, PC506; PR516, PC516
PreMP : modification from PVT		
P34	increase precharge design margin	add PR12 1K
P35	change OTP setting	change PR15 to 23.2K, PR18 to 10.7K
P35	change source	chagne PC9 to SE070104Z80
P37	change 3/5V IC main source	change PU330 to TPS51125A
P38	change 0.75V IC main source	change PU75 to G2992
P40	adjust loadine	change PR535 to 4.53K
P40	adjust transient stability	change PR527 to 220pF