COMPAL CONFIDENTIAL

MODEL NAME : CDP70

PCB NO : LA-E141P

BOM P/N :

GPIO MAP: Dell GPIO map EC16 062416 Compal Only

Breckenridge 14 UMA

Kabylake H

2016-07-01

REV : 0.2 (X01)

@ : Nopop Component

EMI@ : EMI Component

@EMI@ : EMI Nopop Component

ESD@ : ESD Component

@ESD@ : ESD Nopop Component

RF@ : RF Component

@RF@ : RF Nopop Component

XDP@ : XDP Component

CONN@ : Connector Component

MB PCB

Part Number	Description
DAB0001R000	PCB 1SC LA-E141P REV0 MB UMA 1

Layout Dell logo

REV: X01
PWB: K6NHT

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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

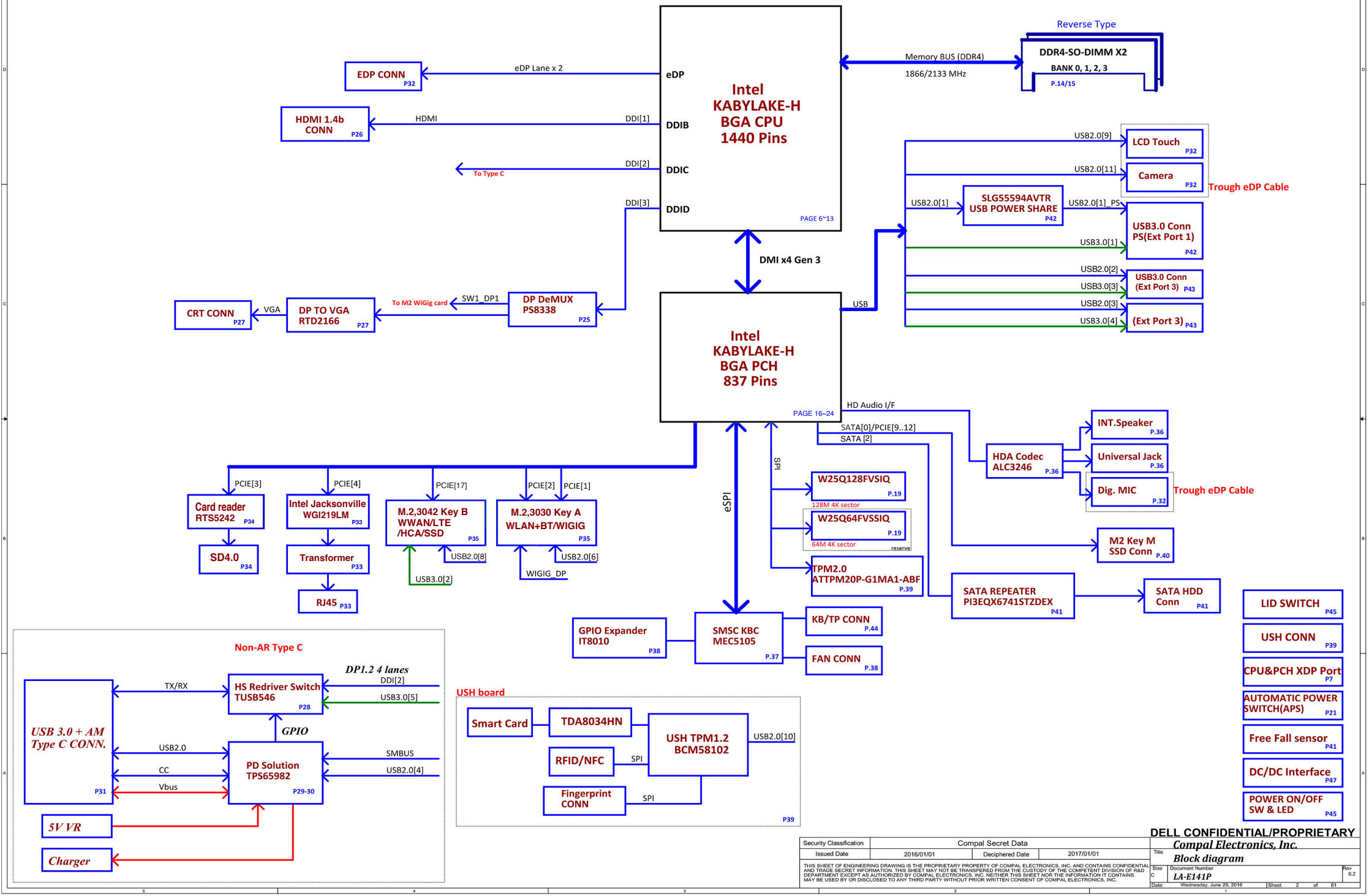
Compal Electronics, Inc.

Title: Cover Sheet

Size: A | Document Number: LA-E141P | Rev: 0.2

Date: Friday, July 01, 2016 | Sheet 1 of 61

Breckenridge 14 UMA non-TBT Block Diagram



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Title	Compal Electronics, Inc.		
	Block diagram		
Size C	Document Number LA-E141P		Rev 0.2
Date: Wednesday, June 29, 2016	Sheet 2 of 61		

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane			
	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_SUS +1.2V_MEM +1.0V_VCCST +2.5V_MEM	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.2V_RUN +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA +1.8V_RUN
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

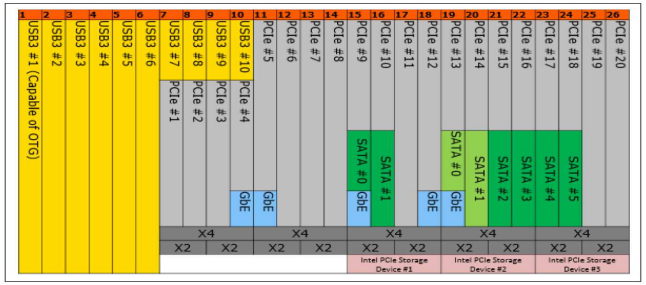
USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB3-->Rear
USB3.0-2	SSIC-1			JNGFF2-->M2 3042(LTE)
USB3.0-3	SSIC-2			JUSB1-->Right
USB3.0-4				JUSB2-->Left
USB3.0-5				NA
USB3.0-6				NA
USB3.0-7		PCIE-1		JNGFF1-->M.2 3030(WIGIG)
USB3.0-8		PCIE-2		JNGFF1-->M.2 3030(WLAN)
USB3.0-9		PCIE-3		Card Reader
USB3.0-10		PCIE-4		LOM
		PCIE-5		NA
		PCIE-6		
		PCIE-7		
		PCIE-8		
		PCIE-9	SATA-0A	M.2 Socket 3 (Key M) M.2 2280 SSD (PCIex4 or SATA)
		PCIE-10	SATA-1A	
		PCIE-11		
		PCIE-12		
		PCIE-13	SATA-0B	NA
		PCIE-14	SATA-1B	NA
		PCIE-15	SATA-2	JSATA1-->HDD SATA
		PCIE-16	SATA-3	NA
		PCIE-17	SATA-4	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-18	SATA-5	NA
		PCIE-19		NA
		PCIE-20		NA

USB PORT#	DESTINATION
1	JUSB3-->Rear
2	JUSB1-->Right
3	JUSB2 ->Left
4	Type C
5	NA
6	JNGFF1--> M.2 3030(BT)
7	NA
8	JNGFF2-->M2 3042(WWAN)
9	JEDP1-->Touch Screen
10	JUSH1-->USH
11	JEDP1-->Camera
12	NA

USH	H	BIO

VIDEO		DESTINATION
eDP		LCD
DDI-B		JHDMI1
DDI-C		Type-C
DDI-D	DeMux 1	M.2 3030 (WiGig)
		MB VGA

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	Material: TU662	0.50
			Add Plating		
1	Top		Copper foil	0.5oz+plating	1.80
		3.7	Prepreg	1080	3.15
2	GND/VCC		Copper foil	0.5 oz	0.60
		3.7	Core	3mil	3.00
3	IN 1		Copper foil	0.5 oz	0.60
		3.7	Prepreg	2116	3.8
4	IN 2		Copper foil	0.5 oz	0.60
		3.7	core	3mil	3.00
5	GND/VCC		Copper foil	0.5 oz	0.60
		3.7	Prepreg	1080	2.70
6	IN 3		Copper foil	0.5 oz	0.60
		3.8	core	4mil	4
7	IN 4		Copper foil	0.5 oz	0.60
		3.7	Prepreg	1080	2.70
8	GND/VCC		Copper foil	0.5 oz	0.60
		3.7	core	3mil	3.00
9	IN 5		Copper foil	0.5 oz	0.60
		3.7	Prepreg	2116	3.8
10	IN 6		Copper foil	0.5 oz	0.60
		3.7	Core	3mil	3.00
11	GND/VCC		Copper foil	0.5 oz	0.60
		3.7	Prepreg	1080	3.15
12	Bottom		Copper foil	0.5oz+plating	1.80
			Add Plating		
			SolderMask		0.50
Overall Thickness (1.2mm ± 10%)					46.90
					1.19129



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Title: Port Assignment

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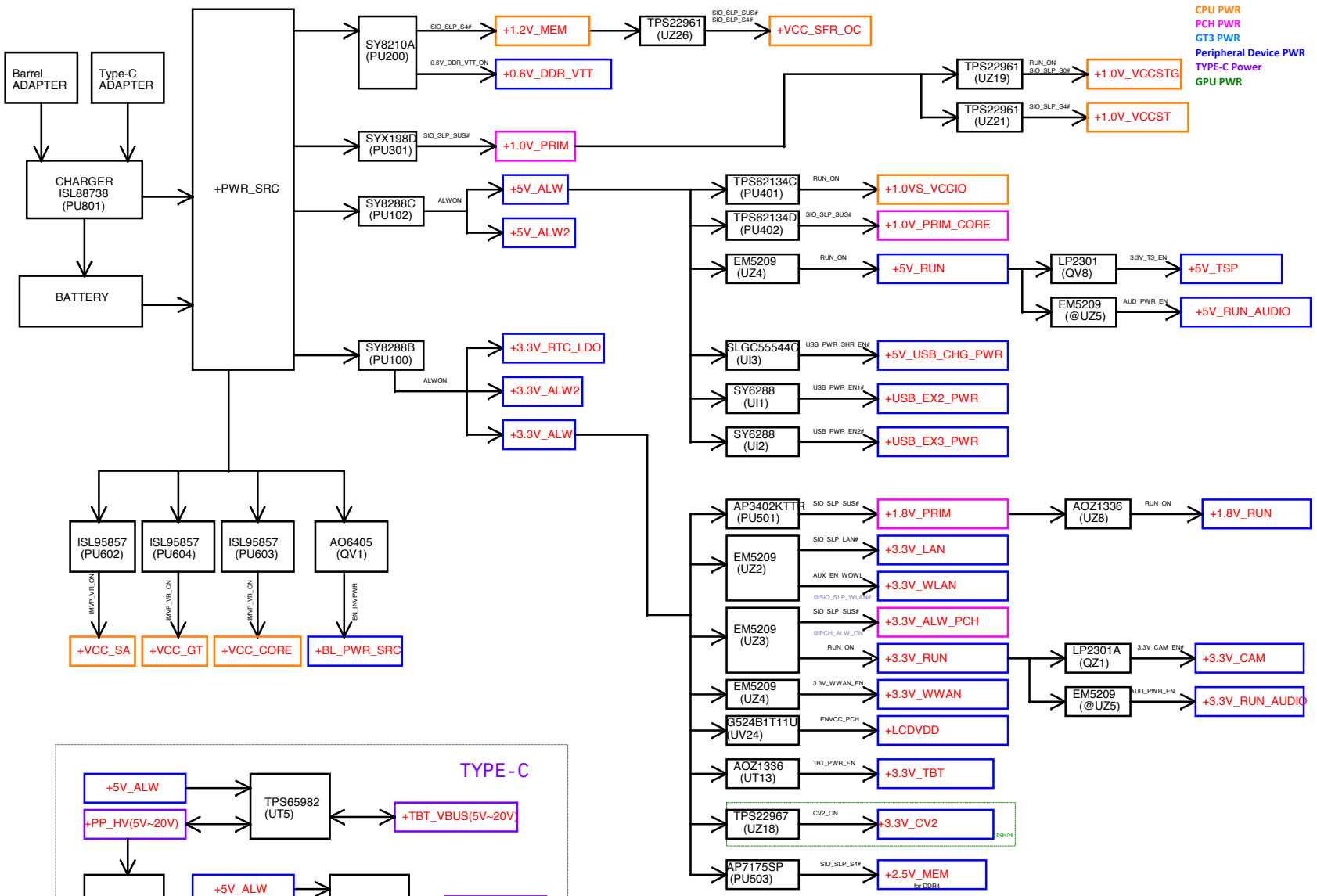
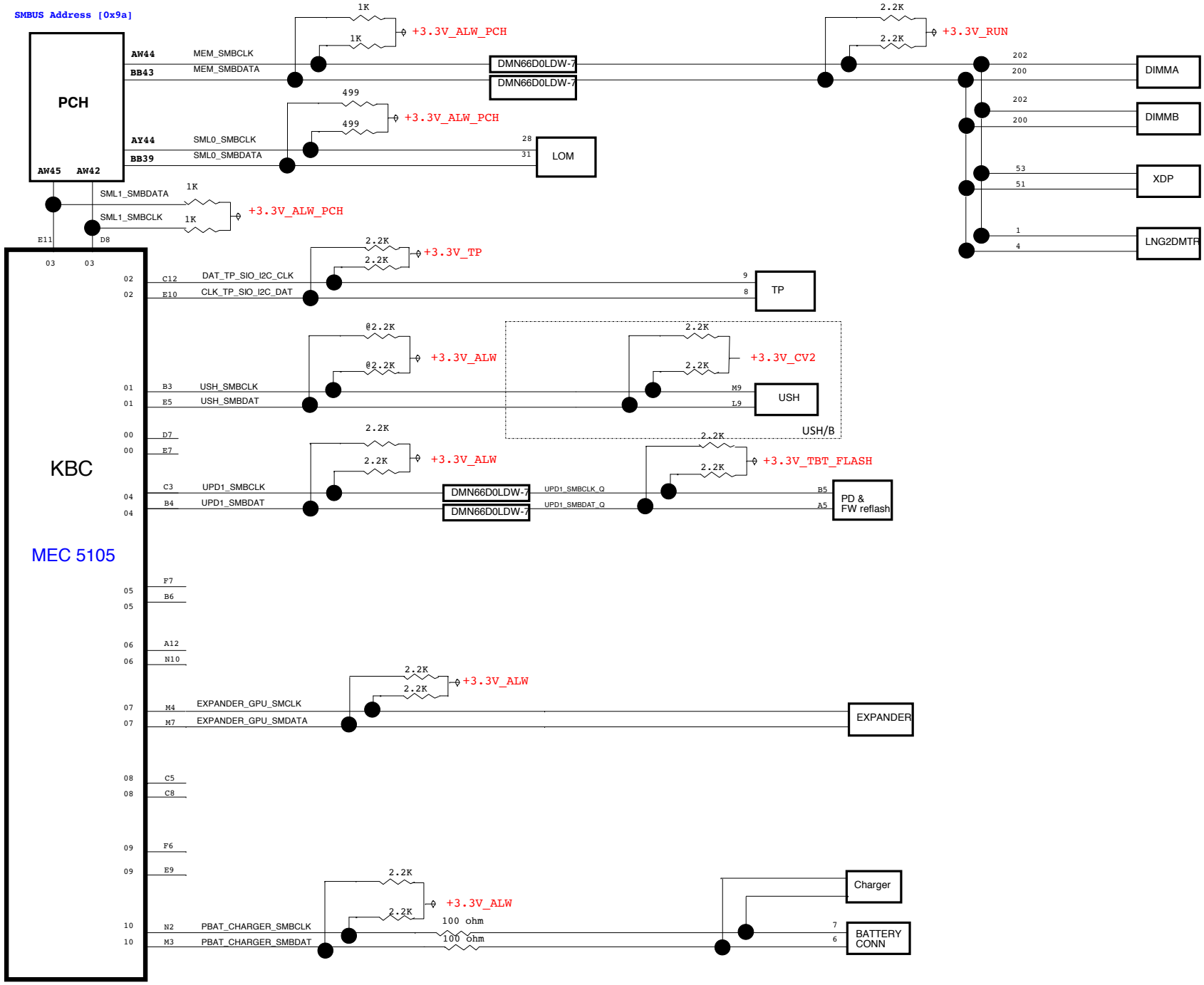
Date: Wednesday, June 29, 2016 | Sheet 3 of 61



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title: Power Rails			
Size: C	Document Number: LA-E141P		Rev: 0.2
Date: Wednesday, June 29, 2016	Sheet 4 of 61		



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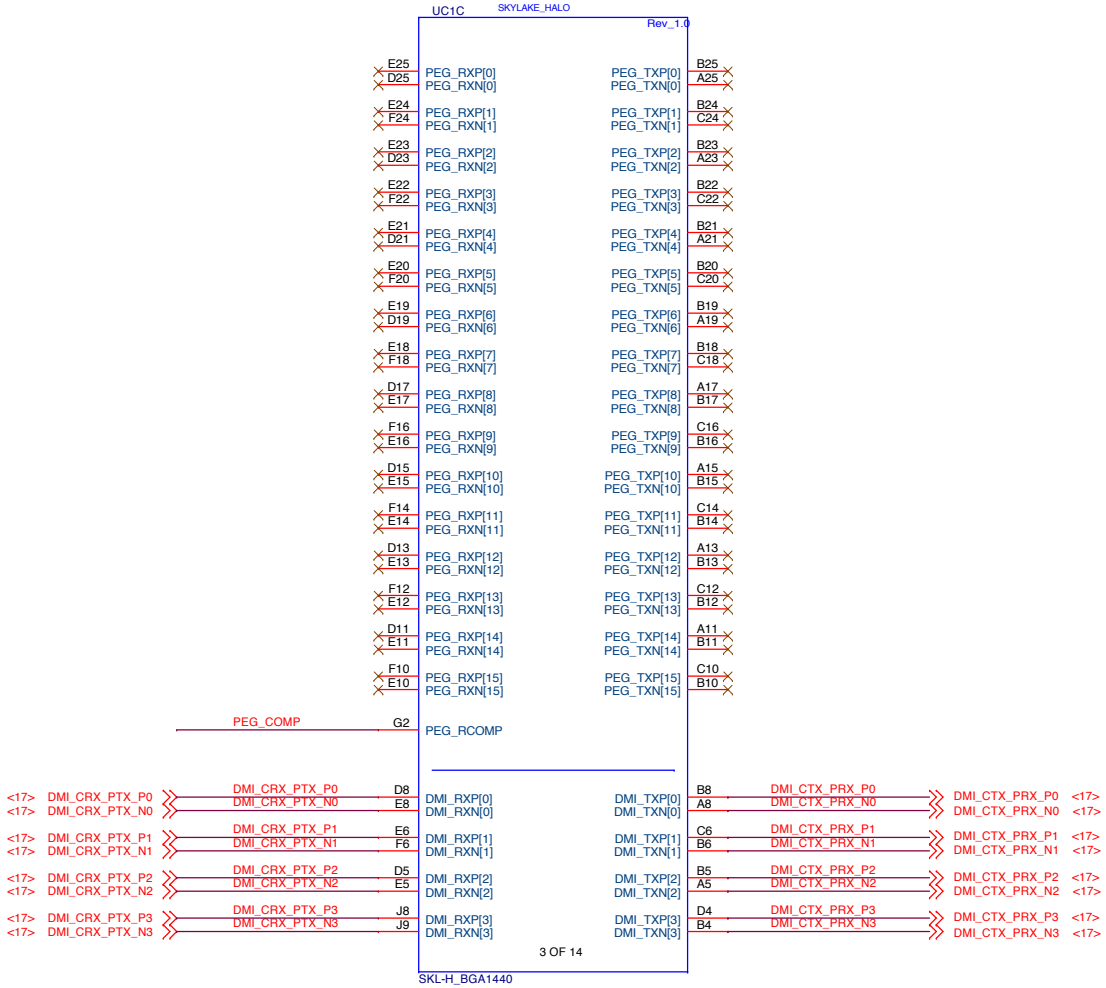
Title: SMbus Block Diagram

Size	Document Number	Rev
B	LA-E141P	0.2

Date: Wednesday, June 29, 2016 | Sheet 5 of 61



+1.0VS_VCCIO

RC2 1 2 PEG_COMP 24.9_0402_1%

Trace width=5 mils
,Spacing=15mil
Max length= 600 mils.

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Title: KBL-H (1/8)

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CPU XDP

Place near JXDP1.47

Place near JXDP1

Place near JXDP1.41

ESD request,Place near JXDP1 side.

ESD Request,place near CPU side

RF Request

Place close CPU side

CFG0	
Stall reset sequence after PCU PLL lock until de-asserted	
No Stall	1
Stall	0

CFG2	
PEG LANE REVERSAL	
NORMAL	1
LANE REVERSED	0

CFG4	
eDP enable	
Disabled	1
Enabled	0

CFG5	
PCI Express* Bifurcation [6:5]	
1x8, 2x4	00
Reserved	01
2x8	10
1x16	11

CFG7	
PEG Training	
(default) PEG Train immediately following RESET# de-assertion	1
PEG Wait for BIOS for training	0

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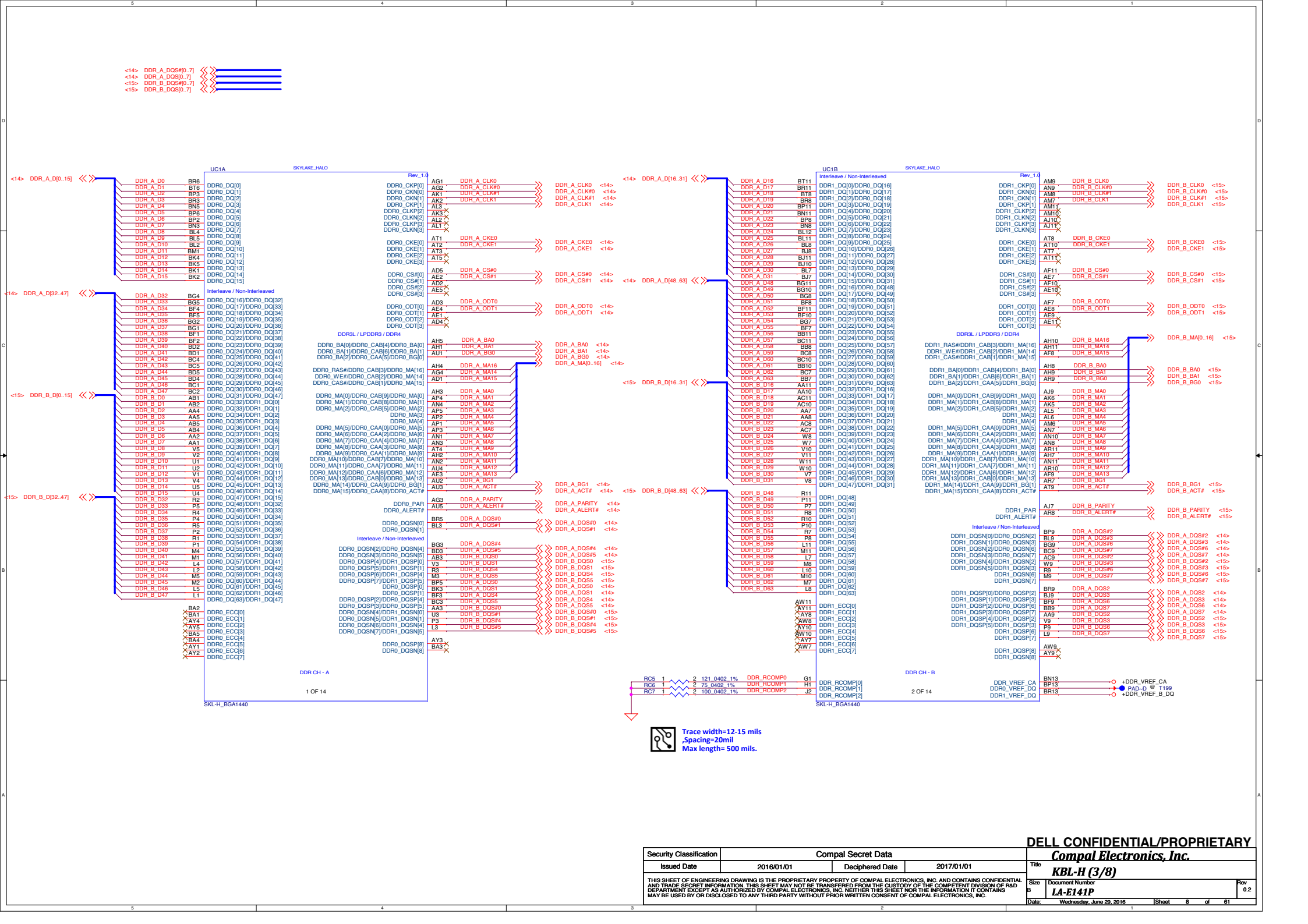

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Size	Document Number	Rev
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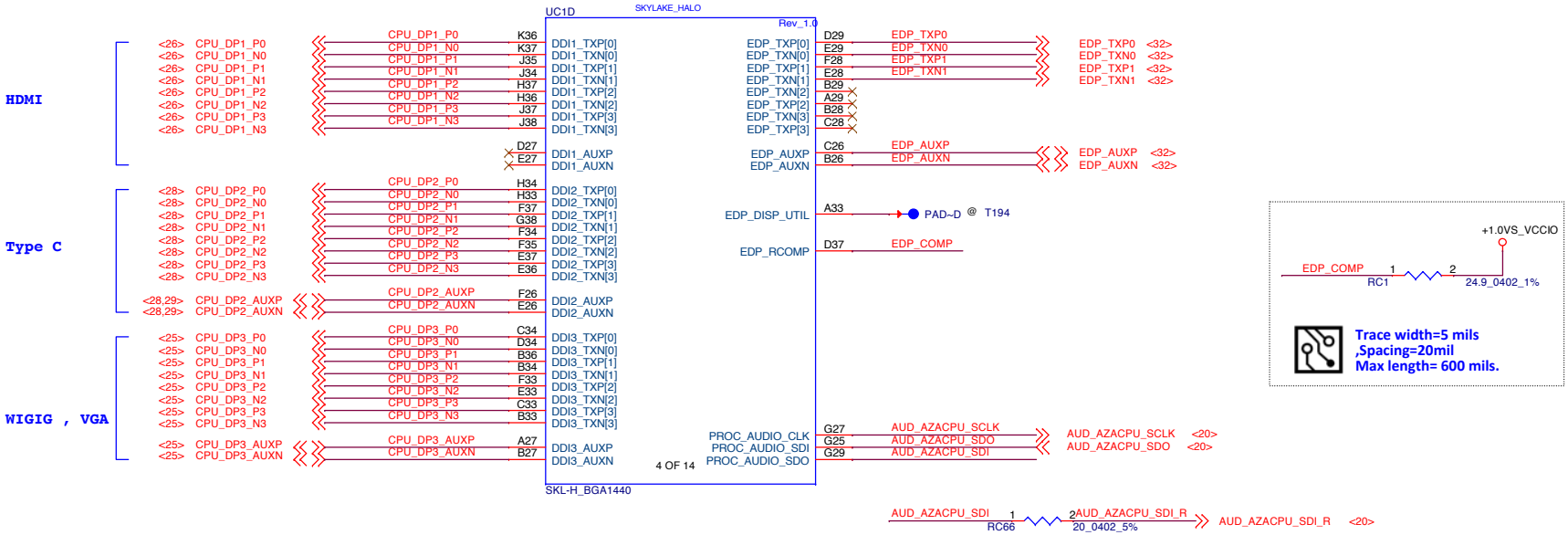

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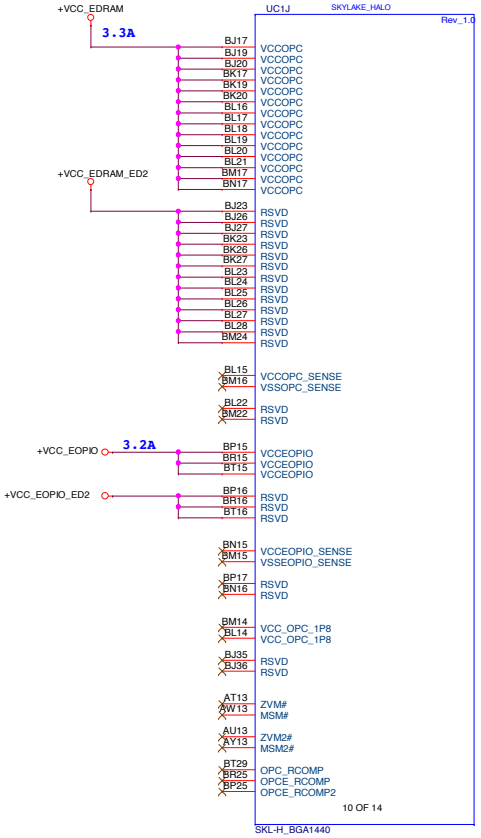

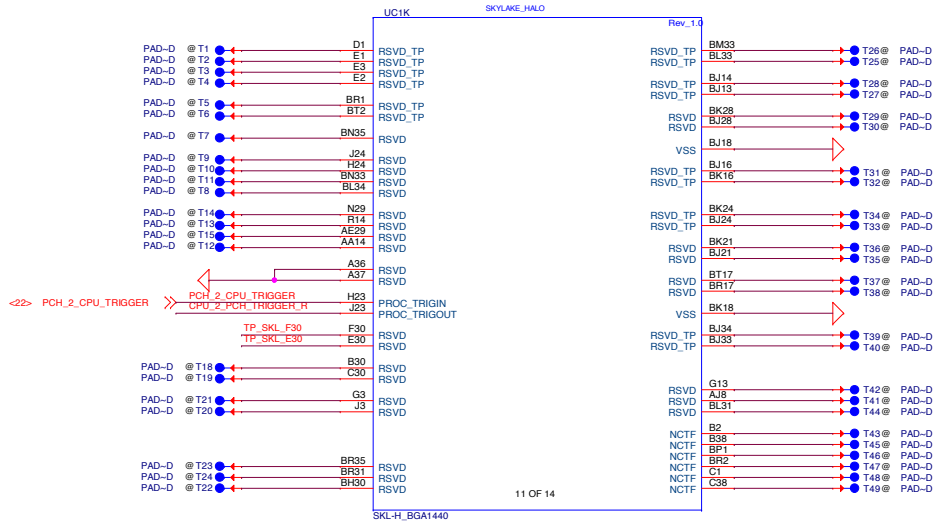

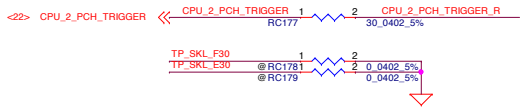

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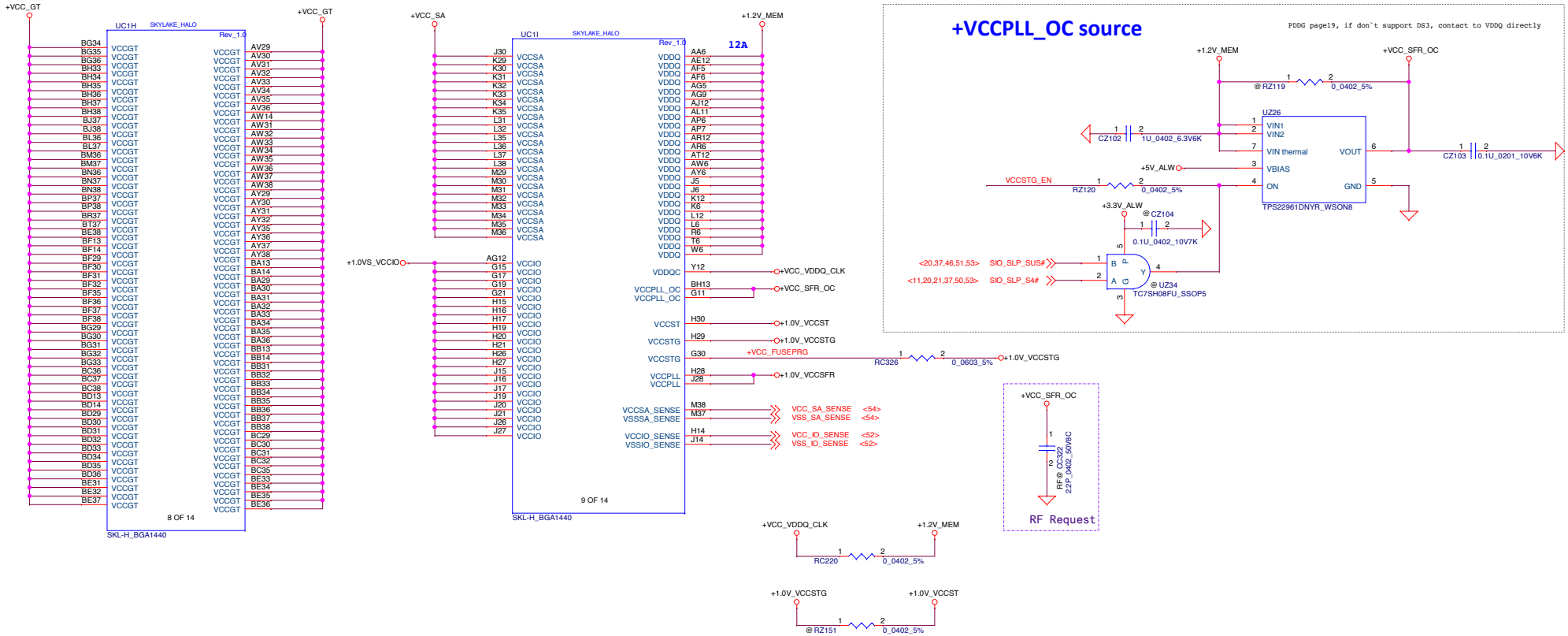
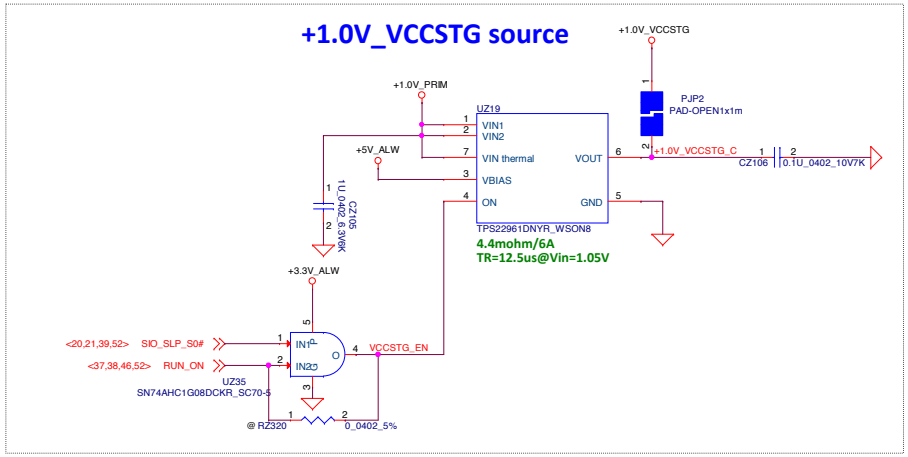
Title: KBL-H (5/8)			
Size: B	Document Number: LA-E141P		Rev: 0.2
Date: Wednesday, June 29, 2016	Sheet 10 of 61		



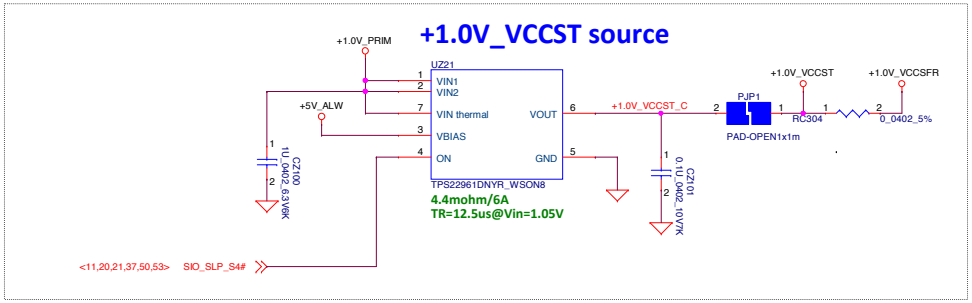
+VCCPLL_OC source

PDDG page19, if don`t support DS3, contact to VDDQ directly

+1.0V_VCCSTG source



+1.0V_VCCST source



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Size	B
Document Number	LA-E141P
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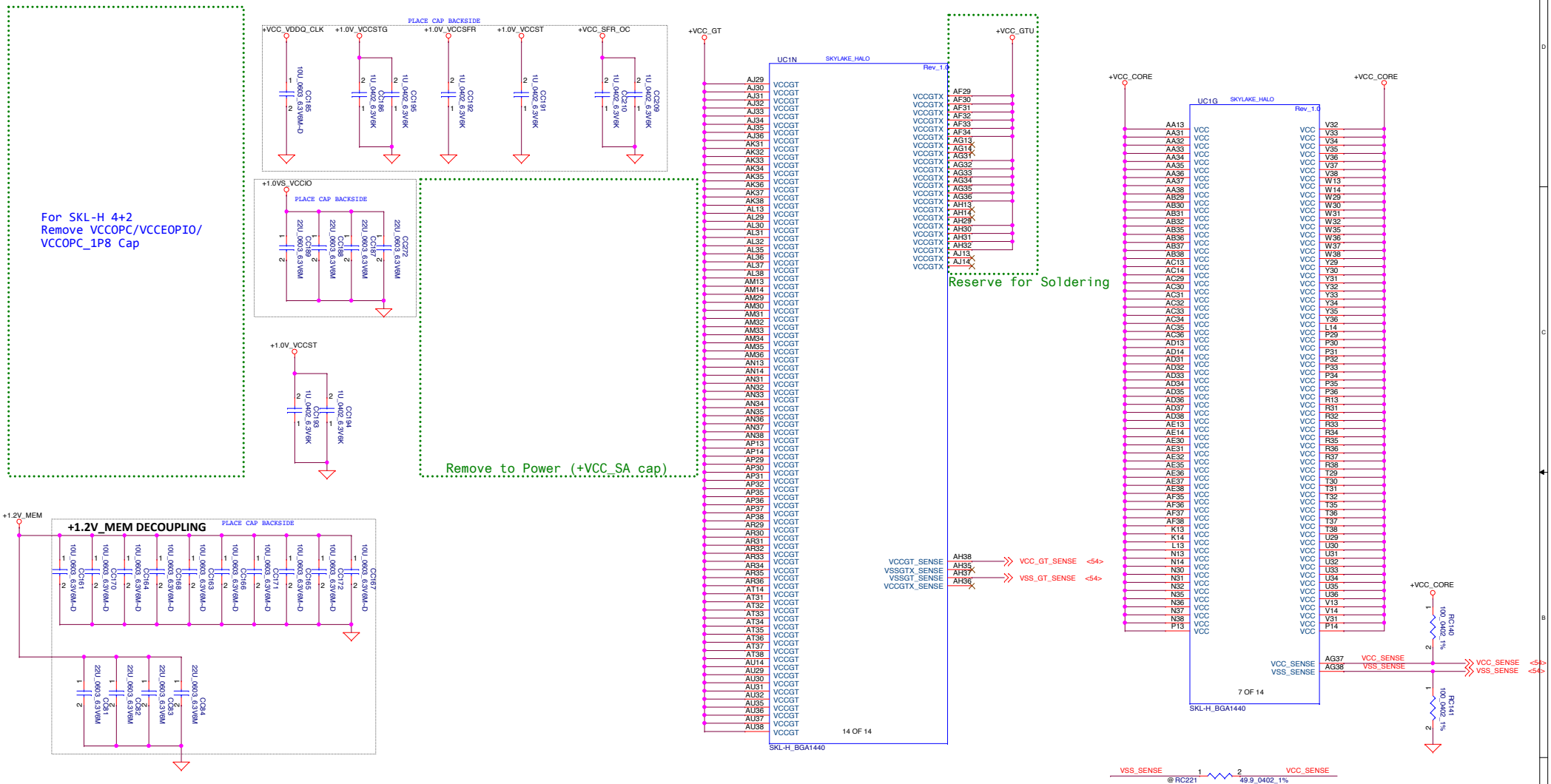

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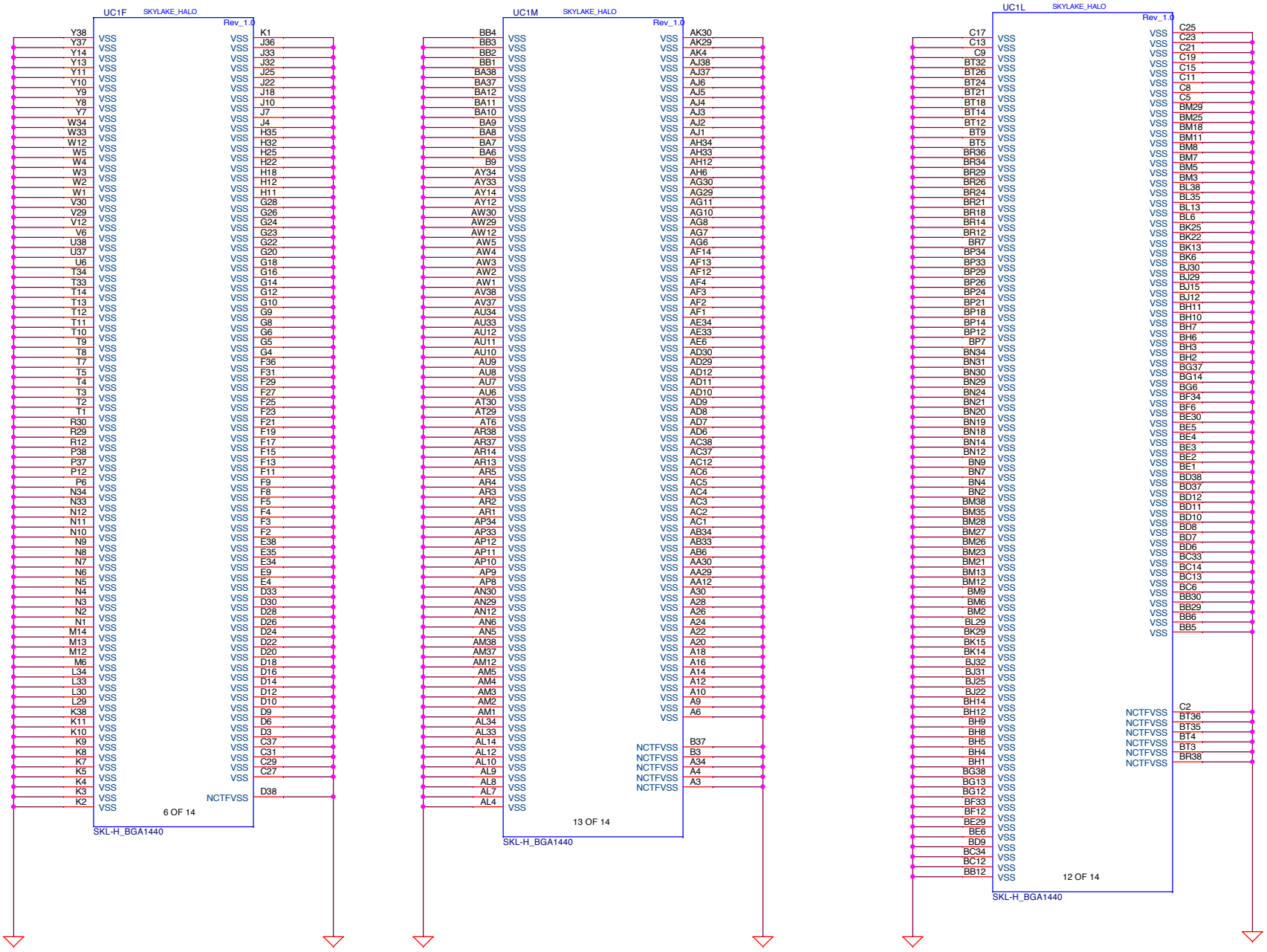
Size: B	Document Number: LA-E141P	Rev: 0.2
Date: Wednesday, June 29, 2016	Sheet 12 of 61	



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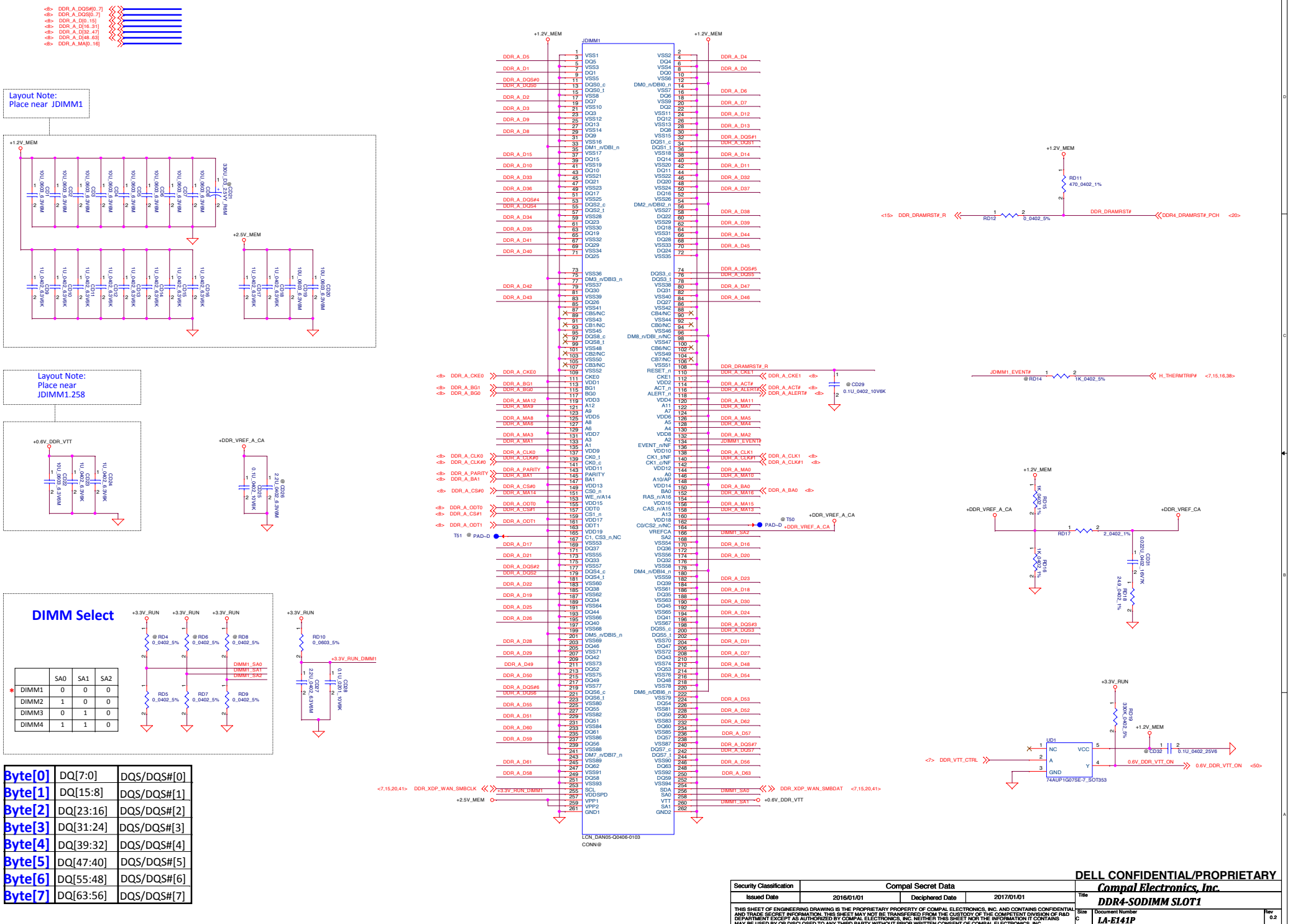
Title: KBL-H (8/8)

Size: A | Document Number: LA-E141P | Rev: 0.2

Date: Wednesday, June 29, 2016 | Sheet 13 of 61



	SA0	SA1	SA2
* DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0

Byte[0]	DQ[7:0]	DQS/DQS#[0]
Byte[1]	DQ[15:8]	DQS/DQS#[1]
Byte[2]	DQ[23:16]	DQS/DQS#[2]
* Byte[3]	DQ[31:24]	DQS/DQS#[3]
Byte[4]	DQ[39:32]	DQS/DQS#[4]
* Byte[5]	DQ[47:40]	DQS/DQS#[5]
Byte[6]	DQ[55:48]	DQS/DQS#[6]
Byte[7]	DQ[63:56]	DQS/DQS#[7]

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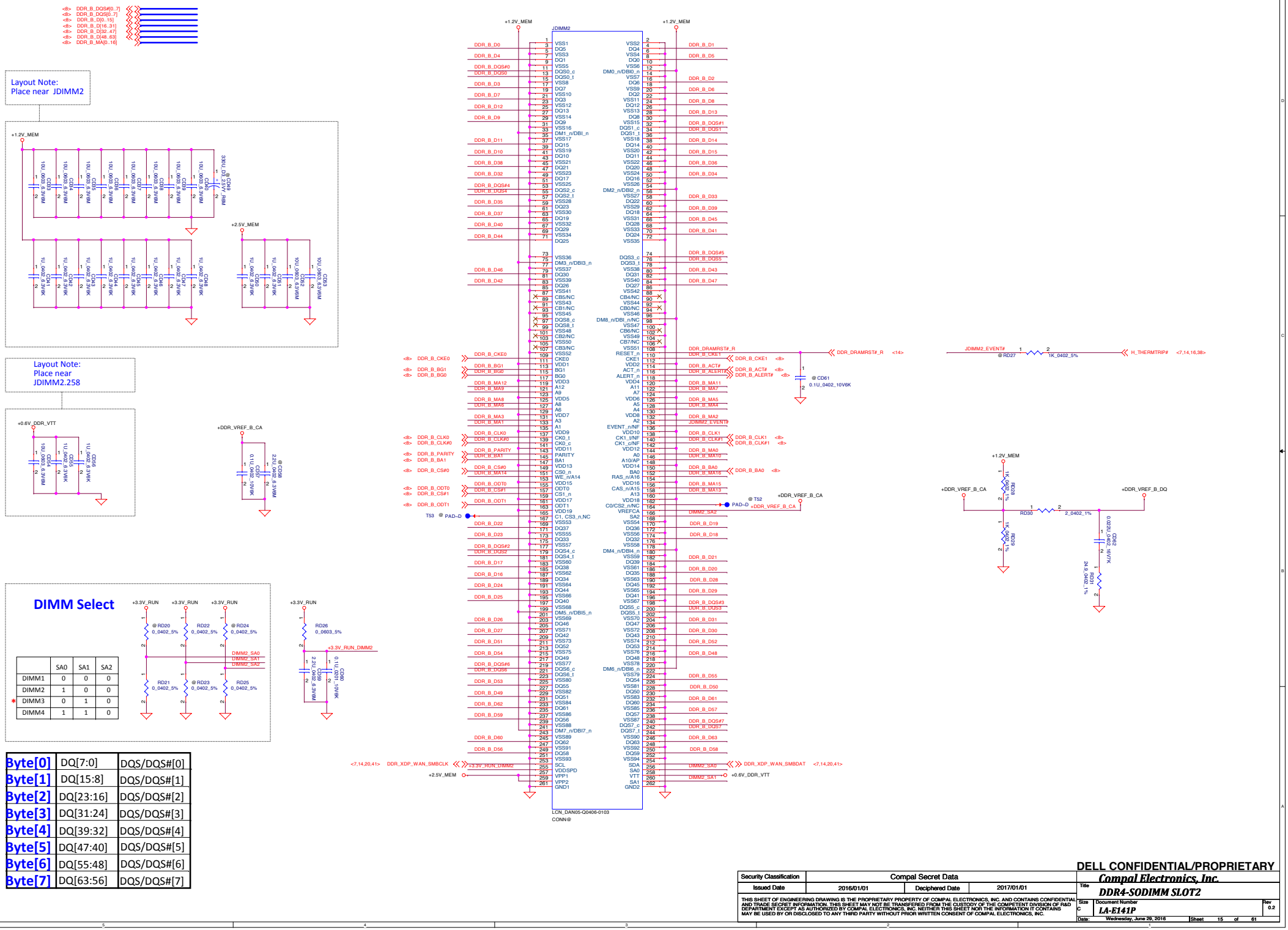
Title: DDR4-SODIMM SLOT1

Size	Document Number	Rev
C	LA-E141P	0.2

Date: Wednesday, June 29, 2016 Sheet 14 of 61



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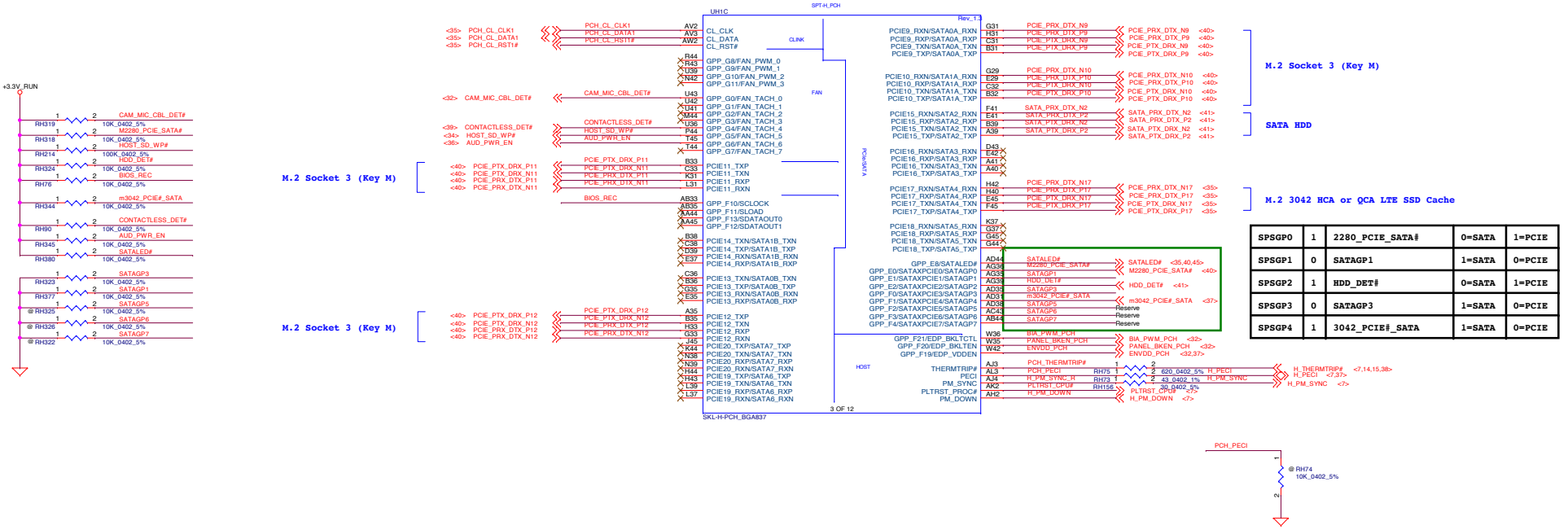
Compal Electronics, Inc.

Title: DDR4-SODIMM SLOT2

Size: C | Document Number: LA-E141P | Rev: 0.2

Date: Wednesday, June 29, 2016 | Sheet 15 of 61



SPSGP0	1	2280_PCIE_SATA#	0=SATA	1=PCIE
SPSGP1	0	SATAGP1	1=SATA	0=PCIE
SPSGP2	1	HDD_DET#	0=SATA	1=PCIE
SPSGP3	0	SATAGP3	1=SATA	0=PCIE
SPSGP4	1	3042_PCIE#_SATA	1=SATA	0=PCIE

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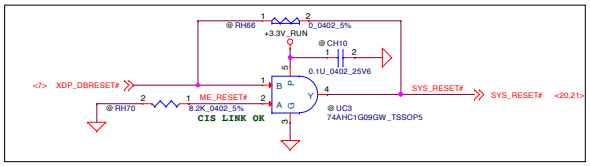
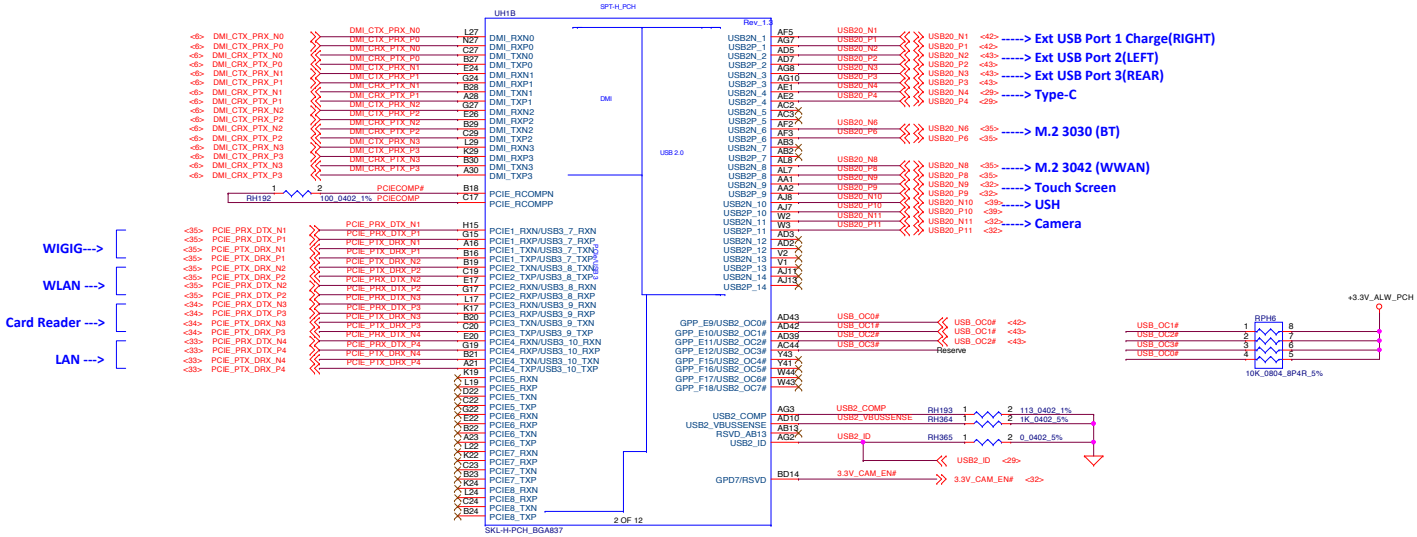
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: KABYLAKE PCH-H (1/9)

Size: C	Document Number: LA-E141P		Rev: 0.2
Date: Wednesday, June 29, 2016	Sheet 16 of 61		





Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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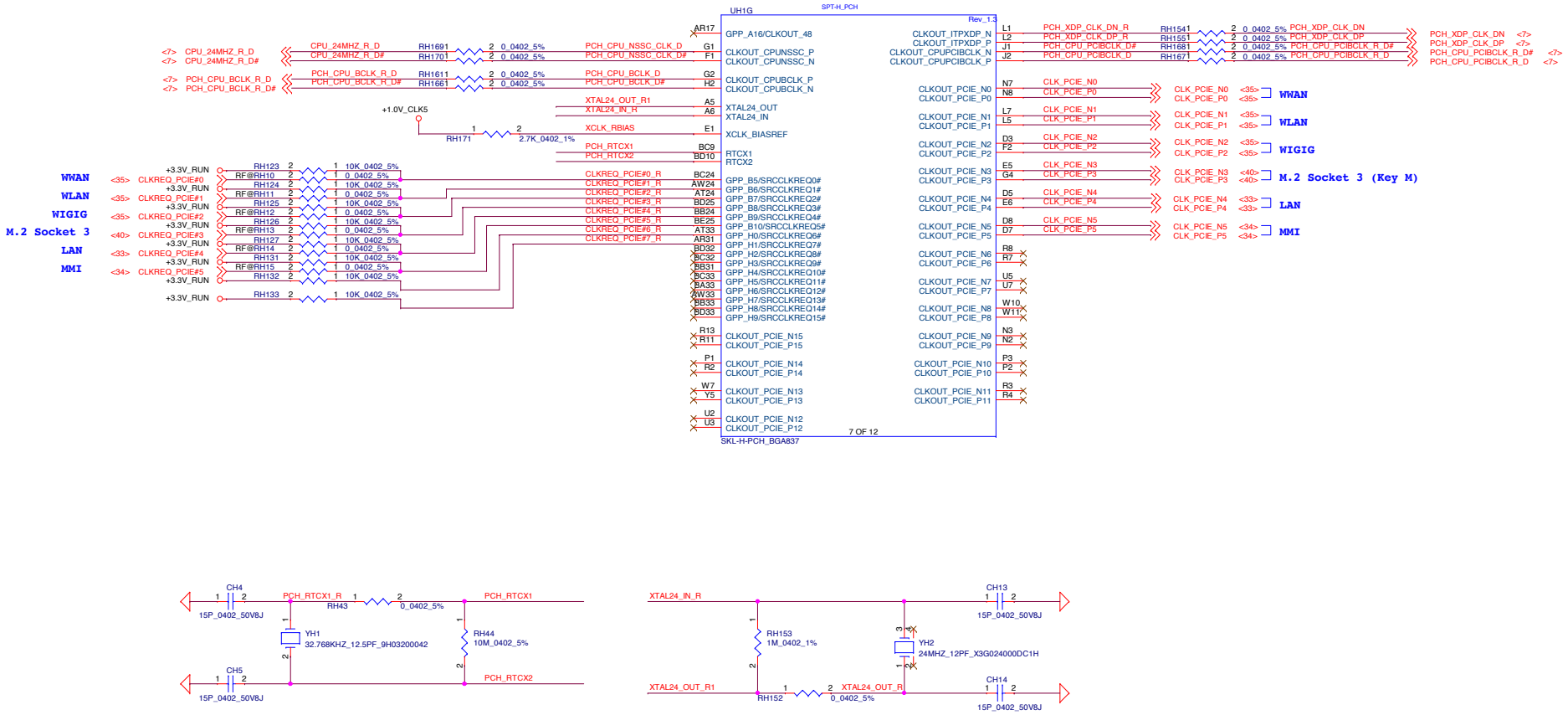
Compal Electronics, Inc.

Title: KABYLAKE PCH-H (2/9)

Size	Document Number	Rev
C	LA-E141P	0.2

Date: Wednesday, June 29, 2016 Sheet 17 of 61



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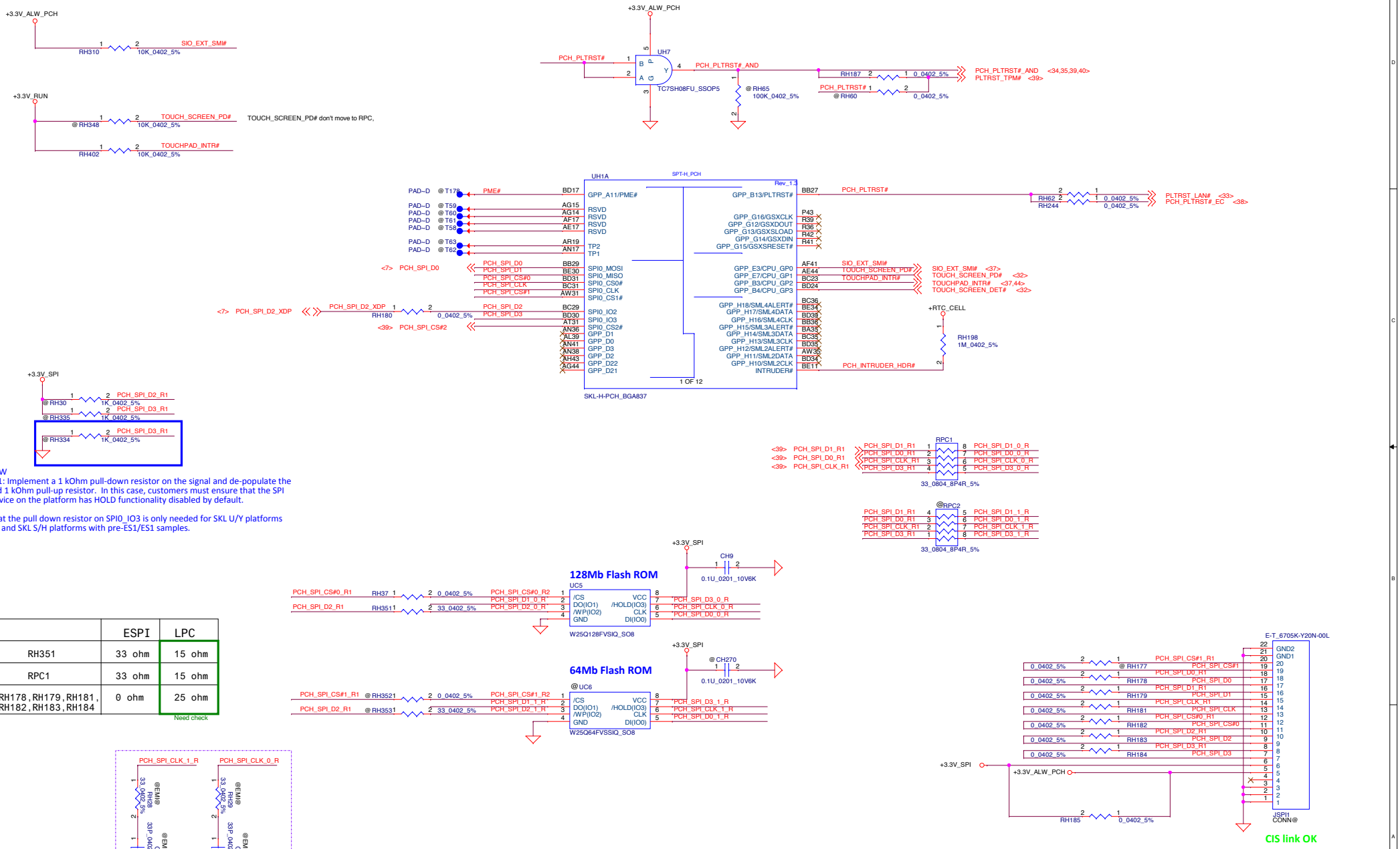
Title: *KABYLAKE PCH-H (3/9)*

Size	Document Number	Rev
B	*LA-E141P*	0.2

Date: Thursday, June 30, 2016 | Sheet 18 of 61



	ESPI	LPC
RH351	33 ohm	15 ohm
RPC1	33 ohm	15 ohm
RH178,RH179,RH181, RH182,RH183,RH184	0 ohm	25 ohm

Need check

Security Classification	Compal Secret Data	
Issued Date	2016/01/01	Deciphered Date 2017/01/01

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Title: *KABYLAKE PCH-H (4/9)*

Size	Document Number	Rev
B	*LA-E141P*	0.2

Date: Wednesday, Jun 29, 2016 Sheet 19 of 61

Ext USB Port 1 Charge(RIGHT)

M.2 3042 (LTE)

Type C

Ext USB Port 2(LEFT)

Ext USB Port 3(REAR)

UH1F SPT-H_PCH Rev_1.3 — SKL-H-PCH_BGA837 — 6 OF 12

UH1D SPT-H_PCH Rev_1.3 — SKL-H-PCH_BGA837 — 4 OF 12

RF Request

ESD Request,place near PCH side

Place close PCH side

CHECK LPC_CLK FOR DEBUG CARD?

EXI BOOT STALL BYPASS

HIGH	ENABLED
LOW(DEFAULT)	DIABLED

WEAK INTERNAL PD

Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.

ME_FWP PCH has internal 20K PD. (suspend power rail)

FLASH DESCRIPTOR SECURITY OVERRIDE

LOW = ENABLE (DEFAULT) -->Pin1 & Pin3 short
HIGH = DISABLE (ME can update) -->Pin2 & Pin3 short

RH215

POP	NO Support Deep sleep
DE-POP	Support Deep sleep

ESD request,Place near PCH side.

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Issued Date	2016/01/01	Deciphered Date	2017/01/01

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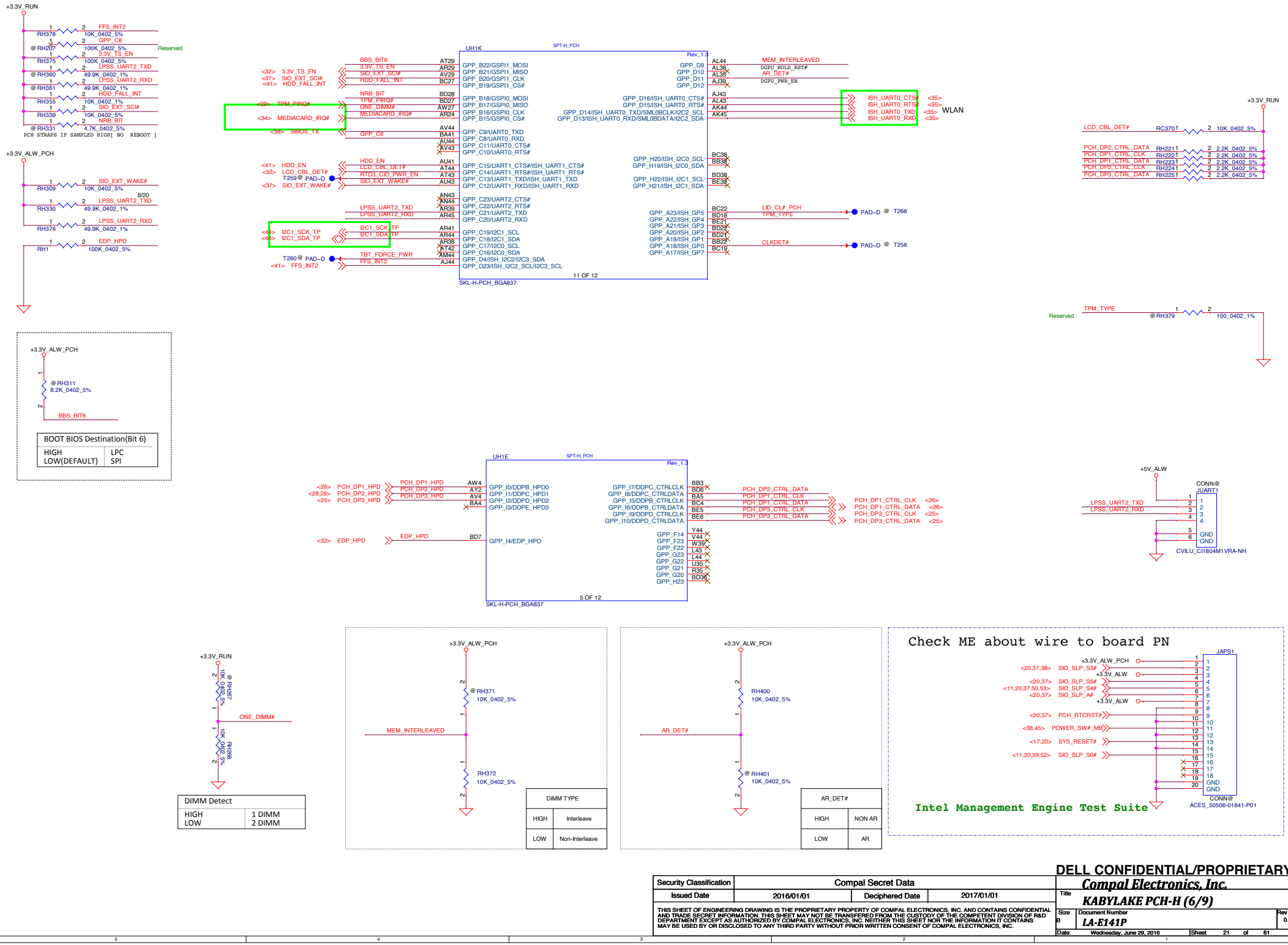
Compal Electronics, Inc.

Title: KABYLAKE PCH-H (5/9)

Size: B | Document Number: LA-E141P | Rev: 0.2

Date: Wednesday, June 29, 2016 | Sheet 20 of 61



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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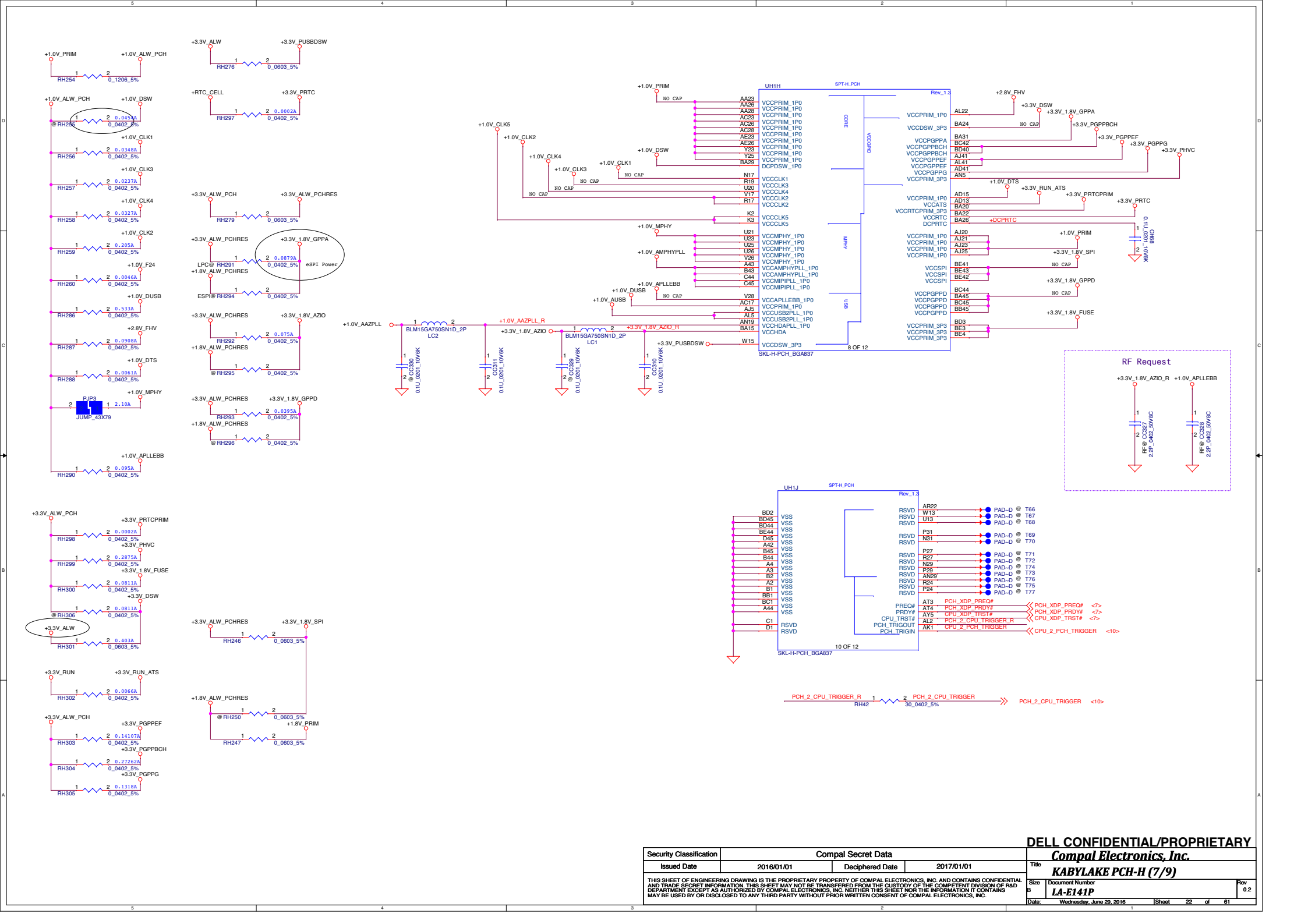
Title: *KABYLAKE PCH-H (6/9)*

Size	Document Number	Rev
B	*LA-E141P*	0.2

Date: Wednesday, June 29, 2016 Sheet 21 of 61



Security Classification	Compal Secret Data		
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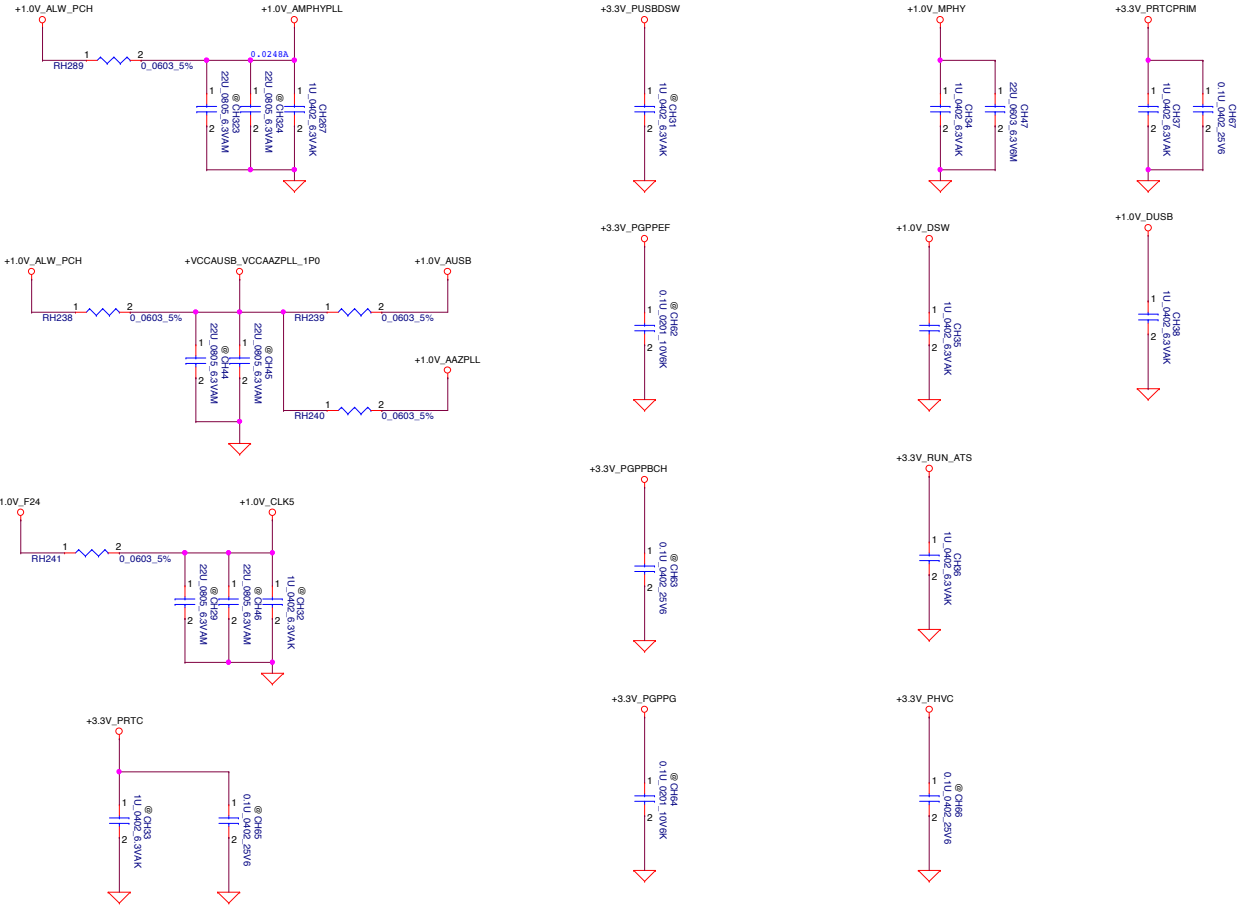
Title: *KABYLAKE PCH-H (7/9)*

Size	Document Number	Rev
B	*LA-E141P*	0.2

Date: Wednesday, June 29, 2016 | Sheet 22 of 61



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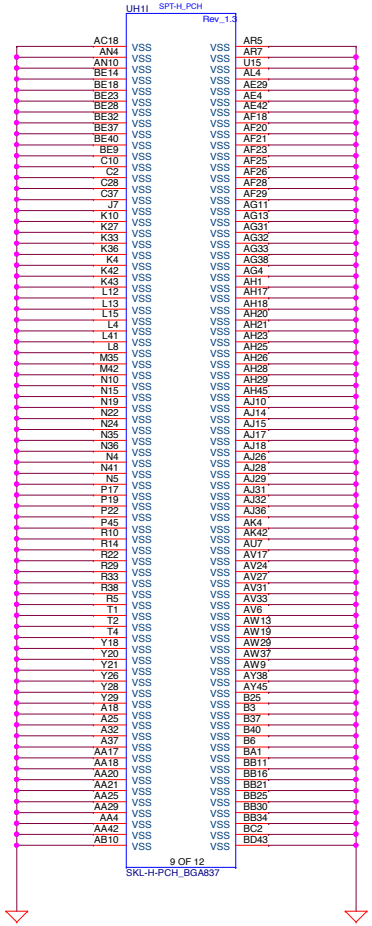
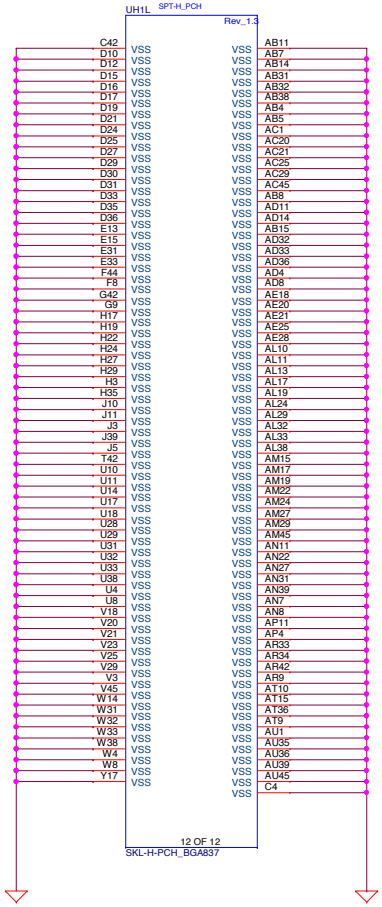
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: KABYLAKE PCH-H (8/9)		
Size: B	Document Number: LA-E141P	Rev: 0.2
Date: Wednesday, June 29, 2016	Sheet 23 of 61	





Security Classification	Compal Secret Data		
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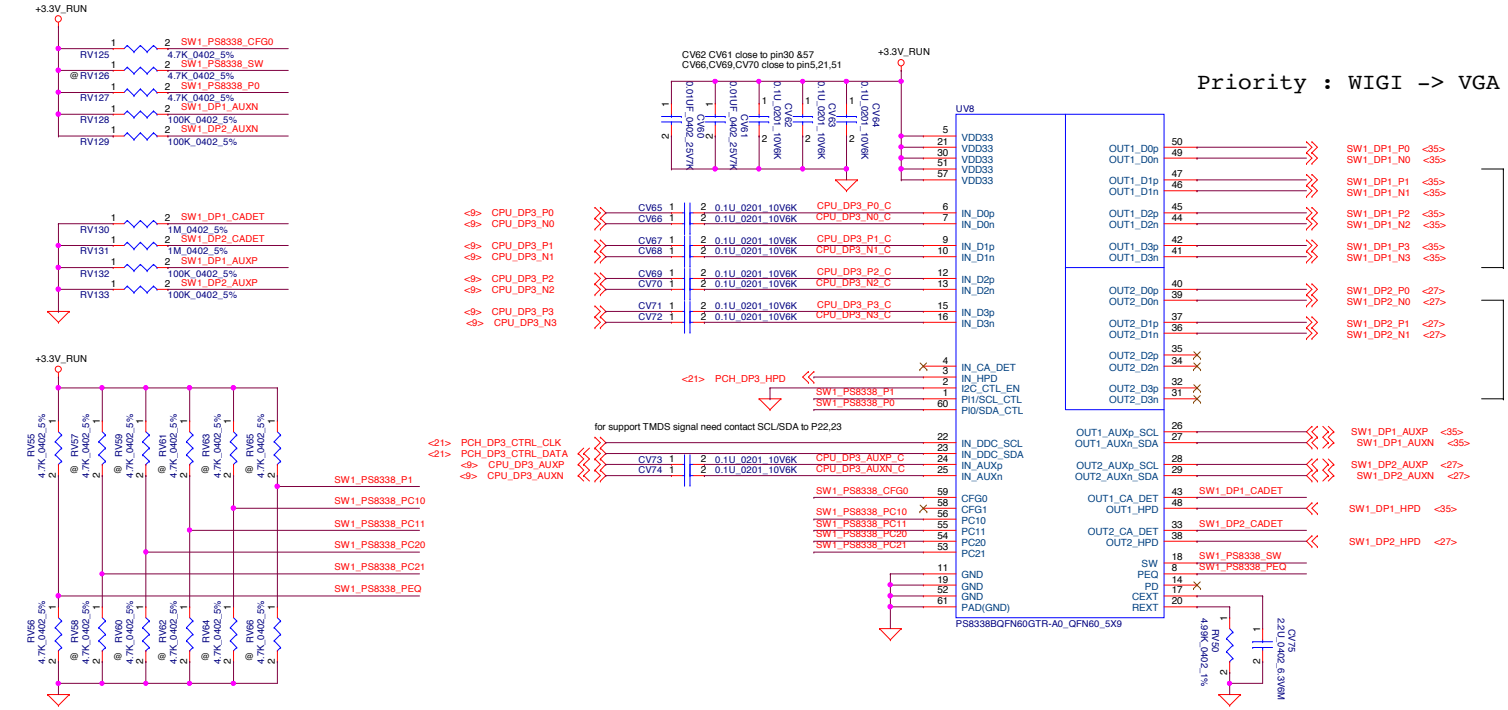
Compal Electronics, Inc.

Title: KABYLAKE PCH-H (9/9)

Size	Document Number	Rev
B	LA-E141P	0.2

Date: Wednesday, June 29, 2016 Sheet 24 of 61



Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected (default)
SW = H: Port2 is selected
For Automatic Switching Mode (CFG0 = H):
SW = L: Port1 has higher priority when both ports are plugged (default)
SW = H: Port2 has higher priority when both ports are plugged

vender suggguest MUX use LLEQ PEQ=M and PI0=H !!

Programmable input equalization levels, Internal pull down at ~150Kohm,3.3V I/O
PEQ =
L: default,LEQ, compensate channel loss up to 11.5dB @HBR2
H: HEQ, compensate channel loss up to 14.5dB @HBR2
M:LLEQ, compensate channel loss up to 8.5dB @HBR2

PI0:Automatic EQ disable, Internal pull down ~150K ohm, 3.3V I/O
PI0 = L: Automatic EQ enable(default)
H: Automatic EQ disable

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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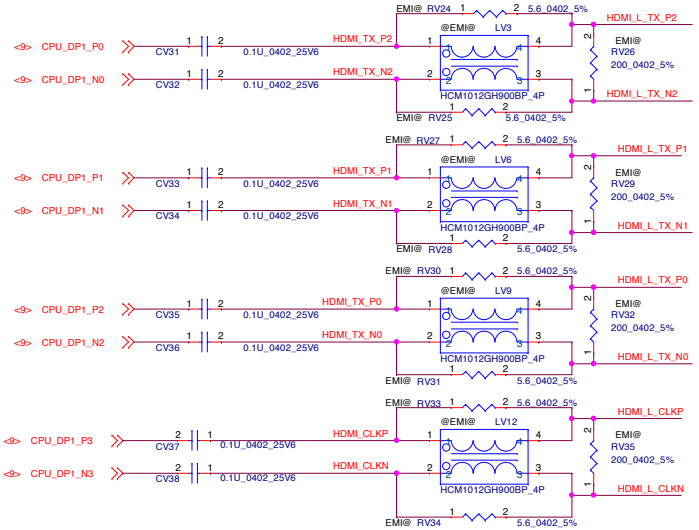
Compal Electronics, Inc.

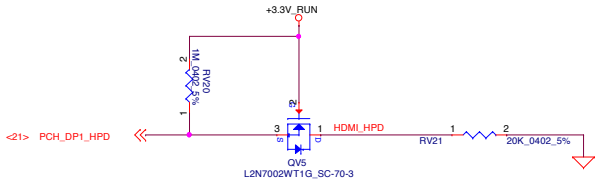
Title: *DP SW2 PS8338*

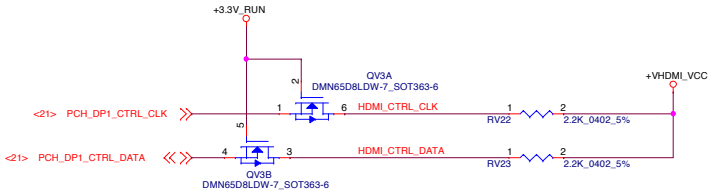
Size: B | Document Number: *LA-E141P* | Rev: 0.2

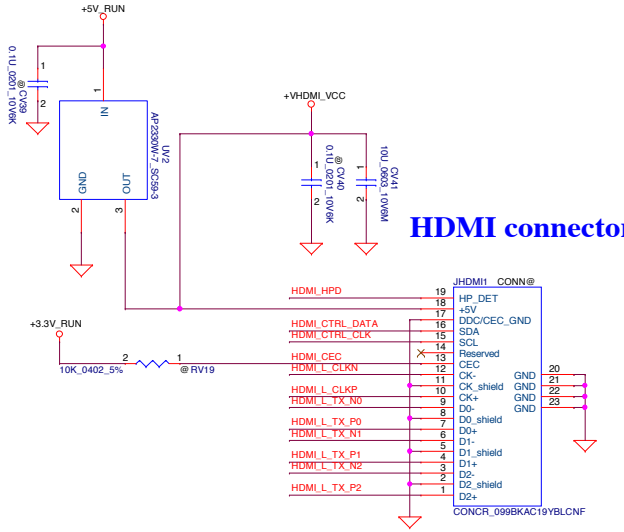
Date: Wednesday, June 29, 2016 | Sheet 25 of 61

For Breckenridge 14

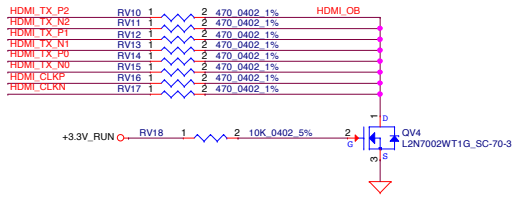








LINK 099BKAC19YBLCNF DONE



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Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Title	HDMI CONN	
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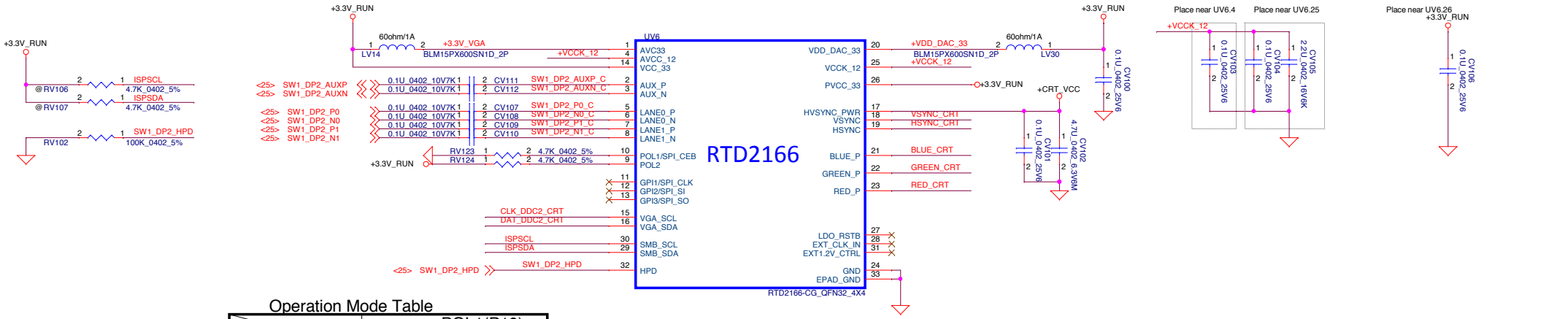
Date: Wednesday, June 29, 2016	Sheet 26 of 61	

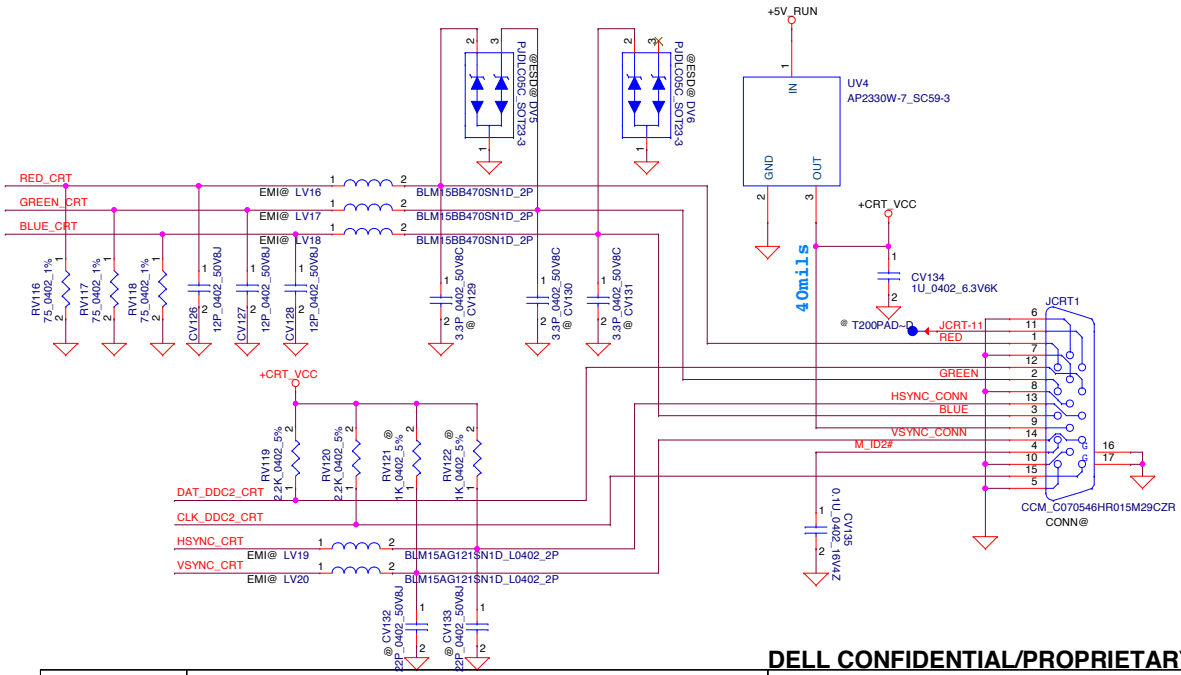
For TBT SW2_DP2
For non-TBT SW1_DP2

For Realtek Solution



Operation Mode Table

		POL1(P10)	
		0	1
POL2 (P9)	0	X	X
	1	ROM	EEPROM



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Security Classification	Compal Secret Data		
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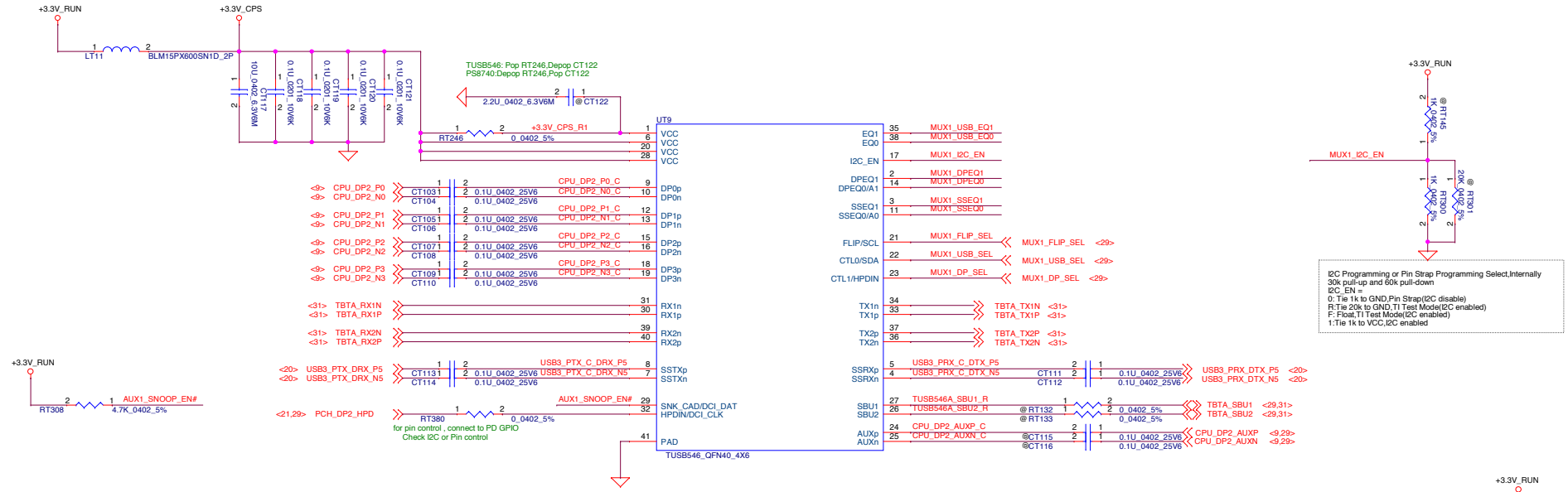
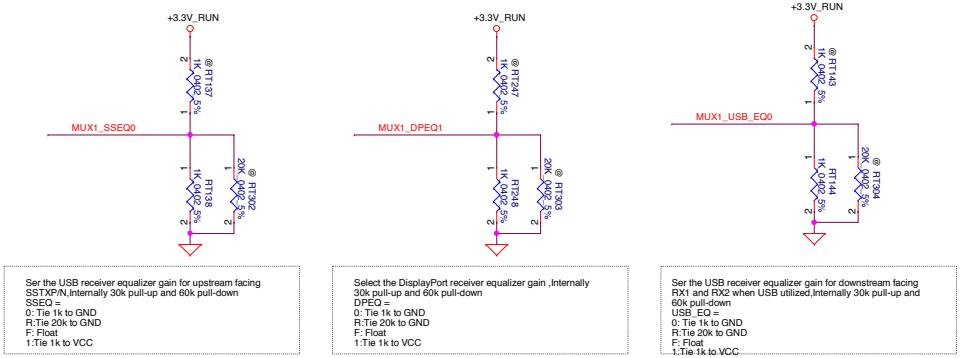
Compal Electronics, Inc.

Title: DP to VGA & VGA Conn

Size: Custom | Document Number: LA-E141P | Rev: 0.2

Date: Wednesday, June 29, 2016 | Sheet 27 of 61





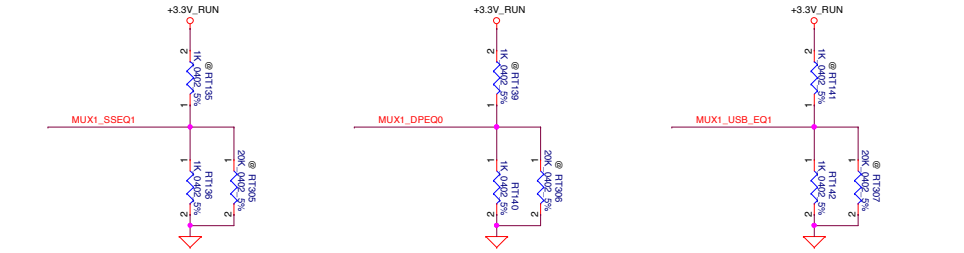


Table 8-7 TUSB546 Receiver Equalization GPIO Control

USB3.1 Downstream Facing Ports			USB 3.1 Upstream Facing Port			All DisplayPort Lanes		
EQ1 pin Level	EQ0 pin Level	EQ GAIN @5GHz (dB)	SSEQ1 pin Level	SSEQ0 pin Level	EQ GAIN @5GHz (dB)	DPEQ1 pin Level	DPEQ0 pin Level	EQ GAIN @5GHz (dB)
0	0	0	0	0	0	0	0	0
0	R	1	0	R	1	0	R	1
0	F	2	0	F	2	0	F	2
0	1	3	0	1	3	0	1	3
R	0	4	R	0	4	R	0	4
R	R	5	R	R	5	R	R	5
R	F	6	R	F	6	R	F	6
R	1	7	R	1	7	R	1	7
F	0	8	F	0	8	F	0	8
F	R	9	F	R	9	F	R	9
F	F	10	F	F	10	F	F	10
F	1	11	F	1	11	F	1	11
1	0	12	1	0	12	1	0	12
1	R	13	1	R	13	1	R	13
1	F	14	1	F	14	1	F	14
1	1	15	1	1	15	1	1	15

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title	DP/USB3 Repeater SW2 TUSB546		
Size B	Document Number LA-E141P		Rev 0.2
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For Non-AR config

DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.20	0.28	2	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to UFP and can initiate.
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to DFP and can initiate.
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

Route in pass through manner so AUX can be snooped by 546

Need Link TPS65982D

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Compal Electronics, Inc.

Title: [Type CJPD Controller TI

Size: C | Document Number: LA-E141P | Rev: 0.2

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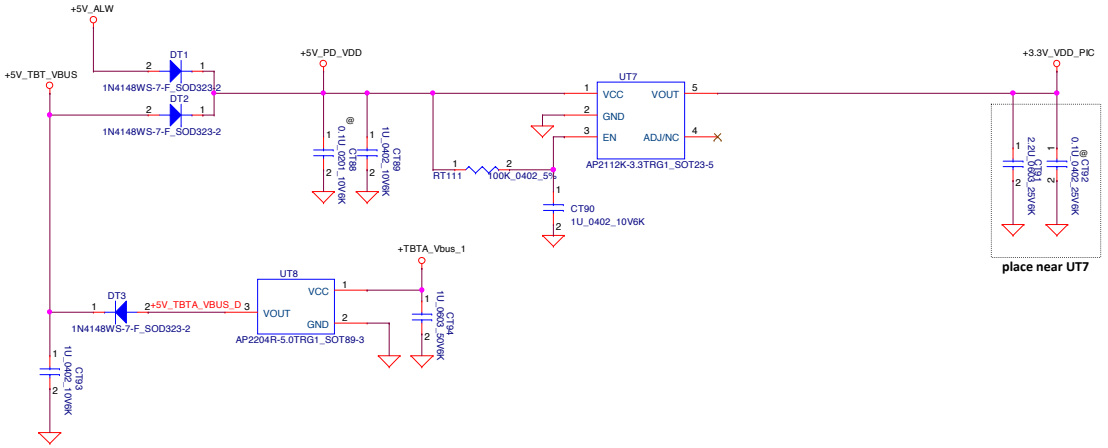

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: [Type C]PD Power

Size	Document Number	Rev
B	LA-E141P	0.2

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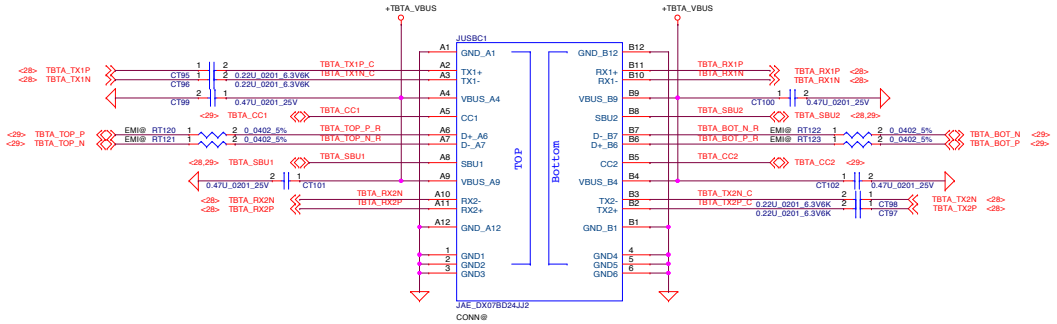
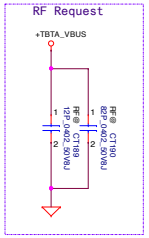
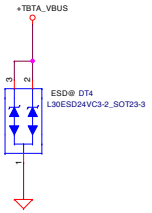
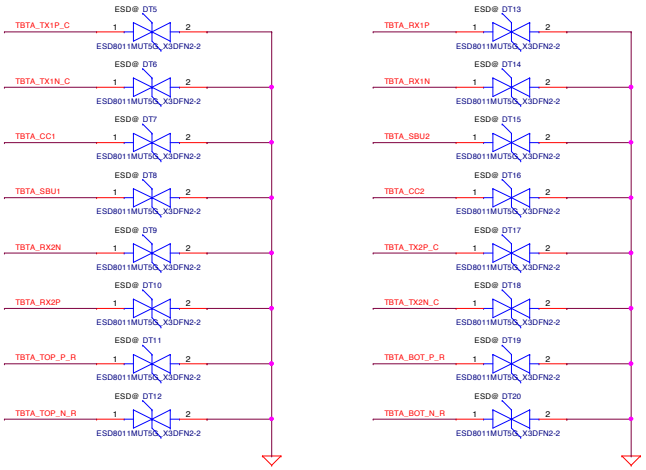
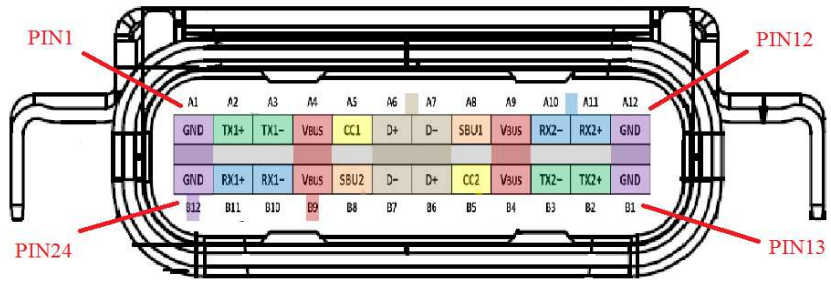
For NON AR Config











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Compal Electronics, Inc.

Title: USB 3.0 CONN TYPE C

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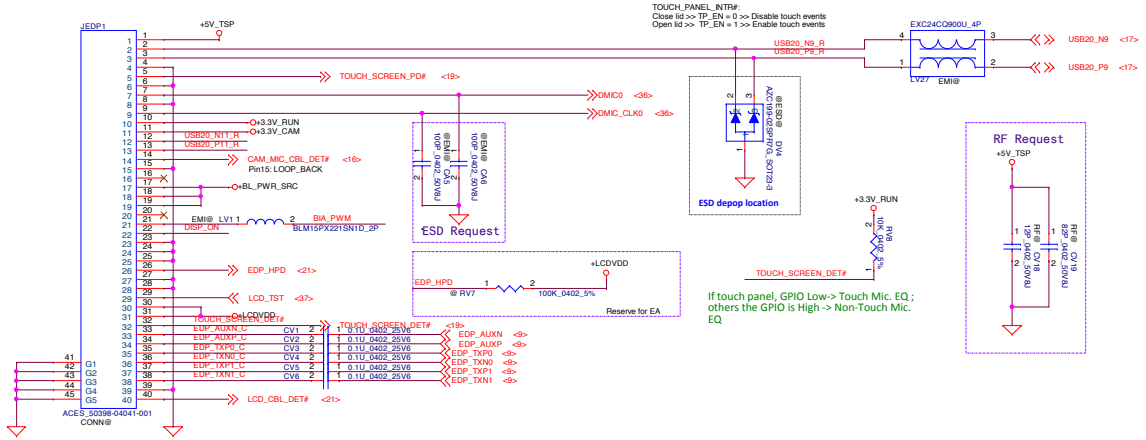
For Breckenridge 14



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Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: eDP CONN & Touch screen

Size	Document Number	Rev
C	LA-E141P	0.2

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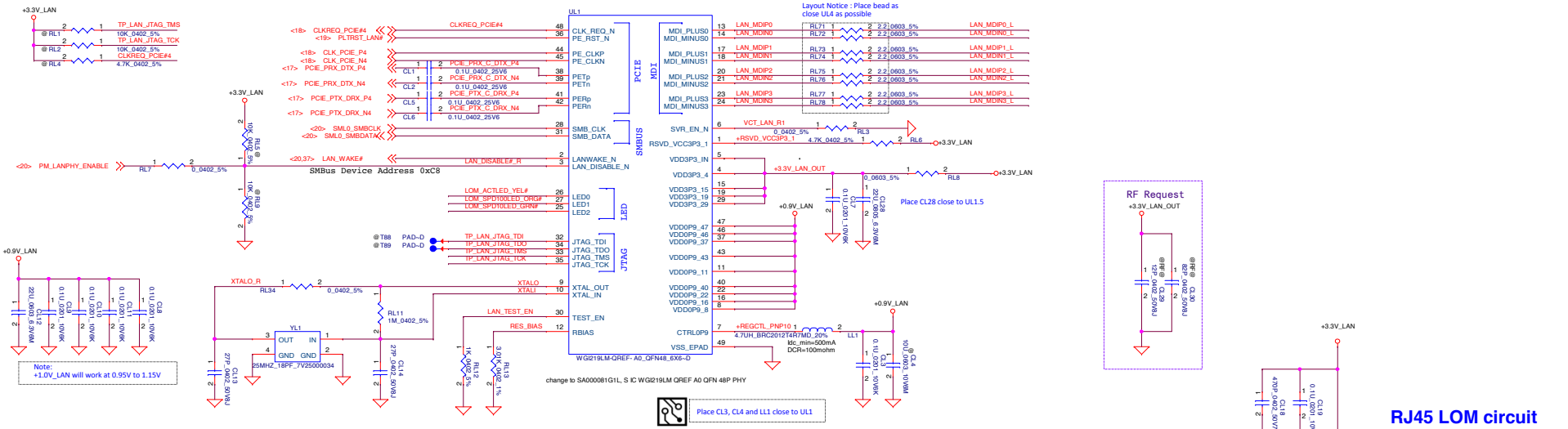

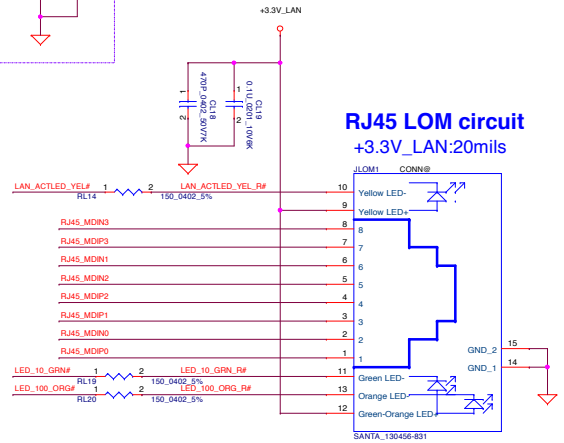

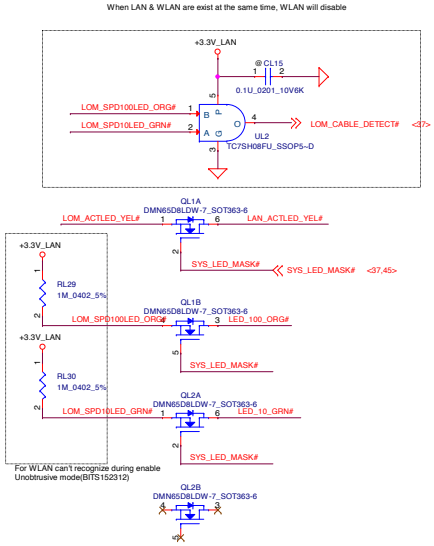

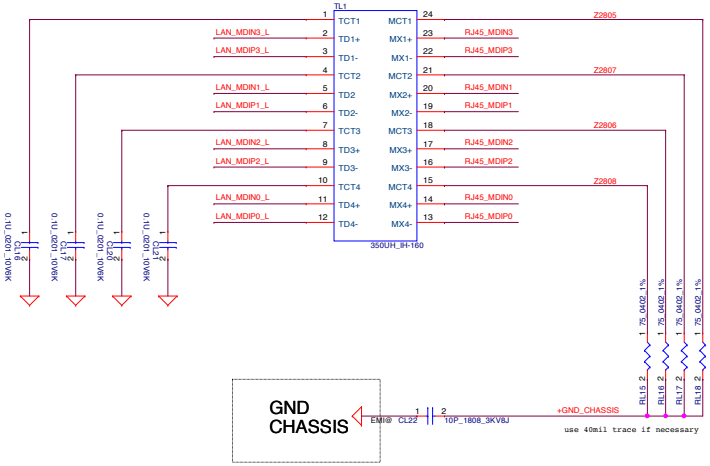

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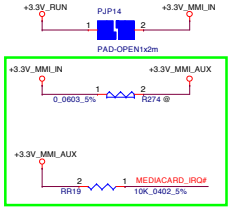
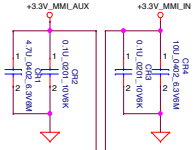
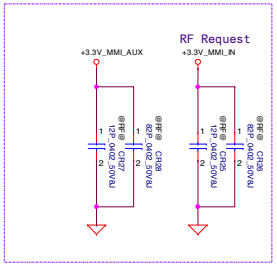
For PCIE Interface



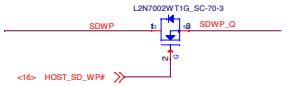
support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/off 3V3AUX)

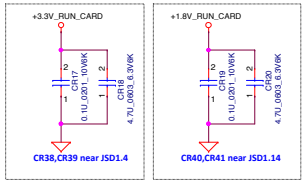
7/18 Vender suggest.

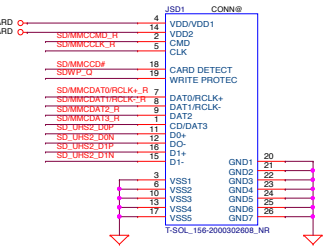




HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)







LINK SP070011U00 DONE

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Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Card Reader

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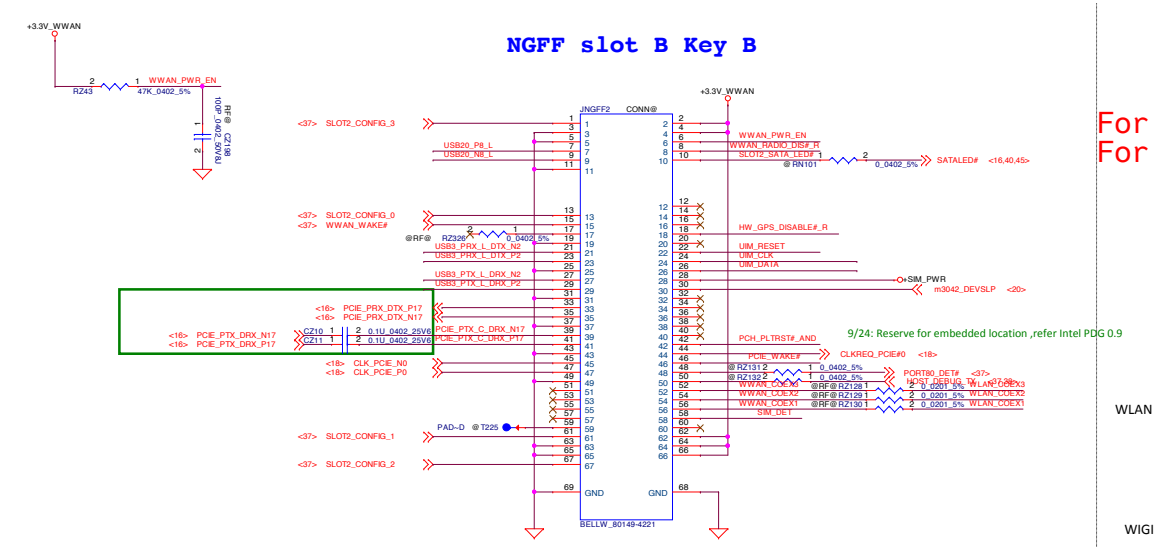
for Brekenridge 12/14/15 UMA

NGFF slot B Key B

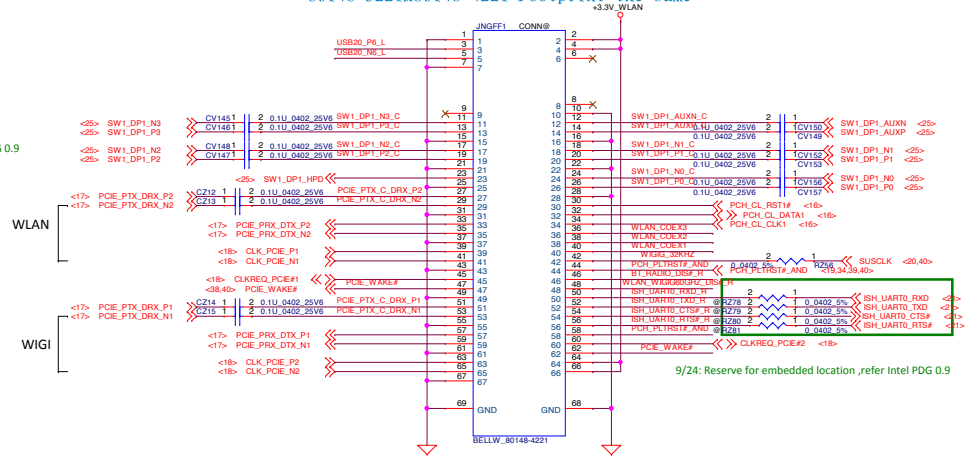


9/24: Reserve for embedded location ,refer Intel PDG 0.9

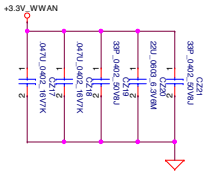
For TBT SW2_DP1
For non-TBT SW1_DP1

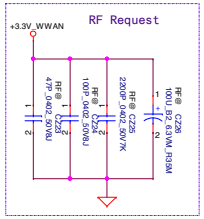
NGFF slot A Key A

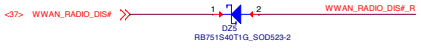
80148-3221&80148-4221 Footprint the same

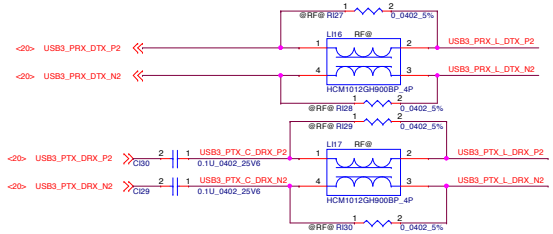


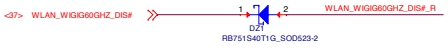
9/24: Reserve for embedded location ,refer Intel PDG 0.9

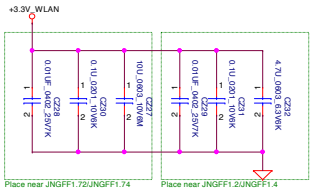




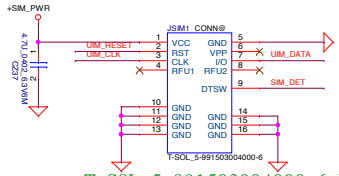




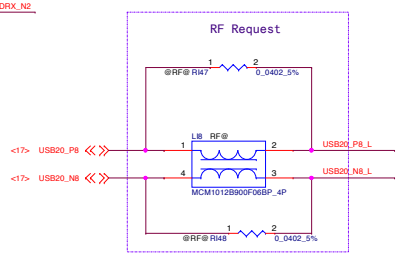


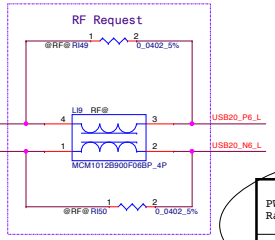


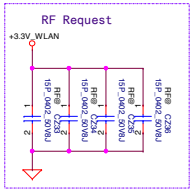
SIM Card Push-Push

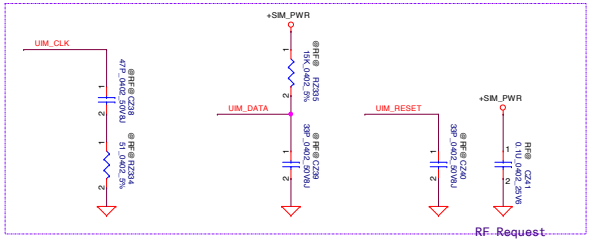


T-SOL_5-991503004000-6 LINK DONE









STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	m3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.	
Title	NGFF Card
Size	Document Number: LA-E141P
Custom	Rev: 0.2
Date:	Wednesday, June 29, 2016
Sheet	35 of 61

1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

CONN@ JSPK1

ACES_50278-00401-001

Close to UA1

Close to UA1 pin6

HDA_BIT_CLK_R

DMIC_CLK0

place close to UA1 pin3

Place closely to Pin 13.

AUD_SENSE_A

AUD_HP_NB_SENSE

Add for solve pop noise and detect issue

place at AGND and DGND plane

PJP19

PAD-OPEN1x1m

CLASS-D POWER DOWN CONTROL CIRCUIT

AUD_NB_MUTE#

HDA_RST#_R

HDA_Link is 3.3V,no need level shift circuit

RE313@one control line if DVDD is 3.3V
DE2@two control lines1

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN

Reserve for support D3 cold

2.5A

500mA

EM5209VF_SON14_2X3

UA1

ALC3246-CG_MQFN48_6X6

Place CA29 close to Codec

SLEEVE/RING2 please keep 40 mils trace width

AUD_HP_OUT_L/ AUD_HP_OUT_Rplease keep 15 mils trace width

Place RA9 close to codec

RF Request

Add this Filter to avoid other components/chips be influenced

HP-Out-Right

HP-Out-Left

Nokia-MIC

iPhone-MIC

Global Headset

Universal Jack

SINGA_2SJ3095-136111F

Normal

Open

Only BR15U UMA use LA2,LA3,because 6L

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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: Codec ALC3246

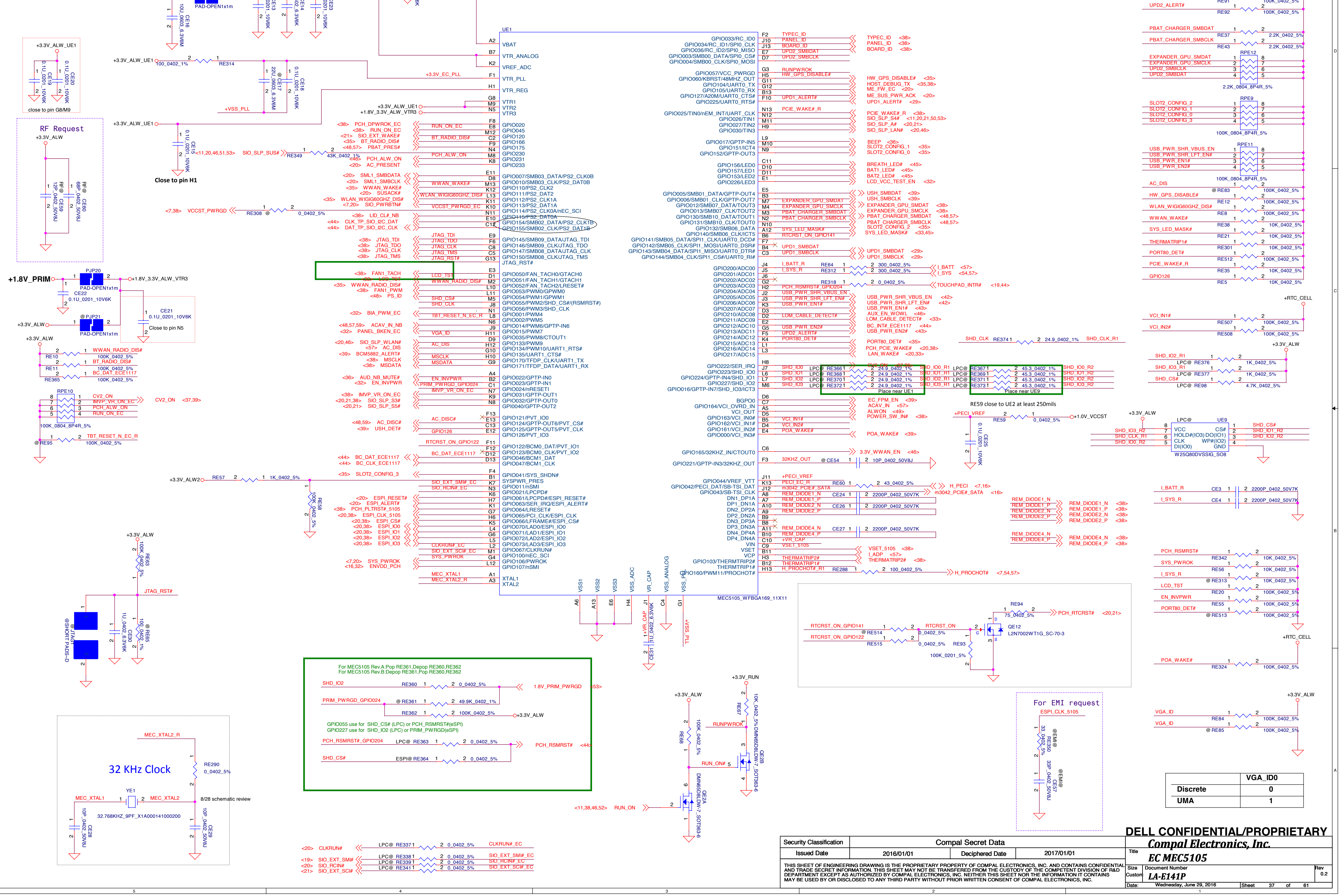
Size: C | Document Number: LA-E141P | Rev: 0.2

Date: Wednesday, June 29, 2016 | Sheet 36 of 61

	GPIO223	GPIO224	GPIO227	GPIO016	GPIO056	GPIO055
eSPI	NA	NA	*PRIM_PWRGD	NA	NA	PCH_RSMRST#
LPC	SHD_IO0	SHD_IO1	SHD_IO2	SHD_IO3	SHD_CLK	SHD_CS#

* For Version B IC

	GPIO204	GPIO011	GPIO100	GPIO021	GPIO067
eSPI	NA	NA	NA	SIO_RCIN#	NA
LPC	RSMRST#	SIO_EXT_SMI#	SIO_EXT_SCI#	LPCPD#	CLKRUN#



	VGA_ID0
Discrete	0
UMA	1

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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

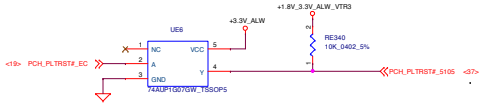
Compal Electronics, Inc.

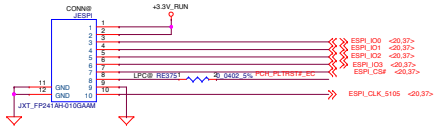
Title: ***EC MEC5105***

Size: Custom | Document Number: ***LA-E141P*** | Rev: 0.2

Date: Wednesday, June 29, 2016 |

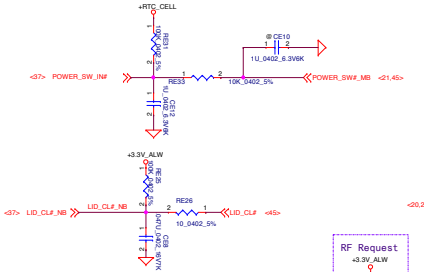
For BR UMA

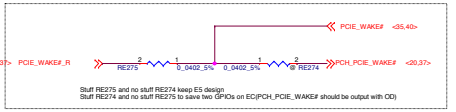


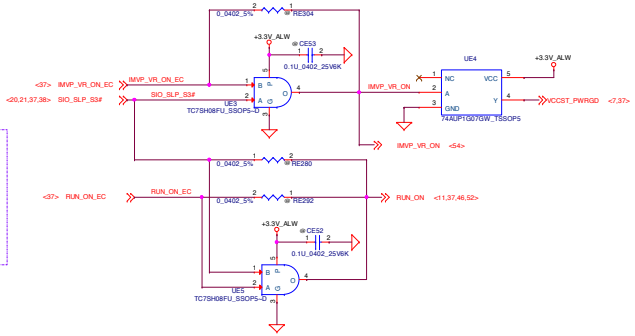


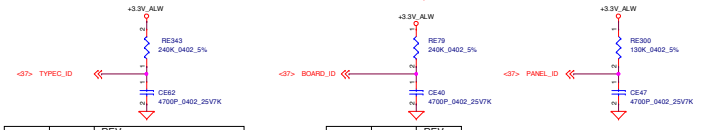
PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	

LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_IO0
4	LPC_LAD1	ESPI_IO1
5	LPC_LAD2	ESPI_IO2
6	LPC_LAD3	ESPI_IO3
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK









RE343	CE62	REV
* 240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	.
2K	4700p	
1K	4700p	

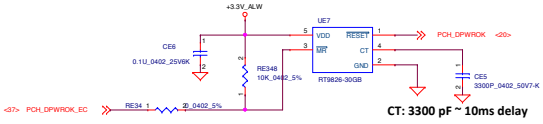
RE79	CE40	REV
* 240K	4700p	X00
130K	4700p	
62K	4700p	
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

RE300	CE47	PANEL SIZE
240K	4700p	12"
130K	4700p	14"
33K	4700p	BR15 H
4.3K	4700p	BR15 P

PD_ACE_DET# rise time is measured from 5%~68%.

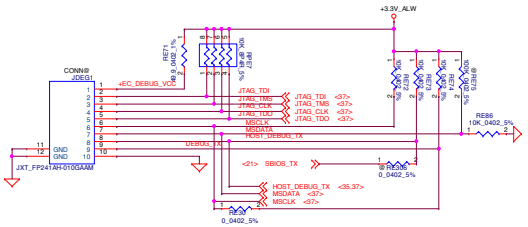
BOARD_ID rise time is measured from 5%~68%.

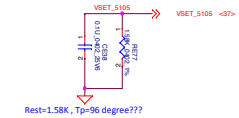
PANEL_ID rise time is measured from 5%~68%.

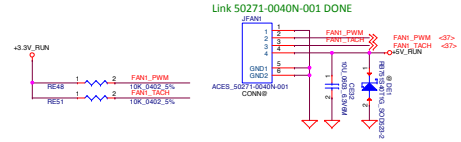


CT: 3300 pF ~ 10ms delay

Reset Threshold Level 3.0V





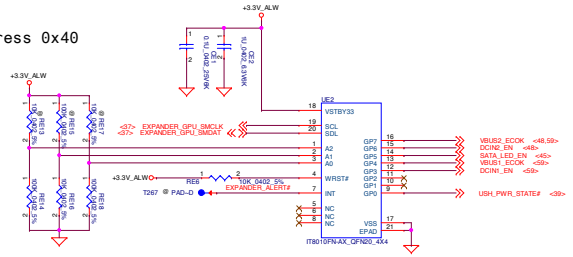


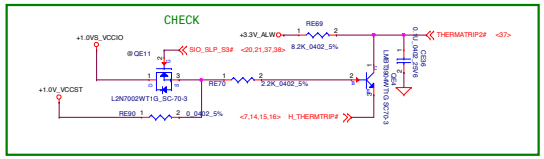
Control Byte

0	1	0	0	A2	A1	A0	R/W

R/W = 0 = Wire
R/W = 1 = Read

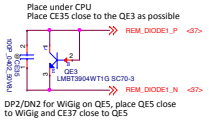
SMBus address 0x40



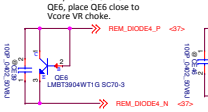


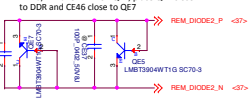
Thermal diode mapping

5105 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)



DP2/DN2 for WiGig on QE5, place QE5 close to WiGig and CE37 close to QE5





Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: MEC5105 SUPPORT

Size: Custom | Document Number: LA-E141P | Rev: 0.2

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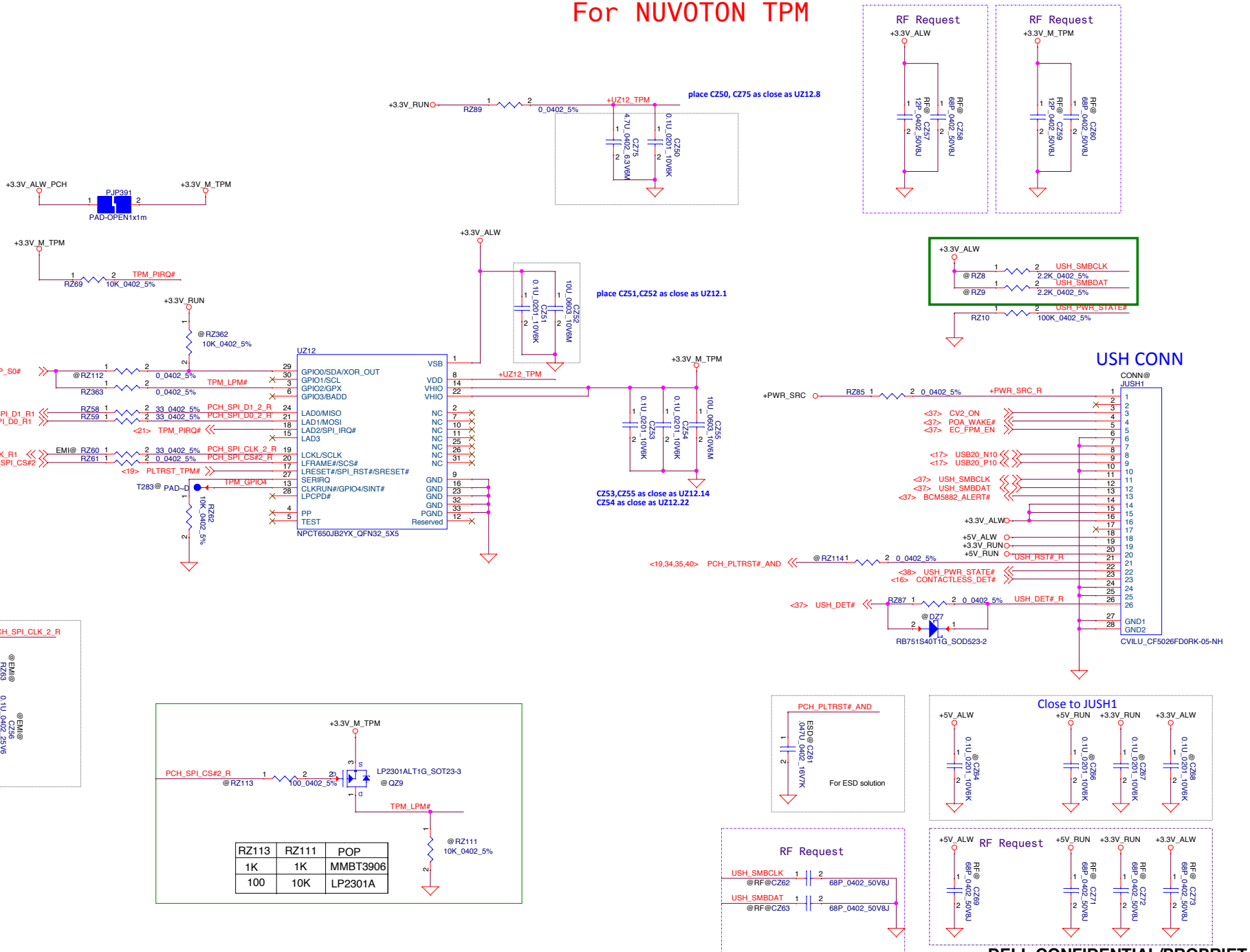
For NUVOTON TPM



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title: *USH & TPM*

Size: Custom | Document Number: *LA-E141P* | Rev: 0.2

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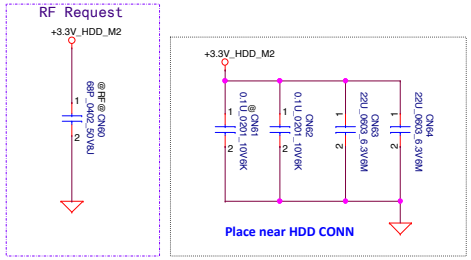
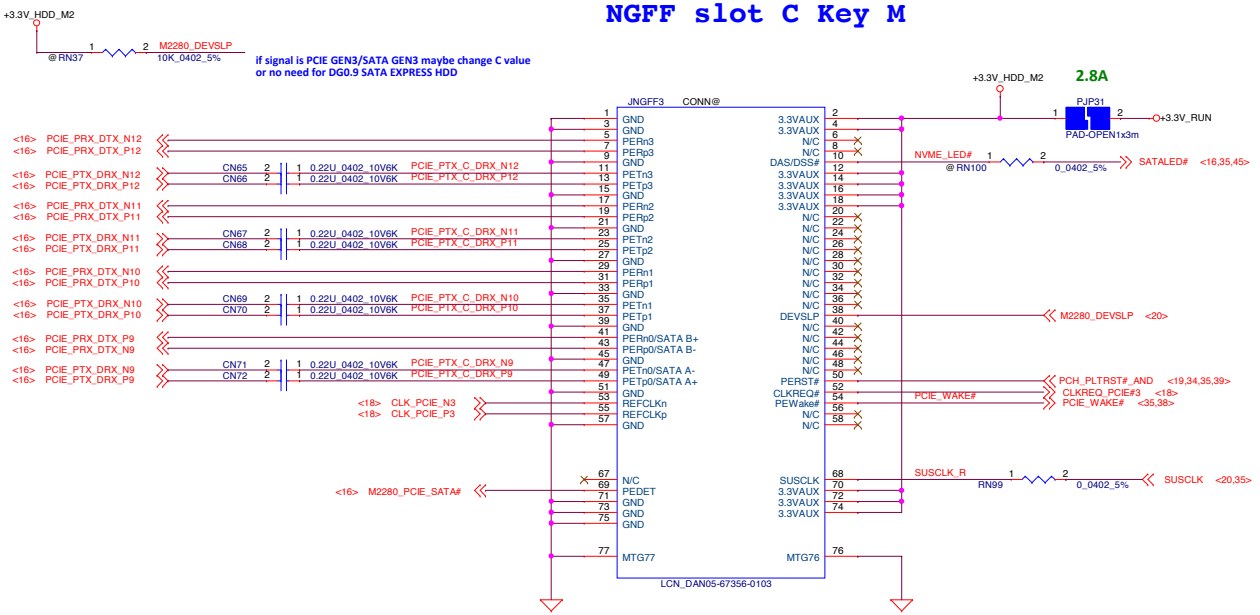
For Breckenridge 15



2280 SSD

NGFF slot C Key M



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.	
Title	M2 2280 Socket
Size	B
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Date:	Wednesday, June 29, 2016
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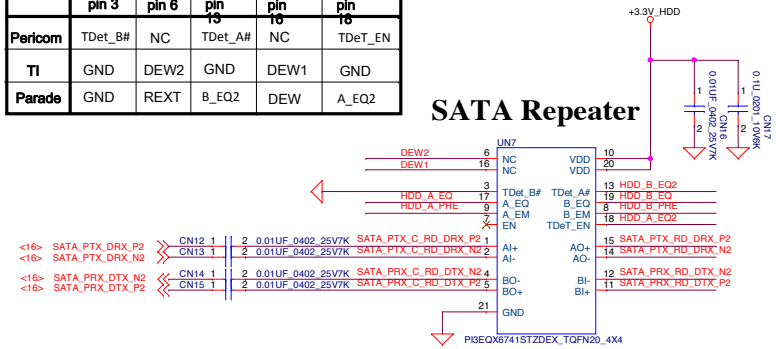
	pin 3	pin 6	pin 15	pin 16	pin 18
Pericom	TDet_B#	NC	TDet_A#	NC	TDeT_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

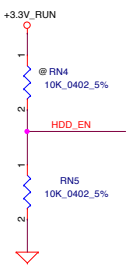
SATA Repeater



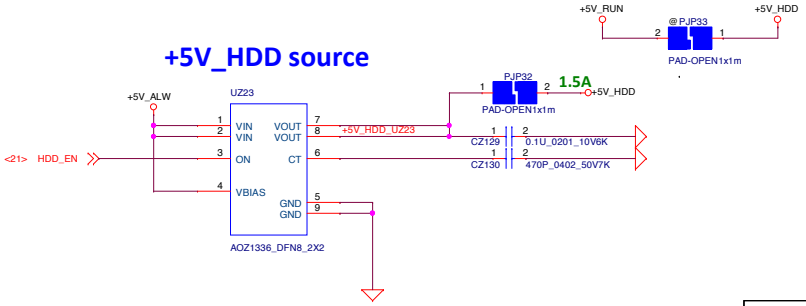
	HDD_A_EQ PIN17	HDD_B_EQ PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
Pericom PI3EQX6741ST	PD (RN13)	PD (RN16)	PD (RN83)	PD (RN23)	NC	NC	PD (RN9)	PD (RN11)
TI SN75LVCP601	PD (RN13)	NC	PD (RN83)	PD (RN23)	NC (IPU)	NC (IPU)	PH (RN8)	PH (RN10)
Parade PS8527C	PD (RN13)	PD (RN16)	PD (RN83)	PD (RN23)	NC (1/2 VDD)	PD (RN19)	NC (1/2 VDD)	NC (1/2 VDD)

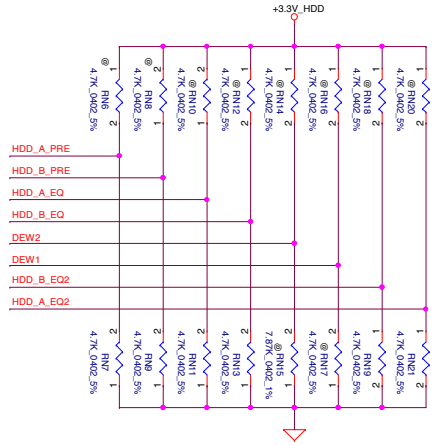
			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0	3dB	3dB	0	0dB	0dB
		NC	6dB	6dB	NC		
		1	9dB	9dB	1	1.5dB	1.5dB
2nd	TI	0	7dB	7dB	0	0dB	0dB
		NC	0dB	0dB	NC	-4dB	-4dB
		1	14dB	14dB	1	-2dB	-2dB
3rd	Parade	EQ2 EQ1	A_EQ	B_EQ		A_EM	B_EM
		(M = VDD/2)					
		0 M	2.4dB	2.4dB			
		0 0	7.4dB	7.4dB			
		0 1	14.4dB	14.4dB	0	0dB	0dB
		M M	12.2dB	12.2dB	M	-3.5dB	-3.5dB
		M 0	9.4dB	9.4dB	1	-1.5dB	-1.5dB
		M 1	13.3dB	13.3dB			
		1 M	6.2dB	6.2dB			
		1 0	11.2dB	11.2dB			
		1 1	5dB	5dB			

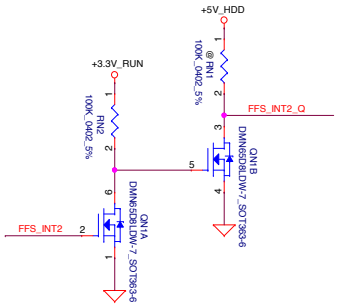
* red color is current setting



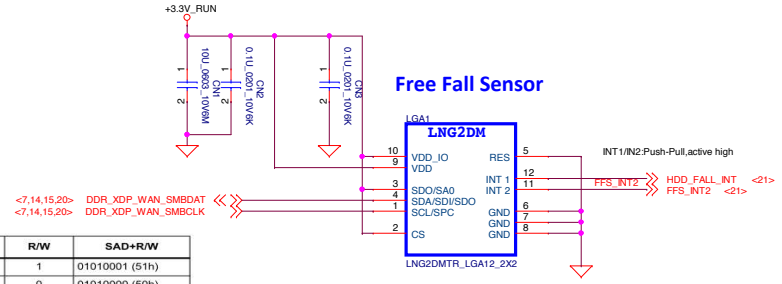
+5V_HDD source



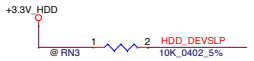


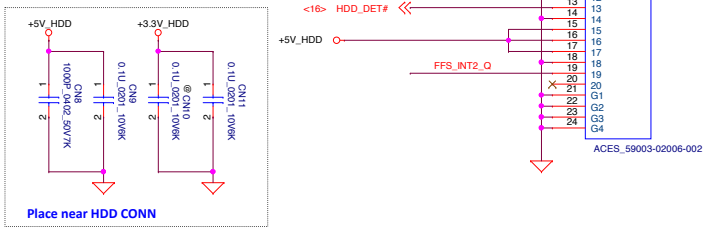


Free Fall Sensor



Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)





Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title: HDD CONN

Size	Document Number	Rev
B	LA-E141P	0.2

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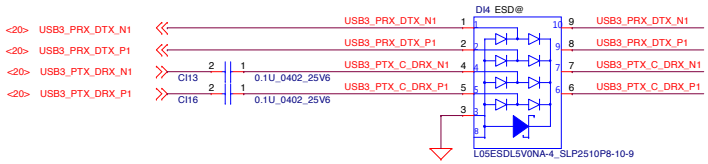
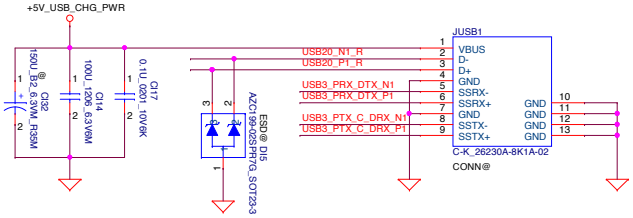
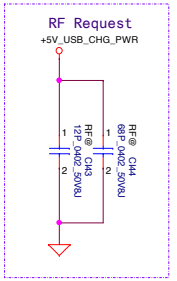
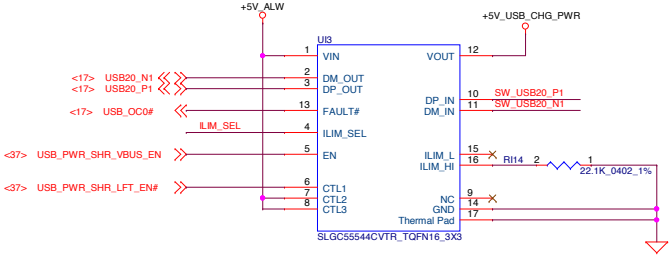
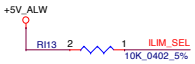
For PWR SW + Charger combine IC

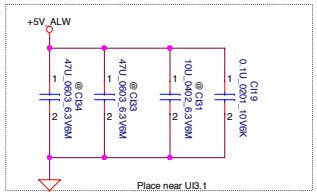












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Compal Electronics, Inc.

Title	USB SW		
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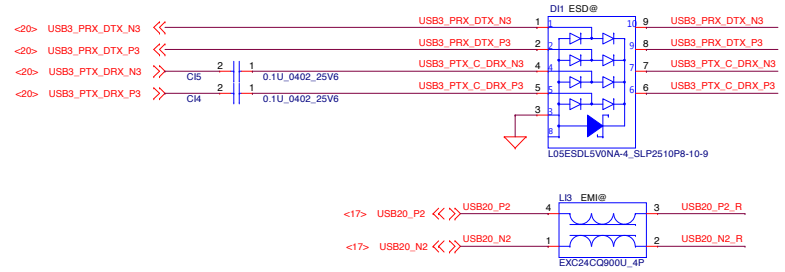
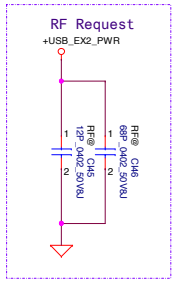
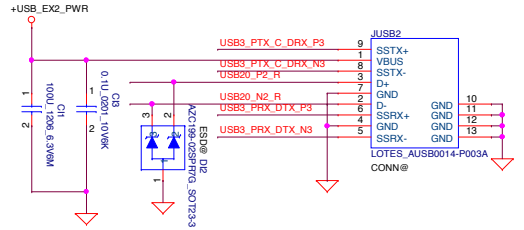
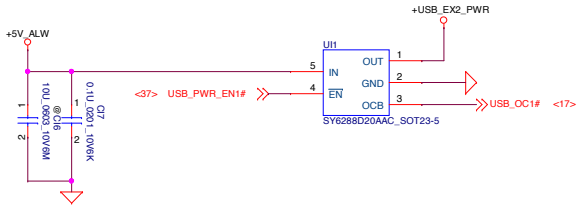
For Breckenridge 14&15/Steamboat 14

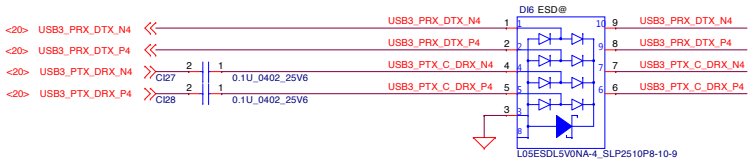


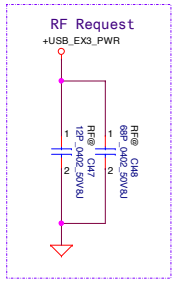


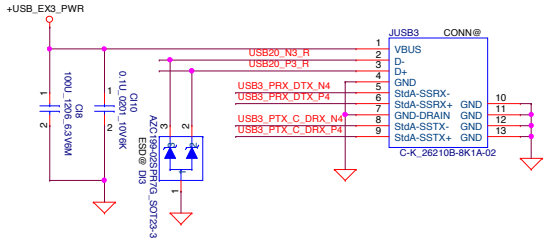


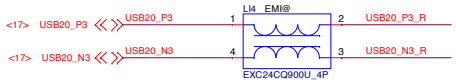
DFB request:
main SM070003Z00 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm

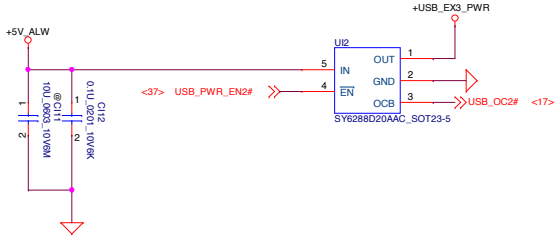












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Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: JUSB2&JUSB3

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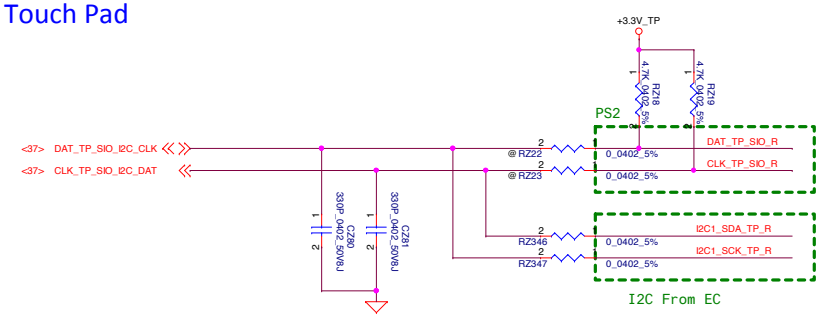
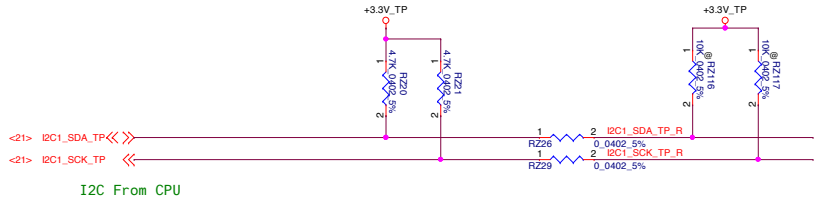
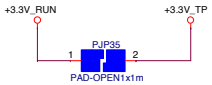
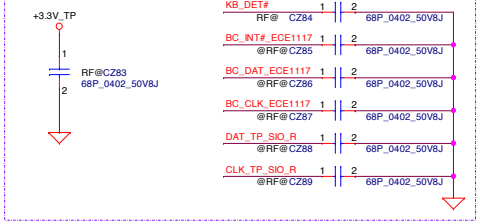
Touch Pad



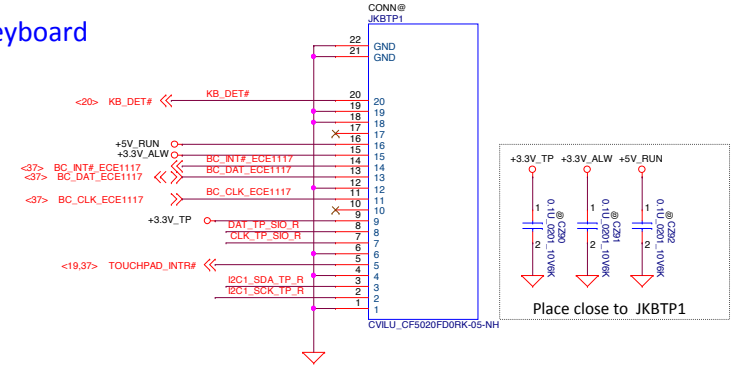


Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues

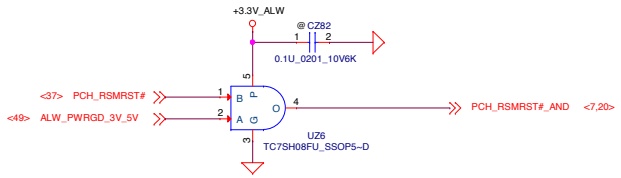




Keyboard



RSMRST circuit



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Compal Electronics, Inc.

Title: *Keyboard*

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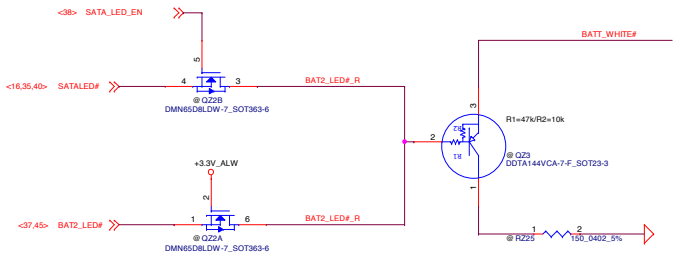
HDD LED MUX

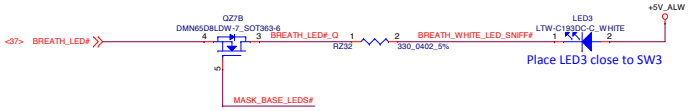
means EC can switch battery white led and HDD LED by hot key "Fn+H"

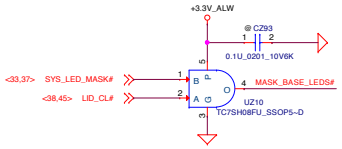


Battery LED

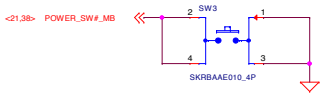
Breath LED

LED P/N change to SC50000FL00 from SC50000BA00

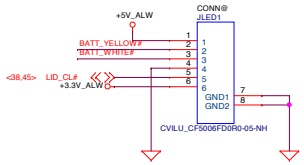




POWER & INSTANT ON SWITCH



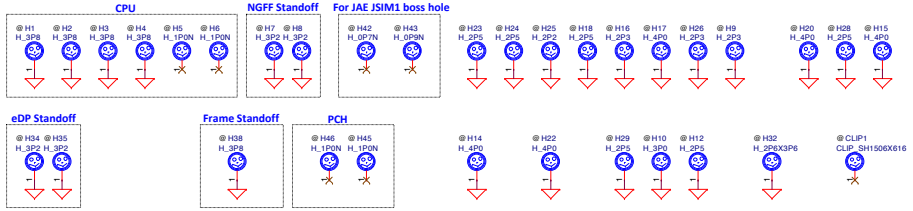
LED board CONN



Fiducial Mark

@ FD1 FIDUCIAL MARK~D
@ FD2 FIDUCIAL MARK~D
@ FD3 FIDUCIAL MARK~D
@ FD4 FIDUCIAL MARK~D

LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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Compal Electronics, Inc.

Title: PAD, LED

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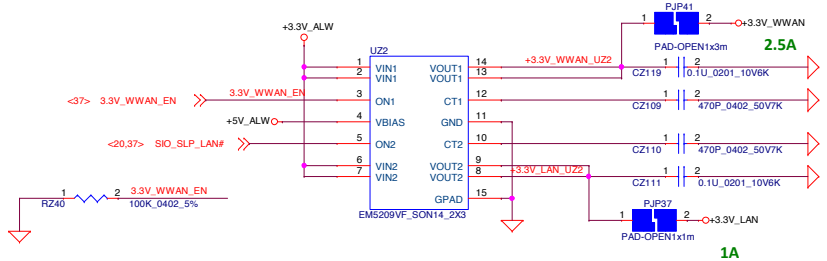
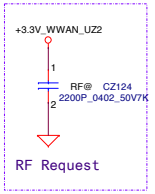
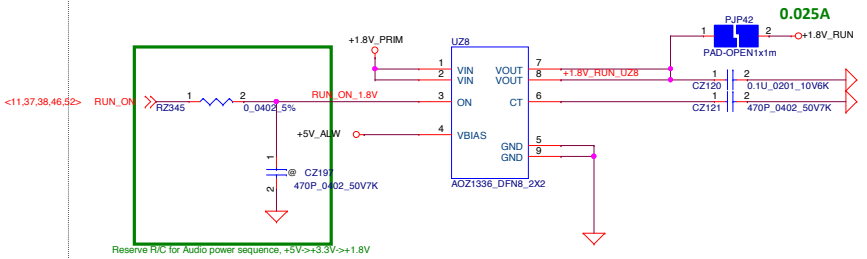
+3.3V_WWAN/+3.3V_LAN source

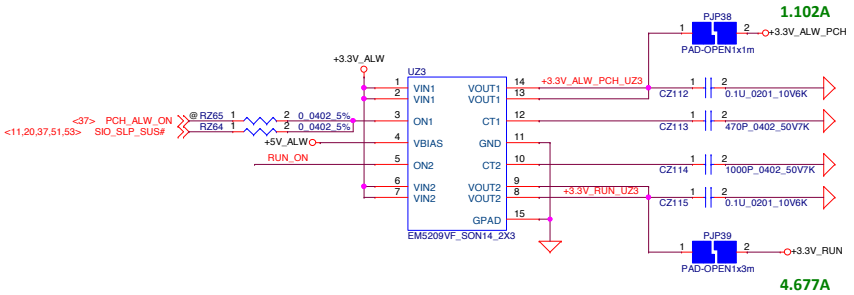




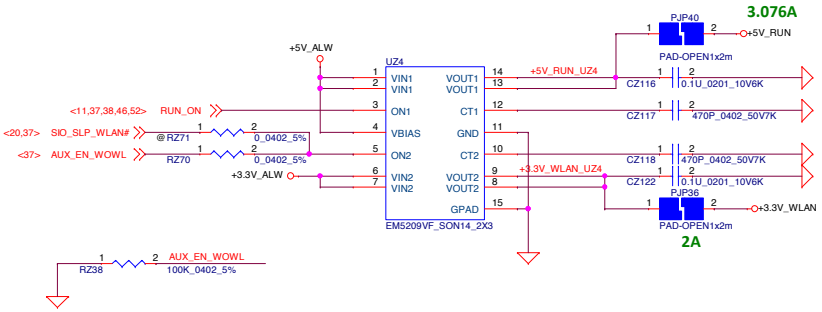
+1.8V_RUN source



+3.3V_ALW_PCH/+3.3V_RUN source



+5V_RUN/+3.3V_WLAN source



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Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: Power control

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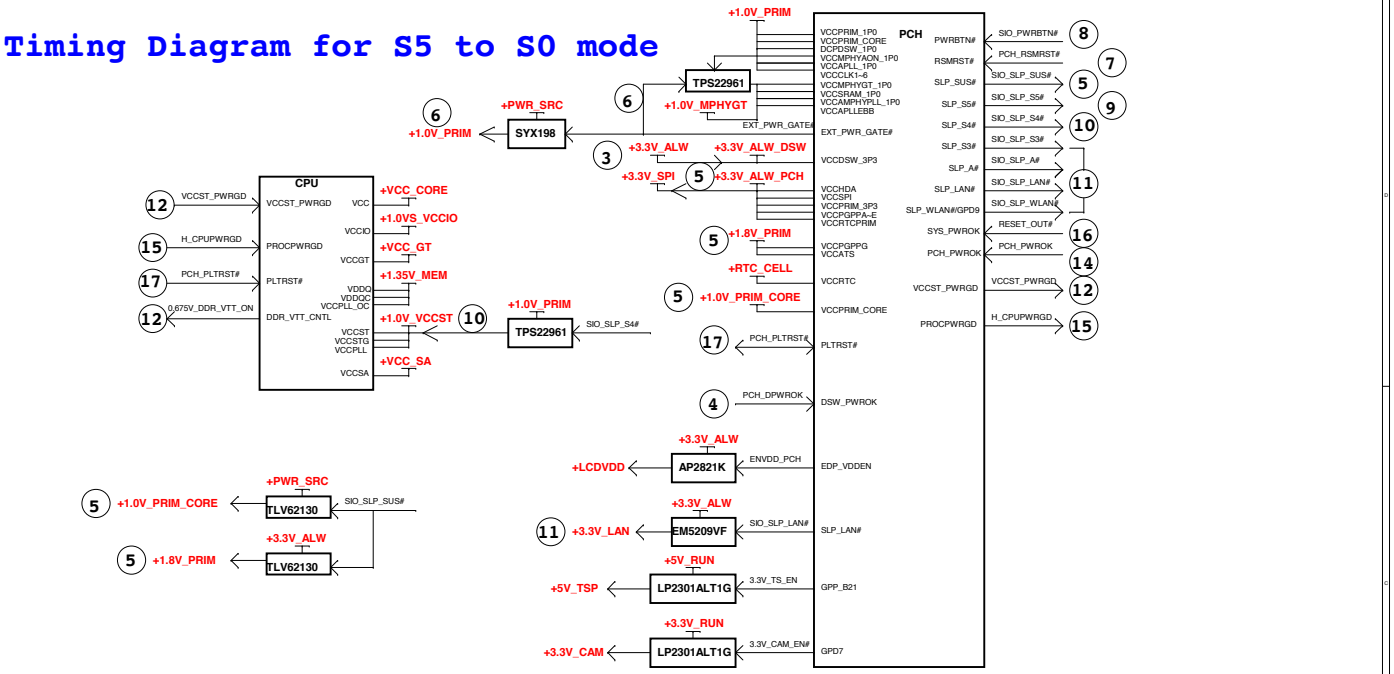
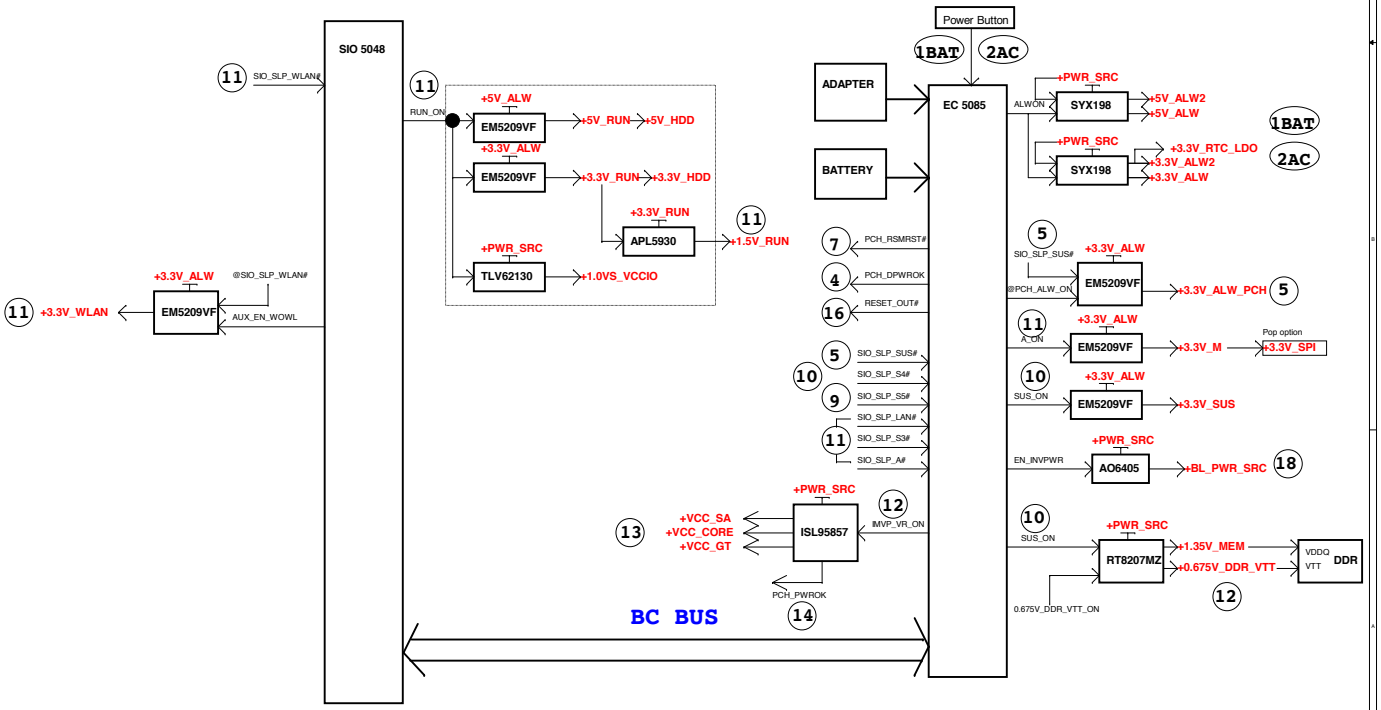
Timing Diagram for S5 to S0 mode





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Issued Date	2016/01/01
Deciphered Date	2017/01/01

Title	Power Sequence		
Size	Document Number		Rev
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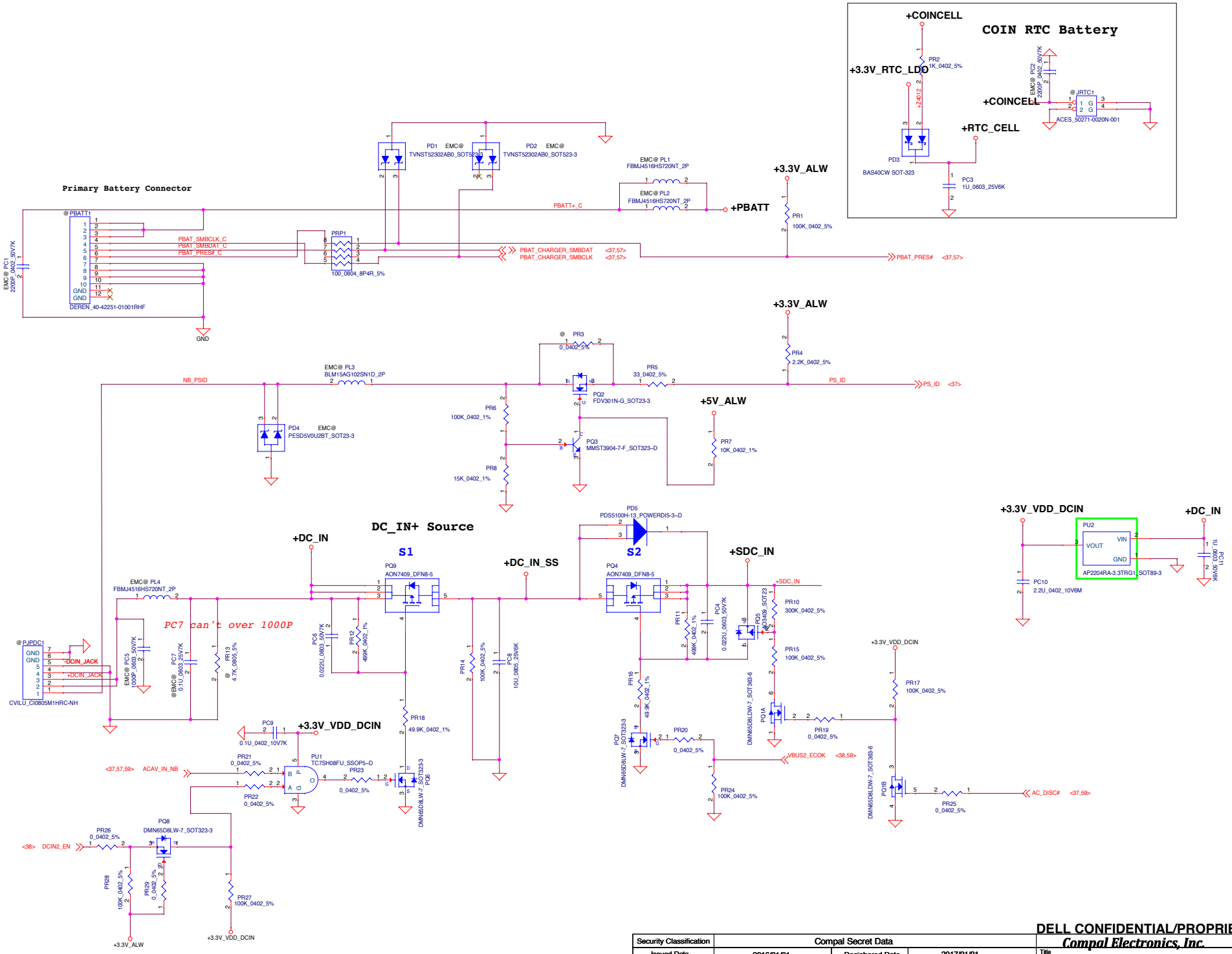

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Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Title	+DCIN		
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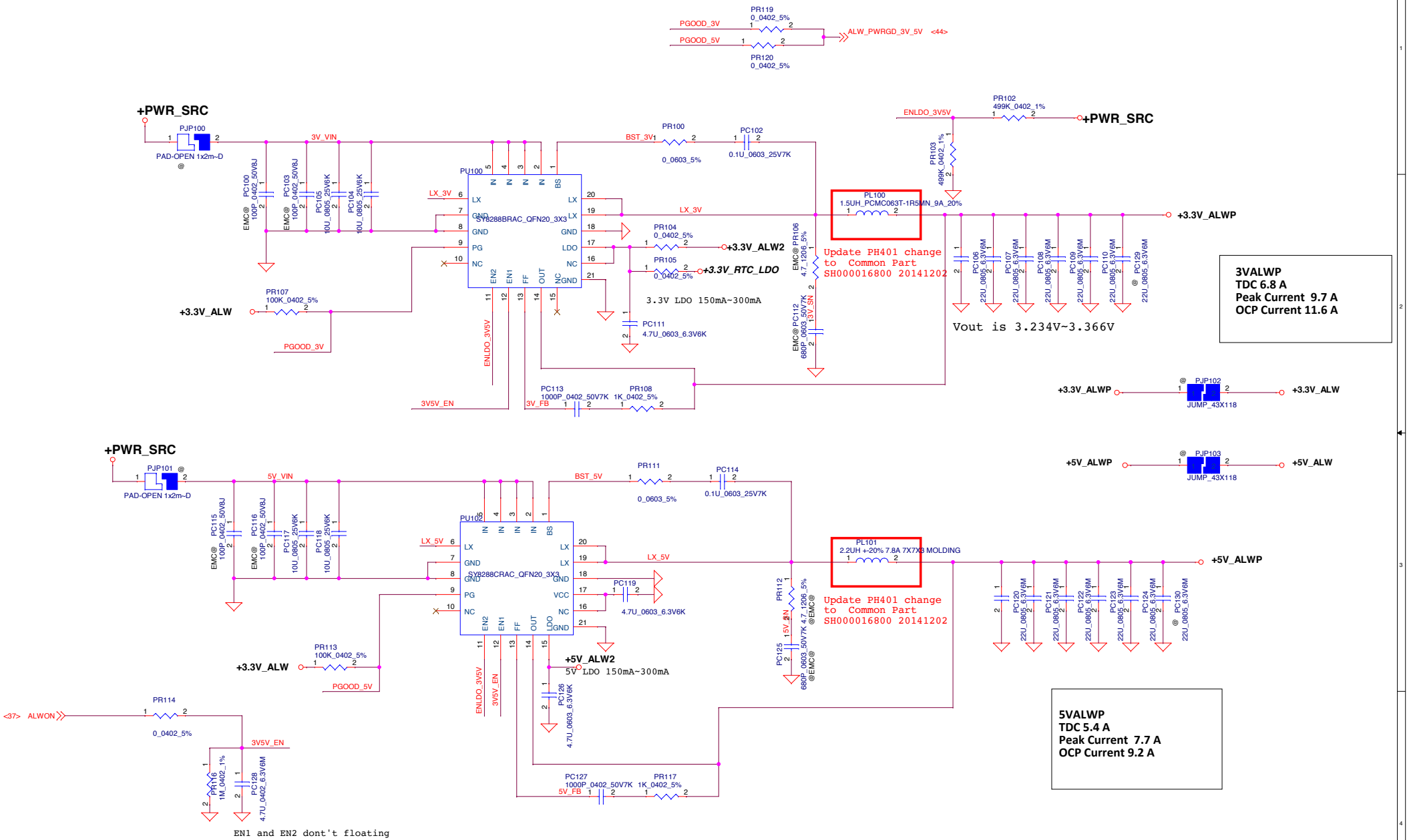

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Title: +5V_ALW/3.3V_ALW

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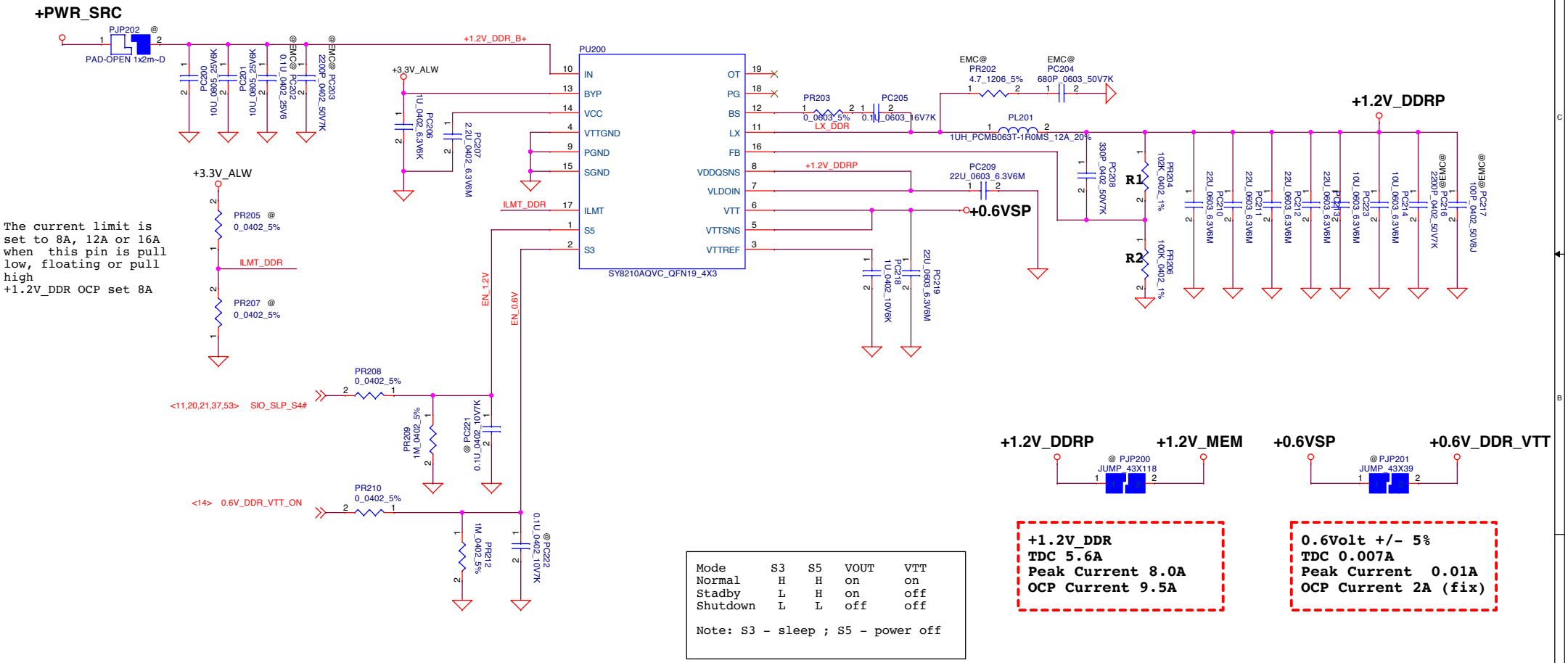

Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

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Title: +1.2V_MEN/+0.6V_DDR_VTT

Size: Custom | Document Number: LA-E141P | Rev: 0.2

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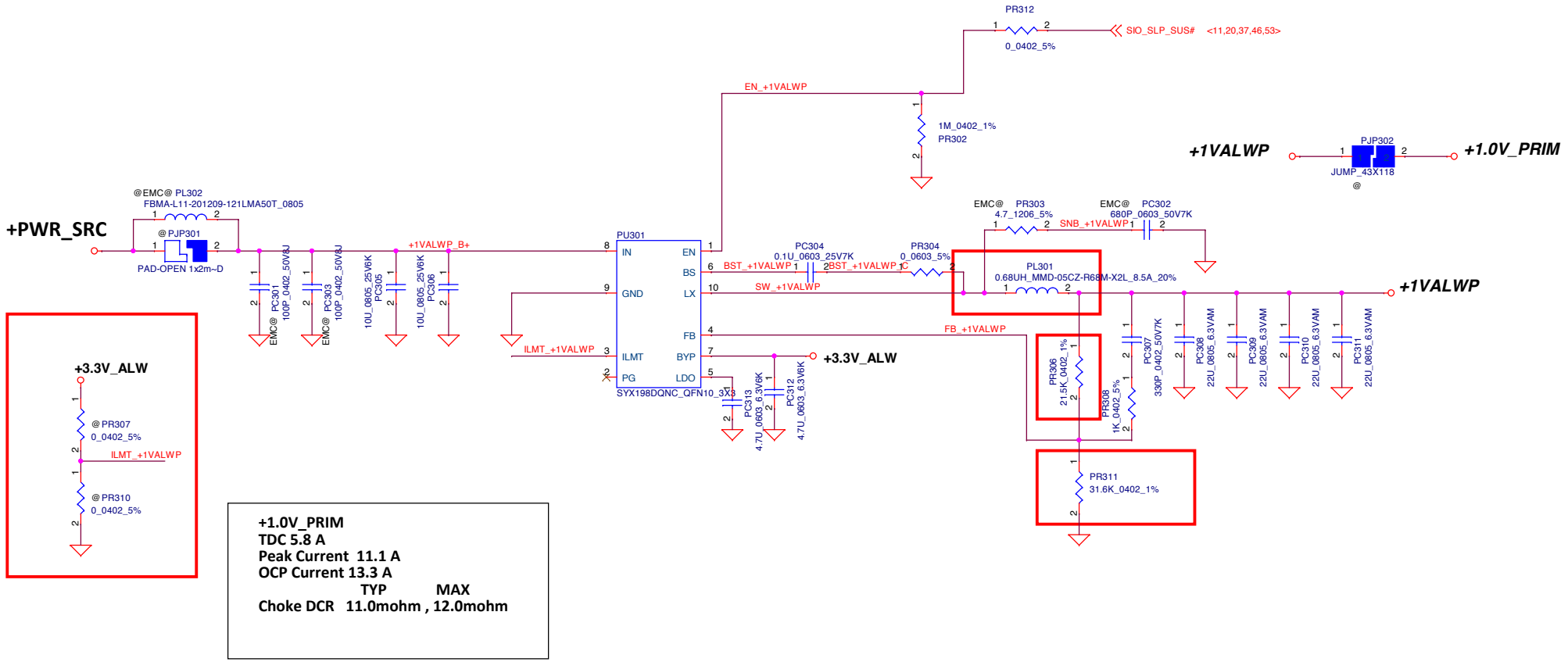

+1.0V_PRIM
TDC 5.8 A
Peak Current 11.1 A
OCP Current 13.3 A

	TYP	MAX
Choke DCR	11.0mohm ,	12.0mohm

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Compal Electronics, Inc.

Title: +1VALWP

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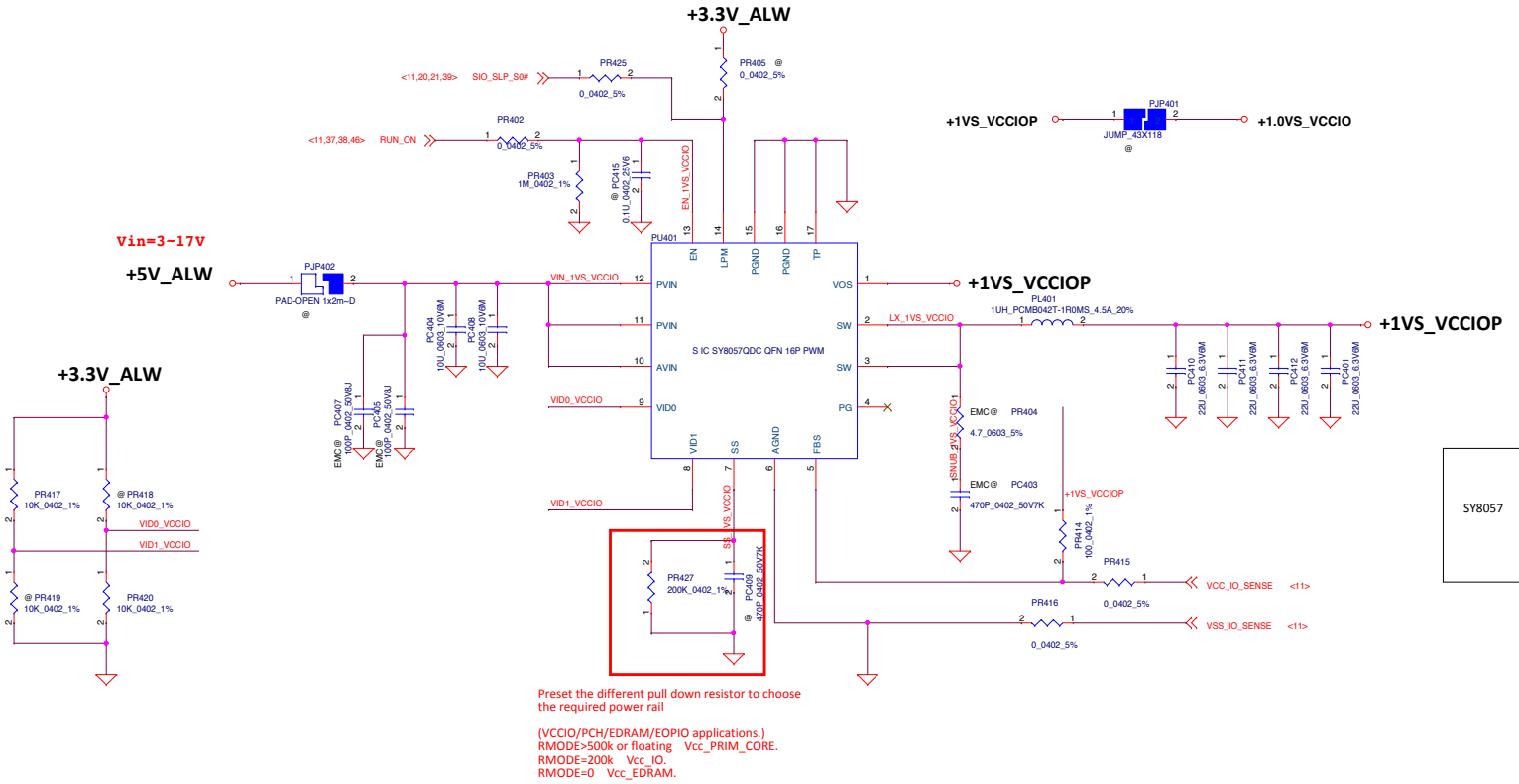

+1.0VS_VCCIO
TDC 3.9A
Peak Current 5.5 A
OCP Current 6.6 A Fix by IC

	TYP	MAX

	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
SY8057	0	X	X	0(LPM)
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Title	+1VS_VCCIO		
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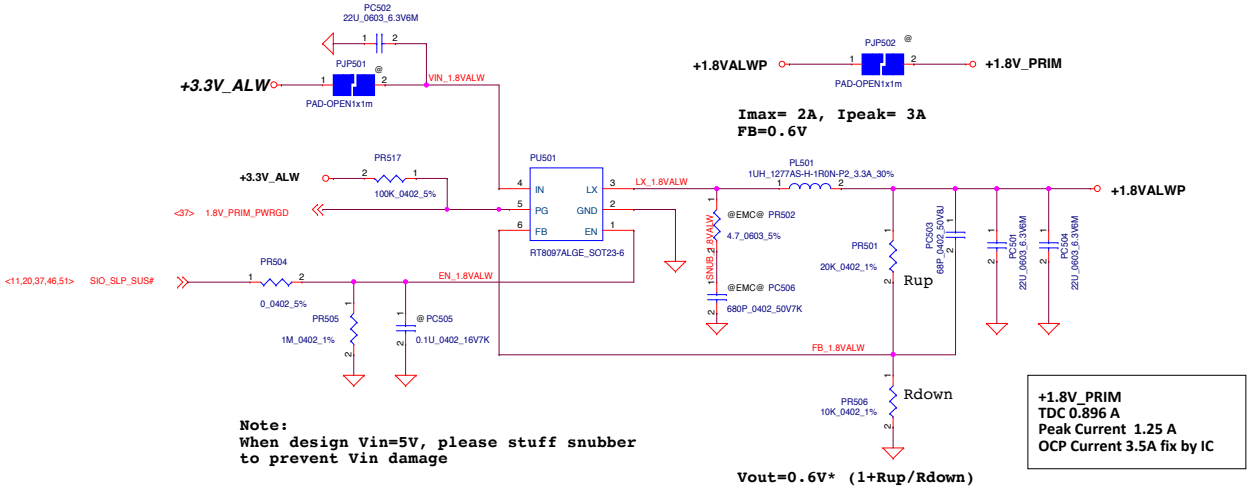

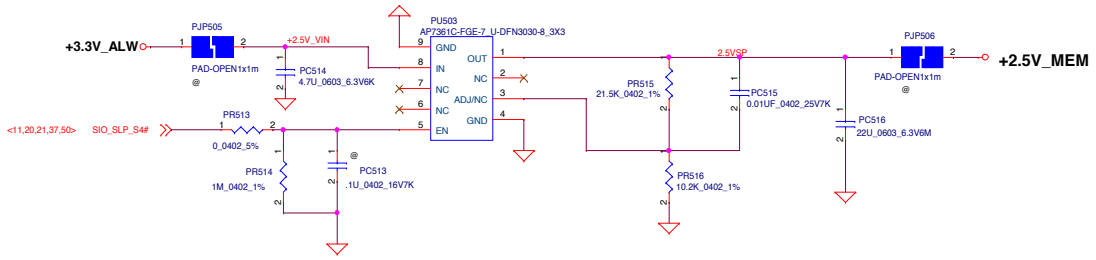

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Title	+1.8VALWP/+1.5VSP/2.5V_MEN		
Size C	Document Number LA-E141P		Rev 0.2
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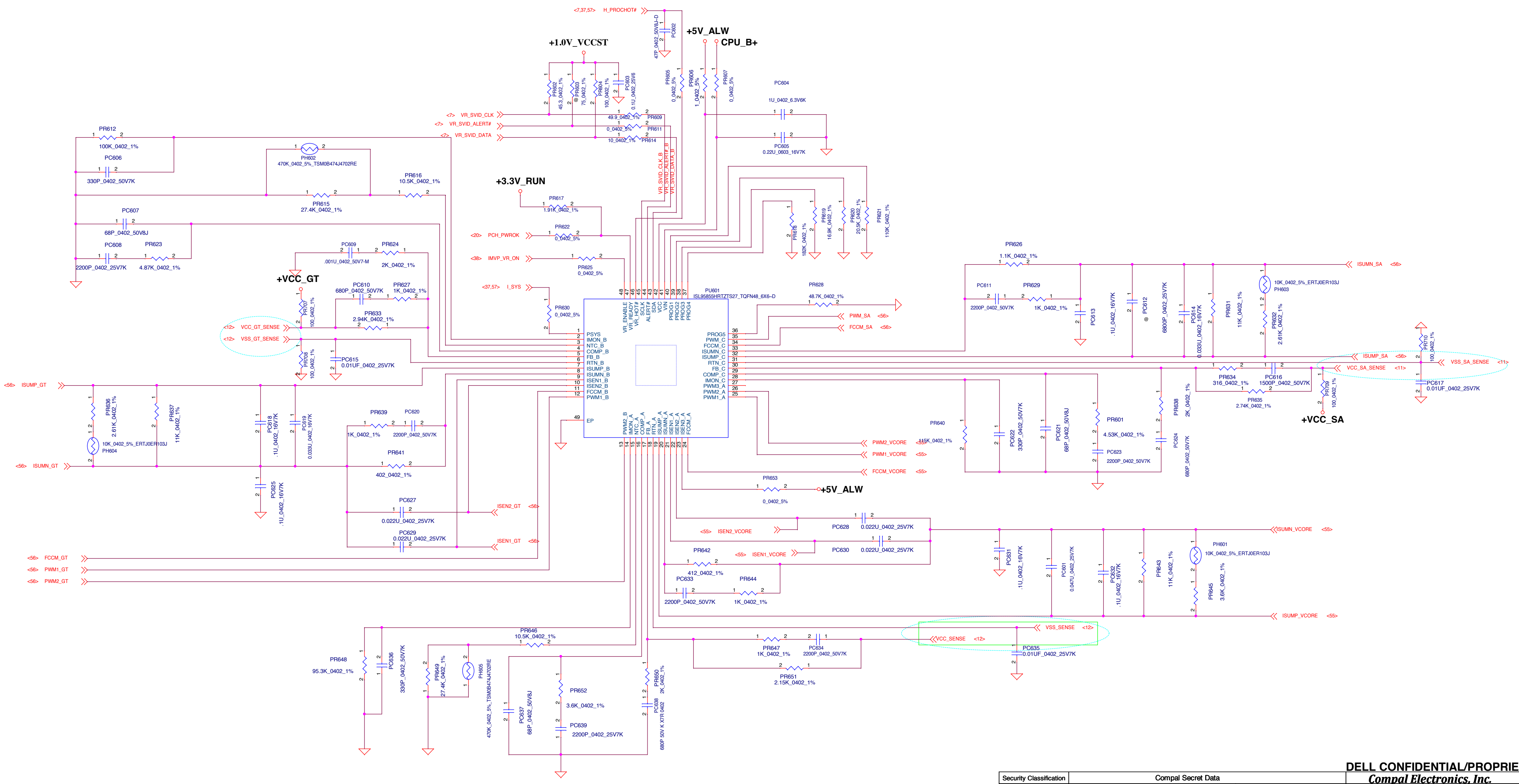

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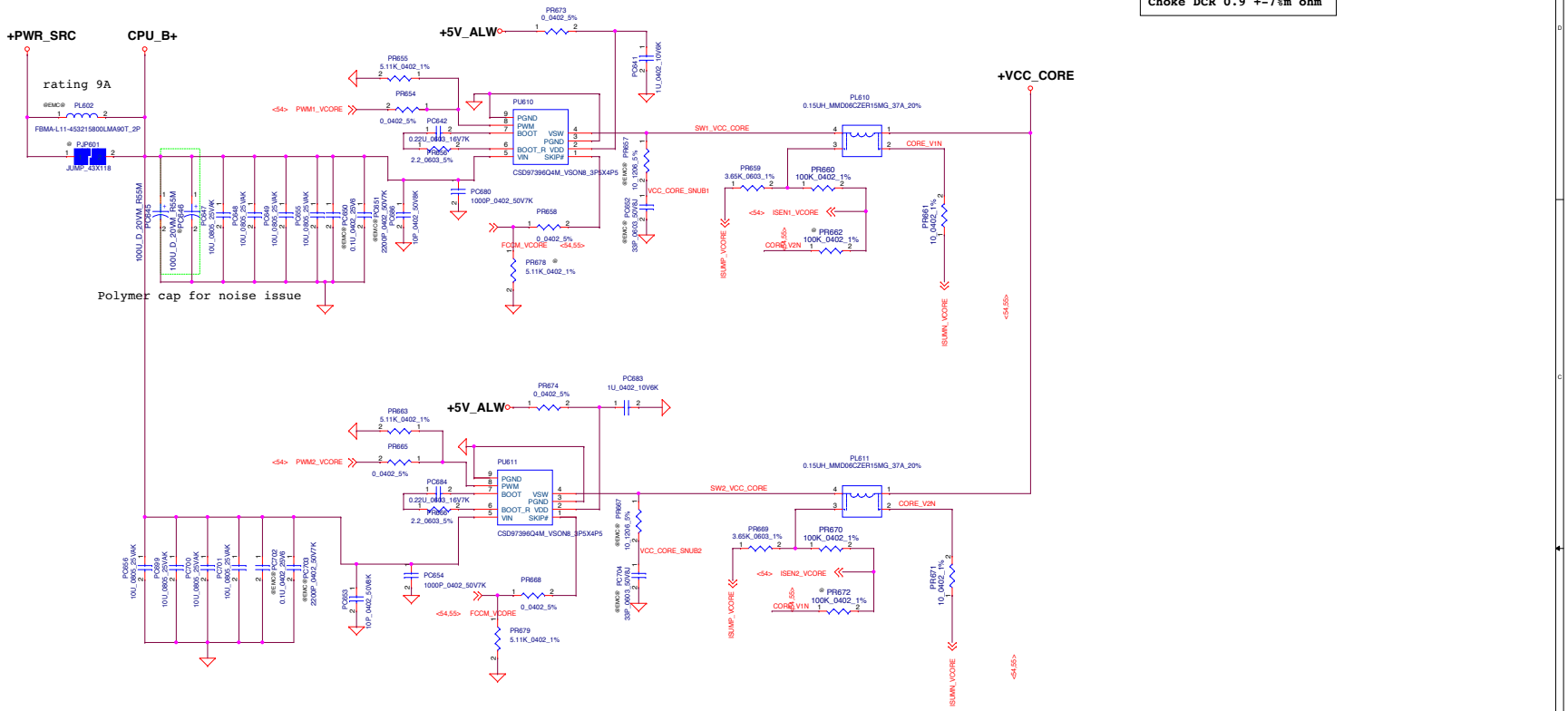
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title	***VCORE_ISL95855***	
Size: Custom	Document Number: ***LA-E141P***	Rev: 0.2
Date: Wednesday, June 29, 2016	Sheet 54 of 61	



Compal Electronics, Inc.

Title	VCORE		
Size	Document Number		Rev
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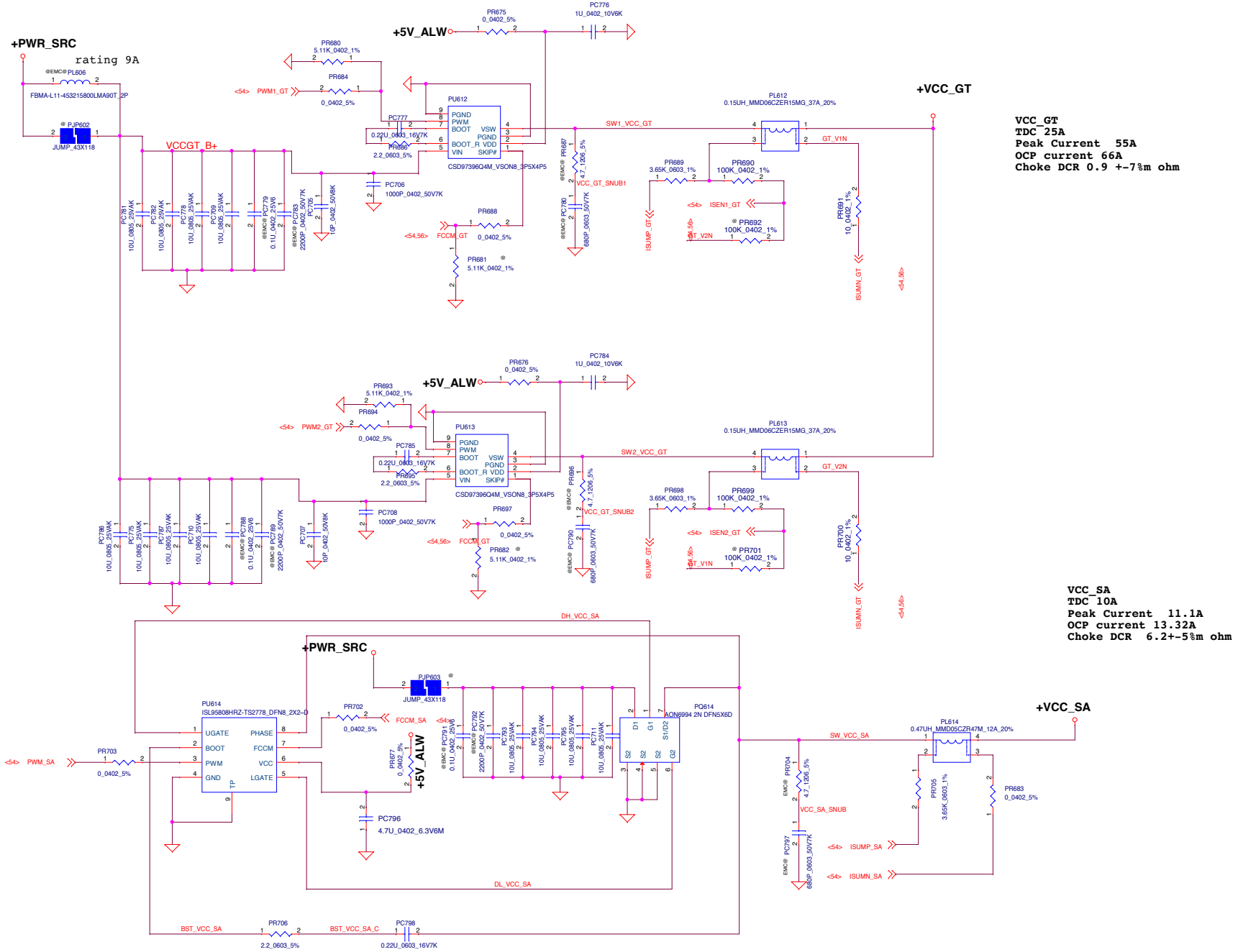

VCC_GT
TDC 25A
Peak Current 55A
OCP current 66A
Choke DCR 0.9 +-7%m ohm

VCC_SA
TDC 10A
Peak Current 11.1A
OCP current 13.32A
Choke DCR 6.2+-5%m ohm

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Title	VGT_VSA		
Size	Document Number		Rev
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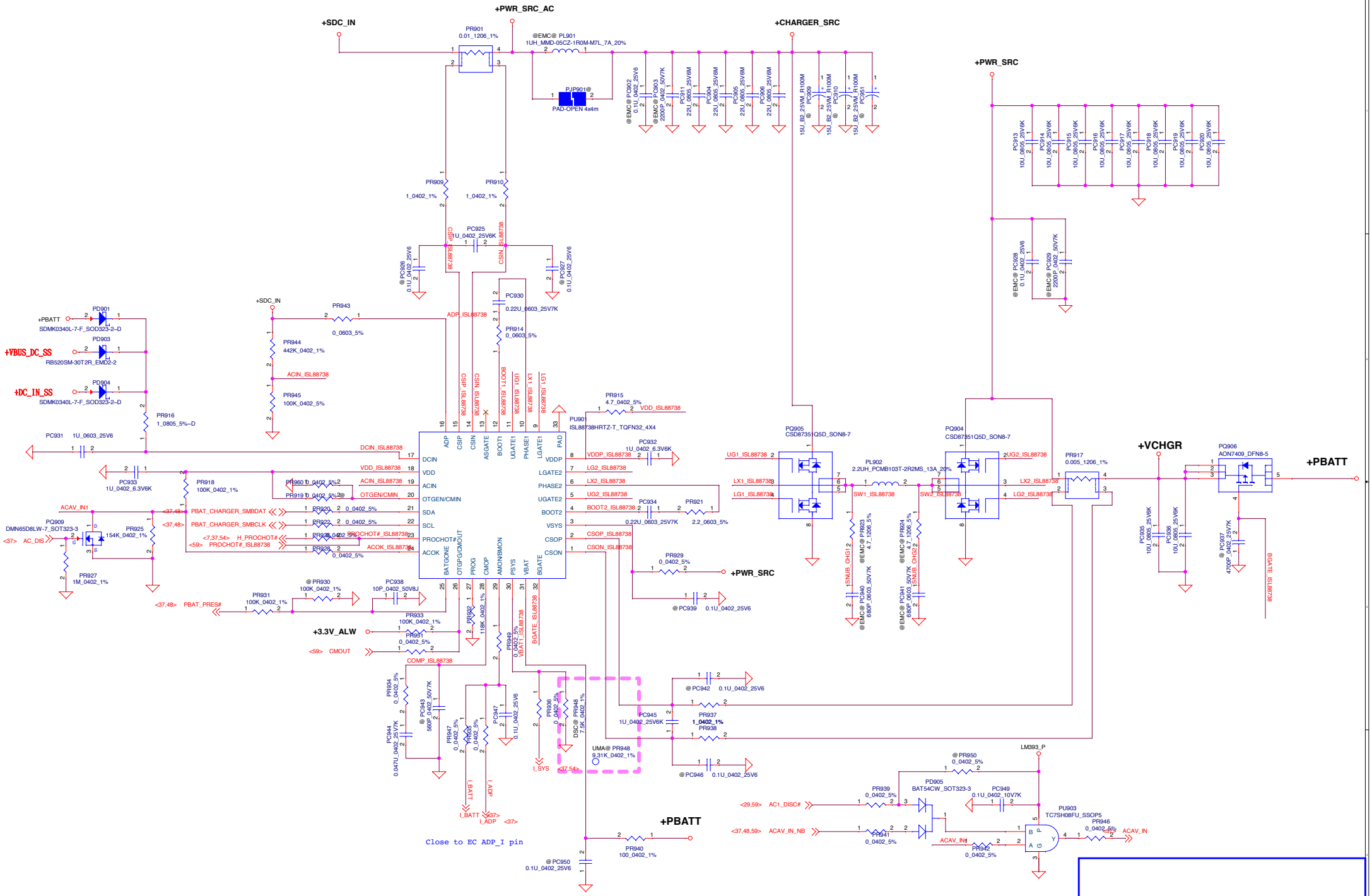

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Title: *PWR_CHARGER_ISL9237 (Colay)*

Size	Document Number	Rev
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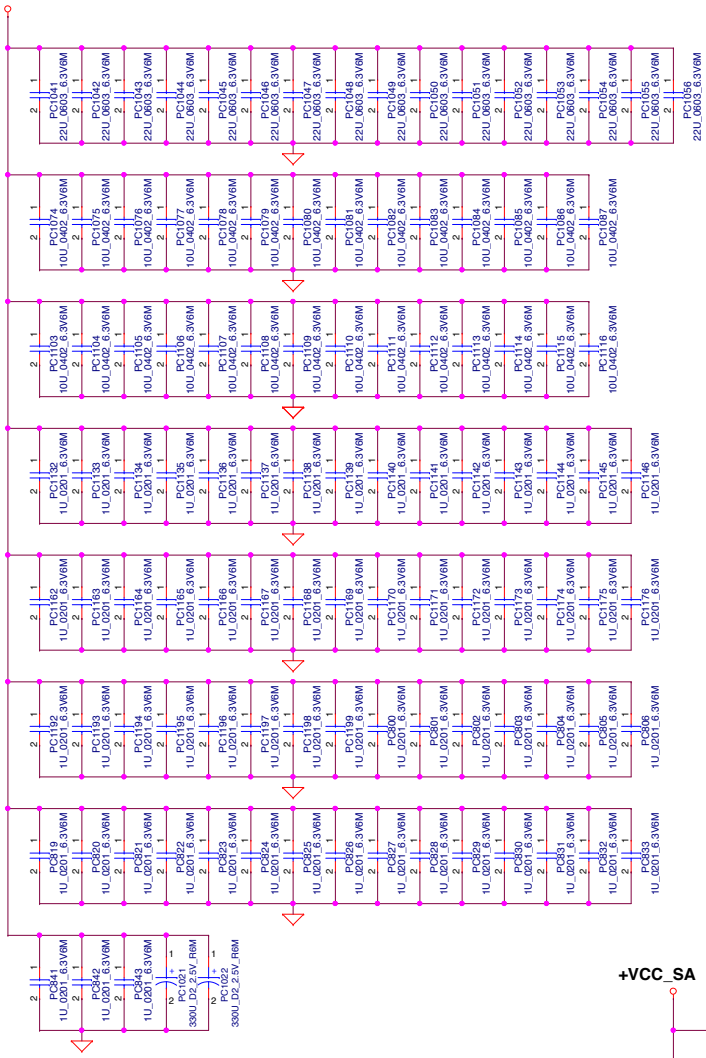
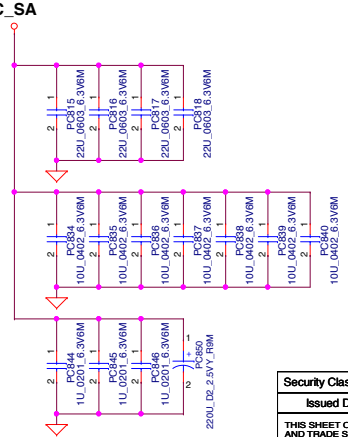
VCC_CORE Place on CPU
Back Side.
22U_0603 * 8 pcs + 10U_0402*28 pcs + 1U_0201*35 pcs
Primary Side.
22U_0603 * 8 pcs+330u_D2*2 pcs

+VCC_CORE



VCC_SA Place on CPU
Back Side.
22U_0603 * 2 pcs + 10U_0402*7 pcs + 1U_0201*3 pcs
Primary Side.
22U_0603 * 2 pcs + 220u_D2*1 pcs

+VCC_SA



VCC_GT Place on CPU
Back Side.
22U_0603 * 8 pcs +10U_0402*35 pcs +1U_0201*68 pcs
Primary Side.
22U_0603 * 12 pcs +470u_D2*2 pcs

+VCC_GT

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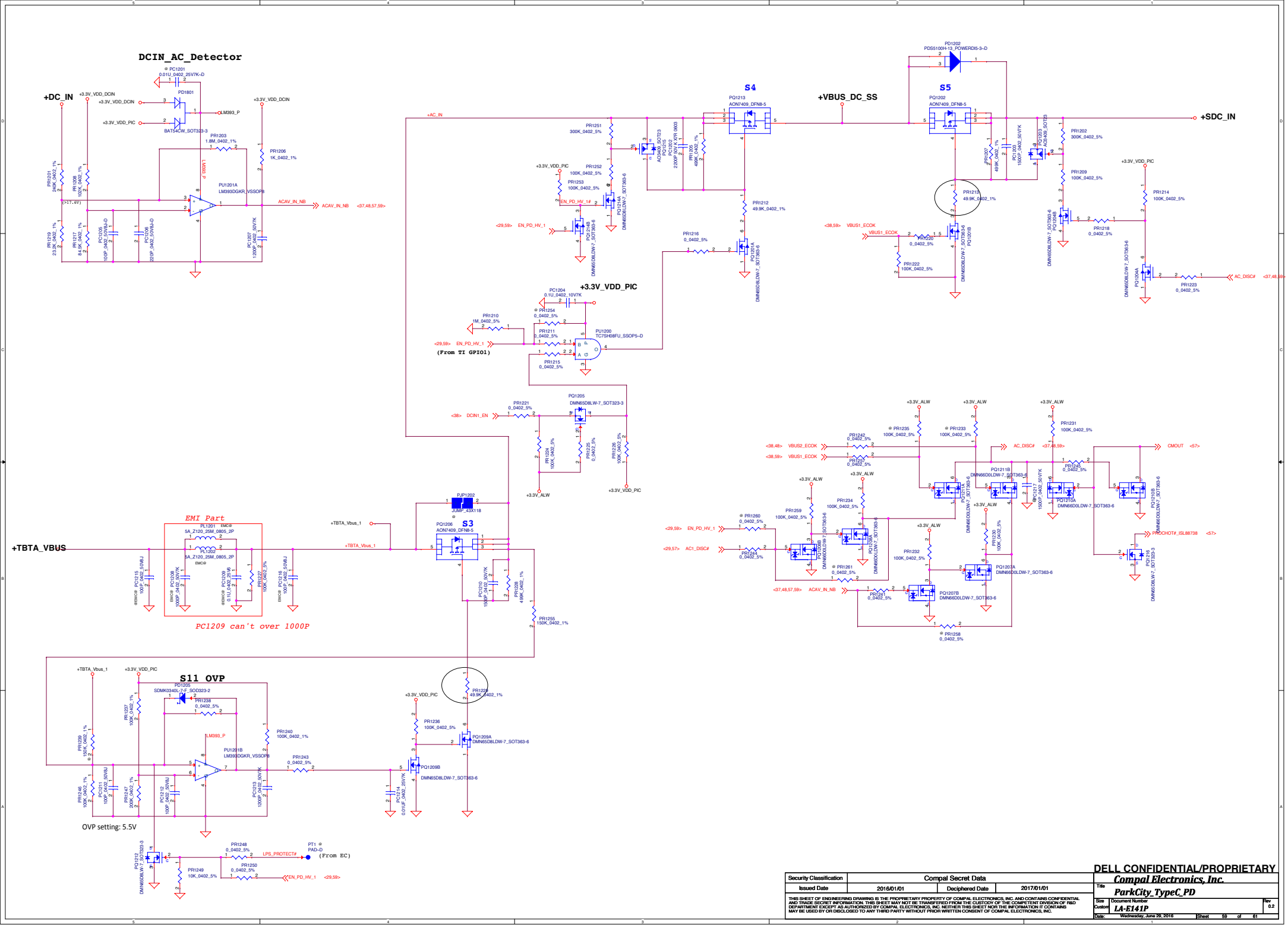

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Title	ParkCity_TypeC_PD		
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	65	PWR_VCORE_ ISL95855	2016 05/23	POWER	change solution version to fix PS4 funciton issue	change solution from ISL95855 to ISL95855A	DVT
2	70	PWR_1Type-C PD Selector	2016 06/14	POWER	Modify PD schematic	PR1219 change from 22.6K to 23.2K(SD034232280) PR1212, PR1213 change from 1M(SD034100480) to 634K(SD034634380)	DVT DVT
3	66	PWR_VCORE _VCORE	2016 06/14	POWER	location alignment	Change location PU602 to PU610, PL603 to PL610, PU603 to PU611, PL604 to PL611	DVT
4	67	PWR_VCORE _VGT,VSA	2016 06/14	POWER	location alignment	Change location PU606 to PU612, PL607 to PL612, PU605 to PU613, PL608 to PL613, PU607 to PU614, PQ601 to PQ614, PL609 to PL614	DVT
5	68	PWR_CHARGER	2016 06/14	POWER	Change footprint	PD903 change from SDMK0340L-7-F_SOD323-2-D (SCS0340L010) to RB520SM-30T2R_EMD2-2 (SCS00006C00)	DVT
6	61,72	PWR_+DCIN PWR_1Type-C PD Selector	2016 06/22	POWER	Modify DC IN schematic	PR12, PR11, PR1205, PR1207 and PR1228 change to 499K from 1M ohm PR16, PR18, PR1212, PR1213 and PR1229 change to 49.9K from 1M ohm PR1251 and PR1202 change to 300K from 100K ohm.	DVT
7			2016 06/22	POWER	Trail run 2nd source	PU1,PU903,PU1200 change the main source part to SA007080180(S IC SN74AHC1G08DCKR SC-70 5P AND) from SA007080120 (S IC TC7SH08FU SSOP 5P AND) BOM change no need link the new footprint.	DVT
8			2016 06/22	POWER	Trail run 2nd source	PQ1210,PQ1207,PQ1208,PQ1211,PQ1,PQ1201,PQ1204,PQ1209,PQ1214 change the main source part to SB00000ZU00 (S TR DMN65D8LDW-7 2N SOT363-6) from SB00000DH00 (S TR DMN66D0LDW-7 2N SOT363-6) BOM change no need link the new footprint.	DVT
9			2016 06/22	POWER	Trail run 2nd source	PQ5,PQ1215,PQ1203 change the main source part to SB934090000 (S TR AO3409 P-CHANNEL SOT-23) from SB00000IU10 (S TR SI2303CDS-T1-GE3 1P SOT23-3) BOM change no need link the new footprint.	DVT
10			2016 06/22	POWER	Trail run 2nd source	PL100 change the main source part to SH000016700 (S COIL 1.5UH +-20% 9A 7X7X3 MOLDING) from SH000008800 (S COIL 1.5UH +-20% 9A) PL201 change the main source part to SH00000YE00 (S COIL 1UH +-20% 11A 7X7X3 MOLDING) from SH00000PJ00 (S COIL 1UH +-20% 1R0MS 12A) PL1301, PL1302(DSC only) 2nd source trial run the SH00000UF00 (S COIL 0.22UH +-20% ETQP4LR22AGM 24A) PL1400(14H DSC only) change the main source part to SH00000Z200 (S COIL 1UH +-20% 6.6A 5X5X3 MOLDING) from SH00000PA00 (S COIL 1UH +-20% 1R0M-M7L 7A)	DVT
11	65	PWR_VCORE_ ISL95855	2016 06/22	POWER	CPU transient	PC601 change from 33nF to 47nF PC609 change from 680pFto 1000pF PC624 change from 330pFto 680pF PC634 change from 680pF to 2200pF PR640 change from 110k to 115k	DVT
12			2016 06/27	POWER	Add RF request part	Pop PC403、PC204、PC797、PC302、PC112 4.7R(1206) Pop PC403、PC204、PC797、PC302、PC112 680pF(0603) Pop PC100、PC405、PC407、PC115、PC116、PC301、PC303、PC103 100pF(0402)	DVT

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	11	HW	2016/5/27	COMPAL	S0ix(modern standy) support for VCCPLL_OC	Pop RZ120 and Depop UZ34 Add net name VCCSTG_EN(UZ19.4) and connect to RZ120.1	0.2(X01)
2	37	HW	2016/5/27	COMPAL	Reserve PORT80_DET# PD resistance	Reserve RE513 100k (SD028100380) to GND	0.2(X01)
3	35	HW	2016/6/1	COMPAL	Intel schematics reivew modify item	CZ28,CZ29 change from 0.047uF to 0.01uF CZ27 change from 0.1uF(@)_0201 to 10uF_0603	0.2(X01)
4	39	HW	2016/6/1	COMPAL	TPM change to NUVOTON	Change TPM from Atmel to NUVOTON.	0.2(X01)
5	35	HW	2016/6/1	COMPAL	Intel reviwe result (WWAN Coex feature support)	Add RZ128 0 ohm connect WWAN_COEX3 and WLAN_COEX3 Add RZ129 0 ohm connect WWAN_COEX2 and WLAN_COEX2 Add RZ130 0 ohm connect WWAN_COEX1 and WLAN_COEX1	0.2(X01)
6	35	HW	2016/6/7	COMPAL	Debug card reserve	Add RZ131, RZ132 for PORT80_DET# and HOST_DEBUG_TX	0.2(X01)
7	37	HW	2016/6/7	COMPAL	For MEC5105K-D1-TN setting	1. Change UE1 to SA00009GL00 2. POP RE360,RE362 3. De-POP RE361	0.2(X01)
8	35,32	HW	2016/6/16	COMPAL	For EMC request	De-pop RZ131, RZ132. CL22 change to 10pf , POP CA7,CZ1 (100P),CH268 modify from 22p to 47p and POP,Change LV1 to SM01000NY00	0.2(X01)
9	41	HW	2016/6/16	COMPAL	BITS284924-HDD is still working after press power button into S5 during POST.	POP RN5	0.2(X01)
10	39	ME	2016/6/17	COMPAL	Connector change	1. JKBTP1 change to CVILU_CF5020FD0RK-05-NH 2. JUSH1 change to CVILU_CF5026FD0RK-05-NH 3. JIR1 change to ACES_50208-0060N-P01	0.2(X01)
11	36	HW	2016/6/20	COMPAL	Vender suggest	RA7,RA8 change to 16.2ohm	0.2(X01)
12	37	HW	2016/6/22	COMPAL	The posibility of GPIO map update	Add RE514,RE515 for RTCRST_ON	0.2(X01)
13	41	HW	2016/6/22	COMPAL	BITS283552 - [BR_CSLP] FFS AP no function when execute FF generator or shake SU	FFS VDD_IO change to +3.3V_RUN	0.2(X01)

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