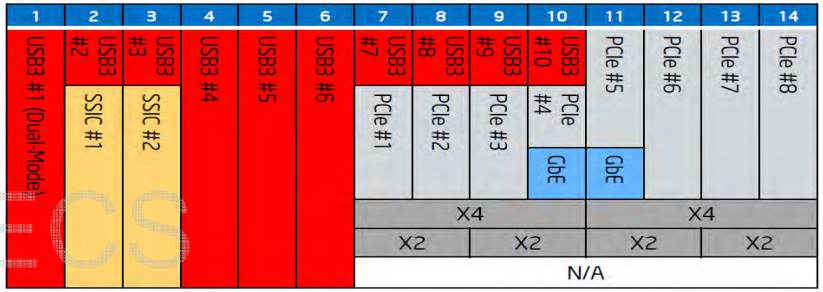
SKYLAKE-S V:1.0

ECS CONFIDENTIAL

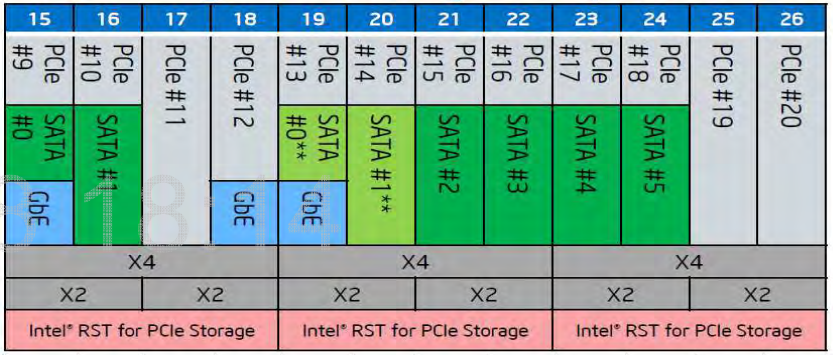
SCHEMATICS TABLE:

HSIO Lane Assignements by SKU (Lanes 1-14)



sku	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	N/A	N/A	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
B150	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
Q150	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3	USB3	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
H170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3	USB3	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
Z170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
Q170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe/ LAN	PCIe /LAN	PCIe	PCIe	PCIe

HSIO Lane Assignements by SKU (Lanes 15-26)

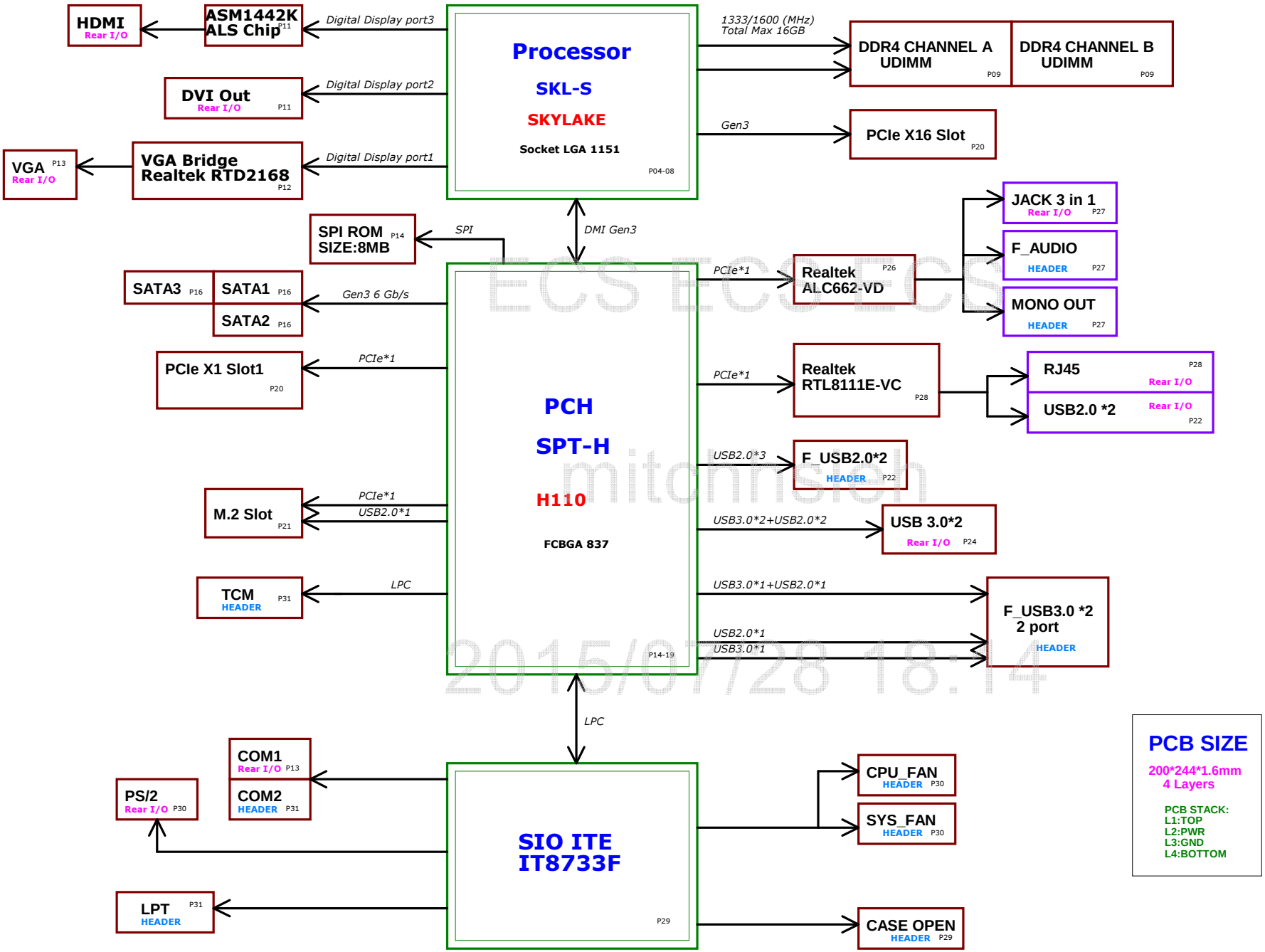


Sku	15	16	17	18	19	20	21	22	23	24	25	26	RST for PCIe Ports
H110	PCIe/ LAN	PCIe	N/A	LAN Only	SATA*/ LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A	0
B150	PCIe/LAN SATA*	PCIe/ SATA*	PCIe	PCIe/ LAN	SATA* /LAN	SATA*	SATA	SATA	SATA	SATA	N/A	N/A	0
Q150	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	SATA	SATA	SATA	SATA	N/A	N/A	0
H170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	SATA	SATA	PCIe	PCIe	2
Z170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	3
Q170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	3

Elitegroup Computer Systems

Title: Cover Page		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 1 of 46	

Skylake-S Desktop Platform



PCB SIZE

200*244*1.6mm
4 Layers

PCB STACK:
L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

Elitegroup Computer Systems			
Title: Block Diagram			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 2 of 46		

PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPP_F17	3VSB	LPC_PME_L	PME# GPI
GPD10	ATX_3VSB	GPD10 (GPD10_DIS_ME)	GPD10 OUTPUT Low/Normal, High/ME disable
GPP_B13	N/A	PCH_PLTRST_L	PLTRST#
GPP_G16	N/A	GPP_G16	GPO S0/S3/S4/S5:High
GPP_G15	VCC3	GPP_G15 (TMP Header Sel)	GPI
GPP_G13	VCC3	HDPANEL_DETECT	GPI
GPP_E7	VCC3	THERMAL_SD	GPI
GPP_B3	VCC3	BT_DIS_L_R	GPO S0/S3/S4/S5:High
GPP_H18	3VSB	GPP_H18	GPI
GPP_H17	3VSB	GPP_H17	GPI
GPP_H16	3VSB	GPP_H16	GPI
GPP_H15	3VSB	GPP_H15	For Acer Reserve
GPP_H14	3VSB	GPP_H14	For Acer Reserve
GPP_B14	+VCC3	PCH_SPKR	SPKR
GPP_A14	3VSB	LPCPD_L	SUS_STAT#
GPP_C6	3VSB	SML1_CLK	SML1CLK
GPP_C7	3VSB	SML1_DATA	SML1DATA
GPP_E8	VCC3	SATALED_L	SATALED#
GPP_E9	3VSB	GPP_E9 (BIOS WP)	GPI INPUT Low/Normal, High/BIOS WP
GPP_E10	3VSB	GPP_E10 (SW BIOS WP)	GPO OUTPUT Low/BIOS WP, High/Normal
GPP_E0	VCC3	GPP_E0 (OBR)	GPI
GPP_E4	VCC3	GPP_E4	GPO S0/S3/S4/S5:High
GPP_F22	VCC3	PCH_GPP_F22 (PCIEX16RST)	GPO S0:High S3/S4/S5:Low
GPP_F16	3VSB	GPP_F16 (USB_EN)	GPO S0/S3:High S4/S5:Low
GPP_F14	3VSB	H_SKTOCC_L	GPI
GPP_B17	VCC3	M.2_DIS_L_R	GPO S0/S3/S4/S5:High
GPP_B6	VCC3	CLK_REQ1_M.2_WLAN_L	GPO
GPP_B8	VCC3	GPP_B8	GPI
GPD0	DSW	RLAN_PWR_EN	GPO
GPP_D4	3VSB	SIO_GP16(PC_health)	GPI

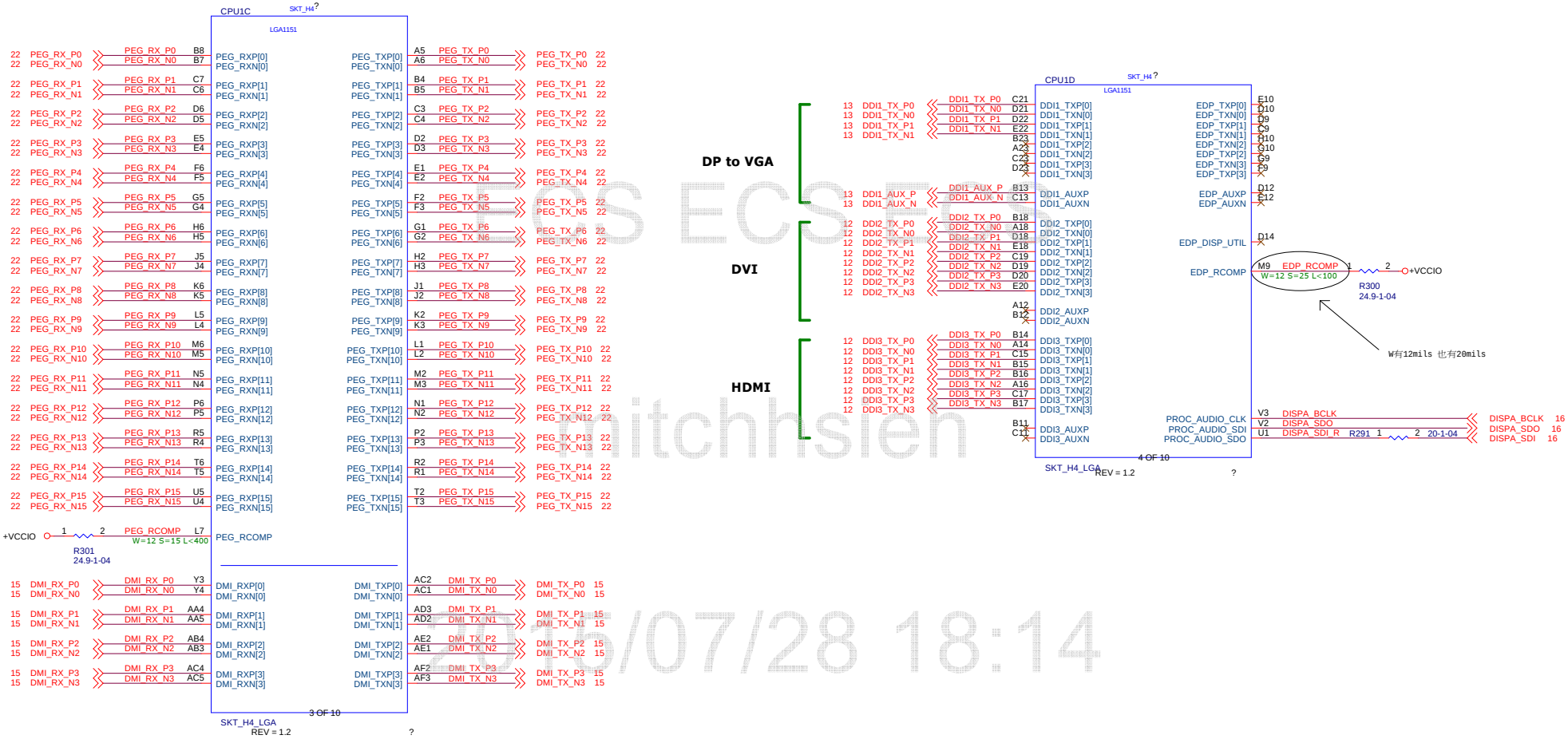
SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP37	+DIMM_5VDUAL	SIO_LED1	FAN_TAC3(DI)
GP36	3VSB	THERMAL_SD	FAN_CTL3(DOD8)
GP35	+DIMM_5VDUAL	SIO_LED0	FAN_TAC4(DI)
GP34	3VSB	SUSWARN_L	SUSWARN#(DOD8)
GP33	3VSB	SUSACK_L	SUSACK#(DOD8)
GP32	ATX3VSB	DPWROK	DPWROK(DOD8)
GP30	VCC	ATX_PWRGD	ATXPG(DI)
GP14	3VSB	SML1_CLK	VCORE_EN(DOD8)
N/A	3VSB	SML1_DATA	PCH_D1
GP13	VCC3	PCH_SYSPWROK	PWROK1(DOD8)
GP12	N/A	PCIRST1_L	PCIRST1#(DO8)
GP11	N/A	PCIRST2_L	PCIRST2#(DO8)
GP44	3VSB	SIO_PWRON_L	PWRON#(DOD8)
GP54	3VSB	LPC_PME_L	PME#(DOD8)
GP43	ATX5VSB	FP_PWRBTN_L	PANSWH#(DI)
GP42	ATX3VSB	ATX_PSON_L	PSON#(DOD8)
GP53	N/A	SLP_S4_L	SUSC#(DI)
GP40	3VSB	3VSBSW_L	3VSBSW#(DO8)
GP10	N/A	PCIRST3_L	PCIRST3#(DO8)
GP55	3VSB	RSMRST_L	RSMRST3#(DOD8)
GP16	3VSB	SIO_GP16(PC_health)	5VSB_CTRL3#(DOD8)

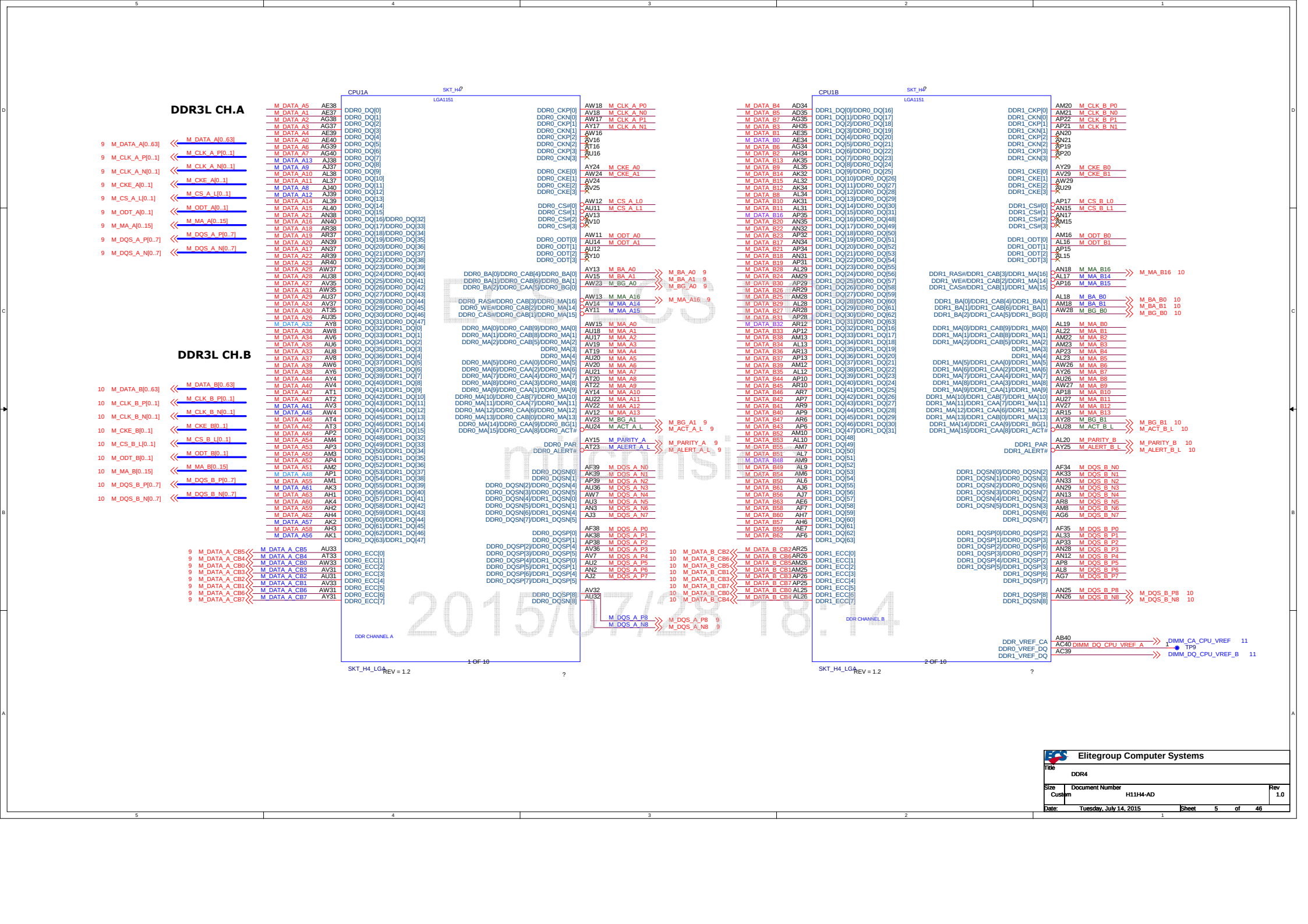
CPU-Strap

Pin Name	Usage	Default Status
CFG0	CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted	1 = (Default) Normal Operation
CFG1	CFG[1]: Reserved configuration lane	
CFG2:5:6	CFG[2]:1 = Normal operation CFG[6:5]:11 = 1 x16 PCI Express	PCIE16X
CFG3	CFG[3]: Reserved configuration lane.	
CFG4	CFG[4]: eDP enable:	1 = Disabled.
CFG7	CFG[7]: PEG Training:	1 = (default) PEG Train immediately following RESET# de assertion.
CFG19:8	CFG[19:8]:Reserved configuration lanes.	
SPKR/GPP_B14	Top Swap Override	0 =Disable “Top Swap” mode. (Default)
GSPI0_MOSI/GPP_B18	No Reboot	0 =Disable “No Reboot” mode
SMBALERT#/GPP_C2	TLS Confidentiality	1 =EnableIntel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS
GSPI1_MOSI/GPP_B22	Boot BIOS Strap Bit BBS	0=SPI
SML0ALERT#/GPP_C5	eSPI or LPC	0 =LPCIs selected for EC.
HDA_SDO	Flash Descriptor Security Override	This signal has a weak internal pull-down. 0 =Enable security measures defined in the Flash Descriptor. 1 =Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
DDPB_CTRLDATA/GPP_I6	Display Port B Detected	1 = Port B is detected.
DDPC_CTRLDATA/GPP_I8	Display Port C Detected	1 = Port C is detected.
DDPB_CTRLDATA/GPP_I10	Display Port D Detected	1 = Port D is detected.

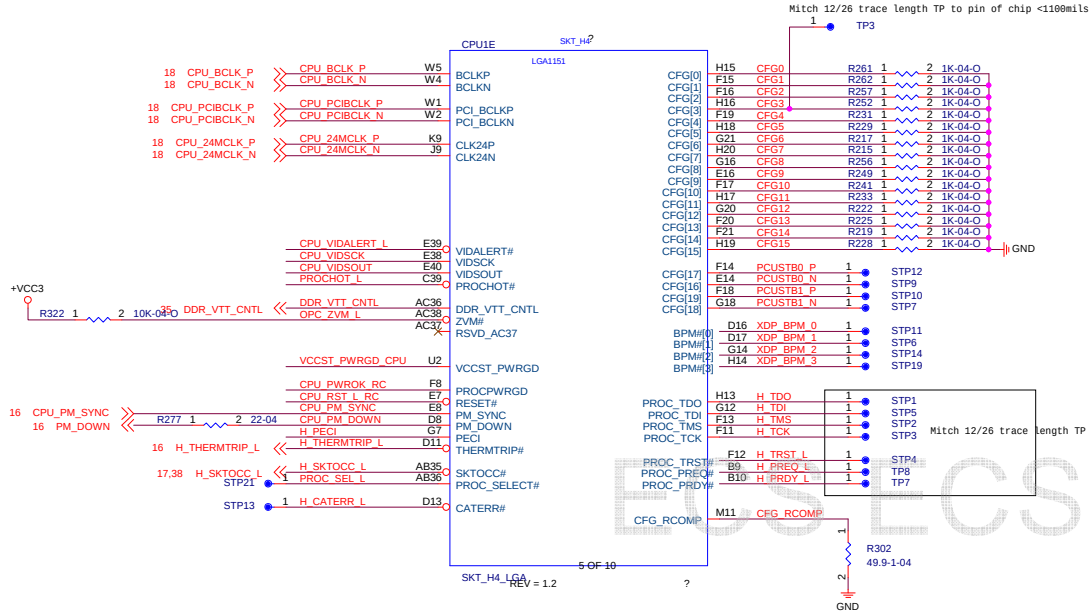
Elitegroup Computer Systems			
Title: GPIO Function & INT# Mapping			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 3 of 46		



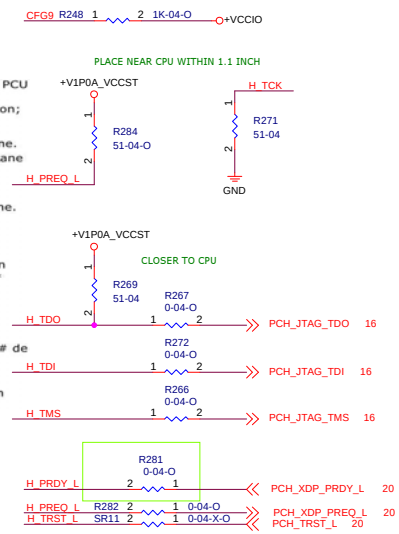
Elitegroup Computer Systems			
Title: CPU-PEG/DMI/DDI/EDP			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 4 of 46		



Elitegroup Computer Systems	
Title	DDR4
Size: Custom	Document Number: H11H4-AD
Rev	1.0
Date: Tuesday, July 14, 2015	Sheet 5 of 46

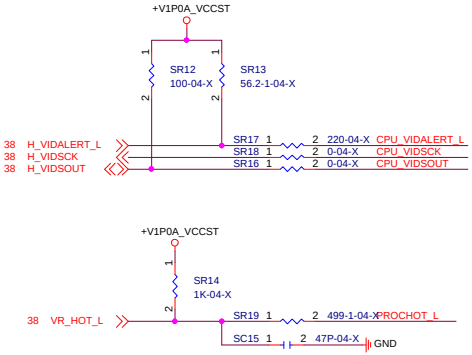


CFG[0:15] Configuration note

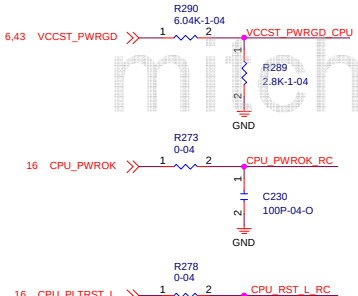


- **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- **CFG[1]**: Reserved configuration lane.
- **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]**: Reserved configuration lane.
- **CFG[4]**: eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]**: PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[7]**: PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]**: Reserved configuration lanes.

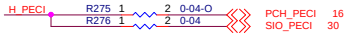
Asynchronous & Sideband Signal



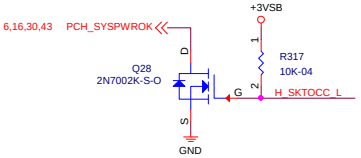
Processor Power Good

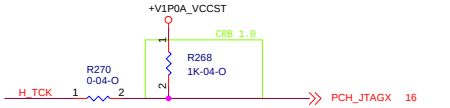


PECI



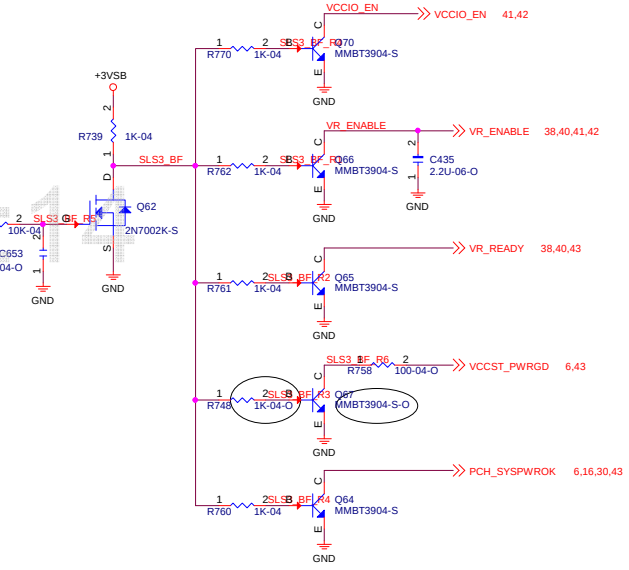
SKTOCC#



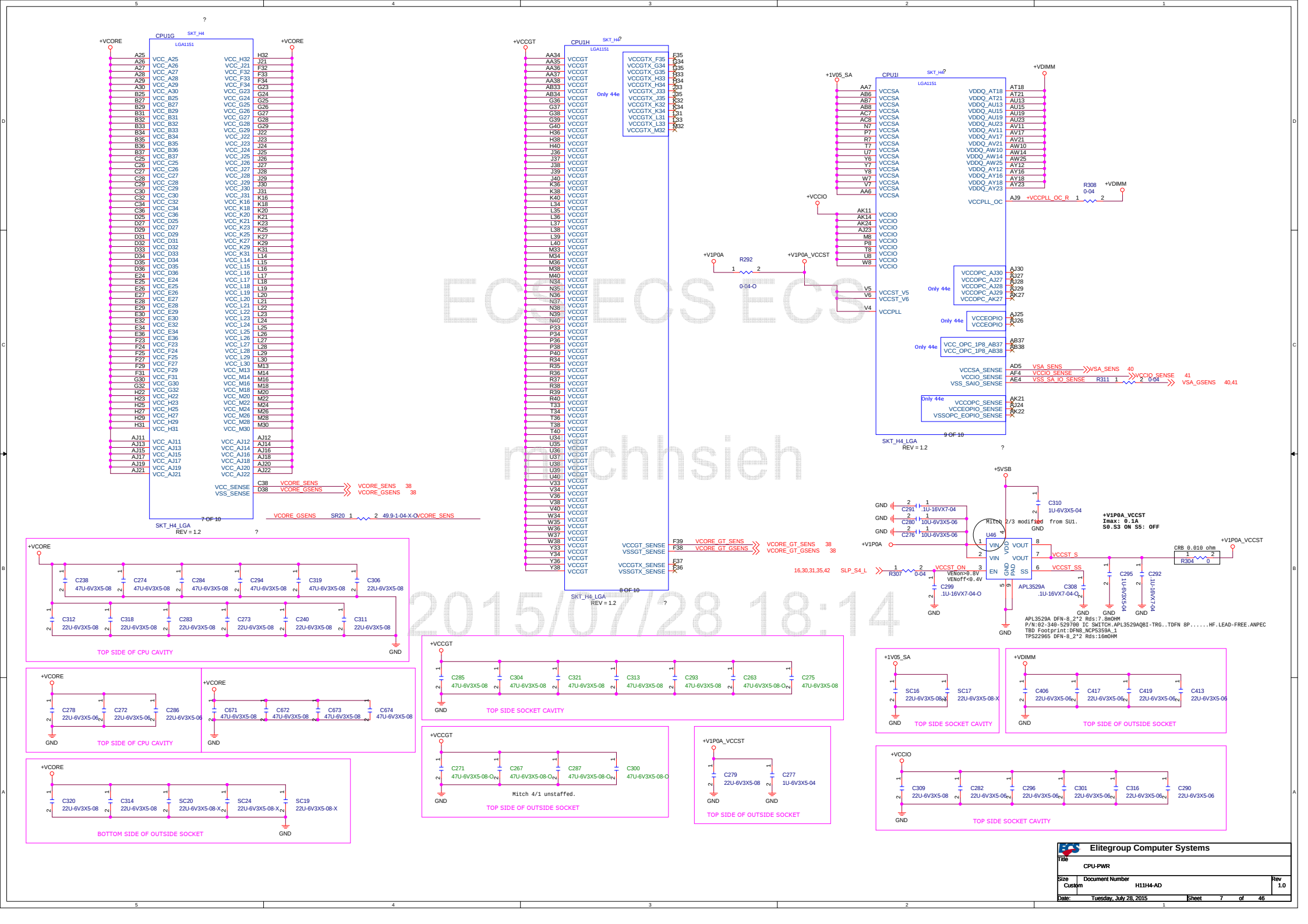


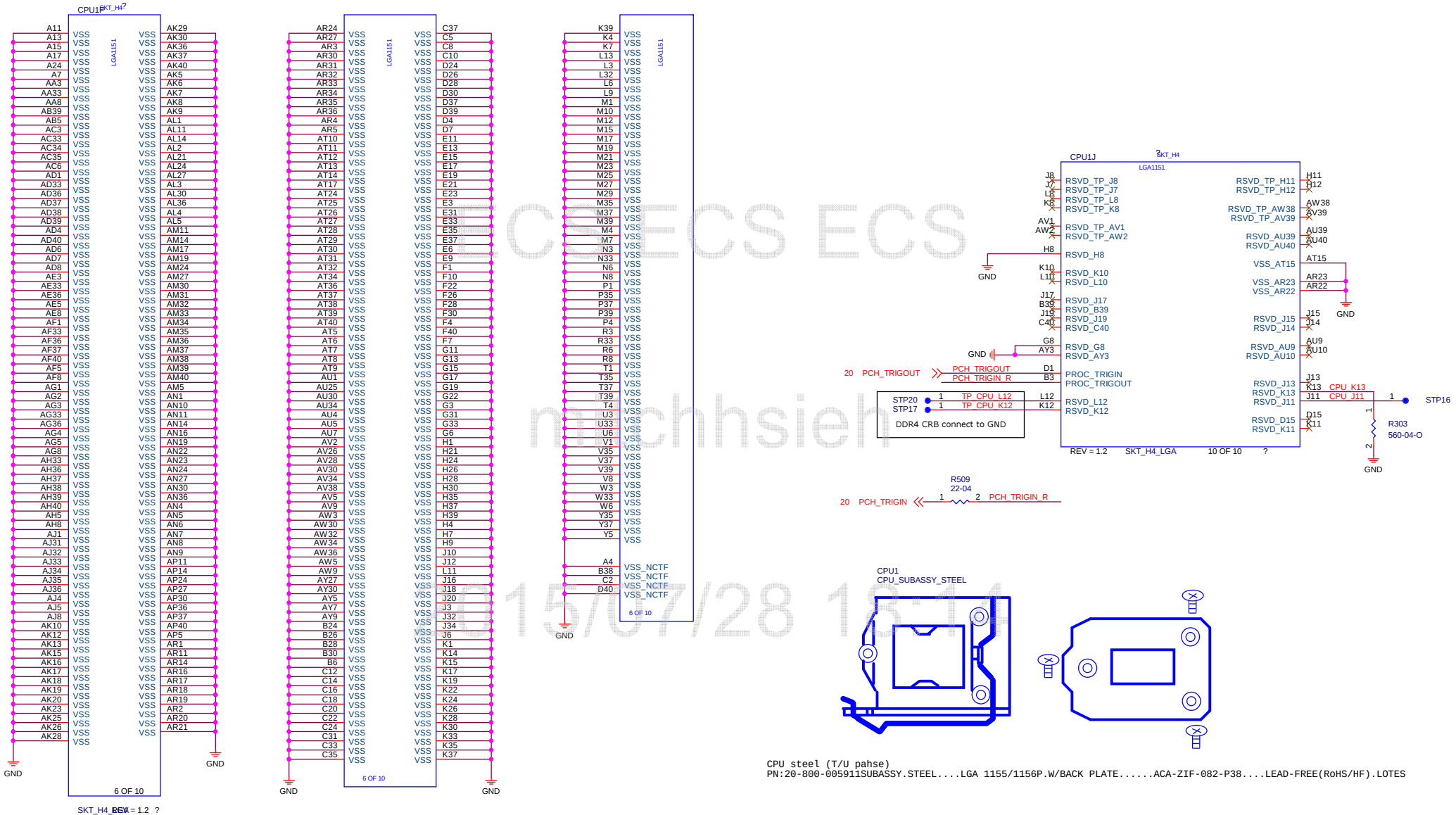
Sequencing Circuit

PLACE WITHIN 1.1 FROM CPU XDP

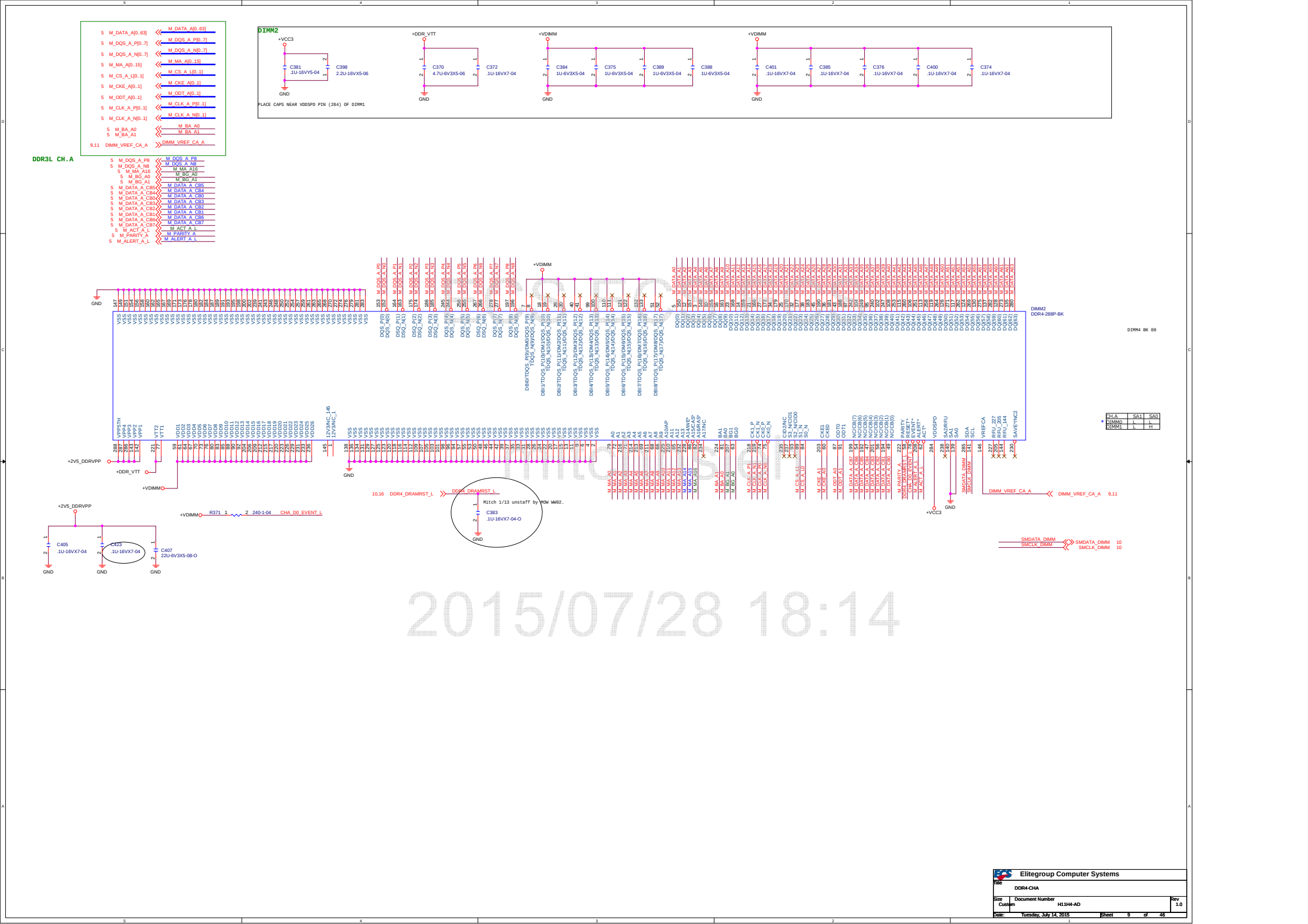


Elitegroup Computer Systems		
Title: CPU-MISC		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
Date: Tuesday, July 28, 2015	Sheet 6 of 46	


CPU1G
SKT_H4
LGA1151
+VCORE
VCC_A25
VCC_A26
VCC_A27
VCC_A28
VCC_A29
VCC_A30
VCC_B25
VCC_B27
VCC_B29
VCC_B31
VCC_B32
VCC_B33
VCC_B34
VCC_B35
VCC_B36
VCC_B37
VCC_C25
VCC_C26
VCC_C27
VCC_C28
VCC_C29
VCC_C30
VCC_C32
VCC_C34
VCC_C36
VCC_D25
VCC_D27
VCC_D29
VCC_D31
VCC_D32
VCC_D33
VCC_D34
VCC_D35
VCC_D36
VCC_E24
VCC_E25
VCC_E26
VCC_E27
VCC_E28
VCC_E29
VCC_E30
VCC_E32
VCC_E34
VCC_E36
VCC_F23
VCC_F24
VCC_F25
VCC_F27
VCC_F29
VCC_F31
VCC_G30
VCC_G32
VCC_H22
VCC_H23
VCC_H25
VCC_H27
VCC_H29
VCC_H31
VCC_AJ11
VCC_AJ13
VCC_AJ15
VCC_AJ17
VCC_AJ19
VCC_AJ21
VCC_H32
VCC_J21
VCC_F32
VCC_F33
VCC_F34
VCC_G23
VCC_G24
VCC_G25
VCC_G26
VCC_G27
VCC_G28
VCC_G29
VCC_J22
VCC_J23
VCC_J24
VCC_J25
VCC_J26
VCC_J27
VCC_J28
VCC_J29
VCC_J30
VCC_J31
VCC_K16
VCC_K18
VCC_K20
VCC_K21
VCC_K23
VCC_K25
VCC_K27
VCC_K29
VCC_K31
VCC_L14
VCC_L15
VCC_L16
VCC_L17
VCC_L18
VCC_L19
VCC_L20
VCC_L21
VCC_L22
VCC_L23
VCC_L24
VCC_L25
VCC_L26
VCC_L27
VCC_L28
VCC_L29
VCC_L30
VCC_M13
VCC_M14
VCC_M16
VCC_M18
VCC_M20
VCC_M22
VCC_M24
VCC_M26
VCC_M28
VCC_M30
VCC_AJ12
VCC_AJ14
VCC_AJ16
VCC_AJ18
VCC_AJ20
VCC_AJ22
VCC_SENSE
VSS_SENSE
C38 VCORE_SENS
D38 VCORE_GSENS
VCORE_SENS 38
VCORE_GSENS 38
VCORE_GSENS SR20 1 2 49.9-1-04-X-O VCORE_SENS
7 OF 10
SKT_H4_LGA
REV = 1.2
CPU1H
+VCCGT
VCCGT
VCCGTX_F35
VCCGTX_G34
VCCGTX_G35
VCCGTX_H33
VCCGTX_H34
VCCGTX_J33
VCCGTX_J35
VCCGTX_K32
VCCGTX_K34
VCCGTX_L31
VCCGTX_L33
VCCGTX_M32
Only 44e
VCCGT_SENSE
VSSGT_SENSE
VCCGTX_SENSE
VSSGTX_SENSE
F39 VCORE_GT_SENS
F38 VCORE_GT_GSENS
F37
F36
VCORE_GT_SENS 38
VCORE_GT_GSENS 38
8 OF 10
CPU1I
+1V05_SA
VCCSA
VDDQ_AT18
VDDQ_AT21
VDDQ_AU13
VDDQ_AU15
VDDQ_AU19
VDDQ_AU23
VDDQ_AV11
VDDQ_AV17
VDDQ_AV21
VDDQ_AW10
VDDQ_AW14
VDDQ_AW25
VDDQ_AY12
VDDQ_AY16
VDDQ_AY18
VDDQ_AY23
VCCPLL_OC
+VDIMM
R308 0-04
AJ9 +VCCPLL_OC_R
+VCCIO
VCCIO
VCCPC_AJ30
VCCPC_AJ27
VCCPC_AJ28
VCCPC_AJ29
VCCPC_AK27
VCCEOPIO
VCC_OPC_1P8_AB37
VCC_OPC_1P8_AB38
VCCSA_SENSE
VCCIO_SENSE
VSS_SAIO_SENSE
VCCOPC_SENSE
VCCEOPIO_SENSE
VSSOPC_EOPIO_SENSE
VSA_SENS
VCCIO_SENSE
VSS_SA_IO_SENSE
R311 0-04
VSA_GSENS 40,41
VCCST_V5
VCCST_V6
VCCPLL
+V1P0A
+V1P0A_VCCST
R292 0-04-O
Only 44e
9 OF 10
SKT_H4_LGA
REV = 1.2
+5VSB
+V1P0A_VCCST
U46
APL3529A
VIN
VOUT
EN
SS
GND PAD
VCCST_ON
VENon>0.8V
VENoff<0.4V
VCCST_S
VCCST_SS
R307 0-04
16,30,31,35,42 SLP_S4_L
C310 1U-6V3X5-04
C291 .1U-16VX7-04
C280 10U-6V3X5-06
C276 10U-6V3X5-06
C299 .1U-16VX7-04-O
C295 1U-6V3X5-04
C292 .1U-16VX7-04
C308 .1U-16VX7-04-O
CRB 0.010 ohm
R304 0
+V1P0A_VCCST
+V1P0A_VCCST
Imax: 0.1A
S0.S3 ON S5: OFF
Mitch 2/3 modified from SU1.
APL3529A DFN-8_2*2 Rds:7.8mOHM
P/N:02-340-529700 IC SWITCH.APL3529AQBI-TRG..TDFN 8P.....HF.LEAD-FREE.ANPEC
TBD Footprint:DFN8_NCP5359A_1
TPS22965 DFN-8_2*2 Rds:16mOHM
TOP SIDE OF CPU CAVITY
C238 47U-6V3X5-08
C274 47U-6V3X5-08
C284 47U-6V3X5-08
C294 47U-6V3X5-08
C319 47U-6V3X5-08
C306 22U-6V3X5-08
C312 22U-6V3X5-08
C318 22U-6V3X5-08
C283 22U-6V3X5-08
C273 22U-6V3X5-08
C240 22U-6V3X5-08
C311 22U-6V3X5-08
TOP SIDE OF CPU CAVITY
C278 22U-6V3X5-06
C272 22U-6V3X5-06
C286 22U-6V3X5-06
C671 47U-6V3X5-08
C672 47U-6V3X5-08
C673 47U-6V3X5-08
C674 47U-6V3X5-08
TOP SIDE SOCKET CAVITY
C285 47U-6V3X5-08
C304 47U-6V3X5-08
C321 47U-6V3X5-08
C313 47U-6V3X5-08
C293 47U-6V3X5-08
C263 47U-6V3X5-08-O
C275 47U-6V3X5-08
TOP SIDE SOCKET CAVITY
SC16 22U-6V3X5-08-X
SC17 22U-6V3X5-08-X
TOP SIDE OF OUTSIDE SOCKET
C406 22U-6V3X5-06
C417 22U-6V3X5-06
C419 22U-6V3X5-06
C413 22U-6V3X5-06
BOTTOM SIDE OF OUTSIDE SOCKET
C320 22U-6V3X5-08
C314 22U-6V3X5-08
SC20 22U-6V3X5-08-X
SC24 22U-6V3X5-08-X
SC19 22U-6V3X5-08-X
TOP SIDE OF OUTSIDE SOCKET
C271 47U-6V3X5-08-O
C267 47U-6V3X5-08-O
C287 47U-6V3X5-08-O
C300 47U-6V3X5-08-O
Mitch 4/1 unstaffed.
TOP SIDE OF OUTSIDE SOCKET
C279 22U-6V3X5-08
C277 1U-6V3X5-04
TOP SIDE OF OUTSIDE SOCKET
C309 22U-6V3X5-08
C282 22U-6V3X5-06
C296 22U-6V3X5-06
C301 22U-6V3X5-06
C316 22U-6V3X5-06
C290 22U-6V3X5-06
TOP SIDE SOCKET CAVITY
Elitegroup Computer Systems
Title
CPU-PWR
Size
Custom
Document Number
H11H4-AD
Rev
1.0
Date: Tuesday, July 28, 2015
Sheet 7 of 46

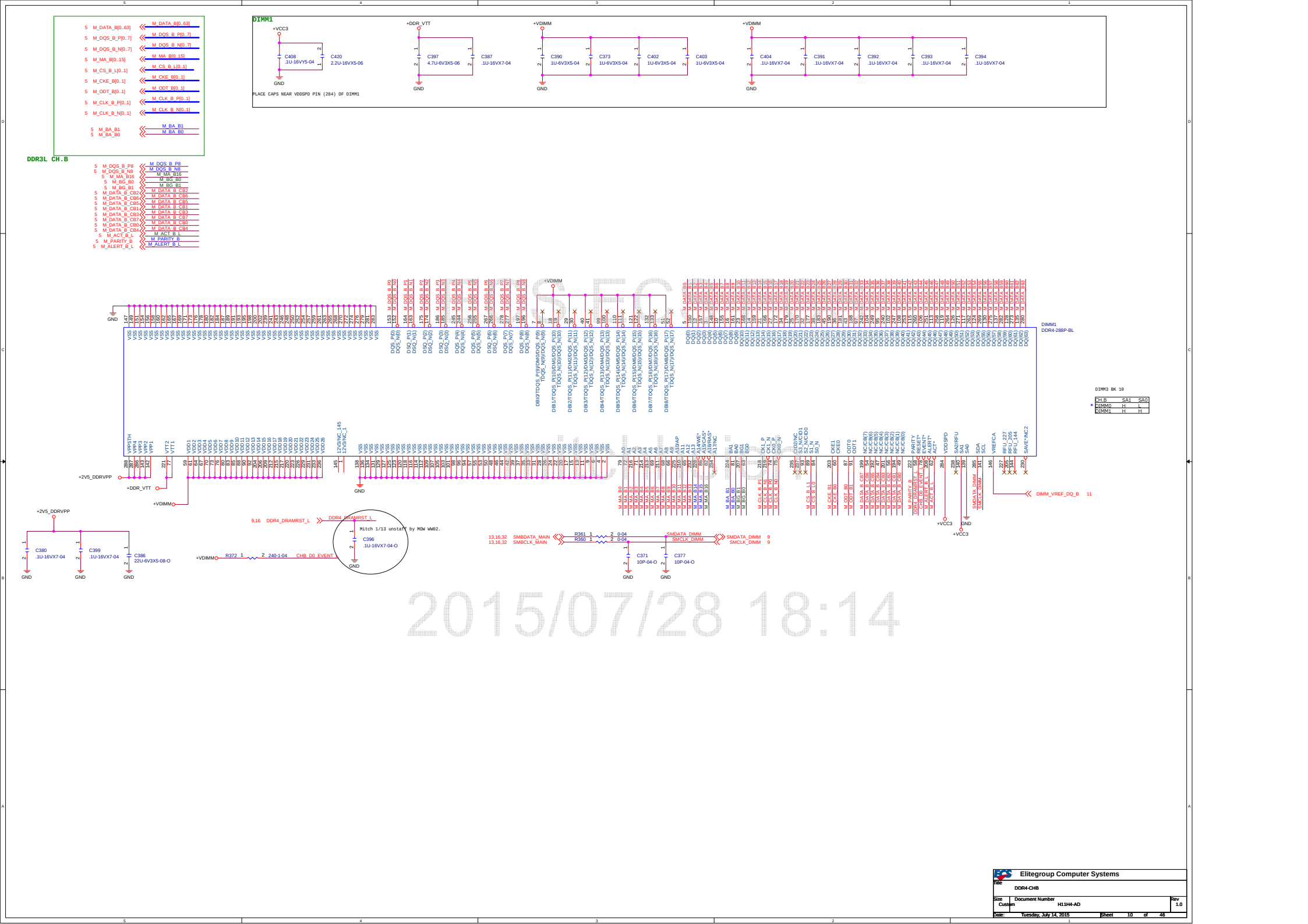


Elitegroup Computer Systems			
Title: CPU-GND			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 8 of 46		

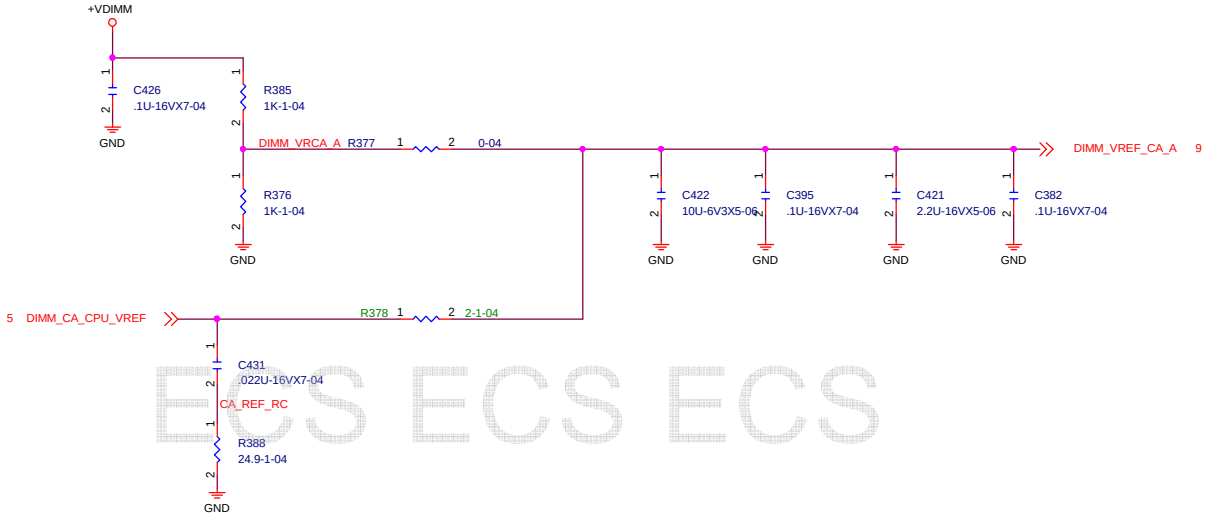


Title	DDR4-CHA		
Size	Document Number		Rev
Custom	H11H4-AD		1.0
Date:	Tuesday, July 14, 2015	Sheet 9 of 46	

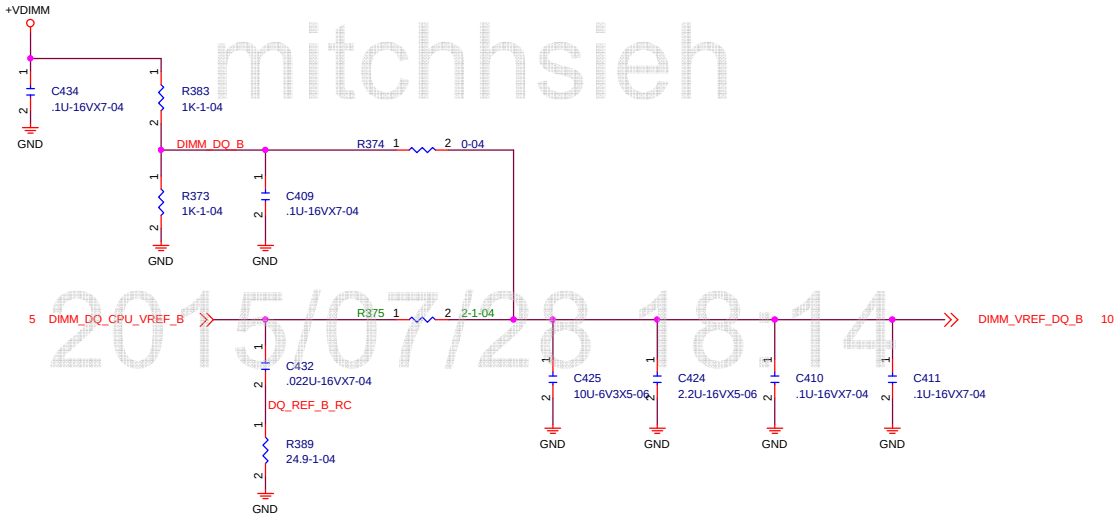
Elitegroup Computer Systems


DDR3L CH.B
DIMM1
PLACE CAPS NEAR VDDSPD PIN (284) OF DIMM1
DIMM1
DDR4-288P-BL
DIMM3 BK 10
CH_B SA1 SA0
DIMM0 H L
DIMM1 H H
+VCC3
+VDIMM
+DDR_VTT
+2V5_DDRVPP
GND
C408 .1U-16VY5-04
C420 2.2U-16VX5-06
C397 4.7U-6V3X5-06
C387 .1U-16VX7-04
C390 1U-6V3X5-04
C373 1U-6V3X5-04
C402 1U-6V3X5-04
C403 1U-6V3X5-04
C404 .1U-16VX7-04
C391 .1U-16VX7-04
C392 .1U-16VX7-04
C393 .1U-16VX7-04
C394 .1U-16VX7-04
C380 .1U-16VX7-04
C399 .1U-16VX7-04
C386 22U-6V3X5-08-O
C396 .1U-16VX7-04-O
C371 10P-04-O
C377 10P-04-O
R372 240-1-04
R361 0-04
R360 0-04
DDR4_DRAMRST_L
CHB_D0_EVENT_L
SMDATA_DIMM
SMCLK_DIMM
DIMM_VREF_DQ_B
Mitch 1/13 unstuff by MOW WW02.
2015/07/28 18:14
Elitegroup Computer Systems
DDR4-CHB
H11H4-AD
Tuesday, July 14, 2015
Sheet 10 of 46

DIMM_VREF_CA



DIMM_VREF_DQ



Elitegroup Computer Systems		
Title: DDR3L-CHB		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 11 of 46	

Port 2			
	DDI2_TXP[0]	DDI2_LANE0_DP	HDMIx_TX2_DP
	DDI2_TXN[0]	DDI2_LANE0_DN	HDMIx_TX2_DN
	DDI2_TXP[1]	DDI2_LANE1_DP	HDMIx_TX1_DP
	DDI2_TXN[1]	DDI2_LANE1_DN	HDMIx_TX1_DN
	DDI2_TXP[2]	DDI2_LANE2_DP	HDMIx_TX0_DP
	DDI2_TXN[2]	DDI2_LANE2_DN	HDMIx_TX0_DN
	DDI2_TXP[3]	DDI2_LANE3_DP	HDMIx_CLK_DP
	DDI2_TXN[3]	DDI2_LANE3_DN	HDMIx_CLK_DN

HDMI

HDMI的DDI_TX得號,TX0和TX2必須交換1次

4 DDI3_TX_N3 — C84 1 2 .1U-16VX7-04-O — HDMI_CLK_N3
4 DDI3_TX_P3 — C83 1 2 .1U-16VX7-04-O — HDMI_CLK_P3
4 DDI3_TX_N2 — C82 1 2 .1U-16VX7-04-O — HDMI_TX_N0
4 DDI3_TX_P2 — C81 1 2 .1U-16VX7-04-O — HDMI_TX_P0
4 DDI3_TX_N1 — C80 1 2 .1U-16VX7-04-O — HDMI_TX_N1
4 DDI3_TX_P1 — C79 1 2 .1U-16VX7-04-O — HDMI_TX_P1
4 DDI3_TX_N0 — C78 1 2 .1U-16VX7-04-O — HDMI_TX_N2
4 DDI3_TX_P0 — C77 1 2 .1U-16VX7-04-O — HDMI_TX_P2

+DVI_VGA_VCC — PFB2 FB-600-S08P-O FB:2A — +5V_HDMI
C27 1000P-50VX7-04-O — GND
C31 1U-6V3Y5-04-O — GND

HDMI_TX_P2_R 1 / HDMI_TX_N2_R 3 / HDMI_TX_P1_R 4 / HDMI_TX_N1_R 6 / HDMI_TX_P0_R 7 / HDMI_TX_N0_R 9 / HDMI_CLK_P3_R 10 / HDMI_CLK_N3_R 12 / HDMI_SCL 15 / HDMI_SDA 16 / +5V_HDMI 18 / HDMI_HPD_CNN 19 / GND 20 21 22 23 — HDMI TYPE A — HDMI-19P-O

HDMI Connector Pin13:CEC
沒有使用必需空接(Floating)
避免HDCP 測試 FAIL

SDA, SCL對地電容，Default 先不要上件， 如 EMI 需求須上件， 請務必確認可以 Pass HDMI 的 Spec

CHOKE1 CMK-90-08-HDMI-O: HDMI_TX_P2 ↔ HDMI_TX_P2_R, HDMI_TX_N2 ↔ HDMI_TX_N2_R
CHOKE2 CMK-90-08-HDMI-O: HDMI_TX_P1 ↔ HDMI_TX_P1_R, HDMI_TX_N1 ↔ HDMI_TX_N1_R
CHOKE3 CMK-90-08-HDMI-O: HDMI_TX_P0 ↔ HDMI_TX_P0_R, HDMI_TX_N0 ↔ HDMI_TX_N0_R
CHOKE4 CMK-90-08-HDMI-O: HDMI_CLK_P3 ↔ HDMI_CLK_P3_R, HDMI_CLK_N3 ↔ HDMI_CLK_N3_R

RN1 0-8P4R-O: HDMI_TX_P2 ↔ HDMI_TX_P2_R, HDMI_TX_N2 ↔ HDMI_TX_N2_R, HDMI_TX_P1 ↔ HDMI_TX_P1_R, HDMI_TX_N1 ↔ HDMI_TX_N1_R
RN2 0-8P4R-O: HDMI_TX_P0 ↔ HDMI_TX_P0_R, HDMI_TX_N0 ↔ HDMI_TX_N0_R, HDMI_CLK_P3 ↔ HDMI_CLK_P3_R, HDMI_CLK_N3 ↔ HDMI_CLK_N3_R
Co-lay

+5V_HDMI — SQ2 BAT54A-S-X-O
+VCC3 — R129 2.2K-04-O — HDMISDA_VCC — HDMI_CTRLDATA — Q13 2N7002K-S-O — HDMI_SDA — R96 2.2K-04-O — HDMISCL_VCC — C97 470P-50VX7-04-O — GND
+VCC3 — R135 2.2K-04-O — HDMI_CTRLCLK — Q14 2N7002K-S-O — HDMI_SCL — R51 2.2K-04-O — HDMISCL_VCC — C50 470P-50VX7-04-O — GND

U1 AZ1045-04F-S-O: HDMI_TX_P2_R ↔ HDMI_TX_P2, HDMI_TX_N2_R ↔ HDMI_TX_N2, HDMI_TX_P1_R ↔ HDMI_TX_P1, HDMI_TX_N1_R ↔ HDMI_TX_N1
U3 AZ1045-04F-S-O: HDMI_TX_P0_R ↔ HDMI_TX_P0, HDMI_TX_N0_R ↔ HDMI_TX_N0, HDMI_CLK_P3_R ↔ HDMI_CLK_P3, HDMI_CLK_N3_R ↔ HDMI_CLK_N3

17 HDMI_CTRLCLK ↔ HDMI_CTRLCLK
17 HDMI_CTRLDATA ↔ HDMI_CTRLDATA
17 HDMI_HPD ↔ HDMI_HPD

HDMI_TX_P2 R70 1 2 470-04-O_DPG
HDMI_TX_N2 R63 1 2 470-04-O
HDMI_TX_P1 R64 1 2 470-04-O
HDMI_TX_N1 R65 1 2 470-04-O
HDMI_TX_P0 R66 1 2 470-04-O
HDMI_TX_N0 R67 1 2 470-04-O
HDMI_CLK_P3 R68 1 2 470-04-O
HDMI_CLK_N3 R69 1 2 470-04-O
→ SQ1 2N7002K-S-X-O, +VCC3

+VCC3 — R136 1M-04-O — HDMI_HPD — Q15 2N7002K-S-O — HDMI_HPD_CNN — R83 20K-04-O, C72 1000P-50VX7-04-O — GND

+5V_HDMI — U10 AZC099-04S-R7G-S-O: HDMI_HPD_CNN ↔ HDMI_HPD_CNN, HDMI_SDA ↔ HDMI_SDA, HDMI_SCL ↔ HDMI_SCL — C56 .1U-16VY5-04-O — GND

DVI

HDMI的DDI_TX得號,TX0和TX2必須交換1次

4 DDI2_TX_P0 — C108 1 2 .1U-16VX7-04 — DVI_TX_P2
4 DDI2_TX_N0 — C109 1 2 .1U-16VX7-04 — DVI_TX_N2
4 DDI2_TX_P1 — C110 1 2 .1U-16VX7-04 — DVI_TX_P1
4 DDI2_TX_N1 — C111 1 2 .1U-16VX7-04 — DVI_TX_N1
4 DDI2_TX_P2 — C112 1 2 .1U-16VX7-04 — DVI_TX_P0
4 DDI2_TX_N2 — C113 1 2 .1U-16VX7-04 — DVI_TX_N0
4 DDI2_TX_P3 — C114 1 2 .1U-16VX7-04 — DVI_CLK_P3
4 DDI2_TX_N3 — C115 1 2 .1U-16VX7-04 — DVI_CLK_N3

17 DVI_CTRLCLK ↔ DVI_CTRLCLK
17 DVI_CTRLDATA ↔ DVI_CTRLDATA
17 DVI_HPD ↔ DVI_HPD

1. 16-400-900143 COMMON CHOKE.90 OHM.-SMD 0805..HDMI2012F25F-900T04.400mA...LEAD-FREE(RoHS).TAI-TECH
2. 16-400-900171 COMMON CHOKE.90 OHM.25%.SMD 0805..QTCW2012H-090-LF.300mA....LEAD-FREE(RoHS/HF).MAGIC

CHOKE11 CMK-90-08-HDMI: DVI_TX_P2 ↔ DVI_TX_P2_R, DVI_TX_N2 ↔ DVI_TX_N2_R
CHOKE12 CMK-90-08-HDMI: DVI_TX_P1 ↔ DVI_TX_P1_R, DVI_TX_N1 ↔ DVI_TX_N1_R
CHOKE13 CMK-90-08-HDMI: DVI_TX_P0 ↔ DVI_TX_P0_R, DVI_TX_N0 ↔ DVI_TX_N0_R
CHOKE14 CMK-90-08-HDMI: DVI_CLK_P3 ↔ DVI_CLK_P3_R, DVI_CLK_N3 ↔ DVI_CLK_N3_R
Mitch 4/15 VB staffed.

U7 AZ1045-04F-S-O: DVI_TX_P2_R ↔ DVI_TX_P2, DVI_TX_N2_R ↔ DVI_TX_N2, DVI_TX_P1_R ↔ DVI_TX_P1, DVI_TX_N1_R ↔ DVI_TX_N1
U8 AZ1045-04F-S-O: DVI_TX_P0_R ↔ DVI_TX_P0, DVI_TX_N0_R ↔ DVI_TX_N0, DVI_CLK_P3_R ↔ DVI_CLK_P3, DVI_CLK_N3_R ↔ DVI_CLK_N3

+DVI_VGA_VCC — PFB1 FB-600-S08P — +DVI_VCC
C17 1000P-50VX7-04 — GND
C33 1U-6V3Y5-04-O — GND

DVI-D — DVI-24P-SH-HIT
DVI_TX_N0_R 17 / DVI_TX_N1_R 18 / DVI_TX_P0_R 19 / DVI_TX_P1_R 21 / +DVI_VCC 22 / DVI_CLK_N3_R 23 / DVI_HPD_CNN 24 / DVI_TX_N2_R 1 / DVI_TX_P2_R 2 / DVI_SCL 4 / DVI_SDA 5 / VSYNC 6 / RED 7 / GREEN 8 / BLUE 13 / HSYNC 14 / GND 25 26

U2 AZC099-04S-R7G-S-O: DVI_HPD_CNN ↔ DVI_HPD_CNN, DVI_SDA ↔ DVI_SDA, DVI_SCL ↔ DVI_SCL
+DVI_VCC — C1 .1U-16VY5-04 — GND

DVI_TX_P2 R100 1 2 470-04_DPG
DVI_TX_N2 R101 1 2 470-04
DVI_TX_P1 R102 1 2 470-04
DVI_TX_N1 R103 1 2 470-04
DVI_TX_P0 R104 1 2 470-04
DVI_TX_N0 R105 1 2 470-04
DVI_CLK_P3 R106 1 2 470-04
DVI_CLK_N3 R107 1 2 470-04
→ Q16 2N7002K-S, +VCC3

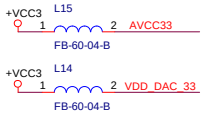
RN7 0-8P4R-O: DVI_TX_P2 ↔ DVI_TX_P2_R, DVI_TX_N2 ↔ DVI_TX_N2_R, DVI_TX_P1 ↔ DVI_TX_P1_R, DVI_TX_N1 ↔ DVI_TX_N1_R
Mitch 4/15 VB unstaffed.
RN8 0-8P4R-O: DVI_TX_P0 ↔ DVI_TX_P0_R, DVI_TX_N0 ↔ DVI_TX_N0_R, DVI_CLK_P3 ↔ DVI_CLK_P3_R, DVI_CLK_N3 ↔ DVI_CLK_N3_R
Mitch 4/15 VB unstaffed.

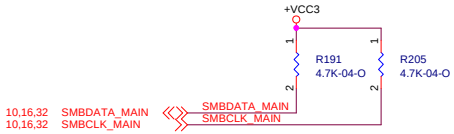
+DVI_VCC — SQ3 BAT54A-S-X
+VCC3 — R119 2.2K-04 — DVISDA_VCC — DVI_CTRLDATA — Q11 2N7002K-S — DVI_SDA — R29 2.2K-04 — DVISCL_VCC — C8 470P-50VX7-04-O — GND
+VCC3 — R73 2.2K-04 — DVISCL_VCC — DVI_CTRLCLK — Q7 2N7002K-S — DVI_SCL — R30 2.2K-04 — C9 470P-50VX7-04-O — GND

+VCC3 — R118 1M-04 — DVI_HPD — Q10 2N7002K-S — DVI_HPD_CNN — R23 20K-04, C5 1000P-50VX7-04-O — GND

Elitegroup Computer Systems			
Title: DP/HDMI			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 12 of 46		

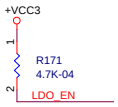
Power



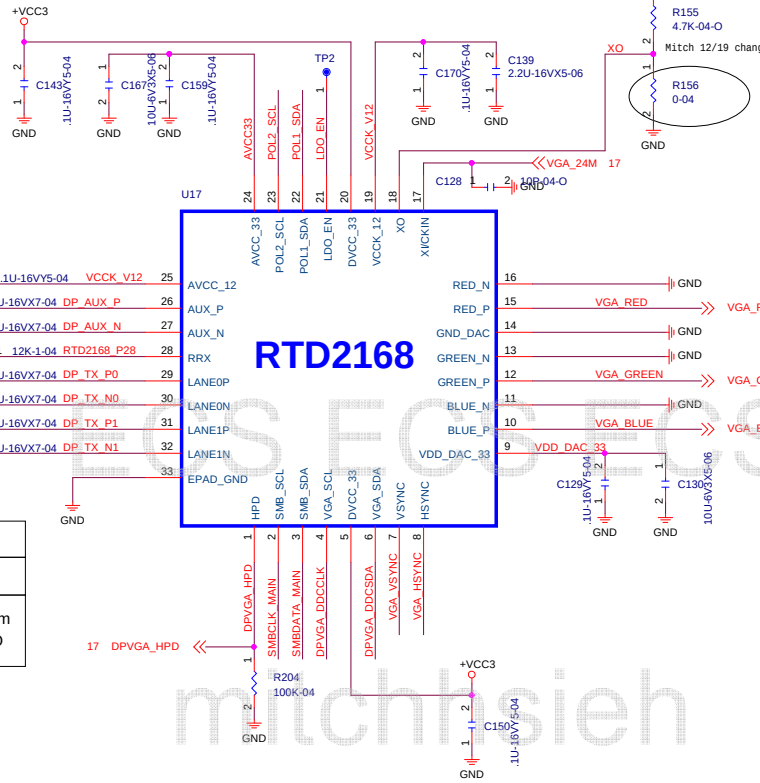


IIC Protocol is used

RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69



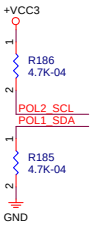
LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

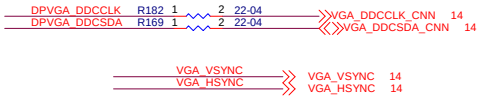


Note: When connected to non-EDID monitor,
XO Pin Pull Down : Disable RTD2168 embedded EDID, CPU handle.
XO Pin Pull High : Enable RTD2168 embedded EDID.

Mode Configure Table(Power On Latch)

to set PIN22 pull low, PIN23 pull high for Rom mode.





Elitegroup Computer Systems			
Title: DP to VGA(RTD2168)			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 13 of 46		

VGA

Part:BLM18BB220SN
P/N:16-105-220130 FB.22 OHM.25%...SMD 0402.BLM15BB220SN1D.300mA...HF.LEAD-FREE.MURATA
P/N:16-105-220140 FB.22 OHM.25%...SMD 0402.FCM1005MF-220T03.300mA...HF.LEAD-FREE.TAI-TECH

13 VGA_RED
13 VGA_GREEN
13 VGA_BLUE
FB1 FB2 FB3 FB-22-04-B
R159 R158 R157 75-1-04
C101 C100 C99 C70 C69 C68 2P-04
C76 C75 C74 10P-04-O
VGA_RED_CONN
VGA_GREEN_CONN
VGA_BLUE_CONN
GND

Level shifter,default 0 ohm

+VGA_VCC
SC6 SC7 1U-16VX7-04-X-O
SU4 SU3 74LVC32-5-S-X-O
13 VGA_HSYNC
13 VGA_VSYNC
VGA_HSYNC
VGA_VSYNC
VGA_HSYNC_5V
VGA_VSYNC_5V
SR6 SR5 0-04-X
SC4 SC3 10P-04-X
SR3 SR2 36-1-04-X
VGA_HSYNC_CNN
VGA_VSYNC_CNN

If build in Internal DVI Con,
that can use the circuit to protect reverse voltage together.

+12V
C148 .1U-25VX5-04-O
R175 10K-04
+VCC
+DVI_VGA_VCC_G
Q20 P8503BMG-S
耐壓:8V
F4 FUSE-1.1A-18
+DVI_VGA_VCC
R194 0-08-O

U9 AZC099-04S-R7G-S-O
C29 .1U-16VY5-04-O

SR1 SR4 2.2K-04-X
13 VGA_DDCCLK_CNN
13 VGA_DDCSDA_CNN
VGA_DDCCLK_CNN
VGA_DDCSDA_CNN
SC2 SC5 100P-04-X-O

SU2 AZC099-04S-R7G-S-X-O
VGA_HSYNC_CNN
VGA_VSYNC_CNN
SC1 .1U-16VY5-04-X-O

VGA
CONN-15P3R-VGA
VGA_RED_CONN
VGA_GREEN_CONN
VGA_BLUE_CONN
VGA_DDCSDA_CNN
VGA_HSYNC_CNN
VGA_VSYNC_CNN
VGA_DDCCLK_CNN
+DVI_VGA_VCC
R210 0-08
C174 .1U-16VX7-04
C175 1U-16VX7-06-O
G1 G2

Elitegroup Computer Systems		
Title: VGA		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
Date: Tuesday, July 28, 2015	Sheet 14 of 46	

Mitch 1/12 modified footprint.

Mitch 12/10 modified.

PCH1A

SPT-H_PCH

PME_L — GPP_A11/PME# — BD17

STP50 TP_AG15 AG15 — RSVD_AG15
STP57 TP_AG14 AG14 — RSVD_AG14
STP54 TP_AF17 AF17 — RSVD_AF17
STP40 TP_AE17 AE17 — RSVD_AE17

STP63 TP_AR19 AR19 — TP5
STP68 TP_AN17 AN17 — TP4

33,34 SPI_MOSI — R650 15-04 — SPI_MOSI_R BB29 — SPI0_MOSI
33,34 SPI_MISO — R651 15-04 — SPI_MISO_R BE30 — SPI0_MISO
33 SPI_CS_L0 — SR41 0-04-X — PCH_SPI_CS0 BD31 — SPI0_CS0#
33 SPI_CLK — R649 15-04 — PCH_SPI_CLK BC31 — SPI0_CLK
PCH_SPI_CS1 AW31 — SPI0_CS1#

STP102 STP118

34 SPI0_IO2 — SPI0_IO2 BC29 — SPI0_IO2
34 SPI0_IO3 — SPI0_IO3 BD30 — SPI0_IO3

STP96 PCH_SPI_CS2 AT31 — SPI0_CS2#
STP74 TP_SPI1_CS_N AL39 — GPP_D1/SPI1_CLK
STP72 TP_SPI1_MOSI AN41 — GPP_D0/SPI1_CS#
STP78 TP_SPI1_MISO AN38 — GPP_D3/SPI1_MOSI
STP79 TP_SPI1_IO3 AH43 — GPP_D2/SPI1_MISO
TP21 TP_SPI1_IO2 AG44 — GPP_D22/SPI1_IO2
TP20 — GPP_D21/SPI1_IO2

SPT_PCH_DT REV = 1.3

1 OF 12

GPP_B13/PLTRST# — BB27 PLTRST_R_N — R629 30-04 — PCH_PLTRST_L — PCH_PLTRST_L 28,30

GPP_G16/GSXCLK — P43 GPP_G16 — TP12
GPP_G12/GSXDOUT — R39 GPP_G12
GPP_G13/GSXSLOAD — R36 HDPANEL_DETECT — HDPANEL_DETECT 27
GPP_G14/GSXDIN — R42 GPP_G14
GPP_G15/GSXSRESET# — R41 GPP_G15 — GPP_G15 32

CPU_GP0 (thermal _down)

GPP_E3/CPU_GP0 — AF41 GPP_E3
GPP_E7/CPU_GP1 — AE44 THERMAL_SD — THERMAL_SD 30
GPP_B3/CPU_GP2 — BC23 BT_DIS_L_R — BT_DIS_L_R 21
GPP_B4/CPU_GP3 — BD24 GPP_B4

BC36 GPP_H18 — SML2CLK/DATA~SML4CLK/DATA for server only
GPP_H18/SML4ALERT# — BE34 GPP_H17
GPP_H17/SML4DATA — BD39 GPP_H16
GPP_H16/SML4CLK — BB36 GPP_H15
GPP_H15/SML3ALERT# — BA35 GPP_H14
GPP_H14/SML3DATA — BC35 GPP_H13
GPP_H13/SML3CLK — BD35 GPP_H12 — GPP_H12 34
GPP_H12/SML2ALERT# — AW35 GPP_H11 1 — STP84
GPP_H11/SML2DATA — BD34 GPP_H10 1 — TP45
GPP_H10/SML2CLK — BE11 PCH_INTRUDER_L — R598 1M-04 — +RTCVCC
INTRUDER#

for ACER reserve

+3VSB — R567 10K-04 — GPP_H14 — A1 — H2X1-WH — GND
+3VSB — R578 10K-04 — GPP_H15 — A2 — H2X1-WH — GND

+3VSB — PME_L — R638 10K-04

+VCC3

GPP_H13 — R652 10K-04-O
THERMAL_SD — R525 10K-04
HDPANEL_DETECT — R400 10K-04
GPP_G14 — R402 10K-04
GPP_G12 — R405 3.3K-04
GPP_B4 — R658 8.2K-04
GPP_E3 — SR25 8.2K-04-X

PCH1B

SPT-H_PCH

4 DMI_TX_N0 — DMI_TX_N0 L27 — DMI_RXN0
4 DMI_TX_P0 — DMI_TX_P0 N27 — DMI_RXP0
4 DMI_RX_N0 — DMI_RX_N0 C27 — DMI_TXN0
4 DMI_RX_P0 — DMI_RX_P0 B27 — DMI_TXP0
4 DMI_TX_N1 — DMI_TX_N1 E24 — DMI_RXN1
4 DMI_TX_P1 — DMI_TX_P1 G24 — DMI_RXP1
4 DMI_RX_N1 — DMI_RX_N1 B28 — DMI_TXN1
4 DMI_RX_P1 — DMI_RX_P1 A28 — DMI_TXP1
4 DMI_TX_N2 — DMI_TX_N2 G27 — DMI_RXN2
4 DMI_TX_P2 — DMI_TX_P2 E26 — DMI_RXP2
4 DMI_RX_N2 — DMI_RX_N2 B29 — DMI_TXN2
4 DMI_RX_P2 — DMI_RX_P2 C29 — DMI_TXP2
4 DMI_TX_N3 — DMI_TX_N3 L29 — DMI_RXN3
4 DMI_TX_P3 — DMI_TX_P3 K29 — DMI_RXP3
4 DMI_RX_N3 — DMI_RX_N3 B30 — DMI_TXN3
4 DMI_RX_P3 — DMI_RX_P3 A30 — DMI_TXP3

DMI

R443 100-1-04 — PCIERCOMP_N B18 — PCIERCOMP_P C17 — PCIE_RCOMPN — PCIE_RCOMPP

W=12 S=12

USB 2.0

22 PEX1_RX_N5 — PEX1_RX_N5 K19 — PEX1_RX_P5 L19 — PEX1_TX_N5 D22 — PEX1_TX_P5 C22

Mitch 12/10 deleted.

28 GLAN_RX_N7 — GLAN_RX_N7 L22 — GLAN_RX_P7 K22 — GLAN_TX_N7 C23 — GLAN_TX_P7 B23

Mitch 12/10 deleted.

PCIE1_RXN/USB3_7_RXN — H15
PCIE1_RXP/USB3_7_RXP — G15
PCIE1_TXN/USB3_7_TXN — A16
PCIE1_TXP/USB3_7_TXP — B16
PCIE2_TXN/USB3_8_TXN — B19
PCIE2_TXP/USB3_8_TXP — C19
PCIE2_RXN/USB3_8_RXN — E17
PCIE2_RXP/USB3_8_RXP — G17
PCIE3_RXN/USB3_9_RXN — L17
PCIE3_RXP/USB3_9_RXP — K17
PCIE3_TXN/USB3_9_TXN — B20
PCIE3_TXP/USB3_9_TXP — C20
PCIE4_RXN/USB3_10_RXN — E20
PCIE4_RXP/USB3_10_RXP — G19
PCIE4_TXN/USB3_10_TXN — B21
PCIE4_TXP/USB3_10_TXP — A21
PCIE5_RXN — K19
PCIE5_RXP — L19
PCIE5_TXN — D22
PCIE5_TXP — C22
PCIE6_RXN — G22
PCIE6_RXP — E22
PCIE6_TXN — B22
PCIE6_TXP — A23
PCIE7_RXN — L22
PCIE7_RXP — K22
PCIE7_TXN — C23
PCIE7_TXP — B23
PCIE8_RXN — K24
PCIE8_RXP — L24
PCIE8_TXN — C24
PCIE8_TXP — B24

PCIE

PCH/USB3.0

N/A

LAN ONLY

USB2N_1 — AF5 USB_N1 — USB_N1 24
USB2P_1 — AG7 USB_P1 — USB_P1 24
USB2N_2 — AD5 USB_N2 — USB_N2 24
USB2P_2 — AD7 USB_P2 — USB_P2 24
USB2N_3 — AG8 USB_N3 — USB_N3 24
USB2P_3 — AG10 USB_P3 — USB_P3 24
USB2N_4 — AE1 USB_N4 — USB_N4 24
USB2P_4 — AE2 USB_P4 — USB_P4 24
USB2N_5 — AC2 USB_N5 — USB_N5 25
USB2P_5 — AC3 USB_P5 — USB_P5 25
USB2N_6 — AF2 USB_N6 — USB_N6 25
USB2P_6 — AF3 USB_P6 — USB_P6 25
USB2N_7 — AB3 USB_N7 — USB_N7 25
USB2P_7 — AB2 USB_P7 — USB_P7 25
USB2N_8 — AL8 USB_N8 — USB_N8 25
USB2P_8 — AL7 USB_P8 — USB_P8 25
USB2N_9 — AA1 USB_N9 — USB_N9 25
USB2P_9 — AA2 USB_P9 — USB_P9 25
USB2N_10 — AJ8 USB_N10 — USB_N10 25
USB2P_10 — AJ7 USB_P10 — USB_P10 25
USB2N_11 — W2
USB2P_11 — W3
USB2N_12 — AD3
USB2P_12 — AD2
USB2N_13 — Y2
USB2P_13 — Y1
USB2N_14 — AJ11
USB2P_14 — AJ13

Rear IO USB3.0
Front USB3.0
Rear IO USB2.0
Front USB2.0
mPCIE

N/A

GPP_E9/USB2_OC0# — AD43 GPP_E9 — GPP_E9 33
GPP_E10/USB2_OC1# — AD42 GPP_E10 — GPP_E10 33
GPP_E11/USB2_OC2# — AD39 USB_OC2_L
GPP_E12/USB2_OC3# — AC44 USB_OC3_L — USB_OC3_L 34
GPP_F15/USB2_OCB_4 — Y43 GPP_F15 — GPP_F15 31
GPP_F16/USB2_OCB_5 — Y41 GPP_F16 — GPP_F16 25
GPP_F17/USB2_OCB_6 — W44 LPC_PME_L — LPC_PME_L 30
GPP_F18/USB2_OCB_7 — W43 USB_OC7_L

USB2_COMP — AG3 USB2_COMP — R494 113-1-04
USB2_VBUSSENSE — AD10 USB2_VBUSSENSE — R492 1K-04
RSVD_AB13 — AB13 TP_PCH_AB13 — STP39
USB2_ID — AG2 USB2_ID — R493 1K-04

GND

GPD7/RSVD — BD14 GPD7

SPT_PCH_DT REV = 1.3

2 OF 12

Model Version	GPP_H18	GPP_H17	GPP_H16
V1.0(For MP)	0	0	0
V1.1(Next Ver)	0	0	1
V1.X(Next Ver)	X	X	X

+3VSB

GPP_E9 — R520 10K-04
GPP_E10 — R502 10K-04-O
USB_OC2_L — R513 10K-04

+3VSB

GPP_F15 — R456 10K-04
GPP_F16 — R491 10K-04
LPC_PME_L — R455 10K-04-O
USB_OC7_L — R437 10K-04

Mitch 6/17 re-staffed.

+ATX_3VSB

GPD7 — SR59 10K-04-X-O

Mitch 1/9 added.

+3VSB — GPP_H18 — SR61 8.2K-04-X(2-3) — GND
+3VSB — GPP_H17 — SR62 8.2K-04-X(2-3) — GND
+3VSB — GPP_H16 — SR60 8.2K-04-X(2-3) — GND

Header — HDA_SDO_R1
ME Disable — 0-04(1-2) RJ4 — HDA_SDO_R — HDA_SDO_R 16
GPIO — PCH_GPIO24_DIS_ME

Disable ME Jumper

MODE	SPI override
Disable ME	2-3
NORMAL	1-2

*HDA_SDO with internal pull-down

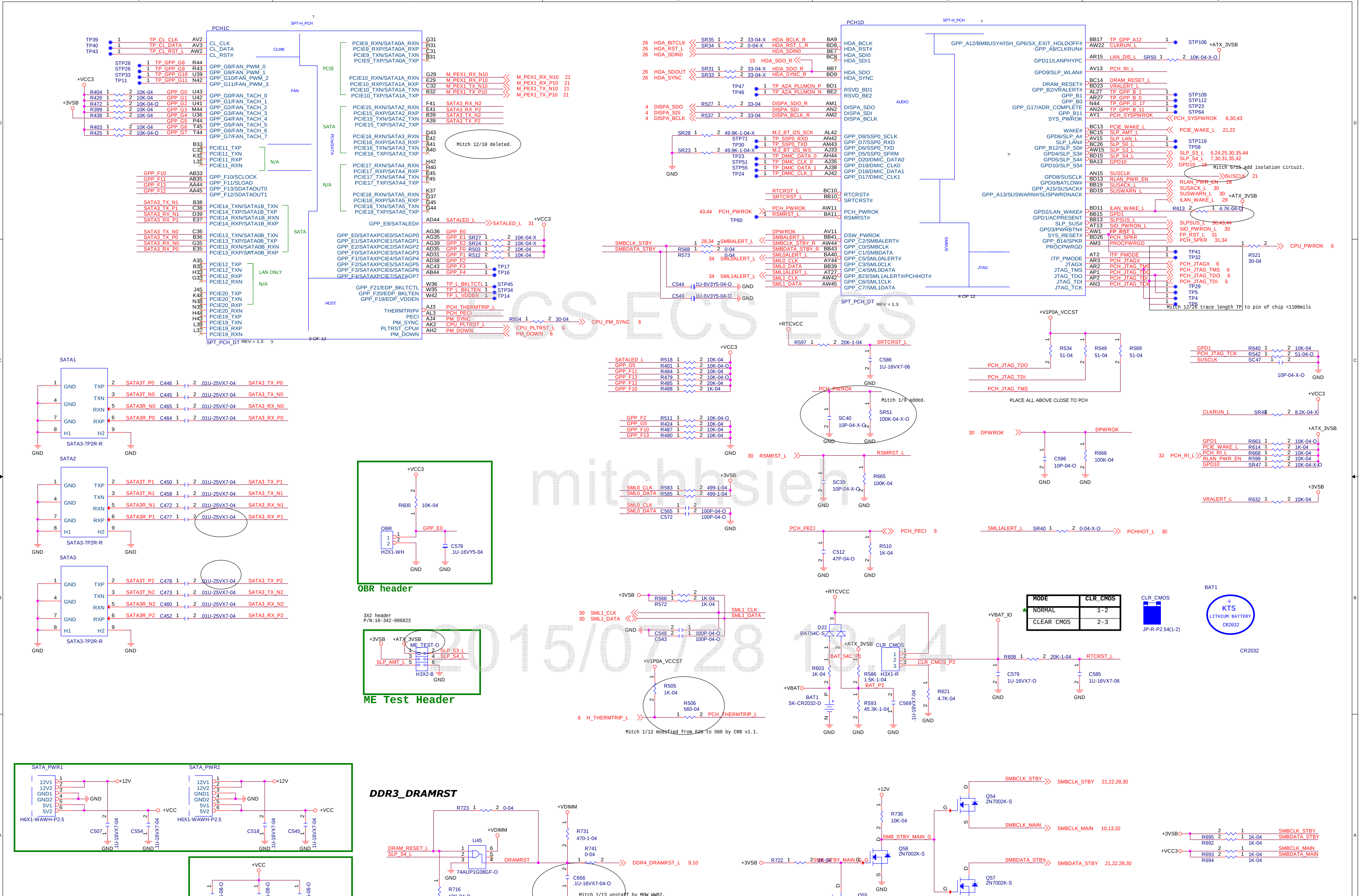
+3VSB — R699 1K-04 — ME_DISABLE — JP-BK(1-2)
ME_DISABLE — HDA_SDO_R_P1 — HDA_SDO_R1 — H3X1-B

ME disable

ME Disable

+3VSB — R704 1K-04 — PCH_GPIO24_DIS_ME_B — PCH_GPIO24_DIS_ME_C
16 GPD10 — R713 4.7K-04 — Q50 MMBT3904-S
PCH_GPIO24_DIS_ME

Elitegroup Computer Systems			
Title: PCH-SPI/DMI/PCIE/USB2.0			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 15 of 46		



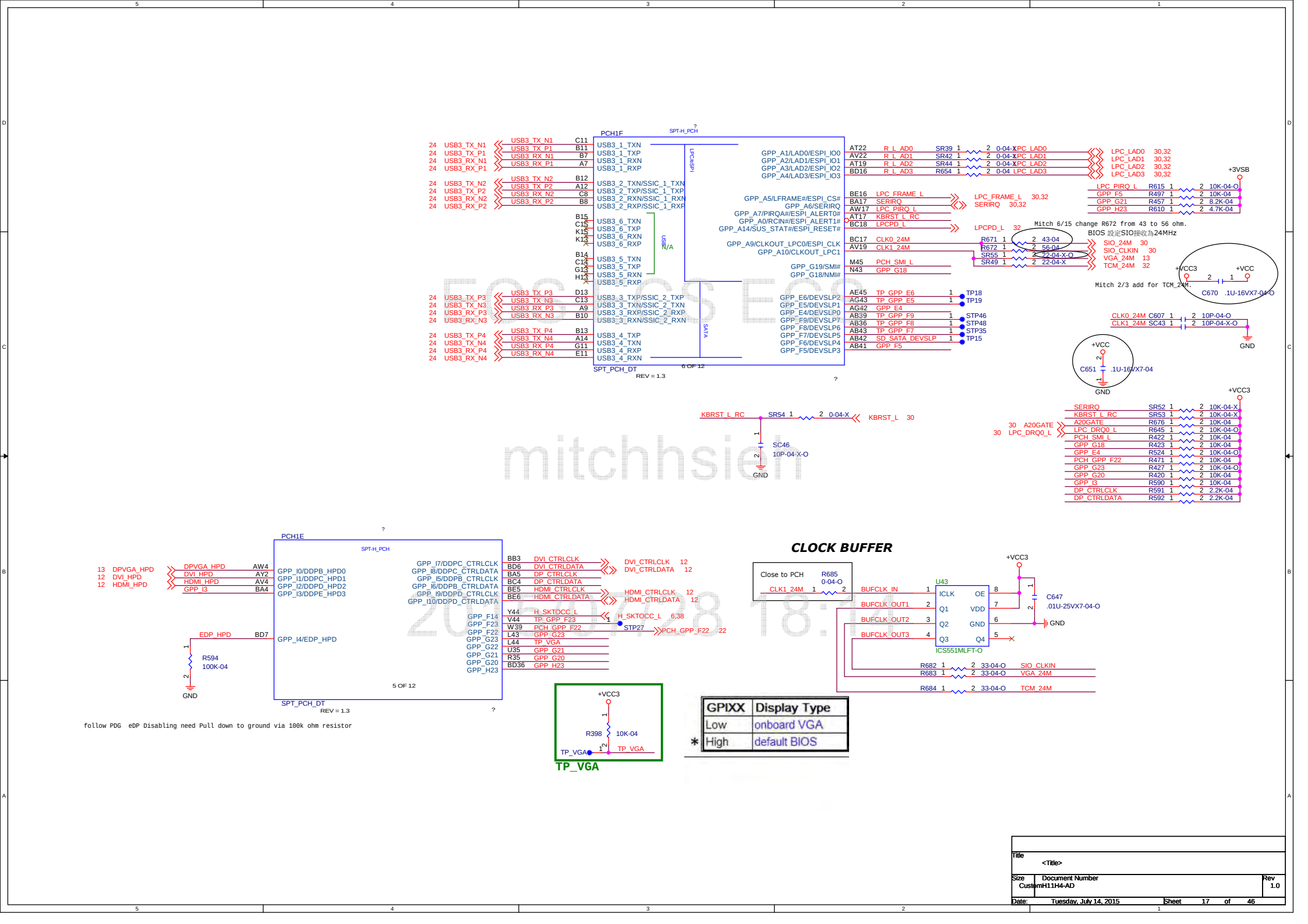
MODE	CLR_CMOS
NORMAL	1-2
CLEAR CMOS	2-3

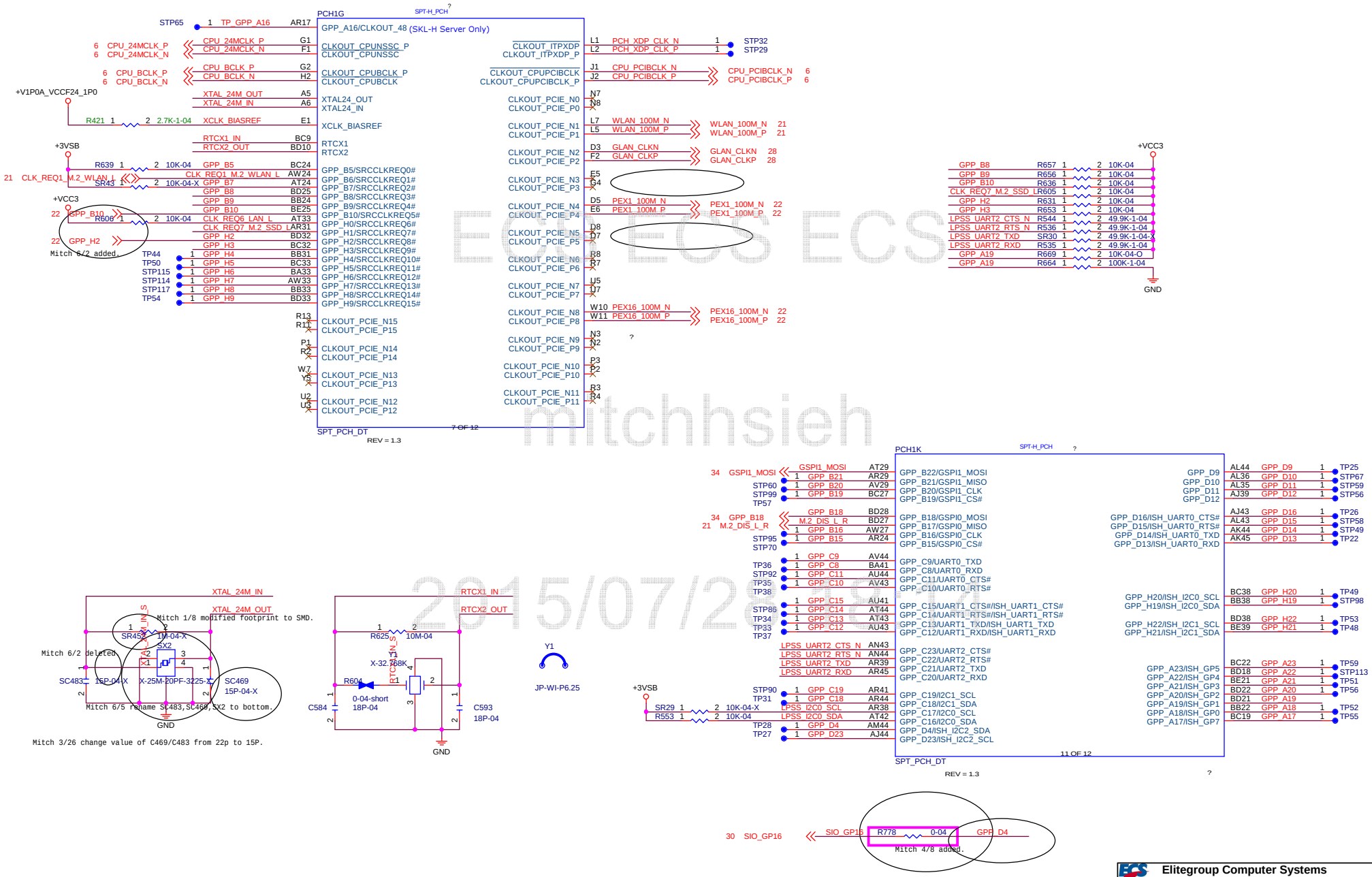
Elitegroup Computer Systems

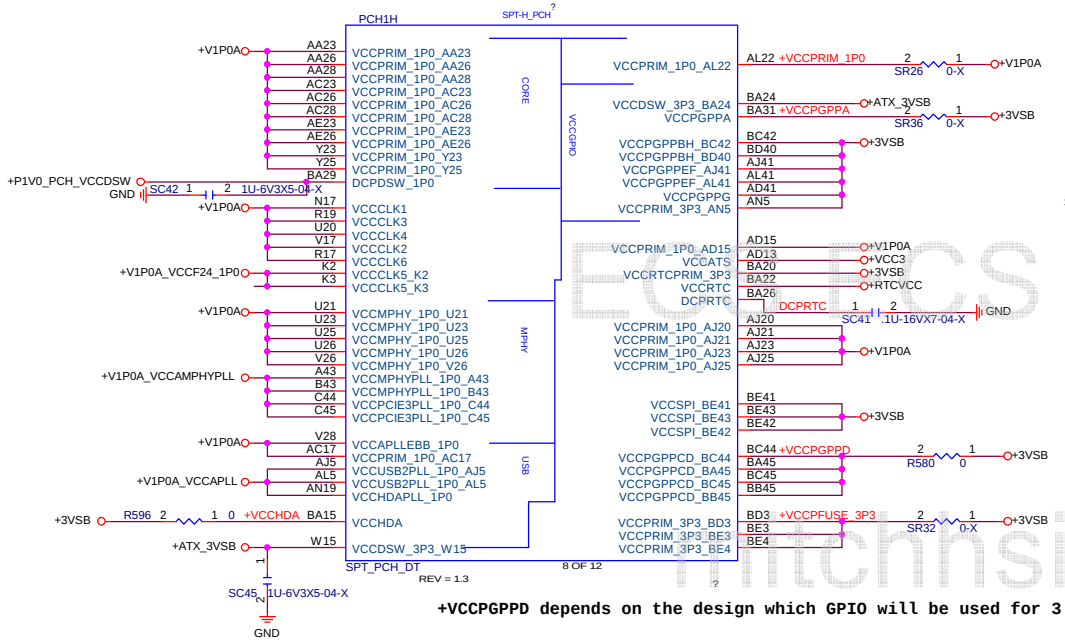
Title: <Title>

Size	Document Number	Rev
A2	H11H4-AD	1.0

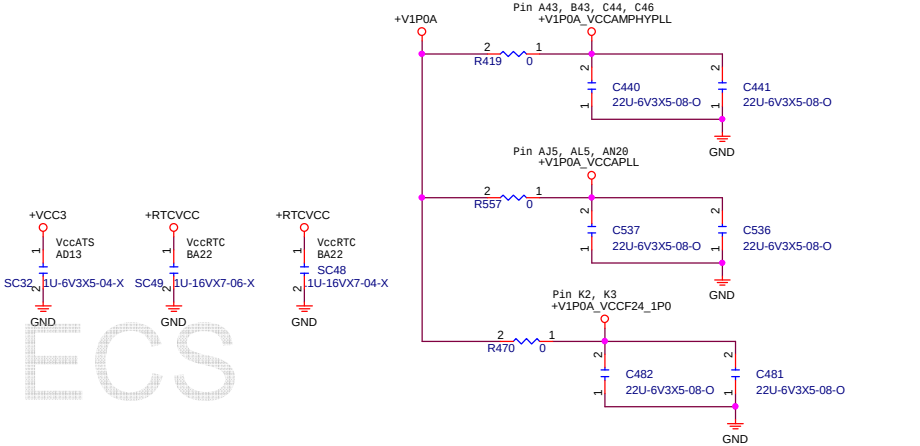
Date: Tuesday, July 14, 2015 Sheet 16 of 46

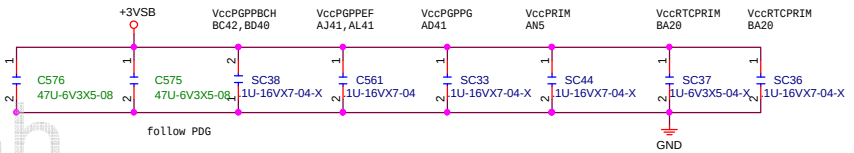

PCH1F
SPT-H_PCH
SPT_PCH_DT
REV = 1.3
6 OF 12
USB3_TX_N1
USB3_TX_P1
USB3_RX_N1
USB3_RX_P1
USB3_TX_N2
USB3_TX_P2
USB3_RX_N2
USB3_RX_P2
USB3_TX_P3
USB3_TX_N3
USB3_RX_P3
USB3_RX_N3
USB3_TX_P4
USB3_TX_N4
USB3_RX_P4
USB3_RX_N4
USB3_1_TXN
USB3_1_TXP
USB3_1_RXN
USB3_1_RXP
USB3_2_TXN/SSIC_1_TXN
USB3_2_TXP/SSIC_1_TXP
USB3_2_RXN/SSIC_1_RXN
USB3_2_RXP/SSIC_1_RXP
USB3_6_TXN
USB3_6_TXP
USB3_6_RXN
USB3_6_RXP
USB3_5_TXN
USB3_5_TXP
USB3_5_RXN
USB3_5_RXP
USB3_3_TXP/SSIC_2_TXP
USB3_3_TXN/SSIC_2_TXN
USB3_3_RXP/SSIC_2_RXP
USB3_3_RXN/SSIC_2_RXN
USB3_4_TXP
USB3_4_TXN
USB3_4_RXP
USB3_4_RXN
LPC&SPI
USB
N/A
SATA
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS#
GPP_A6/SERIRQ
GPP_A7/PIRQA#/ESPI_ALERT0#
GPP_A0/RCIN#/ESPI_ALERT1#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_G19/SMI#
GPP_G18/NMI#
GPP_E6/DEVSLP2
GPP_E5/DEVSLP1
GPP_E4/DEVSLP0
GPP_F9/DEVSLP7
GPP_F8/DEVSLP6
GPP_F7/DEVSLP5
GPP_F6/DEVSLP4
GPP_F5/DEVSLP3
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
LPC_FRAME_L
SERIRQ
LPC_PIRQ_L
KBRST_L_RC
LPCPD_L
CLK0_24M
CLK1_24M
PCH_SMI_L
GPP_G18
TP_GPP_E6
TP_GPP_E5
GPP_E4
TP_GPP_F9
TP_GPP_F8
TP_GPP_F7
SD_SATA_DEVSLP
GPP_F5
TP18
TP19
STP46
STP48
STP35
TP15
SIO_24M
SIO_CLKIN
VGA_24M
TCM_24M
GPP_F5
GPP_G21
GPP_H23
+3VSB
+VCC3
+VCC
GND
C670 .1U-16VX7-04-O
C651 .1U-16VX7-04
C607 10P-04-O
SC43 10P-04-X-O
SC46 10P-04-X-O
SR54 0-04-X
SR52 10K-04-X
SR53 10K-04-X
A20GATE
LPC_DRQ0_L
R676 10K-04
R645 10K-04-O
R422 10K-04
R423 10K-04
R524 10K-04-O
R471 10K-04
R427 10K-04-O
R420 10K-04
R590 10K-04
R591 2.2K-04
R592 2.2K-04
Mitch 6/15 change R672 from 43 to 56 ohm.
BIOS 設定SIO接收為24MHz
Mitch 2/3 add for TCM_24M.
PCH1E
SPT-H_PCH
SPT_PCH_DT
REV = 1.3
5 OF 12
DPVGA_HPD
DVI_HPD
HDMI_HPD
GPP_I3
EDP_HPD
R594 100K-04
GPP_I0/DDPB_HPD0
GPP_I1/DDPC_HPD1
GPP_I2/DDPD_HPD2
GPP_I3/DDPE_HPD3
GPP_I4/EDP_HPD
GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
DVI_CTRLCLK
DVI_CTRLDATA
DP_CTRLCLK
DP_CTRLDATA
HDMI_CTRLCLK
HDMI_CTRLDATA
H_SKTOCC_L
TP_GPP_F23
PCH_GPP_F22
GPP_G23
TP_VGA
GPP_G21
GPP_G20
GPP_H23
STP27
follow PDG eDP Disabling need Pull down to ground via 100k ohm resistor
CLOCK BUFFER
Close to PCH
CLK1_24M
R685 0-04-O
U43
ICS551MLFT-O
BUFCLK_IN
BUFCLK_OUT1
BUFCLK_OUT2
BUFCLK_OUT3
ICLK
Q1
Q2
Q3
OE
VDD
GND
Q4
C647 .01U-25VX7-04-O
R682 33-04-O
R683 33-04-O
R684 33-04-O
SIO_CLKIN
VGA_24M
TCM_24M
R398 10K-04
TP_VGA
GPIXX
Display Type
Low
onboard VGA
High
default BIOS
Title
<Title>
Size
Document Number
CustomH11H4-AD
Rev
1.0
Date:
Tuesday, July 14, 2015
Sheet
17
of
46

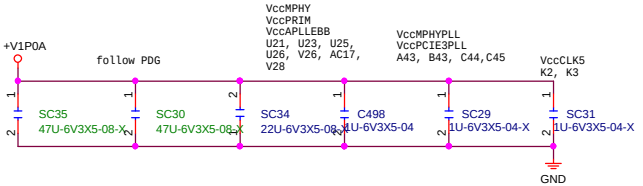

PCH1G
SPT-H_PCH
GPP_A16/CLKOUT_48 (SKL-H Server Only)
CLKOUT_CPUNSSC_P
CLKOUT_CPUNSSC
CLKOUT_CPUBCLK_P
CLKOUT_CPUBCLK
XTAL24_OUT
XTAL24_IN
XCLK_BIASREF
RTCX1
RTCX2
GPP_B5/SRCCLKREQ0#
GPP_B6/SRCCLKREQ1#
GPP_B7/SRCCLKREQ2#
GPP_B8/SRCCLKREQ3#
GPP_B9/SRCCLKREQ4#
GPP_B10/SRCCLKREQ5#
GPP_H0/SRCCLKREQ6#
GPP_H1/SRCCLKREQ7#
GPP_H2/SRCCLKREQ8#
GPP_H3/SRCCLKREQ9#
GPP_H4/SRCCLKREQ10#
GPP_H5/SRCCLKREQ11#
GPP_H6/SRCCLKREQ12#
GPP_H7/SRCCLKREQ13#
GPP_H8/SRCCLKREQ14#
GPP_H9/SRCCLKREQ15#
CLKOUT_PCIE_N15
CLKOUT_PCIE_P15
CLKOUT_PCIE_N14
CLKOUT_PCIE_P14
CLKOUT_PCIE_N13
CLKOUT_PCIE_P13
CLKOUT_PCIE_N12
CLKOUT_PCIE_P12
CLKOUT_ITPXDP
CLKOUT_ITPXDP_P
CLKOUT_CPUPCIBCLK
CLKOUT_CPUPCIBCLK_P
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
CLKOUT_PCIE_N6
CLKOUT_PCIE_P6
CLKOUT_PCIE_N7
CLKOUT_PCIE_P7
CLKOUT_PCIE_N8
CLKOUT_PCIE_P8
CLKOUT_PCIE_N9
CLKOUT_PCIE_P9
CLKOUT_PCIE_N10
CLKOUT_PCIE_P10
CLKOUT_PCIE_N11
CLKOUT_PCIE_P11
7 OF 12
SPT_PCH_DT
REV = 1.3
PCH1K
SPT-H_PCH
11 OF 12
SPT_PCH_DT
REV = 1.3
STP65
TP_GPP_A16
CPU_24MCLK_P
CPU_24MCLK_N
CPU_BCLK_P
CPU_BCLK_N
+V1P0A_VCCF24_1P0
R421 2.7K-1-04
+3VSB
R639 10K-04
SR43 10K-04-X
+VCC3
R606 10K-04
Mitch 6/2 added.
TP44
TP50
STP115
STP114
STP117
TP54
R13
R11
P1
R2
W7
Y5
U2
U3
L1 PCH_XDP_CLK_N
L2 PCH_XDP_CLK_P
STP32
STP29
J1 CPU_PCIBCLK_N
J2 CPU_PCIBCLK_P
N7
N8
L7 WLAN_100M_N
L5 WLAN_100M_P
D3 GLAN_CLKN
F2 GLAN_CLKP
E5
G4
D5 PEX1_100M_N
E6 PEX1_100M_P
D8
D7
R8
R7
U5
Q7
W10 PEX16_100M_N
W11 PEX16_100M_P
N3
N2
P3
P2
R3
R4
GPP_B8 R657 2 10K-04
GPP_B9 R656 2 10K-04
GPP_B10 R636 2 10K-04
CLK_REQ7_M.2_SSD_L R605 2 10K-04
GPP_H2 R631 2 10K-04
GPP_H3 R653 2 10K-04
LPSS_UART2_CTS_N R544 2 49.9K-1-04
LPSS_UART2_RTS_N R536 2 49.9K-1-04
LPSS_UART2_TXD SR30 2 49.9K-1-04-X
LPSS_UART2_RXD R535 2 49.9K-1-04
GPP_A19 R669 2 10K-04-O
GPP_A19 R664 2 100K-1-04
+VCC3
GND
GSPI1_MOSI
GPP_B21
GPP_B20
GPP_B19
GPP_B18
M.2_DIS_L_R
GPP_B16
GPP_B15
GPP_C9
GPP_C8
GPP_C11
GPP_C10
GPP_C15
GPP_C14
GPP_C13
GPP_C12
LPSS_UART2_CTS_N
LPSS_UART2_RTS_N
LPSS_UART2_TXD
LPSS_UART2_RXD
GPP_C19
GPP_C18
LPSS_I2C0_SCL
LPSS_I2C0_SDA
GPP_D4
GPP_D23
GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B20/GSPI1_CLK
GPP_B19/GSPI1_CS#
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B16/GSPI0_CLK
GPP_B15/GSPI0_CS#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_D4/ISH_I2C2_SDA
GPP_D23/ISH_I2C2_SCL
GPP_D9
GPP_D10
GPP_D11
GPP_D12
GPP_D16/ISH_UART0_CTS#
GPP_D15/ISH_UART0_RTS#
GPP_D14/ISH_UART0_TXD
GPP_D13/ISH_UART0_RXD
GPP_H20/ISH_I2C0_SCL
GPP_H19/ISH_I2C0_SDA
GPP_H22/ISH_I2C1_SCL
GPP_H21/ISH_I2C1_SDA
GPP_A23/ISH_GP5
GPP_A22/ISH_GP4
GPP_A21/ISH_GP3
GPP_A20/ISH_GP2
GPP_A19/ISH_GP1
GPP_A18/ISH_GP0
GPP_A17/ISH_GP7
XTAL_24M_IN
XTAL_24M_OUT
Mitch 1/8 modified footprint to SMD.
SR453 1M-04-X
SX2
Mitch 6/2 deleted
SC483 15P-04-X
X-25M-20PF-3225-X
SC469 15P-04-X
Mitch 6/5 rename SC483,SC469,SX2 to bottom.
GND
Mitch 3/26 change value of C469/C483 from 22p to 15P.
RTCX1_IN
RTCX2_OUT
R625 10M-04
X-32.768K
R604 0-04-short 18P-04
C584 18P-04
C593 18P-04
GND
Y1
JP-WI-P6.25
+3VSB
SR29 10K-04-X
R553 10K-04
SIO_GP16
R778 0-04
Mitch 4/8 added.
Elitegroup Computer Systems
Title
<Title>
Size Custom
Document Number H11H4-AD
Rev 1.0
Date: Tuesday, July 28, 2015
Sheet 18 of 46

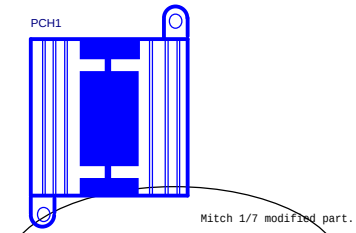


+VCCPGPPD depends on the design which GPIO will be used for 3.3V or 1.8V.

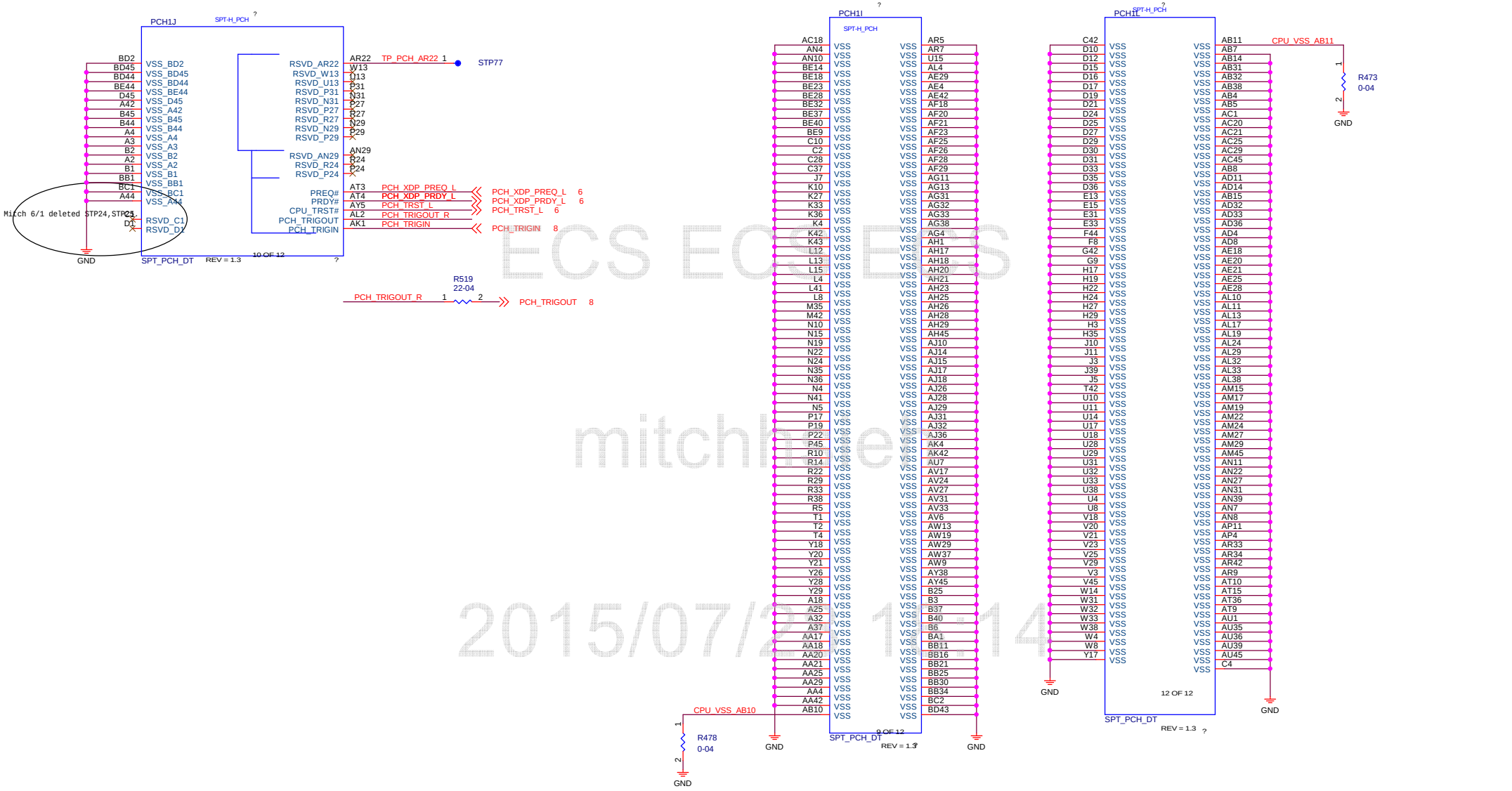






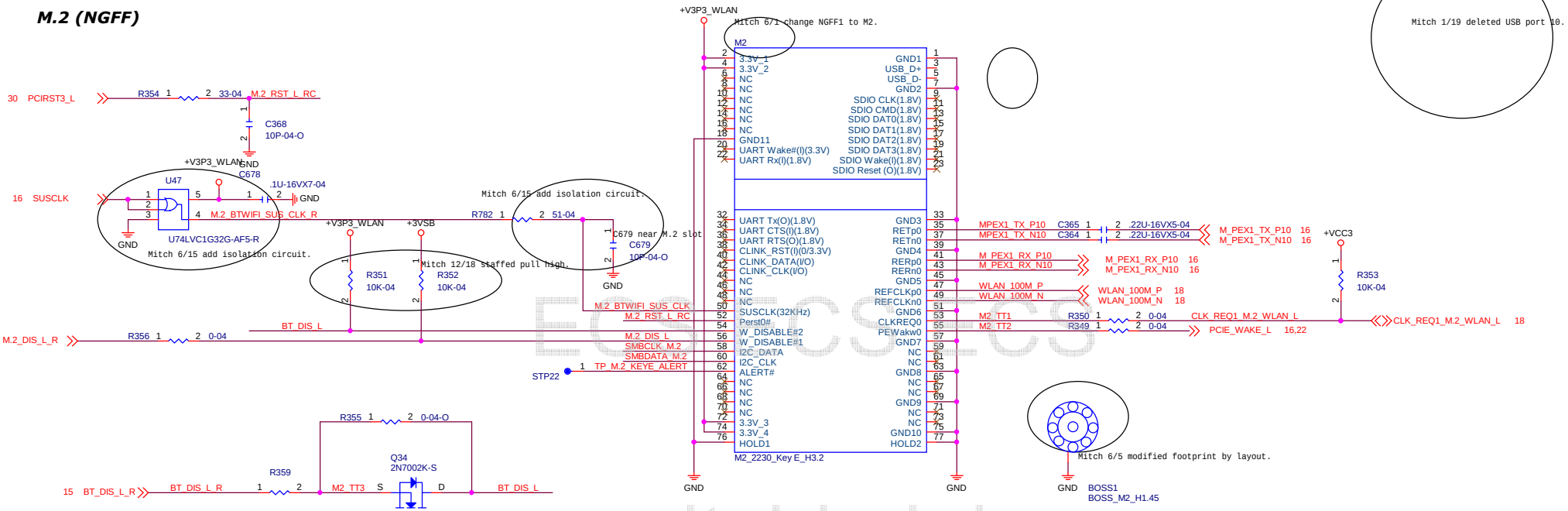


Elitegroup Computer Systems			
Title: PCH-PWR			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 19 of 46		

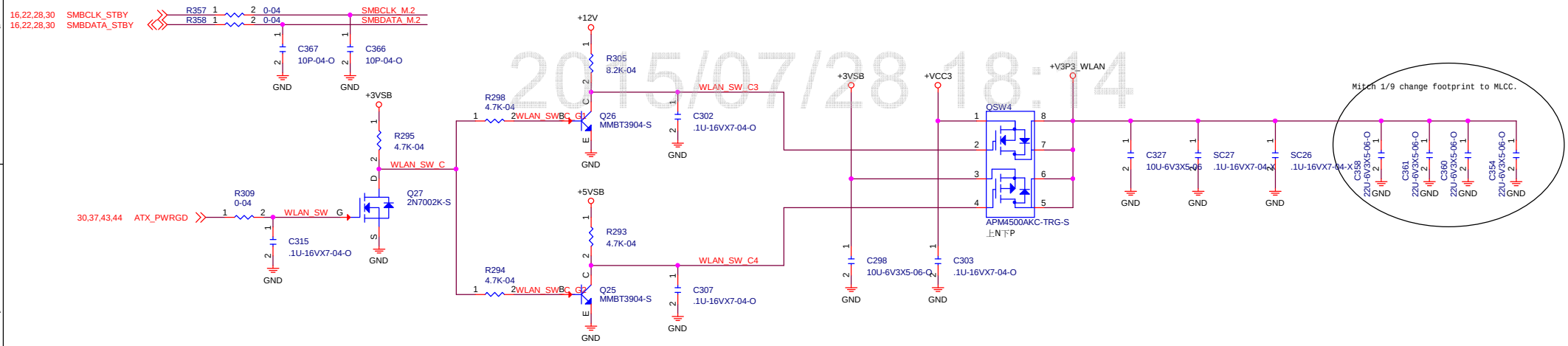


Elitegroup Computer Systems			
Title: PCH-GND			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 20 of 46		

M.2 (NGFF)



Key	Power Rail	Voltage Tolerance	Current Consumption Limit Peak mA Max Avg @ 100 µs	Current Consumption Limit Normal mA Max Avg @ 1 s
E	3.3 V	± 5%	2000	



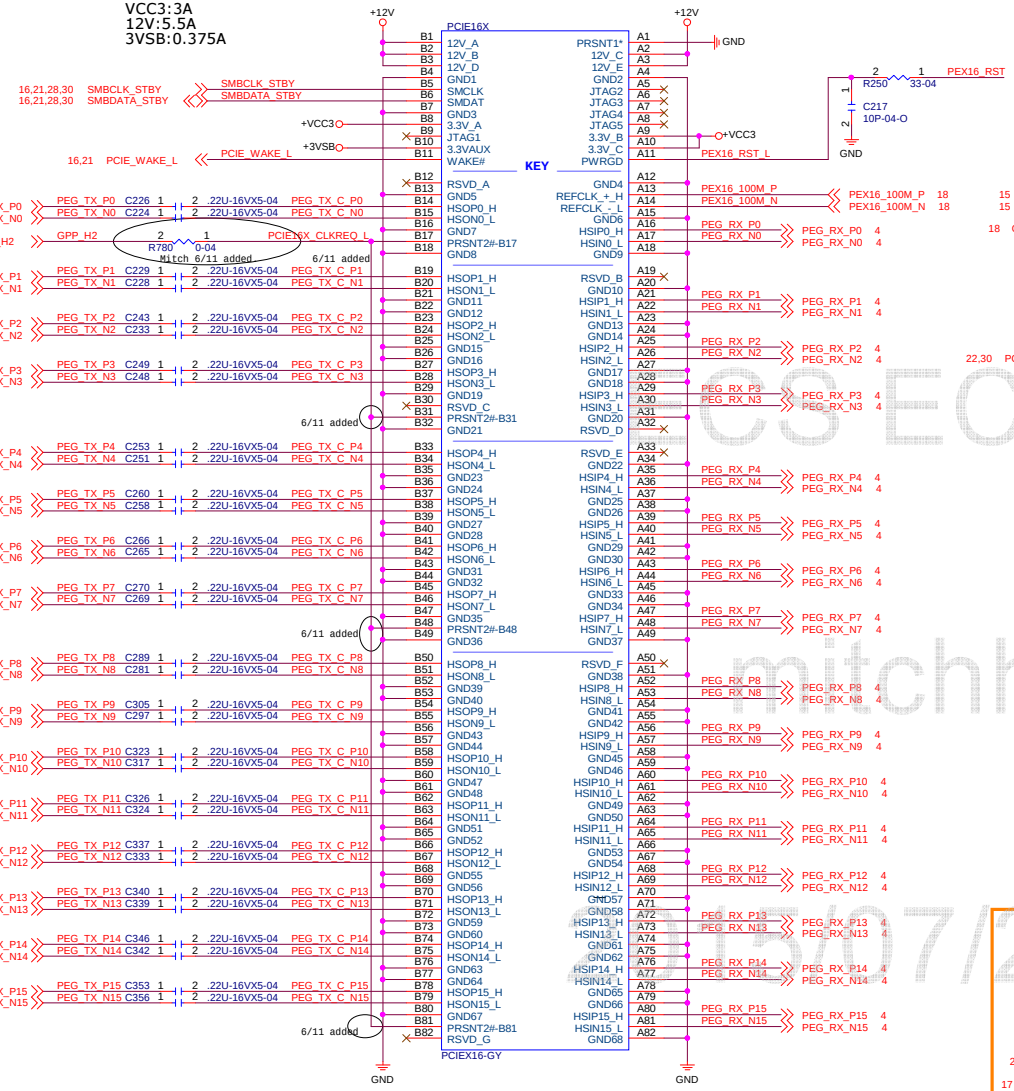
	ATX_PWRGD	+V3P3_WLAN
S0	1	+VCC3
S3/S4/S5	0	+3VSB

Elitegroup Computer Systems	
Title	M.2 Slot
Size: Custom	Document Number: H11H4-AD
Rev	1.0
Date:	Tuesday, July 14, 2015
Sheet	21 of 46

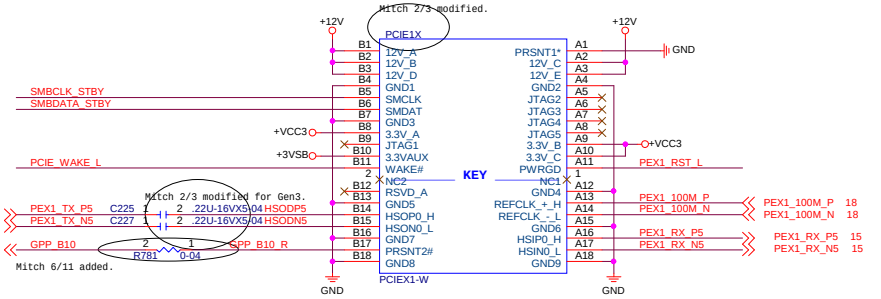
one slot support dual lan card,reserve

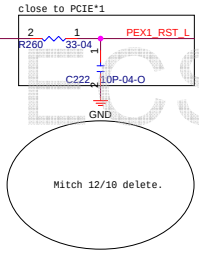
PCI-E X16 SLOT

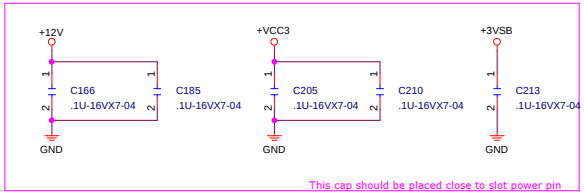
PCI-E SPEC
VCC3:3A
12V:5.5A
3VSB:0.375A



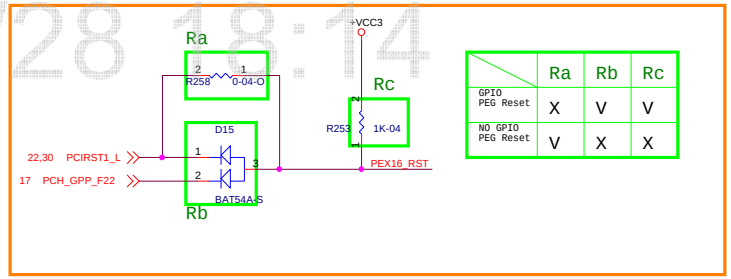
PCI-E X1 SLOT1



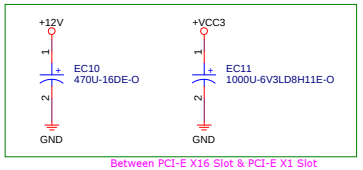


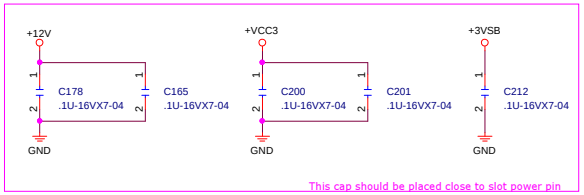


PCI-E X1 SLOT2



	Ra	Rb	Rc
GPIO PEG Reset	X	V	V
NO GPIO PEG Reset	V	X	X



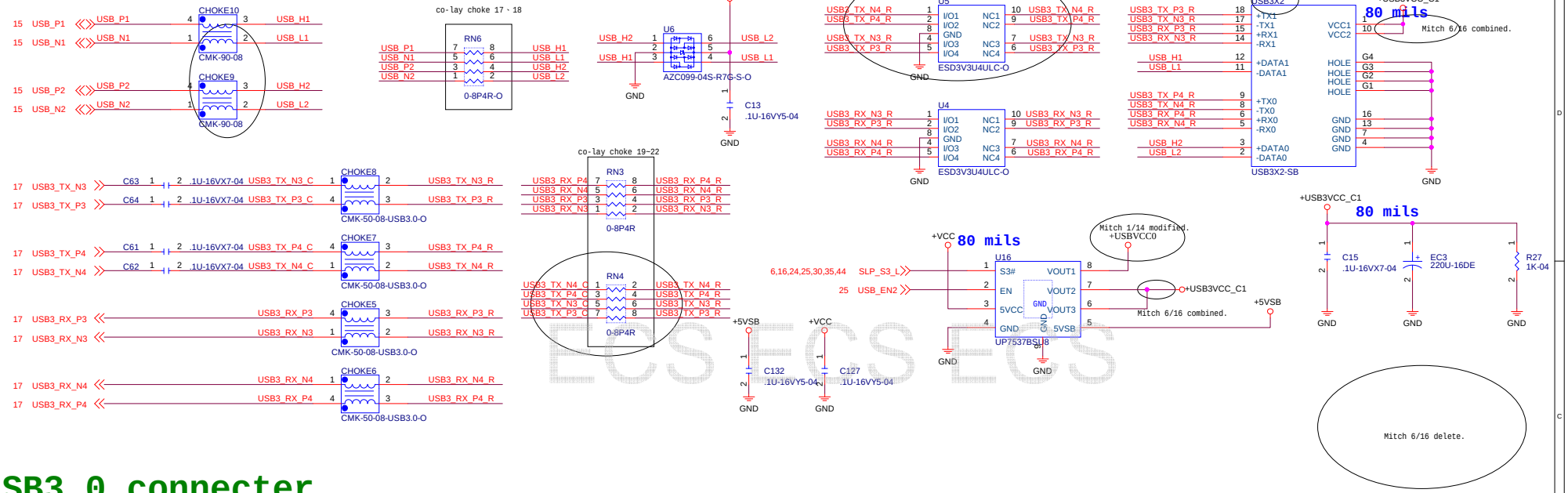


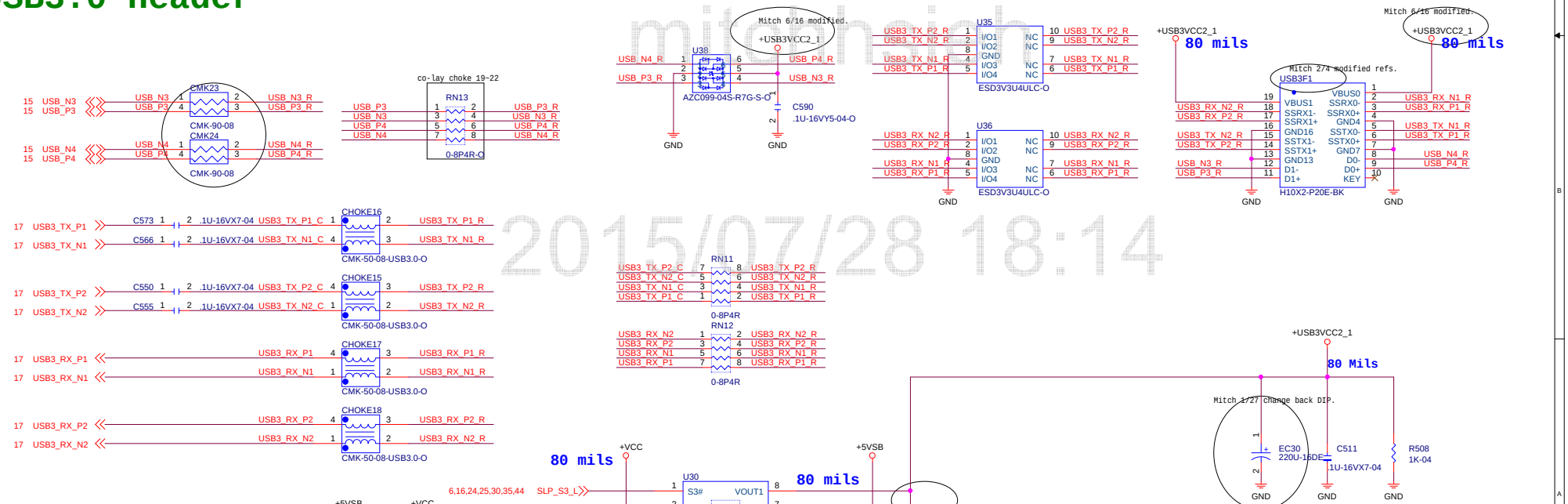
Company	Elitegroup Computer Systems
Title	PCI-E X16/X1
Size	Custom
Document Number	H11H4-AD
Rev	1.0
Date:	Tuesday, July 14, 2015
Sheet	22 of 46

Title: HDMI		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 23 of 46	

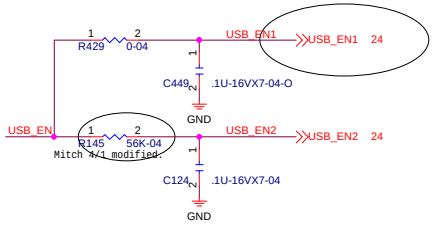
USB3.0 connecter

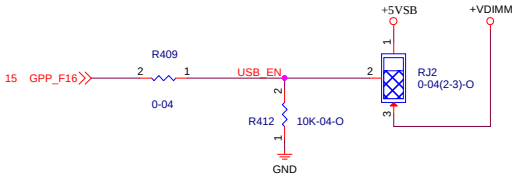
USB3.0 Header



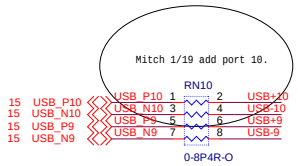


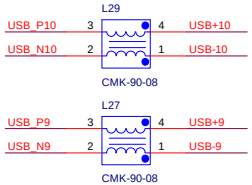
Elitegroup Computer Systems		
Title: USB3.0 Connector/Header		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 24 of 46	

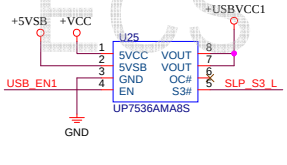


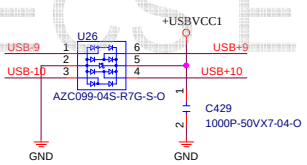


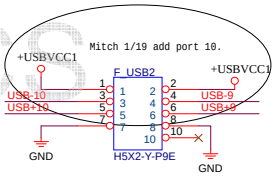
	uP7536 Enable use	RJ?	RJ?	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (1-2)	NA	0 Volt	Acer S4 w/o S5 w/ USB_5VDUAL
	5VSB	0ohm (2-3)	NA	5 Volt	
*	GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	

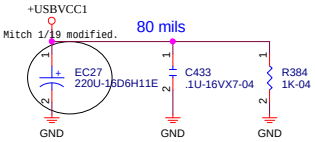


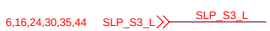


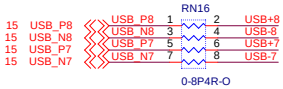


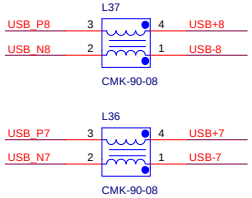


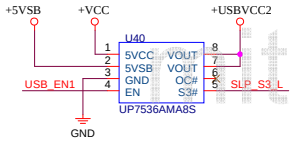


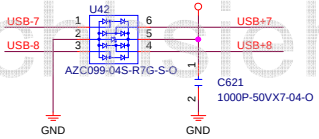


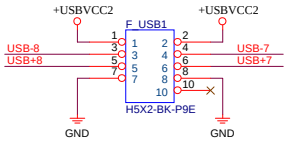


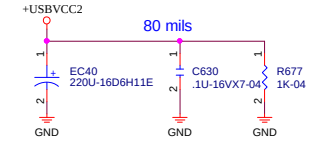






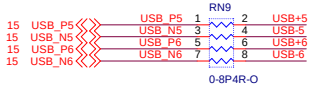


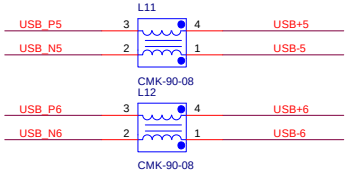


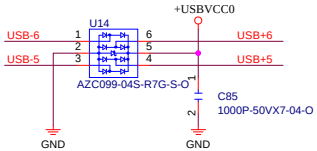


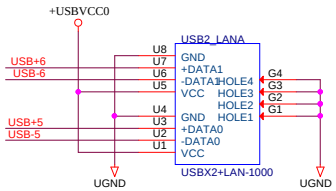
USB2.0 header

USB2.0 connecter

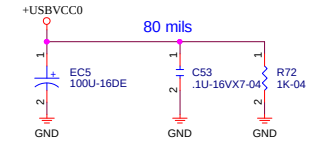




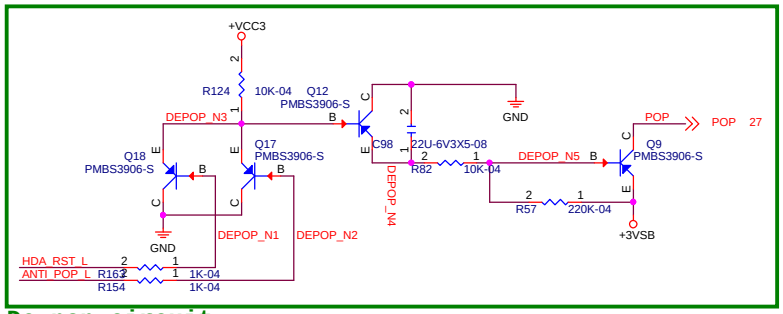




Lan + USB2.0

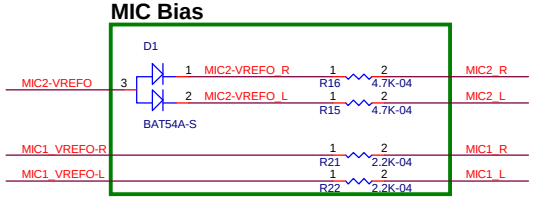


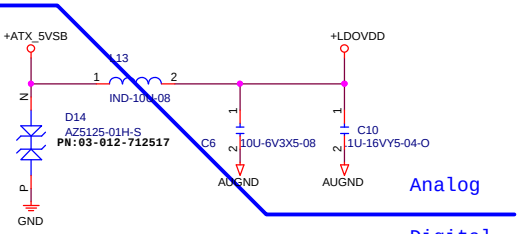
Elitegroup Computer Systems	
Title: USB2.0 Connector/Header	
Size: Custom	Document Number: H11H4-AD
Rev: 1.0	
Date: Tuesday, July 14, 2015	Sheet 25 of 46



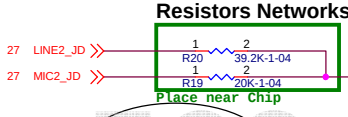
De-pop circuit

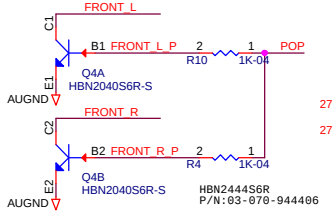
MIC Bias

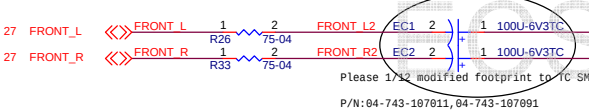


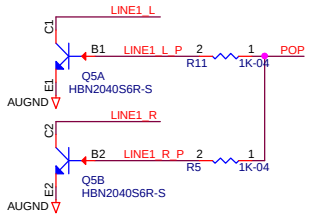


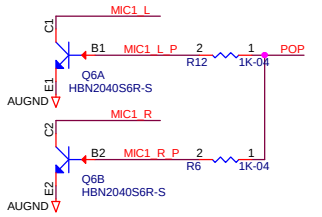
Resistors Networks

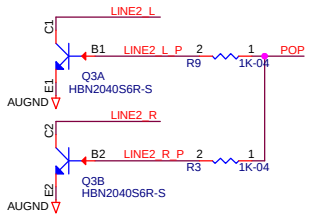


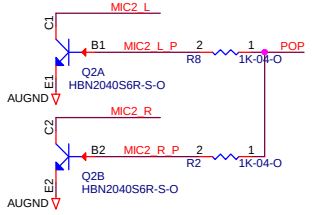


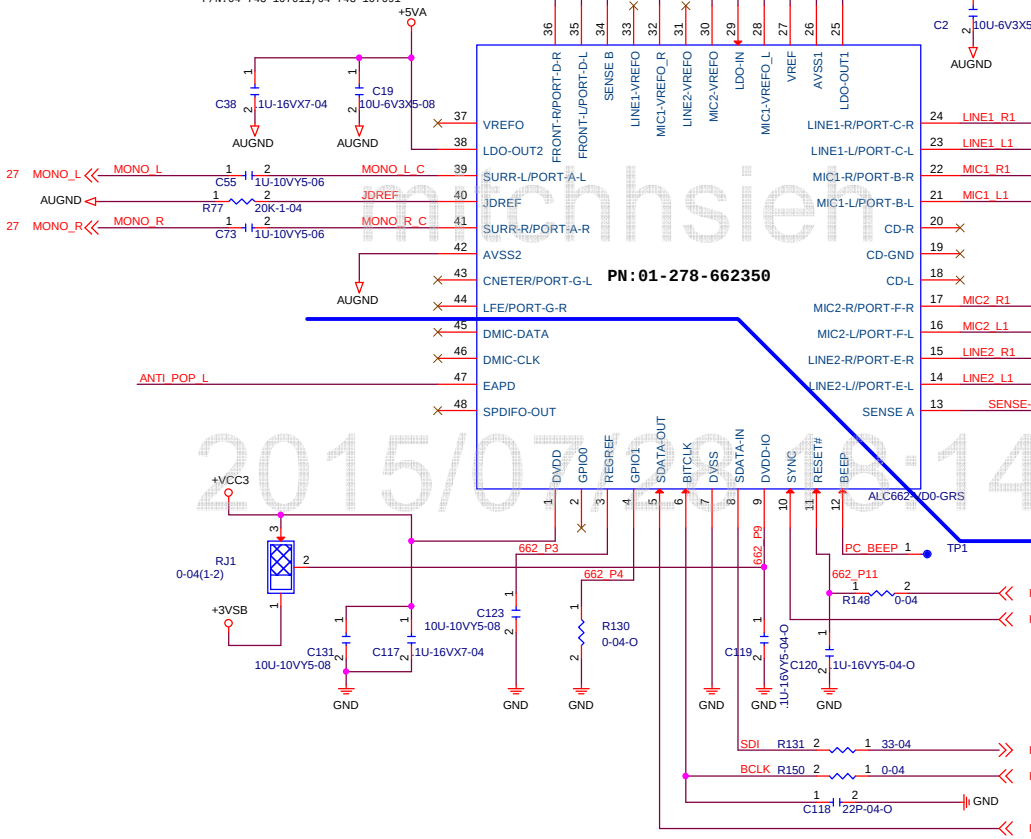


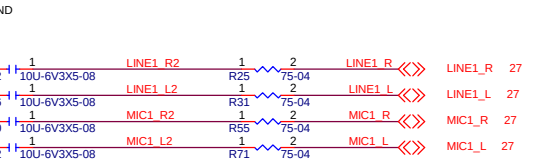


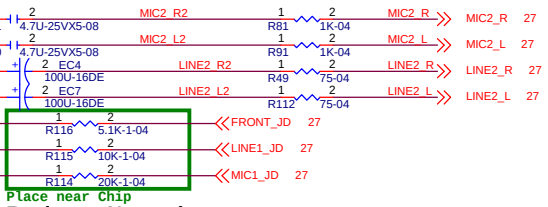


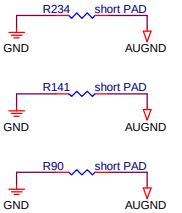




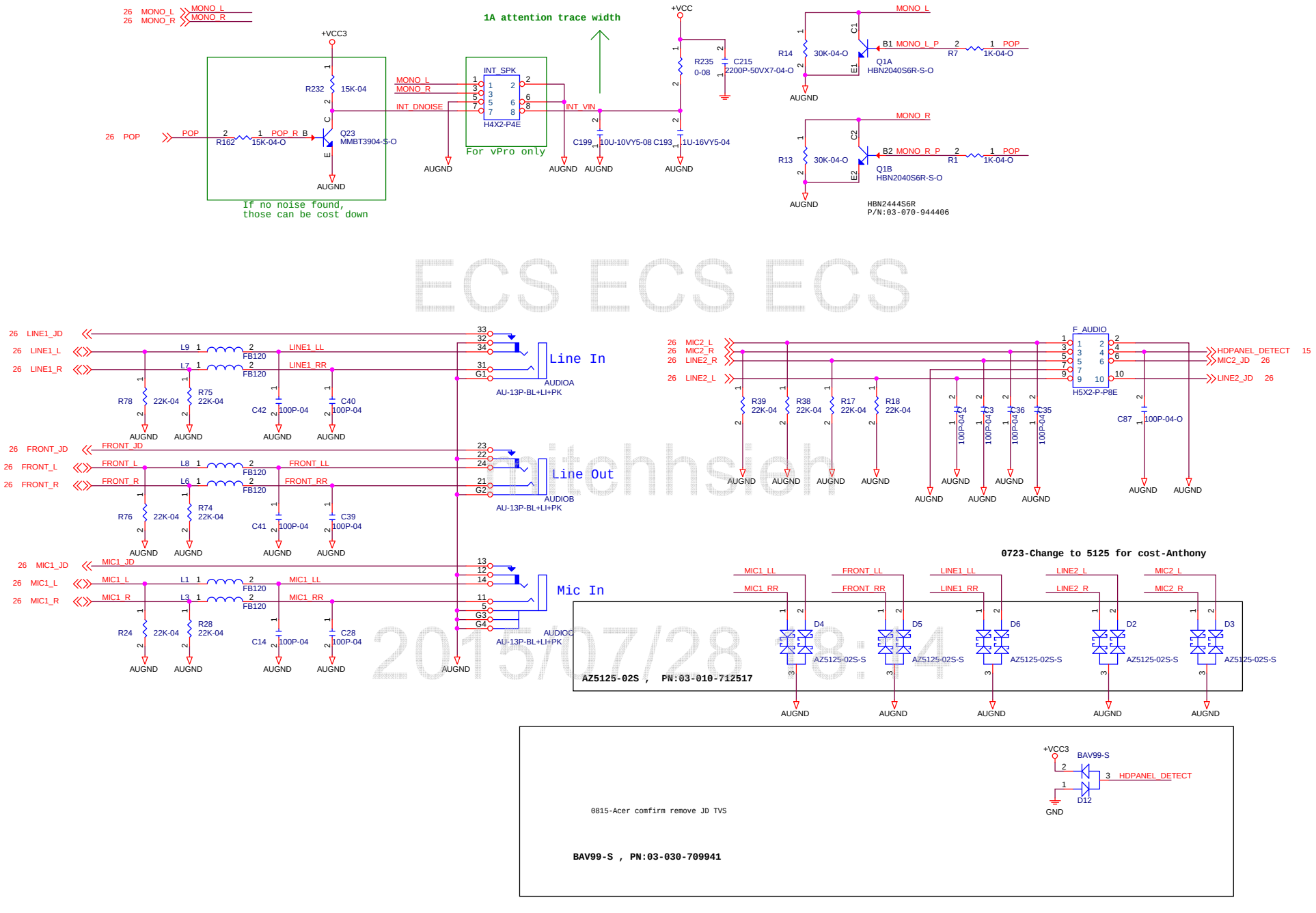




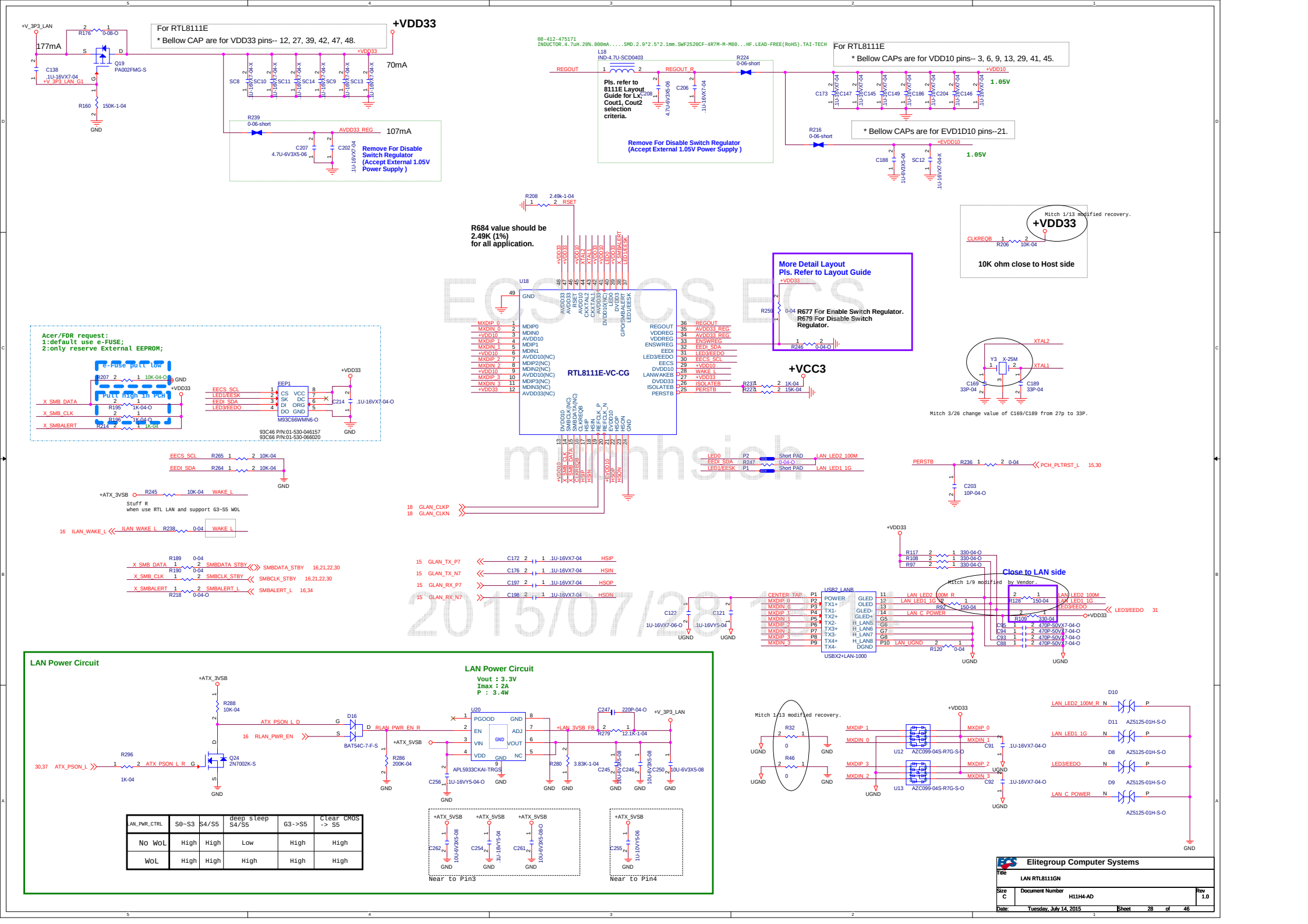




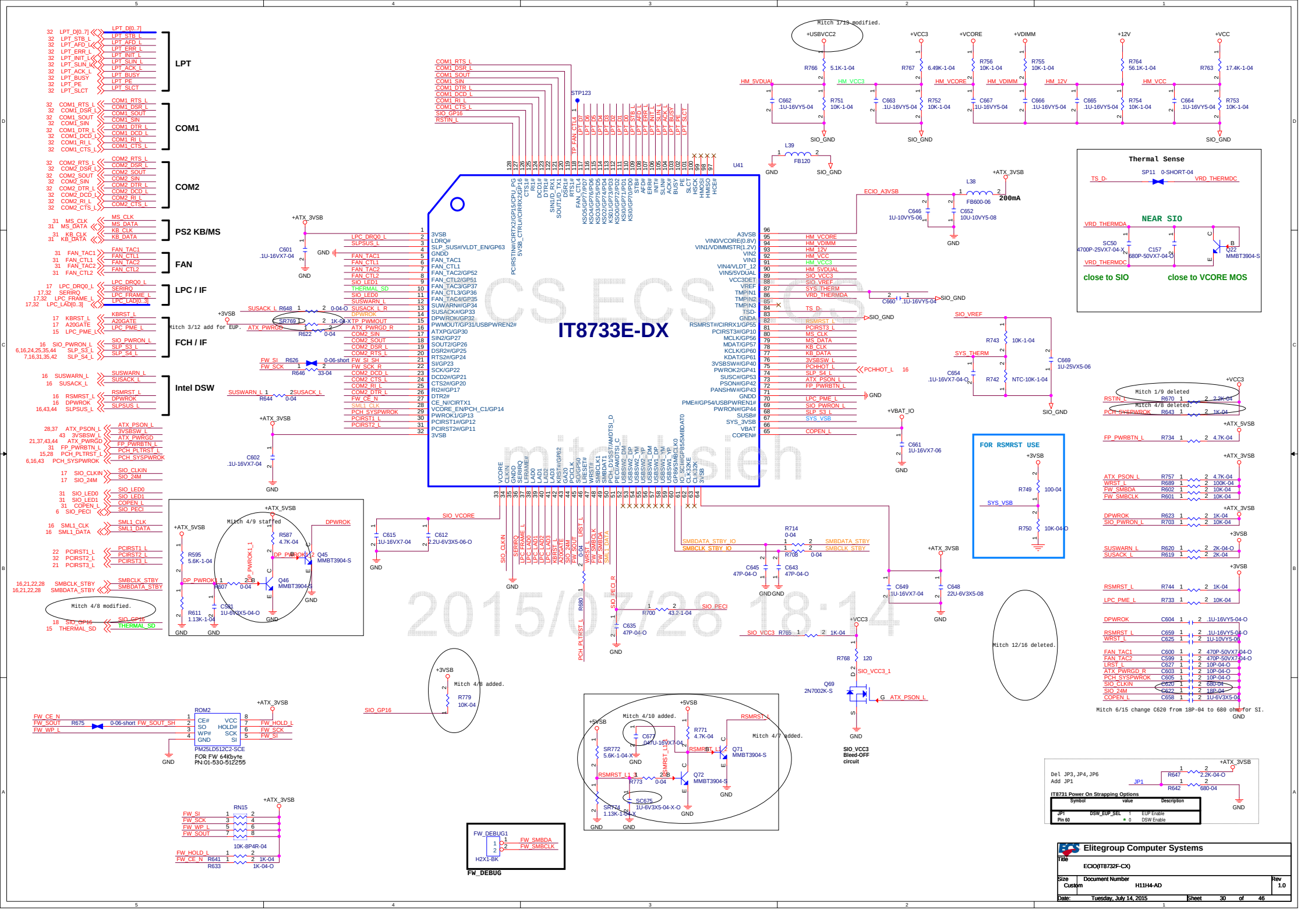
Elitegroup Computer Systems		
Title: Audio ALC662-VD		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 26 of 46	

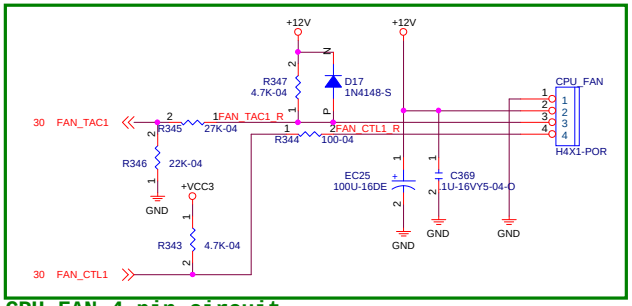


Elitegroup Computer Systems			
Title: Audio Jack/Header			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 27 of 46		

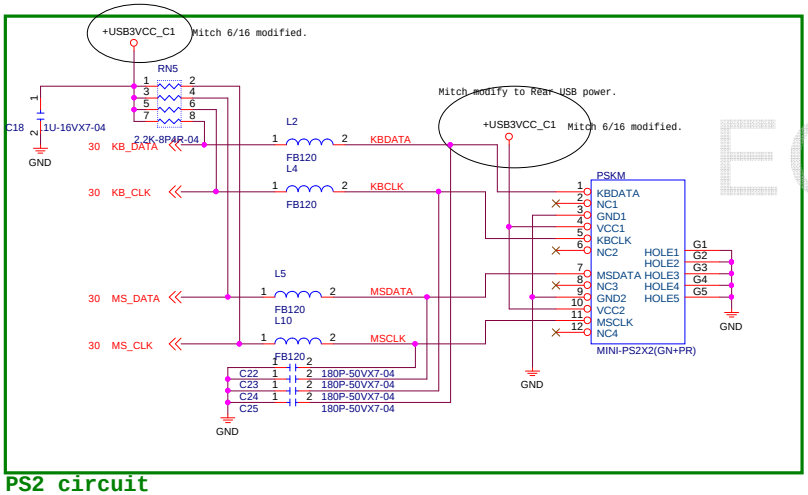

+V_3P3_LAN
177mA
R176 0-08-O
Q19 PA002FMG-S
C138 .1U-16VX7-04
+V_3P3_LAN_G1
R160 150K-1-04
GND
For RTL8111E
* Bellow CAP are for VDD33 pins-- 12, 27, 39, 42, 47, 48.
+VDD33
70mA
SC8 SC10 SC11 SC14 SC9 SC13
1U-16VX7-04-X
R239 0-06-short
AVDD33_REG
107mA
C207 4.7U-6V3X5-06
C202 .1U-16VX7-04
Remove For Disable Switch Regulator (Accept External 1.05V Power Supply)
08-412-475171
INDUCTOR.4.7uH.20%.800mA.....SMD.2.9*2.5*2.1mm.SWF2520CF-4R7M-M-M80...HF.LEAD-FREE(RoHS).TAI-TECH
L18 IND-4.7U-SCD0403
REGOUT
REGOUT_R
R224 0-06-short
Pls. refer to 8111E Layout Guide for LX: Cout1, Cout2 selection criteria.
C208 4.7U-6V3X5-06
C206 .1U-16VX7-04
Remove For Disable Switch Regulator (Accept External 1.05V Power Supply)
For RTL8111E
* Bellow CAPs are for VDD10 pins-- 3, 6, 9, 13, 29, 41, 45.
+VDD10
1.05V
C173 C147 C145 C149 C186 C204 C146
1U-16VX7-04
R216 0-06-short
* Bellow CAPs are for EVD1D10 pins--21.
+EVDD10
1.05V
C188 1U-6V3X5-04
SC12 .1U-16VX7-04-X
R208 2.49k-1-04 RSET
R684 value should be 2.49K (1%) for all application.
U18
RTL8111E-VC-CG
MXDIP_0 MXDIN_0 +VDD10 MXDIP_1 MXDIN_1 +VDD10 MXDIP_2 MXDIN_2 +VDD10 MXDIP_3 MXDIN_3 +VDD33
MDIP0 MDIN0 AVDD10 MDIP1 MDIN1 AVDD10(NC) MDIP2(NC) MDIN2(NC) AVDD10(NC) MDIP3(NC) MDIN3(NC) AVDD33(NC)
REGOUT VDDREG ENSWREG EEDI LED3/EEDO EECS DVDD10 LANWAKEB DVDD33 ISOLATEB PERSTB
AVDD33_REG ENSWREG EEDI_SDA LED3/EEDO_ EECS_SCL +VDD10 WAKE_L +VDD33 ISOLATEB PERSTB
More Detail Layout
Pls. Refer to Layout Guide
R259 0-04
R677 For Enable Switch Regulator.
R679 For Disable Switch Regulator.
R246 0-04-O
+VCC3
R237 1K-04
R227 15K-04
Mitch 1/13 modified recovery.
+VDD33
CLKREQB R206 10K-04
10K ohm close to Host side
Y3 X-25M
XTAL2 XTAL1
C169 33P-04
C189 33P-04
Mitch 3/26 change value of C169/C189 from 27p to 33P.
Acer/FDR request:
1:default use e-FUSE;
2:only reserve External EEPROM;
e-Fuse pull low
Pull High in PCH
R207 10K-04-O
X_SMB_DATA R195 1K-04-O
X_SMB_CLK R196 1K-04-O
X_SMBALERT R214 1K-04
EEP1
EECS_SCL LED1/EESK EEDI_SDA LED3/EEDO
CS SK DI DO VCC DC ORG GND
M93C66WMN6-O
C214 .1U-16VX7-04-O
93C46 P/N:01-530-046157
93C66 P/N:01-530-066020
EECS_SCL R265 10K-04
EEDI_SDA R264 10K-04
+ATX_3VSB R245 10K-04 WAKE_L
Stuff R
when use RTL LAN and support G3~S5 WOL
16 ILAN_WAKE_L R238 0-04 WAKE_L
18 GLAN_CLKP
18 GLAN_CLKN
LED0 P2 Short PAD LAN_LED2_100M
EEDI_SDA R247 0-04-O
LED1/EESK P1 Short PAD LAN_LED1_1G
PERSTB R236 0-04 PCH_PLTRST_L 15,30
C203 10P-04-O
R189 0-04
X_SMB_DATA R190 0-04 SMBDATA_STBY SMBDATA_STBY 16,21,22,30
X_SMB_CLK SMBCLK_STBY SMBCLK_STBY 16,21,22,30
X_SMBALERT R218 0-04-O SMBALERT_L SMBALERT_L 16,34
15 GLAN_TX_P7 C172 .1U-16VX7-04 HSIP
15 GLAN_TX_N7 C176 .1U-16VX7-04 HSIN
15 GLAN_RX_P7 C197 .1U-16VX7-04 HSOP
15 GLAN_RX_N7 C198 .1U-16VX7-04 HSON
C122 1U-16VX7-06-O
C121 .1U-16VY5-04
UGND
+VDD33
R117 R108 R97 330-04-O
Close to LAN side
Mitch 1/9 modified by Vendor.
CENTER_TAP MXDIP_0 MXDIN_0 MXDIP_1 MXDIN_1 MXDIP_2 MXDIN_2 MXDIP_3 MXDIN_3
USB2_LANB
POWER TX1+ TX1- TX2+ TX2- TX3+ TX3- TX4+ TX4- DGND
GLED OLED GLED- GLED+ H_LAN5 H_LAN6 H_LAN7 H_LAN8
LAN_LED2_100M_R LAN_LED1_1G LAN_C_POWER
R92 150-04
R128 150-04
R109 330-04
LAN_LED2_100M LAN_LED1_1G LED3/EEDO
LED3/EEDO 31
C95 C94 C93 C88 470P-50VX7-04-O
R120 0-04
USBX2+LAN-1000
LAN Power Circuit
+ATX_3VSB
R288 10K-04
ATX_PSON_L_D
16 RLAN_PWR_EN
D16 BAT54C-7-F-S
RLAN_PWR_EN_R
R296 1K-04
30,37 ATX_PSON_L
ATX_PSON_L_R
Q24 2N7002K-S
+ATX_5VSB
R286 200K-04
LAN Power Circuit
Vout : 3.3V
Imax : 2A
P : 3.4W
U20 APL5933CKAI-TRGS
PGOOD EN VIN VDD GND ADJ VOUT NC
+LAN_3VSB_FB
R279 12.1K-1-04
R280 3.83K-1-04
C247 220P-04-O
+V_3P3_LAN
C256 1U-16VY5-04
C245 C246 10U-6V3X5-08
C250 10U-6V3X5-08
Near to Pin3
C262 C254 C261 10U-6V3X5-08
C255 1U-16VY5-06
Near to Pin4
Mitch 1/13 modified recovery.
R32 R46
U12 U13 AZC099-04S-R7G-S-O
MXDIP_1 MXDIN_0 MXDIP_3 MXDIN_2
MXDIP_0 MXDIN_1 MXDIP_2 MXDIN_3
C91 C92 .1U-16VX7-04-O
D10 D11 D8 D9 AZ5125-01H-S-O
LAN_LED2_100M_R
LAN_LED1_1G
LED3/EEDO
LAN_C_POWER
LAN_PWR_CTRL | S0~S3 | S4/S5 | deep sleep S4/S5 | G3->S5 | Clear CMOS -> S5
No WoL | High | High | Low | High | High
WoL | High | High | High | High | High
Elitegroup Computer Systems
Title: LAN RTL8111GN
Size: C
Document Number: H11H4-AD
Rev: 1.0
Date: Tuesday, July 14, 2015
Sheet 28 of 46

Elitegroup Computer Systems		
Title: LAN I219LM		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 29 of 46	

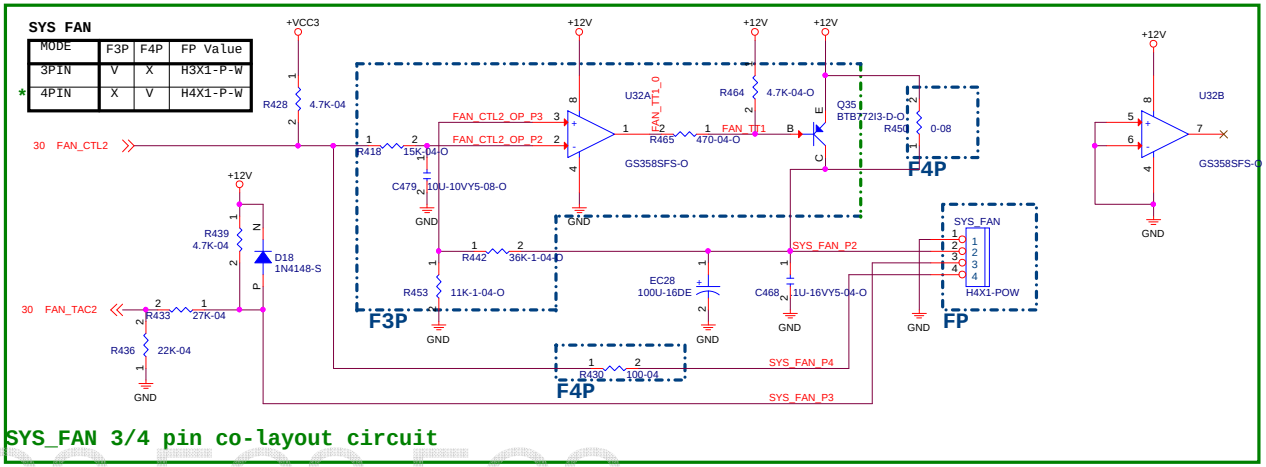

IT8733E-DX
LPT
COM1
COM2
PS2 KB/MS
FAN
LPC / IF
FCH / IF
Intel DSW
NEAR SIO
close to SIO
close to VCORE MOS
FOR RSMRST USE
Thermal Sense
SIO_VCC3 Bleed-OFF circuit
FW_DEBUG
Mitch 1/19 modified.
Mitch 4/8 added.
Mitch 4/9 staffed
Mitch 4/10 added.
Mitch 4/7 added.
Mitch 4/8 modified.
Mitch 12/16 deleted.
Mitch 1/9 deleted
Mitch 4/8 deleted
Mitch 6/15 change C620 from 18P-04 to 680 ohm for SI.
Mitch 3/12 add for EUP.
IT8731 Power On Strapping Options
Elitegroup Computer Systems
ECIO(IT8732F-CX)
H11H4-AD
Tuesday, July 14, 2015



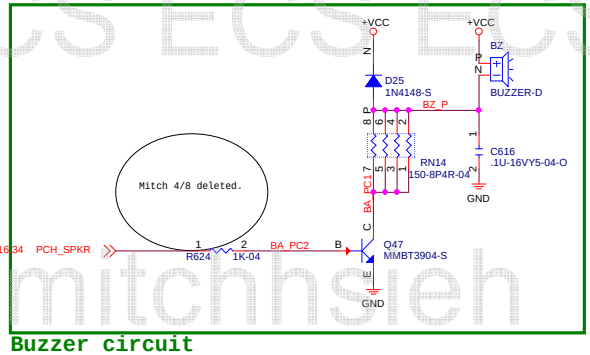
CPU_FAN 4 pin circuit



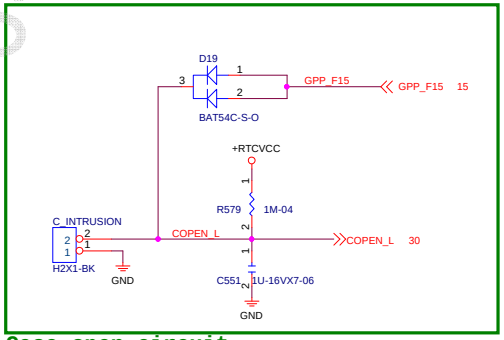
PS2 circuit



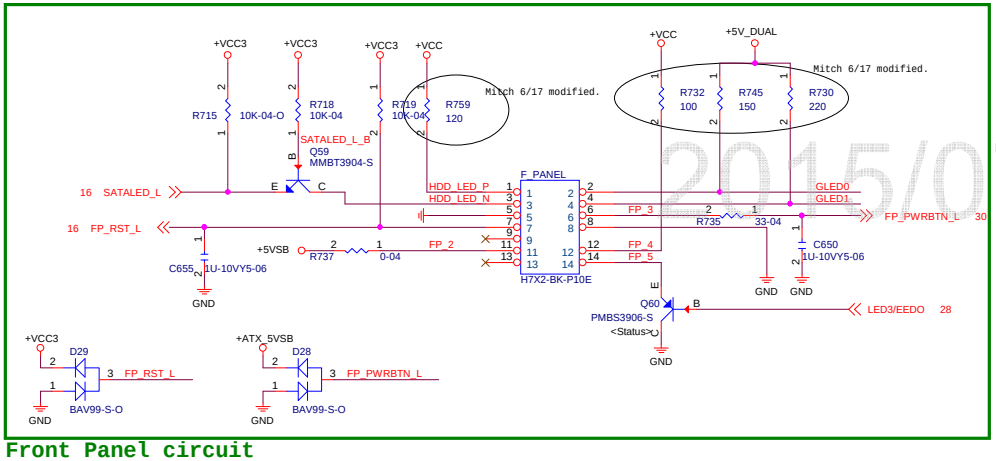
SYS_FAN 3/4 pin co-layout circuit



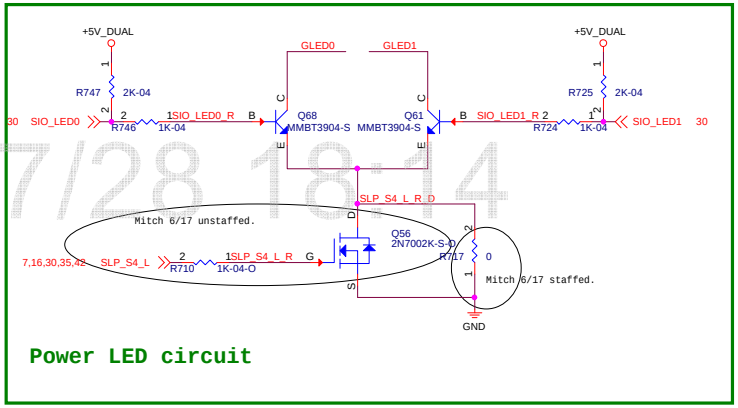
Buzzer circuit



Case open circuit

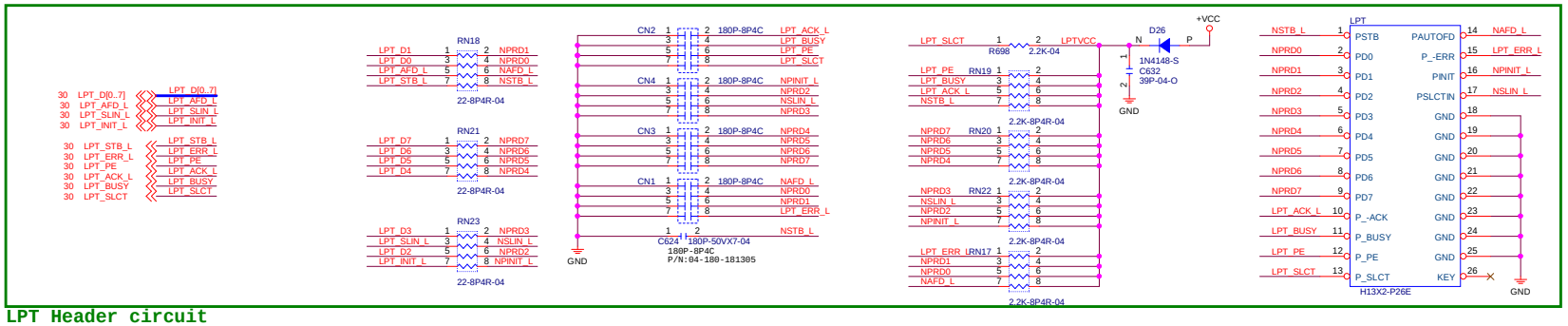


Front Panel circuit

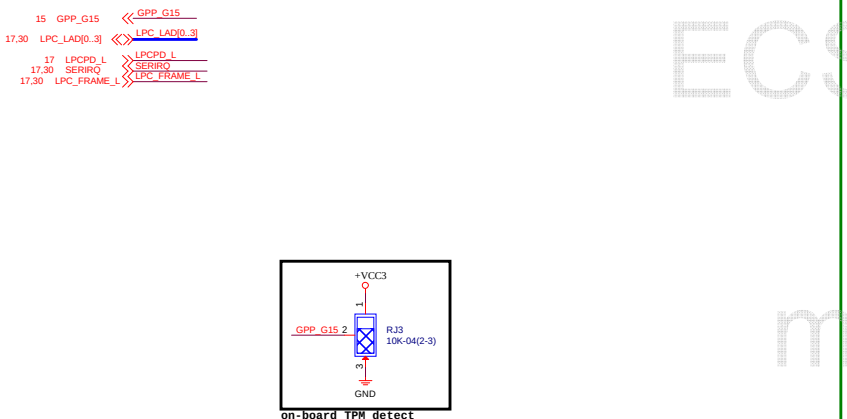


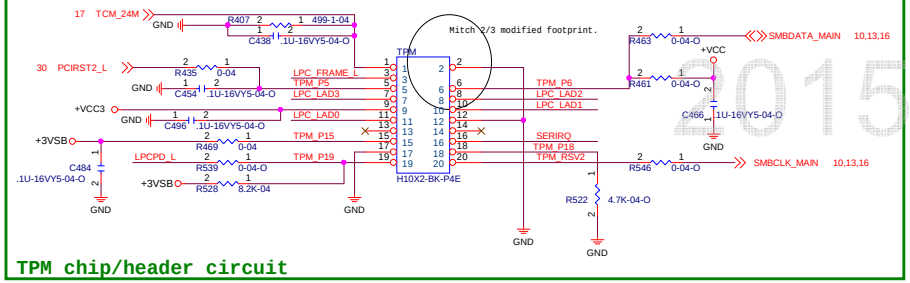
Power LED circuit

ECS	Elitegroup Computer Systems	
Title	FAN/Buzzer/PS2/Front Panel	
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 31 of 46	

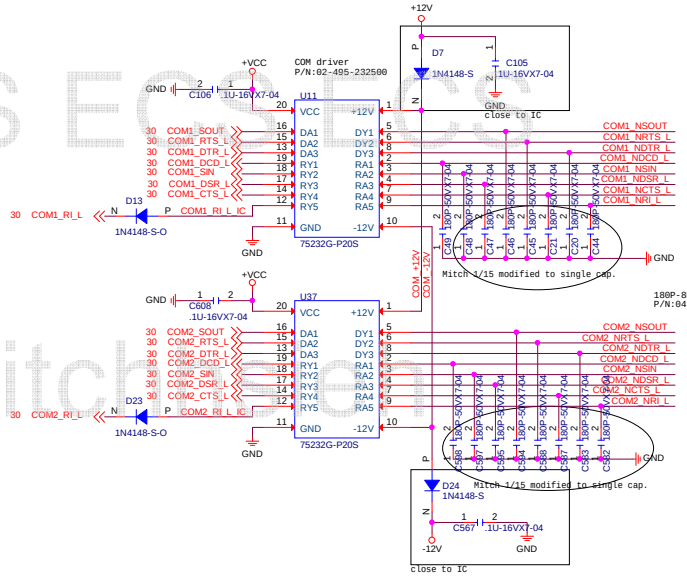


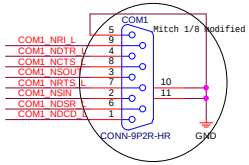
LPT Header circuit

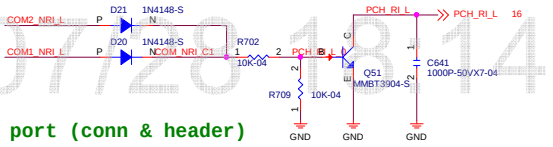




TPM chip/header circuit

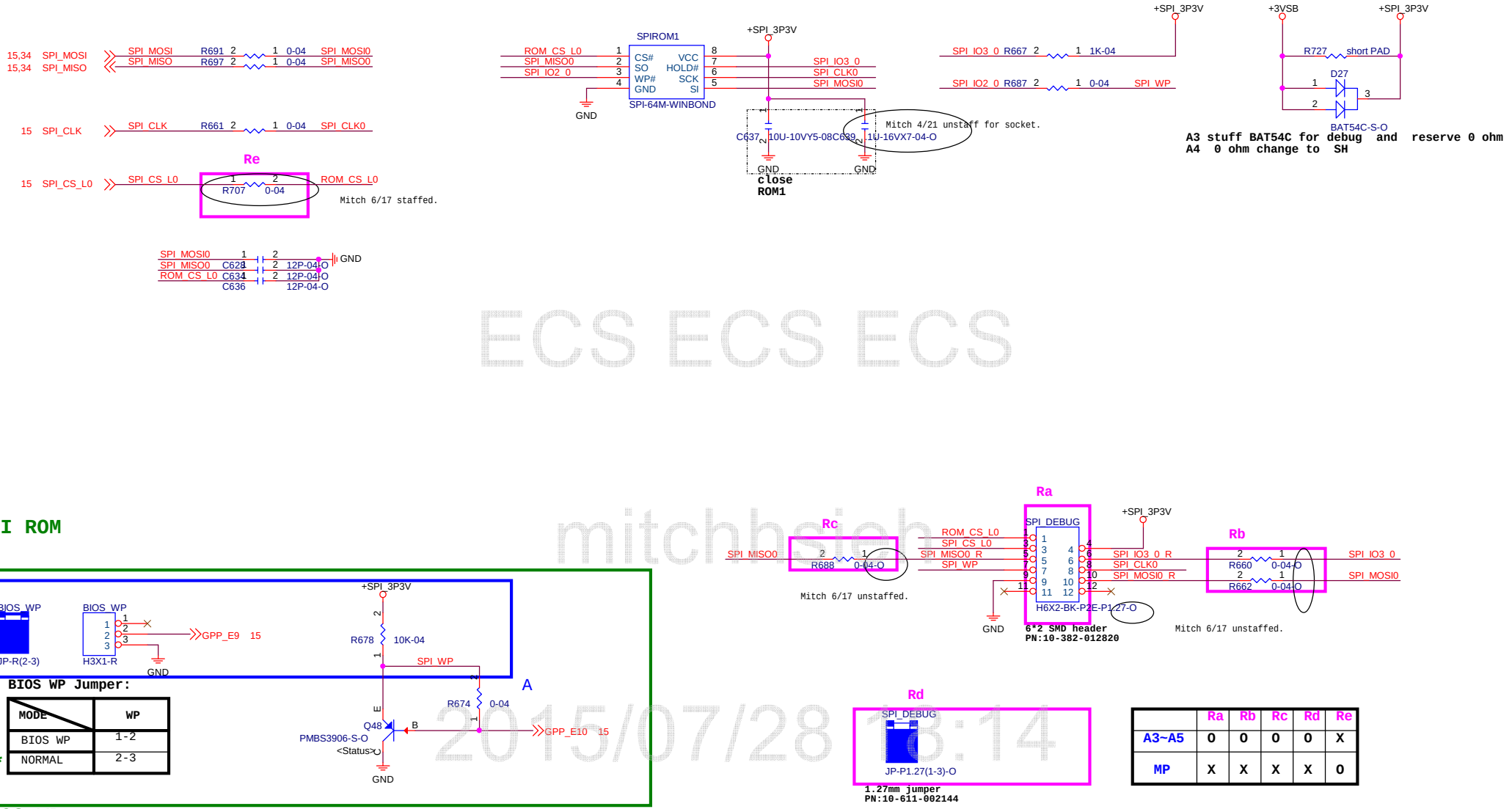






COM port (conn & header)

Elitegroup Computer Systems			
Title: TPM/TCM/LPT/COM/Asset ID			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 32 of 46		

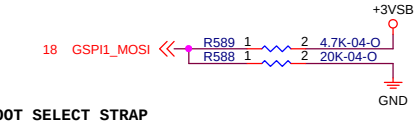


SPI ROM

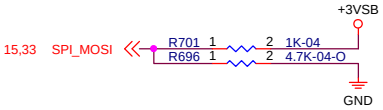
BIOS WP

	Ra	Rb	Rc	Rd	Re
A3~A5	0	0	0	0	X
MP	X	X	X	X	0

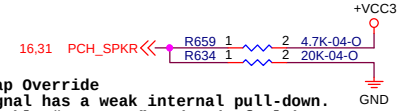
Title: SPI ROM			
Size: B	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 33 of 46		



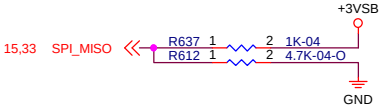
BOOT SELECT STRAP
IF SAMPLED HIGH, LPC IS SELECTED ELSE SPI
PCH HAS INTERNAL WEAK PD



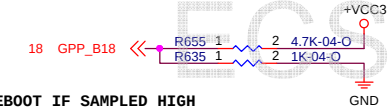
BOOT HALT ENABLED IF LOW
PCH HAS INTERNAL WEAK PU



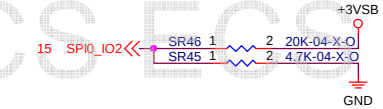
Top Swap Override
The signal has a weak internal pull-down.
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.



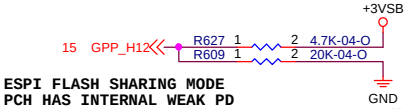
JTAG ODT IS DISABLED IF LOW
PCH HAS INTERNAL WEAK PU



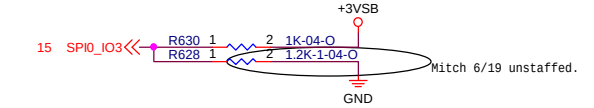
NO REBOOT IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD



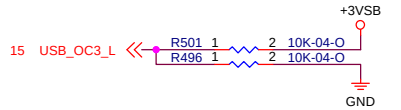
CONSENT STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU



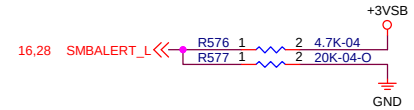
ESPI FLASH SHARING MODE
PCH HAS INTERNAL WEAK PD
0: MASTER ATTACHED FLASH SHARING
1:SLAVE ATTACEHD FLASH SHARING



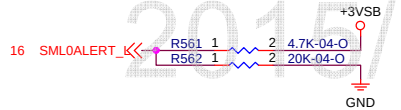
PESONALITY STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU
(P.S. Pull down for pre ES1/ES1 only)



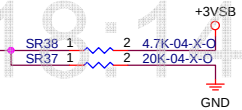
DFX TEST MODE
XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL



TLS CONFIDENTIALITY ENABLED
IF SAMPLED HIGH(DEFAULT)
PCH HAS INTERNAL WEAK PD

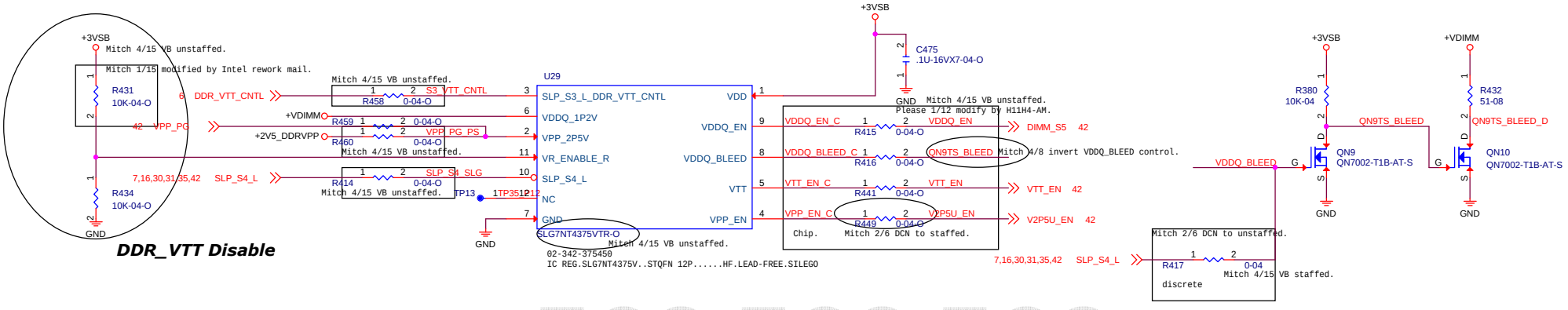


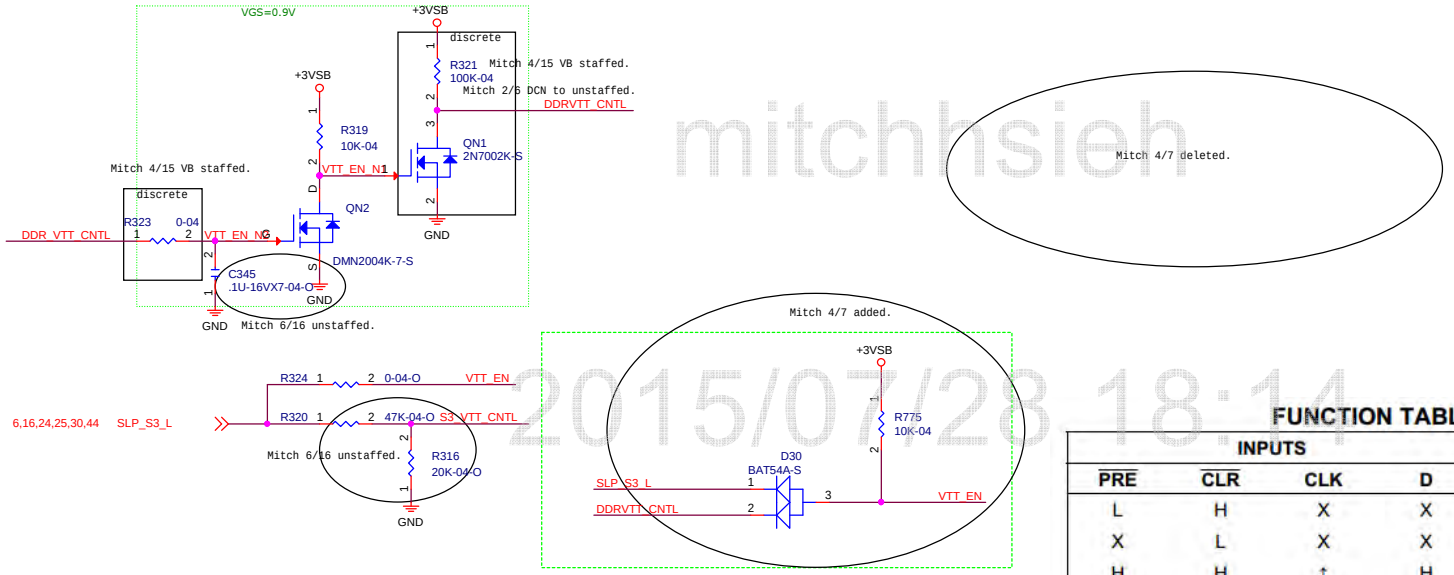
ESPI/LPC SELECT STRAP
IF SAMPLED HIGH, ESPI IS SELECTED ELSE LPC
PCH HAS INTERNAL WEAK PD



EXI BOOT STALL BYPASS IS ENABLED IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD

Title: Strap Pin		
Size: B	Document Number: H11H4-AD	Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 34 of 46	

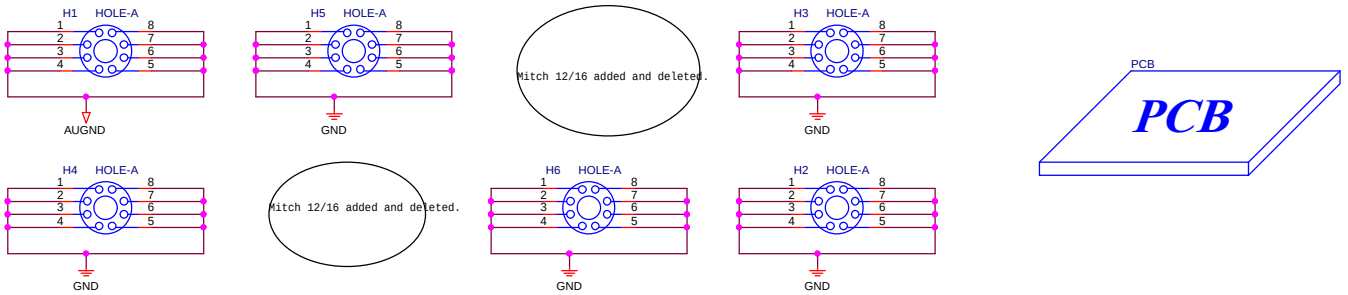




FUNCTION TABLE

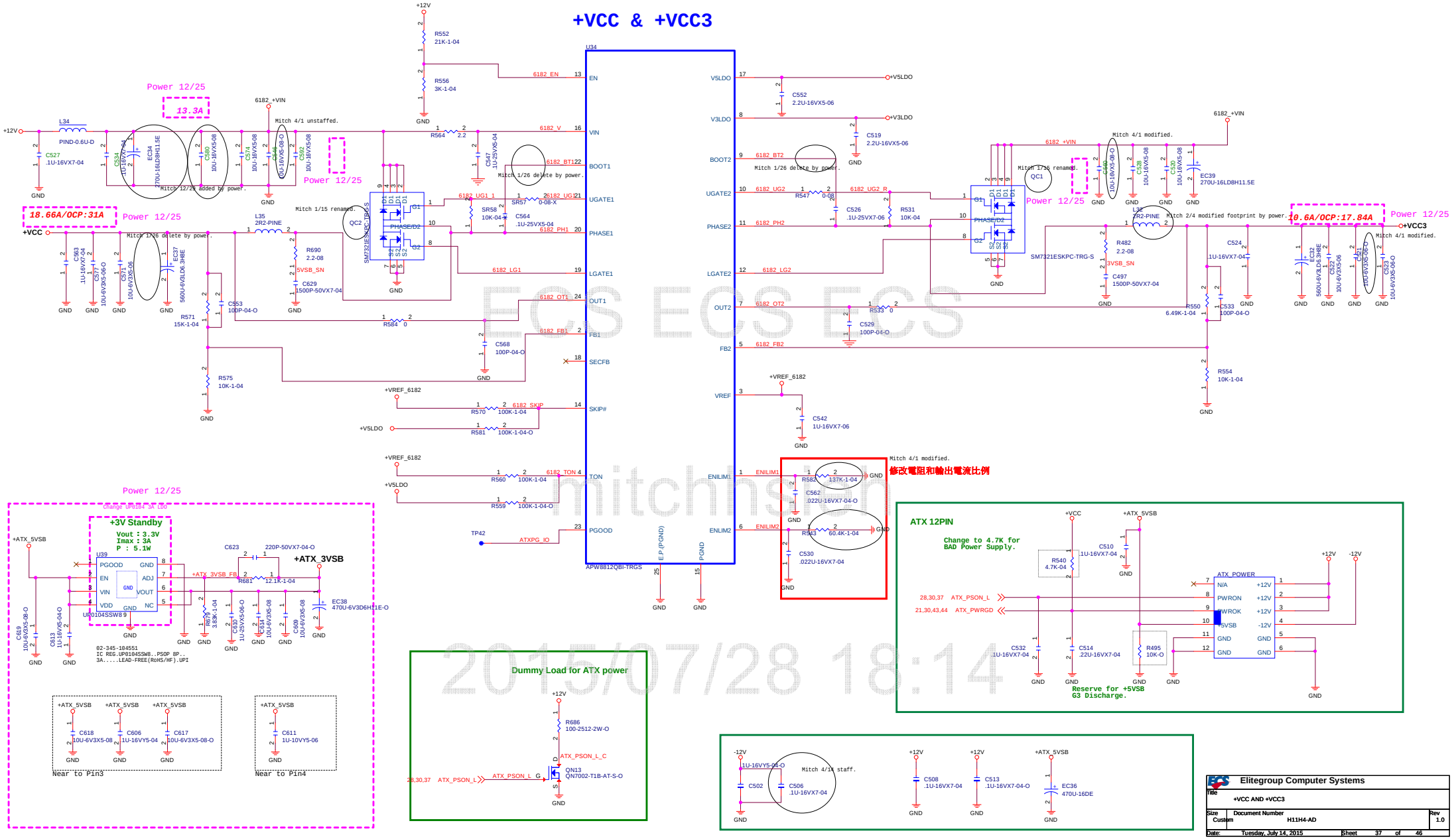
INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
X	L	X	X	L	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

Title: DP SWITCH			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 35 of 46		

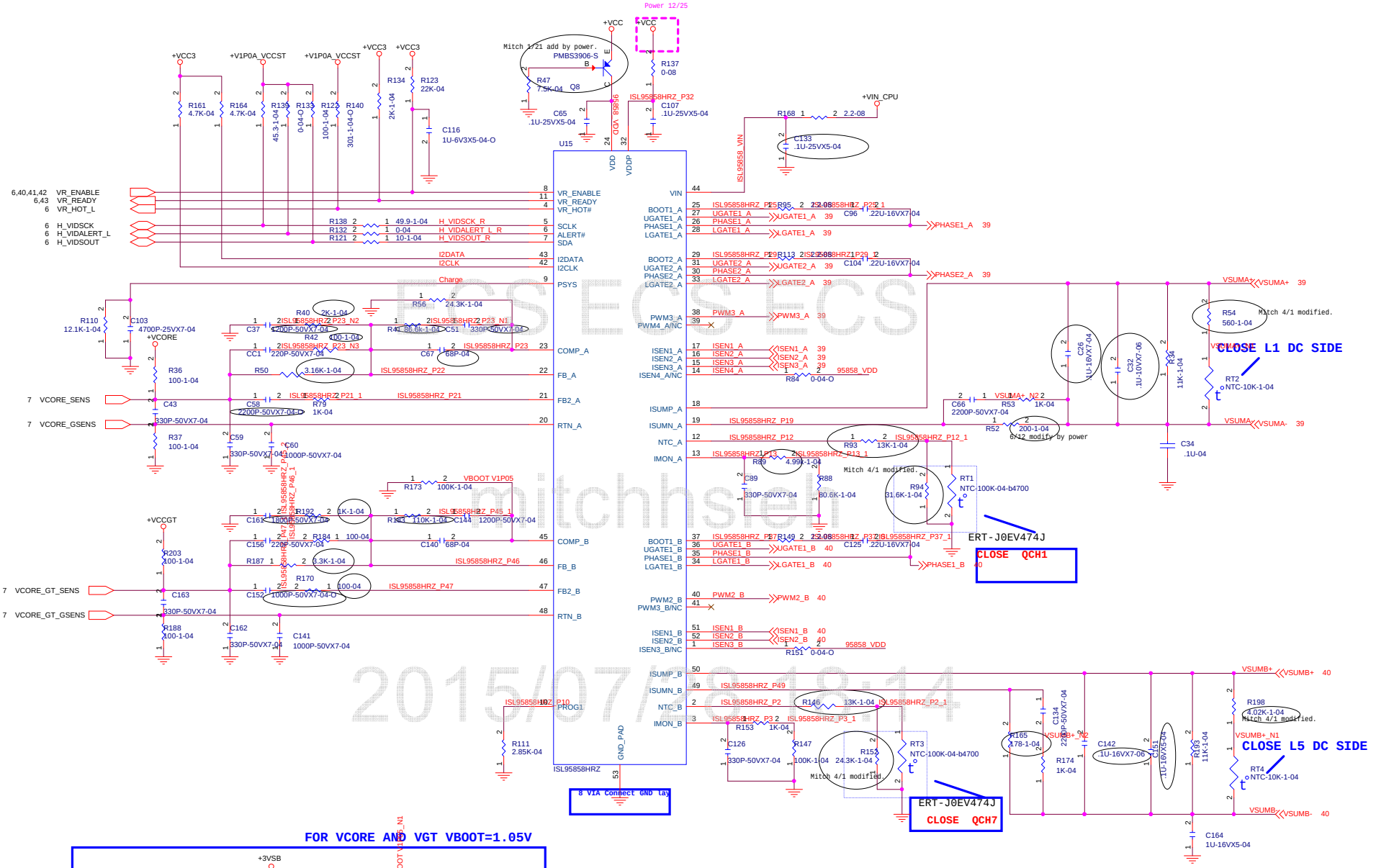


Elitegroup Computer Systems		
Title: XDP		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 36 of 46	

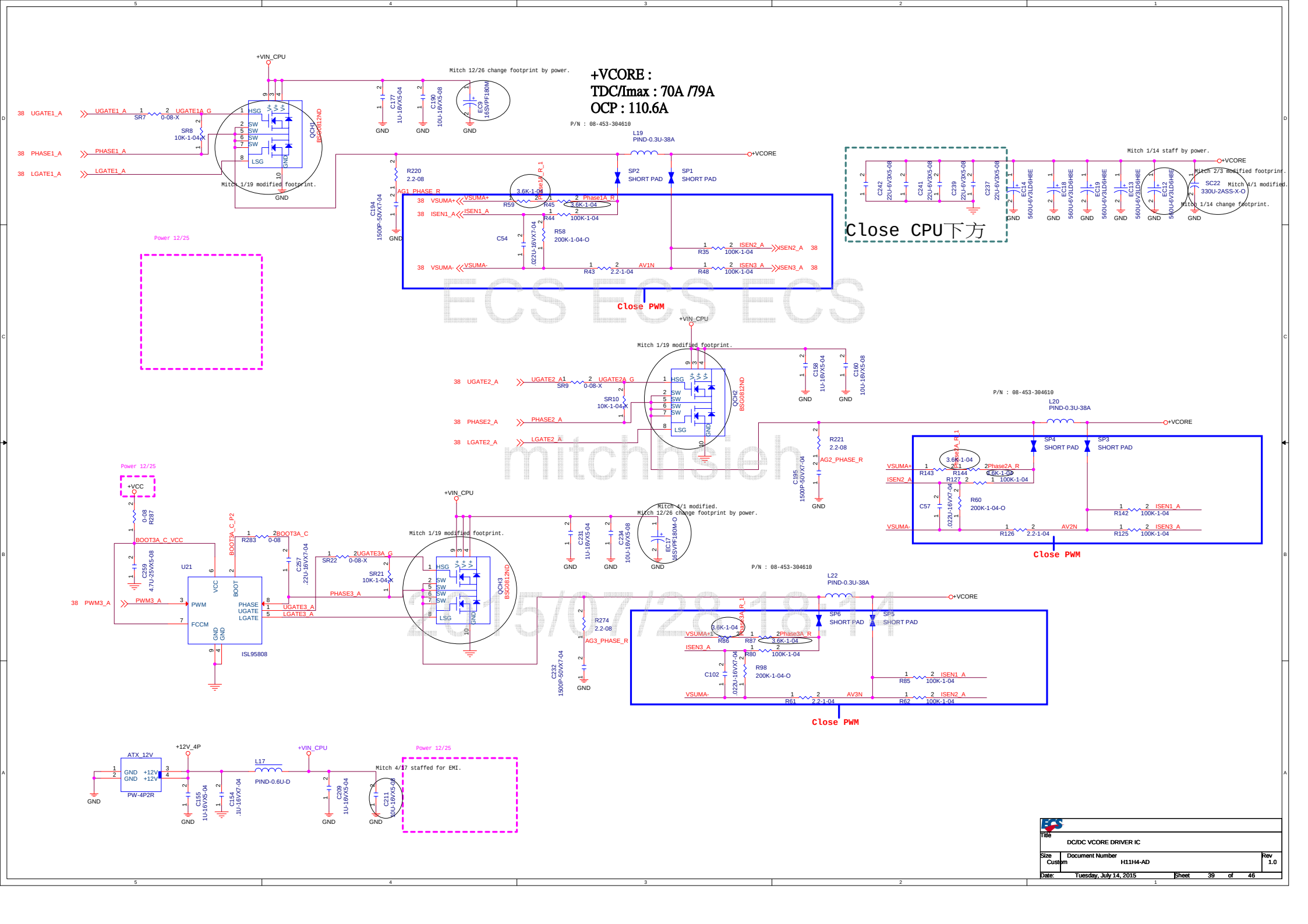
+VCC & +VCC3

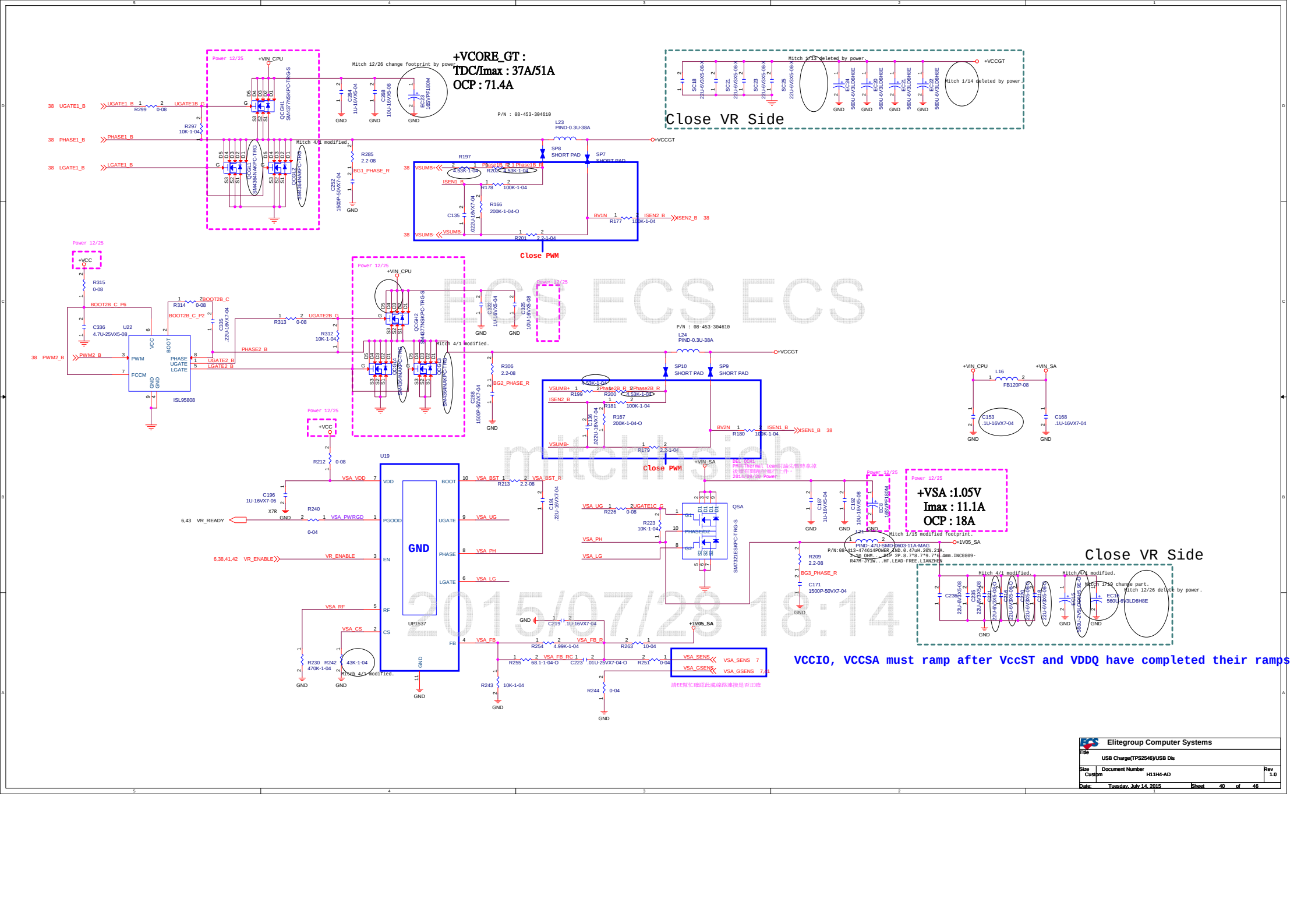


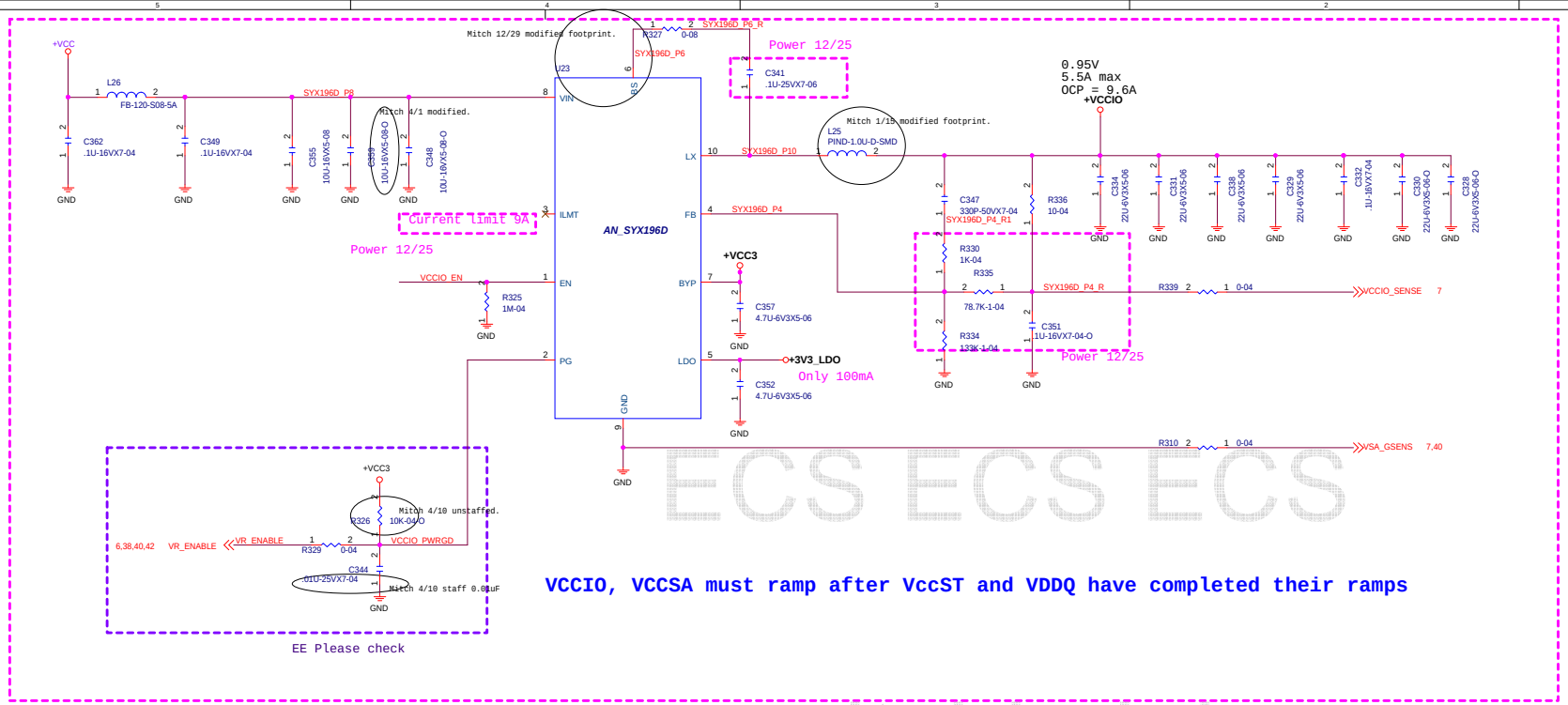
Elitegroup Computer Systems			
Title: +VCC AND +VCC3			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 37 of 46		



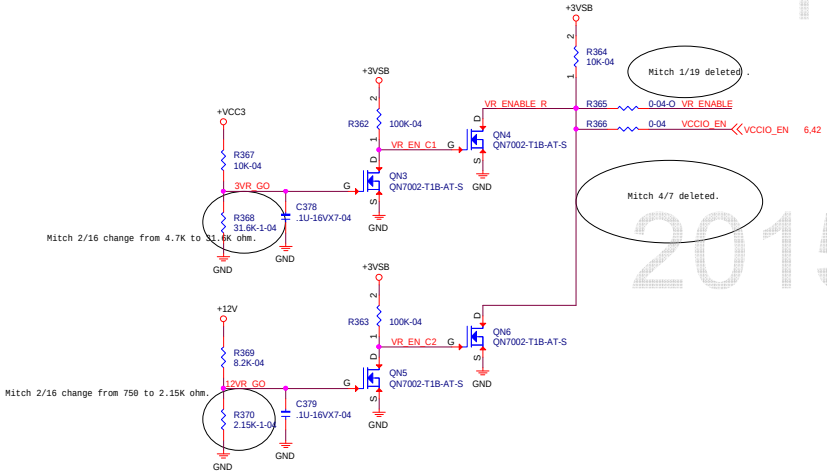
ECS	Elitegroup Computer Systems		
Title	DC/DC VCORE PWM IC		
Size	Document Number		Rev
Custom	H11H4-AD		1.0
Date:	Tuesday, July 14, 2015	Sheet 38 of 46	


+VCORE :
TDC/Imax : 70A /79A
OCP : 110.6A
Close CPU下方
Close PWM
Close PWM
Close PWM
Power 12/25
Power 12/25
Power 12/25
Mitch 12/26 change footprint by power.
Mitch 1/19 modified footprint.
Mitch 1/14 staff by power.
Mitch 2/3 modified footprint.
Mitch 1/14 change footprint.
Mitch 4/1 modified.
Mitch 4/17 staffed for EMI.
P/N : 08-453-304610
L19 PIND-0.3U-38A
L20 PIND-0.3U-38A
L22 PIND-0.3U-38A
L17 PIND-0.6U-D
+VIN_CPU
+VCORE
+VCC
+12V_4P
ATX_12V
PW-4P2R
ISL95808
U21
QCH1 BSC0812ND
QCH2 BSG0812ND
QCH3 BSG0812ND
SP1 SHORT PAD
SP2 SHORT PAD
SP3 SHORT PAD
SP4 SHORT PAD
SP5 SHORT PAD
SP6 SHORT PAD
SC22 330U-2ASS-X-O
ECS
DC/DC VCORE DRIVER IC
Size Custom
Document Number H11H4-AD
Rev 1.0
Date: Tuesday, July 14, 2015
Sheet 39 of 46


+VCORE_GT :
TDC/Imax : 37A/51A
OCP : 71.4A
Close VR Side
Close PWM
Close PWM
Close VR Side
+VSA :1.05V
Imax : 11.1A
OCP : 18A
ISL95808
UP1537
SM7321ESPC-TRG-S
VCCIO, VCCSA must ramp after VccST and VDDQ have completed their ramps
Elitegroup Computer Systems
USB Charge(TPS2546)/USB Dis
H11H4-AD
Tuesday, July 14, 2015



VCCIO & VR ENABLE

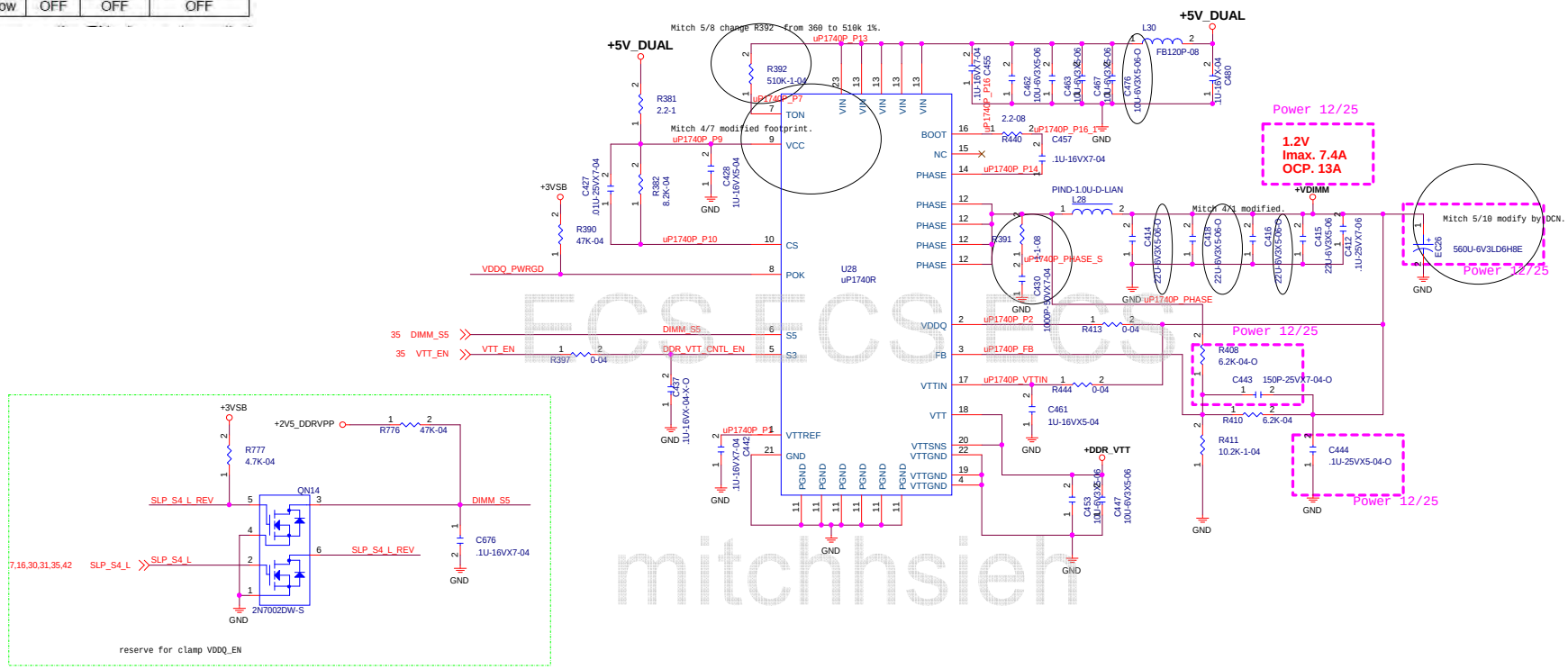


Title	DC/DC VCCIO	
Size C	Document Number H11H4-AD	Rev 1.0
Date: Tuesday, July 14, 2015	Sheet 41 of 46	

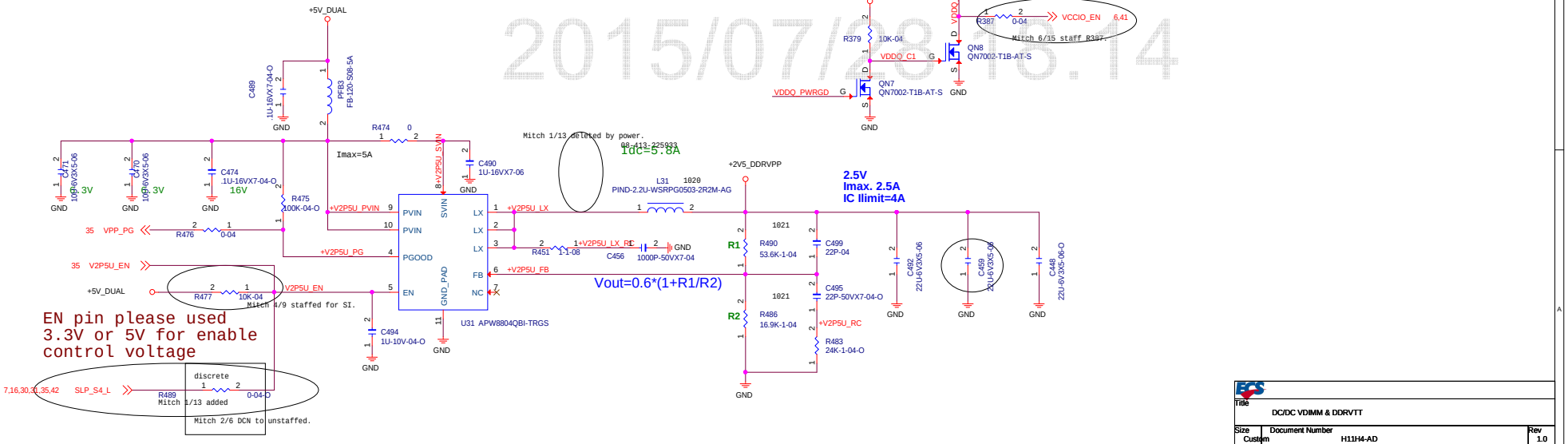
VDIMM

Table 1—EN1/EN2 Control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF

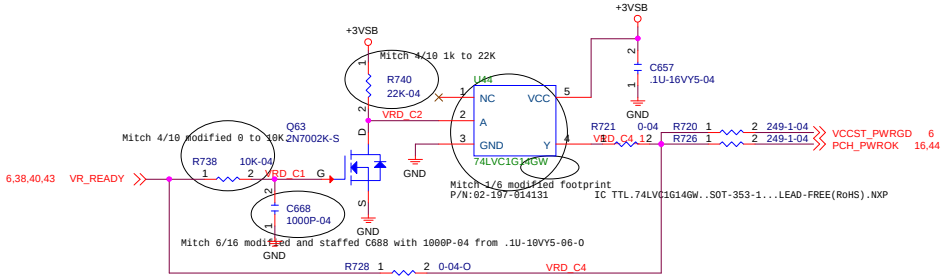


V2P5U

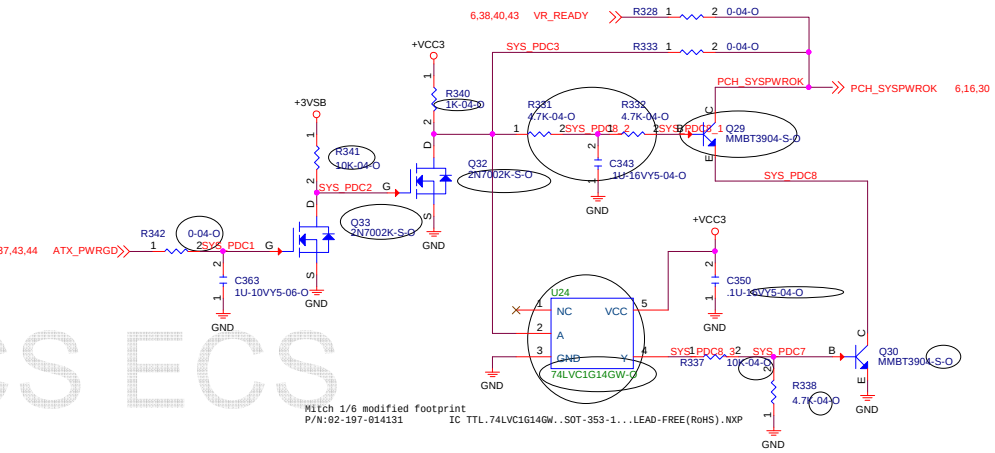


Title	DC/DC VDIMM & DDRVTT		
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 42 of 46		

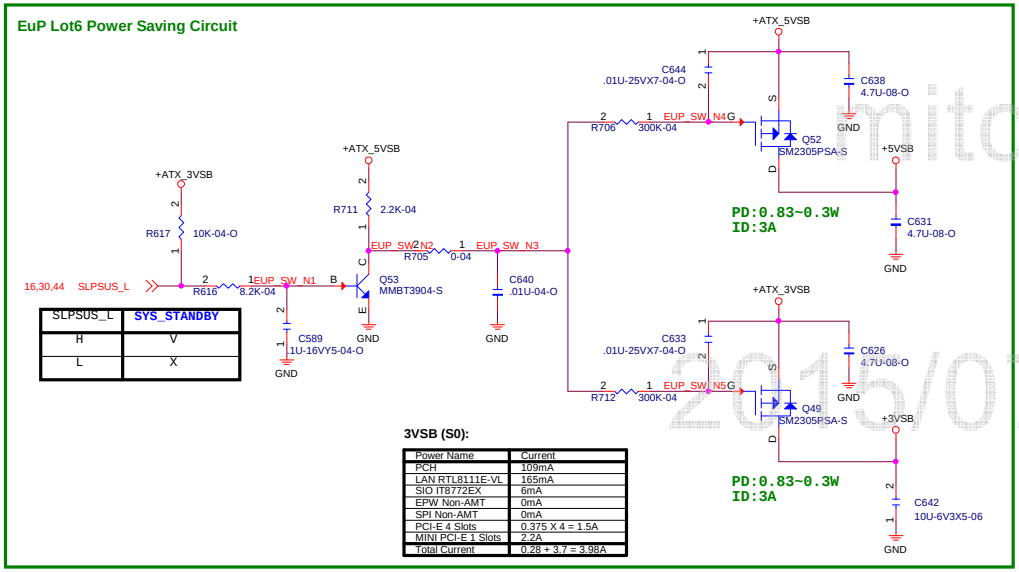
PCH & VCCST PWROK



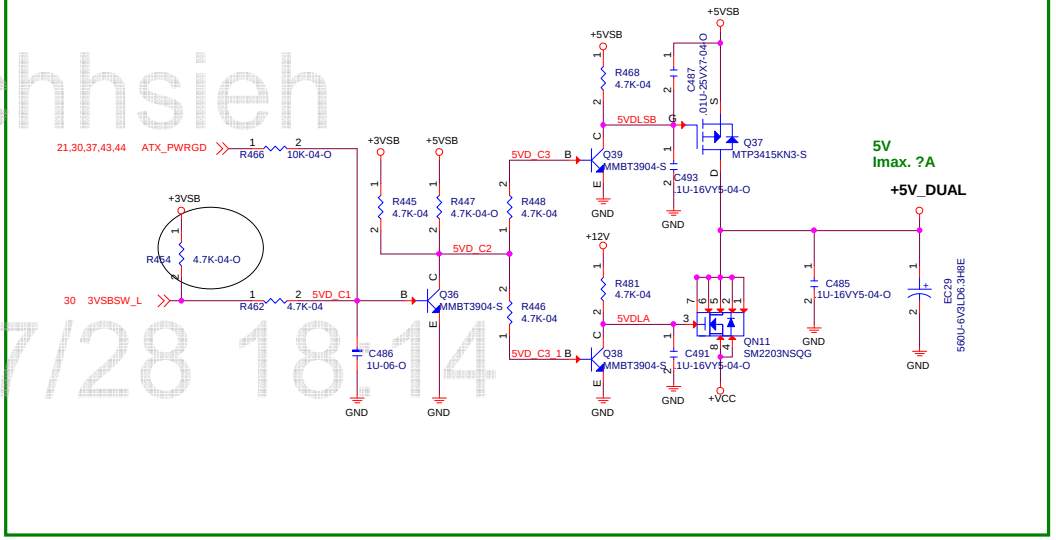
SYS_PWROK SURPRISE POWER DOWN TRIGGERED BY PWRGD_PS



EuP Lot6 Power Saving Circuit



5VDUAL

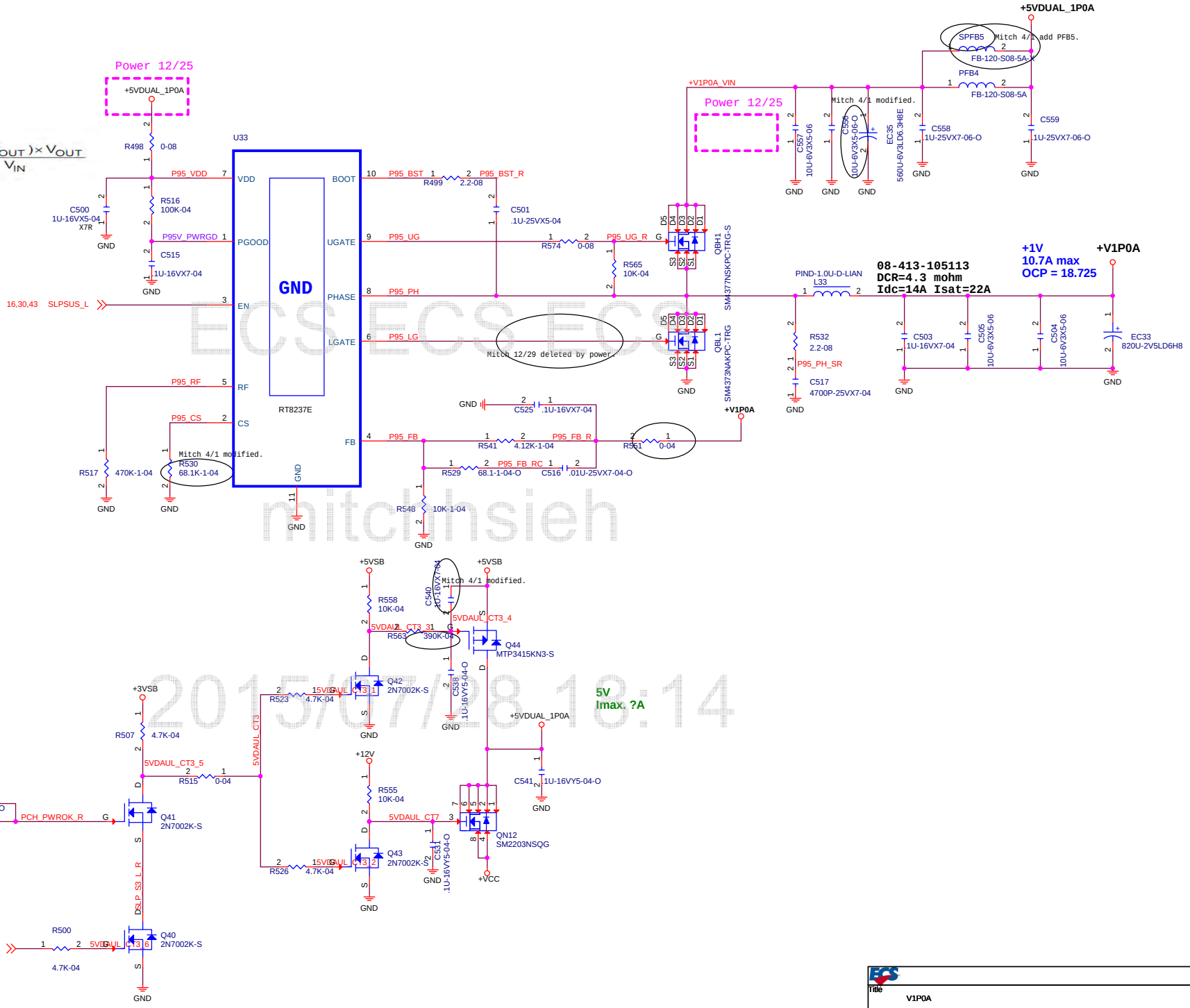


Title	DC/DC DDRVPP & 5VDUAL
Size: Custom	Document Number: H11H4-AD
Rev	1.0
Date: Tuesday, July 14, 2015	Sheet 43 of 46

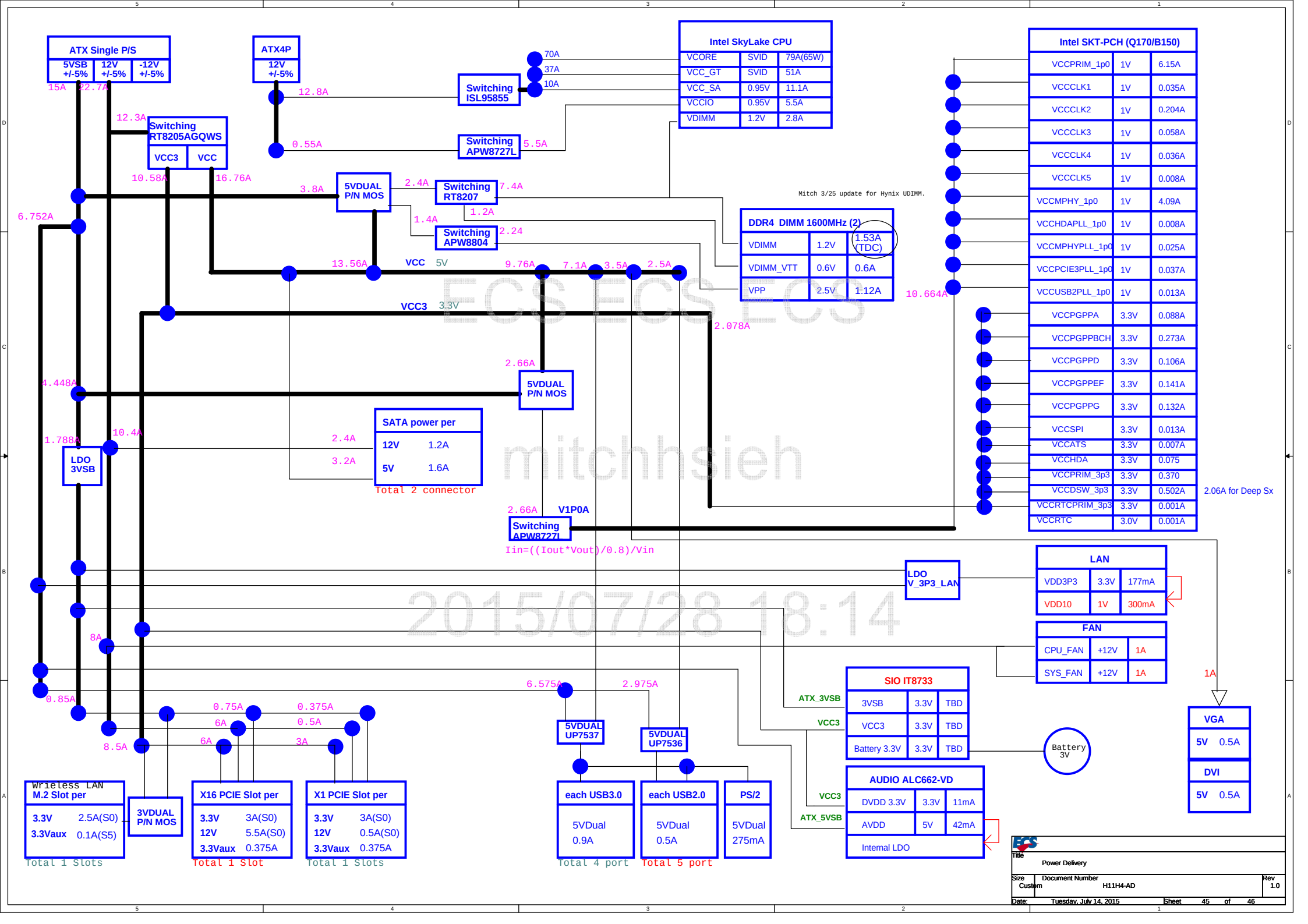
V1P0A

$$I_{LOAD\_OC} = \frac{V_{CS\_OC}}{8 \times R_{DS(ON)}} + \frac{I_{RIPPLE}}{2}$$

$$= \frac{V_{CS\_OC}}{8 \times R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$



Title	V1P0A		
Size	Document Number		Rev
Custom	H11H4-AD		1.0
Date:	Tuesday, July 14, 2015	Sheet 44 of 46	


ATX Single P/S
5VSB +/-5%
12V +/-5%
-12V +/-5%
15A
22.7A
ATX4P
12V +/-5%
12.8A
0.55A
Switching ISL95855
Switching APW8727L
5.5A
70A
37A
10A
Intel SkyLake CPU
VCORE SVID 79A(65W)
VCC_GT SVID 51A
VCC_SA 0.95V 11.1A
VCCIO 0.95V 5.5A
VDIMM 1.2V 2.8A
12.3A
Switching RT8205AGQWS
VCC3
VCC
10.58A
16.76A
3.8A
5VDUAL P/N MOS
2.4A
Switching RT8207
7.4A
1.2A
1.4A
Switching APW8804
2.24
6.752A
13.56A
VCC 5V
9.76A
7.1A
3.5A
2.5A
Mitch 3/25 update for Hynix UDIMM.
DDR4 DIMM 1600MHz (2)
VDIMM 1.2V 1.53A (TDC)
VDIMM_VTT 0.6V 0.6A
VPP 2.5V 1.12A
Intel SKT-PCH (Q170/B150)
VCCPRIM_1p0 1V 6.15A
VCCCLK1 1V 0.035A
VCCCLK2 1V 0.204A
VCCCLK3 1V 0.058A
VCCCLK4 1V 0.036A
VCCCLK5 1V 0.008A
VCCMPHY_1p0 1V 4.09A
VCCHDAPLL_1p0 1V 0.008A
VCCMPHYPLL_1p0 1V 0.025A
VCCPCIE3PLL_1p0 1V 0.037A
VCCUSB2PLL_1p0 1V 0.013A
10.664A
VCCPGPPA 3.3V 0.088A
VCCPGPPBCH 3.3V 0.273A
VCCPGPPD 3.3V 0.106A
VCCPGPPEF 3.3V 0.141A
VCCPGPPG 3.3V 0.132A
VCCSPI 3.3V 0.013A
VCCATS 3.3V 0.007A
VCCHDA 3.3V 0.075
VCCPRIM_3p3 3.3V 0.370
VCCDSW_3p3 3.3V 0.502A
VCCRTCPRIM_3p3 3.3V 0.001A
VCCRTC 3.0V 0.001A
2.06A for Deep Sx
VCC3 3.3V
2.078A
2.66A
5VDUAL P/N MOS
4.448A
1.788A
10.4A
LDO 3VSB
2.4A
3.2A
SATA power per
12V 1.2A
5V 1.6A
Total 2 connector
2.66A
V1P0A
Switching APW8727L
Iin=((Iout*Vout)/0.8)/Vin
LDO V_3P3_LAN
LAN
VDD3P3 3.3V 177mA
VDD10 1V 300mA
FAN
CPU_FAN +12V 1A
SYS_FAN +12V 1A
1A
VGA
5V 0.5A
DVI
5V 0.5A
8A
0.85A
6.575A
2.975A
ATX_3VSB
VCC3
SIO IT8733
3VSB 3.3V TBD
VCC3 3.3V TBD
Battery 3.3V 3.3V TBD
Battery 3V
0.75A
6A
6A
0.375A
0.5A
3A
8.5A
5VDUAL UP7537
5VDUAL UP7536
AUDIO ALC662-VD
DVDD 3.3V 3.3V 11mA
AVDD 5V 42mA
Internal LDO
VCC3
ATX_5VSB
Wrieless LAN M.2 Slot per
3.3V 2.5A(S0)
3.3Vaux 0.1A(S5)
Total 1 Slots
3VDUAL P/N MOS
X16 PCIE Slot per
3.3V 3A(S0)
12V 5.5A(S0)
3.3Vaux 0.375A
Total 1 Slot
X1 PCIE Slot per
3.3V 3A(S0)
12V 0.5A(S0)
3.3Vaux 0.375A
Total 1 Slots
each USB3.0
5VDual 0.9A
Total 4 port
each USB2.0
5VDual 0.5A
Total 5 port
PS/2
5VDual 275mA
ECS ECS ECS
mitchhsieh
2015/07/28 18:14
Title
Power Delivery
Size
Custom
Document Number
H11H4-AD
Rev
1.0
Date:
Tuesday, July 14, 2015
Sheet
45
of
46

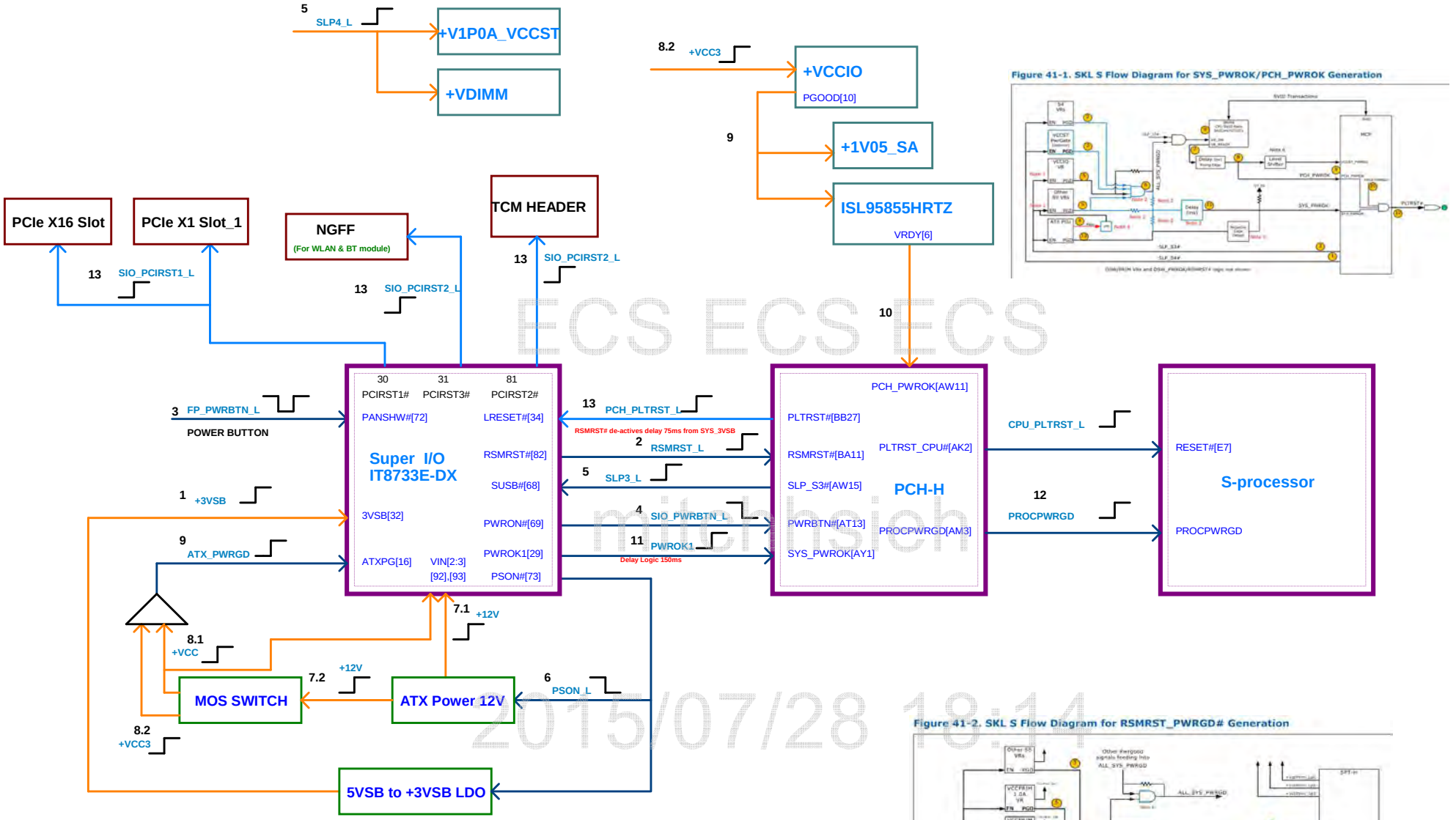
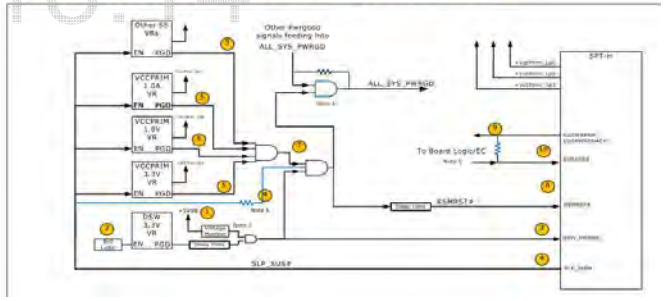


Figure 41-1. SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

Figure 41-2. SKL S Flow Diagram for RSMRST_PWRGD# Generation



Title	Power Sequence MAP		
Size C	Document Number H11H4-AD		Rev 1.0
Date: Tuesday, July 14, 2015		Sheet 46 of 46	