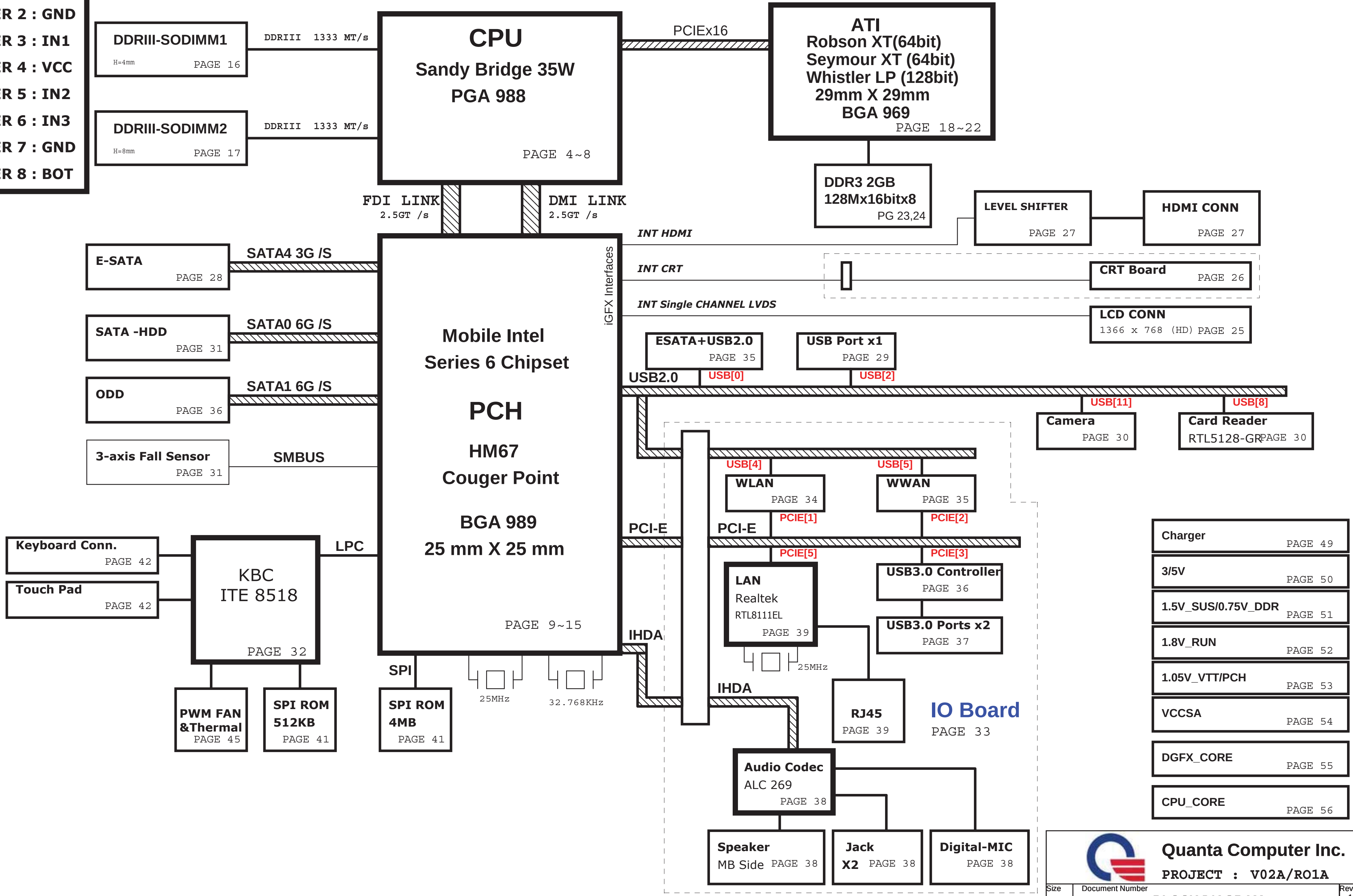
V02A/R01A DIS BLOCK DIAGRAM

PCB STACK UP

8L DIS

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : VCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT



Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	BLOCK DIAGRAM	1A
Date: Wednesday, January 19, 2011	Sheet 1 of 61	

power / State					
S0					
S1					
S3					
S4/S5 AC					
S4/S5 DC Only					
AC/DC No Exist					

SMBCLK SMBDATA								
SMB_CLK_ME1 SMB_DAT_ME1								
AB1A_CLK AB1A_DATA								

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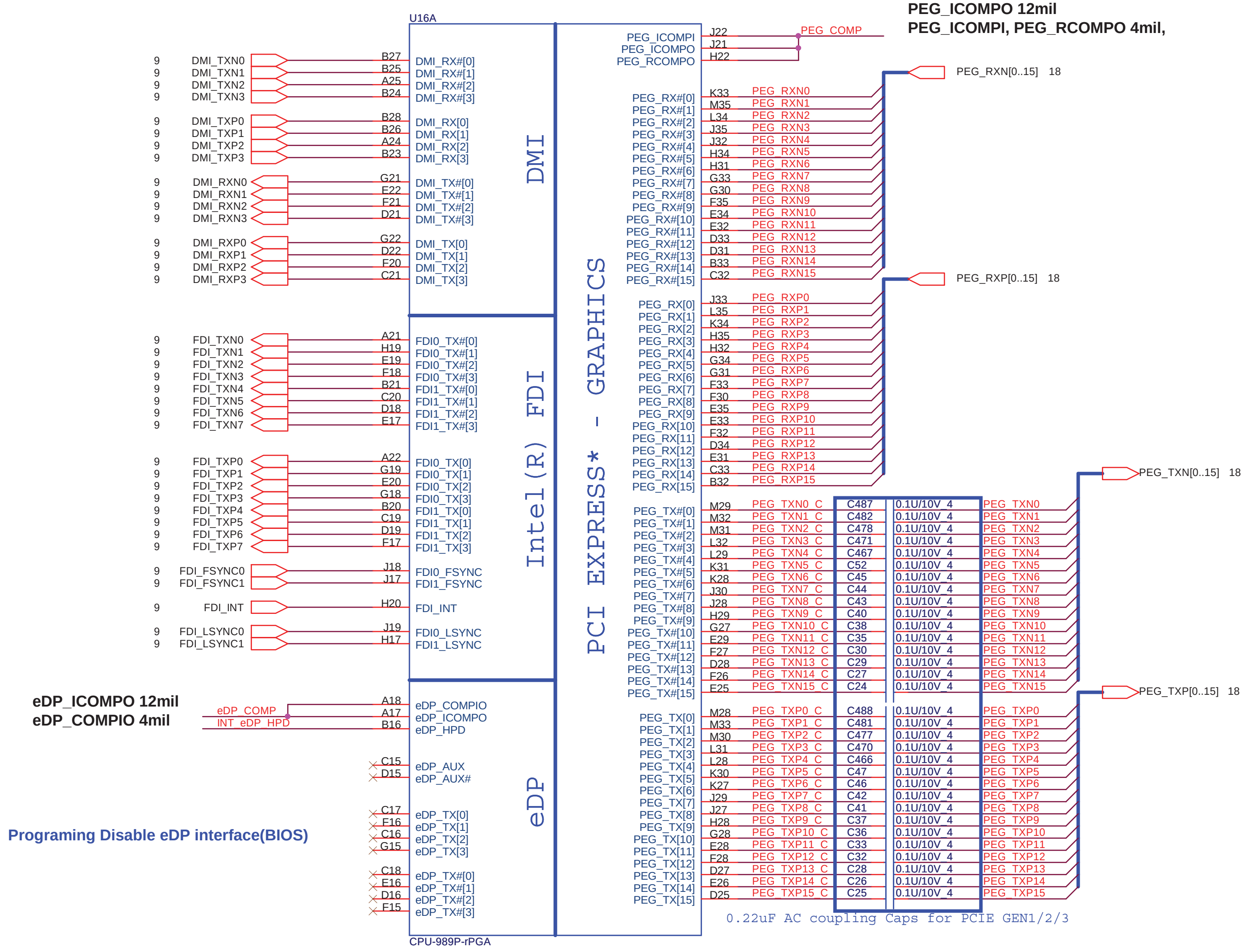
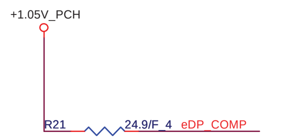
PROJECT : V02A/RO1A		
Size	Document Number: BLANK	Rev: 1A
Date: Wednesday, January 19, 2011	Sheet 3 of 61	

Sandy Bridge Processor (DMI,PEG,FDI)



Programing Disable eDP interface(BIOS)

DP & PEG Compensation

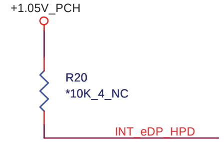


eDP_COMPIO and ICOMPO signals should be shorted near balls and routed within 500 mils

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils

PEG_ICOMPO signals should be routed within 500 mils

eDP Hot-plug (Disable)

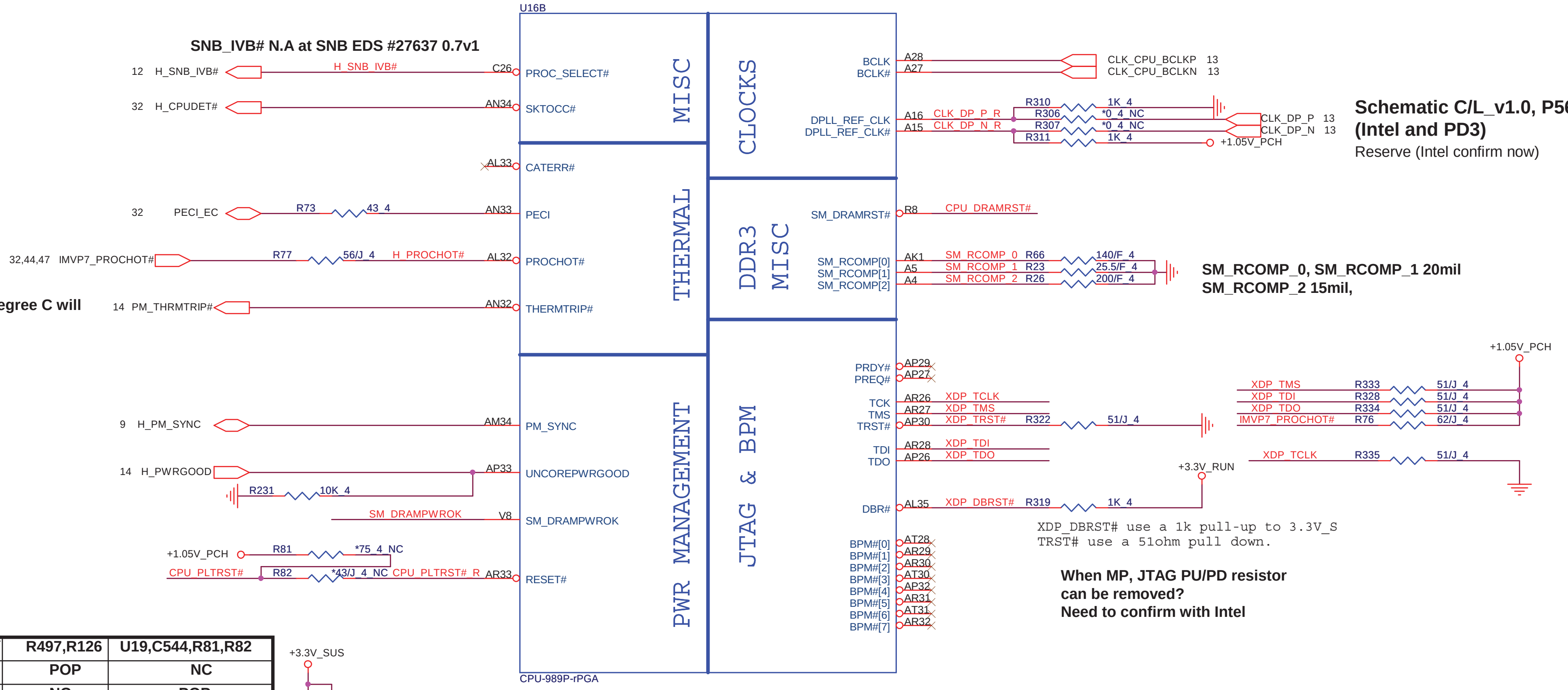


CAD Note: Place PU resistor within 2 inches of CPU

This signal can be left as no connect if entire eDP interface is disabled.

Sandy Bridge Processor (CLK,MISC,JTAG)

SNB_IVB# N.A at SNB EDS #27637 0.7v1



Schematic C/L_v1.0, P56 (PU,PD 1k/J)
(Intel and PD3)
Reserve (Intel confirm now)

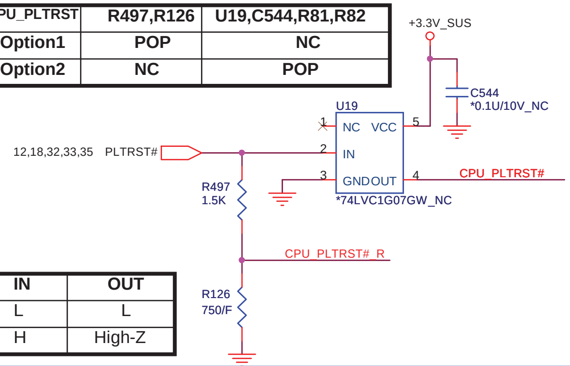
SM_RCOMP_0, SM_RCOMP_1 20mil
SM_RCOMP_2 15mil,

Over 130 degree C will drive low

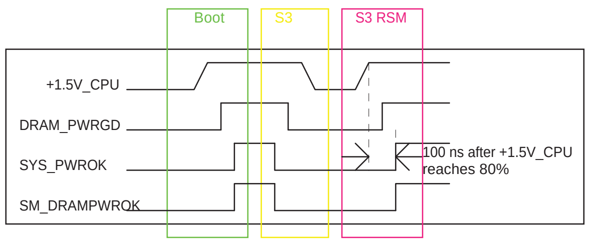
XDP_DBRST# use a 1k pull-up to 3.3V_S
TRST# use a 51ohm pull down.

When MP, JTAG PU/PD resistor can be removed?
Need to confirm with Intel

CPU_PLTRST	R497,R126	U19,C544,R81,R82
Option1	POP	NC
Option2	NC	POP

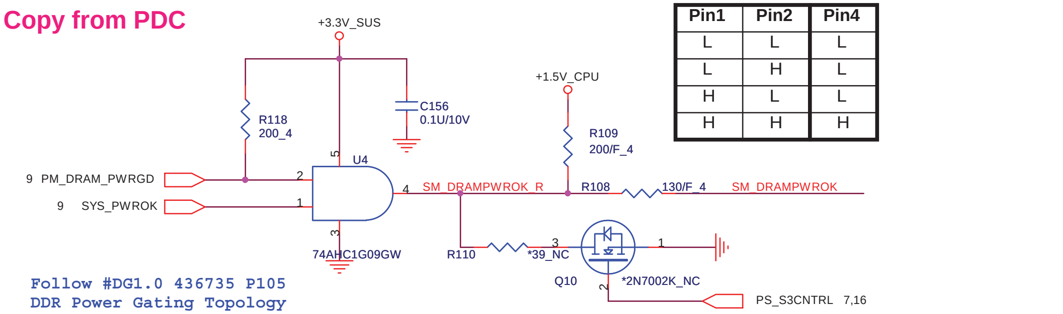


IN	OUT
L	L
H	High-Z



Change OD part same with PDC

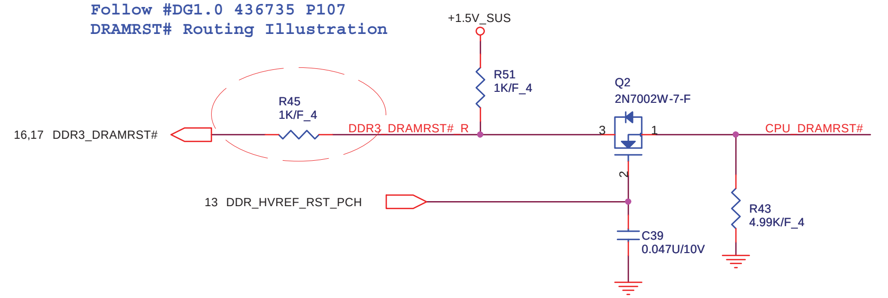
Copy from PDC



Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	H

Follow #DG1.0 436735 P105
DDR Power Gating Topology

Follow #DG1.0 436735 P107
DRAMRST# Routing Illustration



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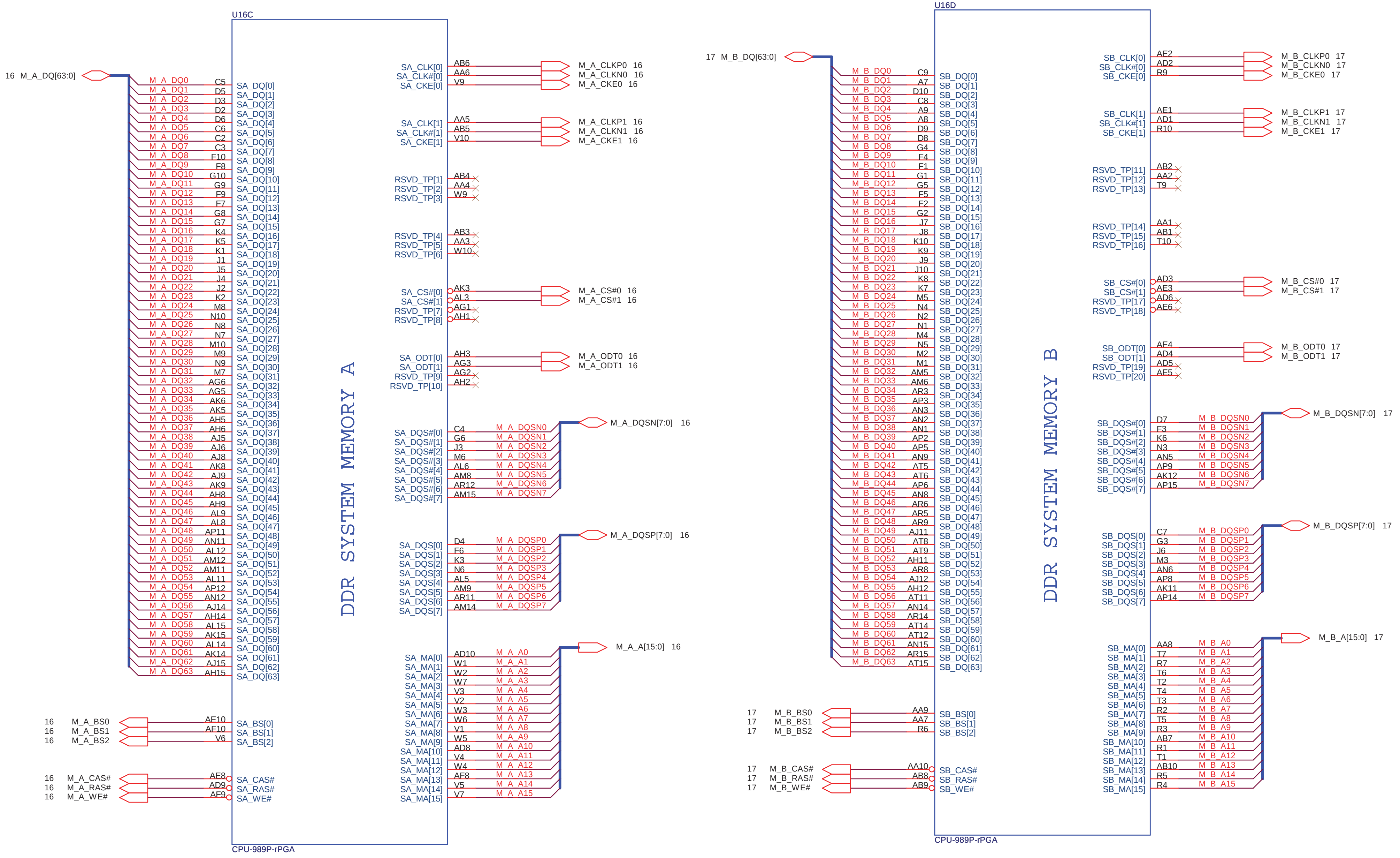
PROJECT : V02A/R01A

Size	Document Number	Rev
	Sandy Bridge 2/5	1A
Date: Wednesday, January 19, 2011	Sheet 5 of 61	

Sandy Bridge Processor (DDR3)



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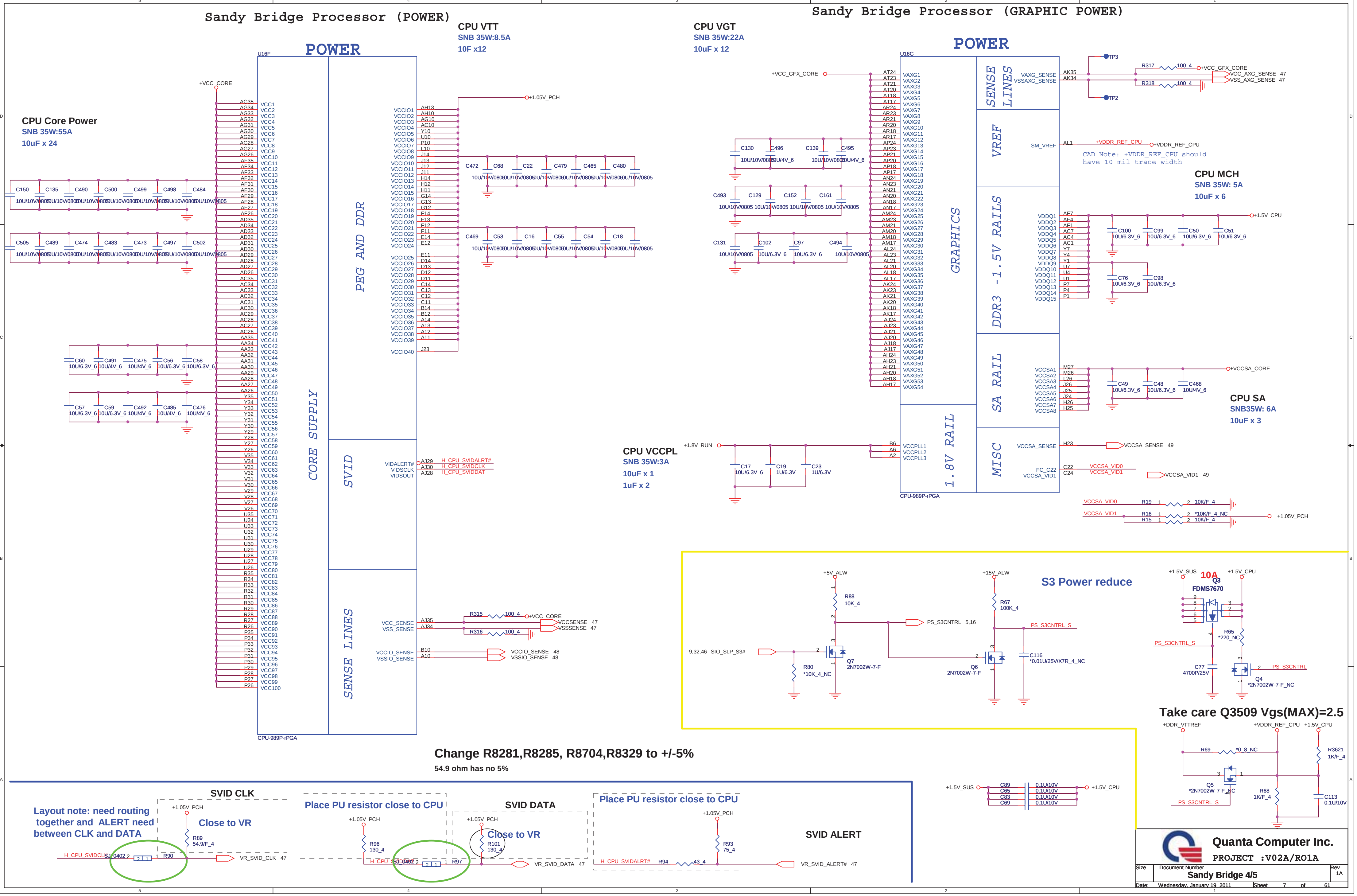
PROJECT : V02A/R01A

Size	Document Number	Rev
	Sandy Bridge 3/5	1A

Date: Wednesday, January 19, 2011 Sheet 6 of 61



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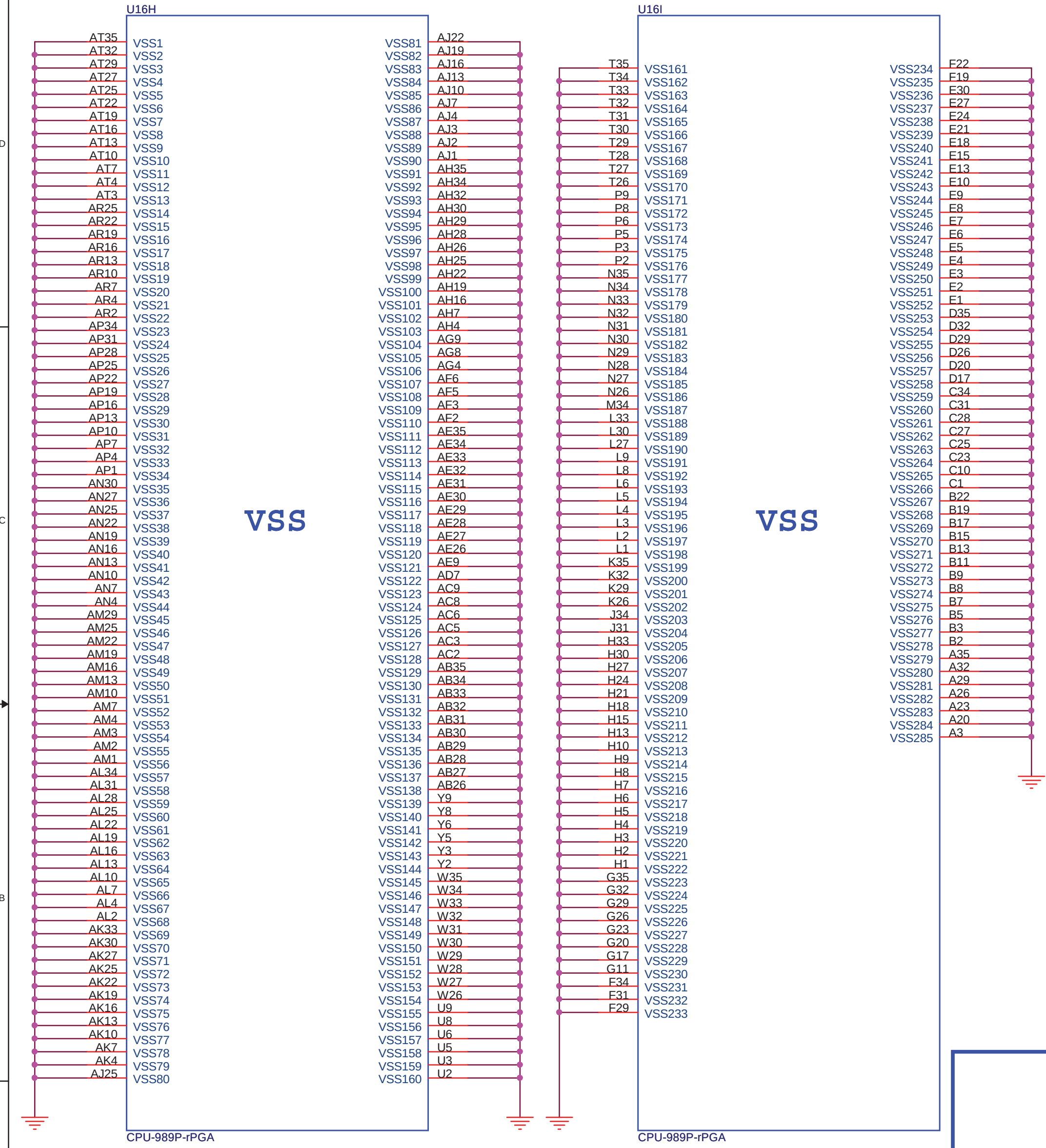
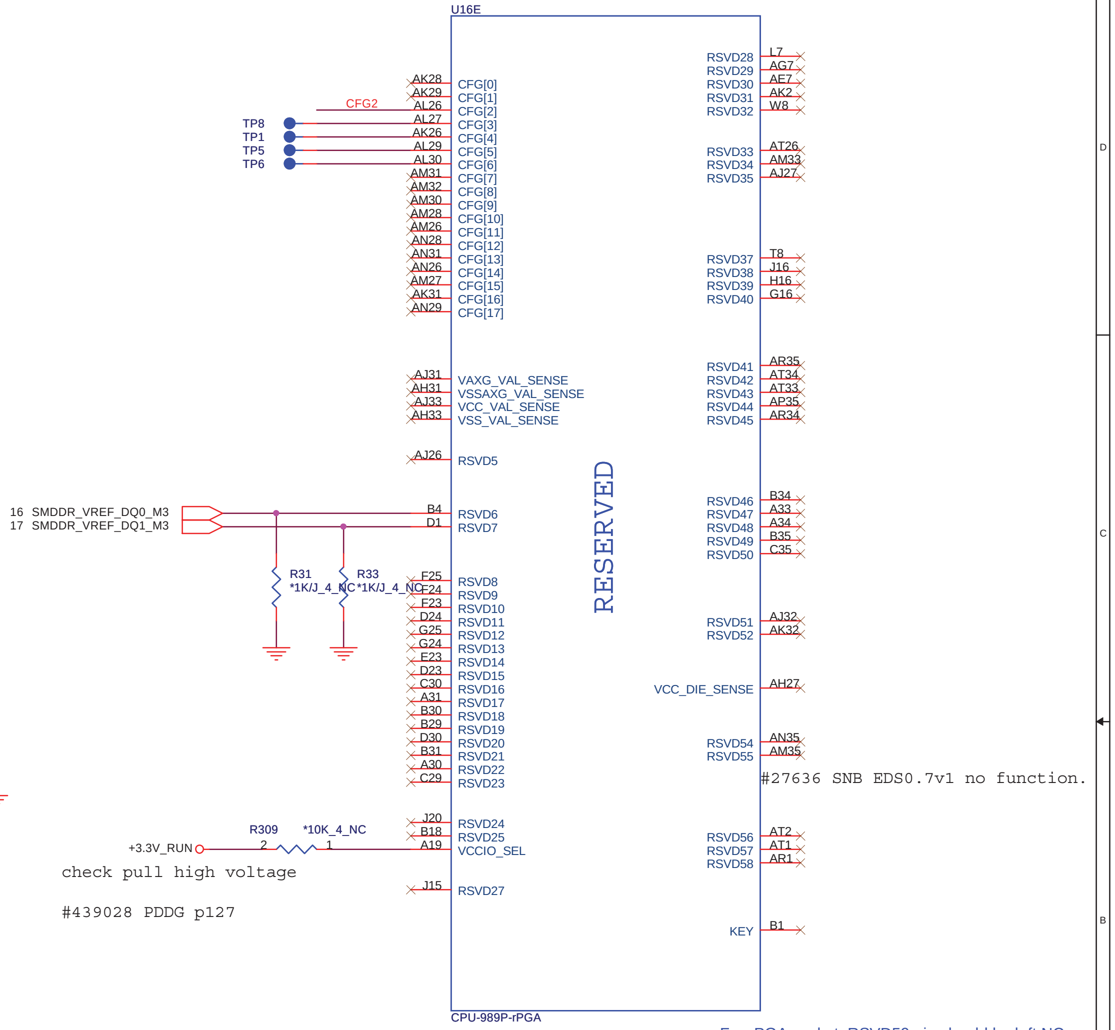
PROJECT :V02A/R01A

Size	Document Number	Rev
	Sandy Bridge 4/5	1A
Date: Wednesday, January 19, 2011	Sheet 7 of 61	

Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)



#27636 SNB EDS0.7v1 no function.

check pull high voltage

#439028 PDDG p127

For rPGA socket, RSVD59 pin should be left NC

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

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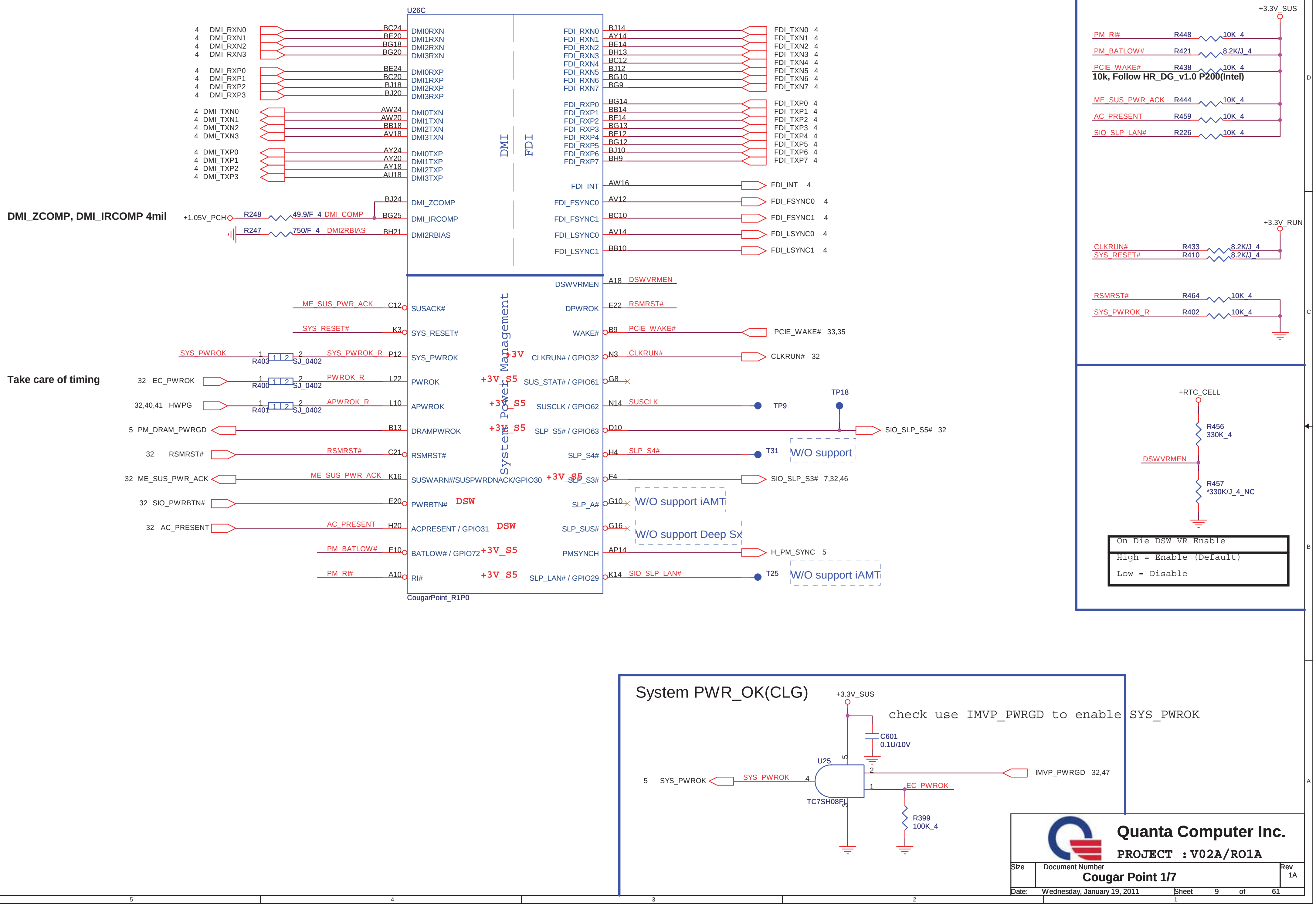
PROJECT : V02A/R01A

Size	Document Number	Rev
	Sandy Bridge 5/5	1A

Date: Wednesday, January 19, 2011 Sheet 8 of 61

Cougar Point (DMI,FDI,PM)



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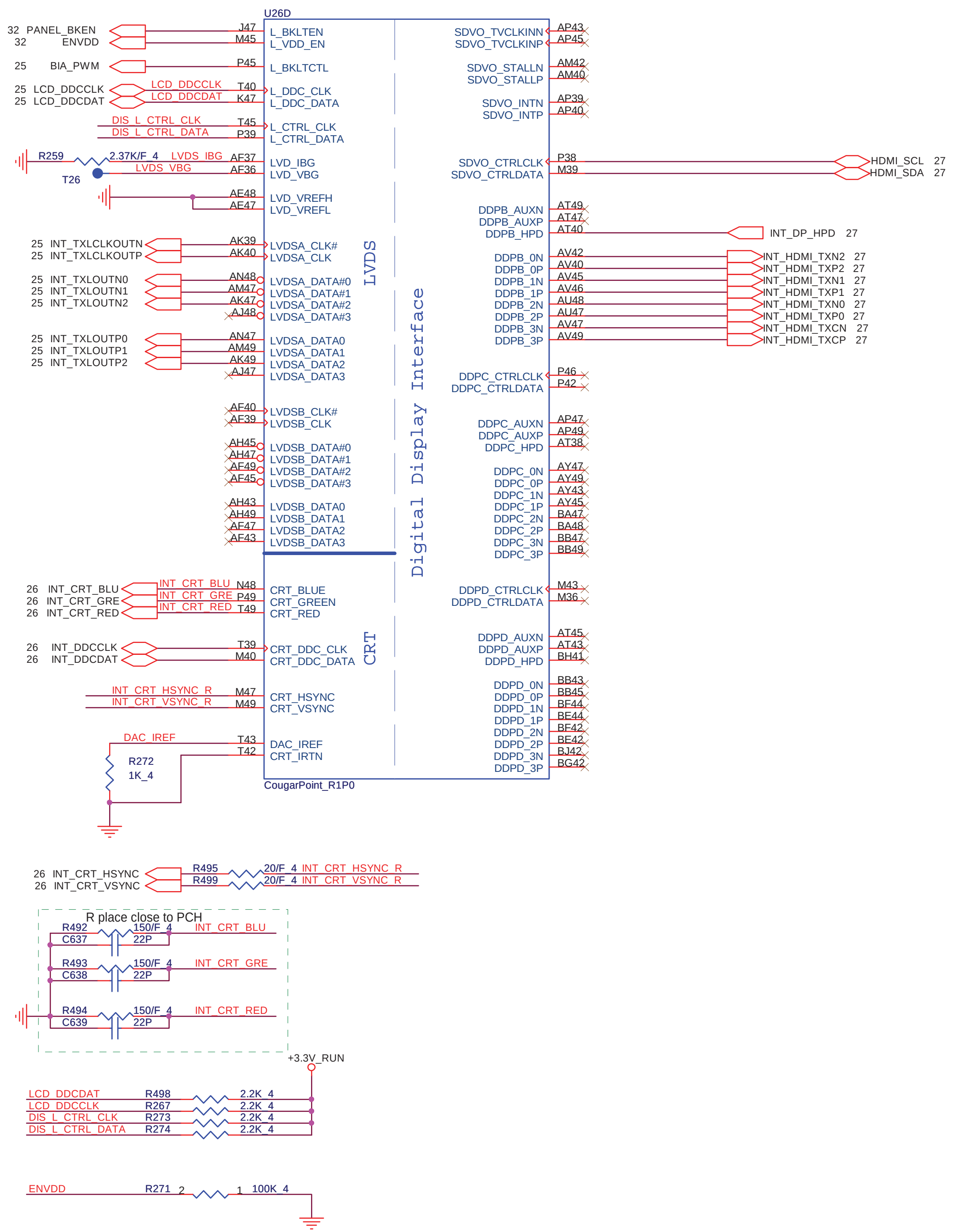
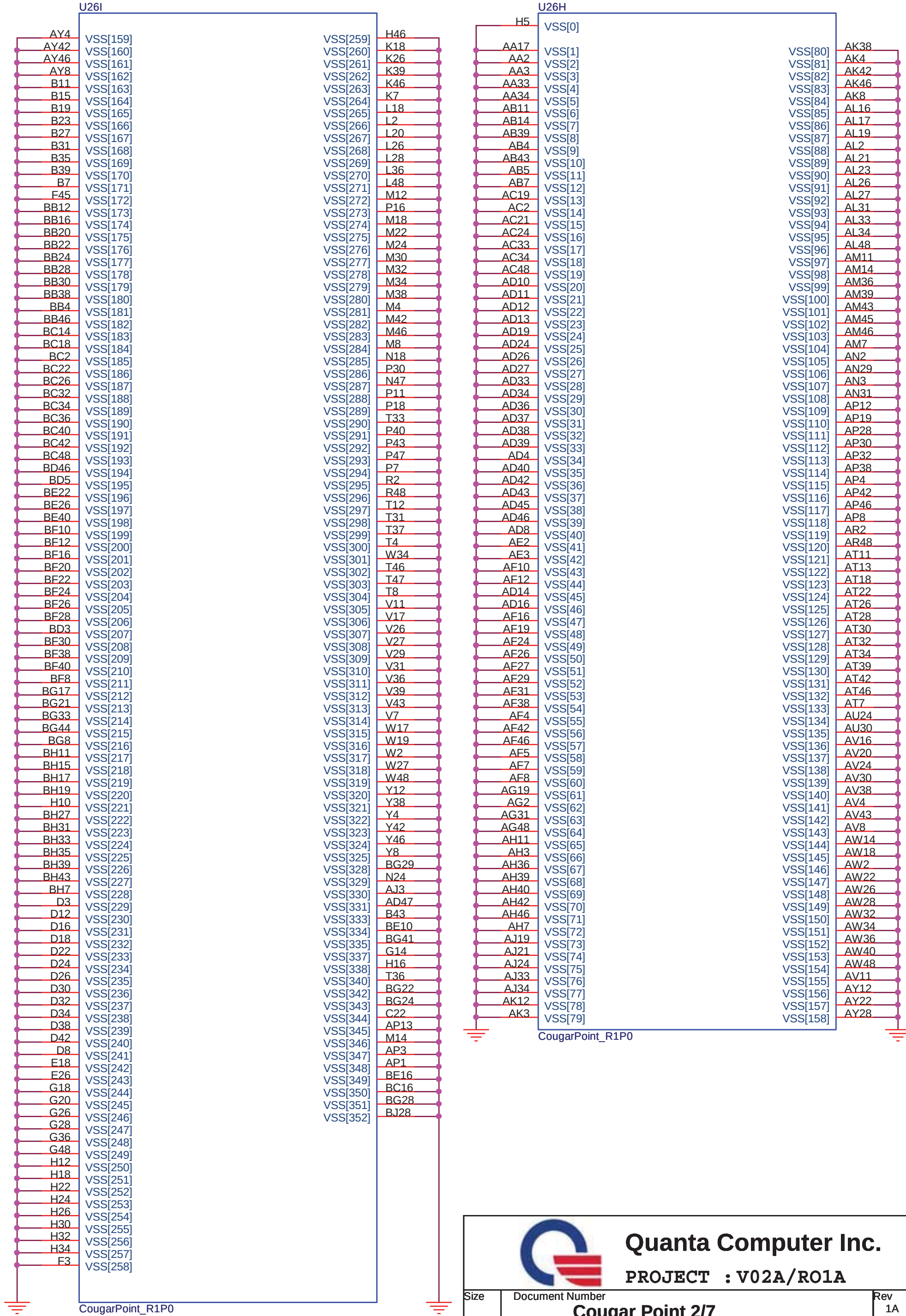
PROJECT : V02A/RO1A

Size	Document Number	Rev
	Cougar Point 1/7	1A
Date: Wednesday, January 19, 2011	Sheet 9 of 61	

Cougar Point (LVDS,DDI)



Cougar Point (GND)



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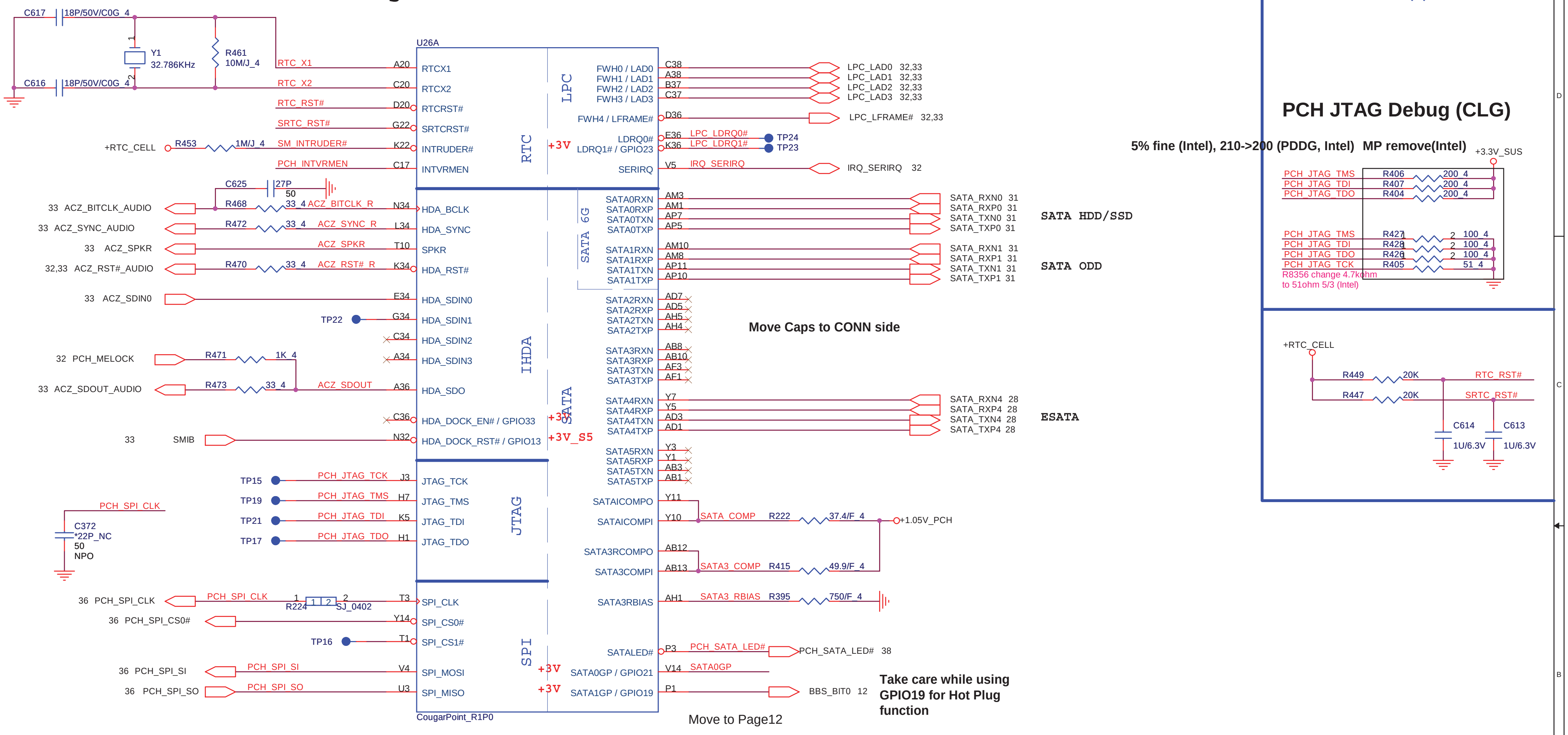
PROJECT : V02A/R01A

Size	Document Number	Rev
	Cougar Point 2/7	1A
Date: Wednesday, January 19, 2011	Sheet 10 of 61	

Cougar Point (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_SUS R413 *1K_4_NC ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS R474 *1K_4_NC ACZ_SDOUT
Del 0510			Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R455 330K_4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS R469 1K_4 ACZ_SYNC_R

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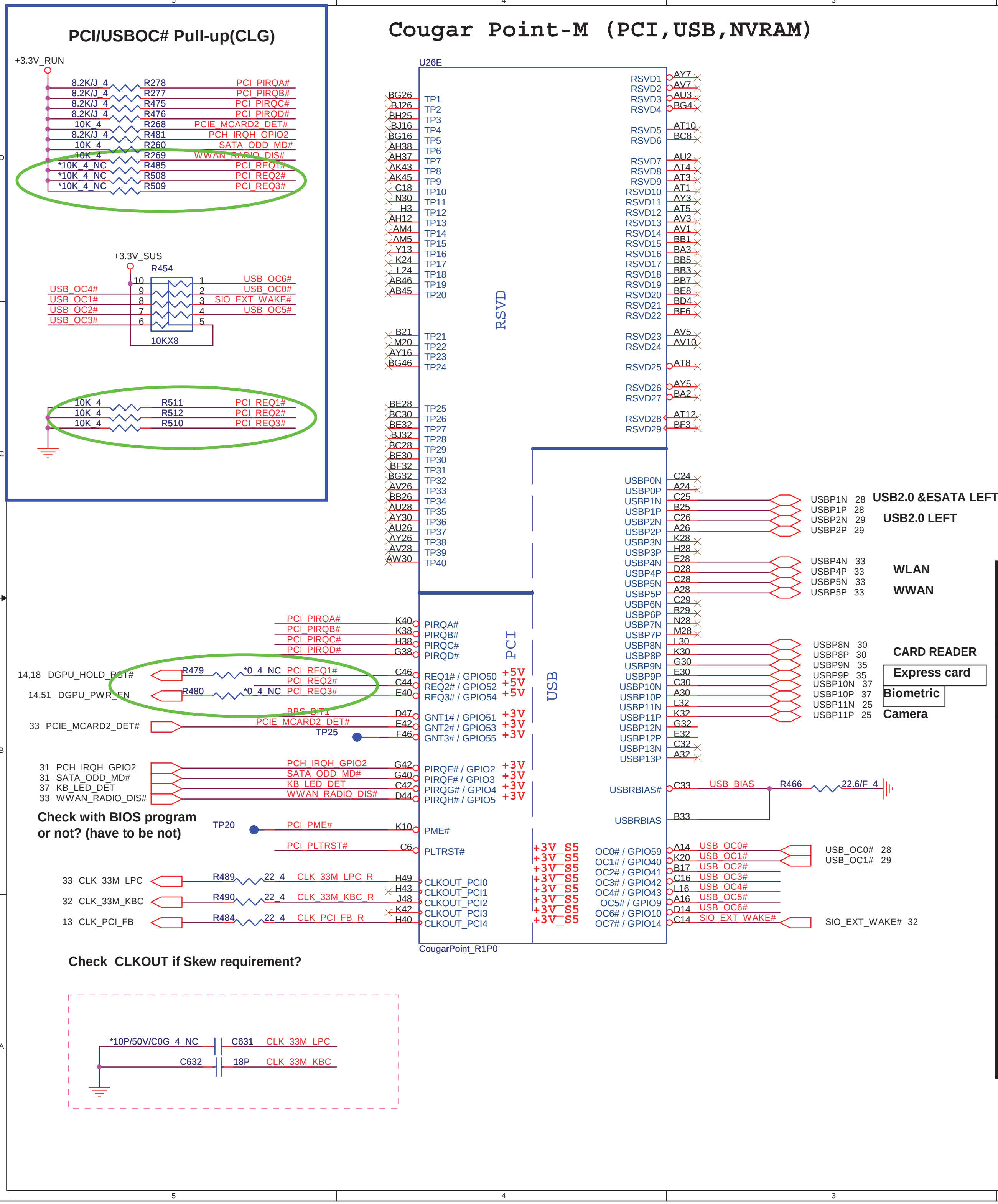
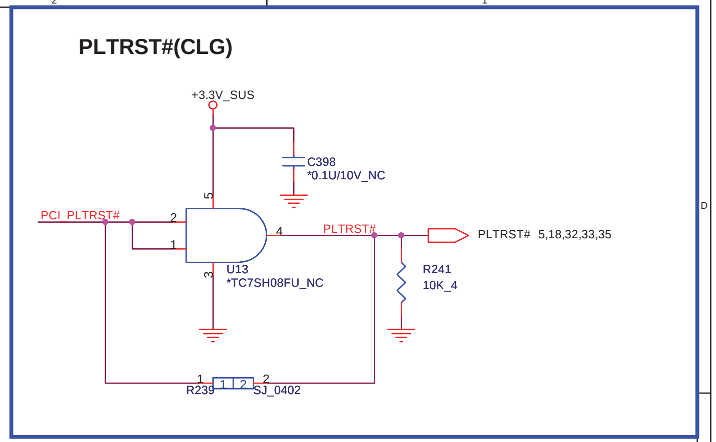
PROJECT : V02A/R01A

Size | Document Number: Cougar Point 3/7 | Rev 1A

Date: Wednesday, January 19, 2011 | Sheet 11 of 61

Cougar Point-M (PCI,USB,NVRAM)





Pin Name	Strap description	Sampled	Configuration
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm

Bit 0	Bit 1	Boot Location
1	1	SPI *
0	0	LPC

Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

CheckList_1.0 p58; HR_v1.0 p450

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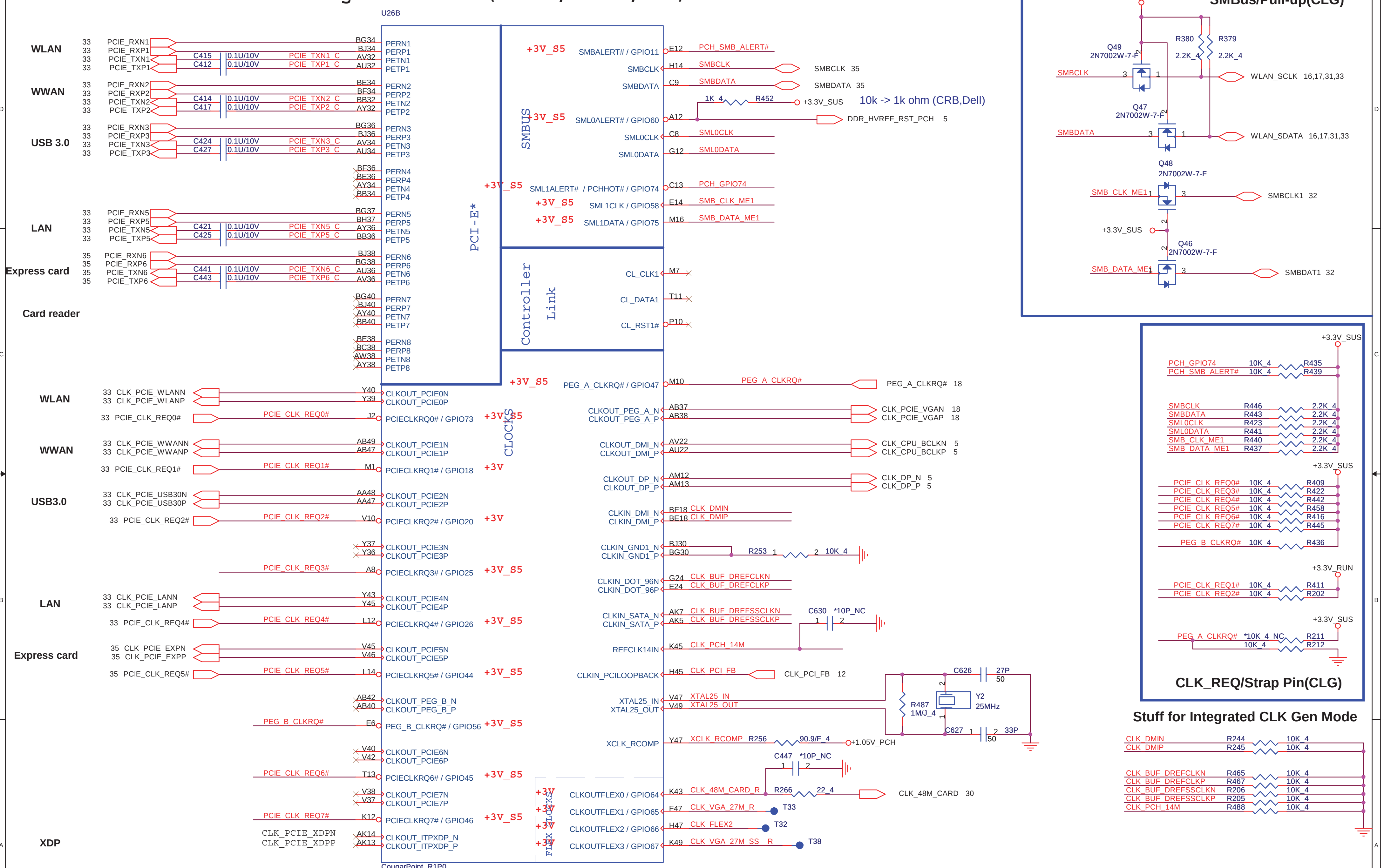
PROJECT : V02A/R01A

Size	Document Number	Rev
	Cougar Point 4/7	1A

Date: Thursday, January 20, 2011 Sheet 12 of 61

Cougar Point-M (PCI-E,SMBUS,CLK)



	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 /GPIO64	• 33 /27 /48/ 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 /GPIO65	unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC /48/24 MHz
CLKOUTFLEX2 /GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 /GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)

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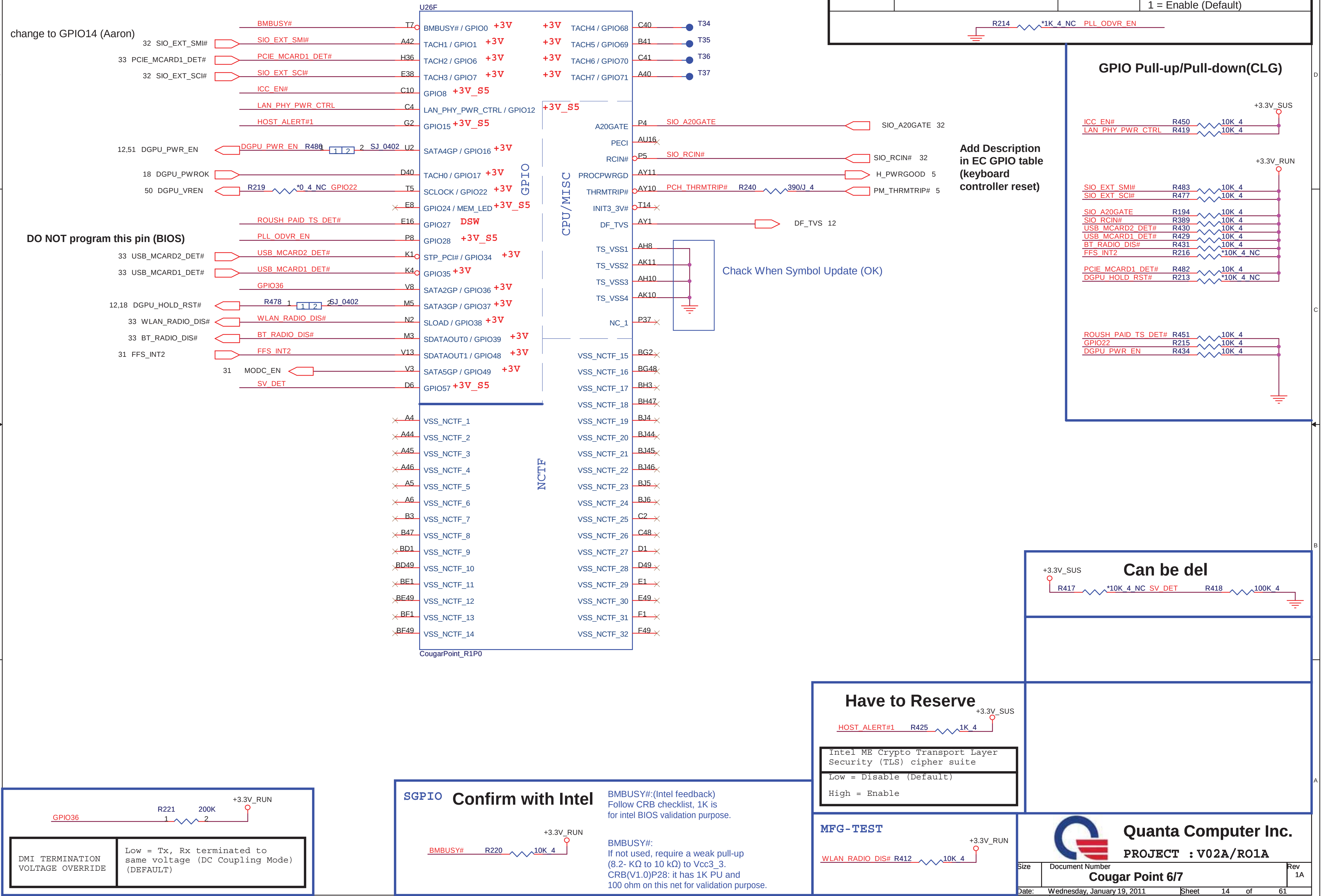
PROJECT : V02A/R01A

Size | Document Number: Cougar Point 5/7 | Rev 1A

Date: Wednesday, January 19, 2011 | Sheet 13 of 61

Cougar Point (GPIO,VSS_NCTF,RSVD)

Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)



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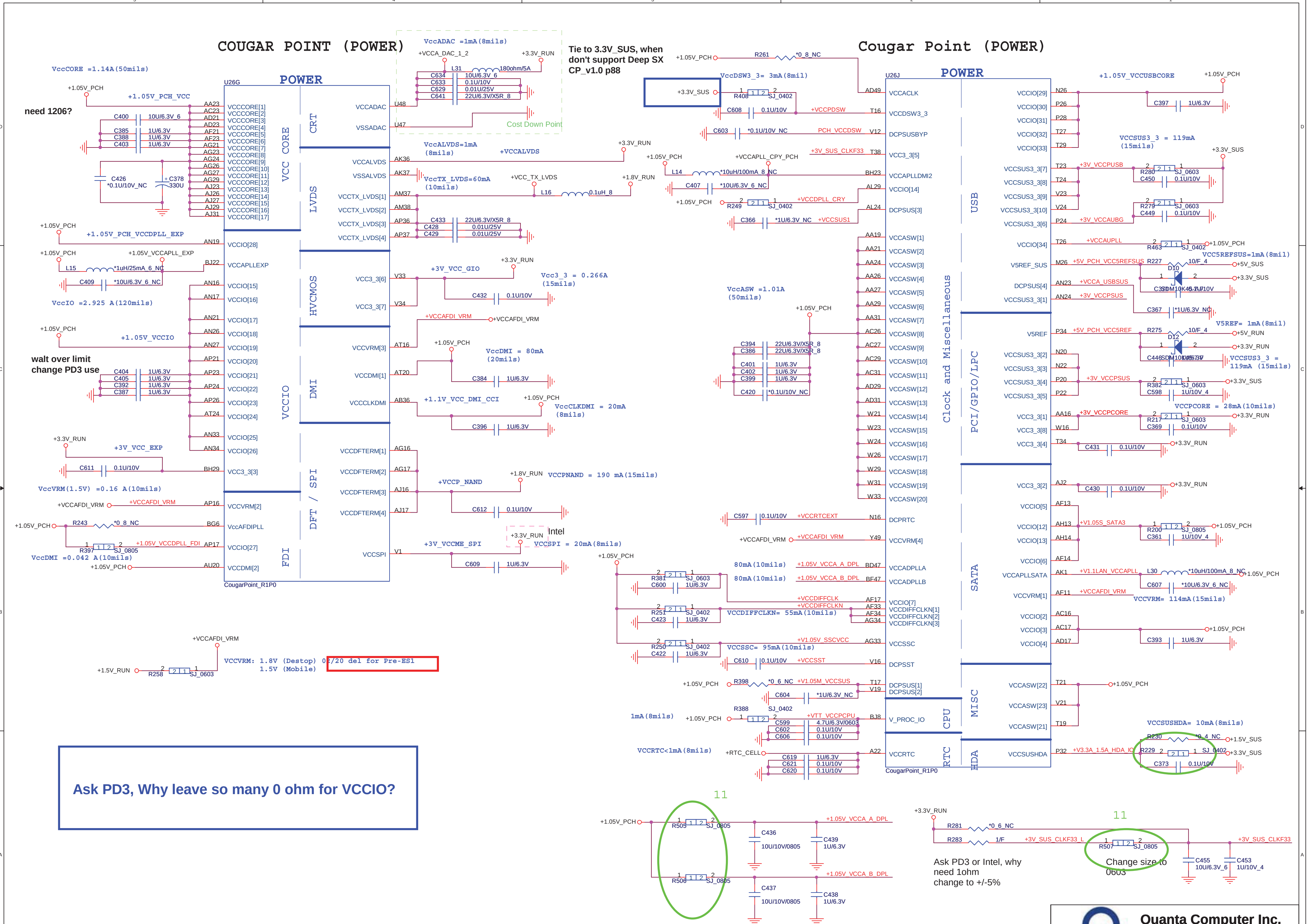
PROJECT : V02A/R01A

Size	Document Number	Rev
	Cougar Point 6/7	1A

Date: Wednesday, January 19, 2011 Sheet 14 of 61



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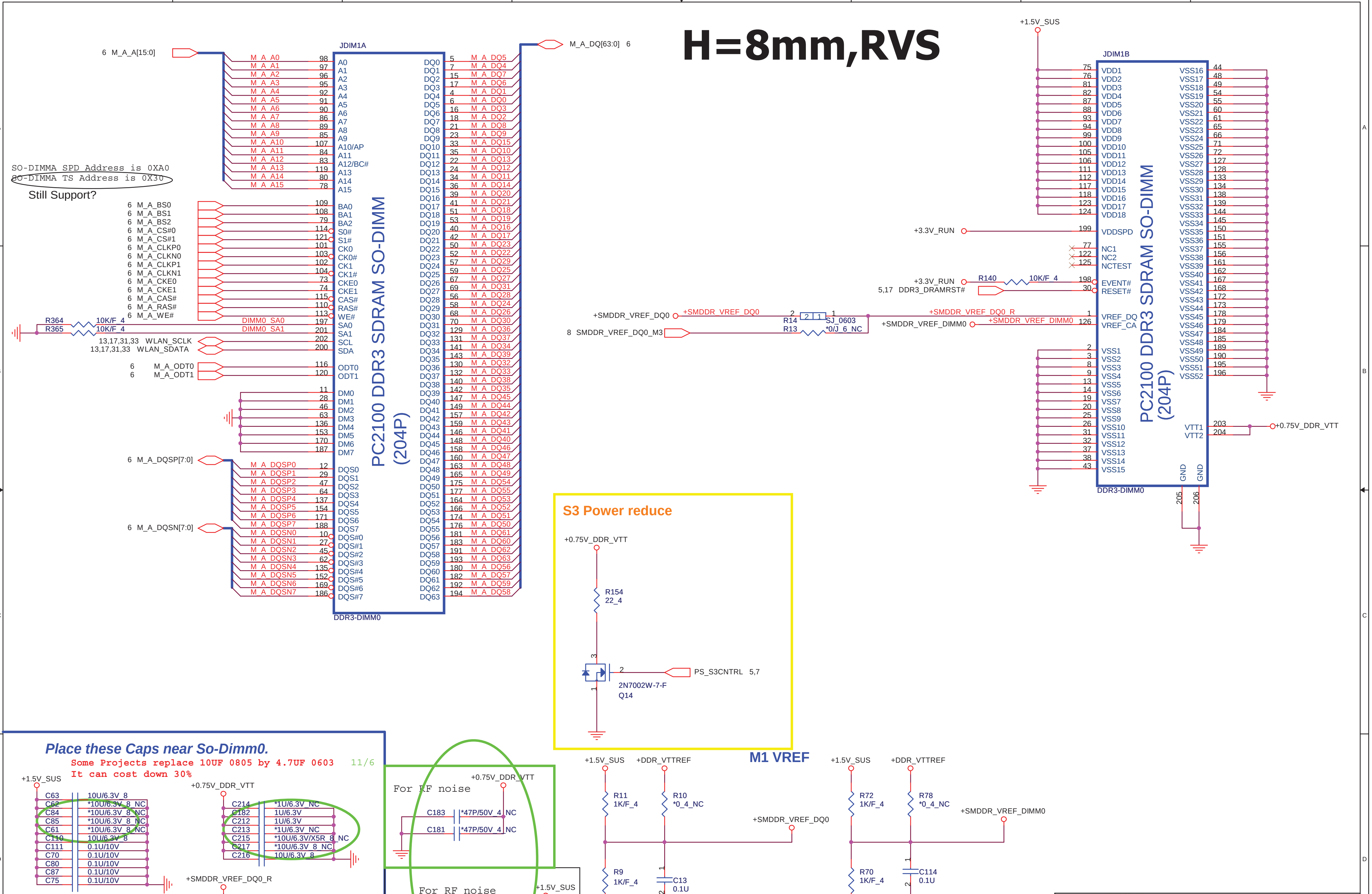
PROJECT :V02A/R01A		
Size	Document Number: Cougar Point 7/7	Rev 1A
Date: Friday, January 21, 2011	Sheet 15 of 61	



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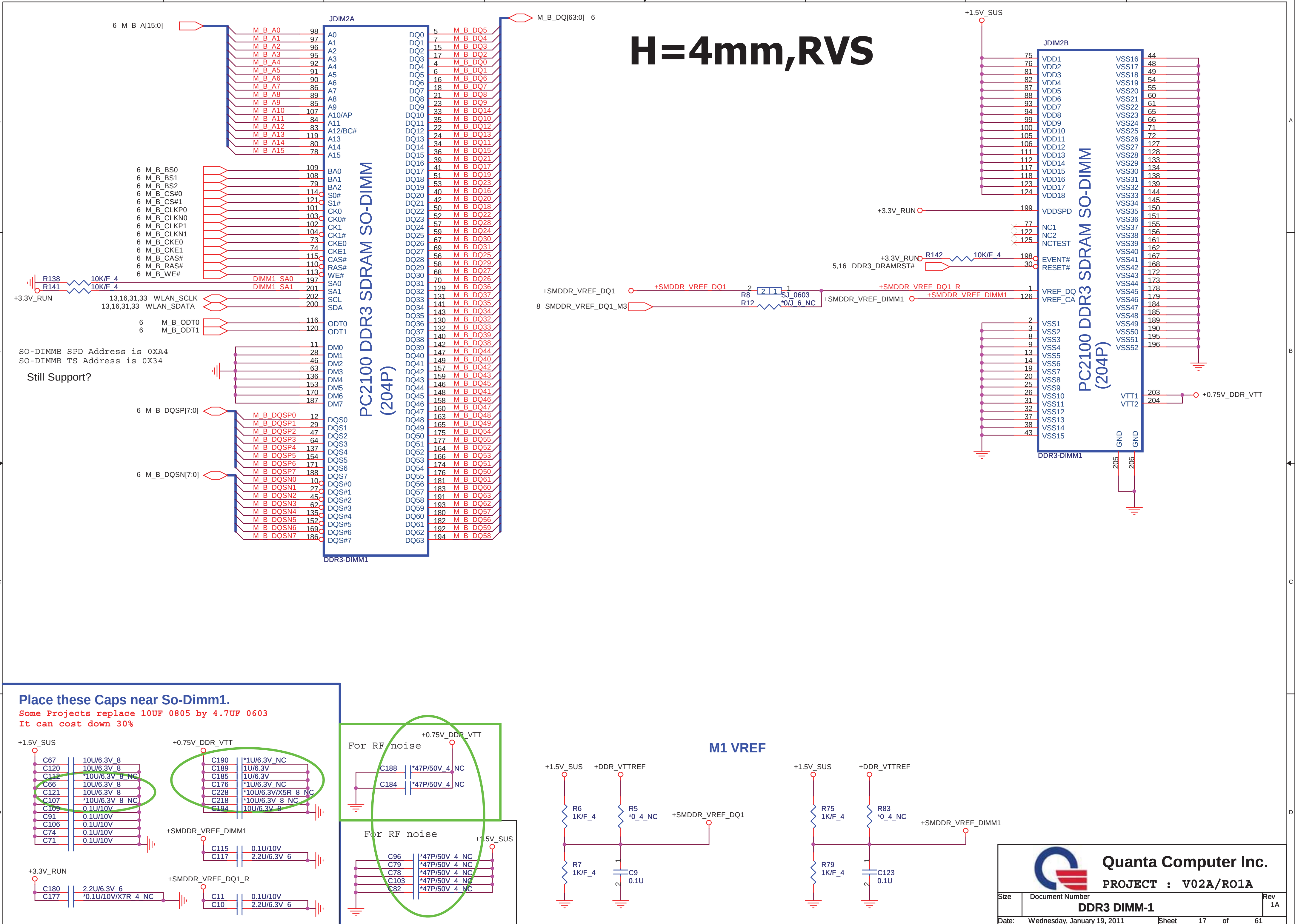
PROJECT : V02A/R01A

Size	Document Number	Rev
	DDR3 DIMM-0	1A
Date: Wednesday, January 19, 2011	Sheet 16 of 61	



H=4mm,RVS
JDIM2A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1
JDIM2B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1
6 M_B_A[15:0]
M_B_DQ[63:0] 6
+1.5V_SUS
+3.3V_RUN
+0.75V_DDR_VTT
+SMDDR_VREF_DQ1
+SMDDR_VREF_DQ1_R
+SMDDR_VREF_DIMM1
8 SMDDR_VREF_DQ1_M3
5,16 DDR3_DRAMRST#
13,16,31,33 WLAN_SCLK
13,16,31,33 WLAN_SDATA
SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34
Still Support?
6 M_B_DQSP[7:0]
6 M_B_DQSN[7:0]
Place these Caps near So-Dimm1.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%
For RF noise
For RF noise
M1 VREF
+DDR_VTTREF
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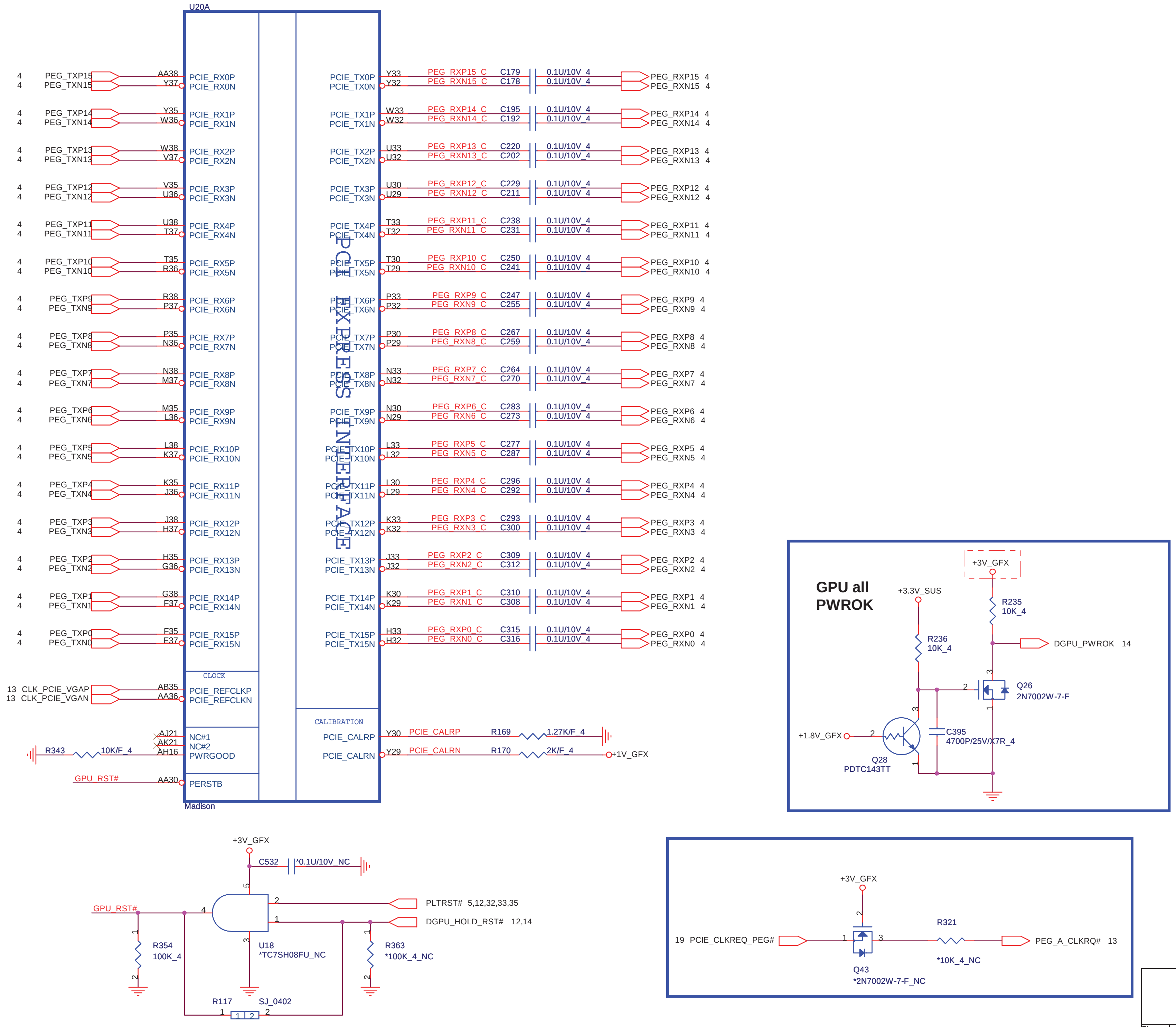
PROJECT : V02A/R01A
Size
Document Number
DDR3 DIMM-1
Rev
1A
Date: Wednesday, January 19, 2011
Sheet 17 of 61



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PROJECT : V02A/RO1A

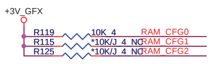
Size	Document Number	Rev
	N11M-GE2 (PCIE I/F) 1/5	1A

Date: Wednesday, January 19, 2011 Sheet 18 of 61

CONFIGURATION STRAPS

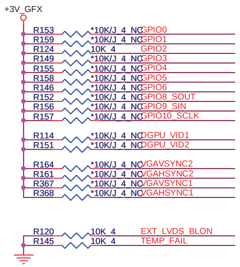
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	0
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	1
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	0
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	00
VIP_DEVICE_STRAP_EN	BIOS_ROM_EN	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0

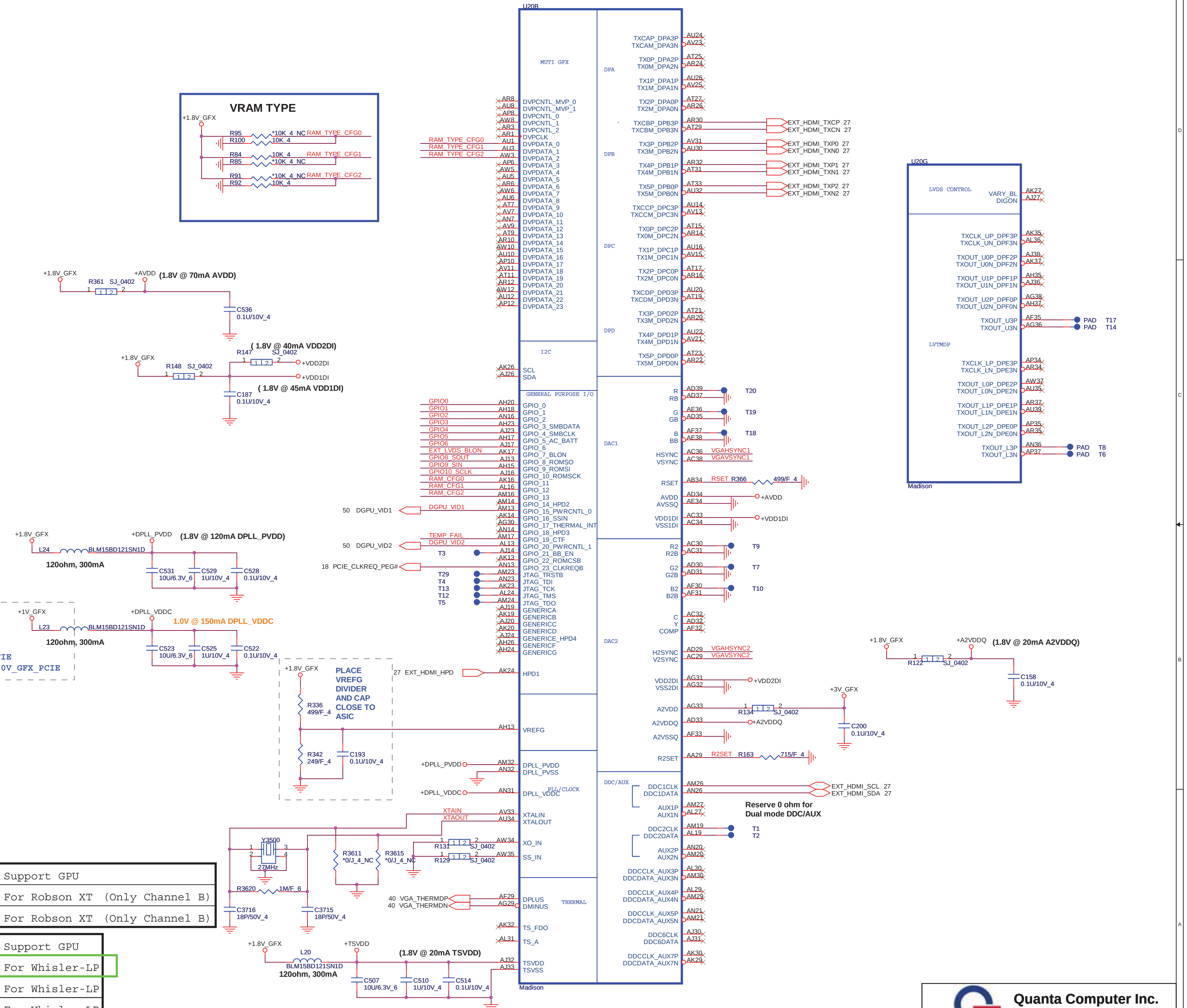
APERTURE SIZE



MEMORY APERTURE SIZE SELECT

MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0





Memory Straps	RAM_TYPE _CFG2	RAM_TYPE _CFG1	RAM_TYPE _CFG0	Quanta PN (QuantaBuy)	Vendor PN	Support GPU
900MHz Samsung 1GB(128M*16*4pcs)	0	0	1	AKD5MGWT507	K4W2G1646C-HC11	For Robson XT (Only Channel B)
900MHz Hynix 1GB(128M*16*4pcs)	0	1	0	AKD5MGWTW06	H5TQ2G63BFR-11C	For Robson XT (Only Channel B)

Memory Straps	RAM_TYPE _CFG2	RAM_TYPE _CFG1	RAM_TYPE _CFG0	Quanta PN (QuantaBuy)	Vendor PN	Support GPU
900MHz Samsung 1GB(64M*16*8pcs)	0	0	1	AKD5LGHT505	K4W1G1646E-HC11	For Whisler-LP
900MHz Hynix 1GB(64M*16*8pcs)	0	1	0	AKD5LZWTW07	H5TQ1G63DFR-11C	For Whisler-LP
900MHz Samsung 1GB(64M*16*8pcs)	1	0	0	AKD5EGGT500	K4W1G1646G-BC11	For Whisler-LP

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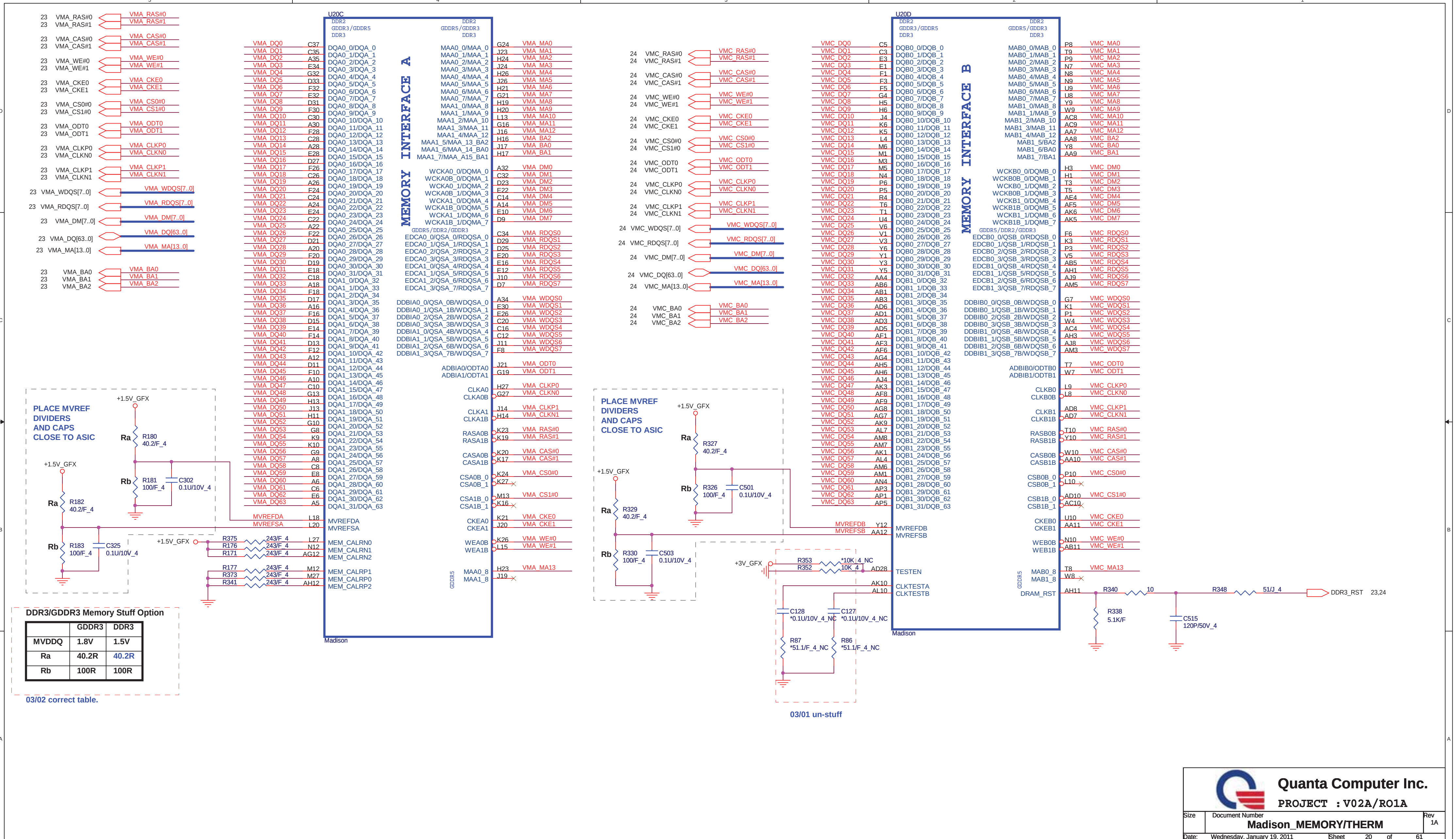
PROJECT :V02A/R01A

Size	Document Number	Rev
	Madison_IO&STRAP	1A
Date: Wednesday, January 19, 2011	Sheet 19 of 61	



DDR3/GDDR3 Memory Stuff Option

	GDDR3	DDR3
MVDDQ	1.8V	1.5V
Ra	40.2R	40.2R
Rb	100R	100R

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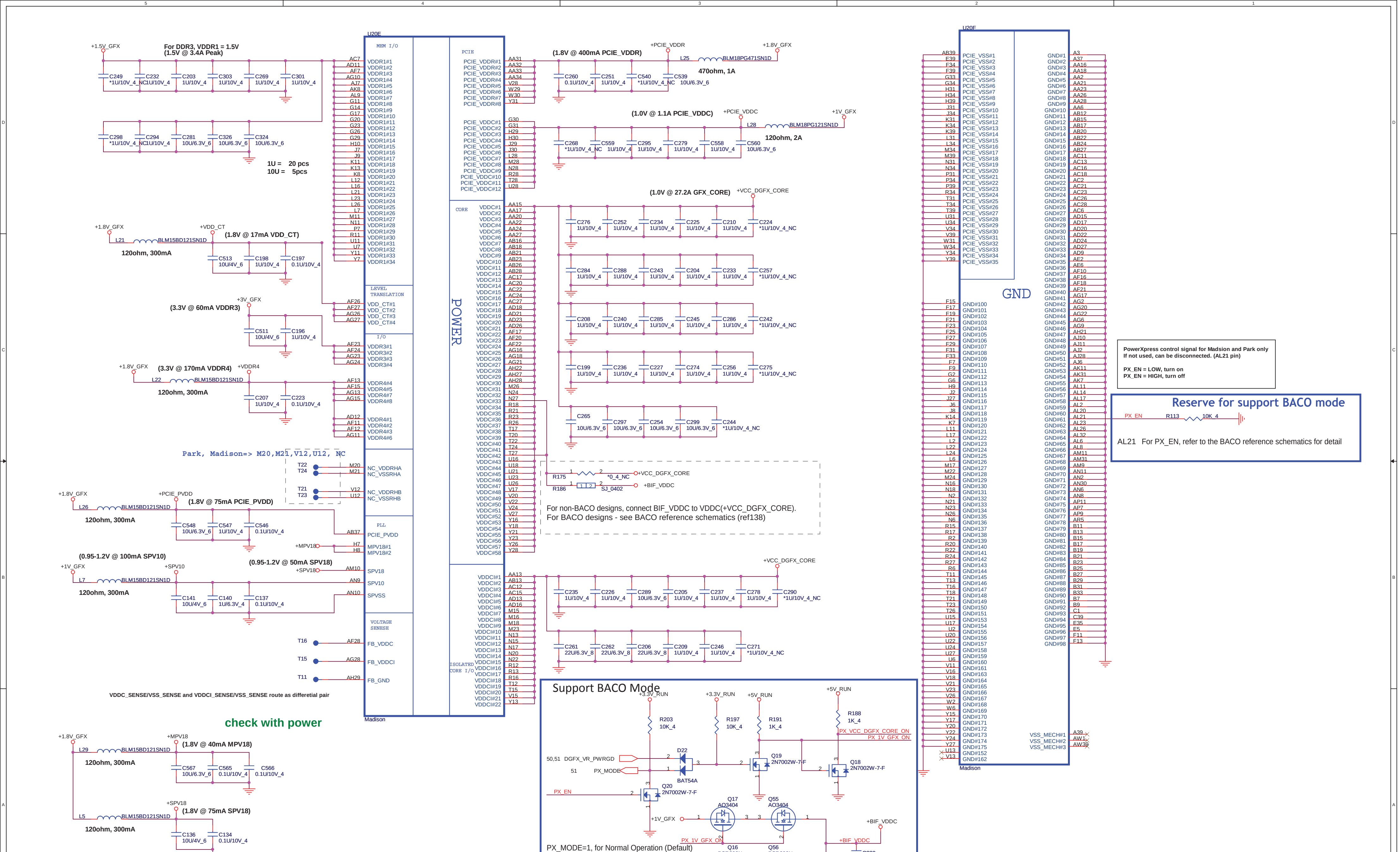
PROJECT : V02A/RO1A

Size	Document Number	Rev
	Madison_MEMORY/THERM	1A

Date: Wednesday, January 19, 2011 Sheet 20 of 61



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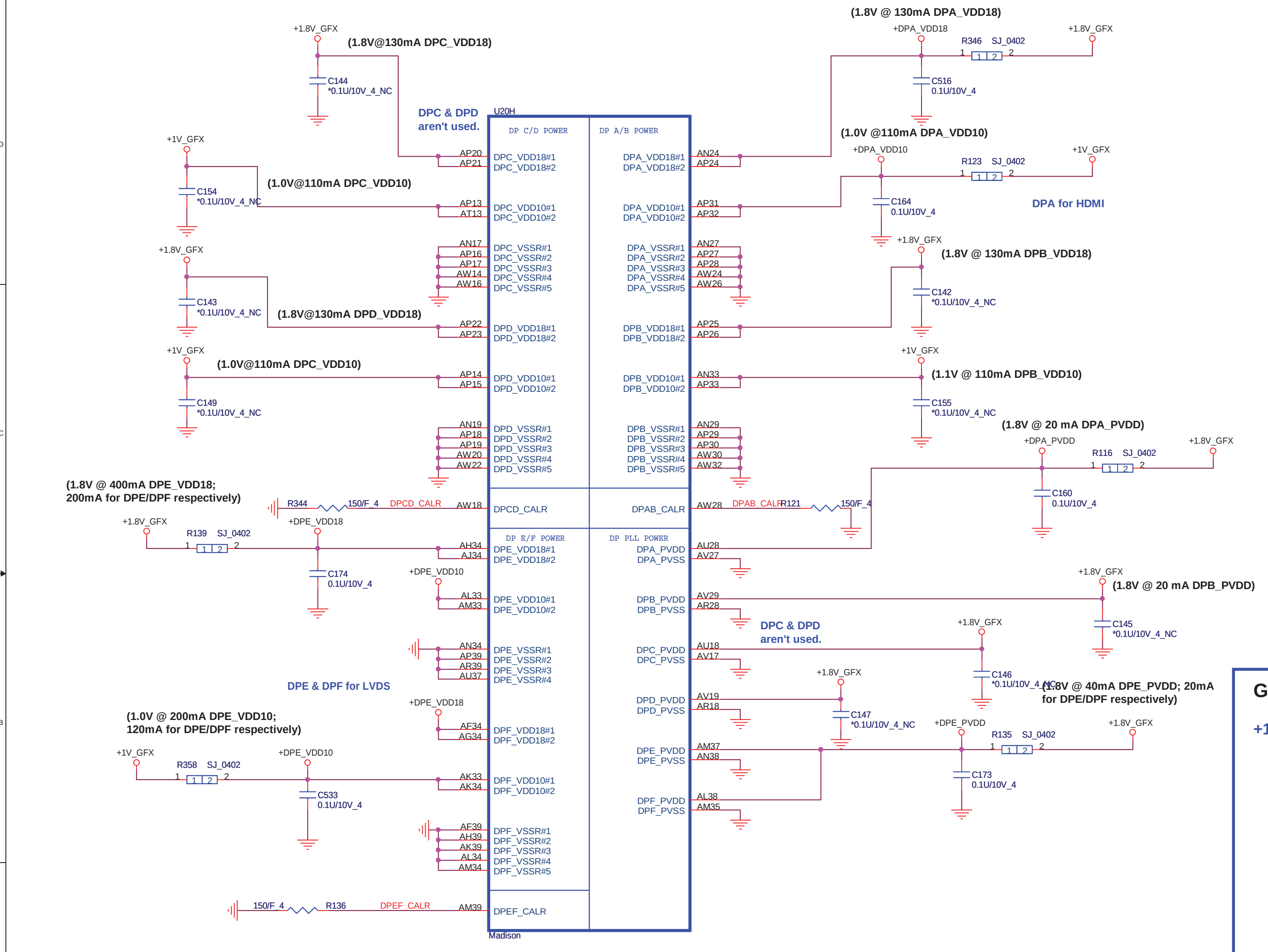
PROJECT : V02A/R01A

Size	Document Number	Rev
	Madison_POWER	1A

Date: Wednesday, January 19, 2011 Sheet 21 of 61



GPU Power Rail List

+1V_GFX=>	+1.8V_GPU=>
+DPA_VDD10	+A2VDDQ
+SPV10	+AVDD
+DPE_VDD10	+DPA_PVDD
+DPLL_VDDC	+DPA_VDD18
+PCIE_VDDC	+DPE_PVDD
	+DPE_VDD18
	+DPLL_PVDD
	+MPV18
	+PCIE_PVDD
	+PCIE_VDDR
	+SPV18
	+TSVDD
	+VDD1DI
	+VDD2DI
	+VDD_CT
	+VDDR4

GPU Power-on sequence

1 => +3V_GFX
2 => +VCC_DGFX_CORE
3 => +1V_GFX
4 => +1.5V_GFX
5 => +1.8V_GFX
6 => dGPU_PWROK

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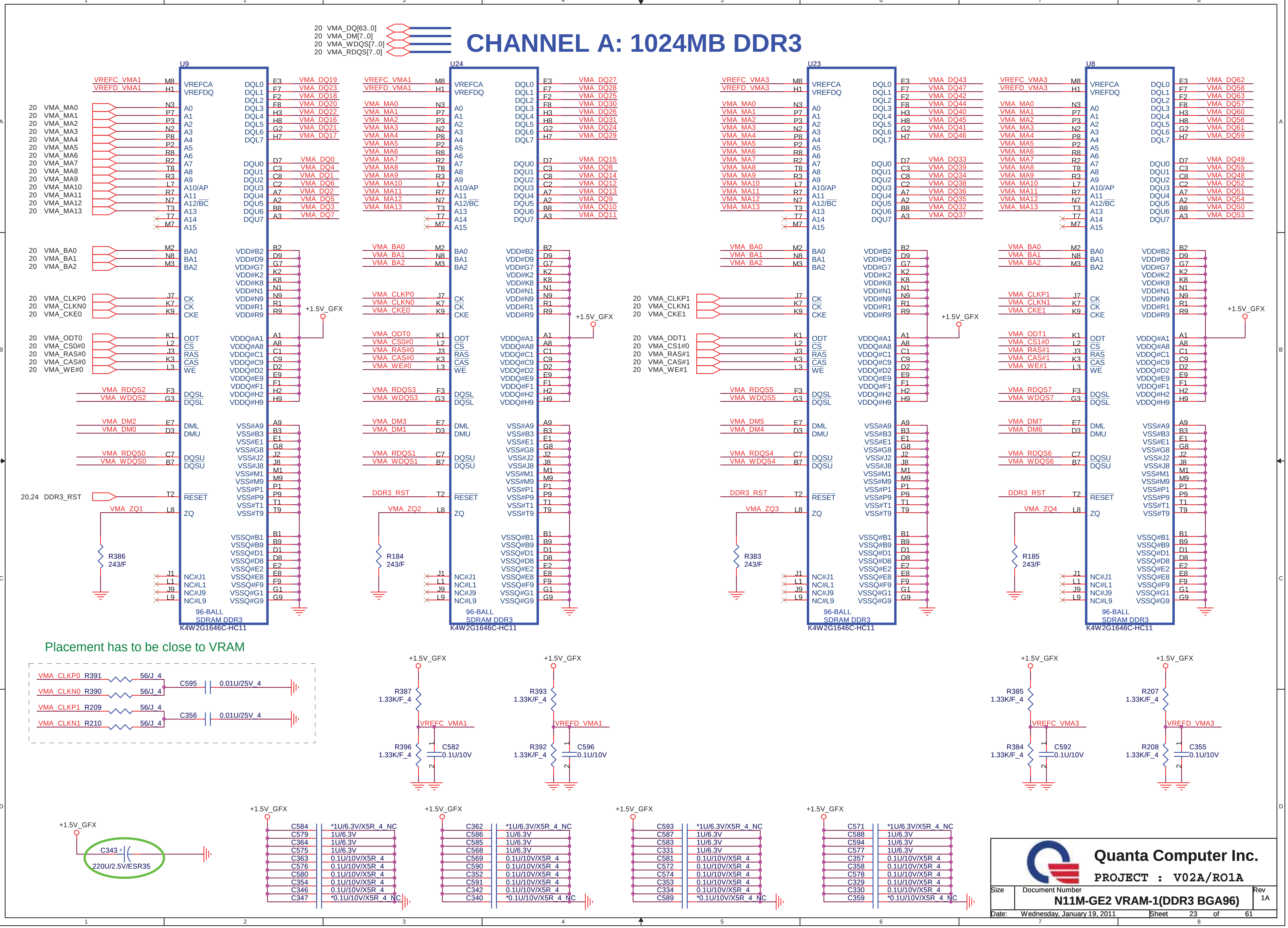
PROJECT : V02A/R01A

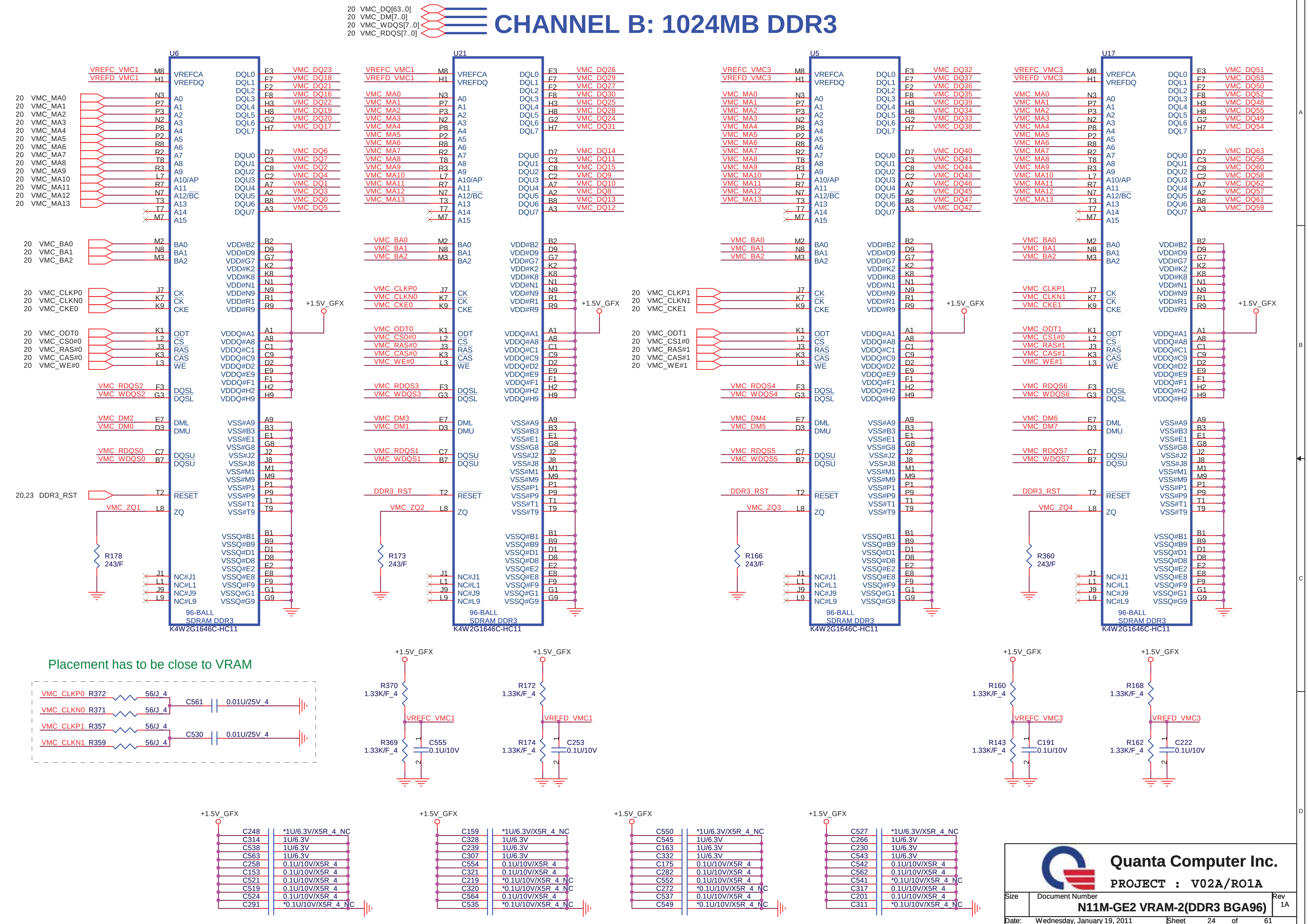
Size	Document Number	Rev
	Madison_DP_POWER	1A

Date: Wednesday, January 19, 2011 Sheet 22 of 61

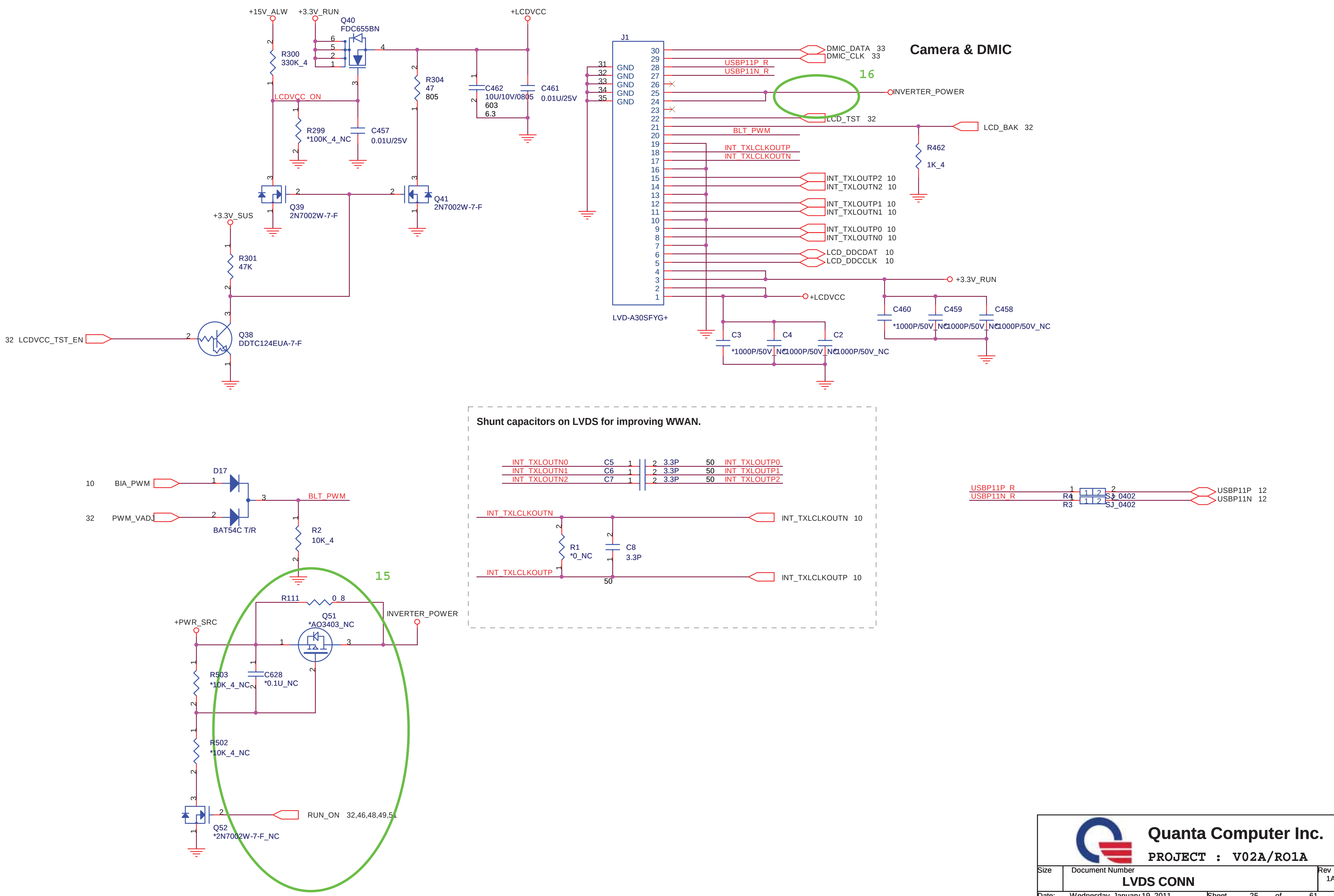


CHANNEL A: 1024MB DDR3
20 VMA_DQ[63..0]
20 VMA_DM[7..0]
20 VMA_WDQS[7..0]
20 VMA_RDQS[7..0]
U9
U24
U23
U8
96-BALL SDRAM DDR3
K4W2G1646C-HC11
VREFCA
VREFDQ
RESET
ZQ
+1.5V_GFX
R386 243/F
R184 243/F
R383 243/F
R185 243/F
Placement has to be close to VRAM
VMA_CLKP0 R391 56/J_4
VMA_CLKN0 R390 56/J_4
VMA_CLKP1 R209 56/J_4
VMA_CLKN1 R210 56/J_4
C595 0.01U/25V_4
C356 0.01U/25V_4
R387 1.33K/F_4
R396 1.33K/F_4
C582 0.1U/10V
VREFC_VMA1
R393 1.33K/F_4
R392 1.33K/F_4
C596 0.1U/10V
VREFD_VMA1
R385 1.33K/F_4
R384 1.33K/F_4
C592 0.1U/10V
VREFC_VMA3
R207 1.33K/F_4
R208 1.33K/F_4
C355 0.1U/10V
VREFD_VMA3
C343 220U/2.5V/ESR35
Quanta Computer Inc.
PROJECT : V02A/R01A
Size
Document Number
N11M-GE2 VRAM-1(DDR3 BGA96)
Rev 1A
Date: Wednesday, January 19, 2011
Sheet 23 of 61

CHANNEL B: 1024MB DDR3



Quanta Computer Inc.	
PROJECT : V02A/RO1A	
Size	Document Number: N11M-GE2 VRAM-2(DDR3 BGA96)	Rev 1A
Date: Wednesday, January 19, 2011	Sheet 24 of 61

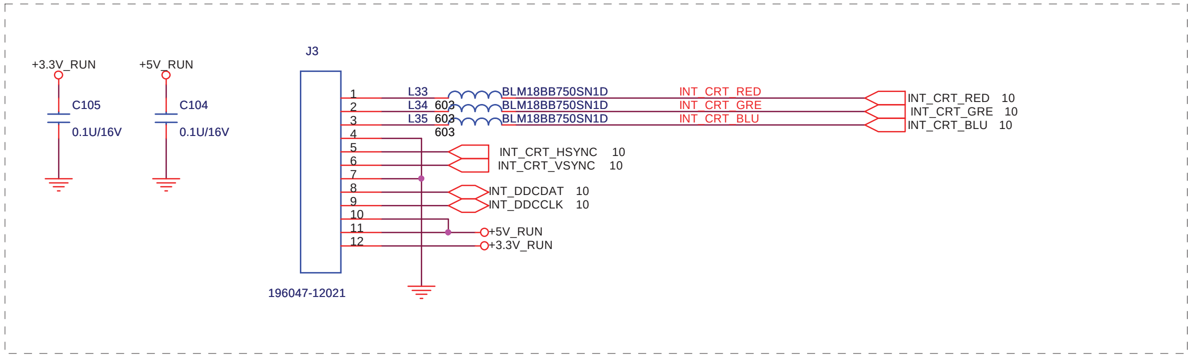


Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	LVDS CONN	1A

Date: Wednesday, January 19, 2011 Sheet 25 of 61

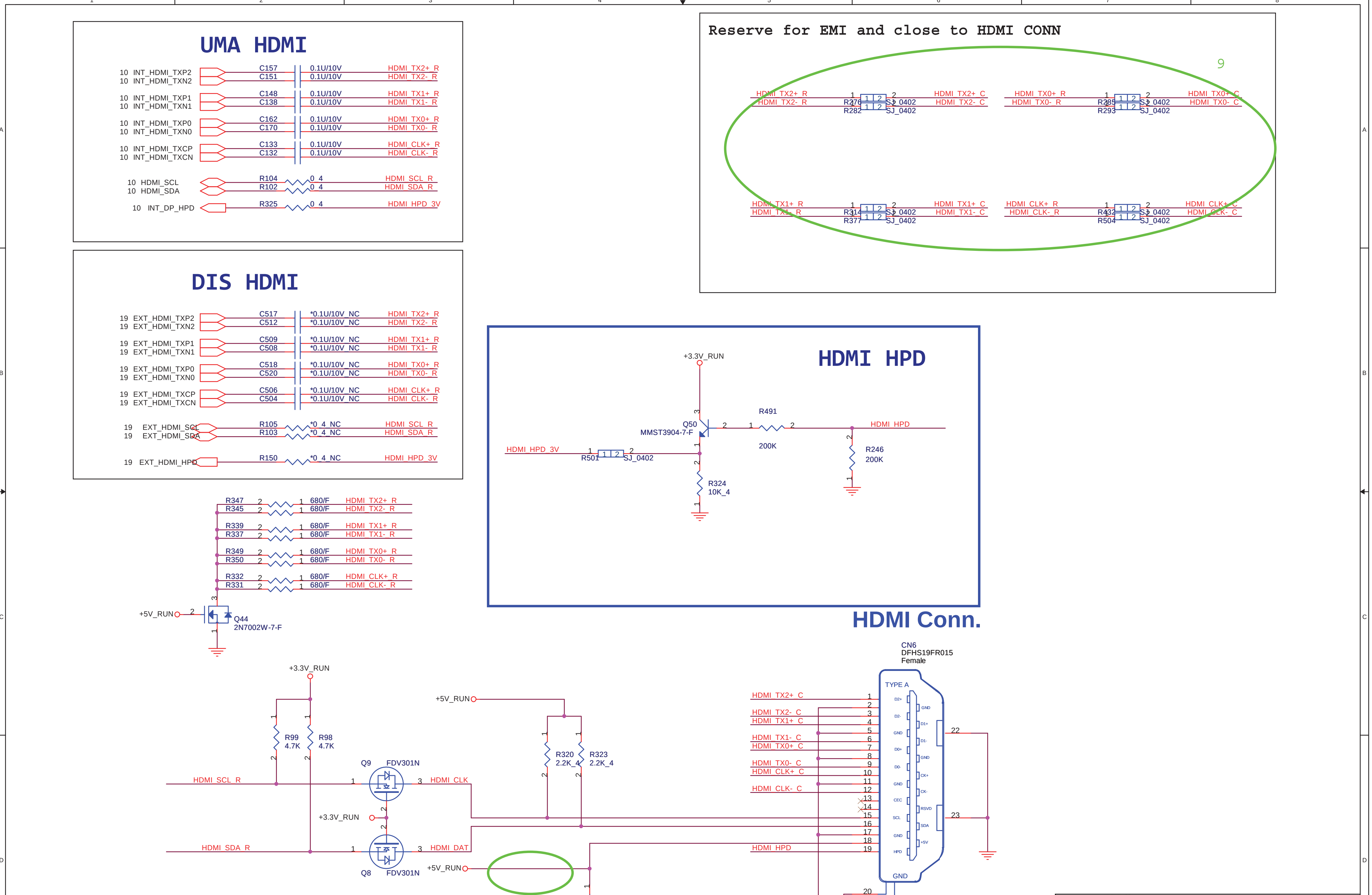


Quanta Computer Inc.

PROJECT : V02A/RO1A

Size	Document Number	Rev
	BLANK	1A

Date: Wednesday, January 19, 2011 | Sheet 26 of 61



Quanta Computer Inc.

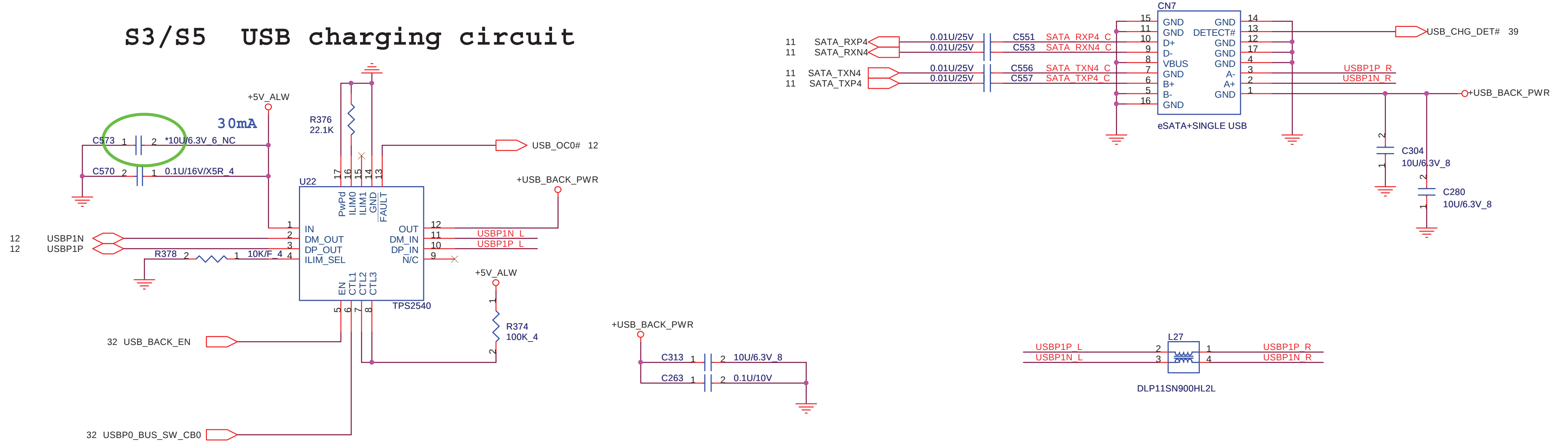
PROJECT : V02A/R01A

Size	Document Number	Rev
	HDMI CONN	1A

Date: Wednesday, January 19, 2011 Sheet 27 of 61

ESATA + USB Conn + Power share

S3/S5 USB charging circuit



USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

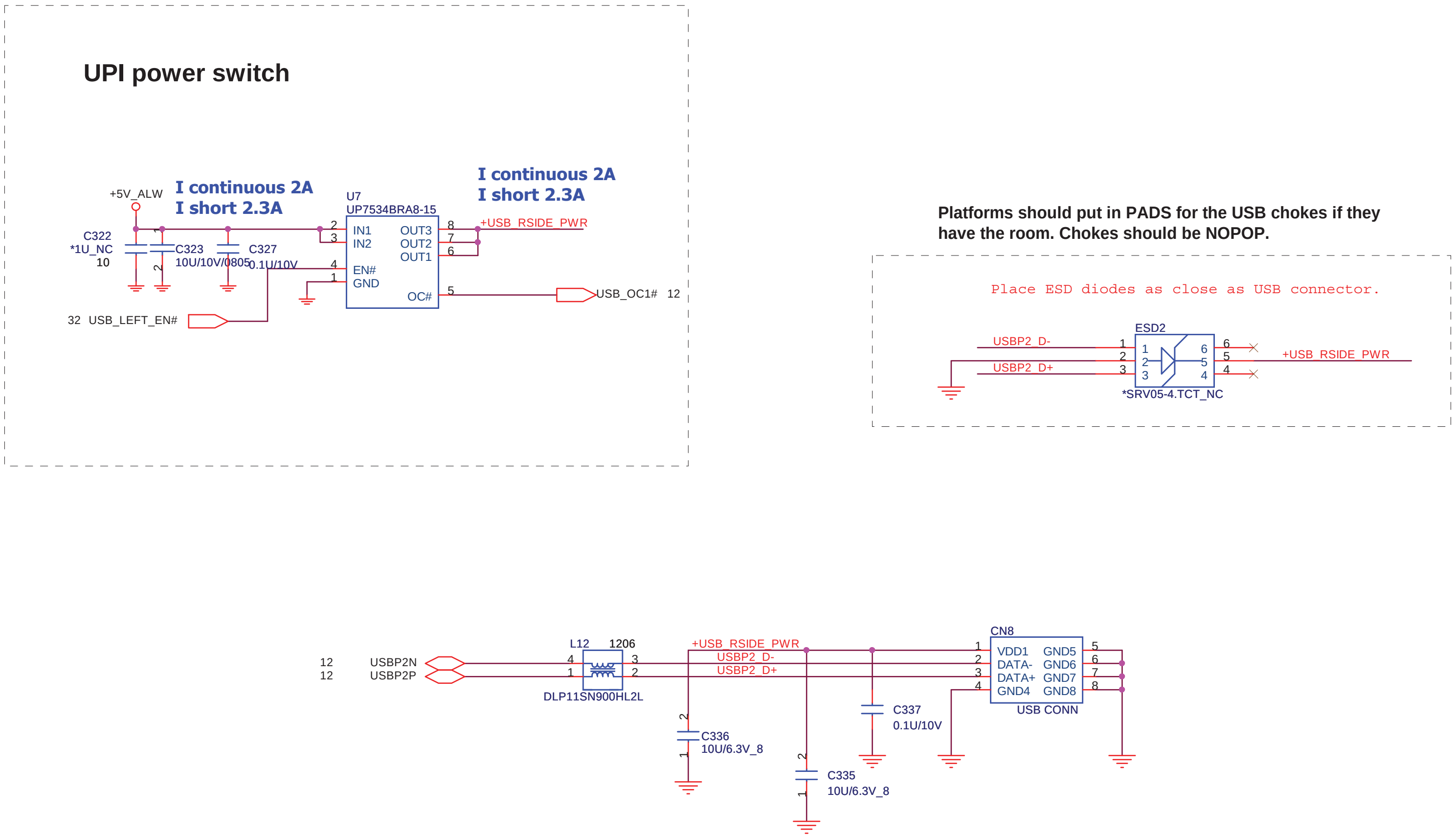
	R8224	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now

Quanta Computer Inc.

PROJECT : V02A/RO1A

Size	Document Number	Rev
	PUSB / ESATA	1A

Date: Wednesday, January 19, 2011 Sheet 28 of 61



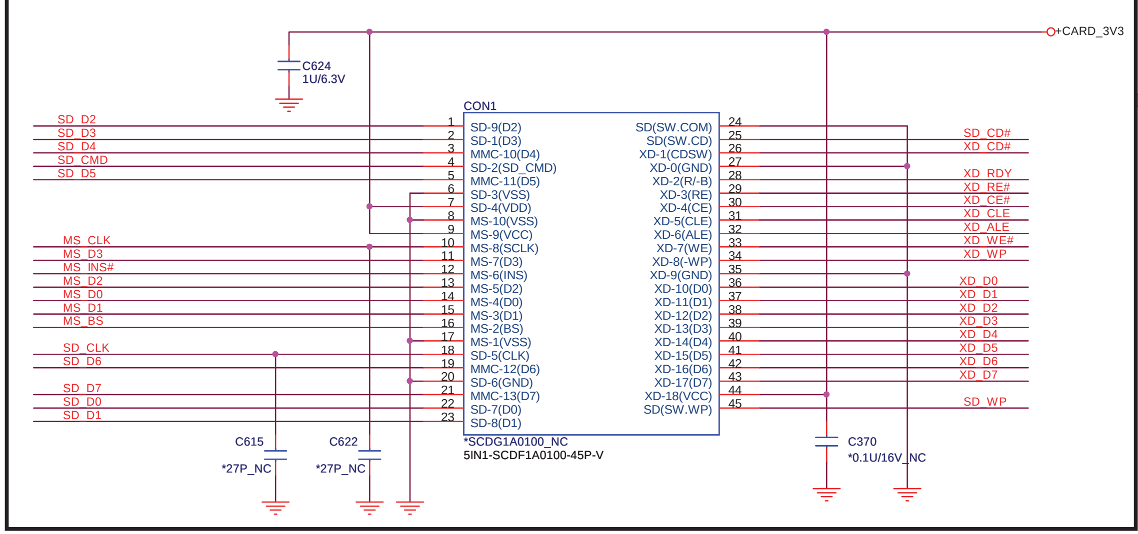
Quanta Computer Inc.

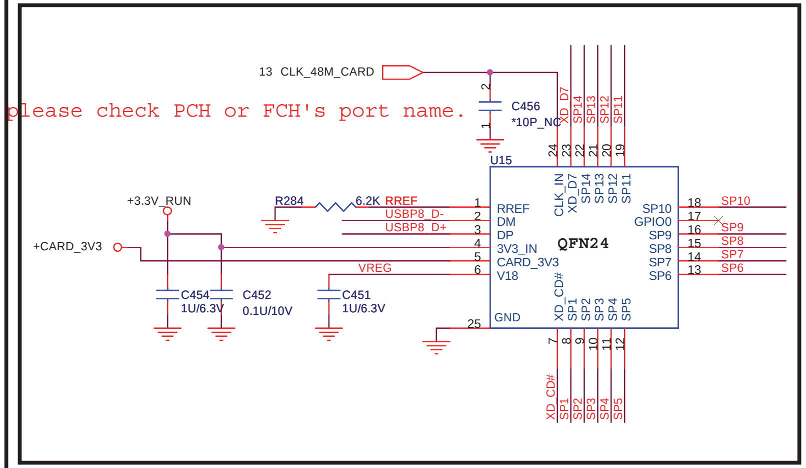
PROJECT : V02A/RO1A

Size	Document Number	Rev
	USB 2.0	1A

Date: Wednesday, January 19, 2011 | Sheet 29 of 61

Inspiron

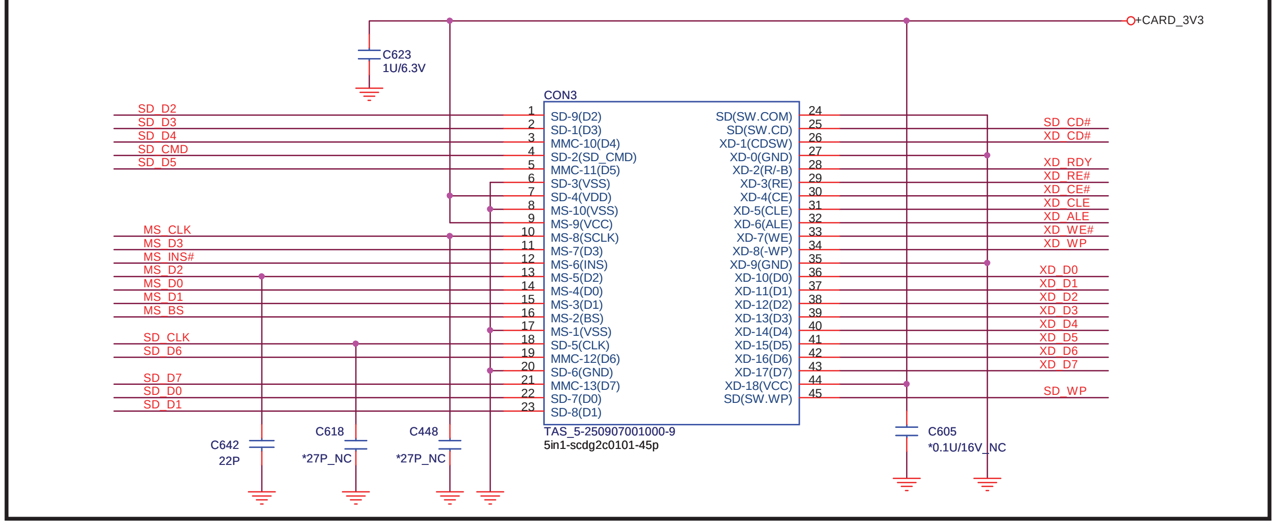


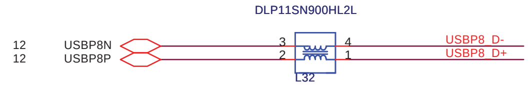


SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS

Share Pin

VOSTOR





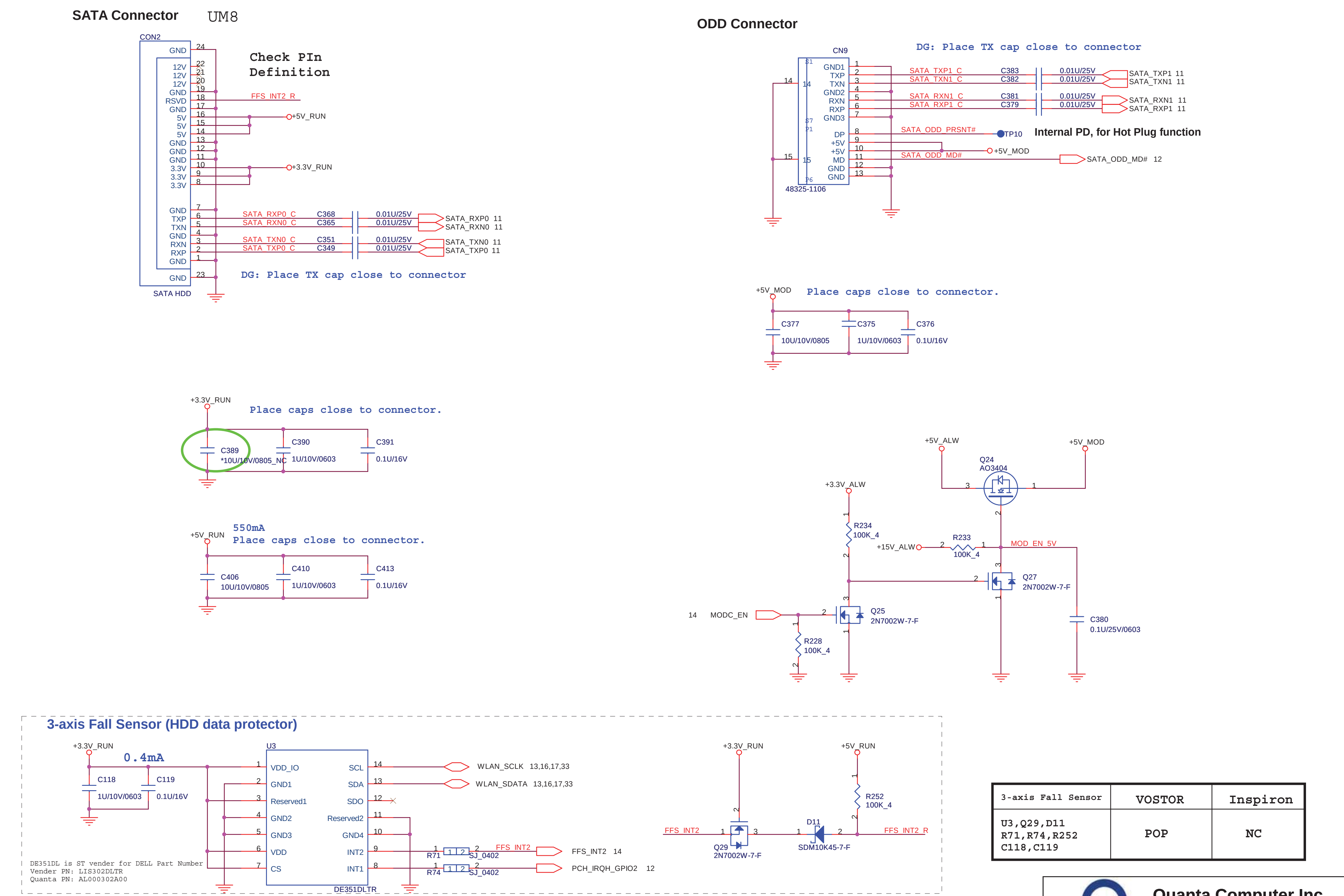
Cardreader	POP	NC
Inspiron	CON1	CON3
VOSTOR	CON3	CON1

Quanta Computer Inc.

PROJECT : V02A/R01A

Size | Document Number: Cardreader (RTS5128) | Rev 1A

Date: Wednesday, January 19, 2011 | Sheet 30 of 61



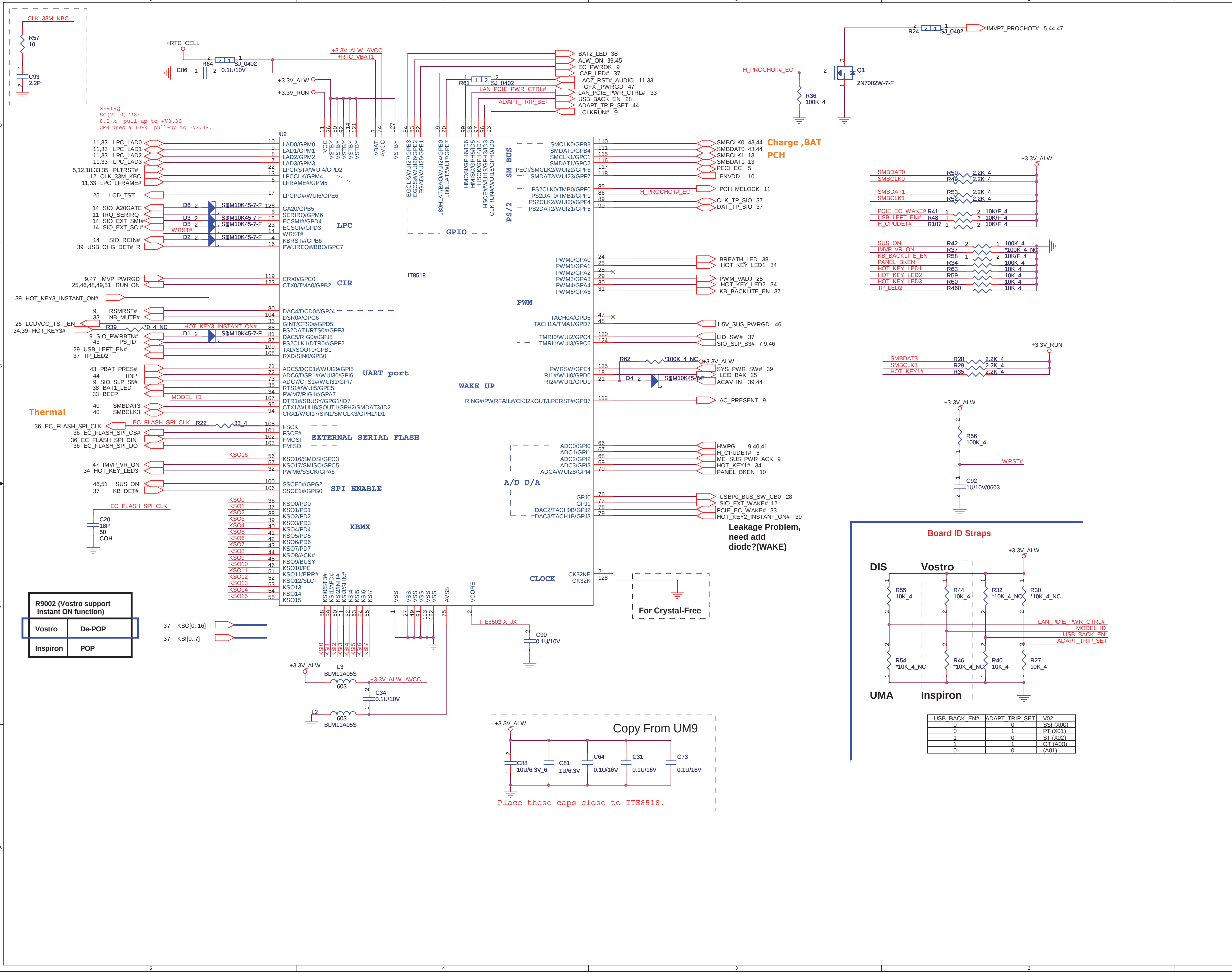
3-axis Fall Sensor	VOSTOR	Inspiron
U3,Q29,D11 R71,R74,R252 C118,C119	POP	NC

Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	SATA HDD/ODD	1A

Date: Wednesday, January 19, 2011 Sheet 31 of 61



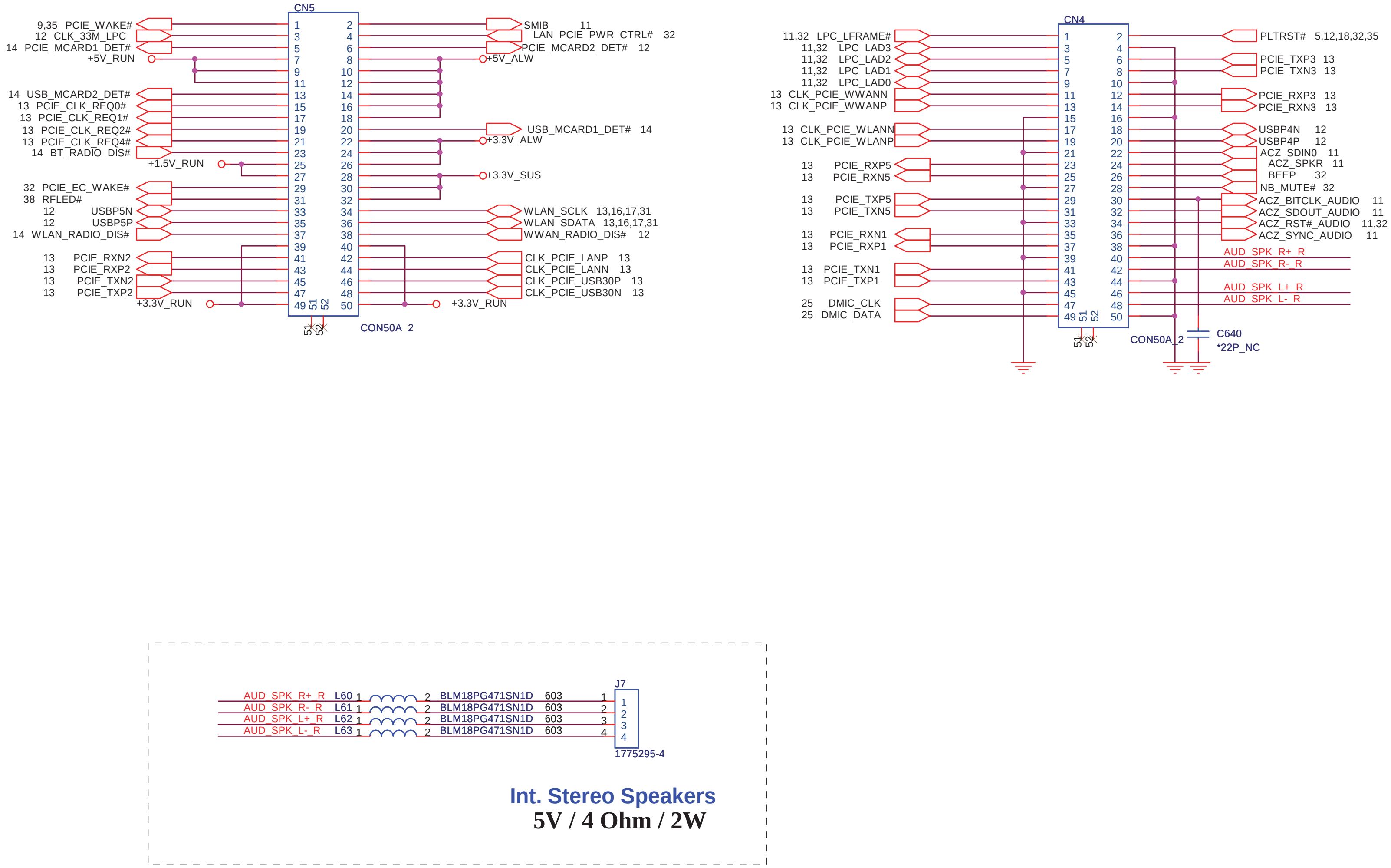
USB_BACK_EN#	ADAPT_TRIP_SET	V02
0	0	SSI (X00)
0	1	PT (X01)
1	0	ST (X02)
1	1	QT (A00)
0	0	(A01)

Quanta Computer Inc.

PROJECT : V02A/R01A

Size | Document Number: SIO (ITE8518E) | Rev 1A

Date: Wednesday, January 19, 2011 | Sheet 32 of 61

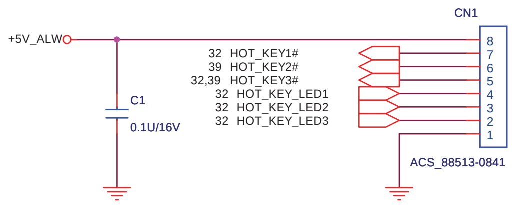


Quanta Computer Inc.

PROJECT : V02A/RO1A

Size	Document Number	Rev
	SIO (ITE8518E)	1A

Date: Wednesday, January 19, 2011 — Sheet 33 of 61



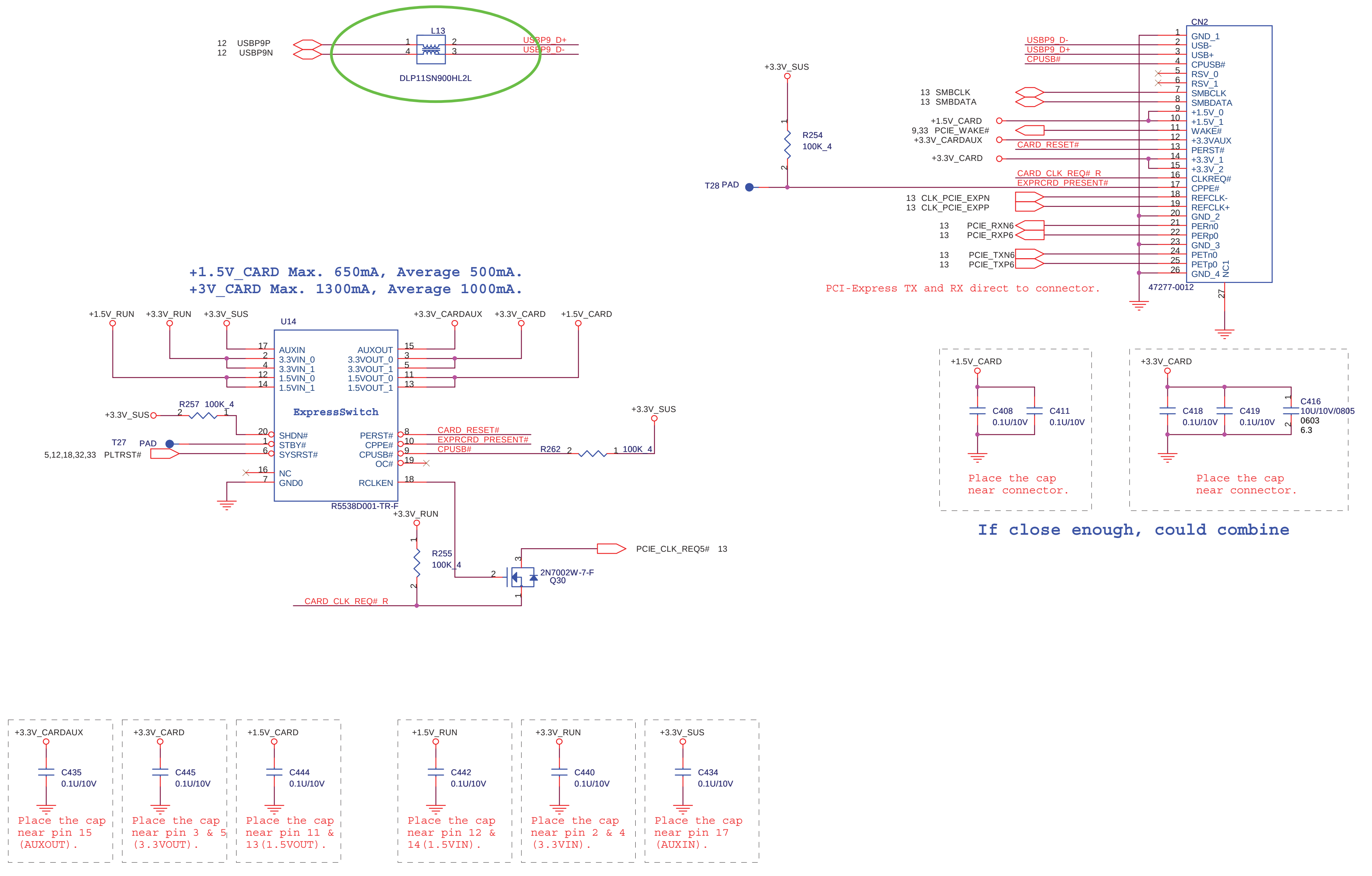
HOTKEY CON

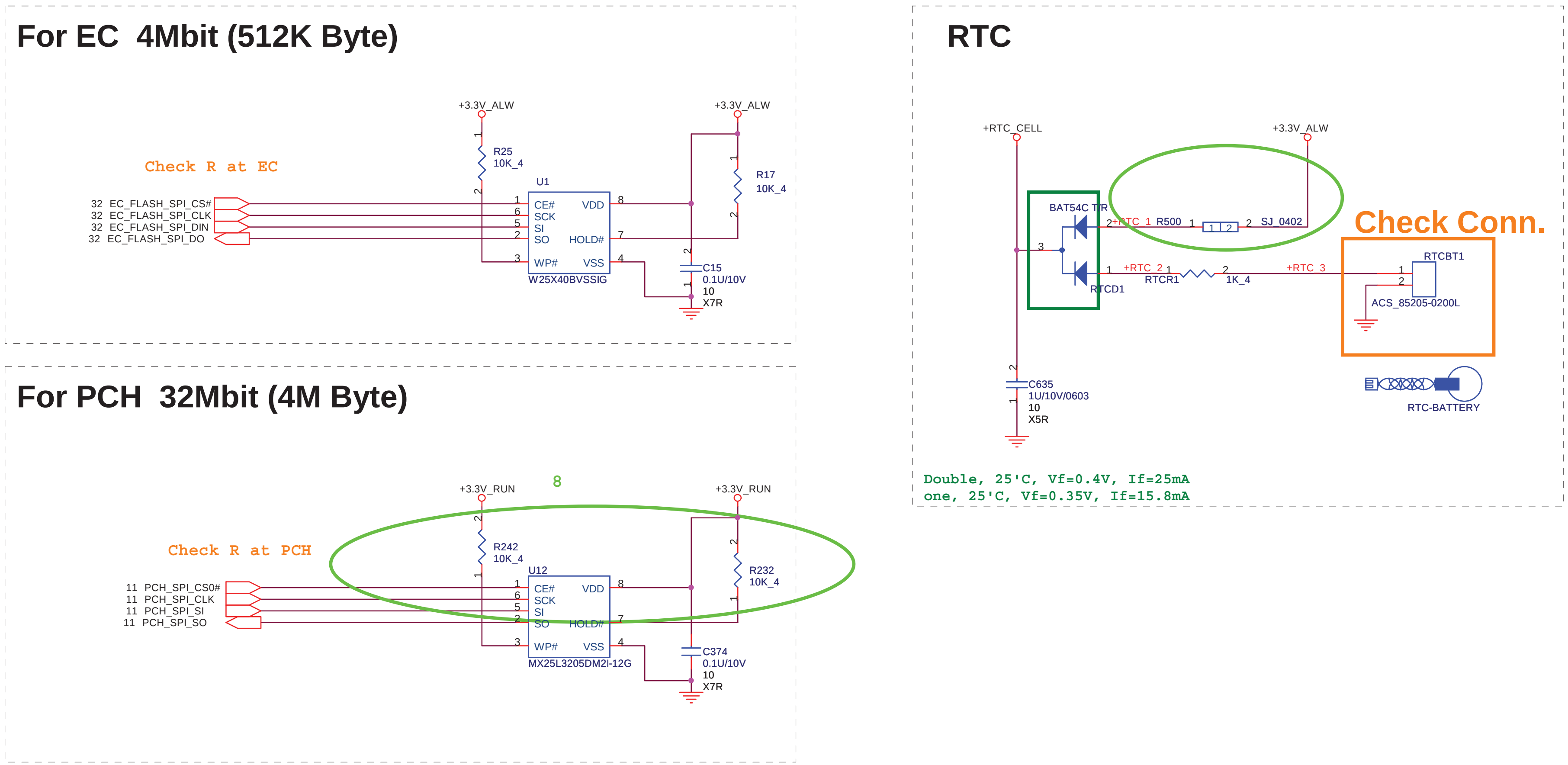
Quanta Computer Inc.

PROJECT : V02A/RO1A

Size	Document Number	Rev
	MINI-PCI (WLAN/WPAN)	1A
Date: Wednesday, January 19, 2011	Sheet 34 of 61	

Express Card





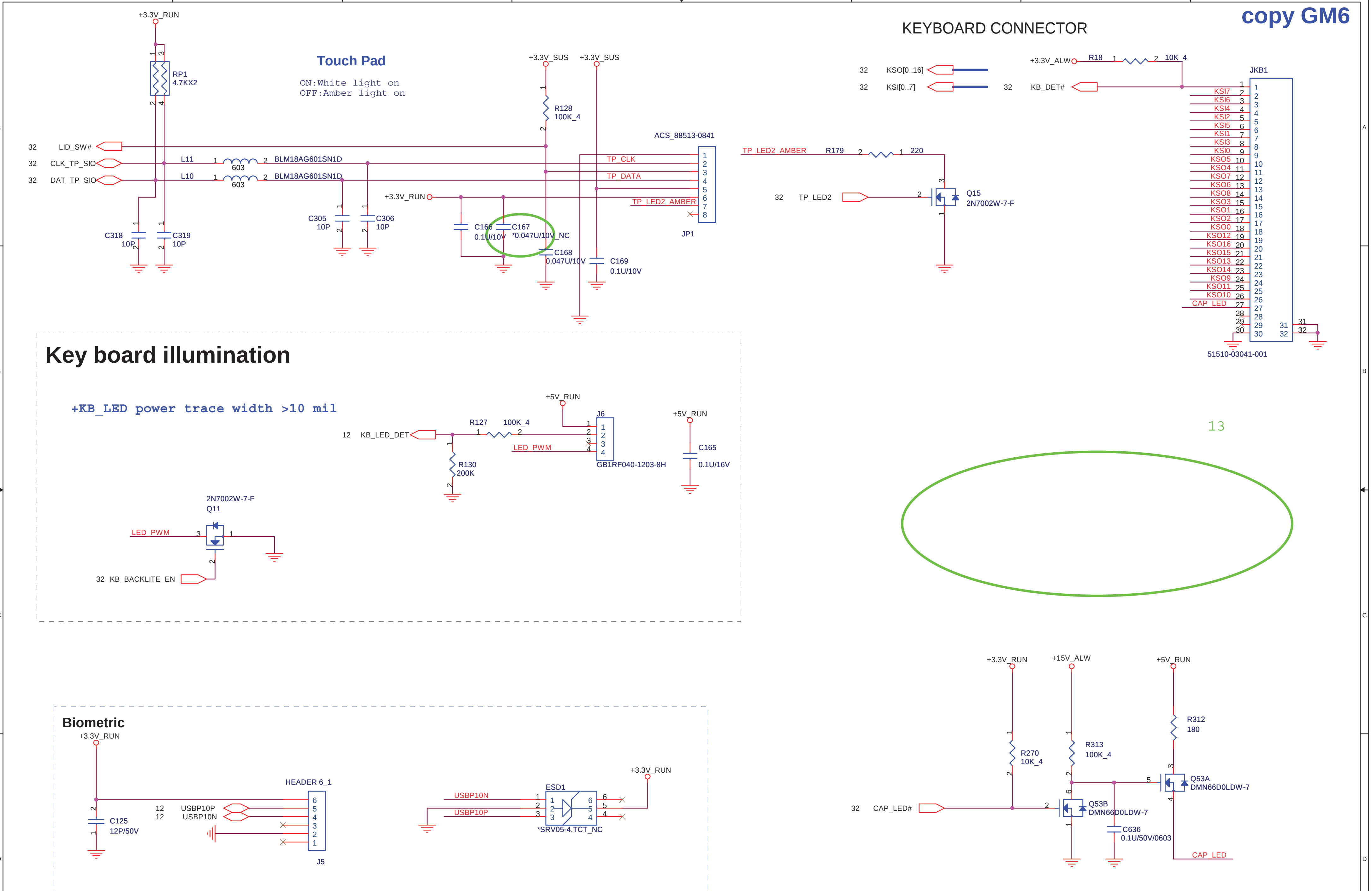
Quanta Computer Inc.

PROJECT : V02A/RO1A

Size	Document Number	Rev
	FLASH / RTC	1A

Date: Wednesday, January 19, 2011 Sheet 36 of 61

copy GM6

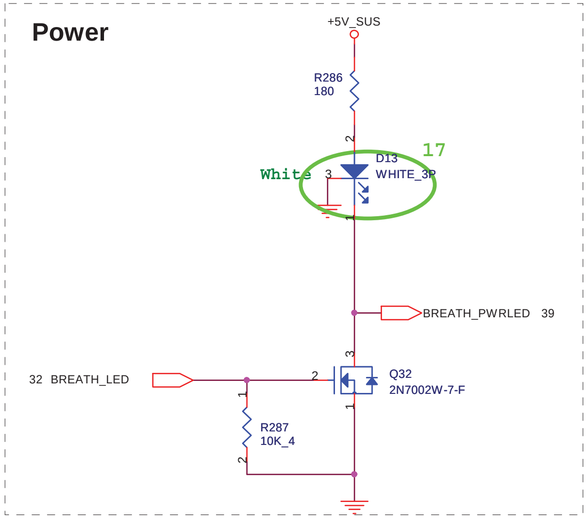


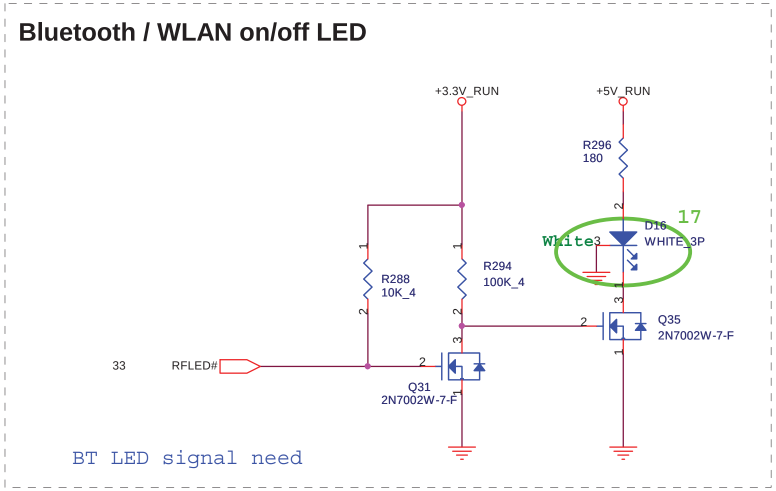
Quanta Computer Inc.

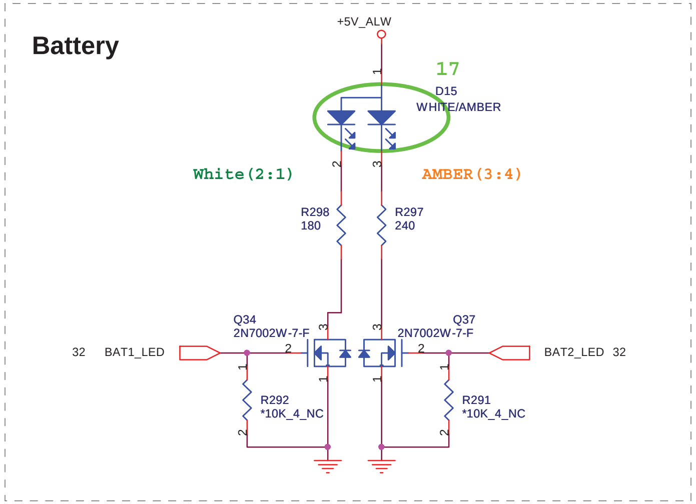
PROJECT : V02A/R01A

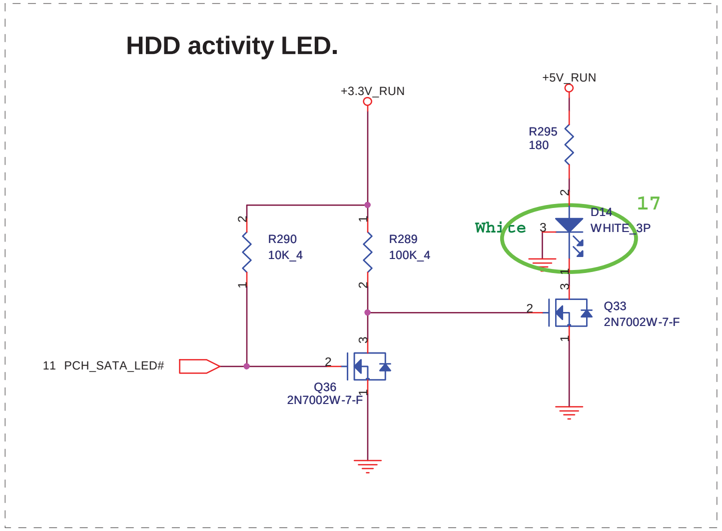
Size	Document Number	Rev
	TP / KB	1A

Date: Wednesday, January 19, 2011 | Sheet 37 of 61









VOSTOR	R286,R295,R296,R298	R297
	180 ohm PN:CS11802JB15	240 ohm PN:CS12402JB13
Inspiron	R286,R295,R296,R298	R297
	390 ohm PN:CS13902JB14	330 ohm PN:CS13302JB21

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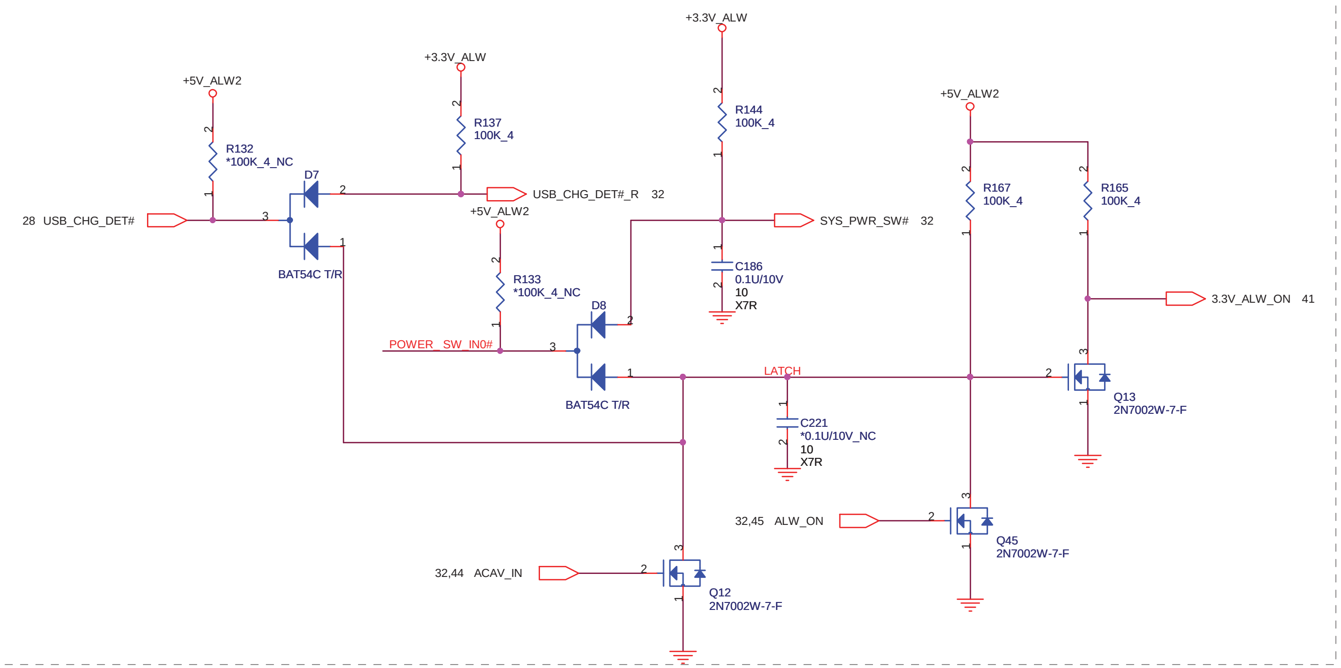
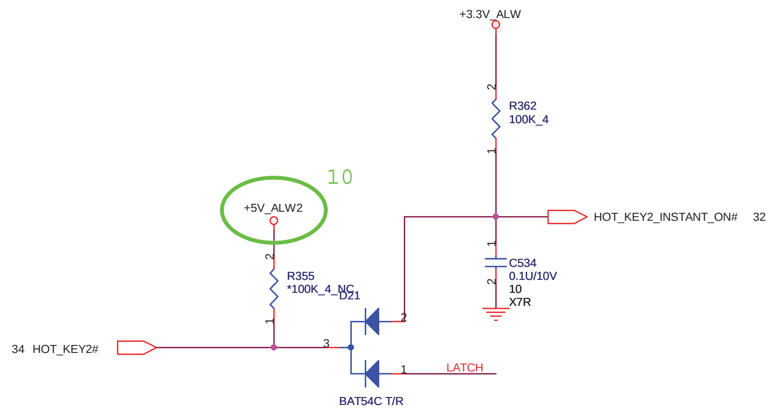
PROJECT : V02A/RO1A

Size	Document Number	Rev
	LED	1A

Date: Wednesday, January 19, 2011 Sheet 38 of 61

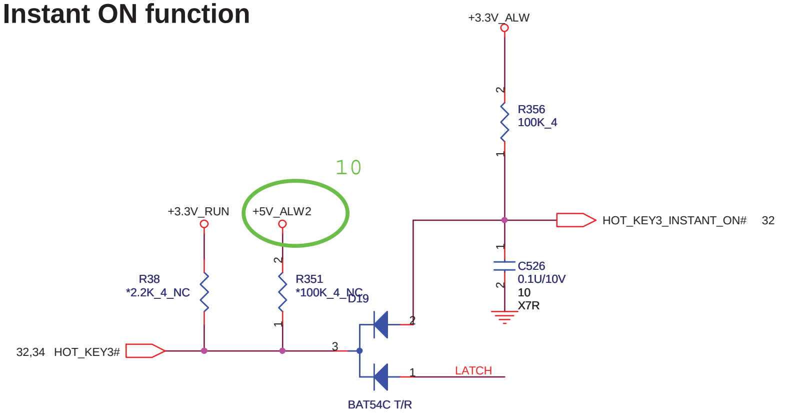
3VALW ON POWER LOGIC



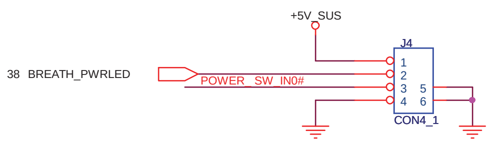


Vostro pop D19,C526,R356 depop R38,R39
Inspiron depop D19,C526,R356 pop R38,R39

Instant ON function

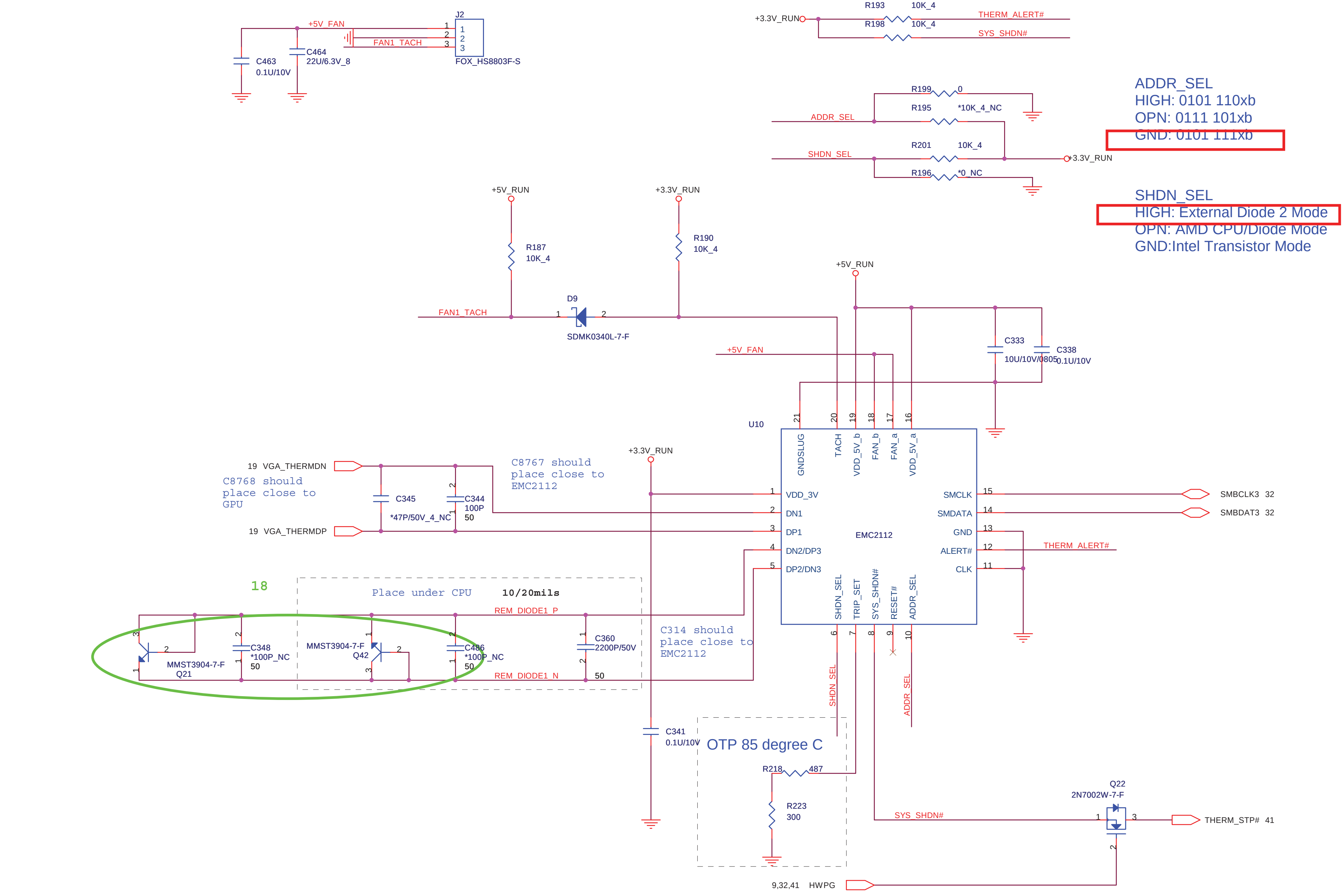


PWR button board



Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	PWR SW/LED	1A
Date: Wednesday, January 19, 2011	Sheet 39 of 61	

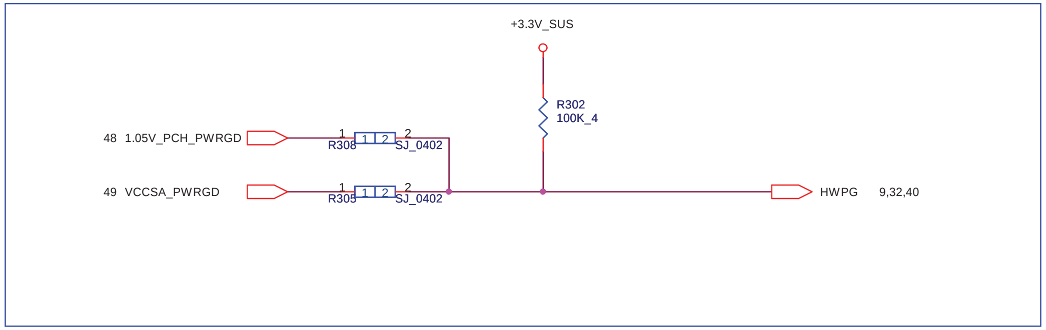


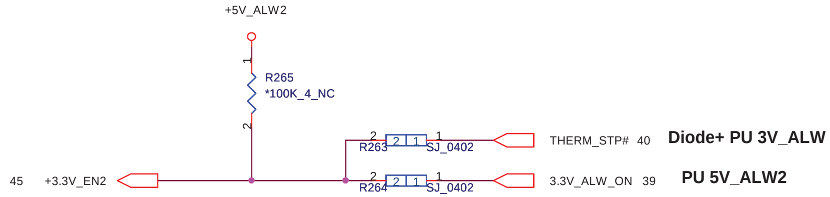
Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	FAN & THERMAL	1A

Date: Wednesday, January 19, 2011 Sheet 40 of 61



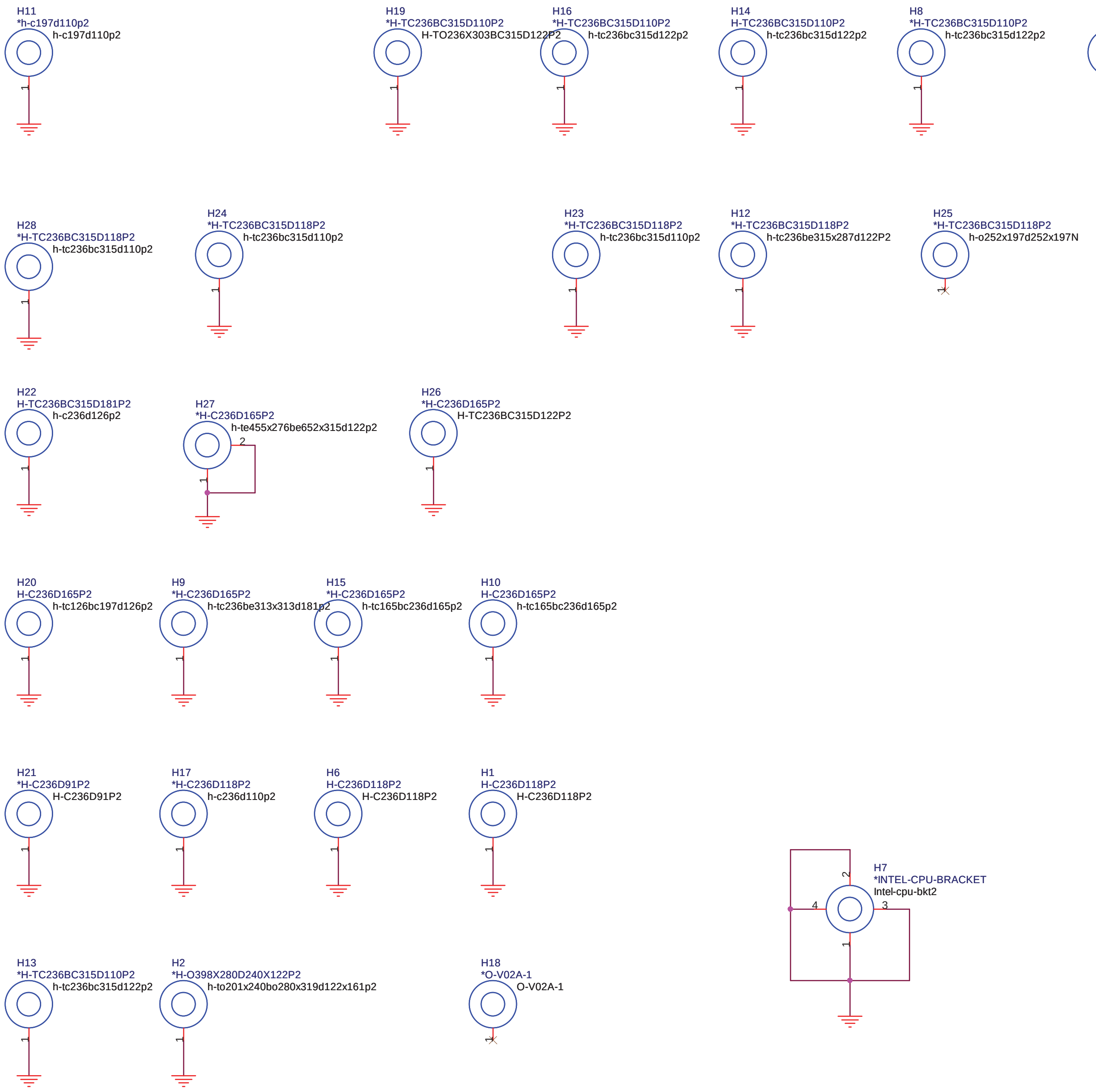


Quanta Computer Inc.

PROJECT : V02A/RO1A

Size	Document Number	Rev
	System Reset Circuit	1A

Date: Wednesday, January 19, 2011 Sheet 41 of 61

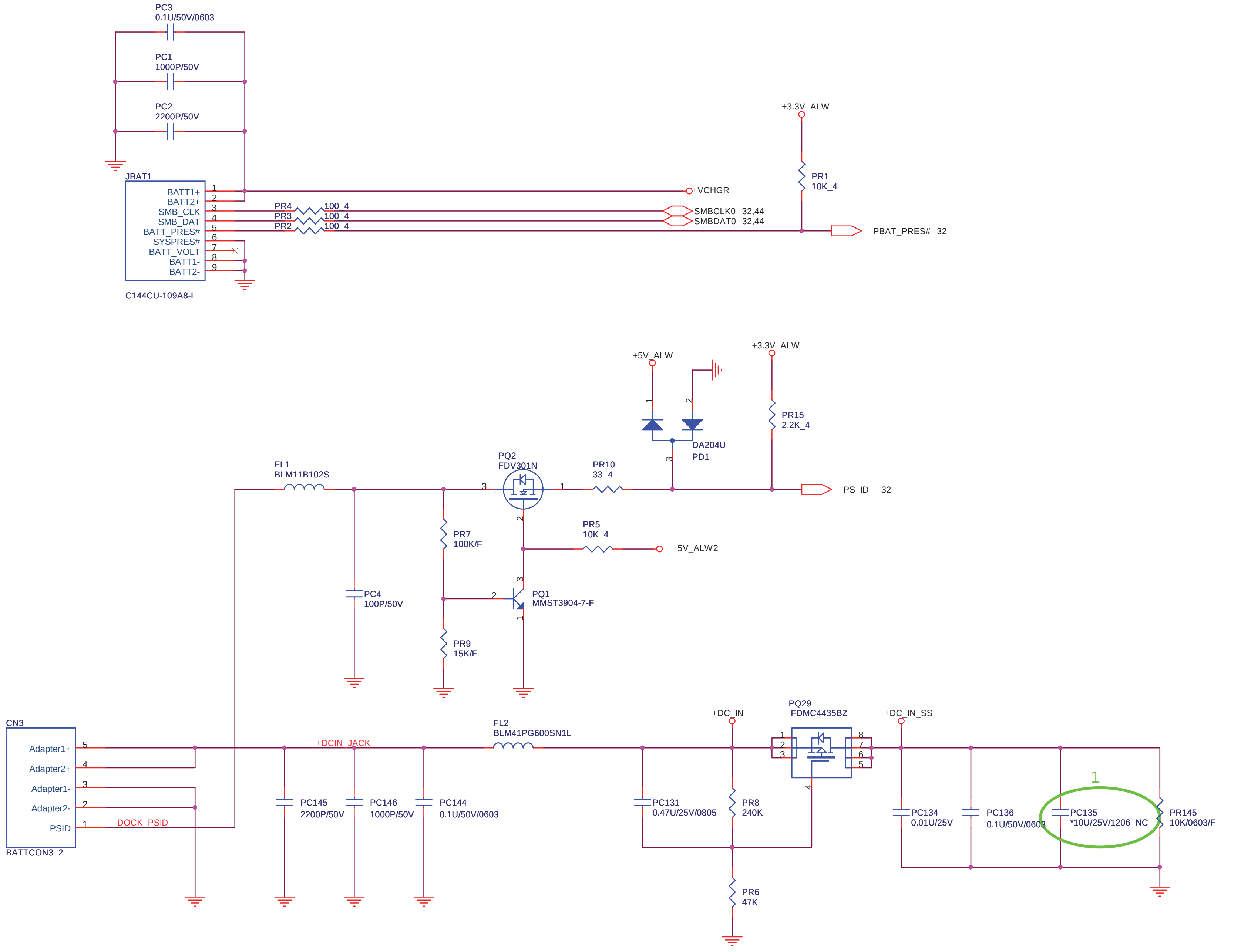


Quanta Computer Inc.

PROJECT : V02A/RO1A

Size	Document Number	Rev
	SCREW PAD	1A

Date: Wednesday, January 19, 2011 Sheet 42 of 61

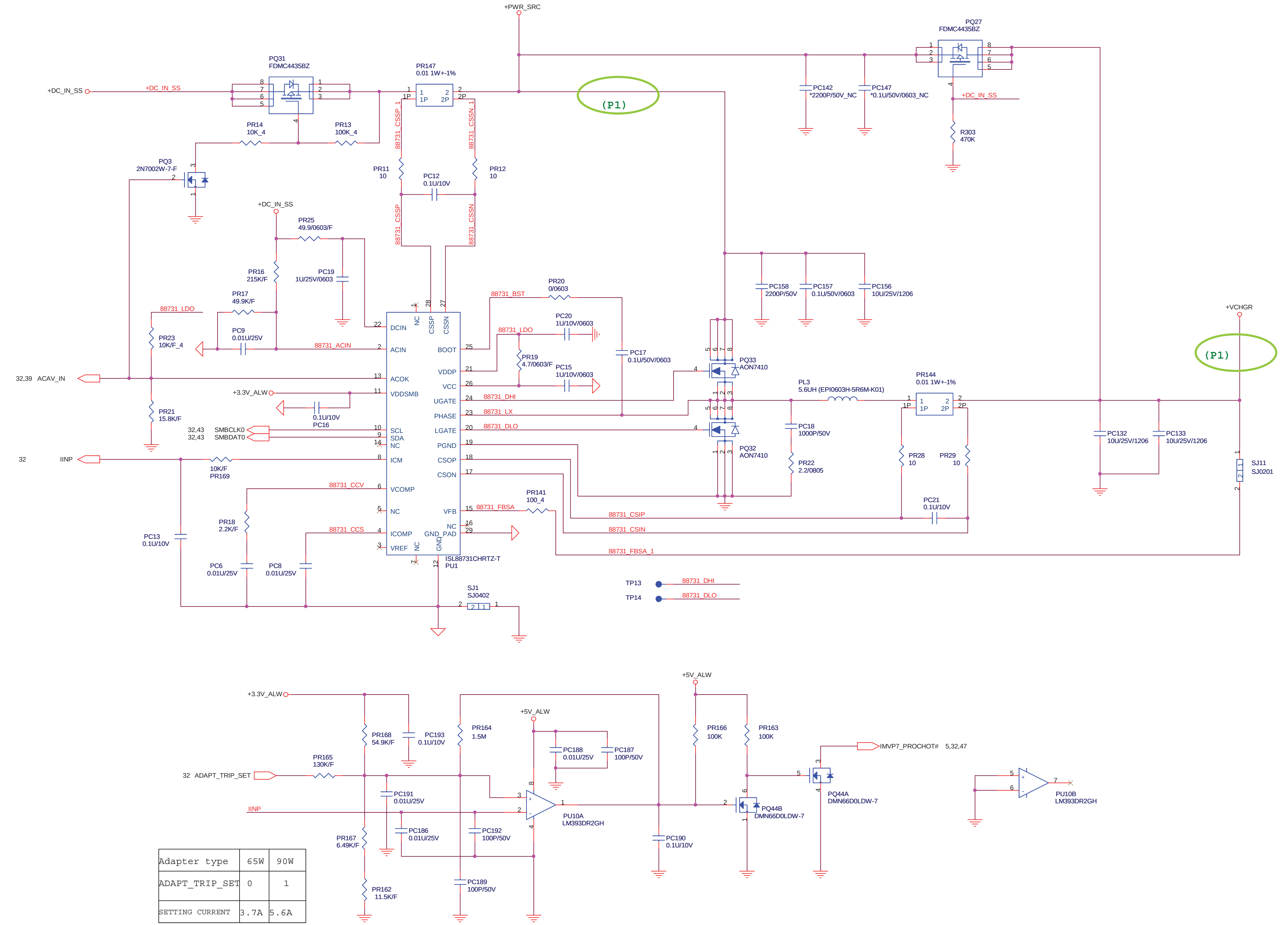


Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	DC IN / BATT	1A

Date: Wednesday, January 19, 2011 Sheet 43 of 61



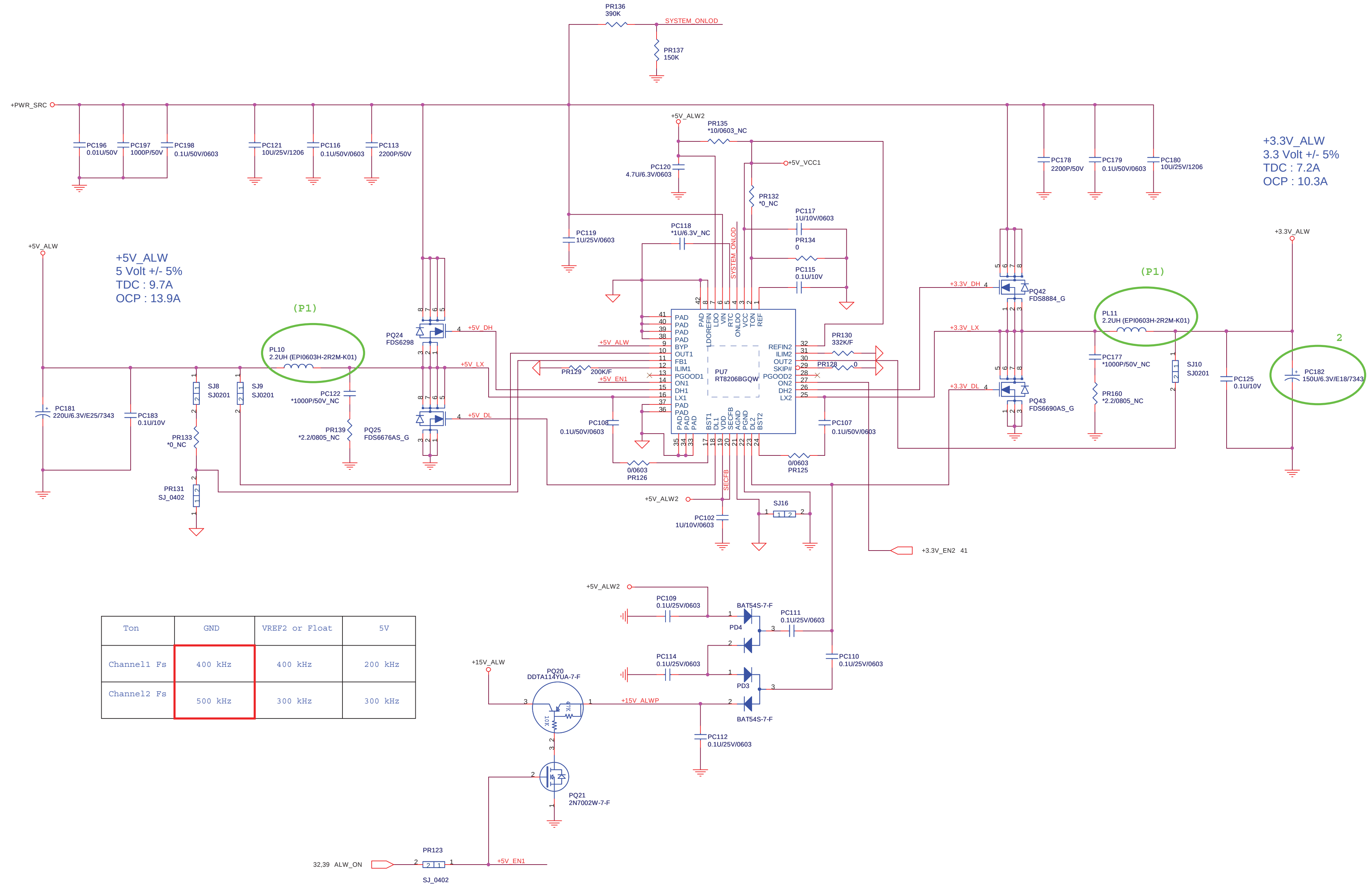
Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A

Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	Charger (BQ24765RUVR)	1A

Date: Wednesday, January 19, 2011 Sheet 44 of 61

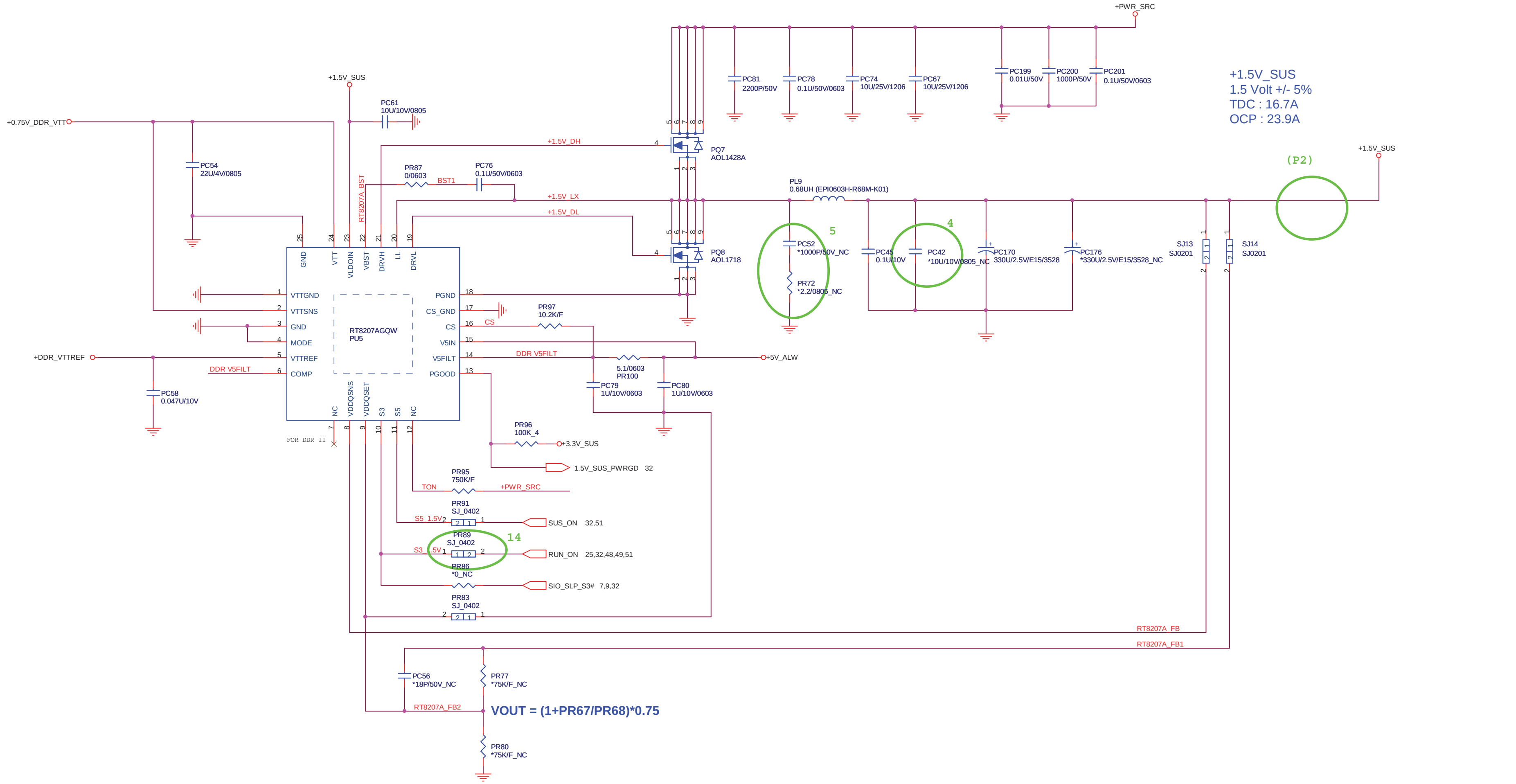


Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz

Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	3.3V_ALW / 5V_ALW (TPS51427ARHBR)	1A
Date:	Wednesday, January 19, 2011	Sheet 45 of 61



VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

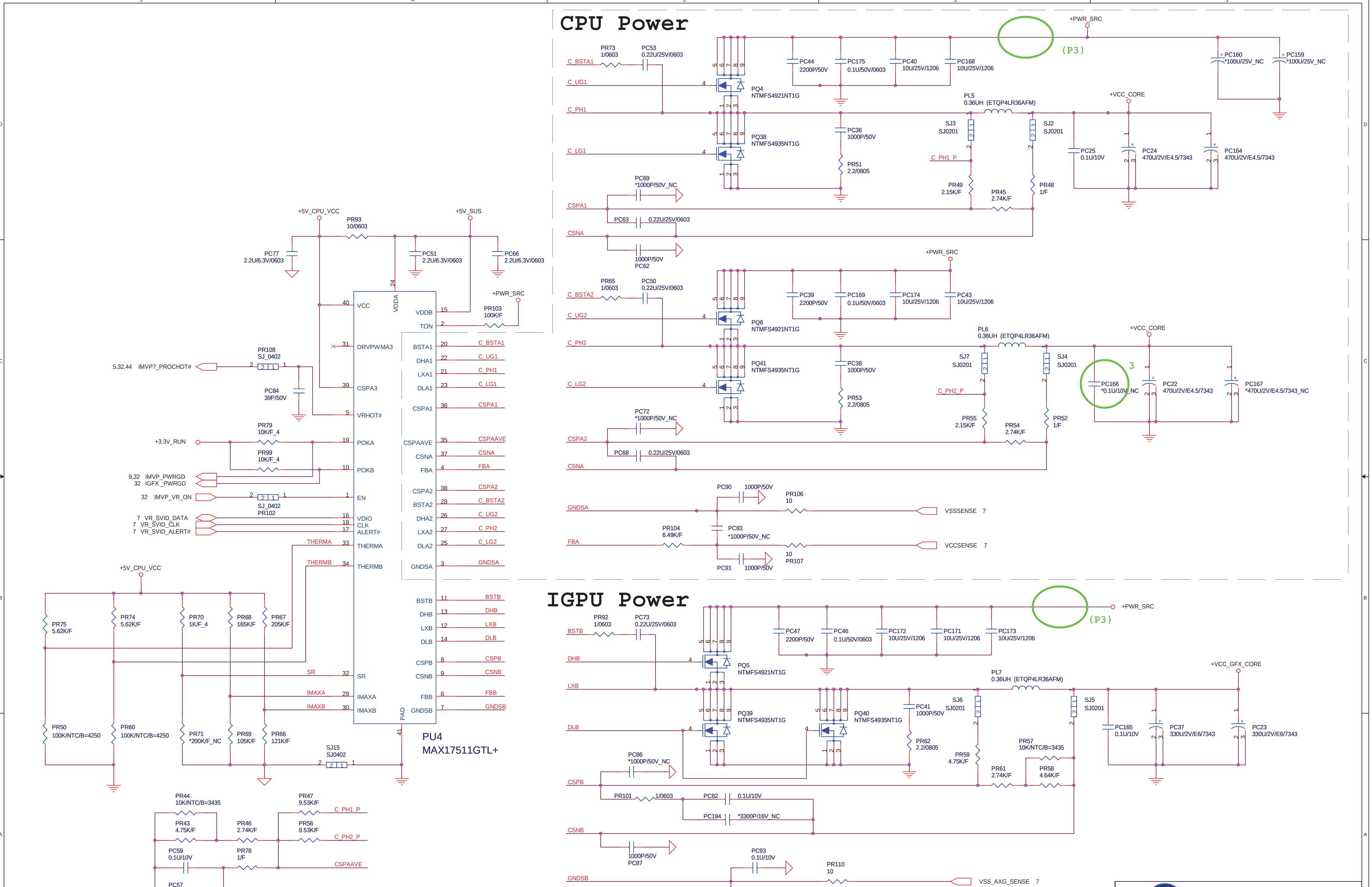
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Quanta Computer Inc.
PROJECT : V02A/R01A
Size | Document Number: 1.5_SUS/0.75_DDR_VTT (RT8207AGQW) | Rev 1A
Date: Wednesday, January 19, 2011 | Sheet 46 of 61

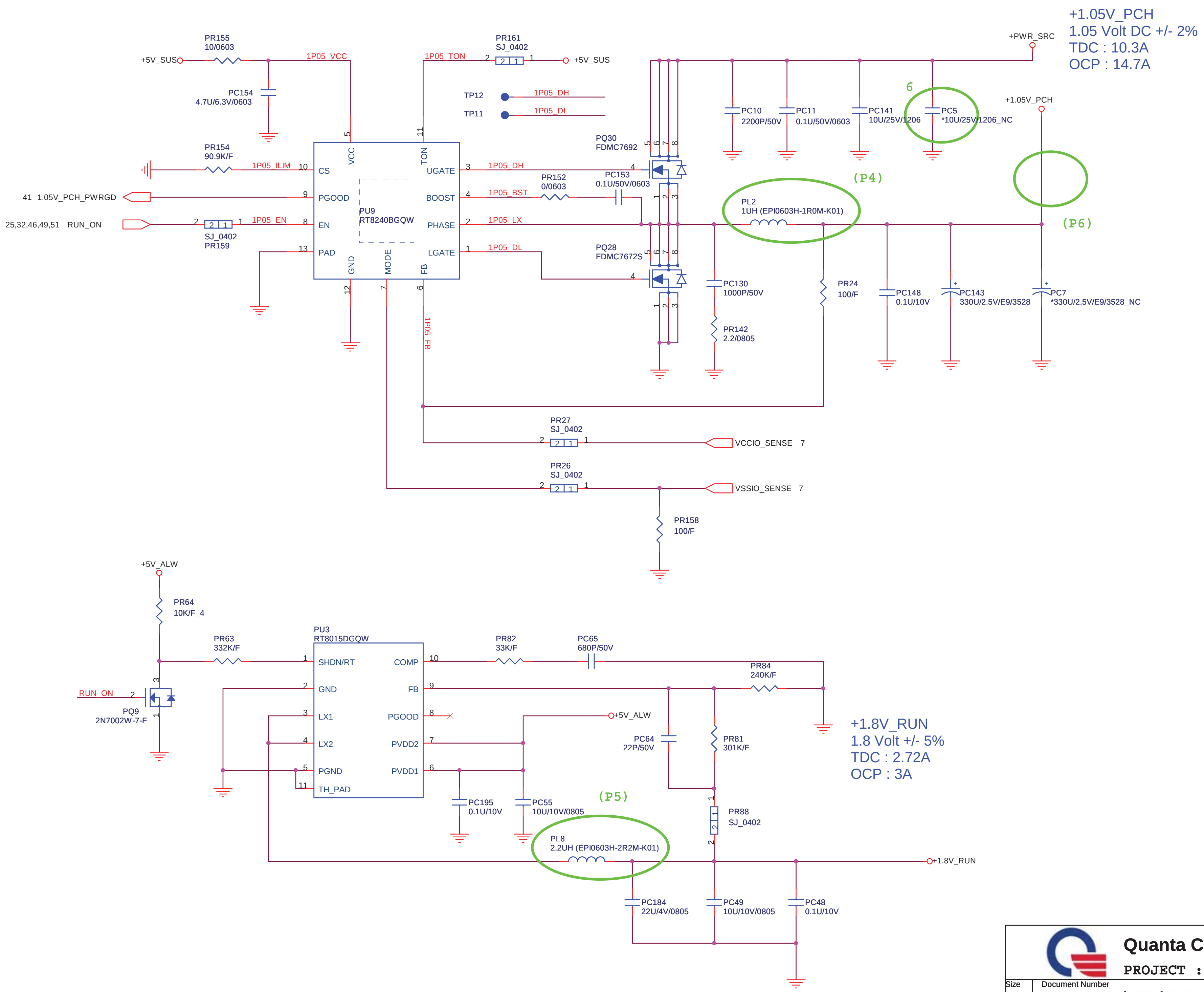


Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	CPU_CORE (MAX17511)	1A

Date: Wednesday, January 19, 2011 Sheet 47 of 61

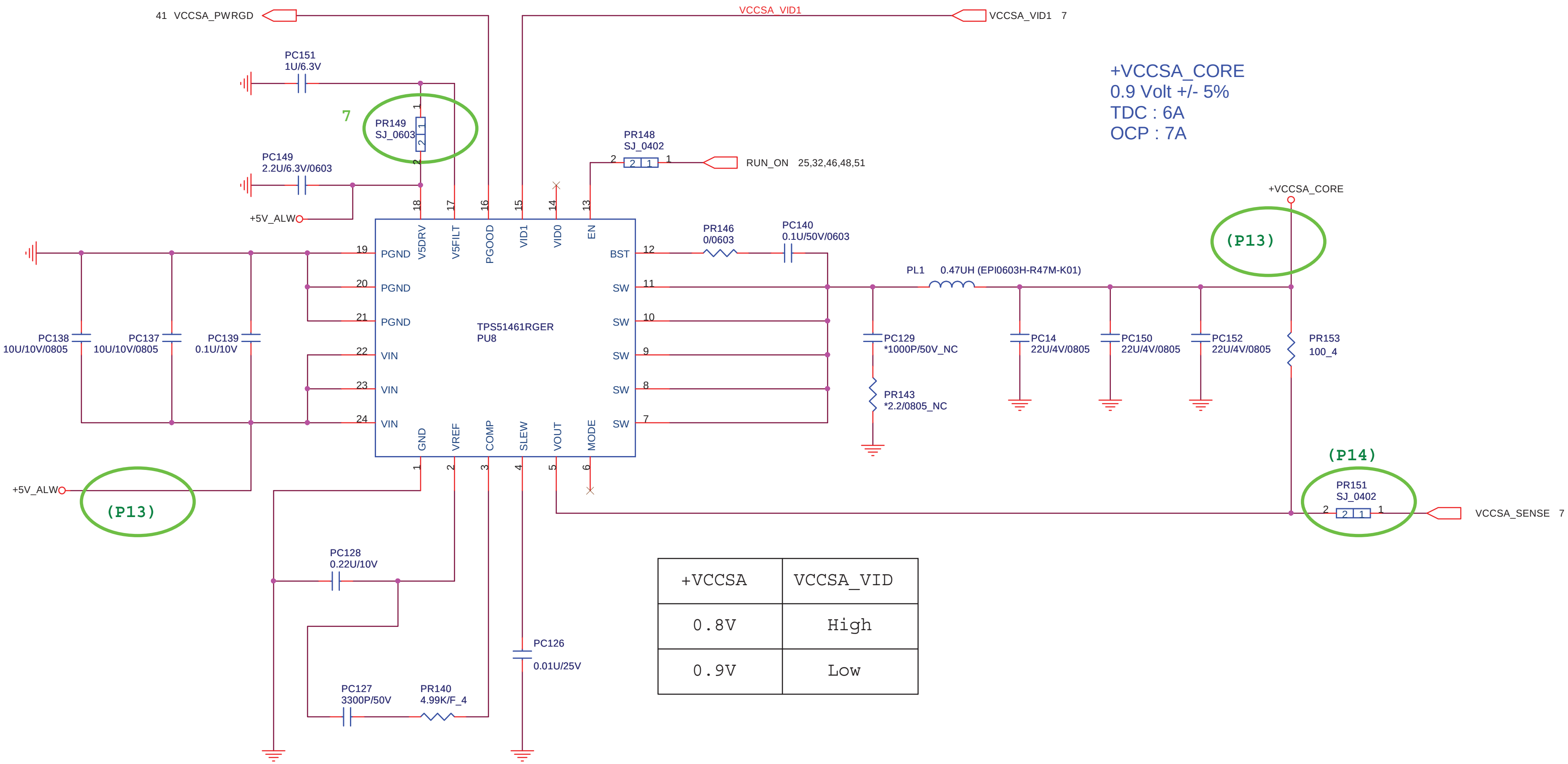


Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	+1.05V_PCH / VTT (TPS51218DSCR)	1A

Date: Wednesday, January 19, 2011 Sheet 48 of 61



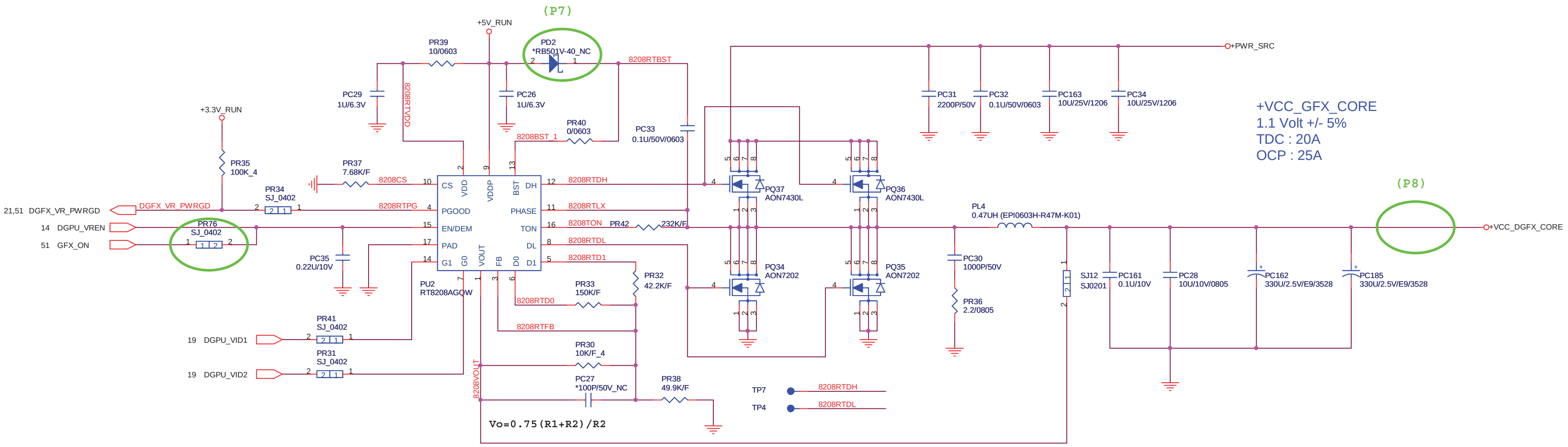
+VCCSA	VCCSA_VID
0.8V	High
0.9V	Low

Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	VCCSA (ISL95870A)	1A

Date: Wednesday, January 19, 2011 Sheet 49 of 61



Robson_XT

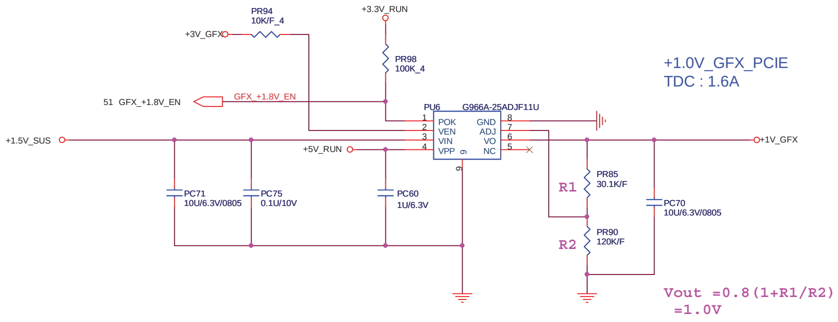
DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
HIGH	HIGH	1.12V
Setting		
Location	**Part No.**	**Value**
PR30	CS31002FB26	10K
PR38	CS34992FB10	49.9K
PR33	CS41502FB18	150K
PR32	CS34222FB00	44.2K

Whistler_LP

DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.85V
HIGH	LOW	0.9V
HIGH	HIGH	1.0V
Setting		
Location	**Part No.**	**Value**
PR30	CS31002FB26	10K
PR38	CS37502FB12	75K
PR33	CS41502FB18	150K
PR32	CS37502FB12	75K

Seymour_XT

DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.85V
HIGH	LOW	0.9V
LOW	HIGH	1.0V
HIGH	HIGH	1.1V
Setting		
Location	**Part No.**	**Value**
PR30	CS31002FB26	10K
PR38	CS37502FB12	75K
PR33	CS41072FB11	107K
PR32	CS34122FB19	41.2K

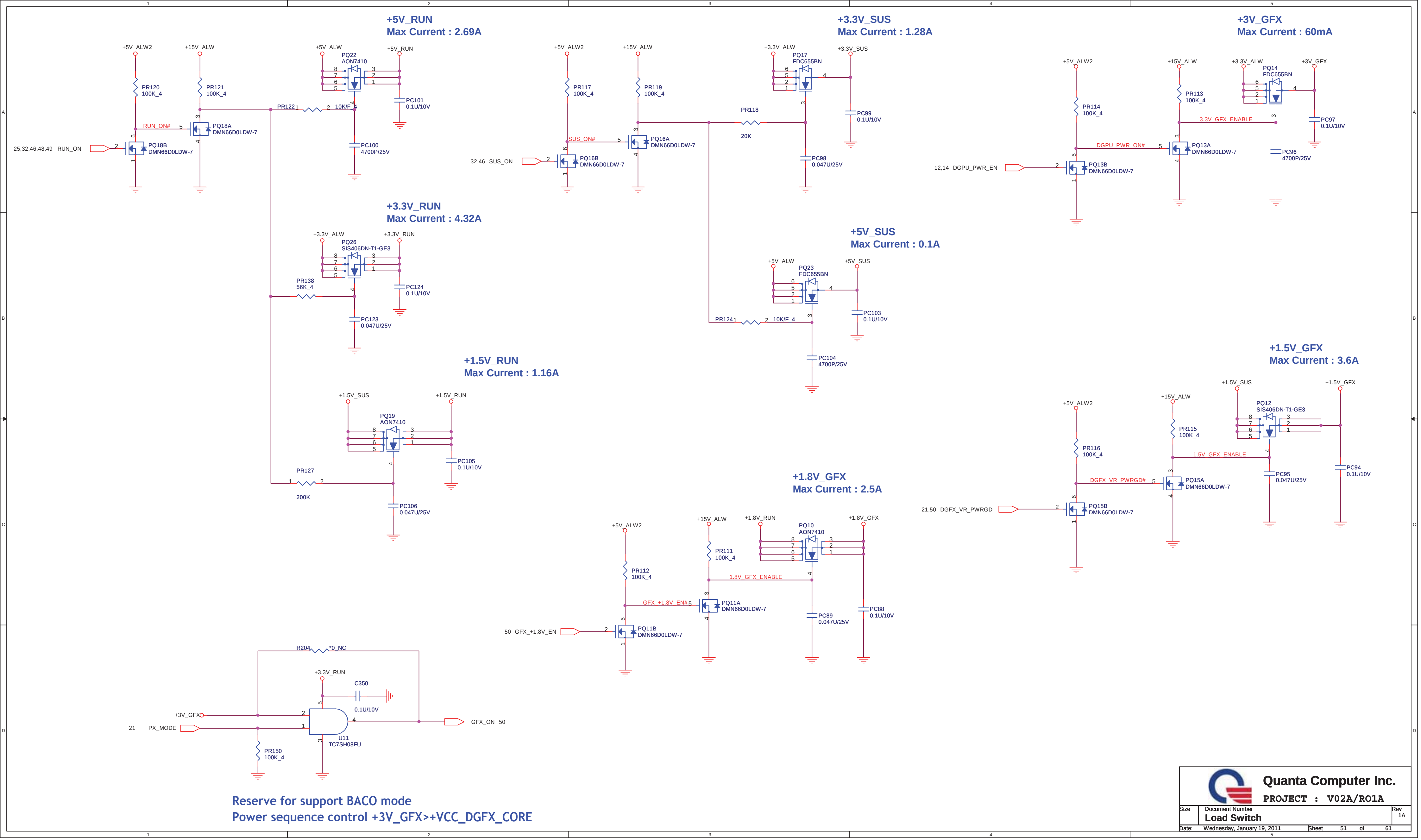


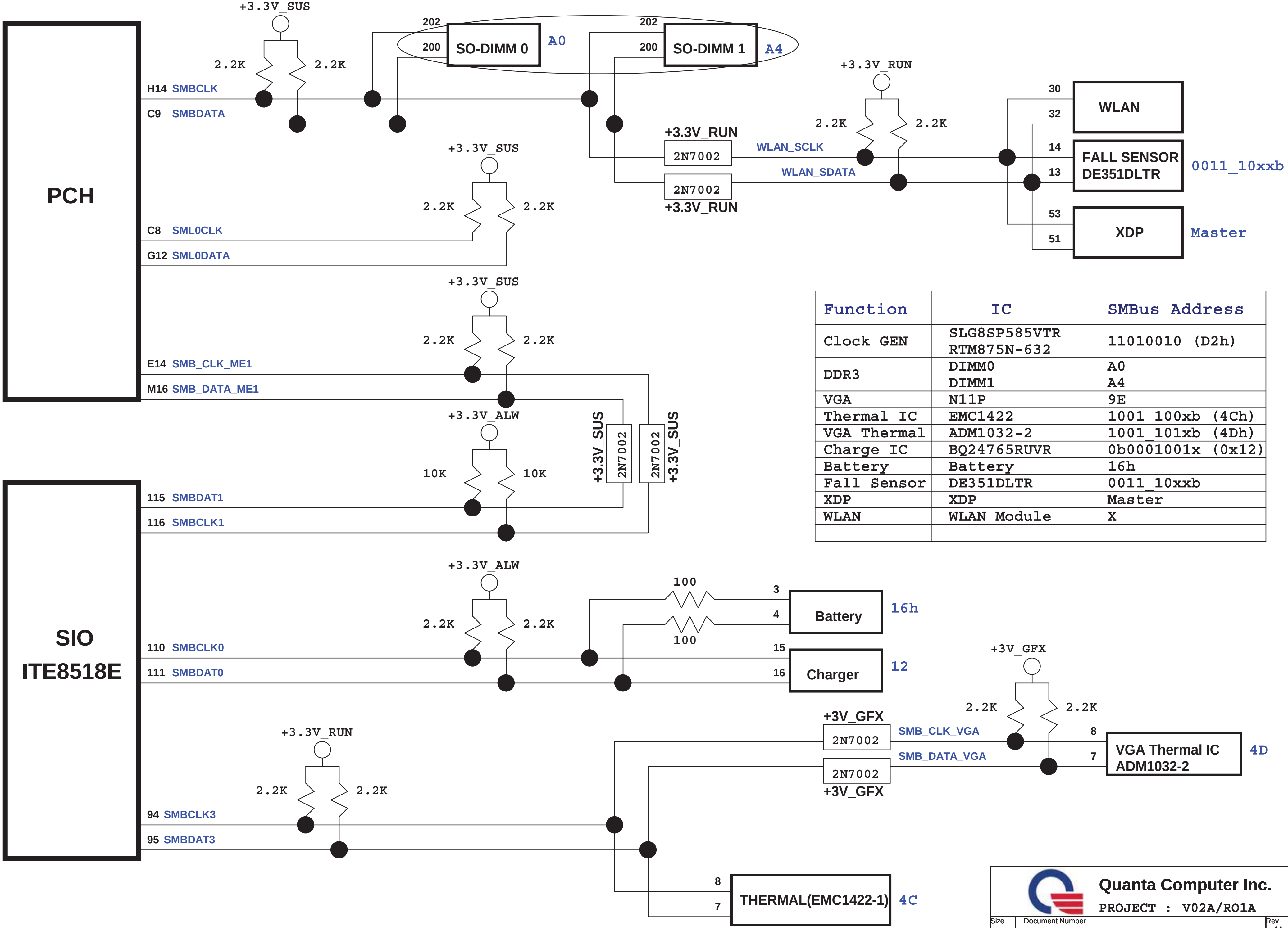
Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	dGFX_CORE (RT8208A)	1A

Date: Wednesday, January 19, 2011 Sheet 50 of 61


+5V_RUN
Max Current : 2.69A
+3.3V_SUS
Max Current : 1.28A
+3V_GFX
Max Current : 60mA
+3.3V_RUN
Max Current : 4.32A
+5V_SUS
Max Current : 0.1A
+1.5V_RUN
Max Current : 1.16A
+1.5V_GFX
Max Current : 3.6A
+1.8V_GFX
Max Current : 2.5A
25,32,46,48,49 RUN_ON
RUN_ON#
PQ18A DMN66D0LDW-7
PQ18B DMN66D0LDW-7
PR120 100K_4
PR121 100K_4
PR122 10K/F_4
PQ22 AON7410
PC101 0.1U/10V
PC100 4700P/25V
32,46 SUS_ON
SUS_ON#
PQ16A DMN66D0LDW-7
PQ16B DMN66D0LDW-7
PR117 100K_4
PR119 100K_4
PR118 20K
PQ17 FDC655BN
PC99 0.1U/10V
PC98 0.047U/25V
12,14 DGPU_PWR_EN
DGPU_PWR_ON#
3.3V_GFX_ENABLE
PR114 100K_4
PR113 100K_4
PQ13A DMN66D0LDW-7
PQ13B DMN66D0LDW-7
PQ14 FDC655BN
PC97 0.1U/10V
PC96 4700P/25V
PQ26 SIS406DN-T1-GE3
PR138 56K_4
PC124 0.1U/10V
PC123 0.047U/25V
PQ23 FDC655BN
PR124 10K/F_4
PC103 0.1U/10V
PC104 4700P/25V
PQ19 AON7410
PR127 200K
PC105 0.1U/10V
PC106 0.047U/25V
21,50 DGFX_VR_PWRGD
DGFX_VR_PWRGD#
1.5V_GFX_ENABLE
PR116 100K_4
PR115 100K_4
PQ15A DMN66D0LDW-7
PQ15B DMN66D0LDW-7
PQ12 SIS406DN-T1-GE3
PC95 0.047U/25V
PC94 0.1U/10V
50 GFX_+1.8V_EN
GFX_+1.8V_EN#
1.8V_GFX_ENABLE
PR112 100K_4
PR111 100K_4
PQ11A DMN66D0LDW-7
PQ11B DMN66D0LDW-7
PQ10 AON7410
PC89 0.047U/25V
PC88 0.1U/10V
R204 *0_NC
C350 0.1U/10V
+3V_GFX
21 PX_MODE
U11 TC7SH08FU
GFX_ON 50
PR150 100K_4
Reserve for support BACO mode
Power sequence control +3V_GFX>+VCC_DGFX_CORE
Quanta Computer Inc.
PROJECT : V02A/RO1A
Size
Document Number
Load Switch
Rev 1A
Date: Wednesday, January 19, 2011
Sheet 51 of 61



Function	IC	SMBus Address
Clock GEN	SLG8SP585VTR RTM875N-632	11010010 (D2h)
DDR3	DIMM0 DIMM1	A0 A4
VGA	N11P	9E
Thermal IC	EMC1422	1001 100xb (4Ch)
VGA Thermal	ADM1032-2	1001 101xb (4Dh)
Charge IC	BQ24765RUVR	0b0001001x (0x12)
Battery	Battery	16h
Fall Sensor	DE351DLTR	0011 10xxb
XDP	XDP	Master
WLAN	WLAN Module	X

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PROJECT : V02A/R01A

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Date: Wednesday, January 19, 2011 | Sheet 52 of 61