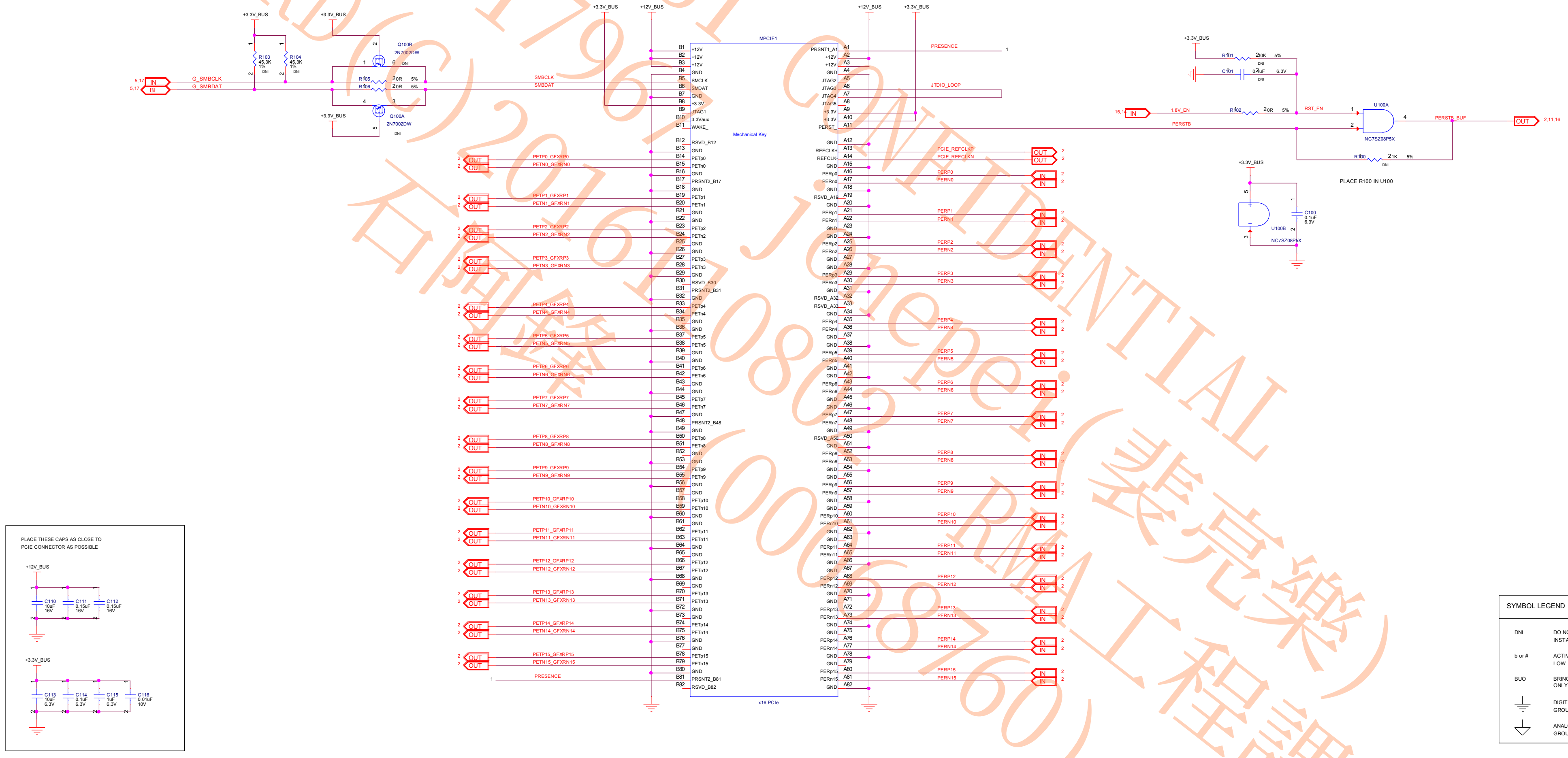
(1) PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
b or #	ACTIVE LOW
BUO	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND

AMD - PLATFORM HARDWARE ENG
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SHEET:	PCI-EXPRESS EDGE CONNECTOR
DATE:	Thu Apr 23 05:56:02 2015
REV:	1.0
SHEET NUMBER:	1 OF 19
DOCUMENT NUMBER:	105_C913xx_00
NOTES:	NOTE
TITLE:	TOBAGO GDDR5 X32

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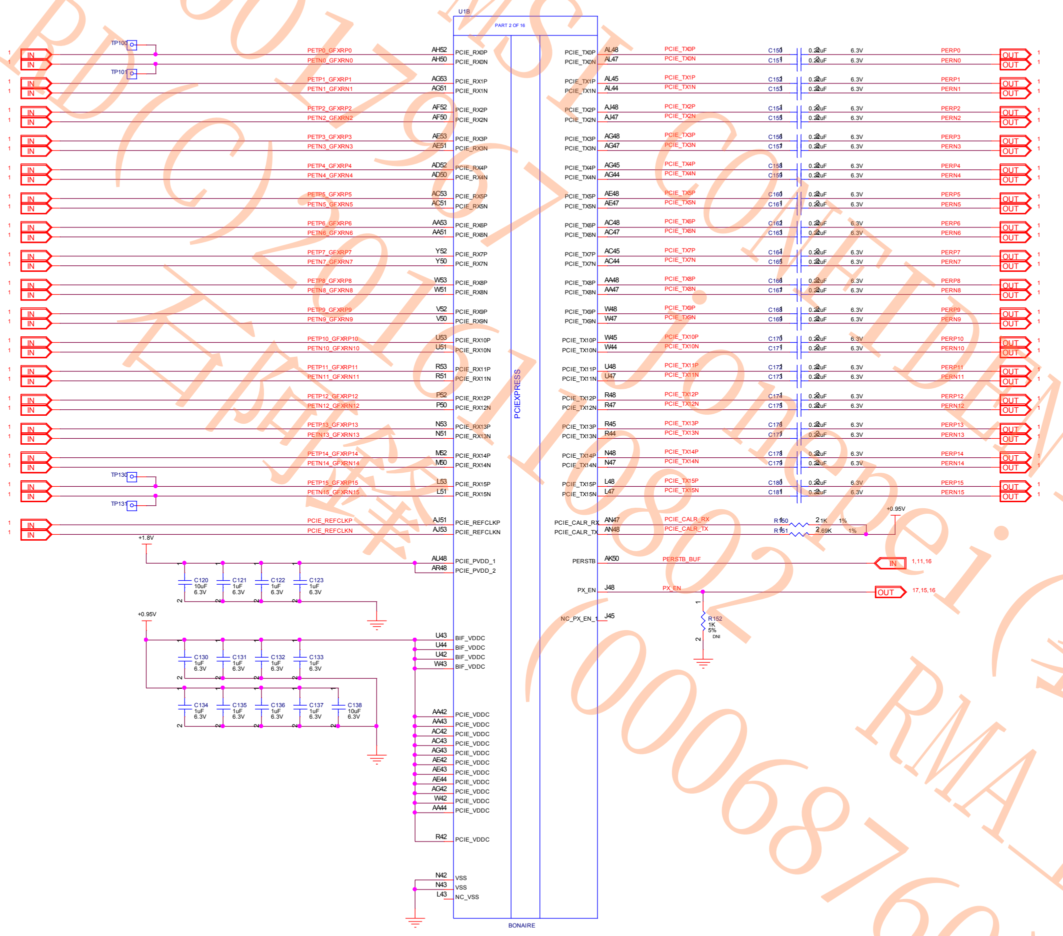
0001796-1708002 RD(C)2016 Jenpei(裴亮樂)(00058760) RMA工程課 石朋鋒

(2) TOBAGO PCIE INTERFACE



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SHEET:	TOBAGO PCIE		
DATE:	Thu Apr 23 05:54:17 2015	REV:	1.0
SHEET NUMBER:	2	OF	19
DOCUMENT NUMBER:	105_C913xx_00		
NOTES:	NOTE		

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TITLE: TOBAGO GDDR5 X32

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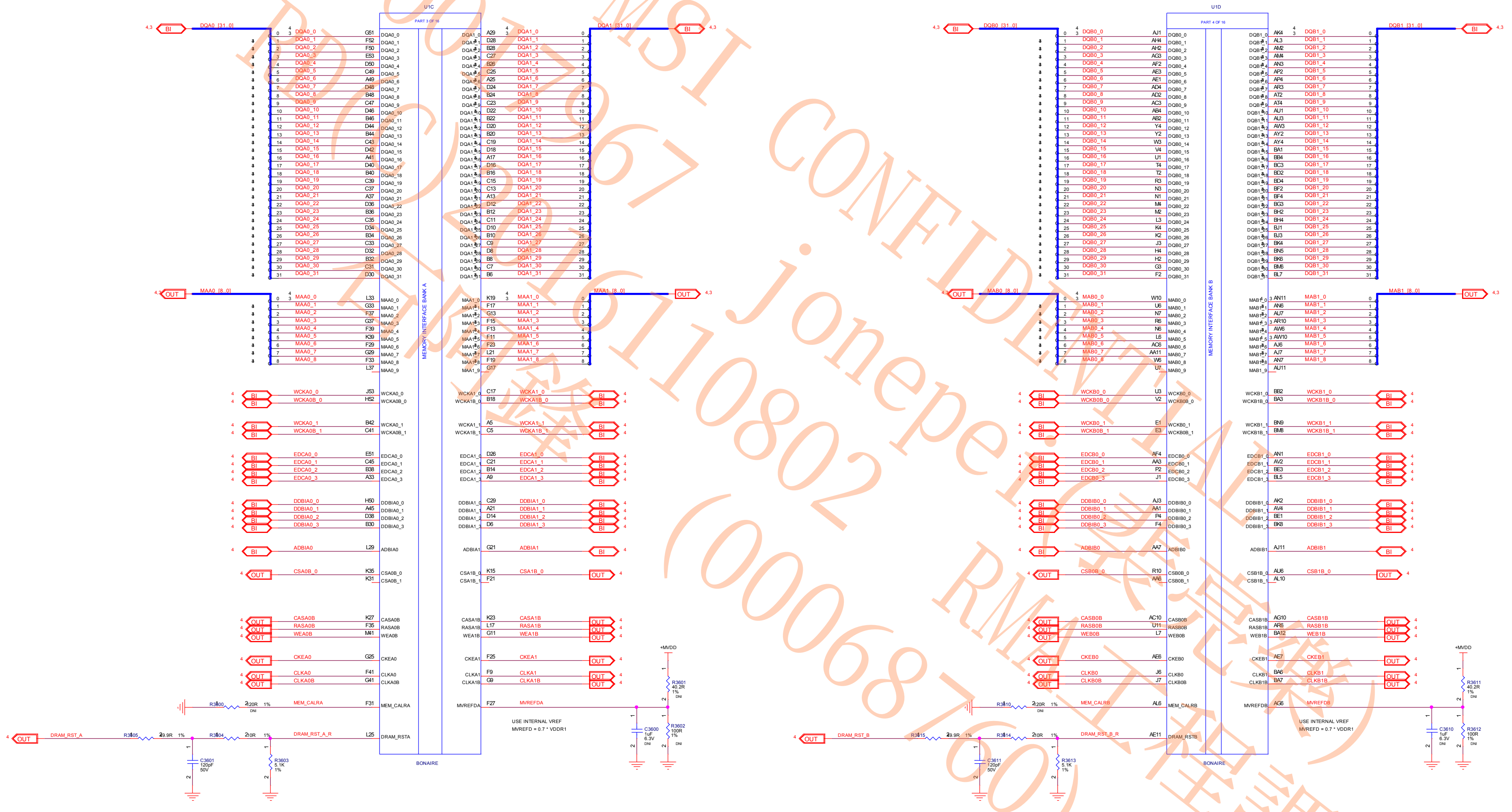
(3) TOBAGO MEMORY INTERFACE



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SHEET:	TOBAGO MEMORY
DATE:	Thu Apr 23 05:54:18 2015
REV:	1.0
SHEET NUMBER:	3 OF 19
DOCUMENT NUMBER:	105_C913xx_00
NOTES:	NOTE
TITLE:	TOBAGO GDDR5 X32

(4) GDDR5 CHAB x32

AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET:	GDDR5 x32 CHAB
DATE: Thu Apr 23 05:54:19 2015	REV: 1.0
SHEET NUMBER: 4 OF 19	
DOCUMENT NUMBER:	105_C913xx_00
NOTES: NOTE	TITLE: TOBAGO GDDR5 X32

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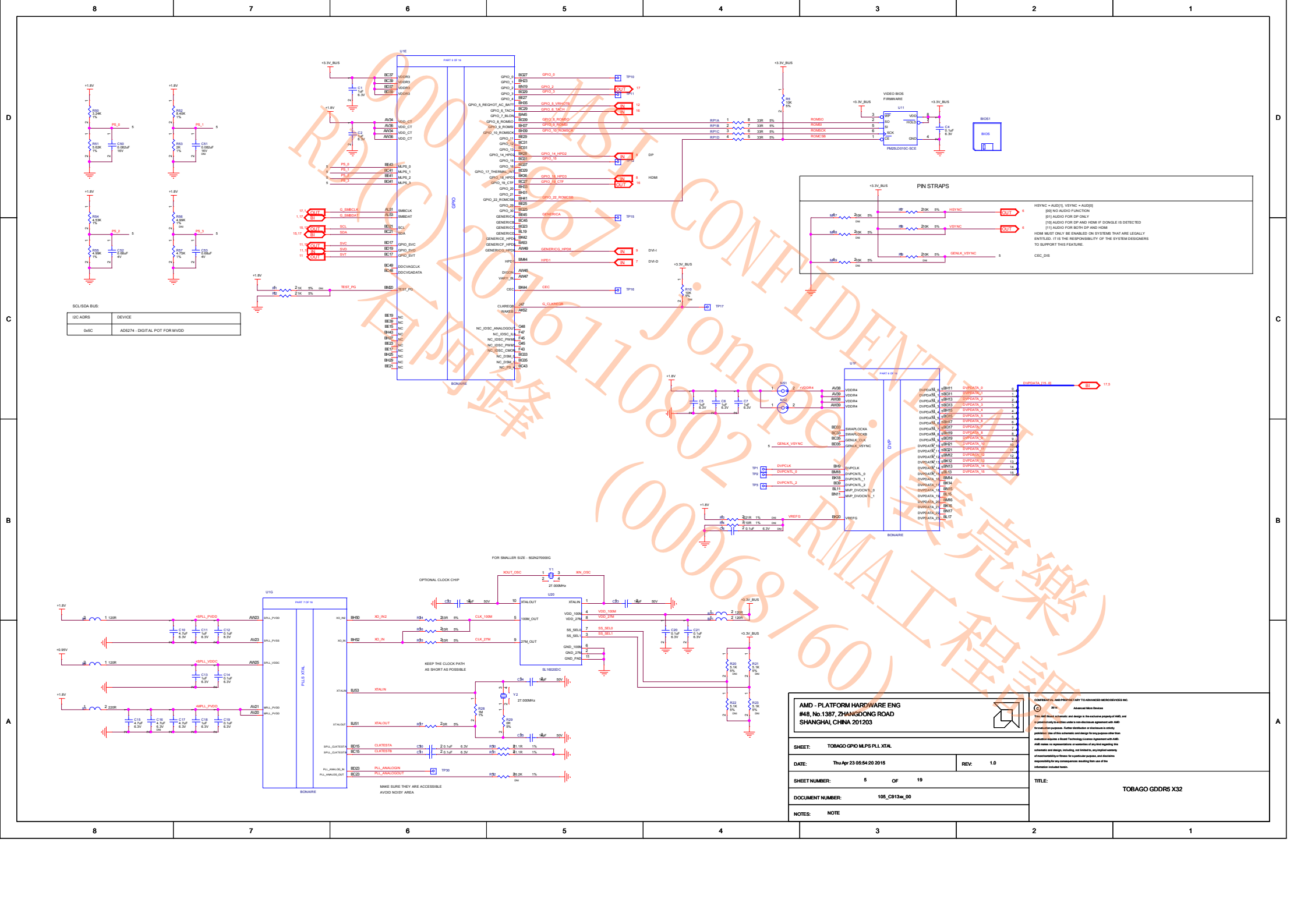
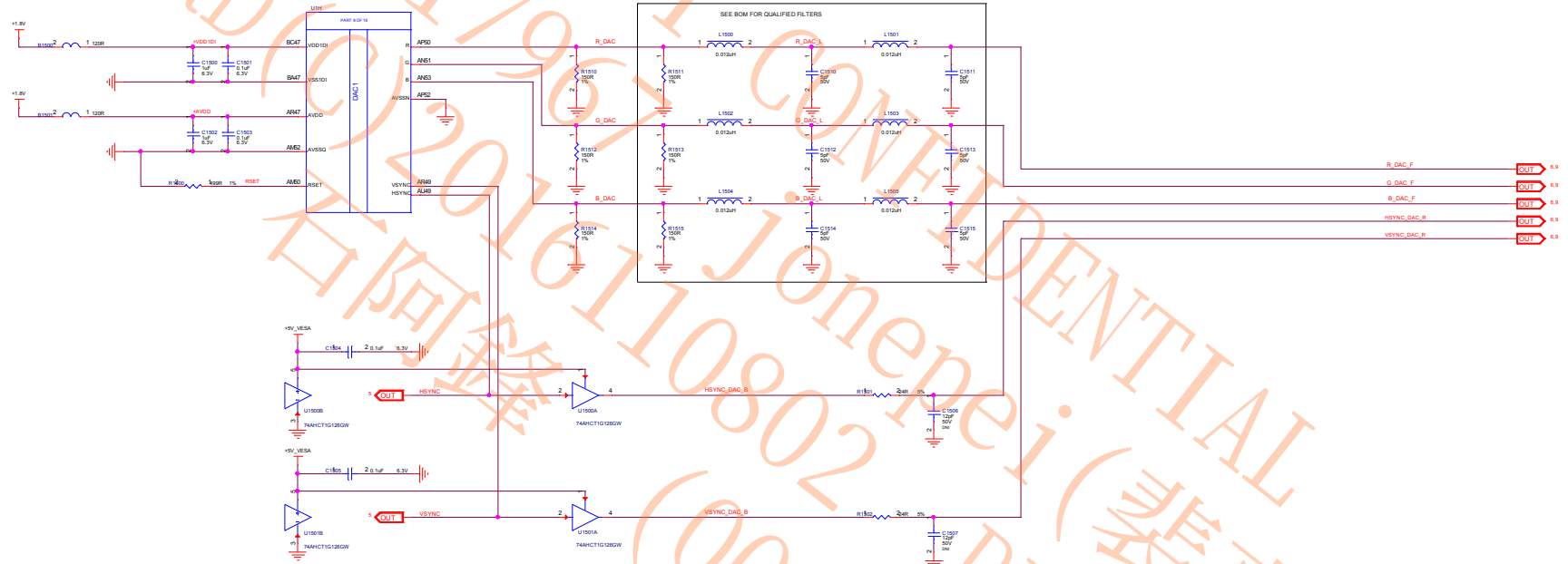
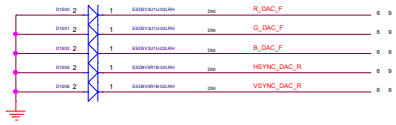

SCL/SDA BUS:
I2C ADRS
DEVICE
0x5C
AD5274 - DIGITAL POT FOR MVDD
PIN STRAPS
HSYNC = AUD[1], VSYNC = AUD[0]
[00] NO AUDIO FUNCTION
[01] AUDIO FOR DP ONLY
[10] AUDIO FOR DP AND HDMI IF DONGLE IS DETECTED
[11] AUDIO FOR BOTH DP AND HDMI
HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNERS TO SUPPORT THIS FEATURE.
CEC_DIS
FOR SMALLER SIZE - 502N270000G
OPTIONAL CLOCK CHIP
KEEP THE CLOCK PATH AS SHORT AS POSSIBLE
MAKE SURE THEY ARE ACCESSIBLE AVOID NOISY AREA
AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203
SHEET: TOBAGO GPIO MLPS PLL XTAL
DATE: Thu Apr 23 05:54:20 2015
REV: 1.0
SHEET NUMBER: 5 OF 19
DOCUMENT NUMBER: 105_C913xx_00
NOTES: NOTE
TITLE: TOBAGO GDDR5 X32

(6) TOBAGO DAC



OPTIONAL ESD PROTECTION DIODES



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: TOBAGO DAC	
DATE: Thu Apr 23 05:54:20 2015	REV: 1.0
SHEET NUMBER: 6 OF 19	
DOCUMENT NUMBER: 105_C913xx_00	
NOTES: NOTE	

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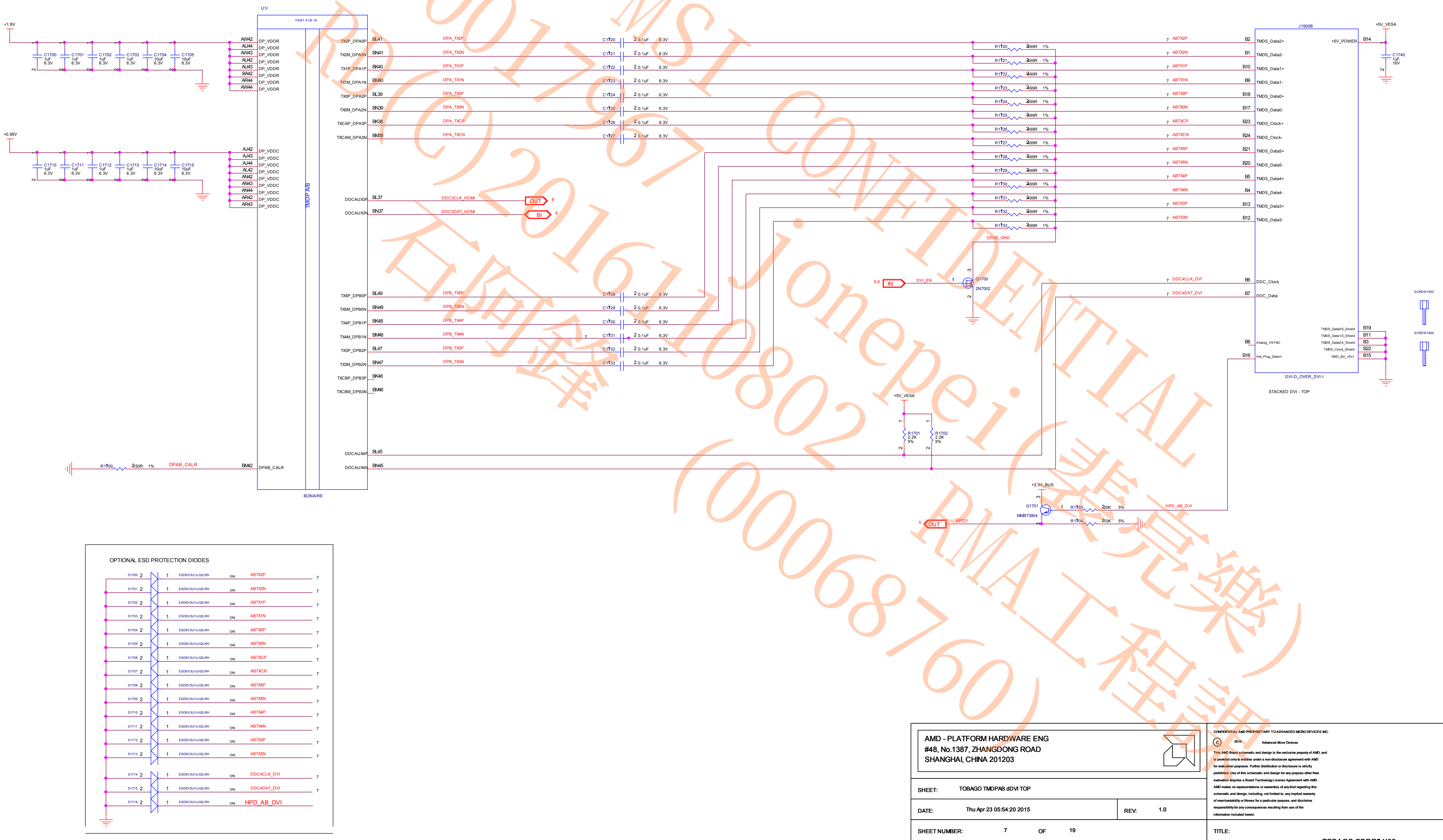
石阿鋒(00068760)

(7) TOBAGO TMDPAB dDVI



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET:	TOBAGO TMDPAB dDVI TOP
DATE:	Thu Apr 23 05:54:20 2015 — REV: 1.0
SHEET NUMBER:	7 OF 19
DOCUMENT NUMBER:	105_C913xx_00
NOTES:	NOTE

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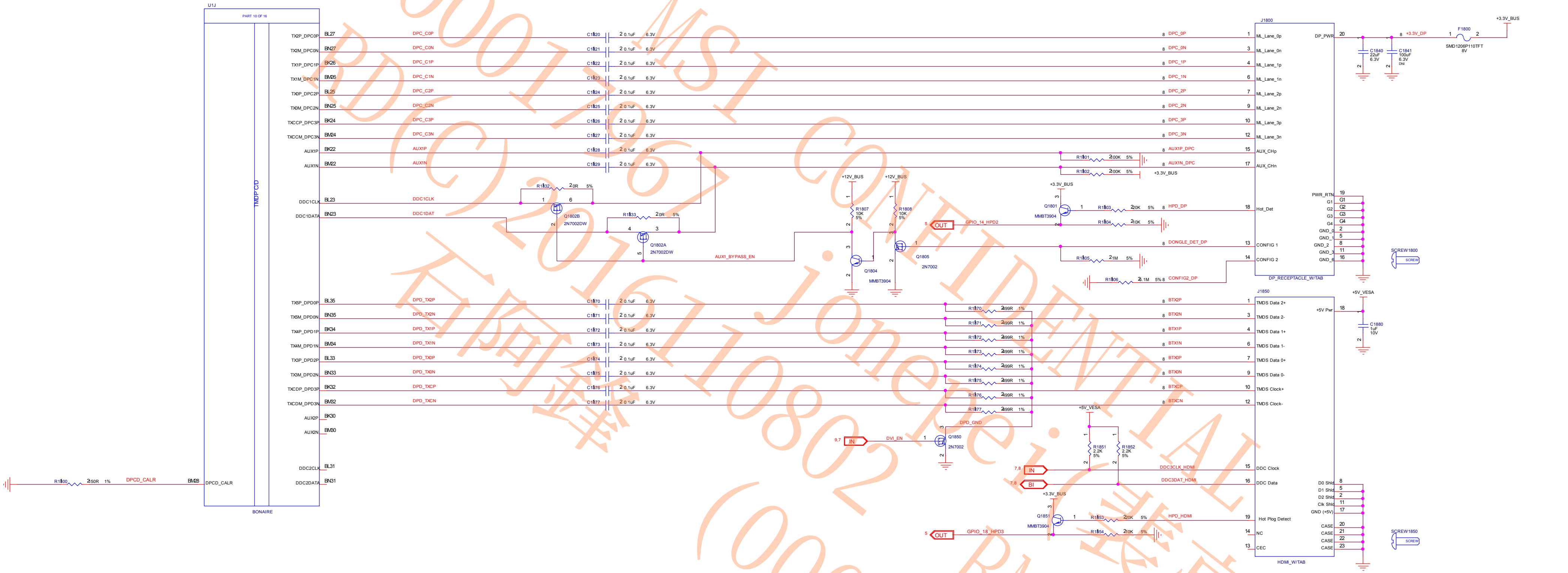
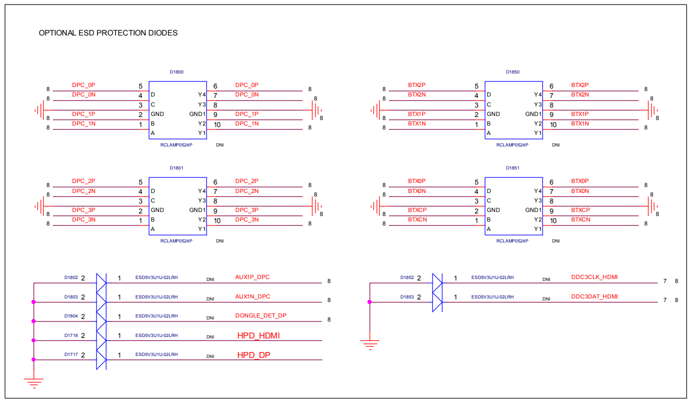
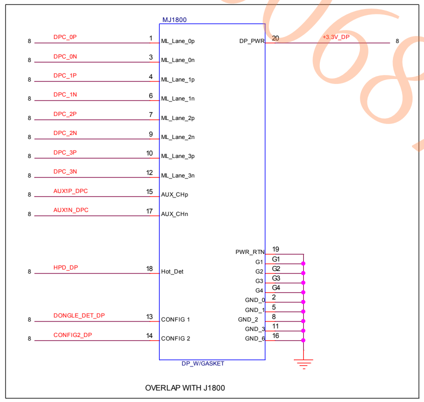
(8) TOBAGO TMDPCD DP HDMI







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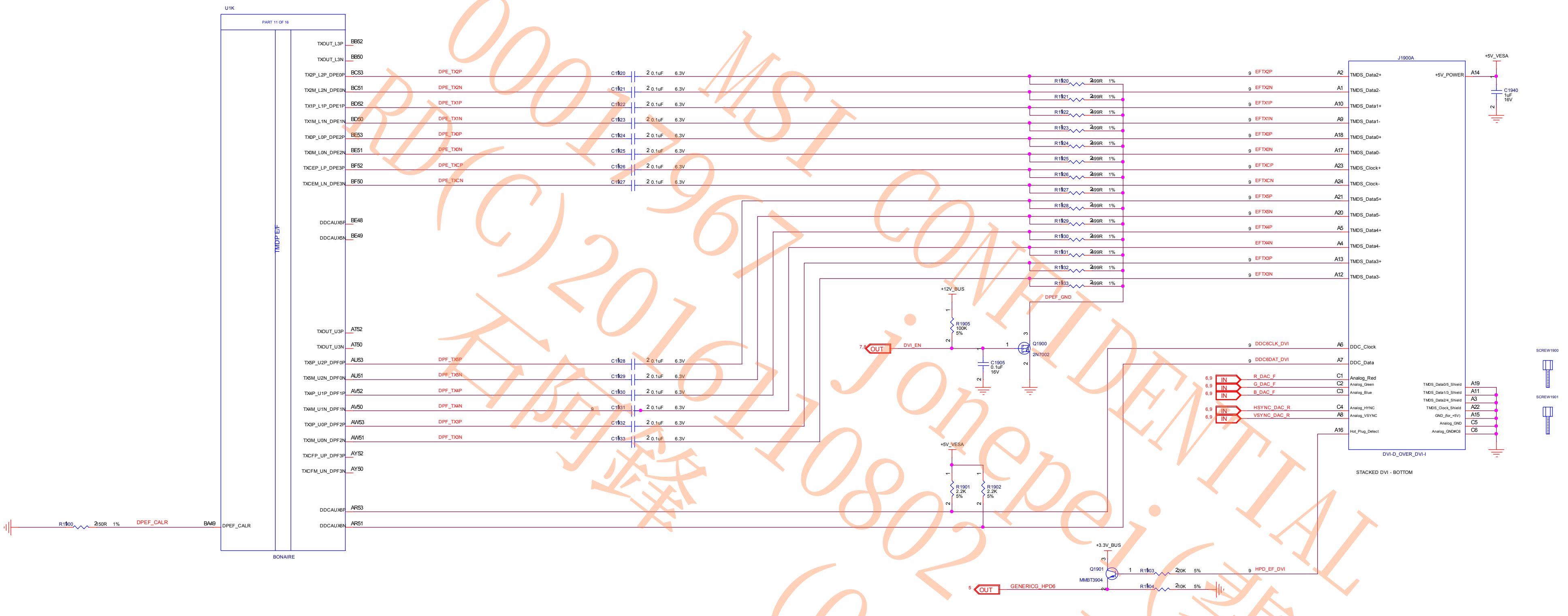
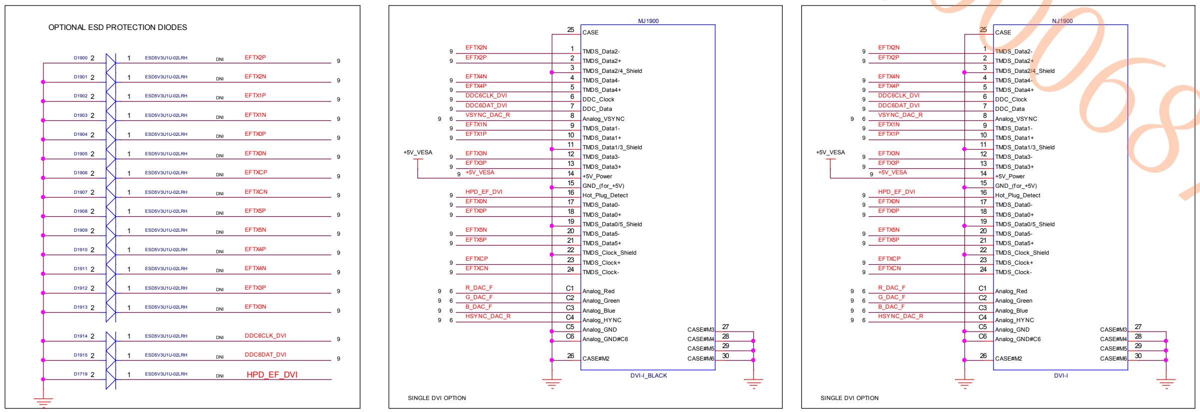
SHEET:	TOBAGO TMDPCD DP HDMI
DATE:	Thu Apr 23 05:54:21 2015
REV:	1.0
SHEET NUMBER:	8 OF 19
DOCUMENT NUMBER:	105_C913xx_00
NOTES:	NOTE
TITLE:	TOBAGO GDDR5 X32

000171967 MSI CONFIDENTIAL
BD(C) 2016110802 jonelei
RMA工程部 (000068760)





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#48, No.1387, ZHANGDONG ROAD
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SHEET: TOBAGO TMDPEF dDVI BOTTOM

DATE: Thu Apr 23 05:54:21 2015 REV: 1.0

SHEET NUMBER: 9 OF 19

DOCUMENT NUMBER: 105_C913xx_00

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TITLE: TOBAGO GDDR5 X32

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MSI CONFIDENTIAL Jonepei(裴亮樂) RMA工程課 (00068760)

00017967 MSI CONFIDENTIAL
RD(C) 20161108 jonepei (黃完樂)
(00068760) RMA工程課
石詢鋒

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SHEET: TOBAGO POWER GND	
DATE: Thu Apr 23 05:54:22 2015	REV: 1.0
SHEET NUMBER: 10 OF 19	
DOCUMENT NUMBER: 105_C913xx_00	
NOTES: NOTE	

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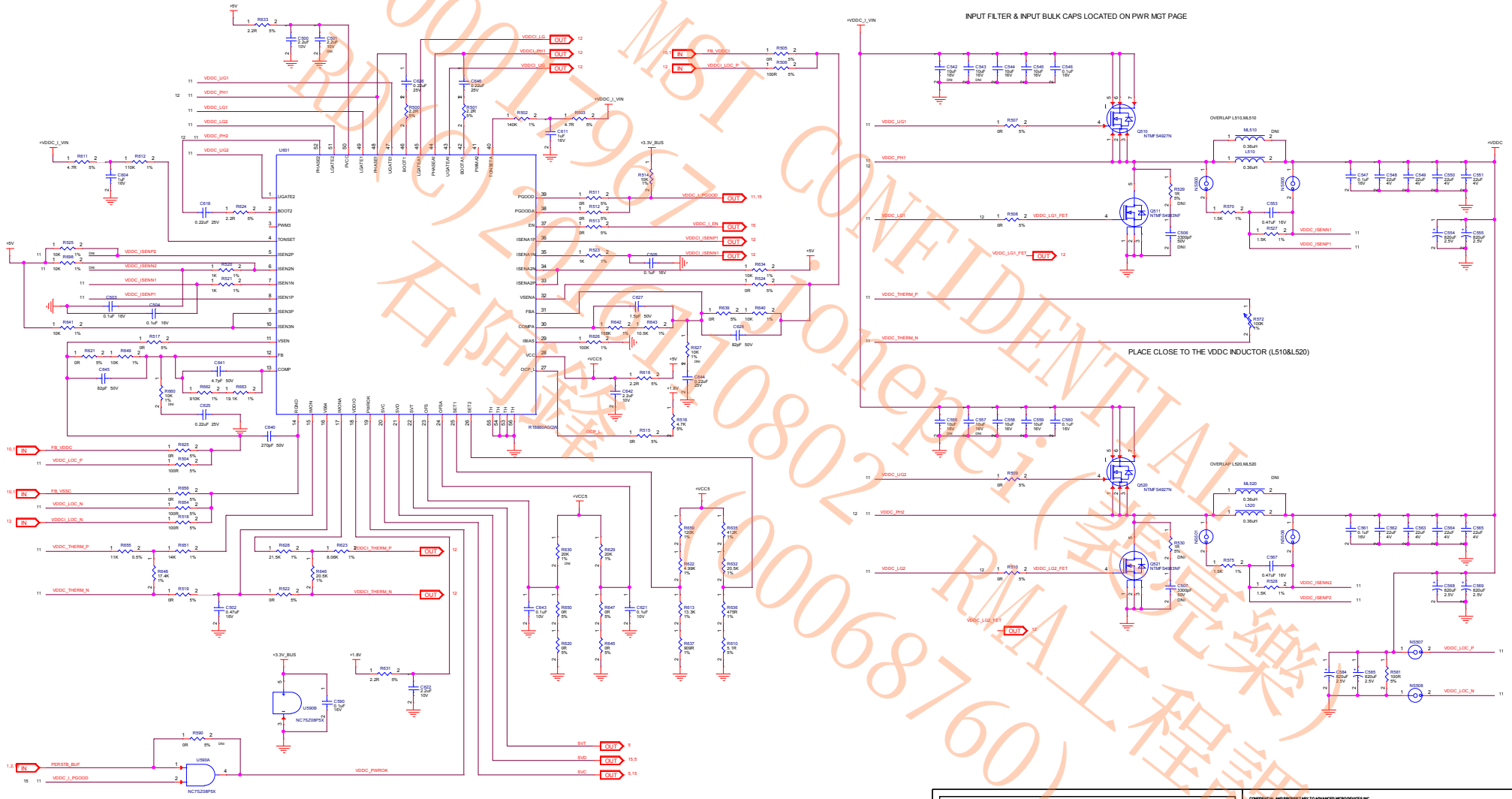
TITLE: TOBAGO GDDR5 X32

16ci203



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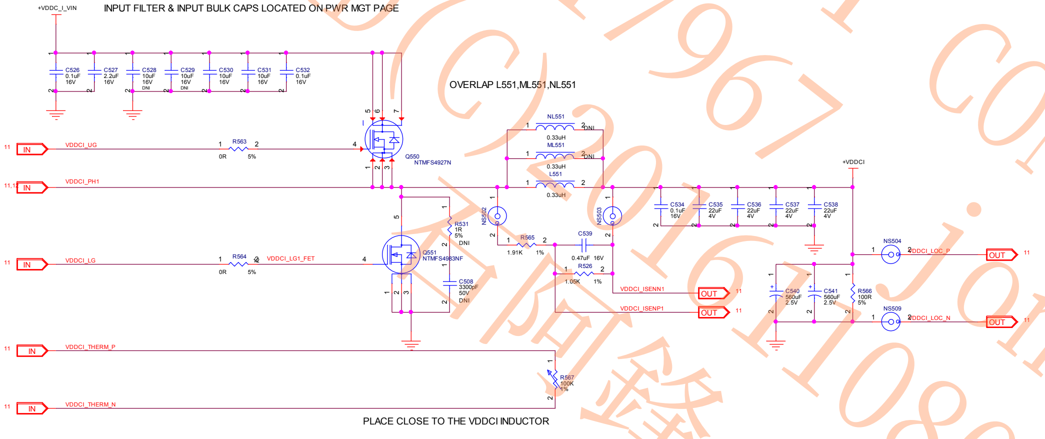
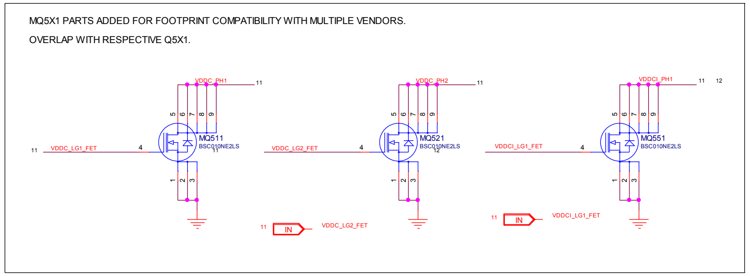
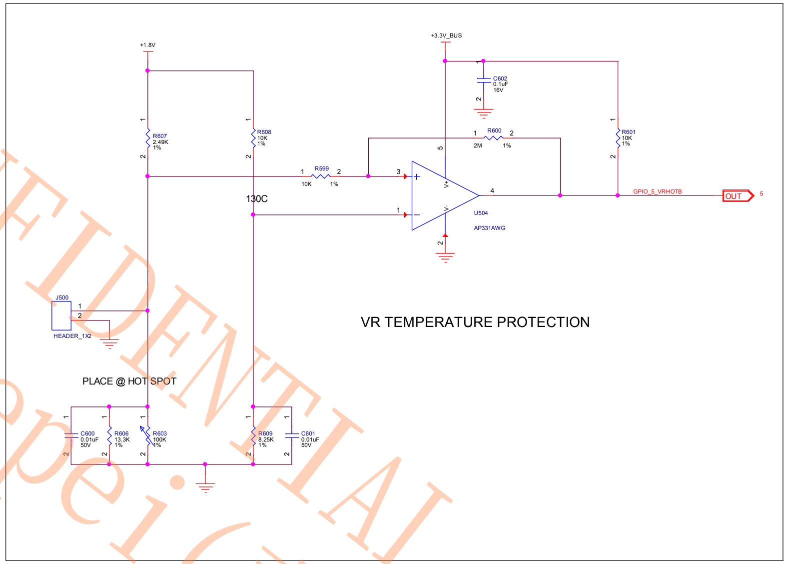
16ci203


INPUT FILTER & INPUT BULK CAPS LOCATED ON PWR MGT PAGE
OVERLAP L551,ML551,NL551
+VDDC_I_VIN
+VDDCI
VDDCI_UG
VDDCI_PH1
VDDCI_LG
VDDCI_LG1_FET
VDDCI_THERM_P
VDDCI_THERM_N
VDDCI_ISENN1
VDDCI_ISENP1
VDDCI_LOC_P
VDDCI_LOC_N
Q550
NTMFS4927N
Q551
NTMFS4983NF
PLACE CLOSE TO THE VDDCI INDUCTOR





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SHANGHAI, CHINA 201203

SHEET:	VDDC_VDDCI_II
DATE:	Thu Apr 23 05:54:23 2015
REV:	1.0
SHEET NUMBER:	12 OF 19
DOCUMENT NUMBER:	105_C913xx_00
NOTES:	NOTE
TITLE:	TOBAGO GDDR5 X32

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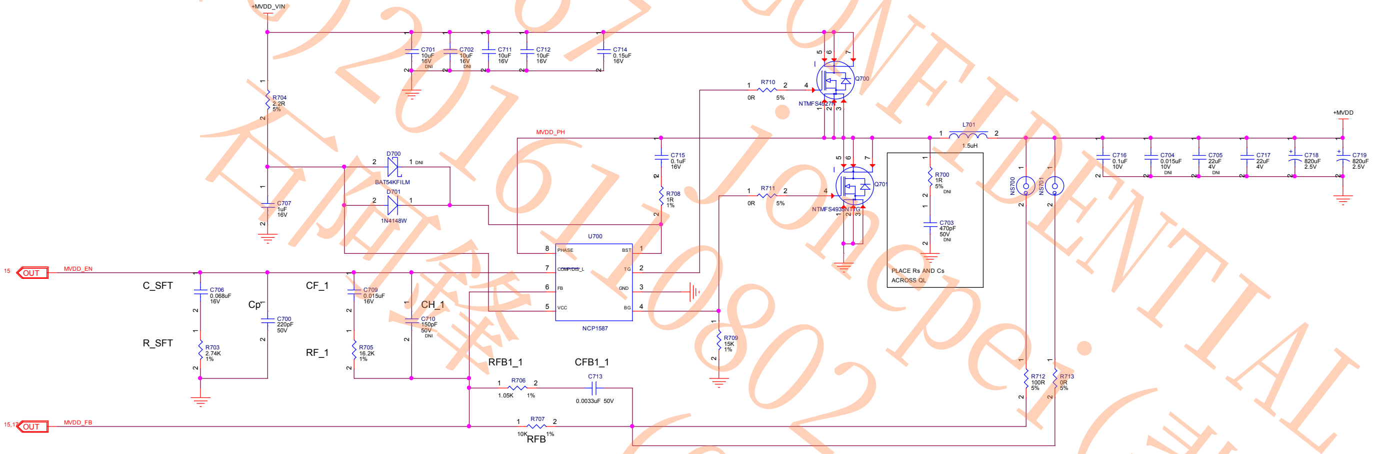

RFB2 is on BFoard Engineer's page.
Default value is 11.3k for 1.5V.
RFB2 = RFB*(Vref/(Vout-Vref))

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SHEET: MVDD

DATE: Thu Apr 23 05:54:24 2015

REV: 1.0

SHEET NUMBER: 13 OF 19

DOCUMENT NUMBER: 105_C913xx_00

NOTES: NOTE

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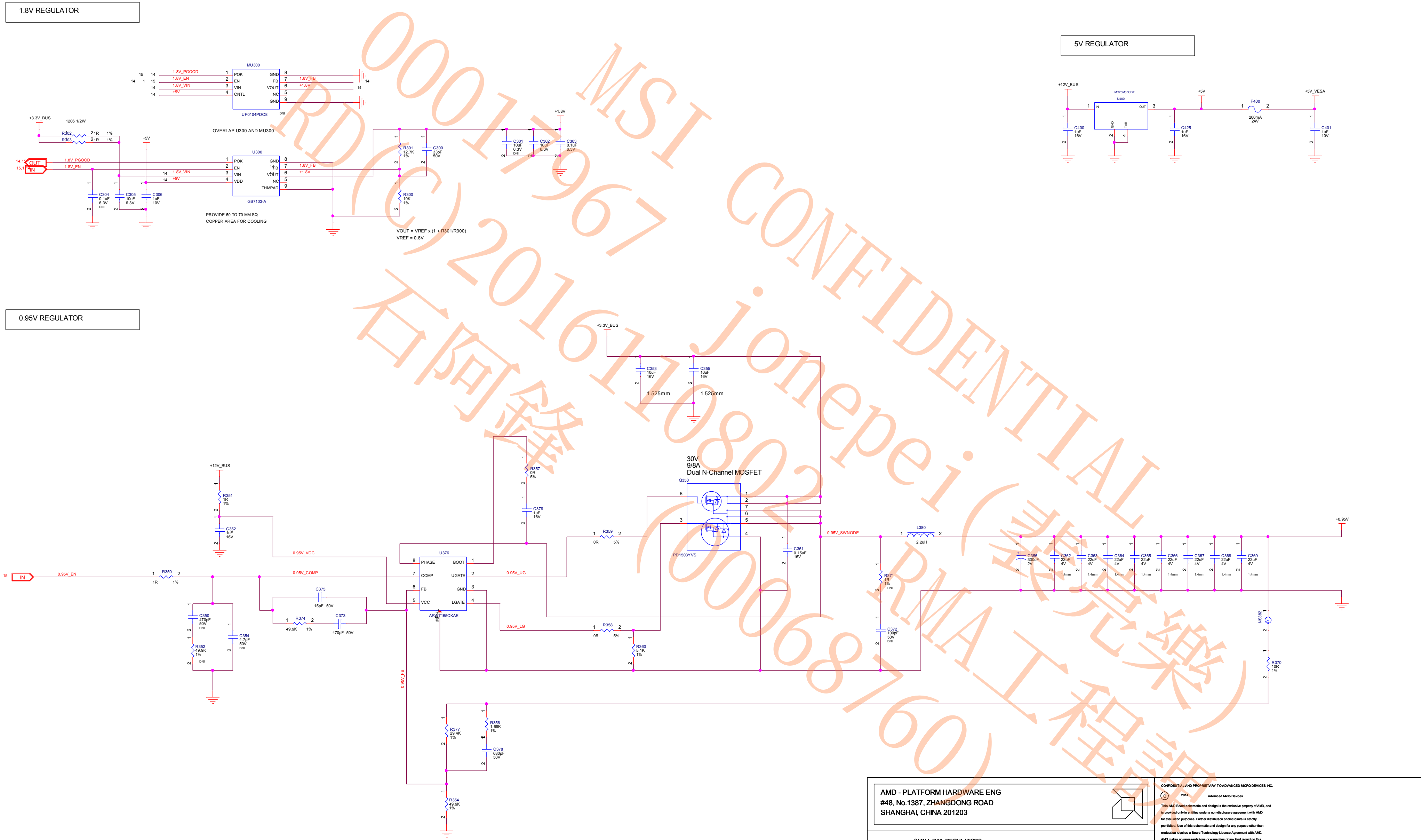
TITLE: TOBAGO GDDR5 X32


1.8V REGULATOR
MU300
UP0104PDC8
1.8V_PGOOD
1.8V_EN
1.8V_VIN
+5V
1.8V_FB
+1.8V
+3.3V_BUS
1206 1/2W
R302
R303
+5V
U300
GS7103-A
OVERLAP U300 AND MU300
PROVIDE 50 TO 70 MM SQ.
COPPER AREA FOR COOLING
C304 0.1uF 6.3V
C305 10uF 6.3V
C306 1uF 10V
R301 12.7K 1%
R300 10K 1%
C300 33pF 50V
C301 10uF 6.3V
C302 10uF 6.3V
C303 0.1uF 6.3V
VOUT = VREF x (1 + R301/R300)
VREF = 0.8V
5V REGULATOR
+12V_BUS
MC78M05CDT
U400
+5V
F400 200mA 24V
+5V_VESA
C400 1uF 16V
C425 1uF 16V
C401 1uF 10V
0.95V REGULATOR
+3.3V_BUS
C353 10uF 16V
C355 10uF 16V
1.525mm
1.525mm
30V
9/8A
Dual N-Channel MOSFET
Q350
PD1503YVS
+12V_BUS
R351 1R 1%
C352 1uF 16V
0.95V_VCC
0.95V_EN
R350 1R 1%
0.95V_COMP
U376
APW7165CKAE
PHASE
COMP
FB
VCC
BOOT
UGATE
GND
LGATE
R357 0R 5%
C379 1uF 16V
R359 0R 5%
0.95V_UG
0.95V_LG
R358 0R 5%
R360 5.1K 1%
C375 15pF 50V
R374 49.9K 1%
C373 470pF 50V
C350 470pF 50V
R352 49.9K 1%
C354 4.7pF 50V
C361 0.15uF 16V
0.95V_SWNODE
L380 2.2uH
+0.95V
R371 1R 1%
C372 100pF 50V
C356 330uF 2V
C362 22uF 4V
C363 22uF 4V
C364 22uF 4V
C365 22uF 4V
C366 22uF 4V
C367 22uF 4V
C368 22uF 4V
C369 22uF 4V
R370 10R 1%
0.95V_FB
R377 29.4K 1%
R356 1.69K 1%
C378 680pF 50V
R354 49.9K 1%

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SHEET:	SMALL RAIL REGULATORS
DATE:	Thu Apr 23 05:54:24 2015
REV:	1.0
SHEET NUMBER:	14 OF 19
DOCUMENT NUMBER:	105_C913xx_00
NOTES:	NOTE
TITLE:	TOBAGO GDDR5 X32

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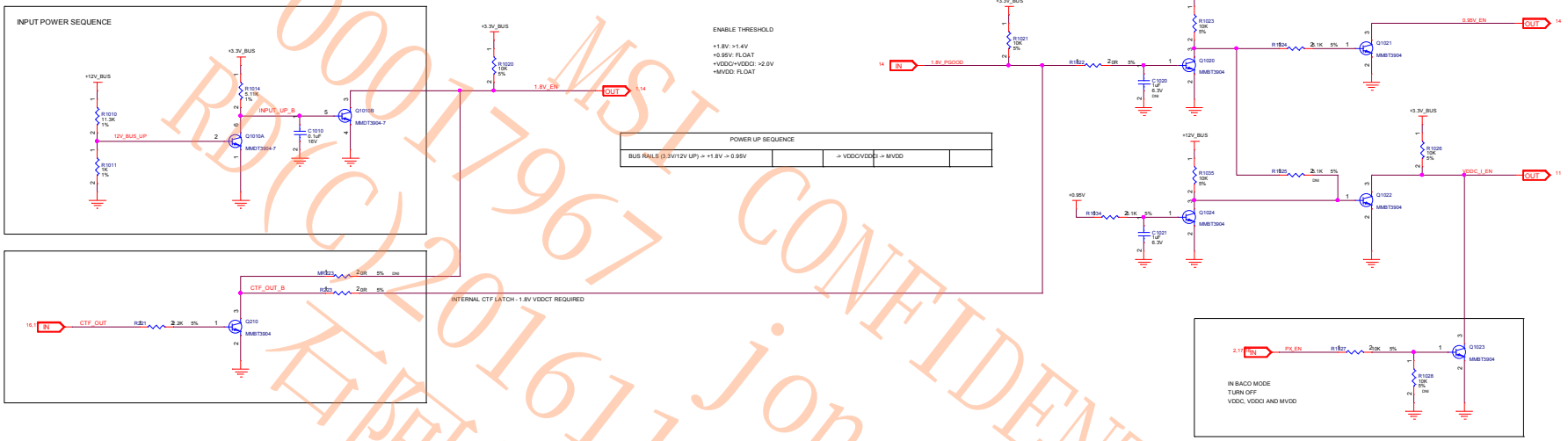

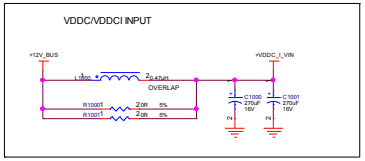

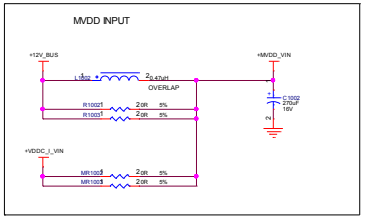

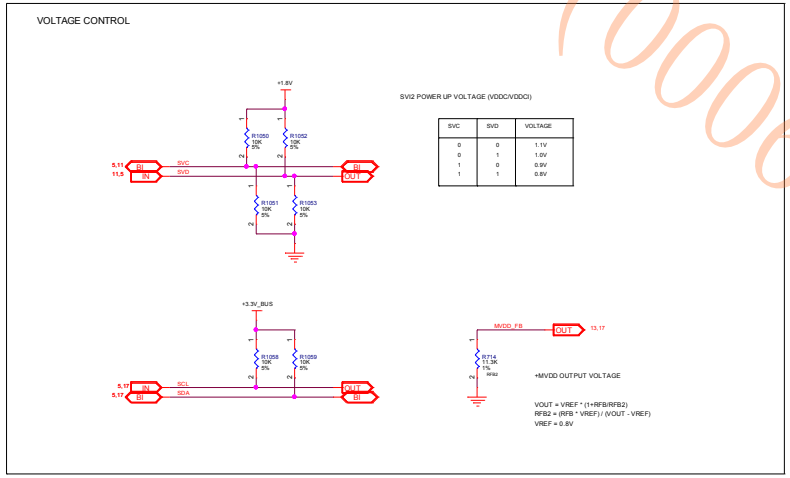

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SHEET:	POWER MANAGEMENT		
DATE:	Thu Apr 23 05:54:25 2015	REV:	1.0
SHEET NUMBER:	15 OF 19		
DOCUMENT NUMBER:	105_C913xx_00		
NOTES:	NOTE		

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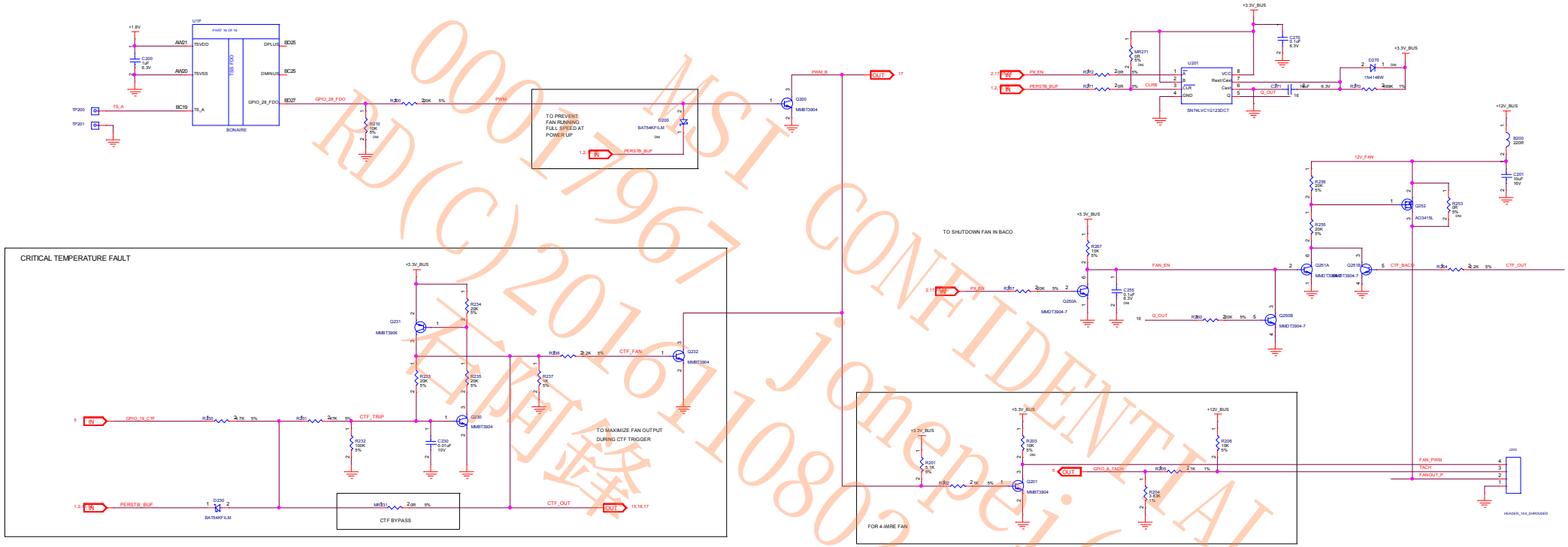

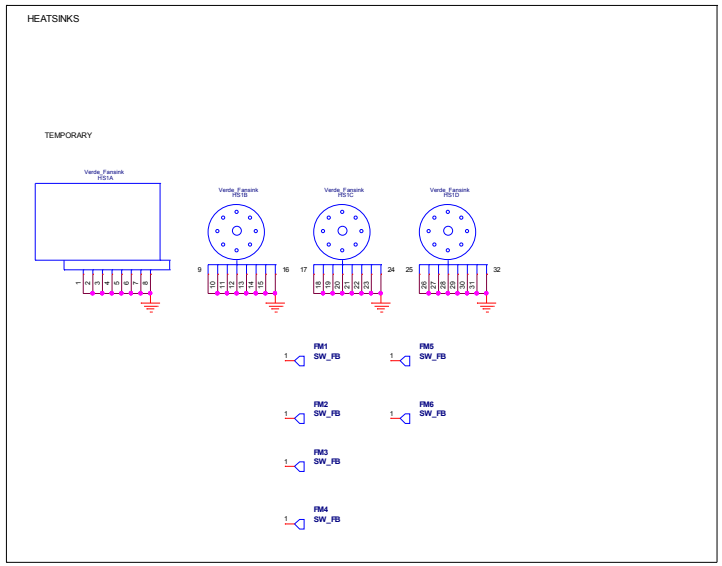

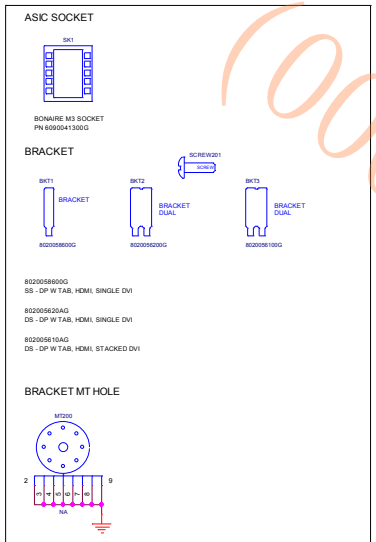

TOP
Single end
Memory
48 ohm +/- 5 ohm
4.33 mils

TOP
Different
PCIE
85 ohm +/- 10 %
4.41 mils / 7.4 mils

L3
Different
TMDS
85 ohm +/- 10 %
4.61 mils / 7.2 mils

Bottom
Different
Memory clock
80 ohm +/- 10 %
4.33 mils / 6.3 mils

L3
Single end
Memory
48 ohm +/- 5 ohm
4.33 mils

Bottom
Single end
Memory
48 ohm +/- 5 ohm
4.33 mils

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SHEET: MECH AND THERM MANAGEMENT	
DATE: Thu Apr 23 05:54:25 2015	REV: 1.0
SHEET NUMBER: 16 OF 19	
DOCUMENT NUMBER: 105_C913xx_00	
NOTES: NOTE	
TITLE: TOBAGO GDDR5 X32	

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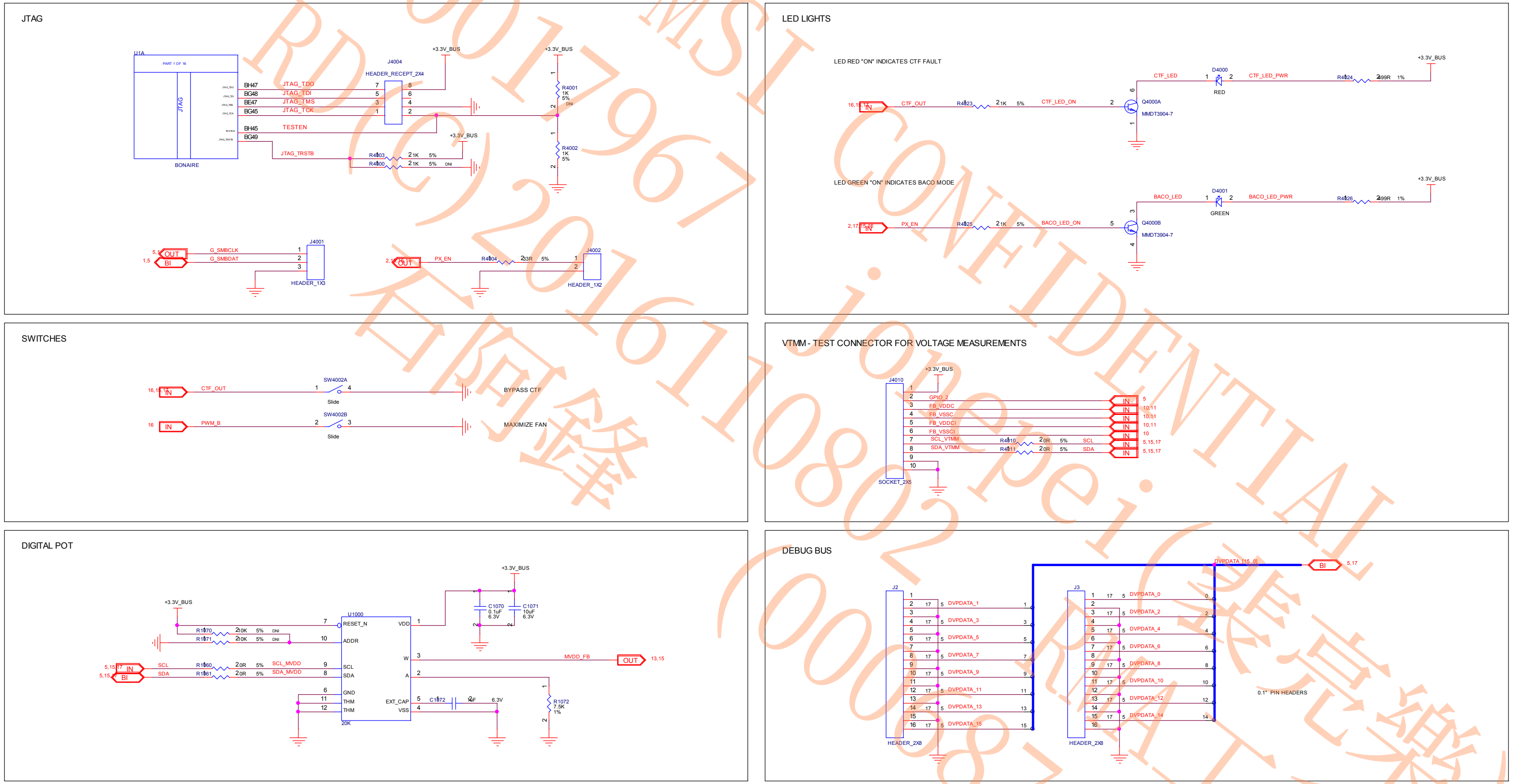
科通锋 (00068760) R&A工程部



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SHEET: DEBUG CIRCUITS

DATE: Thu Apr 23 05:54:25 2015 REV: 1.0

SHEET NUMBER: 17 OF 19

DOCUMENT NUMBER: 105_C913xx_00

NOTES: NOTE

TITLE: TOBAGO GDDR5 X32

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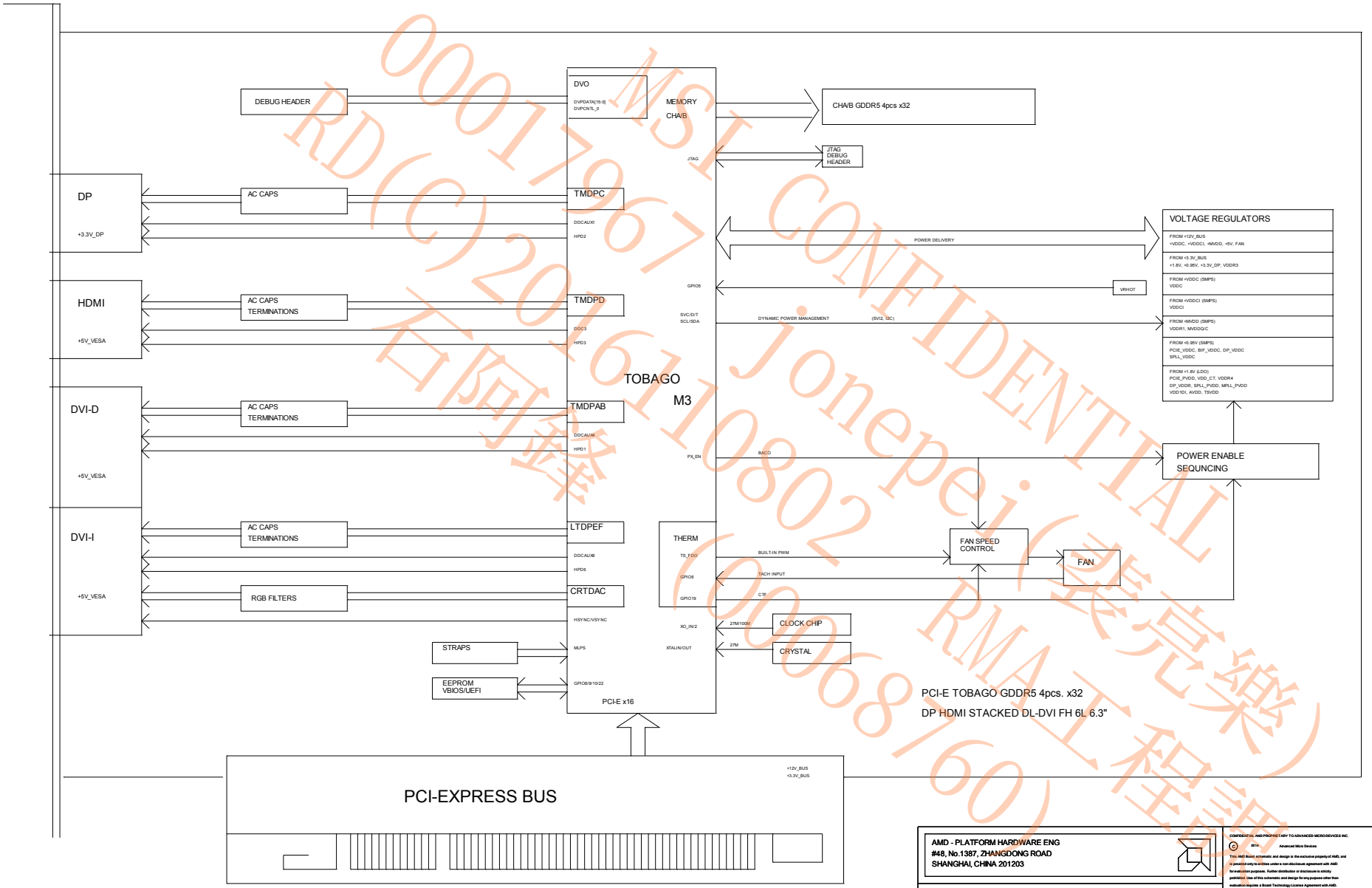

0001796 7 Jonepei(樊完樂) RD(C)2016110802 RMA工程課 (0000068760) 石阿峰 MSI CONFIDENTIAL

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SHEET:	BLOCK DIAGRAM
DATE:	Thu Apr 23 05:54:26 2015
REV:	1.0
SHEET NUMBER:	18 OF 19
DOCUMENT NUMBER:	105_C913xx_00
NOTES:	NOTE
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TITLE: TOBAGO GDDR5 X32

DOCUMENT NUMBER: 105_C913xx_00

DATE: Mon Jan 26 02:32:37 2015

SHEET NUMBER: 19 OF 19

REV: 1.0

REVISION HISTORY

ENGINEER: PEAK DONG

NOTES: NOTE

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SCH Rev	PCB Rev	Date	REVISION DESCRIPTON
0	00A	09/19/2014	INITIAL DESIGN
1	00B	11/25/2014	CORRECTING VCCSTG->VCCS
2	00	1/23/2015	RELEASED TO 00

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