+3V 4,10,11,12,13,14,15,17,18,19,20,21,27,28,29,30,31,33,34,35,36,37,43,46,51
+1.0V 4,6,37,42
+VCCSTPLL 4,5,6,9,42,43

HDMI

29 IN_D2# → IN_D2# E55
29 IN_D2 → IN_D2 F55
29 IN_D1# → IN_D1# E58
29 IN_D1 → IN_D1 F58
29 IN_D0# → IN_D0# F53
29 IN_D0 → IN_D0 G53
29 IN_CLK# → IN_CLK# F56
29 IN_CLK → IN_CLK G56

U1A SKL_ULT ?

Need apply PN

Justsurport FHD 1920x1080

DDI1_TXN[0] C50
DDI1_TXP[0] D50
DDI1_TXN[1] C52
DDI1_TXP[1] D52
DDI1_TXN[2] A50
DDI1_TXP[2] B50
DDI1_TXN[3] B51
DDI1_TXP[3] C51
DDI

DDI2_TXN[0] C50
DDI2_TXP[0] D50
DDI2_TXN[1] C52
DDI2_TXP[1] D52
DDI2_TXN[2] A50
DDI2_TXP[2] B50
DDI2_TXN[3] B51
DDI2_TXP[3] C51

DISPLAY SIDEBANDS

EDP

EDP_TXN[0] C47 → INT_EDP_TXN0 → INT_EDP_TXN0 27
EDP_TXP[0] C46 → INT_EDP_TXP0 → INT_EDP_TXP0 27
EDP_TXN[1] D46 → INT_EDP_TXN1 → INT_EDP_TXN1 27
EDP_TXP[1] C45 → INT_EDP_TXP1 → INT_EDP_TXP1 27
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

EDP_AUXN E45 → INT_EDP_AUXN → INT_EDP_AUXN 27
EDP_AUXP F45 → INT_EDP_AUXP → INT_EDP_AUXP 27

EDP_DISP_UTIL B52 → TP1

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN E48
DDI2_AUXP F48
DDI3_AUXN G46
DDI3_AUXP E46

GPP_E13/DDPB_HPD0 L9 → HDMI_HPD_CON → HDMI_HPD_CON 29
GPP_E14/DDPC_HPD1 L7
GPP_E15/DDPD_HPD2 L6
GPP_E16/DDPE_HPD3 N9
GPP_E17/EDP_HPD L10 → ULT_EDP_HPD → ULT_EDP_HPD 27

EDP_BKLTEN R12 → PCH_LVDS_BLON → PCH_LVDS_BLON 27
EDP_BKLTCTL R11 → PCH_DPST_PWM → PCH_DPST_PWM 27
EDP_VDDEN U13 → PCH_DISP_ON → PCH_DISP_ON 27

29 SDVO_CLK → L13 GPP_E18/DDPB_CTRLCLK
29 SDVO_DATA → L12 GPP_E19/DDPB_CTRLDATA

TP2 1 DDPC_CTRLDATA → N7 GPP_E20/DDPC_CTRLCLK
N6 GPP_E21/DDPC_CTRLDATA

TP3 1 DDPD_CTRLDATA → N11 GPP_E22/DDPD_CTRLCLK
N12 GPP_E23/DDPD_CTRLDATA

+VCCIO R3 24.9_1%_4 EDP_RCOMP → E52 EDP_RCOMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

*SKL_ULT
REV = 1

1 OF 20 ?

Reserve EDP_HPD opposites circuit!

Eletro-XTechnical

+3V
R1 *10K/F_4
ULT_EDP_HPD
R2 100K_4

U1D SKL_ULT ?

Need apply PN

37,43 H_PROCHOT# R4 499/F_4 37 EC_PECI
37 PM_THRMTRIP#

CATERR# D63
EC_PECI A54
PROCHOT# C65
PM_THRMTRIP# C63
SKTOCC# A65

CATERR#
PECI
PROCHOT#
THERMTRIP#
SKTOCC#

CPU MISC

TP127 1 XDP_BPM0 C55
TP128 1 XDP_BPM1 D55
BPM#[0] B54
BPM#[1] C56
BPM#[2]
BPM#[3]

TP113 1 3D_FW_GPIO_R A6
TP4 1 CPU_GP1 A7
TP5 1 CPU_GP2 BA5
TP6 1 CPU_GP3 AY5

GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3

R8 49.9/F_4 PROC_POPIRCOMP AT16
R11 49.9/F_4 PCH_OPI_RCOMP AU16
R12 49.9/F_4 EDRAM_OPIO_RCOMP H66
R14 49.9/F_4 EOPIO_RCOMP H65

PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

JTAG

PROC_TCK B61 XDP_TCK0
PROC_TDI D60 XDP_TDI_CPU 1 TP999
PROC_TDO A61 XDP_TDO_CPU
PROC_TMS C60 XDP_TMS_CPU 1 TP998
PROC_TRST# B59 PROC_TRST#

PCH_JTAG_TCK B56 JTAG_TCK_PCH
PCH_JTAG_TDI D59 JTAG_TDI_PCH
PCH_JTAG_TDO A56 JTAG_TDO_PCH
PCH_JTAG_TMS C59 JTAG_TMS_PCH
PCH_TRST# C61 XDP_TRST#_CPU
JTAGX A59 JTAGX_PCH

XDP_TRST#_CPU R863 0_4 PROC_TRST#

*SKL_ULT
REV = 1

4 OF 20 ?

+VCCSTPLL
R6 *49.9/F_4 CATERR#

+1.0V
R9 *0_4/S
R10 *51_4 JTAGX_PCH
R13 51_4 JTAG_TMS_PCH
R15 51_4 JTAG_TDI_PCH
R16 51_4 JTAG_TDO_PCH
R18 51_4 JTAG_TCK_PCH
Close to Chipset

Close to EC

+VCCSTPLL
PM_THRMTRIP# R5 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

PLACE NEAR CPU

+1.0V
XDP_TMS_CPU R17 *51_4
XDP_TDI_CPU R19 *51_4
XDP_TDO_CPU R20 *51_4

+1.0V
H_PROCHOT# R21 1K_4
XDP_TCK0 R22 51_4
XDP_TRST#_CPU R23 51_4

Eletro-XTechnical

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	02 -- SKYPAKE 1/15 (eDP/DDI)	1A
Date: Tuesday, December 13, 2016	Sheet 2 of 51	

17 M_A_DQSN[7:0]
17 M_A_DQSP[7:0]
18 M_B_DQSN[7:0]
18 M_B_DQSP[7:0]
17 M_A_DQ[63:0]
18 M_B_DQ[63:0]

+1.2VSUS 6,17,18,40,42,48

SkyLake ULT Processor (DDR4)

Need apply PN

U1B SKL_ULT

M_A_DQ0 AL71 … M_A_DQ31 AT60 → DDR0_DQ[0] … DDR0_DQ[31]

DDR0_CKN[0] AU53
DDR0_CKP[0] AT53
DDR0_CKN[1] AU55
DDR0_CKP[1] AT55
DDR0_CKE[0] BA56
DDR0_CKE[1] BB56
DDR0_CKE[2] AW56
DDR0_CKE[3] AY56
DDR0_CS#[0] AU45
DDR0_CS#[1] AU43
DDR0_ODT[0] AT45
DDR0_ODT[1] AT43

M_A_CLKN0 17
M_A_CLKP0 17
M_A_CLKN1 17
M_A_CLKP1 17
M_A_CKE0 17
M_A_CKE1 17
M_A_CS#0 17
M_A_CS#1 17
M_A_DIM0_ODT0 17
M_A_DIM0_ODT1 17

DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5] BA51 M_A_A5
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9] BB54 M_A_A9
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6] BA52 M_A_A6
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8] AY52 M_A_A8
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7] AW52 M_A_A7
DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0] AY55 M_A_BG#0
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12] AW54 M_A_A12
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11] BA54 M_A_A11
DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT# BA55
DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1] AY54

M_A_A5 17
M_A_A9 17
M_A_A6 17
M_A_A8 17
M_A_A7 17
M_A_BG#0 17
M_A_A12 17
M_A_A11 17
M_A_ACT# 17
M_A_BG#1 17

DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13] AU46 M_A_A13
DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15] AU48
DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14] AT46
DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16] AU50
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0] AU52
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2] AY51 M_A_A2
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1] AT48
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10] AT50 M_A_A10
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1] BB50 M_A_A1
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0] AY50 M_A_A0
DDR0_MA[3] BA50 M_A_A3
DDR0_MA[4] BB52 M_A_A4

M_A_A13 17
M_A_CAS# 17
M_A_WE# 17
M_A_RAS# 17
M_A_BS#0 17
M_A_A2 17
M_A_BS#1 17
M_A_A1 17
M_A_A0 17
M_A_A3 17
M_A_A4 17

DDR0_DQSN[0] AM70 M_A_DQSN0
DDR0_DQSP[0] AM69 M_A_DQSP0
DDR0_DQSN[1] AT69 M_A_DQSN1
DDR0_DQSP[1] AT70 M_A_DQSP1
DDR1_DQSN[0]/DDR0_DQSN[2] AH66 M_B_DQSN0
DDR1_DQSP[0]/DDR0_DQSP[2] AH65 M_B_DQSP0
DDR1_DQSN[1]/DDR0_DQSN[3] AG69 M_B_DQSN1
DDR1_DQSP[1]/DDR0_DQSP[3] AG70 M_B_DQSP1
DDR0_DQSN[2]/DDR0_DQSN[4] BA64 M_A_DQSN2
DDR0_DQSP[2]/DDR0_DQSP[4] AY64 M_A_DQSP2
DDR0_DQSN[3]/DDR0_DQSN[5] AY60 M_A_DQSN3
DDR0_DQSP[3]/DDR0_DQSP[5] BA60 M_A_DQSP3
DDR1_DQSN[2]/DDR0_DQSN[6] AR66 M_B_DQSN2
DDR1_DQSP[2]/DDR0_DQSP[6] AR65 M_B_DQSP2
DDR1_DQSN[3]/DDR0_DQSN[7] AR61 M_B_DQSN3
DDR1_DQSP[3]/DDR0_DQSP[7] AR60 M_B_DQSP3

DDR0_ALERT# AW50 M_A_ALERT#
DDR0_PAR AT52 M_A_PARITY
DDR_VREF_CA AY67 SM_VREF
DDR0_VREF_DQ AY68 SMDDR_VREF_DQ0_M3
DDR1_VREF_DQ BA67 SMDDR_VREF_DQ1_M3
DDR_VTT_CNTL AW67 DDR_VTT_CNTL

M_A_ALERT# 17
M_A_PARITY 17
SM_VREF 17
TP7
SMDDR_VREF_DQ1_M3 18
DDR_VTT_CNTL 18

20mils width

NIL-DDR CH - A

*SKL_ULT
REV = 1
2 OF 20

U1C SKL_ULT

Need apply PN

M_A_DQ32 AY39 … M_A_DQ63 AN21 → DDR0_DQ[32]/DDR1_DQ[0] … DDR0_DQ[63]/DDR1_DQ[31]

DDR1_CKN[0] AN45
DDR1_CKP[0] AN46
DDR1_CKN[1] AP45
DDR1_CKP[1] AP46
DDR1_CKE[0] AN56
DDR1_CKE[1] AP55
DDR1_CKE[2] AN55
DDR1_CKE[3] AP53
DDR1_CS#[0] BB42
DDR1_CS#[1] AY42
DDR1_ODT[0] BA42
DDR1_ODT[1] AW42

M_B_CLKN0 18
M_B_CLKN1 18
M_B_CLKP0 18
M_B_CLKP1 18
M_B_CKE0 18
M_B_CKE1 18
M_B_CS#0 18
M_B_CS#1 18
M_B_DIM0_ODT0 18
M_B_DIM0_ODT1 18

DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5] AY48 M_B_A5
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9] AP50 M_B_A9
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6] BA48 M_B_A6
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8] BB48 M_B_A8
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7] AP48 M_B_A7
DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0] AP52 M_B_BG#0
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12] AN50 M_B_A12
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11] AN48 M_B_A11
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT# AN53
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1] AN52 M_B_BG#1

M_B_A5 18
M_B_A9 18
M_B_A6 18
M_B_A8 18
M_B_A7 18
M_B_BG#0 18
M_B_A12 18
M_B_A11 18
M_B_ACT# 18
M_B_BG#1 18

DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13] BA43 M_B_A13
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15] AY43
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14] AY44
DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16] AW44
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0] BB44
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2] AY47 M_B_A2
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1] BA44
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10] AW46 M_B_A10
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1] AY46 M_B_A1
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0] BA46 M_B_A0
DDR1_MA[3] BB46 M_B_A3
DDR1_MA[4] BA47 M_B_A4

M_B_A13 18
M_B_CAS# 18
M_B_WE# 18
M_B_RAS# 18
M_B_BS#0 18
M_B_A2 18
M_B_BS#1 18
M_B_A1 18
M_B_A0 18
M_B_A3 18
M_B_A4 18

DDR0_DQSN[4]/DDR1_DQSN[0] BA38 M_A_DQSN4
DDR0_DQSP[4]/DDR1_DQSP[0] AY38 M_A_DQSP4
DDR0_DQSN[5]/DDR1_DQSN[1] AY34 M_A_DQSN5
DDR0_DQSP[5]/DDR1_DQSP[1] BA34 M_A_DQSP5
DDR1_DQSN[4]/DDR1_DQSN[2] AT38 M_B_DQSN4
DDR1_DQSP[4]/DDR1_DQSP[2] AR38 M_B_DQSP4
DDR1_DQSN[5]/DDR1_DQSN[3] AT32 M_B_DQSN5
DDR1_DQSP[5]/DDR1_DQSP[3] AR32 M_B_DQSP5
DDR0_DQSN[6]/DDR1_DQSN[4] BA30 M_A_DQSN6
DDR0_DQSP[6]/DDR1_DQSP[4] AY30 M_A_DQSP6
DDR0_DQSN[7]/DDR1_DQSN[5] AY26 M_A_DQSN7
DDR0_DQSP[7]/DDR1_DQSP[5] BA26 M_A_DQSP7
DDR1_DQSN[6] AR25 M_B_DQSN6
DDR1_DQSP[6] AR27 M_B_DQSP6
DDR1_DQSP[7] AT22 M_B_DQSN7
AR21 M_B_DQSP7

DDR1_ALERT# AN43 M_B_ALERT#
DDR1_PARITY AP43 M_B_PARITY
DDR1_PAR AT13 SM_DRAMRST#
DRAM_RESET# AR18 SM_RCOMP_0
DDR_RCOMP[0] AT18 SM_RCOMP_1
DDR_RCOMP[1] AU18 SM_RCOMP_2
DDR_RCOMP[2]

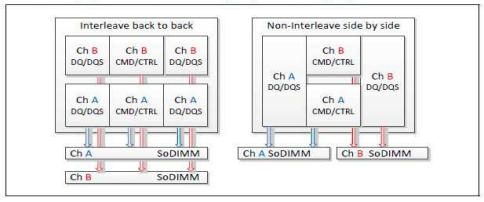
M_B_ALERT# 18
M_B_PARITY 18
DDR3_DRAMRST# 17,18
R25 121/F_4
R26 80.6/F_4
R27 100/F_4

+1.2VSUS
R24 470/F_4

NIL-DDR CH - B

*SKL_ULT
REV = 1
3 OF 20

Interleave (IL) and Non-Interleave (NIL) Modes Mapping

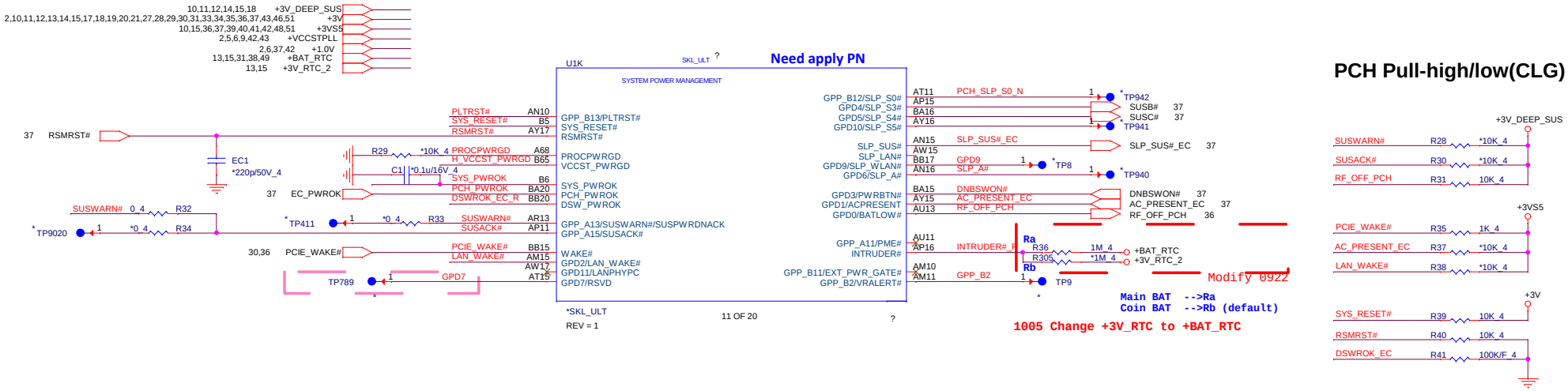


BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	03 -- SKYLAKE 2/15(DDR4 I/F)	1A

Date: Tuesday, December 13, 2016 Sheet 3 of 51



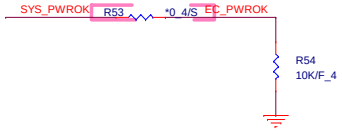
PCH Pull-high/low(CLG)

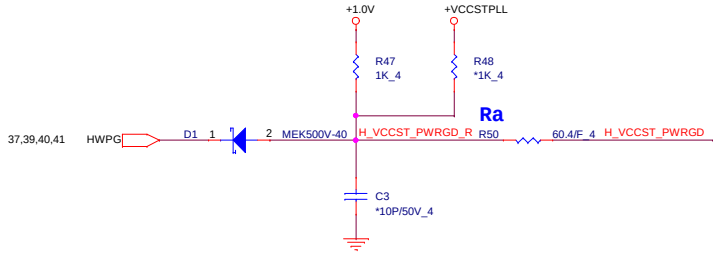
For DS3 Sequence

PLTRST#(CLG)

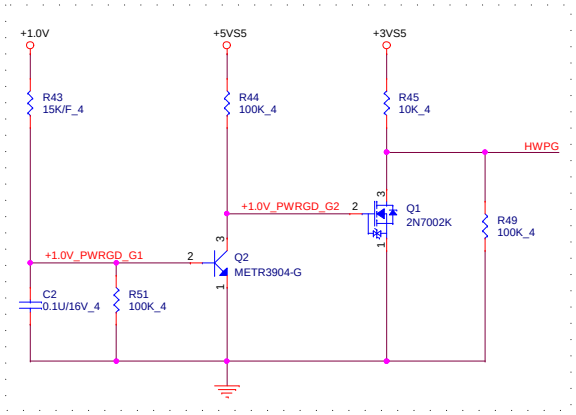
Check Rise/Fall time less than 100ns

System PWR_OK(CLG)





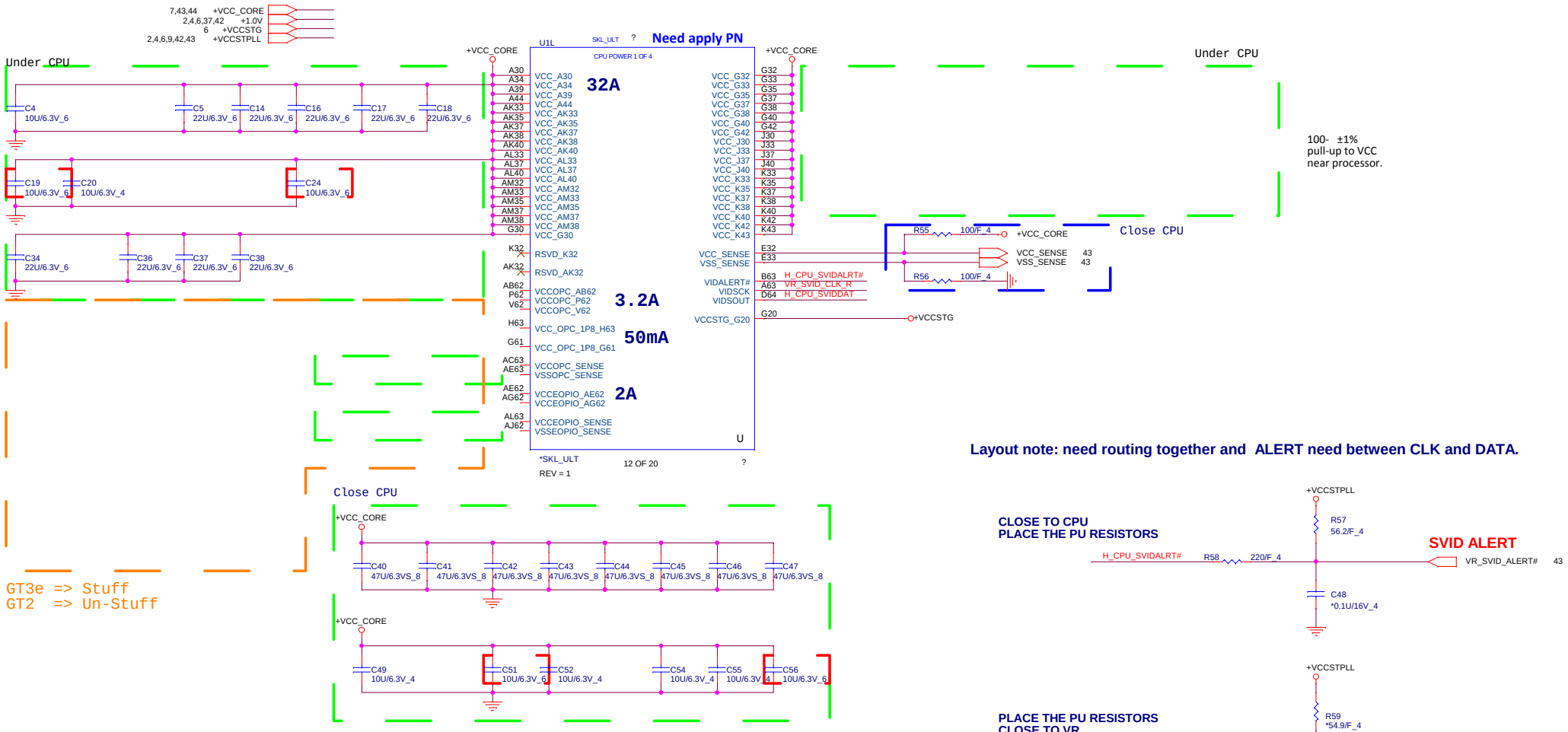
Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	04 -- SKYLAKE 3/15(PowerManger)	1A
Date: Tuesday, December 13, 2016	Sheet 4 of 51	



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

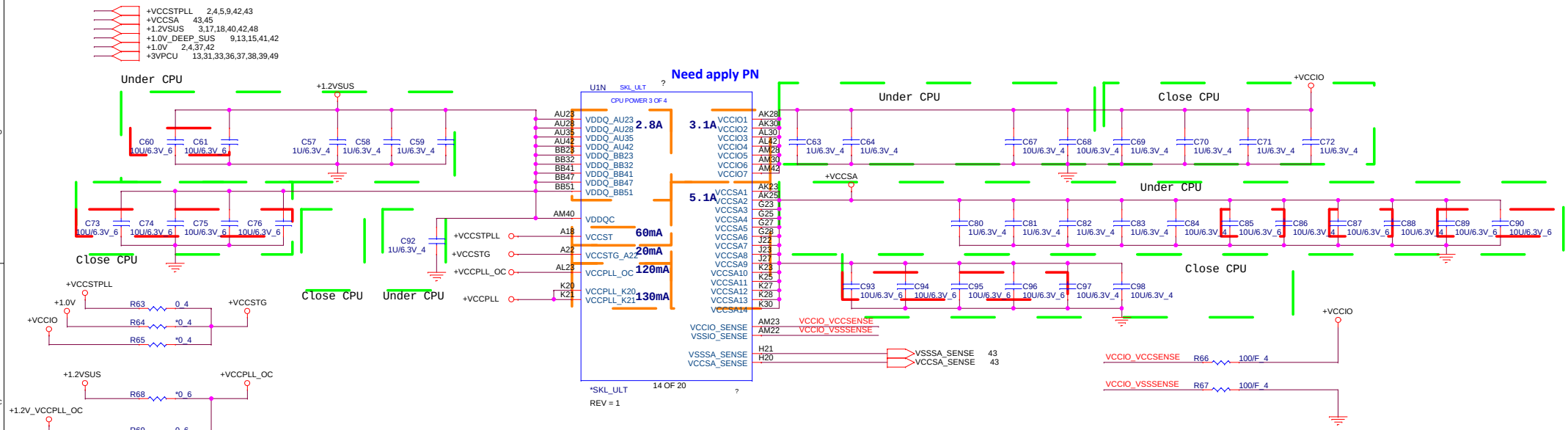
Layout note: need routing together and ALERT need between CLK and DATA.

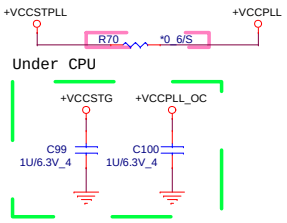
BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	05 -- SKYLAKE 4/15 (POWER-1)	1A

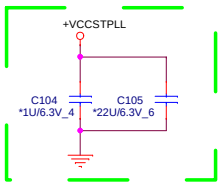
Date: Tuesday, December 13, 2016 Sheet 5 of 51



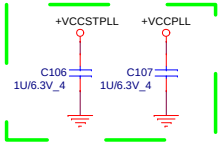


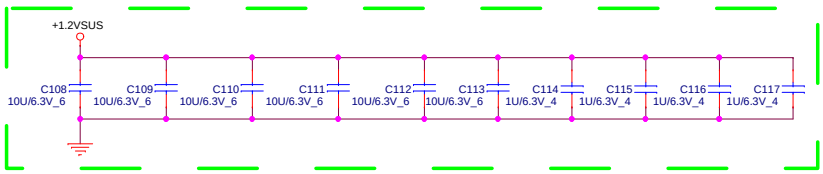
Under CPU

Close A18 Ball



Close CPU

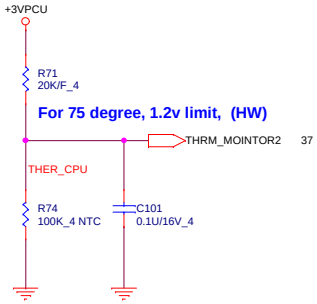




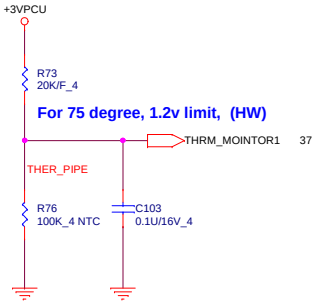
Close to CPU

IO Thrm Protect

For CPU USE



For PIPE USE



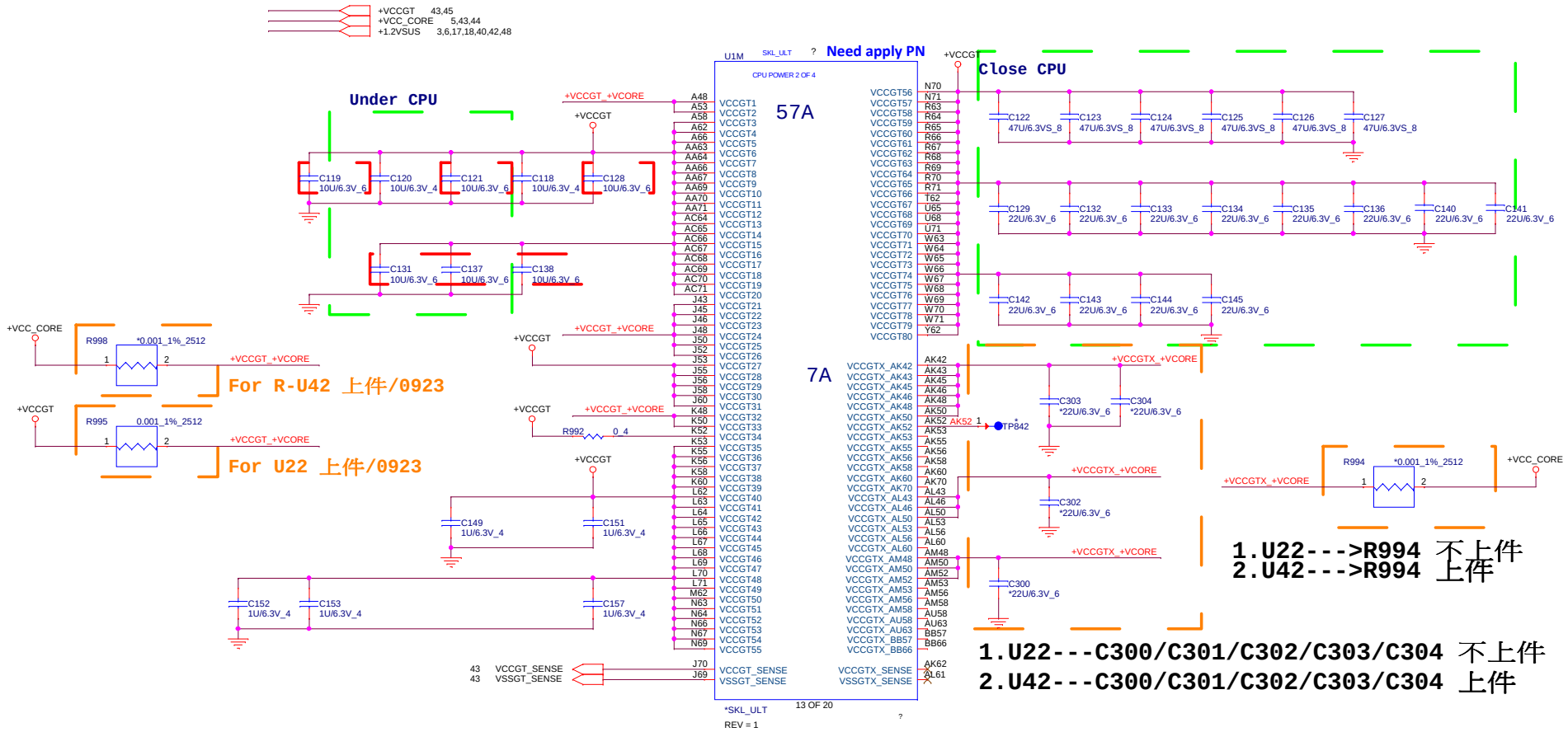
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

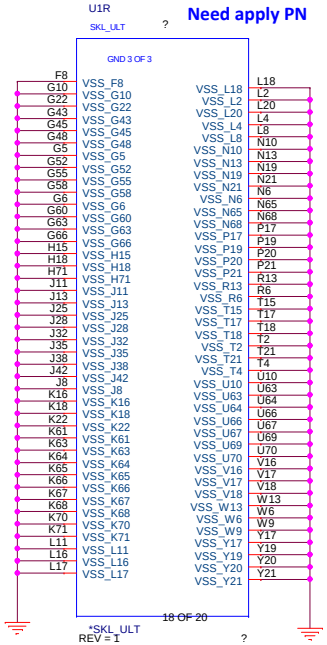
Size	Document Number	Rev
Custom	06 -- SKYLAKE 5/15 (POWER-2)	1A

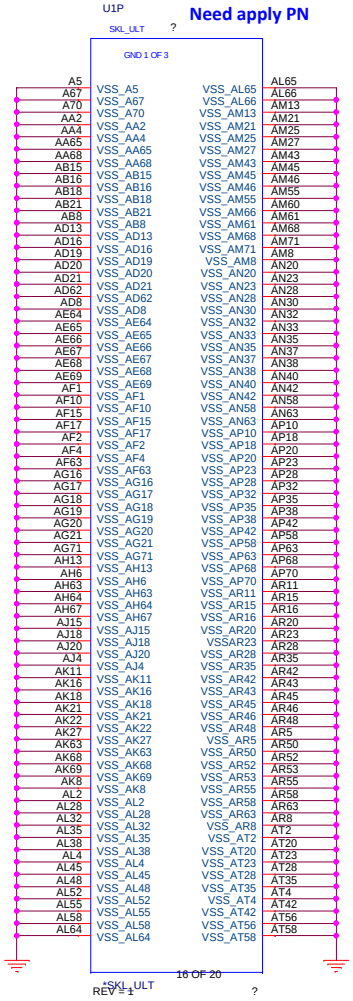
Date: Tuesday, December 13, 2016 Sheet 6 of 51

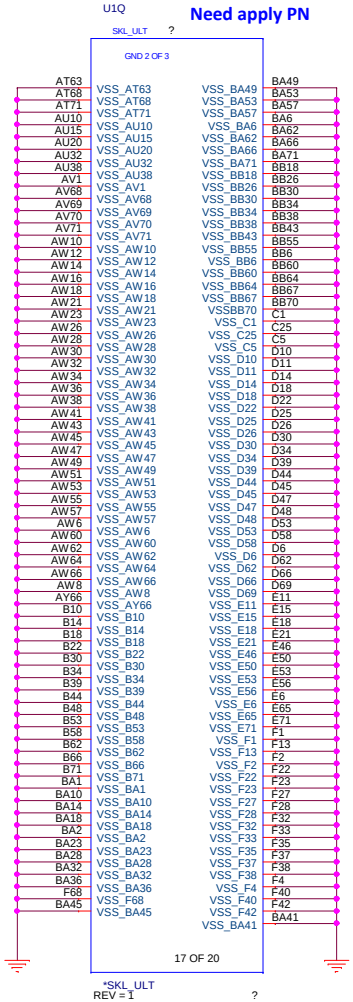


Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.
BU5
Size: Custom | Document Number: 07 -- SKYLAKE 6/15 (POWER-3) | Rev: 1A
Date: Tuesday, December 13, 2016 | Sheet 7 of 51







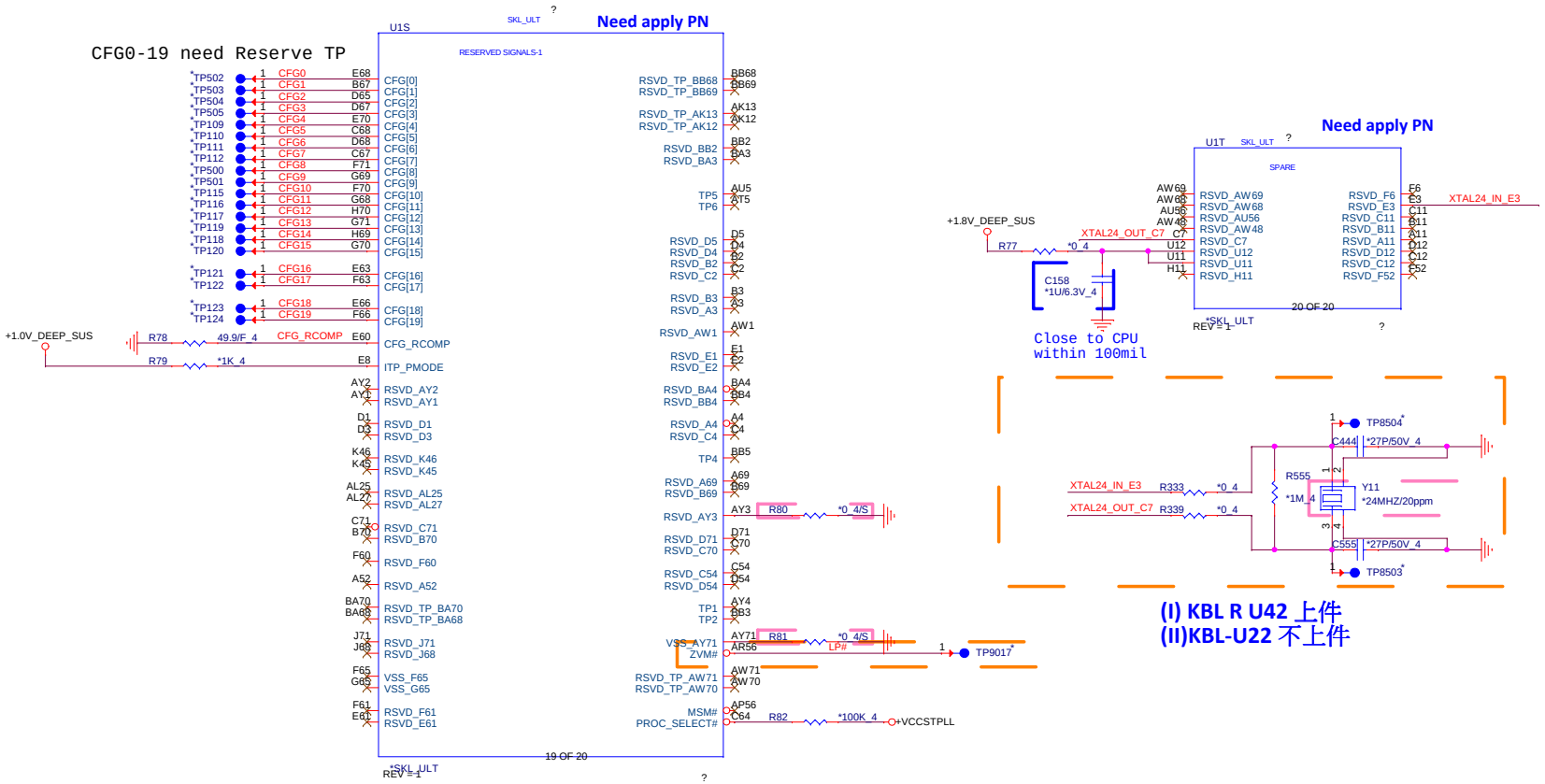
BU5

PROJECT : NFLP_KBLU_DR

Quanta Computer Inc.

Size	Document Number	Rev
Custom	08 -- SKYLAKE 7/15 (GND)	1A

Date: Tuesday, December 13, 2016 | Sheet 8 of 51



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R83 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R84 1K_4

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	09 -- SKYLAKE 8/15 (RSV)	1A

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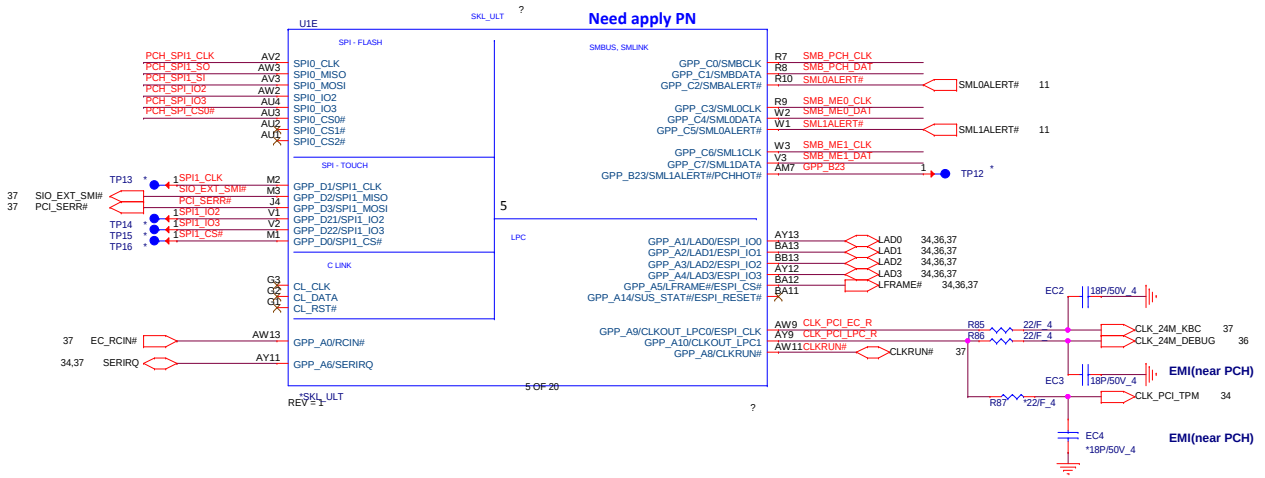
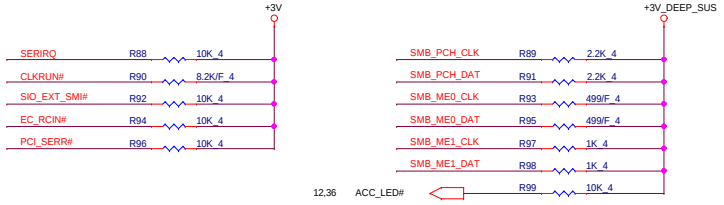
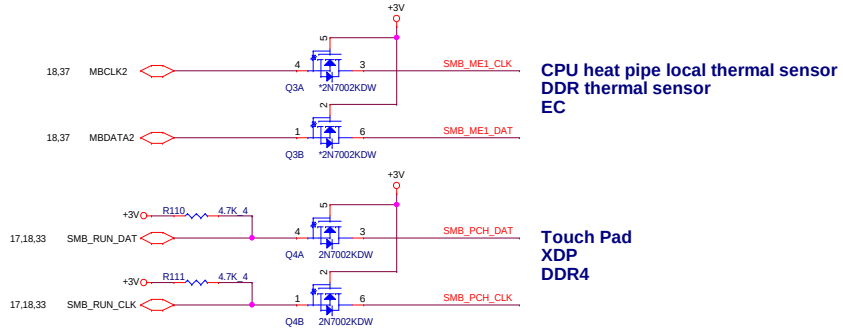
+3V_DEEP_SUS 4,11,12,14,15,18
+3V 2,4,11,12,13,14,15,17,18,19,20,21,27,28,29,30,31,33,34,35,36,37,43,46,51
+5V 27,28,29,33,34,36,51
+1.0V 2,4,6,37,42
+3VS5 4,15,36,37,39,40,41,42,48,51



GPIO Pull UP



SMBus/Pull-up(CLG)

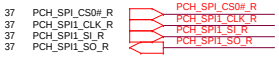


CPU heat pipe local thermal sensor
DDR thermal sensor
EC

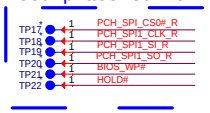
Touch Pad
XDP
DDR4

PCH SPI ROM(CLG)

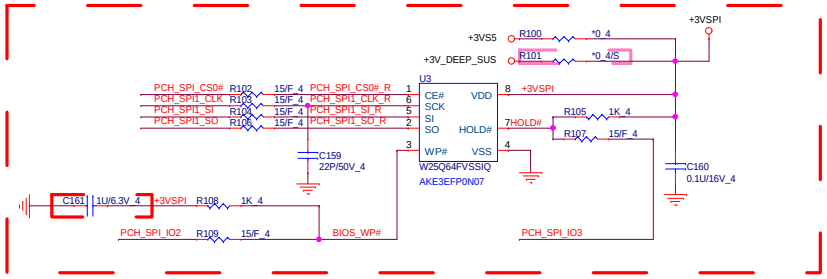
Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023



need place to TOP



PCH SPI ROM(CLG)



1005 Change P/N to DFHS08FS023(Socket)

BU5

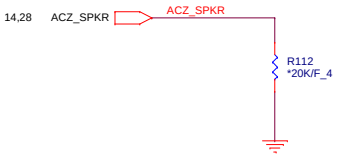
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- SKYLAKE 09/15(SPI/LPC/SM)	1A

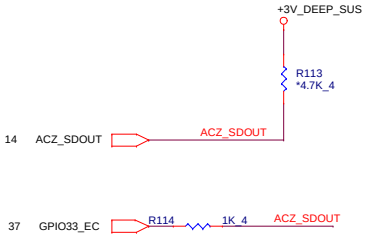
Date: Tuesday, December 13, 2016 Sheet 10 of 51

Functional Strap Definitions

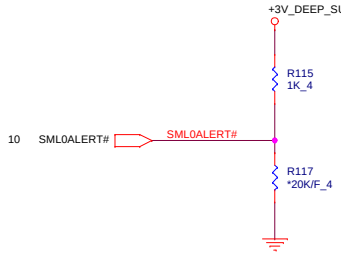
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



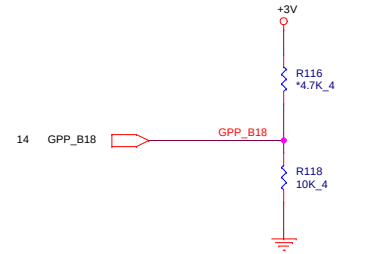
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



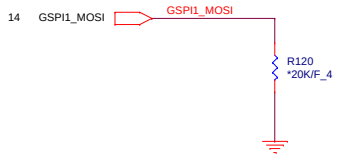
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

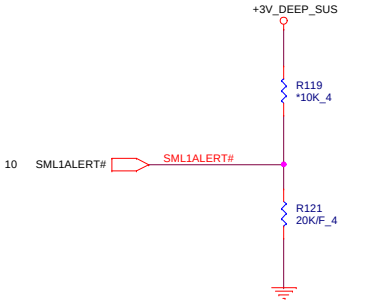


No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO
Timer system reboot feature).
This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	11 -- SKYLAKE 10/15(HDA)	1A

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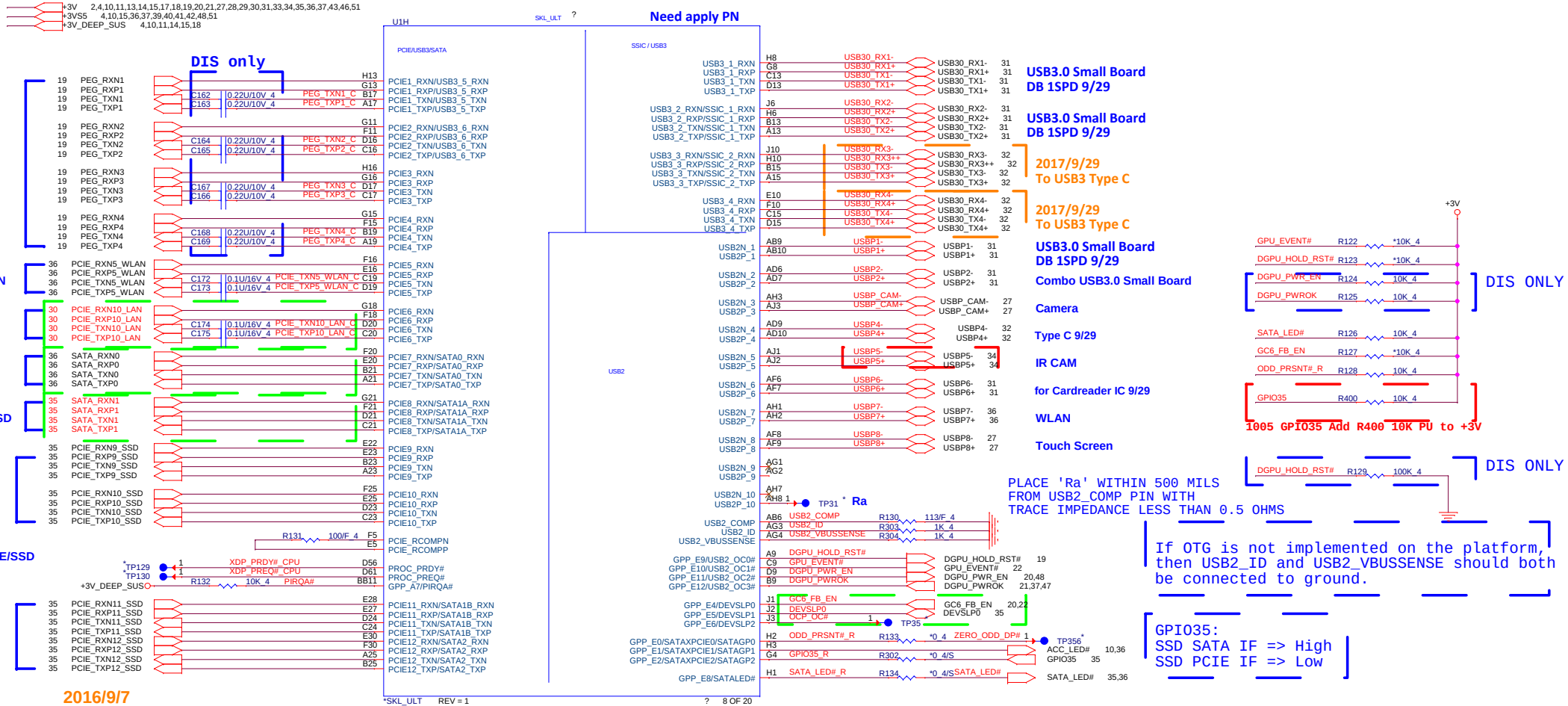

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	VGA
Port2	dGPU	Port1	Un-used
Port3	dGPU	Port2	SSD
Port4	dGPU	Port3	WLAN
Port5	WLAN	Port4	LAN
Port6	LAN	Port5	Un-used
Port7	HDD		
Port8	SATA SSD		
Port9	PCIE_SSD		
Port10	PCIE_SSD		
Port11	PCIE_SSD		
Port12	PCIE_SSD		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	Cobime USB3.0 Small Board
PORT-3	NC
PORT-4	NC

1005 Change Name from DEVSLP2 to DEVSLP0
DEVSLP0 and GC6_FB_EN SWAP
1005 GPIO35 and ACC_LED# SWAP

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	USB3.0 Small Board
PORT-2	USB3.0 Small Board
PORT-3	Camera
PORT-4	Type C
PORT-5	IR CAM
PORT-6	Cardreader IC
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.
BU5
Size: Custom | Document Number: 11 -- SKYLAKE 10/15(HDA) | Rev: 1A
Date: Tuesday, December 13, 2016 | Sheet 12 of 51

+3V_RTC_2 4,15
+BAT_RTC 4,15,31,38,49
+1.8V_DEEP_SUS 9,15,41
+3V 2,4,10,11,12,14,15,17,18,19,20,21,27,28,29,30,31,33,34,35,36,37,43,46,51

VGA
Cardreader
SSD
WLAN
LAN

U1J SKL_ULT ? Need apply PN
CLOCK SIGNALS
CLKOUT_PCIE_N0 CLKOUT_PCIE_P0 GPP_B5/SRCCLKREQ0#
CLKOUT_PCIE_N1 CLKOUT_PCIE_P1 GPP_B6/SRCCLKREQ1#
CLKOUT_PCIE_N2 CLKOUT_PCIE_P2 GPP_B7/SRCCLKREQ2#
CLKOUT_PCIE_N3 CLKOUT_PCIE_P3 GPP_B8/SRCCLKREQ3#
CLKOUT_PCIE_N4 CLKOUT_PCIE_P4 GPP_B9/SRCCLKREQ4#
CLKOUT_PCIE_N5 CLKOUT_PCIE_P5 GPP_B10/SRCCLKREQ5#
CLKOUT_ITPXDP_N CLKOUT_ITPXDP_P GPD8/SUSCLK XTAL24_IN XTAL24_OUT XCLK_BIASREF RTCX1 RTCX2 SRTCRST# RTCRST#
TBT
10 OF 20
*SKL_ULT REV = 1

CLK_VGA_N CLK_VGA_P PCIE_CLKREQ_VGA#
CLK_PCIE_SSDN CLK_PCIE_SSDP PCIE_CLKREQ_CR# PCIE_CLKREQ_SSD#
CLK_PCIE_WLANN CLK_PCIE_WLANP PCIE_CLKREQ_WLAN#
CLK_PCIE_LANN CLK_PCIE_LANP PCIE_CLKREQ_LAN#
PCIE_CLKREQ5#

CK_XDP_N_R CK_XDP_P_R TP125 TP126
XTAL24_IN XTAL24_OUT
XCLK_BIASREF
RTC_X1 RTC_X2 TP38
SRTCRST# SRTC_RST#

+1.0V_DEEP_SUS
R135 2.7K/F_4
XCLK_BIASREF
R137 *60.4/F_4

CLK_REQ/Strap Pin(CLG)
+3V
PCIE_CLKREQ_VGA# R136 10K_4
PCIE_CLKREQ_WLAN# R138 10K_4
PCIE_CLKREQ_LAN# R139 10K_4
PCIE_CLKREQ_CR# R140 10K_4
PCIE_CLKREQ_SSD# R141 10K_4
PCIE_CLKREQ5# R142 10K_4

U1I SKL_ULT ? Need apply PN
CSI-2
CSI2_DN0 CSI2_DP0 CSI2_DN1 CSI2_DP1 CSI2_DN2 CSI2_DP2 CSI2_DN3 CSI2_DP3
CSI2_DN4 CSI2_DP4 CSI2_DN5 CSI2_DP5 CSI2_DN6 CSI2_DP6 CSI2_DN7 CSI2_DP7
CSI2_DN8 CSI2_DP8 CSI2_DN9 CSI2_DP9 CSI2_DN10 CSI2_DP10 CSI2_DN11 CSI2_DP11
CSI2_CLKN0 CSI2_CLKP0 CSI2_CLKN1 CSI2_CLKP1 CSI2_CLKN2 CSI2_CLKP2 CSI2_CLKN3 CSI2_CLKP3
CSI2_COMP GPP_D4/FLASHTRIG
EMMC
GPP_F13/EMMC_DATA0 GPP_F14/EMMC_DATA1 GPP_F15/EMMC_DATA2 GPP_F16/EMMC_DATA3 GPP_F17/EMMC_DATA4 GPP_F18/EMMC_DATA5 GPP_F19/EMMC_DATA6 GPP_F20/EMMC_DATA7
GPP_F21/EMMC_RCLK GPP_F22/EMMC_CLK GPP_F12/EMMC_CMD
EMMC_RCOMP
9 OF 20
*SKL_ULT REV = 1

GPP_D4 R143 100/F_4 TP39
EMMC_RCOMP R144 200/F_4
1005 Delete TP

RTC Clock 32.768KHz

C177 15P/50V_4 RTC_X1
Y1 32.768KHZ/20ppm
R147 10M_4
C179 15P/50V_4 RTC_X2

RTC Circuitry(RTC)

Main BAT -->Ra
Coin BAT -->Rb (default)
+3V_RTC_2 +BAT_RTC 30mils
Rb R306 *0_4
Ra R307 0_4
R145 *0_6 RTC_RST#
R146 20K/F_4
C178 1U/6.3V_4
R149 20K/F_4 SRTC_RST#
C182 1U/6.3V_4
RTC Power trace width 20mils.
+3V_RTC_0
+3VPCUO
+3V_RTC_1
R150 1K_4
D2 BAT54CW-7-F
C181 1U/6.3V_4
R9042 *0_6
R9041 0_6
RTC_RST# R152 *0_6 SRTC_RST#
CN101 *BAT_CONN DFHS02FS027 BAT-23_2-4_2
CN11 88266-020L

R151 10K_4
EC_RTC_RST 37
RTC_RST#
Q5A 2N7002KDW
R942 *0_4
EC_SRTC_RST 37
SRTC_RST#
Q5B 2N7002KDW
R153 10K_4

External Crystal

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

TP51 C176 27P/50V_4
XTAL24_IN R666 0_4
XTAL24_OUT R667 0_4
R148 1M_4
Y2 24MHZ/20ppm
C180 27P/50V_4
TP52

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	13 – SKYLAKE 12/15 (CLK/EMMC)	1A

Date: Tuesday, December 13, 2016 Sheet 13 of 51

Skylake (GPIO)

+3V 2,4,10,11,12,13,15,17,18,19,20,21,27,28,29,30,31,33,34,35,36,37,43,46,51
+3V_DEEP_SUS 4,10,11,12,15,18

+3V_DEEP_SUS
BT_OFF R154 10K_4
PCH_TEMPALERT# R155 10K_4
SIO_EXT_SCI# R156 10K_4
UART2_RXD R157 49.9K/F_4
UART2_TXD R158 49.9K/F_4
SPK_ID R401 10K_4

+3V
ACCEL_INTA# R159 10K_4

U1F SKL_ULT ? Need apply PN

LPSS
11 GPP_B18
33 TP_INTH#_BIOS
11 GSPI1_MOSI
1005 Delete TP
34 ACCEL_INTA#
37 SIO_EXT_SCI#
33 TP_I2C_DATA
33 TP_I2C_CLK
1005 Delete TP

GPP_B15/GSPI0_CS# AN8
GPP_B16/GSPI0_CLK AP7
GPP_B17/GSPI0_MISO AP8
GPP_B18/GSPI0_MOSI AR7
GPP_B19/GSPI1_CS# AM5
GPP_B20/GSPI1_CLK AN7
GPP_B21/GSPI1_MISO AP5
GPP_B22/GSPI1_MOSI AN5
GPP_C8/UART0_RXD AB1
GPP_C9/UART0_TXD AB2
GPP_C10/UART0_RTS# W2
GPP_C11/UART0_CTS# AB5
GPP_C20/UART2_RXD AD1
GPP_C21/UART2_TXD AD2
GPP_C22/UART2_RTS# AD3
GPP_C23/UART2_CTS# AD4
GPP_C16/I2C0_SDA U7
GPP_C17/I2C0_SCL U6
GPP_C18/I2C1_SDA U8
GPP_C19/I2C1_SCL U9
GPP_F4/I2C2_SDA AH9
GPP_F5/I2C2_SCL AH10
GPP_F6/I2C3_SDA AH11
GPP_F7/I2C3_SCL AH12
GPP_F8/I2C4_SDA AF11
GPP_F9/I2C4_SCL AF12

*SKL_ULT REV = 1
6 OF 20

ISH
GPP_D9 P2
GPP_D10 P3
GPP_D11 P4
GPP_D12 P1
GPP_D9 1 3D_CAM_EN_PCH 1 TP114
SPK_ID 28 BT_OFF 36
GPP_D5/ISH_I2C0_SDA M4 ISH_I2C0_SDA 1 TP61
GPP_D6/ISH_I2C0_SCL N3 ISH_I2C0_SCL 1 TP62
1005 Delete TP
GPP_D7/ISH_I2C1_SDA N1
GPP_D8/ISH_I2C1_SCL U2
GPP_F10/I2C5_SDA/ISH_I2C2_SDA AD11
GPP_F11/I2C5_SCL/ISH_I2C2_SCL AD12
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA U1 PCH_TEMPALERT# 1 TP71
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL U2 SML0BDATA 1 TP72
GPP_D15/ISH_UART0_RTS# U3 SML0BCLK 1 TP73
GPP_D16/ISH_UART0_CTS#/SML0BALERT# U4 SML0BALERT# 1 TP74
1005 Delete TP
GPP_C12/UART1_RXD/ISH_UART1_RXD AC1
GPP_C13/UART1_TXD/ISH_UART1_TXD AC2
GPP_C14/UART1_RTS#/ISH_UART1_RTS# AC3
GPP_C15/UART1_CTS#/ISH_UART1_CTS# AB4
GPP_A18/ISH_GP0 AY8
GPP_A19/ISH_GP1 BA8
GPP_A20/ISH_GP2 BB7
GPP_A21/ISH_GP3 BA7
GPP_A22/ISH_GP4 AY7
GPP_A23/ISH_GP5 AW7
GPP_A12/BM_BUSY#/ISH_GP6 AP13

?

HDA Bus(CLG)

close to CPU/1004

+3V_DEEP_SUS
28 ACZ_SYNC_AUDIO
28 ACZ_RST#_AUDIO
28 ACZ_SDOUT_AUDIO
28 BIT_CLK_AUDIO
R160 *1K_4 ACZ_SYNC
R161 33_4 ACZ_SYNC
R162 33_4 ACZ_RST#
R165 33_4 ACZ_SDOUT
R168 33_4 ACZ_BCLK
C183 15P/50V_4
ACZ_SDOUT
ACZ_RST#
ACZ_SDIN0
C647 33P/50V_4
C648 33P/50V_4
C649 33P/50V_4

R163 *10K_4 BOARD_ID0 R164 10K_4 +3V_DEEP_SUS
R166 *10K_4 BOARD_ID1 R167 10K_4
R169 10K_4 BOARD_ID2 R170 *10K_4
R171 *10K_4 BOARD_ID3 R172 10K_4
R173 *10K_4 BOARD_ID4 R174 10K_4
R175 10K_4 BOARD_ID5 R176 10K_4
R177 10K_4 BOARD_ID6 R178 *10K_4
R179 10K_4 BOARD_ID7 R180 *10K_4
R181 10K_4 BOARD_ID8 R182 *10K_4

U1G SKL_ULT ? Need apply PN

AUDIO
11 ACZ_SDOUT
28 ACZ_SDIN0
ACZ_RST#
1005 Delete TP
11,28 ACZ_SPKR

ACZ_SYNC BA22
ACZ_BCLK AY22
ACZ_SDOUT BB22
ACZ_SDIN0 BA21
AY21
AW22
J5
AY20
AW20
HDA_SYNC/I2S0_SFRM
HDA_BLK/I2S0_SCLK
HDA_SDO/I2S0_TXD
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_RST#/I2S1_SCLK
GPP_D23/I2S_MCLK
I2S1_SFRM
I2S1_TXD
AK7
AK5
AK3
AK10
GPP_F1/I2S2_SFRM
GPP_F0/I2S2_SCLK
GPP_F2/I2S2_TXD
GPP_F3/I2S2_RXD
H5
D5
GPP_D19/DMIC_CLK0
GPP_D20/DMIC_DATA0
D8
C5
GPP_D17/DMIC_CLK1
GPP_D18/DMIC_DATA1
ACZ_SPKR AW5
GPP_B14/SPKR

*SKL_ULT REV = 1
7 OF 20

SDIO/SDXC
GPP_G0/SD_CMD AB11 BOARD_ID0
GPP_G1/SD_DATA0 AB13 BOARD_ID1 BOARD_ID1 27
GPP_G2/SD_DATA1 AB12 BOARD_ID2
GPP_G3/SD_DATA2 W12 BOARD_ID3
GPP_G4/SD_DATA3 W11 BOARD_ID4
GPP_G5/SD_CD# W10 BOARD_ID5
GPP_G6/SD_CLK W8 BOARD_ID6
GPP_G7/SD_WP W7 BOARD_ID7
GPP_A17/SD_PWR_EN#/ISH_GP7 BA9 BOARD_ID8
GPP_A16/SD_1P8_SEL BB9 GPP_A16
GPP_A16 31
SD_RCOMP AB7 R183 200/F_4
GPP_F23 AF13 GPP_F23 1 TP100

Skylake U	BOARD_ID[8:7]	BOARD_ID[6:5]	BOARD_ID 5	Board ID 4	Board ID 3	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6 ID5	ID5	ID4	ID3	ID2 ID1	ID0
Definition	Reserve (Default = 00)	Reserve (Default = 00)	0 : AMD 1 : Nvidia	0 4 VRAMs 1 8 VRAMs	0 VGA CAM 1 IR CAM	00 14" 01 15" 1SPD 10 17" 11 2SPD	0 : UMA 1 : DIS

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	14 -- SKYLAKE 13/15 (GPIO)	1A
Date: Tuesday, December 13, 2016	Sheet 14 of 51	

4,10,11,12,14,18 +3V_DEEP_SUS
9,13,41,42 +1.0V_DEEP_SUS
9,41 +1.8V_DEEP_SUS
4,13,31,38,49 +BAT_RTC
4,10,36,37,39,40,41,42,48,51 +3VS5

U1O SKL_ULT

CPU POWER 4 OF 4

Need apply PN

PCH Internal VRM

Ca and Cb close to CPU less then 100 mils

Ca

2.899A

2.57A

1.714A

0.03A

0.09A

close to CPU/1004

120/300MA

L668

C654 3P/50V_4

C653 3P/50V_4

R201 *0_4/S

+VCCPRIM C184 1U/6.3V_4

+1.0V_DEEP_SUS C185 1U/6.3V_4

+VCCDSW_1.0V C187 1U/6.3V_4

+1.0V_DEEP_SUS R188 *0_6/S C188 1U/6.3V_4

+1.0V_DEEP_SUS C189 1U/6.3V_4 C190 47U/6.3VS_8

+1.0V_DEEP_SUS R194 *0_6/S C192 1U/6.3V_4

+1.0V_DEEP_SUS R199 *0_6/S

+3V_DEEP_SUS R205 *0_6/S

+1.0V_DEEP_SUS R206 *0_6/S C196 1U/6.3V_4

+3V_DEEP_SUS R207 *0_6/S

+1.0V_DEEP_SUS R208 *0_6/S

+1.0V_DEEP_SUS R209 *0_6/S C197 1U/6.3V_4

+3V3DX_1.5DX_ADO C193 1U/6.3V_4

+3V3DX_1.5DX_ADO C194 1U/6.3V_4

AB19	VCCPRIM_1P0_AB19	
AB20	VCCPRIM_1P0_AB20	+VCCPRIM
P18	VCCPRIM_1P0_P18	
AF18	VCCPRIM_CORE_AF18	
AF19	VCCPRIM_CORE_AF19	
V20	VCCPRIM_CORE_V20	
V21	VCCPRIM_CORE_V21	
AL1	DCPDSW_1P0	+VCCDSW_1.0V
K17	VCCMPHYAON_1P0_K17	
L1	VCCMPHYAON_1P0_L1	+VCCMPHYAON_1P0
N15	VCCMPHYGT_1P0_N15	
N16	VCCMPHYGT_1P0_N16	
N17	VCCMPHYGT_1P0_N17	
P15	VCCMPHYGT_1P0_P15	
P16	VCCMPHYGT_1P0_P16	
K15	VCCAMPHYPLL_1P0_K15	+VCCAMPHYPLL_1P0
L15	VCCAMPHYPLL_1P0_L15	
V15	VCCAPLL_1P0	+VCCAPLL_1.0V
AB17	VCCPRIM_1P0_AB17	+VCCPRIM
Y18	VCCPRIM_1P0_Y18	
AD17	VCCDSW_3P3_AD17	
AD18	VCCDSW_3P3_AD18	
AJ17	VCCDSW_3P3_AJ17	
AJ19	VCCHDA	
AJ16	VCCSPI	+VCCSPI
AF20	VCCSRAM_1P0_AF20	
AF21	VCCSRAM_1P0_AF21	
T19	VCCSRAM_1P0_T19	
T20	VCCSRAM_1P0_T20	+VCCSRAM_1.0V
AJ21	VCCPRIM_3P3_AJ21	+VCCPRIM_3.3V
AK20	VCCPRIM_1P0_AK20	+VCCPRIM_1.0V
N18	VCCAPLLEBB	+VCCAPLLEBB

15 OF 20

*SKL_ULT REV = 1

AK15	VCCPGPPA	+VCCPGPPA
AG15	VCCPGPPB	+VCCPGPPB
Y16	VCCPGPPC	+VCCPGPPC
Y15	VCCPGPPD	+VCCPGPPD
T16	VCCPGPPE	+VCCPGPPE
AF16	VCCPGPPF	+VCCPGPPF
AD15	VCCPGPPG	+VCCPGPPG
V19	VCCPRIM_3P3_V19	+3V_DEEP_SUS
T1	VCCPRIM_1P0_T1	+VCCPRIM_1.0V_T1
AA1	VCCATS_1P8	+VCCATS_1.8V
AK17	VCCRTCPRIM_3P3	+VCCRTCPRIM_3.3V
AK19	VCCRTC_AK19	+VCCRTC
BB14	VCCRTC_BB14	
BB10	DCPRTC	DCPRTC
A14	VCCCLK1	+VCCCLK1
K19	VCCCLK2	+VCCCLK2
L21	VCCCLK3	+VCCCLK3
N20	VCCCLK4	+VCCCLK4
L19	VCCCLK5	+VCCCLK5
A10	VCCCLK6	+VCCCLK6
AN11	GPP_B0/CORE_VID0	CORE_VID0
AN13	GPP_B1/CORE_VID1	CORE_VID1

C186 1U/6.3V_4

R187 *0_6/S +1.0V_DEEP_SUS

R190 *0_6/S +1.8V_DEEP_SUS

R192 *0_6/S +3V_DEEP_SUS

Ra R308 0_4 +BAT_RTC

Rb R309 *0_4 +3V_RTC_2

20mils

Main BAT -->Ra

Coin BAT -->Rb (default)

Cb C191 0.1U/16V_4

1005 Change +3V_RTC to +BAT_RTC

R195 *0_6/S

R198 *0_6/S

R200 *0_6/S

R202 *0_6/S

R203 *0_6/S

R204 *0_6/S

C195 1U/6.3V_4

TP102 TP103

+3V_DEEP_SUS

+VCCPGPPA R184 *0_6/S

+VCCPGPPB R185 *0_6/S

+VCCPGPPC R186 *0_6/S

+VCCPGPPD R189 *0_6/S

+VCCPGPPE R191 *0_6/S

+VCCPGPPG R193 *0_6/S

+1.8V_DEEP_SUS

+VCCPGPPF R197 *0_6/S

close to CPU/1004

+V3.3DX_1.5DX_ADO

L666 120/300MA +3V

C651 3P/50V_4

C650 3P/50V_4

+1.0V_DEEP_SUS

C203 *1U/6.3V_4

C204 *22U/6.3V_6

for DS3

+3VS5

R211 100K_4

C205 1U/6.3V_4

U4

VIN#1 VOUT

VIN#2 GND

EN

AP2821KTR-G1

37,41,42 SLP_SUS_ON

C210 *10P/50V_4

C209 0.1U/16V_4

+3V_DEEP_SUS

+VCCATS_1.8V C198 1U/6.3V_4

+VCCRTC C199 0.1U/16V_4 C200 1U/6.3V_4

+VCCRTCPRIM_3.3V C201 1U/6.3V_4 C202 0.1U/16V_4

+VCCPGPPB C206 1U/6.3V_4

+VCCPGPPC C207 1U/6.3V_4

+VCCPGPPE C208 1U/6.3V_4

BU5

PROJECT : NFLP_KBLU_DR

Quanta Computer Inc.

Size	Document Number	Rev
Custom	15 -- SKYLAKE 14/15(PCH POWER)	1A

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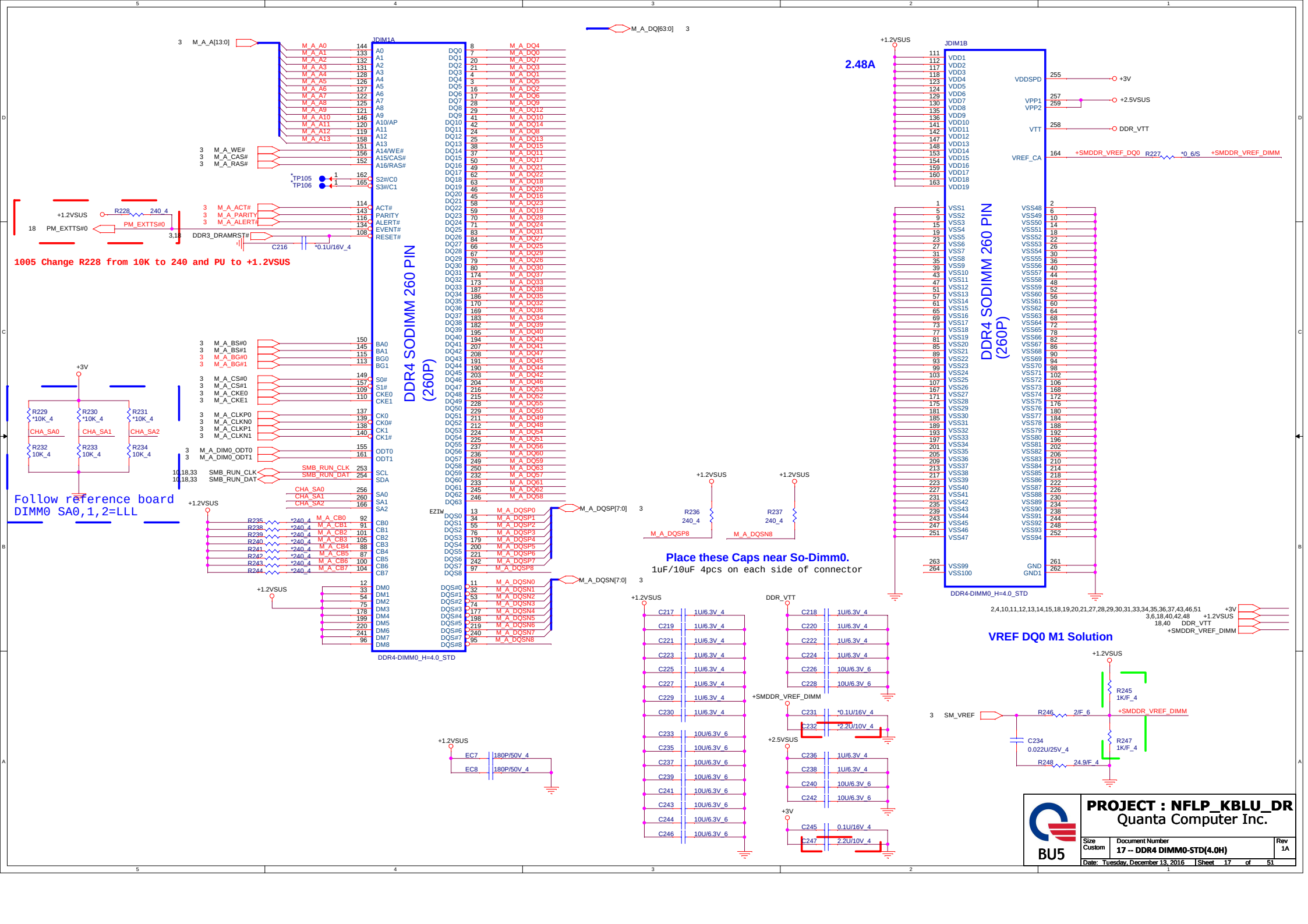
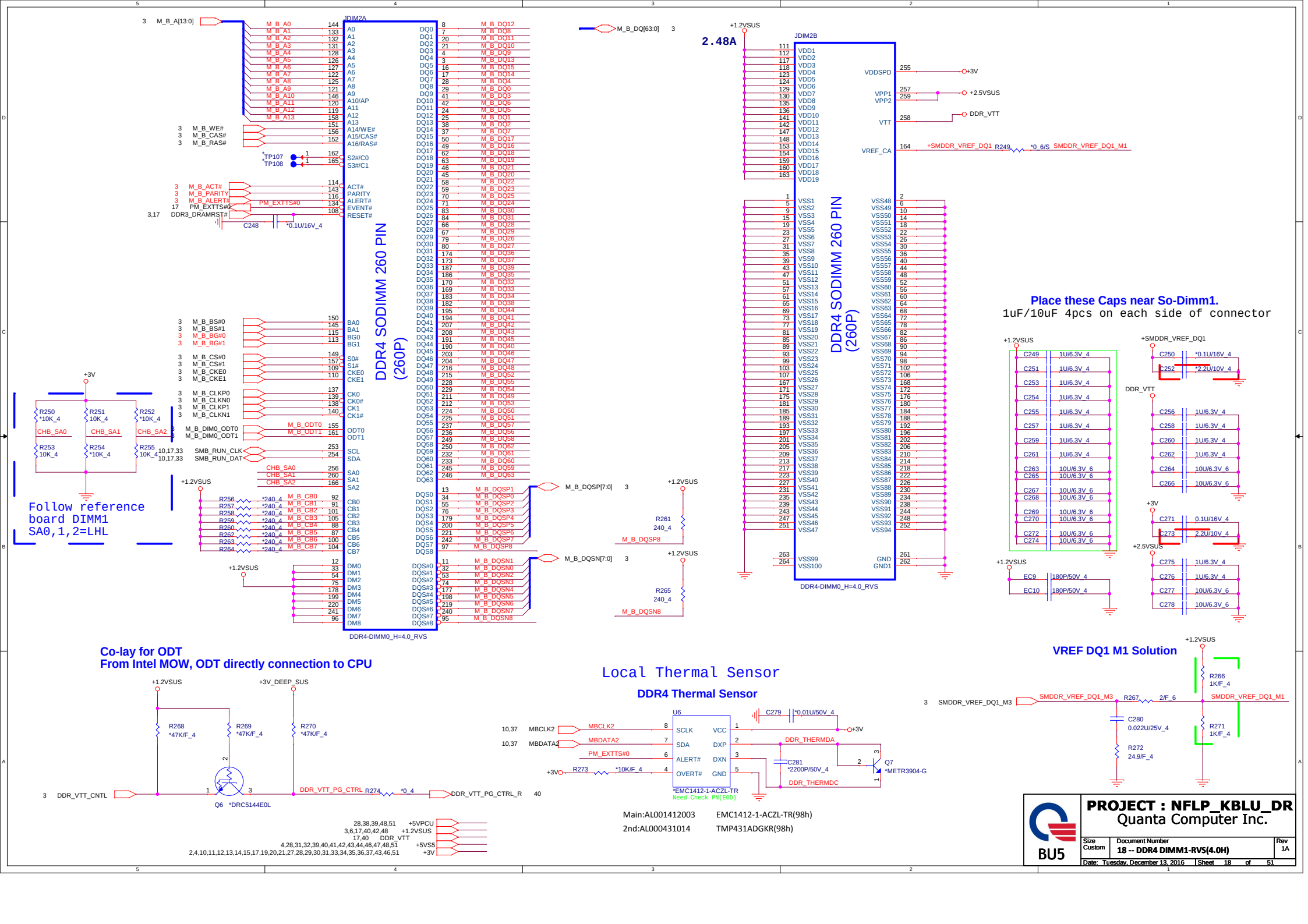

JDIM1A
DDR4 SODIMM 260 PIN
(260P)
DDR4-DIMM0_H=4.0_STD
JDIM1B
DDR4 SODIMM 260 PIN
(260P)
DDR4-DIMM0_H=4.0_STD
2.48A
1005 Change R228 from 10K to 240 and PU to +1.2VSUS
Follow reference board
DIMM0 SA0,1,2=LLL
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
VREF DQ0 M1 Solution
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.
BU5
Size Custom
Document Number
17 -- DDR4 DIMM0-STD(4.0H)
Rev 1A
Date: Tuesday, December 13, 2016
Sheet 17 of 51


JDIM2A
DDR4 SODIMM 260 PIN (260P)
DDR4-DIMM0_H=4.0_RVS
JDIM2B
2.48A
DDR4 SODIMM 260 PIN (260P)
DDR4-DIMM0_H=4.0_RVS
M_B_A[13:0]
M_B_DQ[63:0]
M_B_DQSP[7:0]
M_B_DQSN[7:0]
Follow reference board DIMM1 SA0,1,2=LHL
Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector
Co-lay for ODT
From Intel MOW, ODT directly connection to CPU
Local Thermal Sensor
DDR4 Thermal Sensor
EMC1412-1-ACZL-TR
Need Check PN(E0D)
VREF DQ1 M1 Solution
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.
BU5
Document Number 18 -- DDR4 DIMM1-RVS(4.0H)
Rev 1A
Date: Tuesday, December 13, 2016 Sheet 18 of 51

PEX_IOVDD + PEX_IOVDDQ = 1.042A

PEX_PLL_HVDD +
PEX_SVDD_3V3 = 143mA

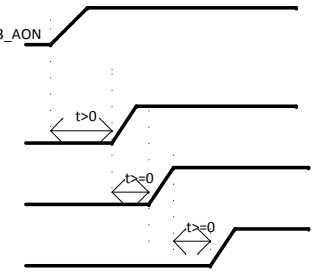
PEX_PLLVDD = 130mA

NVDD = 32.22 ~ 26.66 A

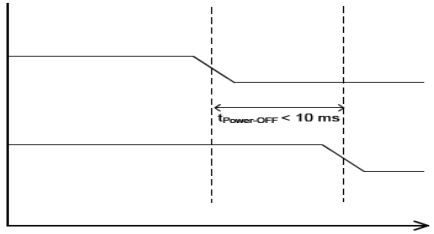
VDD33 = 56mA

If no-install , need install U4003/R4030/C4041 need test

Power up sequence



Power down sequence



BU5	**PROJECT : NFLP_KBLU_DR** Quanta Computer Inc.	
Size Custom	Document Number 19 -- N16S-GT (PCIE I/F) /NVDD	Rev 1A
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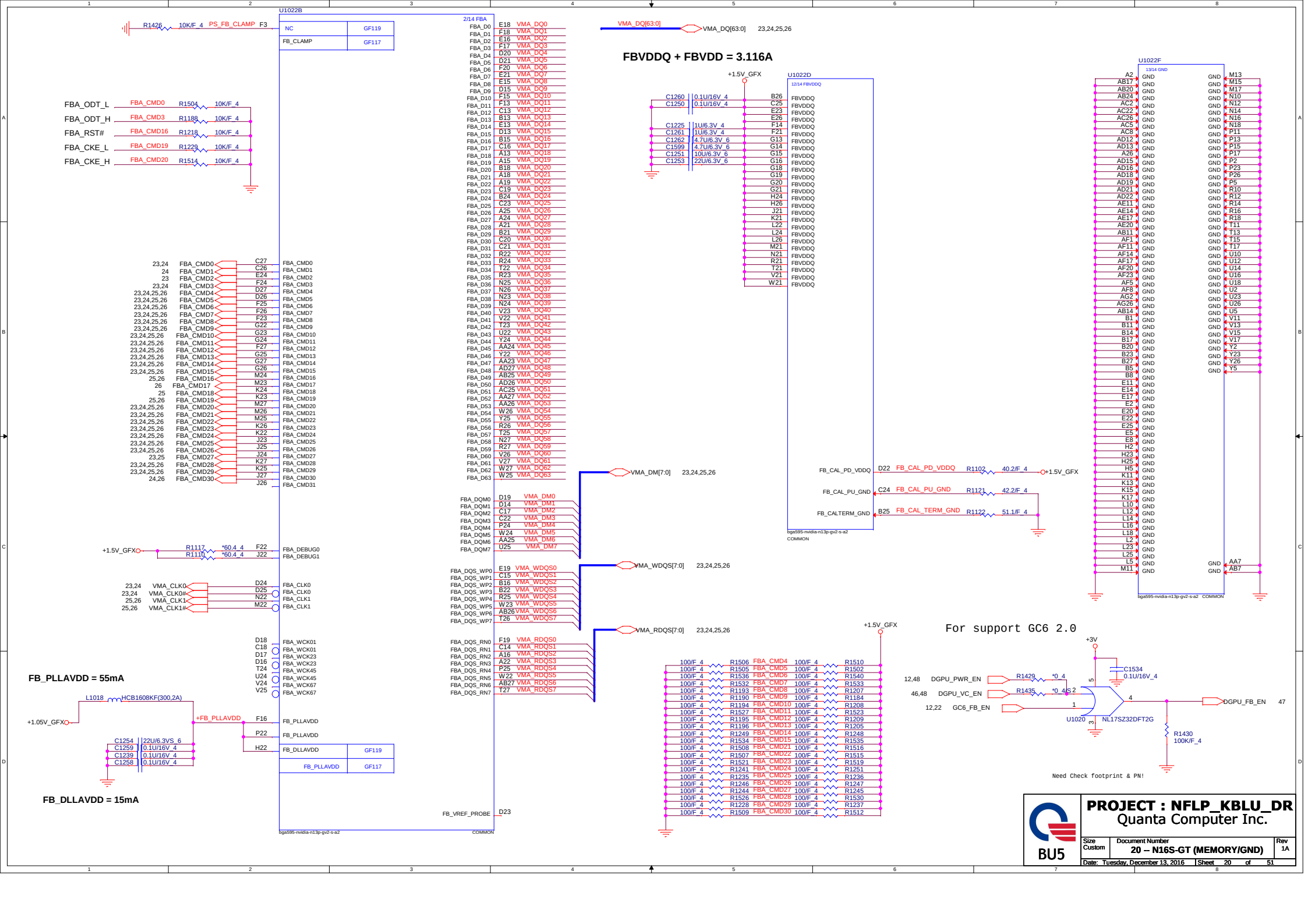

U1022B
2/14 FBA
R1426 10K/F_4 PS_FB_CLAMP F3
NC GF119
FB_CLAMP GF117
FBA_ODT_L FBA_CMD0 R1504 10K/F_4
FBA_ODT_H FBA_CMD3 R1188 10K/F_4
FBA_RST# FBA_CMD16 R1218 10K/F_4
FBA_CKE_L FBA_CMD19 R1229 10K/F_4
FBA_CKE_H FBA_CMD20 R1514 10K/F_4
FBA_D0 E18 VMA_DQ0
FBA_D1 F18 VMA_DQ1
FBA_D2 E16 VMA_DQ2
FBA_D3 F17 VMA_DQ3
FBA_D4 D20 VMA_DQ4
FBA_D5 D21 VMA_DQ5
FBA_D6 F20 VMA_DQ6
FBA_D7 E21 VMA_DQ7
FBA_D8 E15 VMA_DQ8
FBA_D9 D15 VMA_DQ9
FBA_D10 F15 VMA_DQ10
FBA_D11 F13 VMA_DQ11
FBA_D12 C13 VMA_DQ12
FBA_D13 B13 VMA_DQ13
FBA_D14 E13 VMA_DQ14
FBA_D15 D13 VMA_DQ15
FBA_D16 B15 VMA_DQ16
FBA_D17 C16 VMA_DQ17
FBA_D18 A13 VMA_DQ18
FBA_D19 A15 VMA_DQ19
FBA_D20 B18 VMA_DQ20
FBA_D21 A18 VMA_DQ21
FBA_D22 A19 VMA_DQ22
FBA_D23 C19 VMA_DQ23
FBA_D24 B24 VMA_DQ24
FBA_D25 C23 VMA_DQ25
FBA_D26 A25 VMA_DQ26
FBA_D27 A24 VMA_DQ27
FBA_D28 A21 VMA_DQ28
FBA_D29 B21 VMA_DQ29
FBA_D30 C20 VMA_DQ30
FBA_D31 C21 VMA_DQ31
FBA_D32 R22 VMA_DQ32
FBA_D33 R24 VMA_DQ33
FBA_D34 T22 VMA_DQ34
FBA_D35 R23 VMA_DQ35
FBA_D36 N25 VMA_DQ36
FBA_D37 N26 VMA_DQ37
FBA_D38 N23 VMA_DQ38
FBA_D39 N24 VMA_DQ39
FBA_D40 V23 VMA_DQ40
FBA_D41 V22 VMA_DQ41
FBA_D42 T23 VMA_DQ42
FBA_D43 U22 VMA_DQ43
FBA_D44 Y24 VMA_DQ44
FBA_D45 AA24 VMA_DQ45
FBA_D46 Y22 VMA_DQ46
FBA_D47 AA23 VMA_DQ47
FBA_D48 AD27 VMA_DQ48
FBA_D49 AB25 VMA_DQ49
FBA_D50 AD26 VMA_DQ50
FBA_D51 AC25 VMA_DQ51
FBA_D52 AA27 VMA_DQ52
FBA_D53 AA26 VMA_DQ53
FBA_D54 W26 VMA_DQ54
FBA_D55 Y25 VMA_DQ55
FBA_D56 R26 VMA_DQ56
FBA_D57 T25 VMA_DQ57
FBA_D58 N27 VMA_DQ58
FBA_D59 R27 VMA_DQ59
FBA_D60 V26 VMA_DQ60
FBA_D61 V27 VMA_DQ61
FBA_D62 W27 VMA_DQ62
FBA_D63 W25 VMA_DQ63
FBA_CMD0 23,24 FBA_CMD0 C27
FBA_CMD1 24 FBA_CMD1 C26
FBA_CMD2 23 FBA_CMD2 E24
FBA_CMD3 23,24 FBA_CMD3 F24
FBA_CMD4 23,24,25,26 FBA_CMD4 D27
FBA_CMD5 23,24,25,26 FBA_CMD5 D26
FBA_CMD6 23,24,25,26 FBA_CMD6 F25
FBA_CMD7 23,24,25,26 FBA_CMD7 F26
FBA_CMD8 23,24,25,26 FBA_CMD8 F23
FBA_CMD9 23,24,25,26 FBA_CMD9 G22
FBA_CMD10 23,24,25,26 FBA_CMD10 G23
FBA_CMD11 23,24,25,26 FBA_CMD11 G24
FBA_CMD12 23,24,25,26 FBA_CMD12 F27
FBA_CMD13 23,24,25,26 FBA_CMD13 G25
FBA_CMD14 23,24,25,26 FBA_CMD14 G27
FBA_CMD15 23,24,25,26 FBA_CMD15 G26
FBA_CMD16 25,26 FBA_CMD16 M24
FBA_CMD17 26 FBA_CMD17 M23
FBA_CMD18 25 FBA_CMD18 K24
FBA_CMD19 25,26 FBA_CMD19 K23
FBA_CMD20 23,24,25,26 FBA_CMD20 M27
FBA_CMD21 23,24,25,26 FBA_CMD21 M26
FBA_CMD22 23,24,25,26 FBA_CMD22 M25
FBA_CMD23 23,24,25,26 FBA_CMD23 K26
FBA_CMD24 23,24,25,26 FBA_CMD24 K22
FBA_CMD25 23,24,25,26 FBA_CMD25 J23
FBA_CMD26 23,24,25,26 FBA_CMD26 J25
FBA_CMD27 23,25 FBA_CMD27 J24
FBA_CMD28 23,24,25,26 FBA_CMD28 K27
FBA_CMD29 23,24,25,26 FBA_CMD29 K25
FBA_CMD30 24,26 FBA_CMD30 J27
FBA_CMD31 J26
+1.5V_GFX R1117 *60.4_4 F22 FBA_DEBUG0
R1110 *60.4_4 J22 FBA_DEBUG1
23,24 VMA_CLK0 D24 FBA_CLK0
23,24 VMA_CLK0# D25 FBA_CLK0
25,26 VMA_CLK1 N22 FBA_CLK1
25,26 VMA_CLK1# M22 FBA_CLK1
D18 FBA_WCK01
C18 FBA_WCK01
D17 FBA_WCK23
D16 FBA_WCK23
T24 FBA_WCK45
U24 FBA_WCK45
V24 FBA_WCK67
V25 FBA_WCK67
FB_PLLAVDD = 55mA
L1018 HCB1608KF(300,2A)
+1.05V_GFX +FB_PLLAVDD F16 FB_PLLAVDD
P22 FB_PLLAVDD
H22 FB_PLLAVDD
C1254 22U/6.3VS_6
C1259 0.1U/16V_4
C1239 0.1U/16V_4
C1258 0.1U/16V_4
FB_DLLAVDD GF119
FB_PLLAVDD GF117
FB_DLLAVDD = 15mA
FB_VREF_PROBE D23
bga595-nvidia-n13p-gv2-s-a2
COMMON
VMA_DM[7:0] 23,24,25,26
FBA_DQM0 D19 VMA_DM0
FBA_DQM1 D14 VMA_DM1
FBA_DQM2 C17 VMA_DM2
FBA_DQM3 C22 VMA_DM3
FBA_DQM4 P24 VMA_DM4
FBA_DQM5 W24 VMA_DM5
FBA_DQM6 AA25 VMA_DM6
FBA_DQM7 U25 VMA_DM7
VMA_WDQS[7:0] 23,24,25,26
FBA_DQS_WP0 E19 VMA_WDQS0
FBA_DQS_WP1 C15 VMA_WDQS1
FBA_DQS_WP2 B16 VMA_WDQS2
FBA_DQS_WP3 B22 VMA_WDQS3
FBA_DQS_WP4 R25 VMA_WDQS4
FBA_DQS_WP5 W23 VMA_WDQS5
FBA_DQS_WP6 AB26 VMA_WDQS6
FBA_DQS_WP7 T26 VMA_WDQS7
VMA_RDQS[7:0] 23,24,25,26
FBA_DQS_RN0 F19 VMA_RDQS0
FBA_DQS_RN1 C14 VMA_RDQS1
FBA_DQS_RN2 A16 VMA_RDQS2
FBA_DQS_RN3 A22 VMA_RDQS3
FBA_DQS_RN4 P25 VMA_RDQS4
FBA_DQS_RN5 W22 VMA_RDQS5
FBA_DQS_RN6 AB27 VMA_RDQS6
FBA_DQS_RN7 T27 VMA_RDQS7
VMA_DQ[63:0] VMA_DQ[63:0] 23,24,25,26
FBVDDQ + FBVDD = 3.116A
+1.5V_GFX
U1022D
12/14 FBVDDQ
C1260 0.1U/16V_4
C1250 0.1U/16V_4
C1225 1U/6.3V_4
C1261 1U/6.3V_4
C1262 4.7U/6.3V_6
C1599 4.7U/6.3V_6
C1251 10U/6.3V_6
C1253 22U/6.3V_6
B26 C25 E23 E26 F14 F21 G13 G14 G15 G16 G18 G19 G20 G21 H24 H26 J21 K21 L22 L24 L26 M21 N21 R21 T21 V21 W21 FBVDDQ
FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ R1102 40.2/F_4 +1.5V_GFX
FB_CAL_PU_GND C24 FB_CAL_PU_GND R1121 42.2/F_4
FB_CALTERM_GND B25 FB_CAL_TERM_GND R1122 51.1/F_4
bga595-nvidia-n13p-gv2-s-a2
COMMON
U1022F
13/14 GND
A2 AB17 AB20 AB24 AC2 AC22 AC26 AC5 AC8 AD12 AD13 AD15 AD16 AD18 AD19 AD21 AD22 AE11 AE14 AE17 AE20 AB11 AF1 AF11 AF14 AF17 AF20 AF23 AF5 AF8 AG2 AG26 AB14 B1 B11 B14 B17 B20 B23 B27 B5 B8 E11 E14 E17 E2 E20 E22 E25 E5 E8 H2 H23 H25 H5 K11 K13 K15 K17 L10 L12 L14 L16 L18 L2 L23 L25 L5 M11 GND
M13 M15 M17 N10 N12 N14 N16 N18 P11 P13 P15 P17 P2 P23 P26 P5 R10 R12 R14 R16 R18 T11 T13 T15 T17 U10 U12 U14 U16 U18 U2 U23 U26 U5 V11 V13 V15 V17 Y2 Y23 Y26 Y5 GND
AA7 AB7 GND
bga595-nvidia-n13p-gv2-s-a2 COMMON
+1.5V_GFX
100/F_4 R1506 FBA_CMD4 R1505 FBA_CMD5 R1536 FBA_CMD6 R1532 FBA_CMD7 R1193 FBA_CMD8 R1190 FBA_CMD9 R1194 FBA_CMD10 R1527 FBA_CMD11 R1195 FBA_CMD12 R1196 FBA_CMD13 R1249 FBA_CMD14 R1534 FBA_CMD15 R1508 FBA_CMD21 R1507 FBA_CMD22 R1521 FBA_CMD23 R1241 FBA_CMD24 R1235 FBA_CMD25 R1246 FBA_CMD26 R1244 FBA_CMD27 R1526 FBA_CMD28 R1228 FBA_CMD29 R1509 FBA_CMD30 100/F_4 R1510 R1502 R1540 R1533 R1207 R1184 R1208 R1523 R1209 R1205 R1248 R1535 R1516 R1515 R1519 R1251 R1236 R1247 R1245 R1530 R1237 R1512
For support GC6 2.0
+3V
12,48 DGPU_PWR_EN R1429 *0_4
46,48 DGPU_VC_EN R1435 *0_4
12,22 GC6_FB_EN
C1534 0.1U/16V_4
U1020 NL17SZ32DFT2G
DGPU_FB_EN 47
R1430 100K/F_4
Need Check footprint & PN!
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.
BU5
Size Custom
Document Number 20 – N16S-GT (MEMORY/GND)
Rev 1A
Date: Tuesday, December 13, 2016
Sheet 20 of 51

U1022G
4/14 IFPAB

IFPAB

U1022J
7/14 IFPEF

IFPE

IFPF

U1022K
3/14 DACA

U1022H
5/14 IFPC

IFPC

U1022I
6/14 IFPD

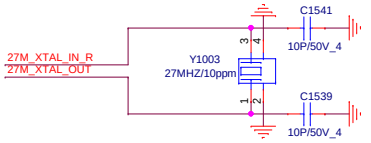
IFPD

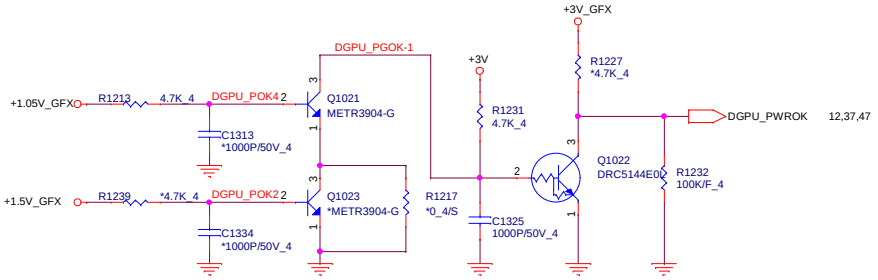
PLLVDD = 38mA

SP_PLLVDD = 17mA

VID_PLLVDD = 41mA

U1022M
9/14 XTAL_PLL





BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	21 – N16S-GT (DISPLAY)	1A
Date: Tuesday, December 13, 2016	Sheet 21 of 51	

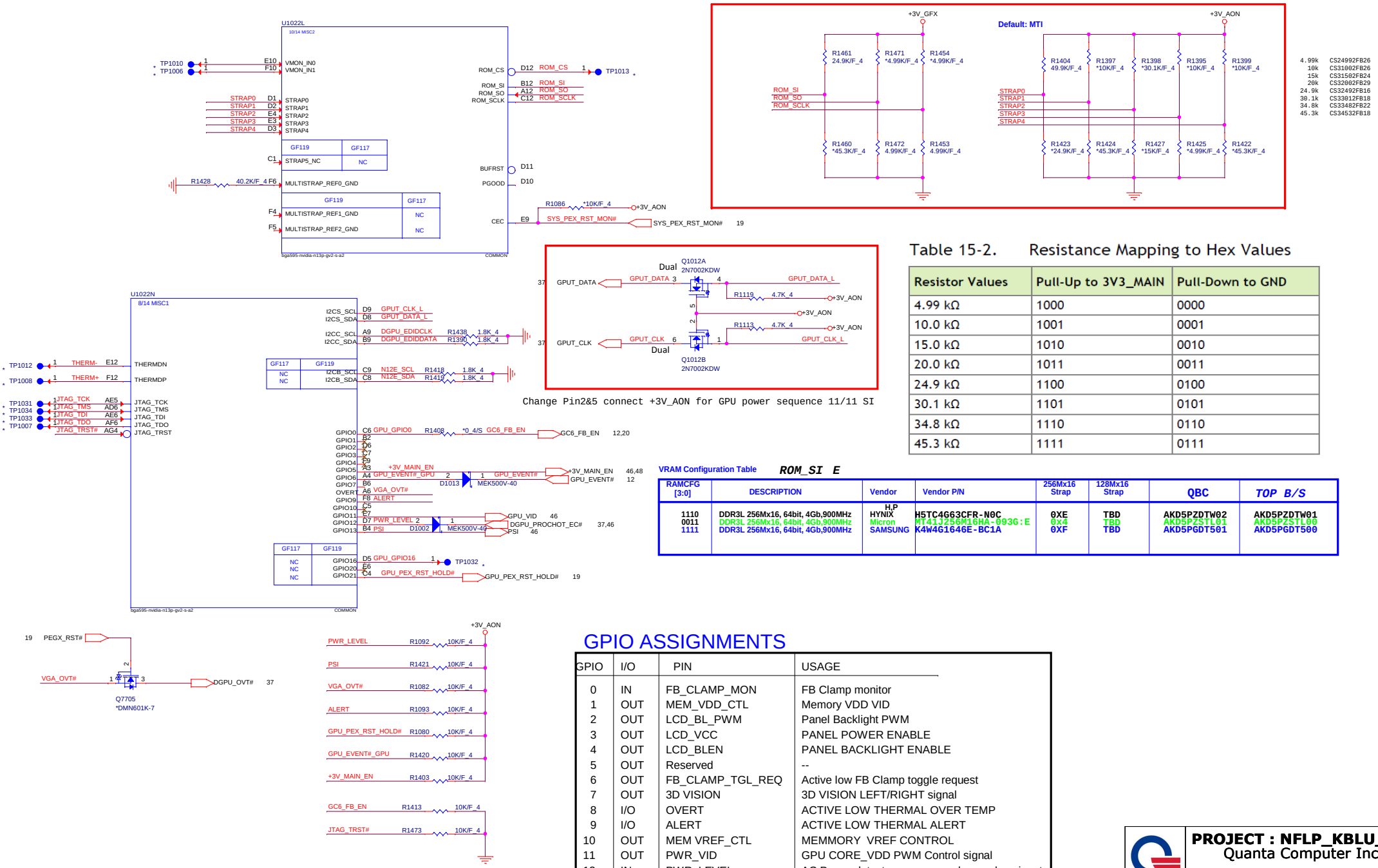


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

VRAM Configuration Table ***ROM_SI E***

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	256Mx16 Strap	128Mx16 Strap	QBC	*TOP B/S*
1110	DDR3L 256Mx16, 64bit, 4Gb,900MHz	H,P HYNIX	H5TC4G63CFR-N0C	0XE	TBD	AKD5PZDTW02	AKD5PZDTW01
0011	DDR3L 256Mx16, 64bit, 4Gb,900MHz	Micron	MT41J256M16HA-093G:E	0x4	TBD	AKD5PZSTL01	AKD5PZSTL00
1111	DDR3L 256Mx16, 64bit, 4Gb,900MHz	SAMSUNG	K4W4G1646E-BC1A	0XF	TBD	AKD5PGDT501	AKD5PGDT500

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	22 -- N16S-GT (GPIO/STRAPS)	1A

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Rank0

HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

U1021

U1024

96-BALL SDRAM DDR3
VRAM _DDR3_MTI_256MX16

PROJECT :	NFLP_KBLU_DR
	Quanta Computer Inc.
Size	Custom
Document Number	23 -- VRAM DDR3L - RANK0
Rev	1A
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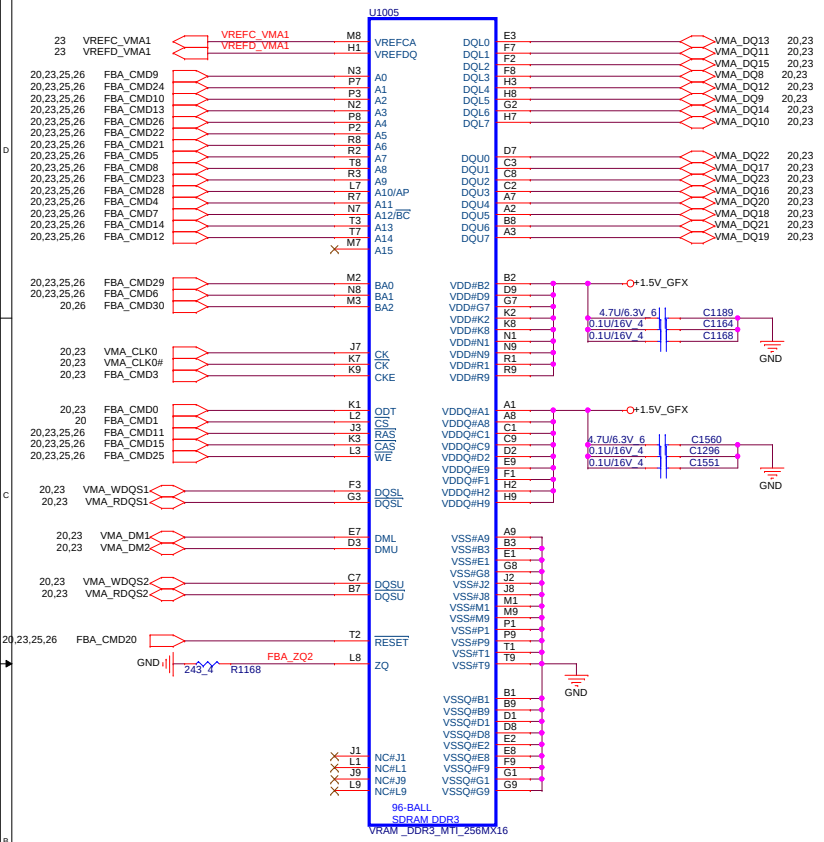
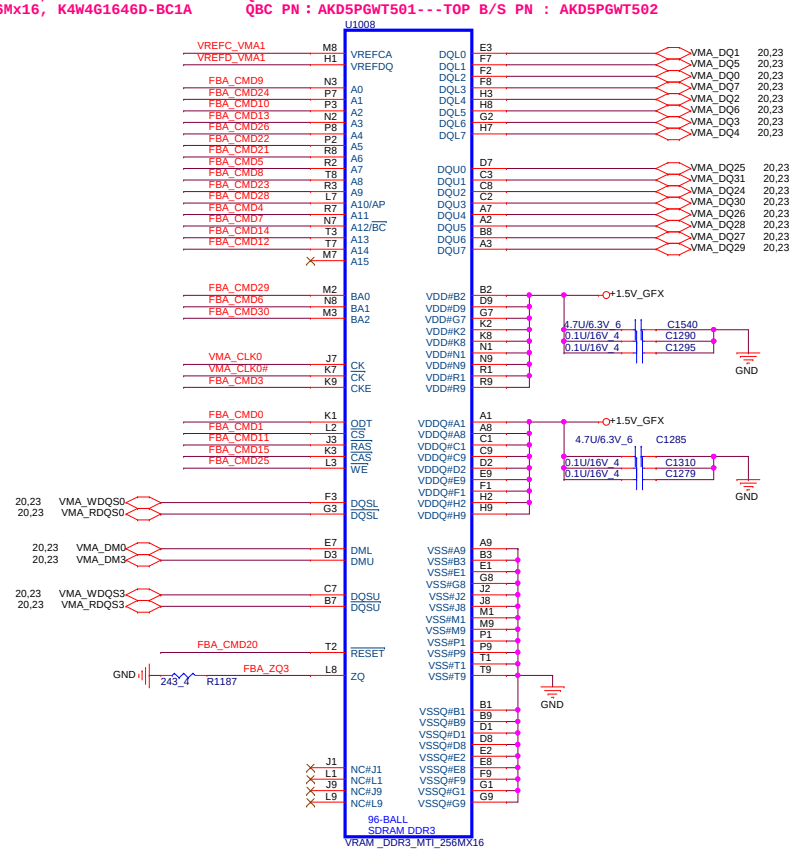
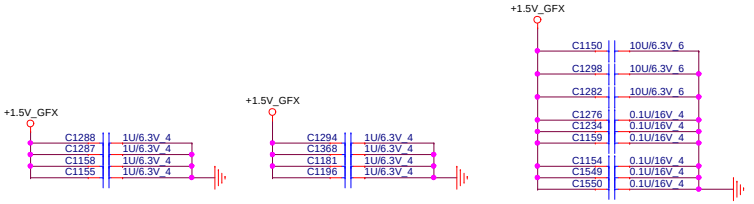
BU5

Rank1

HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502







BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	24 -- VRAM DDR3L - RANK1	1A
Date: Tuesday, December 13, 2016	Sheet 24 of 51	

Rank0

HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502

U1026

VREFC_VMA3 M8 VREFCA
VREFD_VMA3 H1 VREFDQ

FBA_CMD7 N3
FBA_CMD10 P7 A0
FBA_CMD24 P3 A1
FBA_CMD6 N2 A2
FBA_CMD22 P8 A3
FBA_CMD26 P2 A4
FBA_CMD5 R8 A5
FBA_CMD21 R2 A6
FBA_CMD8 T8 A7
FBA_CMD4 R3 A8
FBA_CMD25 L7 A9
FBA_CMD23 R7 A10/AP
FBA_CMD9 N7 A11
FBA_CMD12 T3 A12/BC
FBA_CMD14 T7 A13
M7 A14
A15

FBA_CMD29 M2 BA0
FBA_CMD13 N8 BA1
FBA_CMD27 M3 BA2

VMA_CLK1 J7 CK
VMA_CLK1# K7 CK
FBA_CMD19 K9 CKE

FBA_CMD16 K1 ODT
FBA_CMD18 L2 CS
FBA_CMD11 J3 RAS
FBA_CMD15 K3 CAS
FBA_CMD28 L3 WE

VMA_WDQS4 F3 DQSL
VMA_RDQS4 G3 DQSL

VMA_DM4 E7 DML
VMA_DM7 D3 DMU

VMA_WDQS7 C7 DQSU
VMA_RDQS7 B7 DQSU

FBA_CMD20 T2 RESET

FBA_ZQ4 L8 ZQ
243_4 R1513

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9

+1.5V_GFX
4.7U/6.3V_6
0.1U/16V_4
C1277 C1595 C1157
GND

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

+1.5V_GFX
4.7U/6.3V_6
0.1U/16V_4
C1263 C1548 C1544
GND

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9
GND

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

NC#J1 J1
NC#L1 L1
NC#J9 J9
NC#L9 L9

96-BALL
SDRAM DDR3
VRAM _DDR3_MTI_256MX16

DQU0 E3
DQU1 F7
DQU2 F2
DQU3 F8
DQU4 H3
DQU5 H8
DQU6 G2
DQU7 H7

VMA_DQ34 VMA_DQ38 VMA_DQ35 VMA_DQ39 VMA_DQ32 VMA_DQ36 VMA_DQ33 VMA_DQ37 20,26

DQU0 D7
DQU1 C3
DQU2 C8
DQU3 C2
DQU4 A7
DQU5 A2
DQU6 B8
DQU7 A3

VMA_DQ59 VMA_DQ62 VMA_DQ58 VMA_DQ63 VMA_DQ57 VMA_DQ60 VMA_DQ56 VMA_DQ61 20,26

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

VMA_CLK1
VMA_CLK1#
R1191 162_4

+1.5V_GFX
R1219 1.33K/F_4
VREFC_VMA3
R1215 1.33K/F_4
C1306 0.01U/50V_4

+1.5V_GFX
R1522 1.33K/F_4
VREFD_VMA3
R1518 1.33K/F_4
C1604 0.01U/50V_4

U1027

VREFC_VMA3 M8 VREFCA
VREFD_VMA3 H1 VREFDQ

FBA_CMD7 N3
FBA_CMD10 P7 A0
FBA_CMD24 P3 A1
FBA_CMD6 N2 A2
FBA_CMD22 P8 A3
FBA_CMD26 P2 A4
FBA_CMD5 R8 A5
FBA_CMD21 R2 A6
FBA_CMD8 T8 A7
FBA_CMD4 R3 A8
FBA_CMD25 L7 A9
FBA_CMD23 R7 A10/AP
FBA_CMD9 N7 A11
FBA_CMD12 T3 A12/BC
FBA_CMD14 T7 A13
M7 A14
A15

FBA_CMD29 M2 BA0
FBA_CMD13 N8 BA1
FBA_CMD27 M3 BA2

VMA_CLK1 J7 CK
VMA_CLK1# K7 CK
FBA_CMD19 K9 CKE

FBA_CMD16 K1 ODT
FBA_CMD18 L2 CS
FBA_CMD11 J3 RAS
FBA_CMD15 K3 CAS
FBA_CMD28 L3 WE

VMA_WDQS5 F3 DQSL
VMA_RDQS5 G3 DQSL

VMA_DM5 E7 DML
VMA_DM6 D3 DMU

VMA_WDQS6 C7 DQSU
VMA_RDQS6 B7 DQSU

FBA_CMD20 T2 RESET

FBA_ZQ5 L8 ZQ
243_4 R1226

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9

+1.5V_GFX
4.7U/6.3V_6
0.1U/16V_4
C1624 C1614 C1617
GND

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

+1.5V_GFX
4.7U/6.3V_6
0.1U/16V_4
C1348 C1630 C1626
GND

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9
GND

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

NC#J1 J1
NC#L1 L1
NC#J9 J9
NC#L9 L9

96-BALL
SDRAM DDR3
VRAM _DDR3_MTI_256MX16

DQU0 D7
DQU1 C3
DQU2 C8
DQU3 C2
DQU4 A7
DQU5 A2
DQU6 B8
DQU7 A3

VMA_DQ44 VMA_DQ43 VMA_DQ45 VMA_DQ40 VMA_DQ47 VMA_DQ42 VMA_DQ46 VMA_DQ41 20,26

DQU0 D7
DQU1 C3
DQU2 C8
DQU3 C2
DQU4 A7
DQU5 A2
DQU6 B8
DQU7 A3

VMA_DQ52 VMA_DQ50 VMA_DQ55 VMA_DQ51 VMA_DQ53 VMA_DQ48 VMA_DQ54 VMA_DQ49 20,26

FOR EMI Request

+1.5V_GFX
C1355 C1361 C1364 C1590 C1634 C1553 C1160 C1554 *120P/50V_4

+1.5V_GFX
C1637 C1300 C1627 C1628 1U/6.3V_4

+1.5V_GFX
C1156 C1552 C1623 C1629 1U/6.3V_4

+1.5V_GFX
C1621 C1264 C1622 10U/6.3V_6
C1619 C1546 C1545 0.1U/16V_4
C1632 C1633 C1631 0.1U/16V_4

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	25 -- VRAM DDR3L - RANK0	1A

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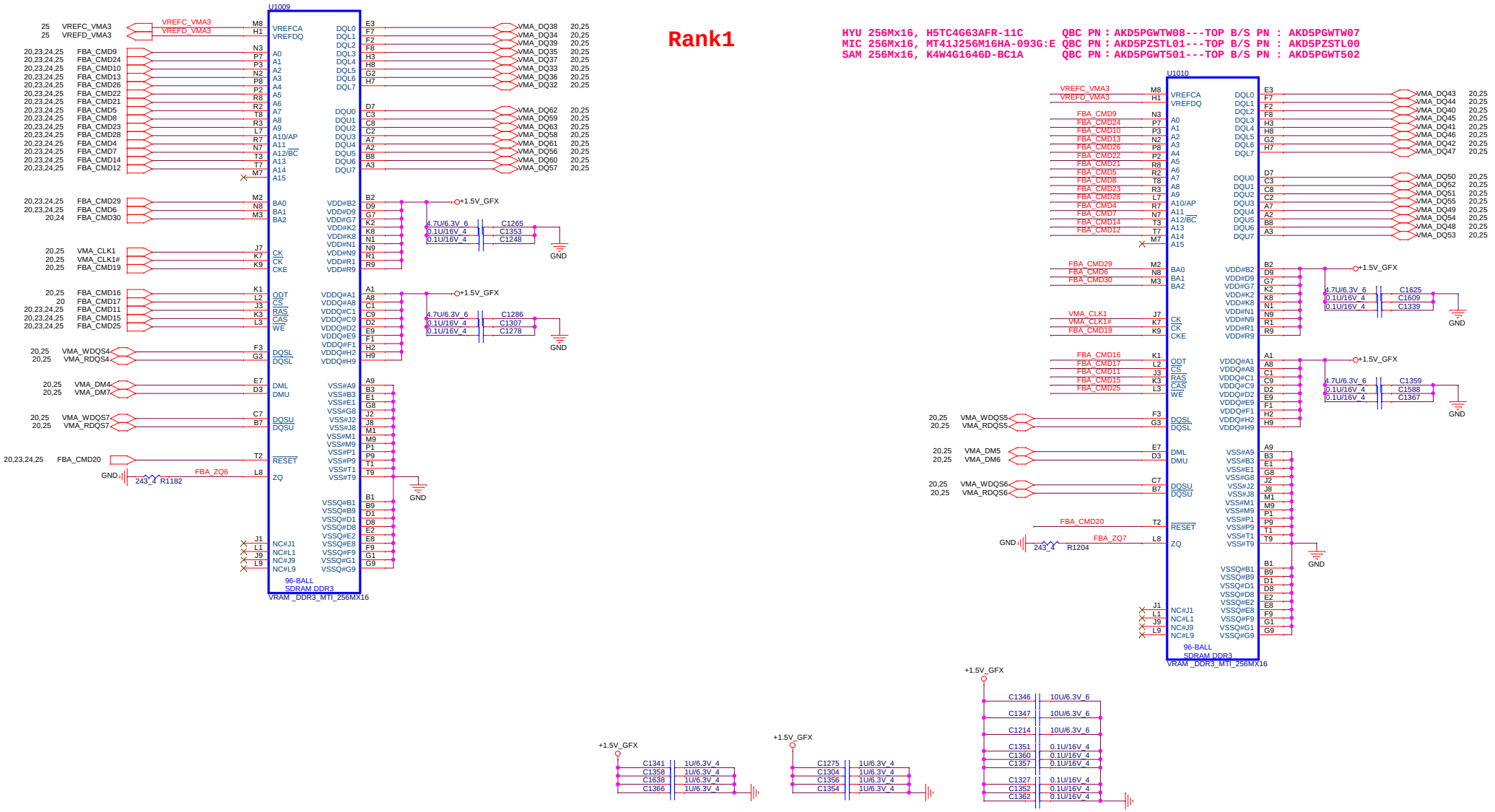
Rank1

HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502

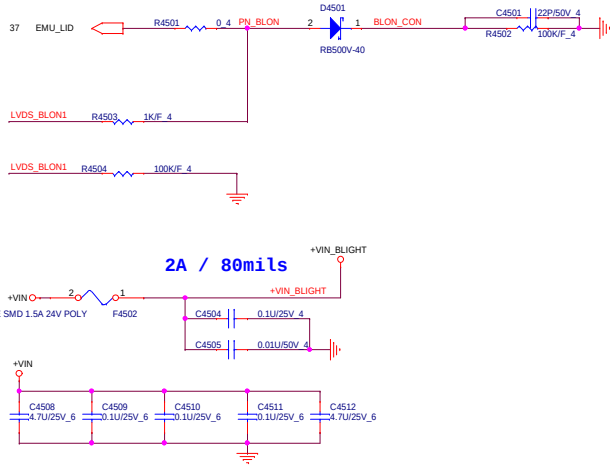


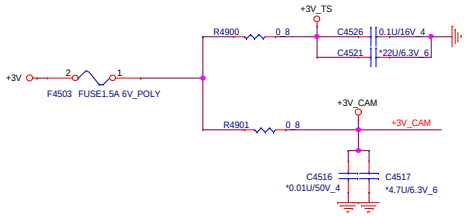
BU5

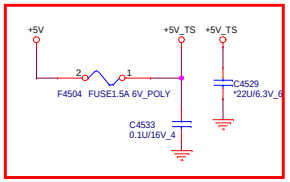
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	26 -- VRAM DDR3L - RANK1	1A
Date: Tuesday, December 13, 2016	Sheet 26 of 51	

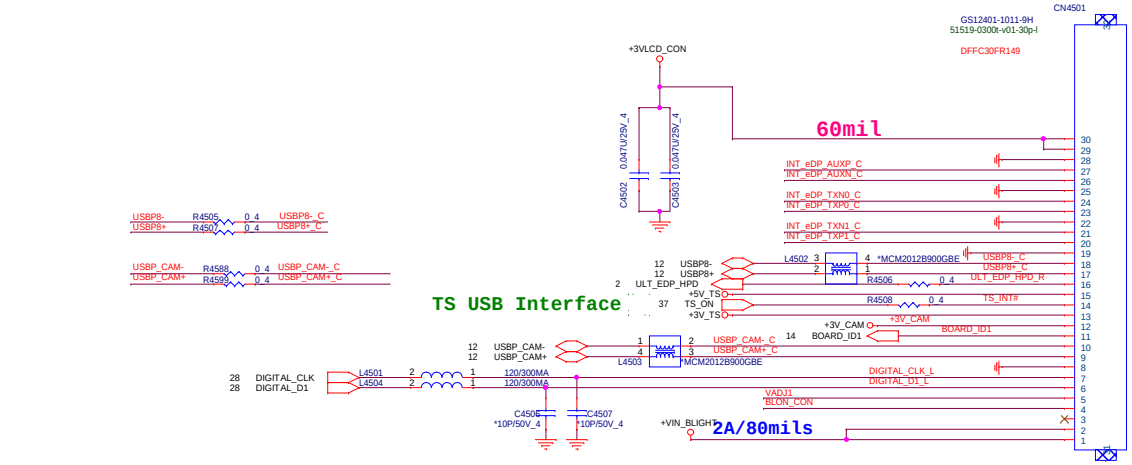
LID Switch

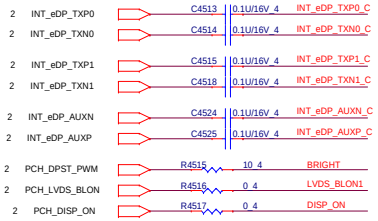


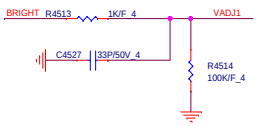


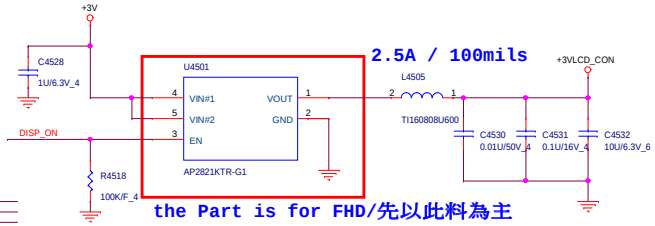


eDP Conn.





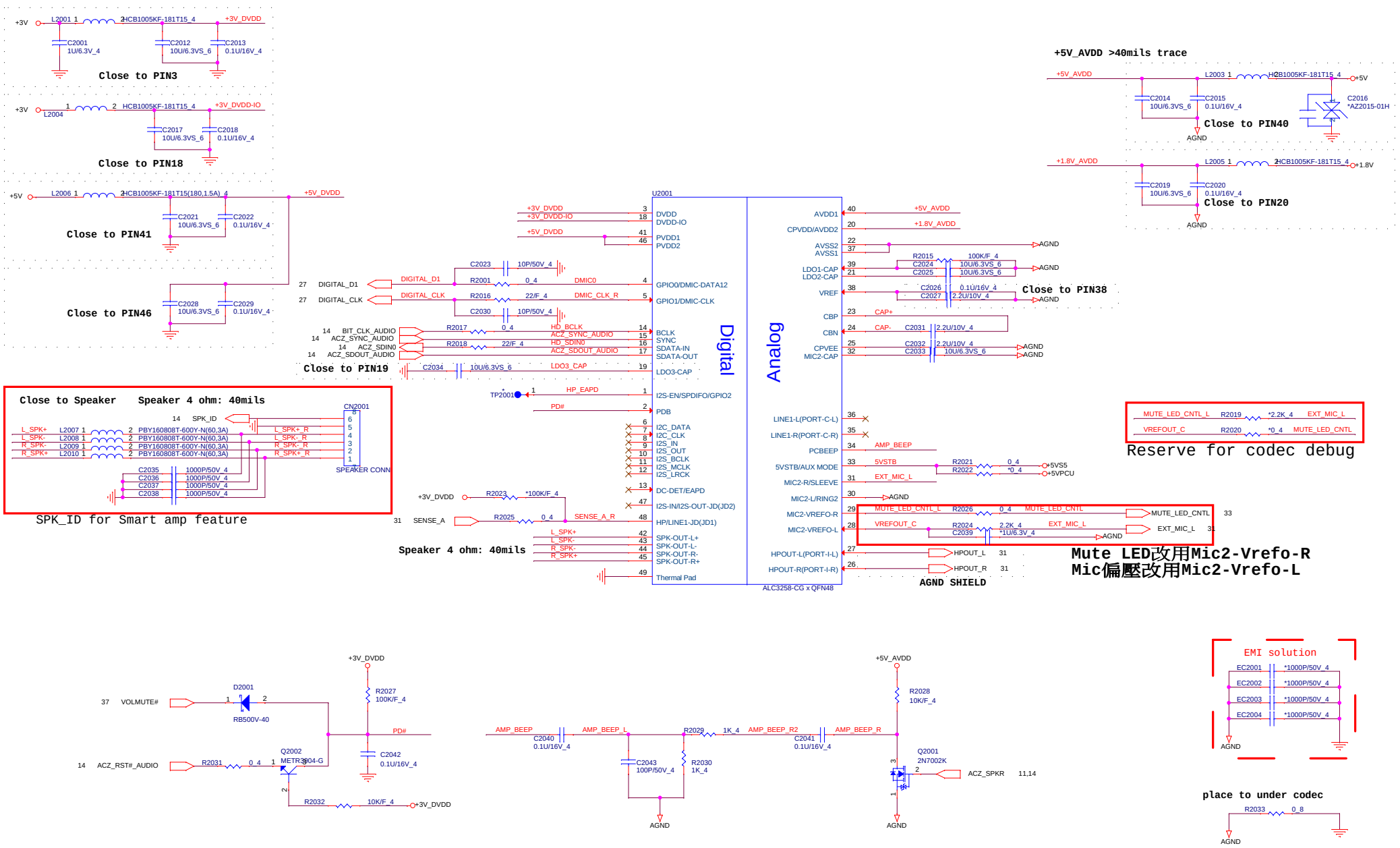




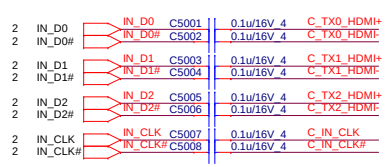
2,4,10,11,12,13,14,15,17,18,19,20,21,28,29,30,31,33,34,35,36,37,43,46,51 +3V
6,13,31,33,36,37,38,39,49 +3VPCU
28,29,33,34,36,51 +5V
33,38,39,40,41,44,45,46,47,50 +VIN

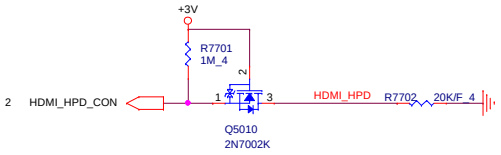
the Part is for FHD/先以此料為主

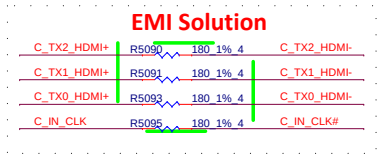
BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.	
Size: Custom	Document Number: 27 -- eDP CONN/LID/CAM/D-MIC/TS	Rev: 1A
Date: Tuesday, December 13, 2016	Sheet 27 of 51	

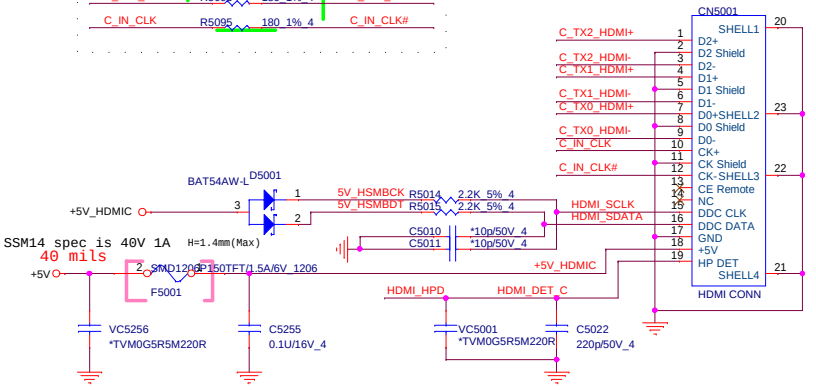

+5V_AVDD >40mils trace
Close to PIN3
Close to PIN18
Close to PIN41
Close to PIN46
Close to PIN40
Close to PIN20
Close to PIN38
Close to PIN19
Close to Speaker
Speaker 4 ohm: 40mils
SPK_ID for Smart amp feature
Reserve for codec debug
Mute LED改用Mic2-Vrefo-R
Mic偏壓改用Mic2-Vrefo-L
AGND SHIELD
EMI solution
place to under codec
U2001
Digital
Analog
ALC3258-CG x QFN48
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.
BU5
Document Number
28 -- Codec ALC3258-CG
Rev 1A
Date: Tuesday, December 13, 2016
Sheet 28 of 51

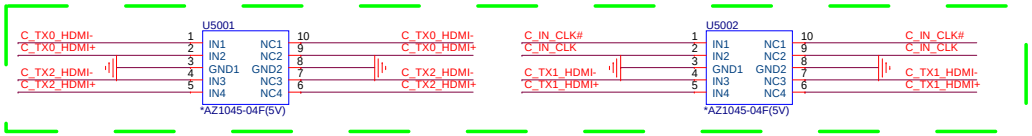
HDMI CONN

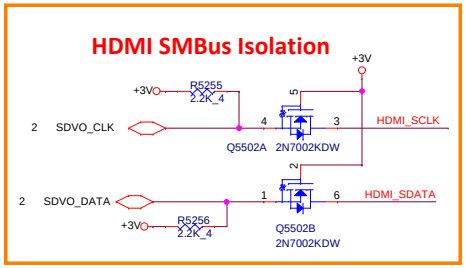


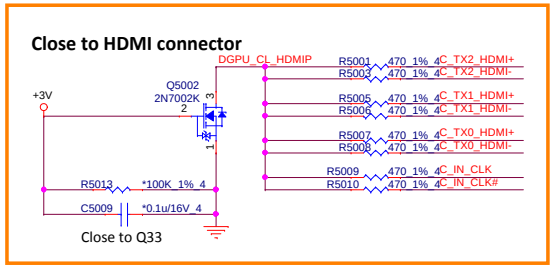




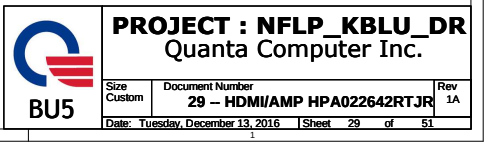








Head Phone out



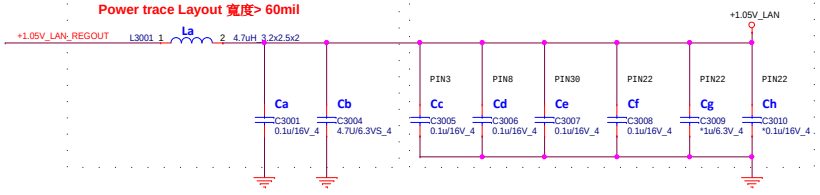
LAN RTL8107EH/RTL8111HSH

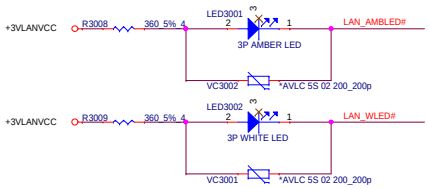
For SWR mode support RTL8111HSH & 8107
Stuff: La, Ca ,Cb

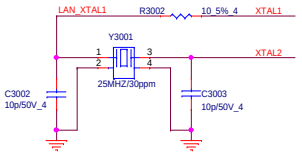
* Place Cc,Cd,Ce,Cf for RTL8111H(S) & RTL8107 close to each VDD10 pin-- 3, 22, 8 , 30

* Place Cg,Ch for RTL8111H(S) &RTL8107 close to each VDD10 pin-- 22(reserved)

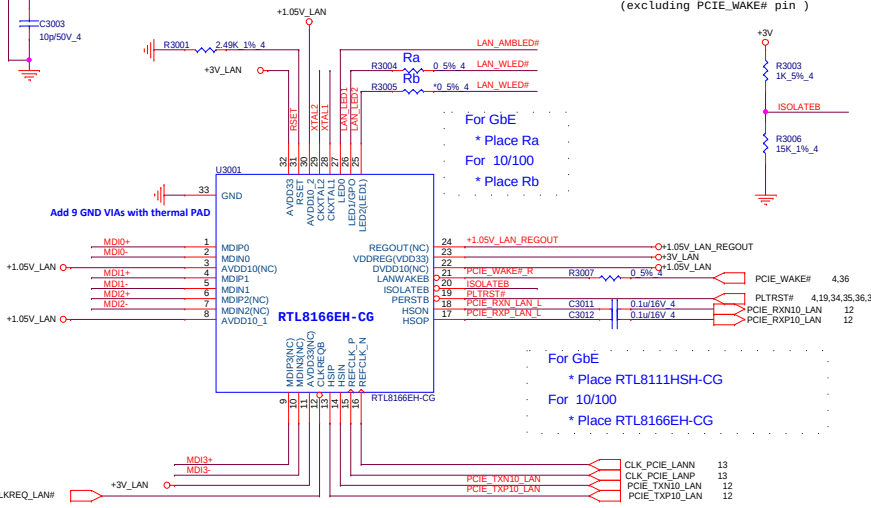
Power trace Layout 寬度> 60mil





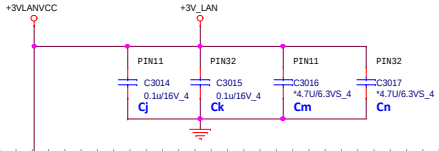


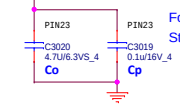
if ISOLATEB pin pull-low,
the LAN chip will not drive it's PCI-E outputs
(excluding PCIE_WAKE# pin)



For GbE
* Place RTL8111HSH-CG
For 10/100
* Place RTL8166EH-CG

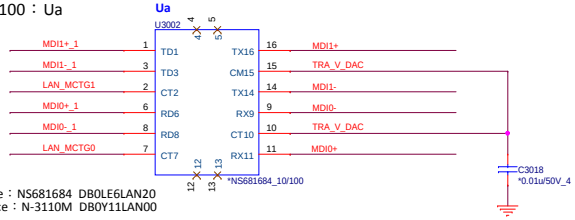
* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8111H(S) & 8107
* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)





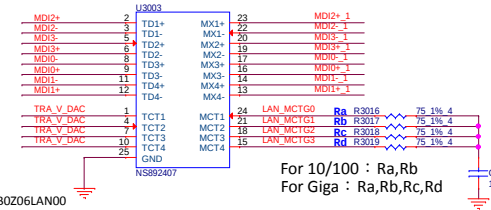
For SWR mode support RTL8111HSH & 8107
Stuff Co, Cp

For 10/100：Ua



1st source：NS681684 DB0LE6LAN20
2nd source：N-3110M DB0Y11LAN00

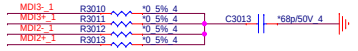
For Giga：Ub



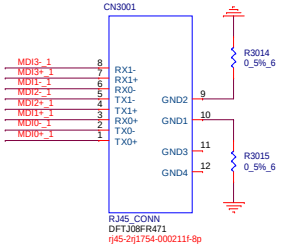
For GiGA
BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 ,DB0LL1LAN00

For 10/100：Ra,Rb
For Giga：Ra,Rb,Rc,Rd

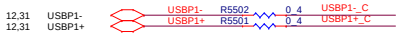
For 10/100 stuff only & Close RJ45

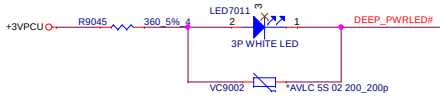


RJ45

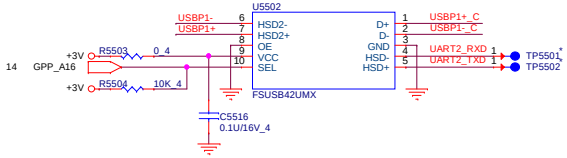


BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.	
Size: C	Document Number: 30 -- LAN RTL8107EH/RTL8111HSH	Rev: 1A
Date: Tuesday, December 13, 2016	Sheet 30 of 51	



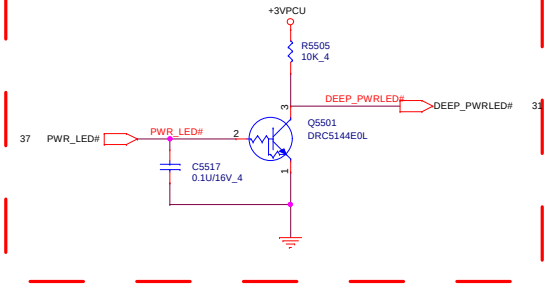


UART for Win7 WHQL DEBUG

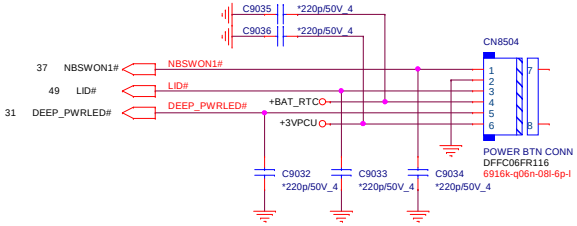


Place Back to Back La

Daughter Board



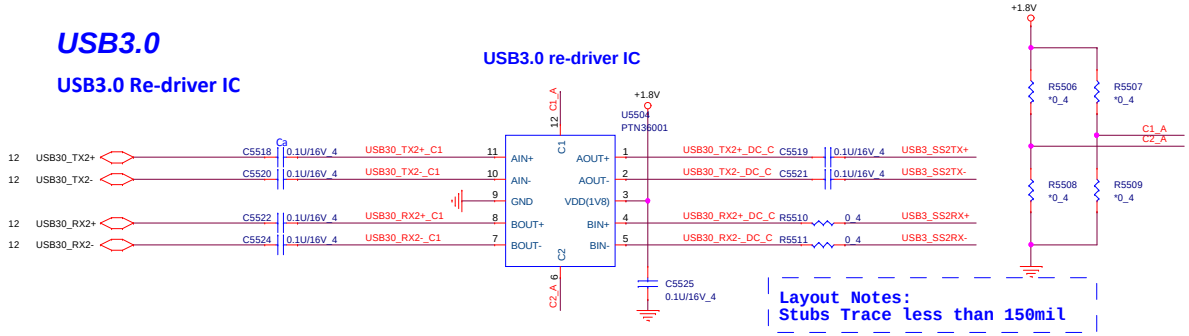
Power Board



USB3.0

USB3.0 Re-driver IC

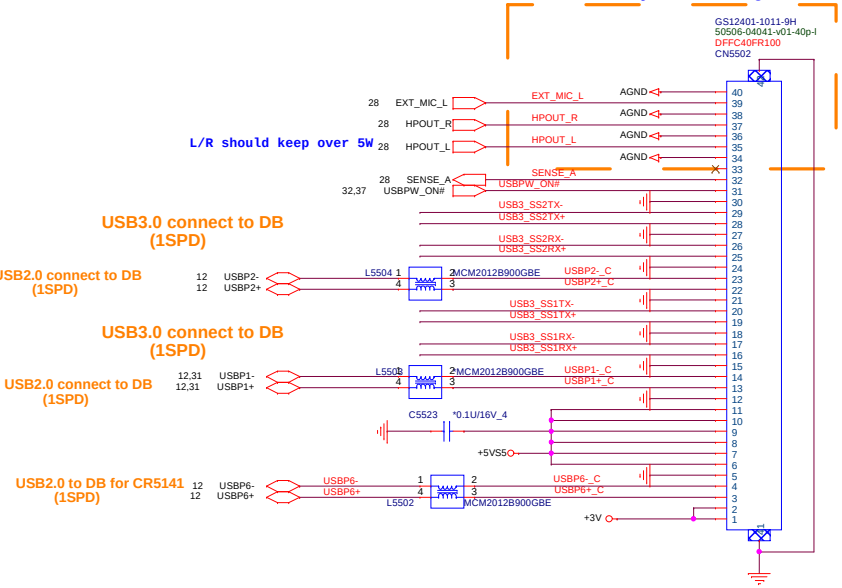
USB3.0 re-driver IC



Layout Notes:
Stubs Trace less than 150mil

Daughter Board

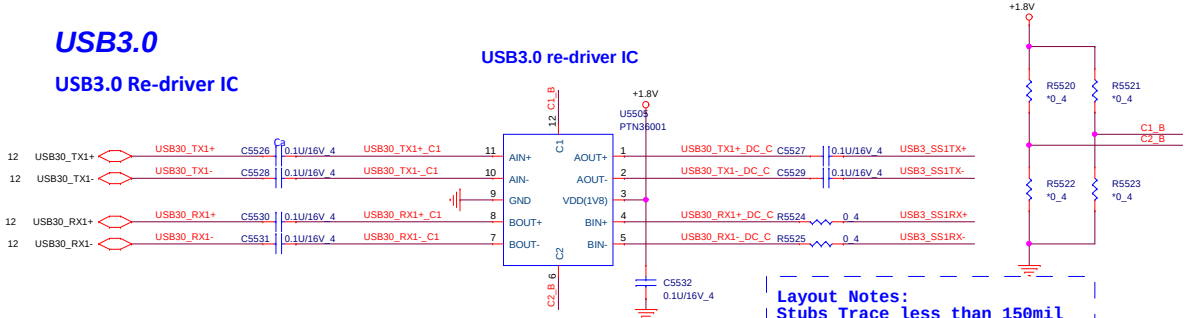
For Audio layout routing



USB3.0

USB3.0 Re-driver IC

USB3.0 re-driver IC



Layout Notes:
Stubs Trace less than 150mil

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	31 -- USB SW & TYPE-C -TPS25810	1A
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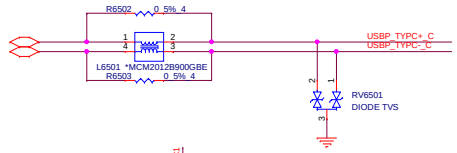
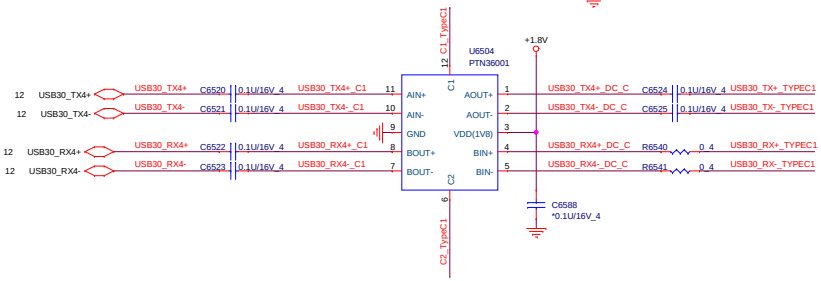
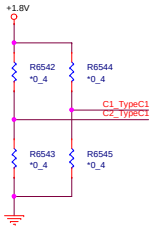
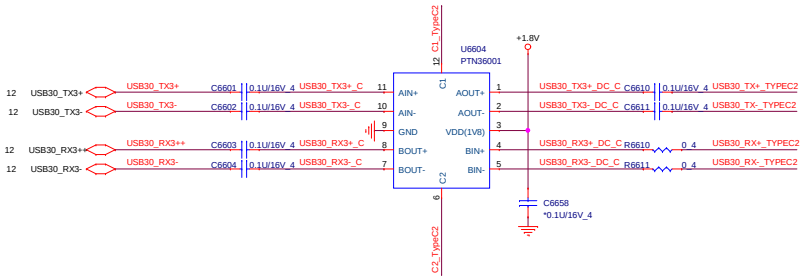
USB TYPE-C - TPS25810

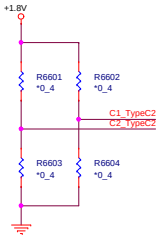
USB2.0



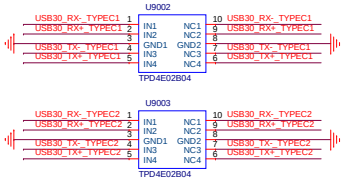


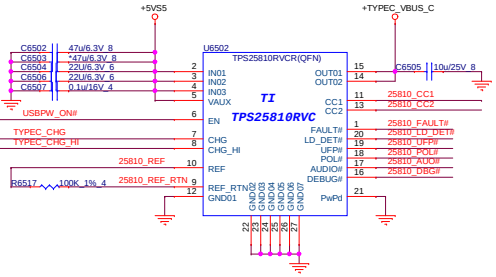


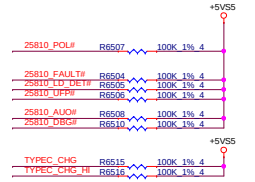




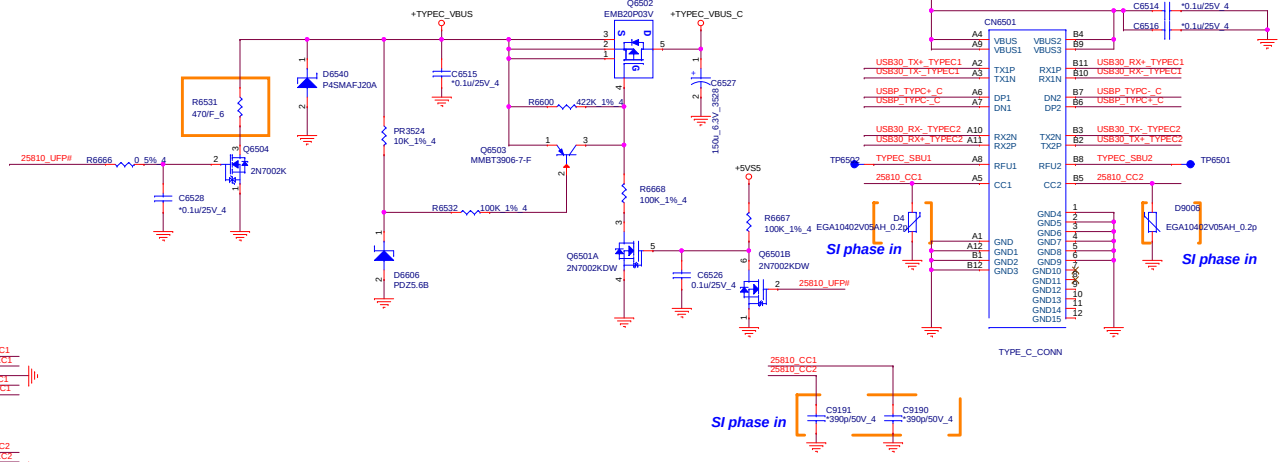
TYPE C USB3.0 ESD







CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A



TPS25810 Port	CC1	CC2	TPS25810 Response					
			OUT	VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

BU5

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Quanta Computer Inc.

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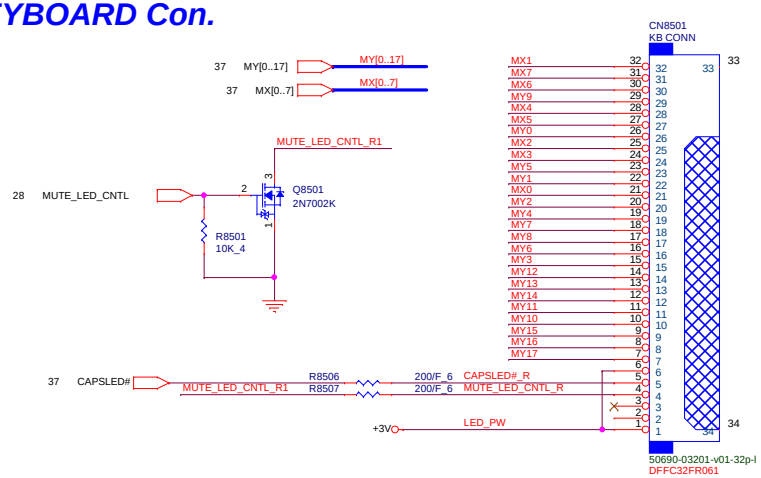
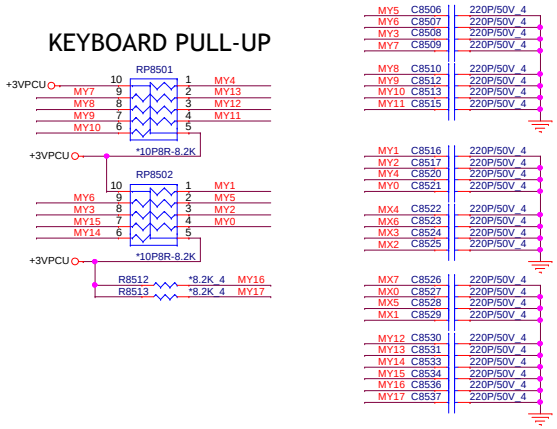
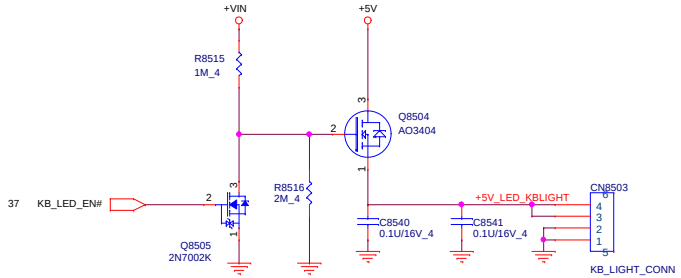
KEYBOARD Con.



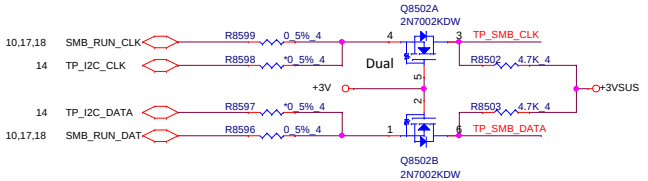
KEYBOARD PULL-UP

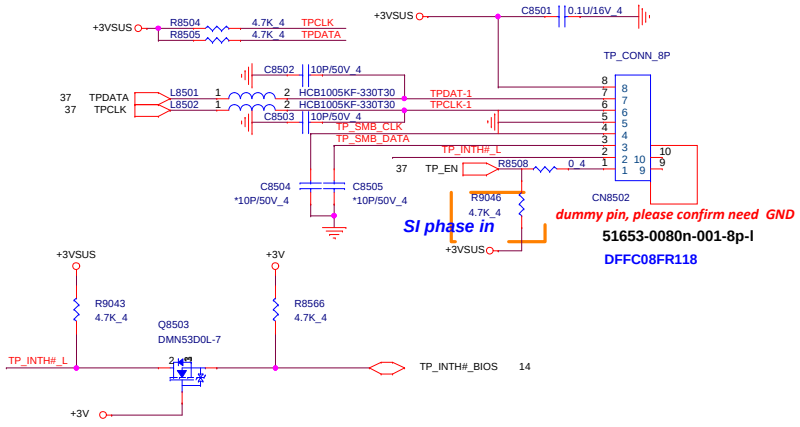


KB LIGHT CONN

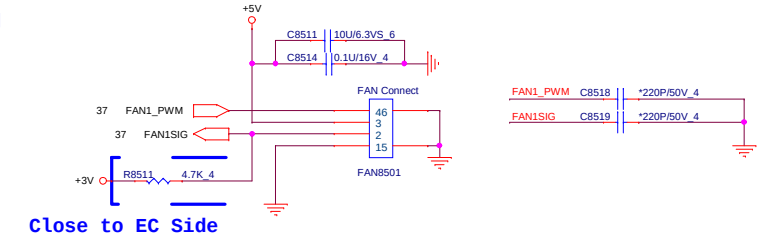


Touch Pad Connector





FAN



BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	33 -- KB/TP/FAN	1A
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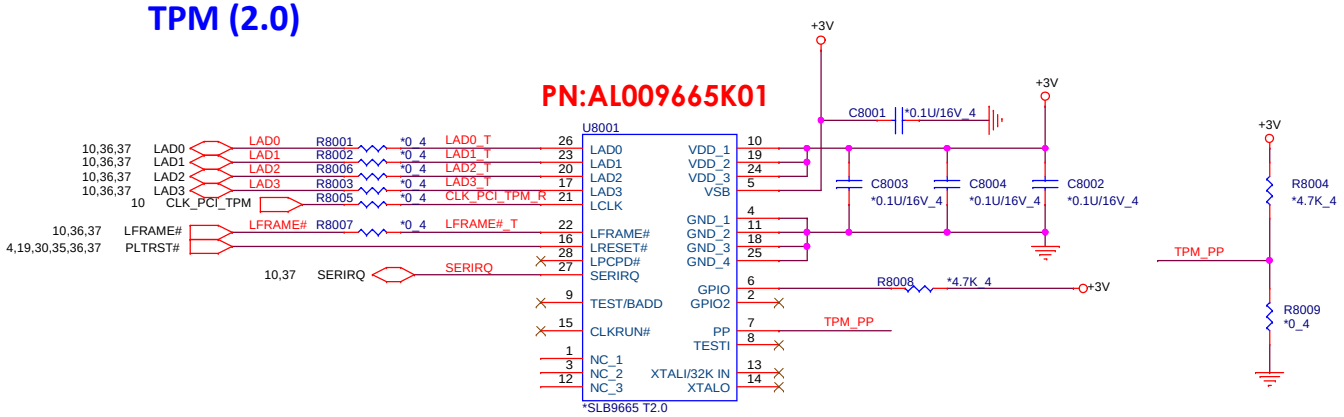
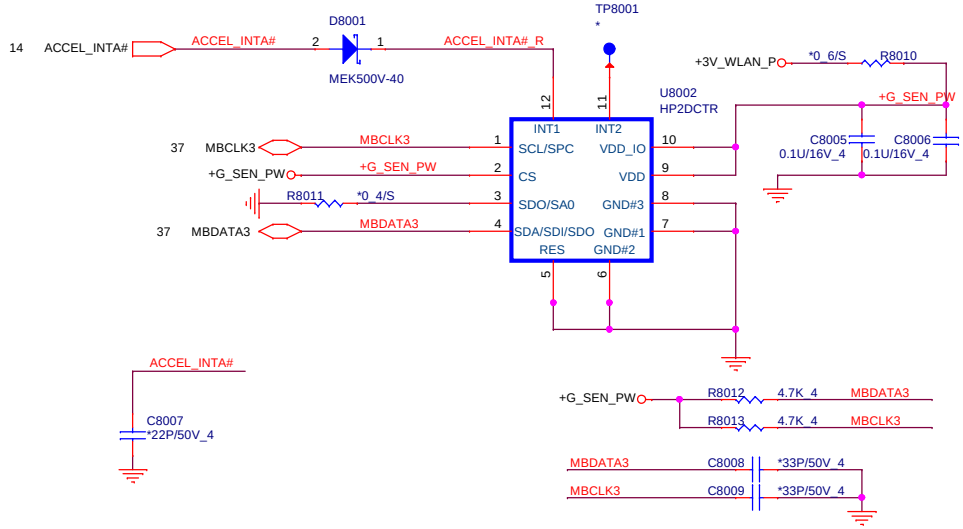
TPM (2.0)

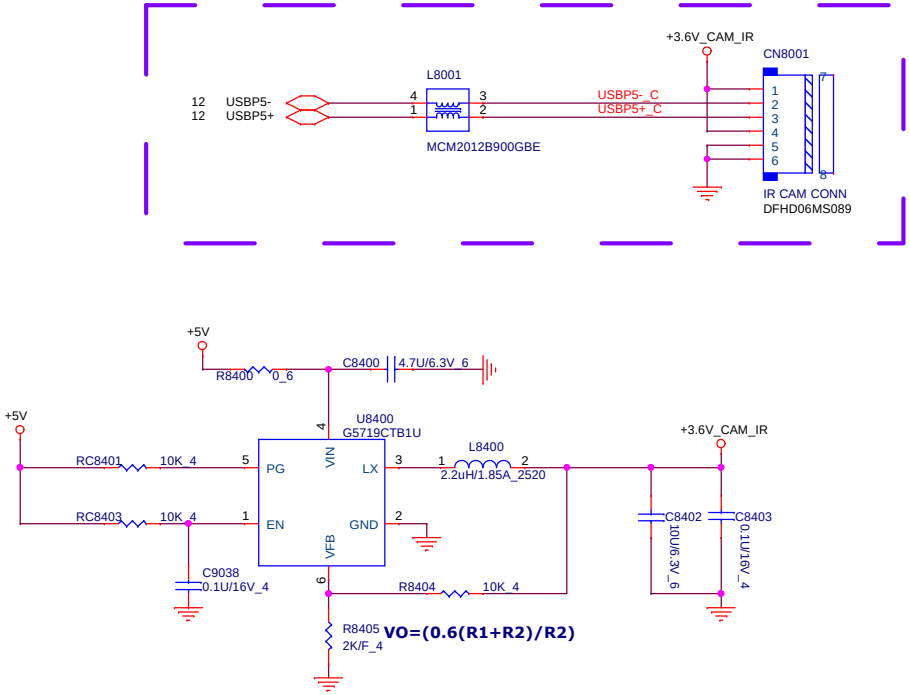


Accelerometer Sensor



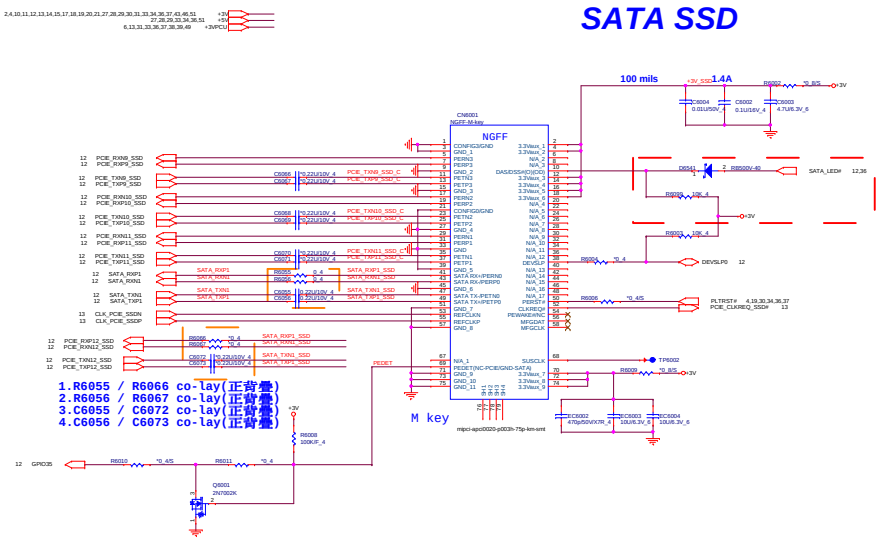
IR CAM

current:4A



BU5	**PROJECT : NFLP_KBLU_DR** Quanta Computer Inc.	
Size: Custom	Document Number: 34 -- TPM/G-Sensor/IR CAM	Rev: 1A
Date: Tuesday, December 13, 2016	Sheet 34 of 51	

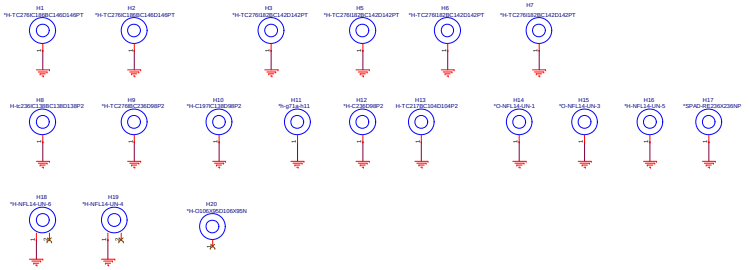
SATA SSD



eMMC

SATA ODD

Screw Hole



PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

BU5

Size	Document Number	Rev
Custom	3S – SSD_ODD_EMMC_ASM1154	1A
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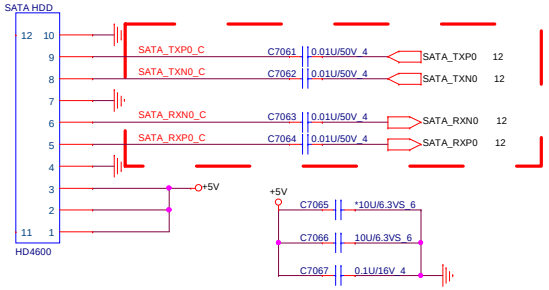
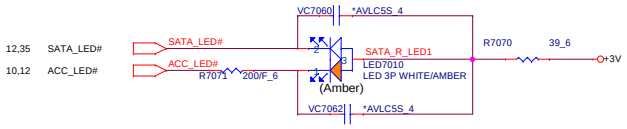
HDD

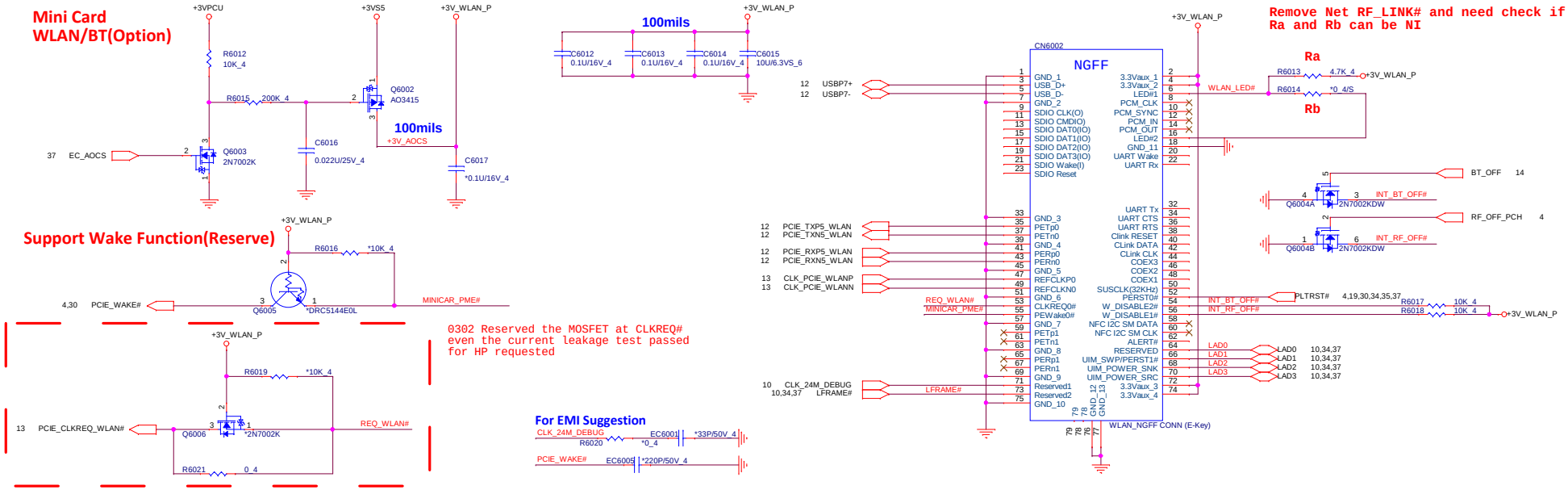
SATA HDD

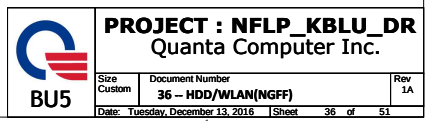


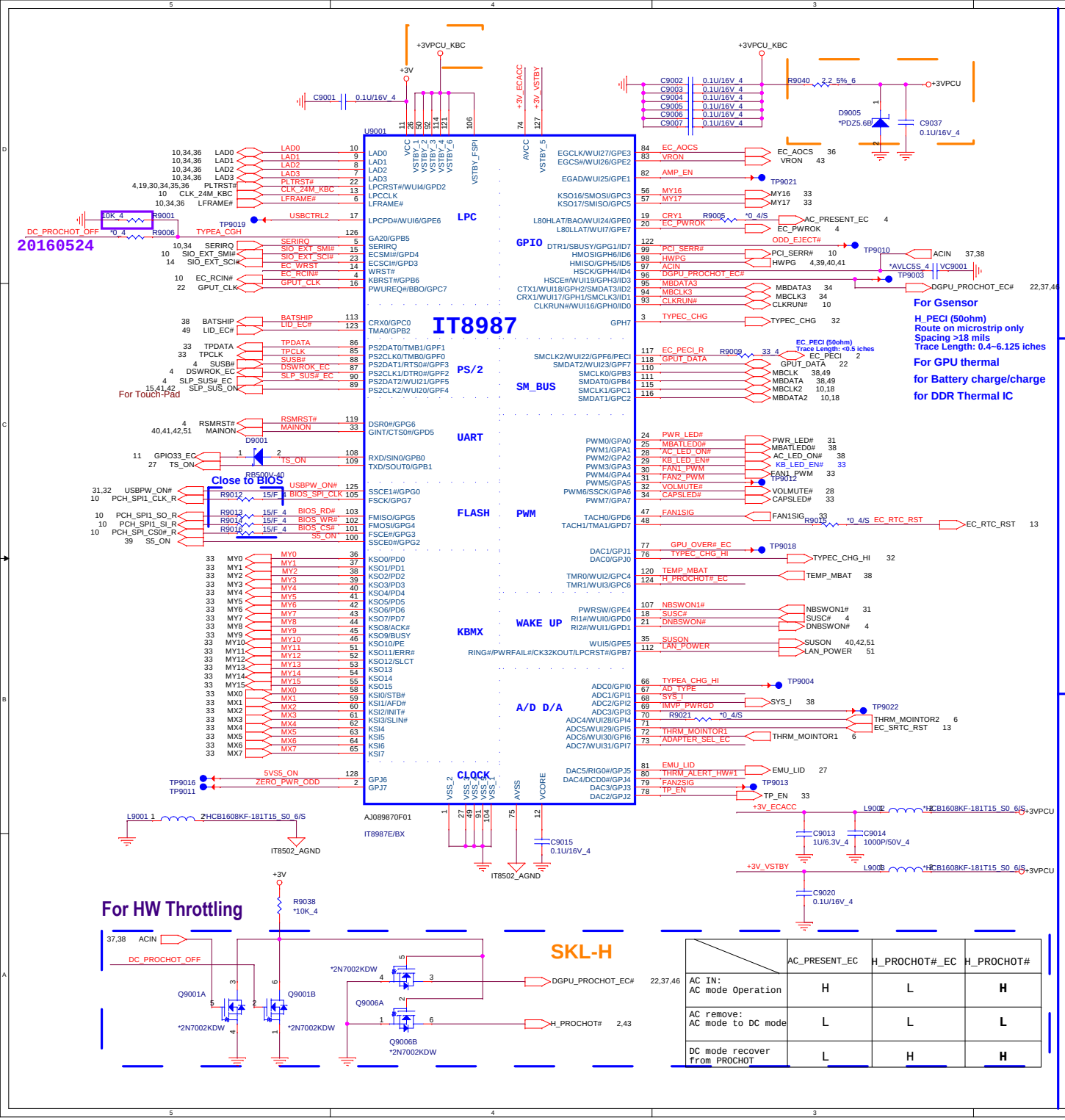
SATA LED



WLAN







	Ra	Rb	ADAPTER_SEL_EC	BOM
200W				
150W	10K(CS31002FB26)	27.4K(CS32742FB14)	3V	
120W	10K(CS31002FB26)		2.25V	
90W	10K(CS31002FB26)		1.5V	
65W	10K(CS31002FB26)	2.94K(CS22942FB0)	0.75V	DIS
45W	NC	10K(CS31002FB26)	0V	UMA

	AC_PRESENT_EC	H_PROCHOT#_EC	H_PROCHOT#
AC IN: AC mode Operation	H	L	H
AC remove: AC mode to DC mode	L	L	L
DC mode recover from PROCHOT	L	H	H

PROJECT	NFLP_KBLU_DR
Quanta Computer Inc.	
Size: Custom	Document Number: 37 -- EC (IT8987)
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+3VPCU 6,13,31,33,36,37,38,39,49
+5VPCU 28,39,48,51
+BAT_RTC 4,13,15,31,49
+VIN 27,33,39,40,41,44,45,46,47,50
+3VPCU 6,13,31,33,36,37,38,39,49

ADP=65W

3S1P 41Whr

CN1
51483-00801-V01_Header

N-channel MOS

PQ1 AP0203GMT-HF
PQ2 AON7408
PQ3 AON6414AL

PL2 *Short_0805
PL1 *Short_0805
PL3 *Short_0805
PL4 *Short_0805
PL5 4.7uH_7x7x3

PD1 P4SMAFJ20A
PD2 *P4SMAFJ20A
PD3 *PDZ5.6B
PD4 *PDZ5.6B
PD5 *PDZ5.6B
PD6 RB500V-40
PD7 *RB500V-40
PD1000 1N4448WS-7-F
PD1001 1N4448WS-7-F

PQ5 METR3904-G
PQ6 AON7408
PQ7 AON7408
PQ8 METR3904-G
PQ9 2N7002K
PQ10 2N7002K
PQ11 METR3904-G
PQ1000 2N7002K

PU9 BQ24738HRGRR

CN2 BP28BC-B401Q-9H

Place this ZVS close to DC_IN conn

Do Not add test pad on BATDIS_G signal

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

Place this R&C close to EC

+BAT_RTC SET
BAT= 1S---10-ohm
BAT >2S---100ohm

ACDET

VIN>22.5V (AC OVP)
VIN>17.2V (Enable Charging)
VIN>15.2V (AC present)

Vacdet=2.4V

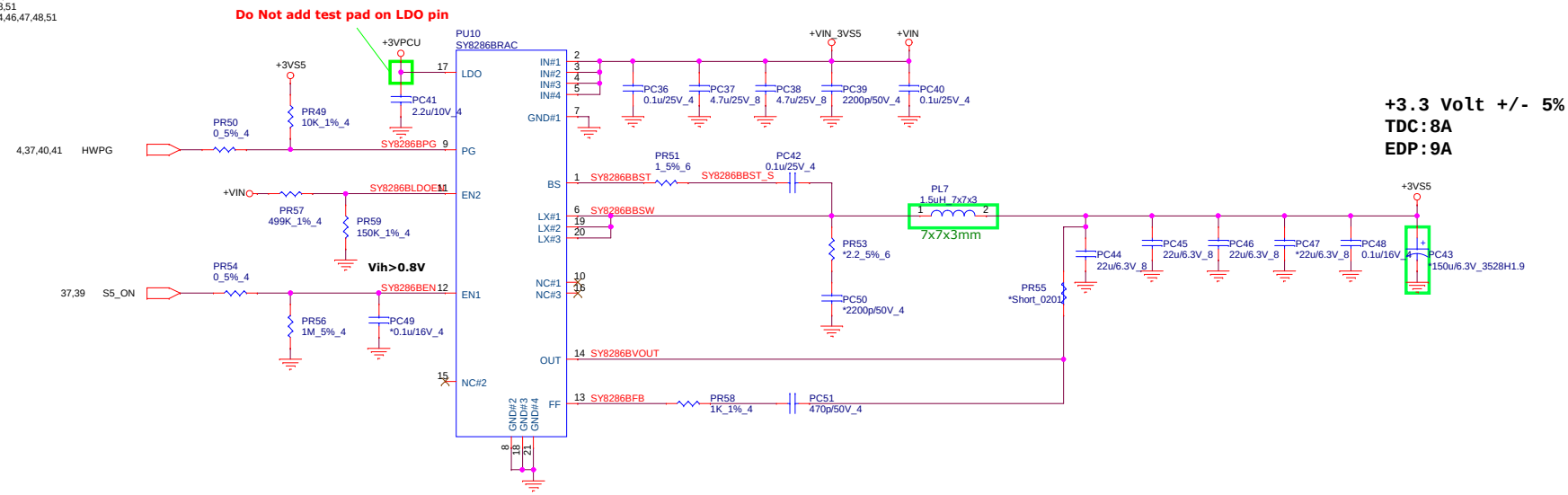
Ra

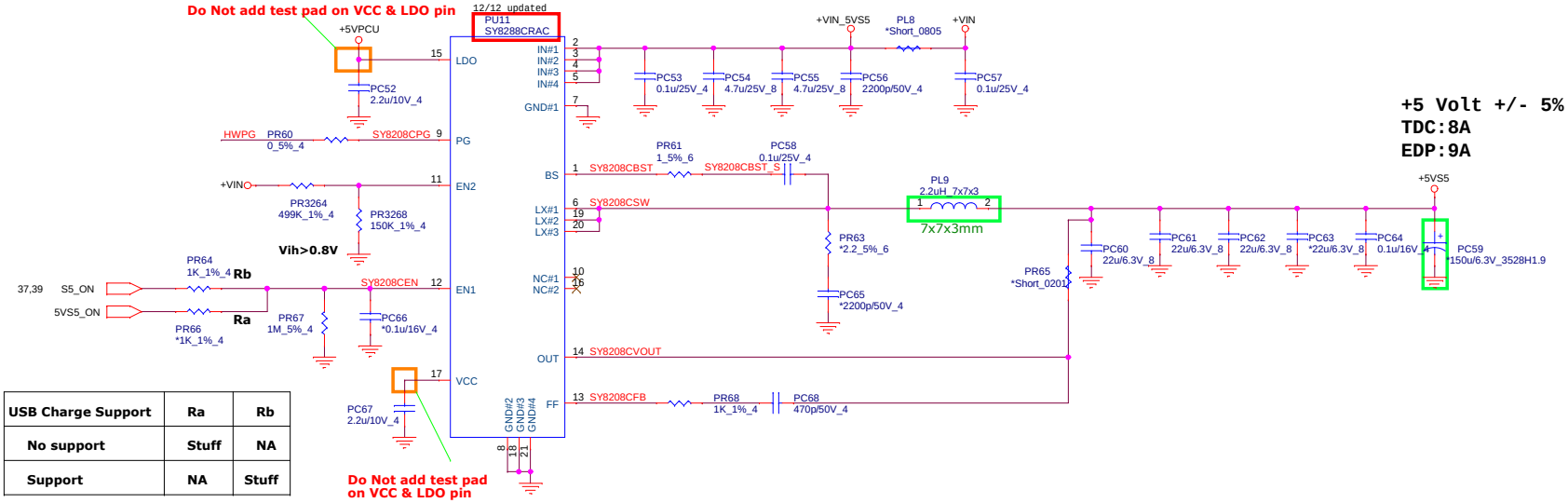
MIN. BATV=7.2V

BU5	**PROJECT : NFLP_KBLU_DR** Quanta Computer Inc.		
	Size: Custom	Document Number: Charger (BQ24738H)	Rev: 1A
	Date: Tuesday, December 13, 2016	Sheet 38 of 51	

DC/DC +3VS5/+5VS5

+VIN 27,33,38,40,41,44,45,46,47,50
+3VS5 4,10,15,36,37,40,41,42,48,51
+5VS5 4,28,31,32,40,41,42,43,44,46,47,48,51
+3VPCU 6,13,31,33,36,37,38,49
+5VPCU 28,38,48,51





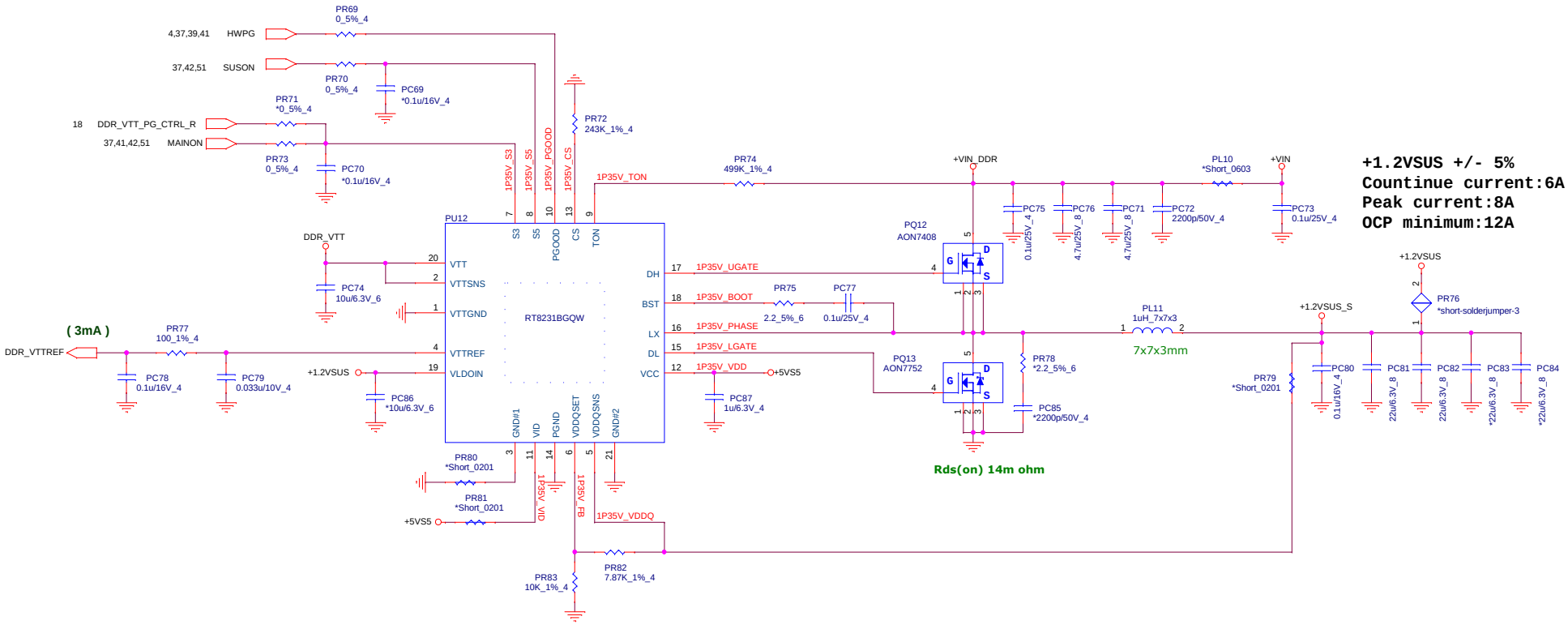
USB Charge Support	Ra	Rb
No support	Stuff	NA
Support	NA	Stuff

BU5

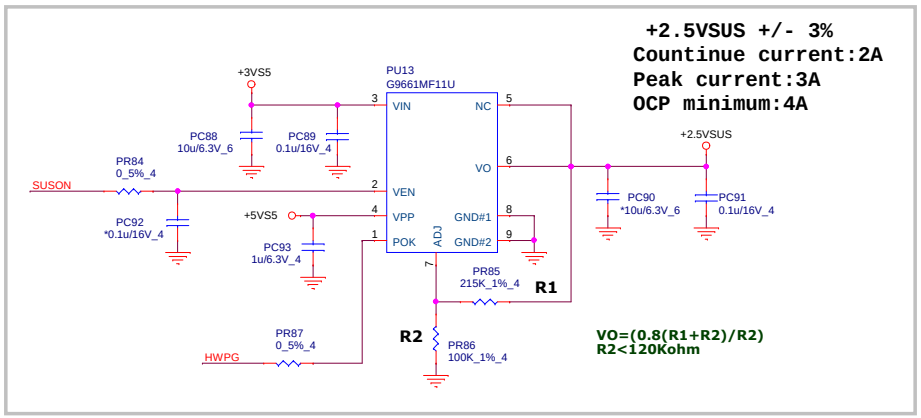
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A
Date: Tuesday, December 13, 2016	Sheet 39 of 51	

+VIN 27,33,38,39,41,44,45,46,47,50
+5VS5 4,28,31,32,39,41,42,43,44,46,47,48,51
+1.2VSUS 3,6,17,18,42,48
DDR_VTT 17,18



20151015 updated



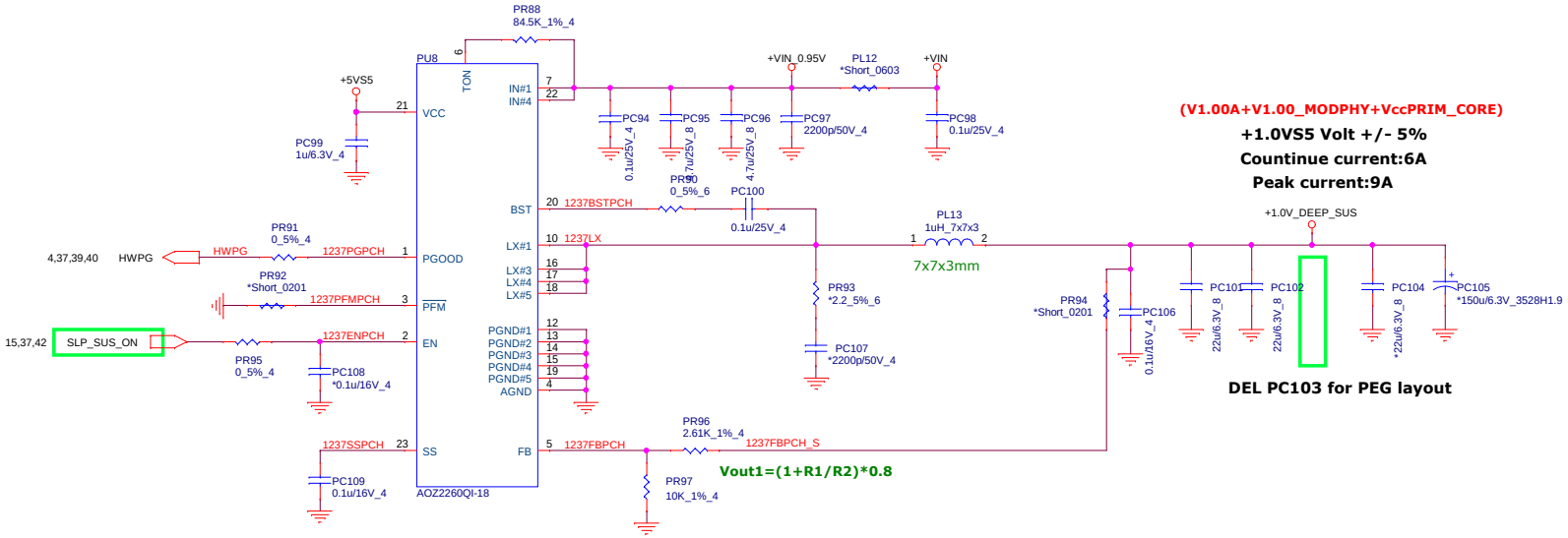
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

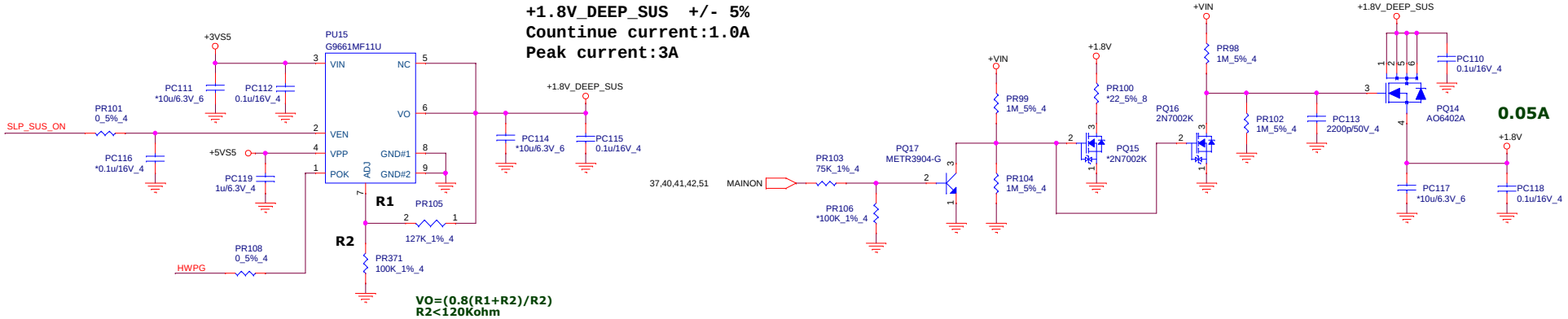
BU5

Size	Document Number	Rev
	DDR4 (G5619RZ1U)	1A

Date: Tuesday, December 13, 2016 Sheet 40 of 51

+VIN 27,33,38,39,40,44,45,46,47,50
+3VS5 4,10,15,36,37,39,40,42,48,51
+5VS5 4,28,31,32,39,40,42,43,44,46,47,48,51
+1.0V_DEEP_SUS 9,13,15,42
+1.8V_DEEP_SUS 9,15
MAINON 37,40,41,42,51
+1.5V





BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

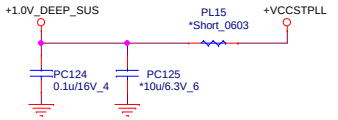
Size	Document Number	Rev
Custom	+1.0V/+1.8V_DEEP_SUS	1A
Date: Tuesday, December 13, 2016	Sheet 41 of 51	

+1.0V 2,4,6,37
+3VS5 4,10,15,36,37,39,40,41,48,51
+5VS5 4,28,31,32,39,40,41,43,44,46,47,48,51
+VCCIO 2,6
+1.2VSUS 3,6,17,18,40,48
+VCCSTPLL 2,4,5,6,9,43
+1.0V_DEEP_SUS 9,13,15,41
+1.2V_VCCPLL_OC 6
MAINON 37,40,41,51

Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)

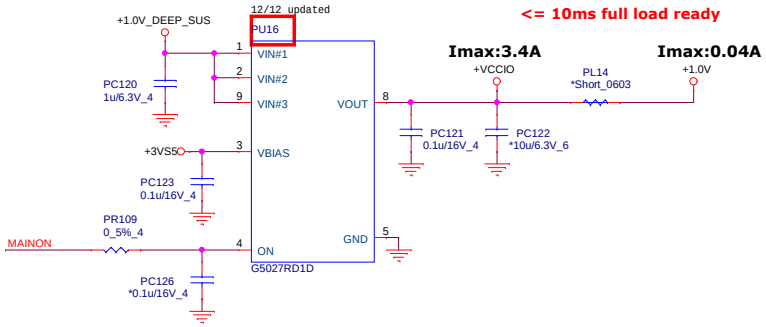
Imax:0.24A

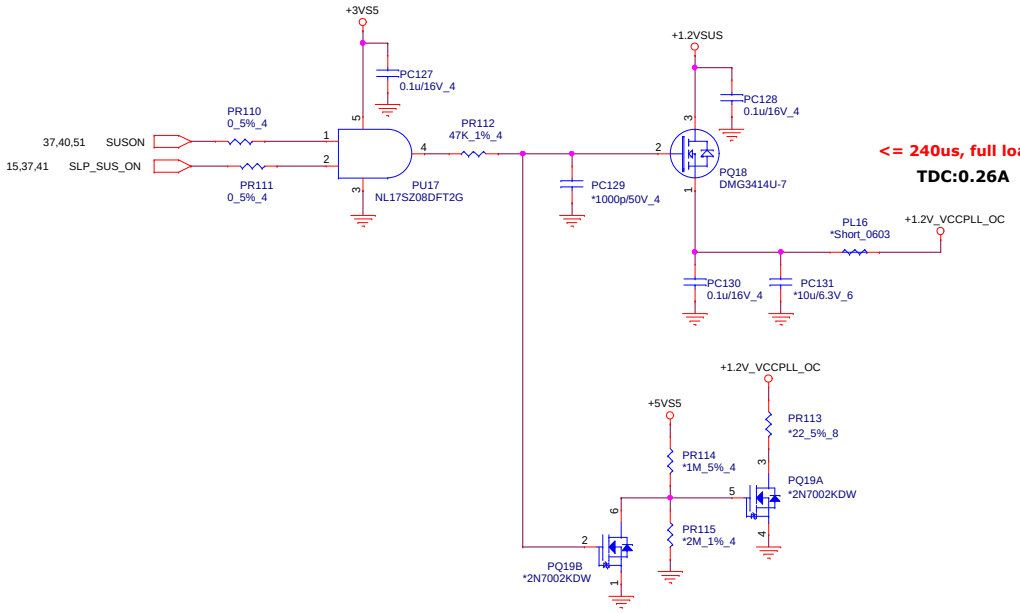


Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 3.4A

<= 10ms full load ready

Imax:3.4A **Imax:0.04A**



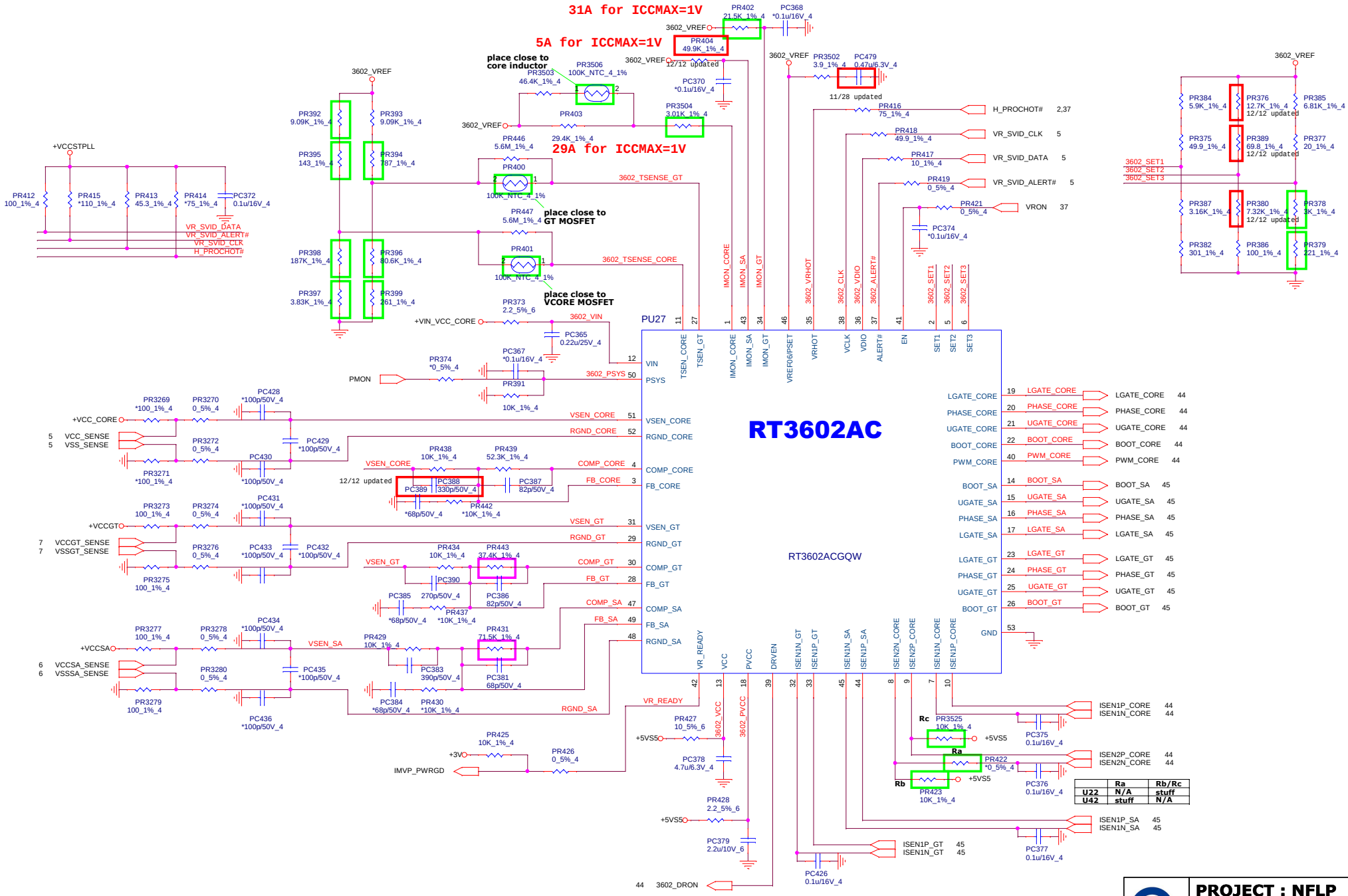


<= 240us, full load ready
TDC:0.26A

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL	1A
Date: Tuesday, December 13, 2016	Sheet 42 of 51	


31A for ICCMAX=1V
5A for ICCMAX=1V
29A for ICCMAX=1V
RT3602AC
RT3602ACGQW
PU27
place close to core inductor
place close to GT MOSFET
place close to VCORE MOSFET
3602_VREF
+VCCSTPLL
+VIN_VCC_CORE
PMON
+VCC_CORE
+VCCGT
+VCCSA
IMVP_PWRGD
3602_DRON
VR_SVID_DATA
VR_SVID_ALERT#
VR_SVID_CLK
H_PROCHOT#
3602_TSENSE_GT
3602_TSENSE_CORE
3602_VIN
3602_PSYS
VSEN_CORE
RGND_CORE
VSEN_GT
RGND_GT
VSEN_SA
RGND_SA
COMP_CORE
FB_CORE
COMP_GT
FB_GT
COMP_SA
FB_SA
VR_READY
3602_VCC
3602_PVCC
IMON_CORE
IMON_SA
IMON_GT
3602_VRHOT
3602_CLK
3602_VDIO
3602_ALERT#
3602_SET1
3602_SET2
3602_SET3
VRON
LGATE_CORE
PHASE_CORE
UGATE_CORE
BOOT_CORE
PWM_CORE
LGATE_SA
UGATE_SA
PHASE_SA
BOOT_SA
LGATE_GT
PHASE_GT
UGATE_GT
BOOT_GT
ISEN1P_CORE
ISEN1N_CORE
ISEN2P_CORE
ISEN2N_CORE
ISEN1P_SA
ISEN1N_SA
ISEN1P_GT
ISEN1N_GT
Rc
Ra
Rb
Ra
Rb/Rc
U22
N/A
stuff
U42
stuff
N/A
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.
BU5
CPU VR IC (RT3602AC)
Size Custom
Document Number
Rev 2A
Date: Tuesday, December 13, 2016
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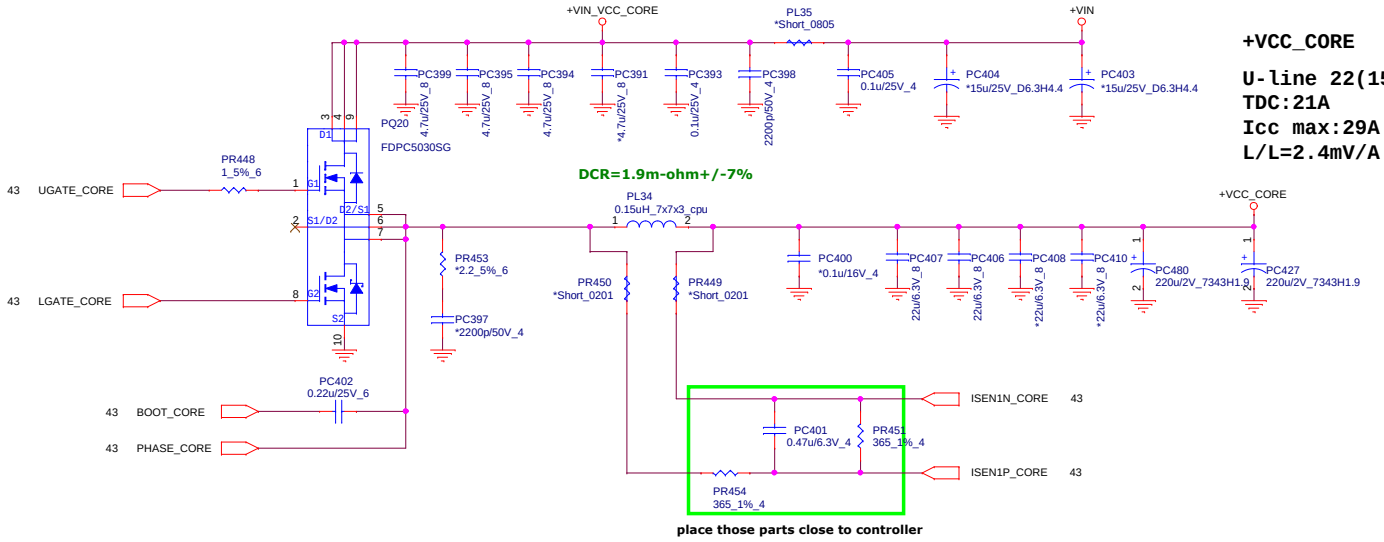
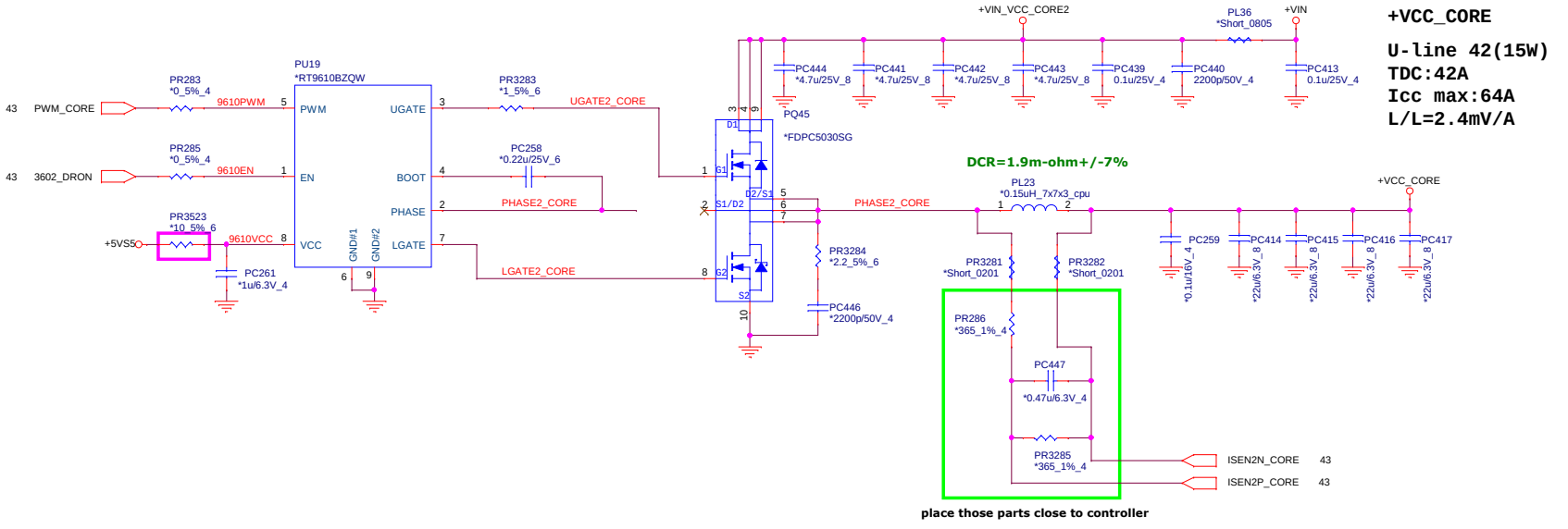
+VIN 27,33,38,39,40,41,45,46,47,50
+5VS5 4,28,31,32,39,40,41,42,43,46,47,48,51



For U42 --> Add These Components



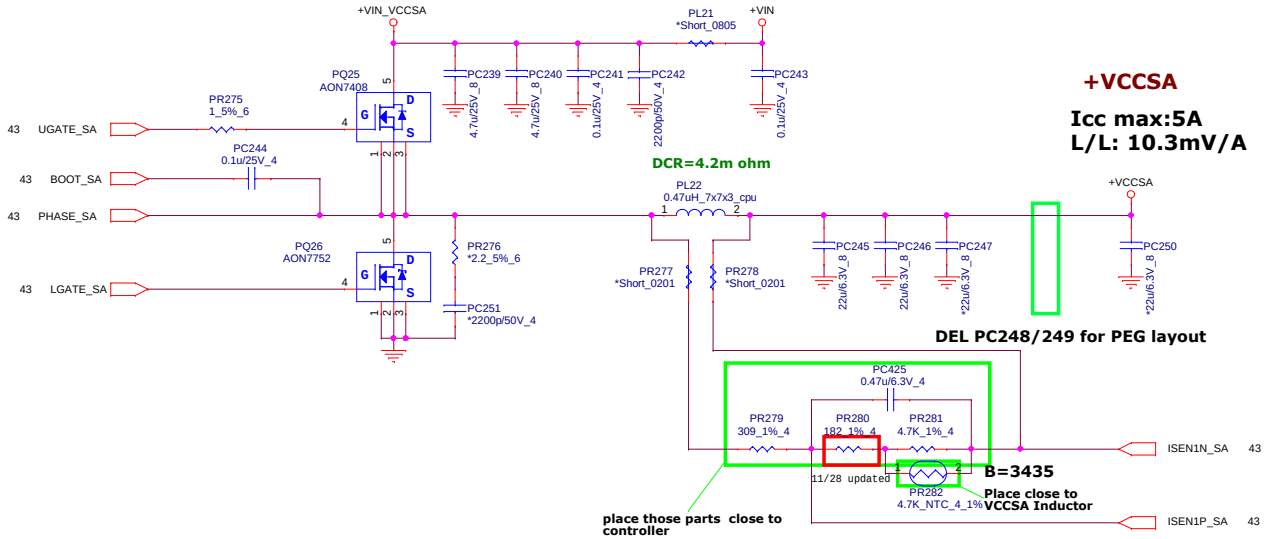
BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

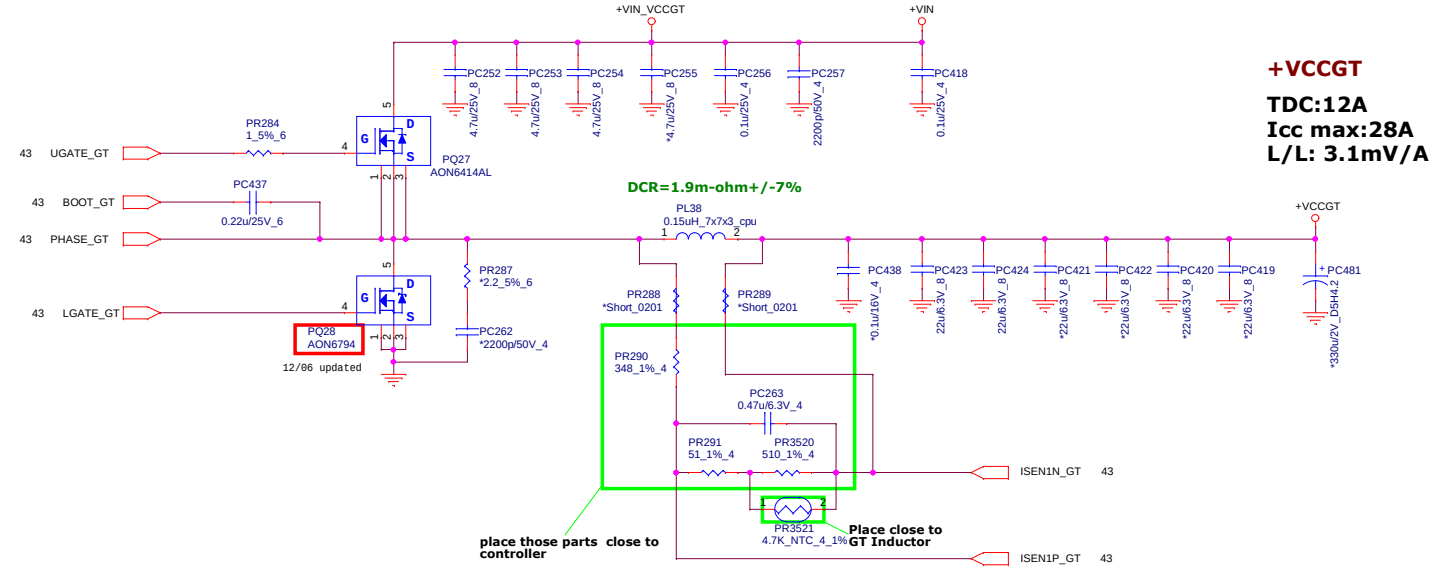
Size	Document Number	Rev
Custom	+VCCSA (NCP81253)	2A

Date: Tuesday, December 13, 2016 Sheet 44 of 51

+VIN 27,33,38,39,40,41,44,46,47,50
+5VS5 4,28,31,32,39,40,41,42,43,44,46,47,48,51
+VCCSA 6,43
+VCCGT 7,43



+VCCSA
Icc max:5A
L/L: 10.3mV/A



+VCCGT
TDC:12A
Icc max:28A
L/L: 3.1mV/A

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCCSA (NCP81253)	2A

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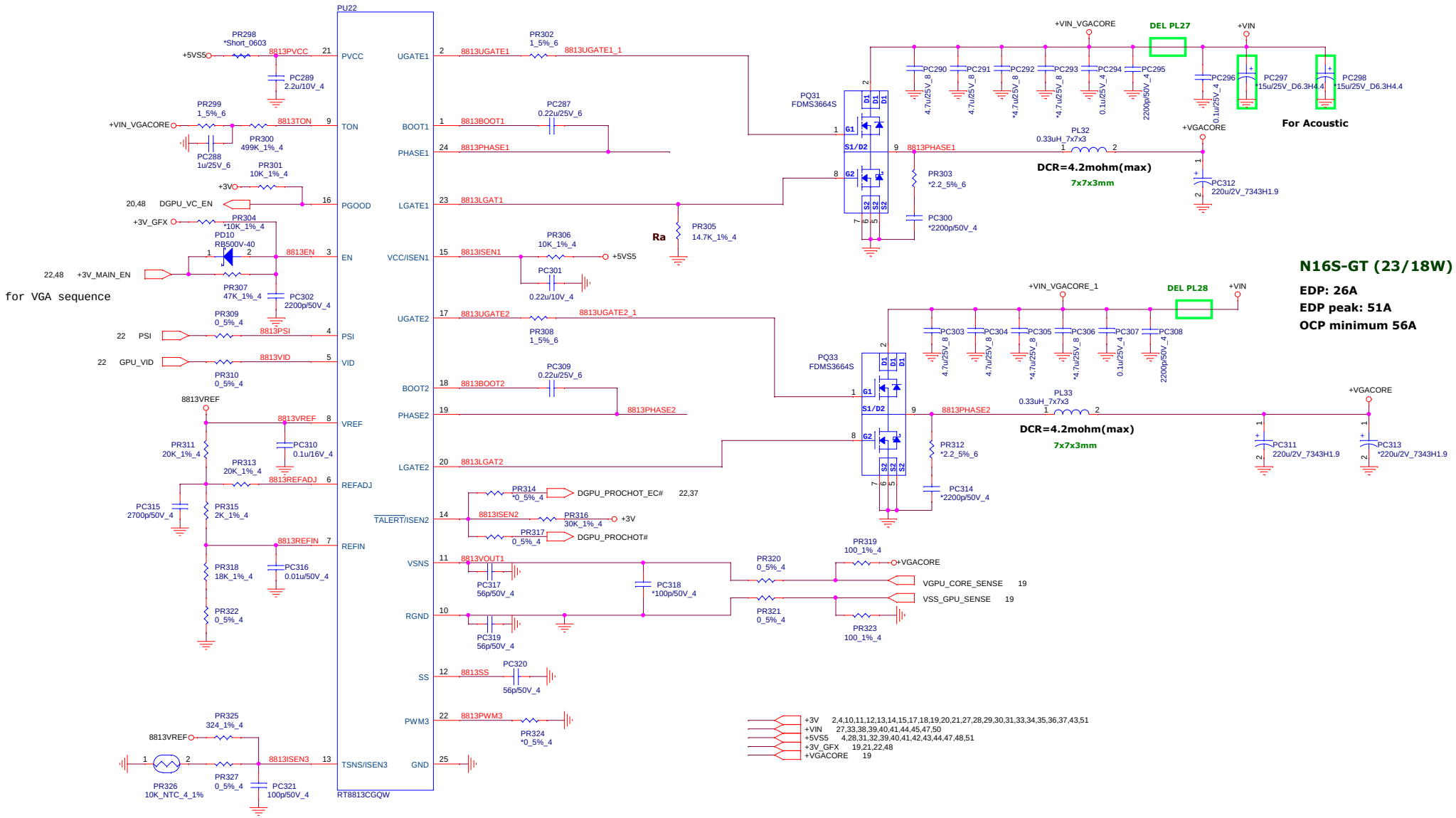
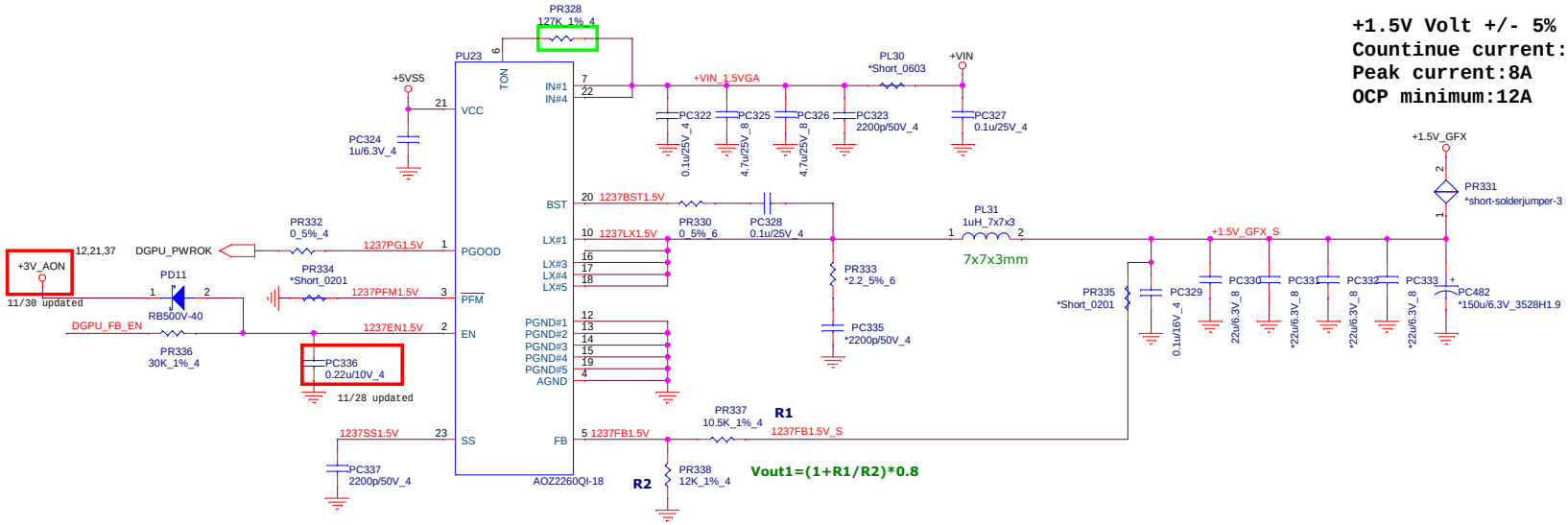
VGA Core

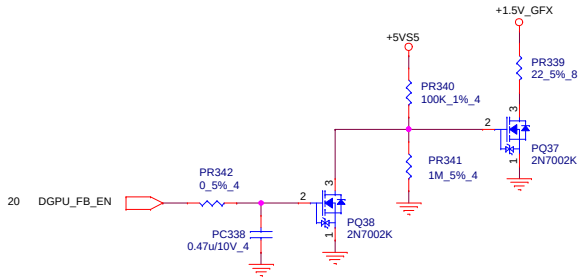


BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.	
Size: Custom	Document Number: +VGACORE (RT8813C)	Rev: 2A
Date: Tuesday, December 13, 2016	Sheet 46 of 51	

+VIN 27,33,38,39,40,41,44,45,46,50
+5VS5 4,28,31,32,39,40,41,42,43,44,46,48,51
+1.5V_GFX 20,21,23,24,25,26

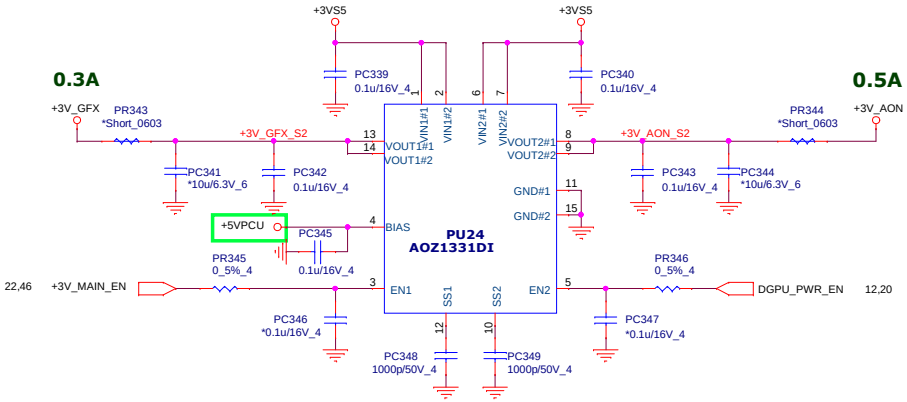
+1.5V Volt +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A

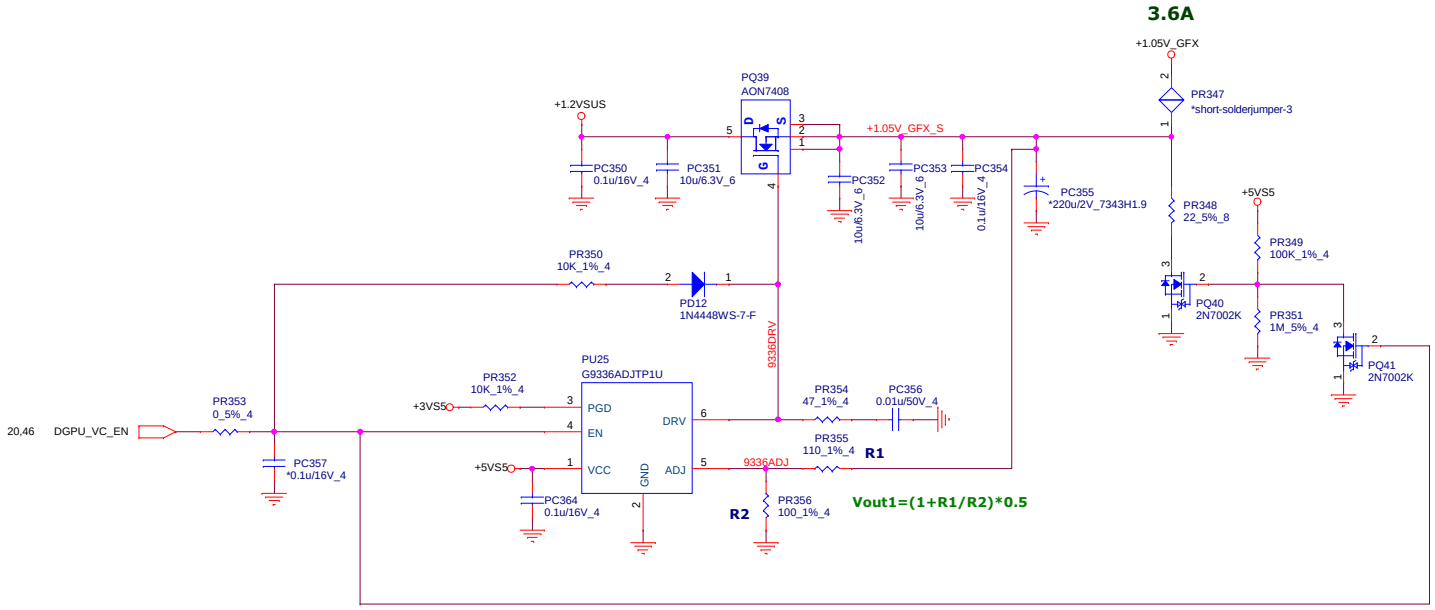




BU5	**PROJECT : NFLP_KBLU_DR** Quanta Computer Inc.	
Size: Custom	Document Number: +1.5V_GFX (AOZ2260QI-18)	Rev: 1A
Date: Tuesday, December 13, 2016	Sheet 47 of 51	

+VIN 27,33,38,39,40,41,44,45,46,47,50
+3VS5 4,10,15,36,37,39,40,41,42,51
+5VS5 4,28,31,32,39,40,41,42,43,44,46,47,51
+3V_GFX 19,21,22,46
+3V_AON 19,22,47
+1.2VSUS 3,6,17,18,40,42
+1.05V_GFX 19,20,21



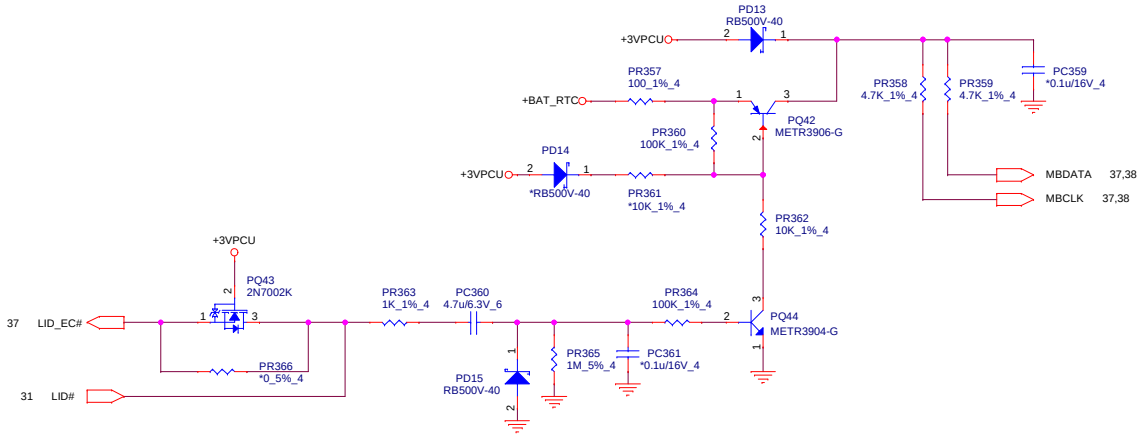


BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+3V/+1.05V_GFX(APL3523A)	1A
Date: Tuesday, December 13, 2016	Sheet 48 of 51	

+3VPCU 6,13,31,33,36,37,38,39
+BAT_RTC 4,13,15,31,38

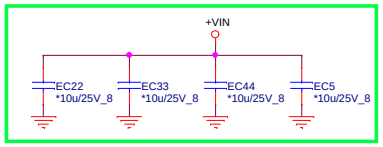


BU5

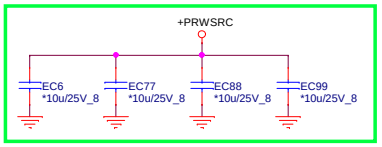
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LID SW for storage mode	1A
Date: Tuesday, December 13, 2016	Sheet 49 of 51	

EMI request for ISN



EMI request for ISN

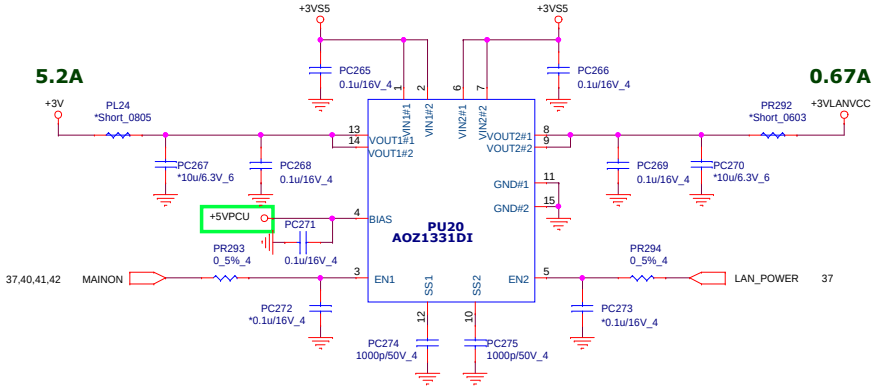


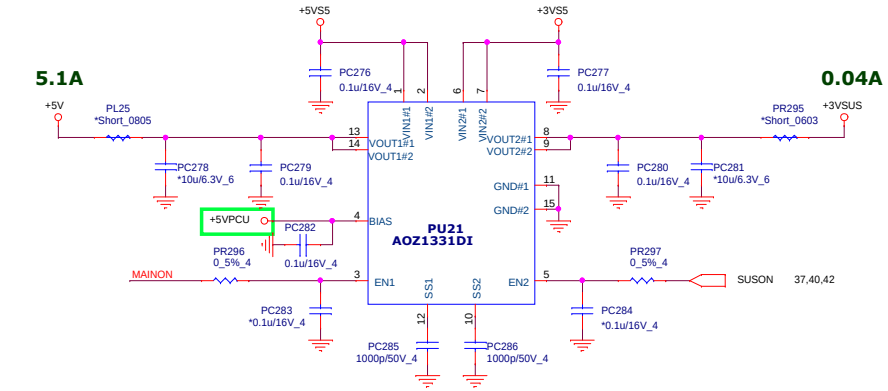
BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EMI solution	1A
Date: Tuesday, December 13, 2016	Sheet 50 of 51	

+3V 2,4,10,11,12,13,14,15,17,18,19,20,21,27,28,29,30,31,33,34,35,36,37,43,46
+5V 27,28,29,33,34,36
+VIN 27,33,38,39,40,41,44,45,46,47,50
+3VS5 4,10,15,36,37,39,40,41,42,48
+5VS5 4,28,31,32,39,40,41,42,43,44,46,47,48
+3VSUS 33
+5VPCU 28,38,39,48
+3VLANVCC 30





BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Load switch IC (APL3523A)	1A
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