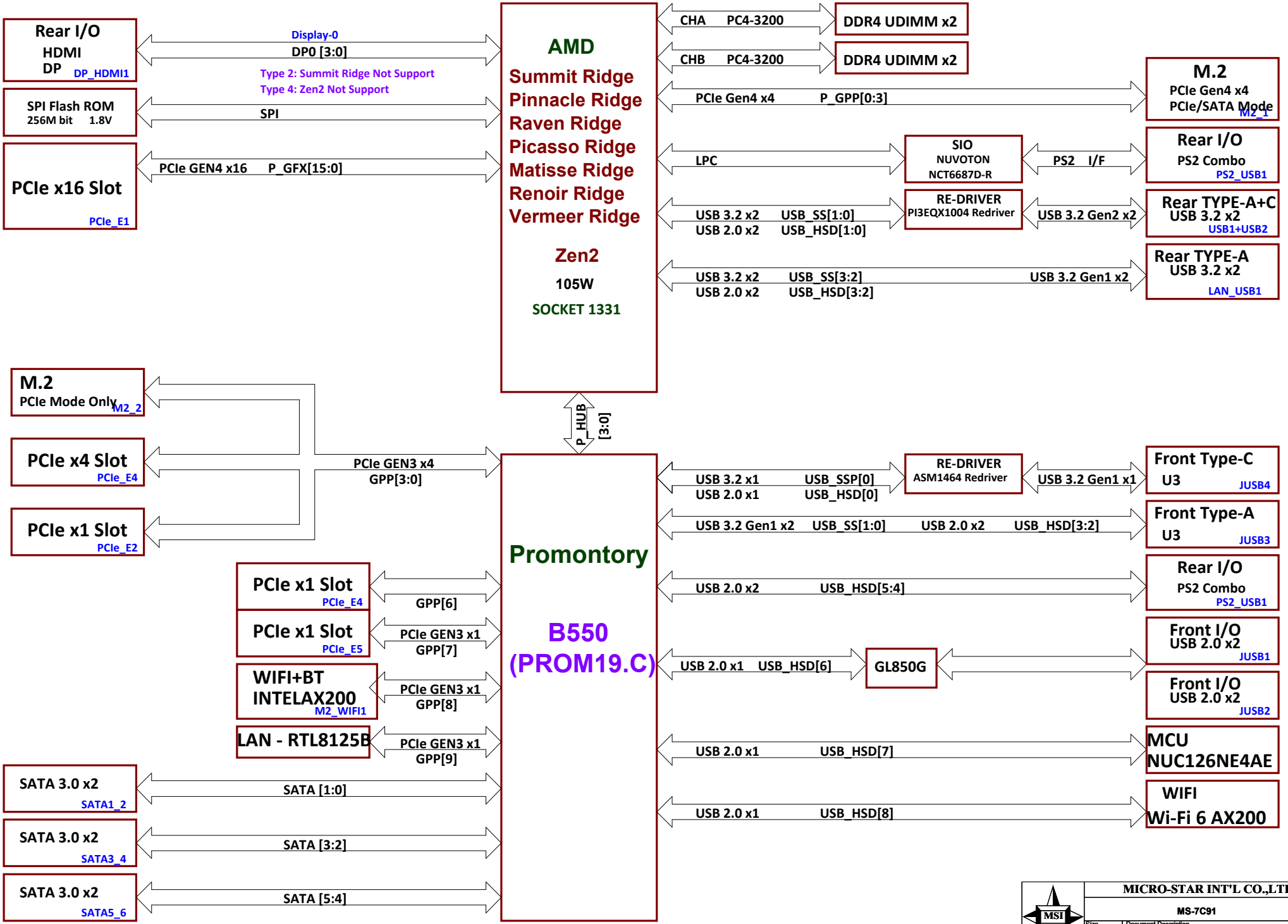
AMD AM4
B550

MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	Cover Sheet	21

Date: Tuesday, April 21, 2020 Sheet 1 of 78

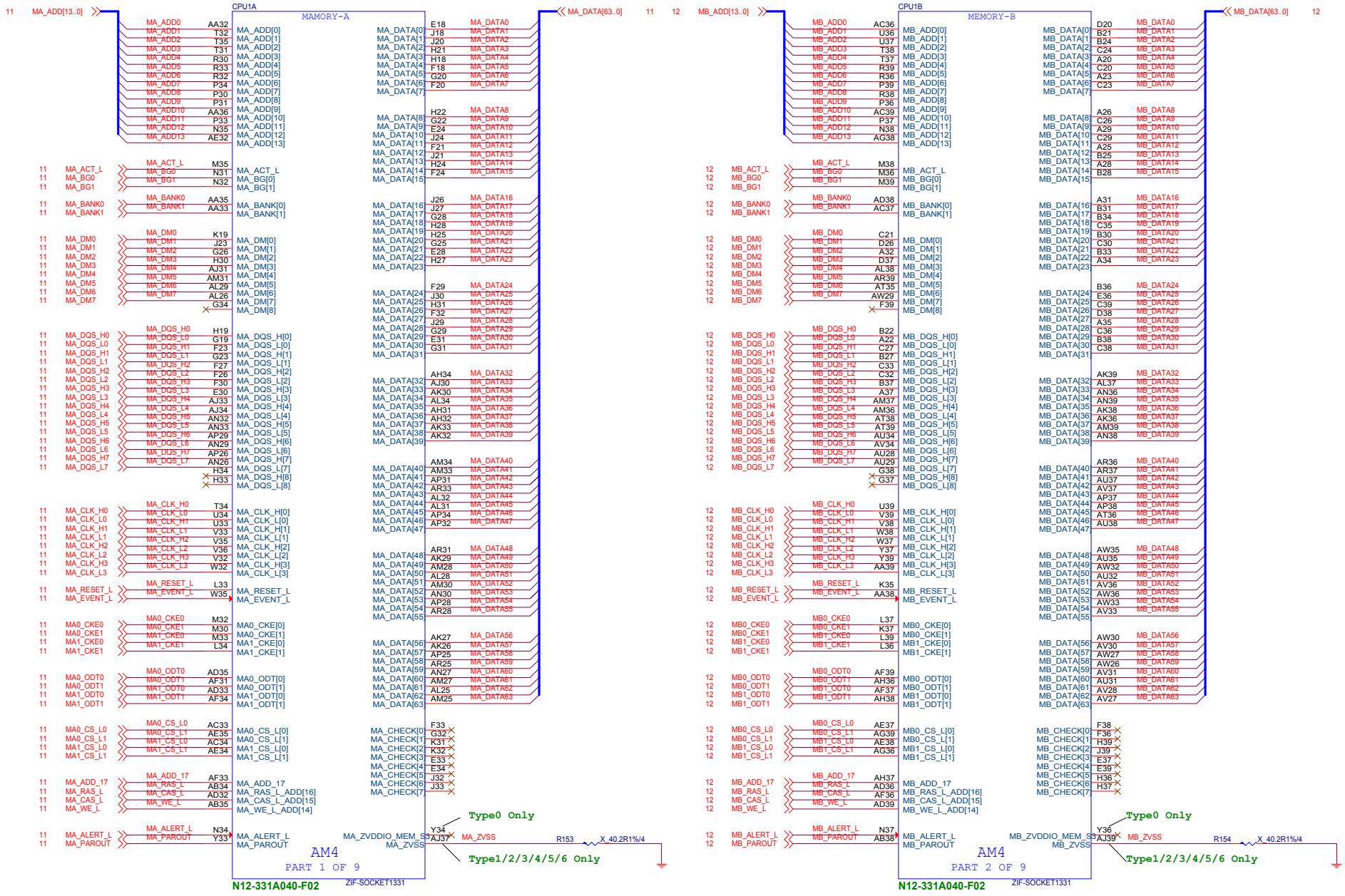


MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	Block Diagram	21

Date: Tuesday, April 21, 2020 Sheet 2 of 78

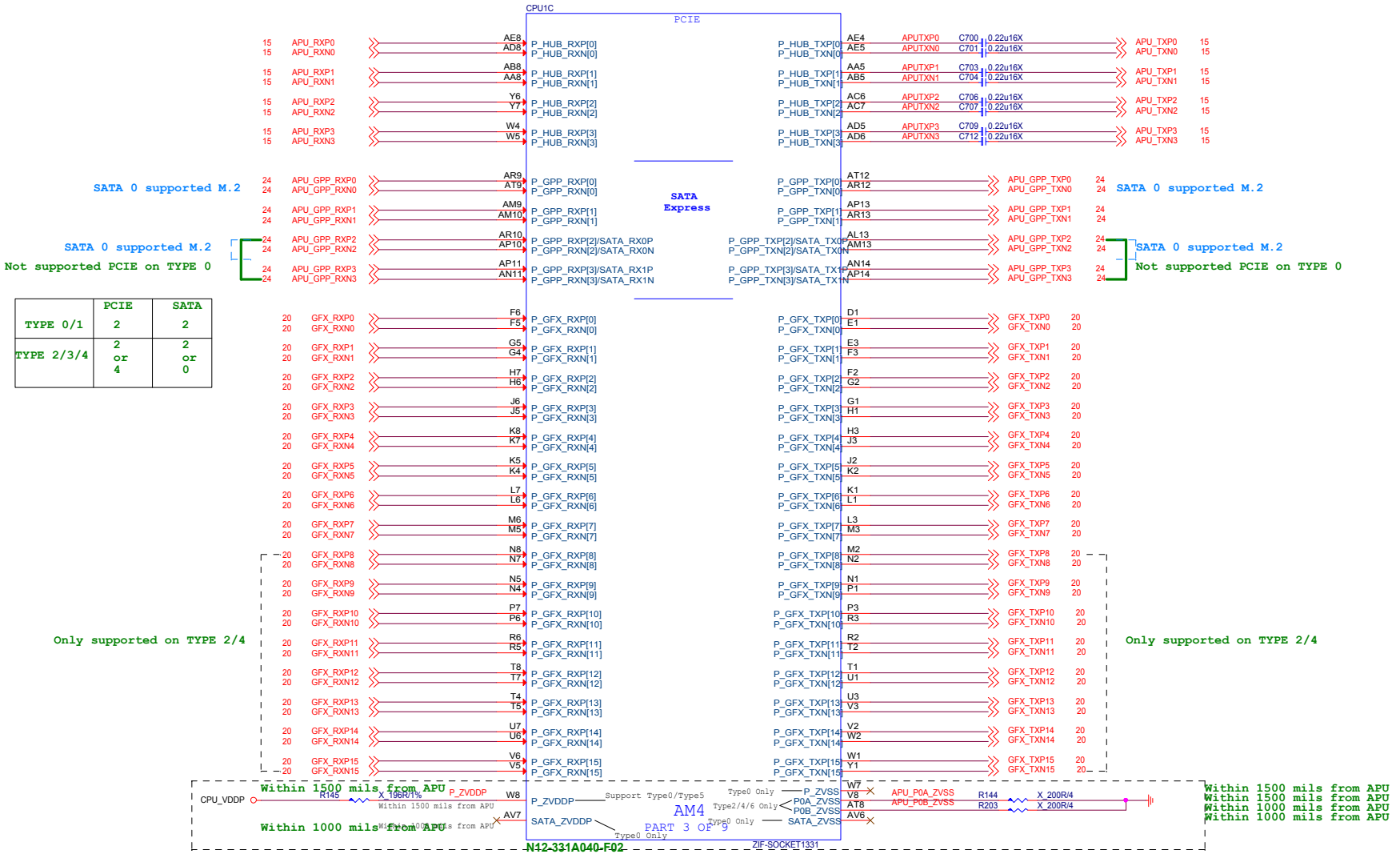


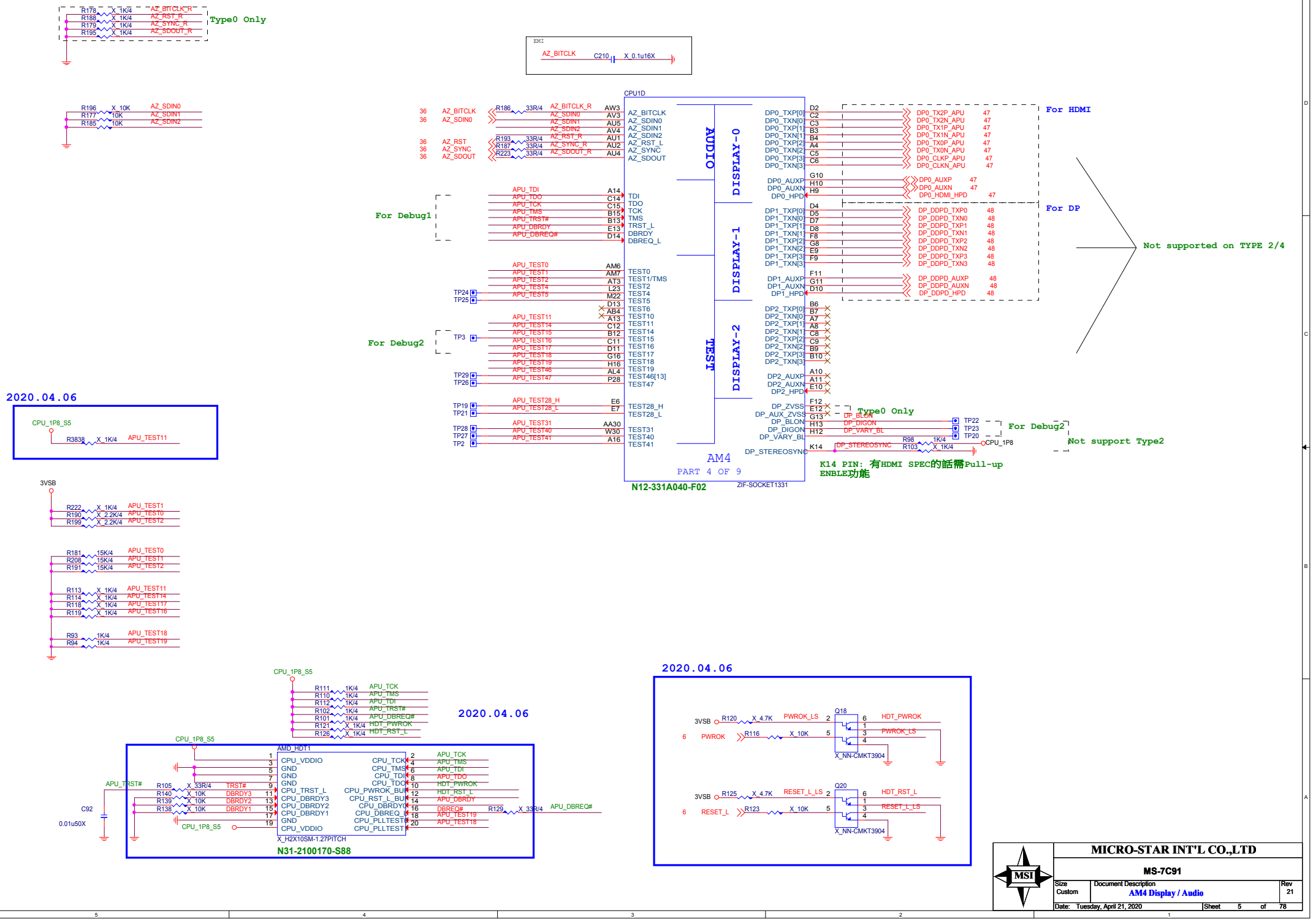
MICRO-STAR INT'L CO.,LTD

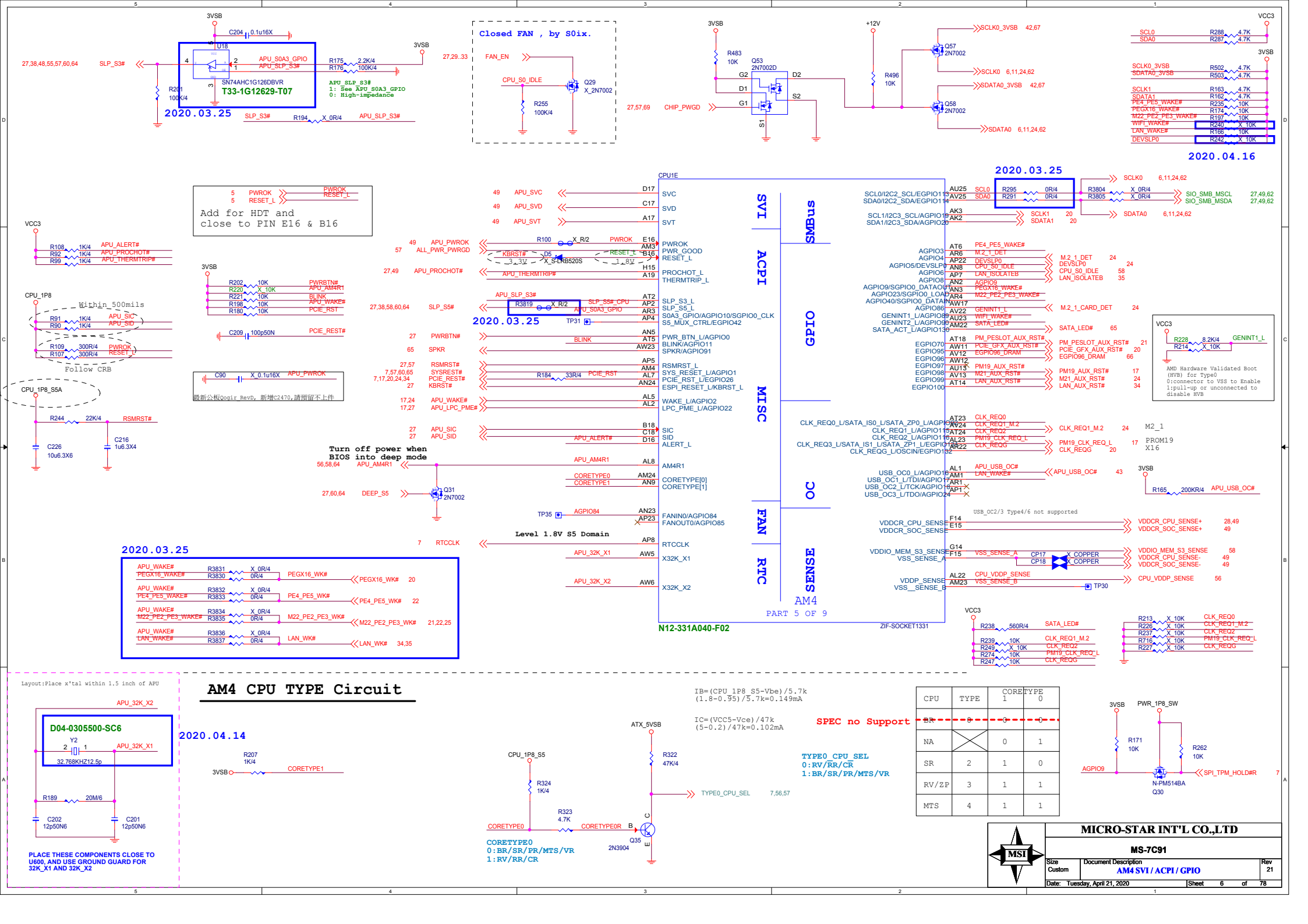
MS-7C91

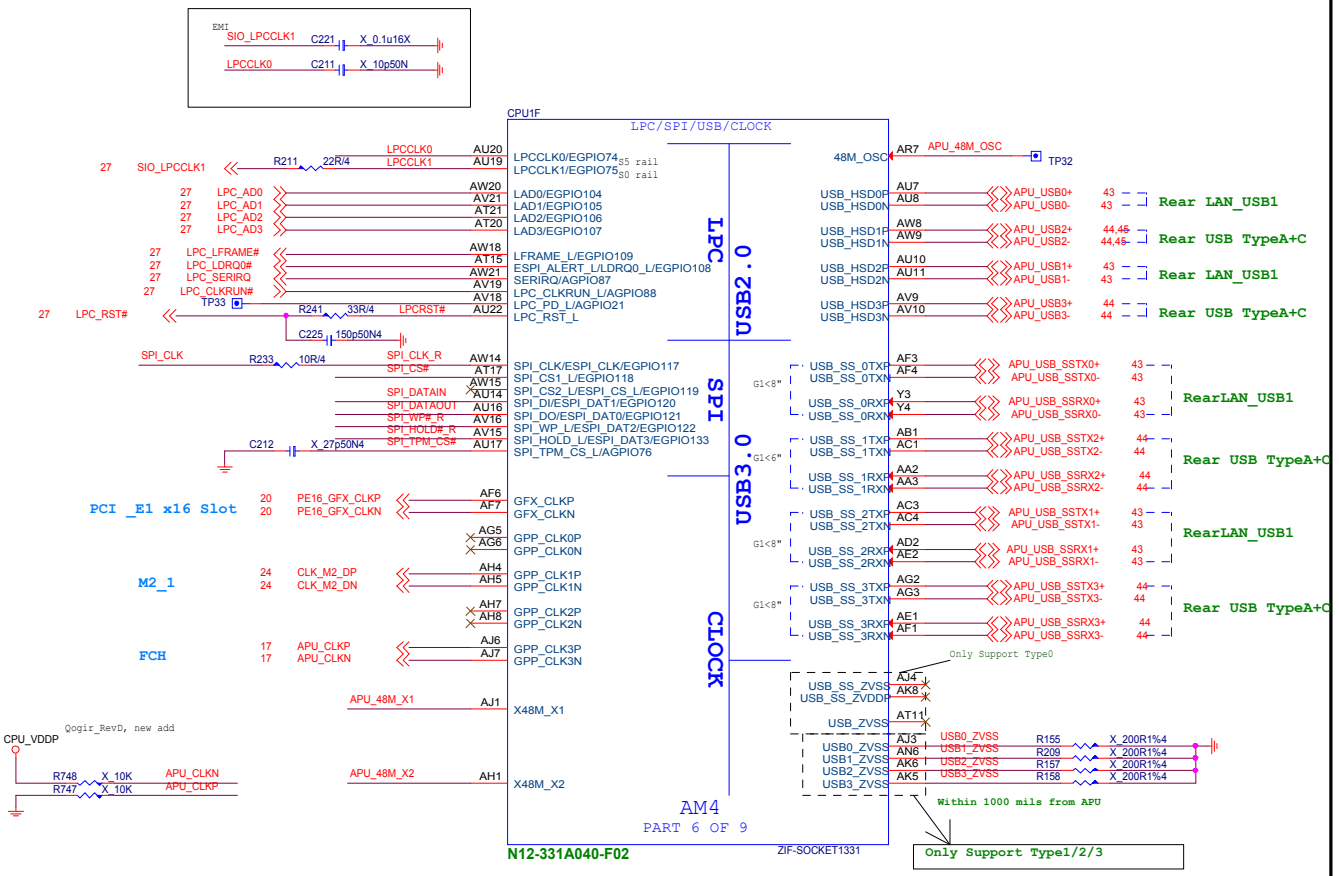
Size	Document Description	Rev
Custom	AM4 DDR4 I/F	21

Date: Tuesday, April 21, 2020 | Sheet 3 of 78

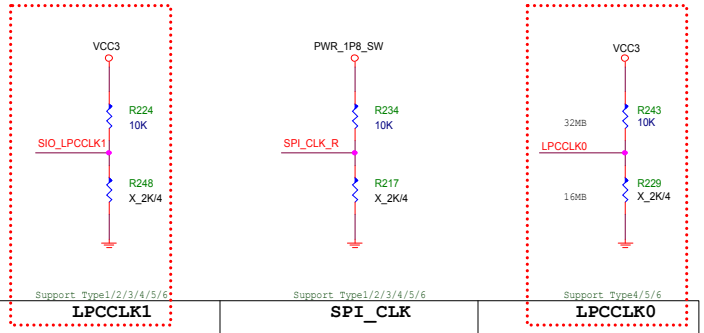

CPU1C
PCIE
SATA Express
AM4
PART 3 OF 9
N12-331A040-F02
ZIF-SOCKET1331
SATA 0 supported M.2
Not supported PCIE on TYPE 0
Only supported on TYPE 2/4
Within 1500 mils from APU
Within 1000 mils from APU
TYPE 0/1 | PCIE 2 | SATA 2
TYPE 2/3/4 | PCIE 2 or 4 | SATA 2 or 0


Type0 Only
EMI
AZ_BITCLK
C210
X_0.1u16X
CPU1D
AUDIO
DISPLAY-0
DISPLAY-1
DISPLAY-2
TEST
AM4
PART 4 OF 9
N12-331A040-F02
ZIF-SOCKET1331
For HDMI
For DP
Not supported on TYPE 2/4
For Debug1
For Debug2
Type0 Only
Not support Type2
K14 PIN: 有HDMI SPEC的話需Pull-up
ENBLE功能
2020.04.06
2020.04.06
2020.04.06
N31-2100170-S88
X_H2X10SM-1.27PITCH
X_NN-CMKT3904
MICRO-STAR INT'L CO.,LTD
MS-7C91
AM4 Display / Audio
Date: Tuesday, April 21, 2020
Sheet 5 of 78

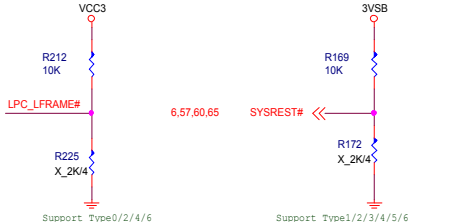

Closed FAN , by S0ix.
Add for HDT and close to PIN E16 & B16
Turn off power when BIOS into deep mode
Level 1.8V S5 Domain
2020.03.25
2020.04.16
2020.04.14
AM4 CPU TYPE Circuit
SVI
ACPI
GPIO
MISC
OC
FAN
RTC
SMBus
SENSE
AM4
PART 5 OF 9
N12-331A040-F02
ZIF-SOCKET1331
SPEC no Support
MICRO-STAR INT'L CO.,LTD
MS-7C91
AM4 SVI / ACPI / GPIO



Strapping Options

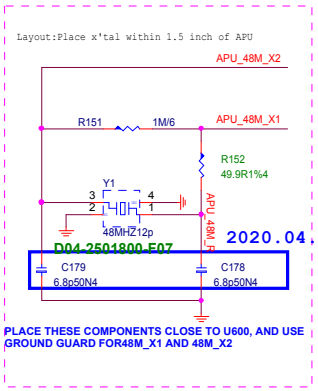


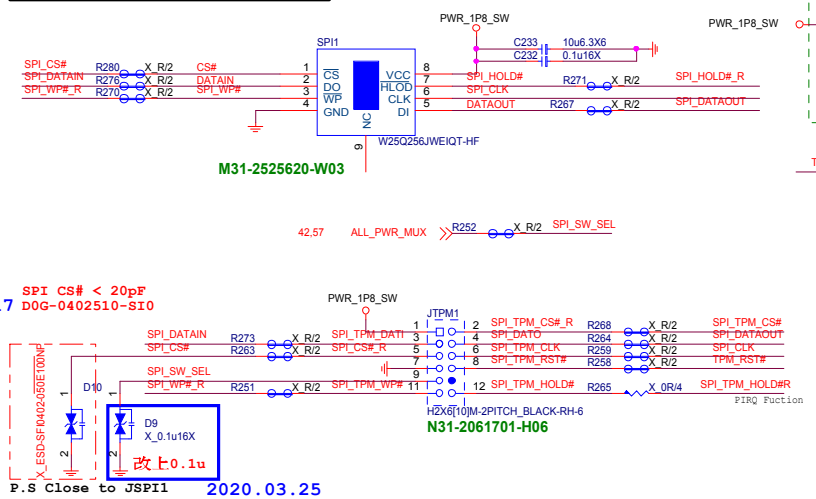
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image (Default)
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]

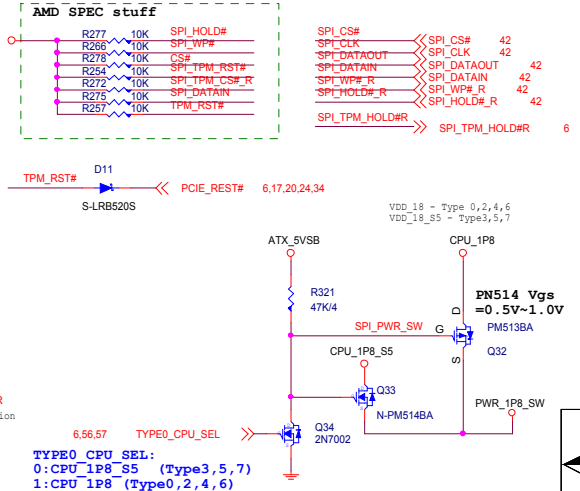


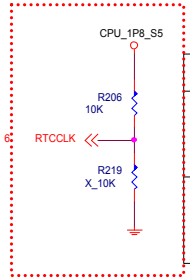
	AGPIO3	LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

SPI ROM(1.8V)









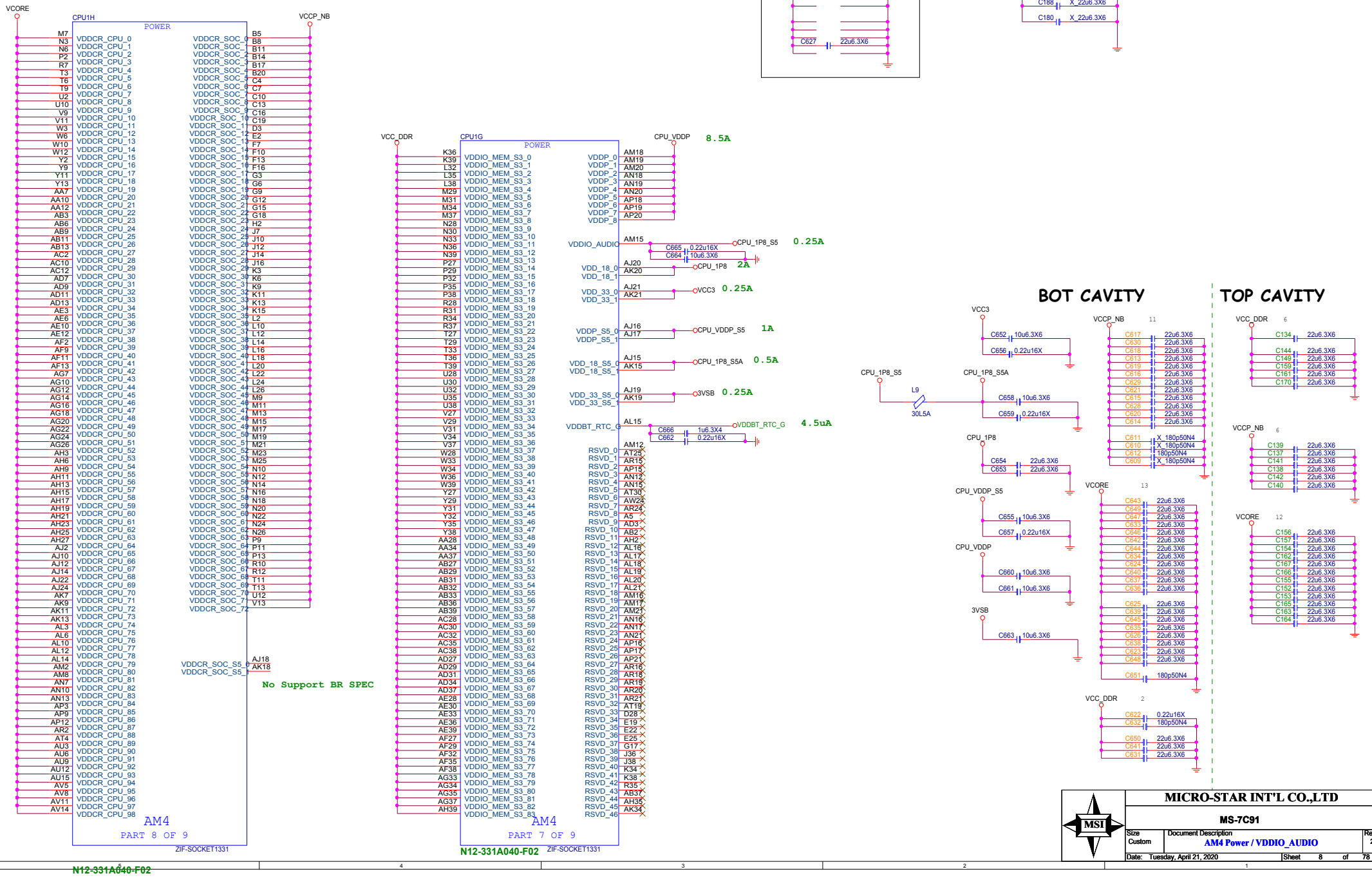
	RTCCLK
PULL HIGH	RTCCLK is input and is used as the bypass clock (Default)
PULL LOW	Normal Mode: Use 32Khz xtal as the source of RTC clock

MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	AM4 LPC / SPI / USB / CLK / STRAP	21

Date: Tuesday, April 21, 2020 Sheet 7 of 78


TOP SIDE
VCCP_NB
C627
22u6.3X6
VCORE
C93
X_22u6.3X6
C188
X_22u6.3X6
C180
X_22u6.3X6
VCORE
VCCP_NB
CPU1H
POWER
VDDCR_CPU_0
VDDCR_CPU_1
VDDCR_CPU_2
VDDCR_CPU_3
VDDCR_CPU_4
VDDCR_CPU_5
VDDCR_CPU_6
VDDCR_CPU_7
VDDCR_CPU_8
VDDCR_CPU_9
VDDCR_CPU_10
VDDCR_CPU_11
VDDCR_CPU_12
VDDCR_CPU_13
VDDCR_CPU_14
VDDCR_CPU_15
VDDCR_CPU_16
VDDCR_CPU_17
VDDCR_CPU_18
VDDCR_CPU_19
VDDCR_CPU_20
VDDCR_CPU_21
VDDCR_CPU_22
VDDCR_CPU_23
VDDCR_CPU_24
VDDCR_CPU_25
VDDCR_CPU_26
VDDCR_CPU_27
VDDCR_CPU_28
VDDCR_CPU_29
VDDCR_CPU_30
VDDCR_CPU_31
VDDCR_CPU_32
VDDCR_CPU_33
VDDCR_CPU_34
VDDCR_CPU_35
VDDCR_CPU_36
VDDCR_CPU_37
VDDCR_CPU_38
VDDCR_CPU_39
VDDCR_CPU_40
VDDCR_CPU_41
VDDCR_CPU_42
VDDCR_CPU_43
VDDCR_CPU_44
VDDCR_CPU_45
VDDCR_CPU_46
VDDCR_CPU_47
VDDCR_CPU_48
VDDCR_CPU_49
VDDCR_CPU_50
VDDCR_CPU_51
VDDCR_CPU_52
VDDCR_CPU_53
VDDCR_CPU_54
VDDCR_CPU_55
VDDCR_CPU_56
VDDCR_CPU_57
VDDCR_CPU_58
VDDCR_CPU_59
VDDCR_CPU_60
VDDCR_CPU_61
VDDCR_CPU_62
VDDCR_CPU_63
VDDCR_CPU_64
VDDCR_CPU_65
VDDCR_CPU_66
VDDCR_CPU_67
VDDCR_CPU_68
VDDCR_CPU_69
VDDCR_CPU_70
VDDCR_CPU_71
VDDCR_CPU_72
VDDCR_CPU_73
VDDCR_CPU_74
VDDCR_CPU_75
VDDCR_CPU_76
VDDCR_CPU_77
VDDCR_CPU_78
VDDCR_CPU_79
VDDCR_CPU_80
VDDCR_CPU_81
VDDCR_CPU_82
VDDCR_CPU_83
VDDCR_CPU_84
VDDCR_CPU_85
VDDCR_CPU_86
VDDCR_CPU_87
VDDCR_CPU_88
VDDCR_CPU_89
VDDCR_CPU_90
VDDCR_CPU_91
VDDCR_CPU_92
VDDCR_CPU_93
VDDCR_CPU_94
VDDCR_CPU_95
VDDCR_CPU_96
VDDCR_CPU_97
VDDCR_CPU_98
VDDCR_SOC_0
VDDCR_SOC_1
VDDCR_SOC_2
VDDCR_SOC_3
VDDCR_SOC_4
VDDCR_SOC_5
VDDCR_SOC_6
VDDCR_SOC_7
VDDCR_SOC_8
VDDCR_SOC_9
VDDCR_SOC_10
VDDCR_SOC_11
VDDCR_SOC_12
VDDCR_SOC_13
VDDCR_SOC_14
VDDCR_SOC_15
VDDCR_SOC_16
VDDCR_SOC_17
VDDCR_SOC_18
VDDCR_SOC_19
VDDCR_SOC_20
VDDCR_SOC_21
VDDCR_SOC_22
VDDCR_SOC_23
VDDCR_SOC_24
VDDCR_SOC_25
VDDCR_SOC_26
VDDCR_SOC_27
VDDCR_SOC_28
VDDCR_SOC_29
VDDCR_SOC_30
VDDCR_SOC_31
VDDCR_SOC_32
VDDCR_SOC_33
VDDCR_SOC_34
VDDCR_SOC_35
VDDCR_SOC_36
VDDCR_SOC_37
VDDCR_SOC_38
VDDCR_SOC_39
VDDCR_SOC_40
VDDCR_SOC_41
VDDCR_SOC_42
VDDCR_SOC_43
VDDCR_SOC_44
VDDCR_SOC_45
VDDCR_SOC_46
VDDCR_SOC_47
VDDCR_SOC_48
VDDCR_SOC_49
VDDCR_SOC_50
VDDCR_SOC_51
VDDCR_SOC_52
VDDCR_SOC_53
VDDCR_SOC_54
VDDCR_SOC_55
VDDCR_SOC_56
VDDCR_SOC_57
VDDCR_SOC_58
VDDCR_SOC_59
VDDCR_SOC_60
VDDCR_SOC_61
VDDCR_SOC_62
VDDCR_SOC_63
VDDCR_SOC_64
VDDCR_SOC_65
VDDCR_SOC_66
VDDCR_SOC_67
VDDCR_SOC_68
VDDCR_SOC_69
VDDCR_SOC_70
VDDCR_SOC_71
VDDCR_SOC_72
VDDCR_SOC_S5_0
VDDCR_SOC_S5_1
No Support BR SPEC
AM4
PART 8 OF 9
ZIF-SOCKET1331
N12-331A040-F02
VCC_DDR
CPU1G
POWER
VDDIO_MEM_S3_0
VDDIO_MEM_S3_1
VDDIO_MEM_S3_2
VDDIO_MEM_S3_3
VDDIO_MEM_S3_4
VDDIO_MEM_S3_5
VDDIO_MEM_S3_6
VDDIO_MEM_S3_7
VDDIO_MEM_S3_8
VDDIO_MEM_S3_9
VDDIO_MEM_S3_10
VDDIO_MEM_S3_11
VDDIO_MEM_S3_12
VDDIO_MEM_S3_13
VDDIO_MEM_S3_14
VDDIO_MEM_S3_15
VDDIO_MEM_S3_16
VDDIO_MEM_S3_17
VDDIO_MEM_S3_18
VDDIO_MEM_S3_19
VDDIO_MEM_S3_20
VDDIO_MEM_S3_21
VDDIO_MEM_S3_22
VDDIO_MEM_S3_23
VDDIO_MEM_S3_24
VDDIO_MEM_S3_25
VDDIO_MEM_S3_26
VDDIO_MEM_S3_27
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VDDIO_MEM_S3_29
VDDIO_MEM_S3_30
VDDIO_MEM_S3_31
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VDDIO_MEM_S3_34
VDDIO_MEM_S3_35
VDDIO_MEM_S3_36
VDDIO_MEM_S3_37
VDDIO_MEM_S3_38
VDDIO_MEM_S3_39
VDDIO_MEM_S3_40
VDDIO_MEM_S3_41
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VDDIO_MEM_S3_43
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VDDIO_MEM_S3_47
VDDIO_MEM_S3_48
VDDIO_MEM_S3_49
VDDIO_MEM_S3_50
VDDIO_MEM_S3_51
VDDIO_MEM_S3_52
VDDIO_MEM_S3_53
VDDIO_MEM_S3_54
VDDIO_MEM_S3_55
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VDDIO_MEM_S3_58
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VDDIO_MEM_S3_64
VDDIO_MEM_S3_65
VDDIO_MEM_S3_66
VDDIO_MEM_S3_67
VDDIO_MEM_S3_68
VDDIO_MEM_S3_69
VDDIO_MEM_S3_70
VDDIO_MEM_S3_71
VDDIO_MEM_S3_72
VDDIO_MEM_S3_73
VDDIO_MEM_S3_74
VDDIO_MEM_S3_75
VDDIO_MEM_S3_76
VDDIO_MEM_S3_77
VDDIO_MEM_S3_78
VDDIO_MEM_S3_79
VDDIO_MEM_S3_80
VDDIO_MEM_S3_81
VDDIO_MEM_S3_82
VDDIO_MEM_S3_83
CPU_VDDP
8.5A
VDDP_0
VDDP_1
VDDP_2
VDDP_3
VDDP_4
VDDP_5
VDDP_6
VDDP_7
VDDP_8
VDDIO_AUDIO
CPU_1P8_S5
0.25A
C665
0.22u16X
C664
10u6.3X6
VDD_18_0
VDD_18_1
CPU_1P8
2A
VDD_33_0
VDD_33_1
VCC3
0.25A
VDDP_S5_0
VDDP_S5_1
CPU_VDDP_S5
1A
VDD_18_S5_0
VDD_18_S5_1
CPU_1P8_S5A
0.5A
VDD_33_S5_0
VDD_33_S5_1
3VSB
0.25A
VDDBT_RTC_G
4.5uA
C666
1u6.3X4
C662
0.22u16X
VDDBT_RTC_G
RSVD_0
RSVD_1
RSVD_2
RSVD_3
RSVD_4
RSVD_5
RSVD_6
RSVD_7
RSVD_8
RSVD_9
RSVD_10
RSVD_11
RSVD_12
RSVD_13
RSVD_14
RSVD_15
RSVD_16
RSVD_17
RSVD_18
RSVD_19
RSVD_20
RSVD_21
RSVD_22
RSVD_23
RSVD_24
RSVD_25
RSVD_26
RSVD_27
RSVD_28
RSVD_29
RSVD_30
RSVD_31
RSVD_32
RSVD_33
RSVD_34
RSVD_35
RSVD_36
RSVD_37
RSVD_38
RSVD_39
RSVD_40
RSVD_41
RSVD_42
RSVD_43
RSVD_44
RSVD_45
RSVD_46
AM4
PART 7 OF 9
ZIF-SOCKET1331
N12-331A040-F02
BOT CAVITY
TOP CAVITY
VCC3
C652
10u6.3X6
C656
0.22u16X
CPU_1P8_S5
L9
30L5A
CPU_1P8_S5A
C658
10u6.3X6
C659
0.22u16X
CPU_1P8
C654
22u6.3X6
C653
22u6.3X6
CPU_VDDP_S5
C655
10u6.3X6
C657
0.22u16X
CPU_VDDP
C660
10u6.3X6
C661
10u6.3X6
3VSB
C663
10u6.3X6
VCCP_NB
11
C617
22u6.3X6
C630
22u6.3X6
C618
22u6.3X6
C613
22u6.3X6
C619
22u6.3X6
C616
22u6.3X6
C629
22u6.3X6
C621
22u6.3X6
C615
22u6.3X6
C628
22u6.3X6
C620
22u6.3X6
C614
22u6.3X6
C611
X_180p50N4
C610
X_180p50N4
C612
180p50N4
C609
X_180p50N4
VCORE
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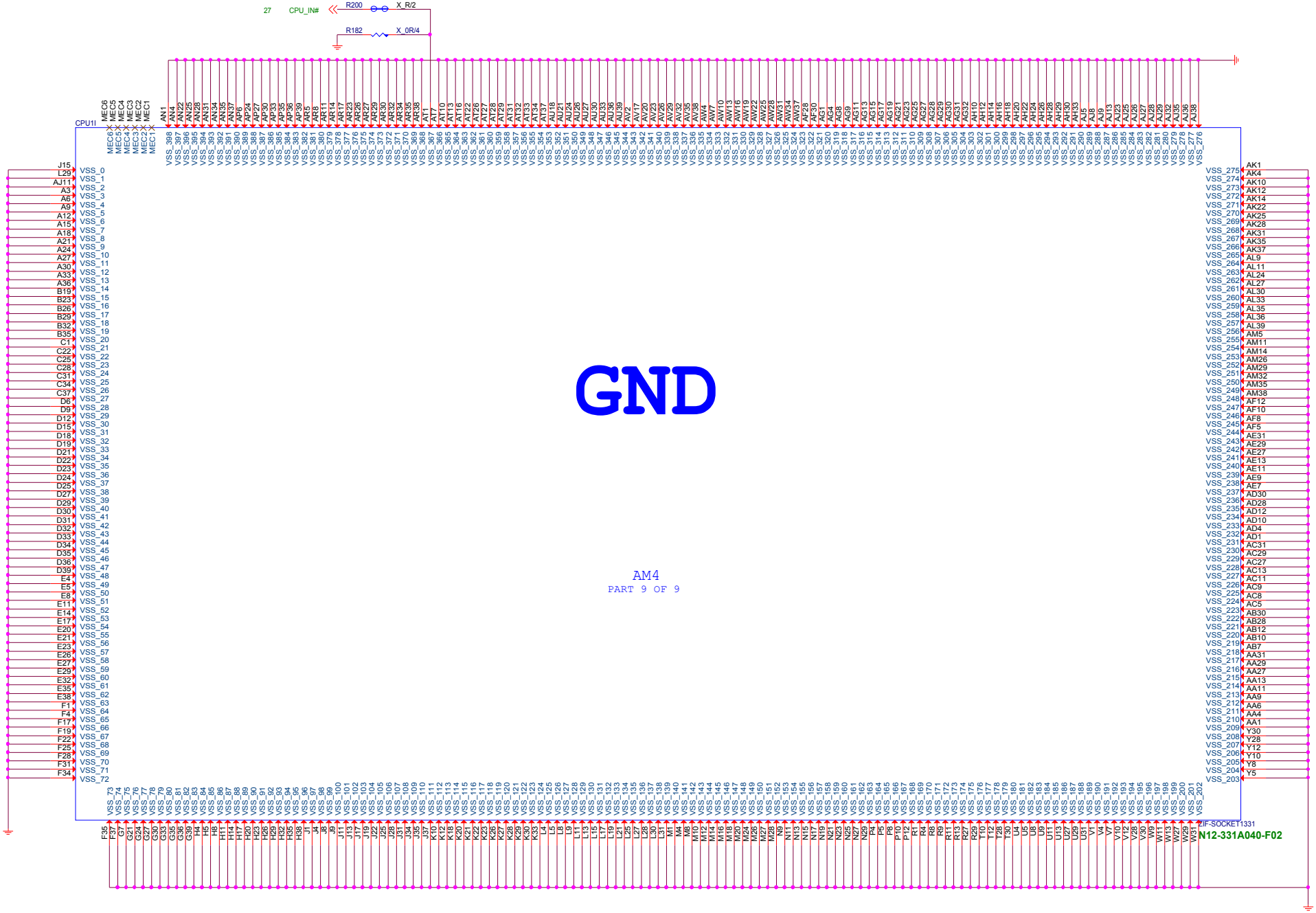
C643
22u6.3X6
C649
22u6.3X6
C647
22u6.3X6
C633
22u6.3X6
C646
22u6.3X6
C642
22u6.3X6
C644
22u6.3X6
C634
22u6.3X6
C624
22u6.3X6
C640
22u6.3X6
C637
22u6.3X6
C636
22u6.3X6
C625
22u6.3X6
C639
22u6.3X6
C645
22u6.3X6
C635
22u6.3X6
C626
22u6.3X6
C638
22u6.3X6
C623
22u6.3X6
C648
22u6.3X6
C651
180p50N4
VCC_DDR
2
C622
0.22u16X
C632
180p50N4
C650
22u6.3X6
C641
22u6.3X6
C631
22u6.3X6
VCC_DDR
6
C134
22u6.3X6
C144
22u6.3X6
C149
22u6.3X6
C159
22u6.3X6
C161
22u6.3X6
C170
22u6.3X6
VCCP_NB
6
C139
22u6.3X6
C137
22u6.3X6
C141
22u6.3X6
C138
22u6.3X6
C142
22u6.3X6
C140
22u6.3X6
VCORE
12
C156
22u6.3X6
C157
22u6.3X6
C154
22u6.3X6
C162
22u6.3X6
C167
22u6.3X6
C166
22u6.3X6
C155
22u6.3X6
C152
22u6.3X6
C153
22u6.3X6
C165
22u6.3X6
C163
22u6.3X6
C164
22u6.3X6
MICRO-STAR INT'L CO.,LTD
MS-7C91
Size
Custom
Document Description
AM4 Power / VDDIO_AUDIO
Rev
21
Date: Tuesday, April 21, 2020
Sheet 8 of 78



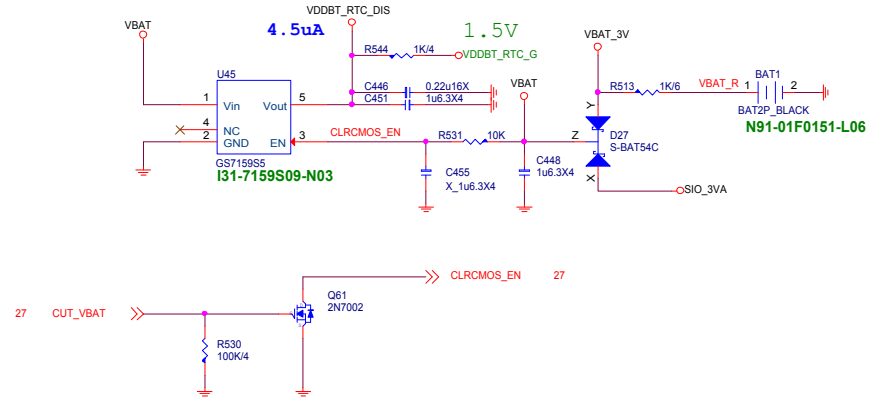
MICRO-STAR INT'L CO.,LTD

MS-7C91

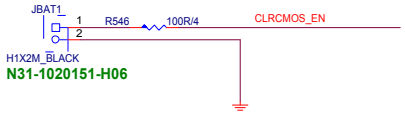
Size	Document Description	Rev
Custom	AM4 GND	21

Date: Tuesday, April 21, 2020 | Sheet 9 of 78

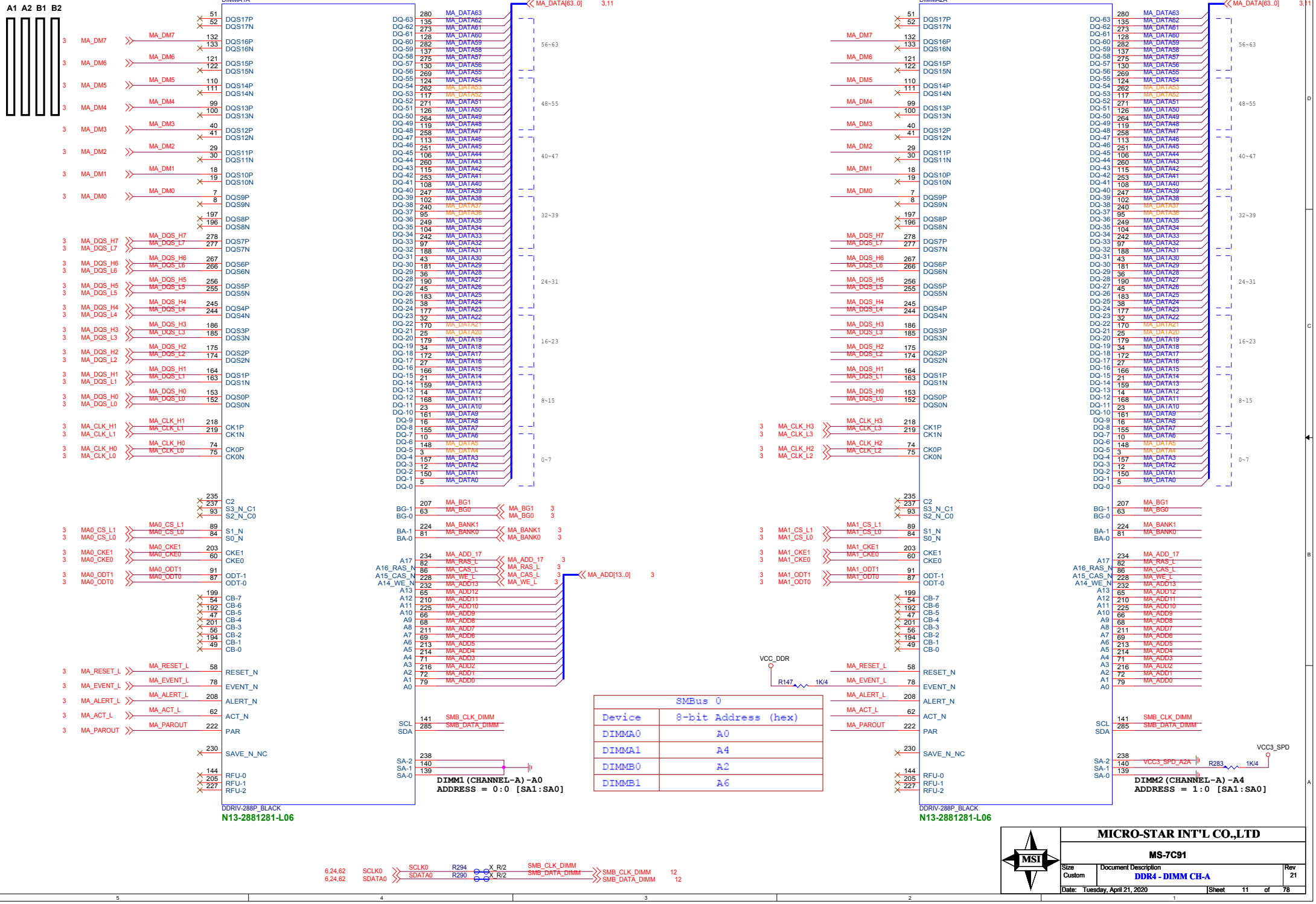
RTC & Clear CMOS Circuit

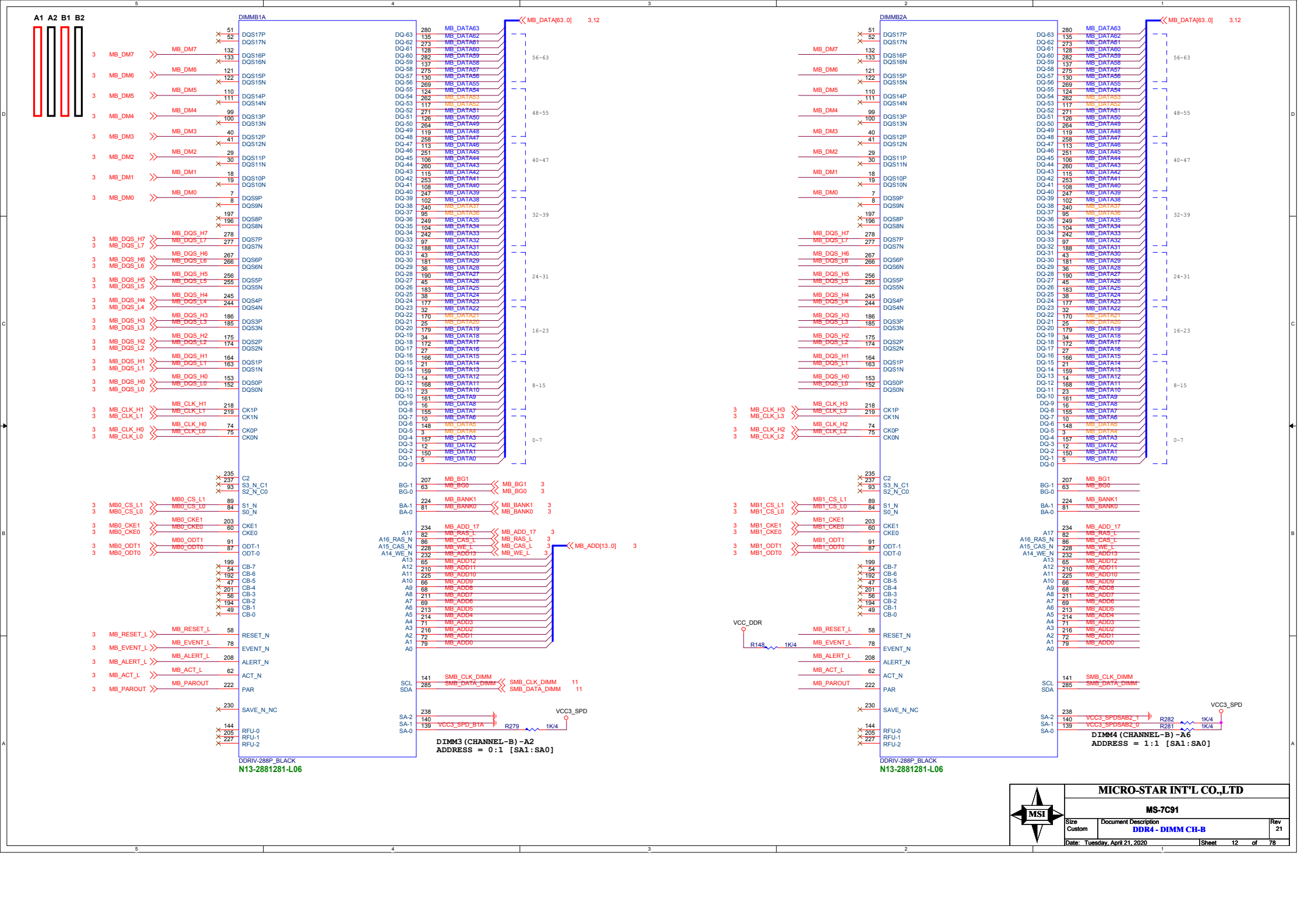


Clear CMOS button



MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: RTC / CMOS	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 10 of 78	


A1 A2 B1 B2
DIMMA1A
DIMMA2A
MA_DATA[63..0]
MA_ADD[13..0]
SMBus 0
Device | 8-bit Address (hex)
DIMMA0 | A0
DIMMA1 | A4
DIMMB0 | A2
DIMMB1 | A6
DIMM1 (CHANNEL-A) -A0
ADDRESS = 0:0 [SA1:SA0]
DIMM2 (CHANNEL-A) -A4
ADDRESS = 1:0 [SA1:SA0]
VCC_DDR
VCC3_SPD
DDRIV-288P_BLACK
N13-2881281-L06
MICRO-STAR INT'L CO.,LTD
MS-7C91
Size Custom
Document Description DDR4 - DIMM CH-A
Rev 21
Date: Tuesday, April 21, 2020
Sheet 11 of 78

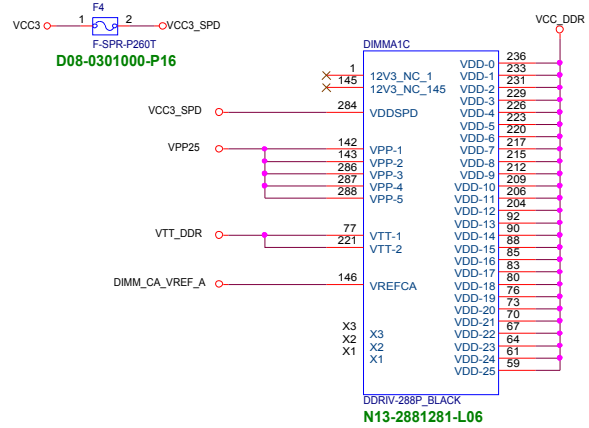

A1 A2 B1 B2
DIMMB1A
DIMMB2A
MB_DATA[63..0] 3,12
MB_ADD[13..0] 3
DDRIV-288P_BLACK
N13-2881281-L06
DIMM3(CHANNEL-B)-A2
ADDRESS = 0:1 [SA1:SA0]
DIMM4(CHANNEL-B)-A6
ADDRESS = 1:1 [SA1:SA0]
VCC_DDR
R148 1K/4
VCC3_SPD
R279 1K/4
R282 1K/4
R281 1K/4
MICRO-STAR INT'L CO.,LTD
MS-7C91
Size Custom
Document Description DDR4 - DIMM CH-B
Rev 21
Date: Tuesday, April 21, 2020
Sheet 12 of 78

avl:D08-0301100-B07

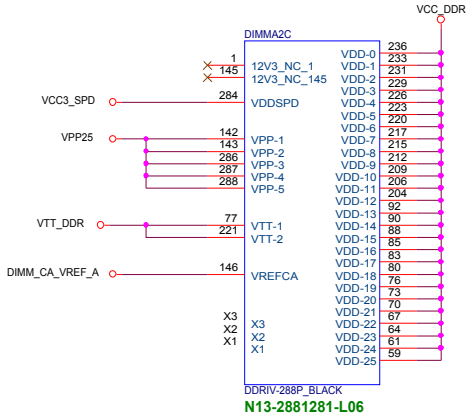
F4
VCC3 1 2 VCC3_SPD
F-SPR-P260T

D08-0301000-P16

DIMM SLOT PN BY SPEC



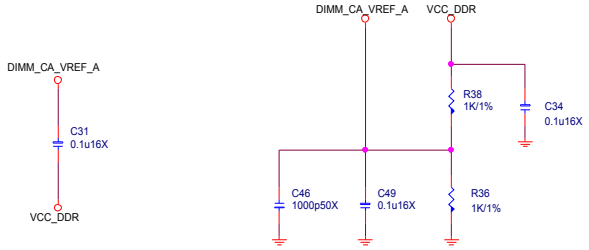
N13-2881281-L06

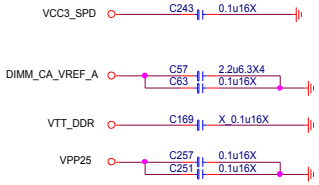


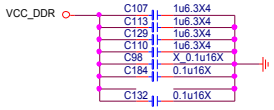
N13-2881281-L06

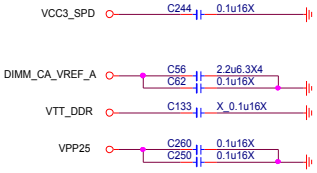
DDR VREF

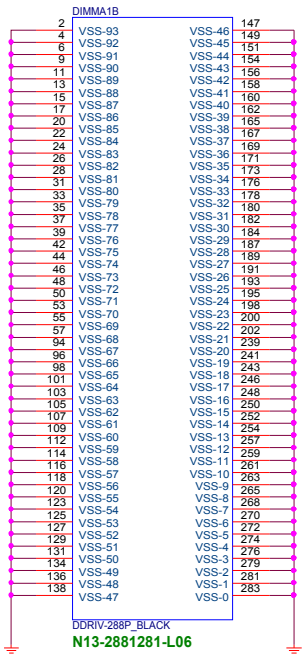
(place resistors close to DIMMs)











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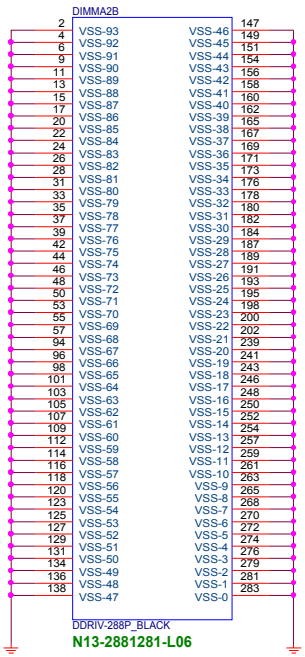


N13-2881281-L06

MICRO-STAR INT'L CO.,LTD

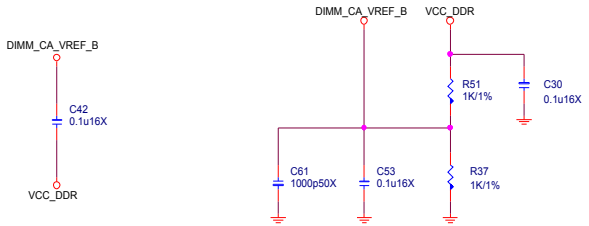
MS-7C91

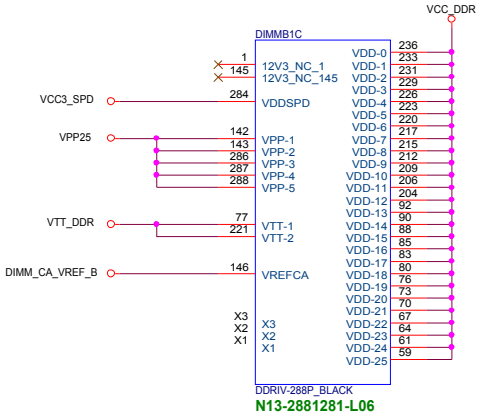
Size	Document Description	Rev
Custom	DDR4 - POWER/GND-1	21

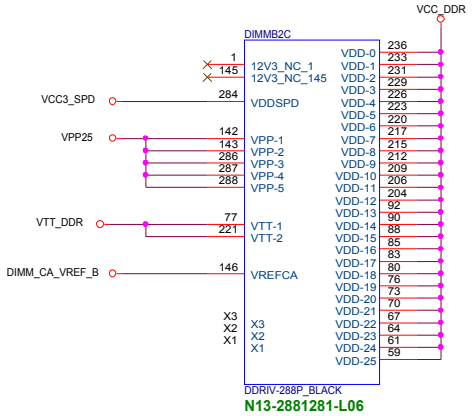
Date: Tuesday, April 21, 2020 Sheet 13 of 78

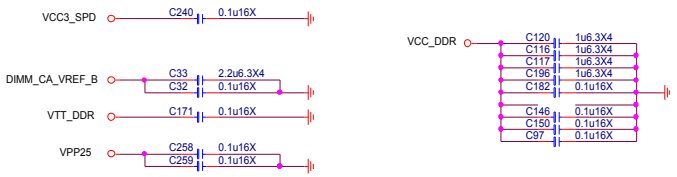
DDR VREF

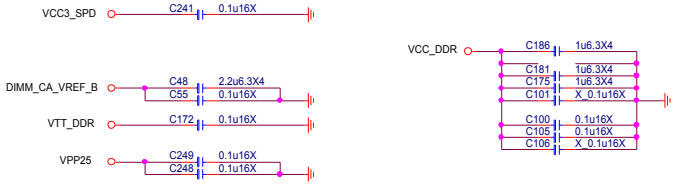
(place resistors close to DIMMs)

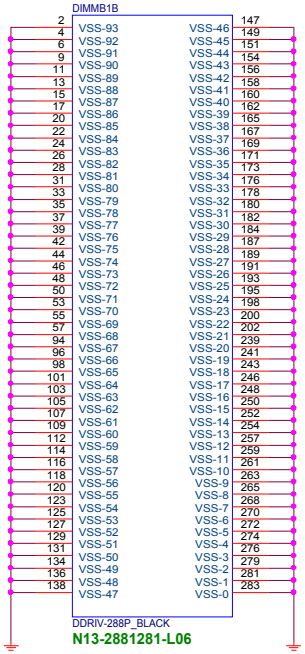


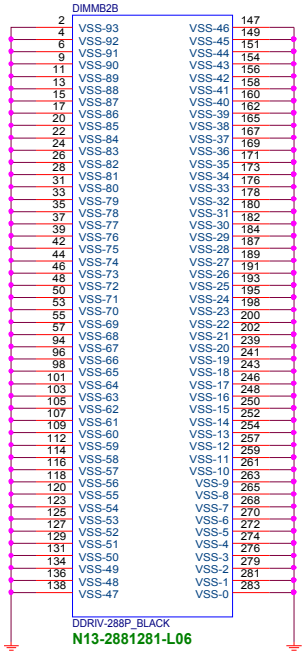










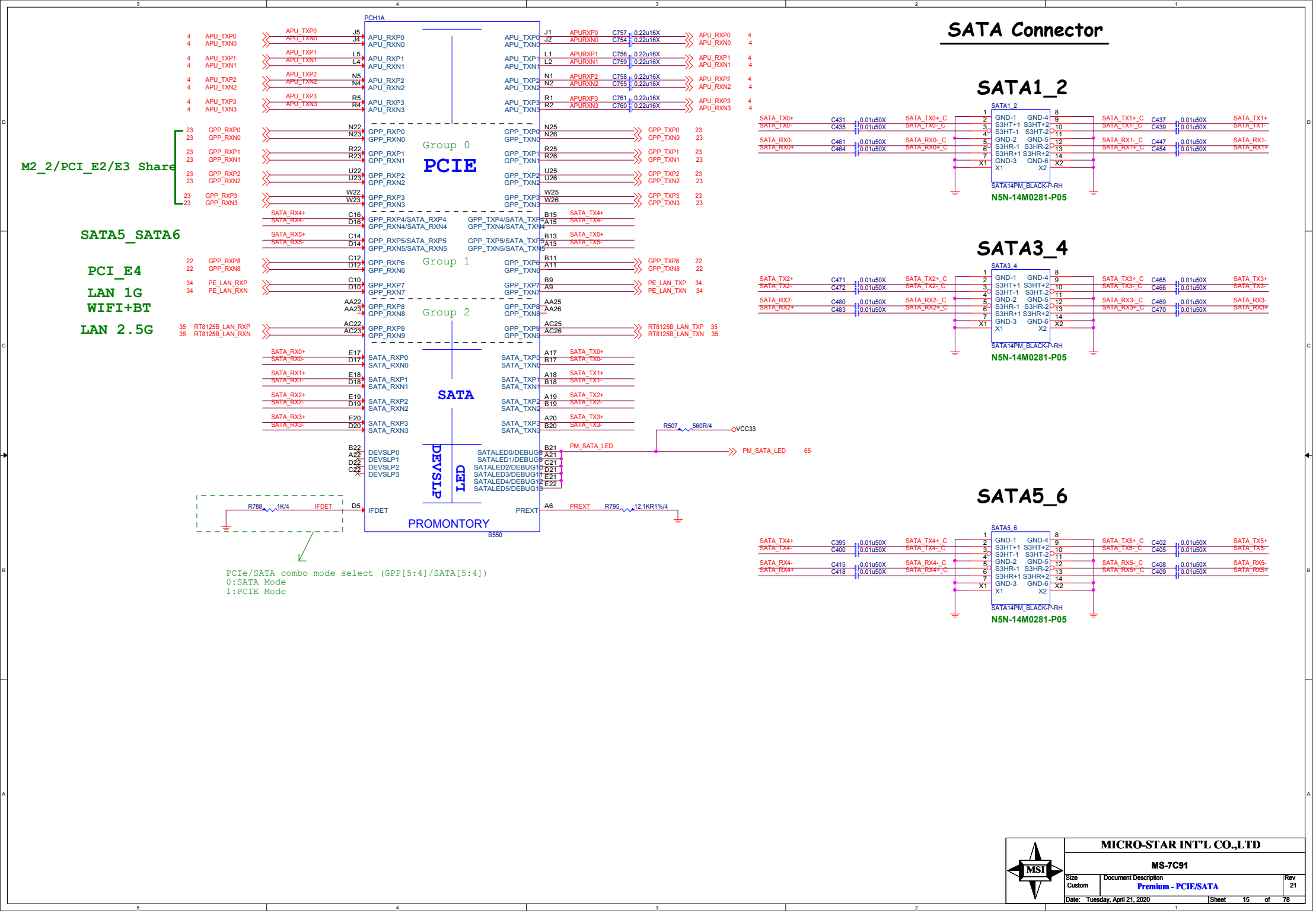


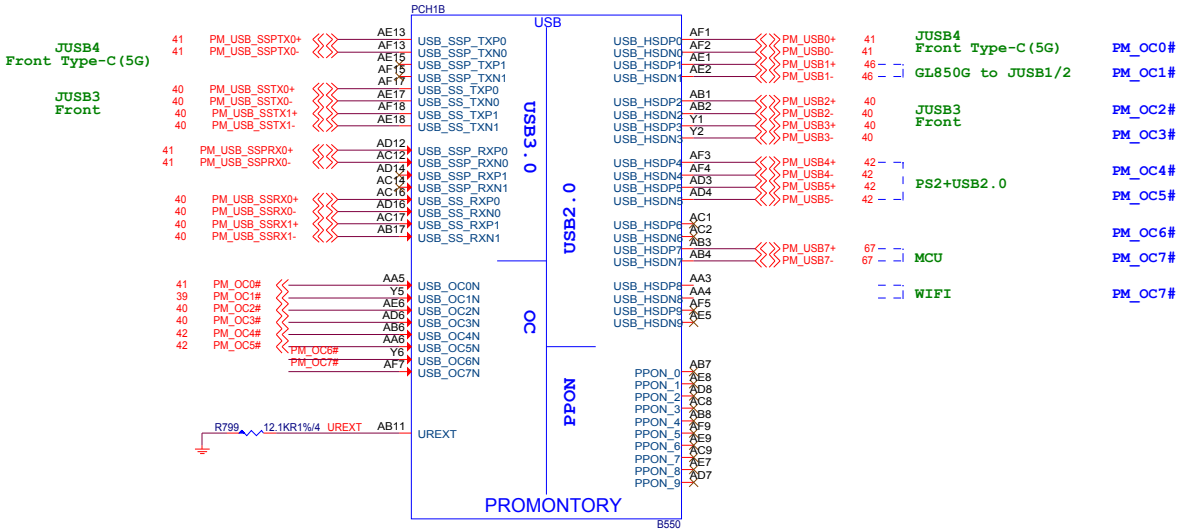
MICRO-STAR INT'L CO.,LTD

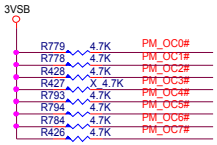
MS-7C91

Size	Document Description	Rev
Custom	DDR4 - POWER/GND-2	21

Date: Tuesday, April 21, 2020 Sheet 14 of 78


SATA Connector
SATA1_2
SATA3_4
SATA5_6
N5N-14M0281-P05
PCH1A
PROMONTORY
B550
PCIE
SATA
DEVSLP
LED
Group 0
Group 1
Group 2
M2_2/PCI_E2/E3 Share
SATA5_SATA6
PCI_E4
LAN 1G
WIFI+BT
LAN 2.5G
PCIe/SATA combo mode select (GPP[5:4]/SATA[5:4])
0:SATA Mode
1:PCIE Mode
MICRO-STAR INT'L CO.,LTD
MS-7C91
Premium - PCIE/SATA
Date: Tuesday, April 21, 2020
Sheet 15 of 78



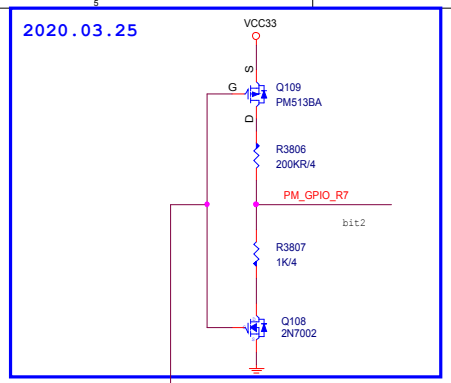


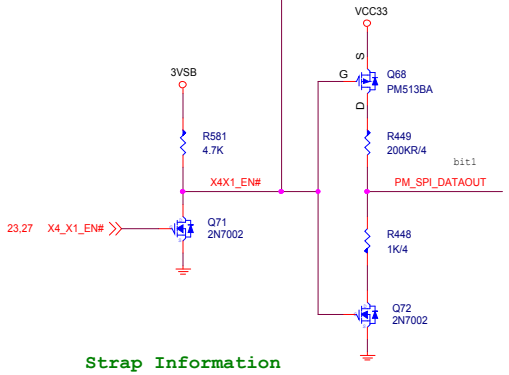
USB mapping

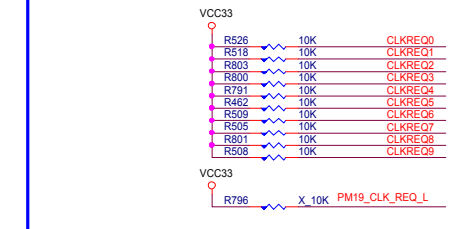
```
USB_SSP_TX/RX[0] + USB_HSDP/N[0] + USB_OC0N
USB_SSP_TX/RX[1] + USB_HSDP/N[1] + USB_OC1N

USB_SS_TX/RX[0] + USB_HSDP/N[2] + USB_OC2N
USB_SS_TX/RX[1] + USB_HSDP/N[3] + USB_OC3N
                  USB_HSDP/N[4] + USB_OC4N
                  USB_HSDP/N[5] + USB_OC5N
                  USB_HSDP/N[6] + USB_OC6N
                  USB_HSDP/N[7] + USB_OC7N
                  USB_HSDP/N[8] + USB_OC7N
                  USB_HSDP/N[9] + USB_OC7N
```

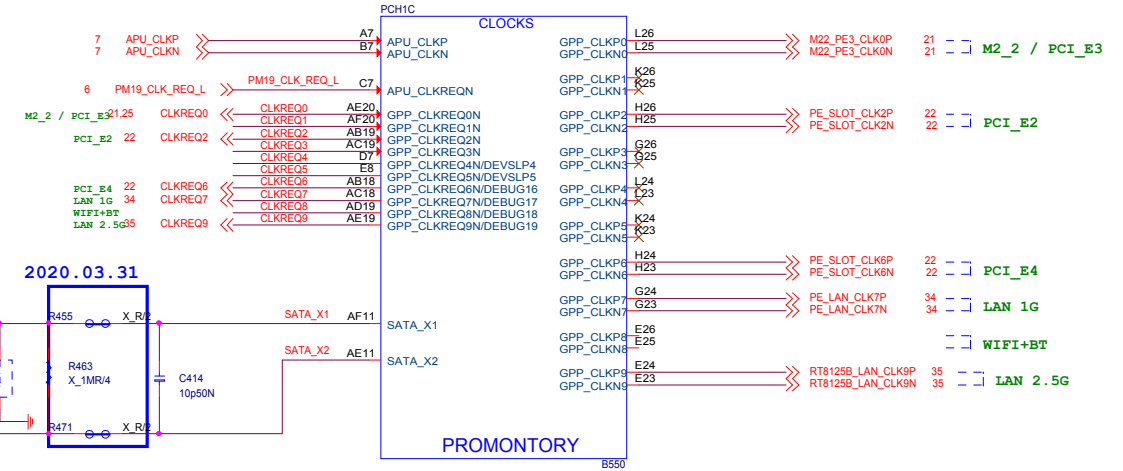
MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: Premium - USB/OC	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 16 of 78	

2020.03.25

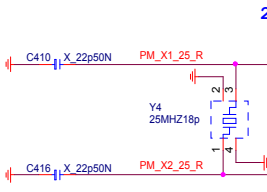




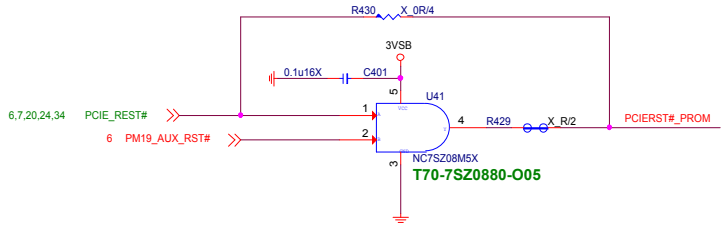


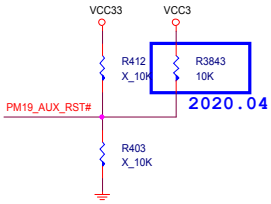


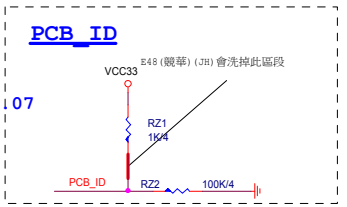
2020.03.31



GPP Group 0 (Lanes 3:0)
111: 1 PCIe x4
011: 1 PCIe x2 + 1 PCIe x2
010: 1 PCIe x2 + 2 PCIe x1
001: 2 PCIe x1 + 1 PCIe x2
000: 4 PCIe x1
Others: Reserved

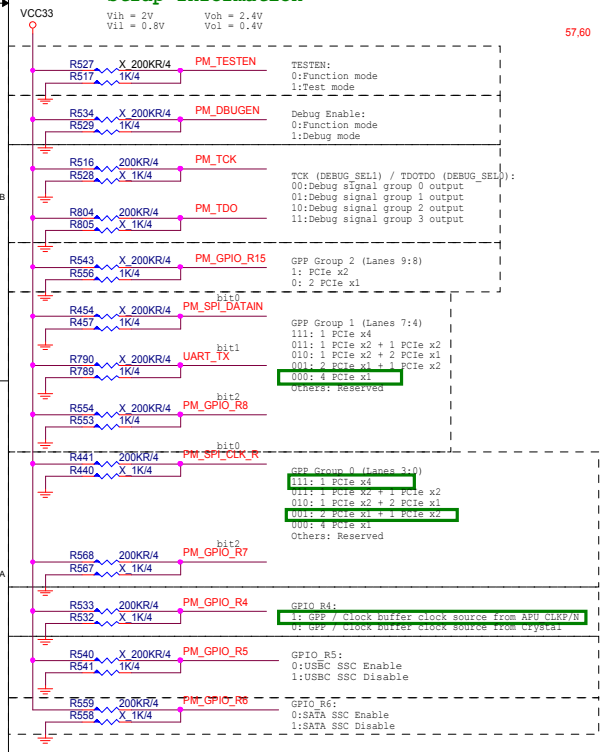


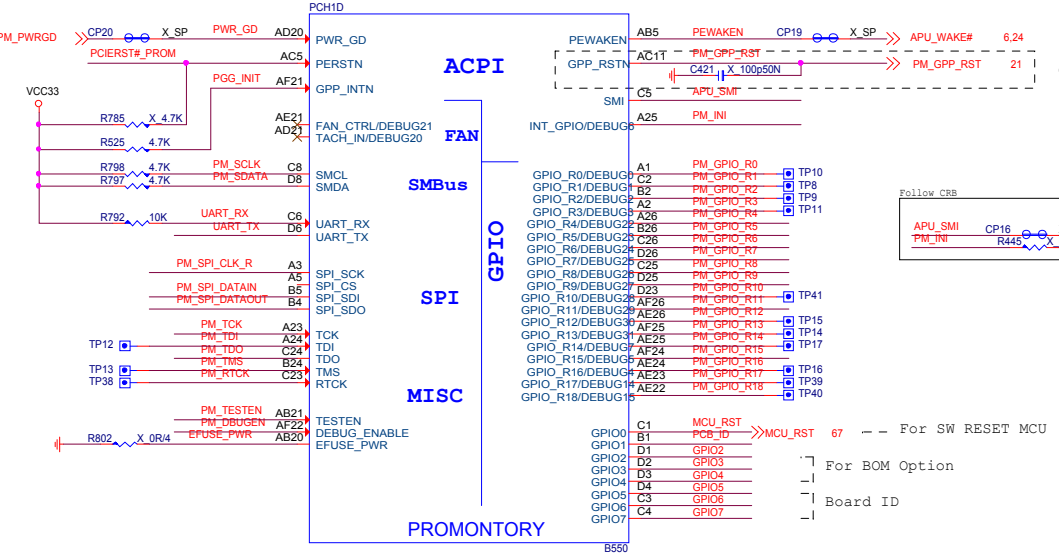




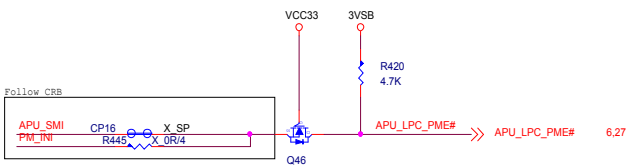
Strap Information

Vih = 2V Voh = 2.4V
Vil = 0.8V Vol = 0.4V





Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.

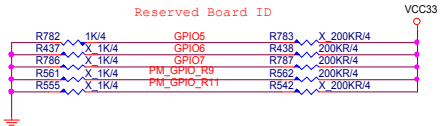


GPIO_R[13:4]
Internal have a PU 200Kohm

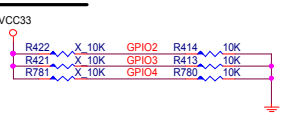
UART_TX/SPI_SDI/SPI_SDO/SPI_SCK/TCK/TDO
Internal have a PU 200Kohm

PM_DBUGEN
Internal have a PD 1Kohm

Reserved Board ID



BOM OPTION



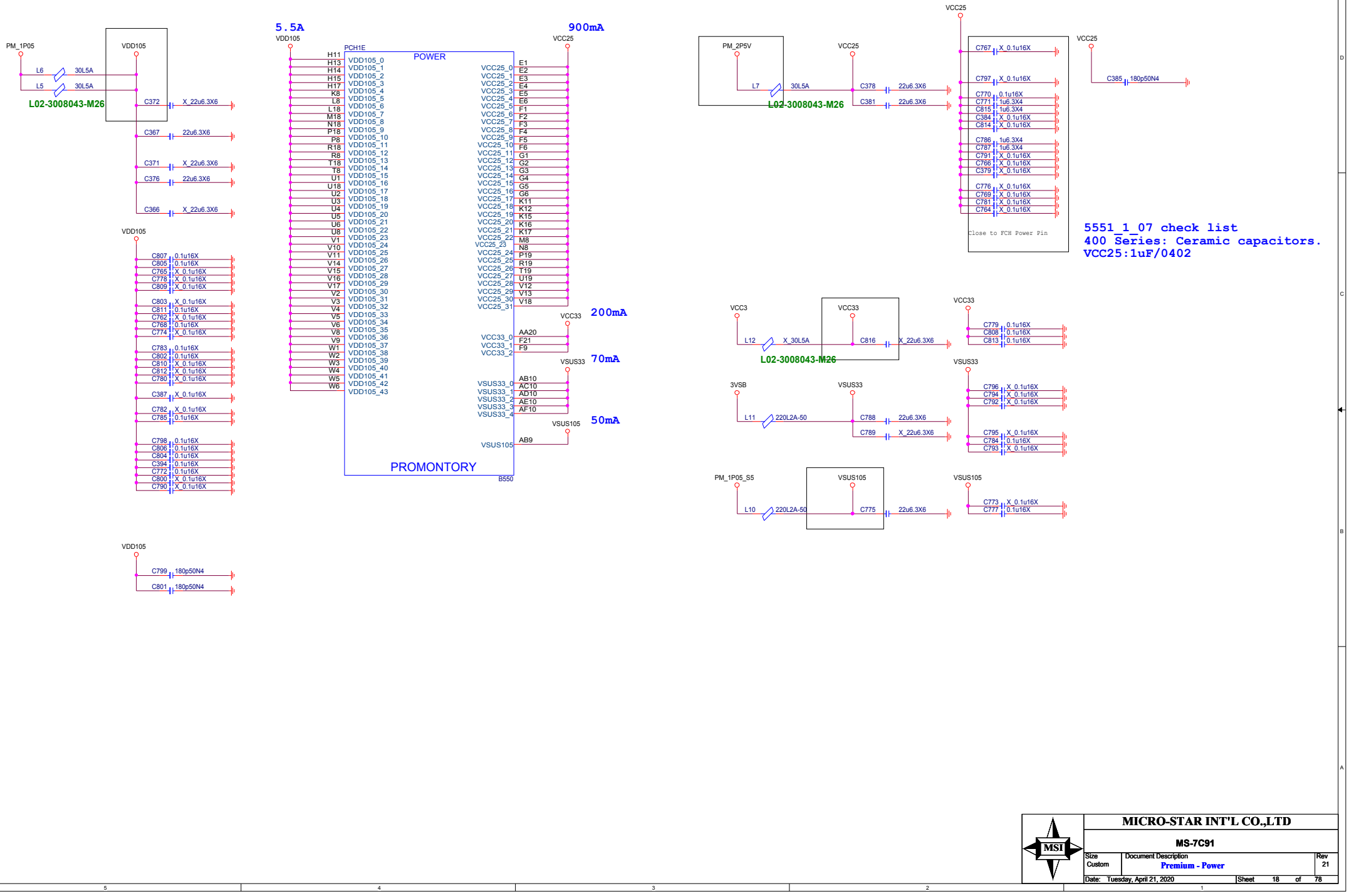
	XXX	XXX	
GPIO2	0	0	
GPIO3	0	0	
GPIO4	0	0	

MICRO-STAR INT'L CO.,LTD

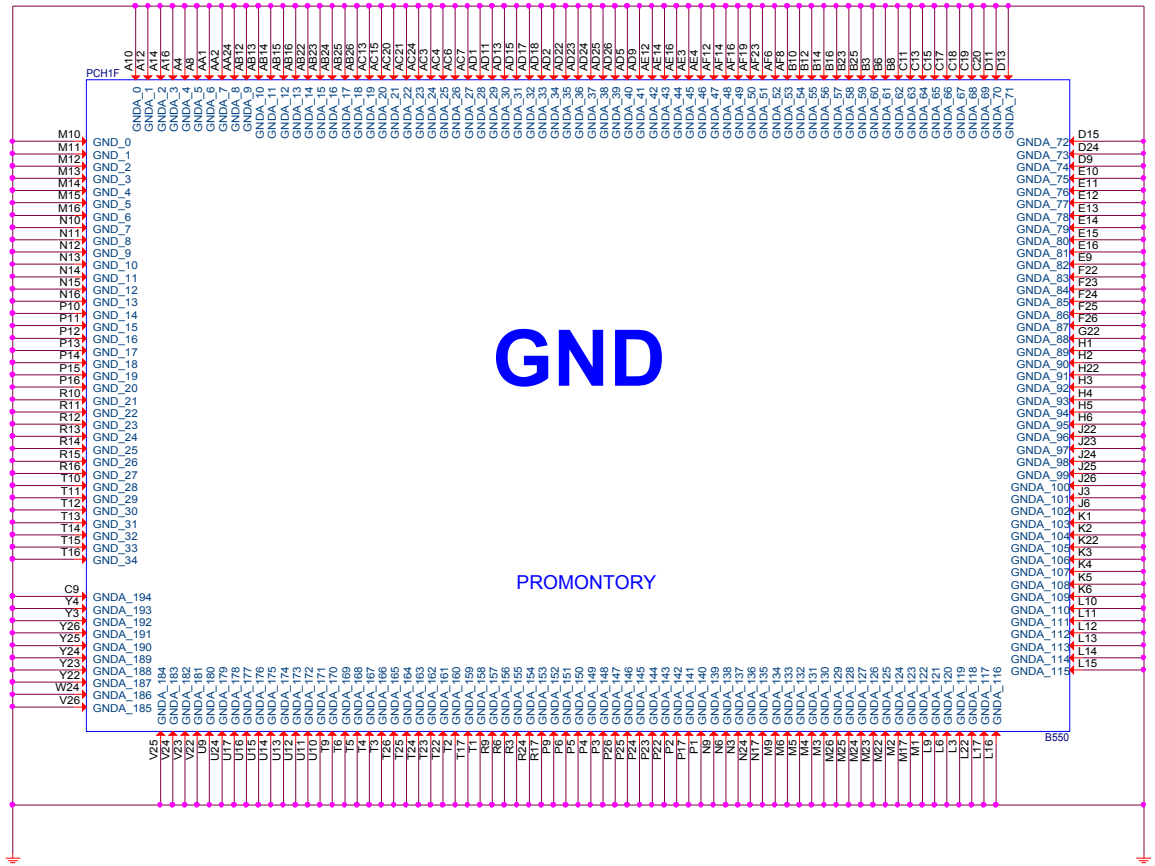
MS-7C91

Size	Document Description	Rev
Custom	Premium - CLK/ACPI/GPIO	21

Date: Tuesday, April 21, 2020 Sheet 17 of 78

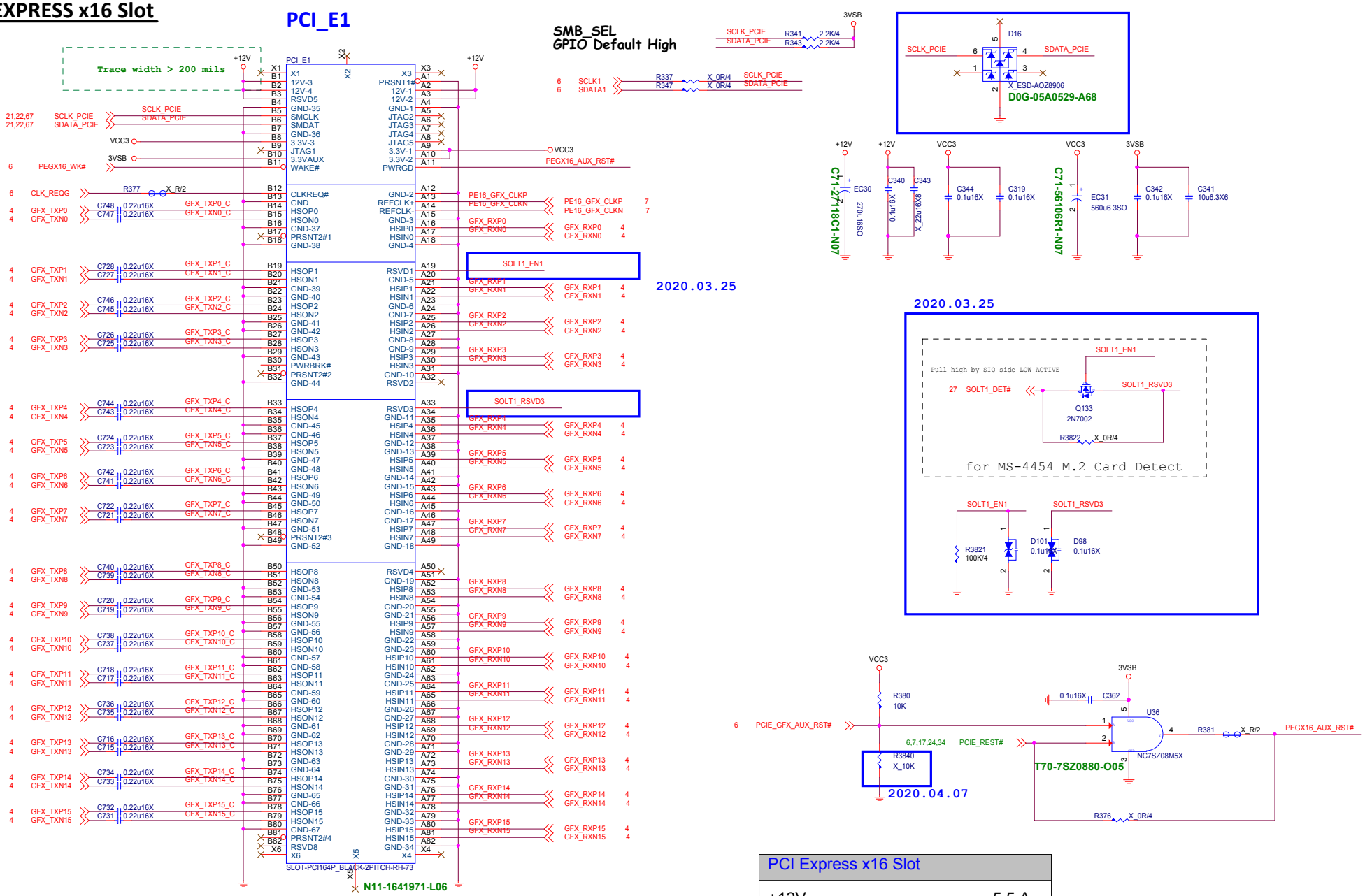


MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: Premium - Power	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 18 of 78	



MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: Premium - GND
Rev: 21	
Date: Tuesday, April 21, 2020	Sheet 19 of 78

PCI EXPRESS x16 Slot



PCI Express x16 Slot		
+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

MICRO-STAR INT'L CO.,LTD

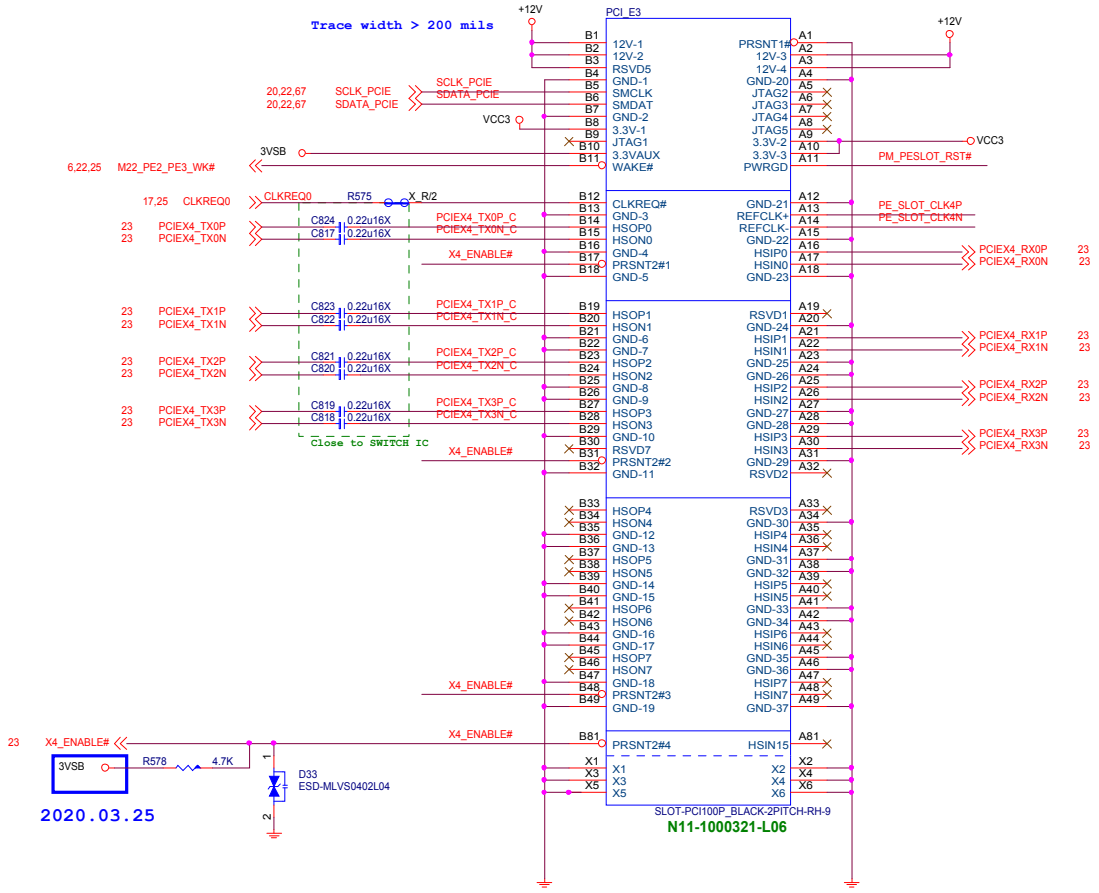
MS-7C91

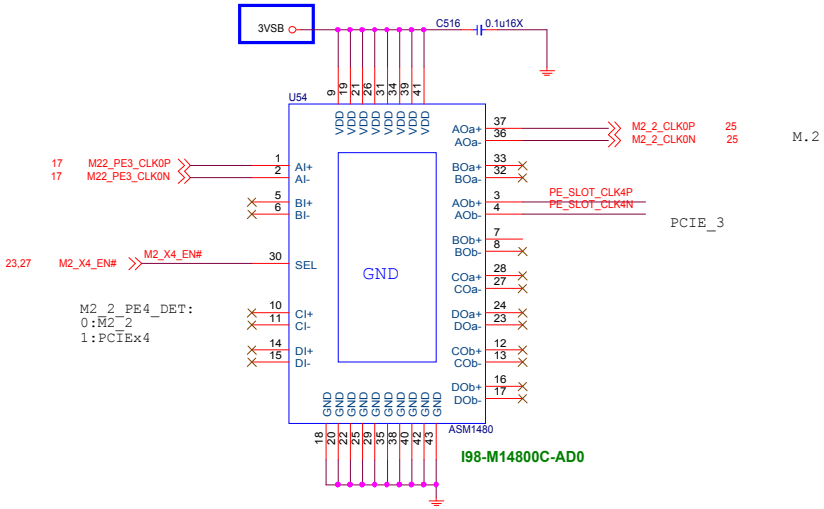
Size	Document Description	Rev
Custom	PCI_E2 (X16)	21

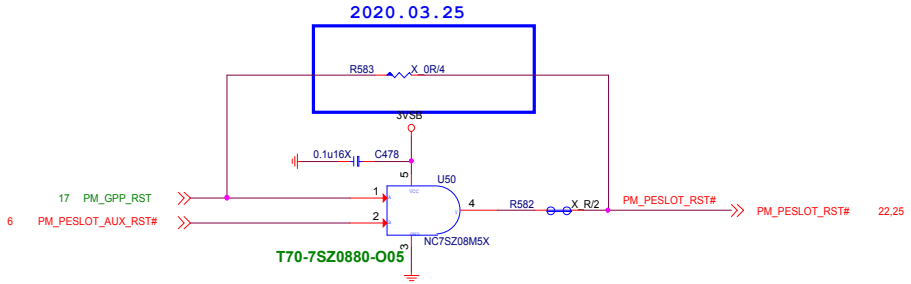
Date: Tuesday, April 21, 2020 Sheet 20 of 78

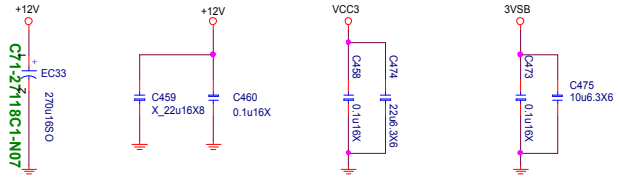
PCI EXPRESS x4 SLOT

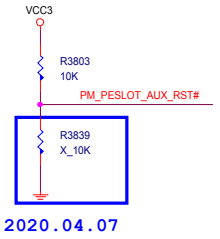
PCI_E3 X4







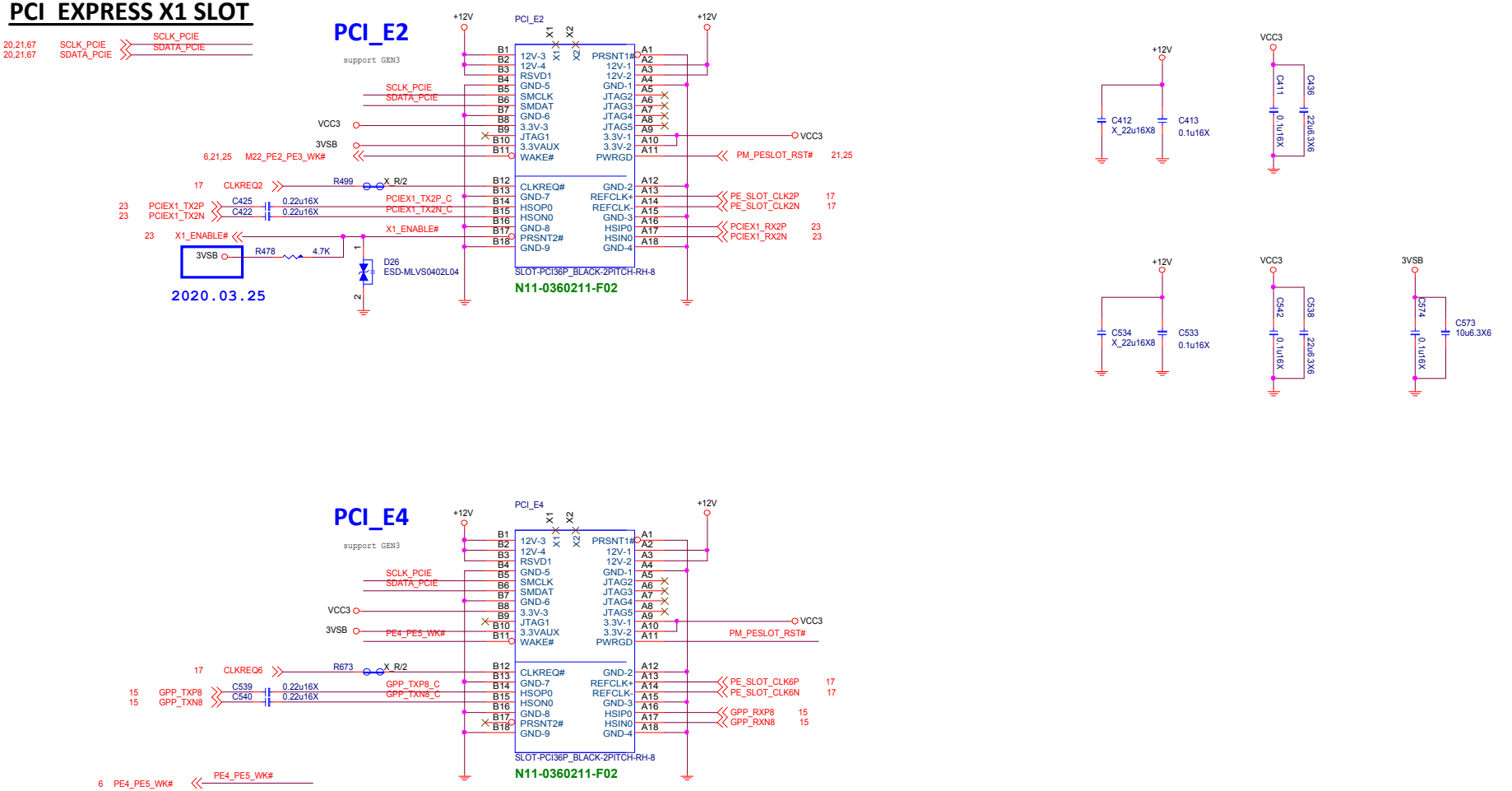




PCI Express x4 Slot		
+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: PCI_E3 (X4)	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 21 of 78	

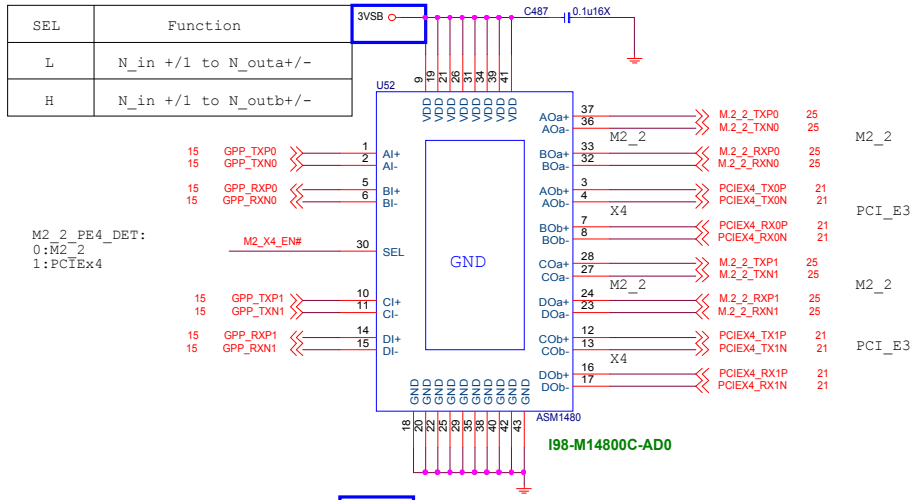
PCI_EXPRESS X1 SLOT

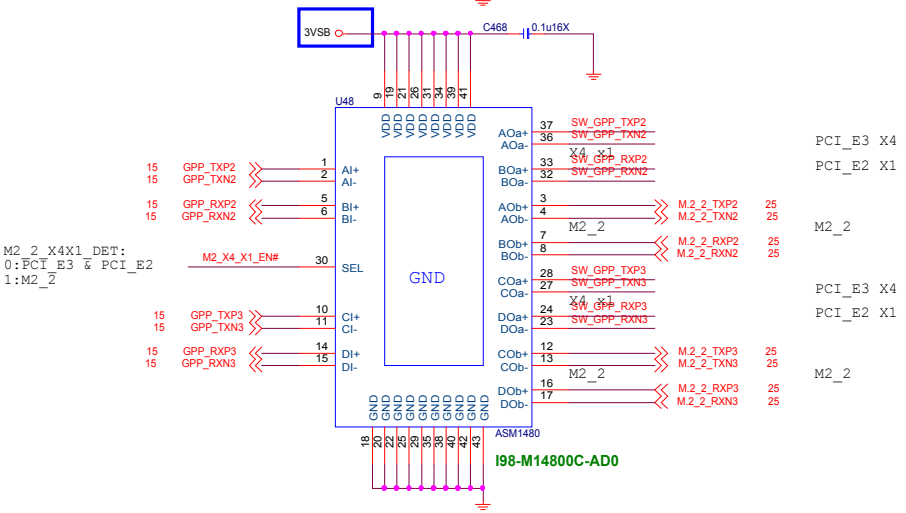


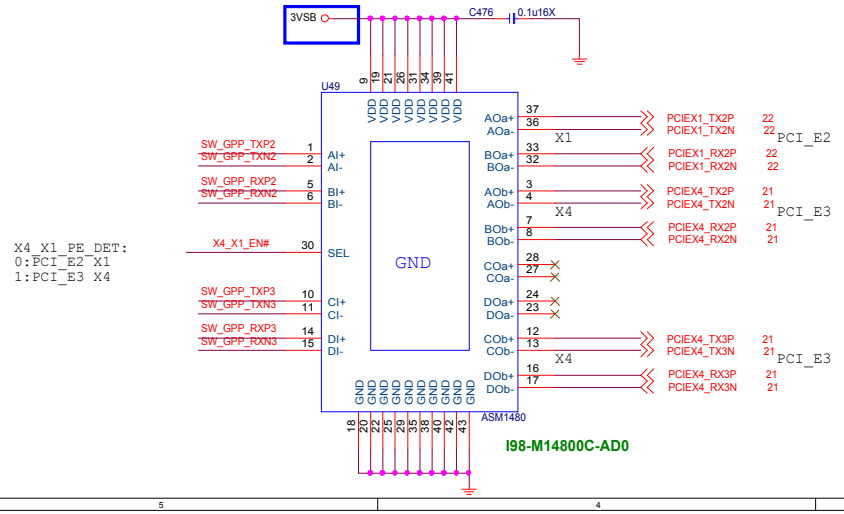
PCI Express x1 Slot *3		
+12V		- 1.5 A
+VCC3		- 9A
+3V3_S5	(wake)	- 1.125A
+3V3_S5	(no wake)	- 20mA

MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: PCI_E2/E4_X1	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 22 of 78	

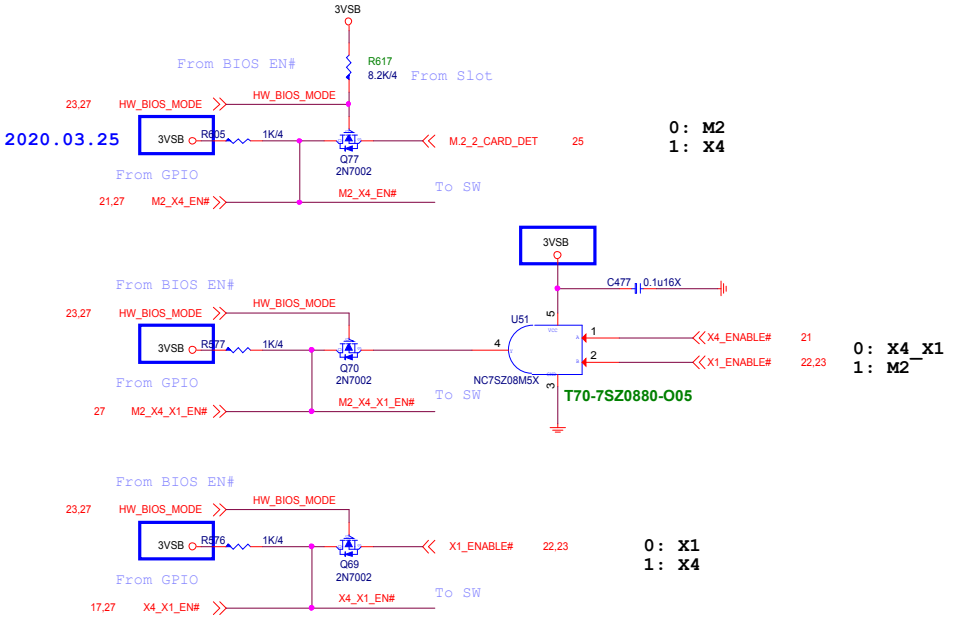
SEL	Function
L	N_in +/1 to N_outa+/-
H	N_in +/1 to N_outb+/-







PCIE Lanes control circuit



HW_BIOS_MODE = High(HW MODE)

DEVICE	M2_2 X4	●(4)	X	X	●(2)	●(2)	X	X	●(2)
	PCI_E3 X4	X	●(4)	X	●(0)	X	●(2)	X	●(0)
	PCI_E2 X1	X	X	●(1)	X	●(1)	●(1)	X	●(1)
DETECT	M.2_2_CARD_DET	0	1	1	0	0	1	1	0
	X1_ENABLE#	1	1	0	1	0	0	1	0
	X4_ENABLE#	1	0	1	0	1	0	1	0

●(X) = availability Lanes number

HW_BIOS_MODE = Low(BIOS MODE)

BIOS GPIO SWITCH	M2_X4_EN#	0	0	0	0	1	1	1	1
	M2_X4_X1_EN#	0	0	1	1	0	0	1	1
	X4_X1_EN#	0	1	0	1	0	1	0	1
DEVICE	M2_2 X4	●(2)	●(2)	●(4)	●(4)	●(0)	●(0)	●(0)	●(0)
	PCI_E3 X4	●(0)	●(0)	●(0)	●(0)	●(2)	●(4)	●(2)	●(2)
	PCI_E2 X1	●(1)	●(0)	●(0)	●(0)	●(1)	●(0)	●(0)	●(0)

MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	PCIE GEN3 SWITCH	21

Date: Tuesday, April 21, 2020 Sheet 23 of 78

M.2_1 Connector

VCC3 4.25A
Max: 14W

M2下方零件擺放限高要小於0.9mm的零件

2020.03.25

LANE REVERSE TO SUPPORT SATA SSD

M2_1

1	GND-1	2	3.3V-1
3	GND-2	4	3.3V-2
5	PERn3	6	PWRDIS(O)(0/1.8/3.3V)/NC
7	PERp3	8	PLN#(I)(0/1.8/3.3V)/NC
9	GND-3	10	DAS/DSS (I/O)/LED_1# (I)(0/3.3V)
11	PETn3	12	3.3V-3
13	PETp3	14	3.3V-4
15	GND-4	16	3.3V-5
17	PERn2	18	3.3V-6
19	PERp2	20	NC-4
21	GND-5	22	VIO 1.8V/NC
23	PETn2	24	NC-6
25	PETp2	26	NC-7
27	GND-6	28	NC-8
29	PERn1	30	PLA_S3#(O)(0/3.3V)/NC
31	PERp1	32	GND/NC
33	GND-7	34	USB_D+/NC
35	PETn1	36	USB_D-/NC
37	PETp1	38	DEVSLP(SATA)/GND(PCIE) (O)
39	GND-8	40	SMB_CLK (I/O)(0/1.8V)
41	PERn0/SATA-B+	42	SMB_DATA (I/O) (0/1.8V)
43	PERp0/SATA-B-	44	ALERT# (I) (0/1.8V)
45	GND-9	46	NC-16
47	PETn0/SATA-A-	48	NC-17
49	PETp0/SATA-A+	50	PERST# (O)(0/1.8/3.3V) or NC
51	GND-10	52	CLKREQ# (I/O)(0/1.8/3.3V) or NC
53	REFCLKN	54	PEWAKE# (I/O)(0/1.8/3.3V) or NC
55	REFCLKP	56	NC-18
57	GND-11	58	NC-19
67	NC-1	68	SUSCLK(32kHz) (O)(0/1.8/3.3V)
69	PEDET (NC-PCIe/GND-SATA)	70	3.3V-7
71	GND-12	72	3.3V-8
73	GND/VIO_CFG(I)	74	3.3V-9
75	GND-14		

KEY M

SLOT-NGFFCARD67P_BLACK-HF-88

APU_GPP_RXN0 / APU_GPP_RXP0 → C245 / C246 0.22u16X → M.2_TXN0_C / M.2_TXP0_C
APU_GPP_TXN0 / APU_GPP_TXP0
APU_GPP_RXN1 / APU_GPP_RXP1 → C247 / C253 0.22u16X → M.2_TXN1_C / M.2_TXP1_C
APU_GPP_TXN1 / APU_GPP_TXP1
APU_GPP_RXN2 / APU_GPP_RXP2 → C263 / C265 0.22u16X → M.2_TXN2_C / M.2_TXP2_C
APU_GPP_TXN2 / APU_GPP_TXP2
APU_GPP_RXP3 / APU_GPP_RXN3 → C272 / C275 0.22u16X → M.2_TXN3_C / M.2_TXP3_C
APU_GPP_TXN3 / APU_GPP_TXP3
CLK_M2_DN / CLK_M2_DP

M.2_1_DAS → M.2_1_DAS 65 → VCC3
M2_1_PLN# / M.2_1_DAS → R286 10K → VCC3
2020.03.25

Close to PIN2,4

C237 22u6.3X6 / C238 0.1u16X / C239 X_1u6.3X4

Close to PIN12, 14, 16, 18

VCC3 → R297 10K → DEVSLP_R → D13 S-LRB520S → DEVSLP0 6
M2_SMB_CLK / M2_SMB_DATA
2020.03.25

C254 X_22u6.3X6 / C256 X_1u6.3X4 / C255 0.1u16X

M2_1_RST# → R307 0R/4 → CLK_REQ1_M.2 6
CLK_REQ_M.2 / APU_WAKE → R313 X_0R/4 → APU_WAKE# 6,17

Close to PIN70, 72, 74

C296 22u6.3X6 / C298 X_1u6.3X4 / C297 0.1u16X

M2TEST → TP4

PIN 69
Low SATA
NC PCIE

VCC3 → R333 10K → M.2_1_CARD_DET 6
3VSB → R320 10K → M.2_1_DET 6
D14 ESD-MLVS0402L04 → M.2_1_DET
D15 ESD-MLVS0402L04 → M.2_1_CARD_DET

M.2_CARD_DET:
0:Have M.2
1:No M.2

PCIE/SATA Mode

PLN#
2020.03.25

VCC3 → R3827 X_10K → M2_1_PLN#
25,27 SIO_PLN → Q135 2N7002

VCC3 → R3802 10K → M21_AUX_RST#
6,7,17,20,34 PCIE_REST# → R3841 X_10K
2020.04.07

3VSB → 0.1u16X C266 → U27 NC7SZ08M5X → R303 X_R/2 → VCC3 → R300 X_10K → M2_1_RST#
T70-7SZ0880-O05
R306 X_0R/4

2020.03.25 SMBUS Level Shift IC 2020.04.16

CPU_1P8 → R3813 X_2.2K/4 M2_SMB_CLK / R3814 X_2.2K/4 M2_SMB_DATA
VCC3 → R3817 X_10K
CPU_1P8 → C1656 X_0.1u16X
VCC3 → C1657 X_0.1u16X
U81 X_PCA9617ADPJ_TSSOP8-RH
25 M2_SMB_CLK / 25 M2_SMB_DATA → R3815 X_0R/4 M2_SMB_CLK_R / R3816 X_0R/4 M2_SMB_DATA_R
M2_SMB_EN
SCLK0 6,11,62 / SDATA0 6,11,62
close to CPU SIDE
CPU Side pull high 4.7K

pull high ESIO SIDE
27 M2_SMB_EN# → Q134 X_2N7002
R3818 X_100K/4

M2_SMB_CLK / M2_SMB_DATA → D99 / D1001 X_ESD-AOZ8131DI
close to U81

RECESS1 SCREW CROSS RECESS E2B-7984020-A89

H1 H2 H3 H4 <HP-BOM> Screw E2B-7B05010

Footprint: H_R240D173_BR189_PT

E2B-7B05010-A89
E2B-7B05010-A89
E2B-7B05010-A89
E2B-7B05010-A89

MICRO-STAR INT'L CO.,LTD

MS-7C91

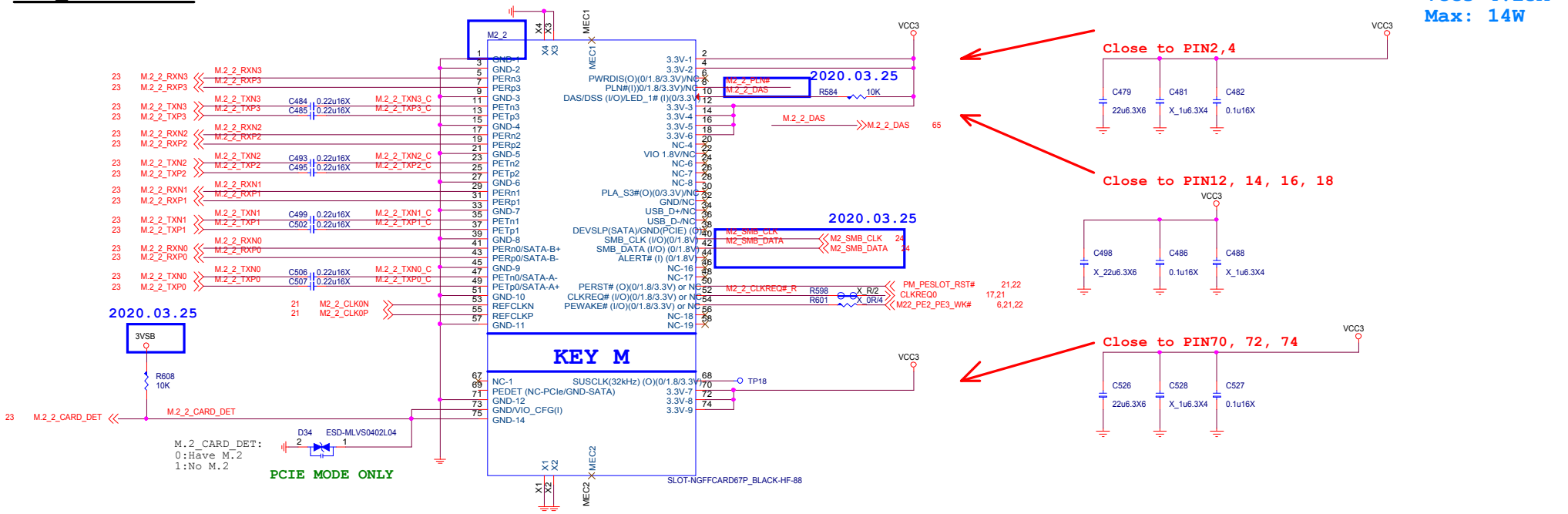
Size	Document Description	Rev
Custom	M2_1 PCIE/SATA Mode(KEY_M)	21

Date: Tuesday, April 21, 2020 Sheet 24 of 78

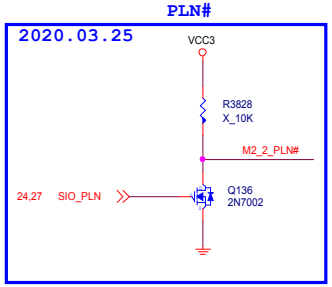
M.2_2 Connector

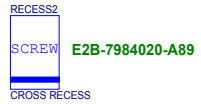
M2下方零件擺放限高要小於0.9mm的零件

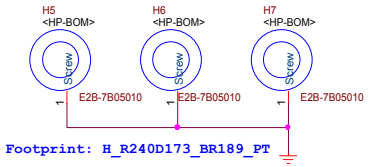
VCC3 4.25A
Max: 14W



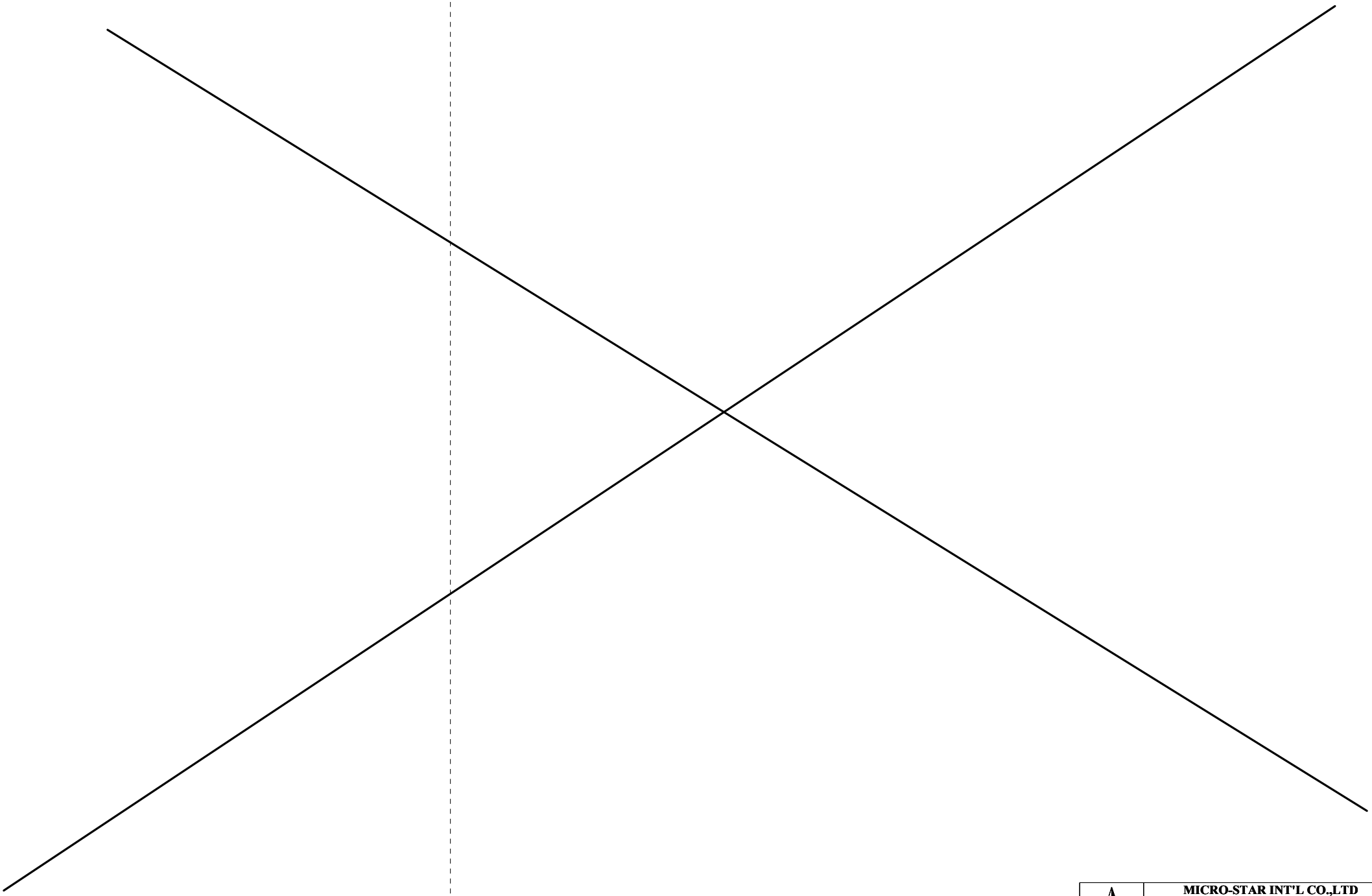
M2_2 use have four-hole footprint
V0A/1.0 BOM : N15-0670330-L06
V2.0 BOM : N15-0671160-F02



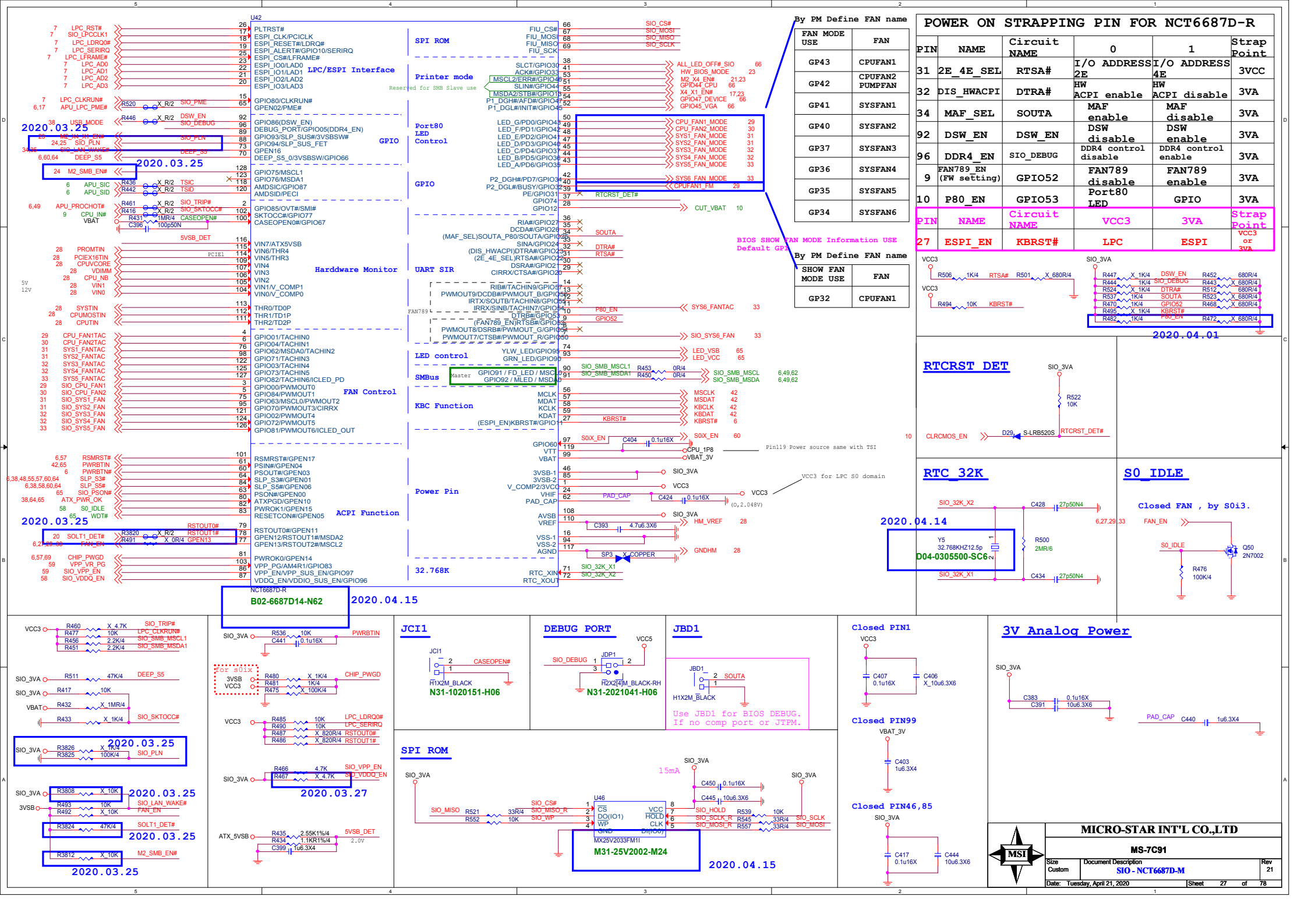




MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: M2_2 PCIE Mode(KEY_M)	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 25 of 78	

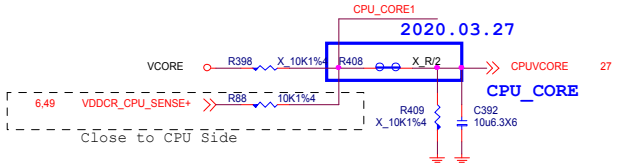


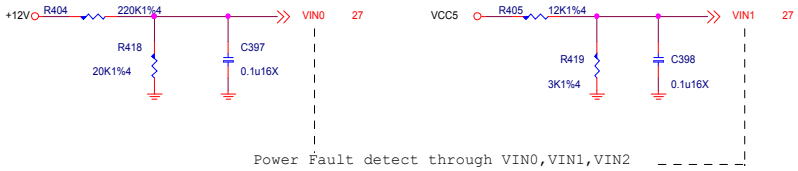
MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: M2_2 - WIFI+BT	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 26 of 78	

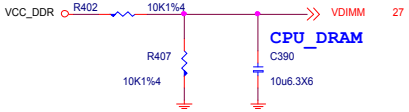

U42
NCT6687D-R
B02-6687D14-N62
2020.04.15
LPC/ESPI Interface
SPI ROM
Printer mode
Port80 LED Control
GPIO
UART SIR
Harddware Monitor
FAN Control
LED control
SMBus
KBC Function
Power Pin
ACPI Function
32.768K
By PM Define FAN name
FAN MODE USE
FAN
GP43 CPUFAN1
GP42 CPUFAN2 PUMPFAN
GP41 SYSFAN1
GP40 SYSFAN2
GP37 SYSFAN3
GP36 SYSFAN4
GP35 SYSFAN5
GP34 SYSFAN6
By PM Define FAN name
SHOW FAN MODE USE
FAN
GP32 CPUFAN1
BIOS SHOW FAN MODE Information USE Default GPI
POWER ON STRAPPING PIN FOR NCT6687D-R
PIN NAME Circuit NAME 0 1 Strap Point
31 2E_4E_SEL RTSA# I/O ADDRESS 2E I/O ADDRESS 4E 3VCC
32 DIS_HWACPI DTRA# HW ACPI enable HW ACPI disable 3VA
34 MAF_SEL SOUTA MAF enable MAF disable 3VA
92 DSW_EN DSW_EN DSW disable DSW enable 3VA
96 DDR4_EN SIO_DEBUG DDR4 control disable DDR4 control enable 3VA
9 FAN789_EN (FW setting) GPIO52 FAN789 disable FAN789 enable 3VA
10 P80_EN GPIO53 Port80 LED GPIO 3VA
PIN NAME Circuit NAME VCC3 3VA Strap Point
27 ESPI_EN KBRST# LPC ESPI VCC3 or 3VA
2020.04.01
RTCRST_DET
RTC_32K
2020.04.14
S0_IDLE
Closed FAN , by S0i3.
JCI1
DEBUG PORT
JBD1
Use JBD1 for BIOS DEBUG. If no comp port or JTPM.
N31-1020151-H06
N31-2021041-H06
SPI ROM
MX25V2033FM1I
M31-25V2002-M24
2020.04.15
Closed PIN1
Closed PIN99
Closed PIN46,85
3V Analog Power
2020.03.25
2020.03.27
MICRO-STAR INT'L CO.,LTD
MS-7C91
SIO - NCT6687D-M
Rev 21
Date: Tuesday, April 21, 2020
Sheet 27 of 78

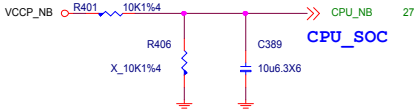
HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect

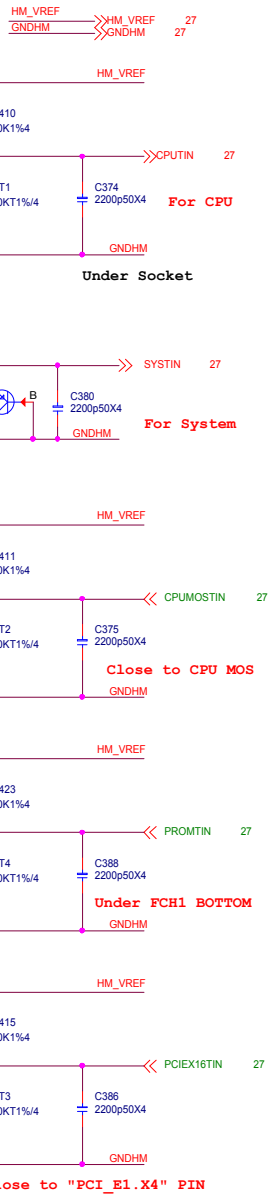








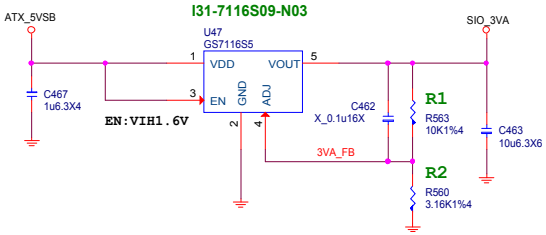
TEMP SENSOR



PM RESET

CPU RESET

SIO_3VA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V

MICRO-STAR INT'L CO.,LTD

MS-7C91

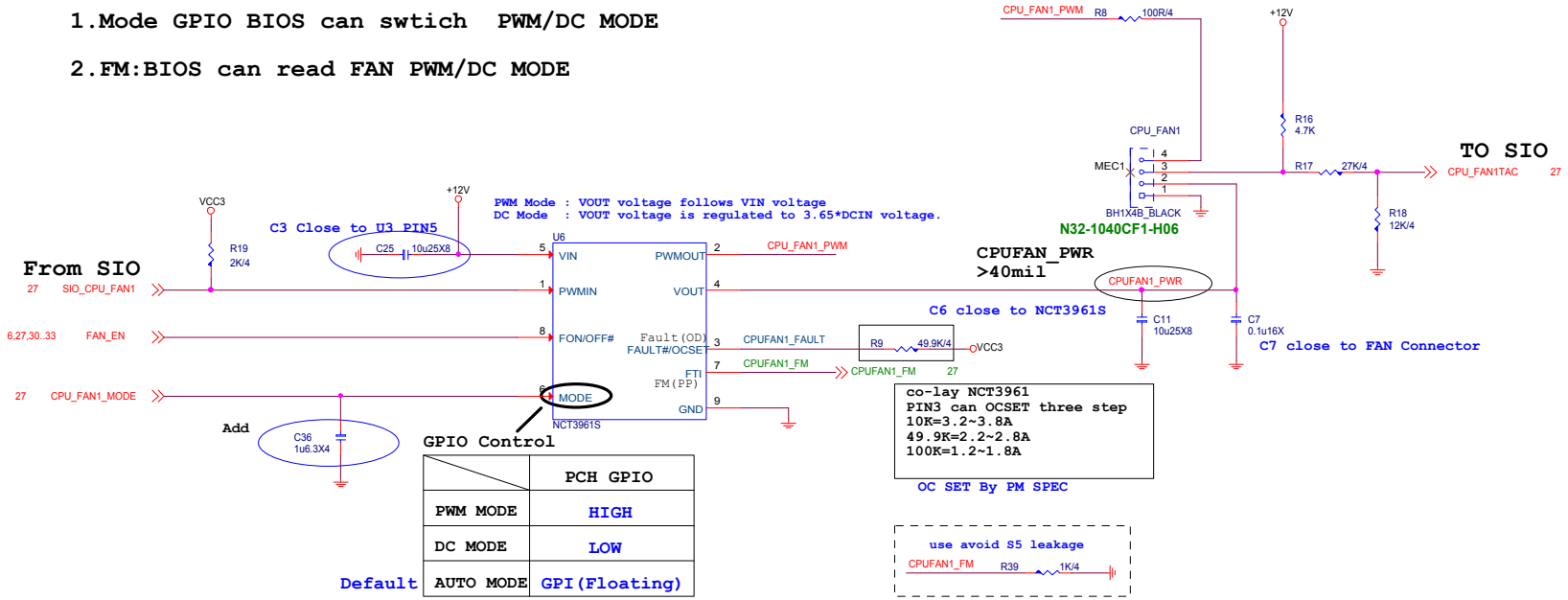
Size	Document Description	Rev
Custom	SIO - HW Monitor	21

Date: Tuesday, April 21, 2020 Sheet 28 of 78

CPUFAN1 TYPE N : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

2.FM:BIOS can read FAN PWM/DC MODE



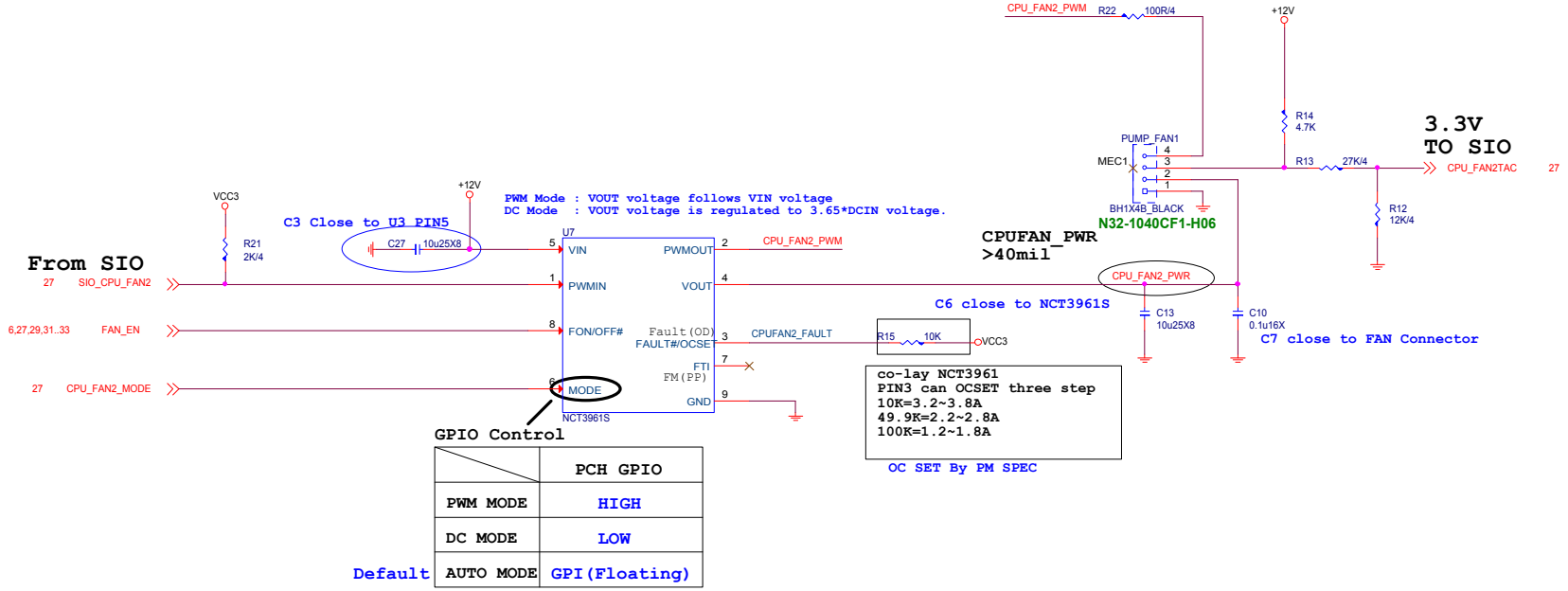
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: FAN TYPE-L CPUFAN1
Rev: 21	
Date: Tuesday, April 21, 2020	Sheet 29 of 78

PUMPFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



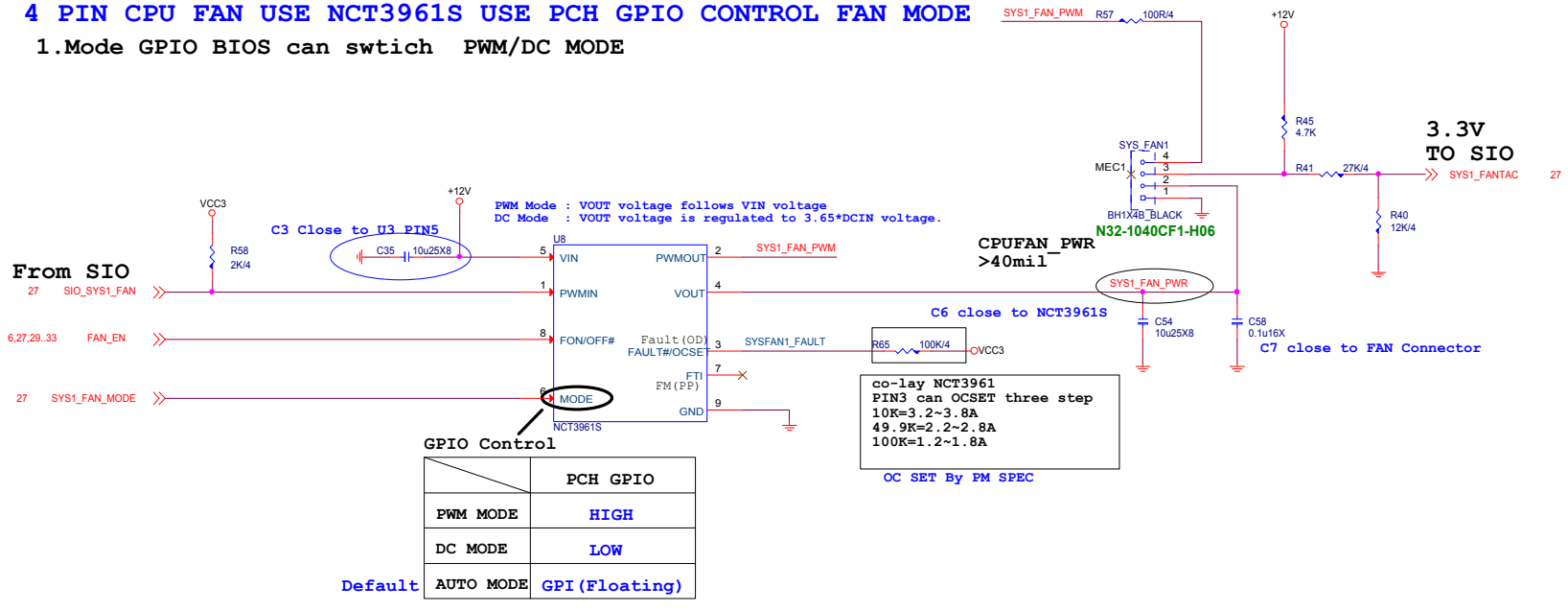
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: FAN TYPE-K PUMPFAN1
Rev: 21	
Date: Tuesday, April 21, 2020	Sheet 30 of 78

SYSFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

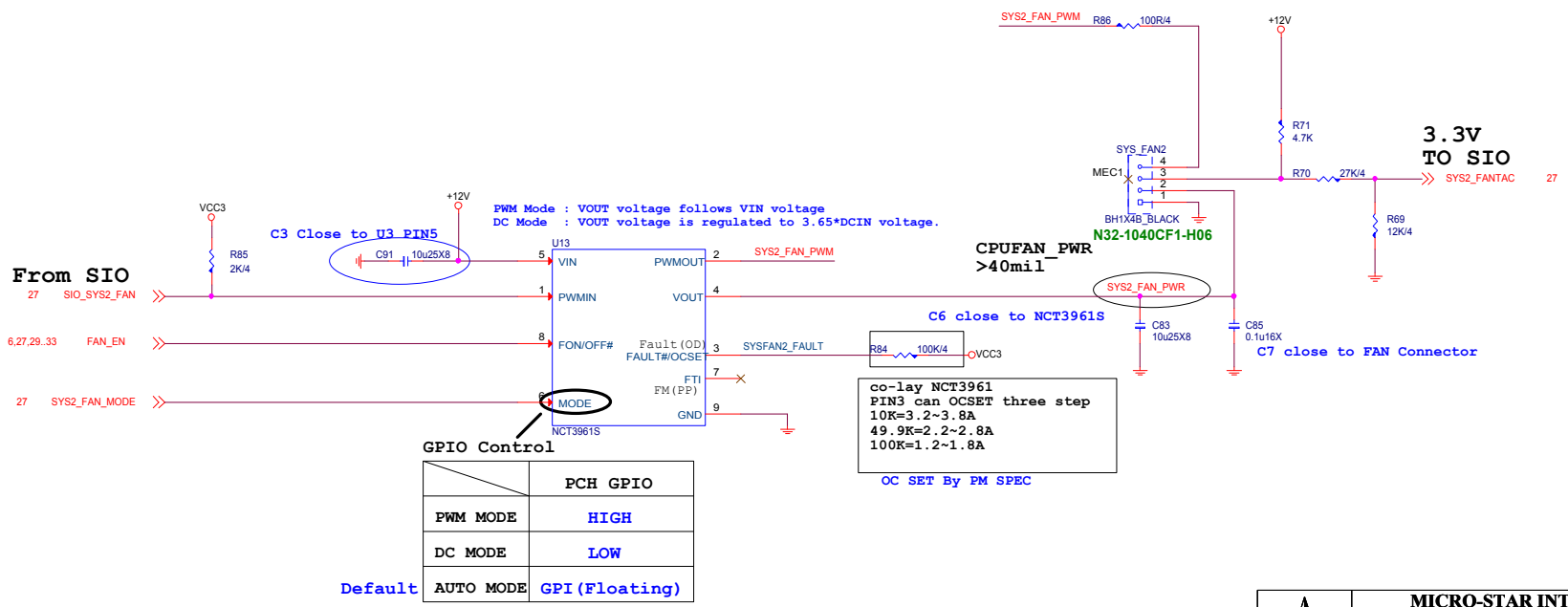


	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

SYSFAN2

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

MS-7C91

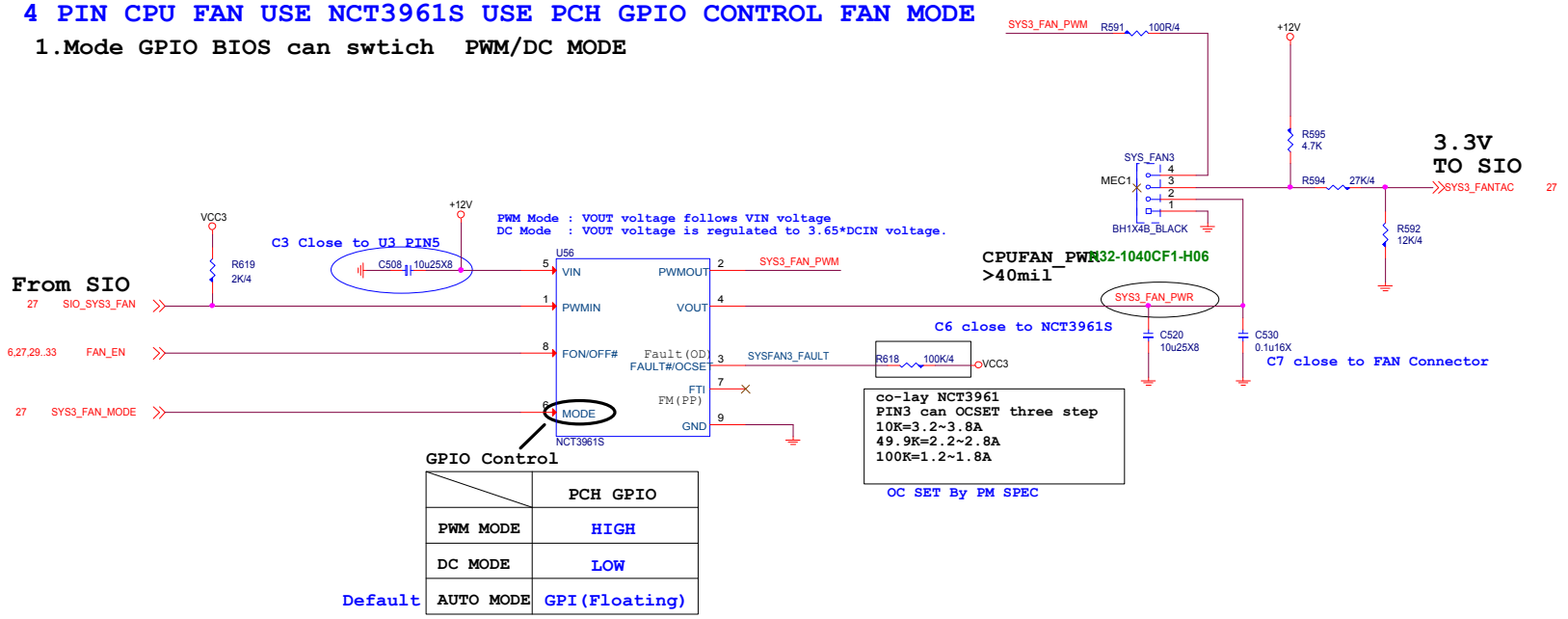
Size	Document Description	Rev
Custom	FAN TYPE-K SYSFAN1/2	21

Date: Tuesday, April 21, 2020 Sheet 31 of 78

SYSFAN3

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

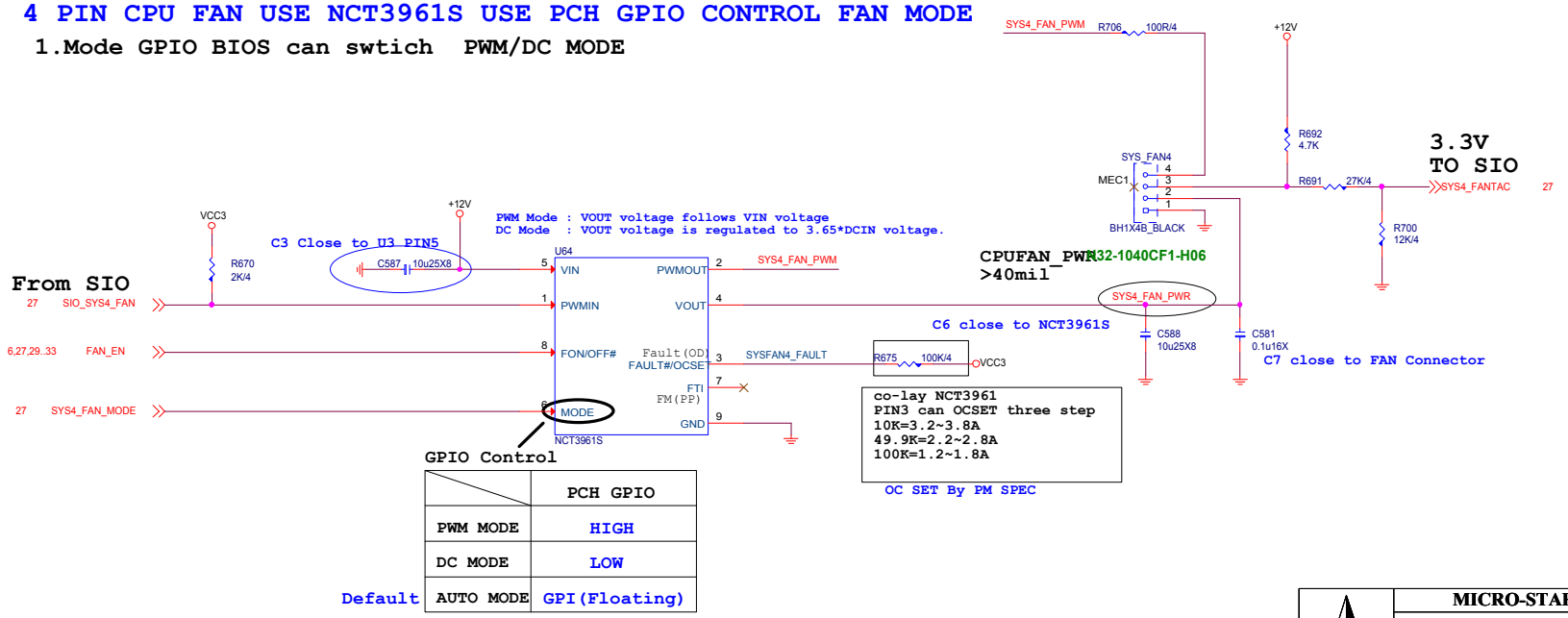


	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

SYSFAN4

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

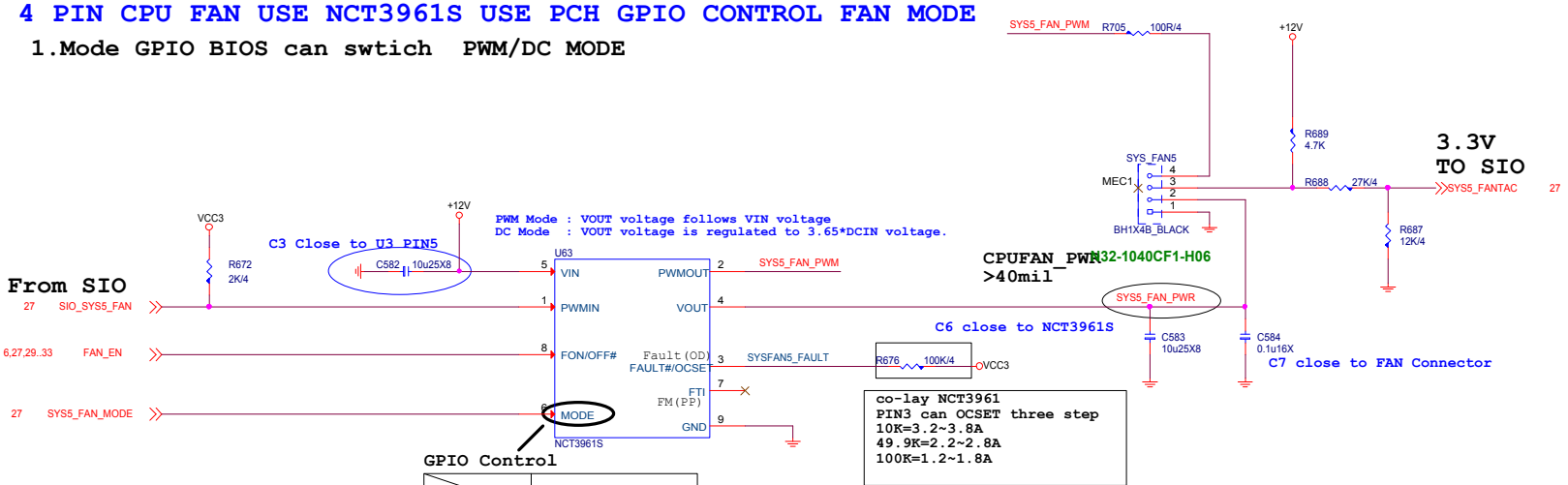
MS-7C91

Size	Document Description	Rev
Custom	FAN TYPE-K SYSFAN3/4	21

Date: Tuesday, April 21, 2020 Sheet 32 of 78

SYSFAN5 TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

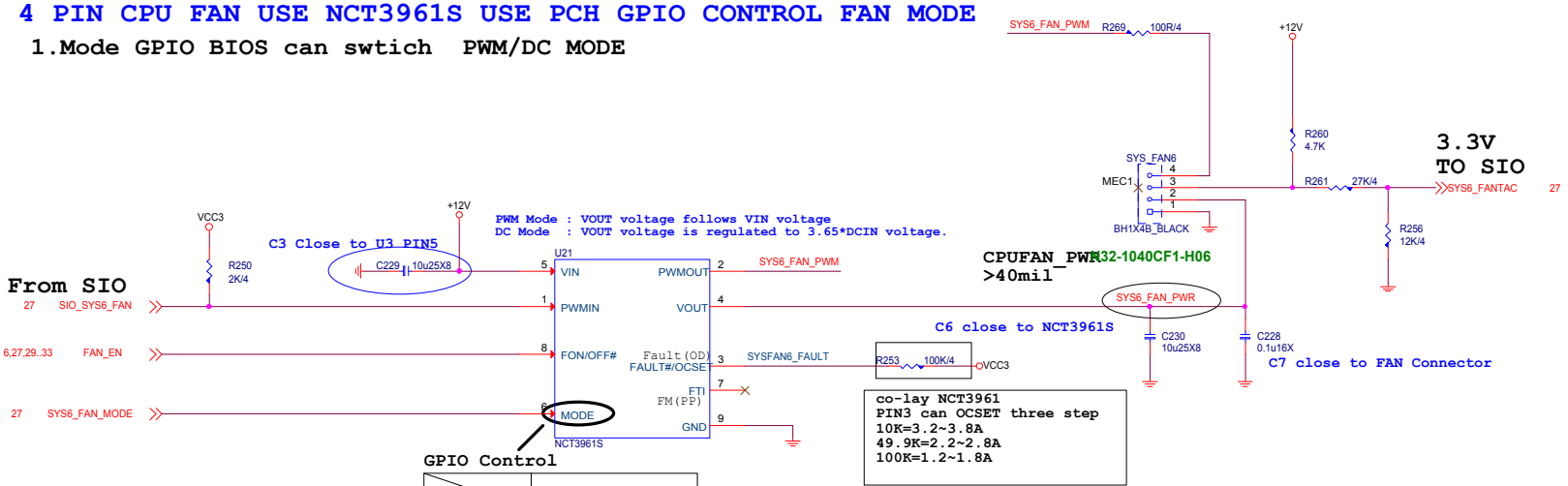
1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

SYSFAN6 TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

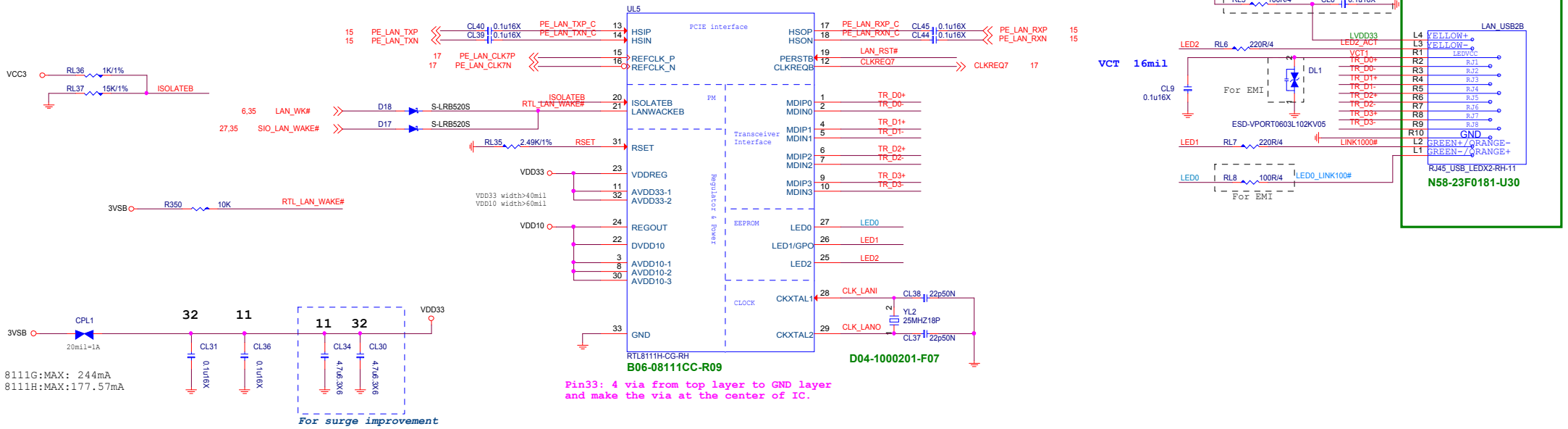
MS-7C91

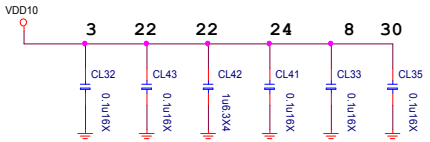
Size	Document Description	Rev
Custom	FAN TYPE-N SYSFAN5	21

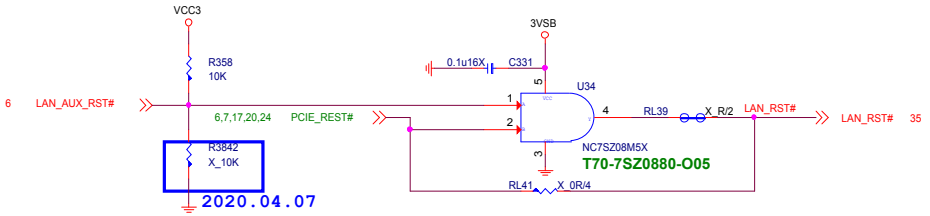
Date: Tuesday, April 21, 2020 Sheet 33 of 78

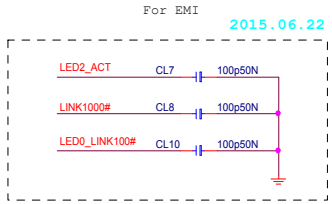
RTL8111H Giga LAN

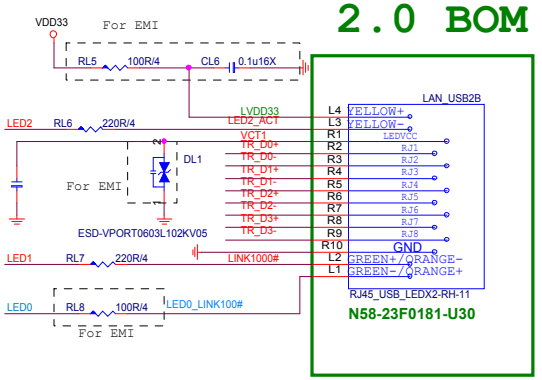
2.0 BOM









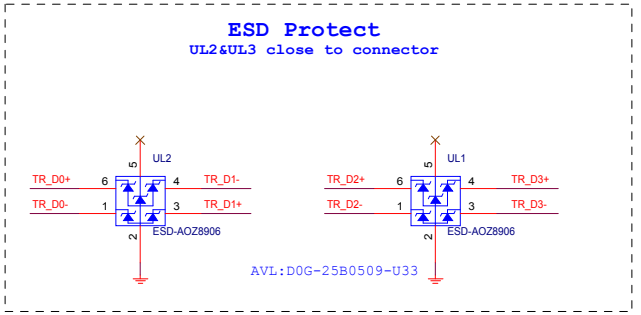


8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15



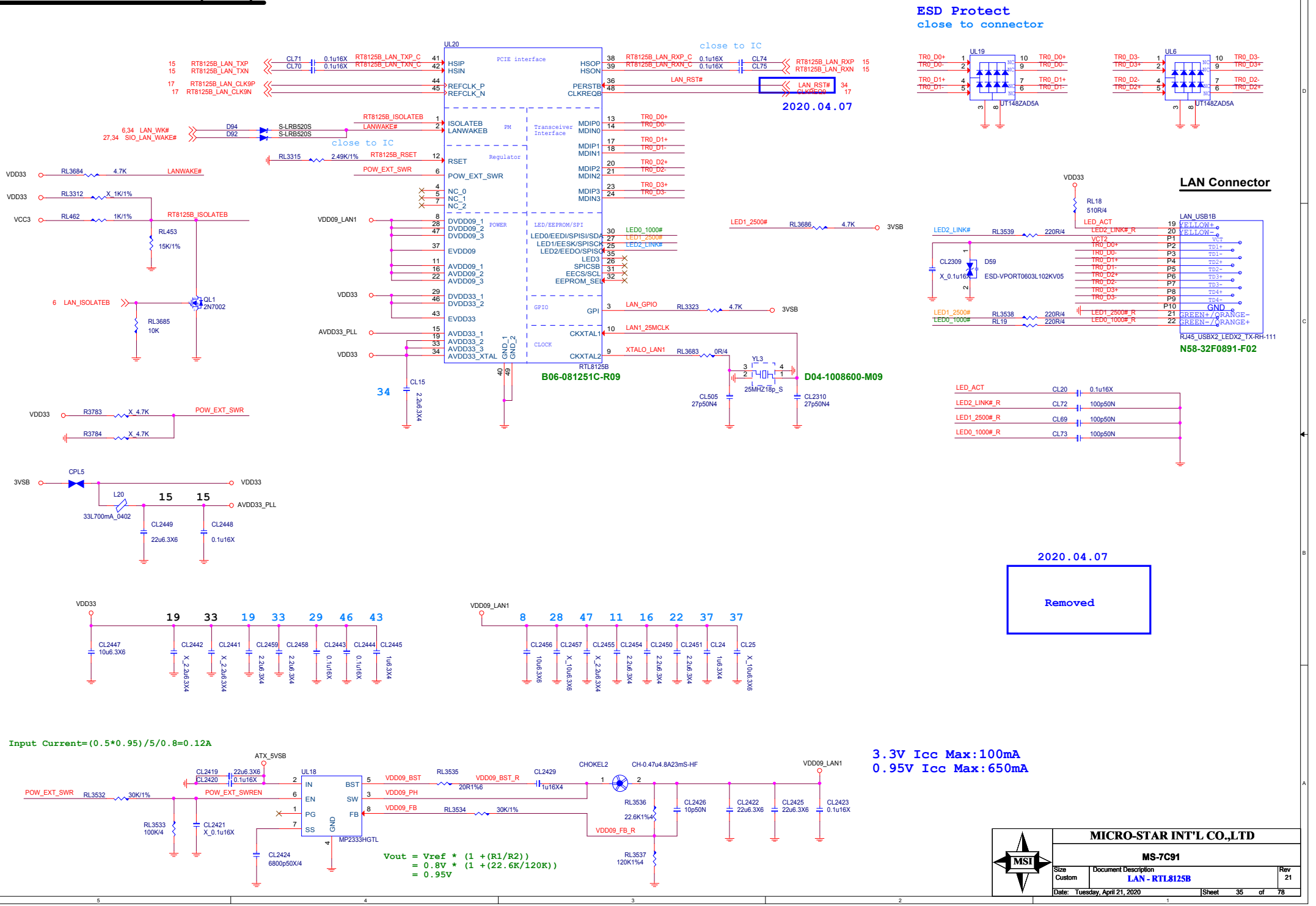
MICRO-STAR INT'L CO.,LTD

MS-7C91

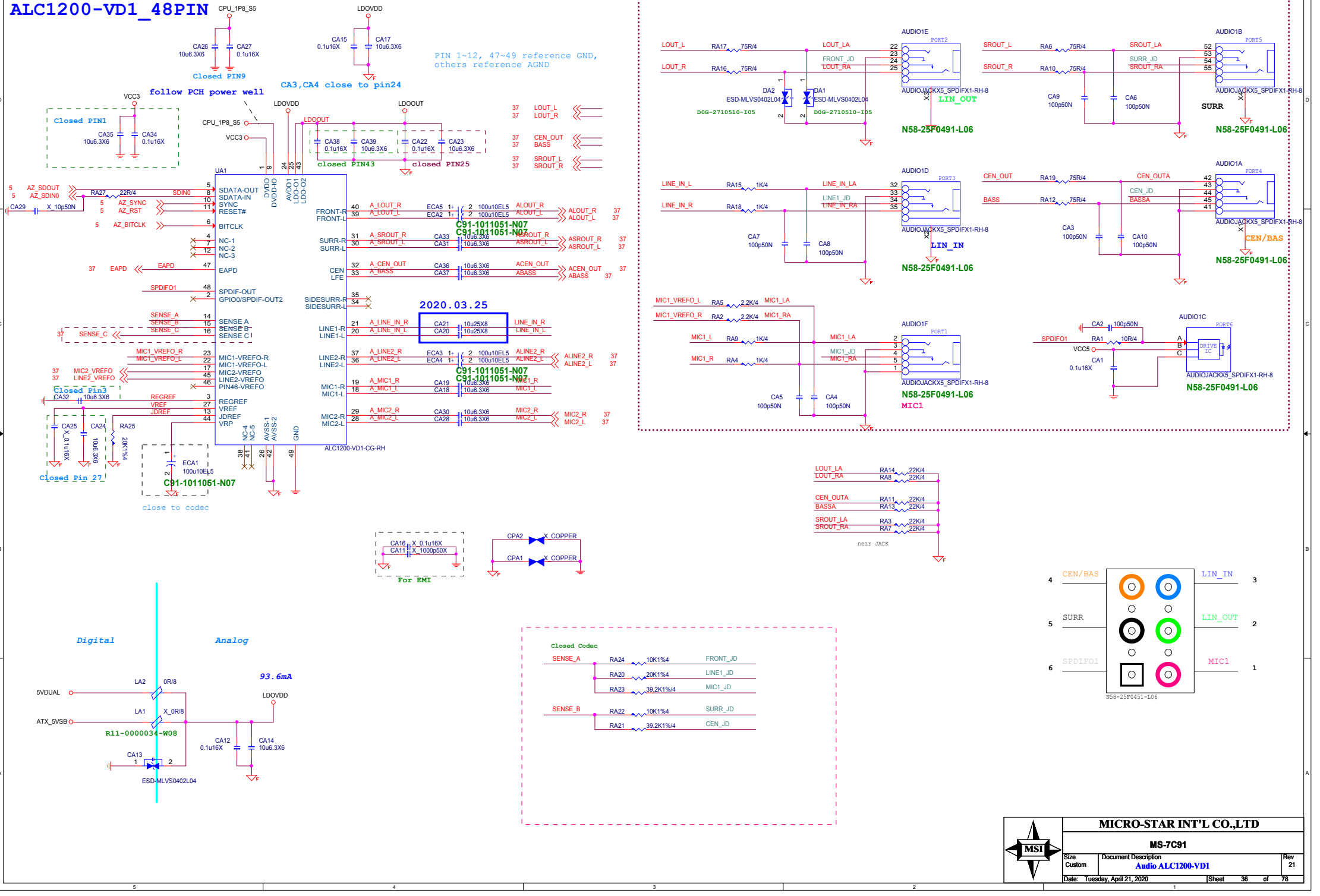
Size	Document Description	Rev
Custom	RTL8111H Giga LAN	21

Date: Tuesday, April 21, 2020 Sheet 34 of 78

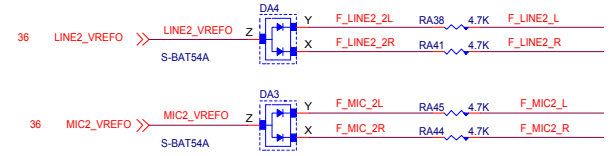
Realtek Lan1-RTL8125B(2.5G)

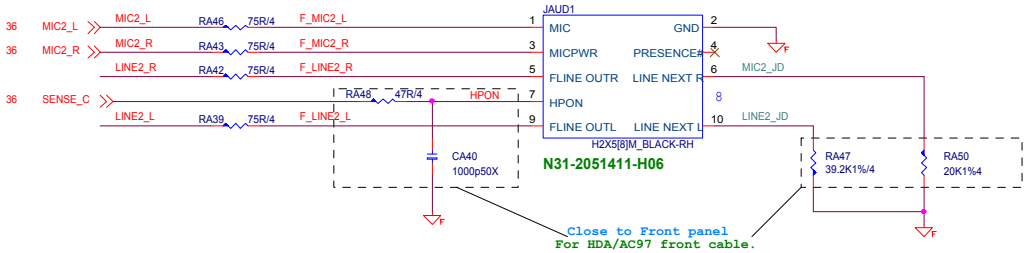


ALC1200-VD1_48PIN



MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: Audio ALC1200-VD1
Rev: 21	
Date: Tuesday, April 21, 2020	Sheet 36 of 78

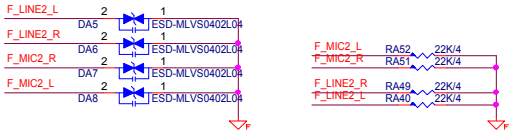




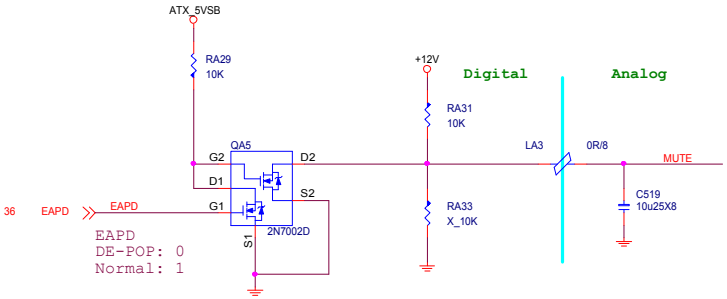
D0G-2710510-I05
Close to Front panel

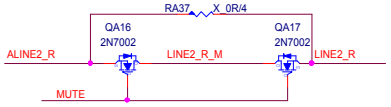
ESD protect

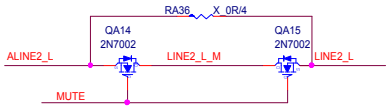
D0G-2710510-I05
AVL:D0G-2950500-SI0

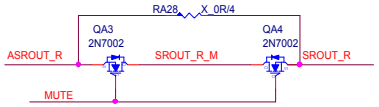


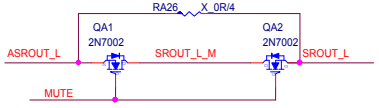
De-POP circuit

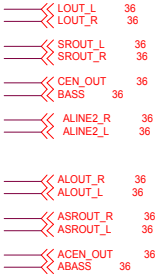


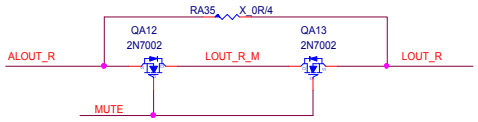


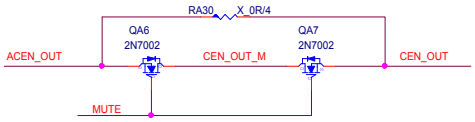


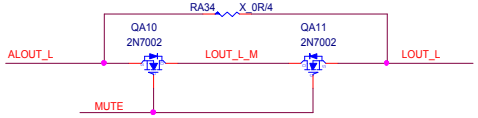


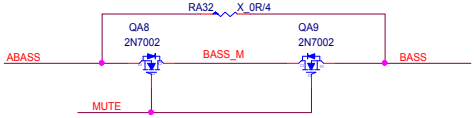












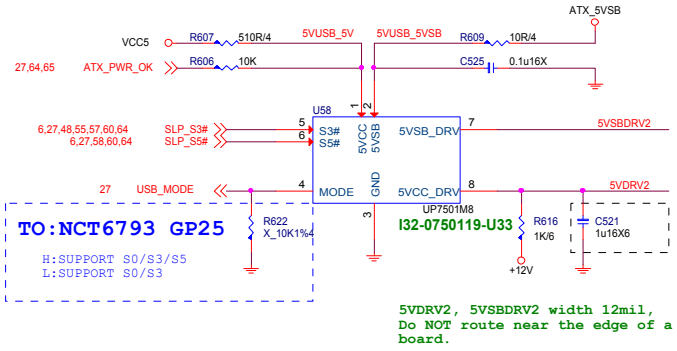
MICRO-STAR INT'L CO.,LTD

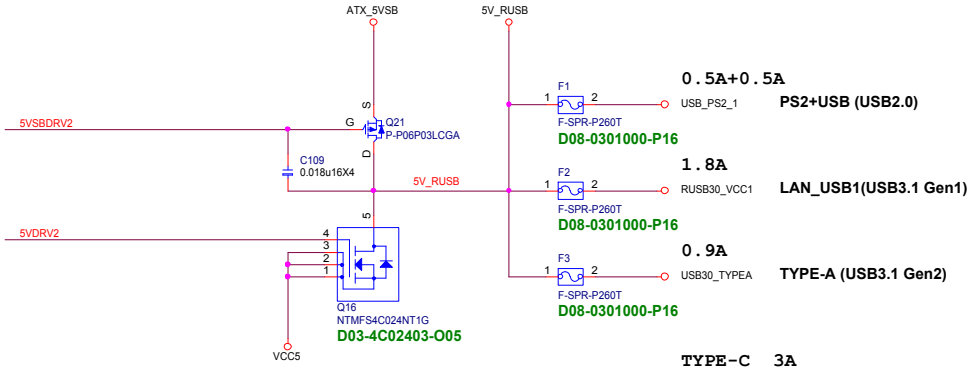
MS-7C91

Size	Document Description	Rev
Custom	Audio DePop	21

Date: Tuesday, April 21, 2020 Sheet 37 of 78

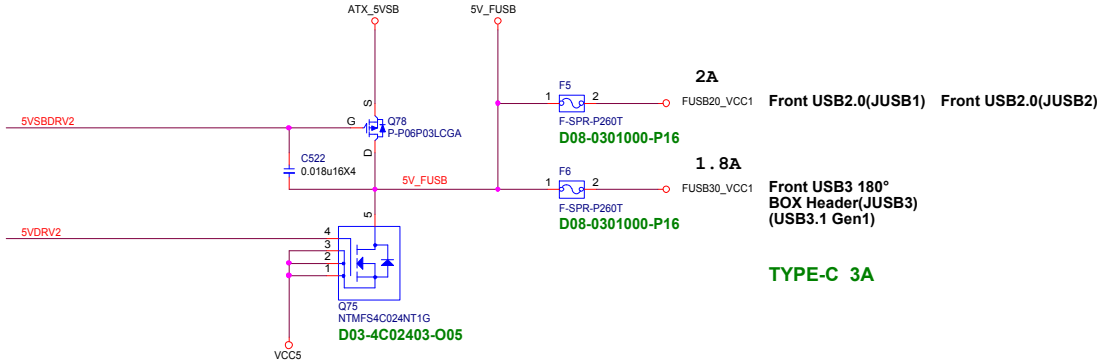
USB Power





Rear (6.7A)

Front (6.8A)

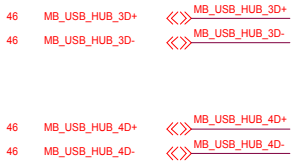


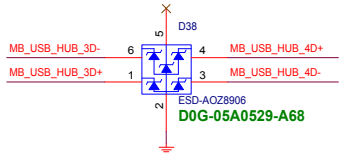
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C91	
Size: Custom	Document Description: USB Power - UP7501	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 38 of 78	

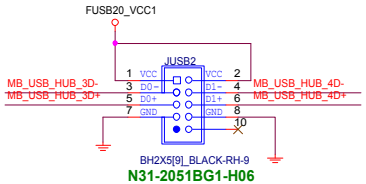
Front USB2.0(JUSB2)

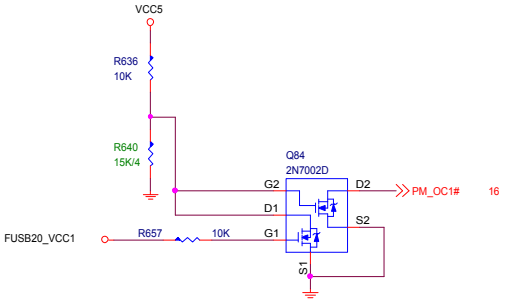
Form GL850G USB2.0 HUB

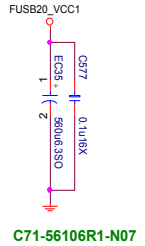
5V@1A







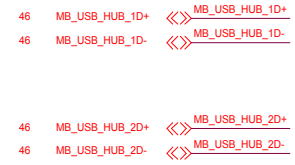


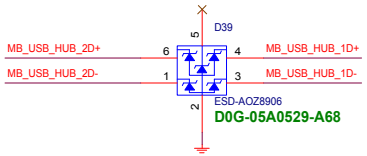


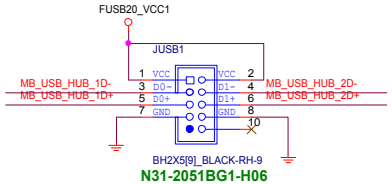
Front USB2.0(JUSB1)

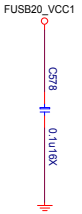
Form GL850G USB2.0 HUB

5V@1A







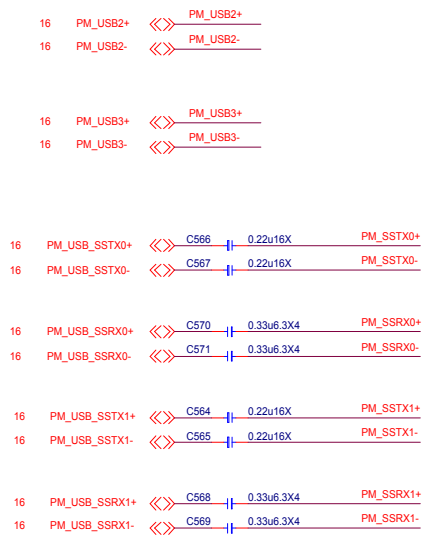


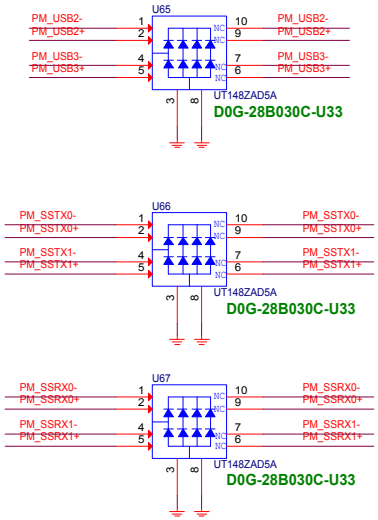
MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: Front USB2.0 Header	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 39 of 78	

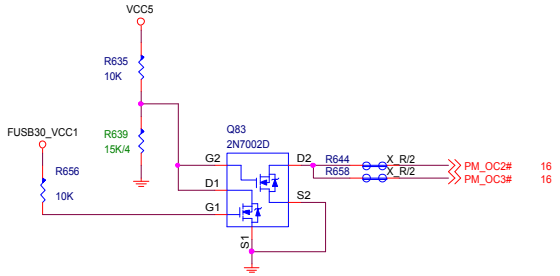
Front USB3 180°

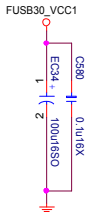
BOX Header(JUSB3)

5V@1.8A

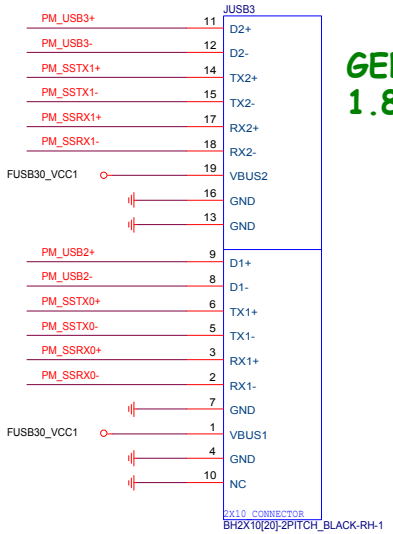








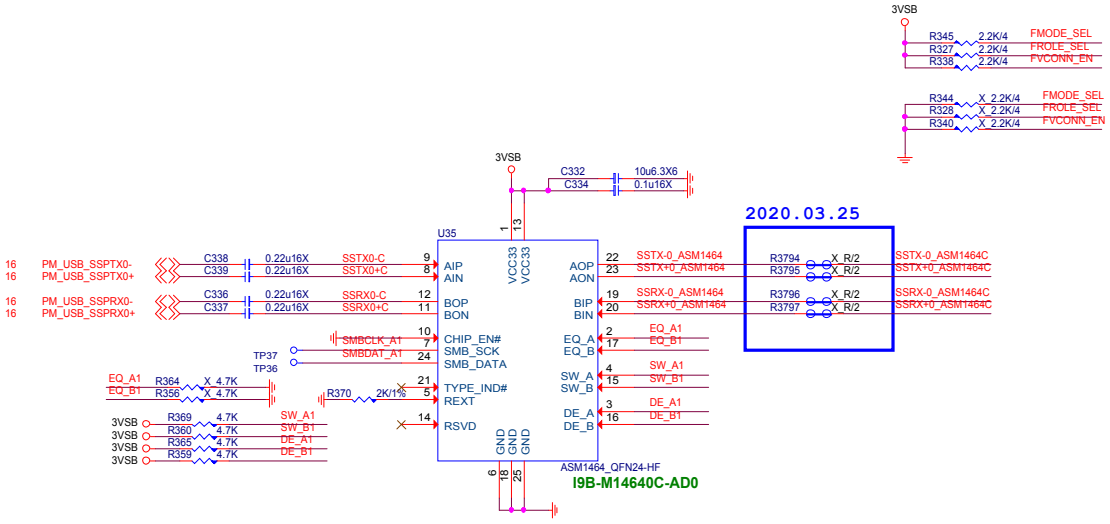
C71-1011761-N07

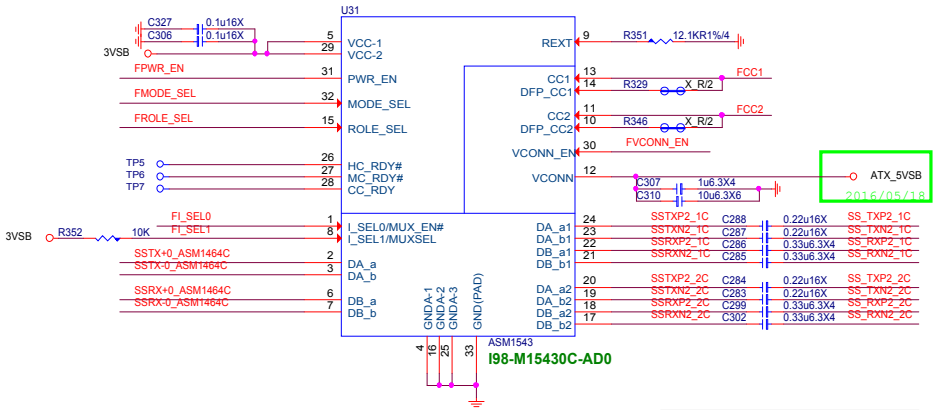


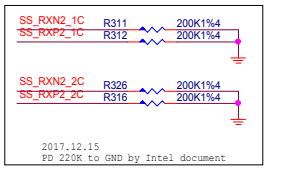
GEN1
1.8A

N32-2101091-H06

MSI	MICRO-STAR INT'L CO.,LTD		
	MS-7C91		
Size: Custom	Document Description: Front USB3.0 Header		Rev: 21
Date: Tuesday, April 21, 2020	Sheet 40 of 78		

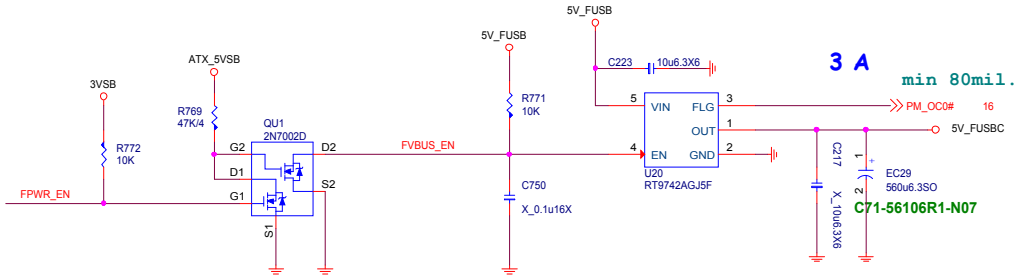




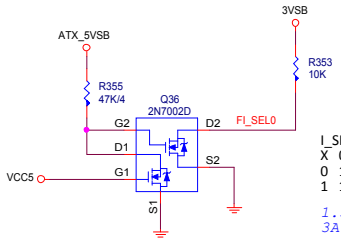


VBUS EN

VCOM OC#

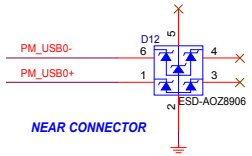


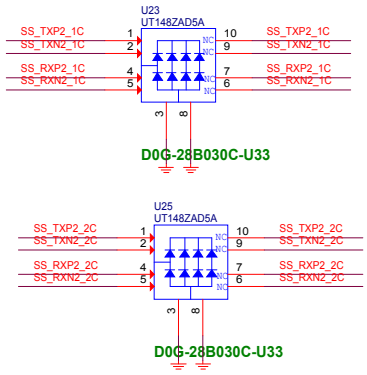
Current Mode

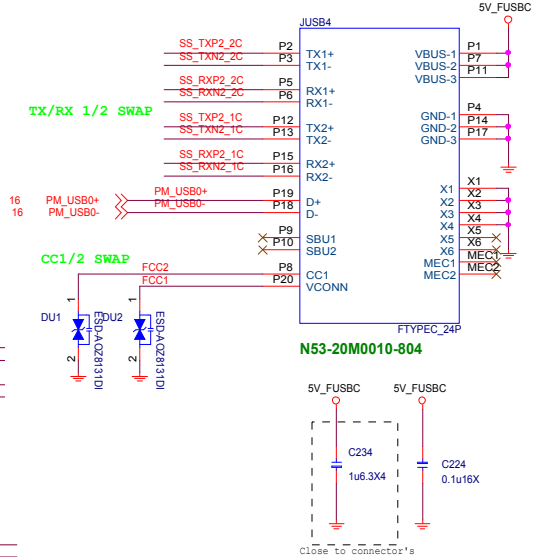


I_SEL0 : I_SEL1
X 0 Default for 900mA
0 1 1.5A @5V
1 1 3A @5V

1.5A under S3 mode
3A under S0 mode







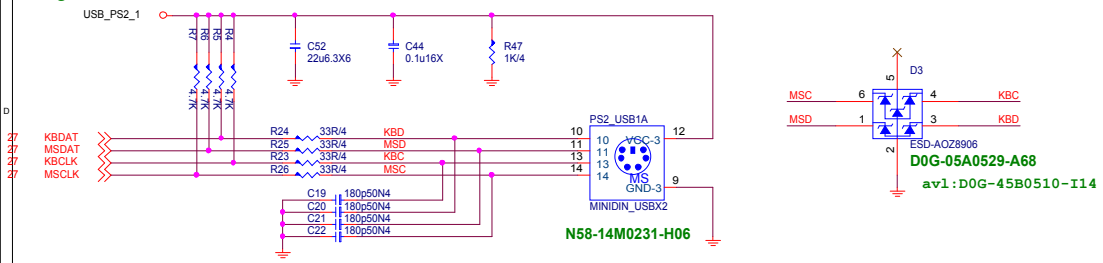
MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title	Front USB3.1 Type C / mux	
Size: Custom	Document Number: MS-7C91	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 41 of 78	

PS2+USB (USB2.0)

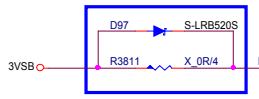
5V@1A

layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch



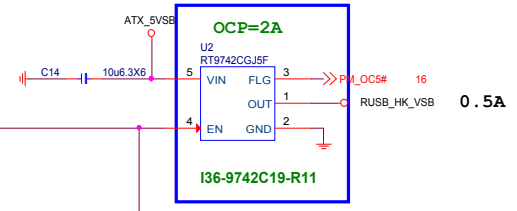
HOTKEY POWER

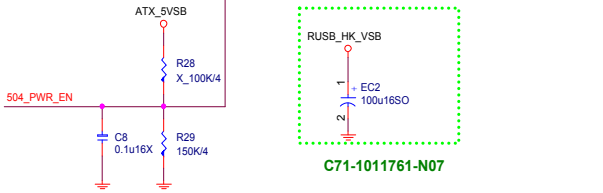
2020.03.25



2020.03.30

OCP=2A

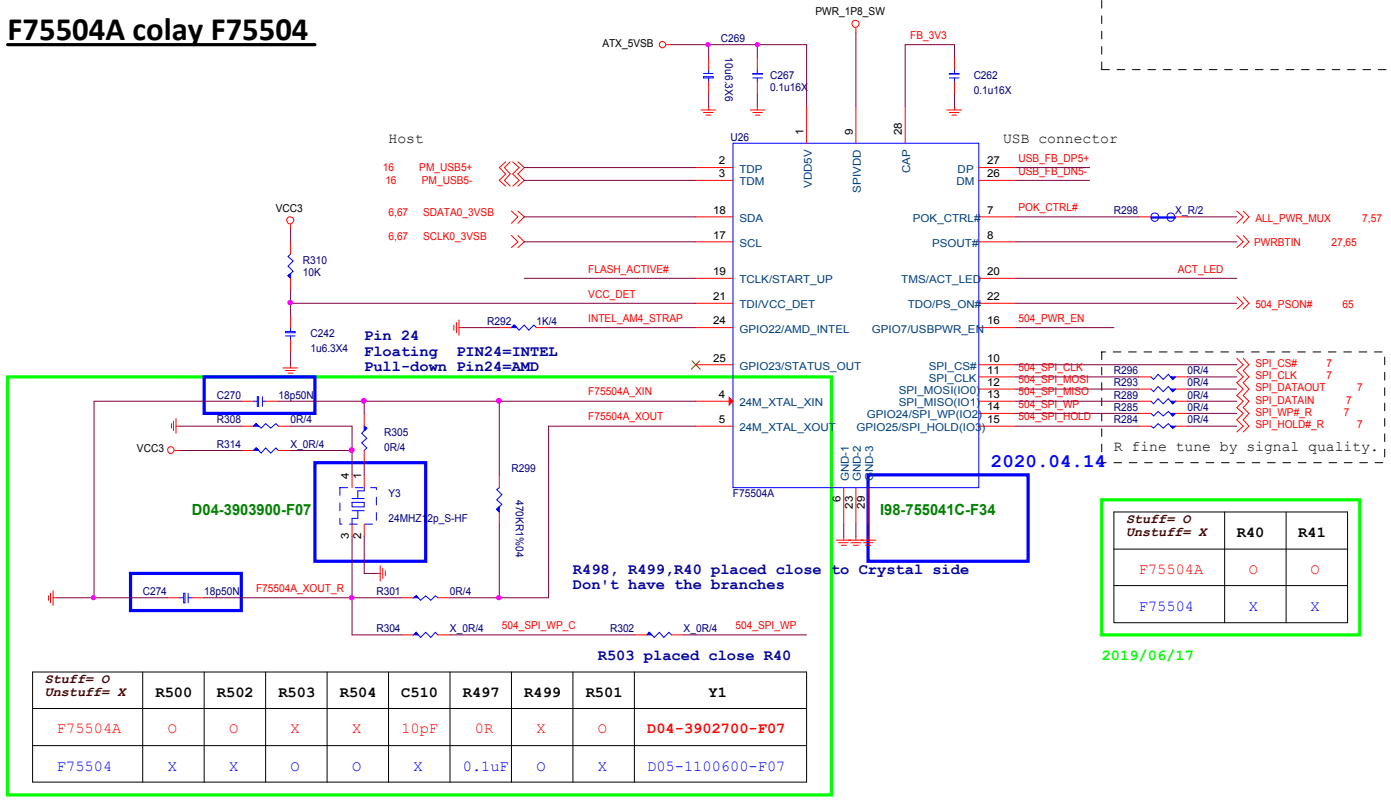




USB Flash BIOS

F75504A colay F75504

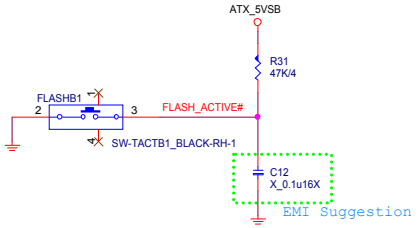
F75504A/F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.

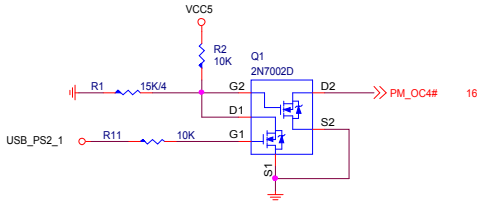


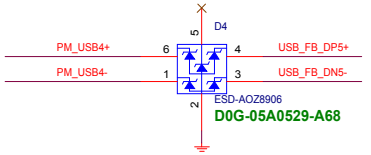
Stuff= O Unstuff= X	R500	R502	R503	R504	C510	R497	R499	R501	Y1
F75504A	O	O	X	X	10pF	0R	X	O	D04-3902700-F07
F75504	X	X	O	O	X	0.1uF	O	X	D05-1100600-F07

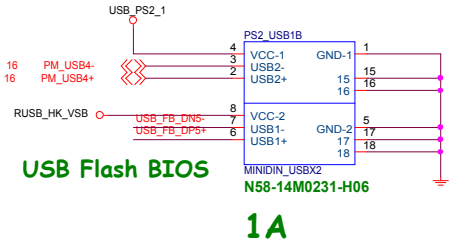
Stuff= O Unstuff= X	R40	R41
F75504A	O	O
F75504	X	X

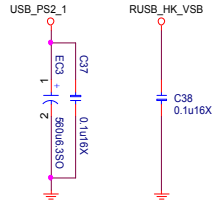
2019/06/17



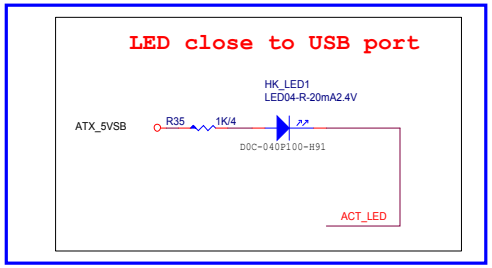






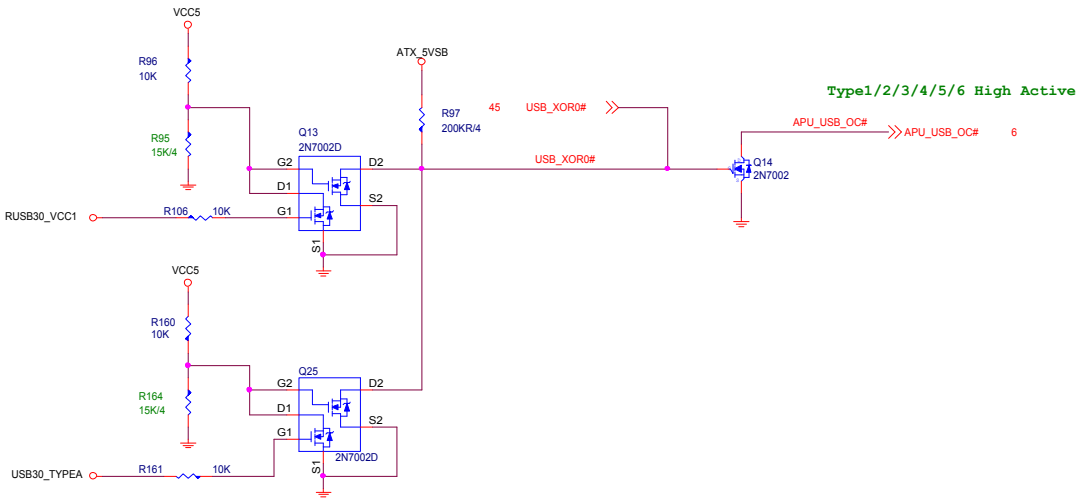


2020.04.14



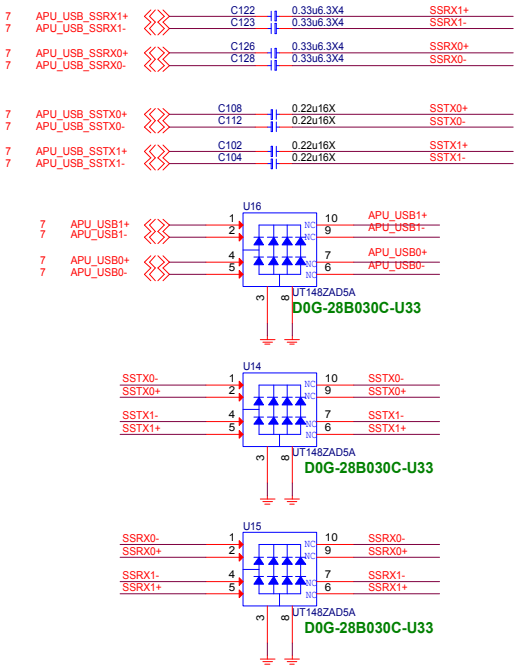
MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: Rear USB2.0+PS2+F75504A
Date: Tuesday, April 21, 2020	Sheet 42 of 78
	Rev 21

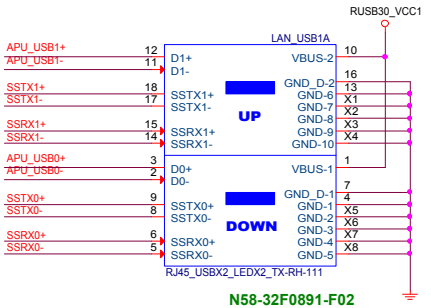
CPU USB_OC



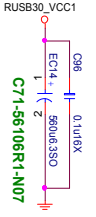
Type1/2/3/4/5/6 High Active

Rear USB3.1 GEN1 5V@1.8A



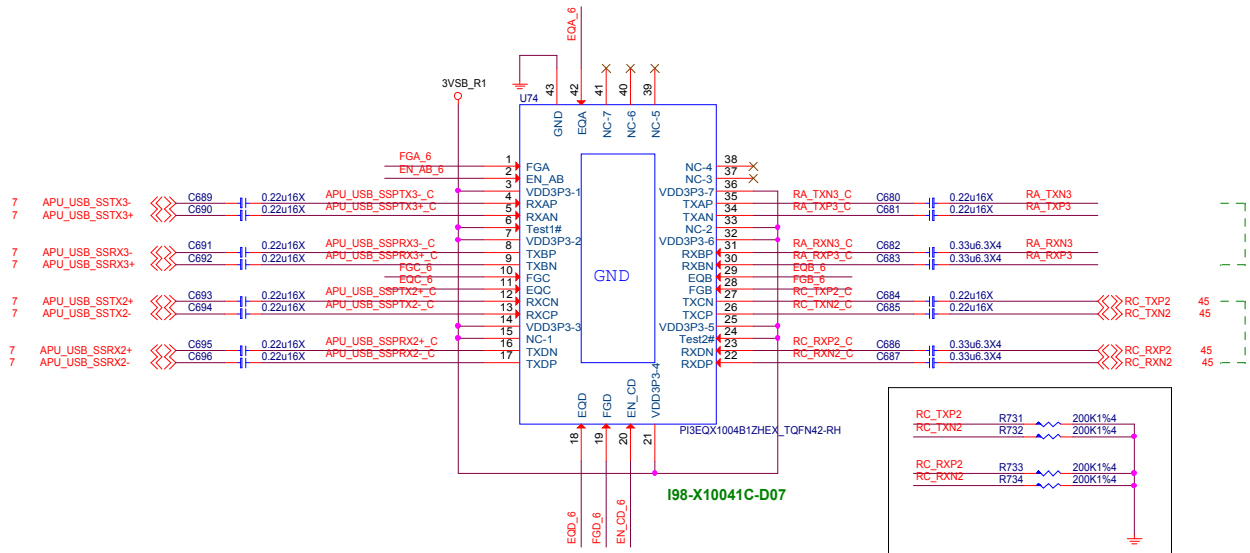


1.8A



MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: Rear USB3.1.
Date: Tuesday, April 21, 2020	Sheet 43 of 78
	Rev 21

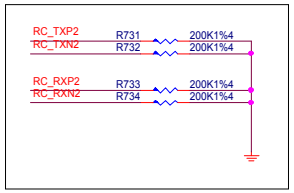
TYPE-A PI3EQX1004 Redriver

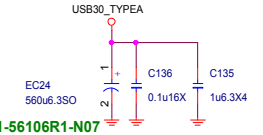


I98-X10041C-D07

Rear TYPE-A

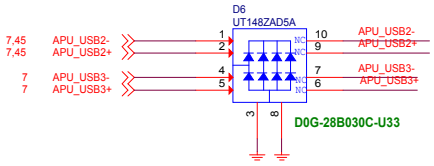
Rear TYPE-C



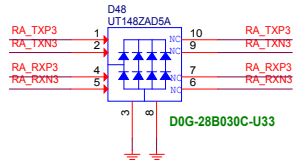


C71-56106R1-N07

close to Type C Connector

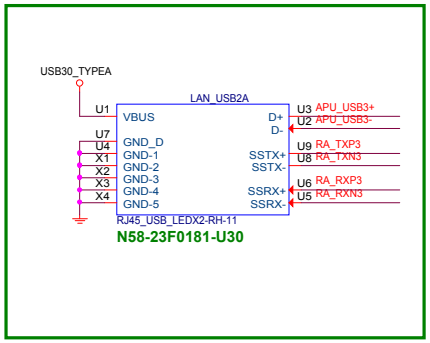


D0G-28B030C-U33

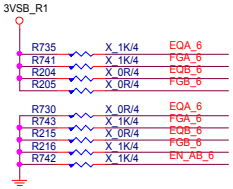


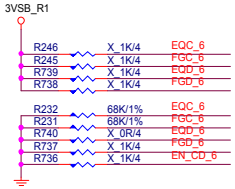
D0G-28B030C-U33

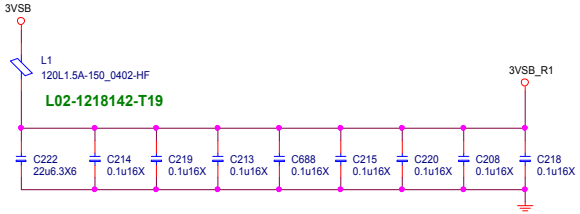
GEN2 0.9A



N58-23F0181-U30







EQ	dB	
0	10.9	0 to GND
R	6.7	68K to GND
F	8.9	NC
1	13.1	0 to VDD

		EQ	FG
USB3_TX4	A	R	F
USB3_RX4	B	R	L
USB3_TX3	C	R	F
USB3_RX3	D	R	L

FG	dB	
0	-3	0 to GND
R	-1.5	68K to GND
F	0	NC
1	2	0 to VDD

0A BOM

MICRO-STAR INT'L CO.,LTD

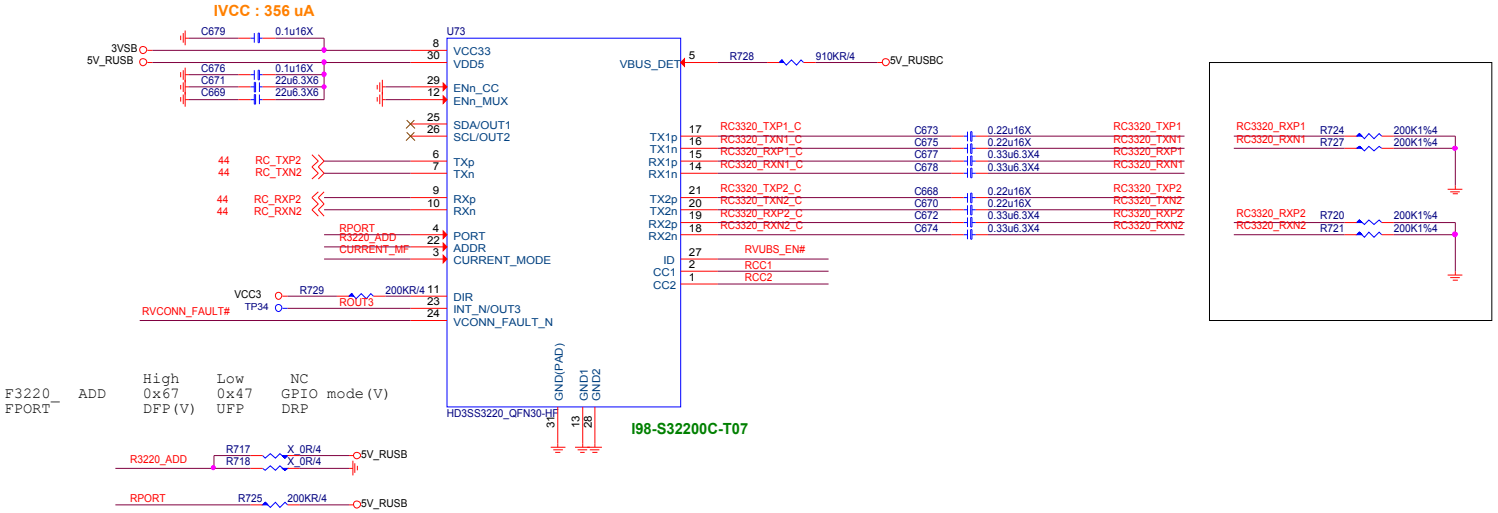
MS-7C91

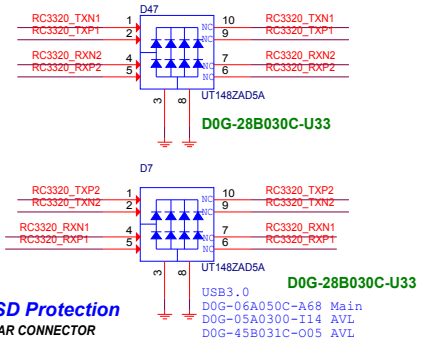
Size	Document Description	Rev
Custom	Rear USB3.1 Type A / Redrive	21

Date: Tuesday, April 21, 2020 Sheet 44 of 78

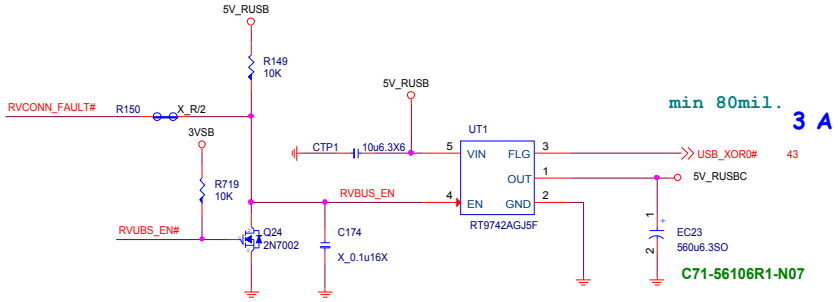
USB 3.1-Type-C

USB Type-C MUX with Configuration Channel (CC)

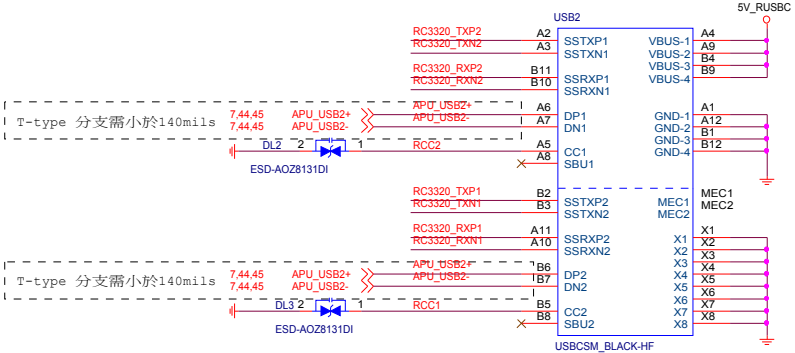




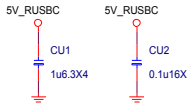
VBUS EN



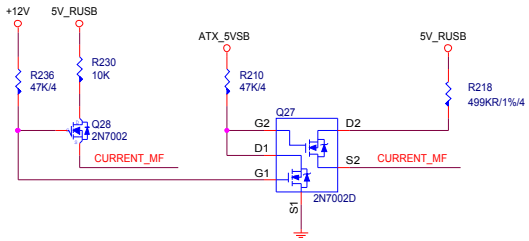
GEN2 3A



close to Type C Connector



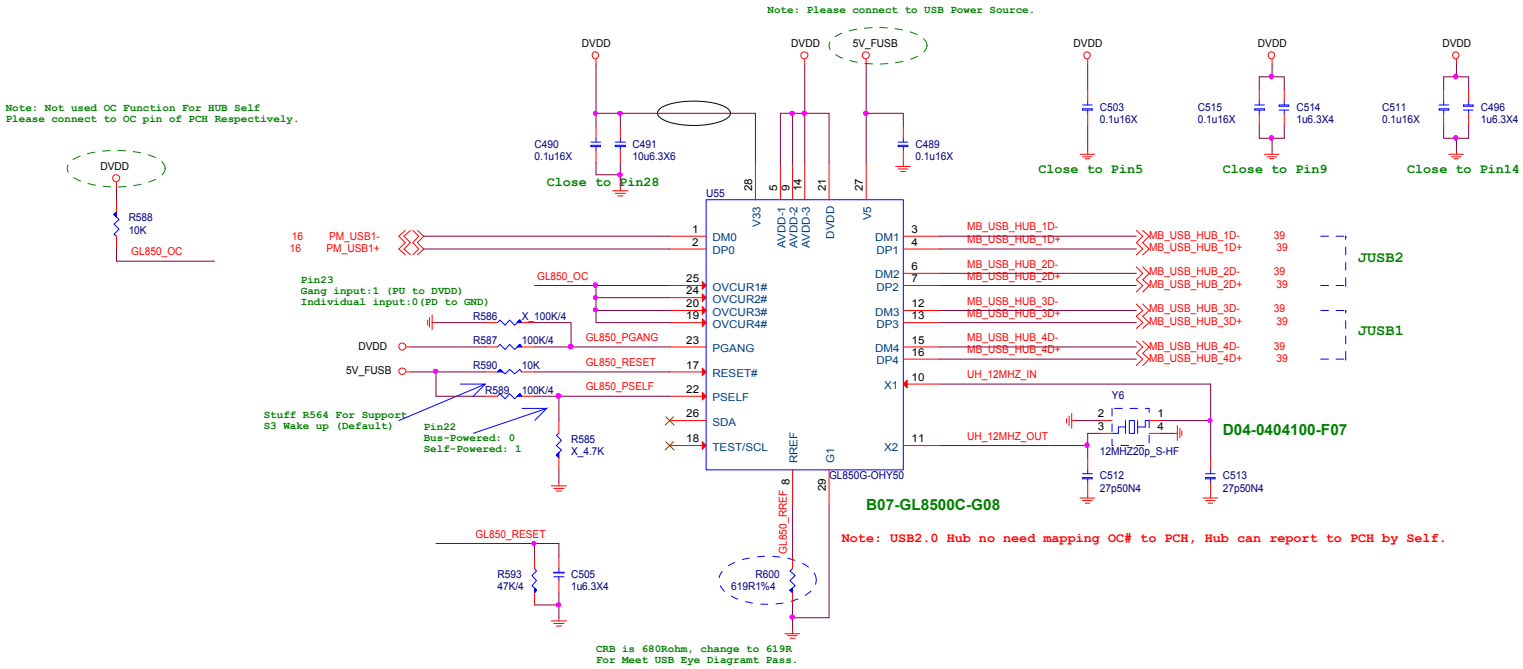
Current Mode



MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: Rear USB3.1 Type C / mux
Rev: 21	
Date: Tuesday, April 21, 2020	Sheet 45 of 78

GL850G USB2.0 HUB

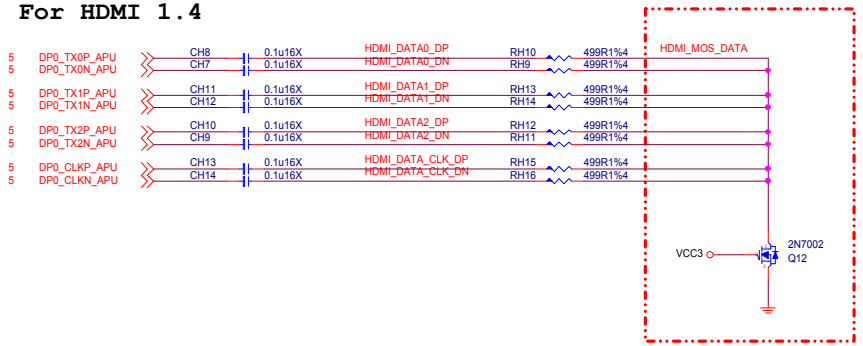
5V_FUSB



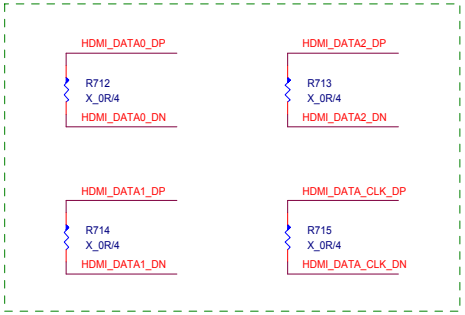
MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: GL850G	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 46 of 78	

HDMI CONNECTOR

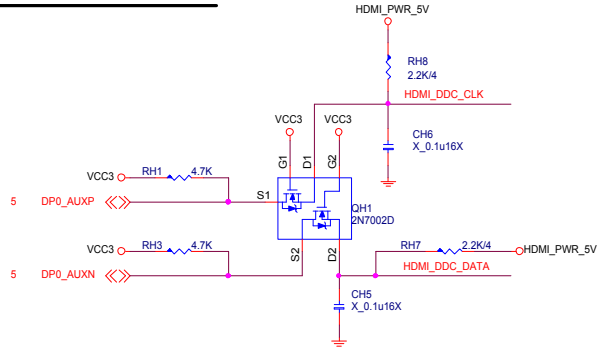
For HDMI 1.4



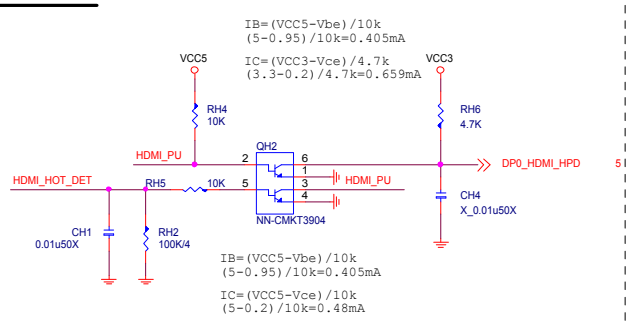
HDMI_MOS_DATA trace length <500mil
other platform please check design guide



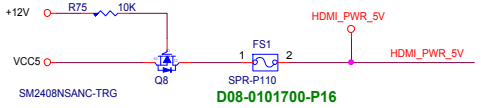
AUX Level Shifter



HPD Circuit



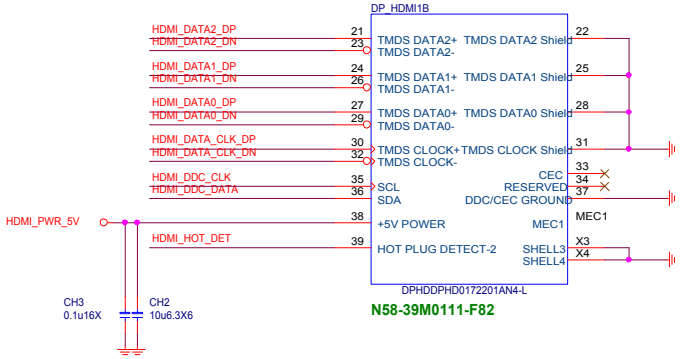
Connector Power



D08-0101700-P16

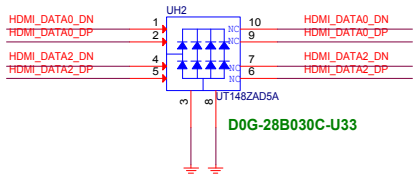
如果用DIODE SA測試電壓會不過

Connector

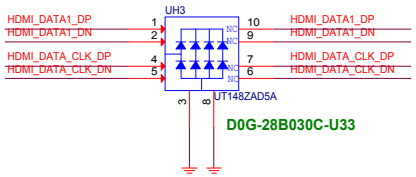


N58-39M0111-F82

For EMI

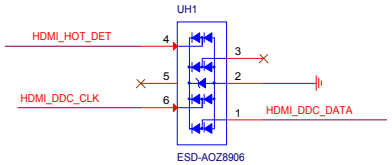


D0G-28B030C-U33



D0G-28B030C-U33

注意:耐壓5v零件

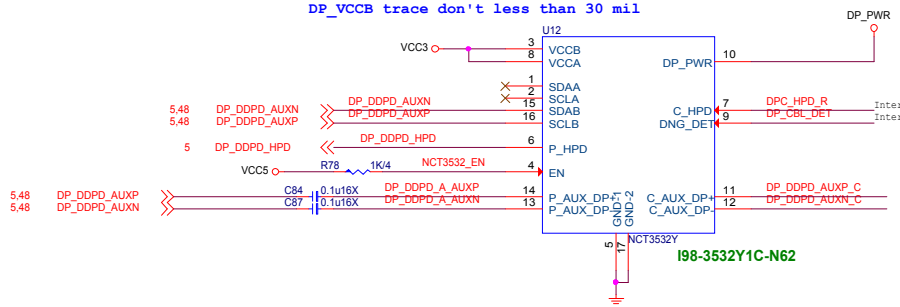


ESD-AOZ8906

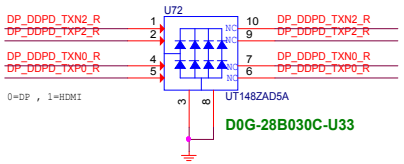
MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: HDMI	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 47 of 78	

500mA

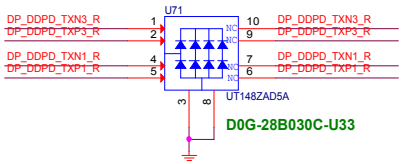
DP_VCCB trace don't less than 30 mil



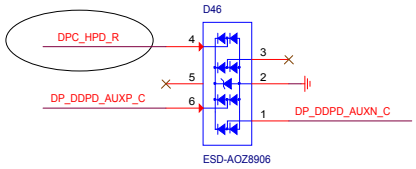
I98-3532Y1C-N62

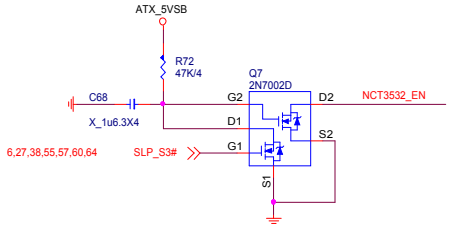


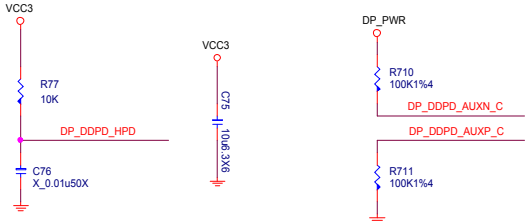
D0G-28B030C-U33

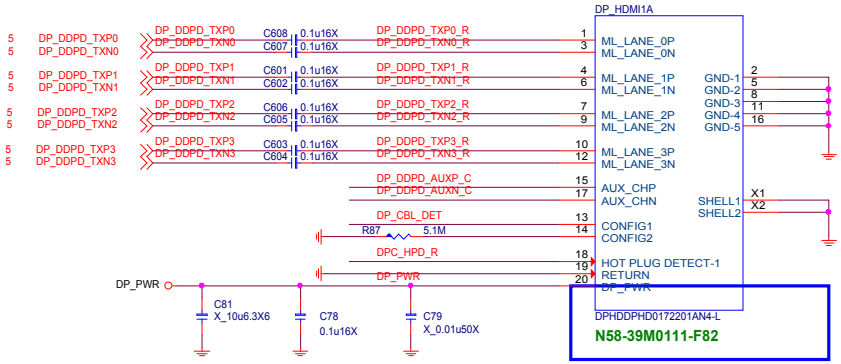


D0G-28B030C-U33





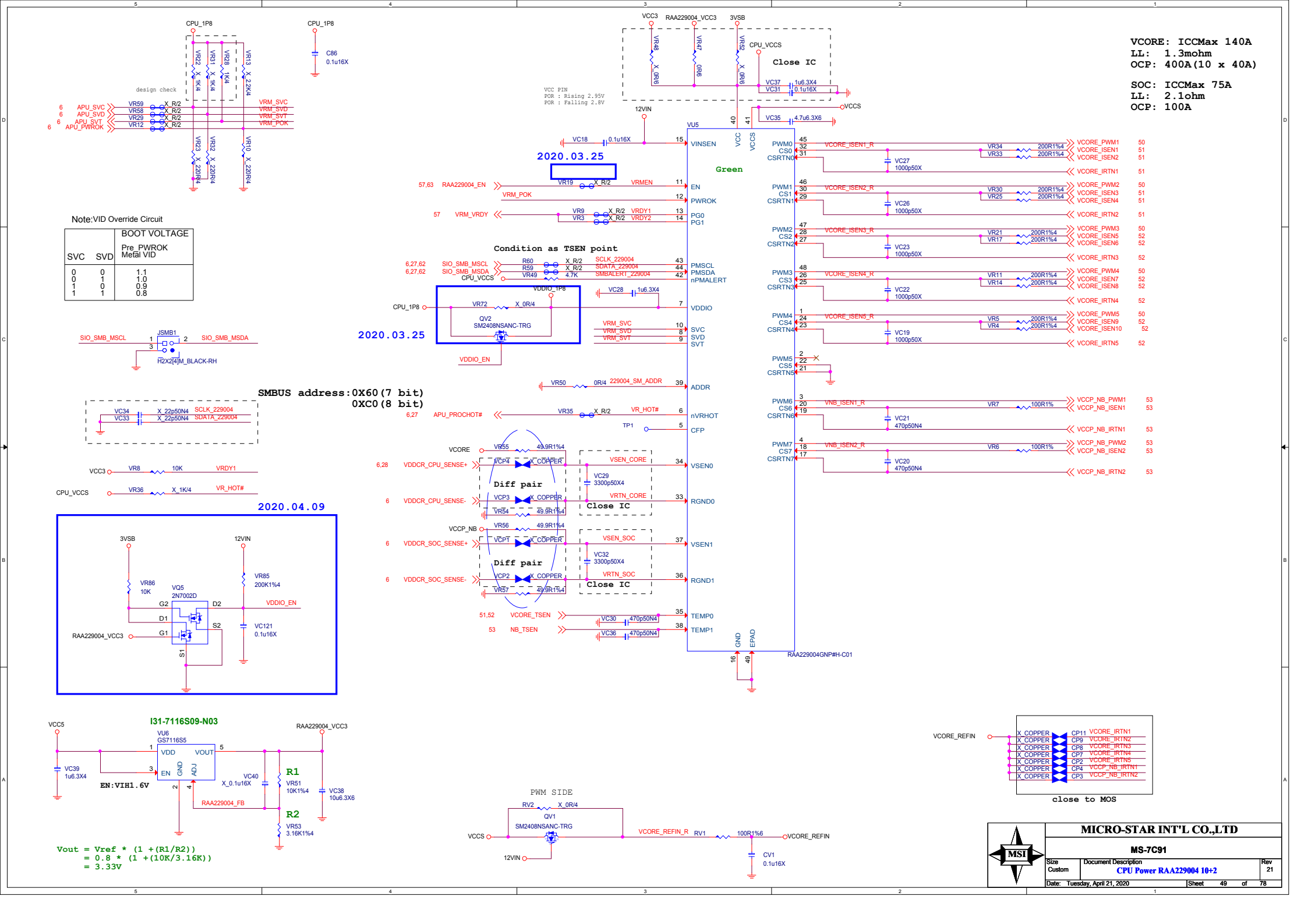




N58-39M0111-F82

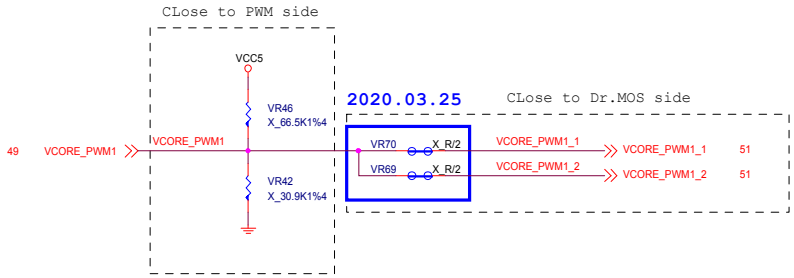
2020.04.13

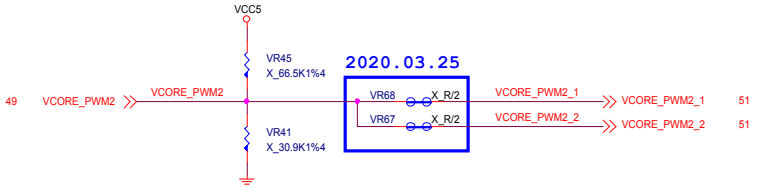
MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: DP	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 48 of 78	

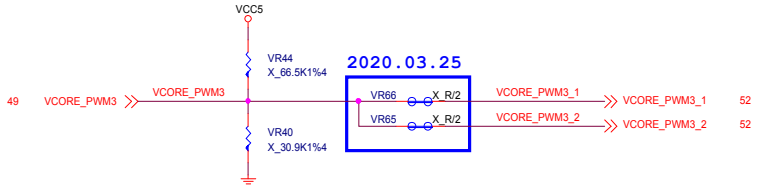

VCORE: ICCMax 140A
LL: 1.3mohm
OCP: 400A(10 x 40A)
SOC: ICCMax 75A
LL: 2.1ohm
OCP: 100A
Note:VID Override Circuit
SVC SVD BOOT VOLTAGE Pre_PWROK Metal VID
0 0 1.1
0 1 1.0
1 0 0.9
1 1 0.8
SMBUS address:0X60(7 bit)
0XC0(8 bit)
2020.03.25
2020.04.09
Close IC
Diff pair
Condition as TSEN point
RAA229004GNP#H-C01
I31-7116S09-N03
Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V
close to MOS
MICRO-STAR INT'L CO.,LTD
MS-7C91
CPU Power RAA229004 10+2
Date: Tuesday, April 21, 2020
Sheet 49 of 78

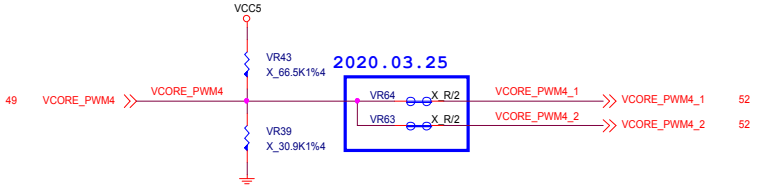
CPU_CORE Driver IC

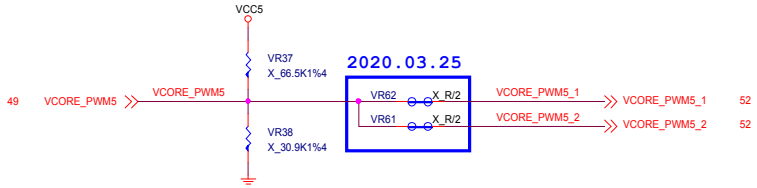
VCORE Double 10-PHASE









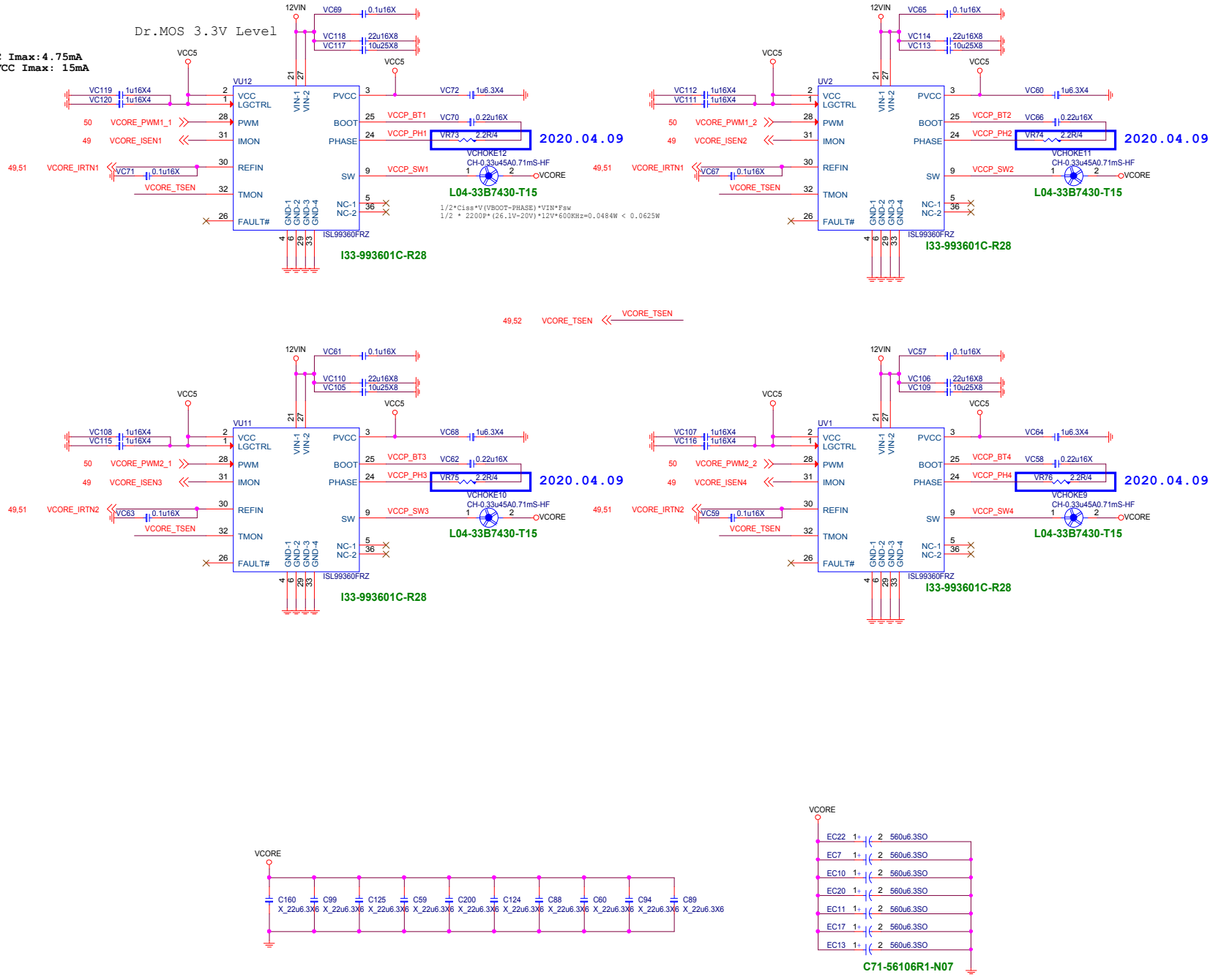


MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: CPU Power Phase Double IC SPS	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 50 of 78	

Vcore EDC Max 140A

Dr.MOS 3.3V Level

VCC Imax:4.75mA
IPVCC Imax: 15mA

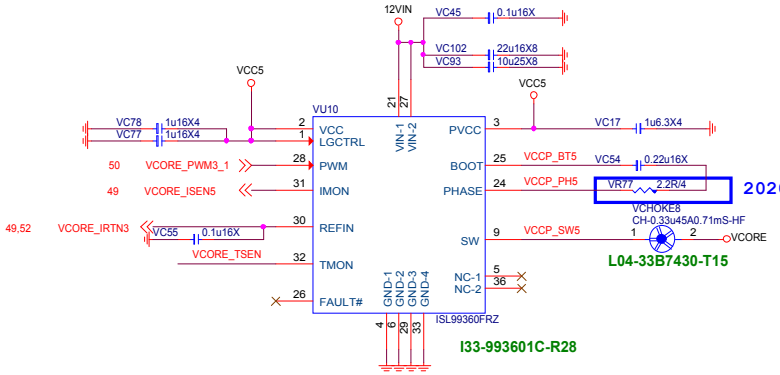


49,52 VCORE_TSEN

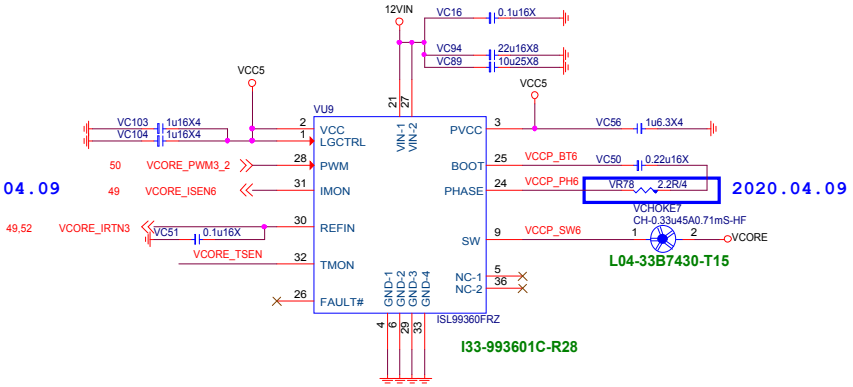
MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: CPU Power Vocre Phase 1- 4	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 51 of 78	

Dr.MOS 5V Level

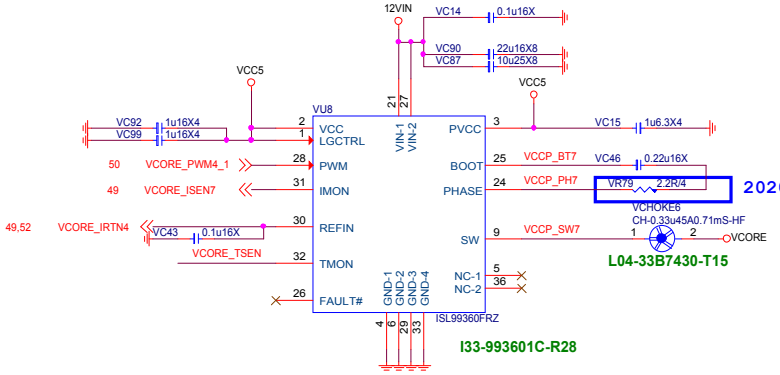
49,51 VCORE_TSEN <<< VCORE_TSEN



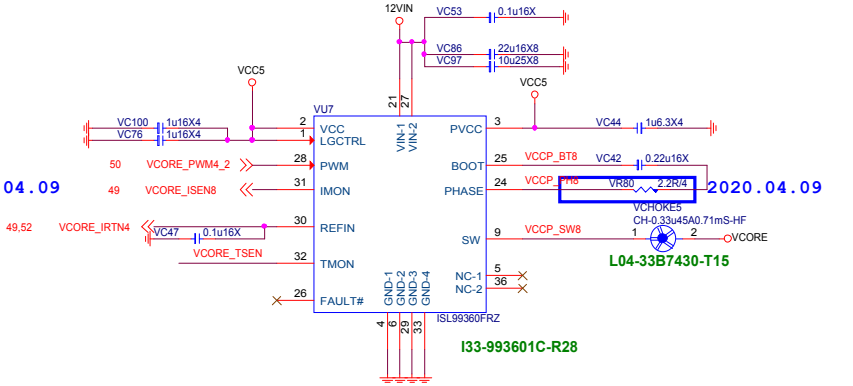
2020.04.09



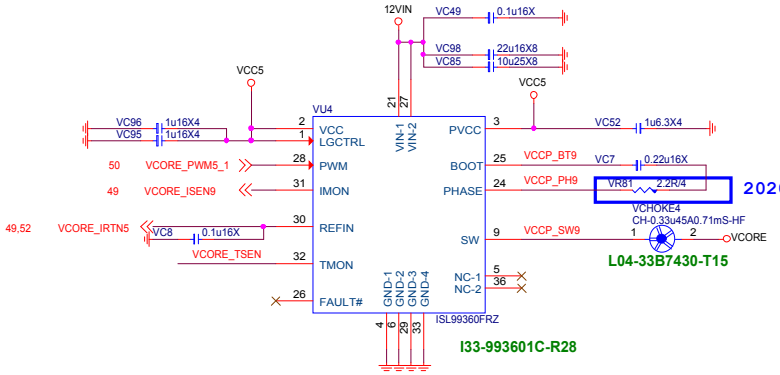
2020.04.09



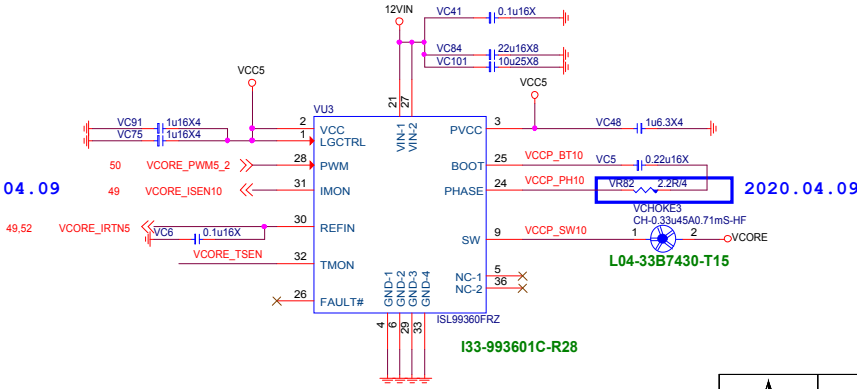
2020.04.09



2020.04.09



2020.04.09



2020.04.09

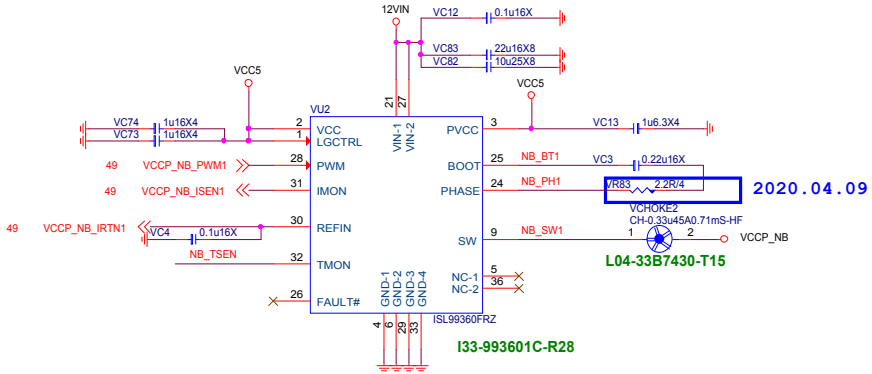
MICRO-STAR INT'L CO.,LTD

MS-7C91

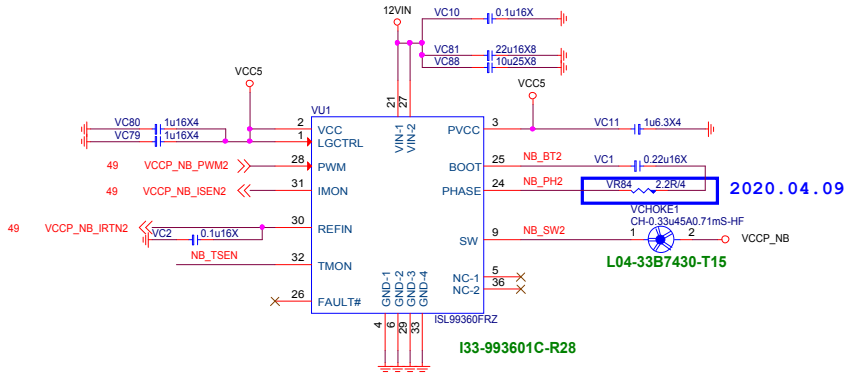
Size	Document Description	Rev
Custom	CPU Power Vocre Phase 6 - 10	21

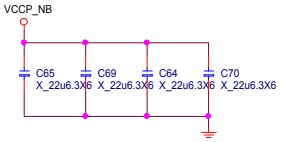
Date: Tuesday, April 21, 2020 Sheet 52 of 78

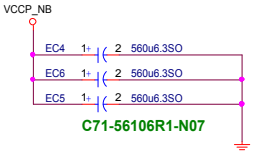
Dr.MOS 3.3V Level



49 NB_TSEN





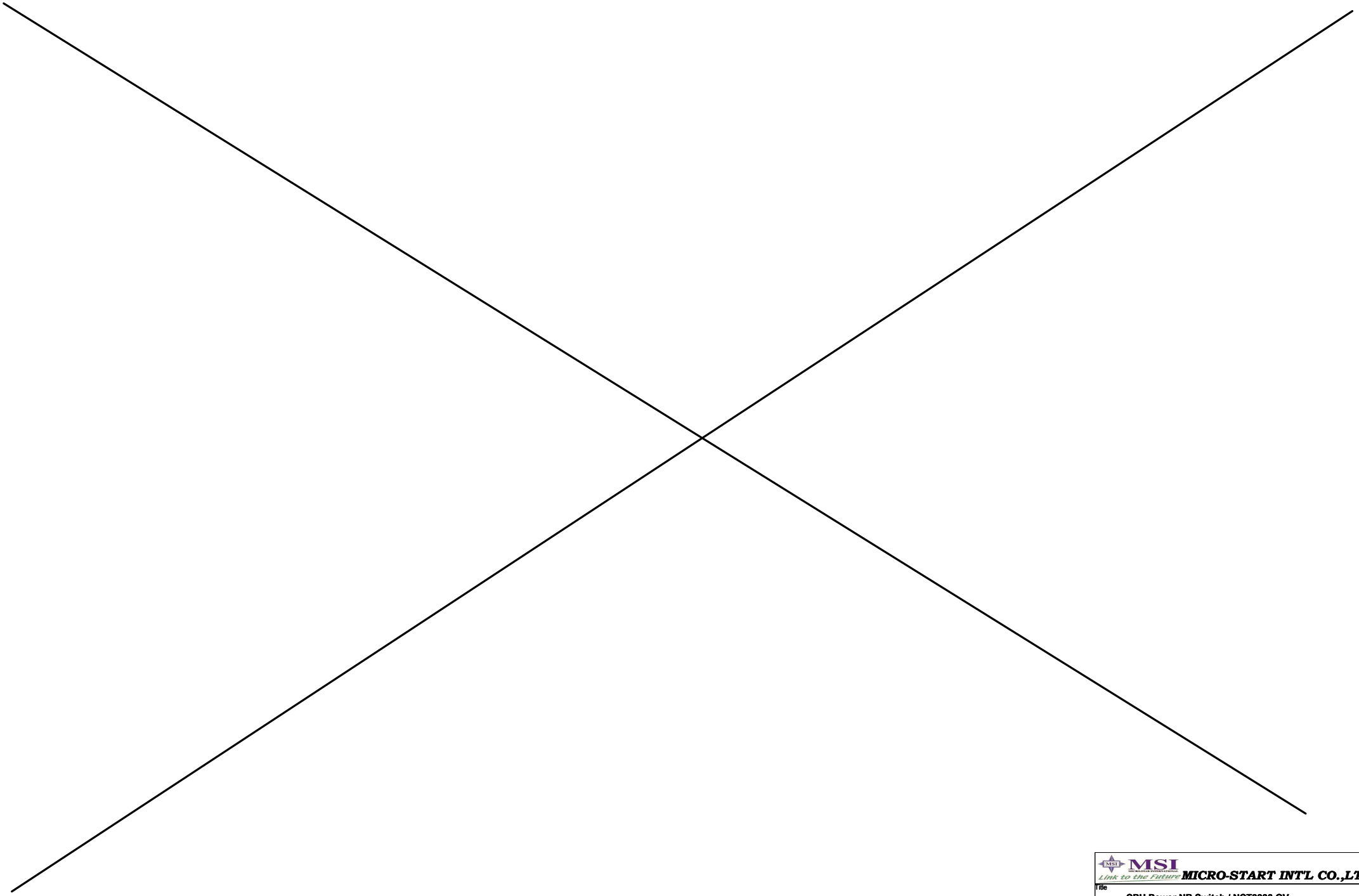


MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	CPU Power NB Phase 1-2	21

Date: Tuesday, April 21, 2020 Sheet 53 of 78



MSI MICRO-STAR INTERNATIONAL
Link to the Future
MICRO-START INT'L CO.,LTD.

Title: CPU Power NB Switch / NCT3933 OV		
Size: Custom	Document Number: MS-7C51	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 54 of 78	

CPU 1.8V S5

CPU 1.8V_S5@0.5A
CPU_VDDP_S5@1A
AUDIO1.8V@0.25A

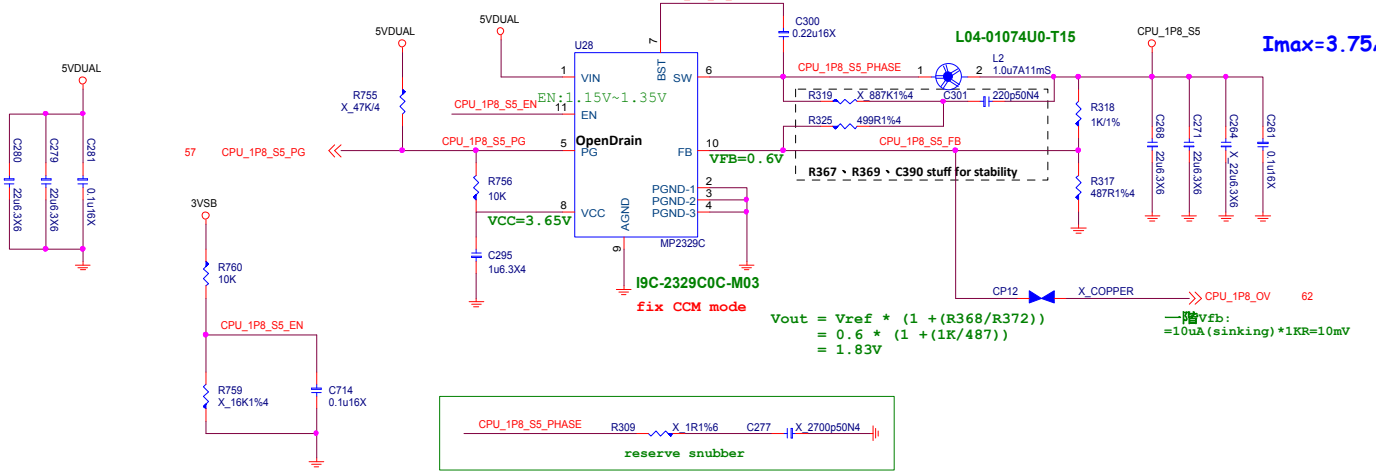
Continuous Conduction Mode (CCM)

Input Current = (6.5A*1.8V)/5V/0.8 = 3A

CPU_1P8_BST、CPU_1P8_BST_R >50 mils.

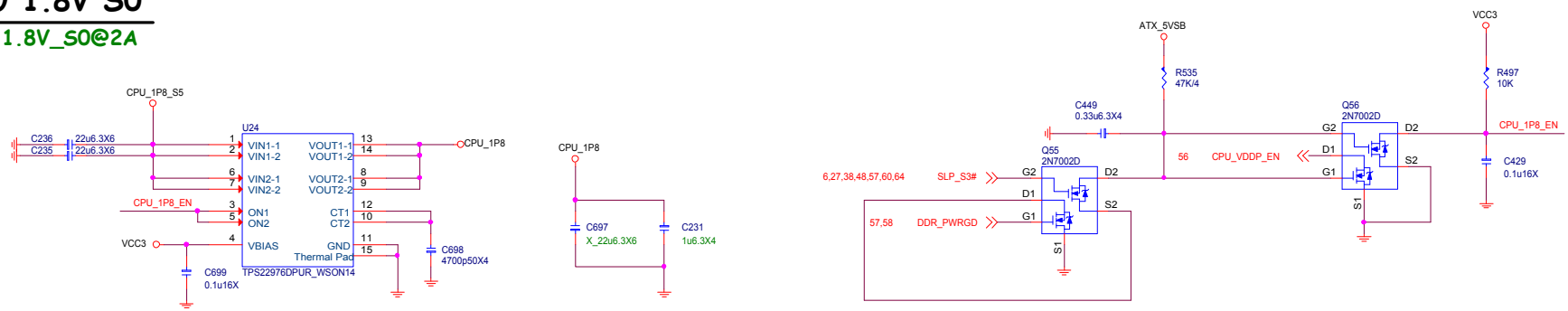
OCP = 6.5A

Imax=3.75A(S5+S0)

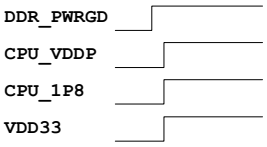


CPU 1.8V S0

CPU 1.8V_S0@2A



Adijustable Rise Time
SR = 0.42*CT+66
SR is the slew rate in (μs/V)
CT is constant value on CT pin (in pF)
The units for the constant 66 is in (μs/V)

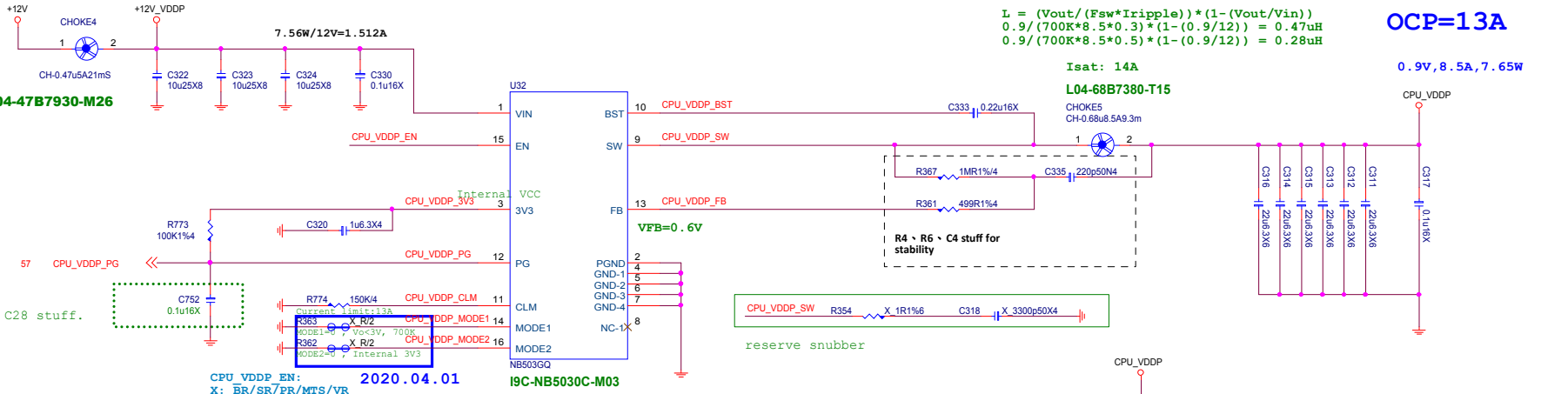


MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: CPU Power 1.8_S0 / S5	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 55 of 78	

CPU_VDDP_S0

0.9V@S0:8.5A

```
Input Current = (13A*0.9V)/12V/0.8 = 1.22A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A
```




```
L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
0.9/(700K*8.5*0.3)*(1-(0.9/12)) = 0.47uH
0.9/(700K*8.5*0.5)*(1-(0.9/12)) = 0.28uH
```

OCP=13A

Isat: 14A

L04-68B7380-T15

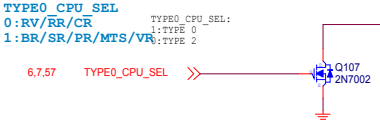
0.9V,8.5A,7.65W

20180822
fix PG glitch when VCC3 ramp up, C28 stuff.

CPU_VDDP_EN:
X: BR/SR/PR/MTS/VR
O: RV/RR/CR

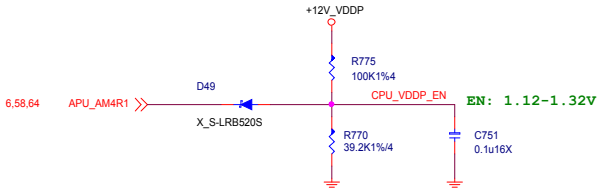
2020.04.01

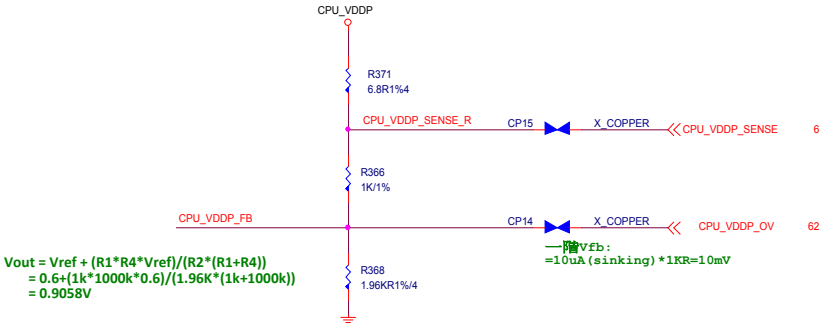
TYPE0_CPU_SEL
0:RV/RR/CR
1:BR/SR/PR/MTS/VR



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	0
NA		0	0
SR	2	CPU VDDP NOT SUPPORT TYPE2	
RV/ZP	3	1	0
MTS	4	CPU VDDP NOT SUPPORT TYPE4	
RR	5	1	0
VM	6	CPU VDDP NOT SUPPORT TYPE6	
CR	7	1	0

SPEC no Support



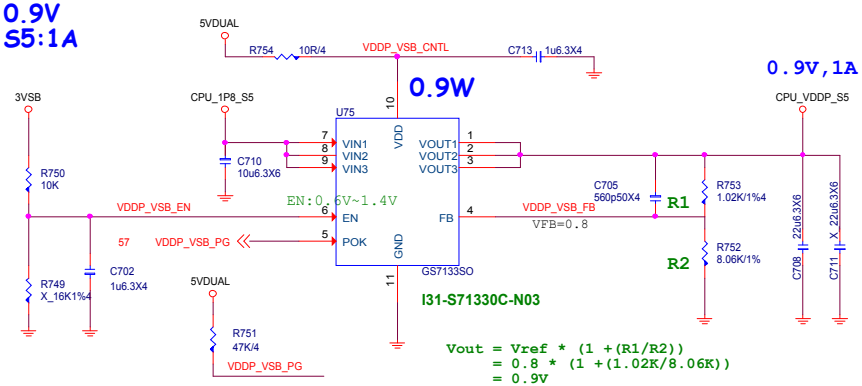



```
Vout = Vref + (R1*R4*Vref)/(R2*(R1+R4))
     = 0.6+(1k*1000k*0.6)/(1.96K*(1k+1000k))
     = 0.9058V
```

一階VFb:
=10uA(sinking)*1KR=10mV

CPU_VDDP_S5

0.9V
S5:1A




```
Vout = Vref * (1 +(R1/R2))
     = 0.8 * (1 +(1.02K/8.06K))
     = 0.9V
```

MICRO-STAR INT'L CO.,LTD

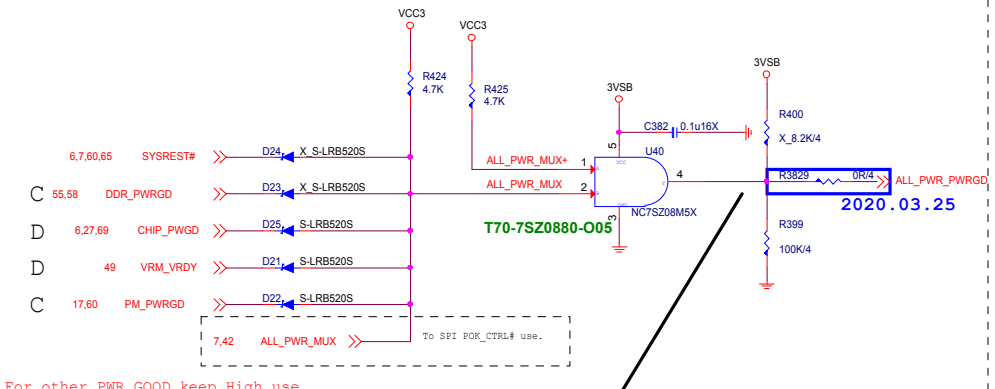
MS-7C91

Size	Document Description	Rev
Custom	CPU Power VDDP - NB503	21

Date: Tuesday, April 21, 2020 Sheet 56 of 78

ALL POWER GOOD MUX

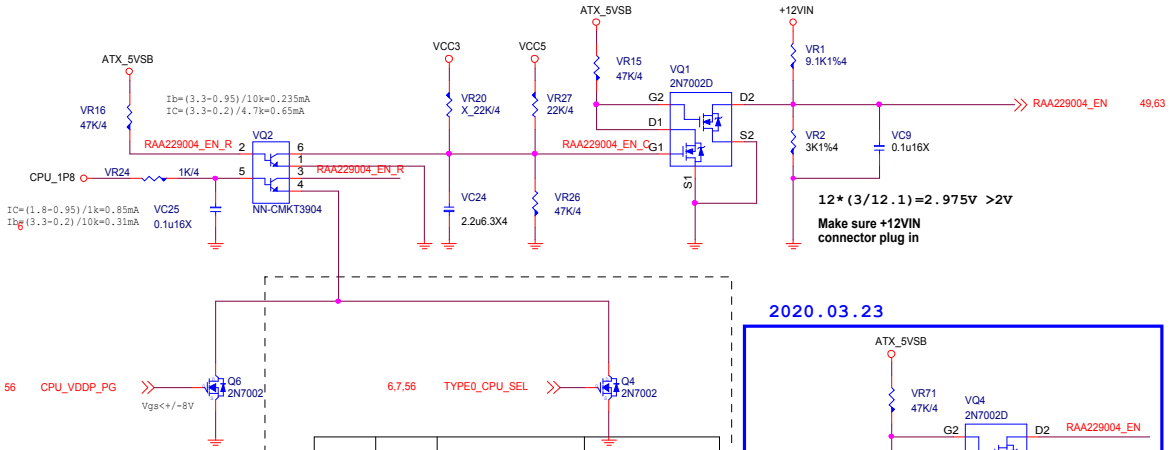
S0 PG

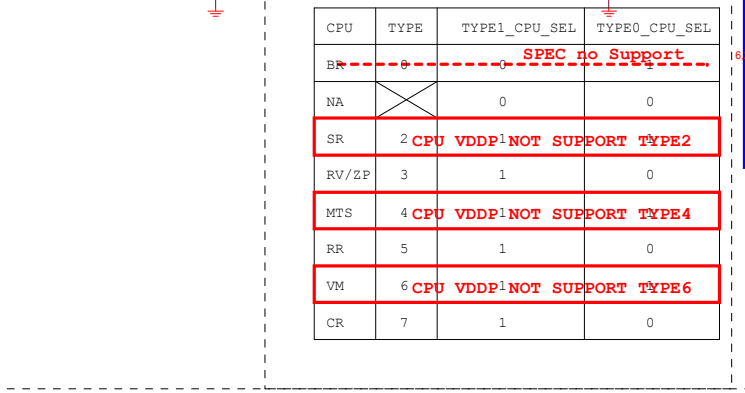


When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

VRM_Enable circuit

2020.03.23
D2 Removed

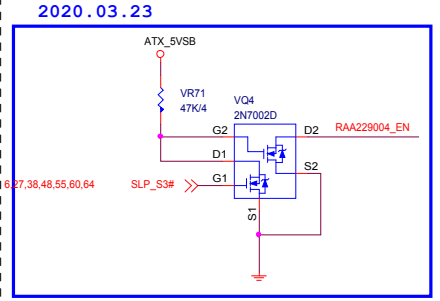




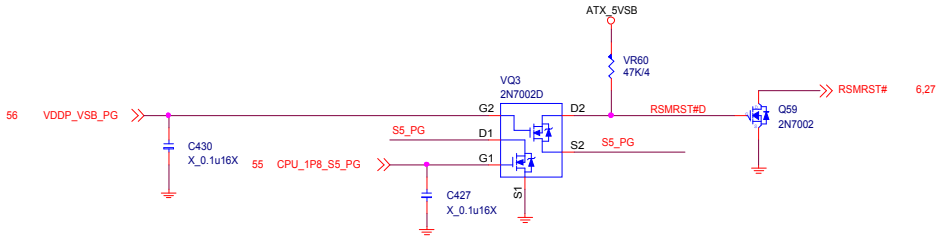
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	CPU VDDP1 NOT SUPPORT TYPE2	
RV/ZP	3	1	0
MTS	4	CPU VDDP1 NOT SUPPORT TYPE4	
RR	5	1	0
VM	6	CPU VDDP1 NOT SUPPORT TYPE6	
CR	7	1	0

SPEC no Support

2020.03.23



S5 PG



MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	VRM PWRGD	21

Date: Tuesday, April 21, 2020 Sheet 57 of 78

DDR4_1.2V@28.7A

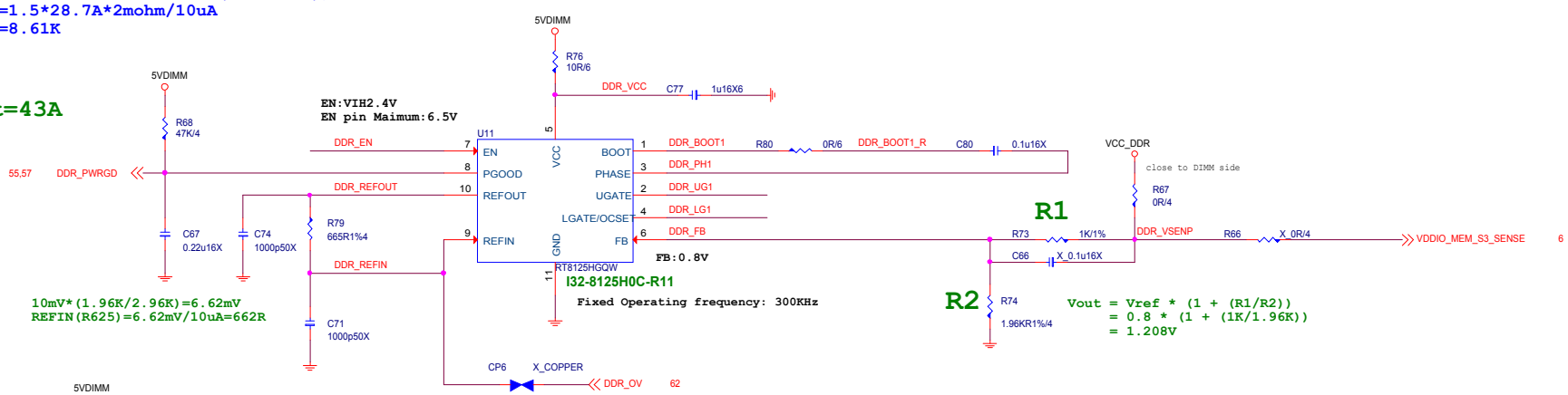
18A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT

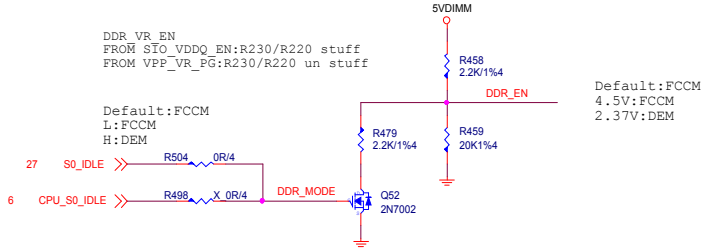
Rocset=1.5*Imax*Rdson(Low side)/Iocset
=1.5*28.7A*2mohm/10uA
=8.61K

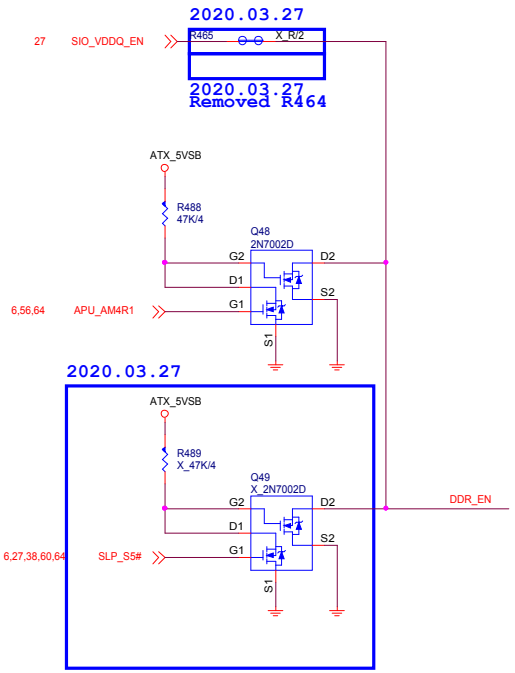
OCP = 43.05A; Choke Isat=43A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
R639 = 1.5 * 28.7 * 2mohm / 10uA
R639 = 8.61K

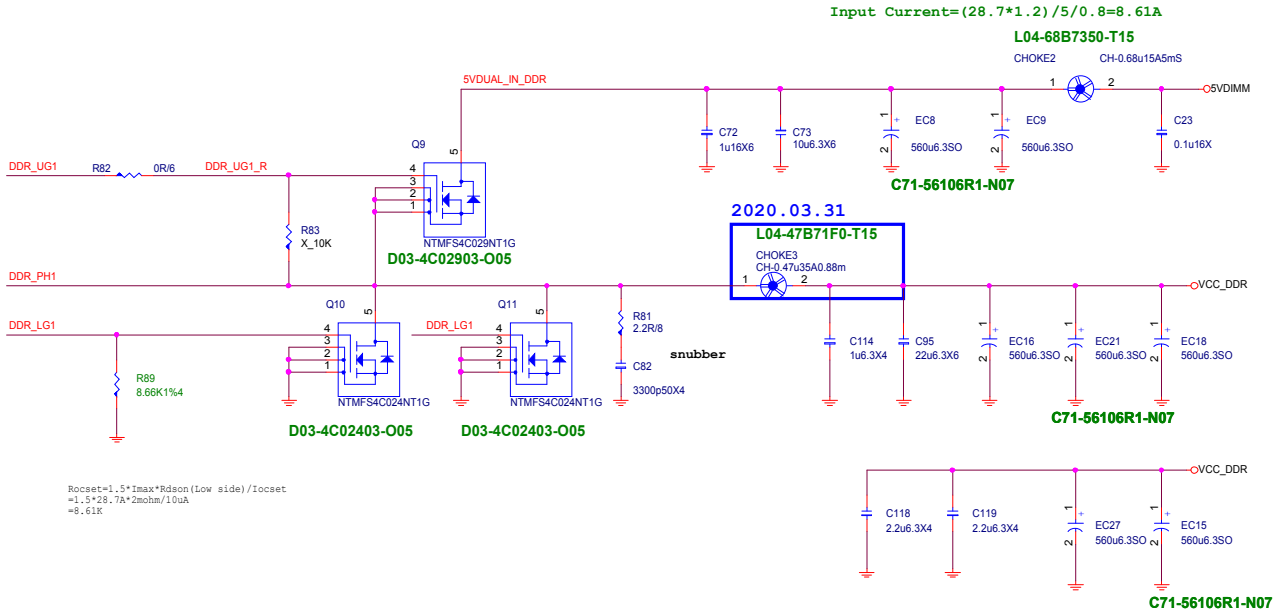
Rdson(Low Side) 5V
D03-4C02403-O05:3.3 ~ 4mohm







Input Current=(28.7*1.2)/5/0.8=8.61A



MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	DDR Power - 8125H	21

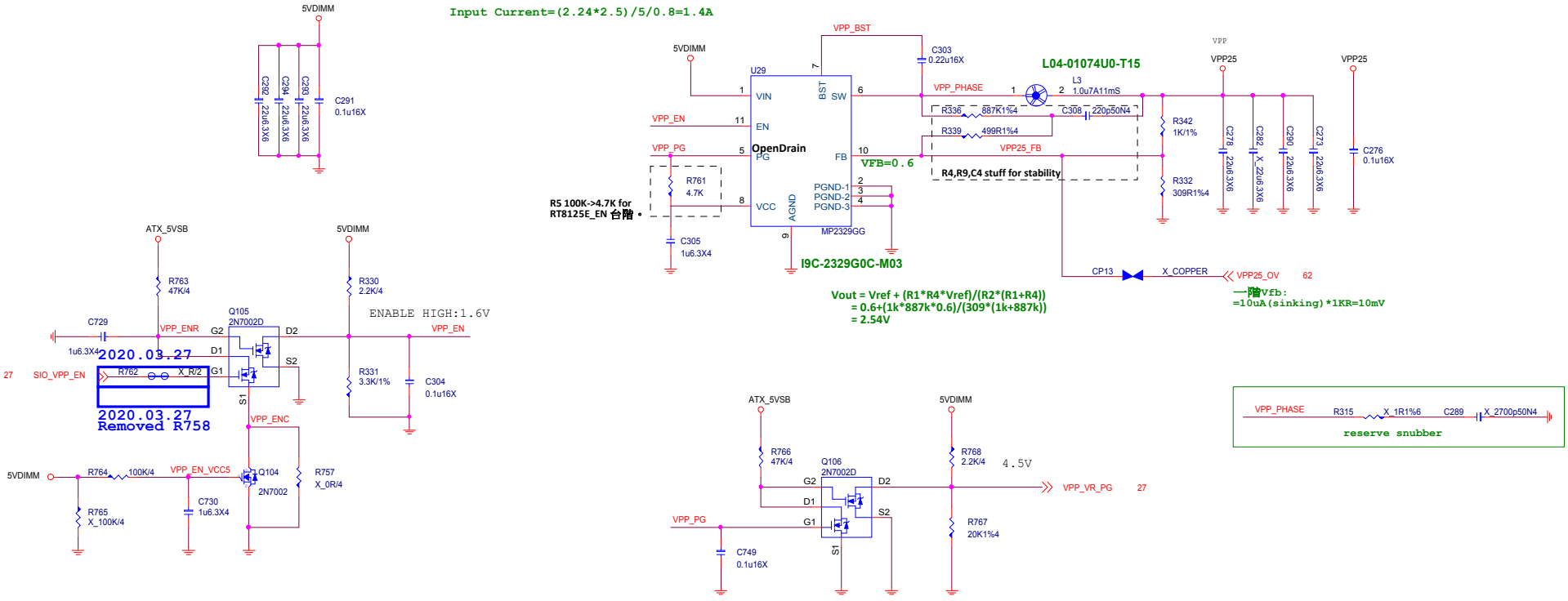
Date: Tuesday, April 21, 2020 Sheet 58 of 78

4DIMM : VPP25

2.5V@2.24A

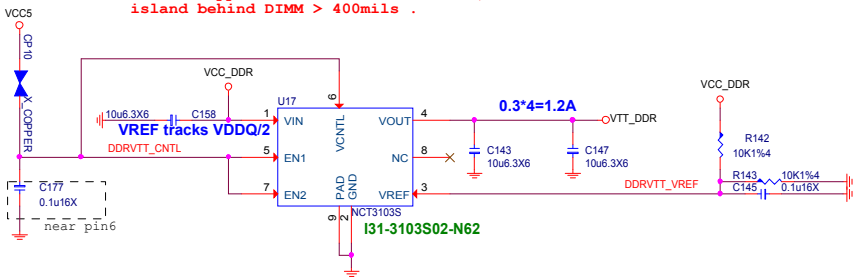
VPP_BST>50 mils.

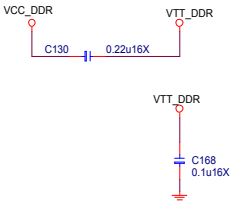
Input Current=(2.24*2.5)/5/0.8=1.4A



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .





MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: DDR VPP25 / VTT	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 59 of 78	

FOR Promontory 1.05V_S0

1.05V
S0:5.5A

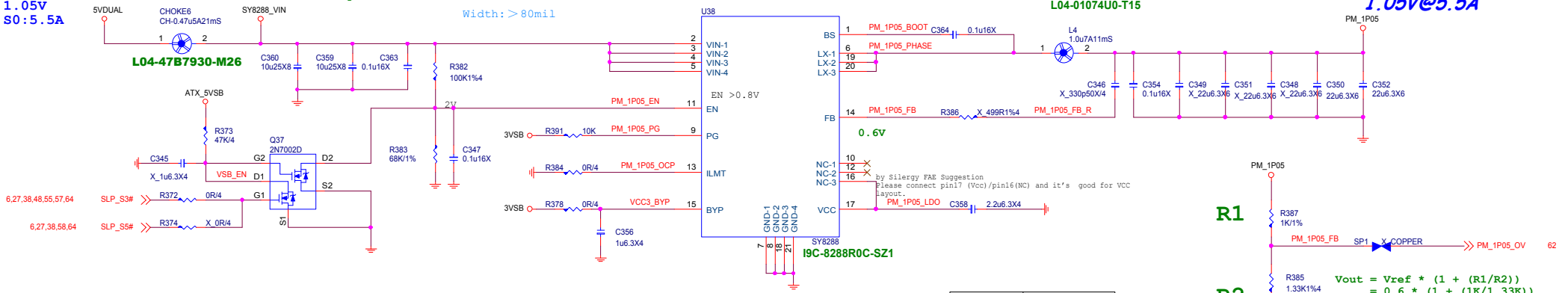
Input Current= (OCP8A*1.05V)/5V/0.8=2.1A

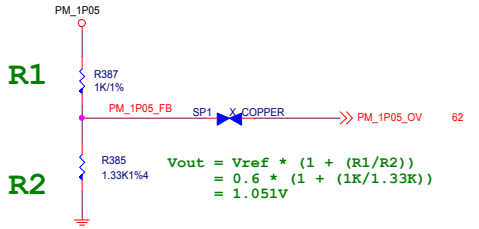
Width: > 80mil

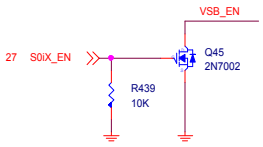
L04-47B7930-M26

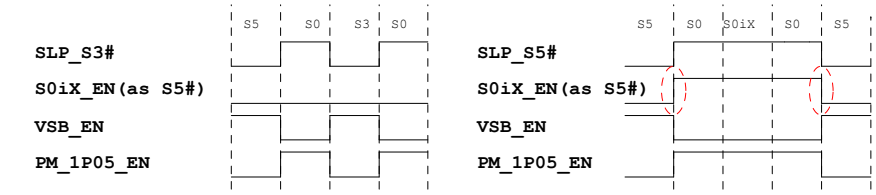
L04-01074U0-T15

OCP=8A
1.05V@5.5A





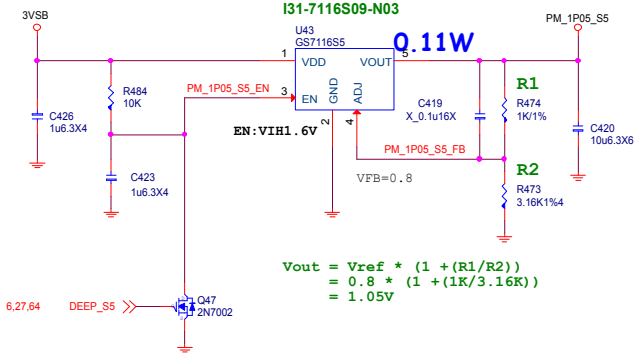




ILIMT	OCP
0	8A
floating	12A
1	16A

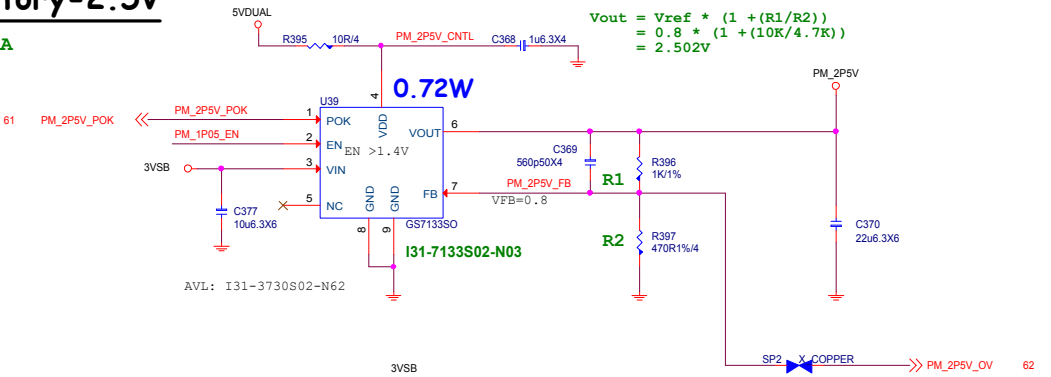
FOR PROM PM_1P05_S5

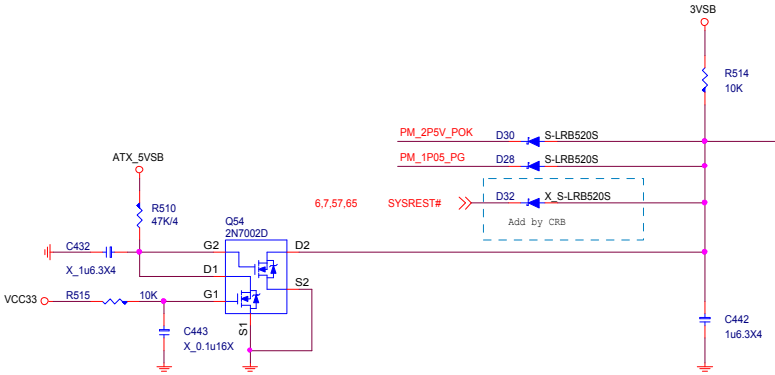
1.05V@0.05A

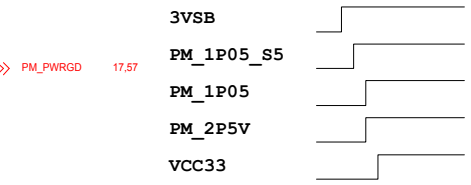


Promontory-2.5V

2.5V@900mA



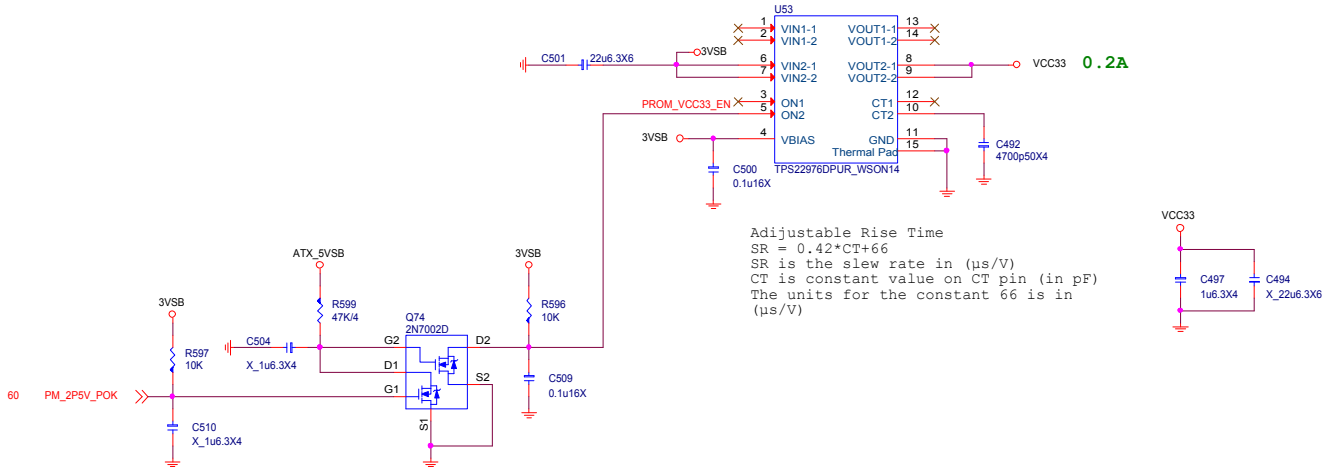




MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: PM - SY8288/PM_1P05/PM_2P5V	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 60 of 78	

PROM VCC33

VCC33@0.2A



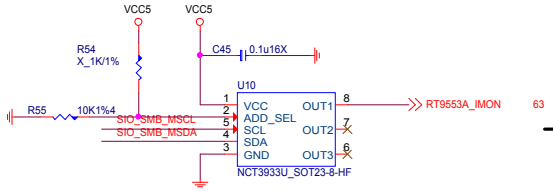
MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: PM - TPS22976DPUR_WSON14	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 61 of 78	

Over Voltage Control IC

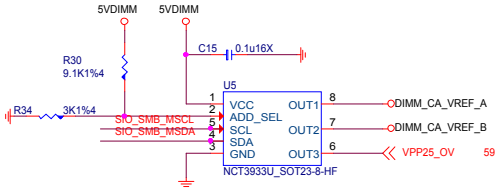
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

0x2A:RH=OPEN,RL=10K



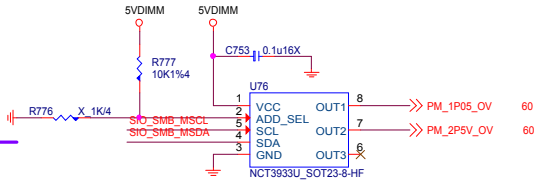
0x28:RH=9.1K,RL=3K



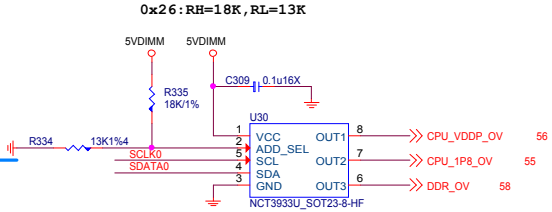
6,27,49 SIO_SMB_MSCL
6,27,49 SIO_SMB_MSDA

SIO_SMB_MSCL
SIO_SMB_MSDA

0x20:RH=10K,RL=OPEN



0x26:RH=18K,RL=13K

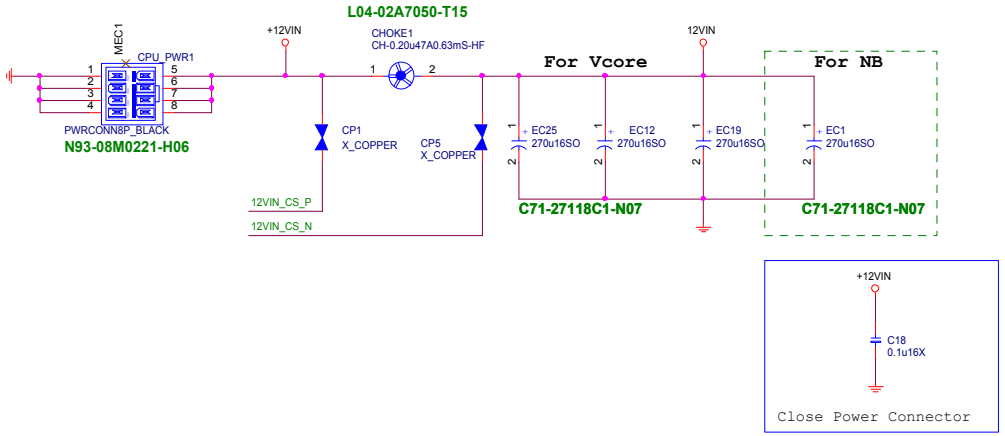


6,11,24 SCLK0
6,11,24 SDATA0

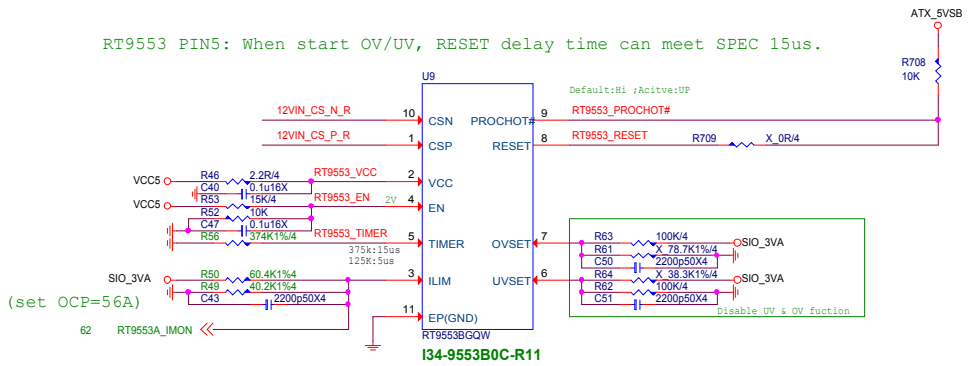
SCLK0
SDATA0

MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: OV Control - NCT3933	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 62 of 78	

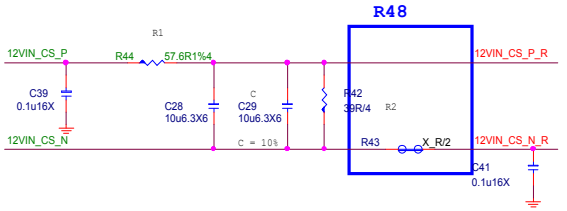
CPU POWER CONNECTOR



RT9553B CURRENT SENSE



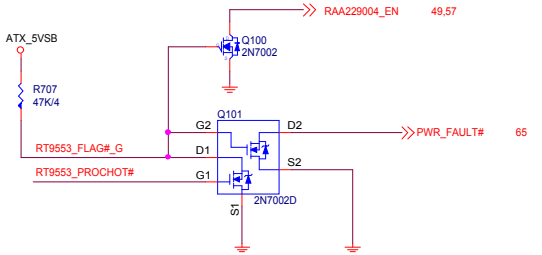
2020.03.25



$$\Delta VILIM = 10uA * [(60.4K * 40.2K) / (60.4K + 40.2K)] = 226mV$$

$$Isense = VILIM / 100 * Rsense$$

$$\Delta Isense = 226mV / 100 * 0.63m = 3.58A$$



Vcore			
D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	2	> output Vcore
D	=	0.166667	
I o = Icore(max)*0.8			
I core(max)	=	200	> Vcore current
I avg.	=	160	A
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	10	phase
I ripple	=	5.962848	A
How many pcs. Of Cap.			
I ripple(cap)	=	4700	m A
COETEMP	=	1	
Input Cap.	=	2	pcs.

SOC			
D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.55	> output Vcore
D	=	0.129167	
I o = Icore(max)*0.8			
I core(max)	=	75	> Vcore current
I avg.	=	60	A
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	2	phase
I ripple	=	10.06153	A
How many pcs. Of Cap.			
I ripple(cap)	=	4700	m A
COETEMP	=	1	
Input Cap.	=	3	pcs.

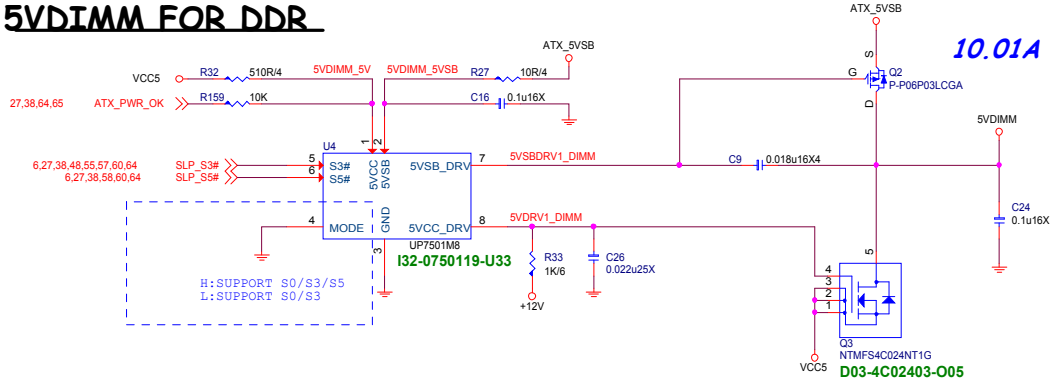
MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	OCP 12VIN - RT9533B	21

Date: Tuesday, April 21, 2020 Sheet 63 of 78

5VDIMM FOR DDR

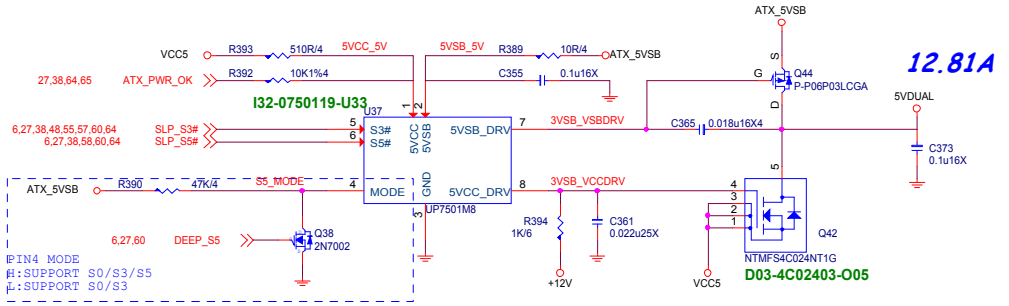


10.01A

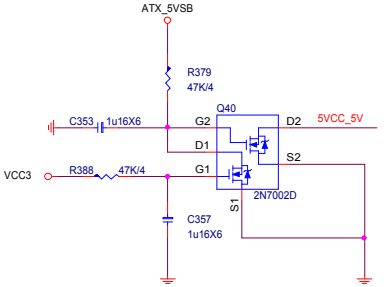
VCC_DDR=8.61A
VPP25=1.4A

5VDUAL For 3VSB/CPU1.8V/VDDP

LDOVDD=93.6mA
CPU_1P8_S5 VIN=3A
PM_1P05 VIN=2.1A
3VSB = 4.71A
LED_VCC5 = 3A



12.81A

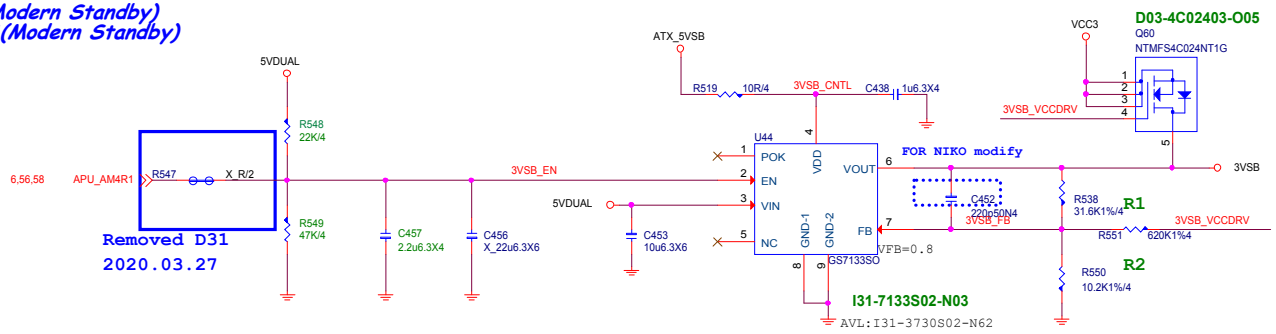


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

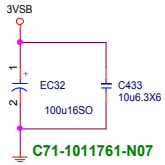
3VSB cost down

3.3V@4.305A

CPU:VDD_33_S5=0.25A
CHIP:VDD_33_S5=0.07A
PCIE=(375mA*5)=1.875A
M.2WIFI= 0.78A
RT8111H LAN=0.18A
PM_1P05_S5 :0.05A
PM_2P5V :0.9A(Modern Standby)
PCH VCC33 :0.2A(Modern Standby)



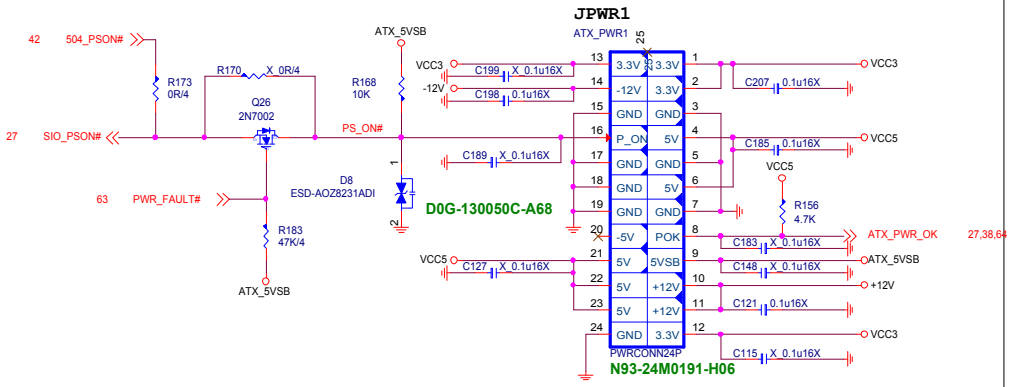
4.305A

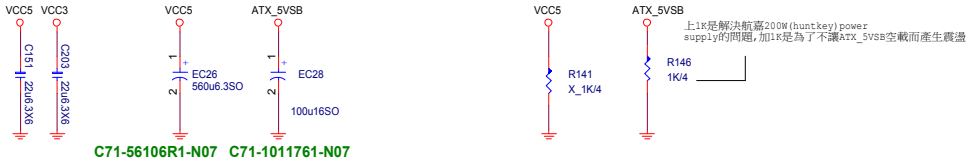


Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(31.6K/10.2K))
= 3.328V

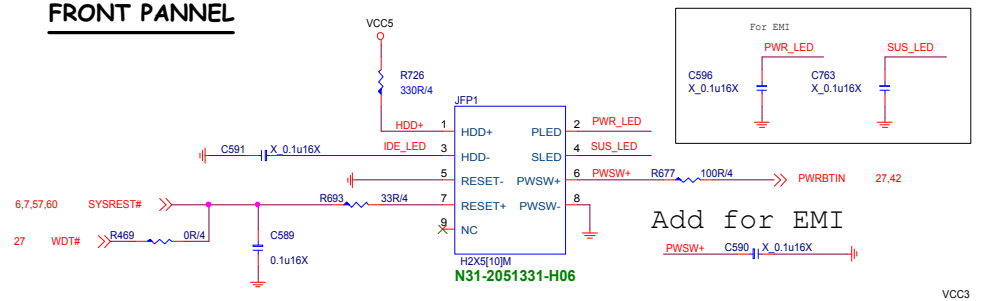
MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: ACPI - 5VDIMM / 3VSB	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 64 of 78	

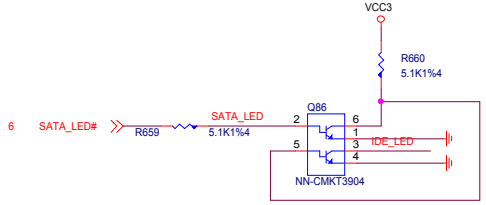
ATX POWER CONNECTOR

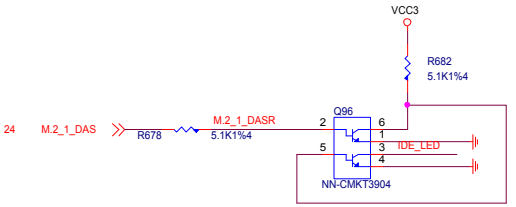


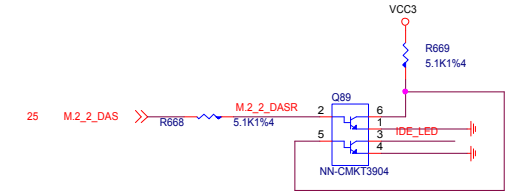


FRONT PANNEL



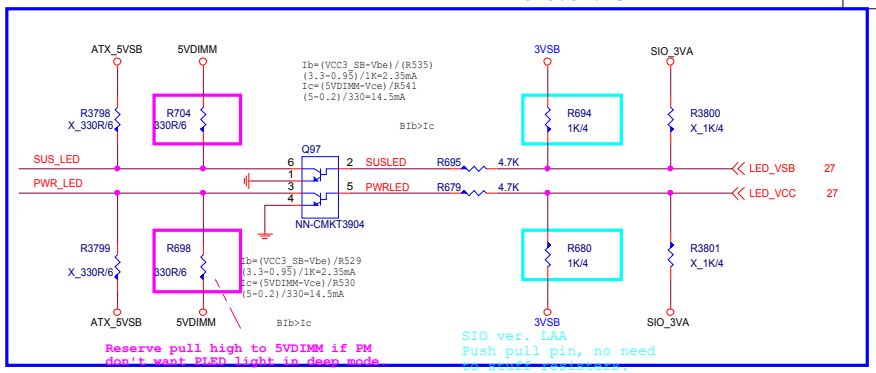


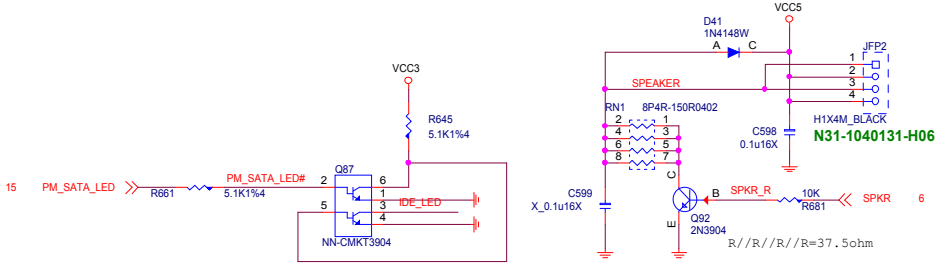




LED (for NCT6687D-R)

2020.04.13





Voltage Mearsure Point

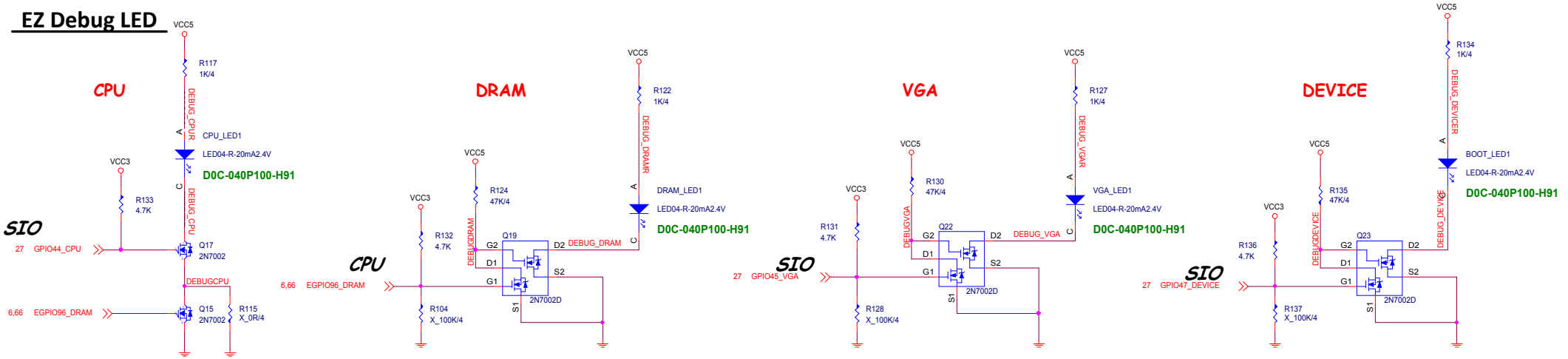
MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	ATX power - FrontPanel / EMI	21

Date: Tuesday, April 21, 2020 Sheet 65 of 78

EZ Debug LED



LED GPIO	GPIO44	EGPIO96	GPIO45	GPIO47
亮	OPEN-Drain	GPO LOW	GPO LOW	GPO LOW
滅	GPO LOW	GPO HIGH	OPEN-Drain	OPEN-Drain

default Input

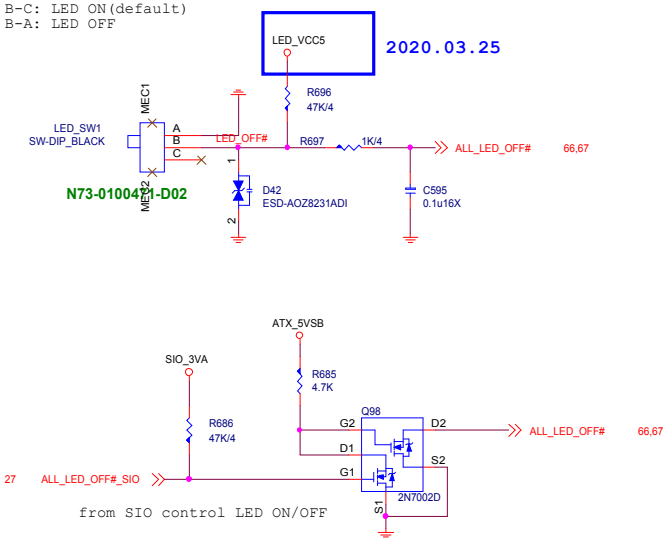
LED亮燈時同時將CPU LED關掉

LED_SW1 FORM SIO

D0C-040P100-H91/D0C-040S500-E07

LED_SW1 for ALL LED OFF

B-C: LED ON(default)
B-A: LED OFF



MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: LED - EZ DEBUG / AMP
Rev: 21	
Date: Tuesday, April 21, 2020	Sheet 66 of 78

48 PIN LED MCU

If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.

ADDRESS:0X52

2020.03.26
R806/R807

U59
NUC126NE4AE

PWM1 for JRGB1
RGB LED STRIPLINE USED

PWM3 for Others
According to demand configuration

PWM2 for JRGB2
RGB LED STRIPLINE USED

PIN1 for JPIPE1 & JRAINBOW1

PIN44 for JRAINBOW2

COM1~8 for PWM3
According to demand configuration.
Can configuration COM1~8,
To achieve 8 group Non-synchronized onboard LED control.

COM9~13 for PWM2
According to demand configuration.
If SPEC. don't have JRGB2,
Can configuration COM9~13,
To achieve 5 group Non-synchronized onboard LED control.

PS. COM1 is the first action block, next is COM2, and so on.

Pin15,16 can configure to master smbus if spec requirement.

detect JRGB 12V

2020.03.25

C1822 & C1823 near AVDD Pin. C1820 & C1821 near VDD Pin.
C1824 near VBAT Pin.
C1827 & C1828 near VDDIO & USB_VBUS Pin.

Clear MCU Circuit

Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2

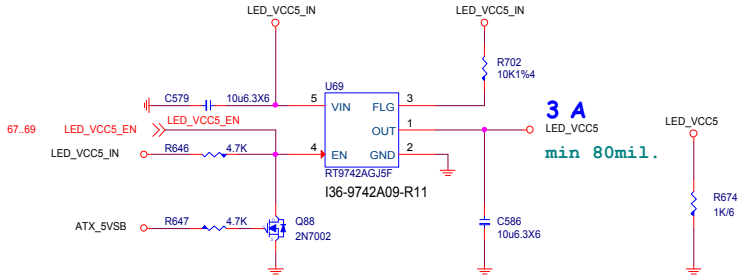
MICRO-STAR INT'L CO.,LTD

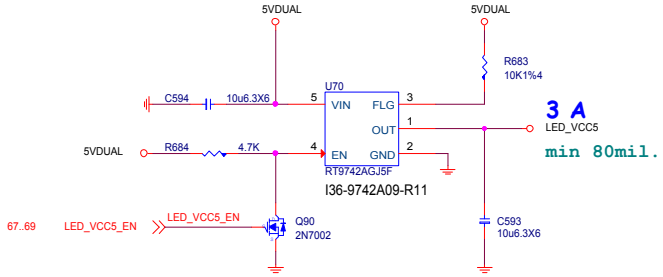
MS-7C91

Size: Custom | Document Description: MCU - LED Control | Rev: 21

Date: Tuesday, April 21, 2020 | Sheet 67 of 78

EXTERNAL POWER INPUT

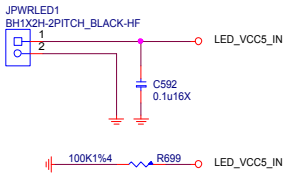




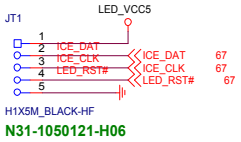
External Power

2A Connector

N32-1020CB1-H06

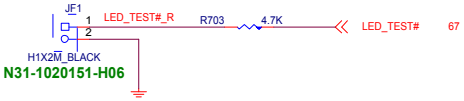


JT1 for FW update



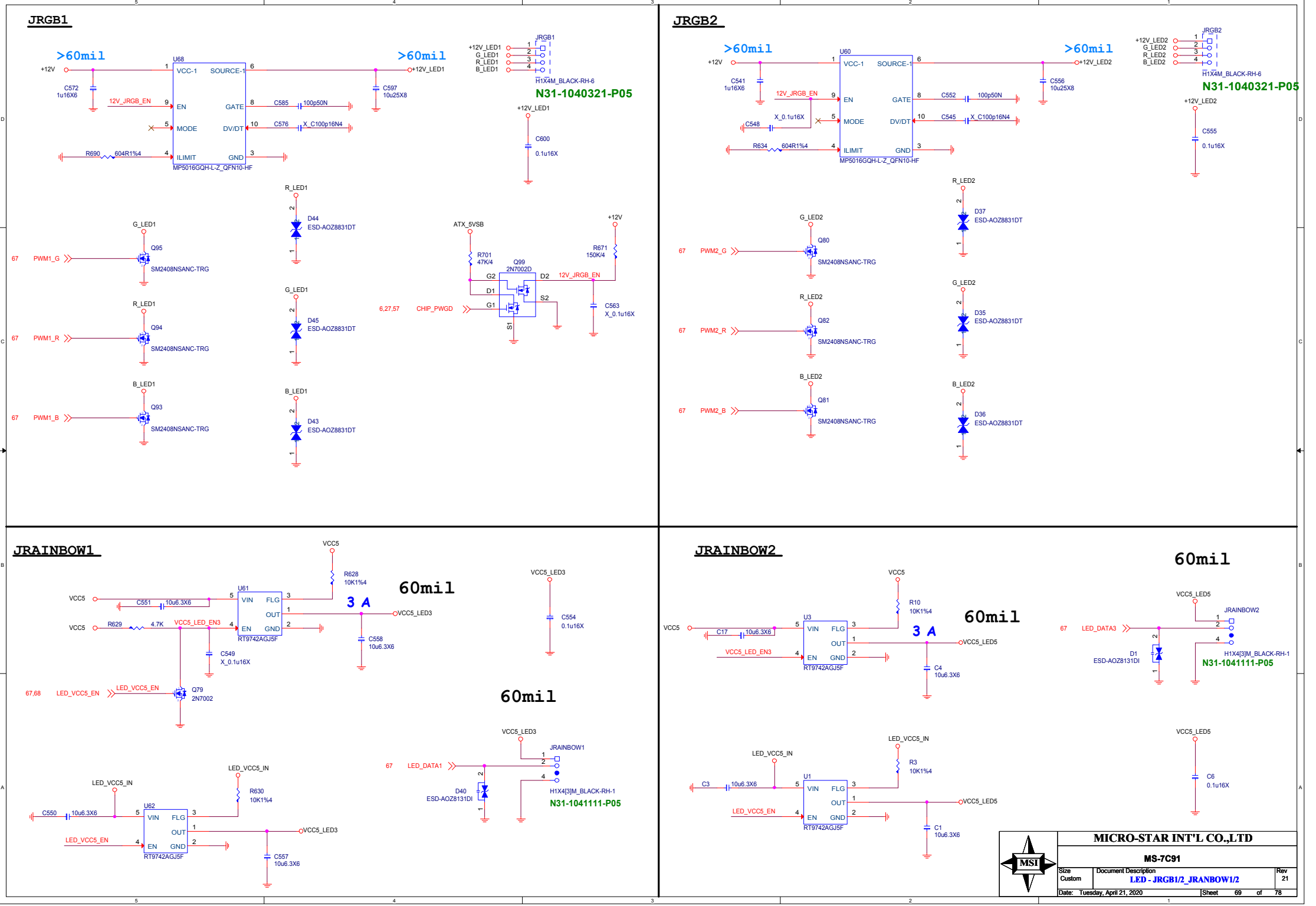
N31-1050121-H06

JF1 for Factory test

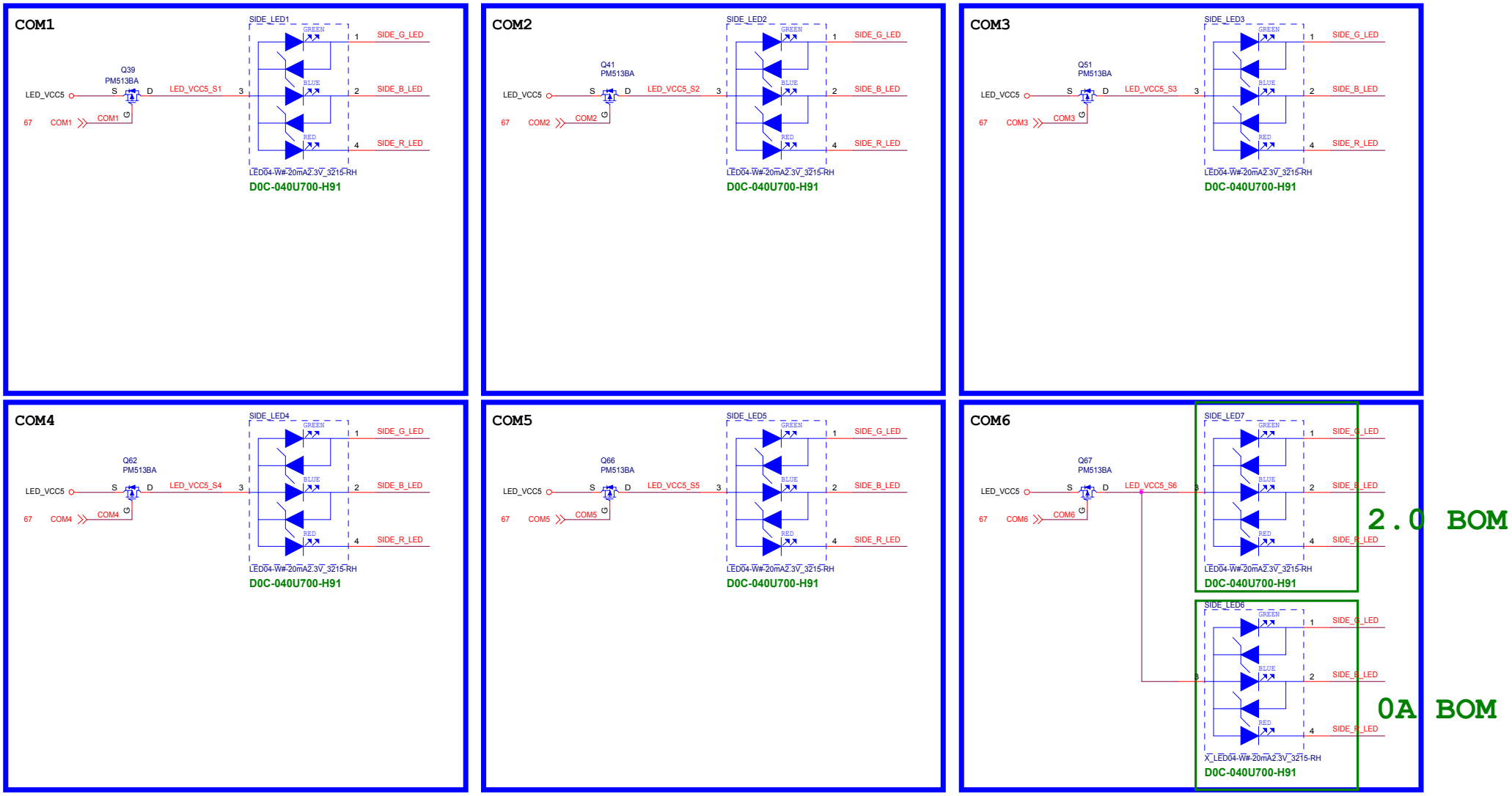


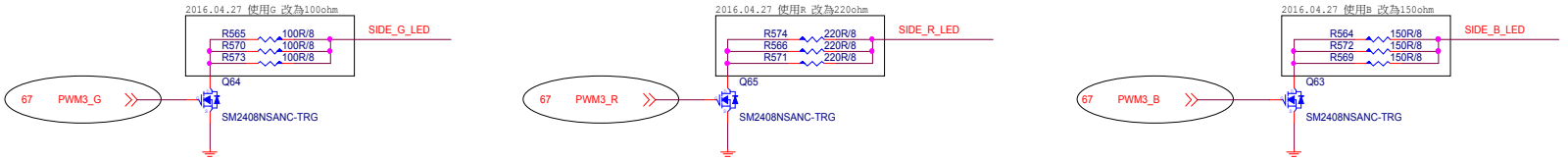
N31-1020151-H06

MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: LED - Power / JPIPE	Rev: 21
Date: Tuesday, April 21, 2020	Sheet 68 of 78	


JRGB1
>60mil
U68
VCC-1
SOURCE-1
EN
GATE
MODE
DV/DT
ILIMIT
GND
MP5016GQH-L-Z_QFN10-HF
+12V
+12V_LED1
12V_JRGB_EN
C572
1u16X6
C597
10u25X8
C585
100p50N
C576
X_C100p16N4
R690
604R1%4
C600
0.1u16X
JRGB1
H1X4M_BLACK-RH-6
N31-1040321-P05
R_LED1
G_LED1
B_LED1
D44
D45
D43
ESD-AOZ8831DT
Q95
Q94
Q93
SM2408NSANC-TRG
67
PWM1_G
PWM1_R
PWM1_B
ATX_5VSB
R701
47K/4
Q99
2N7002D
G2
D1
G1
D2
S2
S1
R671
150K/4
C563
X_0.1u16X
6,27,57
CHIP_PWGD
JRGB2
>60mil
U60
+12V_LED2
C541
1u16X6
C556
10u25X8
C552
100p50N
C545
X_C100p16N4
C548
X_0.1u16X
R634
604R1%4
C555
0.1u16X
N31-1040321-P05
D37
D35
D36
Q80
Q82
Q81
PWM2_G
PWM2_R
PWM2_B
JRAINBOW1
VCC5
U61
VIN
FLG
OUT
EN
GND
RT9742AGJ5F
C551
10u6.3X6
R628
10K1%4
3 A
60mil
VCC5_LED3
R629
4.7K
VCC5_LED_EN3
C549
X_0.1u16X
C558
10u6.3X6
C554
0.1u16X
67,68
LED_VCC5_EN
Q79
2N7002
LED_VCC5_IN
U62
C550
R630
C557
JRAINBOW2
D40
ESD-AOZ8131DI
LED_DATA1
H1X4[3]M_BLACK-RH-1
N31-1041111-P05
JRAINBOW2
U3
U1
R10
R3
C17
C3
C4
C1
C6
VCC5_LED5
LED_DATA3
D1
MICRO-STAR INT'L CO.,LTD
MS-7C91
Size
Custom
Document Description
LED - JRGB1/2_JRANBOW1/2
Rev
21
Date: Tuesday, April 21, 2020
Sheet 69 of 78

BOARD SIDE LED *6





MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: LED - Mystic Light - 1
Rev: 21	
Date: Tuesday, April 21, 2020	Sheet 70 of 78

MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	BOM Option	21

Date: Tuesday, April 21, 2020 | Sheet 71 of 78

CPU Socket

CPU2

E95-0000022-A91

E95-0000022-A91

Simulation

X_JS1 — SIM1 — X_PIN1*2

X_JS2 — SIM2 — X_PIN1*2

X_JS3 — SIM3 — X_PIN1*2

FM2, FM3, FM1, FM4, FM5, FM6, FM8, FM7 — X_FM120

Optics Orientation Holes

MH1, MH2, MH3, MH5, MH6, MH4, MH7, MH8, MH9 — X_MH001

C575 0.1u16X

C559 0.1u16X

2020.04.15

MANUAL PART

AMI_LAB1 — G51-M1SPXXA-A09

G51-M1SPXXA-A09

CFOS1 <MSI-BOM> — Y02-MU00170-CFO

Y02-MU00170-CFO

HDMI_LA1 — Label — HDMI LABEL

Y01-RHDMI03-000

MKT_LA1 — Label — X_MKT LABEL

G51-M1SPP78-Q13

BAT1_X1

BAT-BCR2032P

AVL:
D06-0100161-F52
D06-0100101-K26

PCB

PCB

PCB1

7C91_21

PD0-07C9121-E48
PD0-07C9121-G37

Moat CAP

Reserve for bypass 12VIN noise use

ATX_5VSB — C5 X_0.1u16X — C2 X_0.1u16X

Reserve for bypass VCC5/VCC3/3VSB noise use

VCC5 — C1658 X_0.1u16X — C1659 X_0.1u16X

VCC3 — C1660 X_0.1u16X — C1661 X_0.1u16X

3VSB — C1662 X_0.1u16X

2020.04.14

MOS HEATSINK

N MOS

HS_MOS1 — MEC2 — MEC1

NHS-AURAS(0P10B08484)

E31-0506780-A87

W MOS

HS_MOS2 — MEC2 — MEC1

WHS-AURAS(0P10B08483)

E31-0506770-A87

PCH HEATSINK

PM_HS1 — MEC1 — MEC2

PHS-AURAS(0P10B08485)

E31-0410540-A87

M2 COVER

M2_1_HS1 — MEC2 — MEC1

AURAS(0P10B08291)

E31-0002510-A87

M2_1_HS2 — MEC2 — MEC1

AURAS(0P10B08292)

E31-0002500-A87

IO BRACKET

IO_BKT1 — MEC2 — MEC1

AJOHO(CSCZ-SHIELD301)

E21-7C91010-A91

DDR COVER

20190201 Remove DDR_COVER1

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MS-7C91

Size	Document Description	Rev
Custom	Manual Parts	21

Date: Tuesday, April 21, 2020 Sheet 72 of 78