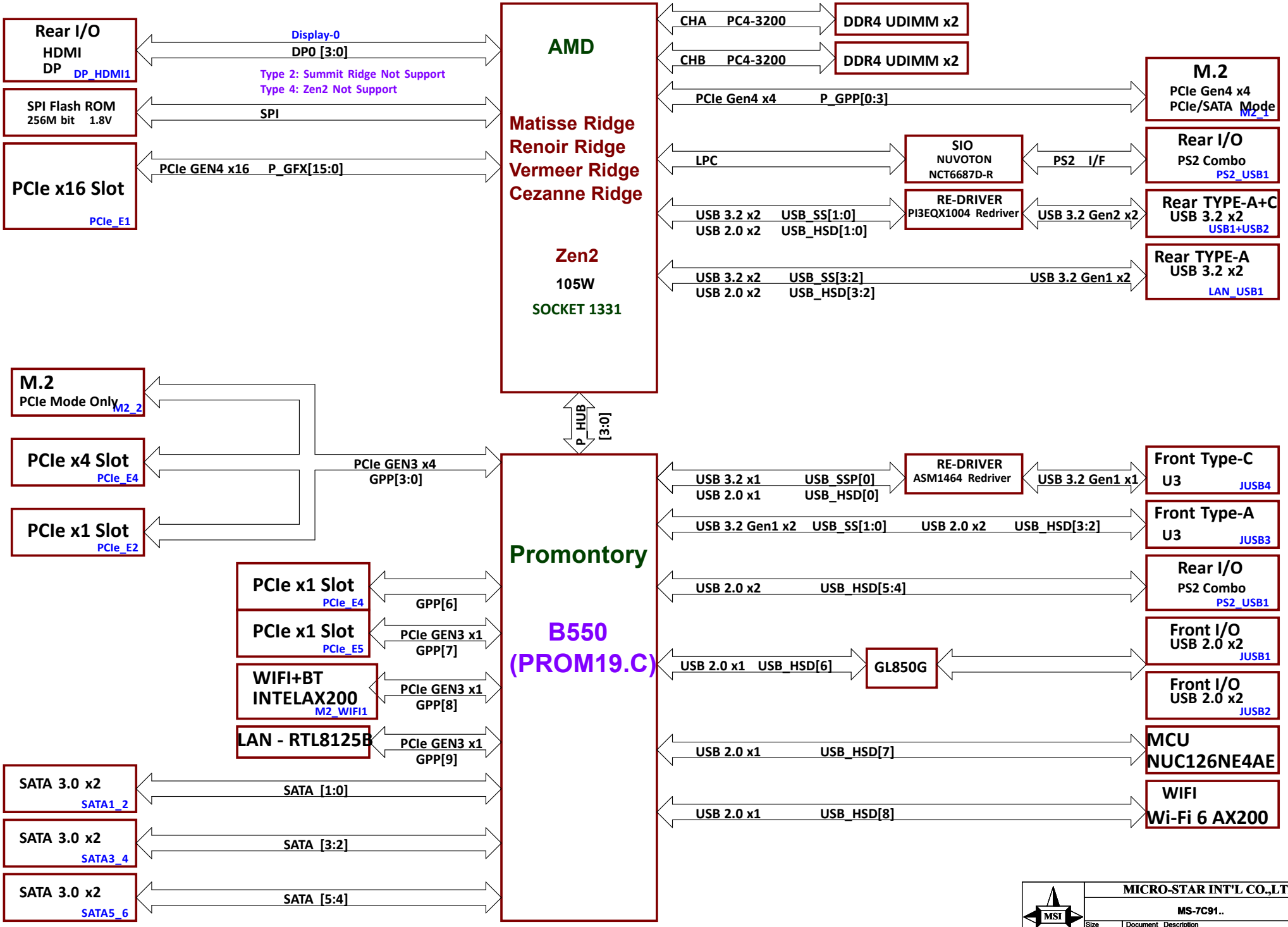
amd am4 b550

MICRO-STAR INT'L CO.,LTD

MS-7C91..

Size	Document Description	Rev
Custom	Cover Sheet	30

Date: Friday, July 24, 2020 Sheet 1 of 78

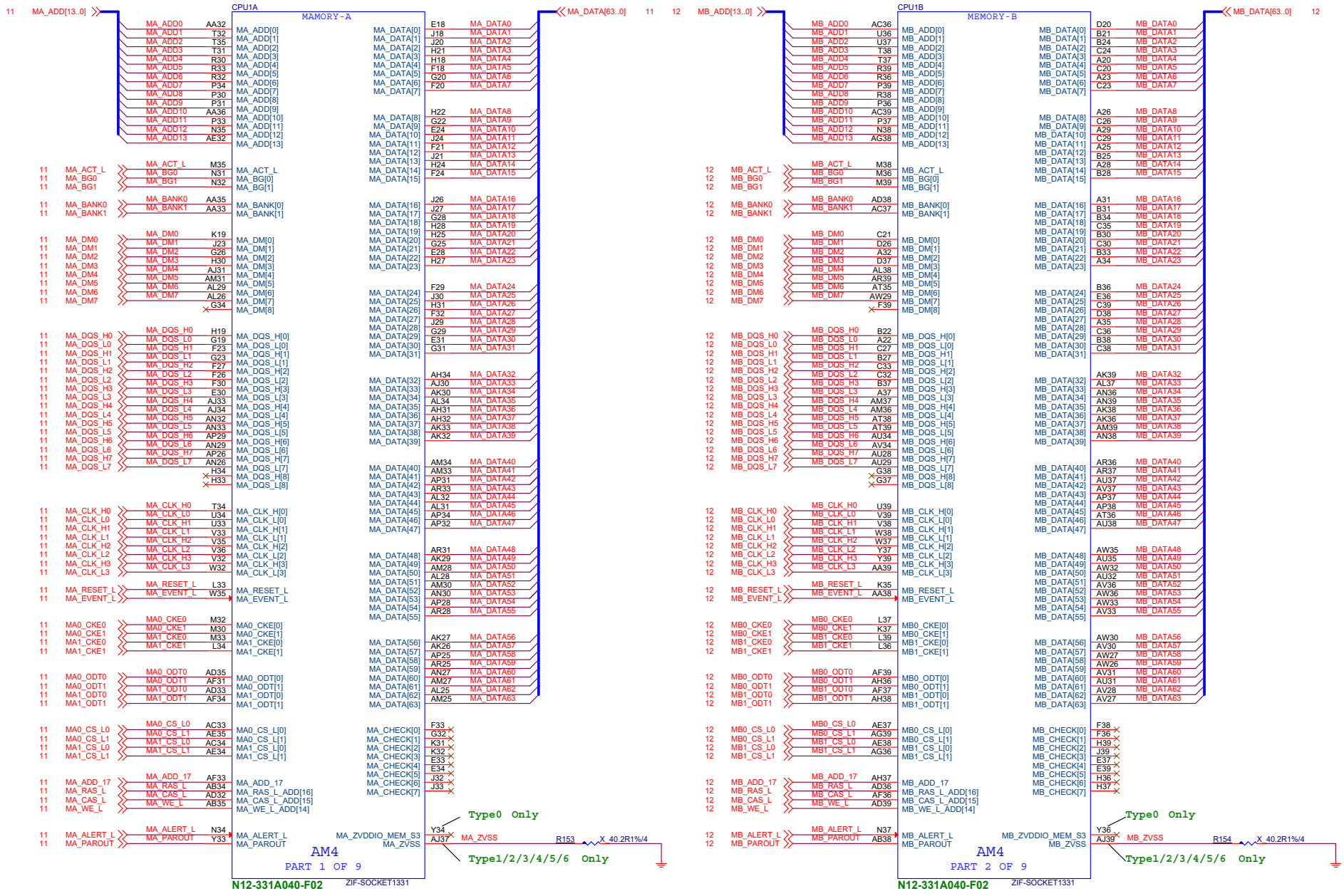


MICRO-STAR INT'L CO.,LTD

MS-7C91..

Size	Document Description	Rev
Custom	Block Diagram	30

Date: Thursday, July 23, 2020 Sheet 2 of 78

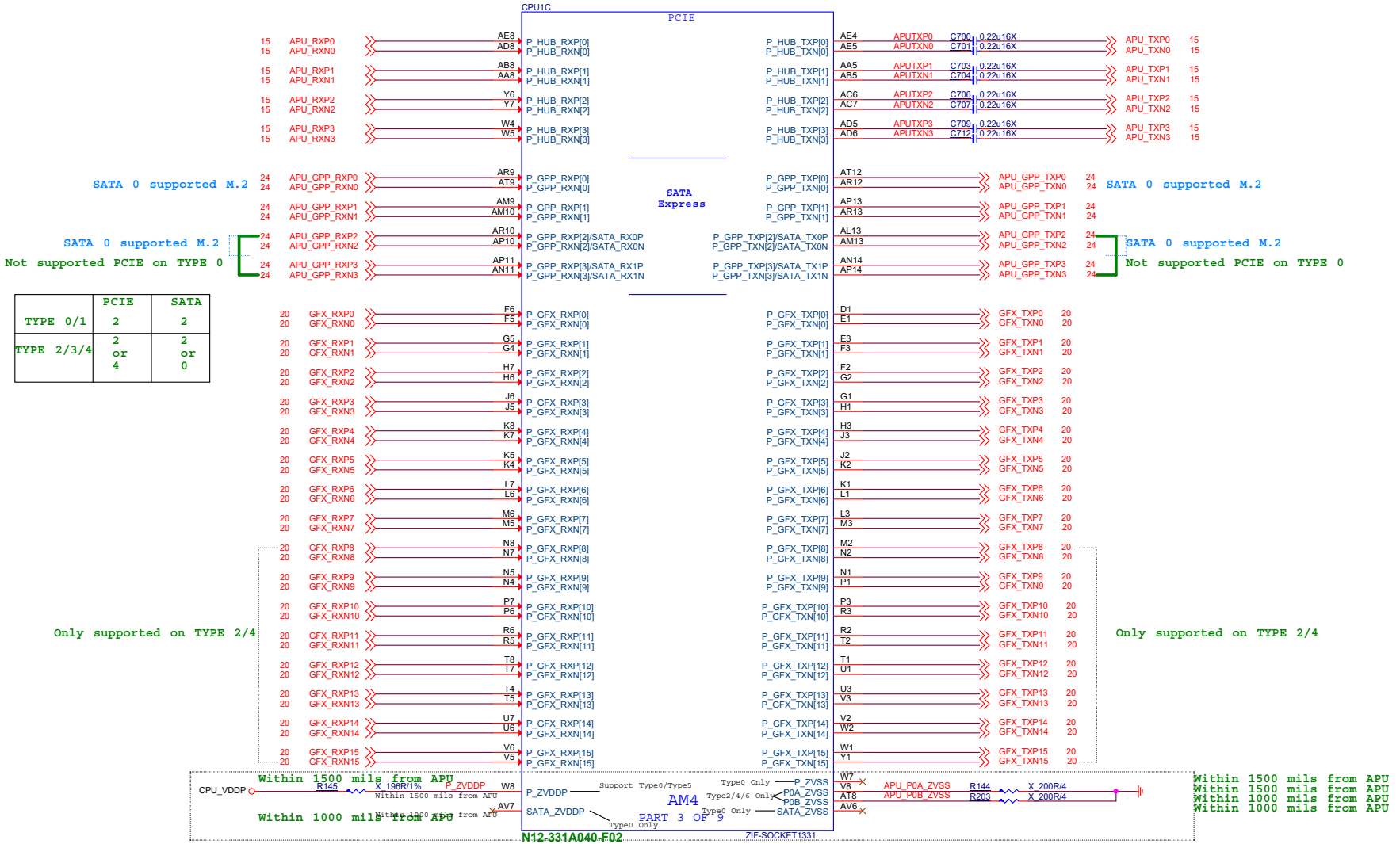


MICRO-STAR INT'L CO.,LTD

MS-7C91..

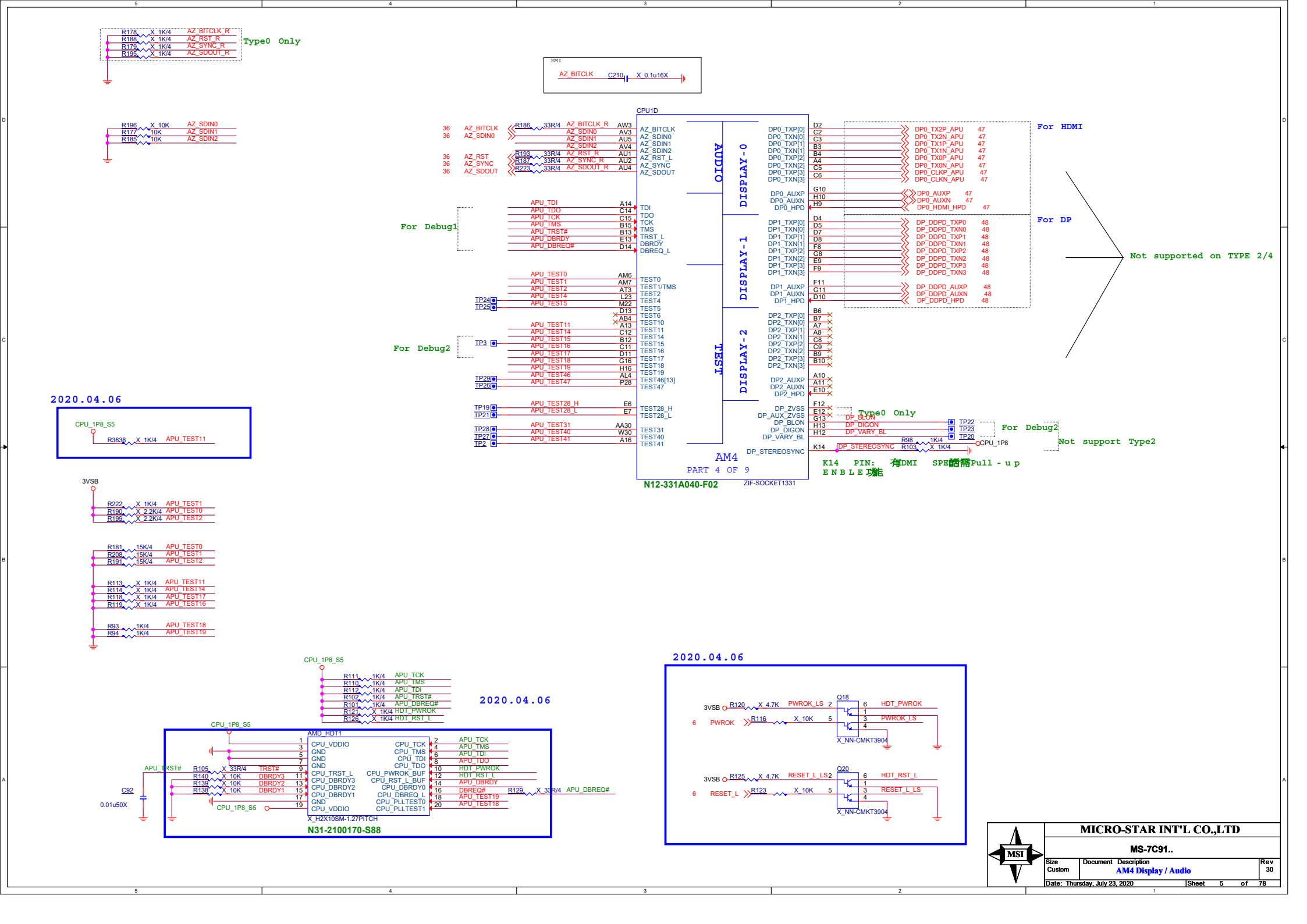
Size	Document Description	Rev
Custom	AM4 DDR4 I/F	30

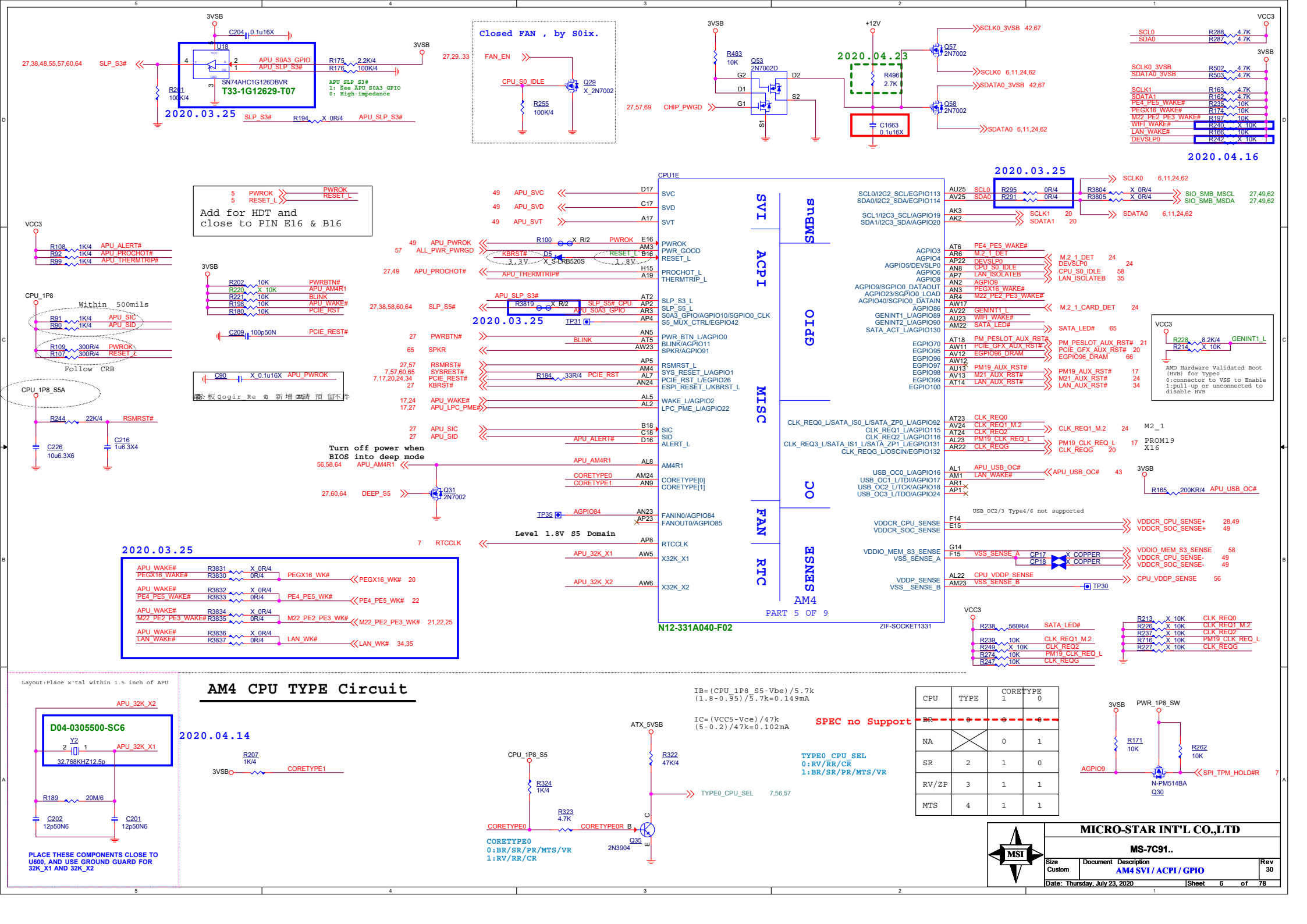
Date: Thursday, July 23, 2020 Sheet 3 of 78

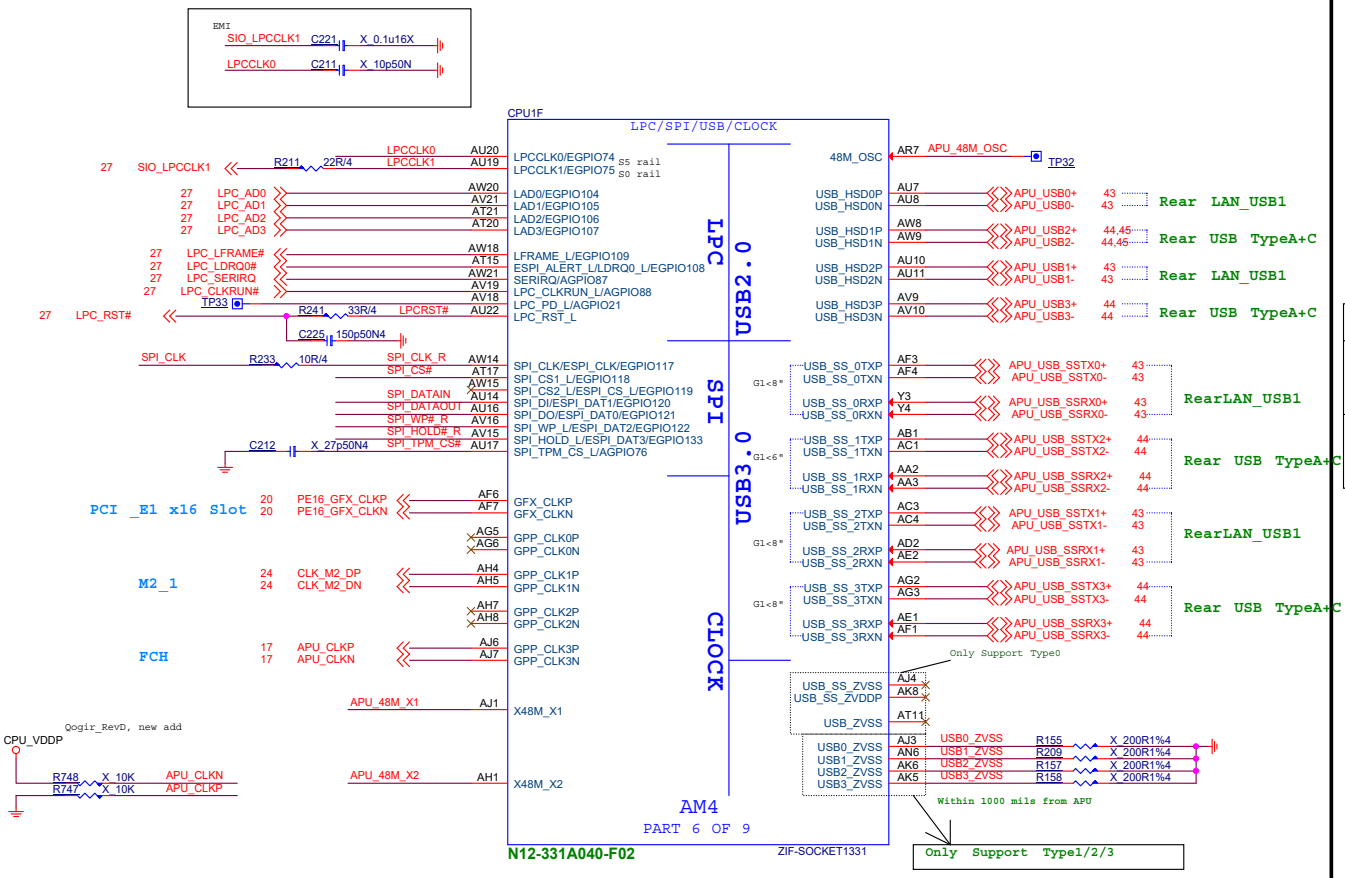


	PCIE	SATA
TYPE 0/1	2	2
TYPE 2/3/4	2 or 4	2 or 0

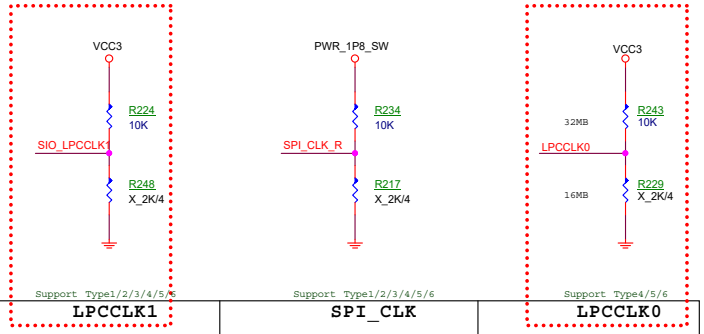
Company	MICRO-STAR INT'L CO.,LTD
Model	MS-7C91..
Size	Custom
Document Description	AM4 PCIE / SATAE
Rev	30
Date	Thursday, July 23, 2020
Sheet	4 of 78


Type0 Only
EMI
AZ_BITCLK C210 X_0.1u16X
CPU1D
AUDIO
DISPLAY-0
DISPLAY-1
DISPLAY-2
TEST
For HDMI
For DP
Not supported on TYPE 2/4
For Debug1
For Debug2
Type0 Only
For Debug2
Not support Type2
K14 PIN: 有DMI SPE需Pull-up
ENBLE功能
AM4
PART 4 OF 9
N12-331A040-F02
ZIF-SOCKET1331
2020.04.06
3VSB
AMD_HDT1
CPU_1P8_S5
APU_TRST#
0.01u50X
X_H2X10SM-1.27PITCH
N31-2100170-S88
2020.04.06
2020.04.06
Q18
Q20
X_NN-CMKT3904
MICRO-STAR INT'L CO.,LTD
MS-7C91..
Size Custom
Document Description AM4 Display / Audio
Rev 30
Date: Thursday, July 23, 2020
Sheet 5 of 78

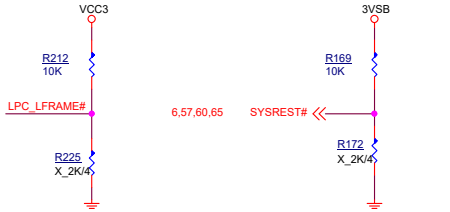

Closed FAN , by S0ix.
Add for HDT and close to PIN E16 & B16
Turn off power when BIOS into deep mode
Level 1.8V S5 Domain
2020.03.25
2020.04.23
2020.04.16
2020.04.14
CPU1E
SVI
ACPI
GPIO
MISC
SMBus
OC
FAN
RTC
SENSE
AM4
PART 5 OF 9
N12-331A040-F02
ZIF-SOCKET1331
SN74AHC1G126DBVR
T33-1G12629-T07
D04-0305500-SC6
AM4 CPU TYPE Circuit
SPEC no Support
MICRO-STAR INT'L CO.,LTD
MS-7C91..
AM4 SVI / ACPI / GPIO
Date: Thursday, July 23, 2020
Sheet 6 of 78



Strapping Options

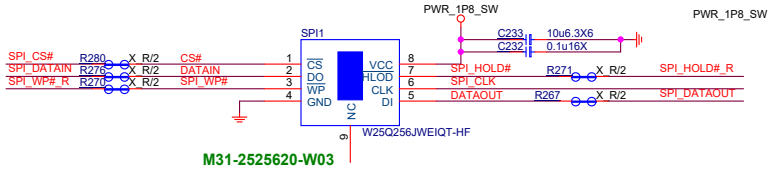


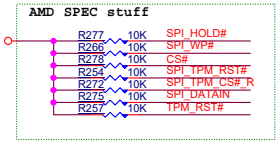
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image (Default)
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]

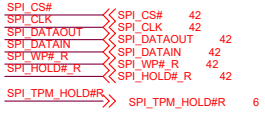


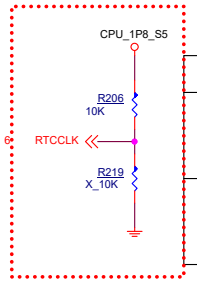
	AGPIO3	LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

SPI ROM(1.8V)



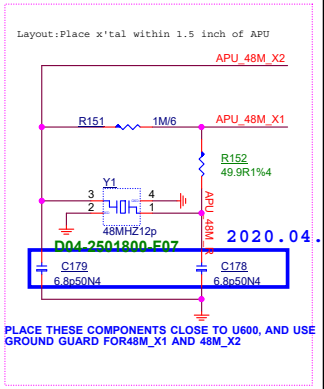


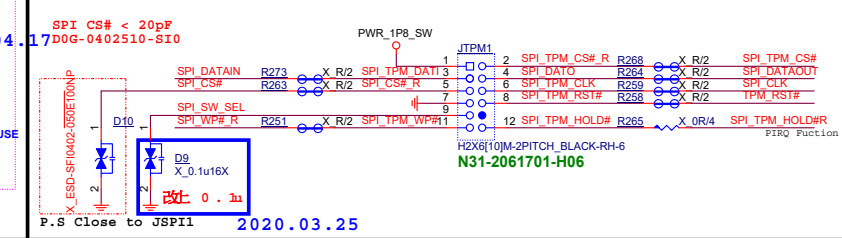


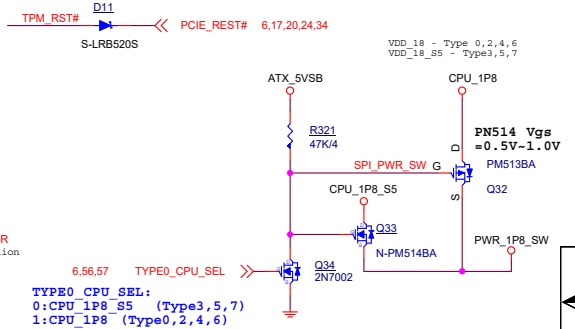


	RTCCLK
PULL HIGH	RTCCLK is input and is used as the bypass clock (Default)
PULL LOW	Normal Mode: Use 32Khz xtal as the source of RTC clock

Support Type4/6





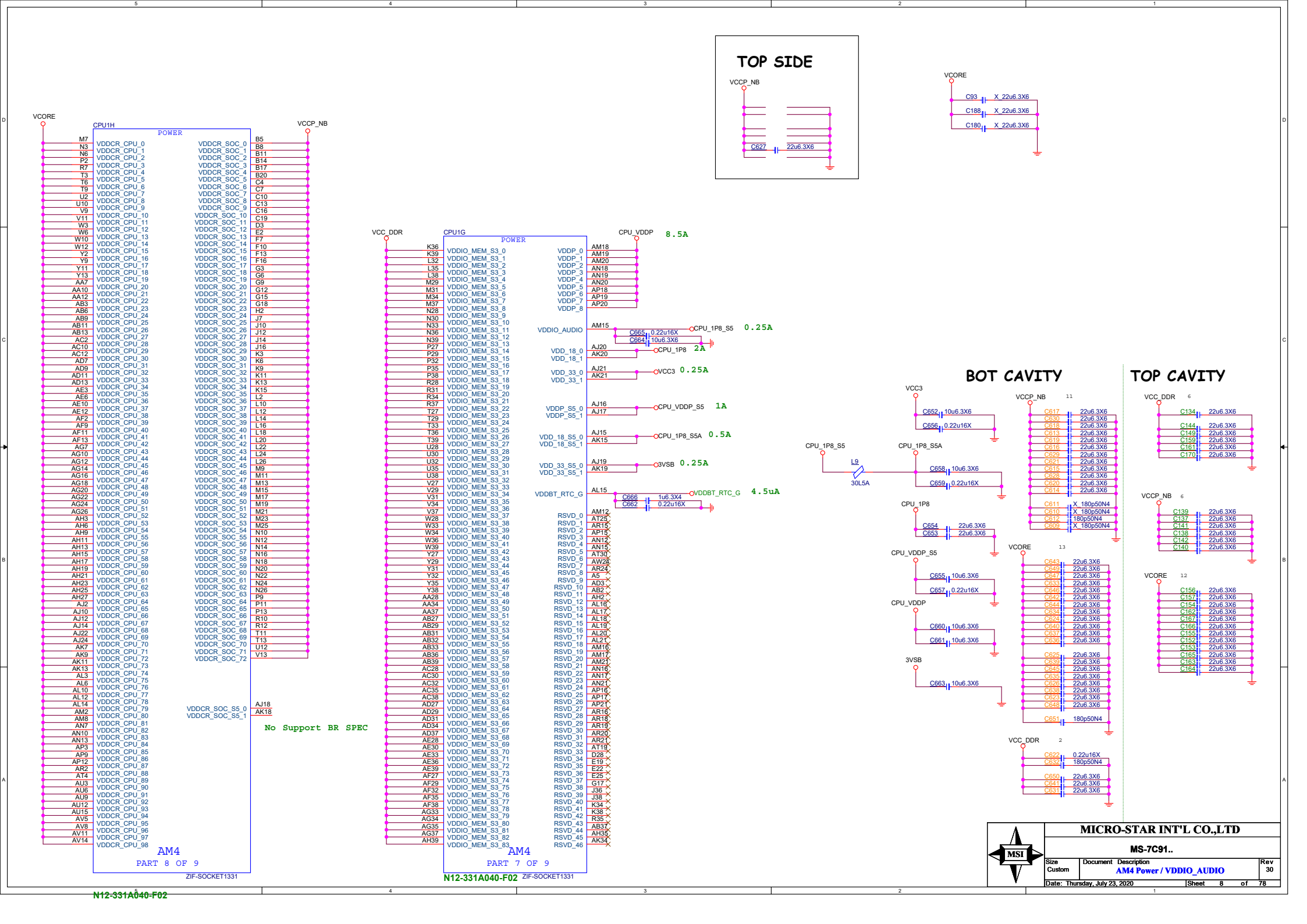


MICRO-STAR INT'L CO.,LTD

MS-7C91..

Size	Document Description	Rev
Custom	AM4 LPC / SPI / USB / CLK / STRAP	30

Date: Thursday, July 23, 2020 Sheet 7 of 78


TOP SIDE
VCCP_NB
C627
22u6.3X6
VCORE
C93
X_22u6.3X6
C188
X_22u6.3X6
C180
X_22u6.3X6
VCORE
CPU1H
POWER
VCCP_NB
VDDCR_CPU_0
VDDCR_CPU_1
VDDCR_CPU_2
VDDCR_CPU_3
VDDCR_CPU_4
VDDCR_CPU_5
VDDCR_CPU_6
VDDCR_CPU_7
VDDCR_CPU_8
VDDCR_CPU_9
VDDCR_CPU_10
VDDCR_CPU_11
VDDCR_CPU_12
VDDCR_CPU_13
VDDCR_CPU_14
VDDCR_CPU_15
VDDCR_CPU_16
VDDCR_CPU_17
VDDCR_CPU_18
VDDCR_CPU_19
VDDCR_CPU_20
VDDCR_CPU_21
VDDCR_CPU_22
VDDCR_CPU_23
VDDCR_CPU_24
VDDCR_CPU_25
VDDCR_CPU_26
VDDCR_CPU_27
VDDCR_CPU_28
VDDCR_CPU_29
VDDCR_CPU_30
VDDCR_CPU_31
VDDCR_CPU_32
VDDCR_CPU_33
VDDCR_CPU_34
VDDCR_CPU_35
VDDCR_CPU_36
VDDCR_CPU_37
VDDCR_CPU_38
VDDCR_CPU_39
VDDCR_CPU_40
VDDCR_CPU_41
VDDCR_CPU_42
VDDCR_CPU_43
VDDCR_CPU_44
VDDCR_CPU_45
VDDCR_CPU_46
VDDCR_CPU_47
VDDCR_CPU_48
VDDCR_CPU_49
VDDCR_CPU_50
VDDCR_CPU_51
VDDCR_CPU_52
VDDCR_CPU_53
VDDCR_CPU_54
VDDCR_CPU_55
VDDCR_CPU_56
VDDCR_CPU_57
VDDCR_CPU_58
VDDCR_CPU_59
VDDCR_CPU_60
VDDCR_CPU_61
VDDCR_CPU_62
VDDCR_CPU_63
VDDCR_CPU_64
VDDCR_CPU_65
VDDCR_CPU_66
VDDCR_CPU_67
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VDDCR_CPU_69
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VDDCR_CPU_71
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VDDCR_CPU_77
VDDCR_CPU_78
VDDCR_CPU_79
VDDCR_CPU_80
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VDDCR_CPU_84
VDDCR_CPU_85
VDDCR_CPU_86
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VDDCR_CPU_88
VDDCR_CPU_89
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VDDCR_CPU_91
VDDCR_CPU_92
VDDCR_CPU_93
VDDCR_CPU_94
VDDCR_CPU_95
VDDCR_CPU_96
VDDCR_CPU_97
VDDCR_CPU_98
VDDCR_SOC_0
VDDCR_SOC_1
VDDCR_SOC_2
VDDCR_SOC_3
VDDCR_SOC_4
VDDCR_SOC_5
VDDCR_SOC_6
VDDCR_SOC_7
VDDCR_SOC_8
VDDCR_SOC_9
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VDDCR_SOC_65
VDDCR_SOC_66
VDDCR_SOC_67
VDDCR_SOC_68
VDDCR_SOC_69
VDDCR_SOC_70
VDDCR_SOC_71
VDDCR_SOC_72
VDDCR_SOC_S5_0
VDDCR_SOC_S5_1
AM4
PART 8 OF 9
ZIF-SOCKET1331
No Support BR SPEC
N12-331A040-F02
VCC_DDR
CPU1G
POWER
CPU_VDDP
8.5A
VDDIO_MEM_S3_0
VDDIO_MEM_S3_1
VDDIO_MEM_S3_2
VDDIO_MEM_S3_3
VDDIO_MEM_S3_4
VDDIO_MEM_S3_5
VDDIO_MEM_S3_6
VDDIO_MEM_S3_7
VDDIO_MEM_S3_8
VDDIO_MEM_S3_9
VDDIO_MEM_S3_10
VDDIO_MEM_S3_11
VDDIO_MEM_S3_12
VDDIO_MEM_S3_13
VDDIO_MEM_S3_14
VDDIO_MEM_S3_15
VDDIO_MEM_S3_16
VDDIO_MEM_S3_17
VDDIO_MEM_S3_18
VDDIO_MEM_S3_19
VDDIO_MEM_S3_20
VDDIO_MEM_S3_21
VDDIO_MEM_S3_22
VDDIO_MEM_S3_23
VDDIO_MEM_S3_24
VDDIO_MEM_S3_25
VDDIO_MEM_S3_26
VDDIO_MEM_S3_27
VDDIO_MEM_S3_28
VDDIO_MEM_S3_29
VDDIO_MEM_S3_30
VDDIO_MEM_S3_31
VDDIO_MEM_S3_32
VDDIO_MEM_S3_33
VDDIO_MEM_S3_34
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VDDIO_MEM_S3_36
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VDDIO_MEM_S3_66
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VDDIO_MEM_S3_77
VDDIO_MEM_S3_78
VDDIO_MEM_S3_79
VDDIO_MEM_S3_80
VDDIO_MEM_S3_81
VDDIO_MEM_S3_82
VDDIO_MEM_S3_83
VDDP_0
VDDP_1
VDDP_2
VDDP_3
VDDP_4
VDDP_5
VDDP_6
VDDP_7
VDDP_8
VDDIO_AUDIO
C665
0.22u16X
C664
10u6.3X6
CPU_1P8_S5
0.25A
VDD_18_0
VDD_18_1
CPU_1P8
2A
VDD_33_0
VDD_33_1
VCC3
0.25A
VDDP_S5_0
VDDP_S5_1
CPU_VDDP_S5
1A
VDD_18_S5_0
VDD_18_S5_1
CPU_1P8_S5A
0.5A
VDD_33_S5_0
VDD_33_S5_1
3VSB
0.25A
VDDBT_RTC_G
C666
1u6.3X4
C662
0.22u16X
VDDBT_RTC_G
4.5uA
RSVD_0
RSVD_1
RSVD_2
RSVD_3
RSVD_4
RSVD_5
RSVD_6
RSVD_7
RSVD_8
RSVD_9
RSVD_10
RSVD_11
RSVD_12
RSVD_13
RSVD_14
RSVD_15
RSVD_16
RSVD_17
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RSVD_28
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RSVD_30
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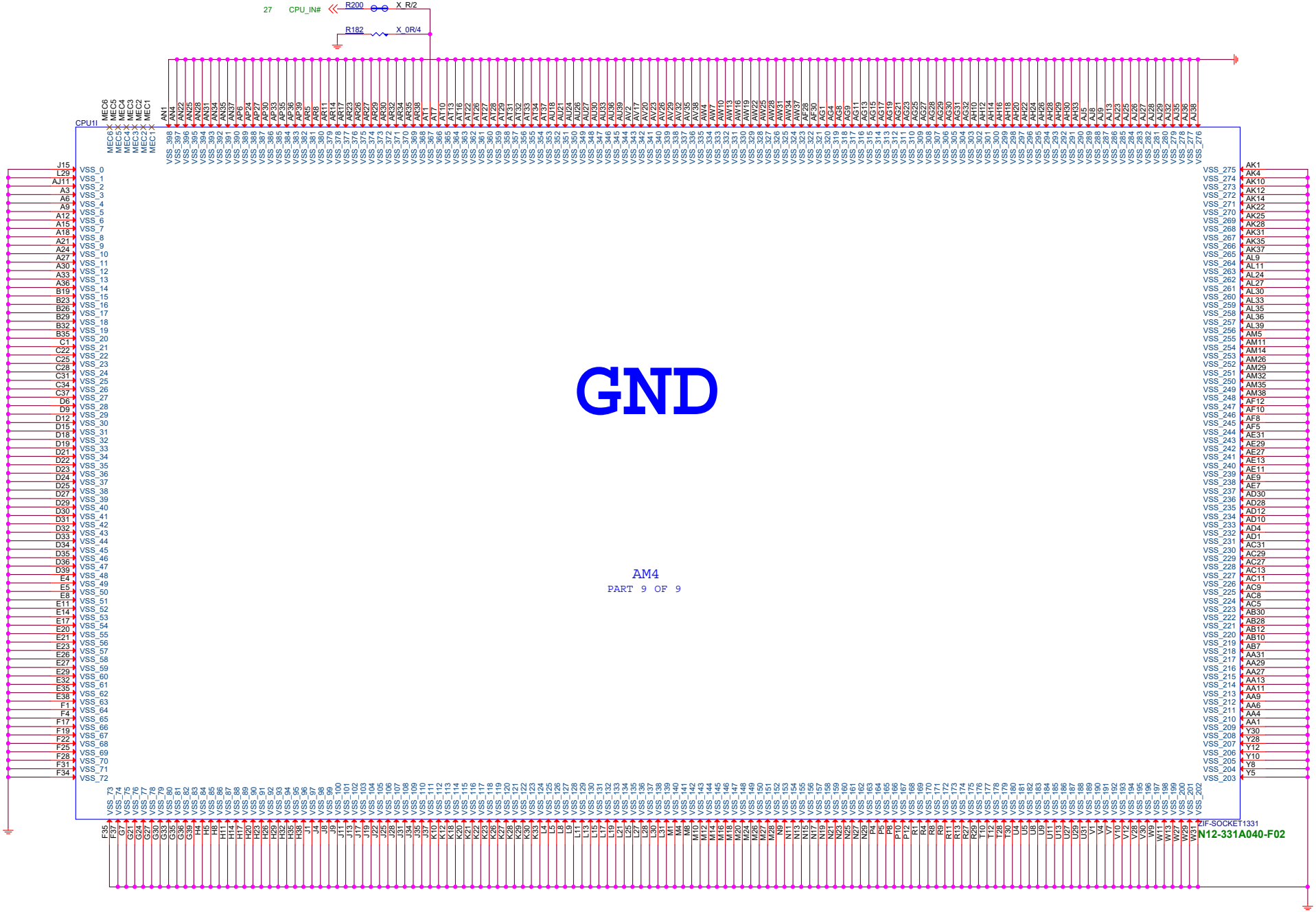
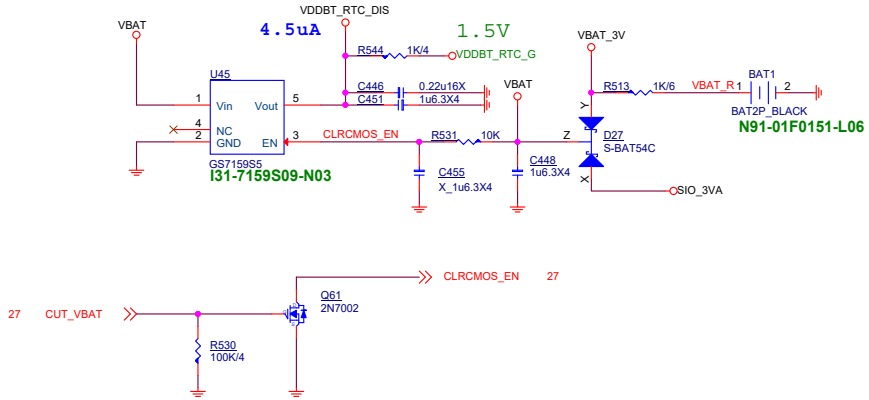
RSVD_37
RSVD_38
RSVD_39
RSVD_40
RSVD_41
RSVD_42
RSVD_43
RSVD_44
RSVD_45
RSVD_46
AM4
PART 7 OF 9
ZIF-SOCKET1331
N12-331A040-F02
BOT CAVITY
TOP CAVITY
CPU_1P8_S5
L9
30L5A
VCC3
C652
10u6.3X6
C656
0.22u16X
CPU_1P8_S5A
C658
10u6.3X6
C659
0.22u16X
CPU_1P8
C654
22u6.3X6
C653
22u6.3X6
CPU_VDDP_S5
C655
10u6.3X6
C657
0.22u16X
CPU_VDDP
C660
10u6.3X6
C661
10u6.3X6
3VSB
C663
10u6.3X6
VCCP_NB
11
C617
C630
C618
C613
C619
C616
C629
C621
C615
C628
C620
C614
22u6.3X6
C611
C610
C612
C609
X_180p50N4
180p50N4
VCORE
13
C643
C649
C647
C633
C646
C642
C644
C634
C624
C640
C637
C636
C625
C639
C645
C635
C626
C638
C623
C648
22u6.3X6
C651
180p50N4
VCC_DDR
2
C622
C632
0.22u16X
180p50N4
C650
C641
C631
22u6.3X6
VCC_DDR
6
C134
C144
C149
C159
C161
C170
22u6.3X6
VCCP_NB
6
C139
C137
C141
C138
C142
C140
22u6.3X6
VCORE
12
C156
C157
C154
C162
C167
C166
C155
C152
C153
C165
C163
C164
22u6.3X6
MSI
MICRO-STAR INT'L CO.,LTD
MS-7C91..
Size
Custom
Document Description
AM4 Power / VDDIO_AUDIO
Rev
30
Date: Thursday, July 23, 2020
Sheet 8 of 78

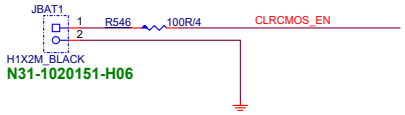


MICRO-STAR INT'L CO.,LTD	
MS-7C91..	
Size: Custom	Document Description: AM4 GND
Rev: 30	
Date: Thursday, July 23, 2020	Sheet 9 of 78

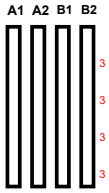
RTC & Clear CMOS Circuit



Clear CMOS button



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C91..	
Size: Custom	Document Description: RTC / CMOS	Rev: 30
Date: Thursday, July 23, 2020	Sheet 10 of 78	



DIMMA1A

DIMMA2A

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

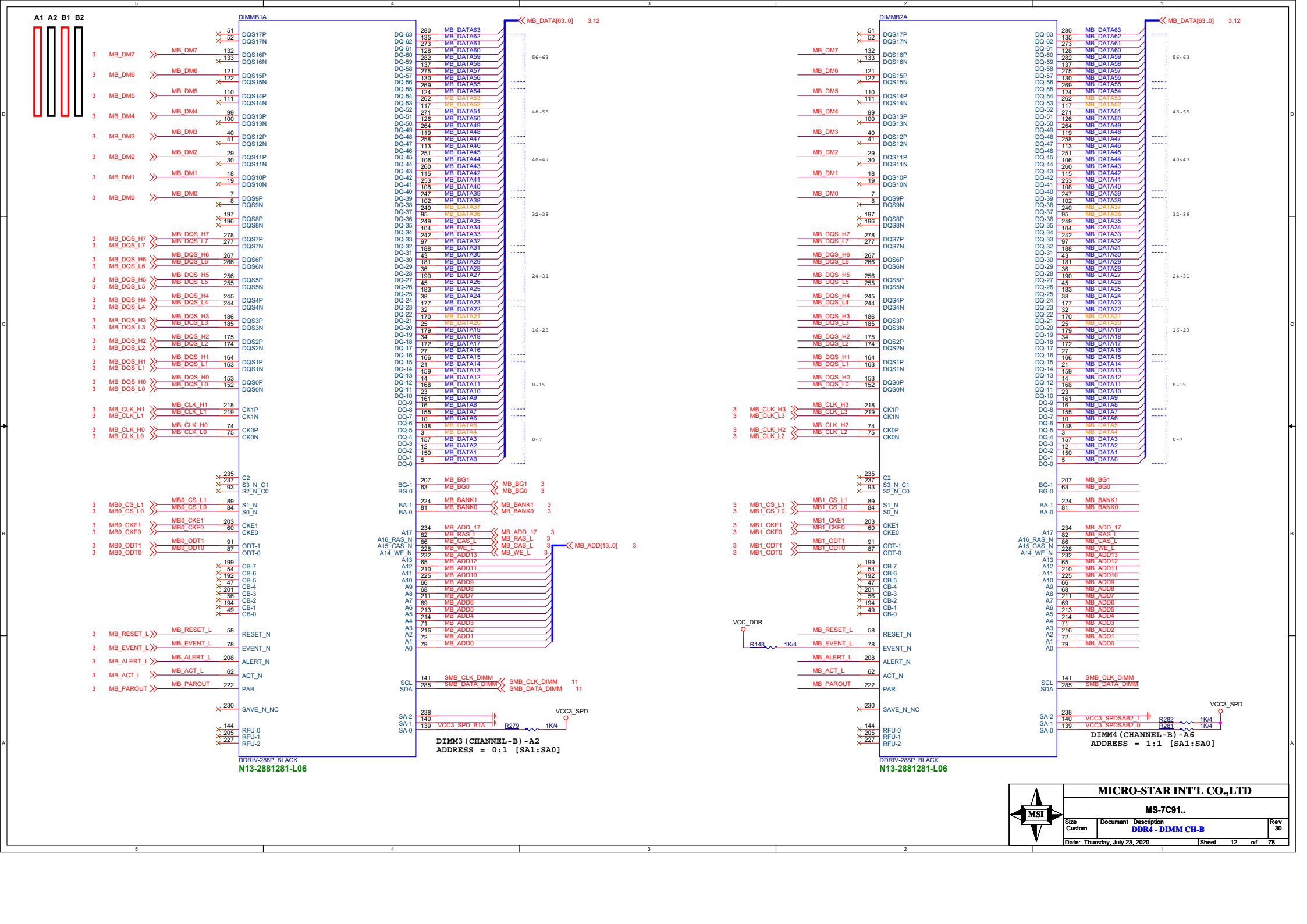
DIMM1(CHANNEL-A)-A0
ADDRESS = 0:0 [SA1:SA0]

DIMM2(CHANNEL-A)-A4
ADDRESS = 1:0 [SA1:SA0]

DDRIV-288P_BLACK
N13-2881281-L06

DDRIV-288P_BLACK
N13-2881281-L06

MICRO-STAR INT'L CO.,LTD		
MS-7C91..		
Size: Custom	Document Description: DDR4 - DIMM CH-A	Rev: 30
Date: Thursday, July 23, 2020	Sheet 11 of 78	


A1 A2 B1 B2
DIMMB1A
DIMMB2A
MB_DATA[63..0] 3,12
MB_ADD[13..0] 3
DDRIV-288P_BLACK
N13-2881281-L06
DIMM3(CHANNEL-B)-A2
ADDRESS = 0:1 [SA1:SA0]
DIMM4(CHANNEL-B)-A6
ADDRESS = 1:1 [SA1:SA0]
VCC_DDR
VCC3_SPD
R148 1K/4
R279 1K/4
R282 1K/4
R281 1K/4
MICRO-STAR INT'L CO.,LTD
MS-7C91..
Size Custom
Document Description DDR4 - DIMM CH-B
Rev 30
Date: Thursday, July 23, 2020
Sheet 12 of 78

avl:D08-0301100-B07

F4
VCC3 1 2 VCC3_SPD
F-SPR-P260T
D08-0301000-P16

DIMM SLOT PN BY SPEC

DIMMA1C
DDRIV-288P_BLACK
N13-2881281-L06

DIMMA2C
DDRIV-288P_BLACK
N13-2881281-L06

DDR VREF

(place resistors close to DIMMs)

DIMM_CA_VREF_A — C31 0.1u16X — VCC_DDR

DIMM_CA_VREF_A, VCC_DDR — R38 1K/1% — C34 0.1u16X; C46 1000p50X; C49 0.1u16X; R36 1K/1%

VCC3_SPD — C243 0.1u16X
DIMM_CA_VREF_A — C57 2.2u6.3X4; C63 0.1u16X
VTT_DDR — C169 X_0.1u16X
VPP25 — C257 0.1u16X; C251 0.1u16X

VCC_DDR — C107 1u6.3X4; C113 1u6.3X4; C129 1u6.3X4; C110 1u6.3X4; C98 X_0.1u16X; C184 0.1u16X; C132 0.1u16X

VCC3_SPD — C244 0.1u16X
DIMM_CA_VREF_A — C56 2.2u6.3X4; C62 0.1u16X
VTT_DDR — C133 X_0.1u16X
VPP25 — C260 0.1u16X; C250 0.1u16X

VCC_DDR — C197 1u6.3X4; C131 1u6.3X4; C103 1u6.3X4; C173 1u6.3X4; C111 X_0.1u16X; C176 0.1u16X; C187 0.1u16X

DIMMA1B
DDRIV-288P_BLACK
N13-2881281-L06

DIMMA2B
DDRIV-288P_BLACK
N13-2881281-L06

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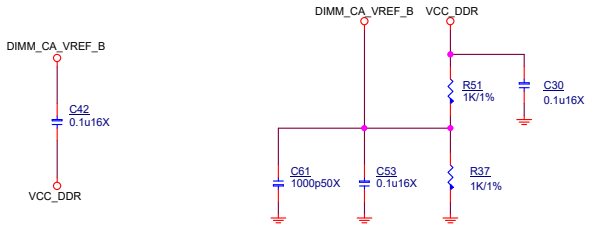
MS-7C91..

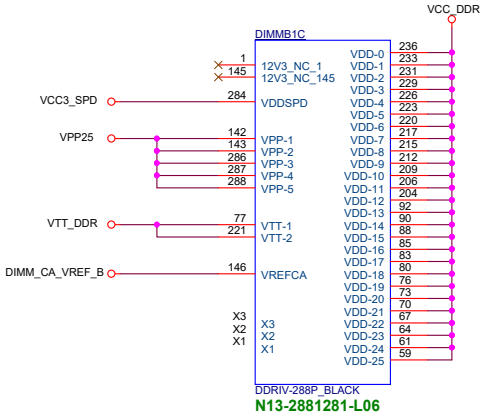
Size	Document Description	Rev
Custom	DDR4 - POWER/GND-1	30

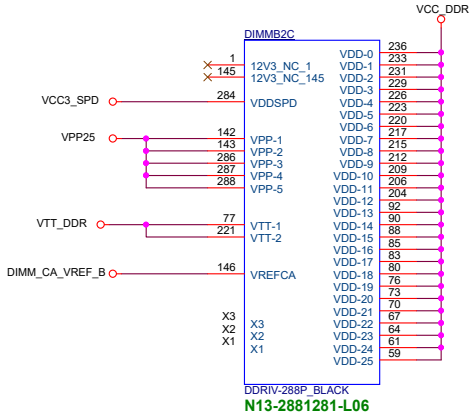
Date: Thursday, July 23, 2020 Sheet 13 of 78

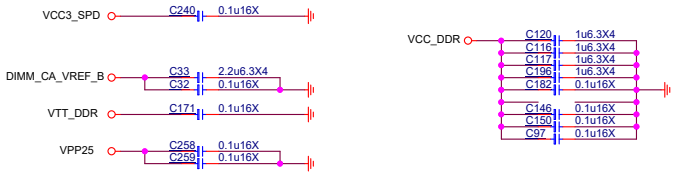
DDR VREF

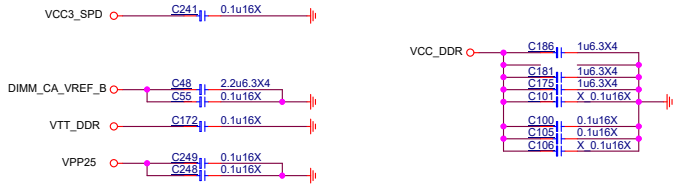
(place resistors close to DIMMs)

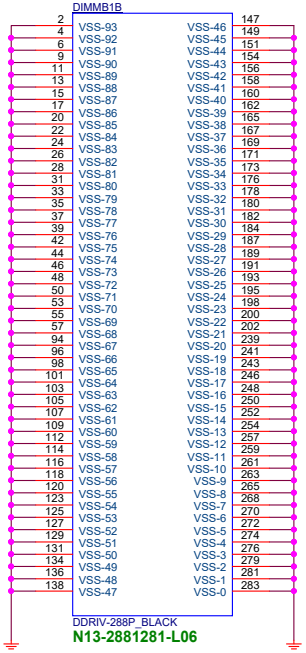


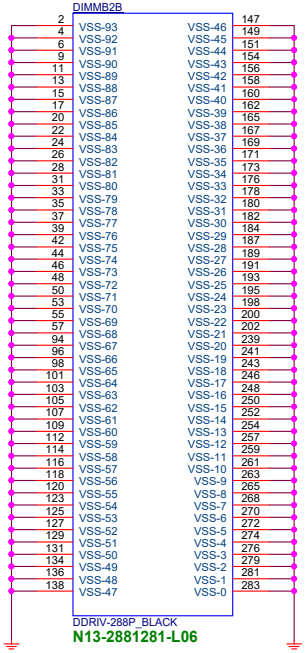












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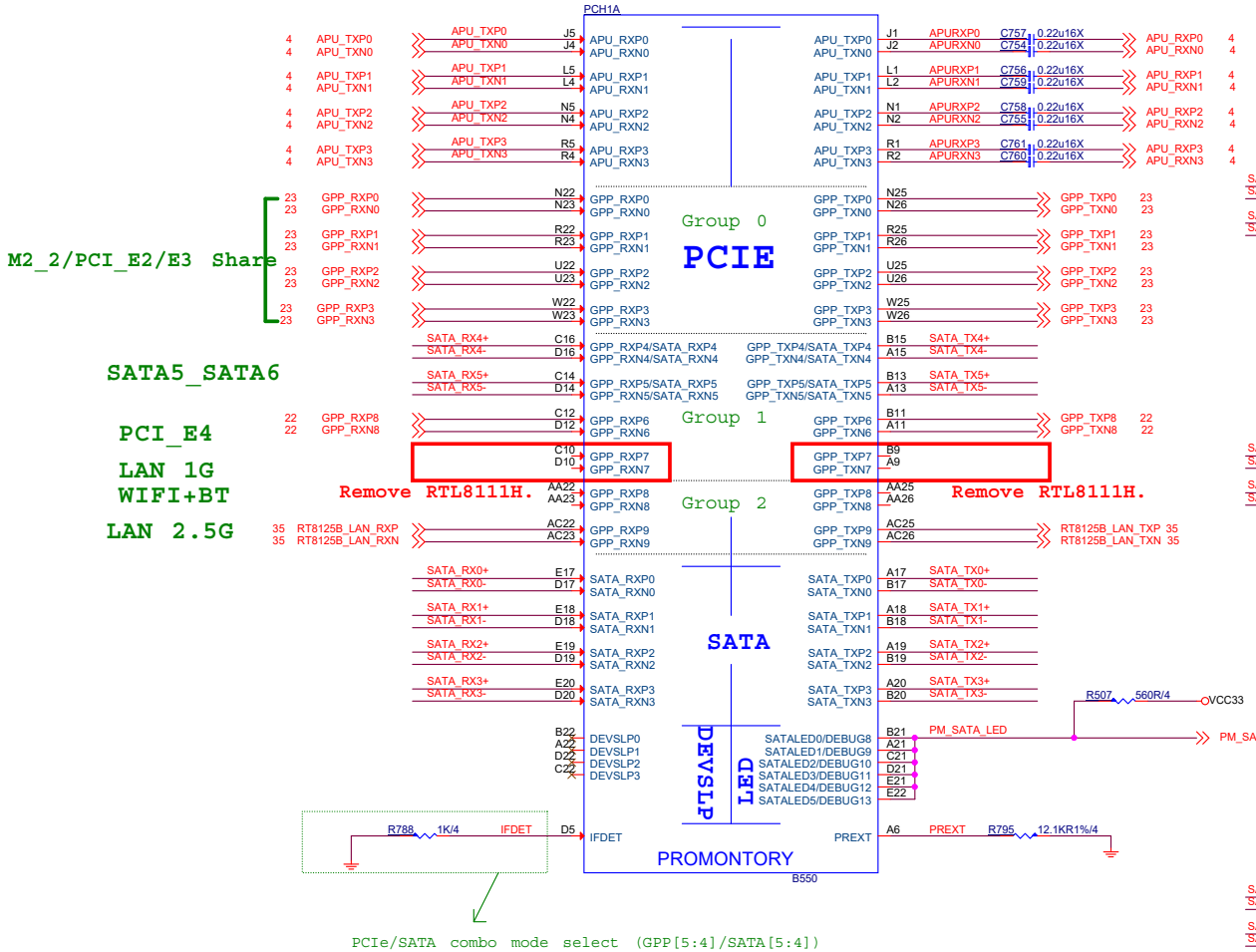
MS-7C91..

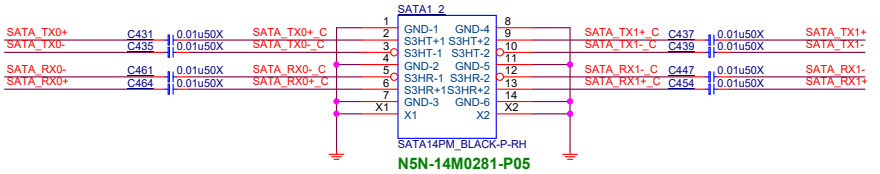
Size	Document Description	Rev
Custom	DDR4 - POWER/GND-2	30

Date: Thursday, July 23, 2020 Sheet 14 of 78

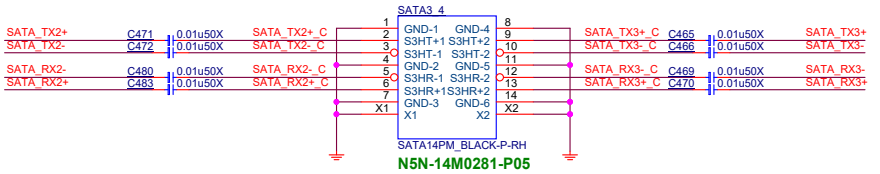
SATA Connector



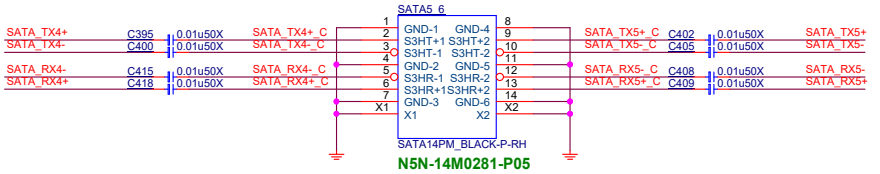
SATA1_2



SATA3_4



SATA5_6



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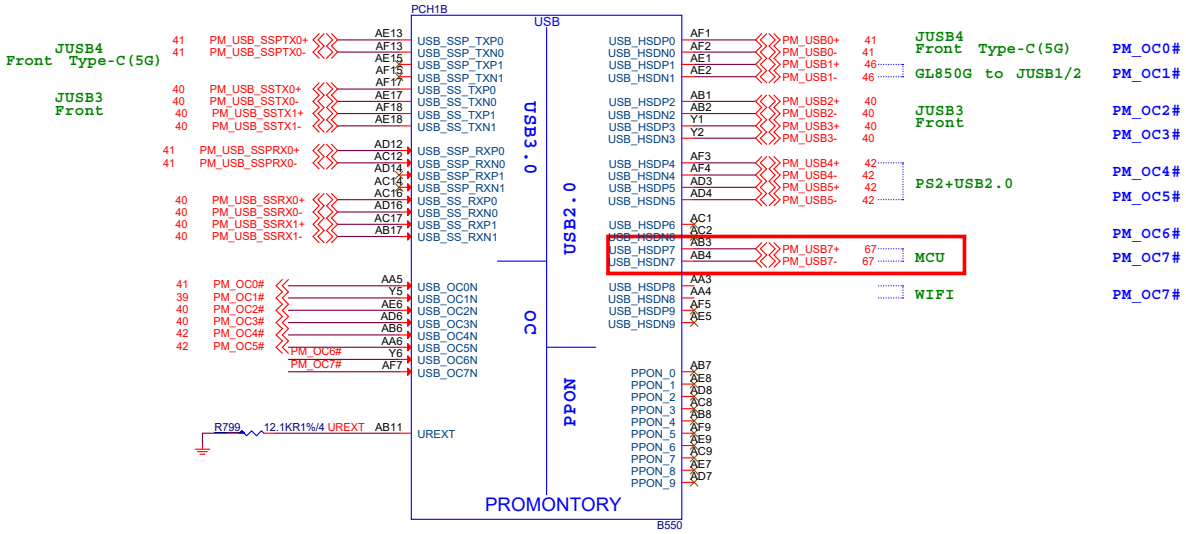
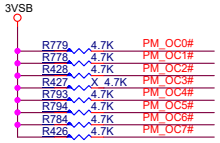
MS-7C91..		
Size: Custom	Document Description: Premium - PCIE/SATA	Rev: 30
Date: Thursday, July 23, 2020	Sheet 15 of 78	





USB mapping

USB_SSP_TX/RX[0] + USB_HSDP/N[0] + USB_OC0N
USB_SSP_TX/RX[1] + USB_HSDP/N[1] + USB_OC1N

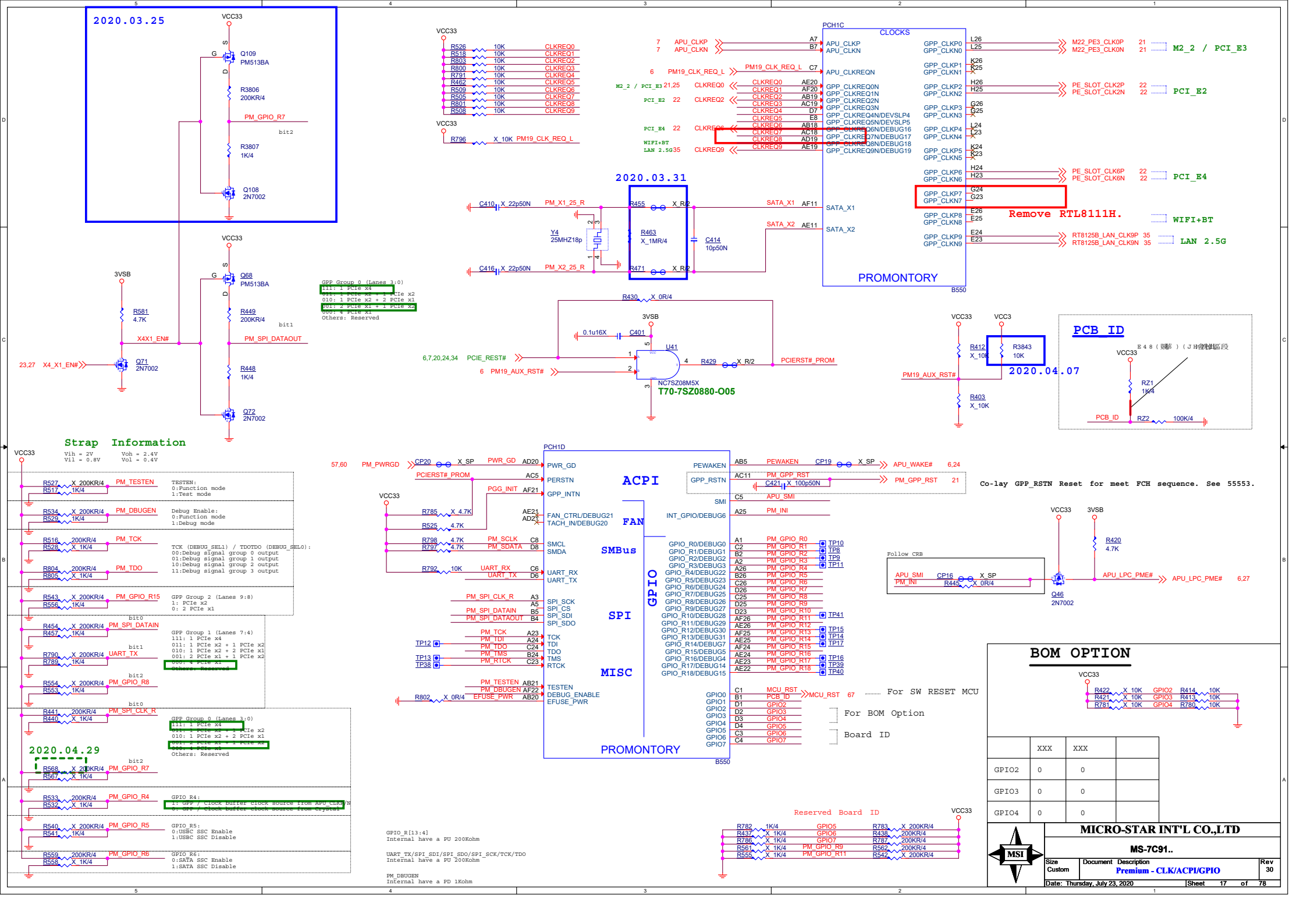
USB_SS_TX/RX[0] + USB_HSDP/N[2] + USB_OC2N
USB_SS_TX/RX[1] + USB_HSDP/N[3] + USB_OC3N
USB_HSDP/N[4] + USB_OC4N
USB_HSDP/N[5] + USB_OC5N
USB_HSDP/N[6] + USB_OC6N
USB_HSDP/N[7] + USB_OC7N
USB_HSDP/N[8] + USB_OC7N
USB_HSDP/N[9] + USB_OC7N

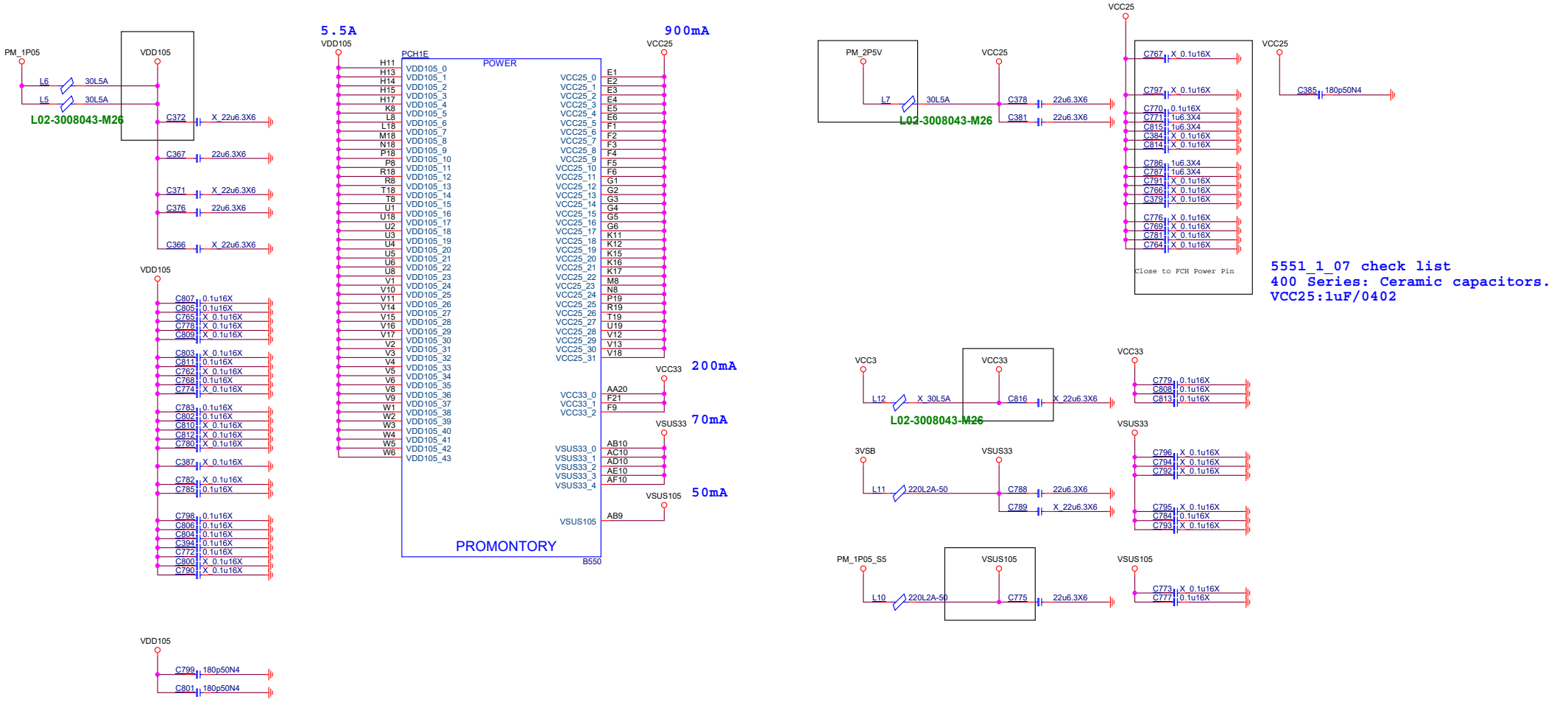
MICRO-STAR INT'L CO.,LTD

MS-7C91..

Size	Document Description	Rev
Custom	Premium - USB/OC	30

Date: Thursday, July 23, 2020 Sheet 16 of 78


2020.03.25
VCC33
Q109
PM513BA
R3806
200KR/4
PM_GPIO_R7
bit2
R3807
1K/4
Q108
2N7002
3VSB
R581
4.7K
X4X1_EN#
23,27 X4_X1_EN#
Q71
2N7002
Q68
PM513BA
R449
200KR/4
bit1
PM_SPI_DATAOUT
R448
1K/4
Q72
2N7002
GPP Group 0 (Lanes 3:0)
111: 1 PCIe x4
010: 1 PCIe x2 + 2 PCIe x1
001: 2 PCIe x1 + 1 PCIe x2
000: 4 PCIe x1
Others: Reserved
Strap Information
Vih = 2V Vil = 0.8V
Voh = 2.4V Vol = 0.4V
R527 X 200KR/4 PM_TESTEN
R517 1K/4
TESTEN:
0:Function mode
1:Test mode
R534 X 200KR/4 PM_DBUGEN
R529 1K/4
Debug Enable:
0:Function mode
1:Debug mode
R516 200KR/4 PM_TCK
R528 X 1K/4
R804 200KR/4 PM_TDO
R805 X 1K/4
TCK (DEBUG_SEL1) / TDOTDO (DEBUG_SEL0):
00:Debug signal group 0 output
01:Debug signal group 1 output
10:Debug signal group 2 output
11:Debug signal group 3 output
R543 X 200KR/4 PM_GPIO_R15
R556 1K/4
GPP Group 2 (Lanes 9:8)
1: PCIe x2
0: 2 PCIe x1
R454 X 200KR/4 PM_SPI_DATAIN
R457 1K/4
bit0
R790 X 200KR/4 UART_TX
R789 1K/4
bit1
GPP Group 1 (Lanes 7:4)
111: 1 PCIe x4
011: 1 PCIe x2 + 1 PCIe x2
010: 1 PCIe x2 + 2 PCIe x1
001: 2 PCIe x1 + 1 PCIe x2
000: 4 PCIe x1
Others: Reserved
R554 X 200KR/4 PM_GPIO_R8
R553 1K/4
bit2
R441 200KR/4 PM_SPI_CLK_R
R440 X 1K/4
bit0
2020.04.29
R568 X 200KR/4 PM_GPIO_R7
R567 X 1K/4
bit2
R533 200KR/4 PM_GPIO_R4
R532 X 1K/4
GPIO_R4:
1: GPP / Clock Buffer Clock Source from APU CLK/N
0: GPP / Clock Buffer Clock Source from Crystal
R540 X 200KR/4 PM_GPIO_R5
R541 1K/4
GPIO_R5:
0:USBC SSC Enable
1:USBC SSC Disable
R559 200KR/4 PM_GPIO_R6
R558 X 1K/4
GPIO_R6:
0:SATA SSC Enable
1:SATA SSC Disable
VCC33
R526 10K CLKREQ0
R518 10K CLKREQ1
R803 10K CLKREQ2
R800 10K CLKREQ3
R791 10K CLKREQ4
R462 10K CLKREQ5
R509 10K CLKREQ6
R505 10K CLKREQ7
R801 10K CLKREQ8
R508 10K CLKREQ9
R796 X 10K PM19_CLK_REQ_L
PCH1C
CLOCKS
7 APU_CLKP
7 APU_CLKN
APU_CLKREQN
6 PM19_CLK_REQ_L
M2_2 / PCI_E3 21,25 CLKREQ0
PCI_E2 22 CLKREQ2
PCI_E4 22 CLKREQ6
WIFI+BT
LAN 2.5G 35 CLKREQ9
GPP_CLKREQ0N/DEBUG16
GPP_CLKREQ1N/DEBUG17
GPP_CLKREQ2N/DEBUG18
GPP_CLKREQ3N/DEBUG19
GPP_CLKP0 L26
GPP_CLKN0 L25
M22_PE3_CLK0P 21
M22_PE3_CLK0N 21
M2_2 / PCI_E3
GPP_CLKP2 H26
GPP_CLKN2 H25
PE_SLOT_CLK2P 22
PE_SLOT_CLK2N 22
PCI_E2
GPP_CLKP6 H24
GPP_CLKN6 H23
PE_SLOT_CLK6P 22
PE_SLOT_CLK6N 22
PCI_E4
GPP_CLKP7 G24
GPP_CLKN7 G23
Remove RTL8111H.
GPP_CLKP8 E26
GPP_CLKN8 E25
WIFI+BT
GPP_CLKP9 E24
GPP_CLKN9 E23
RT8125B_LAN_CLK9P 35
RT8125B_LAN_CLK9N 35
LAN 2.5G
PROMONTORY
B550
2020.03.31
C410 X 22p50N PM_X1_25_R
C416 X 22p50N PM_X2_25_R
Y4
25MHZ18p
R455 X R/2
R463 X_1MR/4
R471 X R/2
C414 10p50N
SATA_X1 AF11
SATA_X2 AE11
R430 X 0R/4
C401 0.1u16X
U41
NC7SZ08M5X
T70-7SZ0880-O05
6,7,20,24,34 PCIE_REST#
6 PM19_AUX_RST#
R429 X R/2
PCIERST#_PROM
VCC33
VCC3
R412 X 10K
R3843 10K
2020.04.07
PM19_AUX_RST#
R403 X 10K
PCB ID
VCC33
RZ1 1K/4
PCB_ID
RZ2 100K/4
PCH1D
ACPI
FAN
SMBus
SPI
MISC
GPIO
PWR_GD AD20
PERSTN AC5
GPP_INTN AF21
FAN_CTRL/DEBUG21 AE21
TACH_IN/DEBUG20 AD21
SMCL C8
SMDA D8
UART_RX C6
UART_TX D6
SPI_SCK A3
SPI_CS A5
SPI_SDI B5
SPI_SDO B4
TCK A23
TDI A24
TDO C24
TMS B24
RTCK C23
TESTEN AB21
DEBUG_ENABLE AF22
EFUSE_PWR AB20
57,60 PM_PWRGD
CP20 X_SP
PCIERST#_PROM
PGG_INIT
R785 X 4.7K
R525 4.7K
R798 4.7K PM_SCLK
R797 4.7K PM_SDATA
R792 10K UART_RX
PM_SPI_CLK_R
PM_SPI_DATAIN
PM_SPI_DATAOUT
PM_TCK
PM_TDI
PM_TDO
PM_TMS
PM_RTCK
TP12
TP13
TP38
PM_TESTEN
PM_DBUGEN
R802 X 0R/4 EFUSE_PWR
PEWAKEN AB5
GPP_RSTN AC11
SMI C5
INT_GPIO/DEBUG6 A25
GPIO_R0/DEBUG0 A1
GPIO_R1/DEBUG1 C2
GPIO_R2/DEBUG2 B2
GPIO_R3/DEBUG3 A2
GPIO_R4/DEBUG22 A26
GPIO_R5/DEBUG23 B26
GPIO_R6/DEBUG24 C26
GPIO_R7/DEBUG25 D26
GPIO_R8/DEBUG26 C25
GPIO_R9/DEBUG27 D25
GPIO_R10/DEBUG28 D23
GPIO_R11/DEBUG29 AF26
GPIO_R12/DEBUG30 AE26
GPIO_R13/DEBUG31 AF25
GPIO_R14/DEBUG7 AE25
GPIO_R15/DEBUG5 AF24
GPIO_R16/DEBUG4 AE24
GPIO_R17/DEBUG14 AE23
GPIO_R18/DEBUG15 AE22
PEWAKEN CP19 X_SP APU_WAKE# 6,24
PM_GPP_RST 21
C421 X 100p50N
APU_SMI
PM_INI A25
PM_GPIO_R0 TP10
PM_GPIO_R1 TP8
PM_GPIO_R2 TP9
PM_GPIO_R3 TP11
PM_GPIO_R10 TP41
PM_GPIO_R13 TP15
PM_GPIO_R14 TP14
PM_GPIO_R15 TP17
PM_GPIO_R16 TP16
PM_GPIO_R17 TP39
PM_GPIO_R18 TP40
GPIO0 C1 MCU_RST
GPIO1 B1 PCB_ID
GPIO2 D1
GPIO3 D2
GPIO4 D3
GPIO5 D4
GPIO6 C3
GPIO7 C4
MCU_RST 67
For SW RESET MCU
For BOM Option
Board ID
PROMONTORY
B550
Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.
Follow CRB
APU_SMI
PM_INI
CP16 X_SP
R445 X 0R/4
Q46
2N7002
VCC33
3VSB
R420 4.7K
APU_LPC_PME#
APU_LPC_PME# 6,27
GPIO_R[13:4]
Internal have a PU 200Kohm
UART_TX/SPI_SDI/SPI_SDO/SPI_SCK/TCK/TDO
Internal have a PU 200Kohm
PM_DBUGEN
Internal have a PD 1Kohm
Reserved Board ID
VCC33
R782 1K/4 GPIO5
R437 X 1K/4 GPIO6
R786 X 1K/4 GPIO7
R561 X 1K/4 PM_GPIO_R9
R559 X 1K/4 PM_GPIO_R11
R783 X 200KR/4
R438 200KR/4
R787 200KR/4
R562 200KR/4
R542 X 200KR/4
BOM OPTION
VCC33
R422 X 10K GPIO2 R414 10K
R421 X 10K GPIO3 R413 10K
R781 X 10K GPIO4 R780 10K
XXX XXX
GPIO2 0 0
GPIO3 0 0
GPIO4 0 0
MICRO-STAR INT'L CO.,LTD
MS-7C91..
Size Custom
Document Description Premium - CLK/ACPI/GPIO
Rev 30
Date: Thursday, July 23, 2020
Sheet 17 of 78



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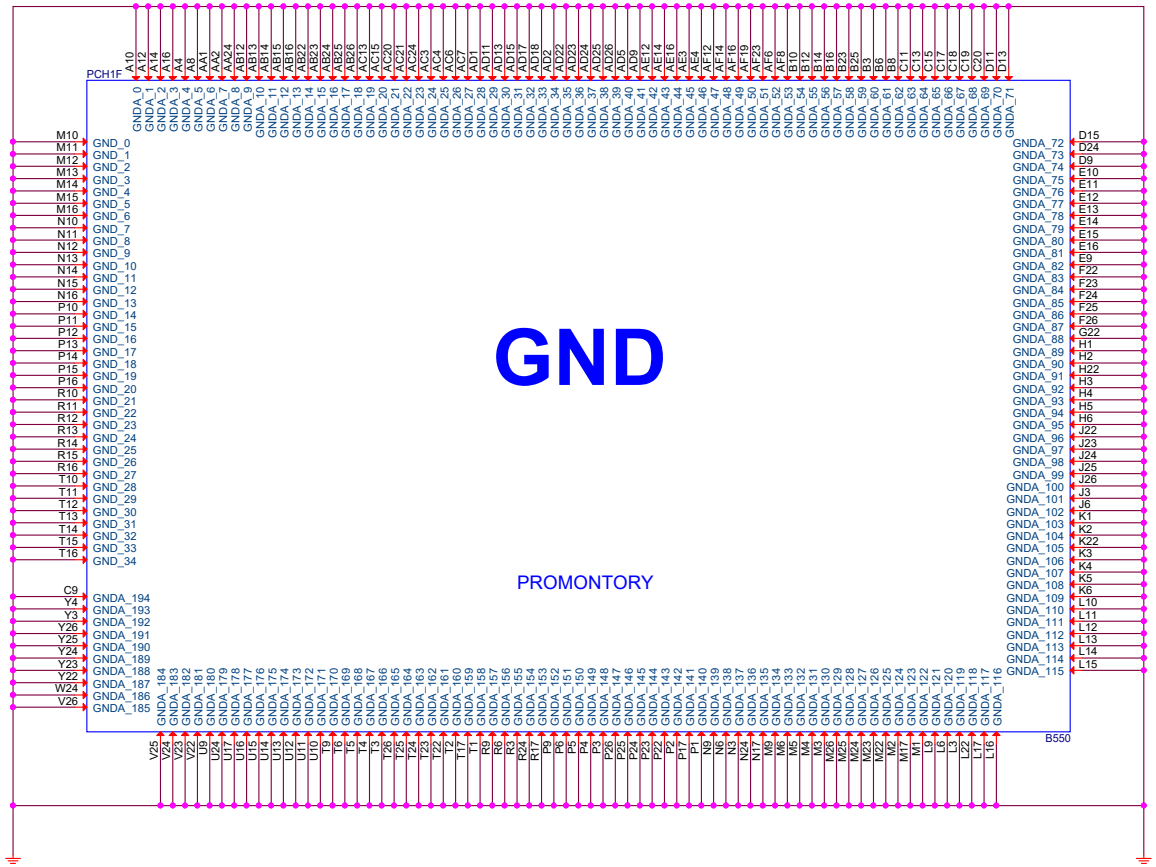
MS-7C91..		
Size: Custom	Document Description: Premium - Power	Rev: 30
Date: Thursday, July 23, 2020	Sheet 18 of 78	



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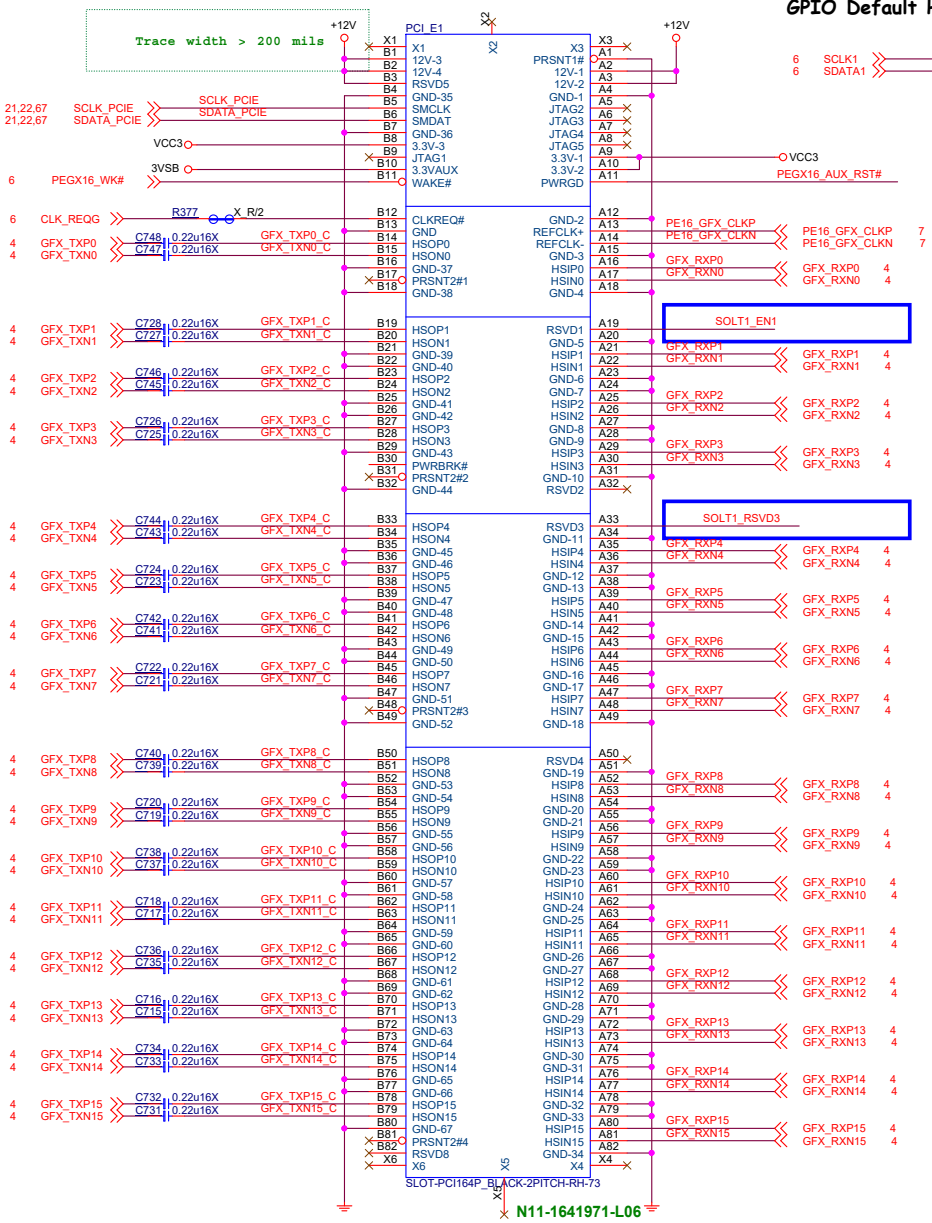
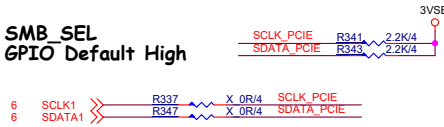
MS-7C91..	
Size: Custom	Document Description: Premium - GND
Rev: 30	
Date: Thursday, July 23, 2020	Sheet 19 of 78

PCI EXPRESS x16 Slot

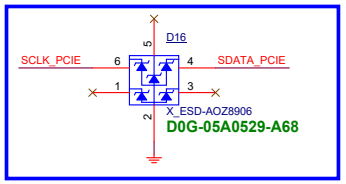
PCI_E1

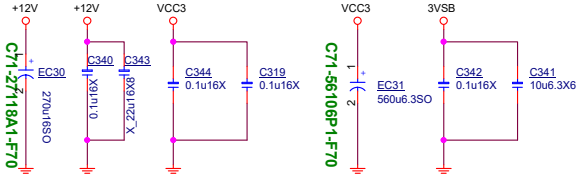


SMB_SEL
GPIO Default High



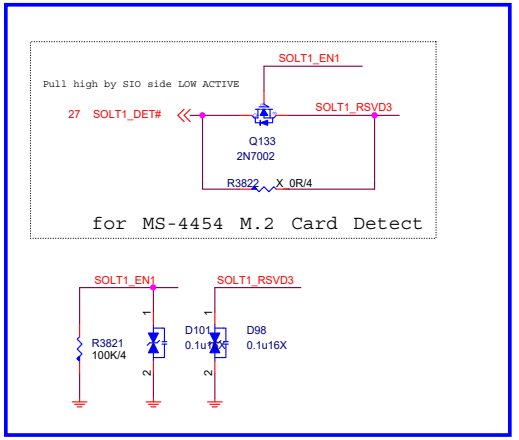
2020.04.06

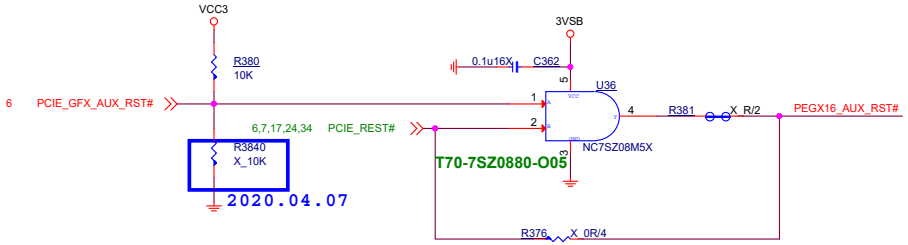




2020.03.25

2020.03.25





PCI Express x16 Slot		
+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

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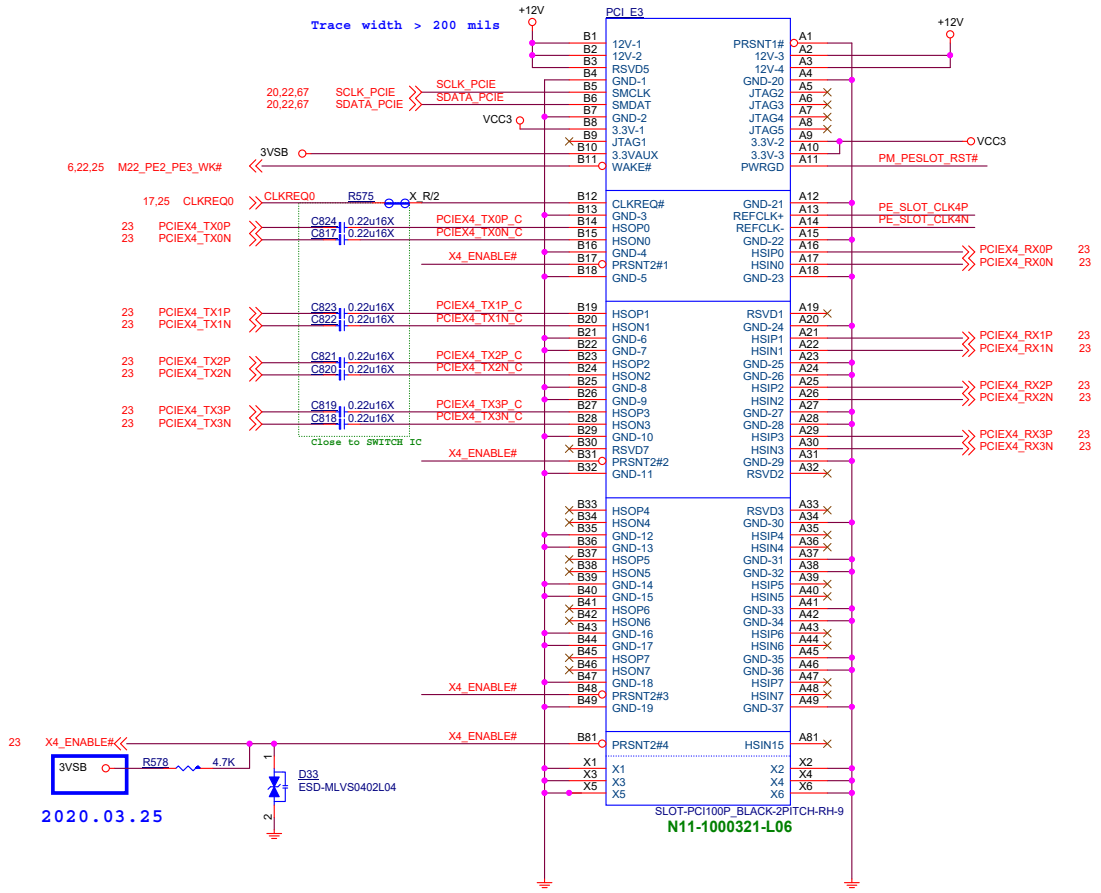
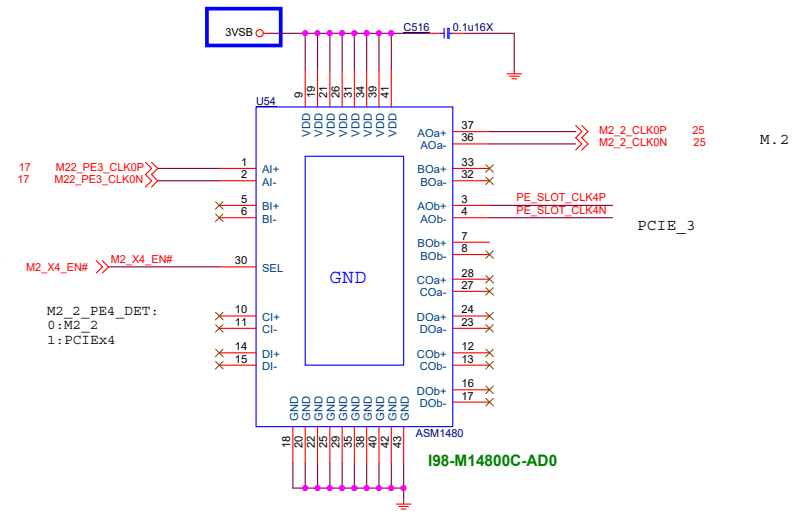
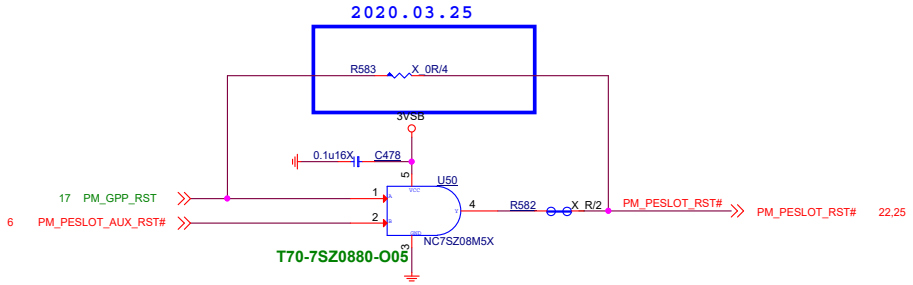
MS-7C91..		
Size: Custom	Document Description: PCI_E2 (X16)	Rev: 30
Date: Thursday, July 23, 2020	Sheet 20 of 78	

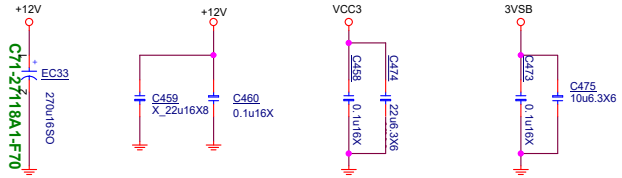
PCI_EXPRESS x4 SLOT

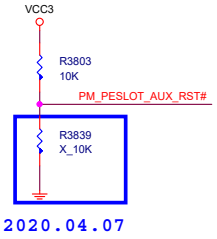
PCI_E3 X4











PCI Express x4 Slot		
+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

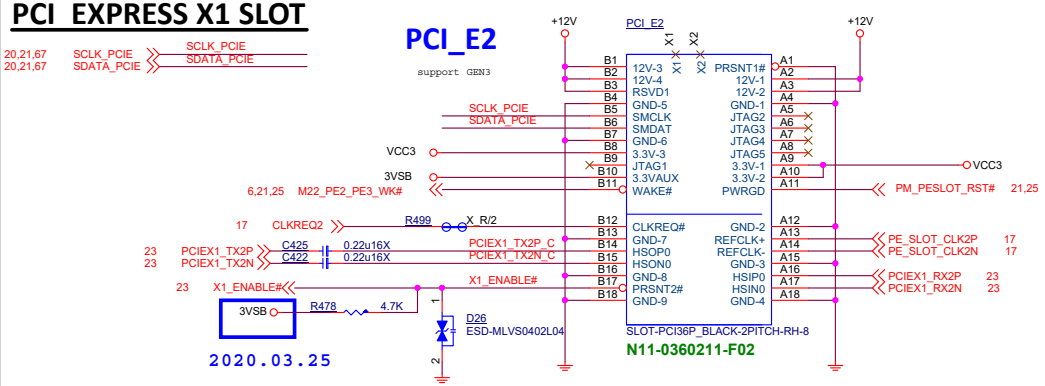
MICRO-STAR INT'L CO.,LTD

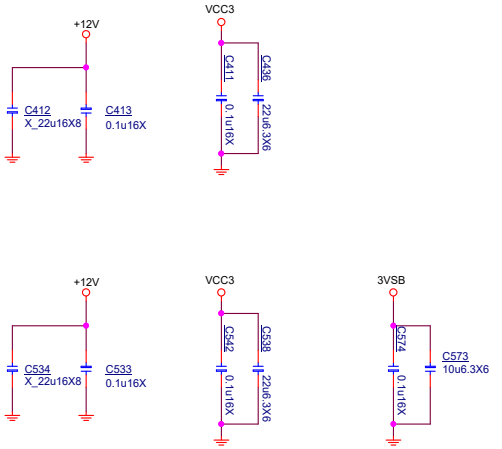
MS-7C91..

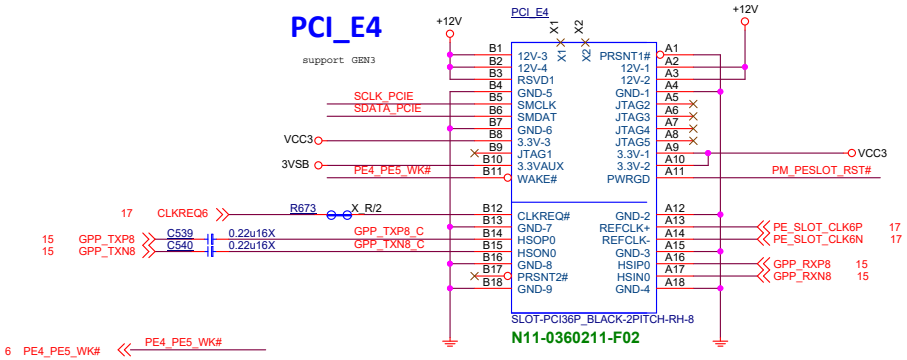
Size: Custom | Document Description: PCI_E3 (X4) | Rev: 30

Date: Thursday, July 23, 2020 | Sheet 21 of 78

PCI_EXPRESS X1 SLOT



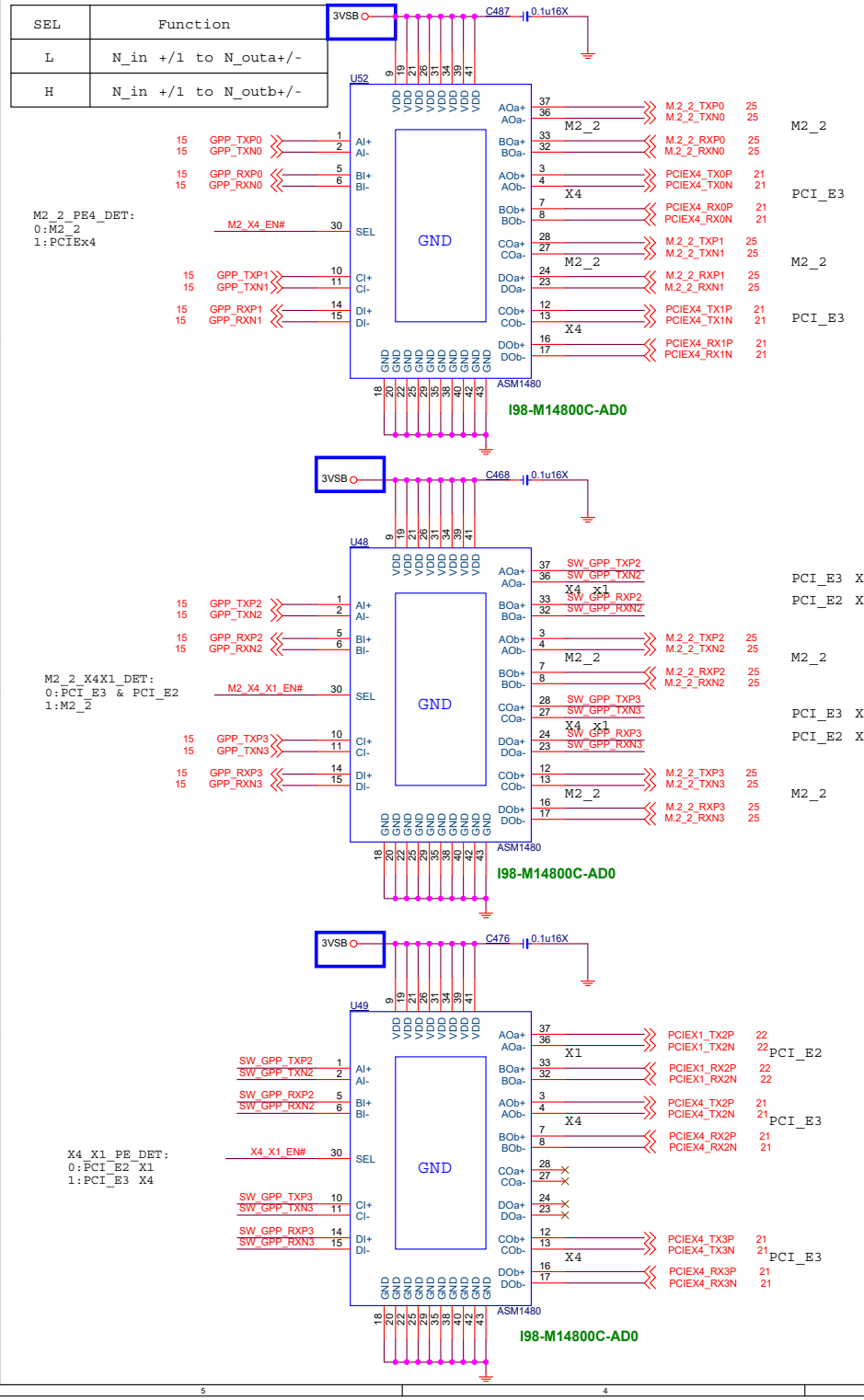




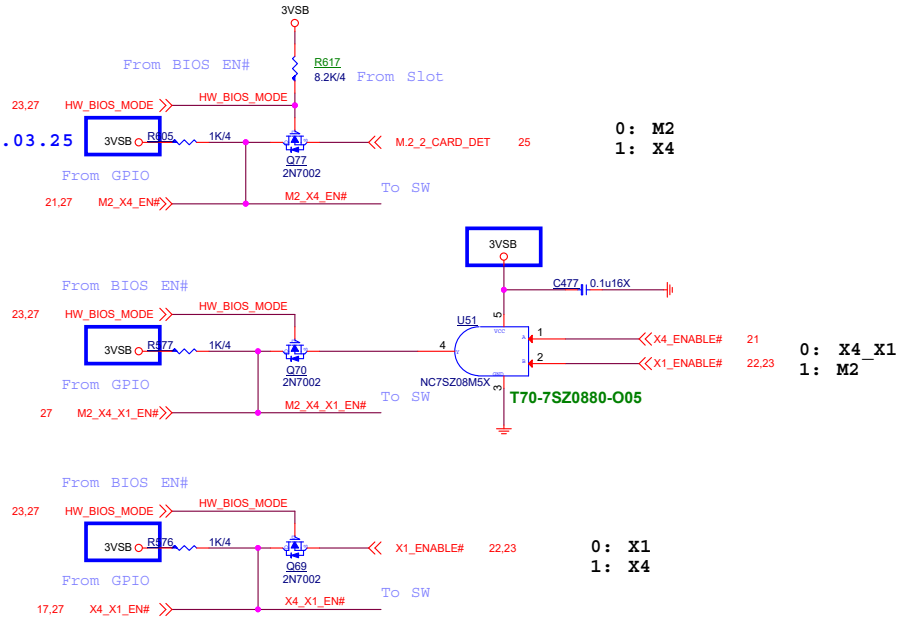
PCI Express x1 Slot *3	
+12V	- 1.5 A
+VCC3	- 9A
+3V3_S5 (wake)	- 1.125A
+3V3_S5 (no wake)	- 20mA

MICRO-STAR INT'L CO.,LTD	
MS-7C91..	
Size: Custom	Document Description: PCI_E2/E4_X1
Rev: 30	
Date: Thursday, July 23, 2020	Sheet 22 of 78

SEL	Function
L	N_in +/1 to N_outa+/-
H	N_in +/1 to N_outb+/-



PCIE Lanes control circuit



HW_BIOS_MODE = High(HW MODE)

DEVICE	M2_2 X4	●(4)	X	X	●(2)	●(2)	X	X	●(2)
	PCI_E3 X4	X	●(4)	X	●(0)	X	●(2)	X	●(0)
	PCI_E2 X1	X	X	●(1)	X	●(1)	●(1)	X	●(1)
DETECT	M.2_2_CARD_DET	O	1	1	O	O	1	1	O
	X1_ENABLE#	1	1	O	1	O	O	1	O
	X4_ENABLE#	1	O	1	O	1	O	1	O

●(X) = availability Lanes number

HW_BIOS_MODE = Low(BIOS MODE)

BIOS GPIO SWITCH	M2_X4_EN#	O	O	O	O	1	1	1	1
	M2_X4_X1_EN#	O	O	1	1	O	O	1	1
	X4_X1_EN#	O	1	O	1	O	1	O	1
DEVICE	M2_2 X4	●(2)	●(2)	●(4)	●(4)	●(0)	●(0)	●(0)	●(0)
	PCI_E3 X4	●(0)	●(0)	●(0)	●(0)	●(2)	●(4)	●(2)	●(2)
	PCI_E2 X1	●(1)	●(0)	●(0)	●(0)	●(1)	●(0)	●(0)	●(0)

MICRO-STAR INT'L CO.,LTD

MS-7C91..

Size	Document Description	Rev
Custom	PCIE GEN3 SWITCH	30

Date: Thursday, July 23, 2020 Sheet 23 of 78

M.2_1 Connector

VCC3 4.25A
Max: 14W

M2下零件数限高要小於09mm的零件

LANE REVERSE TO SUPPORT SATA SSD

2020.03.25

Close to PIN2,4

Close to PIN12, 14, 16, 18

Close to PIN70, 72, 74

PIN 69
Low SATA
NC PCIE

M.2_CARD_DET:
0:Have M.2
1:No M.2

KEY M

SLOT-NGFFCARD67P_BLACK-HF-88

PCIE/SATA Mode

PLN#

2020.04.07

T70-7SZ0880-O05

2020.03.25 SMBUS Level Shift IC 2020.04.16

pull high ESIO SIDE

close to U81

CPU Side pull high 4.7K

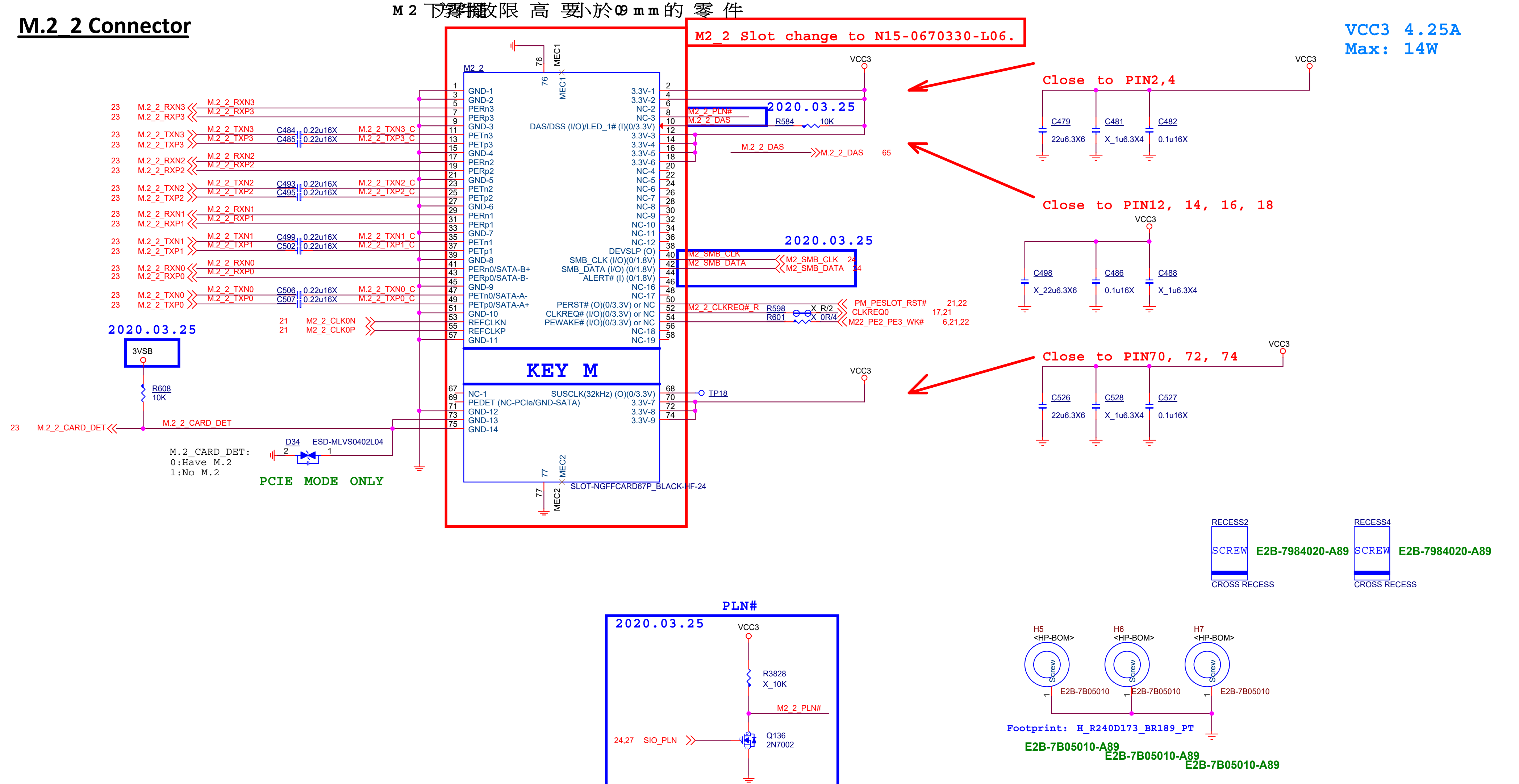
Footprint: H_R240D173_BR189_PT

E2B-7B05010-A89

E2B-7984020-A89

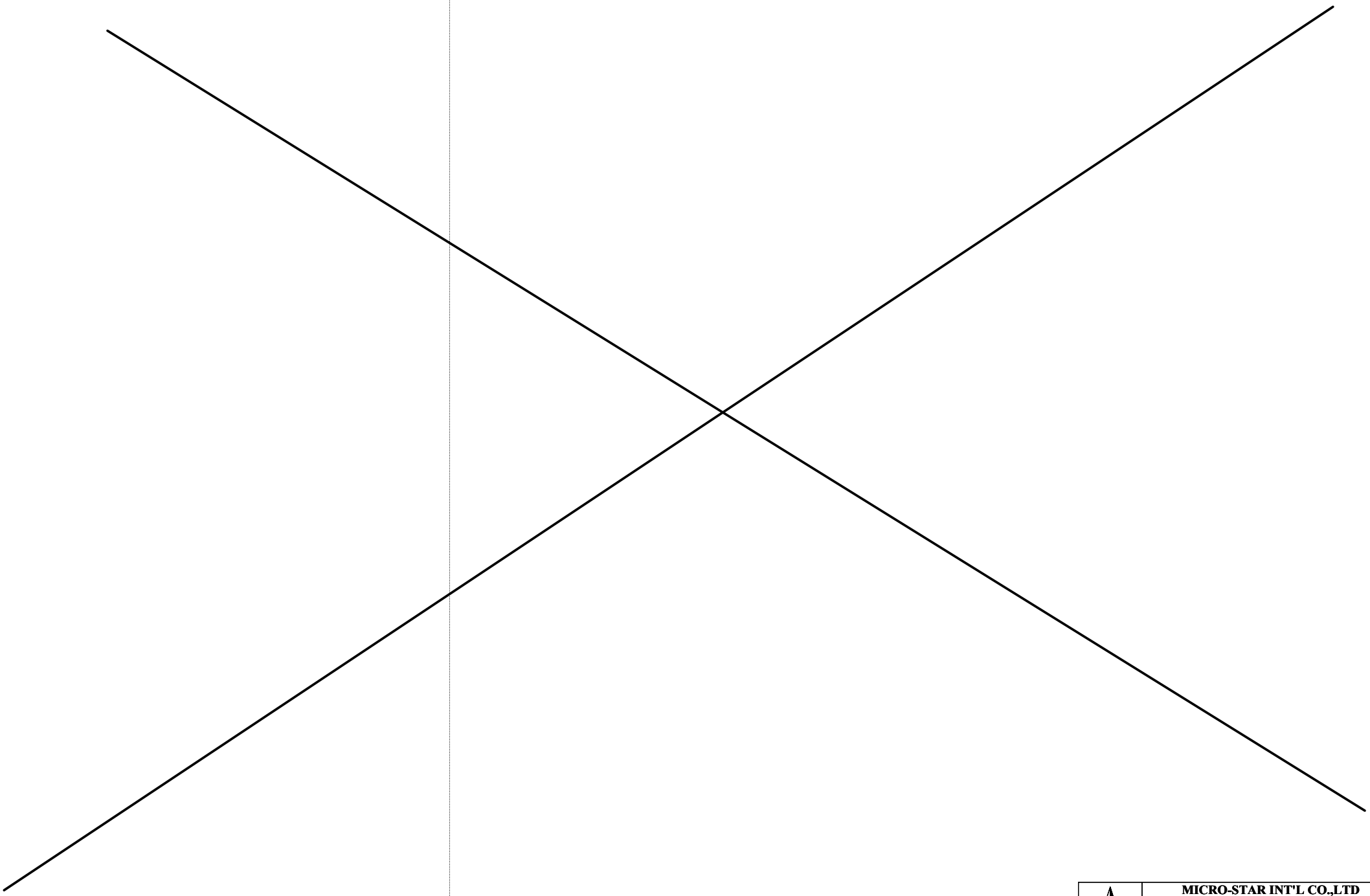
MICRO-STAR INT'L CO.,LTD		
MS-7C91..		
Size: Custom	Document Description: M2_1 PCIE/SATA Mode(KEY_M)	Rev: 30
Date: Thursday, July 23, 2020	Sheet 24 of 78	

M.2_2 Connector

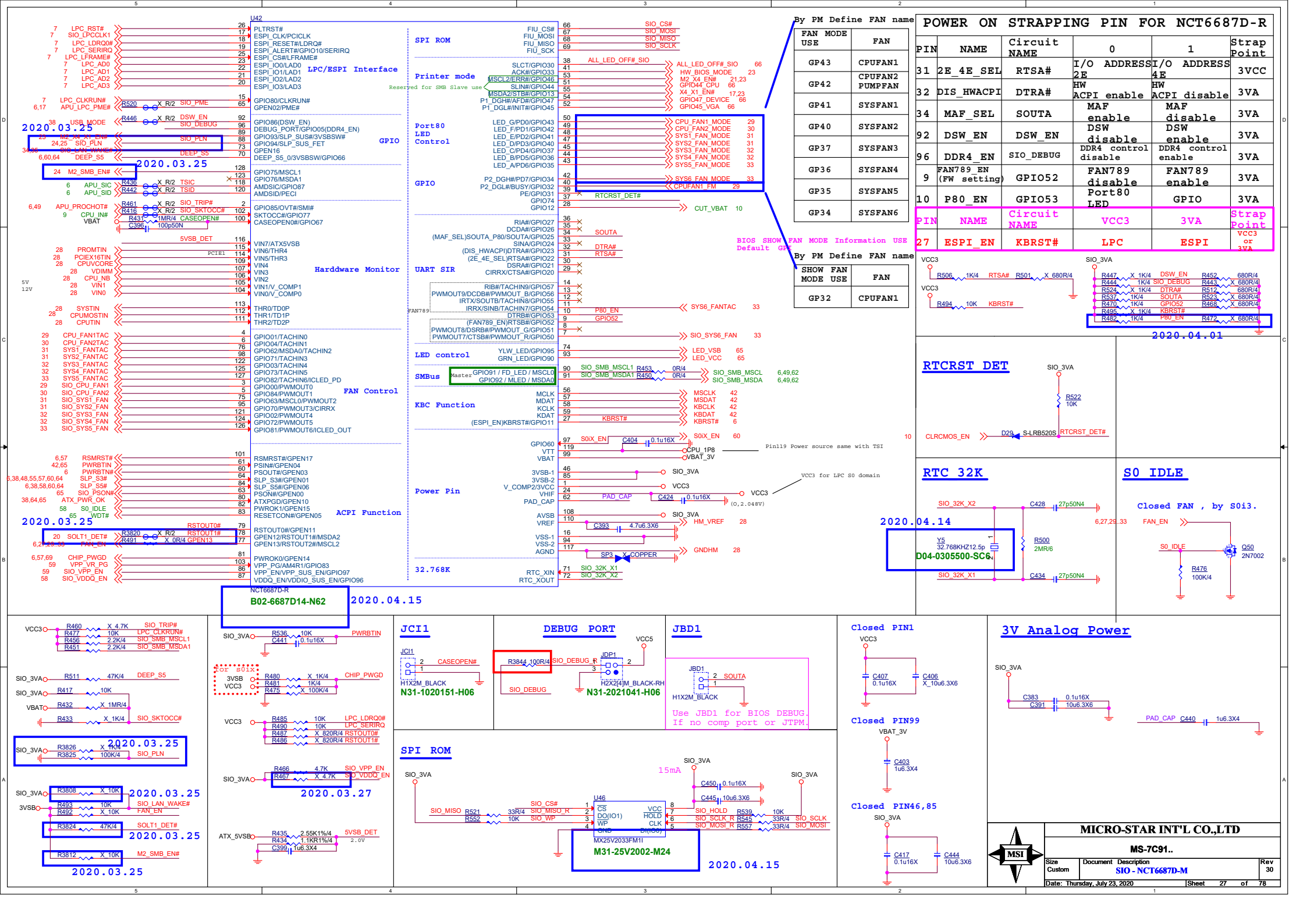


M2_2 Slot change to N15-0670330-L06.
VCC3 4.25A
Max: 14W
Close to PIN2,4
Close to PIN12, 14, 16, 18
Close to PIN70, 72, 74
2020.03.25
KEY M
M2_2
SLOT-NGFFCARD67P_BLACK-HF-24
GND-1
GND-2
PERn3
PERp3
GND-3
PETn3
PETp3
GND-4
PERn2
PERp2
GND-5
PETn2
PETp2
GND-6
PERn1
PERp1
GND-7
PETn1
PETp1
GND-8
PERn0/SATA-B+
PERp0/SATA-B-
GND-9
PETn0/SATA-A-
PETp0/SATA-A+
GND-10
REFCLKN
REFCLKP
GND-11
3.3V-1
3.3V-2
NC-2
NC-3
DAS/DSS (I/O)/LED_1# (I)(0/3.3V)
3.3V-3
3.3V-4
3.3V-5
3.3V-6
DEVSLP (O)
SMB_CLK (I/O)(0/1.8V)
SMB_DATA (I/O) (0/1.8V)
ALERT# (I) (0/1.8V)
PERST# (O)(0/3.3V) or NC
CLKREQ# (I/O)(0/3.3V) or NC
PEWAKE# (I/O)(0/3.3V) or NC
NC-1
PEDET (NC-PCIe/GND-SATA)
GND-12
GND-13
GND-14
SUSCLK(32kHz) (O)(0/3.3V)
3.3V-7
3.3V-8
3.3V-9
MEC1
MEC2
M.2_2_RXN3
M.2_2_RXP3
M.2_2_TXN3
M.2_2_TXP3
M.2_2_RXN2
M.2_2_RXP2
M.2_2_TXN2
M.2_2_TXP2
M.2_2_RXN1
M.2_2_RXP1
M.2_2_TXN1
M.2_2_TXP1
M.2_2_RXN0
M.2_2_RXP0
M.2_2_TXN0
M.2_2_TXP0
C484 0.22u16X
C485 0.22u16X
C493 0.22u16X
C495 0.22u16X
C499 0.22u16X
C502 0.22u16X
C506 0.22u16X
C507 0.22u16X
M.2_2_CLK0N
M.2_2_CLK0P
M2_2_PLN#
M2_2_DAS
R584 10K
M.2_2_DAS 65
M2_SMB_CLK 24
M2_SMB_DATA 24
M2_2_CLKREQ#_R
R598 X_R/2
R601 X_0R/4
PM_PESLOT_RST# 21,22
CLKREQ0 17,21
M22_PE2_PE3_WK# 6,21,22
TP18
VCC3
C479 22u6.3X6
C481 X_1u6.3X4
C482 0.1u16X
C498 X_22u6.3X6
C486 0.1u16X
C488 X_1u6.3X4
C526 22u6.3X6
C528 X_1u6.3X4
C527 0.1u16X
3VSB
R608 10K
M.2_2_CARD_DET
D34 ESD-MLVS0402L04
M.2_CARD_DET:
0:Have M.2
1:No M.2
PCIE MODE ONLY
RECESS2
SCREW E2B-7984020-A89
RECESS4
SCREW E2B-7984020-A89
CROSS RECESS
PLN#
R3828 X_10K
M2_2_PLN#
24,27 SIO_PLN
Q136 2N7002
H5 <HP-BOM>
H6 <HP-BOM>
H7 <HP-BOM>
E2B-7B05010
Footprint: H_R240D173_BR189_PT
E2B-7B05010-A89

MICRO-STAR INT'L CO.,LTD		
MS-7C91..		
Size: Custom	Document Description: M2_2 PCIE Mode(KEY_M)	Rev: 30
Date: Thursday, July 23, 2020	Sheet 25 of 78	

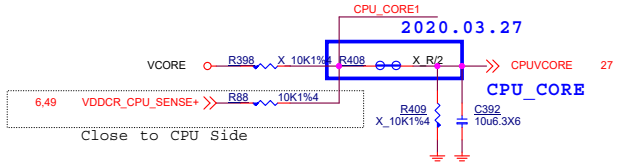


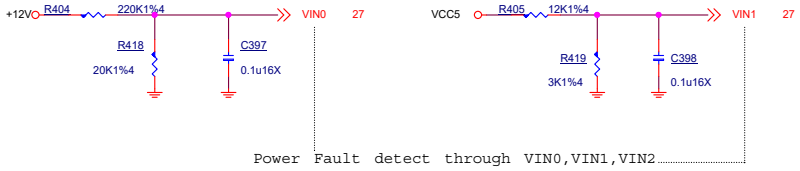
MICRO-STAR INT'L CO.,LTD		
MS-7C91..		
Size: Custom	Document Description: M2_2 - WIFI+BT	Rev: 30
Date: Thursday, July 23, 2020	Sheet 26 of 78	

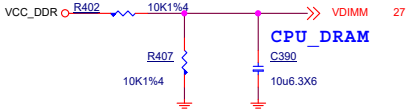

U42
NC16687D-R
B02-6687D14-N62
2020.04.15
LPC/ESPI Interface
GPIO
Harddware Monitor
FAN Control
ACPI Function
SPI ROM
Printer mode
Port80 LED Control
UART SIR
LED control
SMBus
KBC Function
Power Pin
32.768K
By PM Define FAN name
FAN MODE USE
FAN
GP43 CPUFAN1
GP42 CPUFAN2 PUMPFAN
GP41 SYSFAN1
GP40 SYSFAN2
GP37 SYSFAN3
GP36 SYSFAN4
GP35 SYSFAN5
GP34 SYSFAN6
By PM Define FAN name
SHOW FAN MODE USE
FAN
GP32 CPUFAN1
BIOS SHOW FAN MODE Information USE Default GP
POWER ON STRAPPING PIN FOR NCT6687D-R
PIN NAME Circuit NAME 0 1 Strap Point
31 2E_4E_SEL RTSA# I/O ADDRESS 2E I/O ADDRESS 4E 3VCC
32 DIS_HWACPI DTRA# HW ACPI enable HW ACPI disable 3VA
34 MAF_SEL SOUTA MAF enable MAF disable 3VA
92 DSW_EN DSW_EN DSW disable DSW enable 3VA
96 DDR4_EN SIO_DEBUG DDR4 control disable DDR4 control enable 3VA
9 FAN789_EN (FW setting) GPIO52 FAN789 disable FAN789 enable 3VA
10 P80_EN GPIO53 Port80 LED GPIO 3VA
PIN NAME Circuit NAME VCC3 3VA Strap Point
27 ESPI_EN KBRST# LPC ESPI VCC3 or 3VA
2020.04.01
RTCRST DET
RTC 32K
S0 IDLE
Closed FAN , by S0i3.
2020.04.14
D04-0305500-SC6
JCI1
N31-1020151-H06
DEBUG PORT
N31-2021041-H06
JBD1
Use JBD1 for BIOS DEBUG. If no comp port or JTPM.
SPI ROM
M31-25V2002-M24
2020.04.15
Closed PIN1
Closed PIN99
Closed PIN46,85
3V Analog Power
2020.03.25
2020.03.27
MICRO-STAR INT'L CO.,LTD
MS-7C91..
SIO - NCT6687D-M
Date: Thursday, July 23, 2020
Sheet 27 of 78

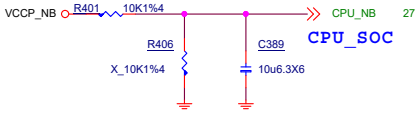
HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect

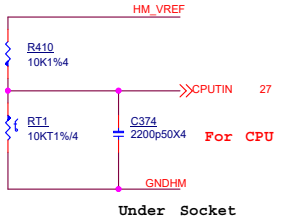


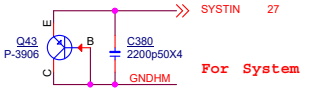


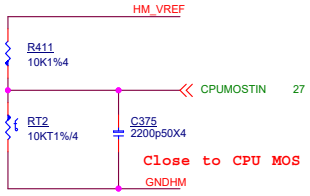


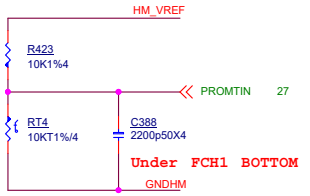


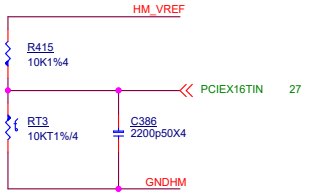
TEMP SENSOR







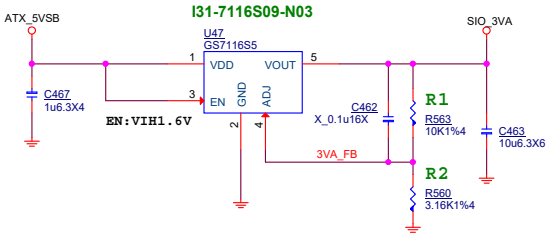




PM RESET

CPU RESET

SIO_3VA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V

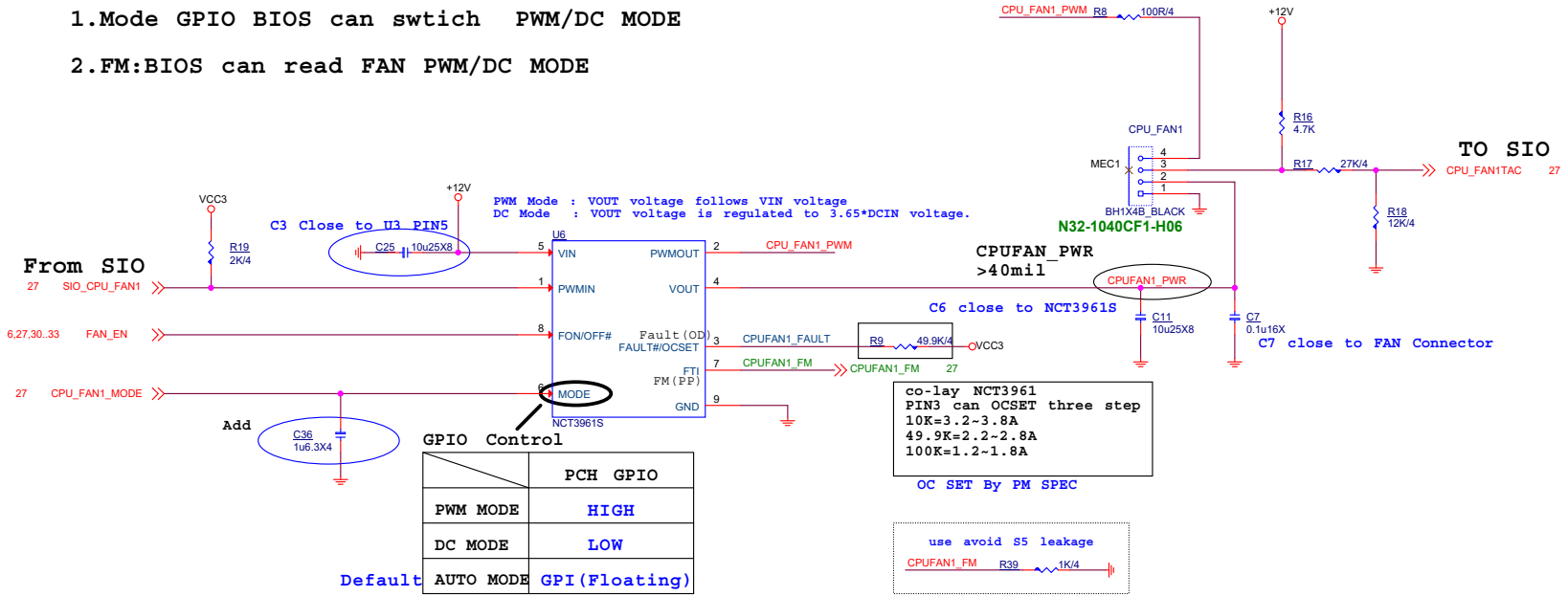
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C91..	
Size: Custom	Document Description: SIO - HW Monitor	Rev: 30
Date: Thursday, July 23, 2020	Sheet 28 of 78	

CPUFAN1

TYPE N : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

2.FM:BIOS can read FAN PWM/DC MODE



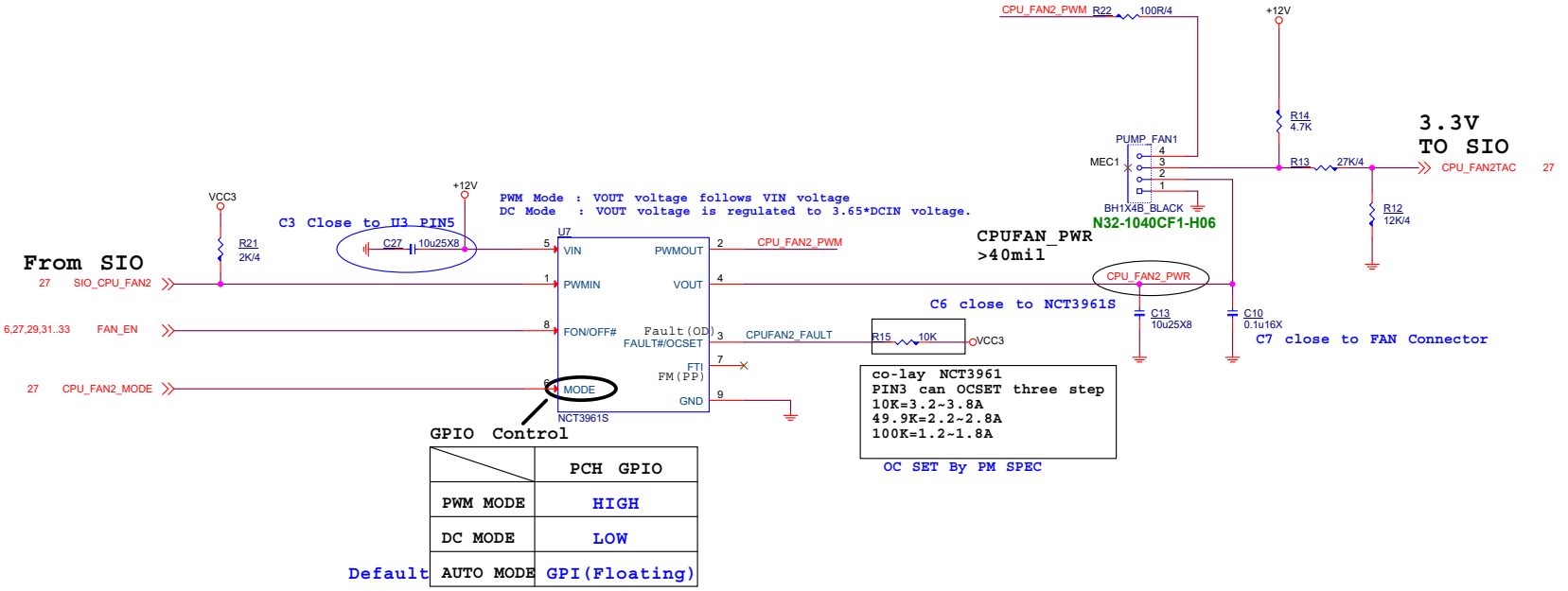
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD	
MS-7C91..	
Size: Custom	Document Description: FAN TYPE-L CPUFAN1
Rev: 30	
Date: Thursday, July 23, 2020	Sheet 29 of 78

PUMPFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



GPIO Control

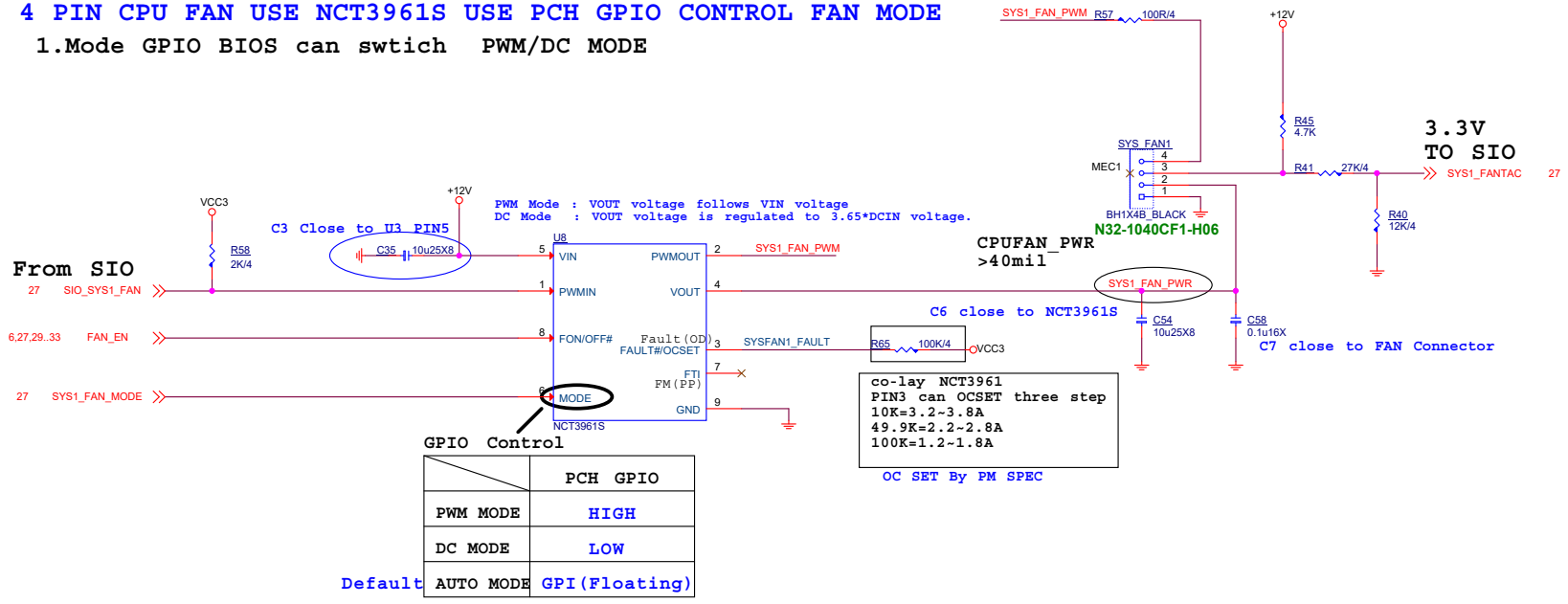
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD	
MS-7C91..	
Size: Custom	Document Description: FAN TYPE-K PUMPFAN1
Rev: 30	
Date: Thursday, July 23, 2020	Sheet 30 of 78

SYSFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

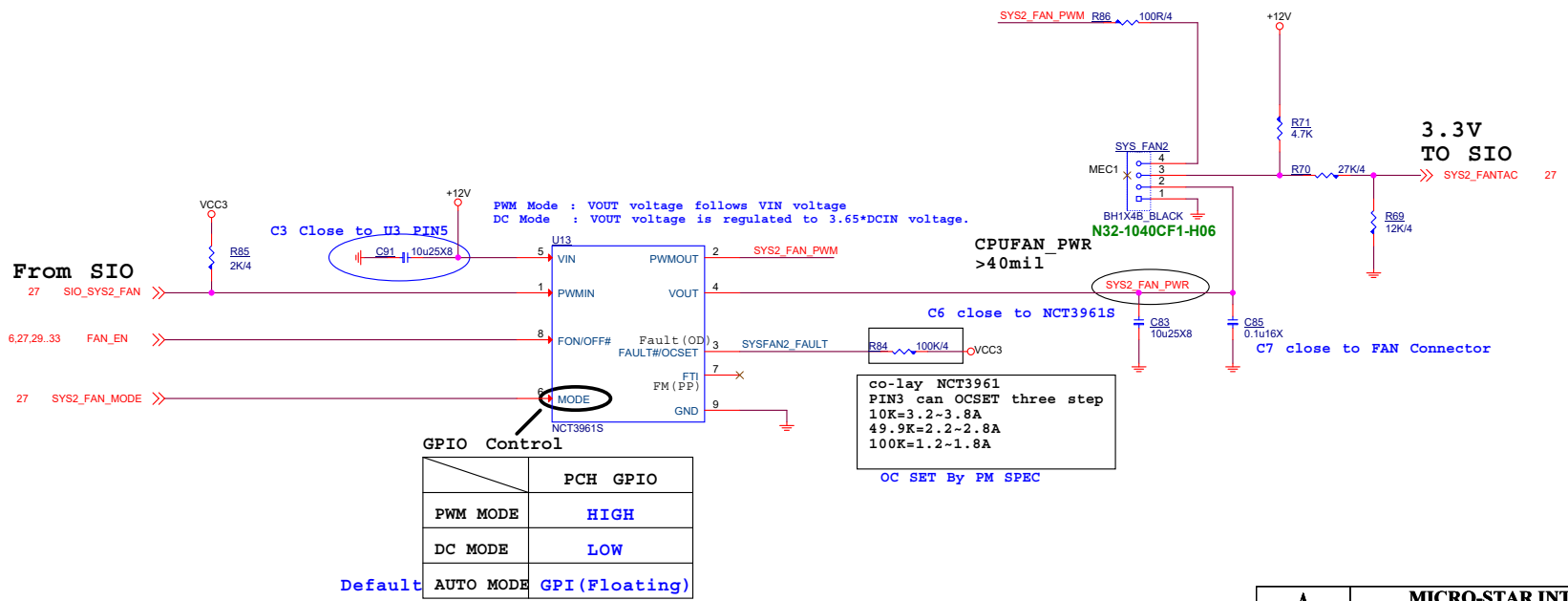


	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

SYSFAN2

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

MS-7C91..

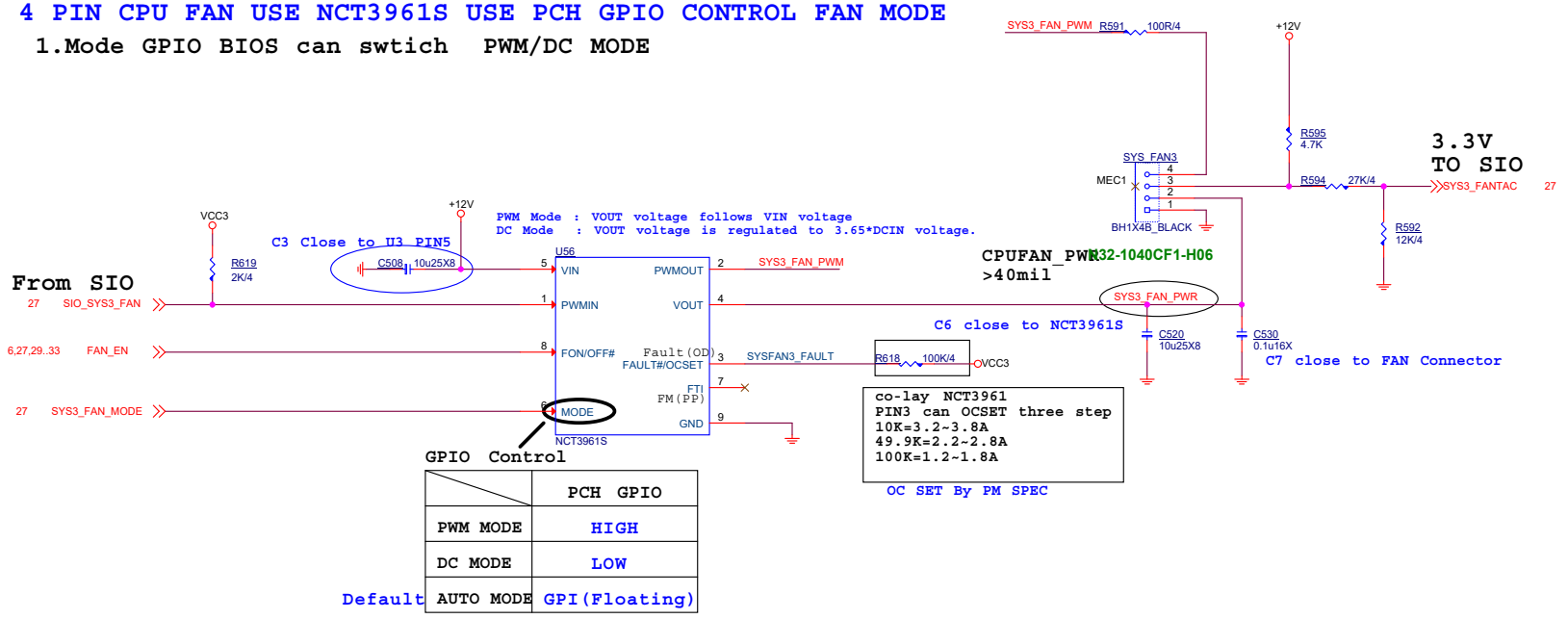
Size: Custom | Document Description: FAN TYPE-K SYSFAN1/2 | Rev: 30

Date: Thursday, July 23, 2020 | Sheet 31 of 78

SYSFAN3

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

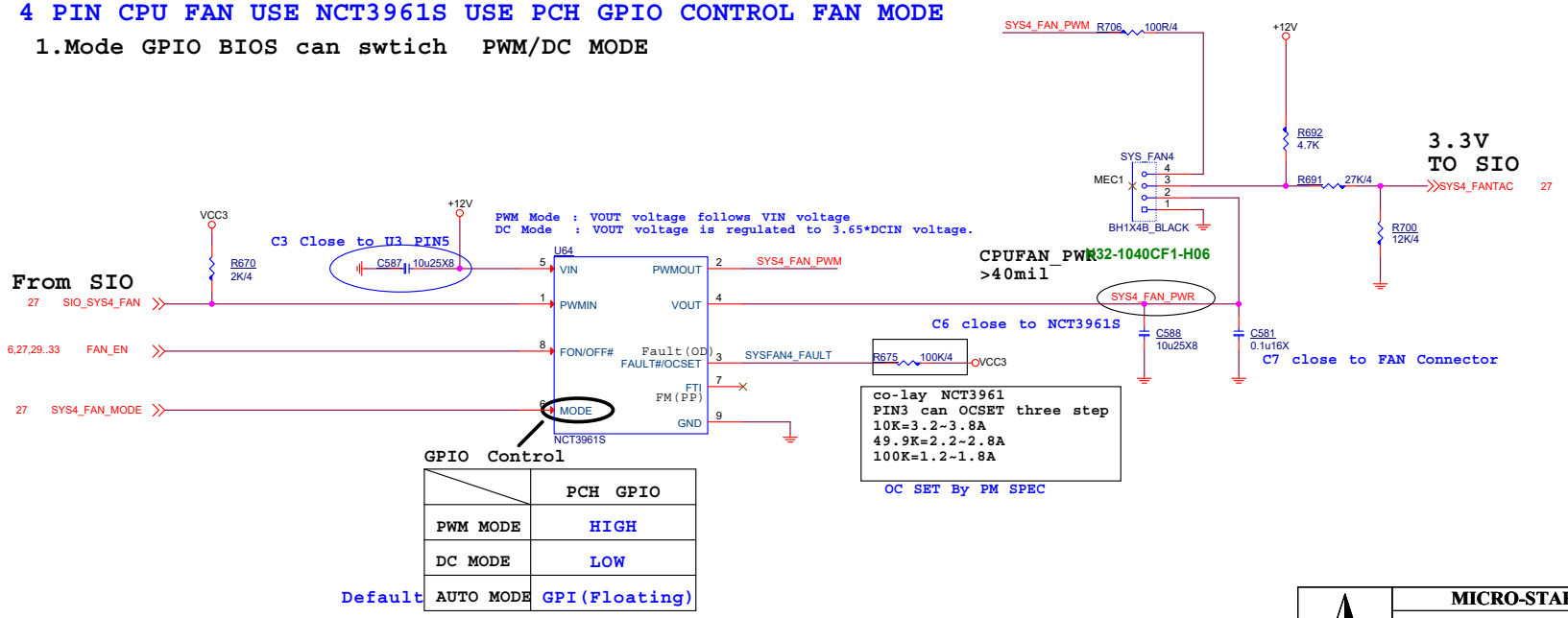


	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

SYSFAN4

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

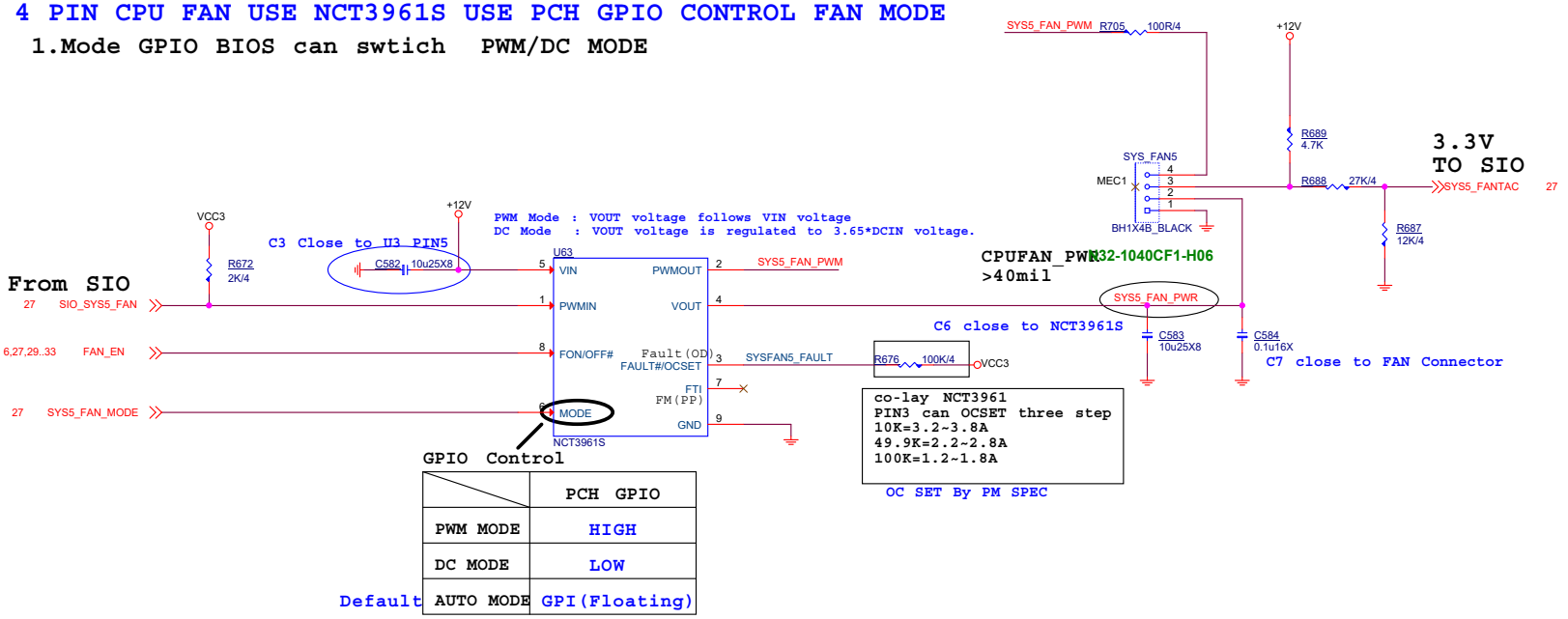
MS-7C91..

Size	Document Description	Rev
Custom	FAN TYPE-K SYSFAN3/4	30

Date: Thursday, July 23, 2020 Sheet 32 of 78

SYSFAN5 TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

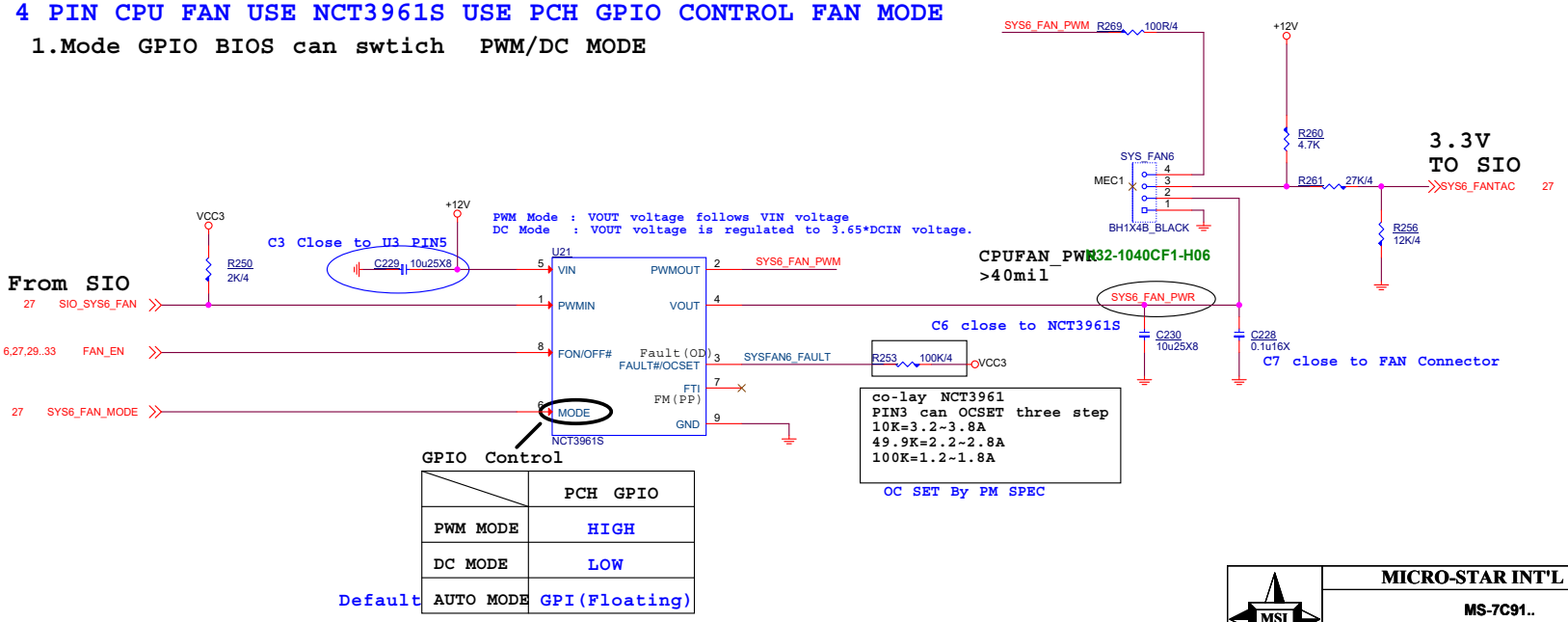
1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

SYSFAN6 TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

MS-7C91..

Size	Document Description	Rev
Custom	FAN TYPE-N SYSFAN5	30

Date: Thursday, July 23, 2020 Sheet 33 of 78

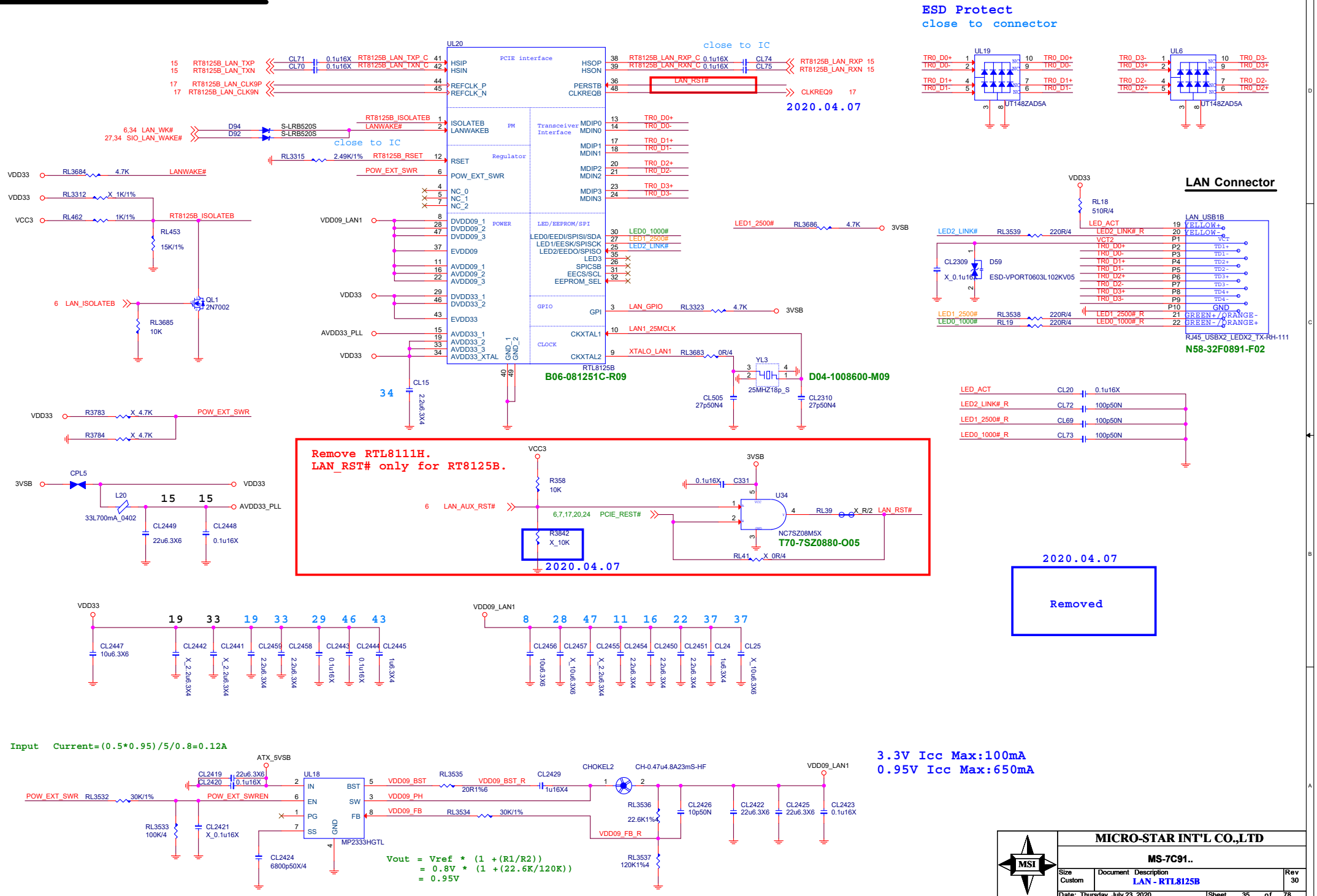
MICRO-STAR INT'L CO.,LTD

MS-7C91..

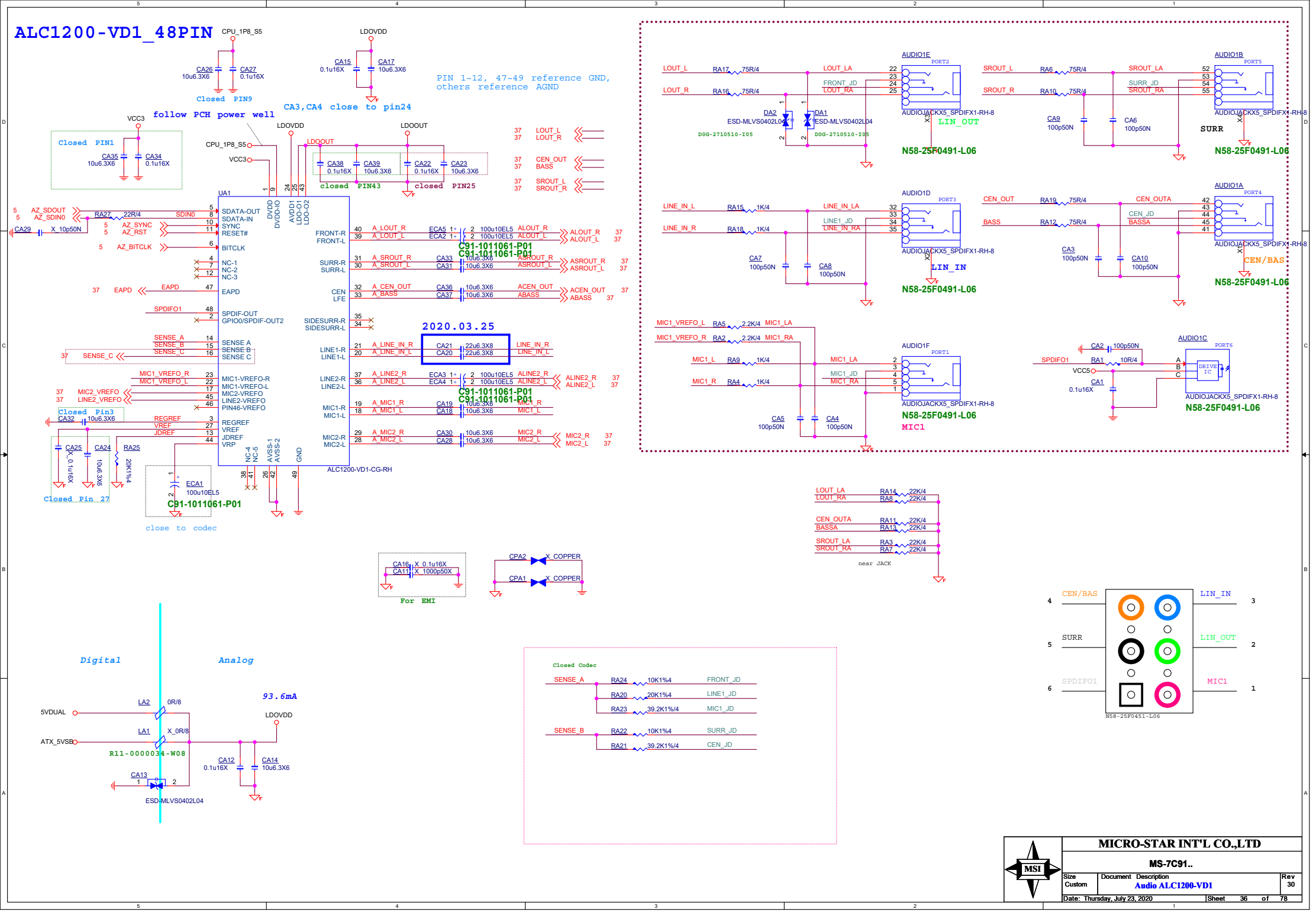
Size	Document Description	Rev
Custom	RTL8111H Giga LAN	30

Date: Thursday, July 23, 2020 | Sheet 34 of 78

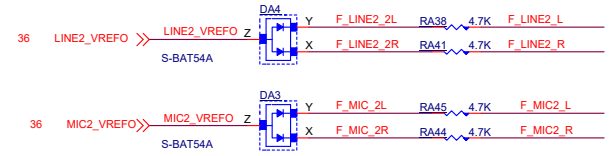
Realtek Lan1-RTL8125B(2.5G)

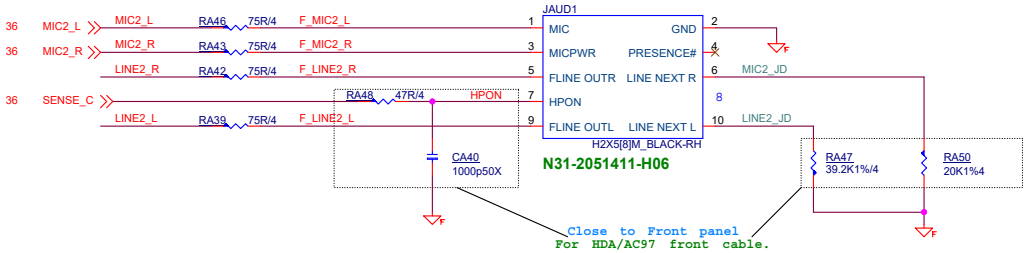


ALC1200-VD1_48PIN



MICRO-STAR INT'L CO.,LTD
MS-7C91..
Size: Custom
Document Description: Audio ALC1200-VD1
Rev: 30
Date: Thursday, July 23, 2020
Sheet 36 of 78

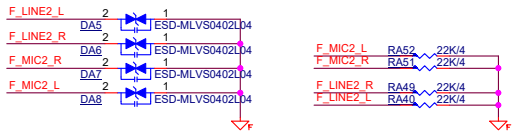




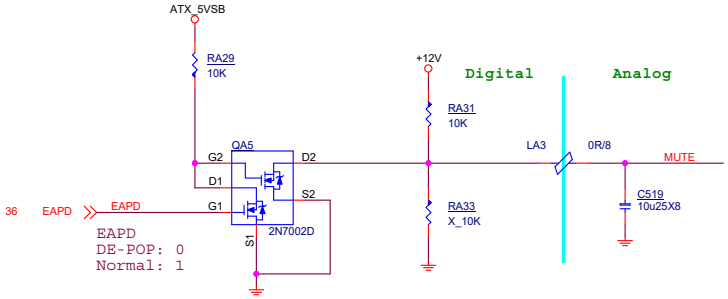
D0G-2710510-I05
Close to Front panel

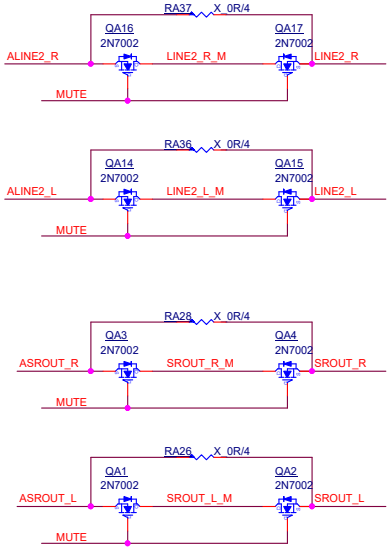
ESD protect

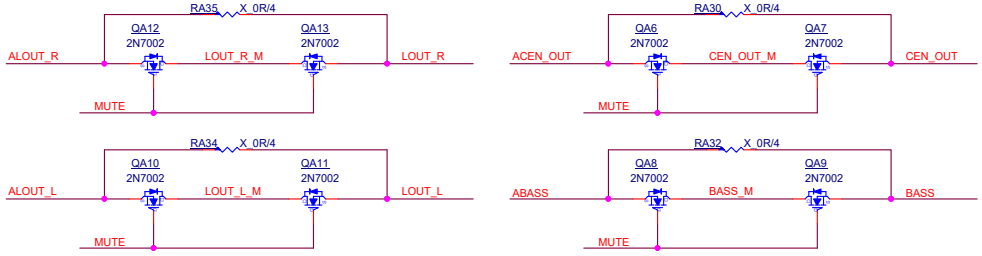
D0G-2710510-I05
AVL:D0G-2950500-SI0

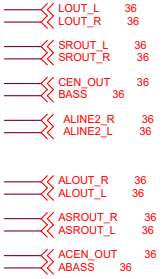


De-POP circuit



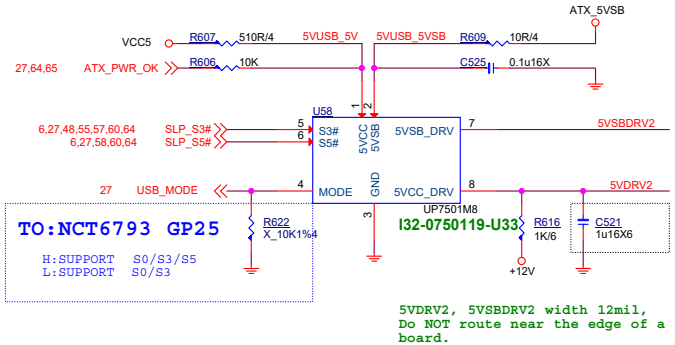


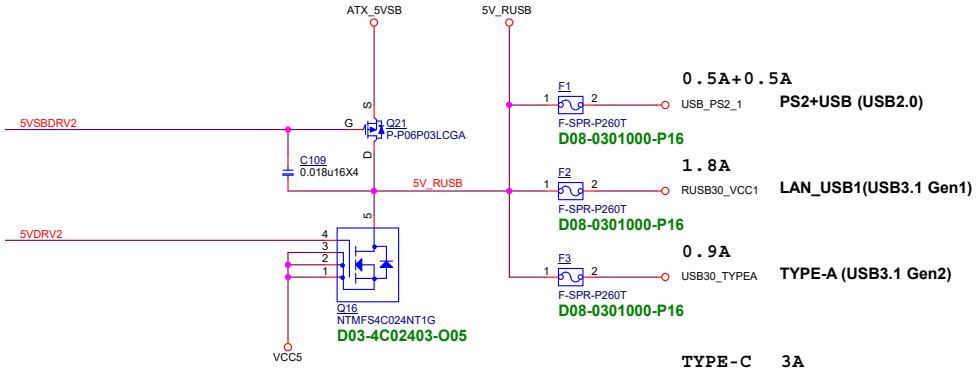




MICRO-STAR INT'L CO.,LTD		
MS-7C91..		
Size: Custom	Document Description: Audio DePop	Rev: 30
Date: Thursday, July 23, 2020	Sheet 37 of 78	

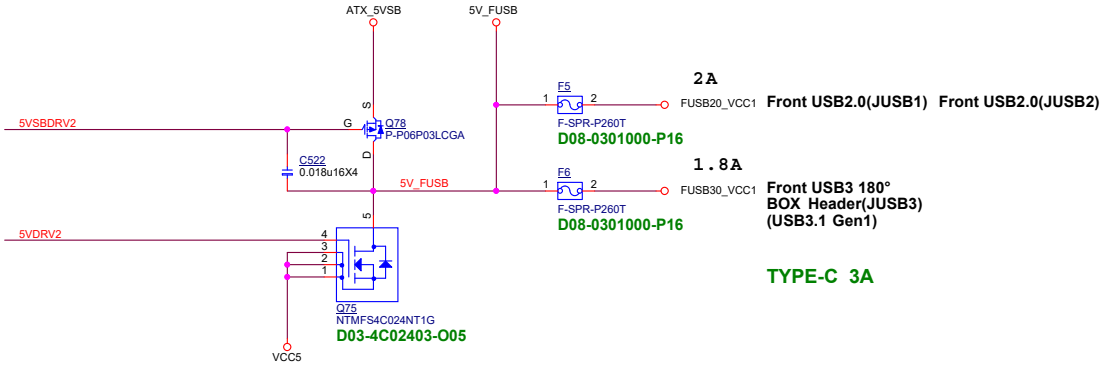
USB Power





Rear (6.7A)

Front (6.8A)



MICRO-STAR INT'L CO.,LTD

MS-7C91..

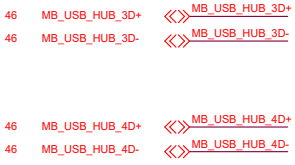
Size	Document Description	Rev
Custom	USB Power - UP7501	30

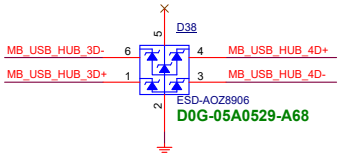
Date: Thursday, July 23, 2020 Sheet 38 of 78

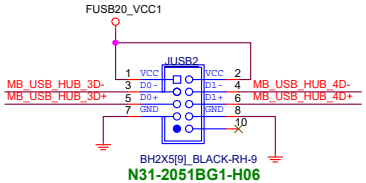
Front USB2.0(JUSB2)

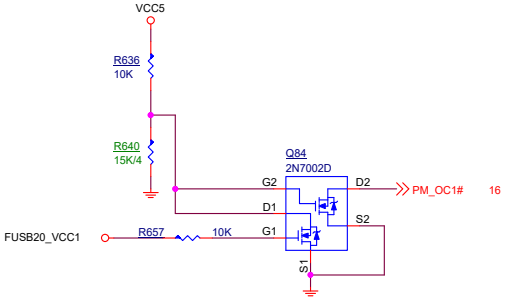
Form GL850G USB2.0 HUB

5V@1A





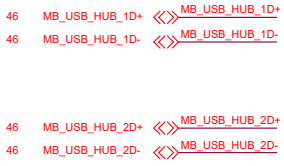


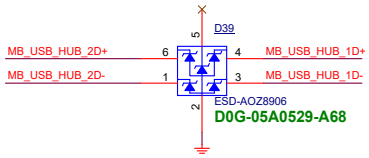


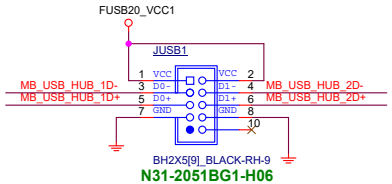
Front USB2.0(JUSB1)

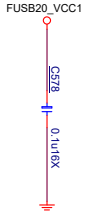
Form GL850G USB2.0 HUB

5V@1A







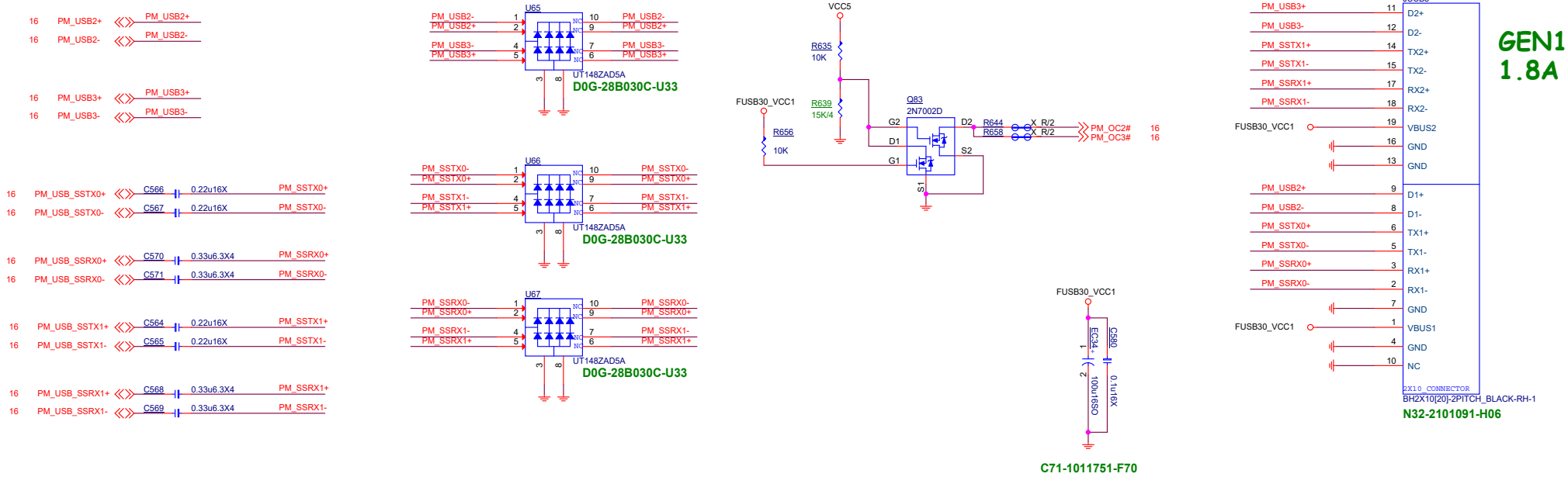


MICRO-STAR INT'L CO.,LTD		
MS-7C91..		
Size: Custom	Document Description: Front USB2.0 Header	Rev: 30
Date: Thursday, July 23, 2020	Sheet 39 of 78	

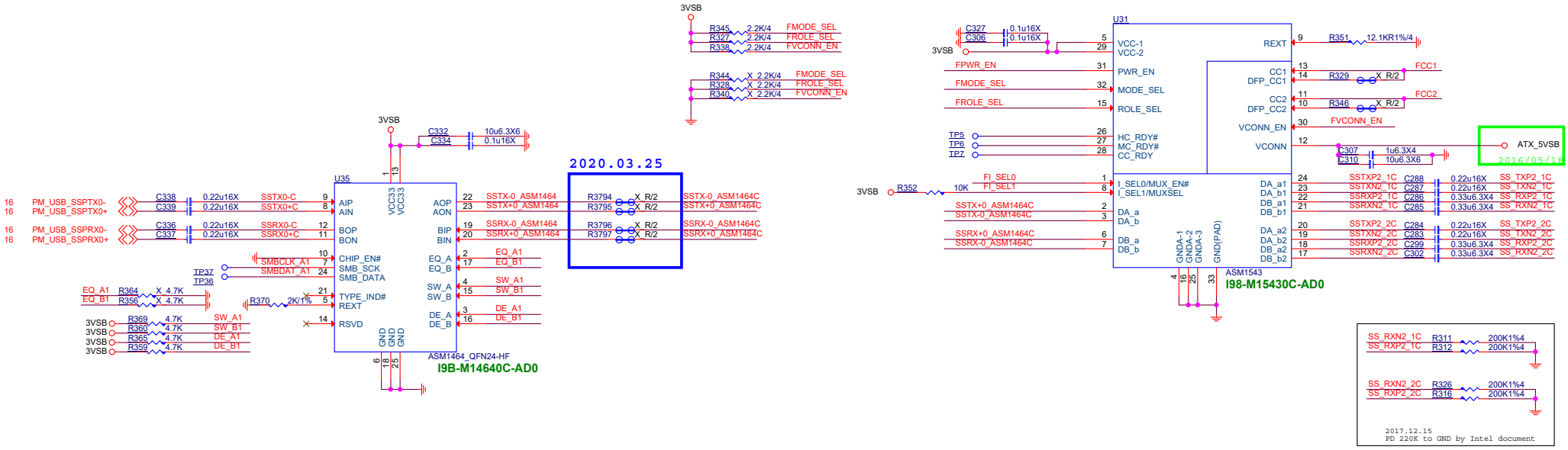
Front USB3 180°

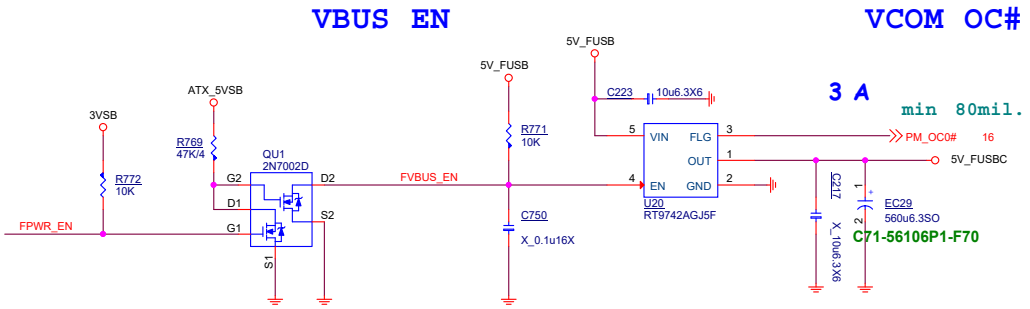
BOX Header(JUSB3)

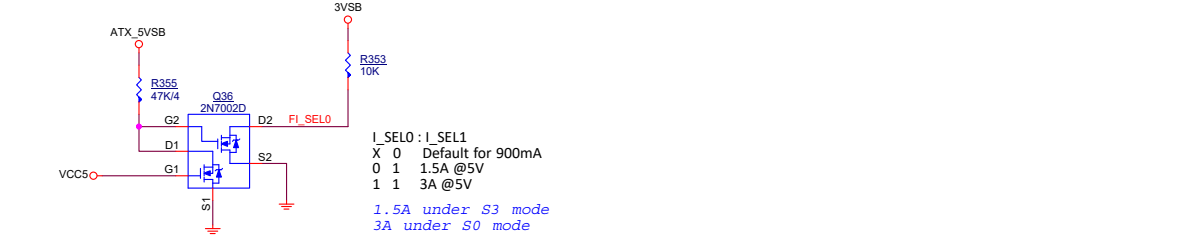
5V@1.8A

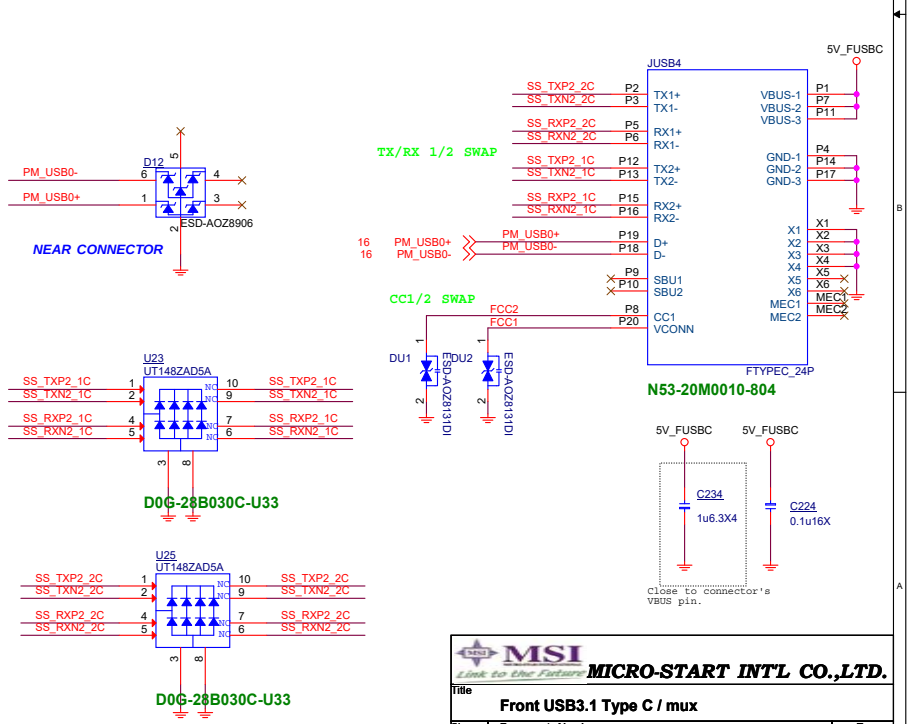


MSI	MICRO-STAR INT'L CO.,LTD		
	MS-7C91..		
Size: Custom	Document Description: Front USB3.0 Header		Rev: 30
Date: Thursday, July 23, 2020		Sheet 40 of 78	







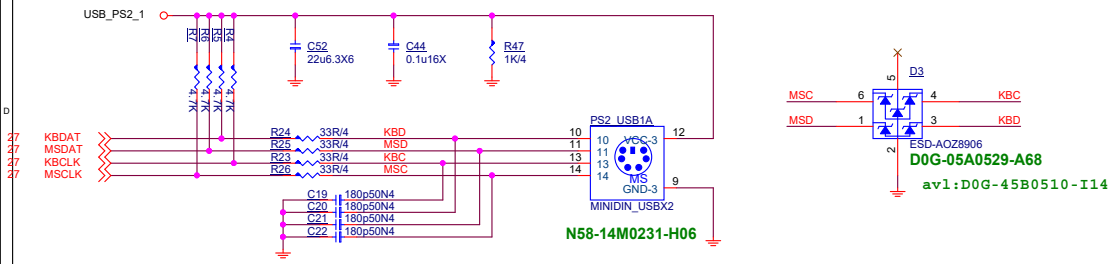


MSI Link to the Future	MICRO-START INTL CO.,LTD.		
Title: Front USB3.1 Type C / mux			
Size: Custom	Document Number: MS-7C91..		Rev: 30
Date: Thursday, July 23, 2020		Sheet 41 of 78	

PS2+USB (USB2.0)

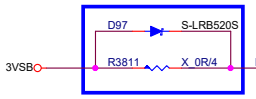
5V@1A

layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch



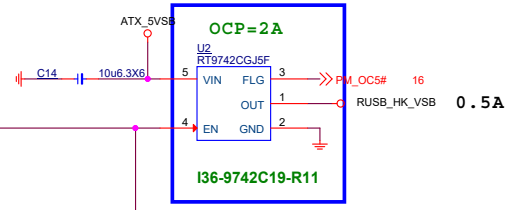
HOTKEY POWER

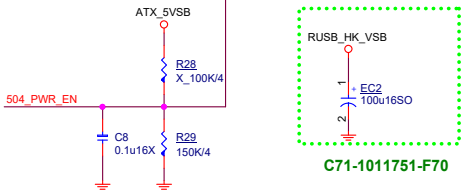
2020.03.25



2020.03.30

OCP=2A

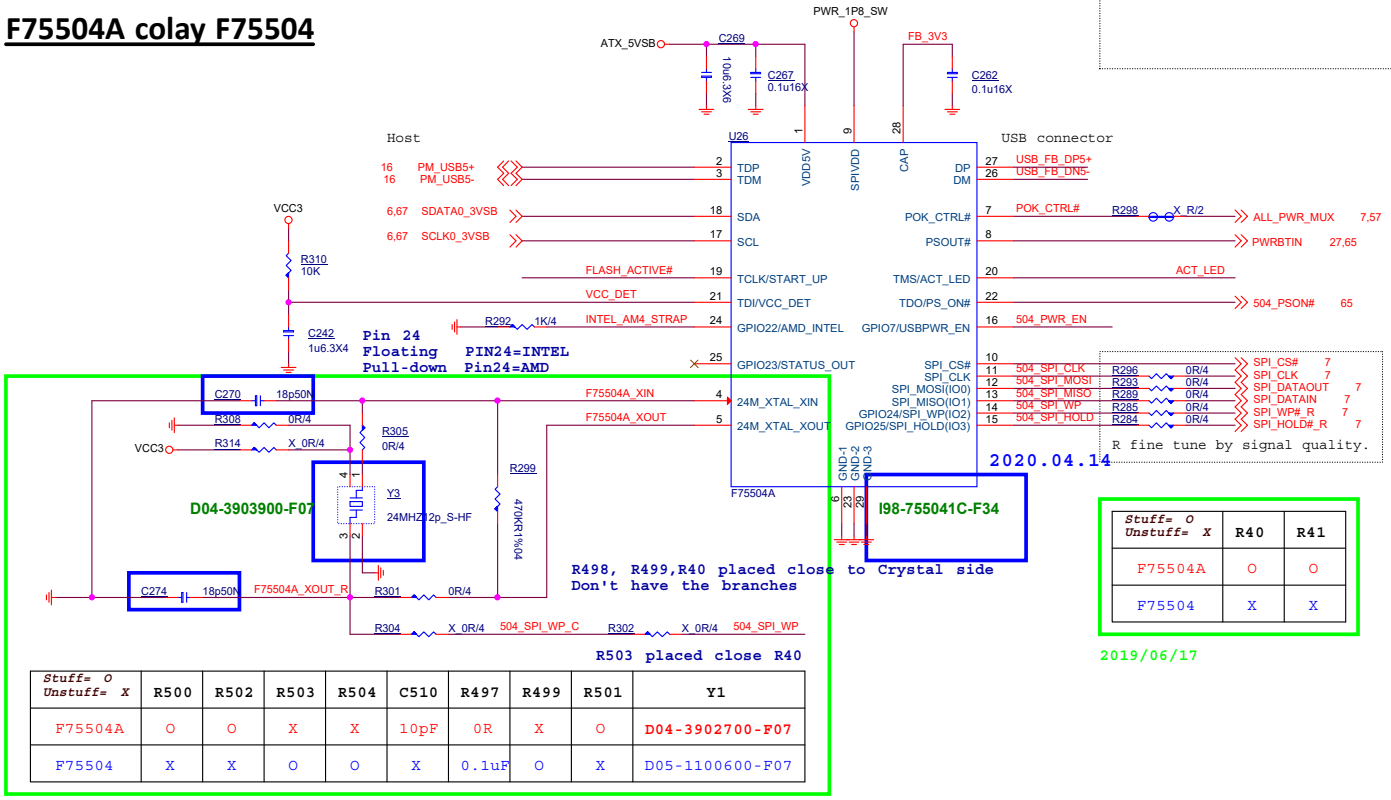




USB Flash BIOS

F75504A colay F75504

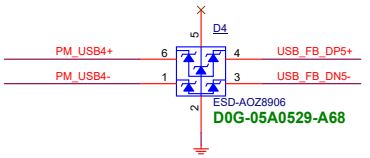
F75504A/F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.

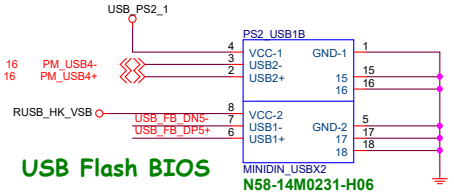


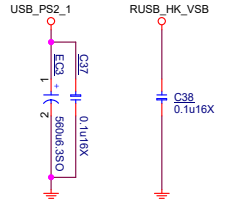
Stuff= O Unstuff= X	R500	R502	R503	R504	C510	R497	R499	R501	Y1
F75504A	O	O	X	X	10pF	0R	X	O	D04-3902700-F07
F75504	X	X	O	O	X	0.1uF	O	X	D05-1100600-F07

Stuff= O Unstuff= X	R40	R41
F75504A	O	O
F75504	X	X

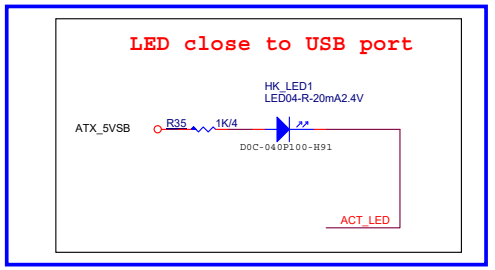
2019/06/17

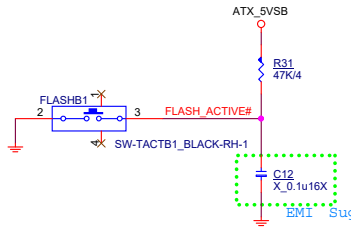


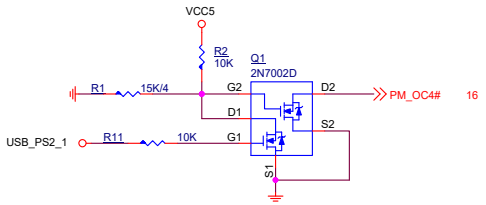




2020.04.14

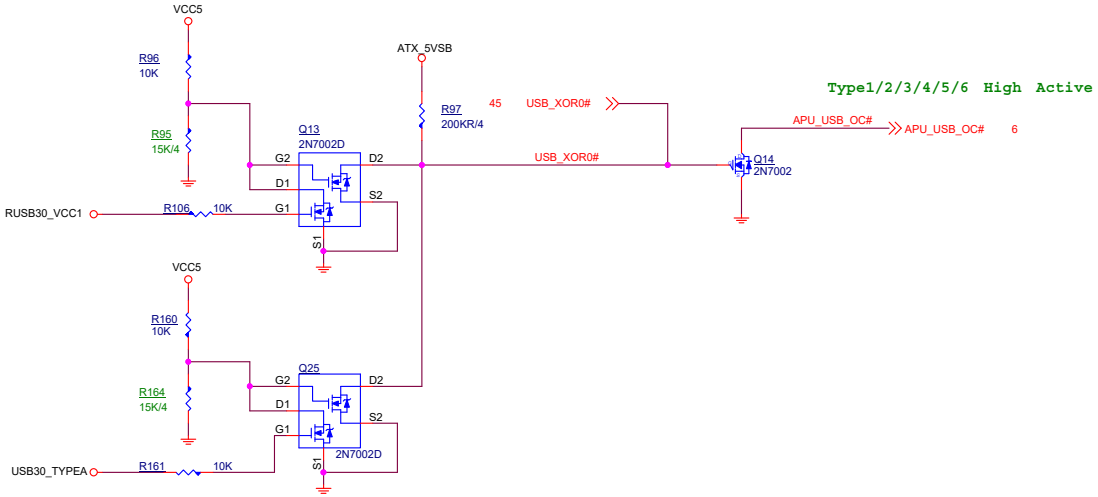




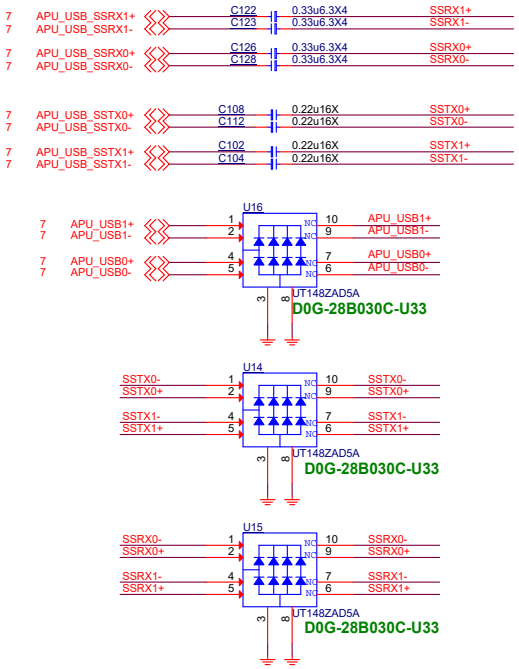


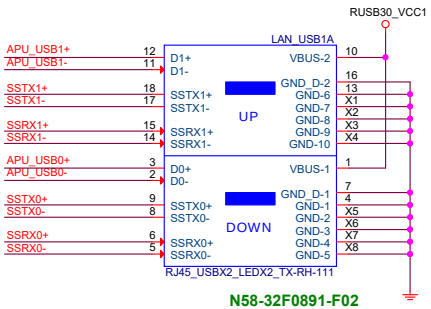
MICRO-STAR INT'L CO.,LTD	
MS-7C91..	
Size: Custom	Document Description: Rear USB2.0+PS2+F75504A
Rev: 30	
Date: Thursday, July 23, 2020	Sheet 42 of 78

CPU_USB_OC

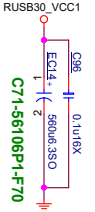


Rear USB3.1 GEN1 5V@1.8A



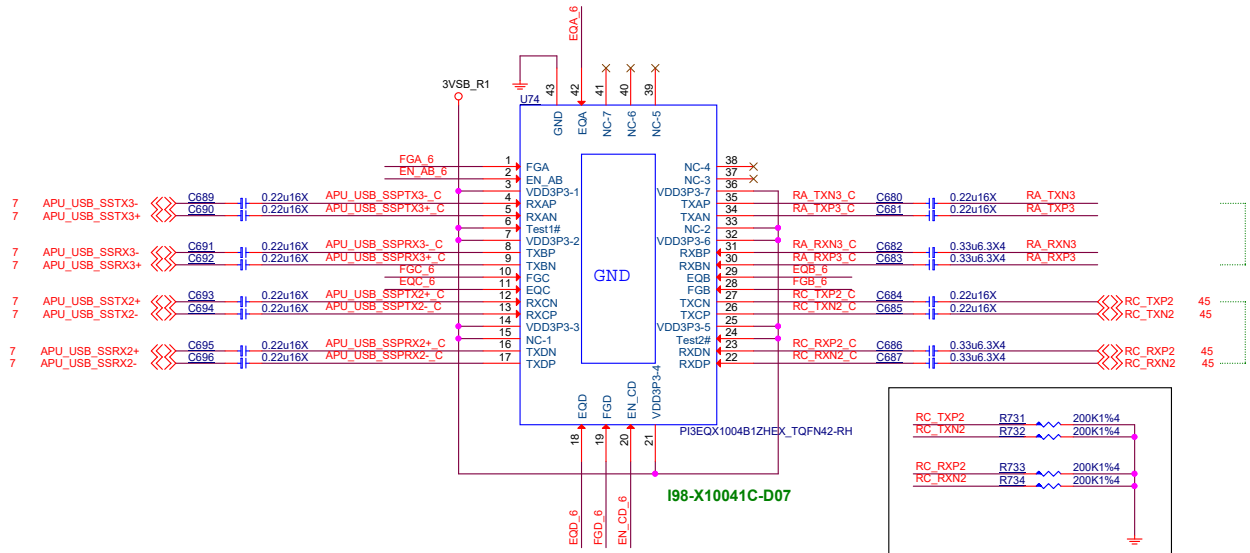


1.8A



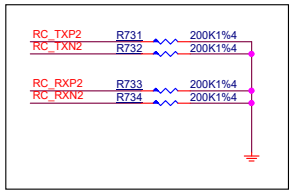
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C91..	
Size: Custom	Document Description: Rear USB3.1.	Rev: 30
Date: Thursday, July 23, 2020	Sheet 43 of 78	

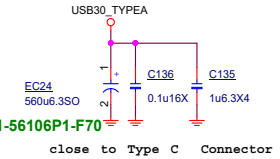
TYPE-A PI3EQX1004 Redriver

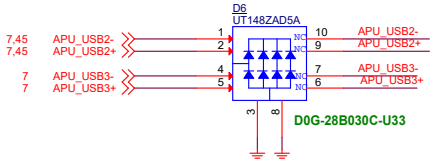


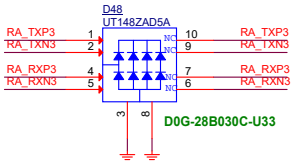
Rear TYPE-A

Rear TYPE-C

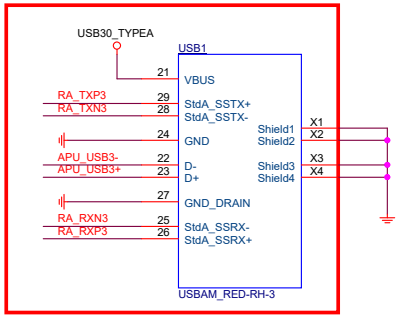


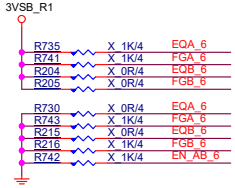


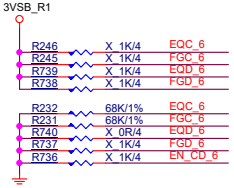


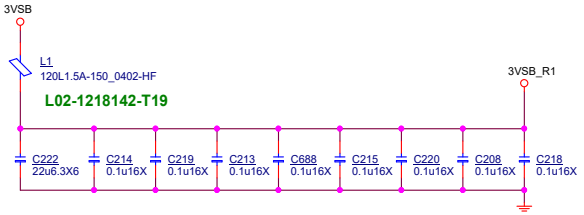


GEN2 0.9A









EQ	dB	
0	10.9	0 to GND
R	6.7	68K to GND
F	8.9	NC
1	13.1	0 to VDD

		EQ	FG
USB3_TX4	A	R	F
USB3_RX4	B	R	L
USB3_TX3	C	R	F
USB3_RX3	D	R	L

FG	dB	
0	-3	0 to GND
R	-1.5	68K to GND
F	0	NC
1	2	0 to VDD

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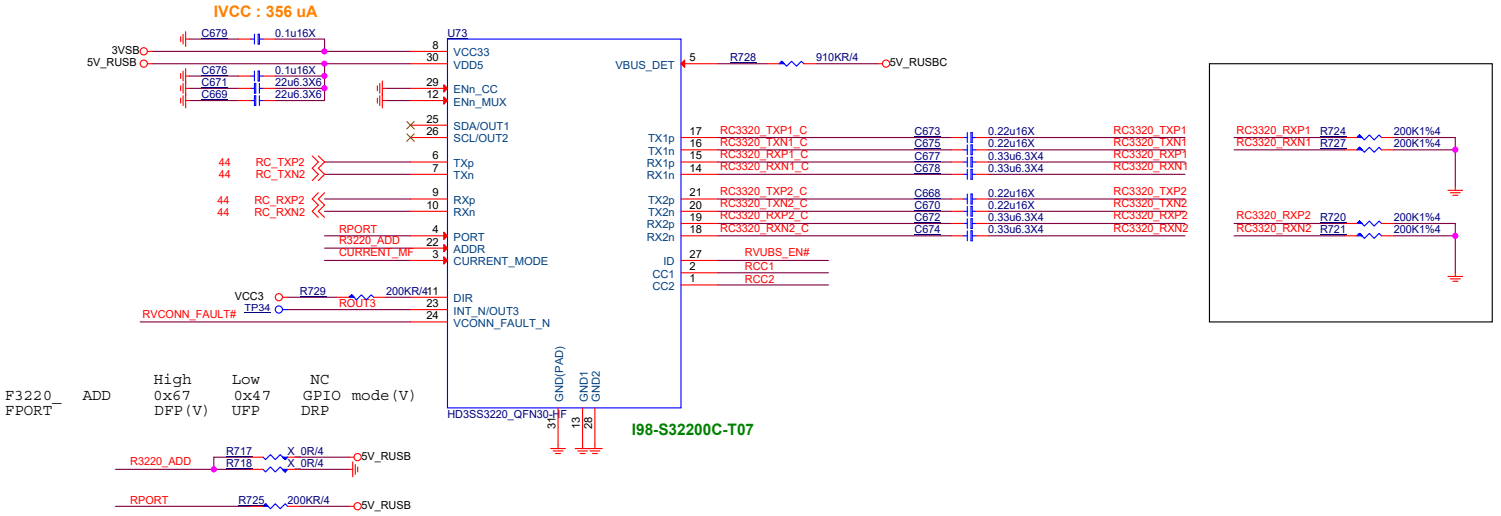
MS-7C91..

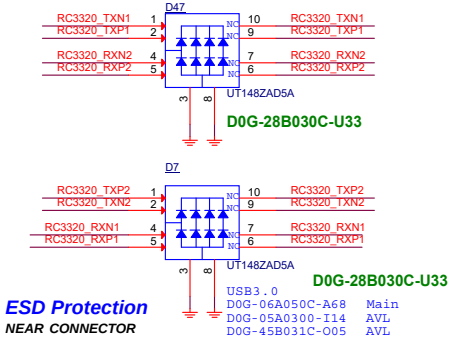
Size	Document Description	Rev
Custom	Rear USB3.1 Type A / Redrive	30

Date: Thursday, July 23, 2020 Sheet 44 of 78

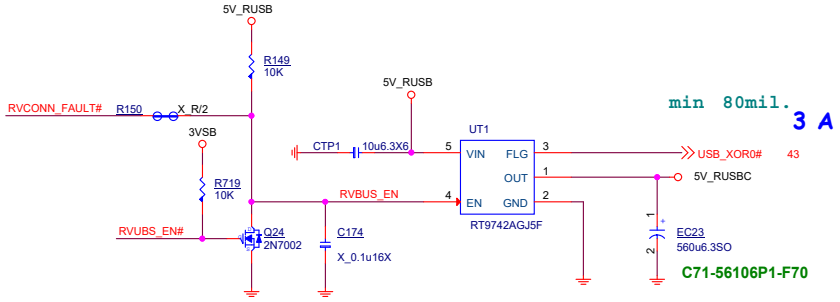
USB 3.1-Type-C

USB Type-C MUX with Configuration Channel (CC)

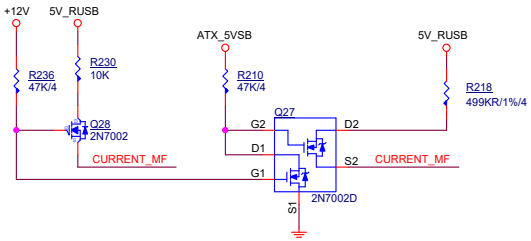


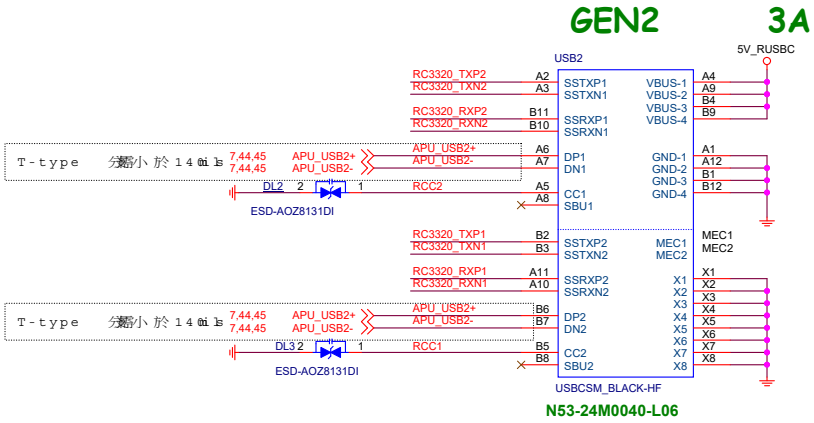


VBUS EN



Current Mode

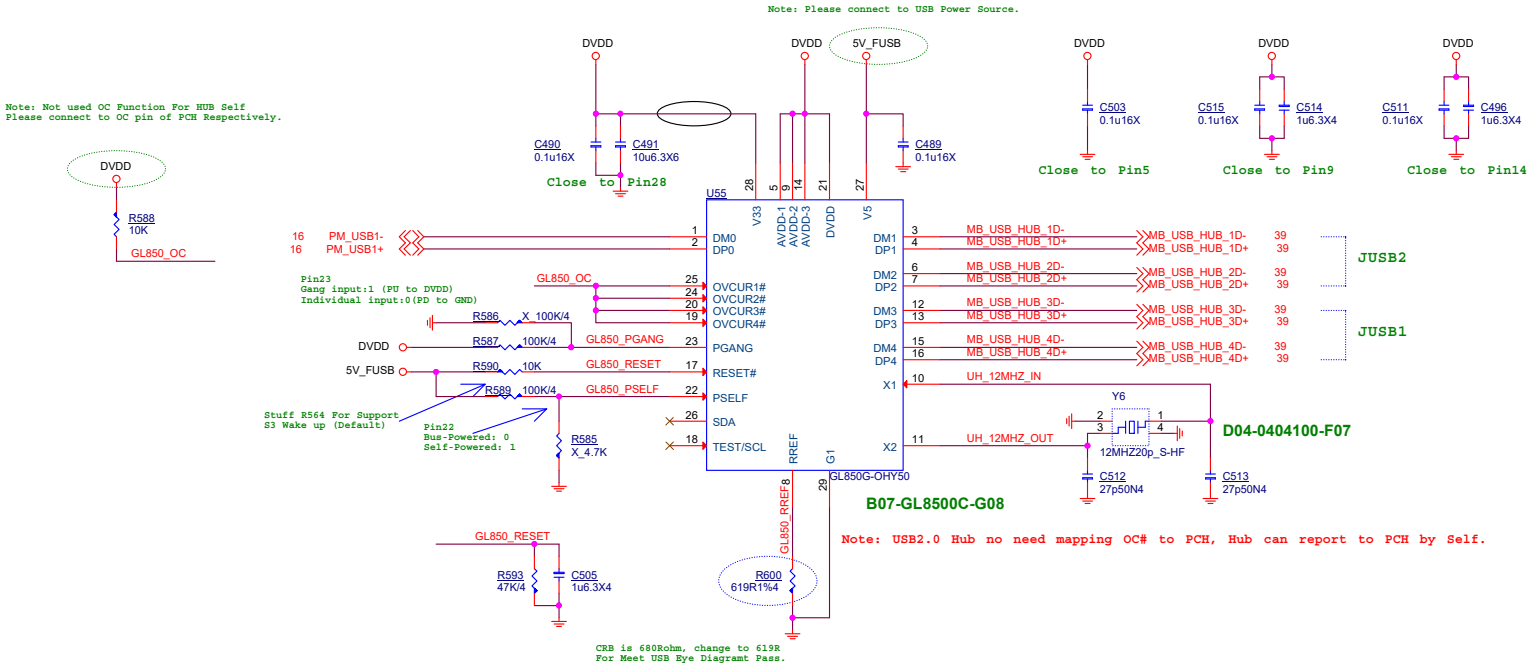




MICRO-STAR INT'L CO.,LTD	
MS-7C91..	
Size: Custom	Document Description: Rear USB3.1 Type C / mux
Rev: 30	
Date: Thursday, July 23, 2020	Sheet 45 of 78

GL850G USB2.0 HUB

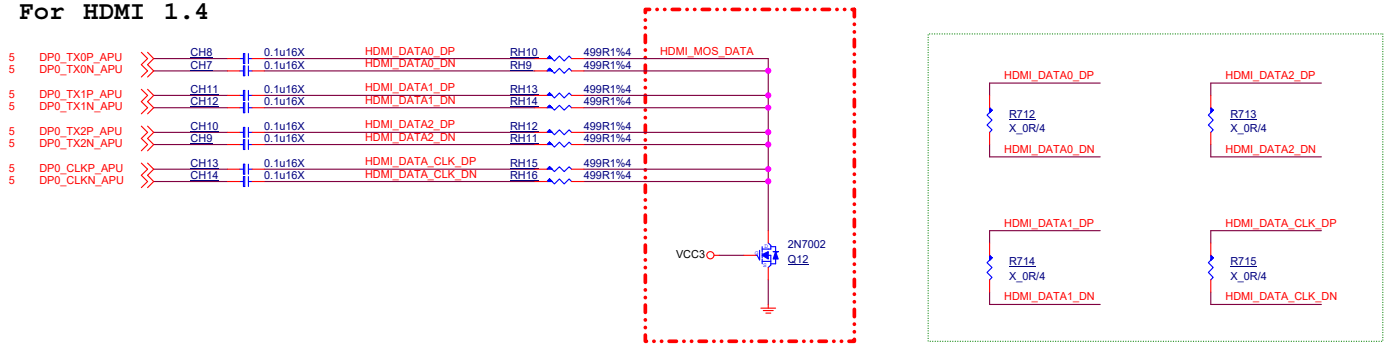
5V_FUSB



MICRO-STAR INT'L CO.,LTD		
MS-7C91..		
Size: Custom	Document Description: GL850G	Rev: 30
Date: Thursday, July 23, 2020	Sheet 46 of 78	

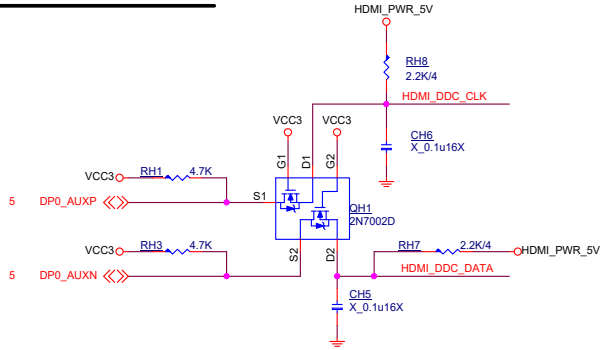
HDMI CONNECTOR

For HDMI 1.4

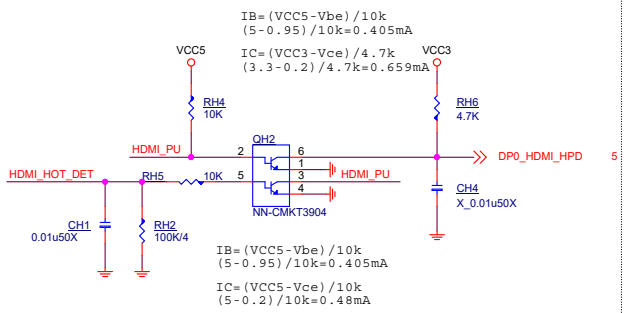


HDMI_MOS_DATA trace length <500mil
other platform please check design guide

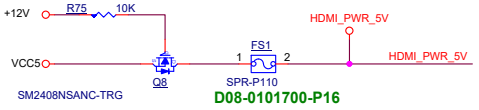
AUX Level Shifter



HPD Circuit



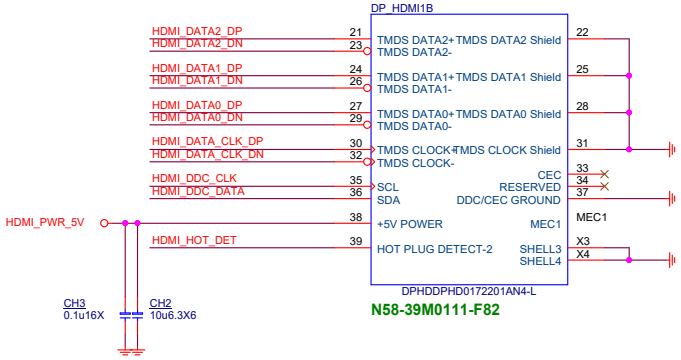
Connector Power



D08-0101700-P16

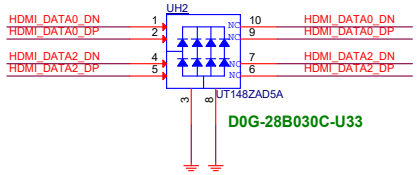
如果用 DIO DE S調整壓會不過

Connector

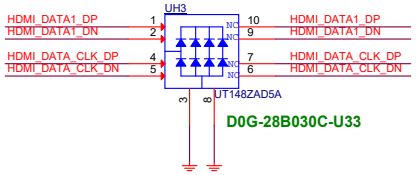


N58-39M0111-F82

For EMI

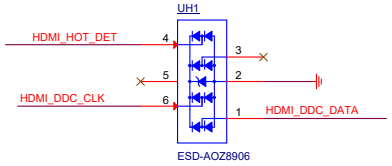


D0G-28B030C-U33



D0G-28B030C-U33

注意:耐 壓 V零件

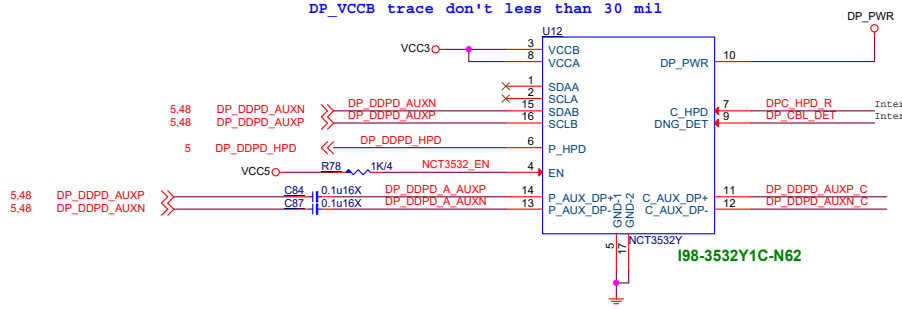


ESD-AOZ8906

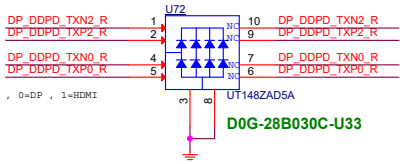
MICRO-STAR INT'L CO.,LTD		
MS-7C91..		
Size: Custom	Document Description: HDMI	Rev: 30
Date: Thursday, July 23, 2020	Sheet 47 of 78	

500mA

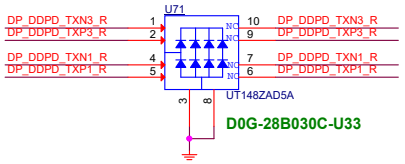
DP_VCCB trace don't less than 30 mil



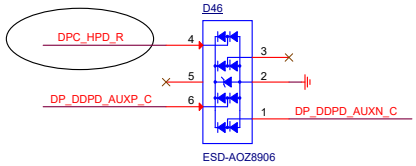
I98-3532Y1C-N62



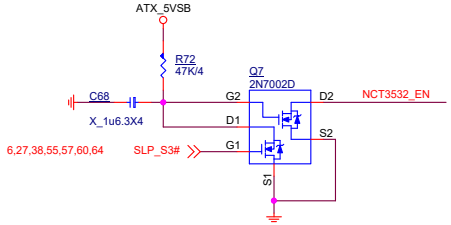
D0G-28B030C-U33

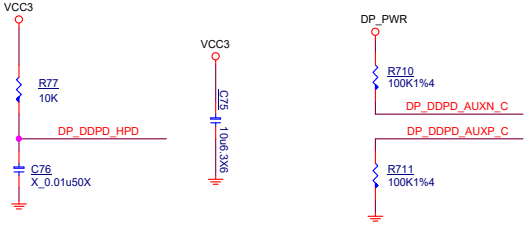


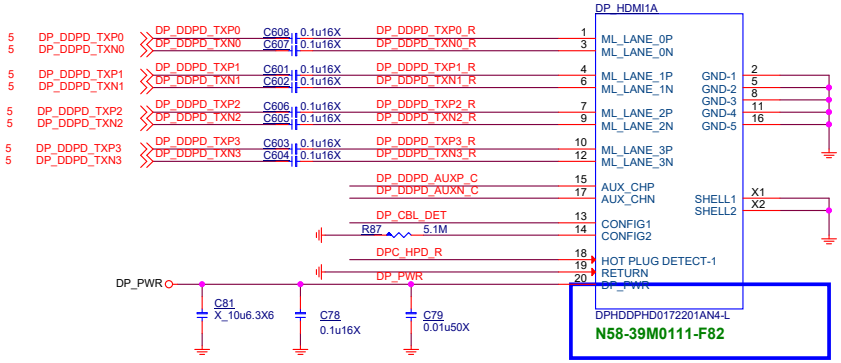
D0G-28B030C-U33



ESD-AOZ8906







DPHDDPHD0172201AN4-L

N58-39M0111-F82

2020.04.13

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MS-7C91..		
Size: Custom	Document Description: DP	Rev: 30
Date: Thursday, July 23, 2020	Sheet 48 of 78	

VCORE: ICCMax 140A
LL: 1.3mohm
OCP: 400A(10 x 40A)

SOC: ICCMax 75A
LL: 2.1ohm
OCP: 100A

Note:VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

SMBUS address:0X60(7 bit)
0XC0(8 bit)

2020.03.25

2020.04.09

I32-229003C-R28

I31-7116S09-N03

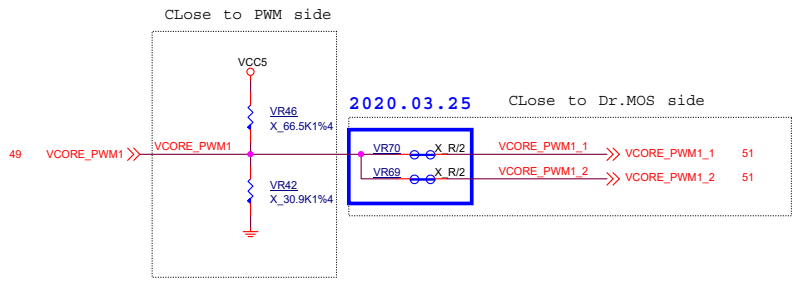
Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V

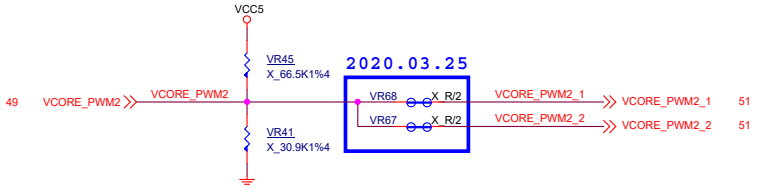
close to MOS

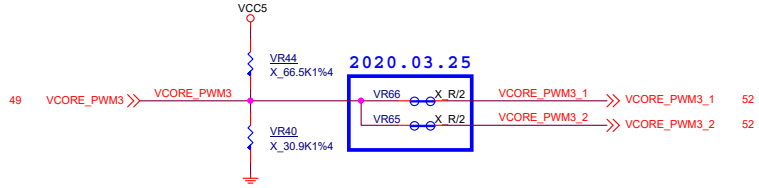
MICRO-STAR INT'L CO.,LTD	
MS-7C91..	
Size: Custom	Document Description: CPU Power RAA229004 10+2
Rev: 30	
Date: Thursday, July 23, 2020	Sheet 49 of 78

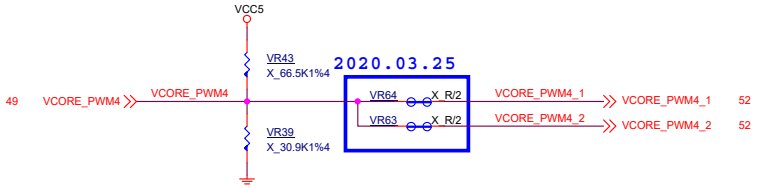
CPU_CORE Driver IC

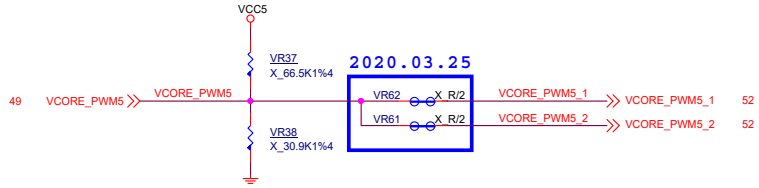
VCORE Double 10-PHASE











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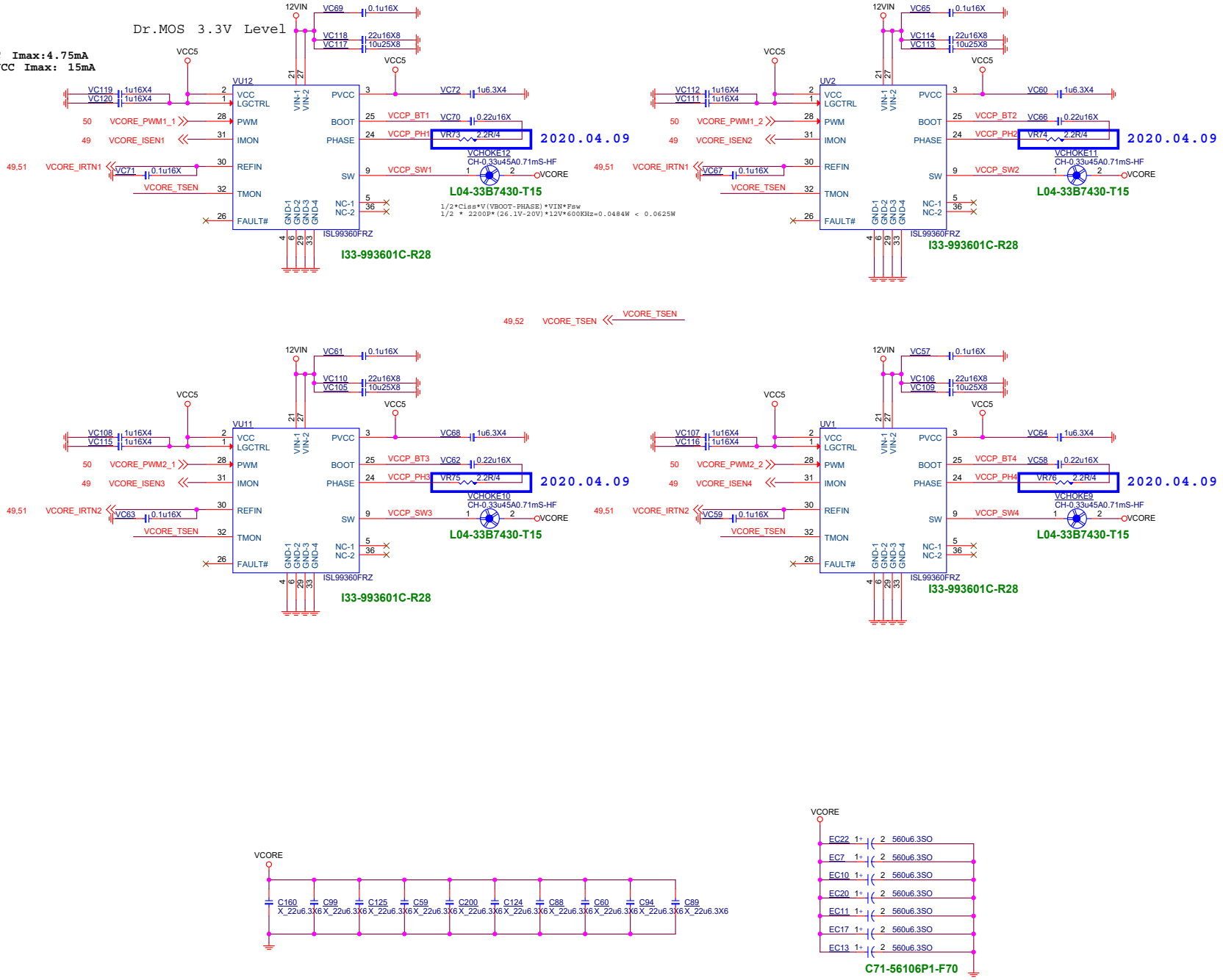
MS-7C91..		
Size: Custom	Document Description: CPU Power Phase Double IC SPS	Rev: 30
Date: Thursday, July 23, 2020	Sheet 50 of 78	

Vcore EDC Max 140A

Dr.MOS 3.3V Level

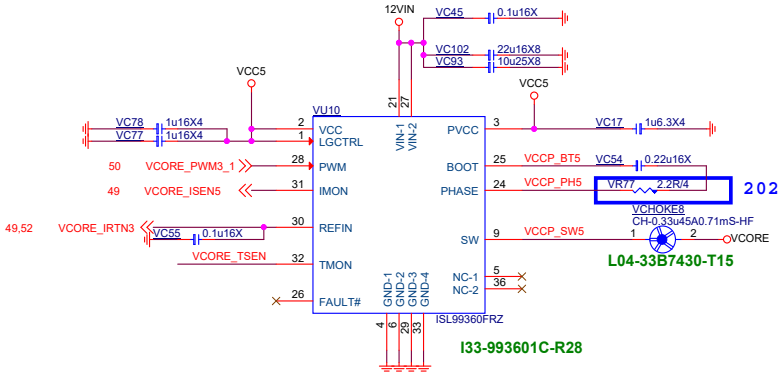
VCC Imax:4.75mA
IPVCC Imax: 15mA



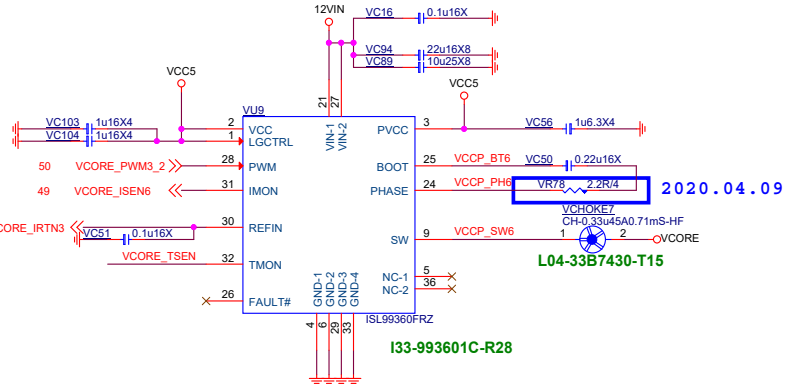
MICRO-STAR INT'L CO.,LTD		
MS-7C91..		
Size: Custom	Document Description: CPU Power Vocre Phase 1- 4	Rev: 30
Date: Thursday, July 23, 2020	Sheet 51 of 78	

Dr.MOS 5V Level

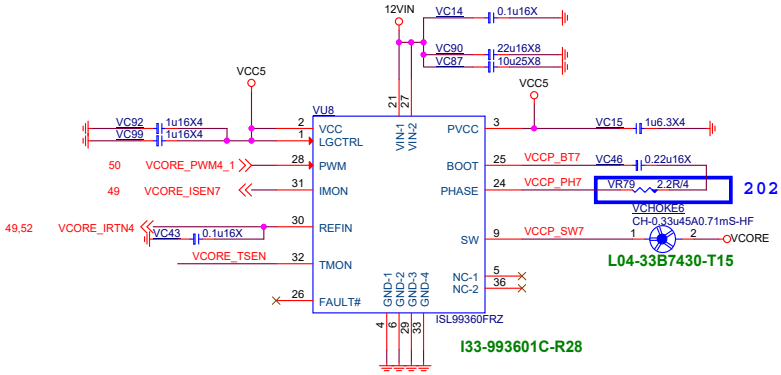
49,51 VCORE_TSEN <<< VCORE_TSEN



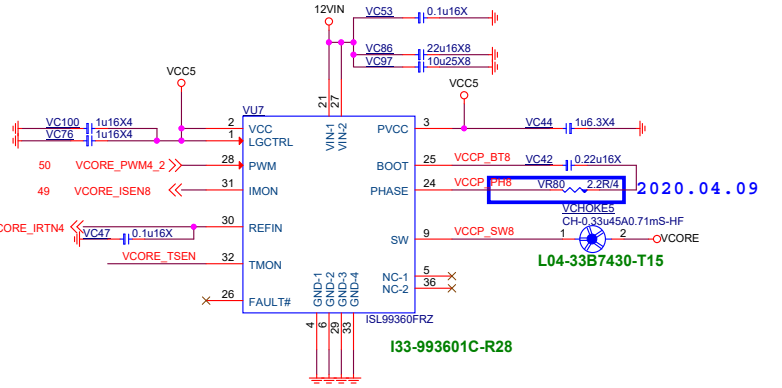
2020.04.09



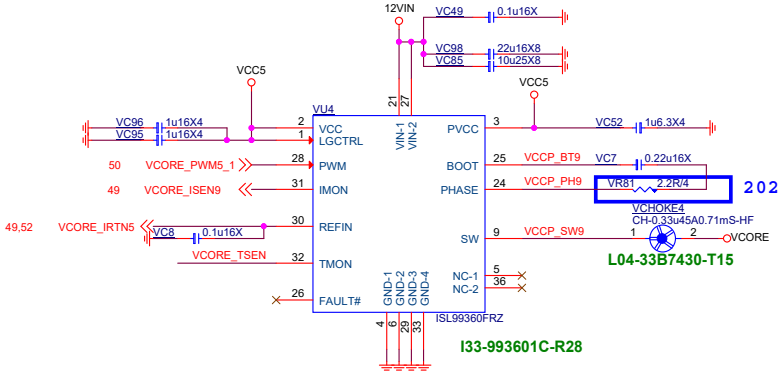
2020.04.09



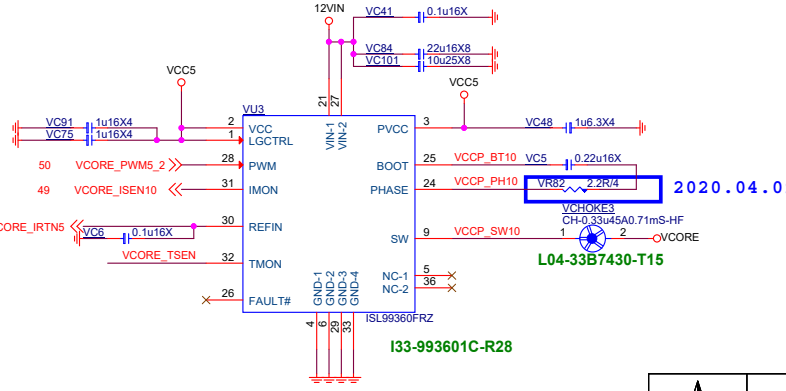
2020.04.09



2020.04.09



2020.04.09



2020.04.09

MICRO-STAR INT'L CO.,LTD

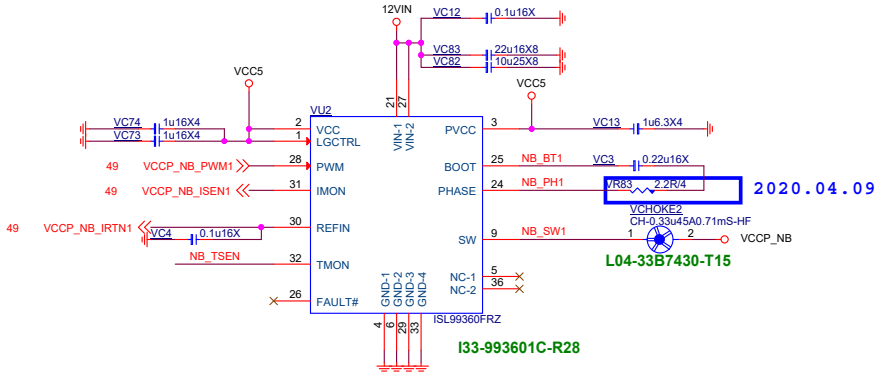
MS-7C91..

Size	Document Description	Rev
Custom	CPU Power Vocre Phase 6 - 10	30

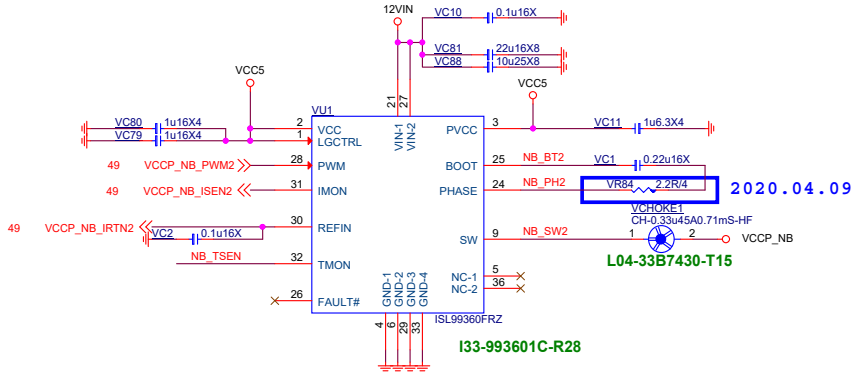
Date: Thursday, July 23, 2020 Sheet 52 of 78

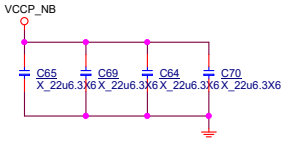
SOC EDC Max 75A

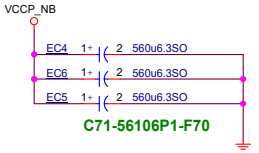
Dr.MOS 3.3V Level



49 NB_TSEN NB_TSEN





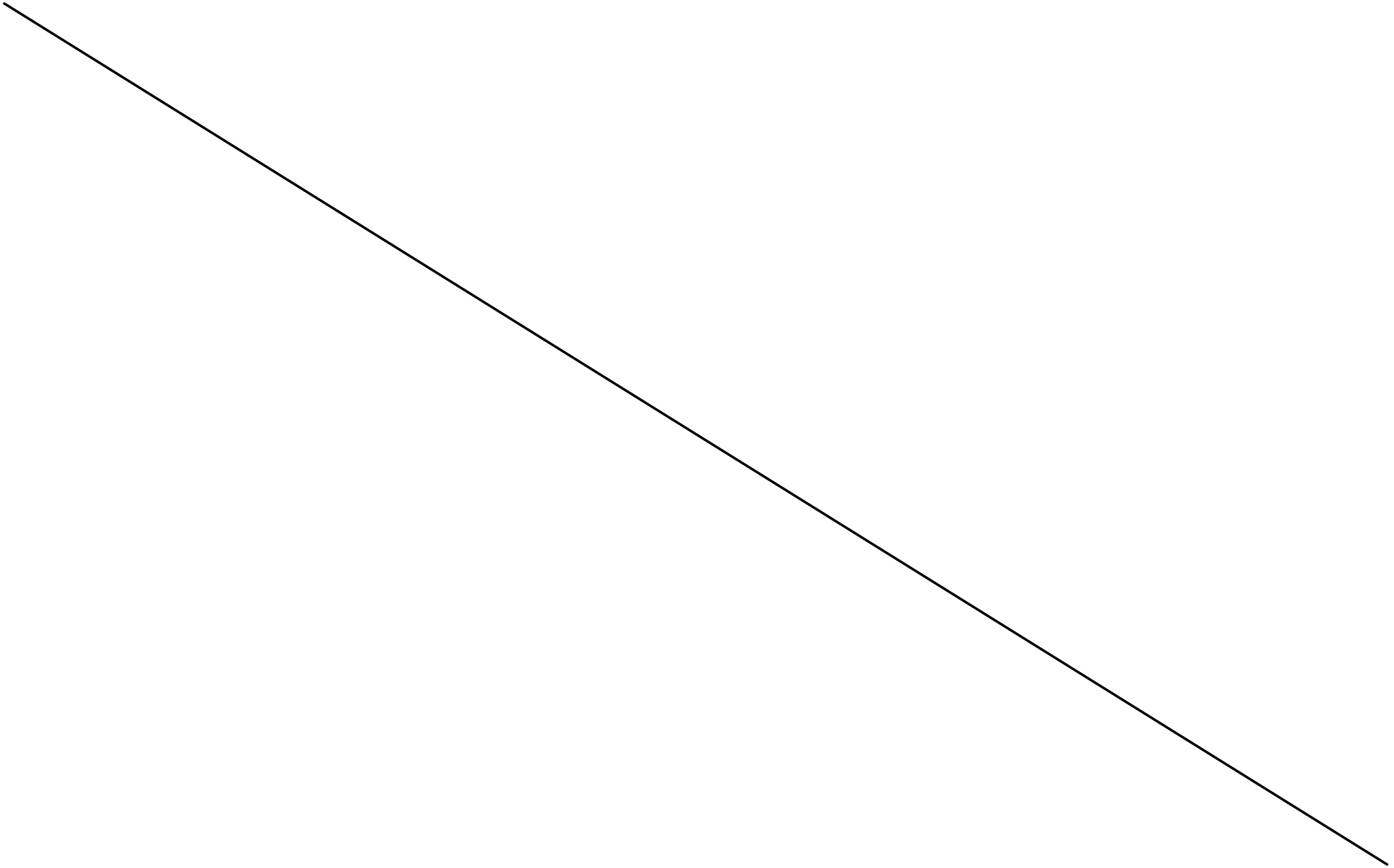


MICRO-STAR INT'L CO.,LTD

MS-7C91..

Size	Document Description	Rev
Custom	CPU Power NB Phase 1-2	30

Date: Thursday, July 23, 2020 Sheet 53 of 78



MICRO-START INT'L CO.,LTD.

Title: CPU Power NB Switch / NCT3933 OV

Size: Custom | Document Number: MS-7C91.. | Rev: 30

Date: Thursday, July 23, 2020 | Sheet 54 of 78

CPU 1.8V S5

CPU 1.8V_S5@0.5A
CPU_VDDP_S5@1A
AUDIO1.8V@0.25A

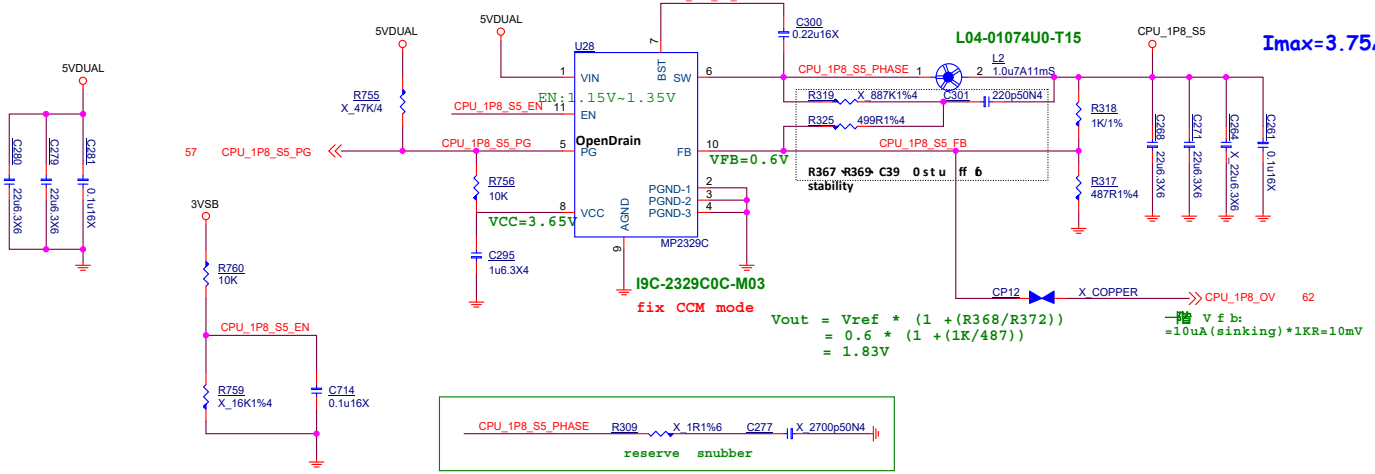
Continuous Conduction Mode (CCM)

Input Current = (6.5A*1.8V)/5V/0.8 = 3A

CPU_1P8_BST ↔ CPU_1P8_BST_R >50 mils.

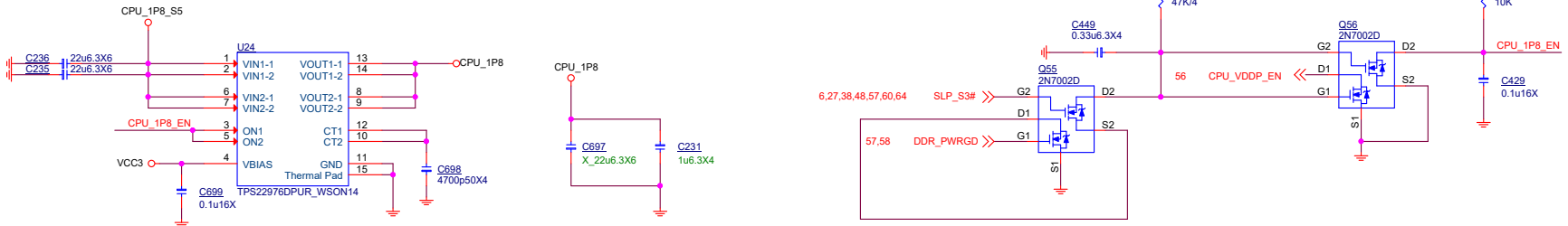
OCP = 6.5A

Imax=3.75A(S5+S0)



CPU 1.8V S0

CPU 1.8V_S0@2A



Adjustable Rise Time
SR = 0.42*CT+66
SR is the slew rate in (μ s/V)
CT is constant value on CT pin (in pF)
The units for the constant 66 is in
(μ s/V)

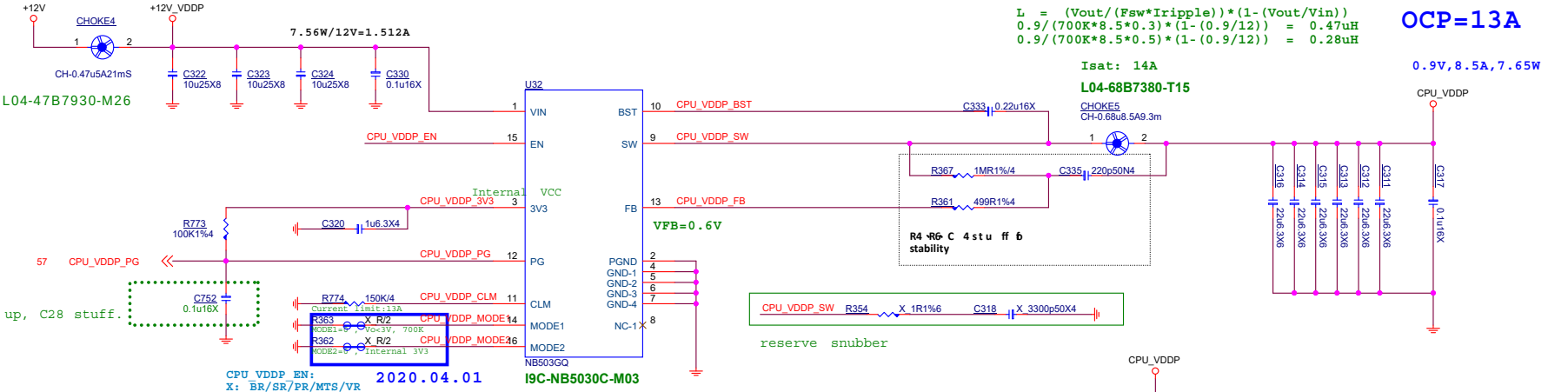
DDR_PWRGD
CPU_VDDP
CPU_1P8
VDD33

MICRO-STAR INT'L CO.,LTD		
MS-7C91..		
Size: Custom	Document Description: CPU Power 1.8_S0 / S5	Rev: 30
Date: Thursday, July 23, 2020	Sheet 55 of 78	

CPU_VDDP_S0

0.9V@S0:8.5A

```
Input Current = (13A*0.9V)/12V/0.8 = 1.22A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A
```

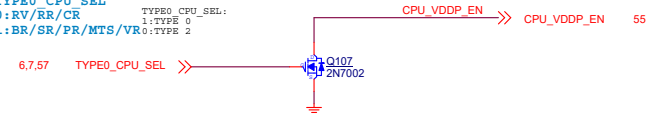


20180822
fix PG glitch when VCC3 ramp up, C28 stuff.

CPU_VDDP_EN:
X: BR/SR/PR/MTS/VR
O: RV/RR/CR

2020.04.01

TYPE0_CPU_SEL
0:RV/RR/CR
1:BR/SR/PR/MTS/VR



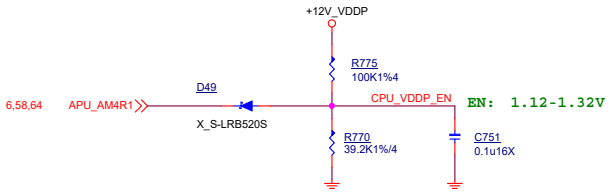
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	0
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0
MTS	4	1	1
RR	5	1	0
VM	6	1	1
CR	7	1	0

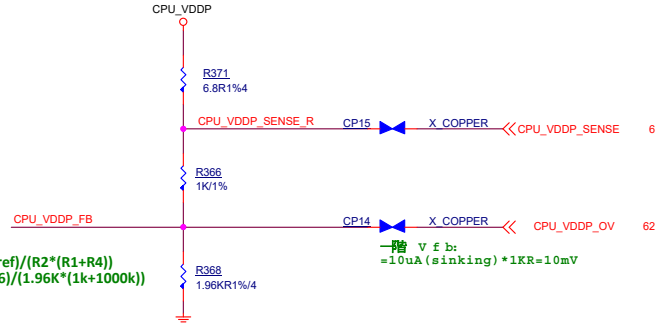
SPEC no Support

CPU VDDP NOT SUPPORT TYPE2

CPU VDDP NOT SUPPORT TYPE4

CPU VDDP NOT SUPPORT TYPE6



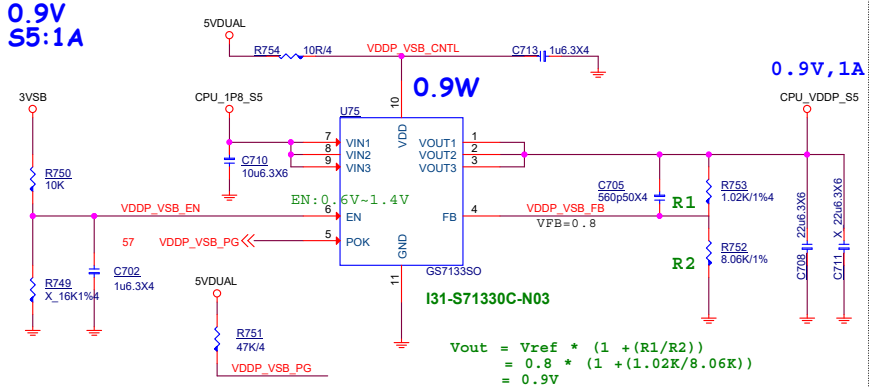


Vout = Vref + (R1*R4*Vref)/(R2*(R1+R4))
= 0.6+(1k*1000k*0.6)/(1.96K*(1k+1000k))
= 0.9058V

一階 V f b:
=10uA(sinking)*1KR=10mV

CPU_VDDP_S5

0.9V
S5:1A



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(1.02K/8.06K))
= 0.9V

MICRO-STAR INT'L CO.,LTD

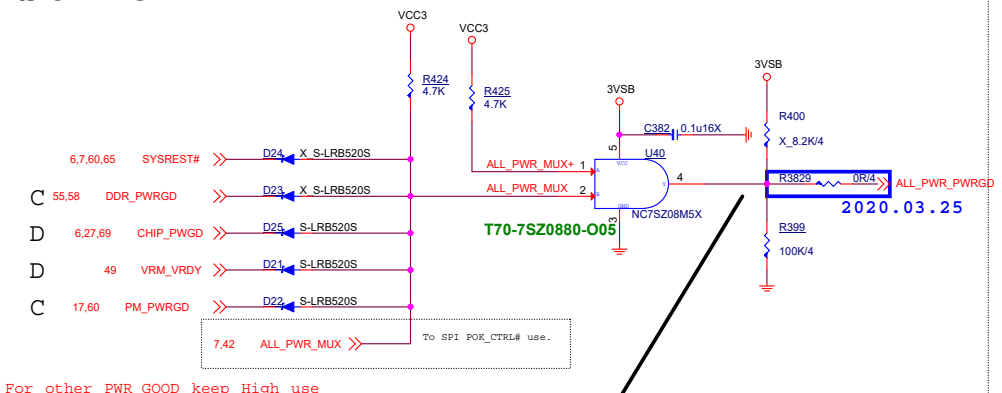
MS-7C91..

Size	Document Description	Rev
Custom	CPU Power VDDP - NB503	30

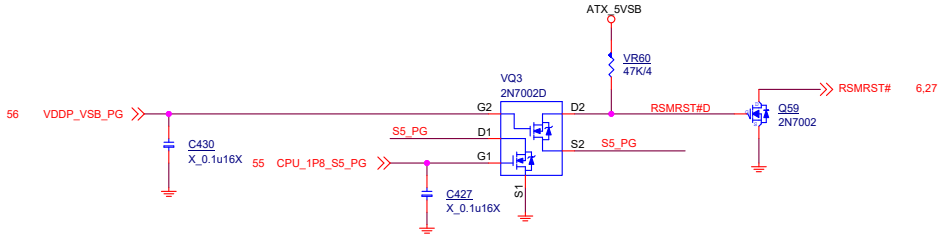
Date: Thursday, July 23, 2020 Sheet 56 of 78

ALL POWER GOOD MUX

S0 PG



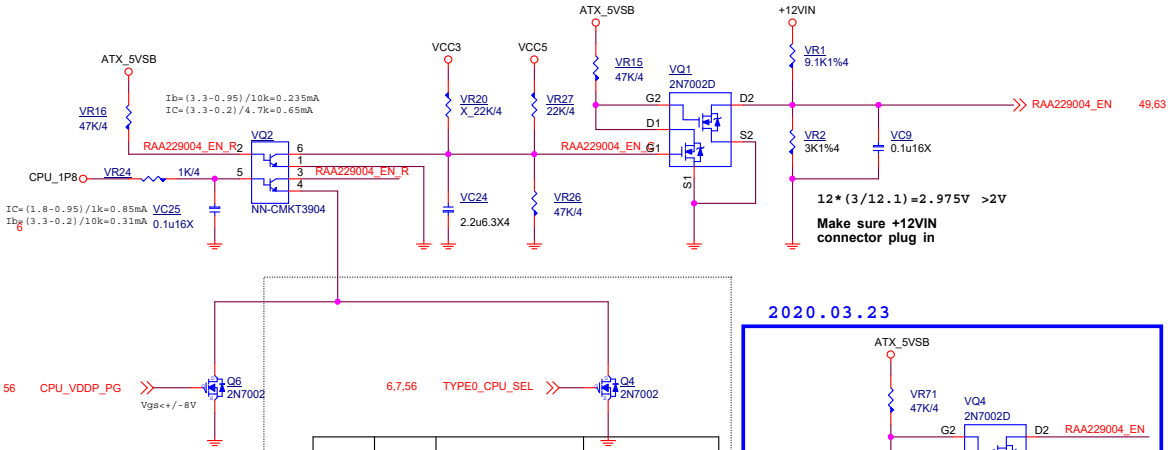
S5 PG

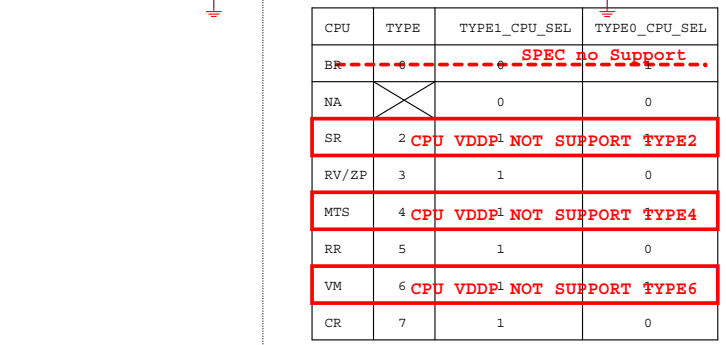


VRM_Enable circuit

2020.03.23

D2 Removed





CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	0
NA		0	0
SR	2	1	1
RV/ZP	3	1	0
MTS	4	1	1
RR	5	1	0
VM	6	1	1
CR	7	1	0

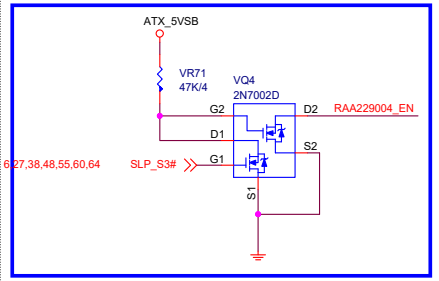
SPEC no Support

CPU VDDP NOT SUPPORT TYPE2

CPU VDDP NOT SUPPORT TYPE4

CPU VDDP NOT SUPPORT TYPE6

2020.03.23



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MS-7C91..	
Size: Custom	Document Description: VRM PWRGD
Rev: 30	
Date: Thursday, July 23, 2020	Sheet 57 of 78

DDR4_1.2V@28.7A

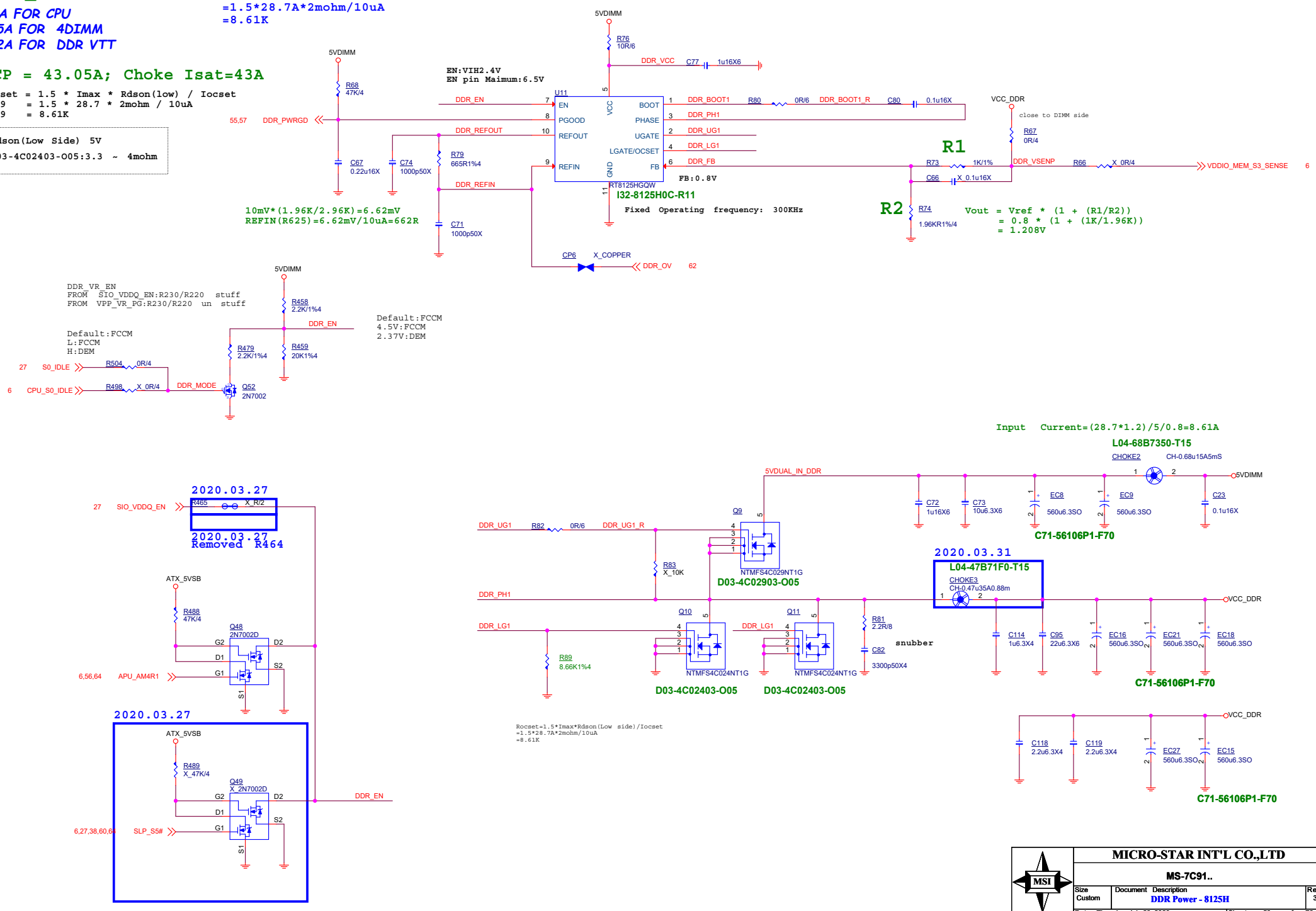
18A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT

Rocset=1.5*Imax*Rdson(Low side)/Iocset
=1.5*28.7A*2mohm/10uA
=8.61K

OCP = 43.05A; Choke Isat=43A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
R639 = 1.5 * 28.7 * 2mohm / 10uA
R639 = 8.61K

Rdson(Low Side) 5V
D03-4C02403-O05:3.3 ~ 4mohm



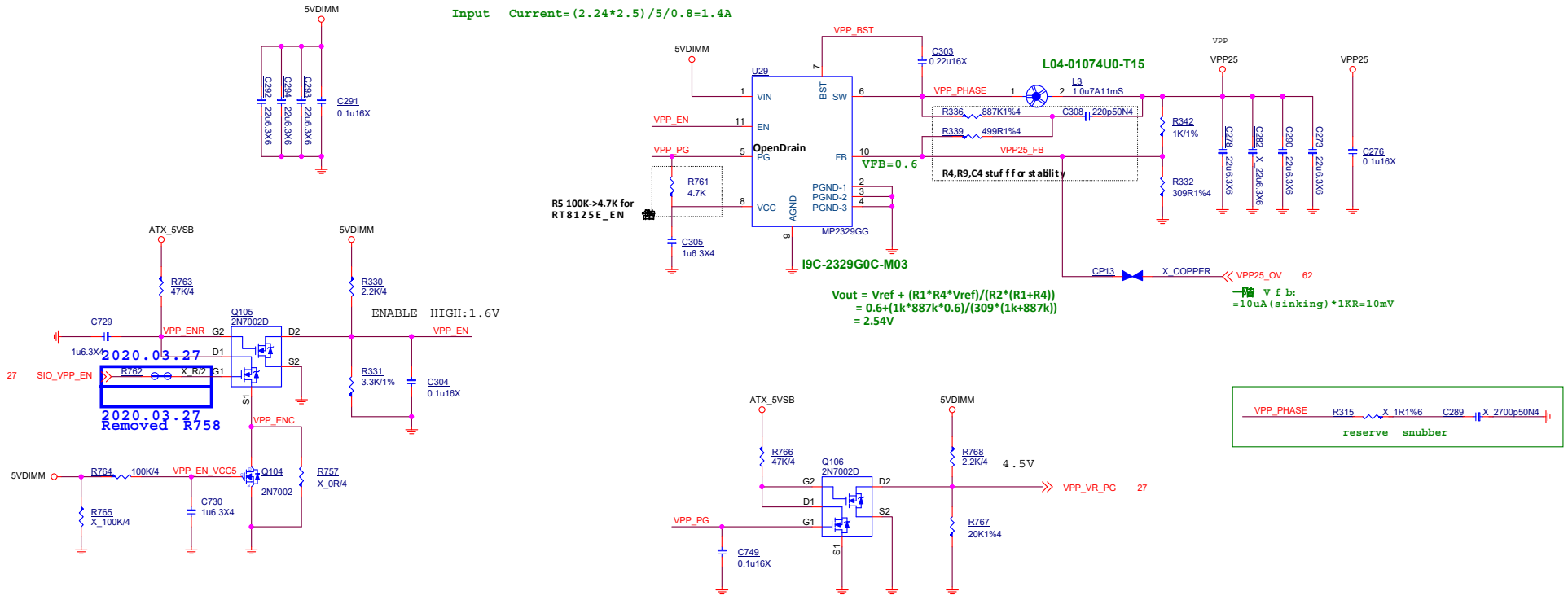
MICRO-STAR INT'L CO.,LTD			
MS-7C91..			
Size: Custom	Document Description: DDR Power - 8125H		Rev: 30
Date: Thursday, July 23, 2020		Sheet 58 of 78	

4DIMM : VPP25

2.5V@2.24A

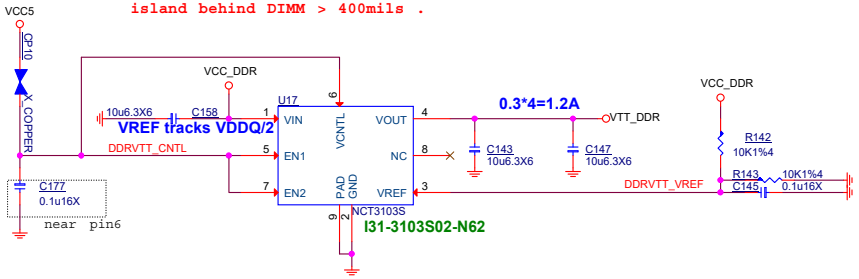
VPP_BST>50 mils.

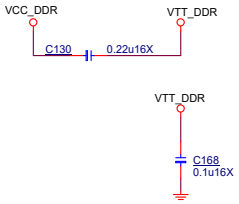
Input Current=(2.24*2.5)/5/0.8=1.4A



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .





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MS-7C91..		
Size: Custom	Document Description: DDR VPP25 / VTT	Rev: 30
Date: Thursday, July 23, 2020	Sheet 59 of 78	

FOR Promontory 1.05V_S0

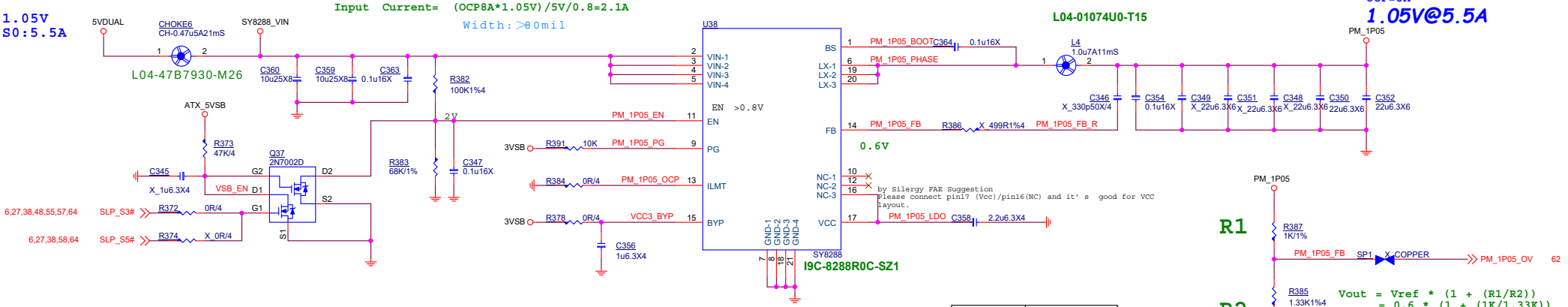
1.05V
S0:5.5A

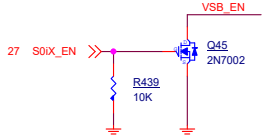
Input Current= (OCP8A*1.05V)/5V/0.8=2.1A

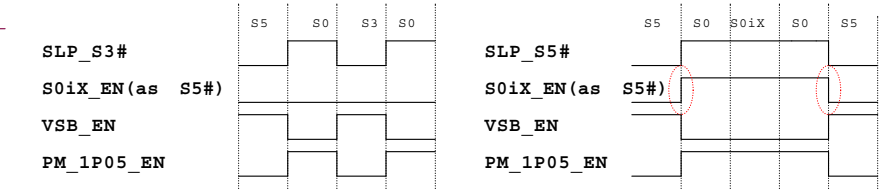
Width: >80mil

L04-01074U0-T15

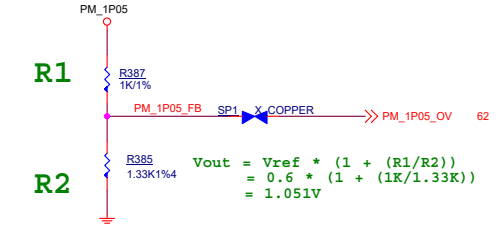
OCP=8A
1.05V@5.5A





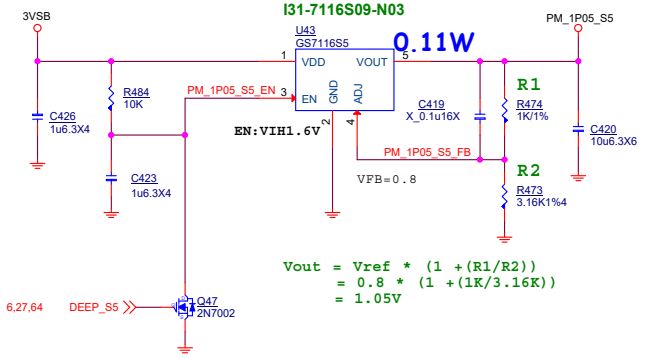


ILIMT	OCP
0	8A
floating	12A
1	16A



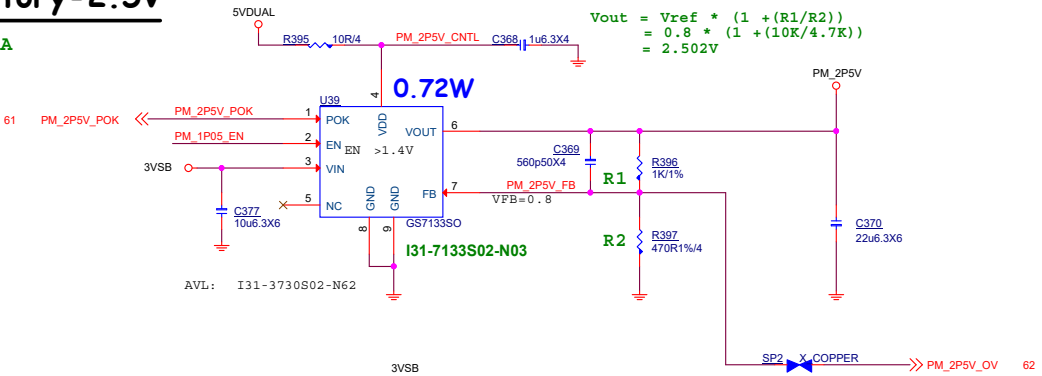
FOR PROM PM_1P05_S5

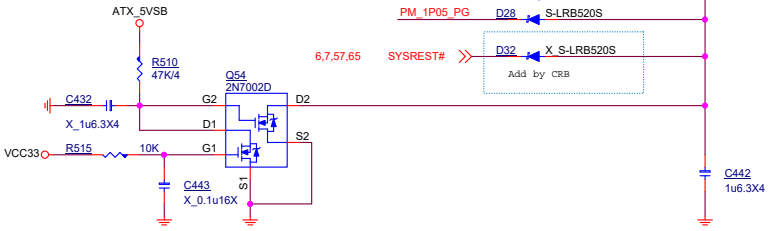
1.05V@0.05A

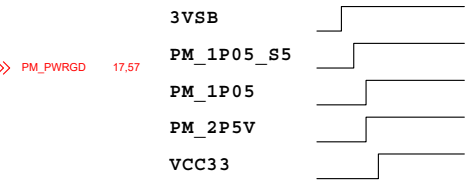


Promontory-2.5V

2.5V@900mA







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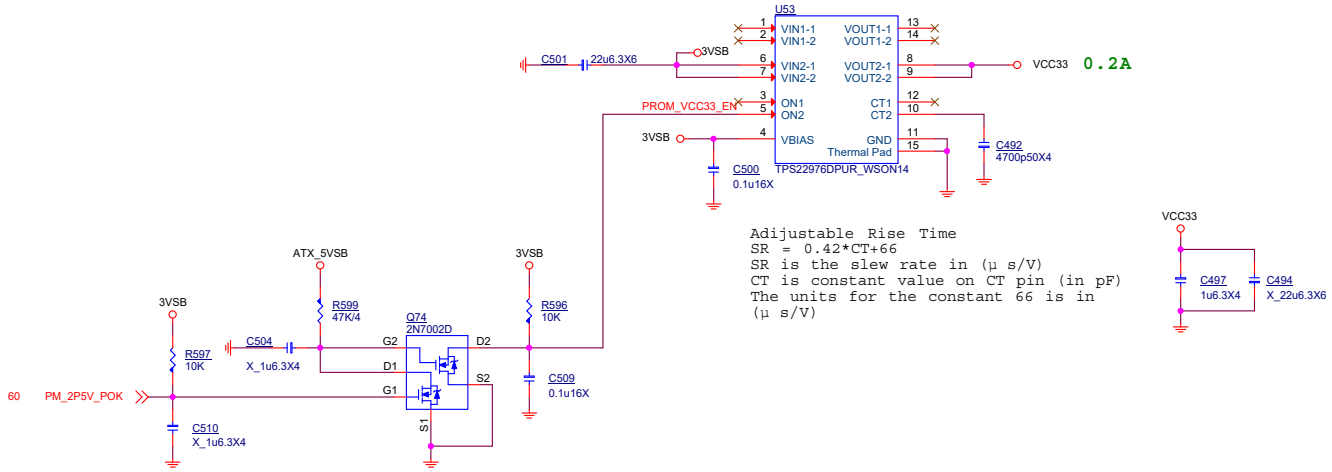
Size	Document Description	Rev
Custom	PM - SY8288/PM_1P05/PM_2P5V	30

Date: Thursday, July 23, 2020 Sheet 60 of 78

PROM VCC33

VCC33@0.2A



Adjustable Rise Time
SR = 0.42*CT+66
SR is the slew rate in (μ s/V)
CT is constant value on CT pin (in pF)
The units for the constant 66 is in
(μ s/V)

MICRO-STAR INT'L CO.,LTD

MS-7C91..

Size	Document Description	Rev
Custom	PM - TPS22976DPUR_WSON14	30

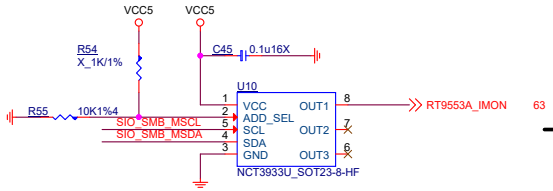
Date: Thursday, July 23, 2020 Sheet 61 of 78

Over Voltage Control IC

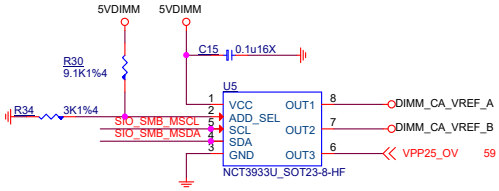
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

0x2A:RH=OPEN,RL=10K



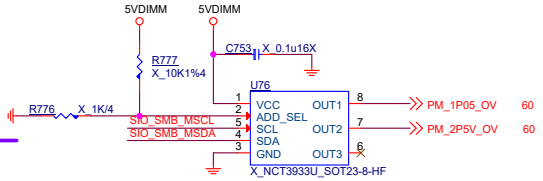
0x28:RH=9.1K,RL=3K



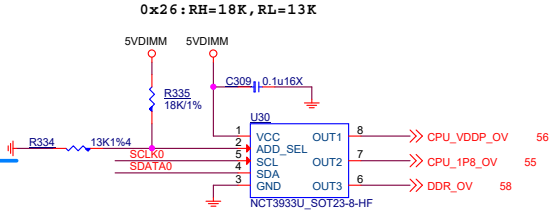
6,27,49 SIO_SMB_MSCL
6,27,49 SIO_SMB_MSDA

SIO_SMB_MSCL
SIO_SMB_MSDA

0x20:RH=10K,RL=OPEN



0x26:RH=18K,RL=13K

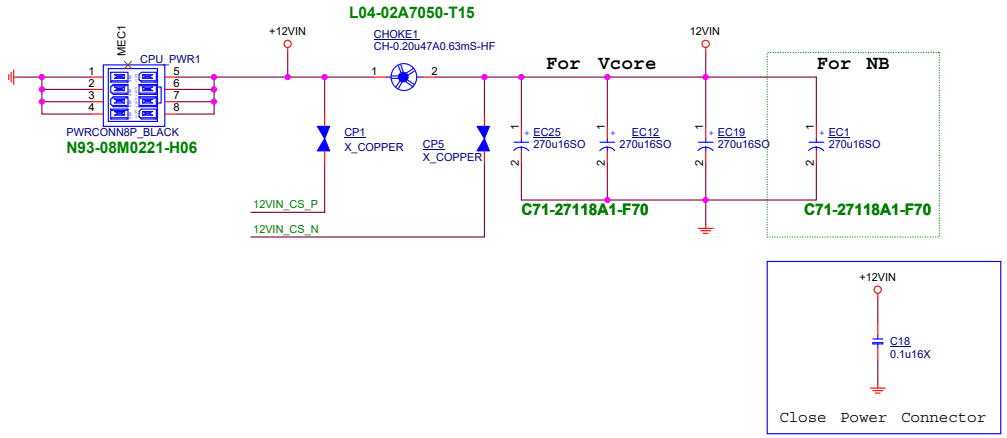


6,11,24 SCLK0
6,11,24 SDATA0

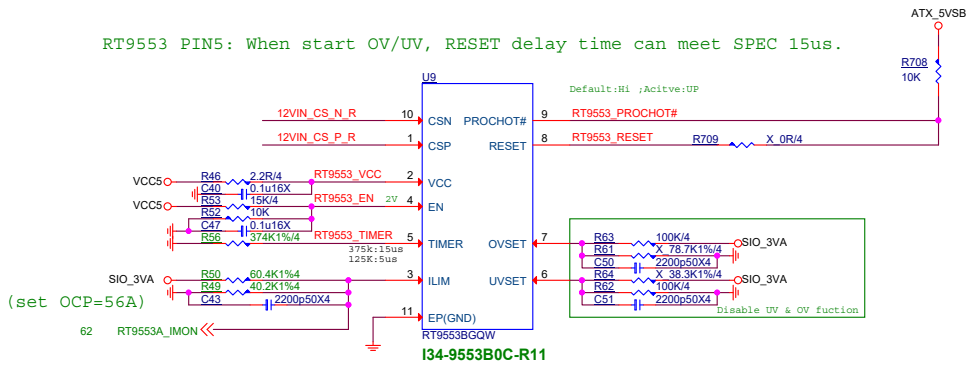
SCLK0
SDATA0

MICRO-STAR INT'L CO.,LTD			
MS-7C91..			
Size: Custom	Document Description: OV Control - NCT3933		Rev: 30
Date: Thursday, July 23, 2020		Sheet 62 of 78	

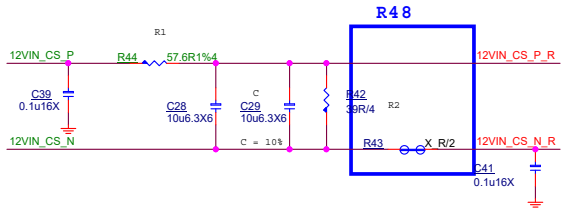
CPU POWER CONNECTOR



RT9553B CURRENT SENSE



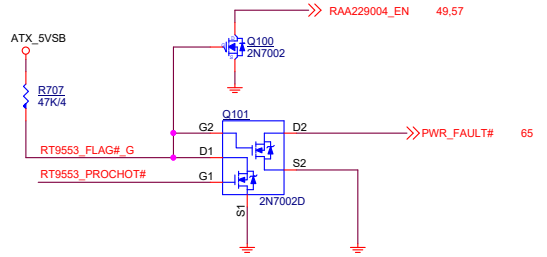
2020.03.25



$$\Delta\ VILIM=10uA*[(60.4K*40.2K)/(60.4K+40.2K)]$$
$$=226mV$$

$$Isense = VILIM / 100*Rsense$$

$$\Delta\ Isense=226mV/100*0.63m=3.58A$$



Vcore

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	2	> output Vcore
D	=	0.166667	

I o = Icore(max)*0.8			
I core(max)	=	200	> Vcore current
I avg.	=	160	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	10	phase
I ripple	=	5.962848	A

How many pcs. Of Cap.			
I ripple(cap)	=	4700	m A
COETEMP	=	1	
Input Cap.	=	2	pcs.

SOC

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.55	> output Vcore
D	=	0.129167	

I o = Icore(max)*0.8			
I core(max)	=	75	> Vcore current
I avg.	=	60	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	2	phase
I ripple	=	10.06153	A

How many pcs. Of Cap.			
I ripple(cap)	=	4700	m A
COETEMP	=	1	
Input Cap.	=	3	pcs.

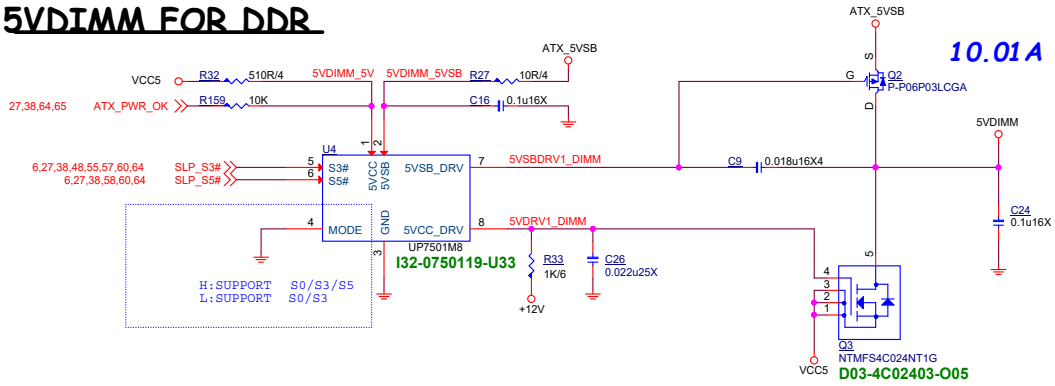
MICRO-STAR INT'L CO.,LTD

MS-7C91..

Size	Document Description	Rev
Custom	OCP 12VIN - RT9533B	30

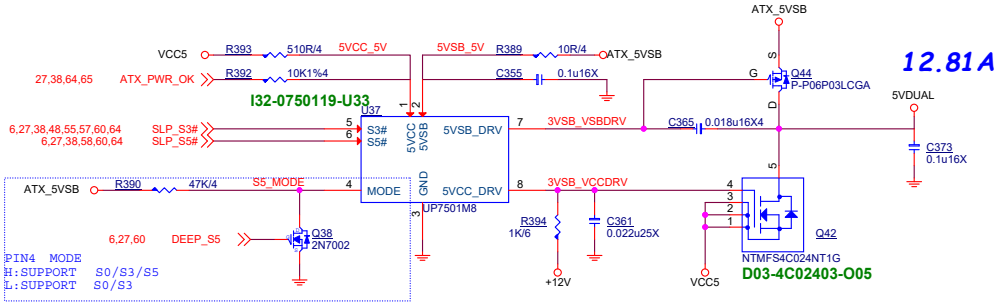
Date: Thursday, July 23, 2020 Sheet 63 of 78

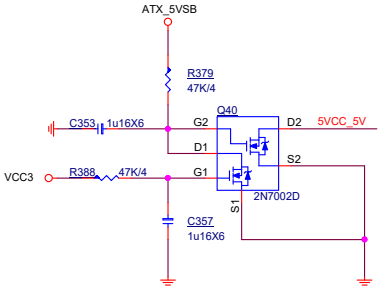
5VDIMM FOR DDR



5VDUAL For 3VSB/CPU1.8V/VDDP

LDOVDD=93.6mA
CPU_1P8_S5 VIN=3A
PM_1P05 VIN=2.1A
3VSB = 4.71A
LED_VCC5 = 3A



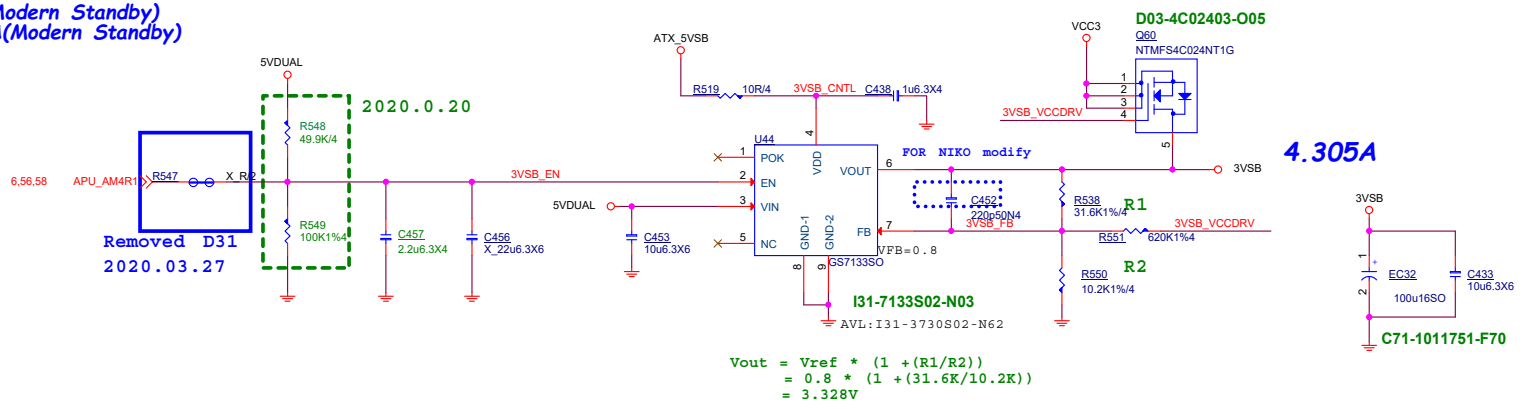


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

3VSB cost down

3.3V@4.305A

CPU:VDD_33_S5=0.25A
CHIP:VDD_33_S5=0.07A
PCIE=(375mA*5)=1.875A
M.2WIFI= 0.78A
RT8111H LAN=0.18A
PM_1P05_S5 :0.05A
PM_2P5V :0.9A(Modern Standby)
PCH VCC33 :0.2A(Modern Standby)



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(31.6K/10.2K))
= 3.328V

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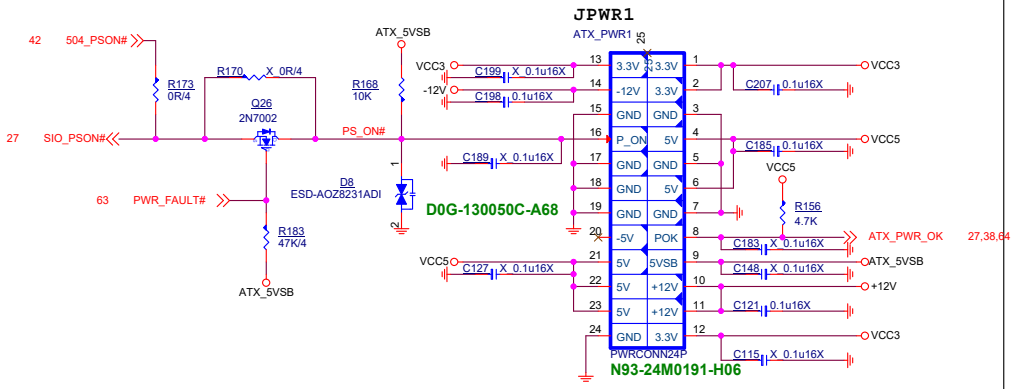
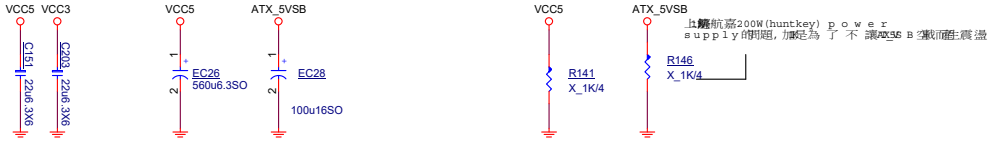
MS-7C91..		
Size: Custom	Document Description: ACPI - 5VDIMM / 3VSB	Rev: 30
Date: Thursday, July 23, 2020	Sheet 64 of 78	

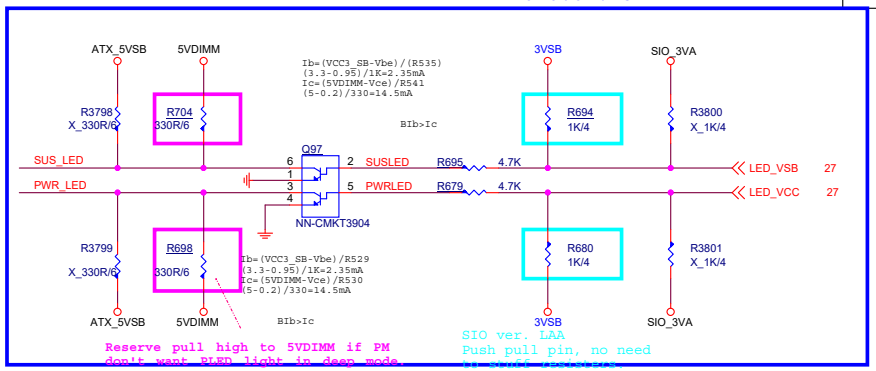
ATX POWER CONNECTOR



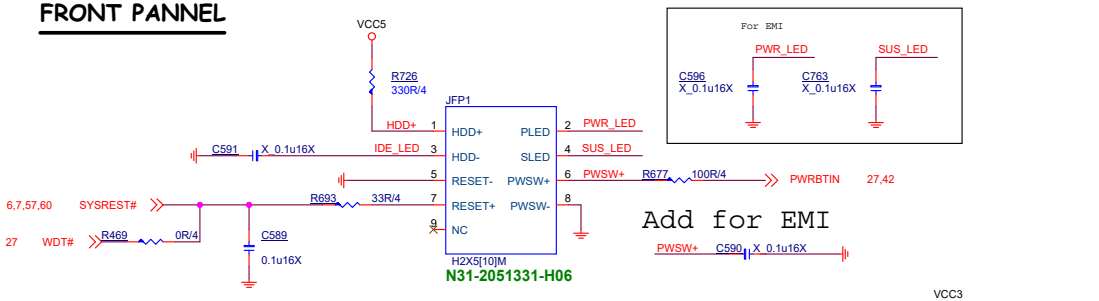


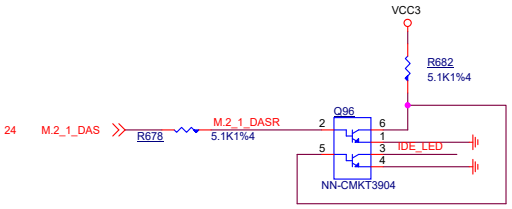
LED (for NCT6687D-R)

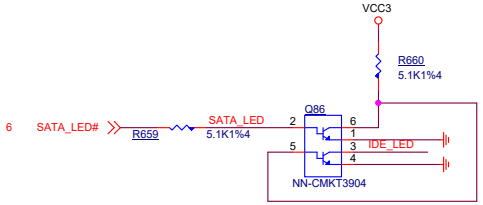
2020.04.13

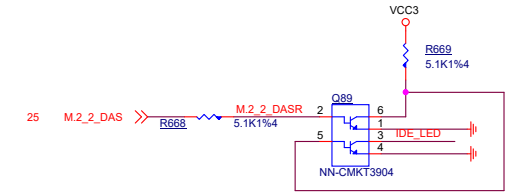


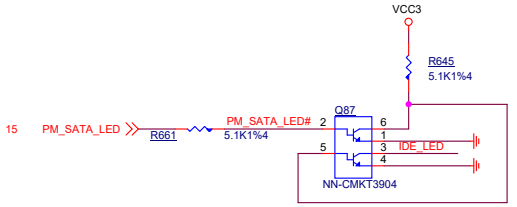
FRONT PANNEL

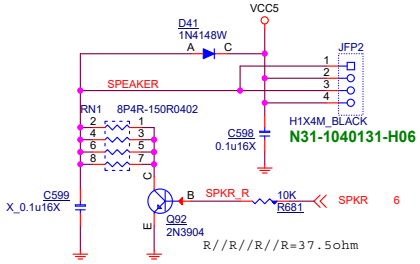












Voltage Mearsure Point

MSI

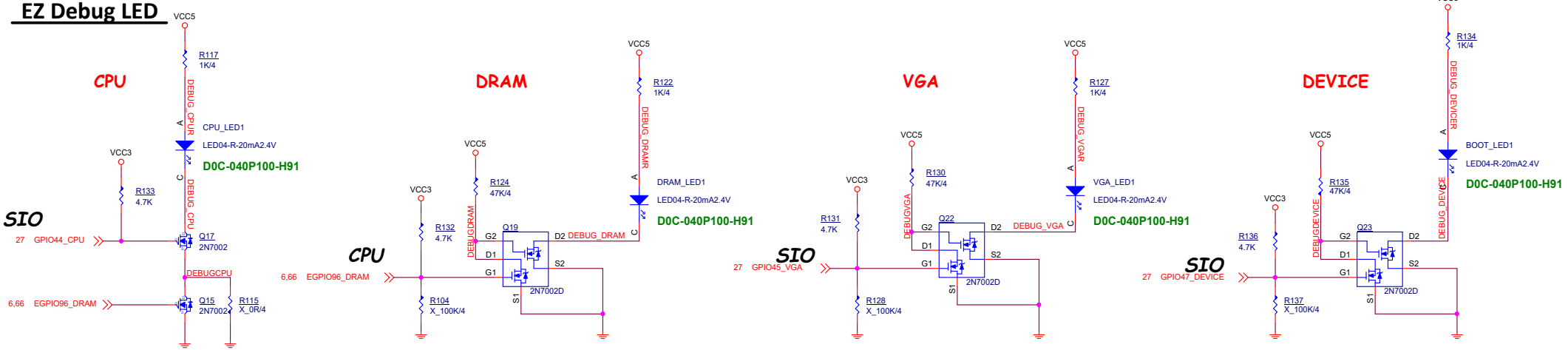
MICRO-STAR INT'L CO.,LTD

MS-7C91..

Size	Document Description	Rev
Custom	ATX power - FrontPanel / EMI	30

Date: Thursday, July 23, 2020 Sheet 65 of 78

EZ Debug LED



LEDGPIO	GPIO44	EGPIO96	GPIO45	GPIO47
亮	OPEN-Drain	GPO LOW	GPO LOW	GPO LOW
滅	GPO LOW	GPO HIGH	OPEN-Drain	OPEN-Drain

default Input

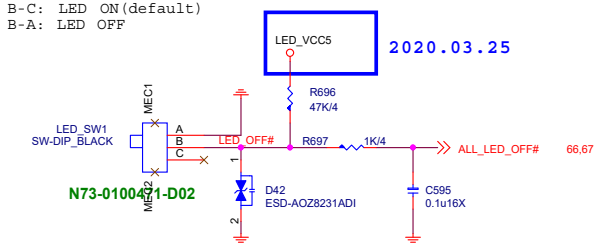
LED亮燈同時將CRUED關掉

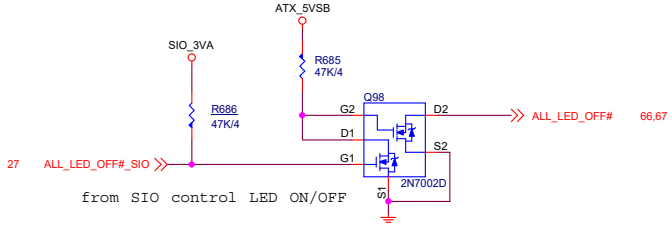
LED_SW1 FORM SIO

D0C-040P100-H91/D0C-040S500-E07

LED SW1 for ALL LED OFF

B-C: LED ON(default)
B-A: LED OFF





MICRO-STAR INT'L CO.,LTD	
MS-7C91..	
Size: Custom	Document Description: LED - EZ DEBUG / AMP
Rev: 30	
Date: Thursday, July 23, 2020	Sheet 66 of 78

48 PIN LED MCU

If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.

ADDRESS:0X52

2020.03.26
R806/R807

U59 NUC126NE4AE

PWM1 for JRGB1
RGB LED STRIPLINE USED

PWM3 for Others
According to demand configuration

PWM2 for JRGB2
RGB LED STRIPLINE USED

PIN1 for JPIPE1 & JRAINBOW1

PIN44 for JRAINBOW2

detect JRGB 12V

2020.03.25

COM1~8 for PWM3
According to demand configuration.
Can configuration COM1~8,
To achieve 8 group Non-synchronized onboard LED control.

COM9~13 for PWM2
According to demand configuration.
If SPEC. don't have JRGB2,
Can configuration COM9~13,
To achieve 5 group Non-synchronized onboard LED control.

PS. COM1 is the first action block, next is COM2, and so on.

Pin15,16 can configure to master smbus if spec requirement.

Remove Onboard RGB LED.

Remove Onboard RGB LED.

C1822 & C1823 near AVDD Pin. C1820 & C1821 near VDD Pin.
C1824 near VBAT Pin.
C1827 & C1828 near VDDIO & USB_VBUS Pin.

Clear MCU Circuit

Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2

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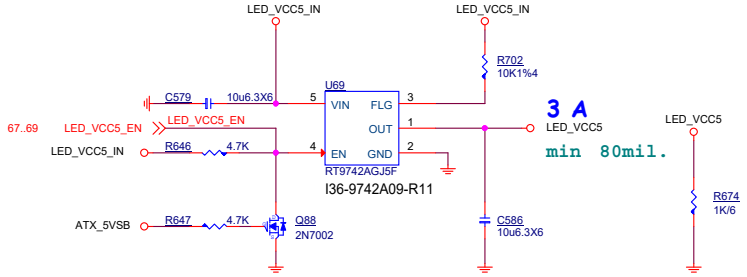
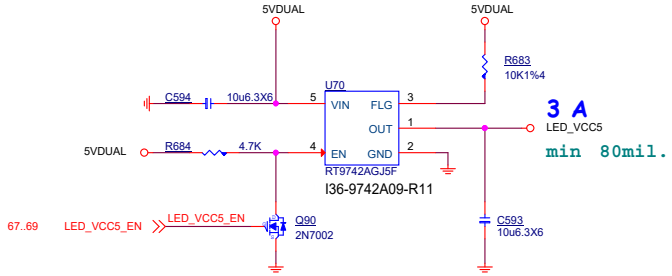
MS-7C91..

Size: Custom | Document Description: MCU - LED Control | Rev: 30

Date: Thursday, July 23, 2020 | Sheet 67 of 78

EXTERNAL POWER INPUT

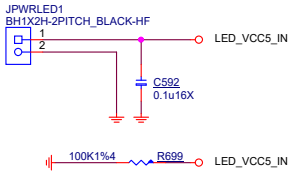




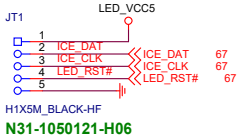
External Power

2A Connector

N32-1020CB1-H06

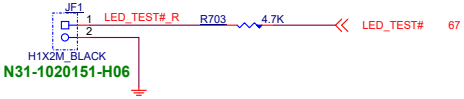


JT1 for FW update



N31-1050121-H06

JF1 for Factory test



N31-1020151-H06

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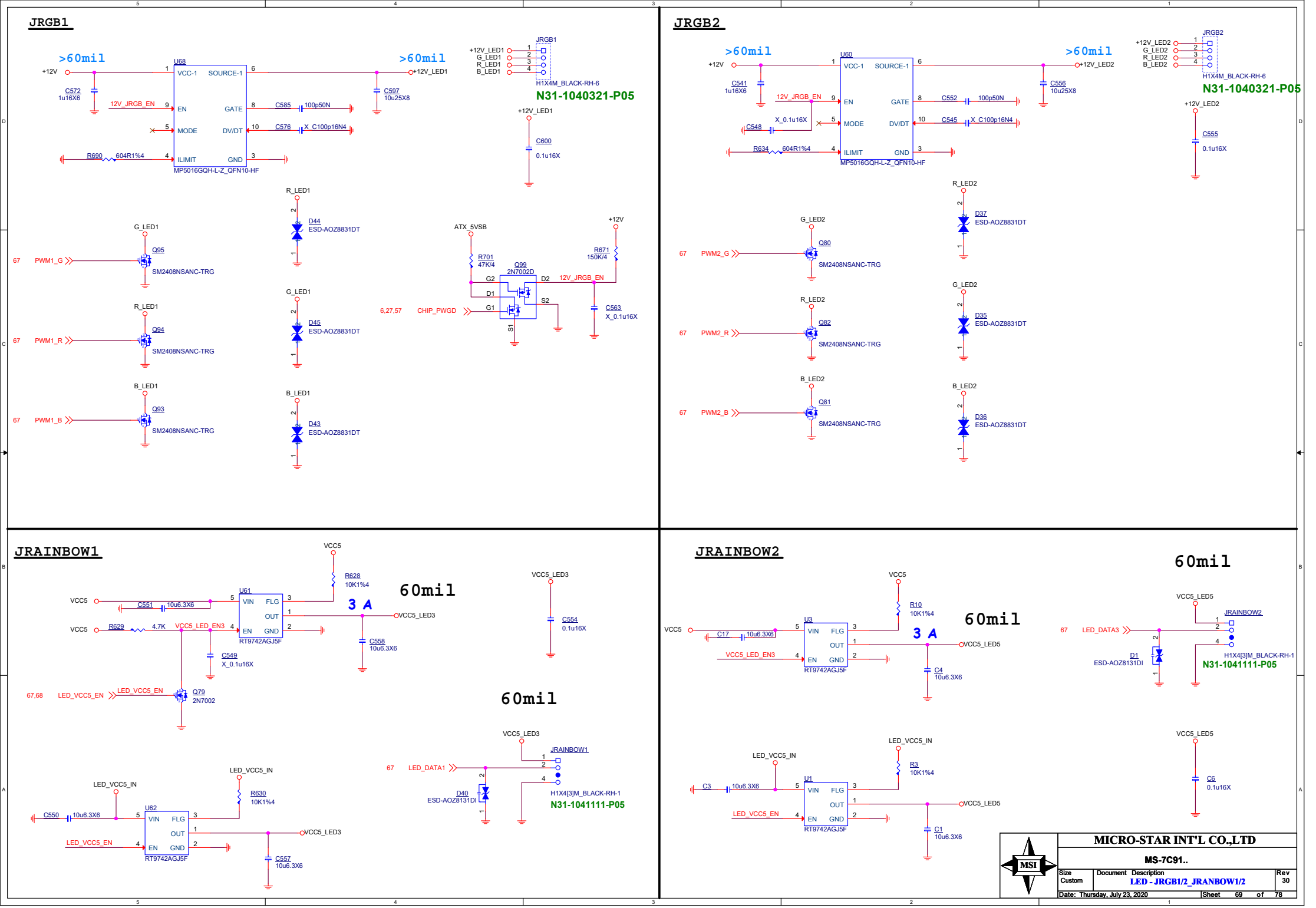
	MS-7C91..	
Size: Custom	Document Description: LED - Power / JPIPE	Rev: 30
Date: Thursday, July 23, 2020	Sheet 68 of 78	


JRGB1
>60mil
U68
+12V
VCC-1
SOURCE-1
+12V_LED1
C572
1u16X6
12V_JRGB_EN
EN
GATE
C585
100p50N
MODE
DV/DT
C576
X_C100p16N4
R690
604R1%4
ILIMIT
GND
MP5016GQH-L-Z_QFN10-HF
C597
10u25X8
JRGB1
G_LED1
R_LED1
B_LED1
H1X4M_BLACK-RH-6
N31-1040321-P05
C600
0.1u16X
R_LED1
D44
ESD-AOZ8831DT
G_LED1
D45
ESD-AOZ8831DT
B_LED1
D43
ESD-AOZ8831DT
PWM1_G
Q95
SM2408NSANC-TRG
PWM1_R
Q94
SM2408NSANC-TRG
PWM1_B
Q93
SM2408NSANC-TRG
ATX_5VSB
R701
47K/4
Q99
2N7002D
G2
D1
G1
D2
S2
S1
R671
150K/4
12V_JRGB_EN
C563
X_0.1u16X
6,27,57
CHIP_PWGD
JRGB2
>60mil
U60
+12V
VCC-1
SOURCE-1
+12V_LED2
C541
1u16X6
12V_JRGB_EN
EN
GATE
C552
100p50N
X_0.1u16X
C548
MODE
DV/DT
C545
X_C100p16N4
R634
604R1%4
ILIMIT
GND
MP5016GQH-L-Z_QFN10-HF
C556
10u25X8
JRGB2
G_LED2
R_LED2
B_LED2
H1X4M_BLACK-RH-6
N31-1040321-P05
C555
0.1u16X
R_LED2
D37
ESD-AOZ8831DT
G_LED2
D35
ESD-AOZ8831DT
B_LED2
D36
ESD-AOZ8831DT
PWM2_G
Q80
SM2408NSANC-TRG
PWM2_R
Q82
SM2408NSANC-TRG
PWM2_B
Q81
SM2408NSANC-TRG
JRAINBOW1
VCC5
R628
10K1%4
60mil
3 A
U61
VCC5
C551
10u6.3X6
VIN
FLG
OUT
VCC5_LED3
R629
4.7K
VCC5_LED_EN3
EN
GND
RT9742AGJ5F
C549
X_0.1u16X
C558
10u6.3X6
67,68
LED_VCC5_EN
Q79
2N7002
C554
0.1u16X
60mil
VCC5_LED3
JRAINBOW1
67
LED_DATA1
D40
ESD-AOZ8131DI
H1X4[3]M_BLACK-RH-1
N31-1041111-P05
LED_VCC5_IN
R630
10K1%4
U62
C550
10u6.3X6
C557
10u6.3X6
JRAINBOW2
60mil
VCC5
R10
10K1%4
U3
C17
10u6.3X6
3 A
VCC5_LED5
C4
10u6.3X6
VCC5_LED5
JRAINBOW2
67
LED_DATA3
D1
ESD-AOZ8131DI
H1X4[3]M_BLACK-RH-1
N31-1041111-P05
LED_VCC5_IN
R3
10K1%4
U1
C3
10u6.3X6
C1
10u6.3X6
C6
0.1u16X
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MS-7C91..
Size
Custom
Document Description
LED - JRGB1/2_JRANBOW1/2
Rev
30
Date: Thursday, July 23, 2020
Sheet 69 of 78

BOARD SIDE LED *6

Remove Onboard RGB LED.

MICRO-STAR INT'L CO.,LTD	
MS-7C91..	
Size: Custom	Document Description: LED - Mystic Light - 1
Rev: 30	
Date: Thursday, July 23, 2020	Sheet 70 of 78

601-7C91-01S ---> for 2.0
601-7C91-02S --> for 2.1
601-7C91-010 --> for 2.1(MP)

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MS-7C91..		
Size: Custom	Document Description: BOM Option	Rev: 30
Date: Thursday, July 23, 2020	Sheet 71 of 78	

CPU Socket

CPU2

E95-0000022-A91

E95-0000022-A91

Simulation

X_JS1 — SIM1 — X_PIN1*2

X_JS2 — SIM2 — X_PIN1*2

X_JS3 — SIM3 — X_PIN1*2

FM2 FM3 FM1 — X_FM120

FM4 FM5 FM6 — X_FM120

FM8 FM7 — X_FM120

Optics Orientation Holes

MH1 MH2 MH3 MH5 MH6 MH4 MH7 MH8 MH9 — X_MH001

C575 0.1u16X

C559 0.1u16X

2020.04.15

MANUAL PART

AMI_LAB1 — G51-M1SPXXA-A09

G51-M1SPXXA-A09

CFOS1 <MSI-BOM> — Y02-MU00170-CFO

Y02-MU00170-CFO

HDMI_LA1 — Label — HDMI

HDMI LABEL

Y01-RHDMI03-000

MKT_LA1 — Label — MKT_LABEL

X_MKT LABEL

G51-M1SPP78-Q13

BAT1_X1

BAT-I.SOBCR2032P

AVL:
D06-0100161-F52
D06-0100101-K26

PCB

PCB

PCB1

7C91_21

PD0-07C9121-E48
PD0-07C9121-G37

Moat CAP

Reserve for bypass 12VIN noise use

ATX_5VSB — C5 C2 — X_0.1u16X

Reserve for bypass VCC5/VCC3/3VSB noise use

VCC5 — C1658 C1659 — X_0.1u16X

VCC3 — C1660 C1661 — X_0.1u16X

3VSB — C1662 — X_0.1u16X

2020.04.14

MOS HEATSINK

N MOS

HS_MOS1 — MEC2 — MEC1

NHS-AURAS(0P10B08484)

E31-0506780-A87

W MOS

HS_MOS2 — MEC2 — MEC1

WHS-AURAS(0P10B08483)

E31-0506770-A87

PCH HEATSINK

PM_HS1 — MEC1 — MEC2

PHS-AURAS(0P10B08485)

E31-0410540-A87

M2 COVER

20200716 Remove M2_1_HS1/M2_1_HS2

IO BRACKET

20200716 Remove IO_BKT1.

DDR COVER

20190201 Remove DDR_COVER1

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Size: Custom | Document Description: Manual Parts | Rev: 30

Date: Friday, July 24, 2020 | Sheet 72 of 78