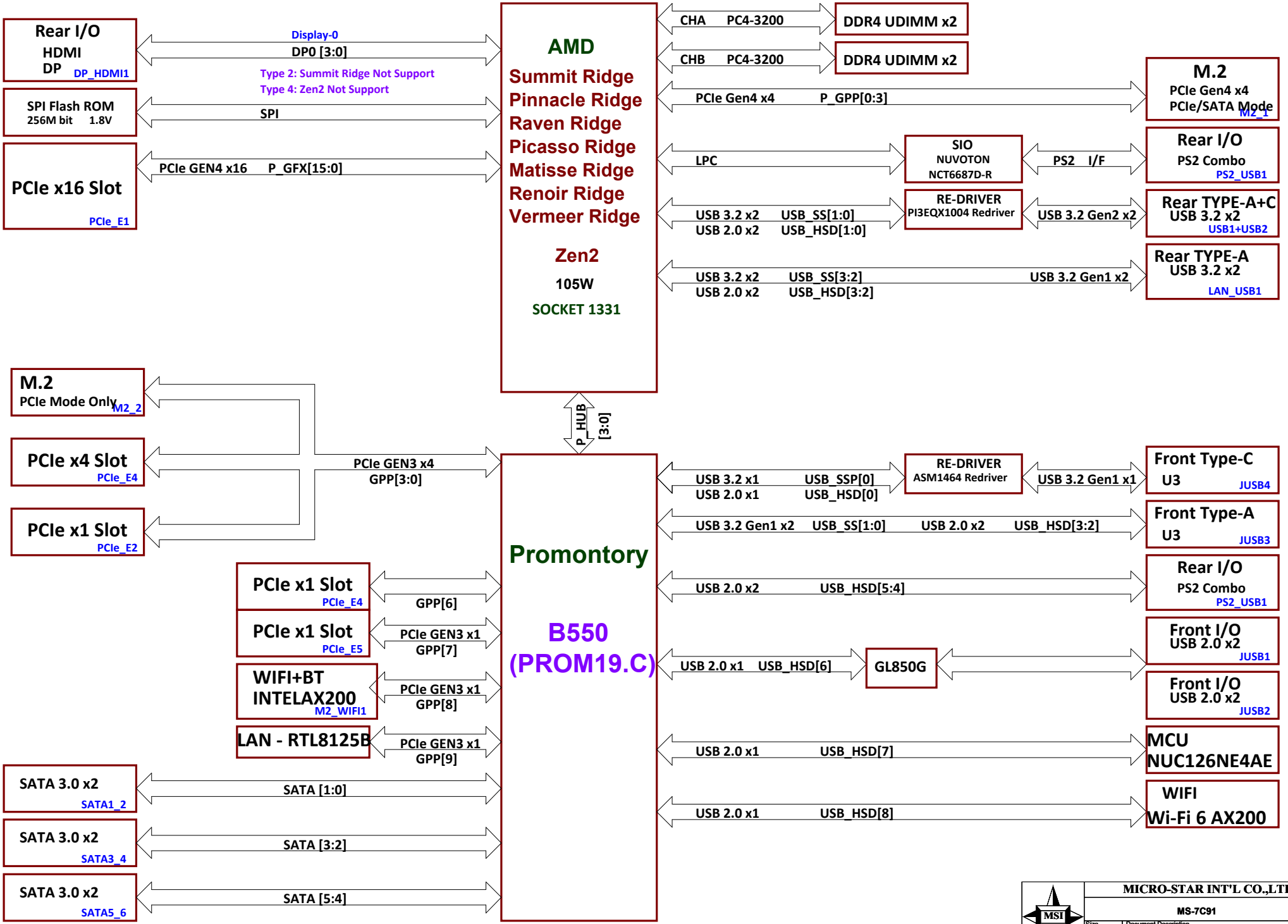
AMD AM4
B550

MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	Cover Sheet	10

Date: Tuesday, April 21, 2020 Sheet 1 of 78

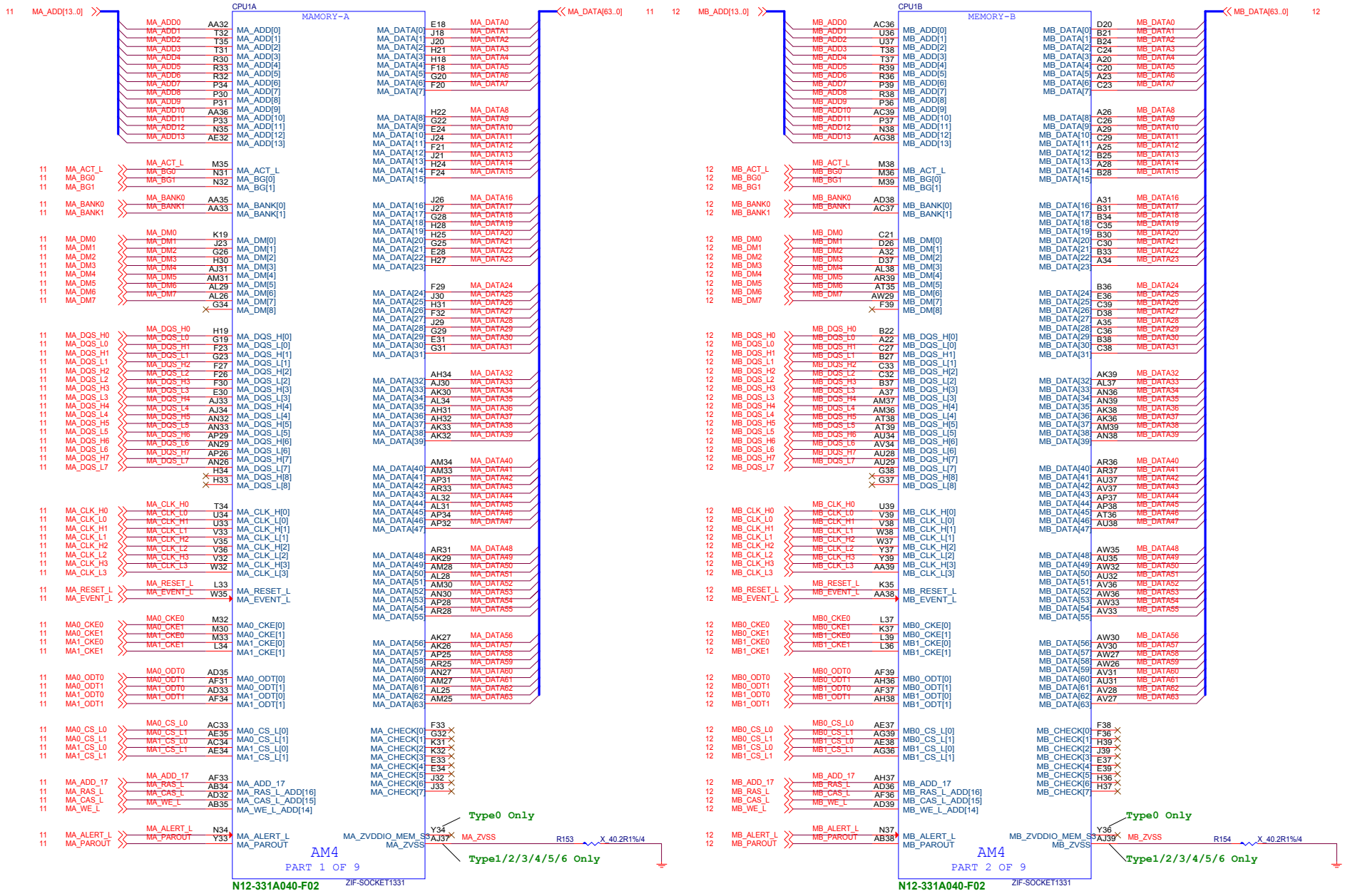


MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	Block Diagram	10

Date: Tuesday, April 21, 2020 Sheet 2 of 78

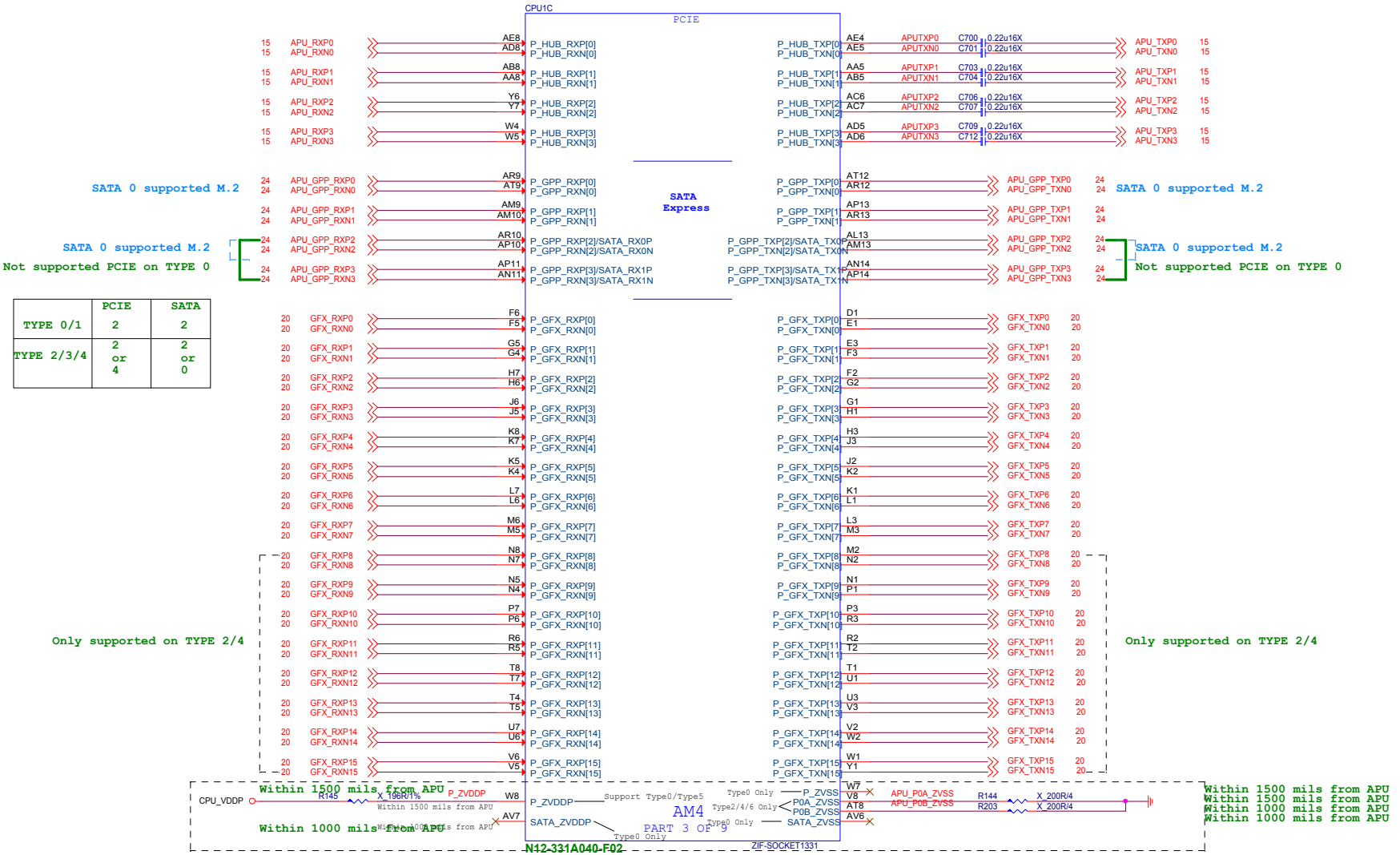


MICRO-STAR INT'L CO.,LTD

MS-7C91

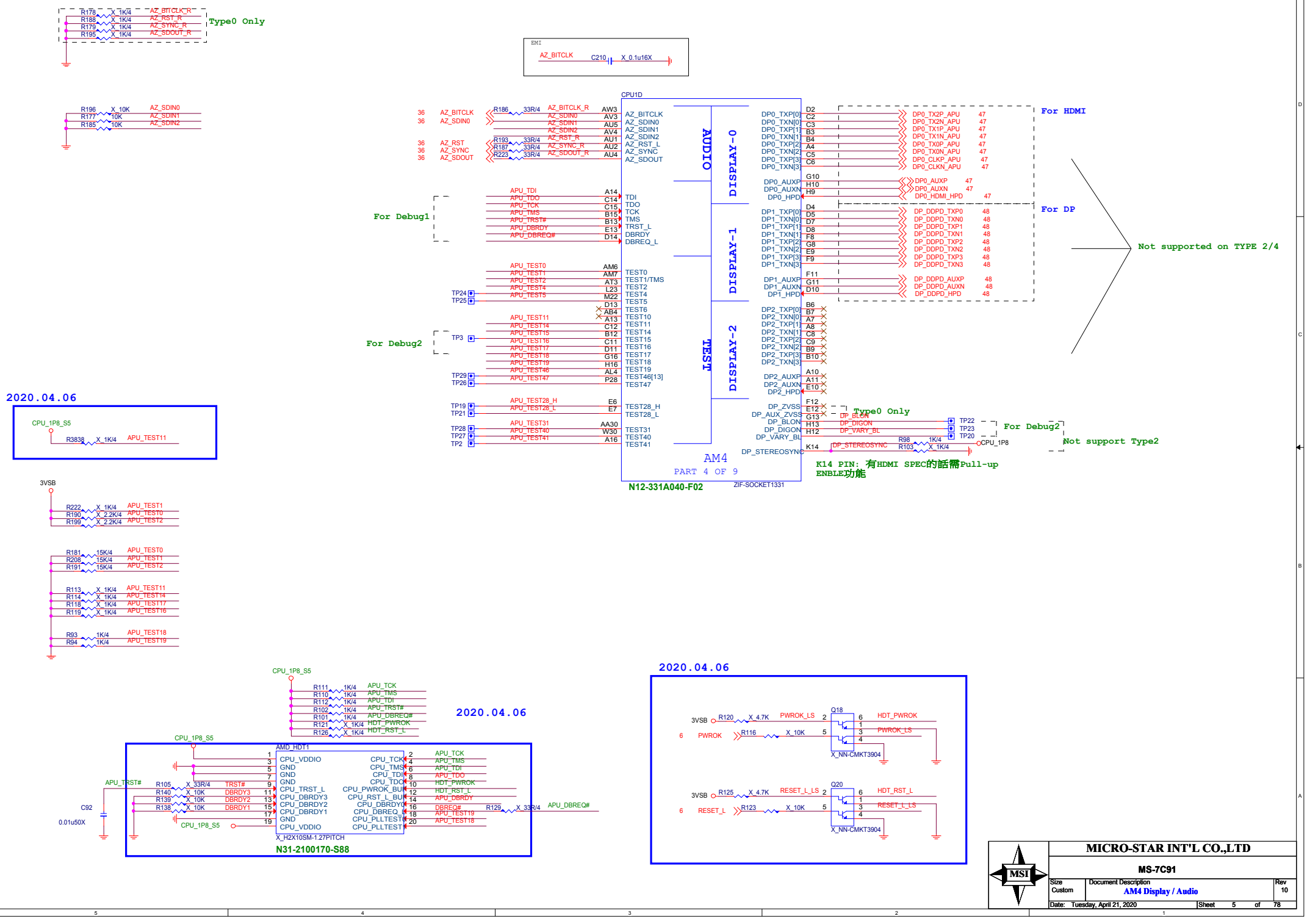
Size	Document Description	Rev
Custom	AM4 DDR4 I/F	10

Date: Tuesday, April 21, 2020 | Sheet 3 of 78



	PCIE	SATA
TYPE 0/1	2	2
TYPE 2/3/4	2 or 4	2 or 0

MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: AM4 PCIE / SATAE
Rev: 10	
Date: Tuesday, April 21, 2020	Sheet 4 of 78

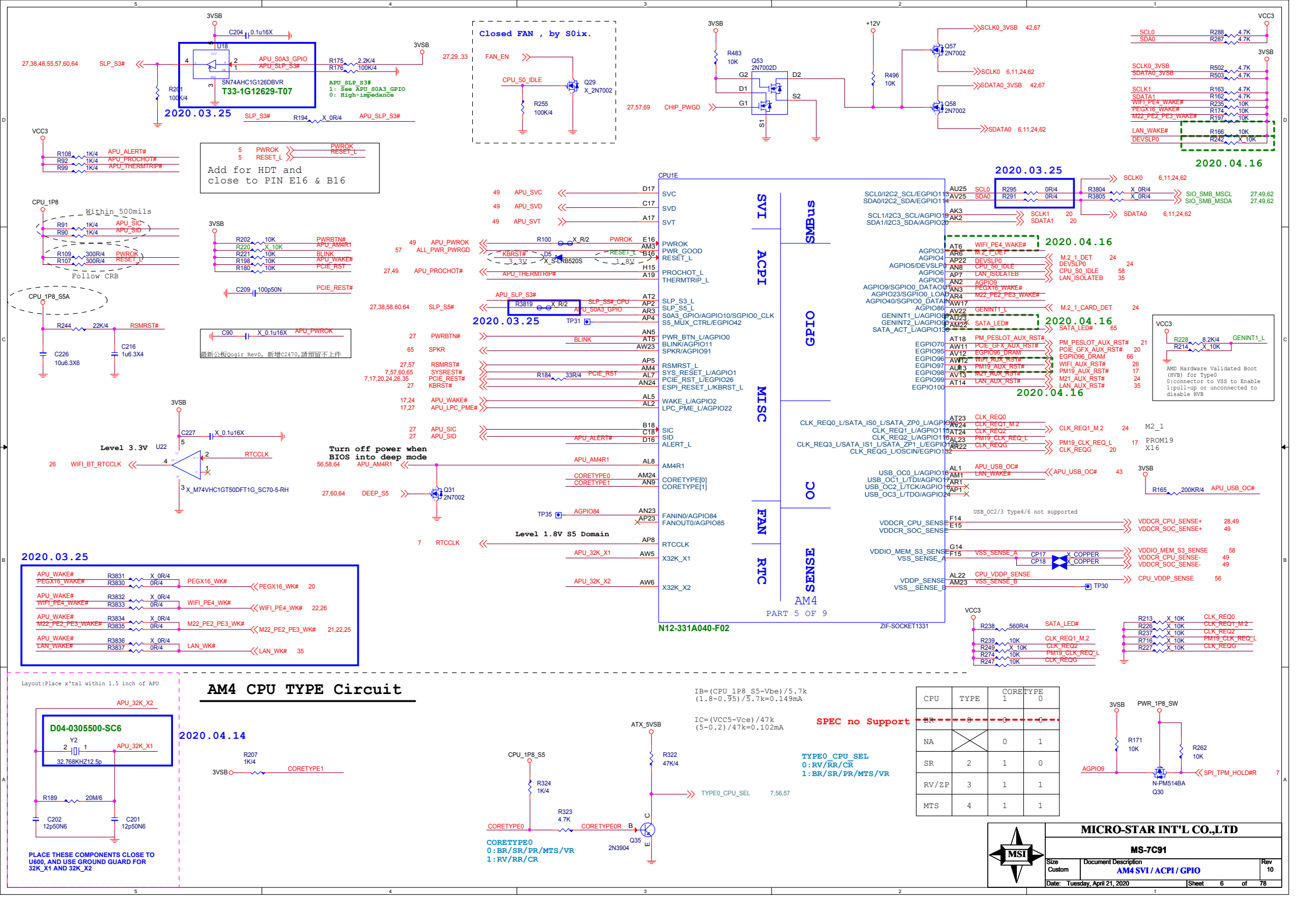


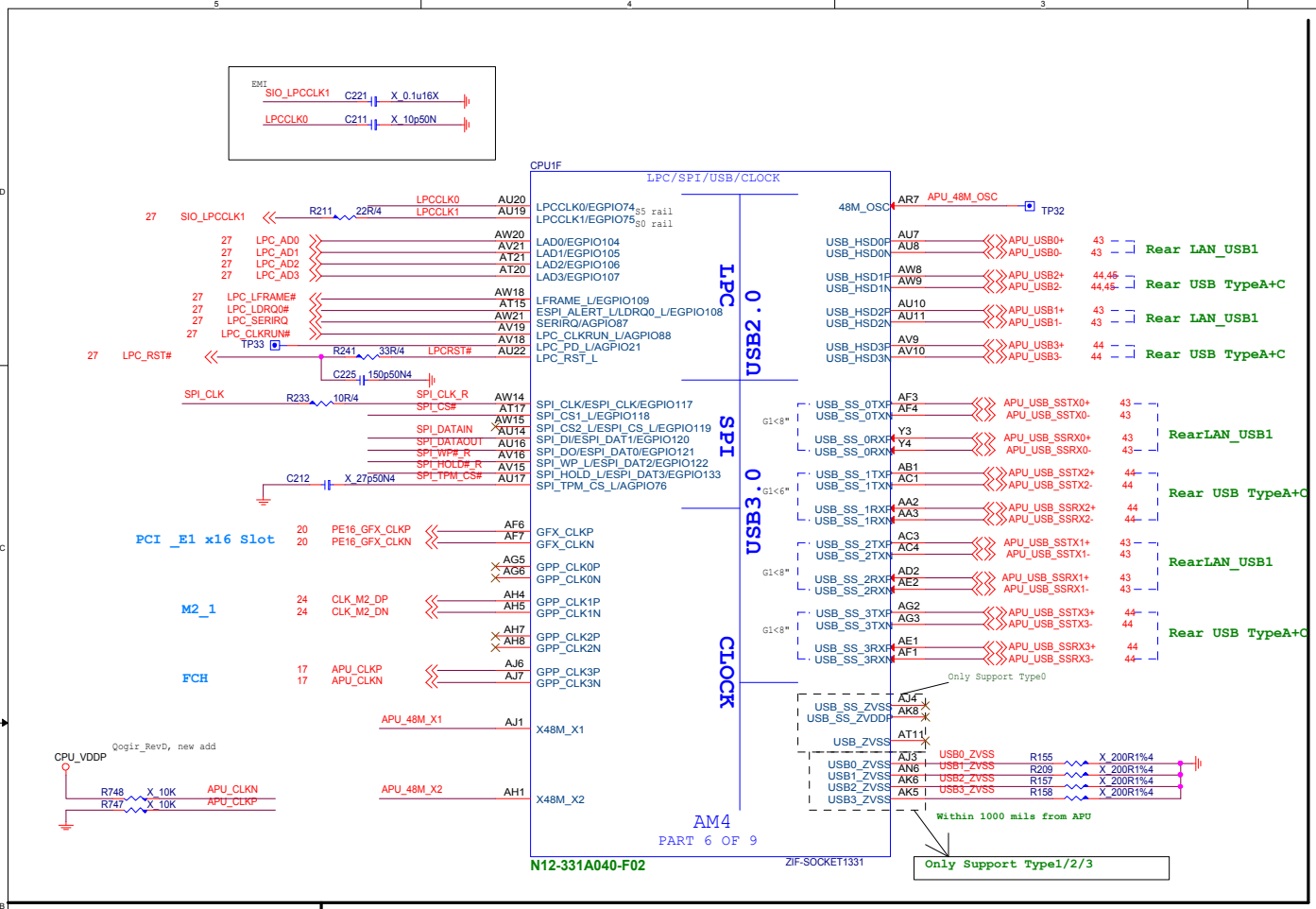
MICRO-STAR INT'L CO.,LTD

MS-7C91

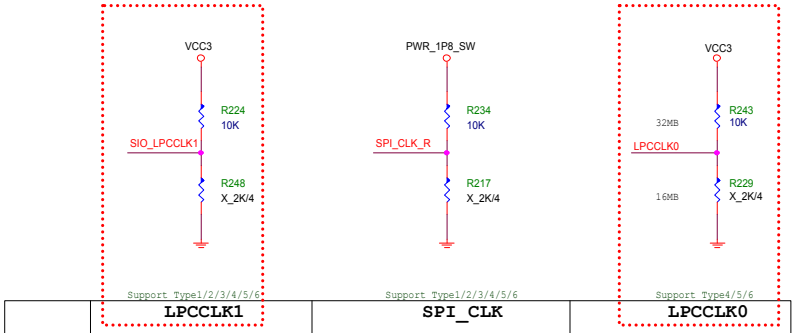
Size	Document Description	Rev
Custom	AM4 Display / Audio	10

Date: Tuesday, April 21, 2020 Sheet 5 of 78

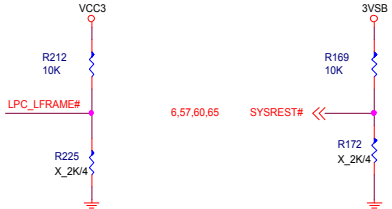

Closed FAN , by S0ix.
Add for HDT and close to PIN E16 & B16
Follow CRB
Within_500mils
Level 3.3V U22
Level 1.8V S5 Domain
Turn off power when BIOS into deep mode
2020.03.25
2020.04.16
2020.04.14
AM4 CPU TYPE Circuit
CPU1E
SVI
ACPI
GPIO
MISC
OC
FAN
RTC
SMBus
SENSE
AM4
PART 5 OF 9
N12-331A040-F02
ZIF-SOCKET1331
SPEC no Support
TYPE0_CPU_SEL
0:RV/RR/CR
1:BR/SR/PR/MTS/VR
CORETYPE0
0:BR/SR/PR/MTS/VR
1:RV/RR/CR
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2
MICRO-STAR INT'L CO.,LTD
MS-7C91
AM4 SVI / ACPI / GPIO
Date: Tuesday, April 21, 2020
Sheet 6 of 78



Strapping Options

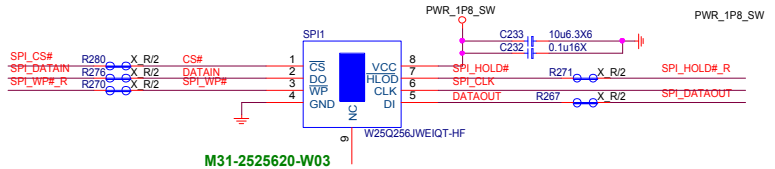


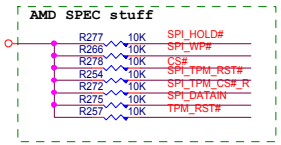
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image **(Default)**
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]

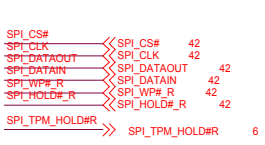


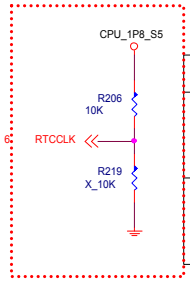
	AGPIO3	LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic **(Default)**	SPI ROM **(Default)**	Normal reset mode **(Default)**
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

SPI ROM(1.8V)



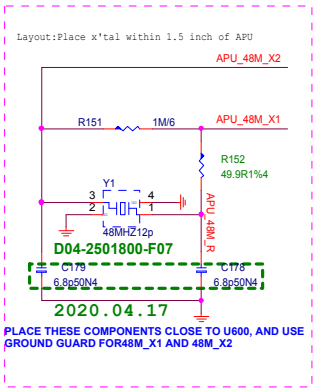


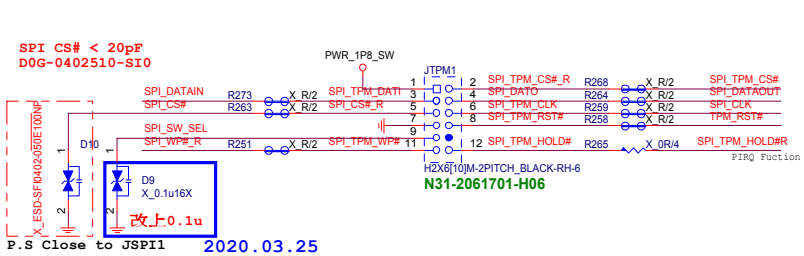


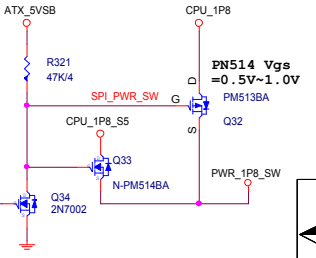


	RTCCLK
PULL HIGH	RTCCLK is input and is used as the bypass clock **(Default)**
PULL LOW	Normal Mode: Use 32Khz xtal as the source of RTC clock

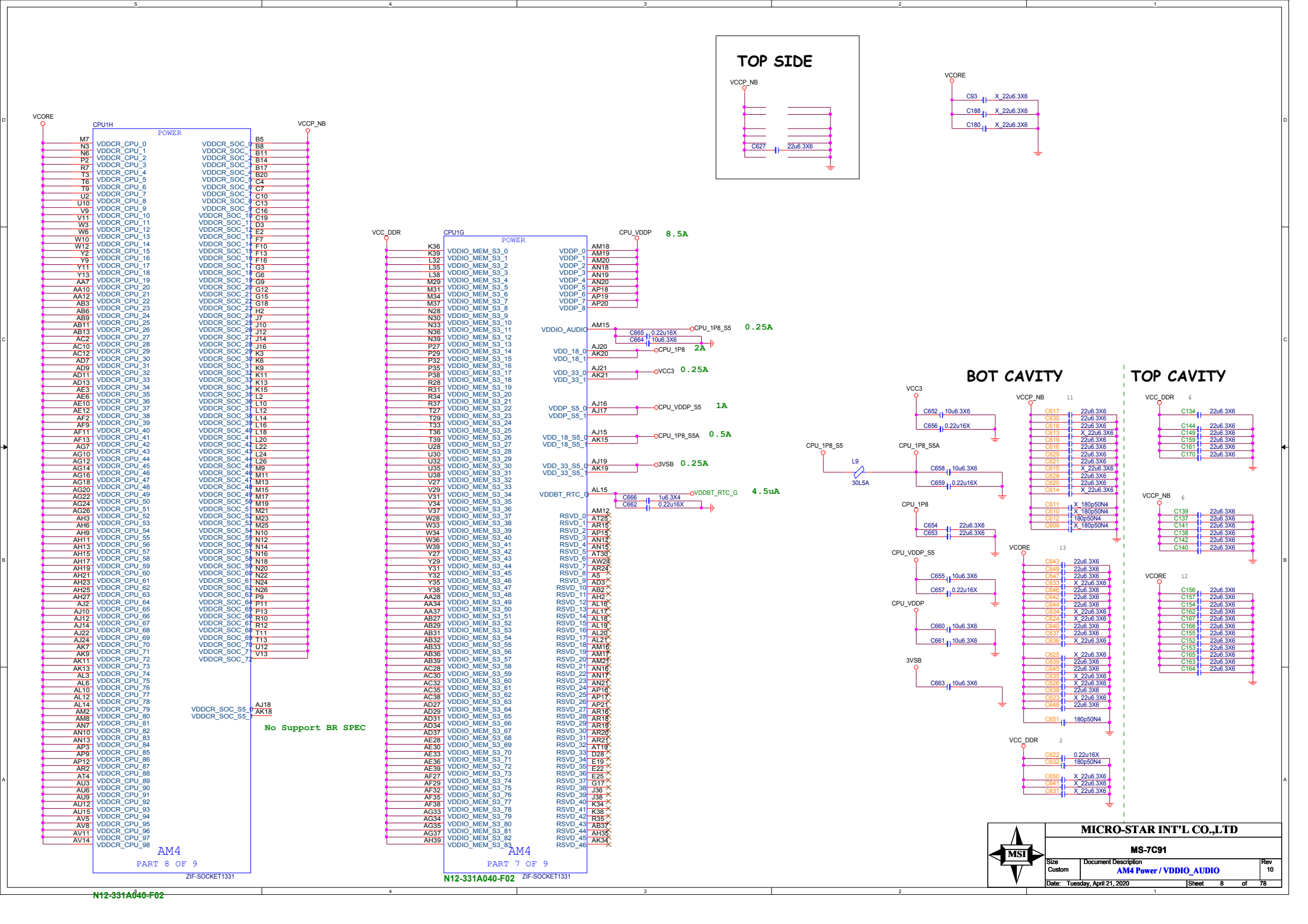
Support Type4/6

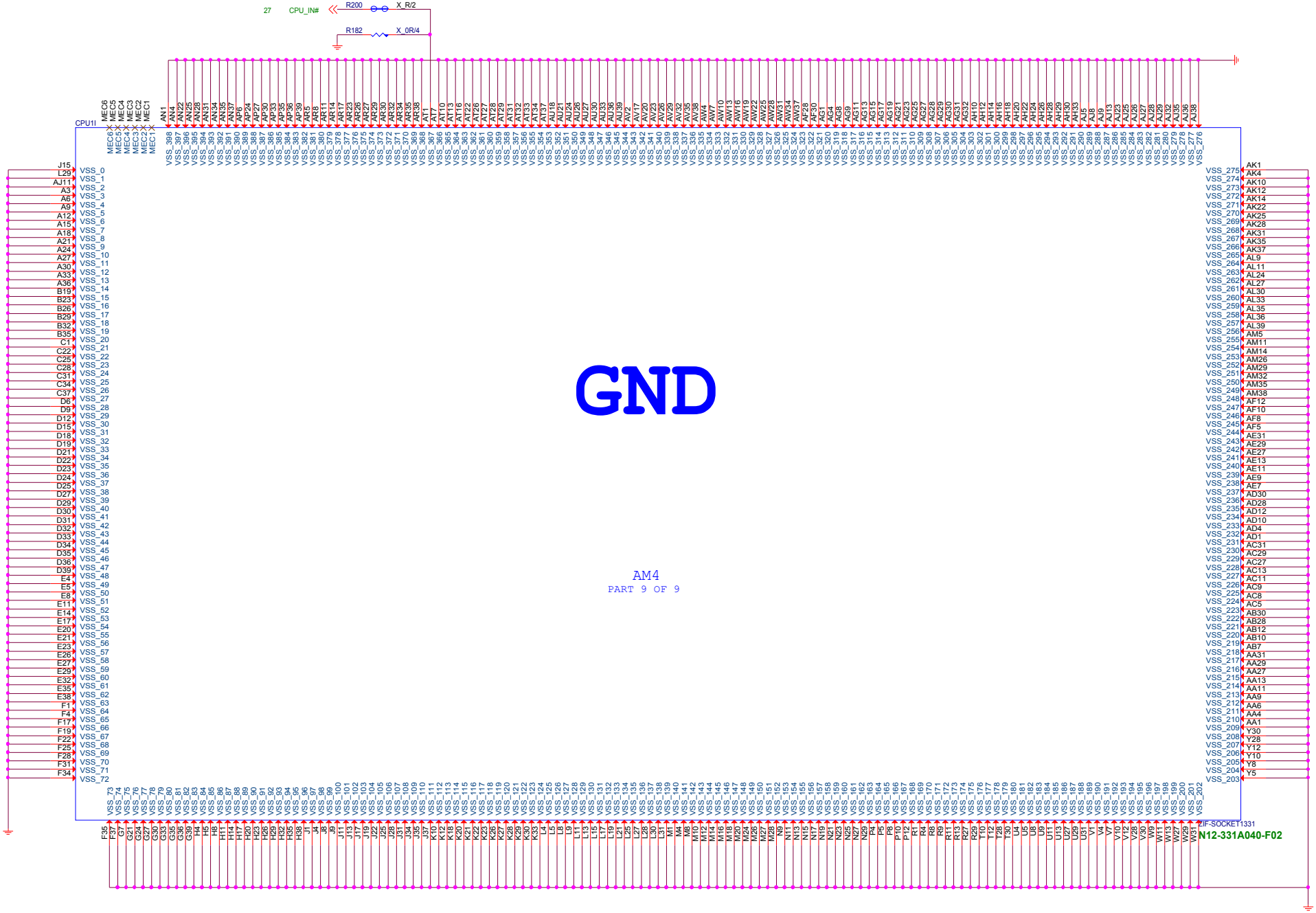






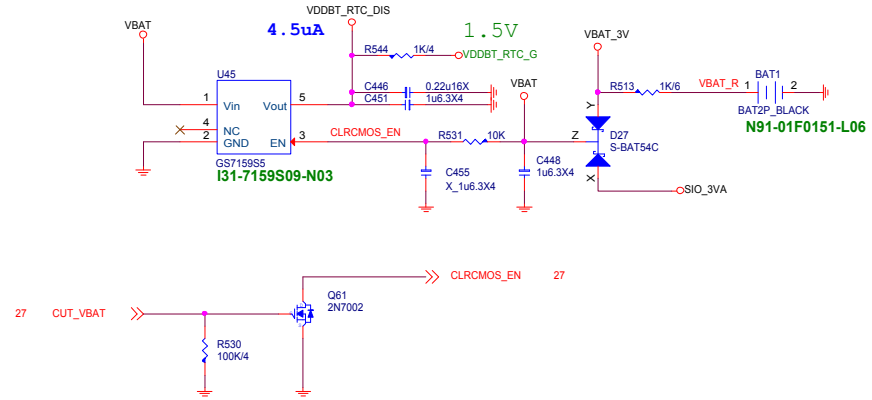
MICRO-STAR INT'L CO.,LTD			
MS-7C91			
Size: Custom	Document Description: AM4 LPC / SPI / USB / CLK / STRAP		Rev: 10
Date: Tuesday, April 21, 2020		Sheet 7 of 78	


TOP SIDE
VCCP_NB
C627
22u6.3X6
VCORE
C93
X_22u6.3X6
C188
X_22u6.3X6
C180
X_22u6.3X6
VCORE
CPU1H
POWER
VCCP_NB
VDDCR_CPU_0
VDDCR_CPU_1
VDDCR_CPU_2
VDDCR_CPU_3
VDDCR_CPU_4
VDDCR_CPU_5
VDDCR_CPU_6
VDDCR_CPU_7
VDDCR_CPU_8
VDDCR_CPU_9
VDDCR_CPU_10
VDDCR_CPU_11
VDDCR_CPU_12
VDDCR_CPU_13
VDDCR_CPU_14
VDDCR_CPU_15
VDDCR_CPU_16
VDDCR_CPU_17
VDDCR_CPU_18
VDDCR_CPU_19
VDDCR_CPU_20
VDDCR_CPU_21
VDDCR_CPU_22
VDDCR_CPU_23
VDDCR_CPU_24
VDDCR_CPU_25
VDDCR_CPU_26
VDDCR_CPU_27
VDDCR_CPU_28
VDDCR_CPU_29
VDDCR_CPU_30
VDDCR_CPU_31
VDDCR_CPU_32
VDDCR_CPU_33
VDDCR_CPU_34
VDDCR_CPU_35
VDDCR_CPU_36
VDDCR_CPU_37
VDDCR_CPU_38
VDDCR_CPU_39
VDDCR_CPU_40
VDDCR_CPU_41
VDDCR_CPU_42
VDDCR_CPU_43
VDDCR_CPU_44
VDDCR_CPU_45
VDDCR_CPU_46
VDDCR_CPU_47
VDDCR_CPU_48
VDDCR_CPU_49
VDDCR_CPU_50
VDDCR_CPU_51
VDDCR_CPU_52
VDDCR_CPU_53
VDDCR_CPU_54
VDDCR_CPU_55
VDDCR_CPU_56
VDDCR_CPU_57
VDDCR_CPU_58
VDDCR_CPU_59
VDDCR_CPU_60
VDDCR_CPU_61
VDDCR_CPU_62
VDDCR_CPU_63
VDDCR_CPU_64
VDDCR_CPU_65
VDDCR_CPU_66
VDDCR_CPU_67
VDDCR_CPU_68
VDDCR_CPU_69
VDDCR_CPU_70
VDDCR_CPU_71
VDDCR_CPU_72
VDDCR_CPU_73
VDDCR_CPU_74
VDDCR_CPU_75
VDDCR_CPU_76
VDDCR_CPU_77
VDDCR_CPU_78
VDDCR_CPU_79
VDDCR_CPU_80
VDDCR_CPU_81
VDDCR_CPU_82
VDDCR_CPU_83
VDDCR_CPU_84
VDDCR_CPU_85
VDDCR_CPU_86
VDDCR_CPU_87
VDDCR_CPU_88
VDDCR_CPU_89
VDDCR_CPU_90
VDDCR_CPU_91
VDDCR_CPU_92
VDDCR_CPU_93
VDDCR_CPU_94
VDDCR_CPU_95
VDDCR_CPU_96
VDDCR_CPU_97
VDDCR_CPU_98
VDDCR_SOC_0
VDDCR_SOC_1
VDDCR_SOC_2
VDDCR_SOC_3
VDDCR_SOC_4
VDDCR_SOC_5
VDDCR_SOC_6
VDDCR_SOC_7
VDDCR_SOC_8
VDDCR_SOC_9
VDDCR_SOC_10
VDDCR_SOC_11
VDDCR_SOC_12
VDDCR_SOC_13
VDDCR_SOC_14
VDDCR_SOC_15
VDDCR_SOC_16
VDDCR_SOC_17
VDDCR_SOC_18
VDDCR_SOC_19
VDDCR_SOC_20
VDDCR_SOC_21
VDDCR_SOC_22
VDDCR_SOC_23
VDDCR_SOC_24
VDDCR_SOC_25
VDDCR_SOC_26
VDDCR_SOC_27
VDDCR_SOC_28
VDDCR_SOC_29
VDDCR_SOC_30
VDDCR_SOC_31
VDDCR_SOC_32
VDDCR_SOC_33
VDDCR_SOC_34
VDDCR_SOC_35
VDDCR_SOC_36
VDDCR_SOC_37
VDDCR_SOC_38
VDDCR_SOC_39
VDDCR_SOC_40
VDDCR_SOC_41
VDDCR_SOC_42
VDDCR_SOC_43
VDDCR_SOC_44
VDDCR_SOC_45
VDDCR_SOC_46
VDDCR_SOC_47
VDDCR_SOC_48
VDDCR_SOC_49
VDDCR_SOC_50
VDDCR_SOC_51
VDDCR_SOC_52
VDDCR_SOC_53
VDDCR_SOC_54
VDDCR_SOC_55
VDDCR_SOC_56
VDDCR_SOC_57
VDDCR_SOC_58
VDDCR_SOC_59
VDDCR_SOC_60
VDDCR_SOC_61
VDDCR_SOC_62
VDDCR_SOC_63
VDDCR_SOC_64
VDDCR_SOC_65
VDDCR_SOC_66
VDDCR_SOC_67
VDDCR_SOC_68
VDDCR_SOC_69
VDDCR_SOC_70
VDDCR_SOC_71
VDDCR_SOC_72
VDDCR_SOC_S5_0
VDDCR_SOC_S5_1
No Support BR SPEC
AM4
PART 8 OF 9
ZIF-SOCKET1331
N12-331A040-F02
VCC_DDR
CPU1G
POWER
VDDIO_MEM_S3_0
VDDIO_MEM_S3_1
VDDIO_MEM_S3_2
VDDIO_MEM_S3_3
VDDIO_MEM_S3_4
VDDIO_MEM_S3_5
VDDIO_MEM_S3_6
VDDIO_MEM_S3_7
VDDIO_MEM_S3_8
VDDIO_MEM_S3_9
VDDIO_MEM_S3_10
VDDIO_MEM_S3_11
VDDIO_MEM_S3_12
VDDIO_MEM_S3_13
VDDIO_MEM_S3_14
VDDIO_MEM_S3_15
VDDIO_MEM_S3_16
VDDIO_MEM_S3_17
VDDIO_MEM_S3_18
VDDIO_MEM_S3_19
VDDIO_MEM_S3_20
VDDIO_MEM_S3_21
VDDIO_MEM_S3_22
VDDIO_MEM_S3_23
VDDIO_MEM_S3_24
VDDIO_MEM_S3_25
VDDIO_MEM_S3_26
VDDIO_MEM_S3_27
VDDIO_MEM_S3_28
VDDIO_MEM_S3_29
VDDIO_MEM_S3_30
VDDIO_MEM_S3_31
VDDIO_MEM_S3_32
VDDIO_MEM_S3_33
VDDIO_MEM_S3_34
VDDIO_MEM_S3_35
VDDIO_MEM_S3_36
VDDIO_MEM_S3_37
VDDIO_MEM_S3_38
VDDIO_MEM_S3_39
VDDIO_MEM_S3_40
VDDIO_MEM_S3_41
VDDIO_MEM_S3_42
VDDIO_MEM_S3_43
VDDIO_MEM_S3_44
VDDIO_MEM_S3_45
VDDIO_MEM_S3_46
VDDIO_MEM_S3_47
VDDIO_MEM_S3_48
VDDIO_MEM_S3_49
VDDIO_MEM_S3_50
VDDIO_MEM_S3_51
VDDIO_MEM_S3_52
VDDIO_MEM_S3_53
VDDIO_MEM_S3_54
VDDIO_MEM_S3_55
VDDIO_MEM_S3_56
VDDIO_MEM_S3_57
VDDIO_MEM_S3_58
VDDIO_MEM_S3_59
VDDIO_MEM_S3_60
VDDIO_MEM_S3_61
VDDIO_MEM_S3_62
VDDIO_MEM_S3_63
VDDIO_MEM_S3_64
VDDIO_MEM_S3_65
VDDIO_MEM_S3_66
VDDIO_MEM_S3_67
VDDIO_MEM_S3_68
VDDIO_MEM_S3_69
VDDIO_MEM_S3_70
VDDIO_MEM_S3_71
VDDIO_MEM_S3_72
VDDIO_MEM_S3_73
VDDIO_MEM_S3_74
VDDIO_MEM_S3_75
VDDIO_MEM_S3_76
VDDIO_MEM_S3_77
VDDIO_MEM_S3_78
VDDIO_MEM_S3_79
VDDIO_MEM_S3_80
VDDIO_MEM_S3_81
VDDIO_MEM_S3_82
VDDIO_MEM_S3_83
CPU_VDDP
8.5A
VDDP_0
VDDP_1
VDDP_2
VDDP_3
VDDP_4
VDDP_5
VDDP_6
VDDP_7
VDDP_8
VDDIO_AUDIO
C665
0.22u16X
C664
10u6.3X6
CPU_1P8_S5
0.25A
VDD_18_0
VDD_18_1
CPU_1P8
2A
VDD_33_0
VDD_33_1
VCC3
0.25A
VDDP_S5_0
VDDP_S5_1
CPU_VDDP_S5
1A
VDD_18_S5_0
VDD_18_S5_1
CPU_1P8_S5A
0.5A
VDD_33_S5_0
VDD_33_S5_1
3VSB
0.25A
VDDBT_RTC_G
C666
1u6.3X4
C662
0.22u16X
VDDBT_RTC_G
4.5uA
RSVD_0
RSVD_1
RSVD_2
RSVD_3
RSVD_4
RSVD_5
RSVD_6
RSVD_7
RSVD_8
RSVD_9
RSVD_10
RSVD_11
RSVD_12
RSVD_13
RSVD_14
RSVD_15
RSVD_16
RSVD_17
RSVD_18
RSVD_19
RSVD_20
RSVD_21
RSVD_22
RSVD_23
RSVD_24
RSVD_25
RSVD_26
RSVD_27
RSVD_28
RSVD_29
RSVD_30
RSVD_31
RSVD_32
RSVD_33
RSVD_34
RSVD_35
RSVD_36
RSVD_37
RSVD_38
RSVD_39
RSVD_40
RSVD_41
RSVD_42
RSVD_43
RSVD_44
RSVD_45
RSVD_46
AM4
PART 7 OF 9
ZIF-SOCKET1331
N12-331A040-F02
BOT CAVITY
TOP CAVITY
VCC3
C652
10u6.3X6
C656
0.22u16X
CPU_1P8_S5
L9
30L5A
CPU_1P8_S5A
C658
10u6.3X6
C659
0.22u16X
CPU_1P8
C654
22u6.3X6
C653
22u6.3X6
CPU_VDDP_S5
C655
10u6.3X6
C657
0.22u16X
CPU_VDDP
C660
10u6.3X6
C661
10u6.3X6
3VSB
C663
10u6.3X6
VCCP_NB
11
C617
22u6.3X6
C630
22u6.3X6
C618
22u6.3X6
C613
X_22u6.3X6
C619
22u6.3X6
C616
22u6.3X6
C629
22u6.3X6
C621
22u6.3X6
C615
X_22u6.3X6
C628
22u6.3X6
C620
22u6.3X6
C614
X_22u6.3X6
C611
X_180p50N4
C610
X_180p50N4
C612
180p50N4
C609
X_180p50N4
VCORE
13
C643
22u6.3X6
C649
22u6.3X6
C647
22u6.3X6
C633
X_22u6.3X6
C646
22u6.3X6
C642
22u6.3X6
C644
22u6.3X6
C634
X_22u6.3X6
C624
X_22u6.3X6
C640
22u6.3X6
C637
22u6.3X6
C636
X_22u6.3X6
C625
X_22u6.3X6
C639
22u6.3X6
C645
22u6.3X6
C635
X_22u6.3X6
C626
X_22u6.3X6
C638
22u6.3X6
C623
X_22u6.3X6
C648
22u6.3X6
C651
180p50N4
VCC_DDR
2
C622
0.22u16X
C632
180p50N4
C650
X_22u6.3X6
C641
X_22u6.3X6
C631
X_22u6.3X6
VCC_DDR
6
C134
22u6.3X6
C144
22u6.3X6
C149
22u6.3X6
C159
22u6.3X6
C161
22u6.3X6
C170
22u6.3X6
VCCP_NB
6
C139
22u6.3X6
C137
22u6.3X6
C141
22u6.3X6
C138
22u6.3X6
C142
22u6.3X6
C140
22u6.3X6
VCORE
12
C156
22u6.3X6
C157
22u6.3X6
C154
22u6.3X6
C162
22u6.3X6
C167
22u6.3X6
C166
22u6.3X6
C155
22u6.3X6
C152
22u6.3X6
C153
22u6.3X6
C165
22u6.3X6
C163
22u6.3X6
C164
22u6.3X6
MICRO-STAR INT'L CO.,LTD
MS-7C91
Size
Custom
Document Description
AM4 Power / VDDIO_AUDIO
Rev
10
Date: Tuesday, April 21, 2020
Sheet 8 of 78

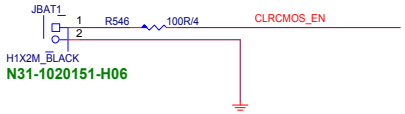


MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: AM4 GND
Rev: 10	
Date: Tuesday, April 21, 2020	Sheet 9 of 78

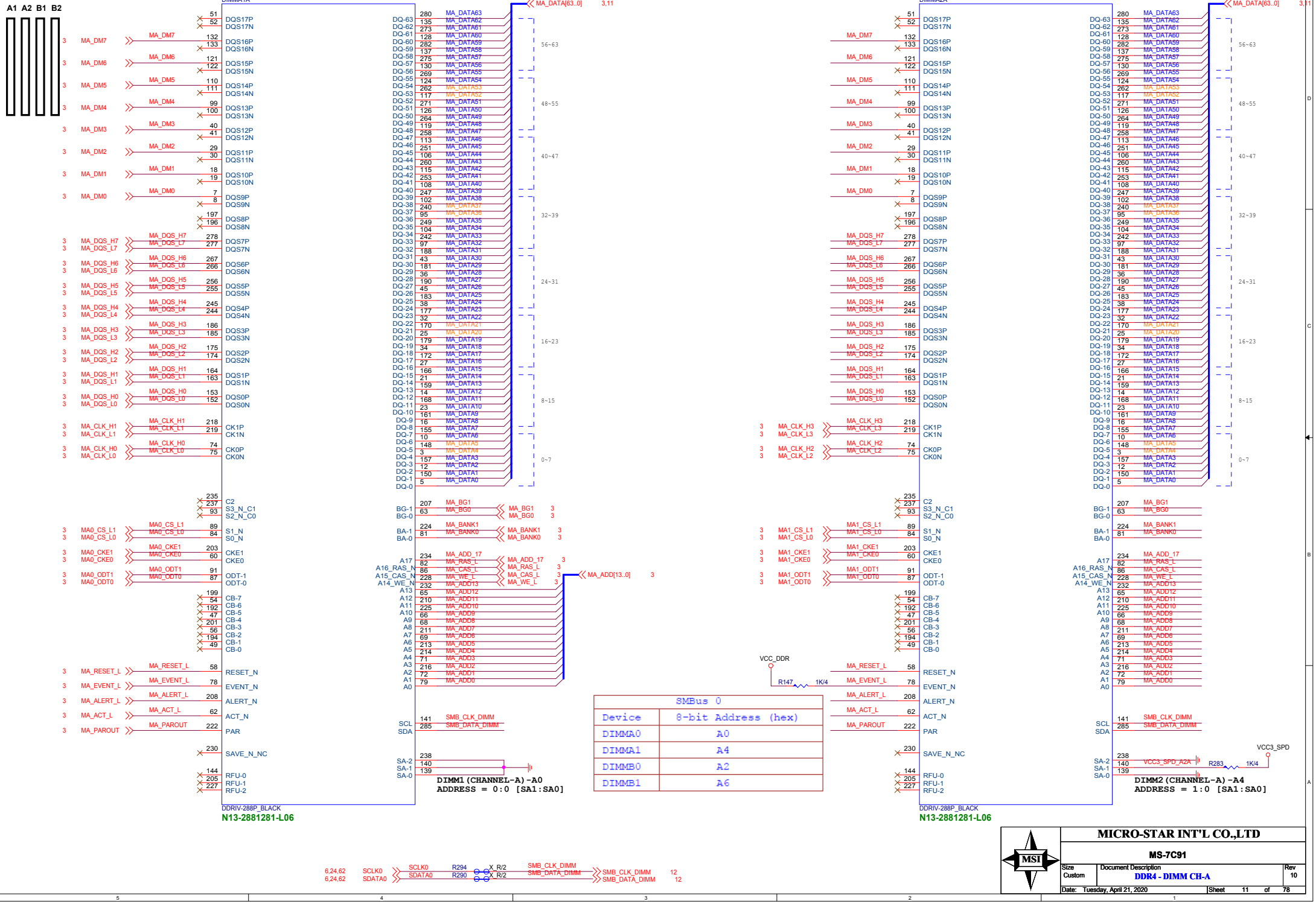
RTC & Clear CMOS Circuit



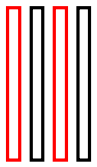
Clear CMOS button



MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: RTC / CMOS	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 10 of 78	



MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: DDR4 - DIMM CH-A
Rev: 10	
Date: Tuesday, April 21, 2020	Sheet 11 of 78



DIMMB1A

DIMM3(CHANNEL-B)-A2
ADDRESS = 0:1 [SA1:SA0]

DDRIV-288P_BLACK
N13-2881281-L06

DIMMB2A

DIMM4(CHANNEL-B)-A6
ADDRESS = 1:1 [SA1:SA0]

DDRIV-288P_BLACK
N13-2881281-L06

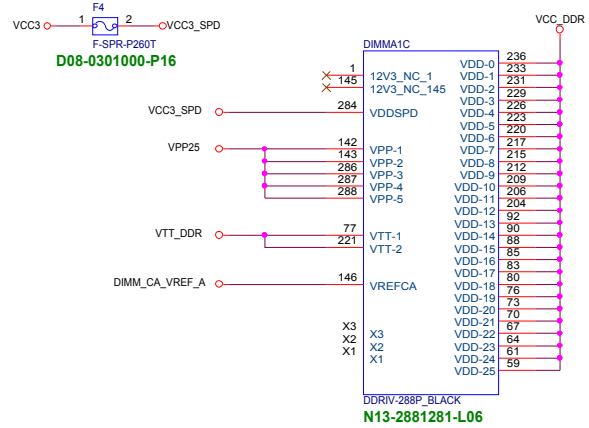
MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: DDR4 - DIMM CH-B
Rev: 10	
Date: Tuesday, April 21, 2020	Sheet 12 of 78

avl:D08-0301100-B07

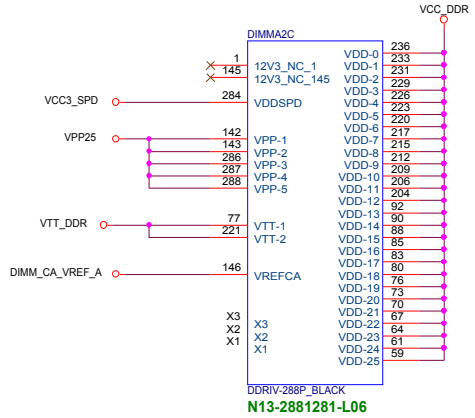
F4
VCC3 1 2 VCC3_SPD
F-SPR-P260T

D08-0301000-P16

DIMM SLOT PN BY SPEC



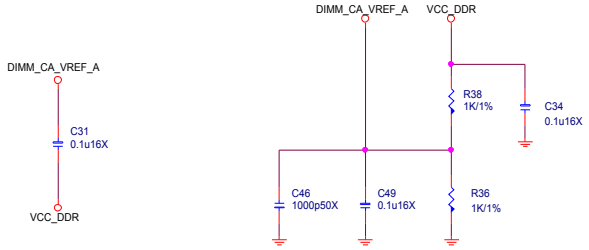
N13-2881281-L06

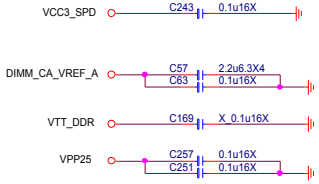


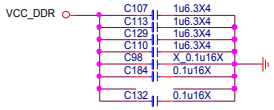
N13-2881281-L06

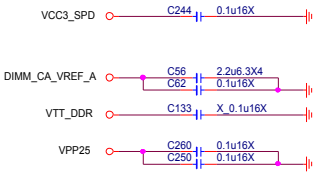
DDR VREF

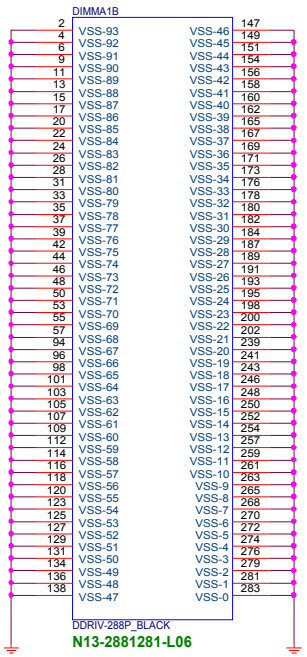
(place resistors close to DIMMs)



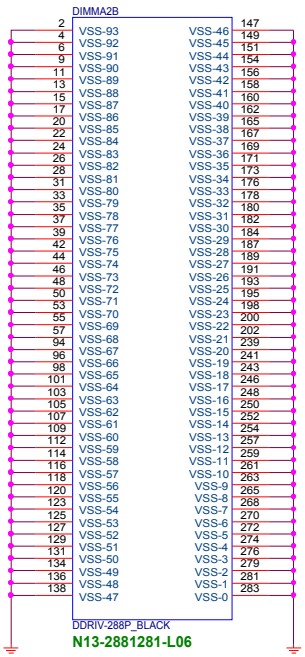








N13-2881281-L06



N13-2881281-L06

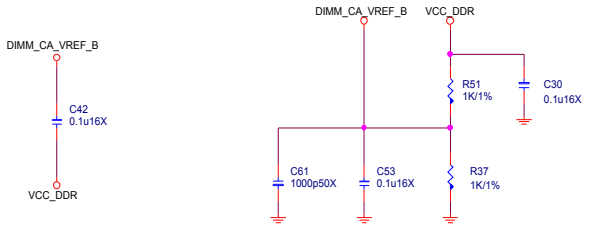
MICRO-STAR INT'L CO.,LTD

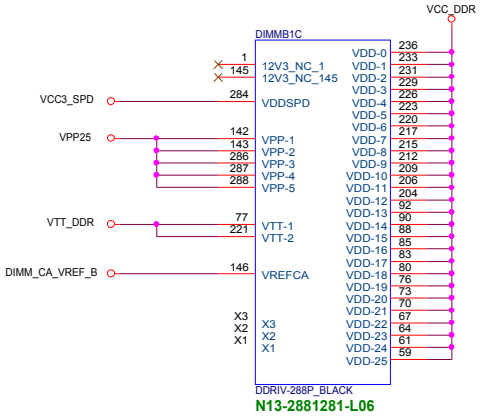
MS-7C91

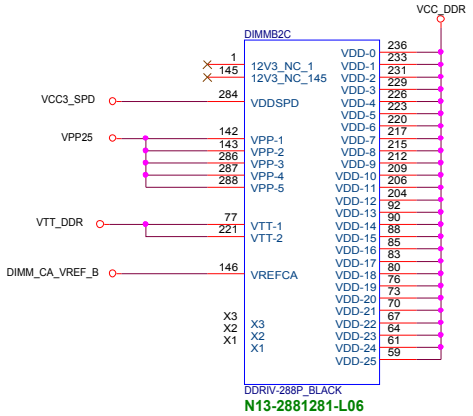
Size	Document Description	Rev
Custom	DDR4 - POWER/GND-1	10
Date: Tuesday, April 21, 2020	Sheet 13 of 78	

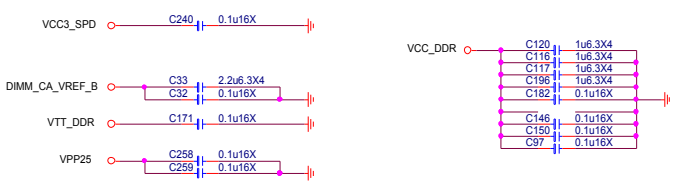
DDR VREF

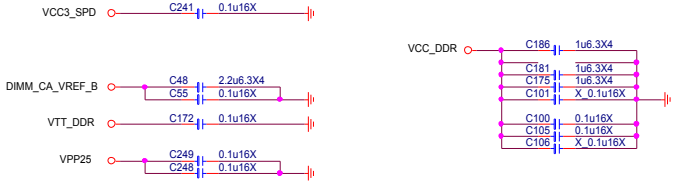
(place resistors close to DIMMs)

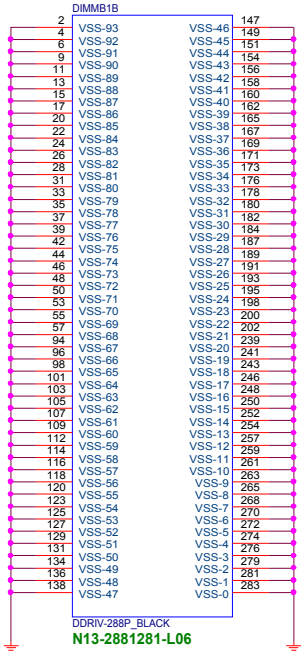


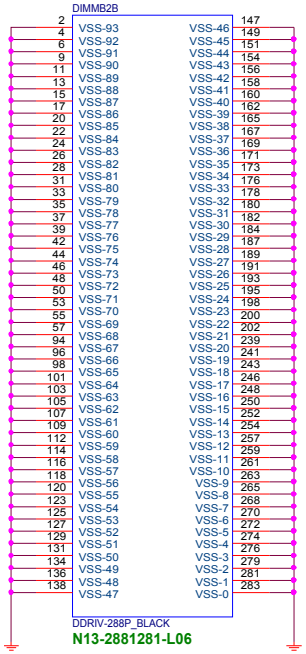










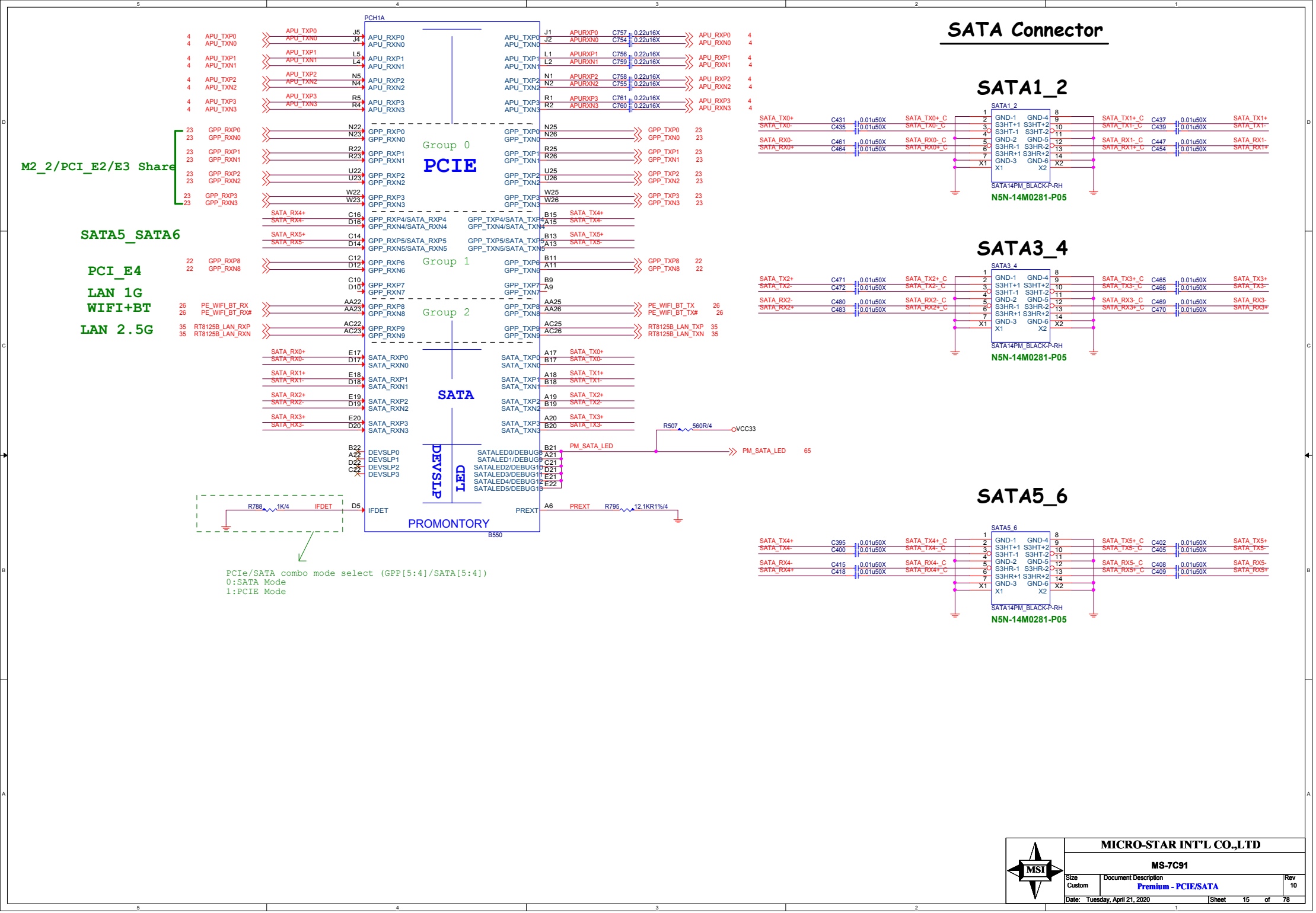


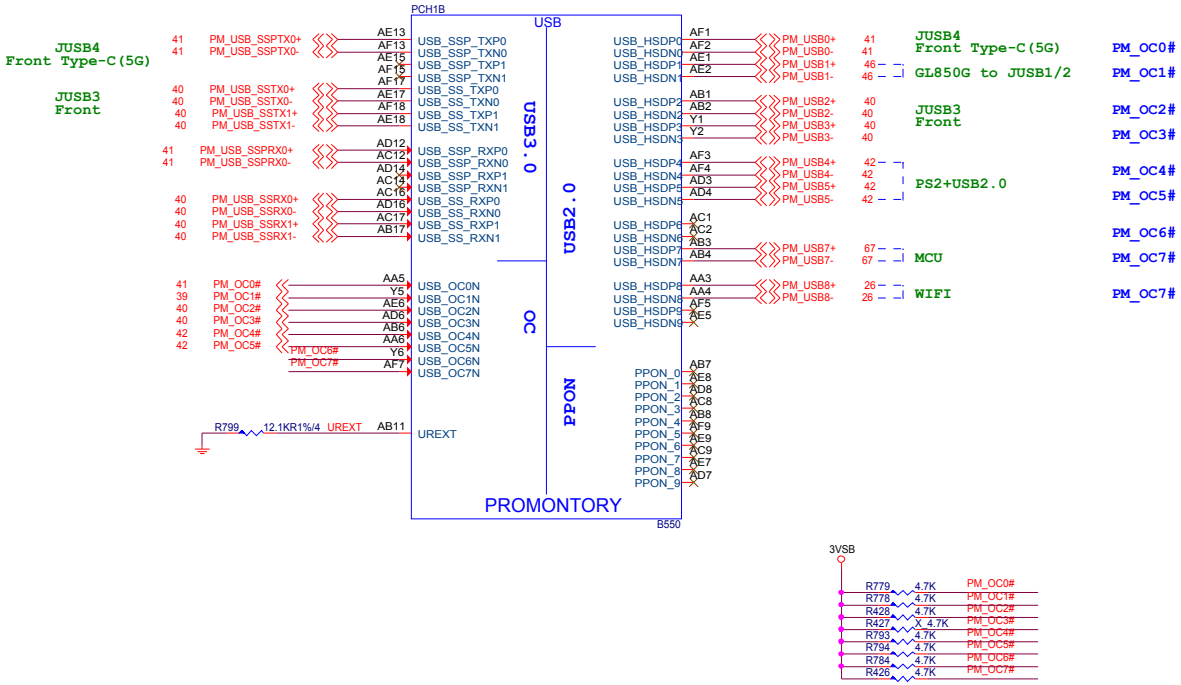
MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	DDR4 - POWER/GND-2	10

Date: Tuesday, April 21, 2020 Sheet 14 of 78


SATA Connector
SATA1_2
SATA3_4
SATA5_6
N5N-14M0281-P05
PCH1A
PROMONTORY
B550
M2_2/PCI_E2/E3 Share
SATA5_SATA6
PCI_E4
LAN 1G
WIFI+BT
LAN 2.5G
Group 0
Group 1
Group 2
PCIE
SATA
DEVSLP
LED
PCIe/SATA combo mode select (GPP[5:4]/SATA[5:4])
0:SATA Mode
1:PCIE Mode
MICRO-STAR INT'L CO.,LTD
MS-7C91
Premium - PCIE/SATA
Date: Tuesday, April 21, 2020
Sheet 15 of 78



USB mapping

USB_SSP_TX/RX[0] + USB_HSDP/N[0] + USB_OC0N
USB_SSP_TX/RX[1] + USB_HSDP/N[1] + USB_OC1N

USB_SS_TX/RX[0] + USB_HSDP/N[2] + USB_OC2N
USB_SS_TX/RX[1] + USB_HSDP/N[3] + USB_OC3N
USB_HSDP/N[4] + USB_OC4N
USB_HSDP/N[5] + USB_OC5N
USB_HSDP/N[6] + USB_OC6N
USB_HSDP/N[7] + USB_OC7N
USB_HSDP/N[8] + USB_OC7N
USB_HSDP/N[9] + USB_OC7N

MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: Premium - USB/OC
Rev: 10	
Date: Tuesday, April 21, 2020	Sheet 16 of 78

2020.03.25

VCC33
Q109 PM513BA
R3806 200KR/4
PM_GPIO_R7
bit2
R3807 1K/4
Q108 2N7002

VCC33
Q68 PM513BA
3VSB
R581 4.7K
R449 200KR/4
bit1
X4X1_EN#
PM_SPI_DATAOUT
23,27 X4_X1_EN#
Q71 2N7002
R448 1K/4
Q72 2N7002

GPP Group 0 (Lanes 3:0)
111: 1 PCIe x4
011: 1 PCIe x2 + 1 PCIe x2
010: 1 PCIe x2 + 2 PCIe x1
001: 2 PCIe x1 + 1 PCIe x2
000: 4 PCIe x1
Others: Reserved

VCC33
R526 10K CLKREQ0
R518 10K CLKREQ1
R803 10K CLKREQ2
R800 10K CLKREQ3
R791 10K CLKREQ4
R462 10K CLKREQ5
R509 10K CLKREQ6
R505 10K CLKREQ7
R801 10K CLKREQ8
R508 10K CLKREQ9

VCC33
R796 X_10K PM19_CLK_REQ_L

PCH1C
CLOCKS

7 APU_CLKP
7 APU_CLKN
6 PM19_CLK_REQ_L
M2_2 / PCI_E3 21,25 CLKREQ0
PCI_E2 22 CLKREQ2
PCI_E4 22 CLKREQ6
WIFI+BT 26 CLKREQ8
LAN 2.5G 35 CLKREQ9

APU_CLKP A7
APU_CLKN B7
PM19_CLK_REQ_L C7
APU_CLKREQN
CLKREQ0 AE20
CLKREQ1 AF20
CLKREQ2 AB19
CLKREQ3 AC19
CLKREQ4 D7
CLKREQ5 E8
CLKREQ6 AB18
CLKREQ7 AC18
CLKREQ8 AD19
CLKREQ9 AE19
GPP_CLKREQ0N
GPP_CLKREQ1N
GPP_CLKREQ2N
GPP_CLKREQ3N
GPP_CLKREQ4N/DEVSLP4
GPP_CLKREQ5N/DEVSLP5
GPP_CLKREQ6N/DEBUG16
GPP_CLKREQ7N/DEBUG17
GPP_CLKREQ8N/DEBUG18
GPP_CLKREQ9N/DEBUG19

GPP_CLKP0 L26
GPP_CLKN0 L25
GPP_CLKP1 K26
GPP_CLKN1 K25
GPP_CLKP2 H26
GPP_CLKN2 H25
GPP_CLKP3 G26
GPP_CLKN3 G25
GPP_CLKP4 L24
GPP_CLKN4 L23
GPP_CLKP5 K24
GPP_CLKN5 K23
GPP_CLKP6 H24
GPP_CLKN6 H23
GPP_CLKP7 G24
GPP_CLKN7 G23
GPP_CLKP8 E26
GPP_CLKN8 E25
GPP_CLKP9 E24
GPP_CLKN9 E23

M22_PE3_CLK0P 21
M22_PE3_CLK0N 21
M2_2 / PCI_E3
PE_SLOT_CLK2P 22
PE_SLOT_CLK2N 22
PCI_E2
PE_SLOT_CLK6P 22
PE_SLOT_CLK6N 22
PCI_E4
WIFI_BT_CLK8P 26
WIFI_BT_CLK8N 26
WIFI+BT
RT8125B_LAN_CLK9P 35
RT8125B_LAN_CLK9N 35
LAN 2.5G

PROMONTORY
B550

2020.03.31

C410 X_22p50N PM_X1_25_R
C416 X_22p50N PM_X2_25_R
Y4 25MHZ18p
R455 X_R/2
R463 X_1MR/4
R471 X_R/2
C414 10p50N
SATA_X1 AF11
SATA_X2 AE11

R430 X_0R/4
3VSB
0.1u16X C401
U41
NC7SZ08M5X
T70-7SZ0880-O05
6,7,20,24,26,35 PCIE_REST#
6 PM19_AUX_RST#
R429 X_R/2
PCIERST#_PROM

VCC33 VCC3
R412 X_10K
R3843 10K
2020.04.07
PM19_AUX_RST#
R403 X_10K

PCB_ID
VCC33
RZ1 1K/4
PCB_ID
RZ2 100K/4
E48(競華)(JH)會洗掉此區段

Strap Information
Vih = 2V Voh = 2.4V
Vil = 0.8V Vol = 0.4V

VCC33
R527 X_200KR/4 R517 1K/4 PM_TESTEN
TESTEN:
0:Function mode
1:Test mode

R534 X_200KR/4 R529 1K/4 PM_DBUGEN
Debug Enable:
0:Function mode
1:Debug mode

R516 200KR/4 R528 X_1K/4 PM_TCK
R804 200KR/4 R805 X_1K/4 PM_TDO
TCK (DEBUG_SEL1) / TDOTDO (DEBUG_SEL0):
00:Debug signal group 0 output
01:Debug signal group 1 output
10:Debug signal group 2 output
11:Debug signal group 3 output

R543 X_200KR/4 R556 1K/4 PM_GPIO_R15
GPP Group 2 (Lanes 9:8)
1: PCIe x2
0: 2 PCIe x1

bit0
R454 X_200KR/4 R457 1K/4 PM_SPI_DATAIN
bit1
R790 X_200KR/4 R789 1K/4 UART_TX
bit2
R554 X_200KR/4 R553 1K/4 PM_GPIO_R8
bit0
R441 200KR/4 R440 X_1K/4 PM_SPI_CLK_R

GPP Group 1 (Lanes 7:4)
111: 1 PCIe x4
011: 1 PCIe x2 + 1 PCIe x2
010: 1 PCIe x2 + 2 PCIe x1
001: 2 PCIe x1 + 1 PCIe x2
000: 4 PCIe x1
Others: Reserved

GPP Group 0 (Lanes 3:0)
111: 1 PCIe x4
011: 1 PCIe x2 + 1 PCIe x2
010: 1 PCIe x2 + 2 PCIe x1
001: 2 PCIe x1 + 1 PCIe x2
000: 4 PCIe x1
Others: Reserved

bit2
R568 200KR/4 R567 X_1K/4 PM_GPIO_R7
R533 200KR/4 R532 X_1K/4 PM_GPIO_R4
GPIO_R4:
1: GPP / Clock buffer clock source from APU CLKP/N
0: GPP / Clock buffer clock source from Crystal

R540 X_200KR/4 R541 1K/4 PM_GPIO_R5
GPIO_R5:
0:USBC SSC Enable
1:USBC SSC Disable

R559 200KR/4 R558 X_1K/4 PM_GPIO_R6
GPIO_R6:
0:SATA SSC Enable
1:SATA SSC Disable

PCH1D
PROMONTORY
B550

57,60 PM_PWRGD CP20 X_SP PWR_GD AD20
PCIERST#_PROM AC5
PGG_INIT AF21
VCC33
R785 X_4.7K
R525 4.7K
AE21 AD21
R798 4.7K PM_SCLK C8
R797 4.7K PM_SDATA D8
R792 10K UART_RX C6 UART_TX D6
PM_SPI_CLK_R A3
PM_SPI_DATAIN A5
PM_SPI_DATAOUT B5
B4
TP12 PM_TCK A23 PM_TDI A24
TP13 PM_TDO C24 PM_TMS B24
TP38 PM_RTCK C23
PM_TESTEN AB21
PM_DBUGEN AF22
R802 X_0R/4 EFUSE_PWR AB20

PWR_GD
PERSTN
GPP_INTN
FAN_CTRL/DEBUG21
TACH_IN/DEBUG20
SMCL
SMDA
UART_RX
UART_TX
SPI_SCK
SPI_CS
SPI_SDI
SPI_SDO
TCK
TDI
TDO
TMS
RTCK
TESTEN
DEBUG_ENABLE
EFUSE_PWR

ACPI
FAN
SMBus
SPI
GPIO
MISC

PEWAKEN AB5 PEWAKEN CP19 X_SP APU_WAKE# 6,24
GPP_RSTN AC11 PM_GPP_RST C421 X_100p50N PM_GPP_RST 21
SMI C5 APU_SMI
INT_GPIO/DEBUG6 A25 PM_INI

GPIO_R0/DEBUG0 A1 PM_GPIO_R0
GPIO_R1/DEBUG1 C2 PM_GPIO_R1 TP10
GPIO_R2/DEBUG2 B2 PM_GPIO_R2 TP8
GPIO_R3/DEBUG3 A2 PM_GPIO_R3 TP9
GPIO_R4/DEBUG22 A26 PM_GPIO_R4 TP11
GPIO_R5/DEBUG23 B26 PM_GPIO_R5
GPIO_R6/DEBUG24 C26 PM_GPIO_R6
GPIO_R7/DEBUG25 D26 PM_GPIO_R7
GPIO_R8/DEBUG26 C25 PM_GPIO_R8
GPIO_R9/DEBUG27 D25 PM_GPIO_R9
GPIO_R10/DEBUG28 D23 PM_GPIO_R10
GPIO_R11/DEBUG29 AF26 PM_GPIO_R11 TP41
GPIO_R12/DEBUG30 AE26 PM_GPIO_R12
GPIO_R13/DEBUG31 AF25 PM_GPIO_R13 TP15
GPIO_R14/DEBUG7 AE25 PM_GPIO_R14 TP14
GPIO_R15/DEBUG5 AF24 PM_GPIO_R15 TP17
GPIO_R16/DEBUG4 AE24 PM_GPIO_R16
GPIO_R17/DEBUG14 AE23 PM_GPIO_R17 TP16
GPIO_R18/DEBUG15 AE22 PM_GPIO_R18 TP39 TP40

GPIO0 C1 MCU_RST
GPIO1 B1 PCB_ID
GPIO2 D1
GPIO3 D2
GPIO4 D3
GPIO5 D4
GPIO6 C3
GPIO7 C4
MCU_RST 67 For SW RESET MCU
For BOM Option
Board ID

Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.

Follow CRB
APU_SMI
PM_INI
CP16 X_SP
R445 X_0R/4
VCC33 3VSB
R420 4.7K
Q46 2N7002
APU_LPC_PME# APU_LPC_PME# 6,27

Reserved Board ID
VCC33
R782 1K/4 GPIO5 R783 X_200KR/4
R437 X_1K/4 GPIO6 R438 200KR/4
R786 X_1K/4 GPIO7 R787 200KR/4
R561 X_1K/4 PM_GPIO_R9 R562 200KR/4
R555 X_1K/4 PM_GPIO_R11 R542 X_200KR/4

GPIO_R[13:4]
Internal have a PU 200Kohm

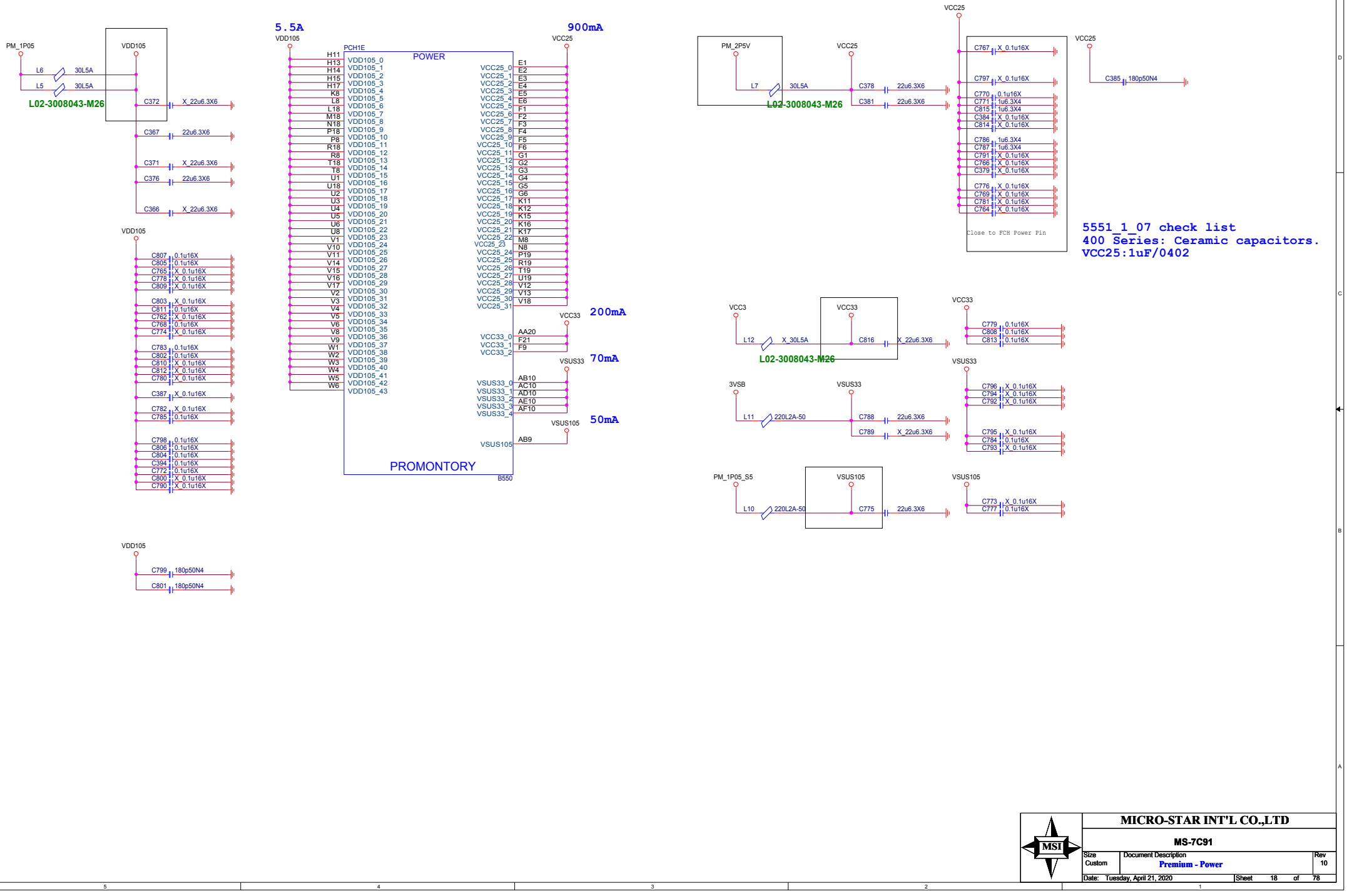
UART_TX/SPI_SDI/SPI_SDO/SPI_SCK/TCK/TDO
Internal have a PU 200Kohm

PM_DBUGEN
Internal have a PD 1Kohm

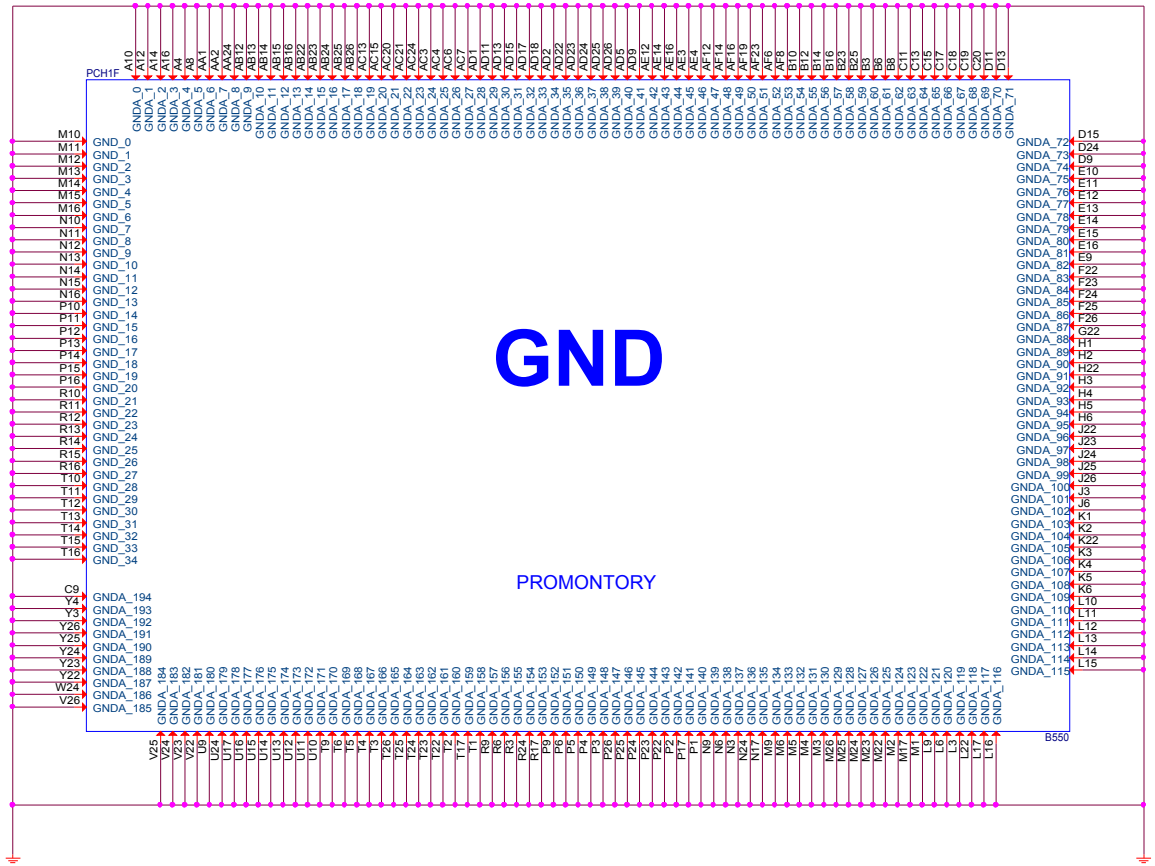
BOM OPTION
VCC33
R422 X_10K GPIO2 R414 10K
R421 X_10K GPIO3 R413 10K
R781 X_10K GPIO4 R780 10K

	XXX	XXX	
GPIO2	0	0	
GPIO3	0	0	
GPIO4	0	0	

MICRO-STAR INT'L CO.,LTD
MS-7C91
Size: Custom
Document Description: Premium - CLK/ACPI/GPIO
Rev: 10
Date: Tuesday, April 21, 2020
Sheet 17 of 78

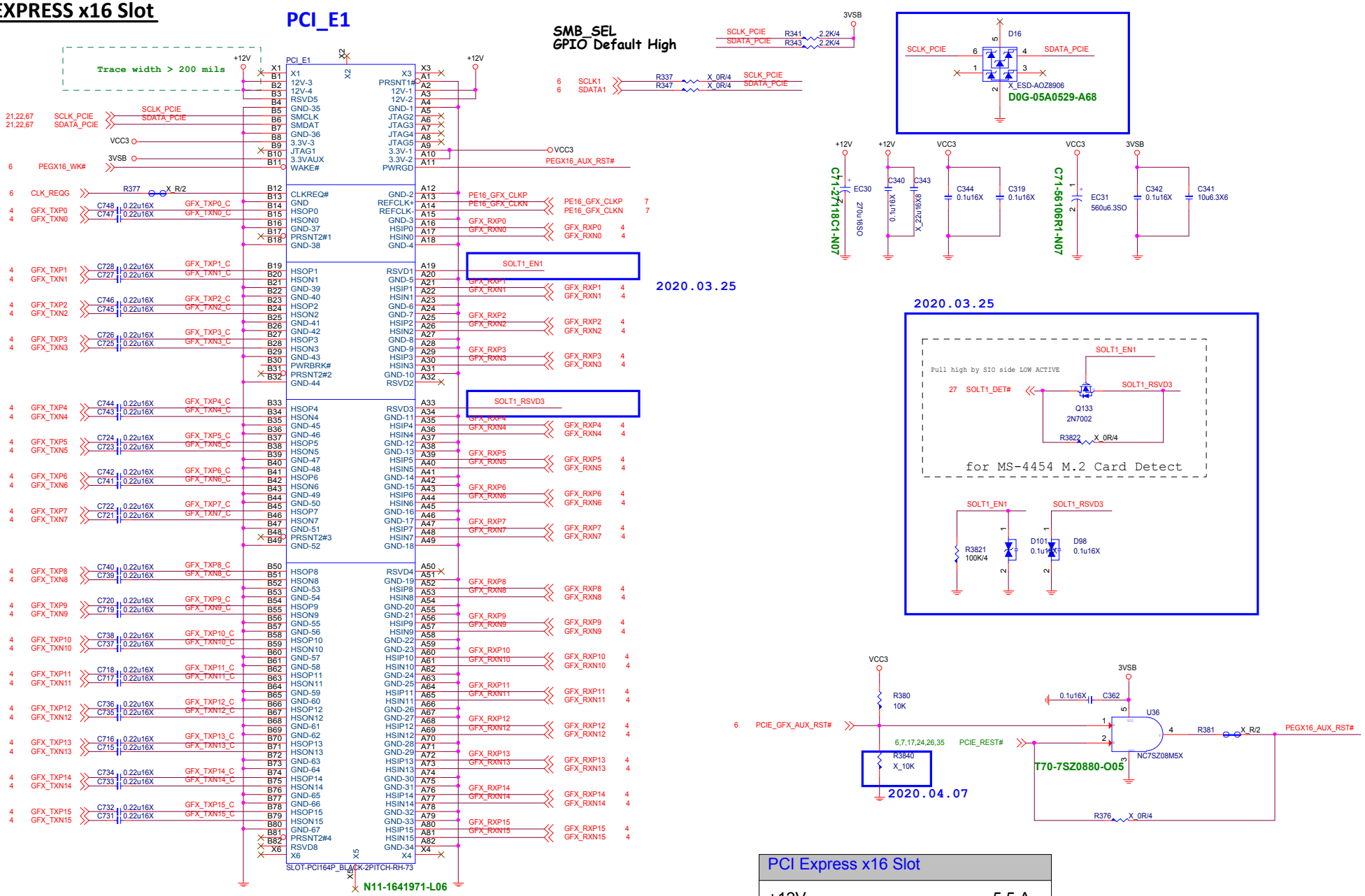


MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: Premium - Power	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 18 of 78	



MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: Premium - GND
Rev: 10	
Date: Tuesday, April 21, 2020	Sheet 19 of 78

PCI EXPRESS x16 Slot

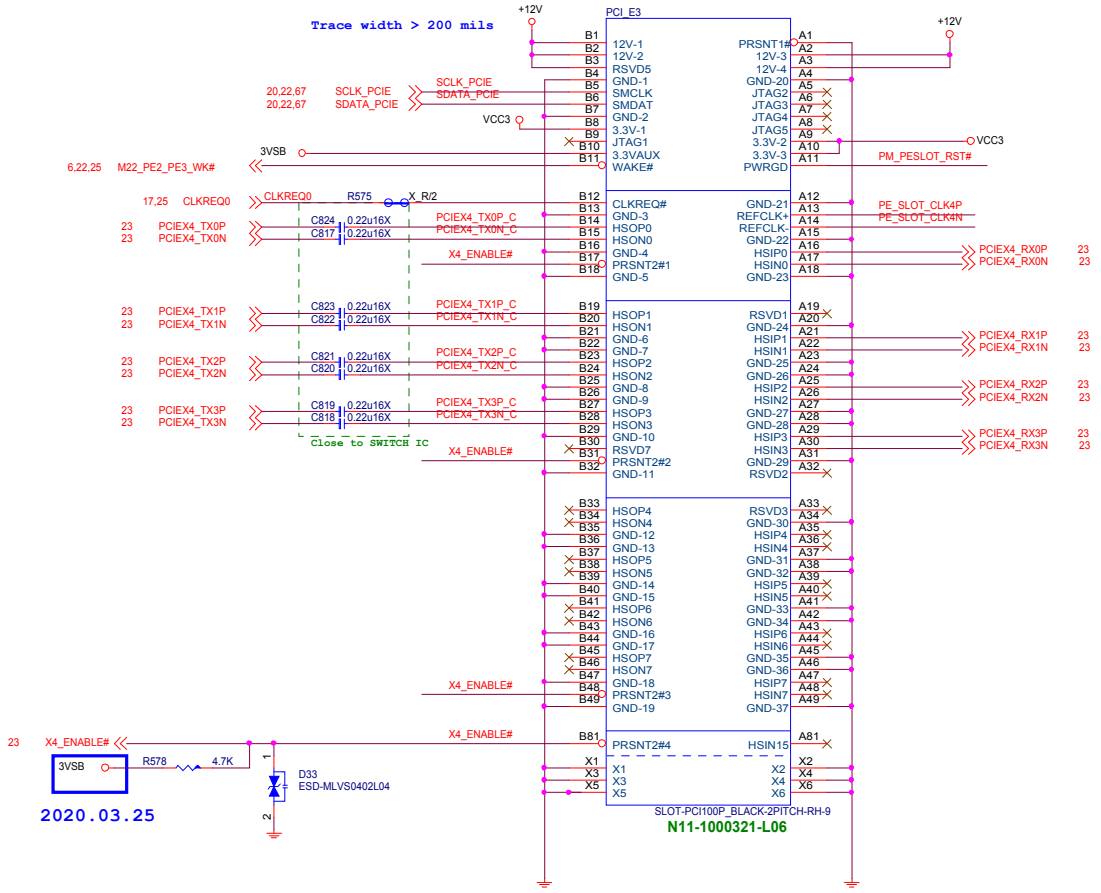


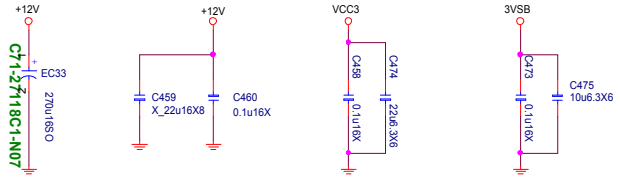
PCI Express x16 Slot		
+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

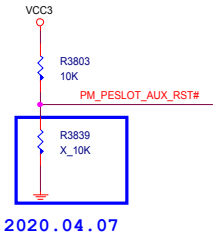
MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: PCI_E2 (X16)
Rev: 10	
Date: Tuesday, April 21, 2020	Sheet 20 of 78

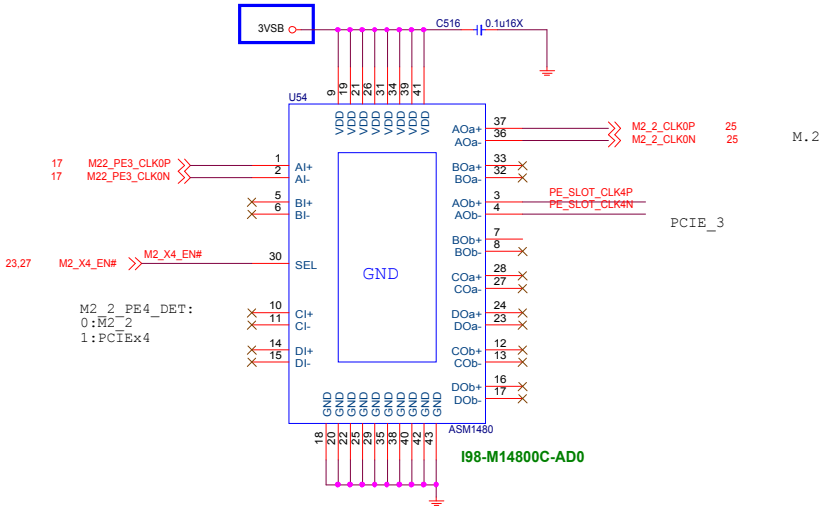
PCI EXPRESS x4 SLOT

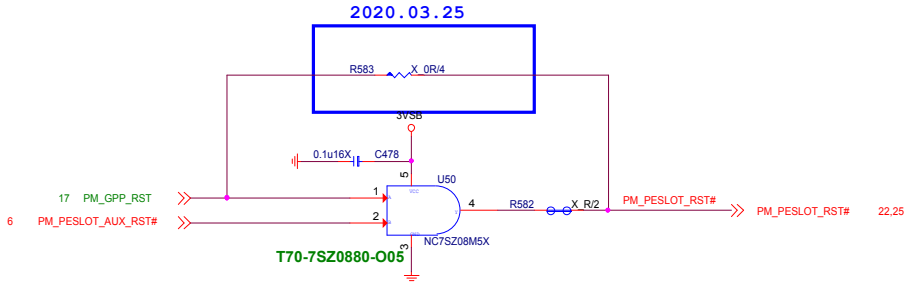
PCI_E3 X4











PCI Express x4 Slot		
+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

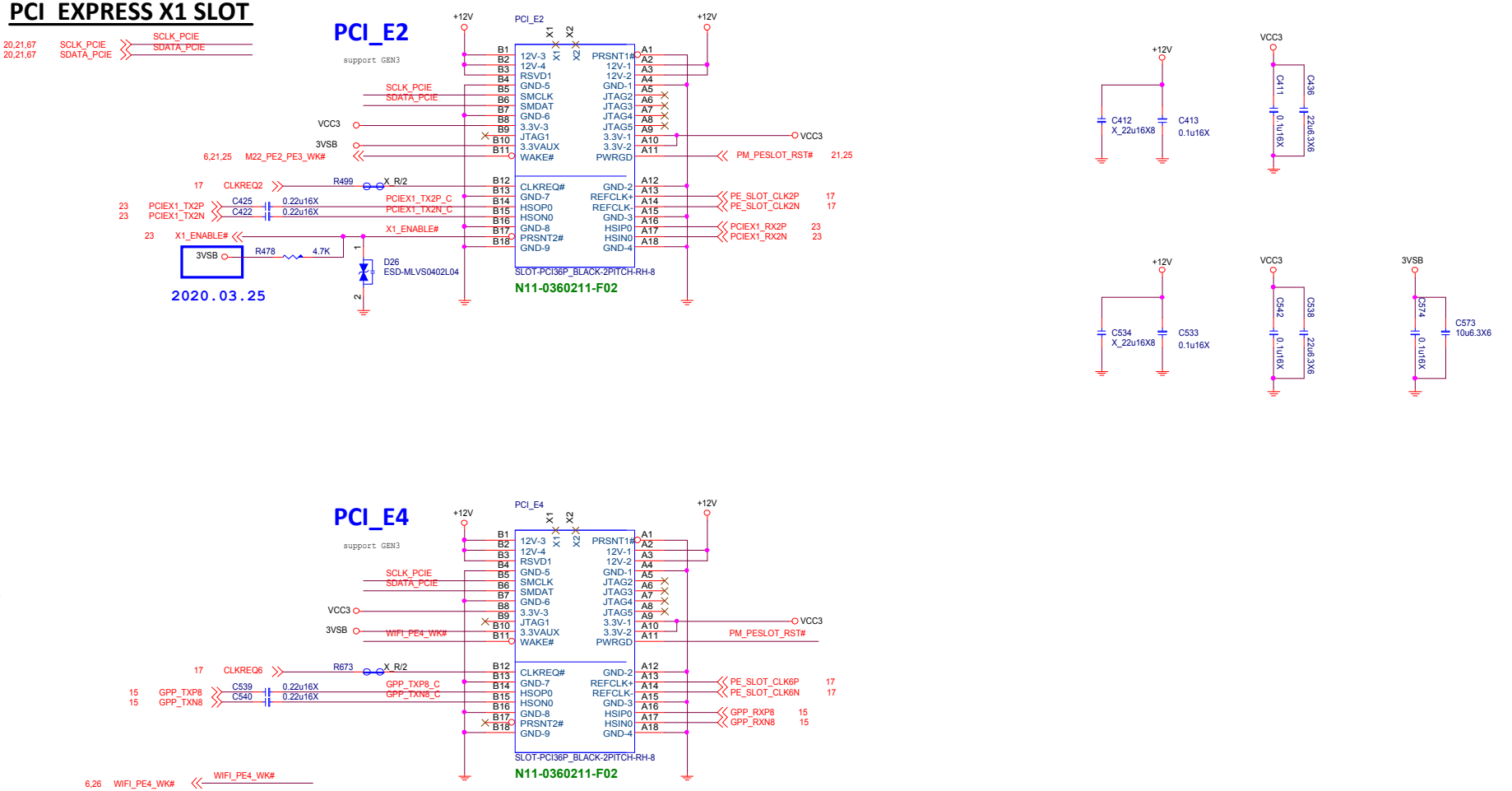
MICRO-STAR INT'L CO.,LTD

MS-7C91

Size: Custom | Document Description: PCI_E3 (X4) | Rev: 10

Date: Tuesday, April 21, 2020 | Sheet 21 of 78

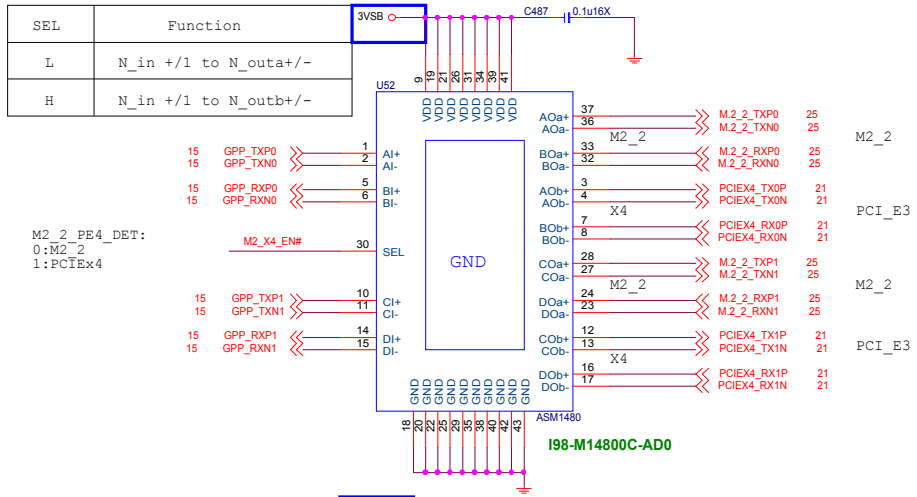
PCI_EXPRESS X1 SLOT

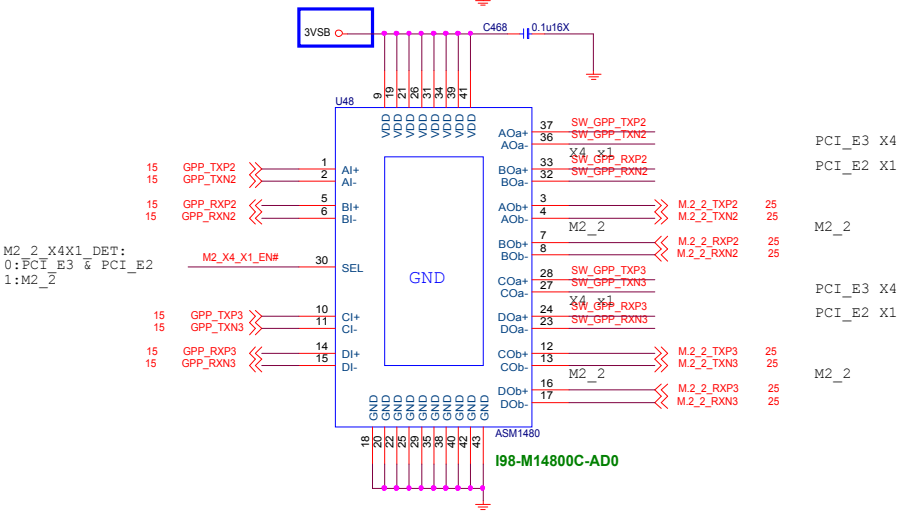


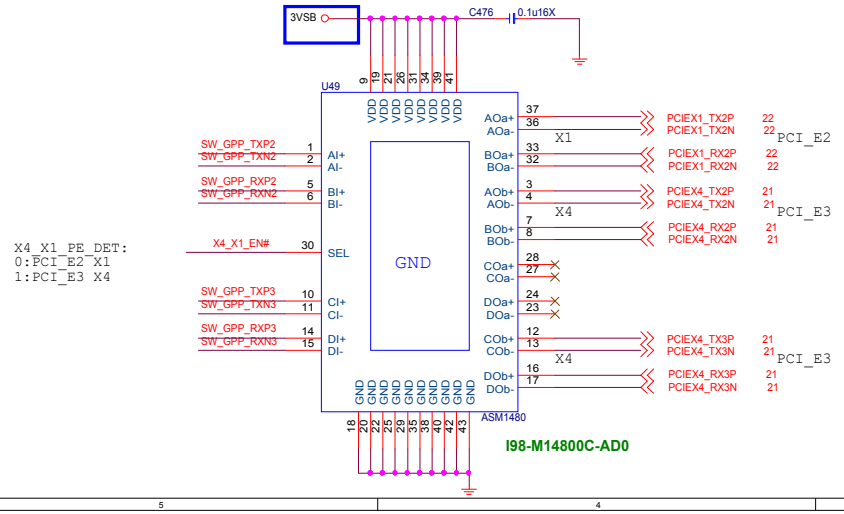
PCI Express x1 Slot *3		
+12V		- 1.5 A
+VCC3		- 9A
+3V3_S5	(wake)	- 1.125A
+3V3_S5	(no wake)	- 20mA

MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: PCI_E2/E4_X1	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 22 of 78	

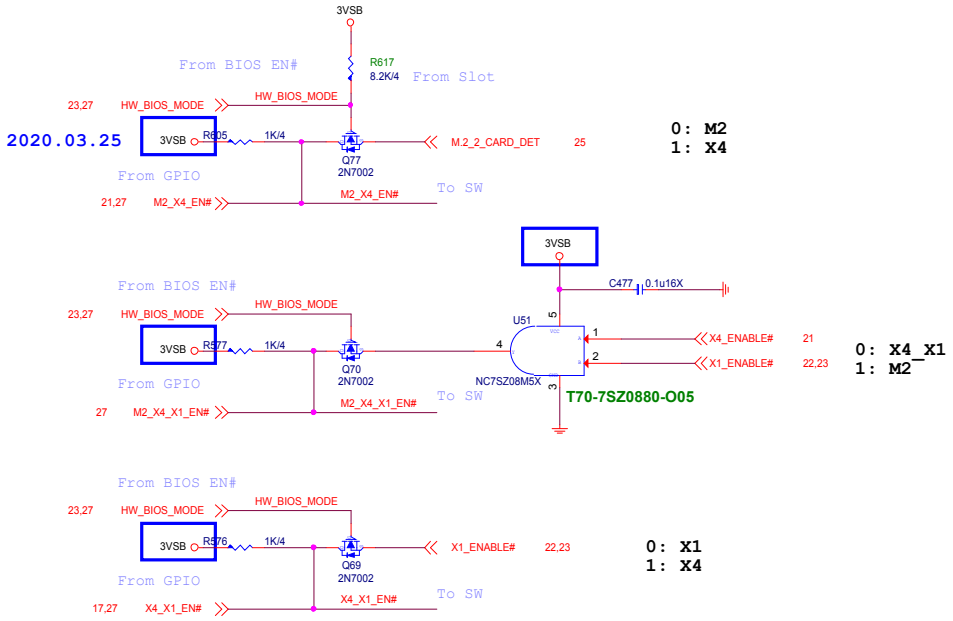
SEL	Function
L	N_in +/1 to N_outa+/-
H	N_in +/1 to N_outb+/-







PCIE Lanes control circuit



HW_BIOS_MODE = High(HW MODE)

DEVICE	M2_2 X4	●(4)	X	X	●(2)	●(2)	X	X	●(2)
	PCI_E3 X4	X	●(4)	X	●(0)	X	●(2)	X	●(0)
	PCI_E2 X1	X	X	●(1)	X	●(1)	●(1)	X	●(1)
DETECT	M.2_2_CARD_DET	0	1	1	0	0	1	1	0
	X1_ENABLE#	1	1	0	1	0	0	1	0
	X4_ENABLE#	1	0	1	0	1	0	1	0

●(X) = availability Lanes number

HW_BIOS_MODE = Low(BIOS MODE)

BIOS GPIO SWITCH	M2_X4_EN#	0	0	0	0	1	1	1	1
	M2_X4_X1_EN#	0	0	1	1	0	0	1	1
	X4_X1_EN#	0	1	0	1	0	1	0	1
DEVICE	M2_2 X4	●(2)	●(2)	●(4)	●(4)	●(0)	●(0)	●(0)	●(0)
	PCI_E3 X4	●(0)	●(0)	●(0)	●(0)	●(2)	●(4)	●(2)	●(2)
	PCI_E2 X1	●(1)	●(0)	●(0)	●(0)	●(1)	●(0)	●(0)	●(0)

MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	PCIE GEN3 SWITCH	10

Date: Tuesday, April 21, 2020 Sheet 23 of 78

M.2_1 Connector

VCC3 4.25A
Max: 14W

M2下方零件擺放限高要小於0.9mm的零件

2020.03.25

LANE REVERSE TO SUPPORT SATA SSD

Close to PIN2,4

Close to PIN12, 14, 16, 18

Close to PIN70, 72, 74

PIN 69
Low SATA
NC PCIE

M.2_CARD_DET:
0:Have M.2
1:No M.2

KEY M

SLOT-NGFFCARD67P_BLACK-HF-88

PCIE/SATA Mode

PLN#

2020.03.25

2020.04.07

2020.03.25 SMBUS Level Shift IC

2020.04.16

pull high ESIO SIDE

CPU Side pull high 4.7K

close to U81

close to CPU SIDE

RECESS1
SCREW
E2B-7984020-A89
CROSS RECESS

H1 H2 H3 H4
<HP-BOM>
E2B-7B05010

Footprint: H_R240D173_BR189_PT

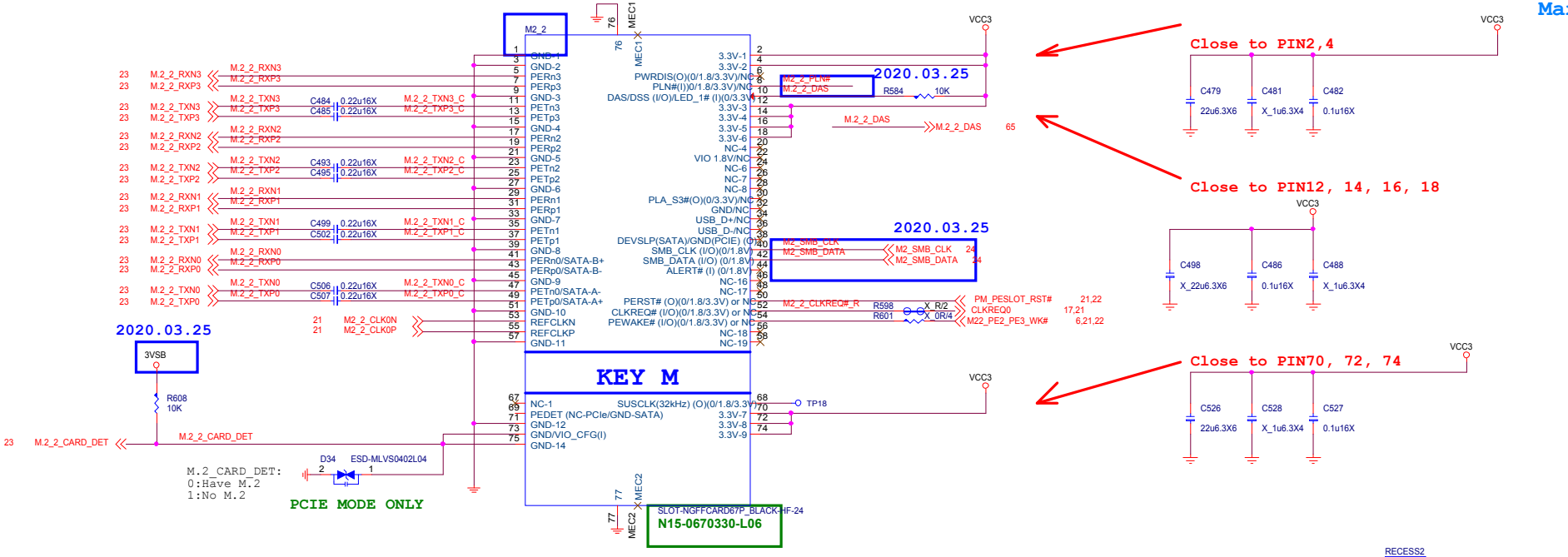
E2B-7B05010-A89

MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: M2_1 PCIE/SATA Mode(KEY_M)
Date: Tuesday, April 21, 2020	Sheet 24 of 78
	Rev 10

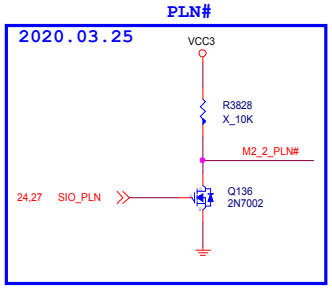
M.2_2 Connector

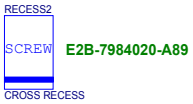
M2下方零件擺放限高要小於0.9mm的零件

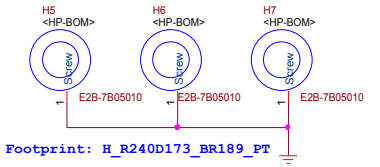
VCC3 4.25A
Max: 14W



M2_2 use have four-hole footprint
V0A/1.0 BOM : N15-0670330-L06
V2.0 BOM : N15-0671160-F02







MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: M2_2 PCIE Mode(KEY_M)	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 25 of 78	

EMI

NEAR CONNECTOR

U19 ESD-AOZ8906

PM_USB8+ 16

PM_USB8- 16

3VSB C667 X_0.1u16X

ATX_5VSB R745 47K/4

3VSB R744 47K/4

Q102 2N7002D

27 WIFI_BTDIS# WIFI_BTDIS# G2 D1 G1 S2 S1 D2 BT_DISABLE_L#

ATX_5VSB R746 47K/4

Q103 2N7002D

WIFI_BTDIS# G2 D1 G1 S2 S1 D2 WIFI_DISABLE_L#

780mA

3VSB C194 1u6.3X4 C191 10u6.3X6 C190 0.01u50X

M2_WIFI1 MEC2

	1 GND-1	2	3.3V-1
PM_USB8+	3 USB_D+	4	3.3V-2
PM_USB8-	5 USB_D-	6	LED1#
	7 GND-11	8	PCM_CLK / I2S SCK
	9 SDIO CLK	10	PCM_SYNC / I2S WS
	11 SDIO CMD	12	PCM_IN / I2S SD_IN
	13 SDIO DATA0	14	PCM_OUT / I2S SD_OUT
	15 SDIO DATA1	16	LED2#
	17 SDIO DATA2	18	GND-2
	19 SDIO DATA3	20	UART WAKE#
	21 SDIO WAKE#	22	UART RXD
	23 SDIO RESET#		

KEY E

	33 GND-10	32	UART TXD
15 PE_WIFI_BT_TX	0.22u16X C205 PE_WIFI_BT_TXC 35 PETp0	34	UART CTS
15 PE_WIFI_BT_TX#	0.22u16X C206 PE_WIFI_BT_TX#C 37 PETn0	36	UART RTS
	39 GND-9	38	VENDOR DEFINED-1
15 PE_WIFI_BT_RX	41 PERp0	40	VENDOR DEFINED-2
15 PE_WIFI_BT_RX#	43 PERn0	42	VENDOR DEFINED-3
	45 GND-8	44	COEX3
17 WIFI_BT_CLK8P	47 REFCLKP0	46	COEX2
17 WIFI_BT_CLK8N	49 REFCLKN0	48	COEX1
	51 GND-7	50	SUSCLK WIFI_BT_RTCCLK_R R167 X_0R/4 WIFI_BT_RTCCLK 6
17 CLKREQ8 R192 X_R/2 CLKREQ8_R	53 CLKREQ0#	52	PERST0# WIFI_RST#
6,22 WIFI_PE4_WK# D20 S-LRB520S WIFI_LAN_WAKE#	55 PEWAKE0#	54	W_DISABLE2# BT_DISABLE_L# R722 3.3KR/4 3VSB
23,35 SIO_LAN_WAKE# D19 S-LRB520S	57 GND-6	56	W_DISABLE1# WIFI_DISABLE_L# R723 3.3KR/4
	59 RESERVED / PETp1	58	I2C DATA
3VSB R375 10K WIFI_LAN_WAKE#	61 RESERVED / PETn1	60	I2C CLK
	63 GND-5	62	ALERT#
	65 RESERVED / PERp1	64	RESERVED
	67 RESERVED / PERn1	66	UIM_SWP / PERST1#
	69 GND-4	68	UIM_POWER_SNK / CLKREQ1#
	71 RESERVED / REFCLKP1	70	UIM_POWER_SRC/GPIO1 / PEWAKE1#
	73 RESERVED / REFCLKN1	72	3.3V-3 3VSB
	75 GND-3	74	3.3V-4 C192 0.01u50X C195 1u6.3X4 C193 10u6.3X6

MEC1 SLOT-NGFFCARD67P_BLACK-HF-46

N15-0670610-L06

10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V3V pins 2 and 4.
10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V3V pins 70 and 72.

VCC3 R3844 X_10K R357 10K 3VSB 0.1u16X C321

6 WIFI_AUX_RST# 6,7,17,20,24,35 PCIE_REST# U33 NC7SZ08M5X R349 33R/4 WIFI_RST#

R348 X_0R/4

T70-7SZ0880-O05

COVER1 VR Cover X1 X2 X_604-4467-XXX

604-4467-XXX

SCREW1 SCREW 鎖WiFi Module螺絲

SCREW2 SCREW 鎖WiFi Module螺絲

E43-1204046-P65 E43-1204046-P65

Wireless1 INTEL-AX200 MS-4467 Wireless

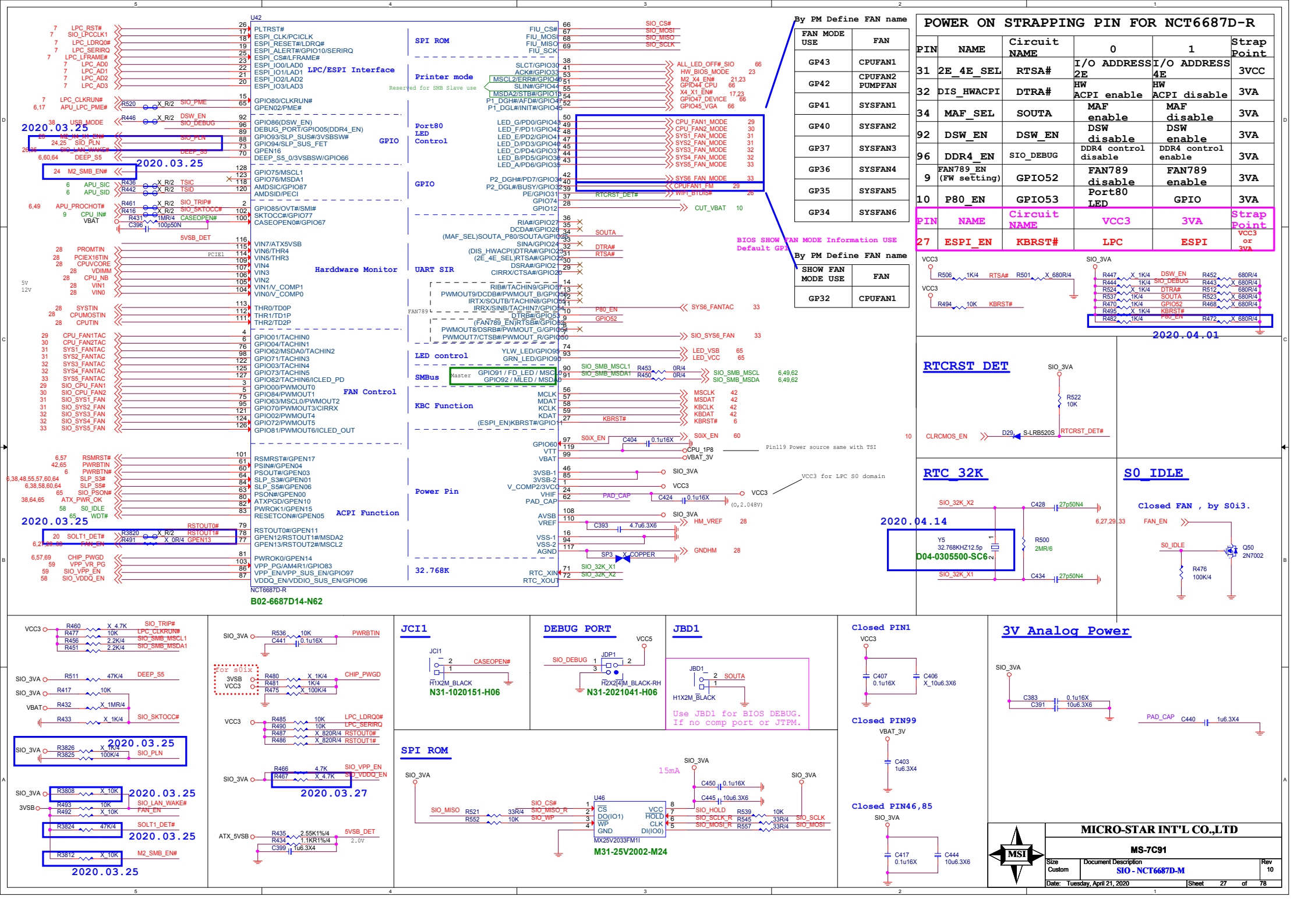
604-4467-020

MICRO-STAR INT'L CO.,LTD

MS-7C91

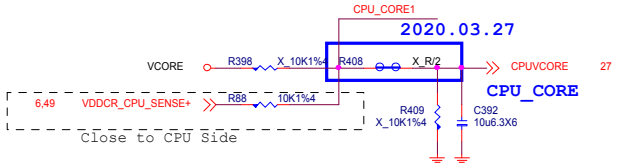
Size	Document Description	Rev
Custom	M2_2 - WIFI+BT	10

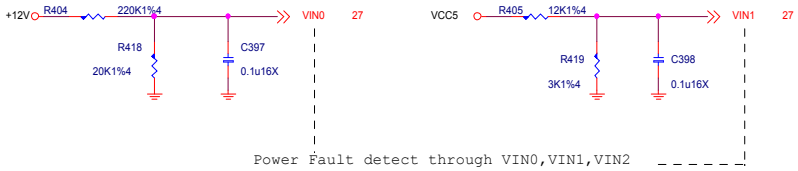
Date: Tuesday, April 21, 2020 Sheet 26 of 78

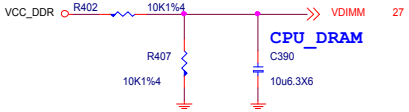

U42
NCT6687D-R
B02-6687D14-N62
LPC/ESPI Interface
SPI ROM
Printer mode
Reserved for SMB Slave use
Port80 LED Control
GPIO
UART SIR
Harddware Monitor
FAN Control
LED control
SMBus
KBC Function
Power Pin
ACPI Function
32.768K
FAN789
2020.03.25
2020.04.01
2020.04.14
2020.03.27
By PM Define FAN name
FAN MODE USE
FAN
GP43 CPUFAN1
GP42 CPUFAN2 PUMPFAN
GP41 SYSFAN1
GP40 SYSFAN2
GP37 SYSFAN3
GP36 SYSFAN4
GP35 SYSFAN5
GP34 SYSFAN6
By PM Define FAN name
SHOW FAN MODE USE
FAN
GP32 CPUFAN1
BIOS SHOW FAN MODE Information USE Default GPI
POWER ON STRAPPING PIN FOR NCT6687D-R
PIN | NAME | Circuit NAME | 0 | 1 | Strap Point
31 | 2E_4E_SEL | RTSA# | I/O ADDRESS 2E | I/O ADDRESS 4E | 3VCC
32 | DIS_HWACPI | DTRA# | HW ACPI enable | HW ACPI disable | 3VA
34 | MAF_SEL | SOUTA | MAF enable | MAF disable | 3VA
92 | DSW_EN | DSW_EN | DSW disable | DSW enable | 3VA
96 | DDR4_EN | SIO_DEBUG | DDR4 control disable | DDR4 control enable | 3VA
9 | FAN789_EN (FW setting) | GPIO52 | FAN789 disable | FAN789 enable | 3VA
10 | P80_EN | GPIO53 | Port80 LED | GPIO | 3VA
PIN | NAME | Circuit NAME | VCC3 | 3VA | Strap Point
27 | ESPI_EN | KBRST# | LPC | ESPI | VCC3 or 3VA
RTCRST_DET
RTC_32K
S0_IDLE
Closed FAN , by S0i3.
Pin119 Power source same with TSI
VCC3 for LPC S0 domain
JCI1
DEBUG PORT
JBD1
Use JBD1 for BIOS DEBUG. If no comp port or JTPM.
N31-1020151-H06
N31-2021041-H06
SPI ROM
MX25V2033FM1I
M31-25V2002-M24
Closed PIN1
Closed PIN99
Closed PIN46,85
3V Analog Power
MICRO-STAR INT'L CO.,LTD
MS-7C91
SIO - NCT6687D-M
Date: Tuesday, April 21, 2020
Sheet 27 of 78

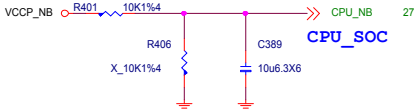
HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect

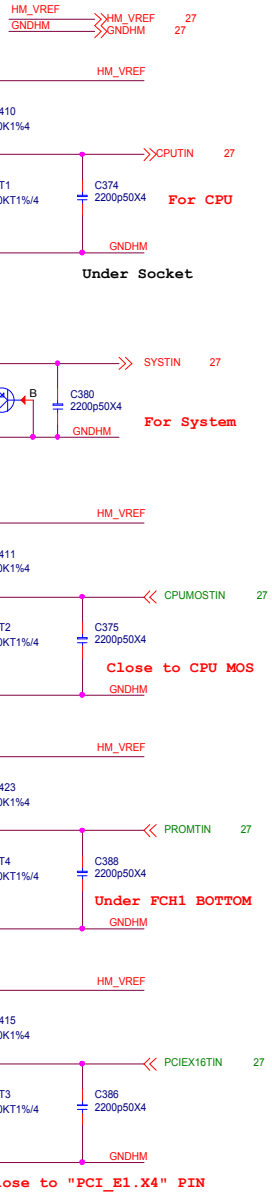








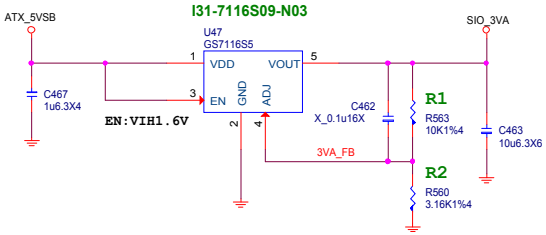
TEMP SENSOR



PM RESET

CPU RESET

SIO_3VA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V

MICRO-STAR INT'L CO.,LTD

MS-7C91

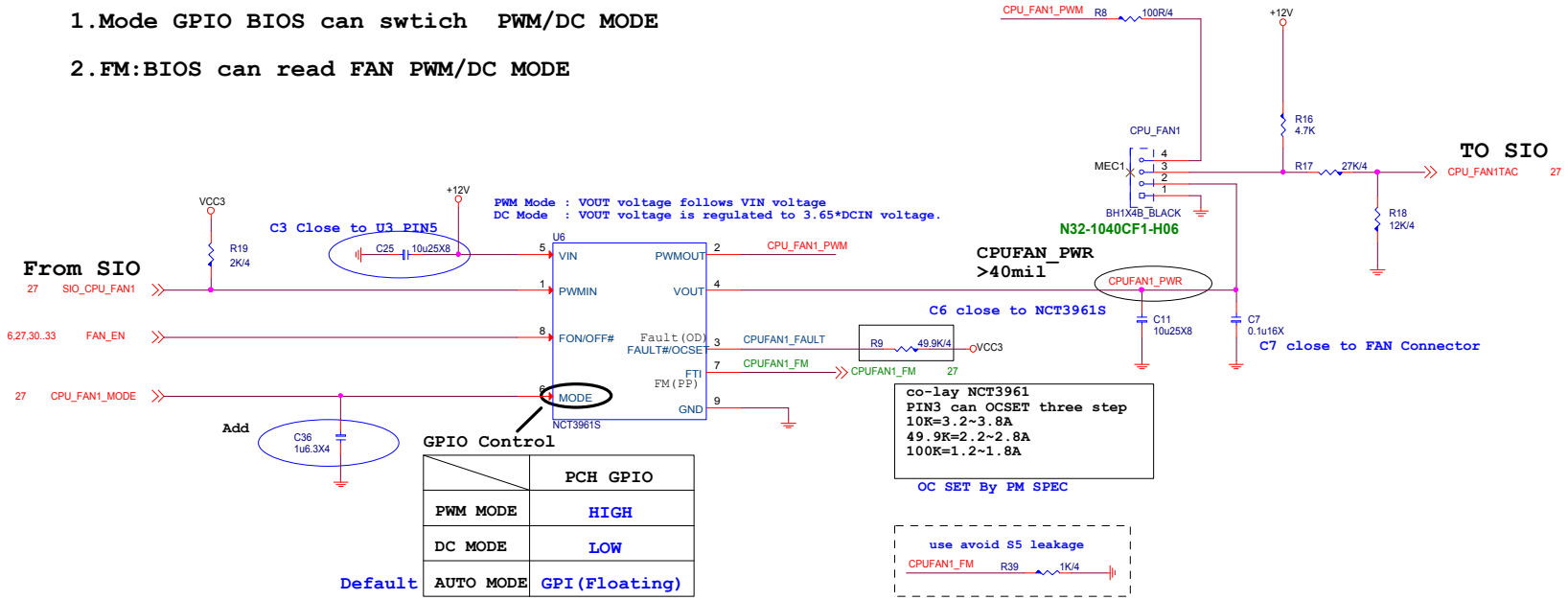
Size	Document Description	Rev
Custom	SIO - HW Monitor	10

Date: Tuesday, April 21, 2020 Sheet 28 of 78

CPUFAN1 TYPE N : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

2.FM:BIOS can read FAN PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

MS-7C91

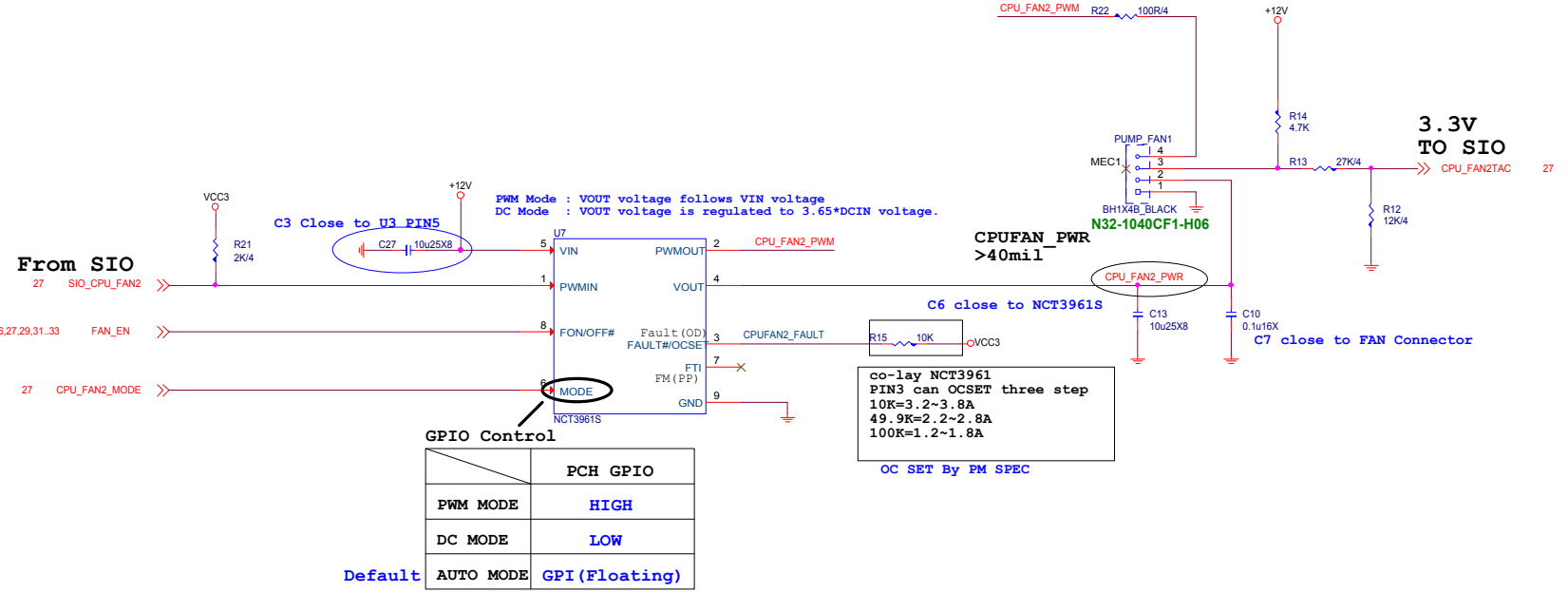
Size: Custom | Document Description: FAN TYPE-L CPUFAN1 | Rev: 10

Date: Tuesday, April 21, 2020 | Sheet 29 of 78

PUMPFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



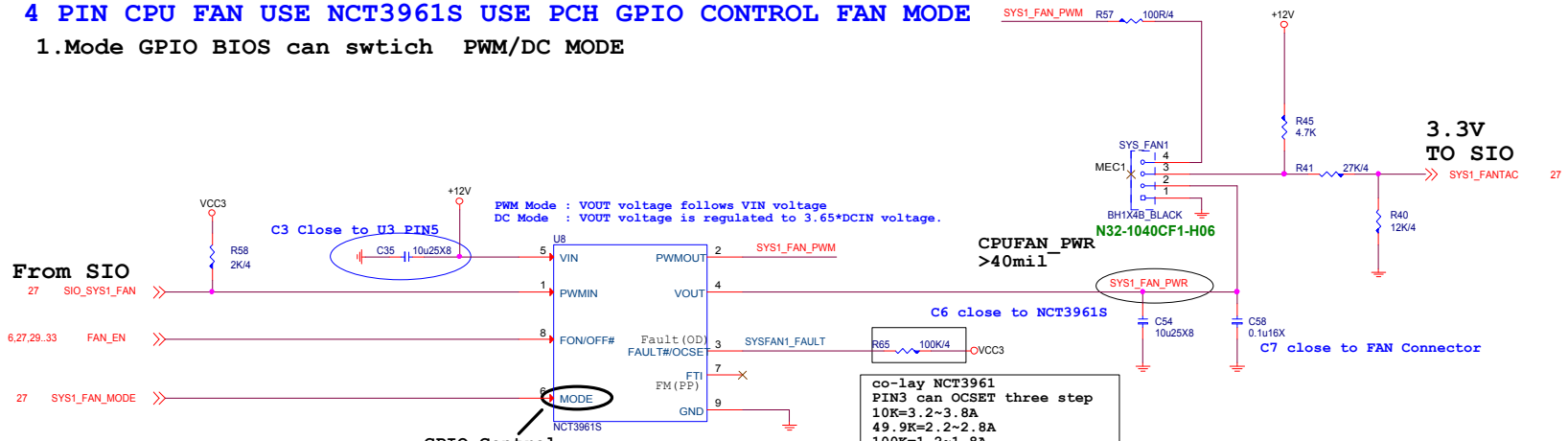
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: FAN TYPE-K PUMPFAN1
Rev: 10	
Date: Tuesday, April 21, 2020	Sheet 30 of 78

SYSFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

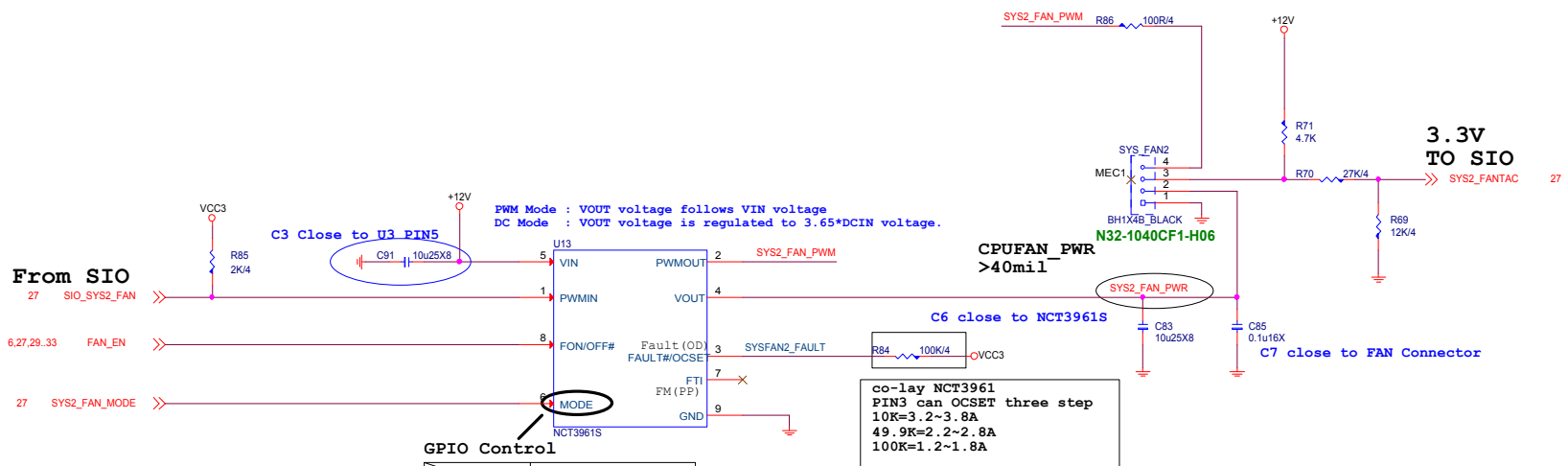


	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

SYSFAN2

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

MS-7C91

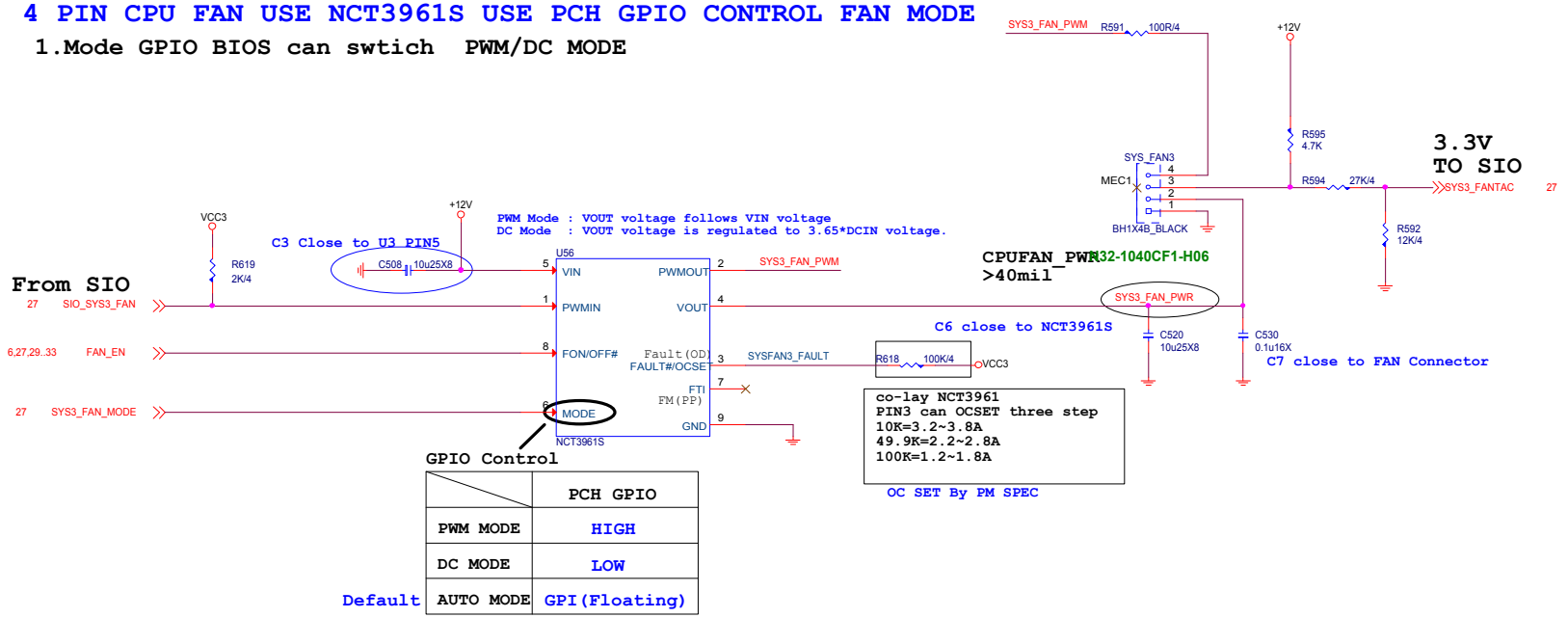
Size: Custom | Document Description: FAN TYPE-K SYSFAN1/2 | Rev: 10

Date: Tuesday, April 21, 2020 | Sheet 31 of 78

SYSFAN3

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

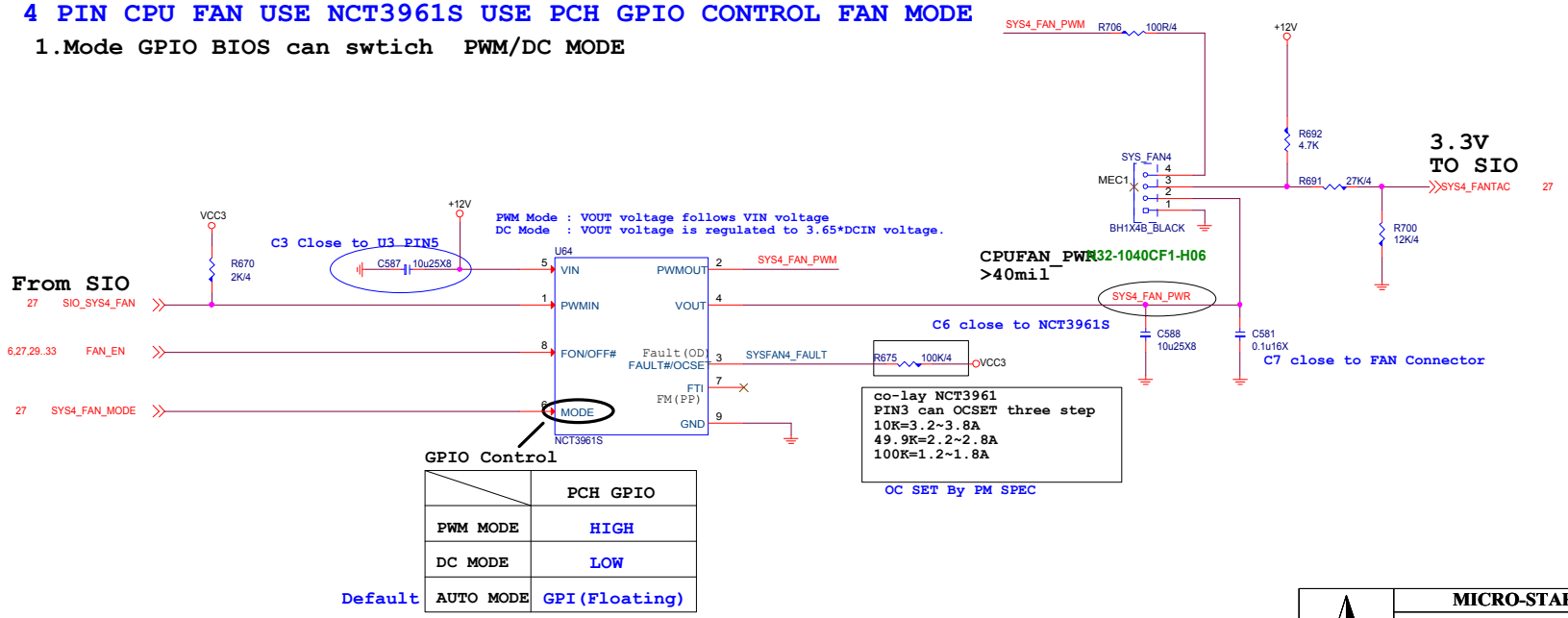


	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

SYSFAN4

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

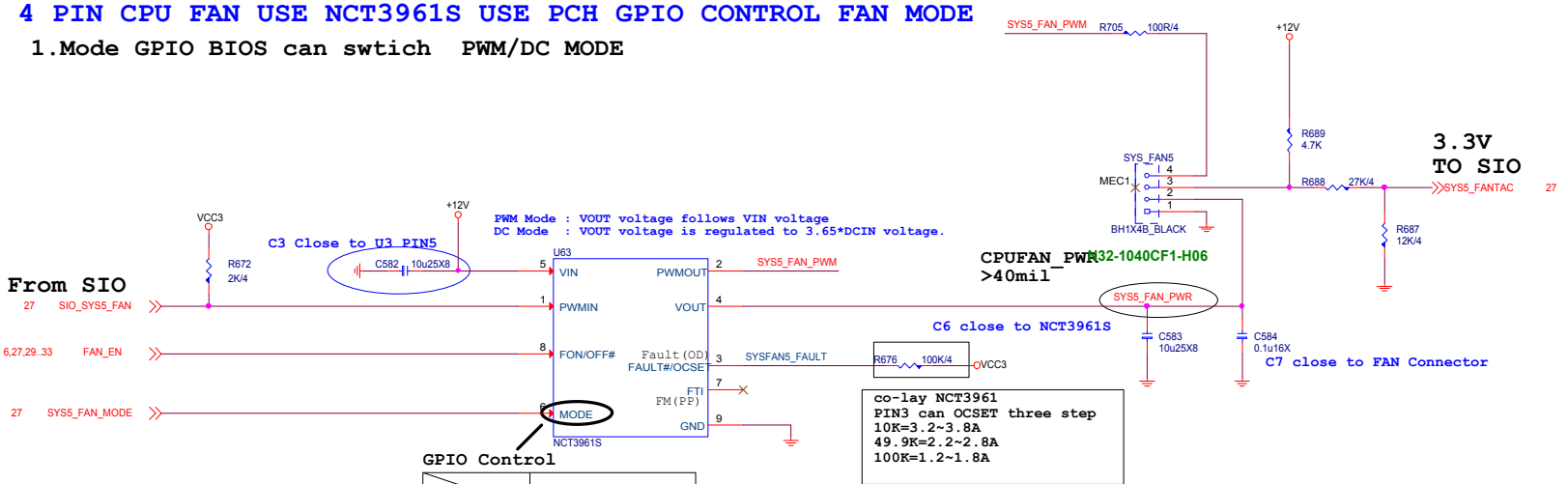
MS-7C91

Size	Document Description	Rev
Custom	FAN TYPE-K SYSFAN3/4	10

Date: Tuesday, April 21, 2020 Sheet 32 of 78

SYSFAN5 TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

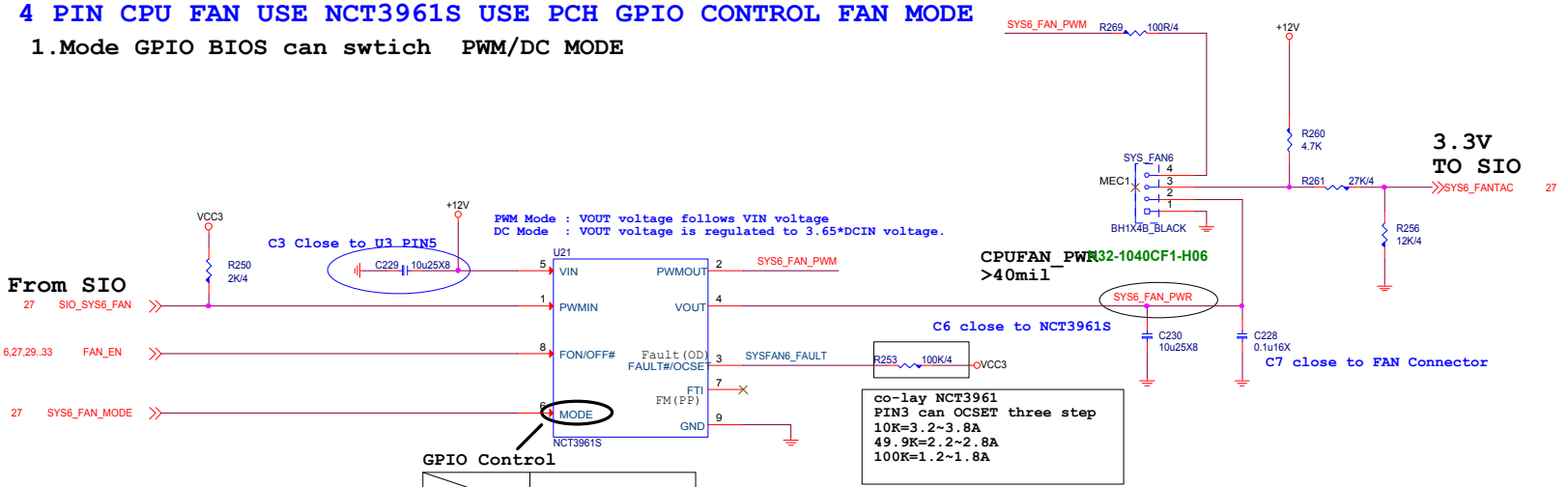
1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

SYSFAN6 TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

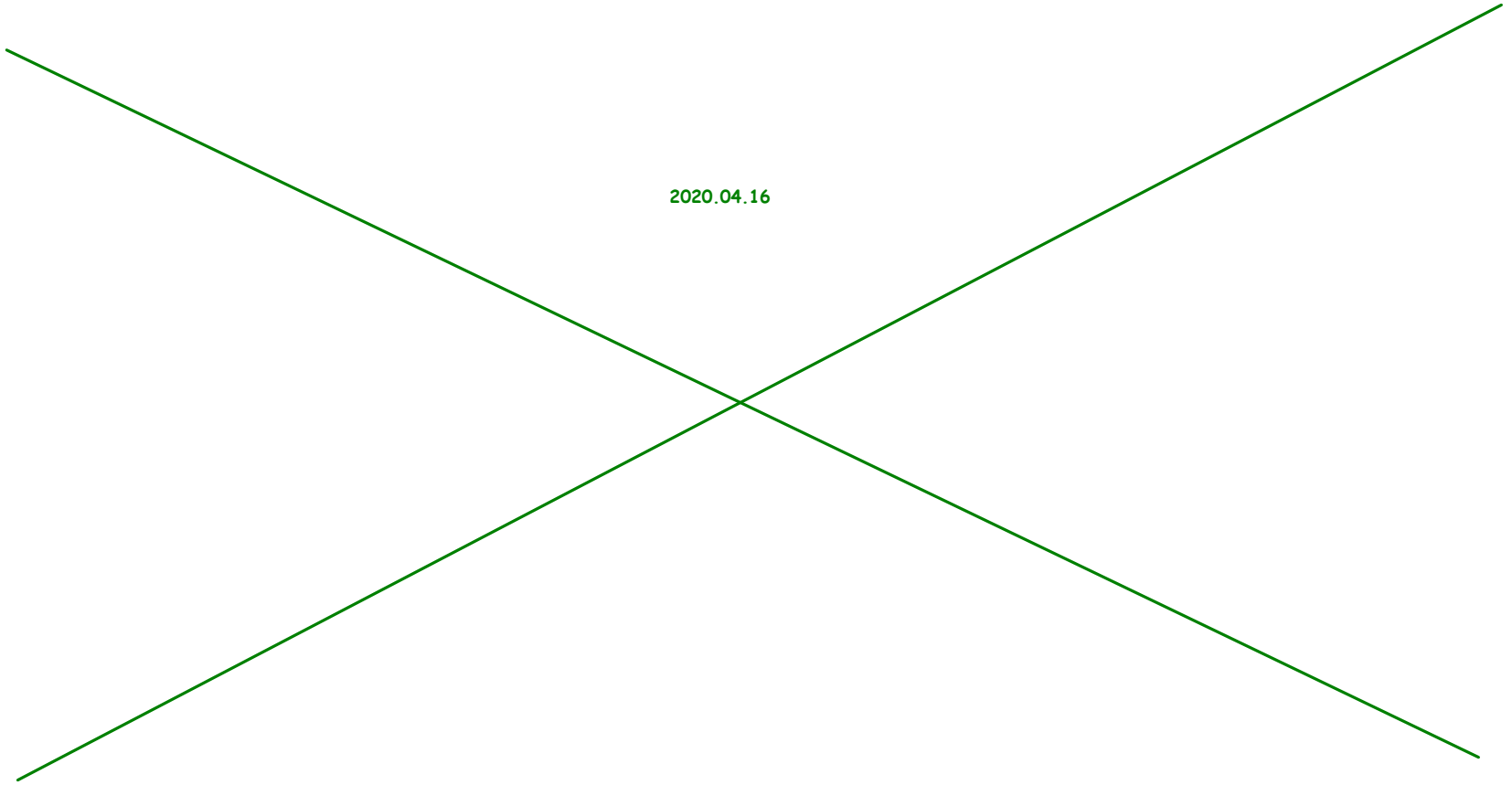
MS-7C91

Size	Document Description	Rev
Custom	FAN TYPE-N SYSFAN5	10

Date: Tuesday, April 21, 2020 Sheet 33 of 78

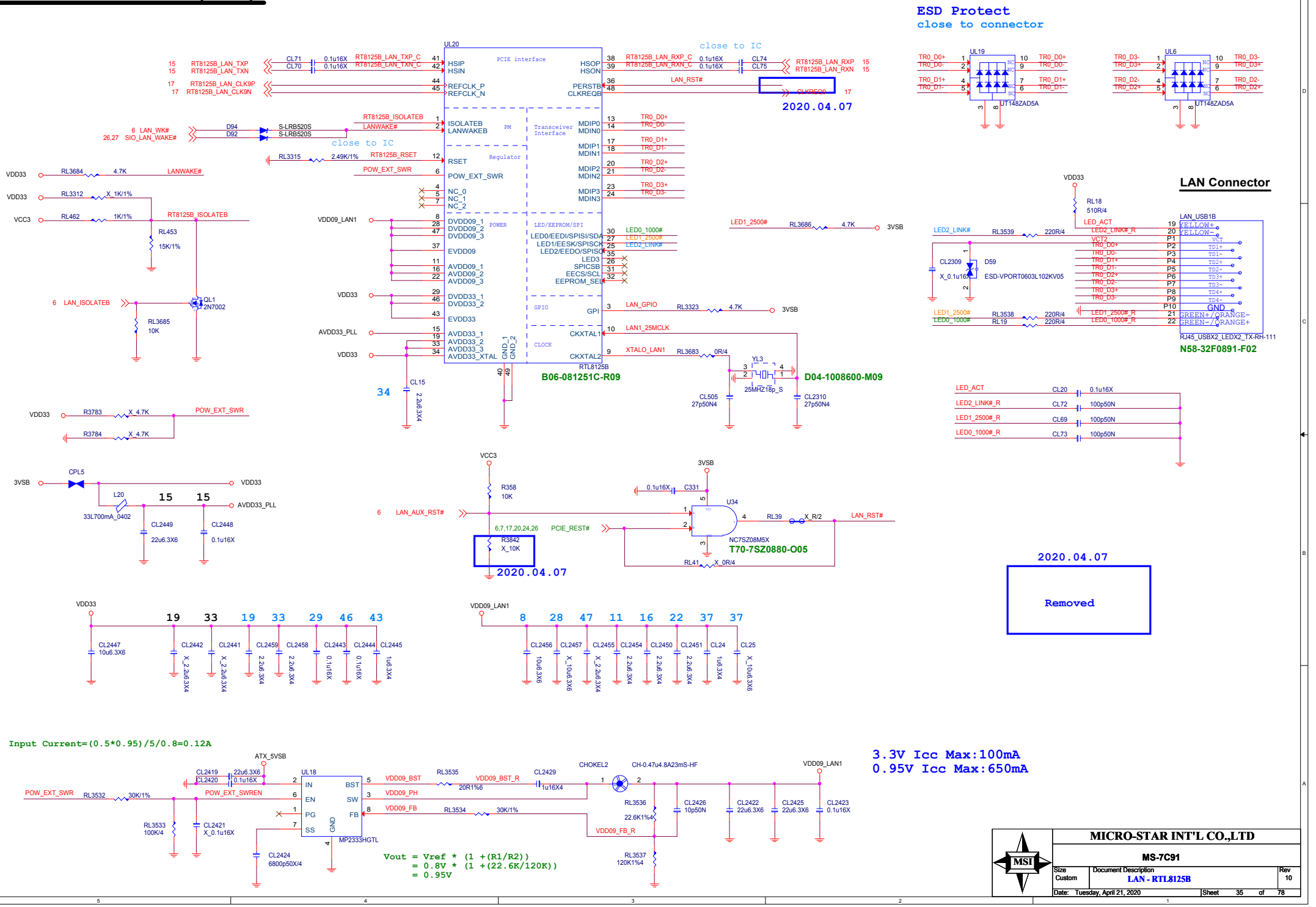
RTL8111H Giga LAN

2020.04.16



MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: RTL8111H Giga LAN	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 34 of 78	

Realtek Lan1-RTL8125B(2.5G)



MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: LAN - RTL8125B
Rev: 10	
Date: Tuesday, April 21, 2020	Sheet 35 of 78

ALC1200-VD1_48PIN

PIN 1~12, 47~49 reference GND, others reference AGND

follow PCH power well

CA3,CA4 close to pin24

Closed PIN9

Closed PIN1

closed PIN43

closed PIN25

2020.03.25

Closed Pin3

Closed Pin 27

close to codec

ALC1200-VD1-CG-RH

C91-1011051-N07

For EMI

Digital

Analog

93.6mA

R11-0000034-W08

ESD-MLVS0402L04

Closed Codec

near JACK

AUDIOJACKX5_SPDIFX1-RH-8

LIN_OUT

SURR

LIN_IN

CEN/BAS

MIC1

N58-25F0491-L06

N58-25F0451-L06

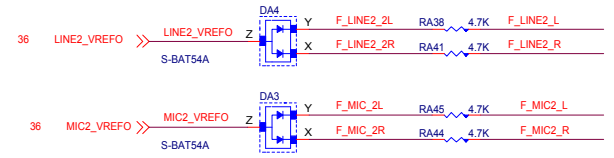
4	CEN/BAS
5	SURR
6	SPDIFO1
3	LIN_IN
2	LIN_OUT
1	MIC1

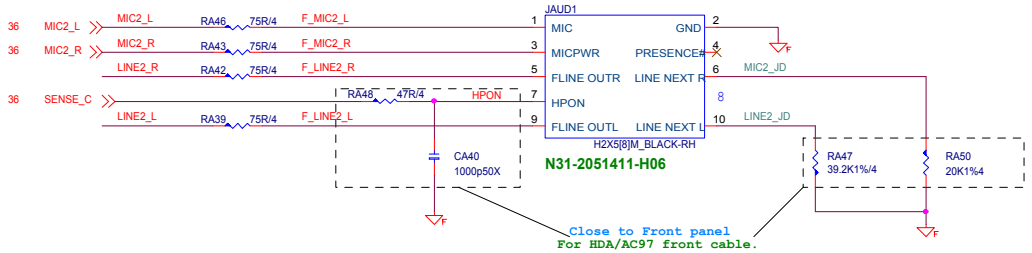
MICRO-STAR INT'L CO.,LTD

MS-7C91

Size: Custom | Document Description: Audio ALC1200-VD1 | Rev: 10

Date: Tuesday, April 21, 2020 | Sheet 36 of 78

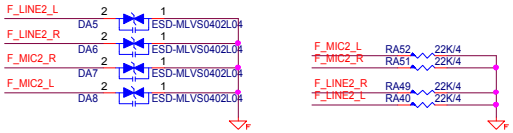




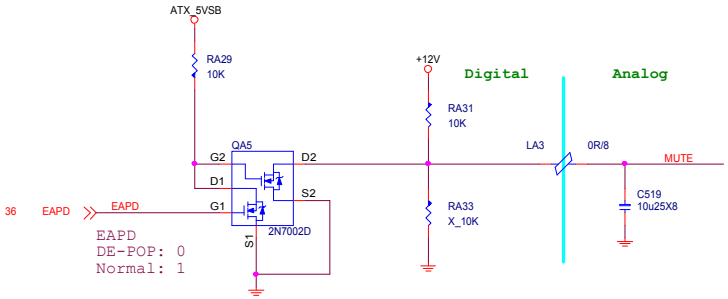
D0G-2710510-I05
Close to Front panel

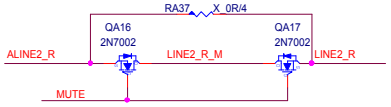
ESD protect

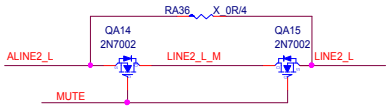
D0G-2710510-I05
AVL:D0G-2950500-SI0

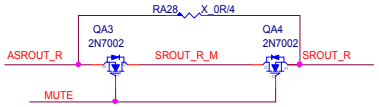


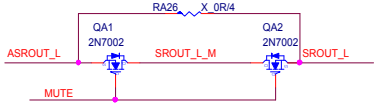
De-POP circuit

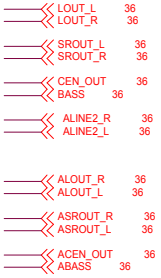


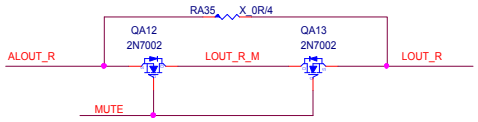


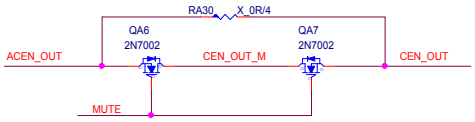


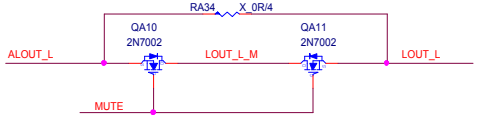


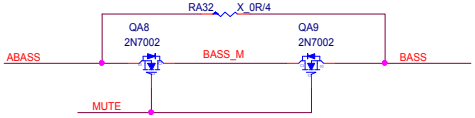












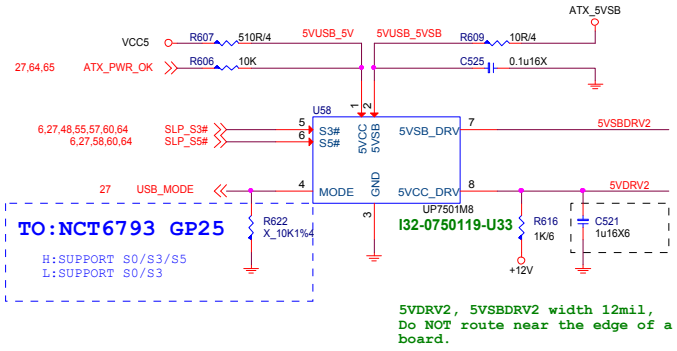
MICRO-STAR INT'L CO.,LTD

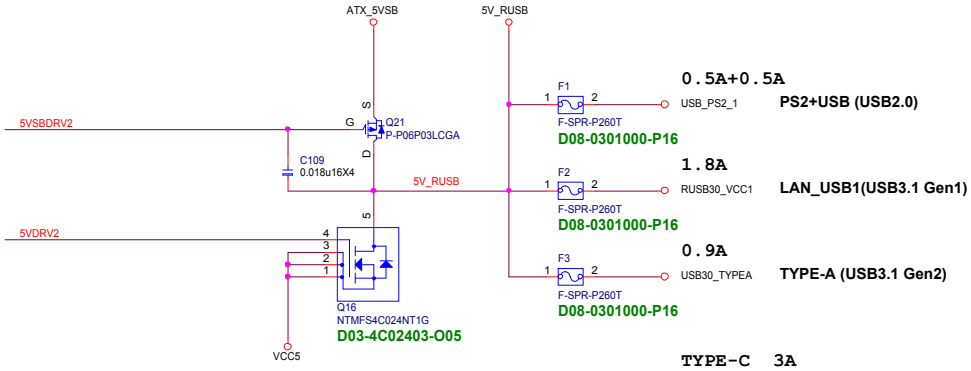
MS-7C91

Size	Document Description	Rev
Custom	Audio DePop	10

Date: Tuesday, April 21, 2020 Sheet 37 of 78

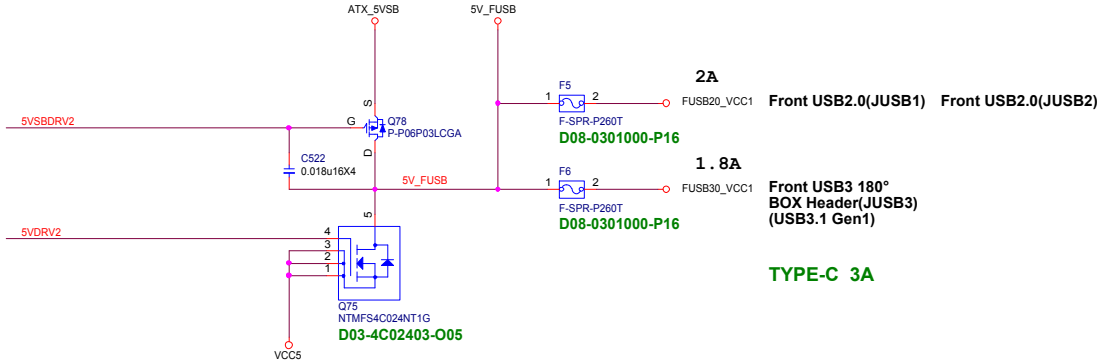
USB Power





Rear (6.7A)

Front (6.8A)

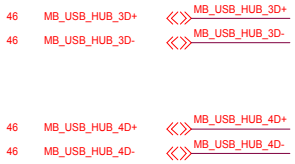


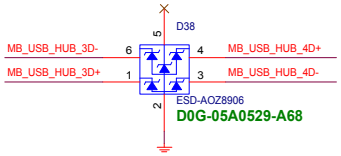
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C91	
Size: Custom	Document Description: USB Power - UP7501	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 38 of 78	

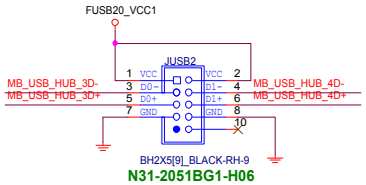
Front USB2.0(JUSB2)

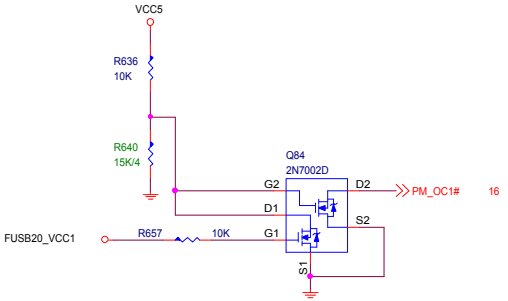
Form GL850G USB2.0 HUB

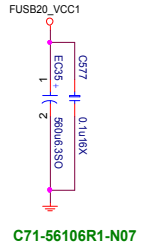
5V@1A







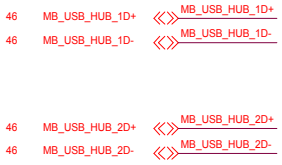


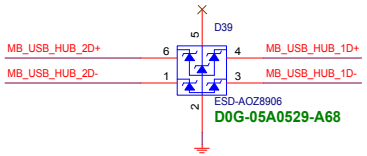


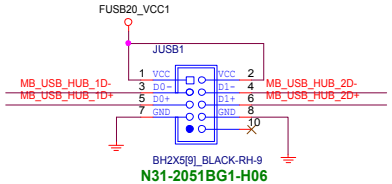
Front USB2.0(JUSB1)

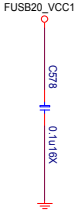
Form GL850G USB2.0 HUB

5V@1A







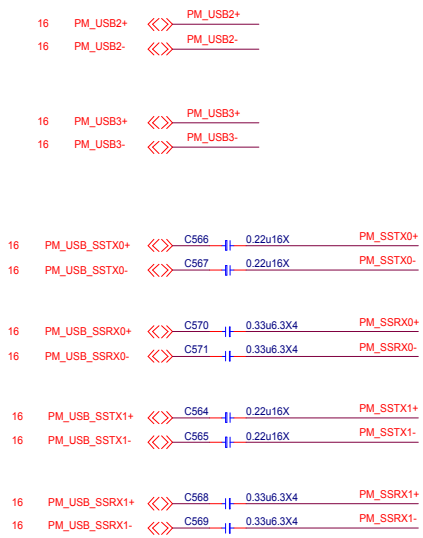


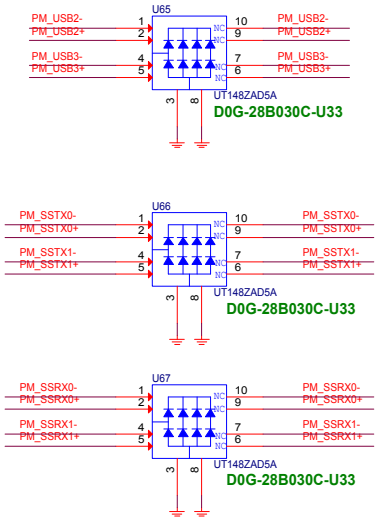
MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: Front USB2.0 Header	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 39 of 78	

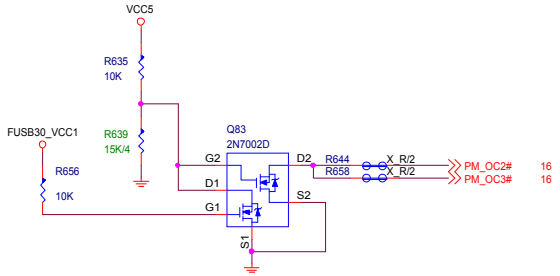
Front USB3 180°

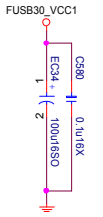
BOX Header(JUSB3)

5V@1.8A

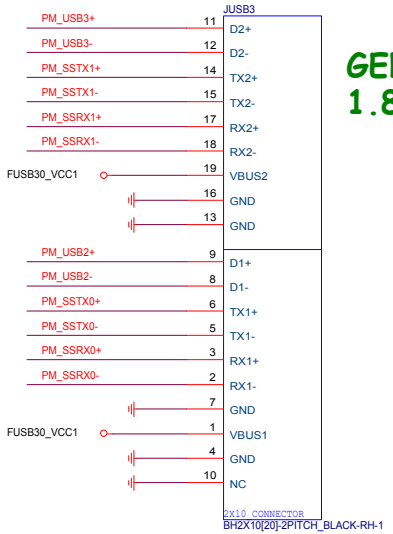








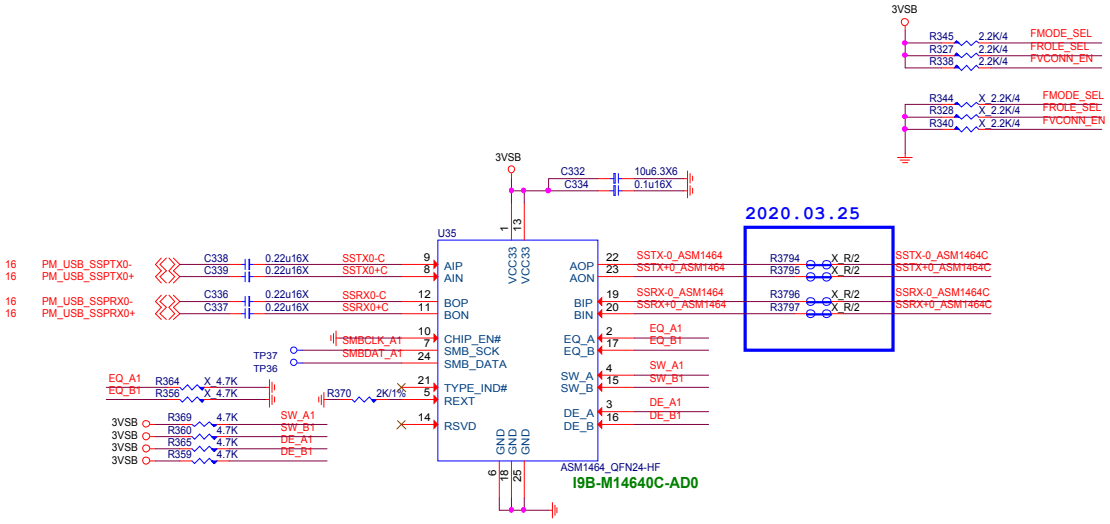
C71-1011761-N07

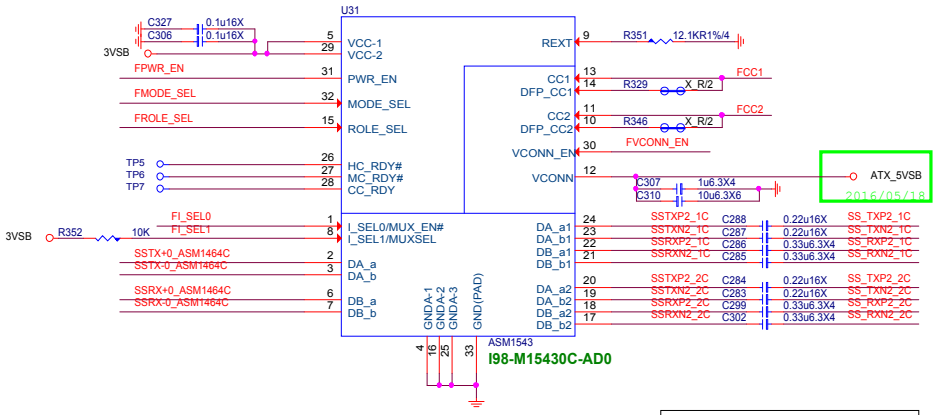


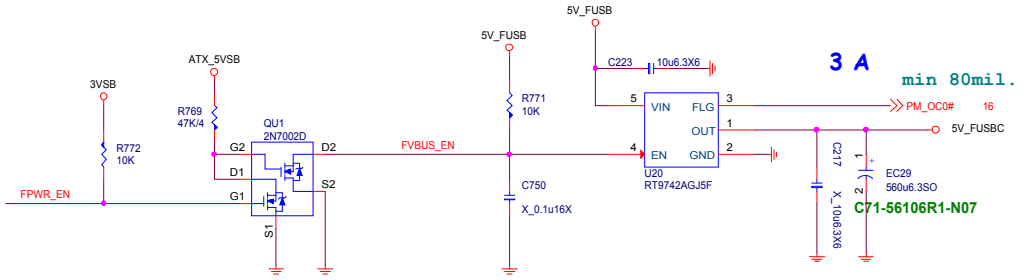
GEN1
1.8A

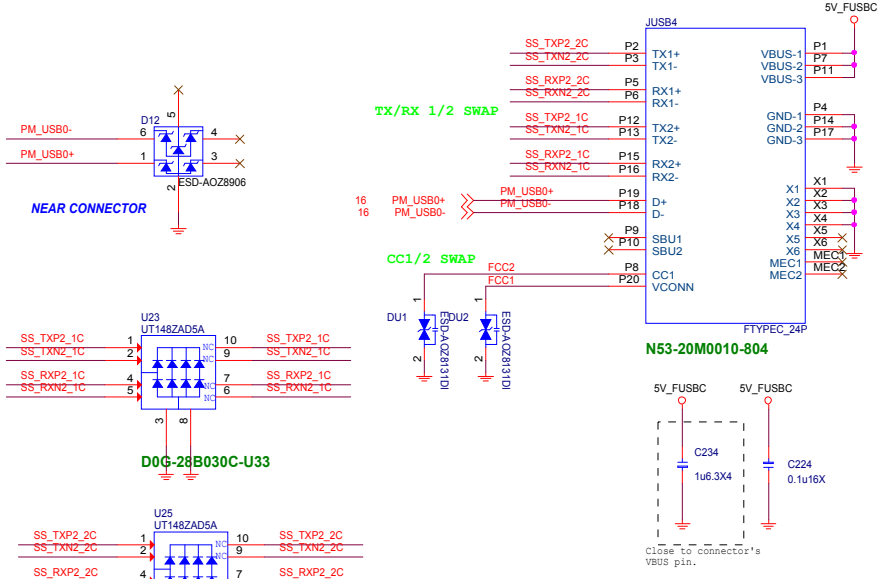
N32-2101091-H06

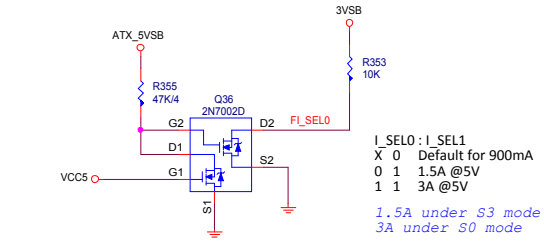
MICRO-STAR INT'L CO.,LTD			
MS-7C91			
Size: Custom	Document Description: Front USB3.0 Header		Rev: 10
Date: Tuesday, April 21, 2020		Sheet 40 of 78	











MICRO-START INT'L CO.,LTD.

Title: Front USB3.1 Type C / mux

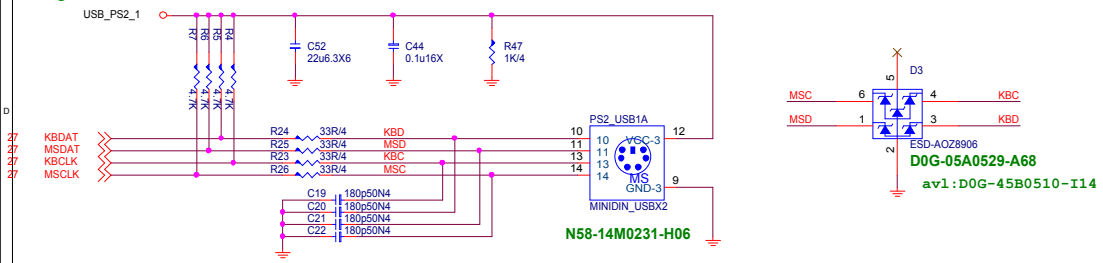
Size: Custom | Document Number: MS-7C91 | Rev: 10

Date: Tuesday, April 21, 2020 | Sheet 41 of 78

PS2+USB (USB2.0)

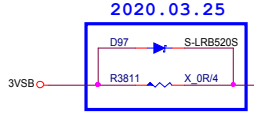
5V@1A

layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch



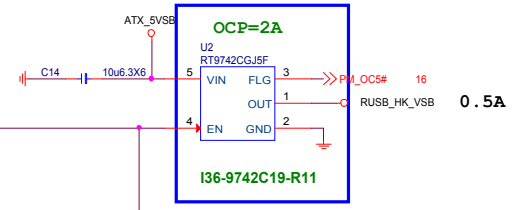
HOTKEY POWER

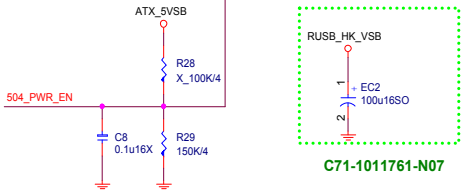
2020.03.25



2020.03.30

OCP=2A

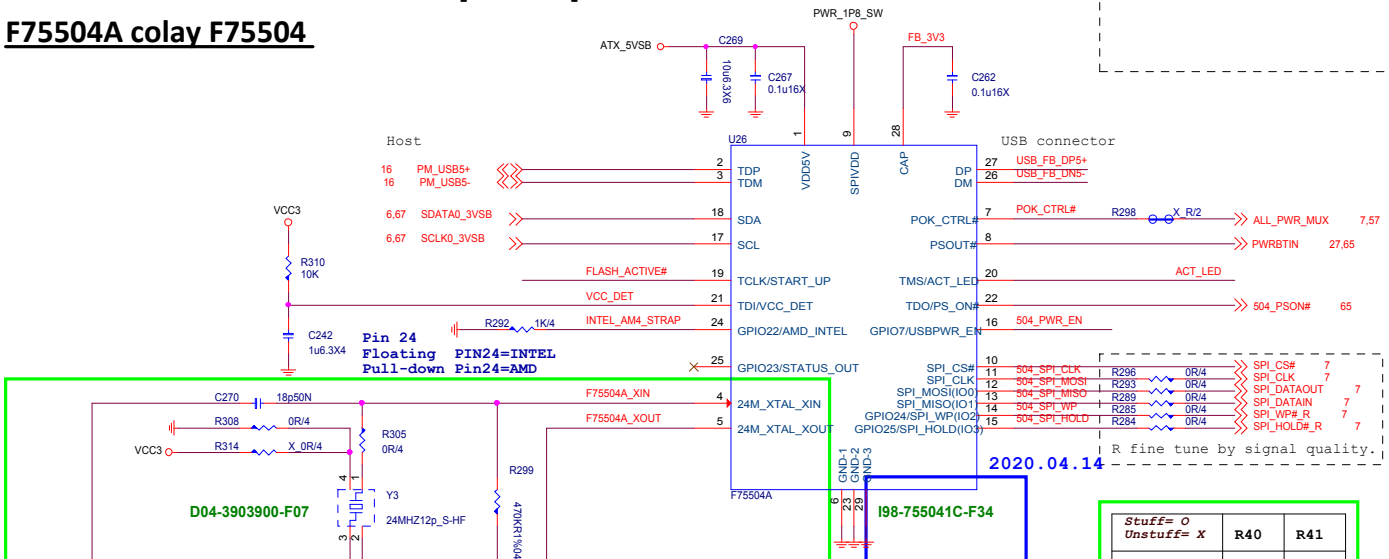




USB Flash BIOS

F75504A colay F75504

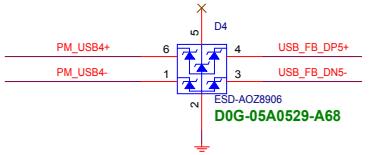
F75504A/F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.

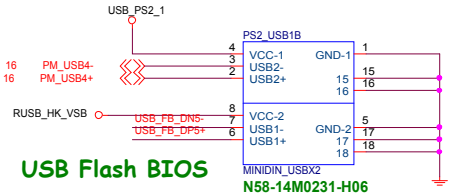


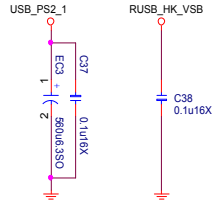
Stuff= O Unstuff= X	R500	R502	R503	R504	C510	R497	R499	R501	Y1
F75504A	O	O	X	X	10pF	0R	X	O	D04-3902700-F07
F75504	X	X	O	O	X	0.1uF	O	X	D05-1100600-F07

Stuff= O Unstuff= X	R40	R41
F75504A	O	O
F75504	X	X

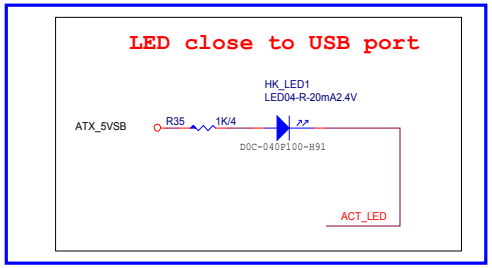
2019/06/17

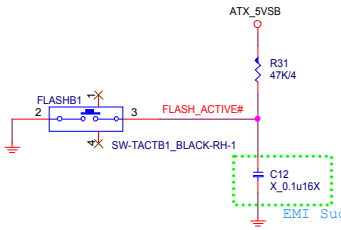


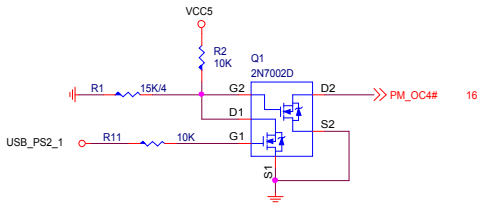




2020.04.14

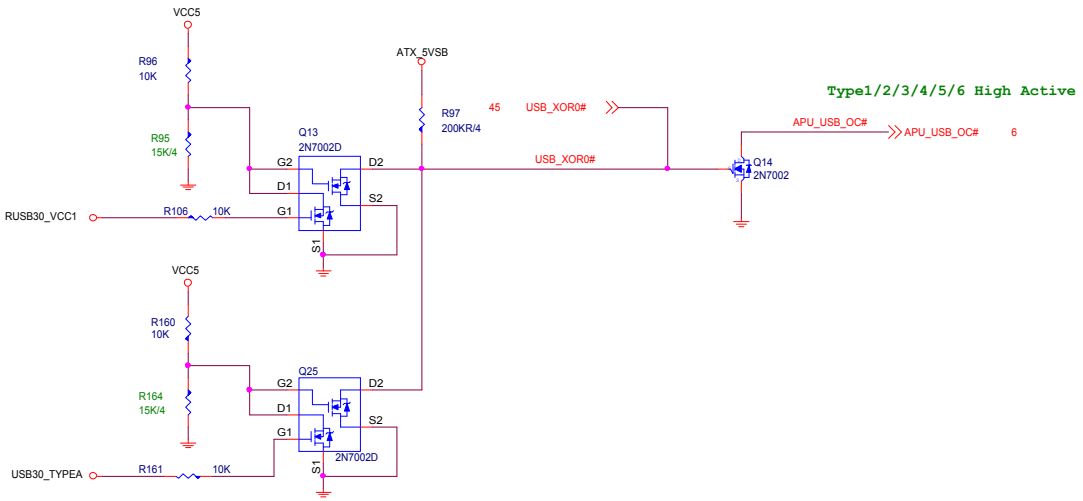




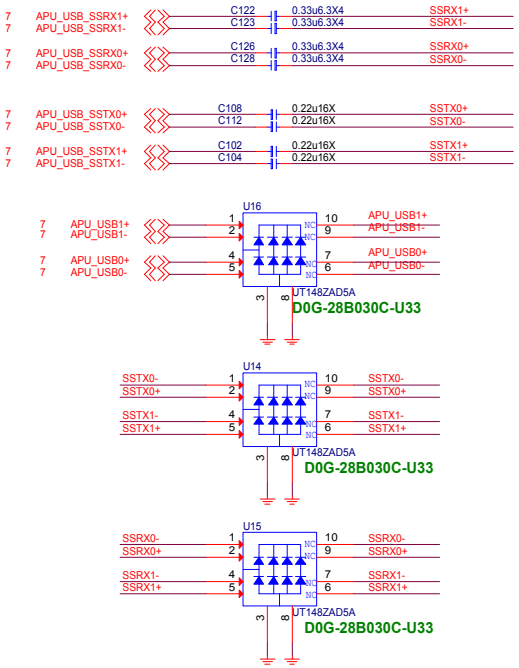


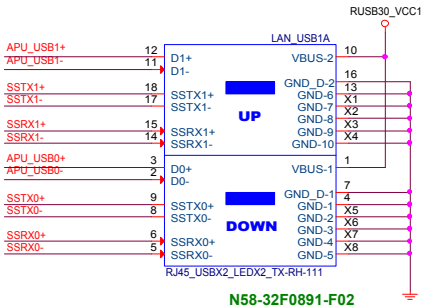
MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: Rear USB2.0+PS2+F75504A	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 42 of 78	

CPU USB_OC

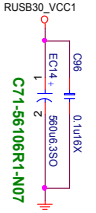


Rear USB3.1 GEN1 5V@1.8A



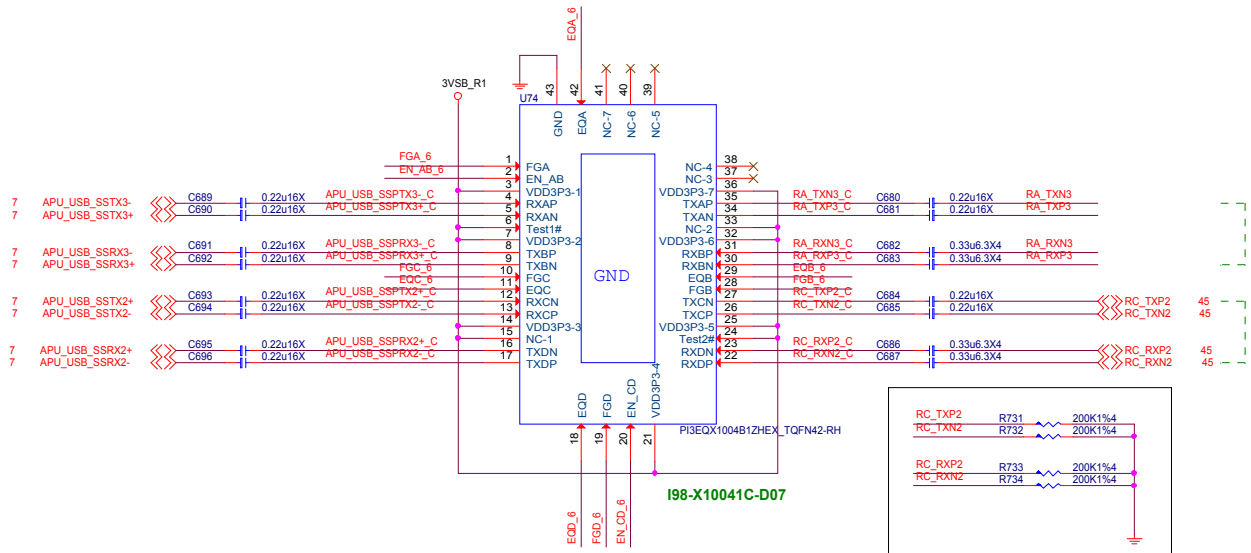


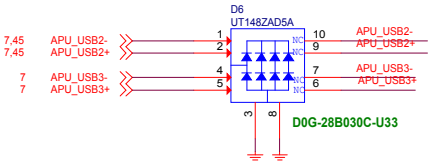
1.8A

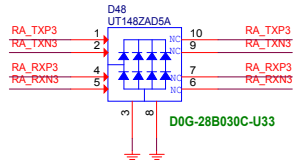


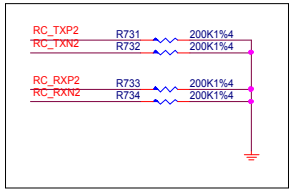
MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: Rear USB3.1.
Rev: 10	
Date: Tuesday, April 21, 2020	Sheet 43 of 78

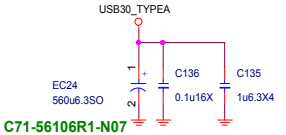
TYPE-A PI3EQX1004 Redriver

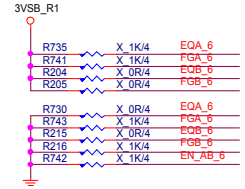


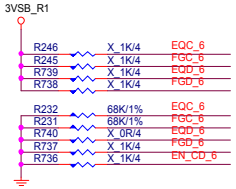


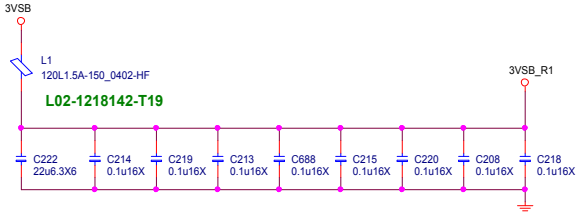












EQ	dB	
0	10.9	0 to GND
R	6.7	68K to GND
F	8.9	NC
1	13.1	0 to VDD

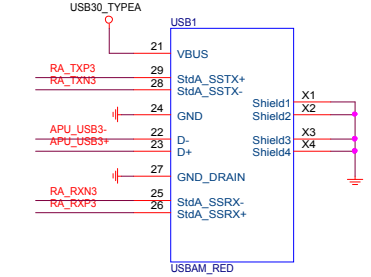
		EQ	FG
USB3_TX4	A	R	F
USB3_RX4	B	R	L
USB3_TX3	C	R	F
USB3_RX3	D	R	L

FG	dB	
0	-3	0 to GND
R	-1.5	68K to GND
F	0	NC
1	2	0 to VDD

GEN2 0.9A

2020.04.16

1.0 BOM



MICRO-STAR INT'L CO.,LTD

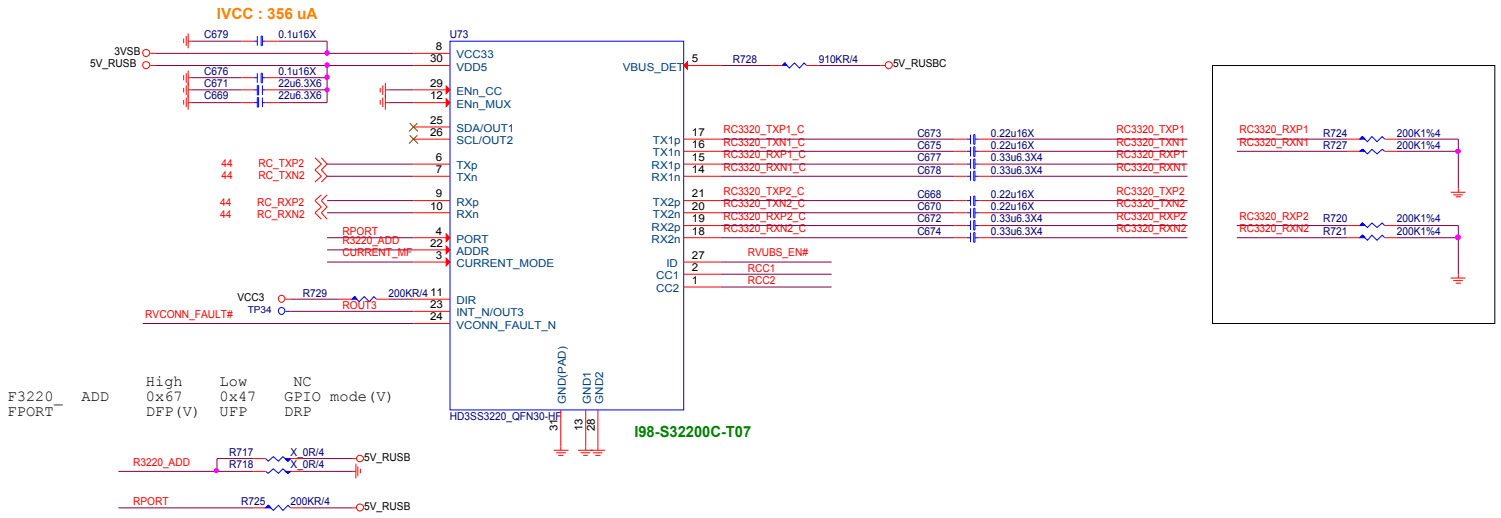
MS-7C91

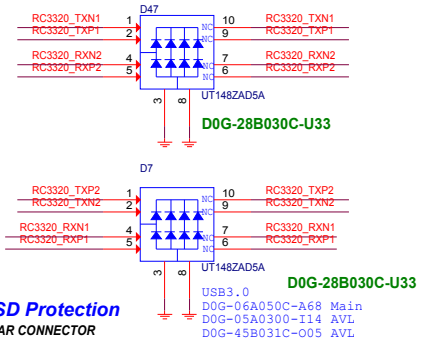
Size	Document Description	Rev
Custom	Rear USB3.1 Type A / Redrive	10

Date: Tuesday, April 21, 2020 Sheet 44 of 78

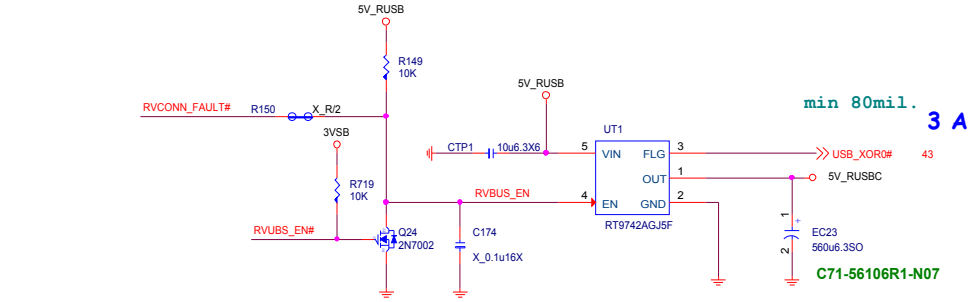
USB 3.1-Type-C

USB Type-C MUX with Configuration Channel (CC)

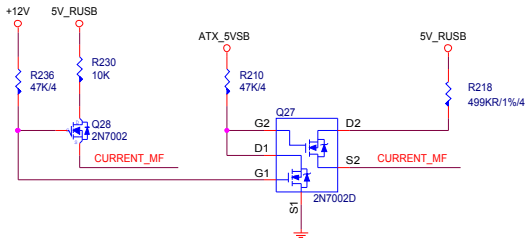


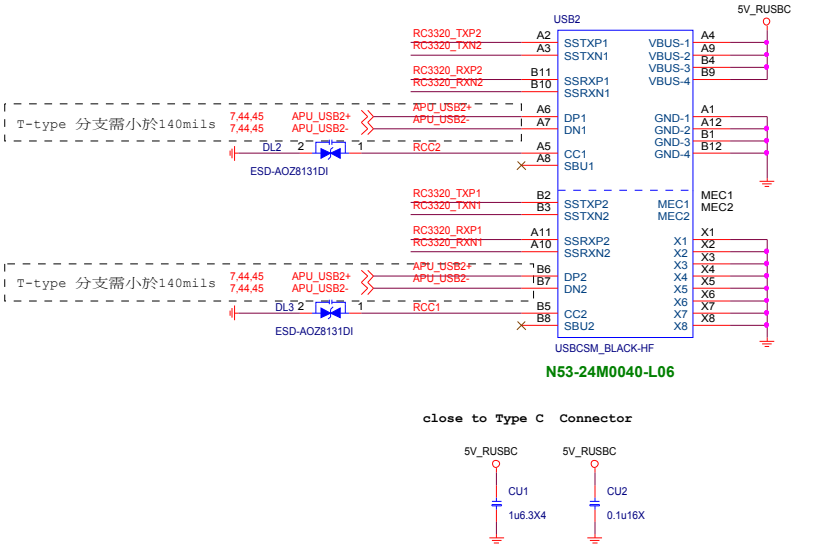


VBUS EN



Current Mode



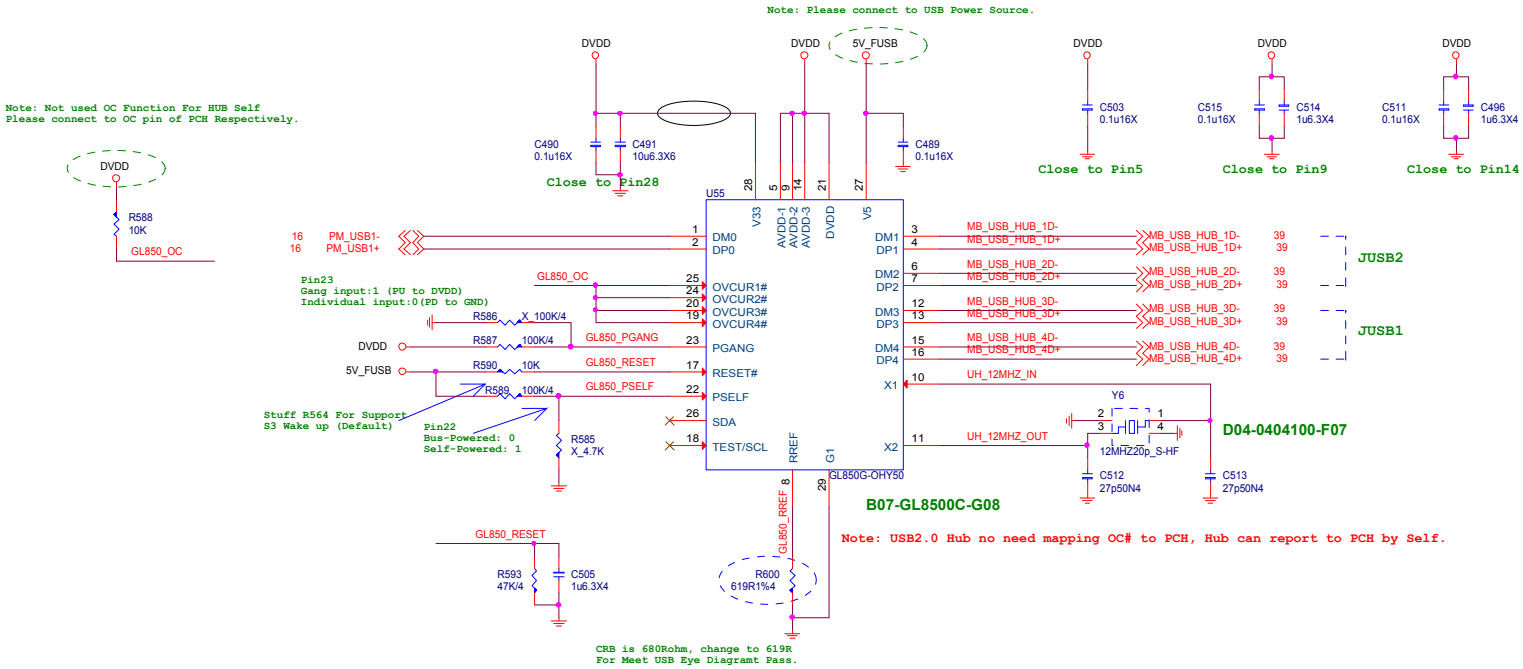


close to Type C Connector

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C91	
Size: Custom	Document Description: Rear USB3.1 Type C / mux	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 45 of 78	

GL850G USB2.0 HUB

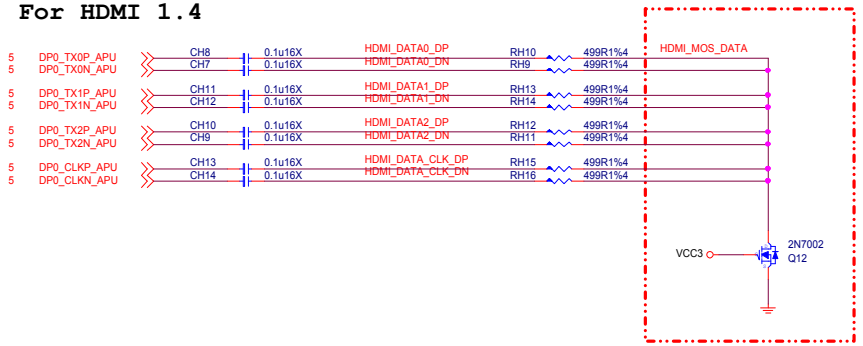
5V_FUSB

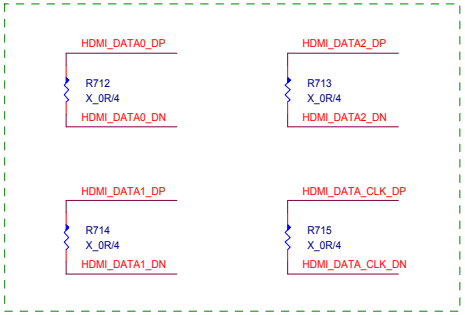


MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: GL850G	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 46 of 78	

HDMI CONNECTOR

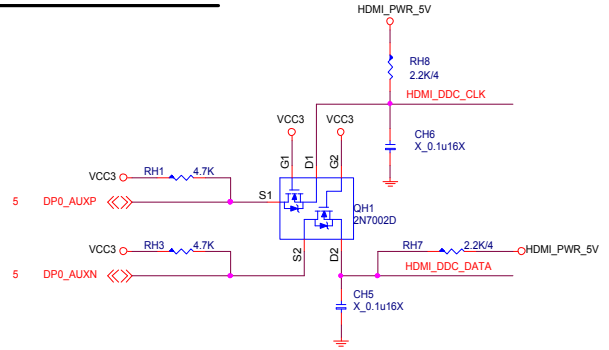
For HDMI 1.4



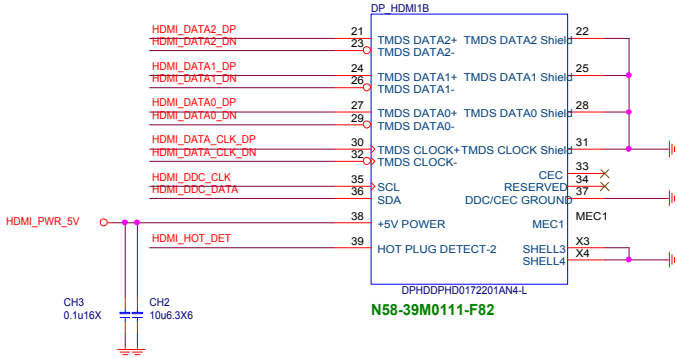


HDMI_MOS_DATA trace length <500mil
other platform please check design guide

AUX Level Shifter

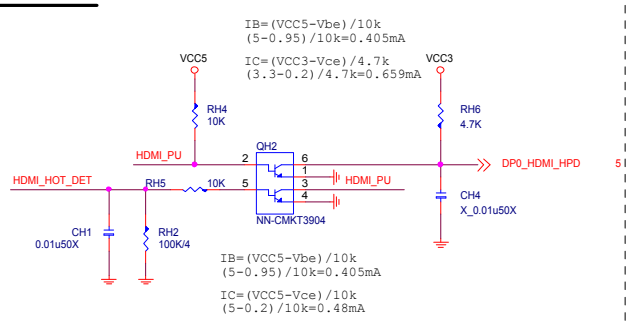


Connector

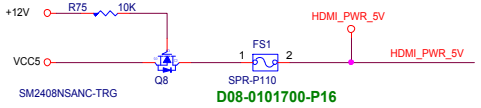


N58-39M0111-F82

HPD Circuit



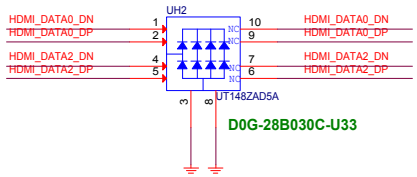
Connector Power



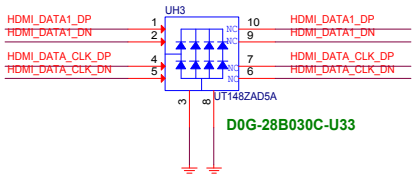
D08-0101700-P16

如果用DIODE SA測試電壓會不過

For EMI

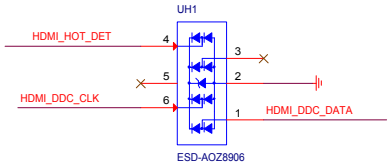


D0G-28B030C-U33



D0G-28B030C-U33

注意:耐壓5v零件

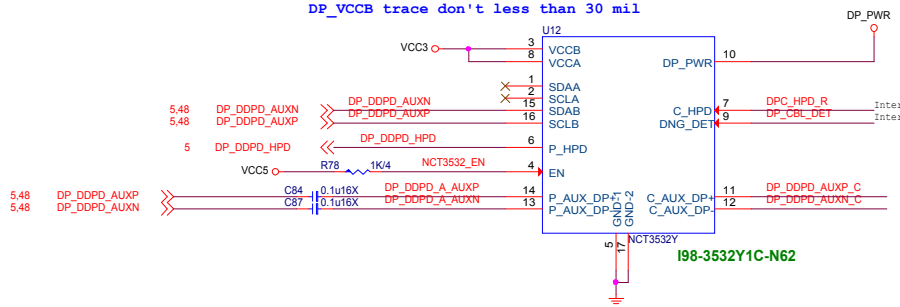


ESD-AOZ8906

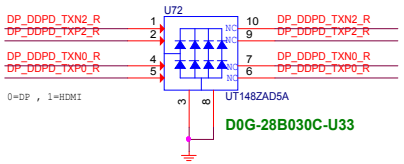
MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: HDMI	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 47 of 78	

500mA

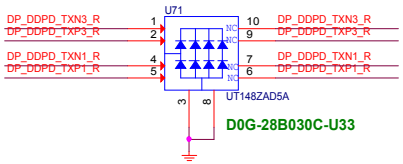
DP_VCCB trace don't less than 30 mil



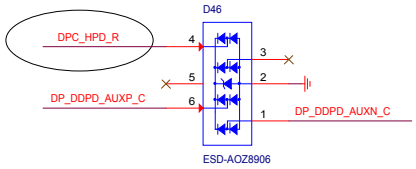
I98-3532Y1C-N62

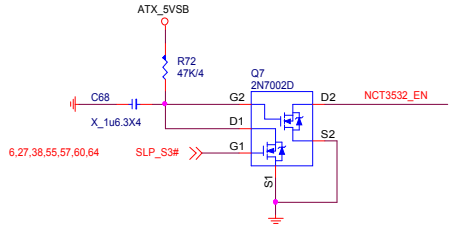


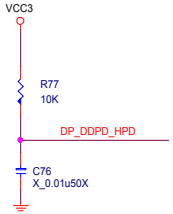
D0G-28B030C-U33

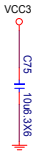


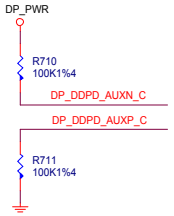
D0G-28B030C-U33

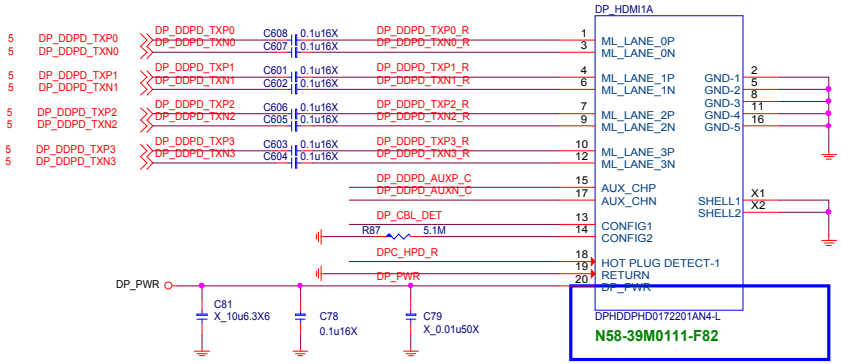








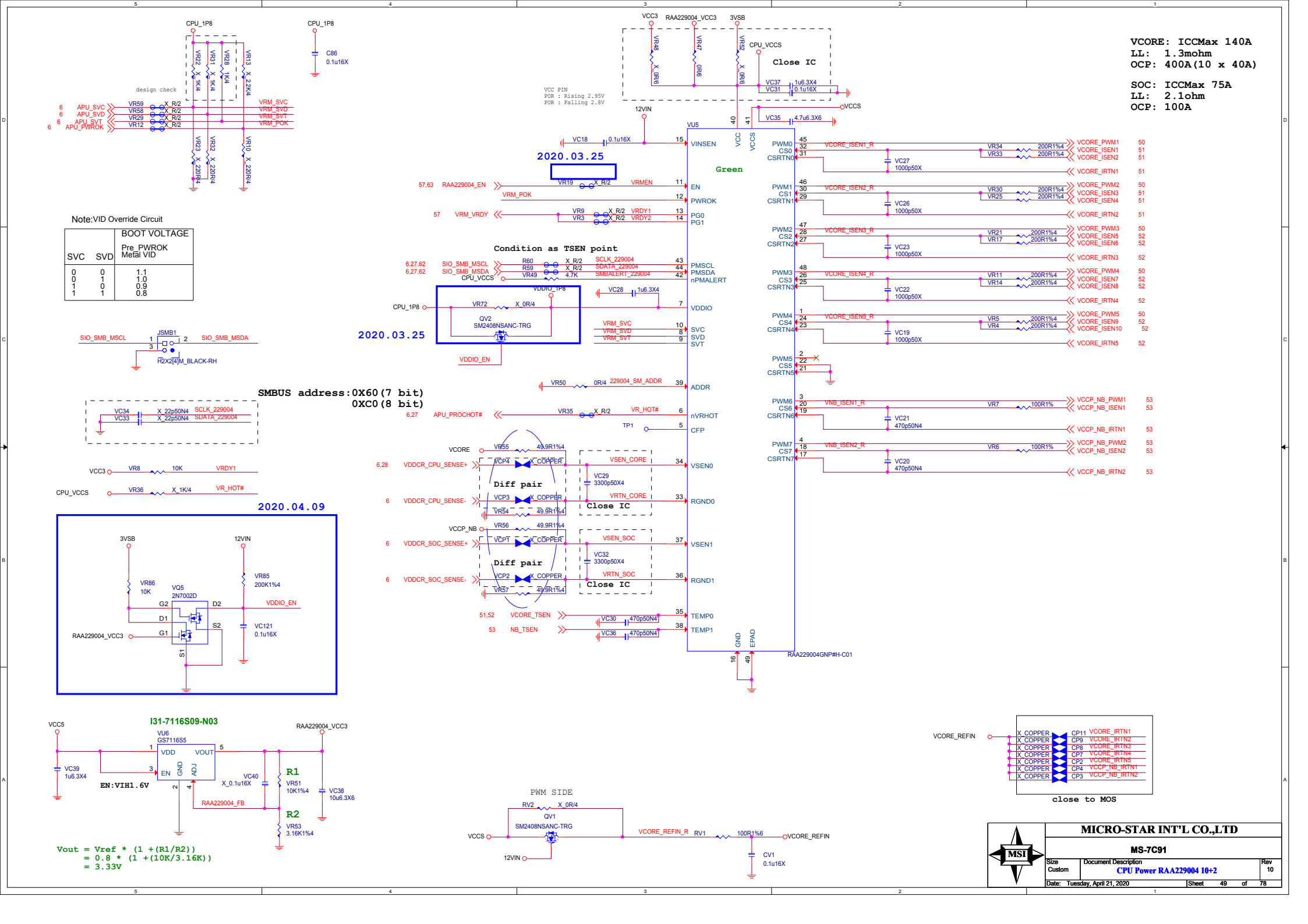




N58-39M0111-F82

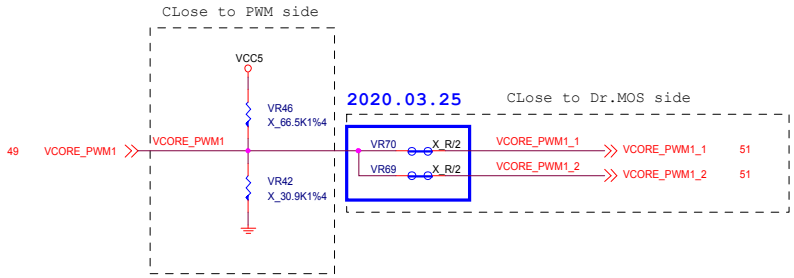
2020.04.13

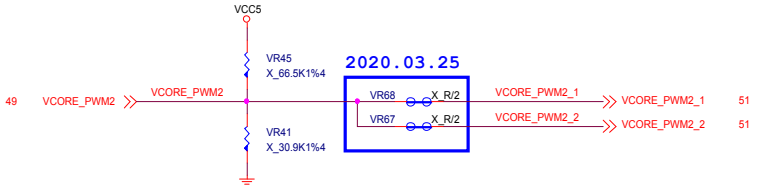
MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: DP	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 48 of 78	

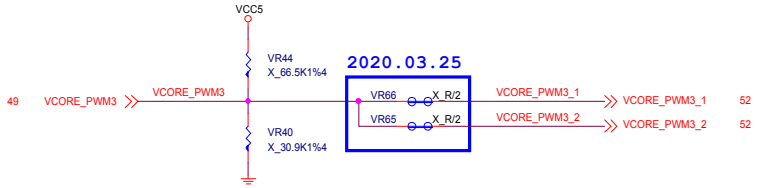

VCORE: ICCMax 140A
LL: 1.3mohm
OCP: 400A(10 x 40A)
SOC: ICCMax 75A
LL: 2.1ohm
OCP: 100A
Note:VID Override Circuit
SVC SVD BOOT VOLTAGE Pre_PWROK Metal VID
0 0 1.1
0 1 1.0
1 0 0.9
1 1 0.8
SMBUS address:0X60(7 bit)
0XC0(8 bit)
2020.03.25
2020.04.09
Close IC
Diff pair
Condition as TSEN point
Green
RAA229004GNP#H-C01
I31-7116S09-N03
Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V
close to MOS
MICRO-STAR INT'L CO.,LTD
MS-7C91
CPU Power RAA229004 10+2
Date: Tuesday, April 21, 2020
Sheet 49 of 78

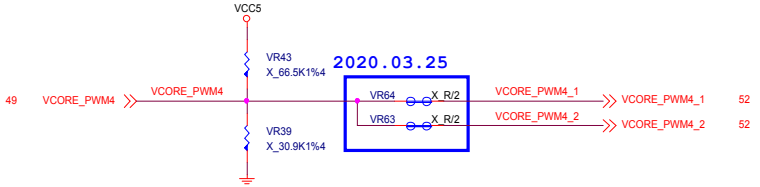
CPU_CORE Driver IC

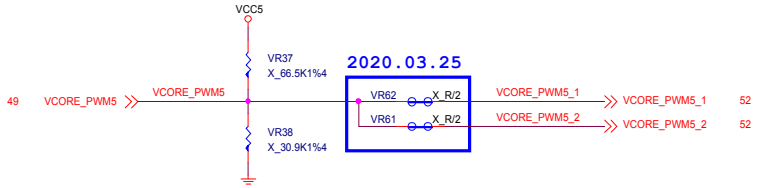
VCORE Double 10-PHASE









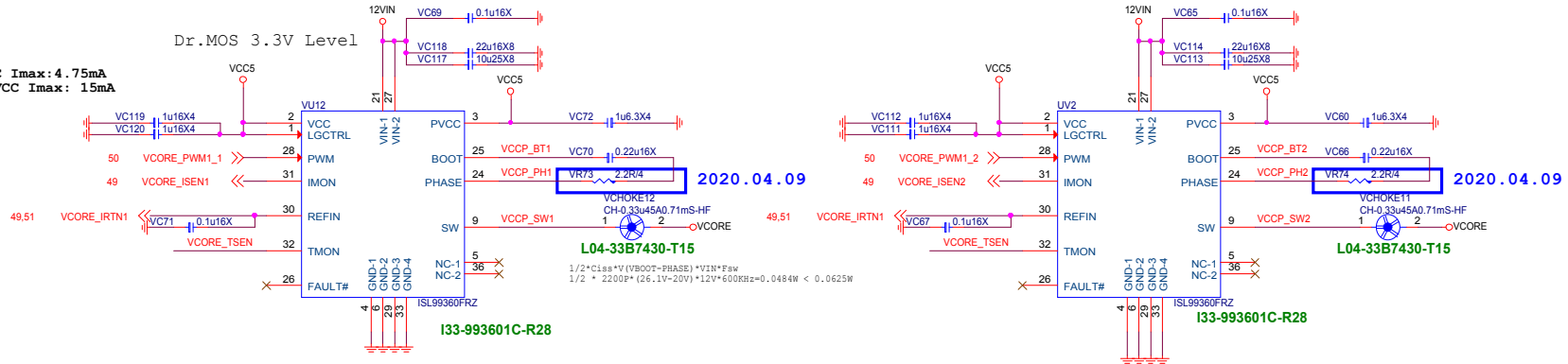


MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: CPU Power Phase Double IC SPS	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 50 of 78	

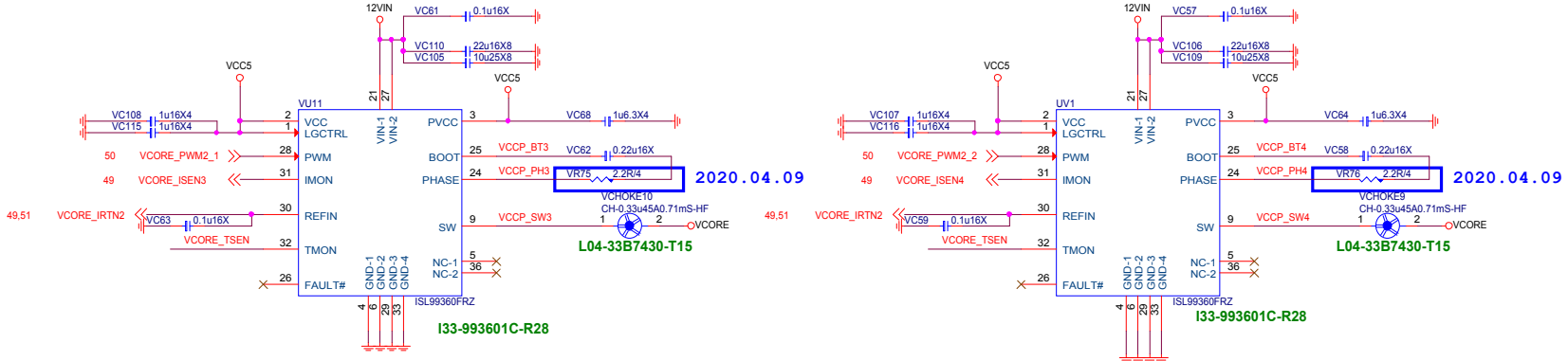
Vcore EDC Max 140A

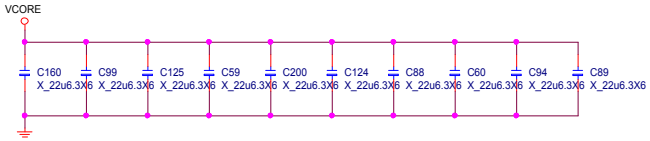
Dr.MOS 3.3V Level

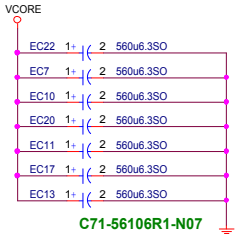
VCC Imax:4.75mA
IPVCC Imax: 15mA



49,52 VCORE_TSEN <<< VCORE_TSEN



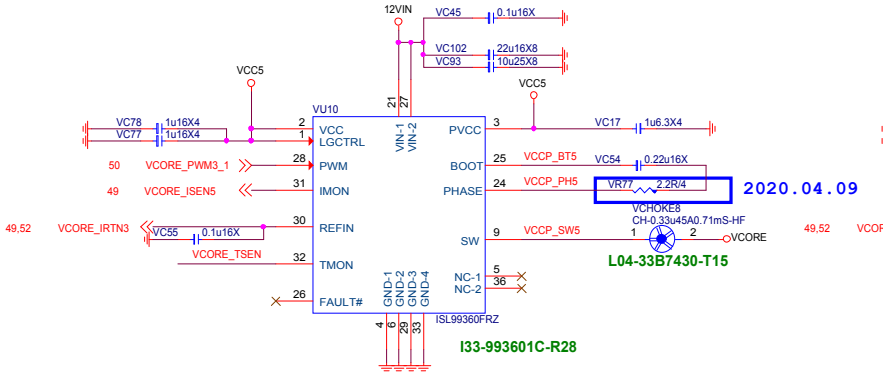




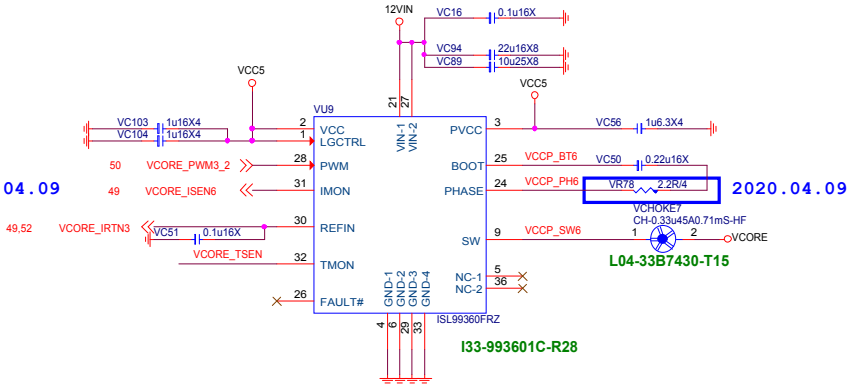
MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: CPU Power Vocre Phase 1- 4	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 51 of 78	

Dr.MOS 5V Level

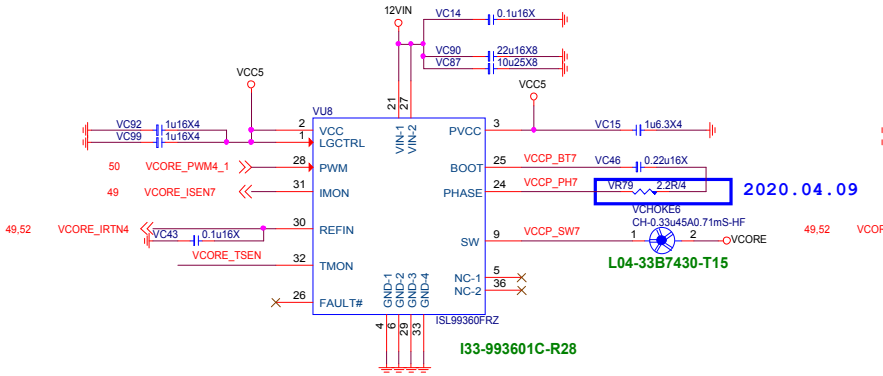
49,51 VCORE_TSEN <<< VCORE_TSEN



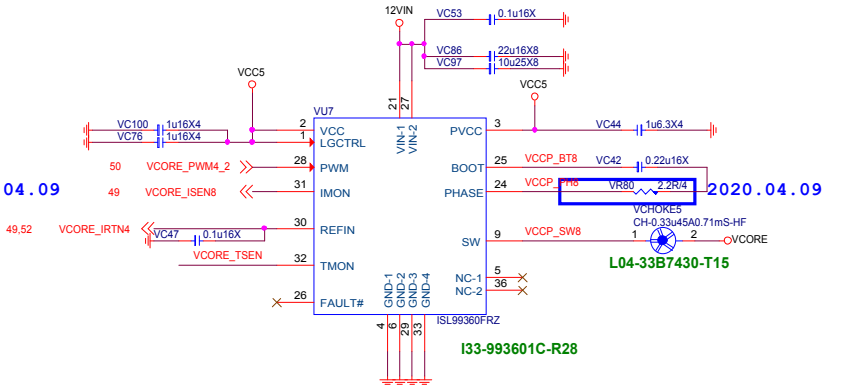
2020.04.09



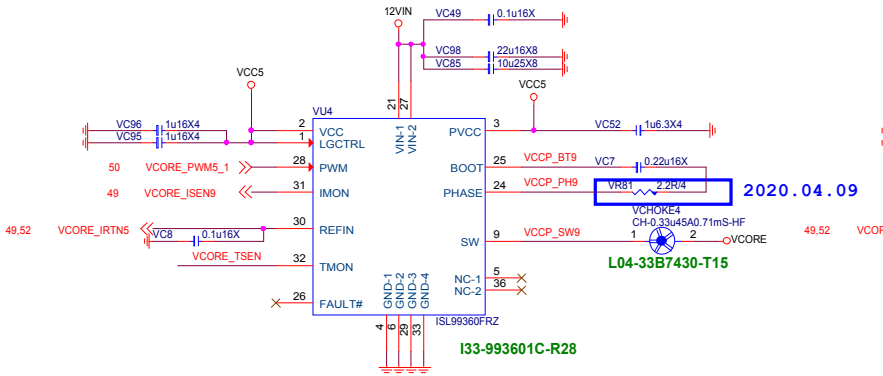
2020.04.09



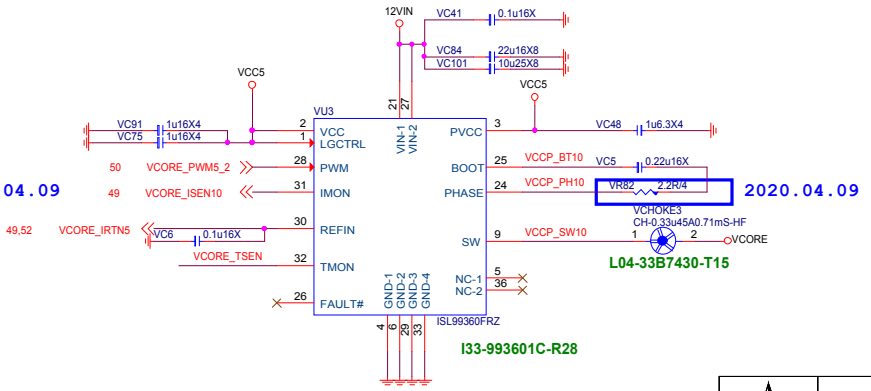
2020.04.09



2020.04.09



2020.04.09



2020.04.09

MICRO-STAR INT'L CO.,LTD

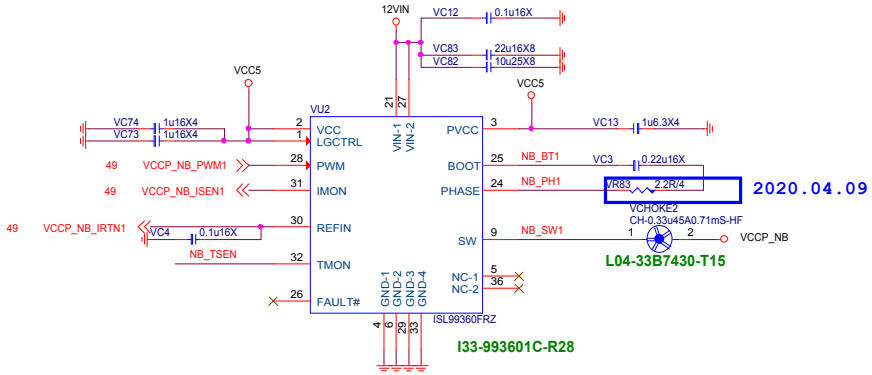
MS-7C91

Size	Document Description	Rev
Custom	CPU Power Vocre Phase 6 - 10	10

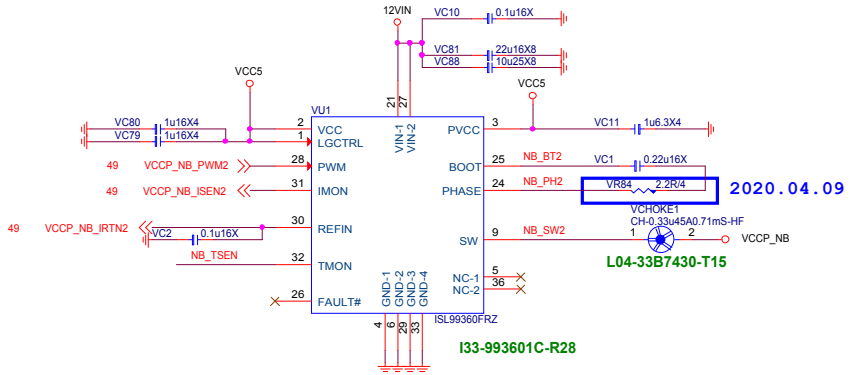
Date: Tuesday, April 21, 2020 Sheet 52 of 78

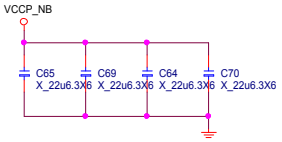
SOC EDC Max 75A

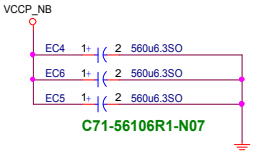
Dr.MOS 3.3V Level



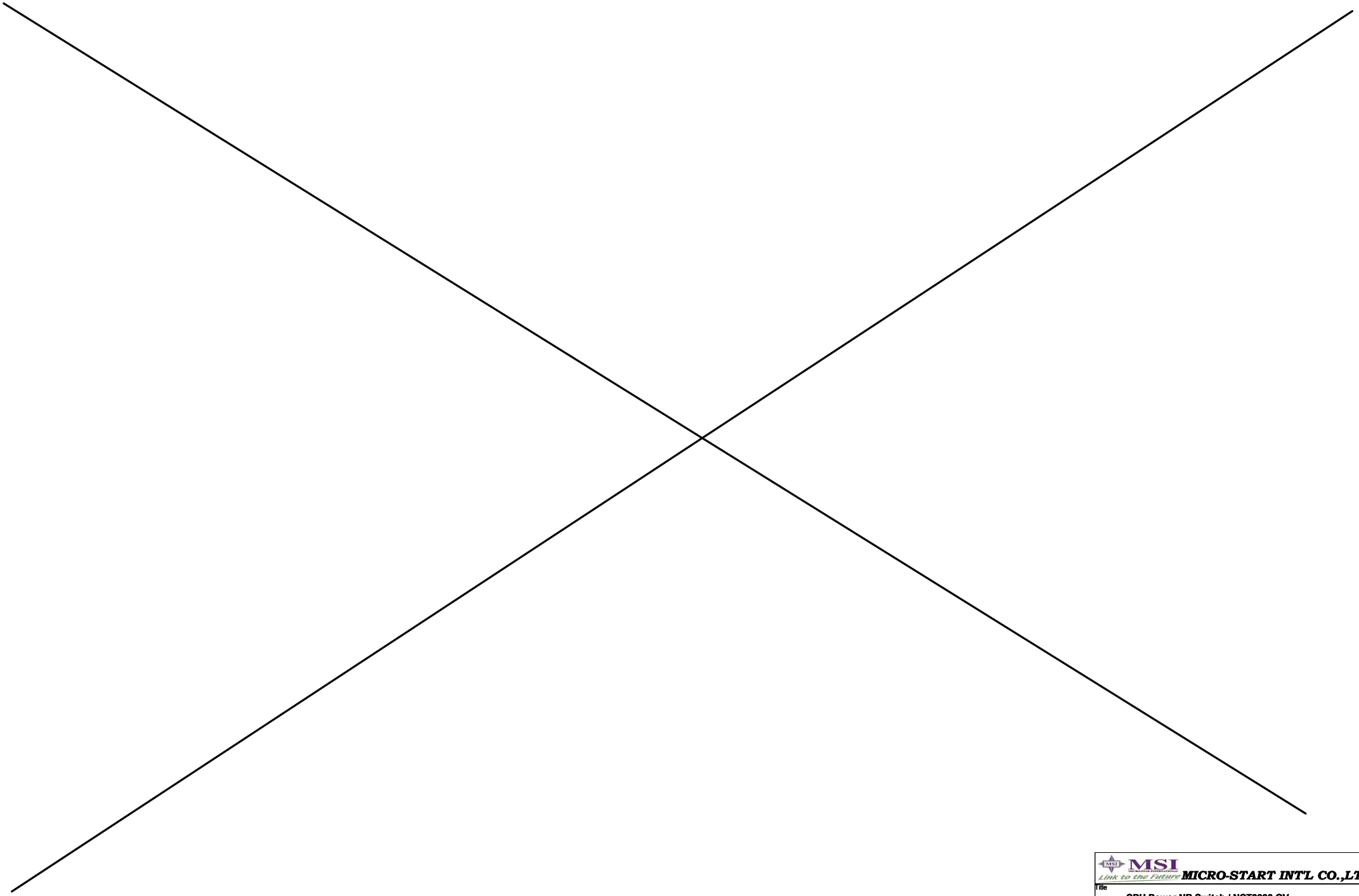
49 NB_TSEN NB_TSEN







MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: CPU Power NB Phase 1-2	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 53 of 78	



MSI MICRO-STAR INTERNATIONAL
Link to the Future
MICRO-START INT'L CO.,LTD.

Title: CPU Power NB Switch / NCT3933 OV		
Size: Custom	Document Number: MS-7C51	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 54 of 78	

CPU 1.8V S5

CPU 1.8V_S5@0.5A
CPU_VDDP_S5@1A
AUDIO1.8V@0.25A

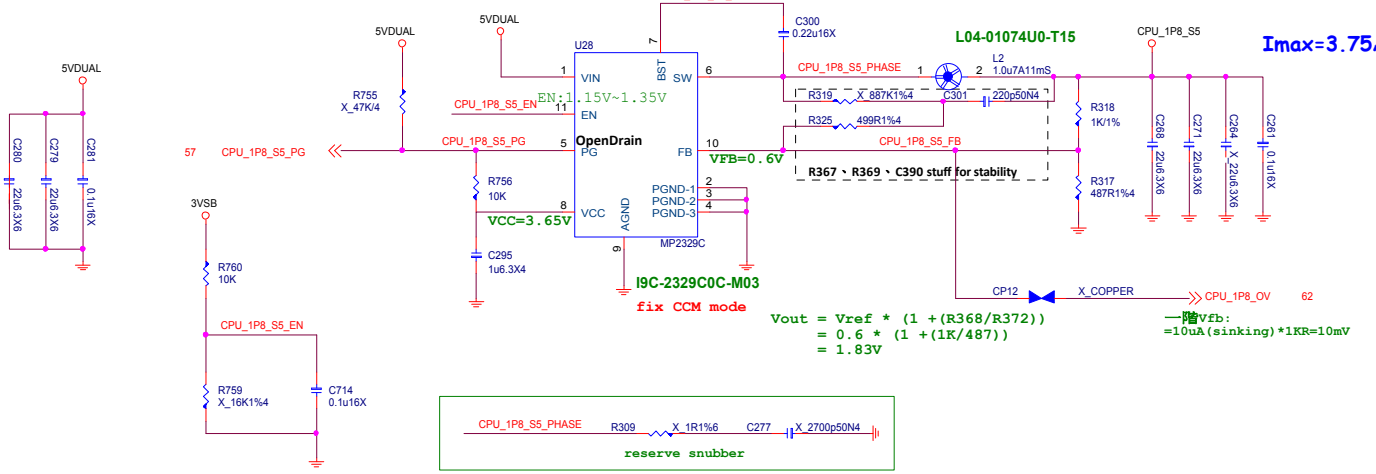
Continuous Conduction Mode (CCM)

Input Current = (6.5A*1.8V)/5V/0.8 = 3A

CPU_1P8_BST、CPU_1P8_BST_R >50 mils.

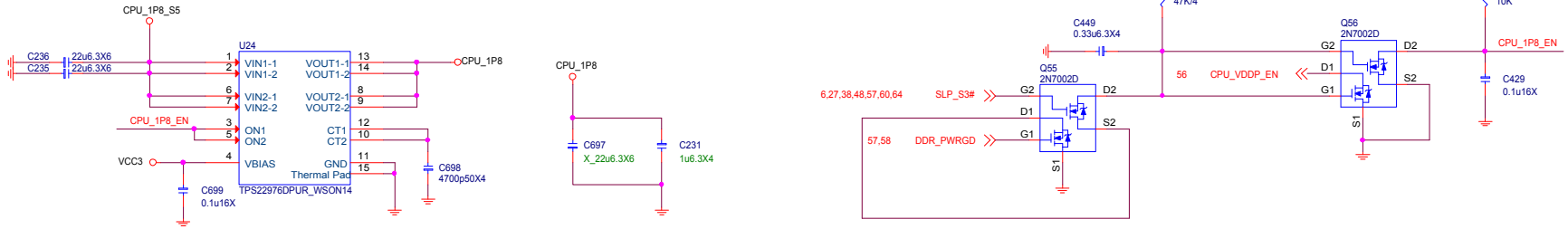
OCP = 6.5A

Imax=3.75A(S5+S0)

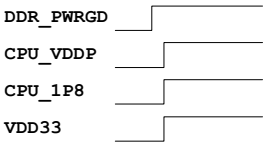


CPU 1.8V S0

CPU 1.8V_S0@2A



Adijustable Rise Time
SR = 0.42*CT+66
SR is the slew rate in (μs/V)
CT is constant value on CT pin (in pF)
The units for the constant 66 is in (μs/V)

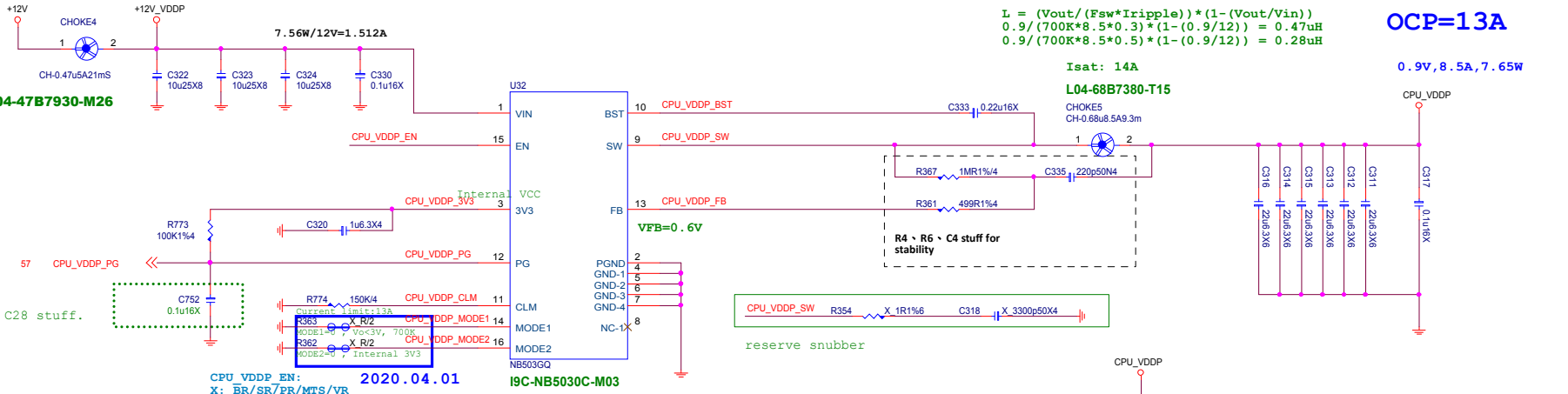


MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: CPU Power 1.8_S0 / S5	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 55 of 78	

CPU_VDDP_S0

0.9V@S0:8.5A

```
Input Current = (13A*0.9V)/12V/0.8 = 1.22A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A
```




```
L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
0.9/(700K*8.5*0.3)*(1-(0.9/12)) = 0.47uH
0.9/(700K*8.5*0.5)*(1-(0.9/12)) = 0.28uH
```

OCP=13A

Isat: 14A

L04-68B7380-T15

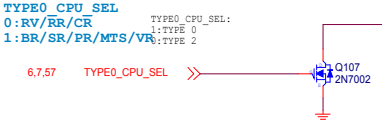
0.9V,8.5A,7.65W

```
20180822
fix PG glitch when VCC3 ramp up, C28 stuff.
```

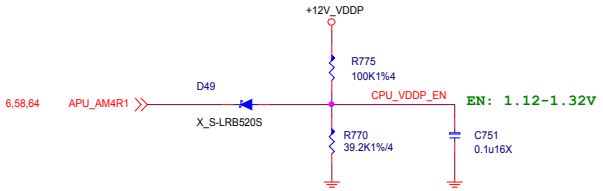
CPU_VDDP_EN:
X: BR/SR/PR/MTS/VR
O: RV/RR/CR

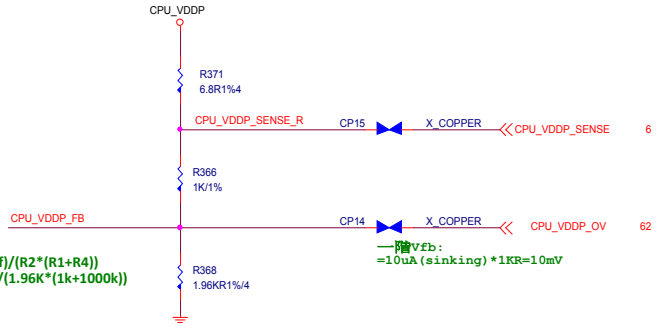
2020.04.01

TYPE0_CPU_SEL
0:RV/RR/CR
1:BR/SR/PR/MTS/VR



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	SPEC no Support
NA	X	0	0
SR	2	CPU VDDP NOT SUPPORT TYPE2	
RV/ZP	3	1	0
MTS	4	CPU VDDP NOT SUPPORT TYPE4	
RR	5	1	0
VM	6	CPU VDDP NOT SUPPORT TYPE6	
CR	7	1	0

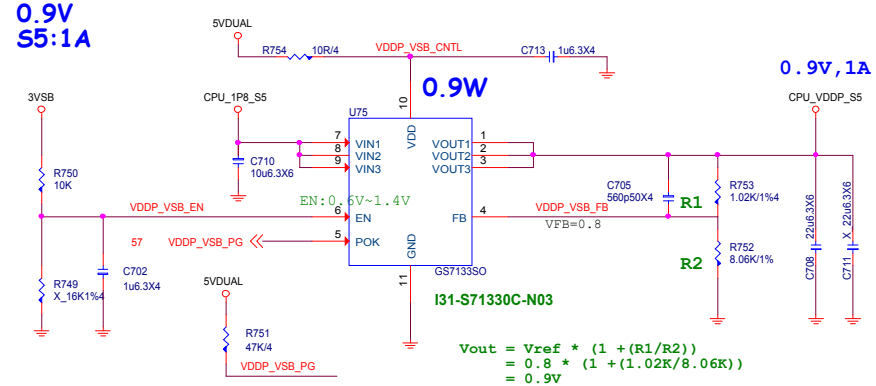





```
Vout = Vref + (R1*R4*Vref)/(R2*(R1+R4))
     = 0.6+(1k*1000k*0.6)/(1.96K*(1k+1000k))
     = 0.9058V
```

CPU_VDDP_S5

0.9V
S5:1A




```
Vout = Vref * (1 +(R1/R2))
     = 0.8 * (1 +(1.02K/8.06K))
     = 0.9V
```

MICRO-STAR INT'L CO.,LTD

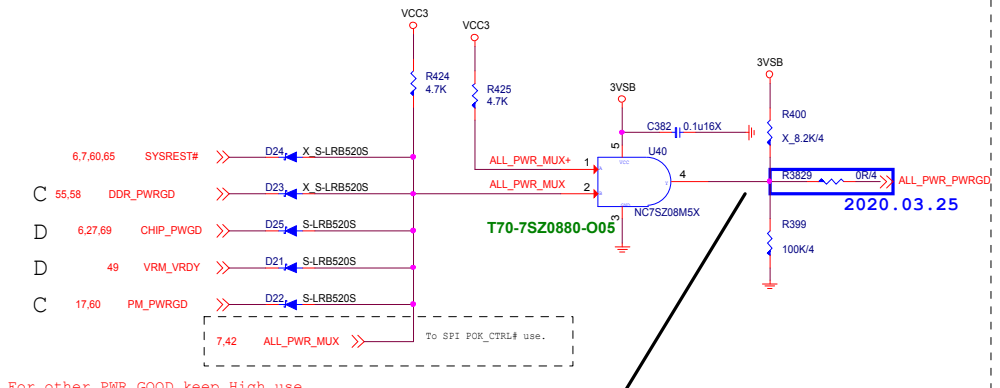
MS-7C91

Size	Document Description	Rev
Custom	CPU Power VDDP - NB503	10

Date: Tuesday, April 21, 2020 | Sheet 56 of 78

ALL POWER GOOD MUX

S0 PG



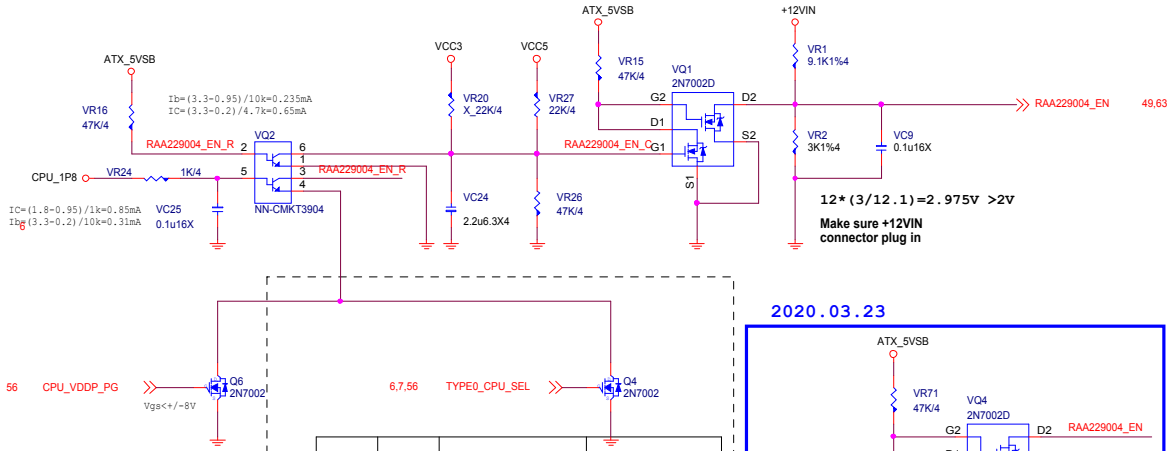
For other PWR_GOOD keep High use

When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

VRM_Enable circuit

2020.03.23

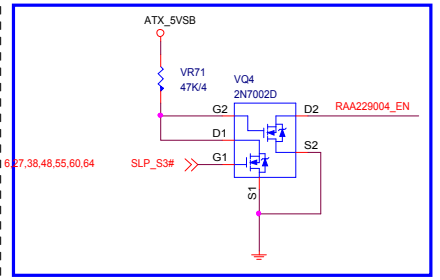
D2 Removed



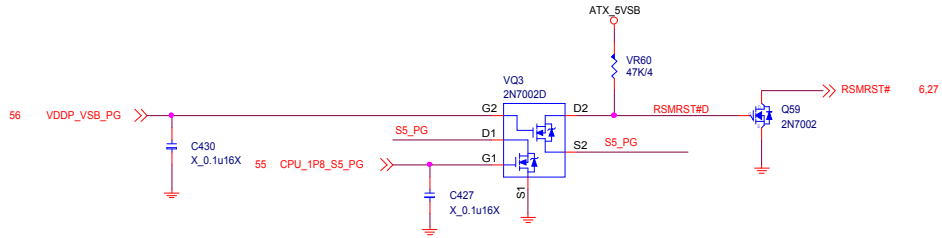
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	CPU VDDP1 NOT SUPPORT TYPE2	
RV/ZP	3	1	0
MTS	4	CPU VDDP1 NOT SUPPORT TYPE4	
RR	5	1	0
VM	6	CPU VDDP1 NOT SUPPORT TYPE6	
CR	7	1	0

SPEC no Support

2020.03.23



S5 PG



MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: VRM PWRGD	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 57 of 78	

DDR4_1.2V@28.7A

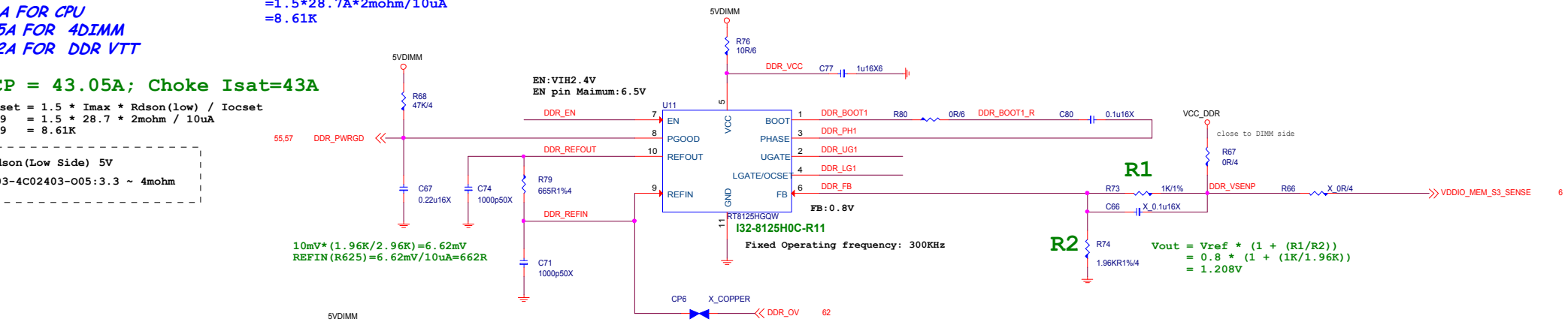
18A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT

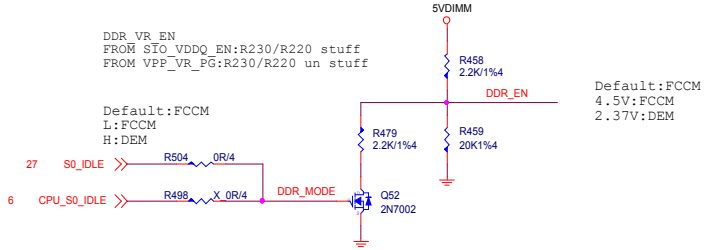
Rocset=1.5*Imax*Rdson(Low side)/Iocset
=1.5*28.7A*2mohm/10uA
=8.61K

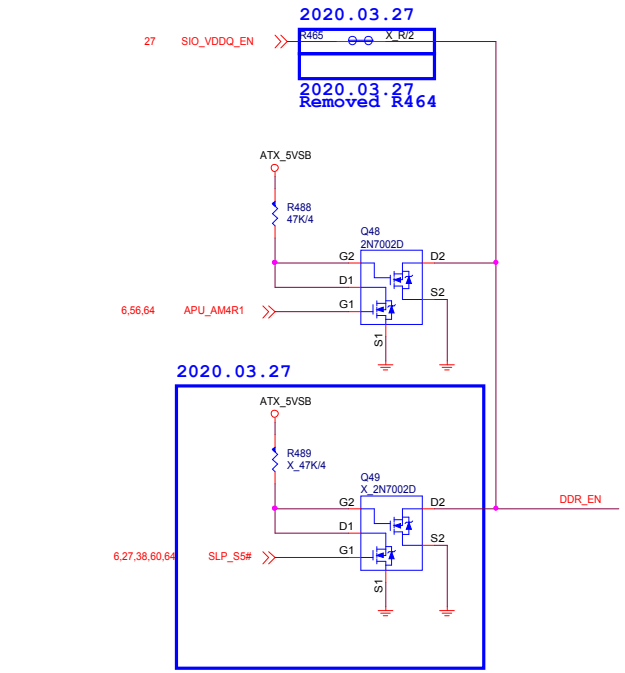
OCP = 43.05A; Choke Isat=43A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
R639 = 1.5 * 28.7 * 2mohm / 10uA
R639 = 8.61K

Rdson(Low Side) 5V
D03-4C02403-O05:3.3 ~ 4mohm

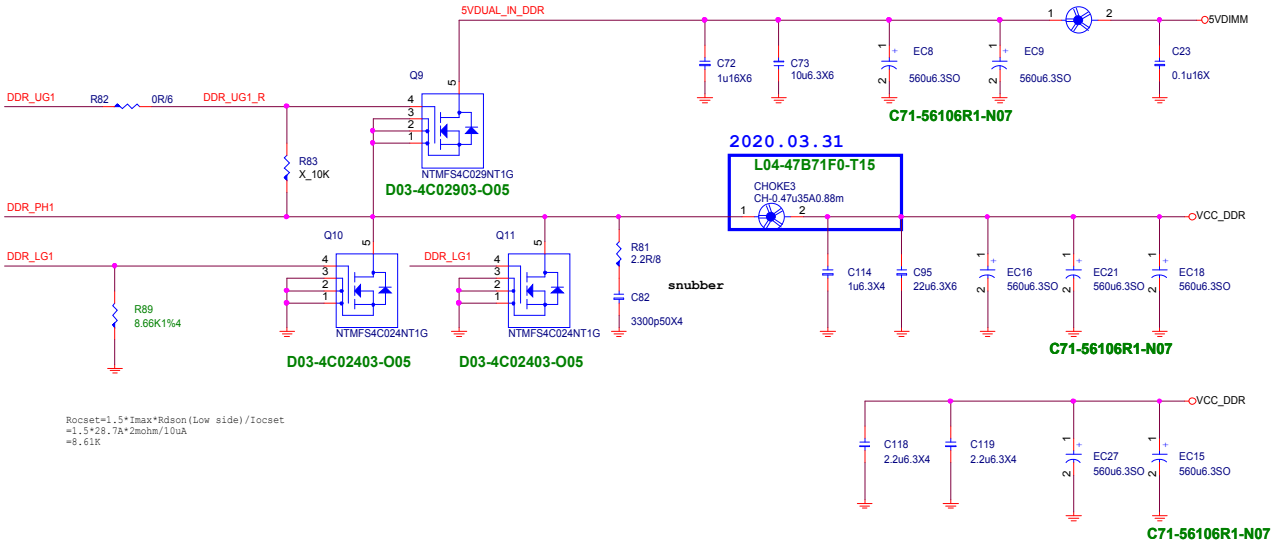






Input Current=(28.7*1.2)/5/0.8=8.61A

L04-68B7350-T15
CHOKE2 CH-0.68u15A5mS



Rocset=1.5*Imax*Rdson(Low side)/Iocset
=1.5*28.7A*2mohm/10uA
=8.61K

MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	DDR Power - 8125H	10

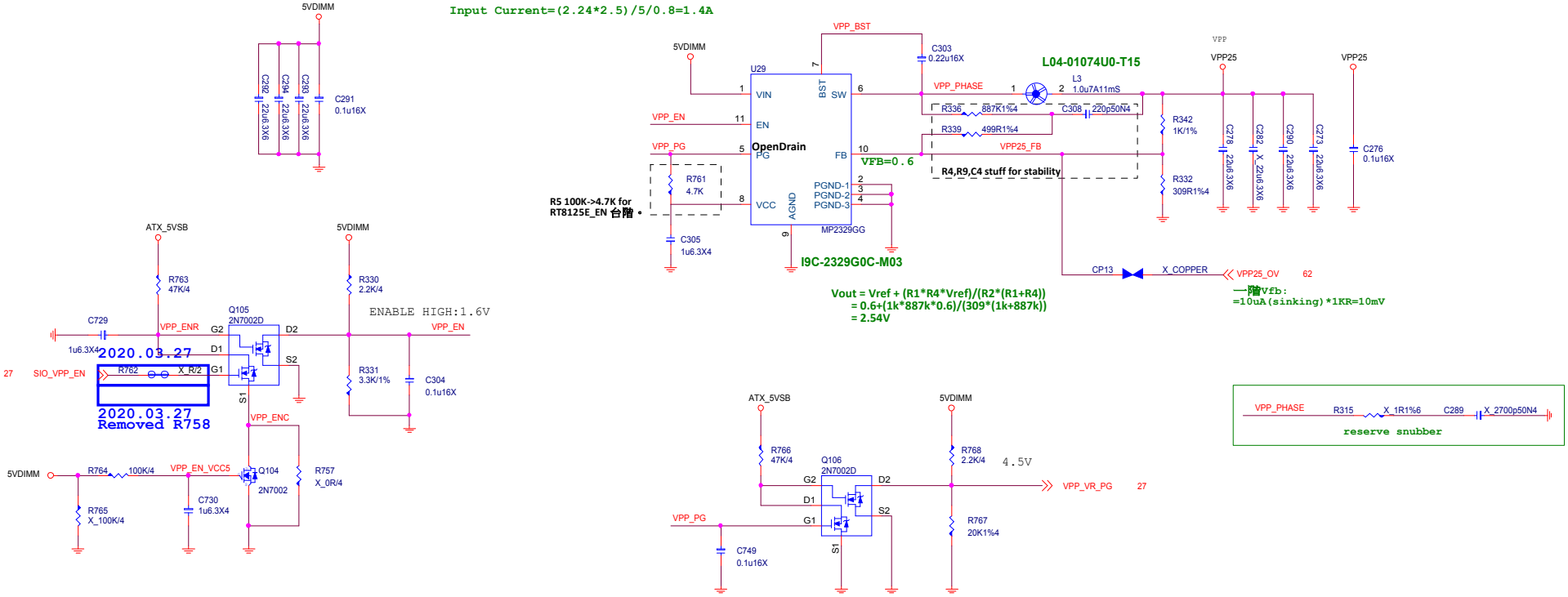
Date: Tuesday, April 21, 2020 Sheet 58 of 78

4DIMM : VPP25

2.5V@2.24A

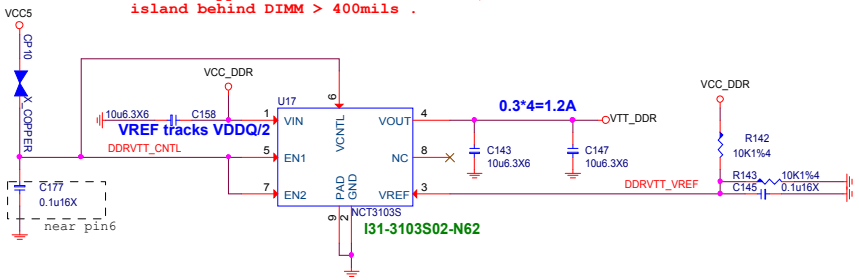
VPP_BST>50 mils.

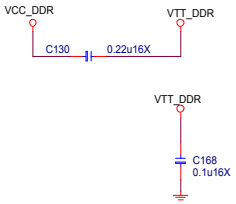
Input Current=(2.24*2.5)/5/0.8=1.4A



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .





MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: DDR VPP25 / VTT	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 59 of 78	

FOR Promontory 1.05V_S0

1.05V
S0:5.5A

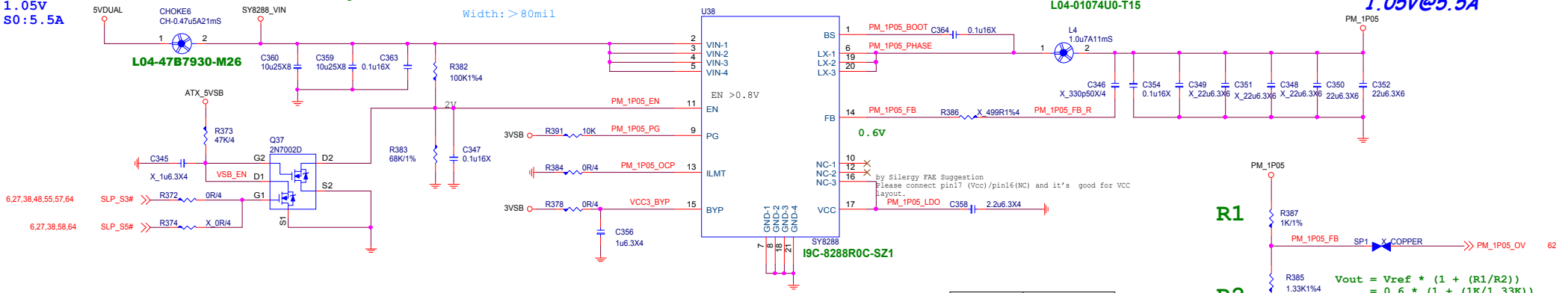
Input Current= (OCP8A*1.05V)/5V/0.8=2.1A

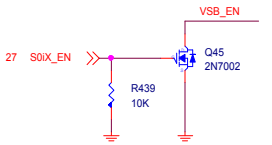
Width: > 80mil

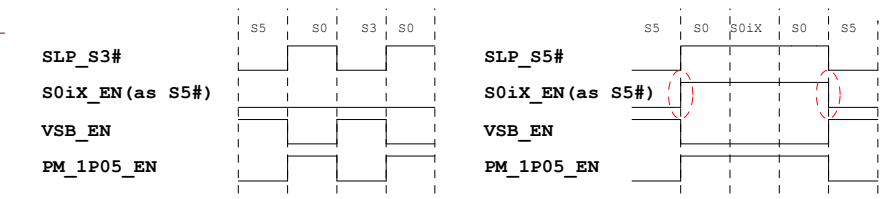
L04-47B7930-M26

L04-01074U0-T15

OCP=8A
1.05V@5.5A







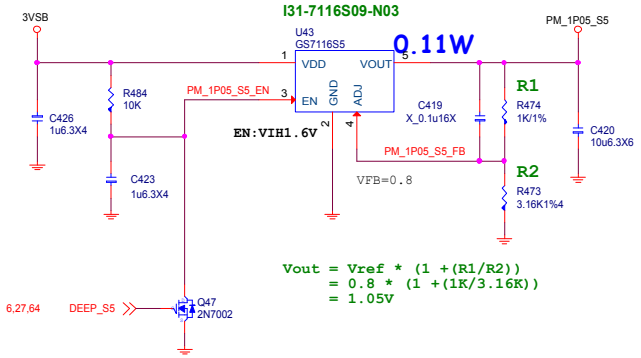
ILIMT	OCP
0	8A
floating	12A
1	16A

R1
R2

Vout = Vref * (1 + (R1/R2))
= 0.6 * (1 + (1K/1.33K))
= 1.051V

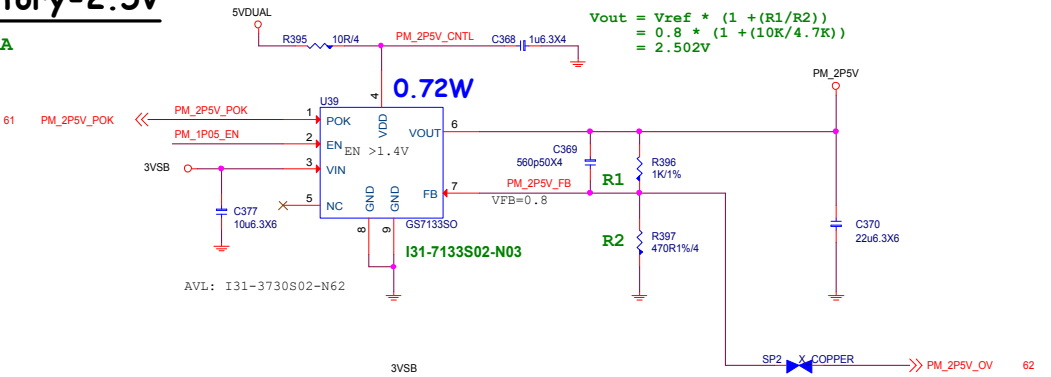
FOR PROM PM_1P05_S5

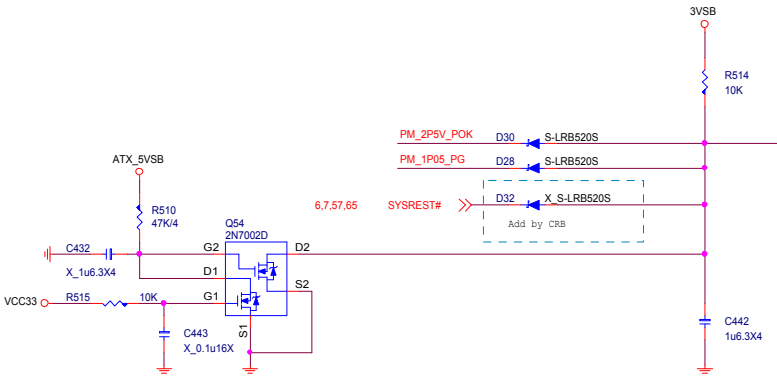
1.05V@0.05A

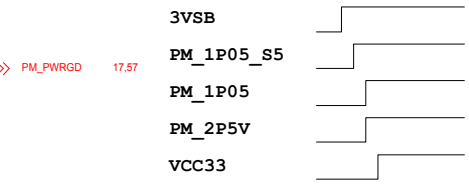


Promontory-2.5V

2.5V@900mA







MICRO-STAR INT'L CO.,LTD

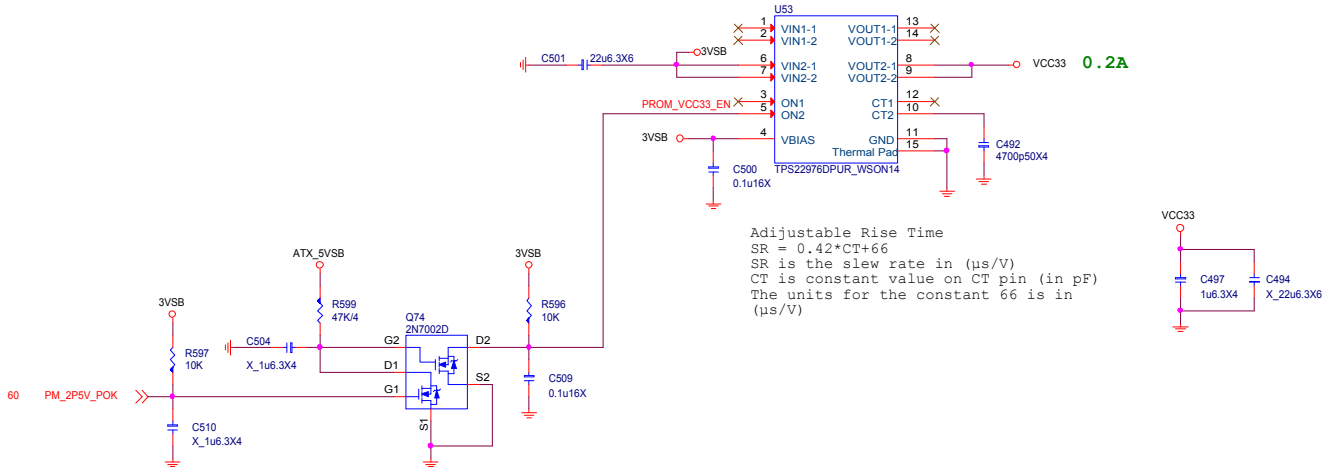
MS-7C91

Size	Document Description	Rev
Custom	PM - SY8288/PM_1P05/PM_2P5V	10

Date: Tuesday, April 21, 2020 Sheet 60 of 78

PROM VCC33

VCC33@0.2A



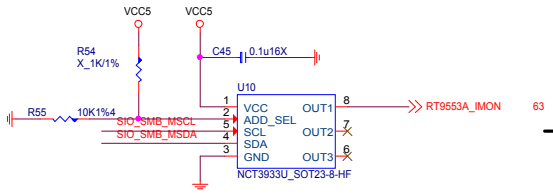
MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: PM - XXXXXXXX	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 61 of 78	

Over Voltage Control IC

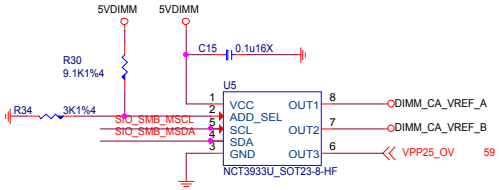
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

0x2A:RH=OPEN,RL=10K

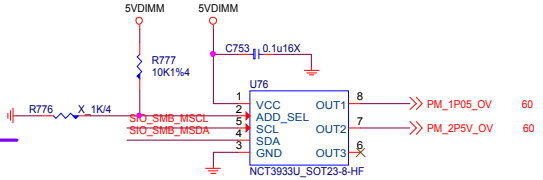


0x28:RH=9.1K,RL=3K

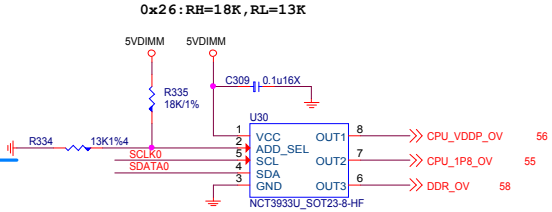


6,27,49 SIO_SMB_MSCL — SIO_SMB_MSCL
6,27,49 SIO_SMB_MSDA — SIO_SMB_MSDA

0x20:RH=10K,RL=OPEN



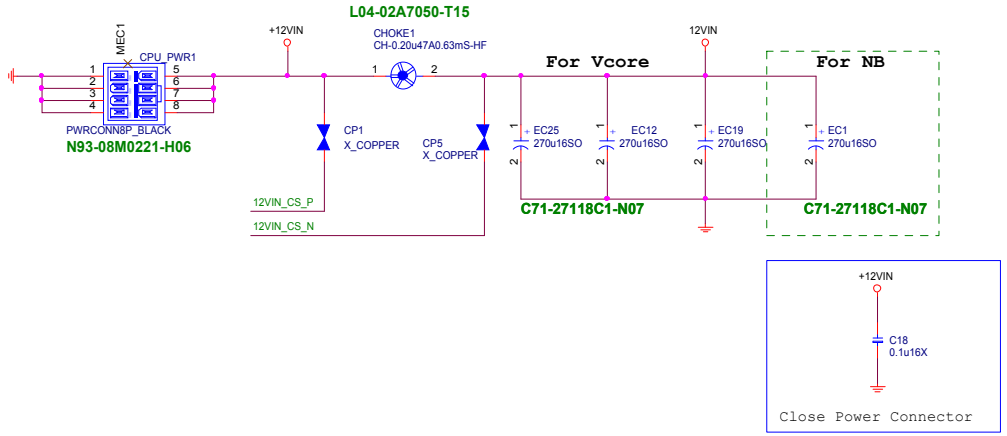
0x26:RH=18K,RL=13K



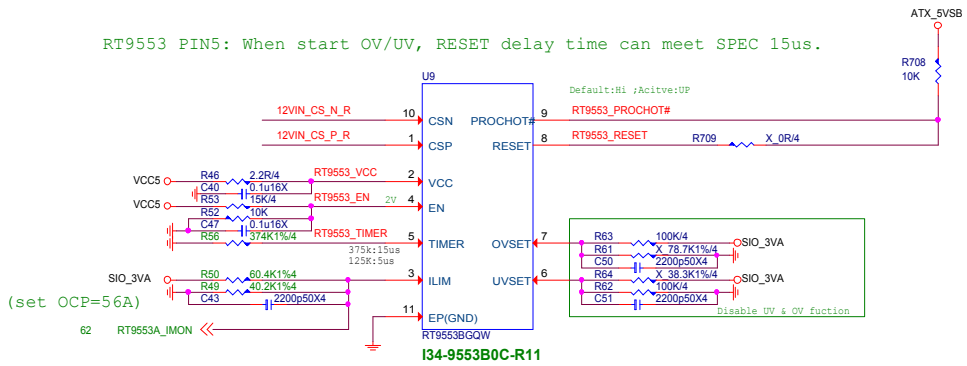
6,11,24 SCLK0 — SCLK0
6,11,24 SDATA0 — SDATA0

MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: OV Control - NCT3933	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 62 of 78	

CPU POWER CONNECTOR

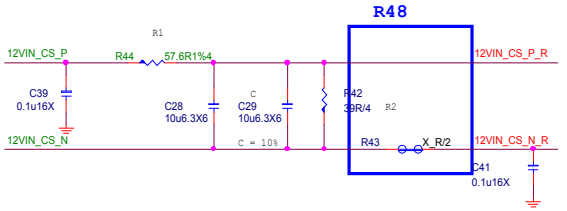


RT9553B CURRENT SENSE



2020.03.25

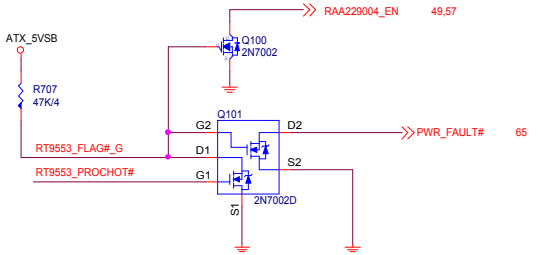
R48



$$\Delta VILIM = 10uA * [(60.4K * 40.2K) / (60.4K + 40.2K)] = 226mV$$

$$Isense = VILIM / 100 * Rsense$$

$$\Delta Isense = 226mV / 100 * 0.63m = 3.58A$$



Vcore			
D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	2	> output Vcore
D	=	0.166667	
I o = Icore(max)*0.8			
I core(max)	=	200	> Vcore current
I avg.	=	160	A
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	10	phase
I ripple	=	5.962848	A
How many pcs. Of Cap.			
I ripple(cap)	=	4700	m A
COE TEMP	=	1	
Input Cap.	=	2	pcs.

SOC			
D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.55	> output Vcore
D	=	0.129167	
I o = Icore(max)*0.8			
I core(max)	=	75	> Vcore current
I avg.	=	60	A
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	2	phase
I ripple	=	10.06153	A
How many pcs. Of Cap.			
I ripple(cap)	=	4700	m A
COE TEMP	=	1	
Input Cap.	=	3	pcs.

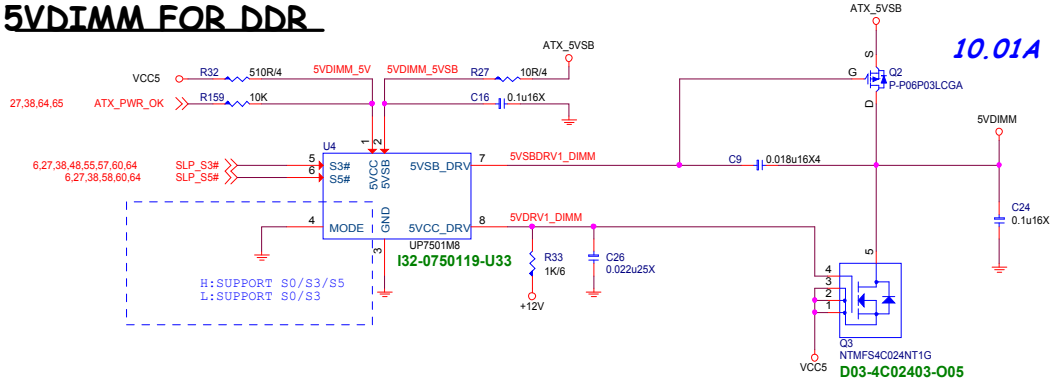
MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	OCP 12VIN - RT9533B	10

Date: Tuesday, April 21, 2020 Sheet 63 of 78

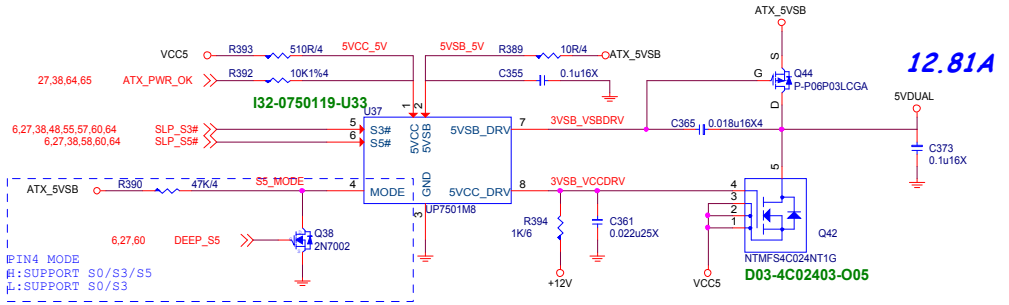
5VDIMM FOR DDR

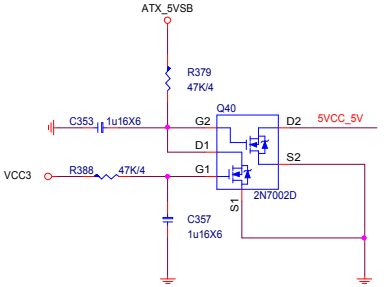


VCC_DDR=8.61A
VPP25=1.4A

5VDUAL For 3VSB/CPU1.8V/VDDP

LDOVDD=93.6mA
CPU_1P8_S5 VIN=3A
PM_1P05 VIN=2.1A
3VSB = 4.71A
LED_VCC5 = 3A



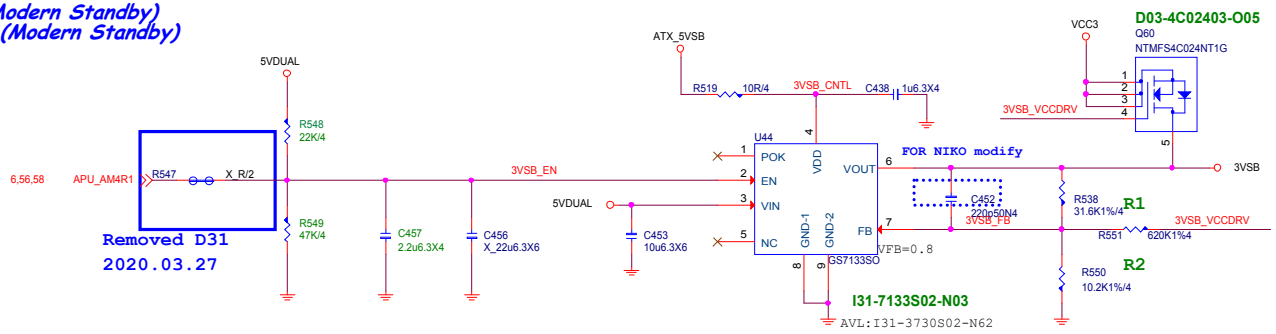


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

3VSB cost down

3.3V@4.305A

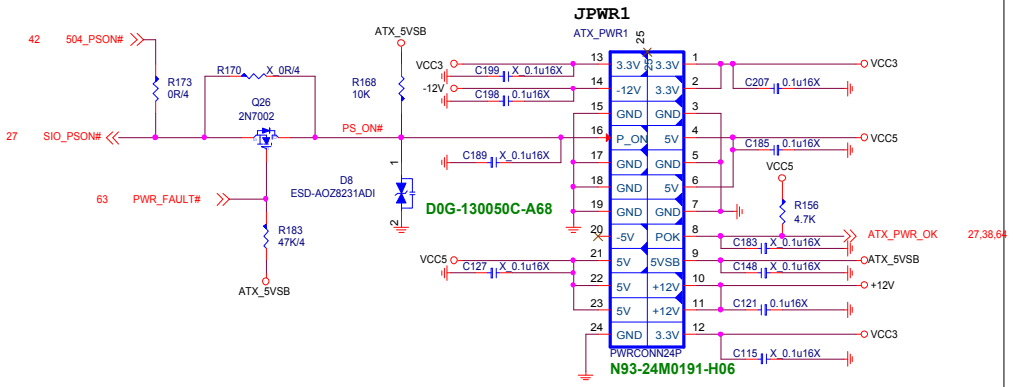
CPU:VDD_33_S5=0.25A
CHIP:VDD_33_S5=0.07A
PCIE=(375mA*5)=1.875A
M.2WIFI= 0.78A
RT8111H LAN=0.18A
PM_1P05_S5 :0.05A
PM_2P5V :0.9A(Modern Standby)
PCH VCC33 :0.2A(Modern Standby)

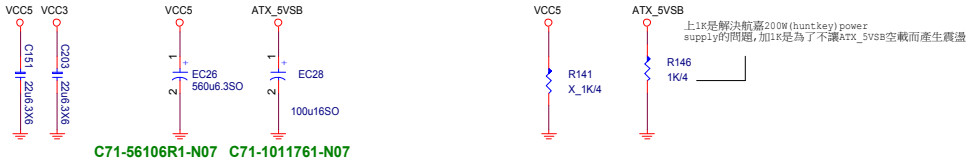


Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(31.6K/10.2K))
= 3.328V

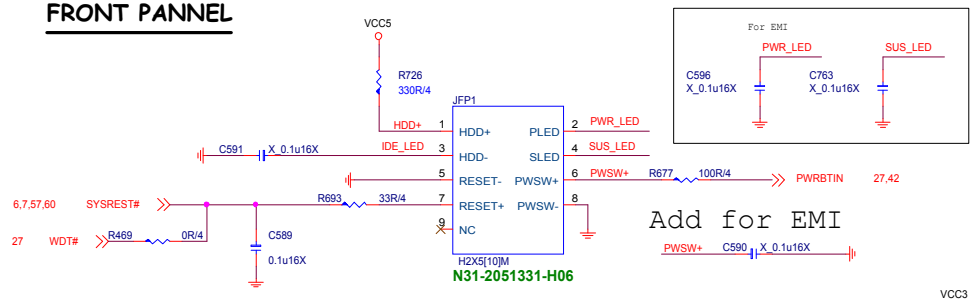
MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: ACPI - 5VDIMM / 3VSB	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 64 of 78	

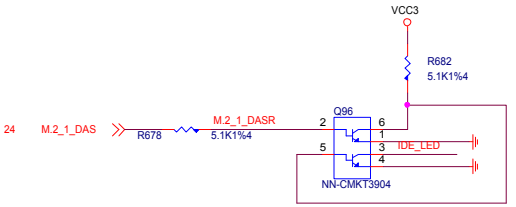
ATX POWER CONNECTOR

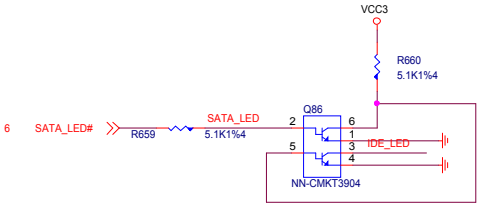


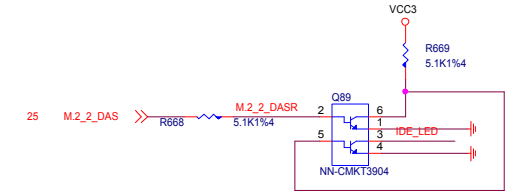


FRONT PANNEL



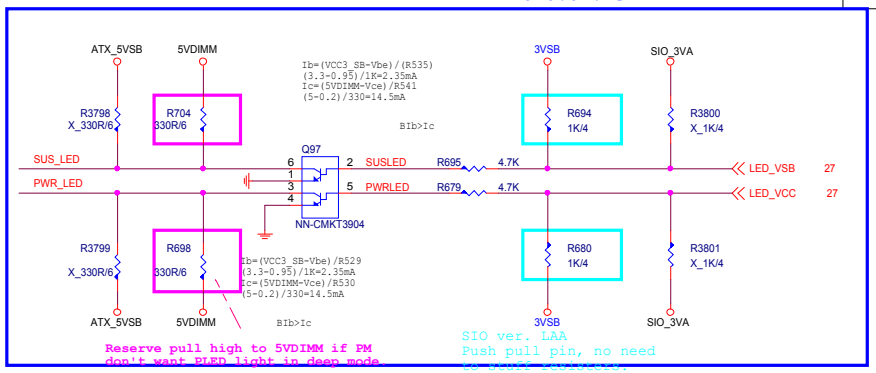


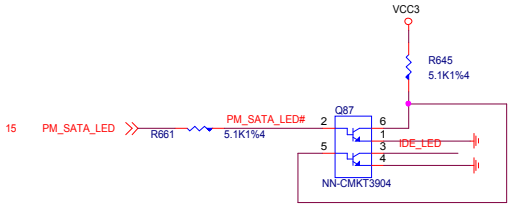


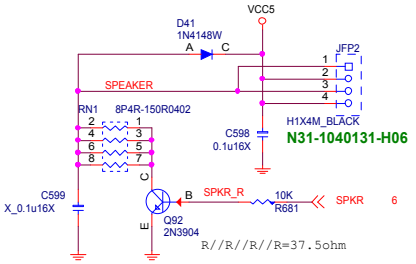


LED (for NCT6687D-R)

2020.04.13



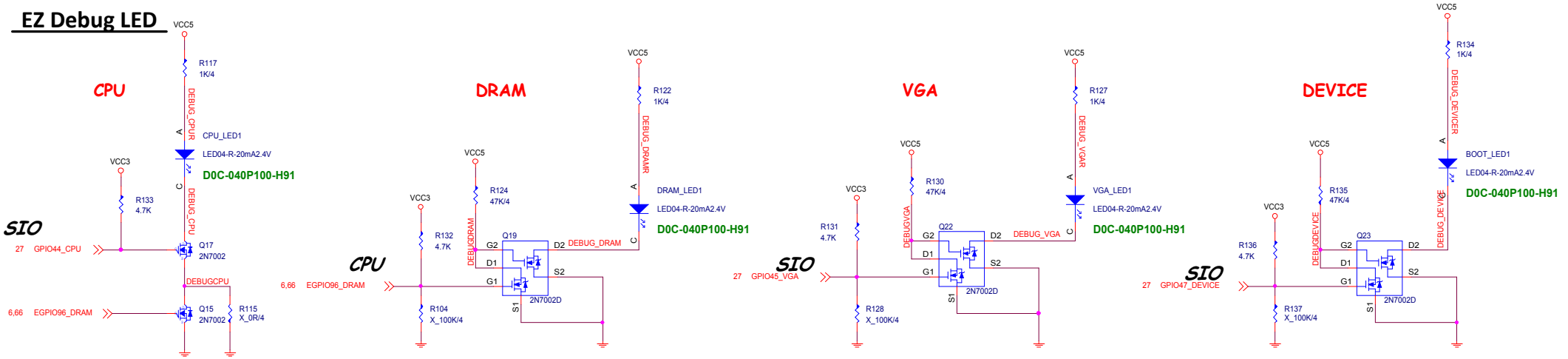




Voltage Mearsure Point

MSI	MICRO-STAR INT'L CO.,LTD		
	MS-7C91		
	Size: Custom	Document Description: ATX power - FrontPanel / EMI	Rev: 10
	Date: Tuesday, April 21, 2020	Sheet 65 of 78	

EZ Debug LED



LED GPIO	GPIO44	EGPIO96	GPIO45	GPIO47
亮	OPEN-Drain	GPO LOW	GPO LOW	GPO LOW
滅	GPO LOW	GPO HIGH	OPEN-Drain	OPEN-Drain

default Input

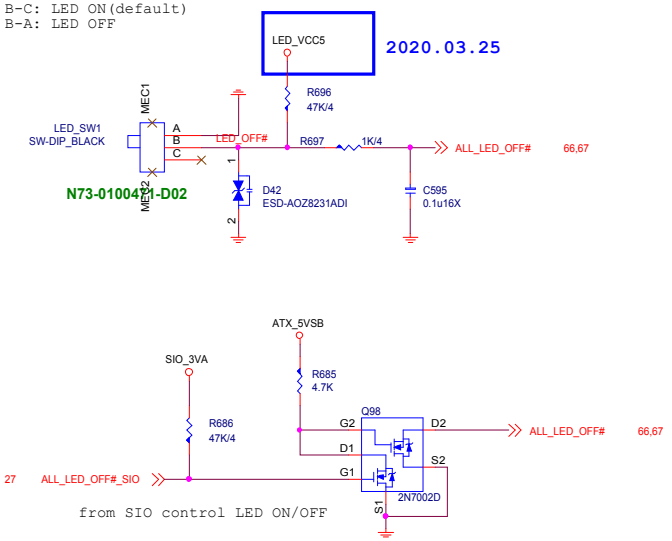
LED亮燈時同時將CPU LED關掉

LED_SW1 FORM SIO

D0C-040P100-H91/D0C-040S500-E07

LED_SW1 for ALL LED OFF

B-C: LED ON(default)
B-A: LED OFF



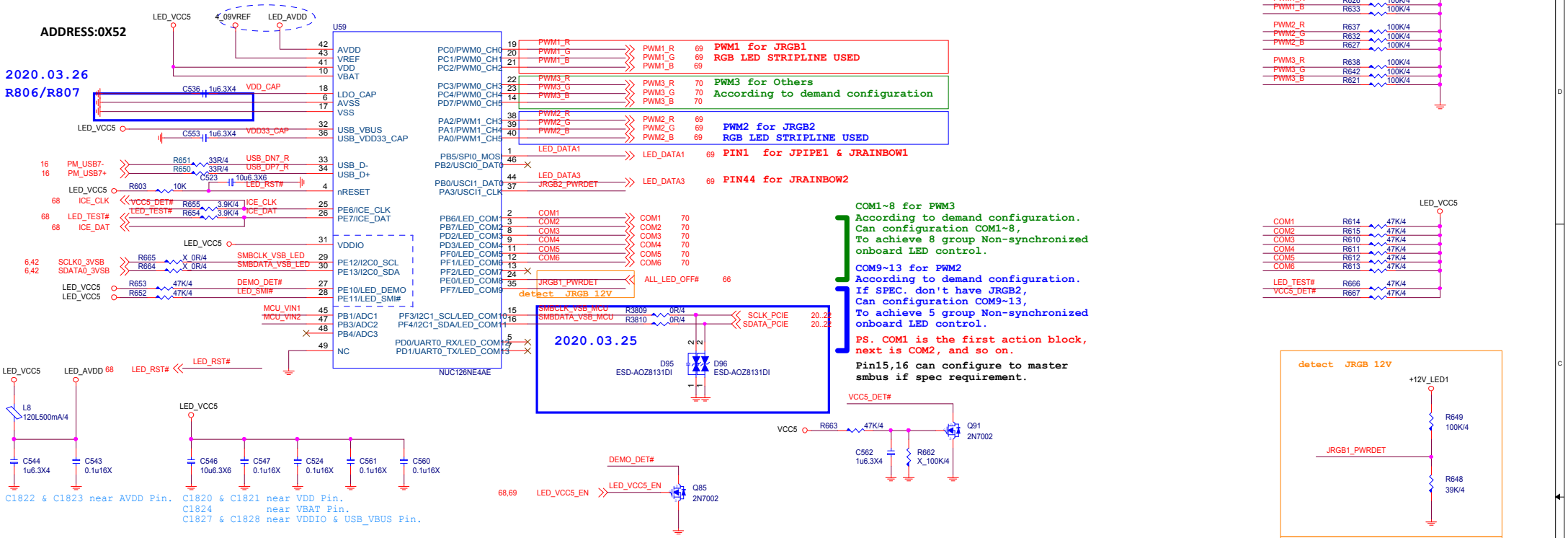
MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: LED - EZ DEBUG / AMP
Rev: 10	
Date: Tuesday, April 21, 2020	Sheet 66 of 78

48 PIN LED MCU

If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.

ADDRESS:0X52

2020.03.26
R806/R807



COM1~8 for PWM3
According to demand configuration.
Can configuration COM1~8,
To achieve 8 group Non-synchronized onboard LED control.

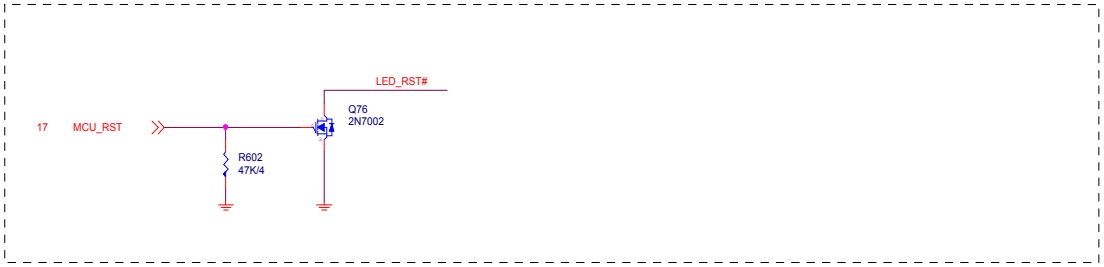
COM9~13 for PWM2
According to demand configuration.
If SPEC. don't have JRGB2,
Can configuration COM9~13,
To achieve 5 group Non-synchronized onboard LED control.

PS. COM1 is the first action block, next is COM2, and so on.

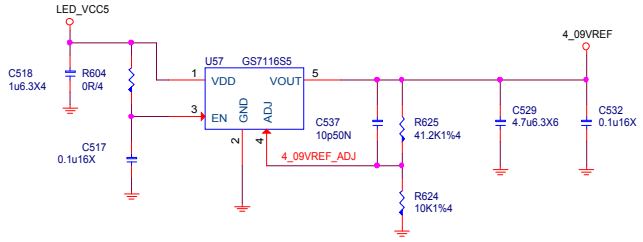
Pin15,16 can configure to master smbus if spec requirement.

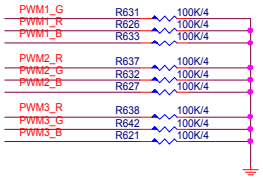
C1822 & C1823 near AVDD Pin. C1820 & C1821 near VDD Pin.
C1824 near VBAT Pin.
C1827 & C1828 near VDDIO & USB_VBUS Pin.

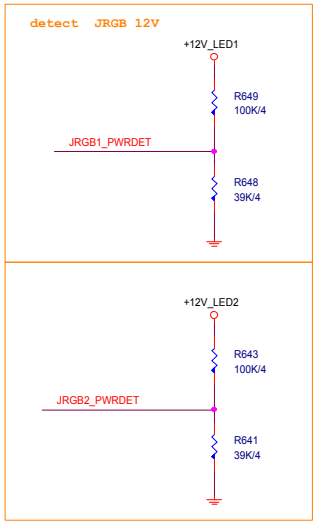
Clear MCU Circuit

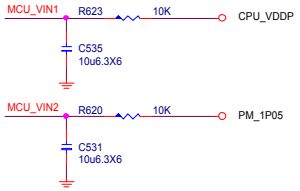


Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2



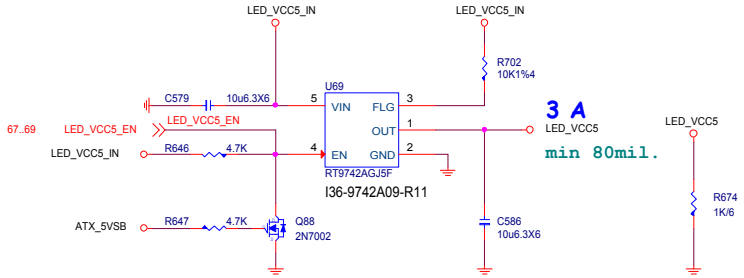


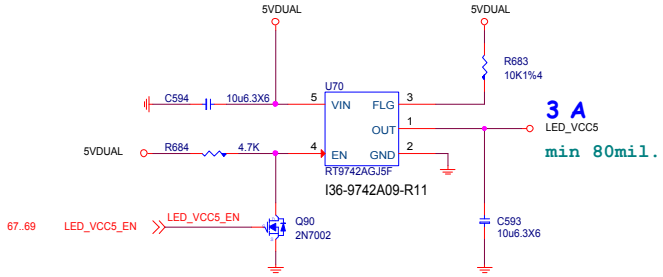




MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: MCU - LED Control	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 67 of 78	

EXTERNAL POWER INPUT

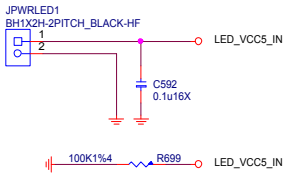




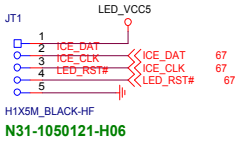
External Power

2A Connector

N32-1020CB1-H06

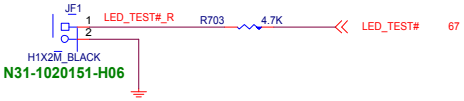


JT1 for FW update



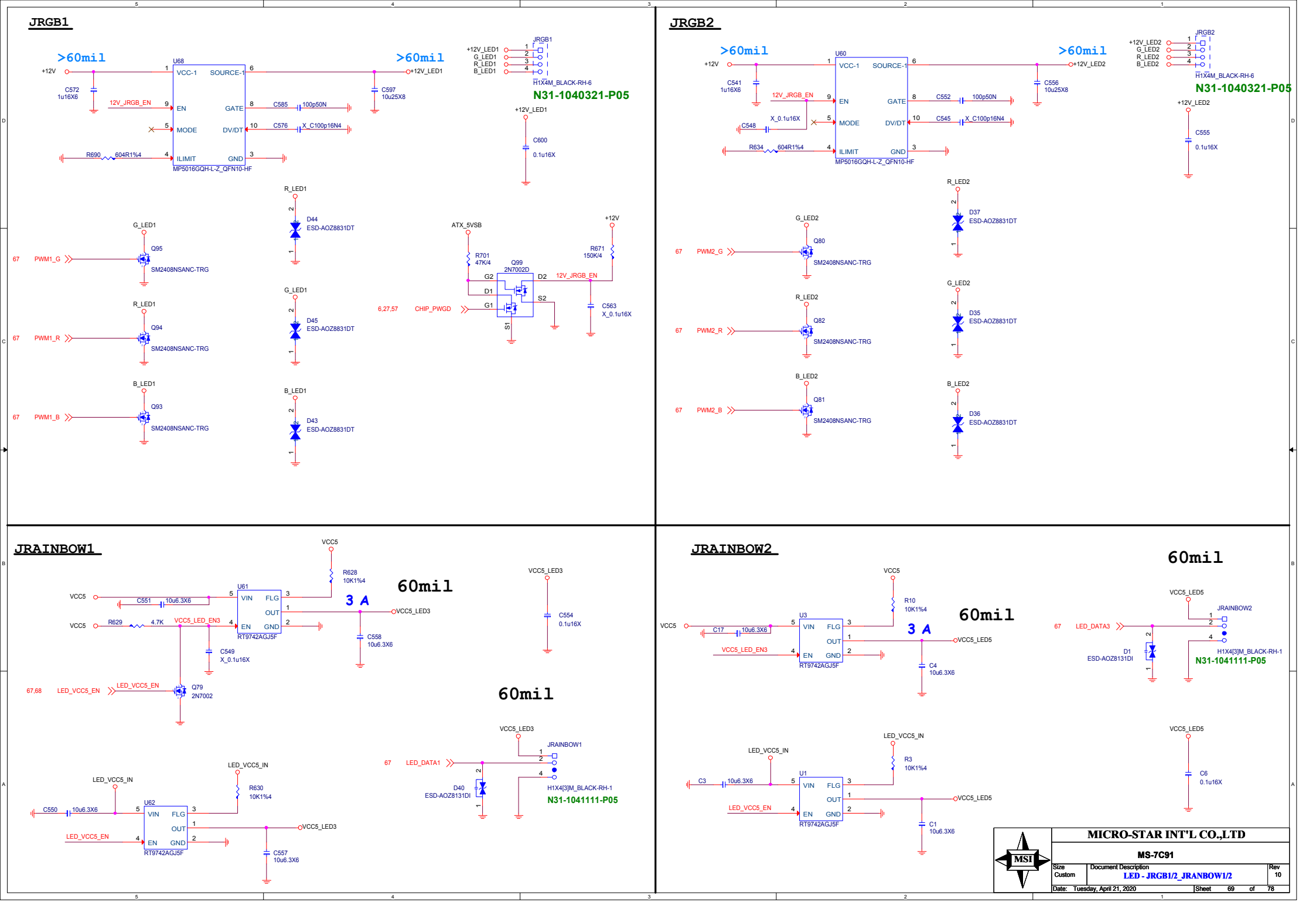
N31-1050121-H06

JF1 for Factory test

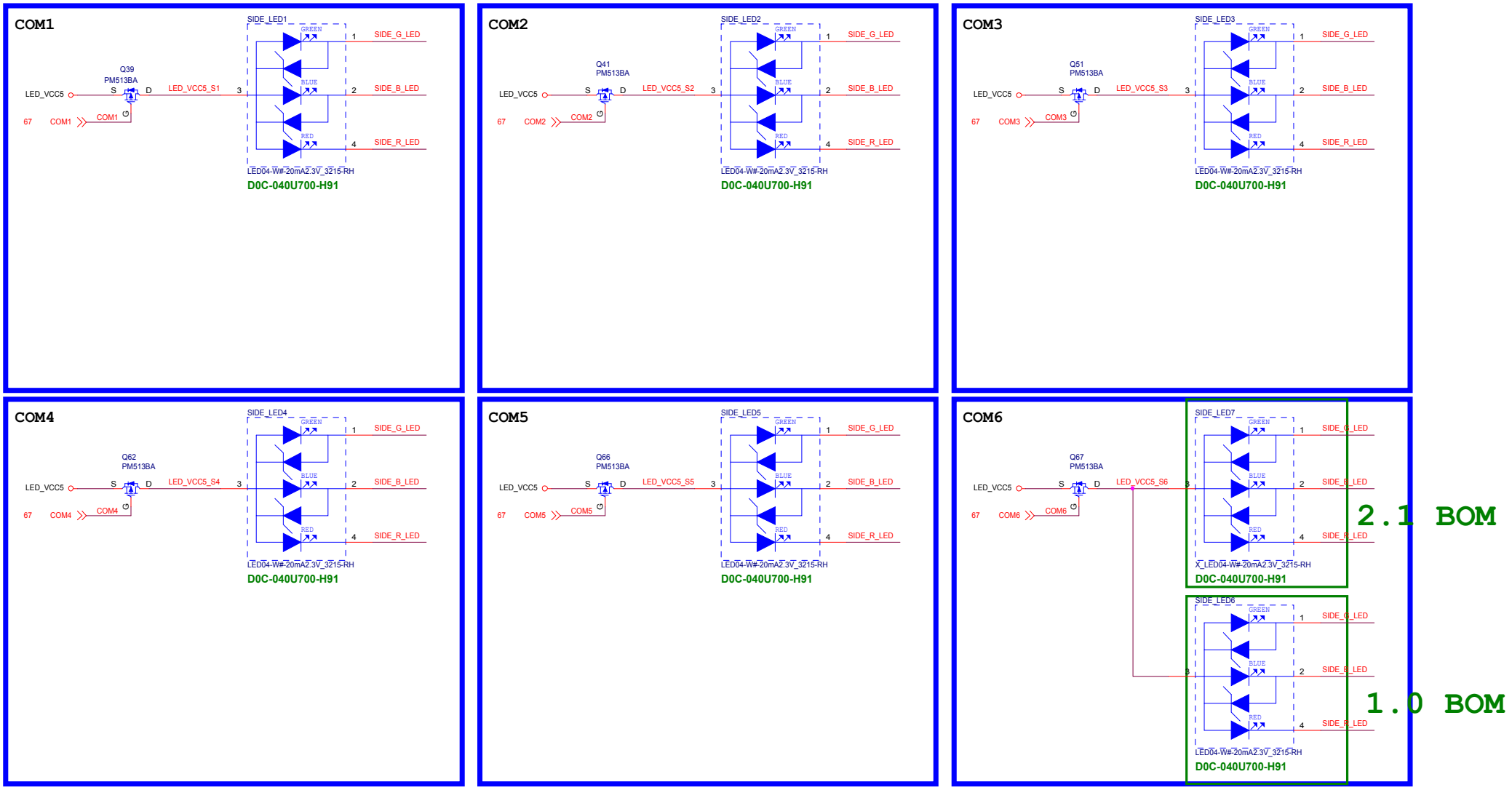


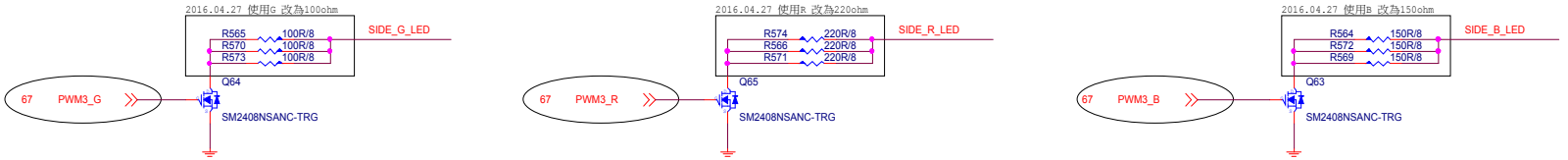
N31-1020151-H06

MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size: Custom	Document Description: LED - Power / JPIPE	Rev: 10
Date: Tuesday, April 21, 2020	Sheet 68 of 78	


JRGB1
>60mil
U68
VCC-1
SOURCE-1
EN
GATE
MODE
DV/DT
ILIMIT
GND
MP5016GQH-L-Z_QFN10-HF
+12V
+12V_LED1
12V_JRGB_EN
C572
1u16X6
C597
10u25X8
C585
100p50N
C576
X_C100p16N4
R690
604R1%4
C600
0.1u16X
JRGB1
H1X4M_BLACK-RH-6
N31-1040321-P05
R_LED1
G_LED1
B_LED1
D44
D45
D43
ESD-AOZ8831DT
Q95
Q94
Q93
SM2408NSANC-TRG
PWM1_G
PWM1_R
PWM1_B
67
ATX_5VSB
R701
47K/4
Q99
2N7002D
G2
D1
G1
D2
S2
S1
12V_JRGB_EN
R671
150K/4
C563
X_0.1u16X
6,27,57
CHIP_PWGD
JRGB2
U60
+12V_LED2
C541
1u16X6
C556
10u25X8
C552
C545
C548
X_0.1u16X
R634
C555
D37
D35
D36
Q80
Q82
Q81
PWM2_G
PWM2_R
PWM2_B
JRAINBOW1
U61
VIN
FLG
OUT
EN
GND
RT9742AGJ5F
VCC5
VCC5_LED3
VCC5_LED_EN3
C551
10u6.3X6
R629
4.7K
R628
10K1%4
3 A
60mil
C549
X_0.1u16X
C558
10u6.3X6
C554
0.1u16X
67,68
LED_VCC5_EN
Q79
2N7002
LED_VCC5_IN
U62
C550
R630
10K1%4
C557
10u6.3X6
JRAINBOW2
LED_DATA1
LED_DATA3
D40
D1
ESD-AOZ8131DI
H1X4[3]M_BLACK-RH-1
N31-1041111-P05
U3
U1
R10
R3
C17
C3
C4
C1
C6
VCC5_LED5
MICRO-STAR INT'L CO.,LTD
MS-7C91
Size
Custom
Document Description
LED - JRGB1/2_JRANBOW1/2
Rev
10
Date: Tuesday, April 21, 2020
Sheet 69 of 78

BOARD SIDE LED *6





MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: LED - Mystic Light - 1
Rev: 10	
Date: Tuesday, April 21, 2020	Sheet 70 of 78

MICRO-STAR INT'L CO.,LTD	
MS-7C91	
Size: Custom	Document Description: BOM Option
Rev: 10	
Date: Tuesday, April 21, 2020	Sheet 71 of 78

CPU Socket

CPU2

E95-0000022-A91

E95-0000022-A91

Simulation

X_JS1 — SIM1 — X_PIN1*2

X_JS2 — SIM2 — X_PIN1*2

X_JS3 — SIM3 — X_PIN1*2

FM2 FM3 FM1 FM4 FM5 FM6 FM8 FM7 — X_FM120

Optics Orientation Holes

MH1 MH2 MH3 MH5 MH6 MH4 MH7 MH8 MH9 — X_MH001

2020.04.15

C575 0.1u16X

C559 0.1u16X

MANUAL PART

AMI_LAB1 — G51-M1SPXXA-A09

G51-M1SPXXA-A09

CFOS1 <MSI-BOM> — Y02-MU00170-CFO

Y02-MU00170-CFO

HDMI_LA1 — Label — HDMI

HDMI LABEL

Y01-RHDMI03-000

MKT_LA1 — Label — MKT_LABEL

X_MKT LABEL

G51-M1SPP78-Q13

BAT1_X1

BAT-BCR2032P

AVL:
D06-0100161-F52
D06-0100101-K26

PCB

PCB

PCB1

7C91_21

PD0-07C9121-E48
PD0-07C9121-G37

Moat CAP

Reserve for bypass 12VIN noise use

ATX_5VSB — C5 C2 — X_0.1u16X

Reserve for bypass VCC5/VCC3/3VSB noise use

VCC5 — C1658 C1659 — X_0.1u16X

VCC3 — C1660 C1661 — X_0.1u16X

3VSB — C1662 — X_0.1u16X

2020.04.14

MOS HEATSINK

2020.04.15

N MOS

HS_MOS1 MEC2 MEC1

NHS-KWO GER(0436-3160R)

E31-0506810-K08

W MOS

HS_MOS2 MEC2 MEC1

WHS-KWO GER(0436-3150R)

E31-0506800-K08

PCH HEATSINK

2020.04.15

PM_HS1 MEC1 MEC2

PHS-KWO GER(0436-3161R)

E31-0410550-K08

M2 COVER

IO BRACKET

DDR COVER

20190201 Remove DDR_COVER1

MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	Manual Parts	10

Date: Tuesday, April 21, 2020 Sheet 72 of 78