AMD AM4

GAMING EDGE AC

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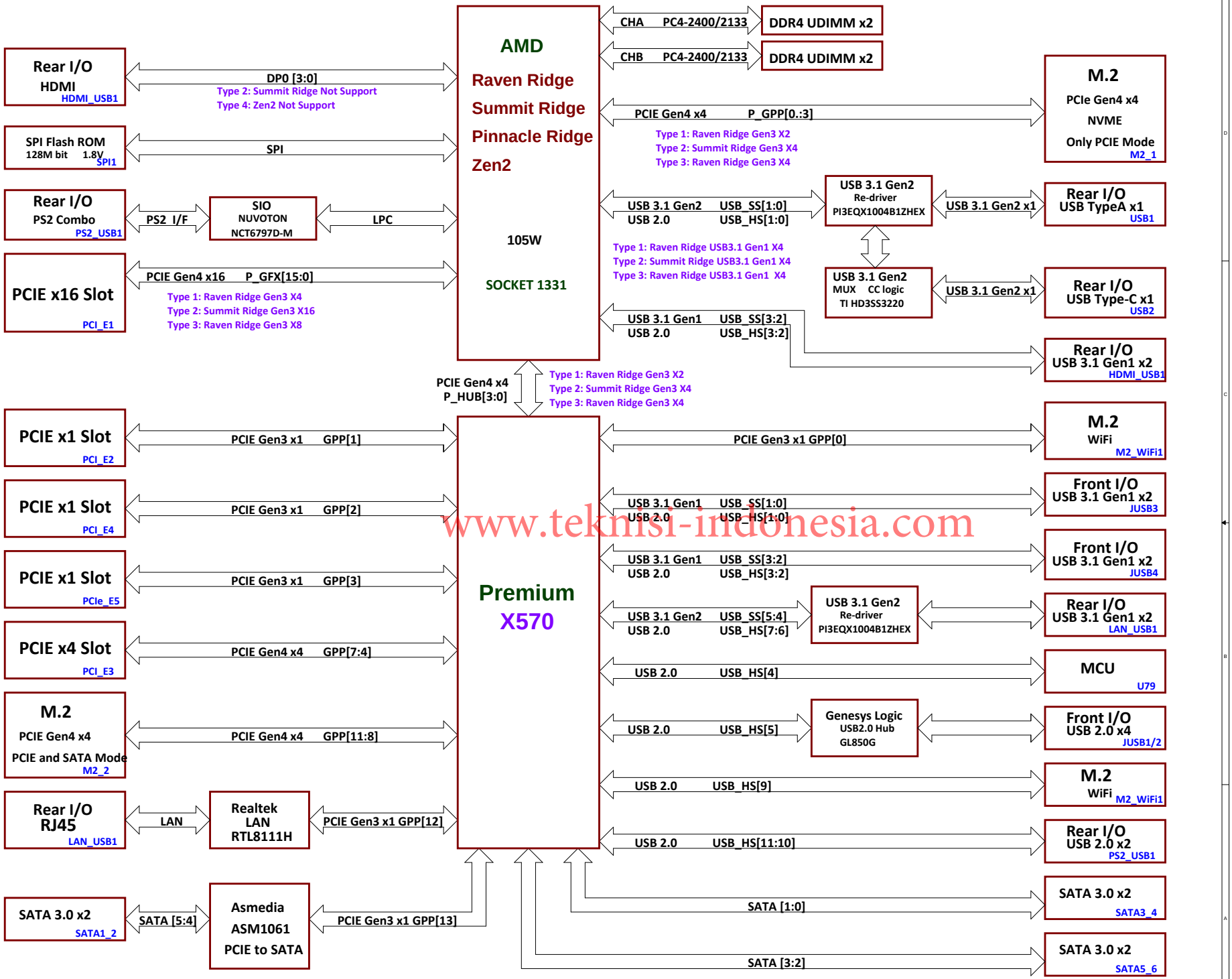

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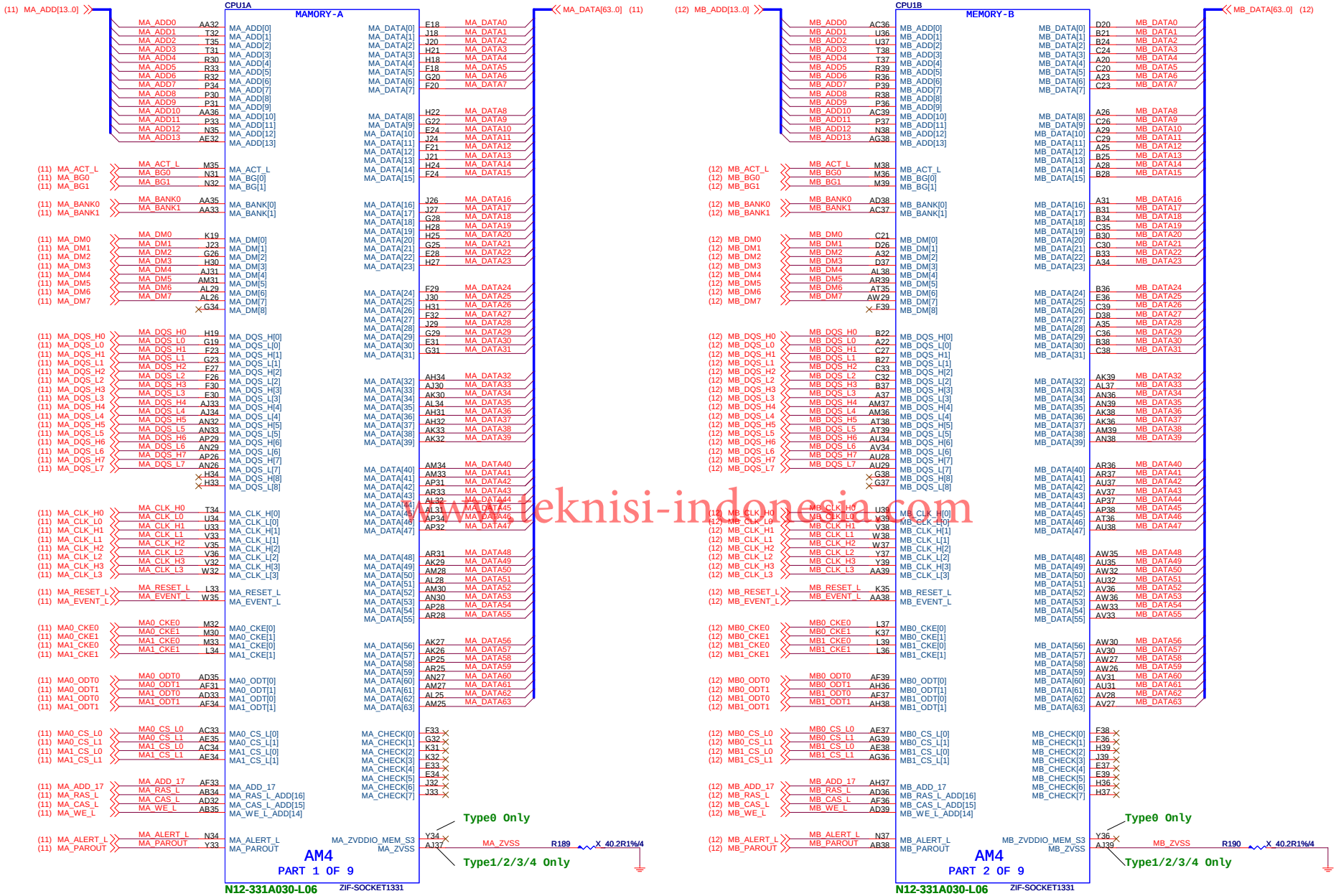

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Custom	AM4 DDR4 I/F	1.2

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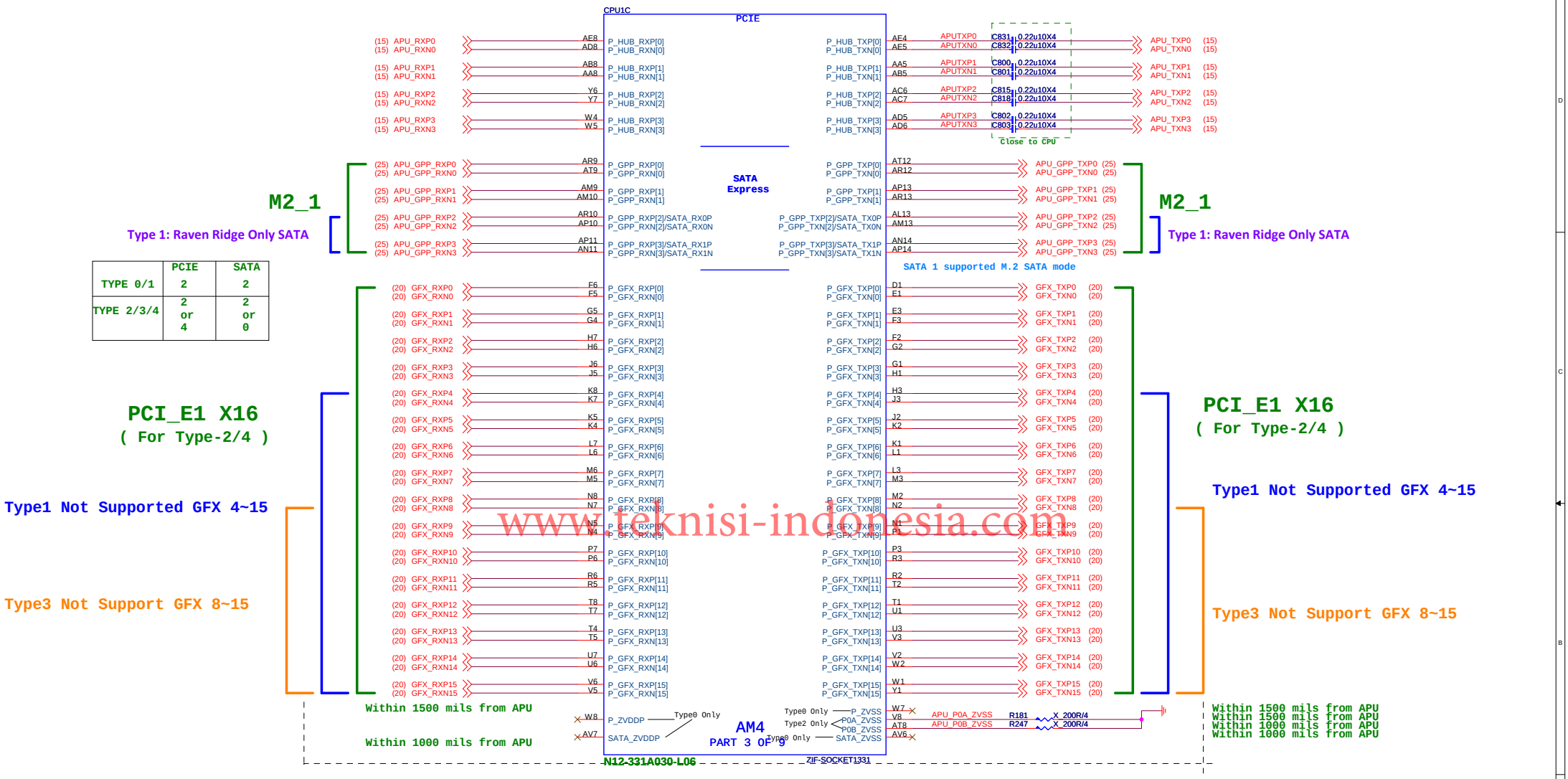

	PCIE	SATA
TYPE 0/1	2	2
TYPE 2/3/4	2 or 4	2 or 0

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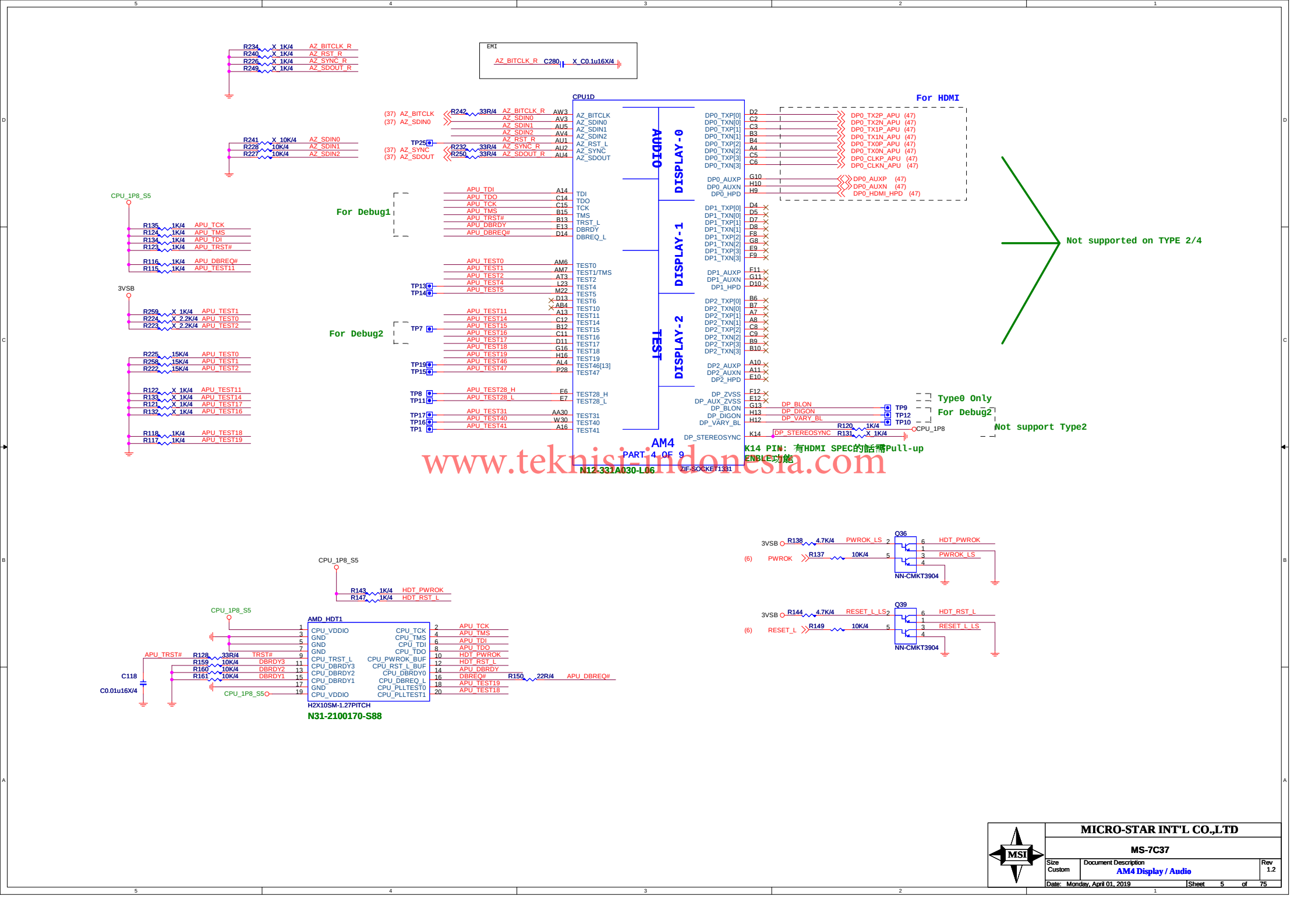
EMI
AZ_BITCLK_R C280 X_C0.1u16X/4
CPU1D
AUDIO
DISPLAY-0
DISPLAY-1
DISPLAY-2
TEST
AM4
PART 4 OF 9
ZIF-SOCKET1331
N12-331A030-L06
For HDMI
For Debug1
For Debug2
Not supported on TYPE 2/4
Type0 Only
For Debug2
Not support Type2
K14 PIN: 有HDMI SPEC的話需Pull-up
ENBLE功能
CPU_1P8_S5
3VSB
AMD_HDT1
H2X10SM-1.27PITCH
N31-2100170-S88
NN-CMKT3904
NN-CMKT3904
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MS-7C37
Size Custom
Document Description
AM4 Display / Audio
Rev 1.2
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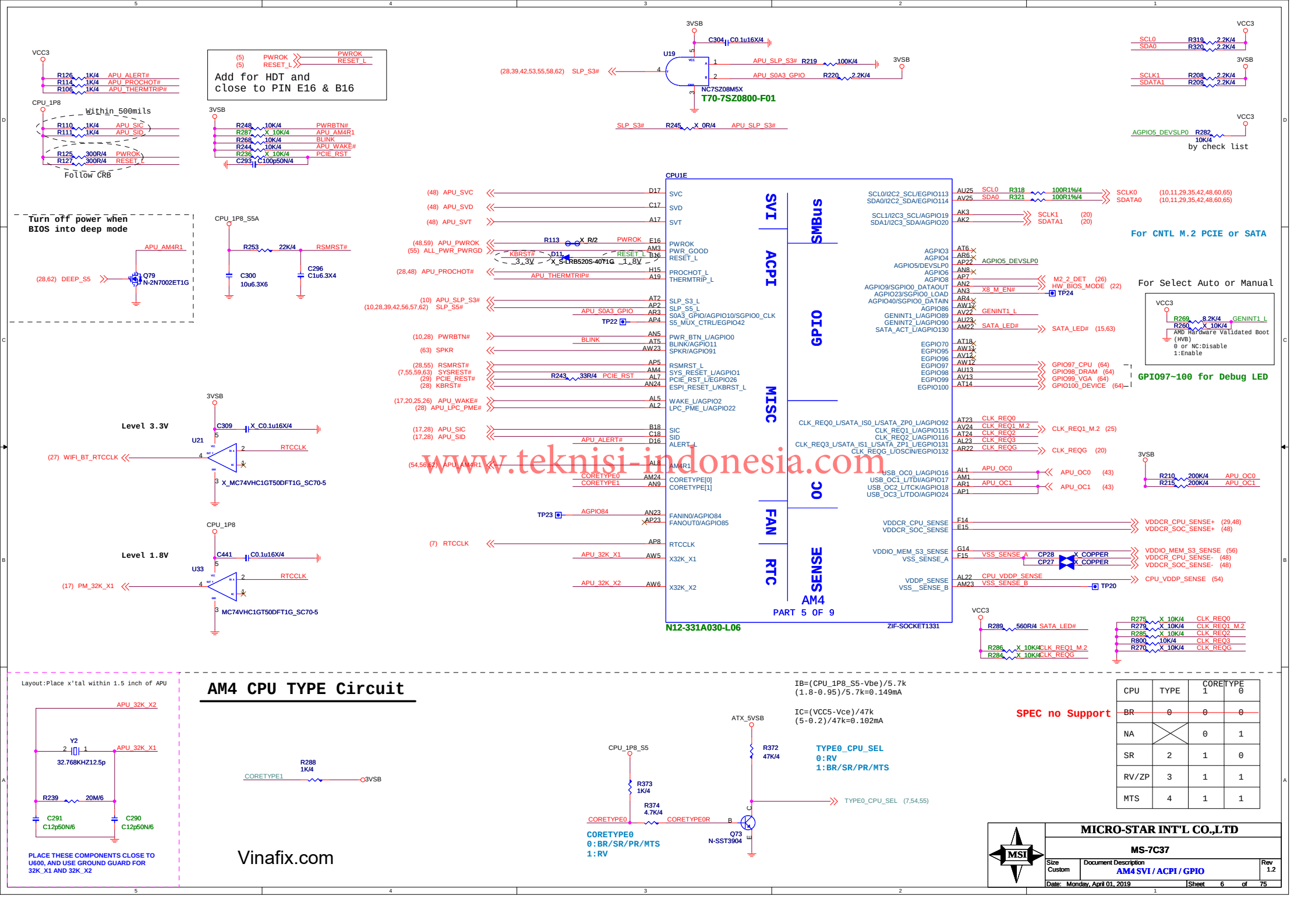
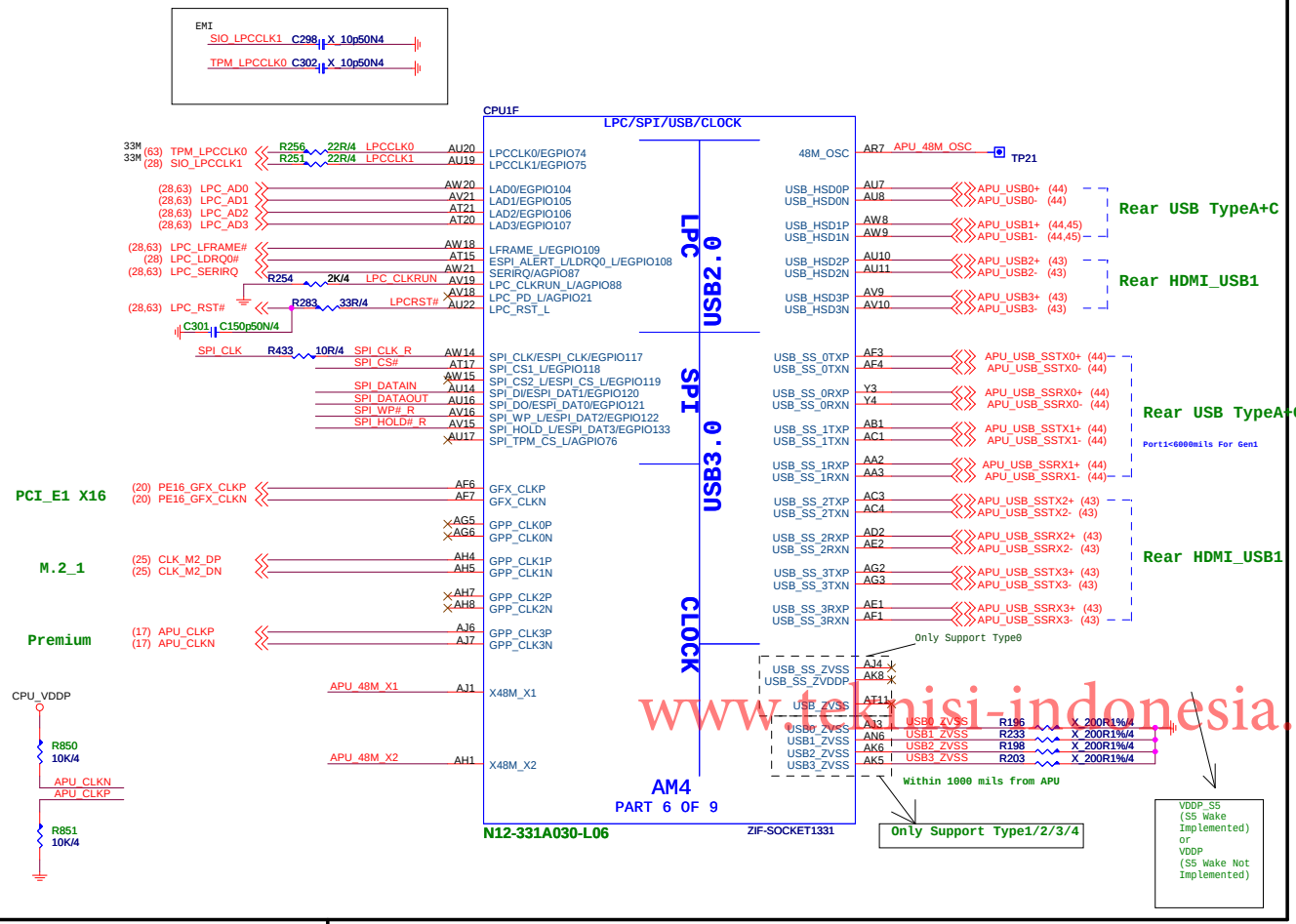
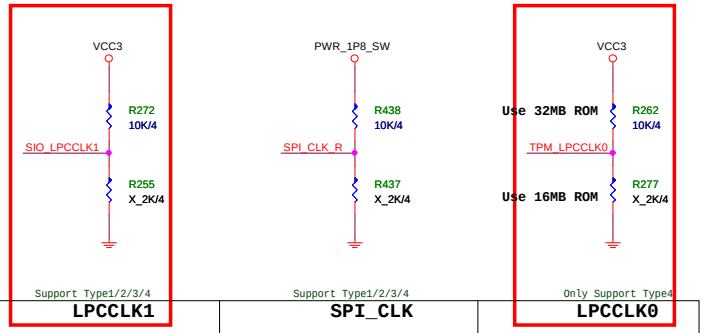


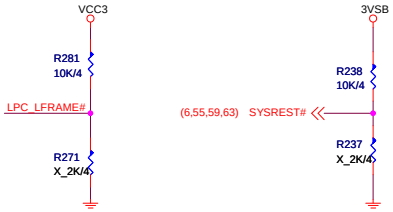
CPU	TYPE	CORETYPE 1	CORETYPE 0
~~BR~~	~~0~~	~~0~~	~~0~~
NA	X	0	1
SR	2	1	0
RV/ZP	3	1	1
MTS	4	1	1



Strapping Options

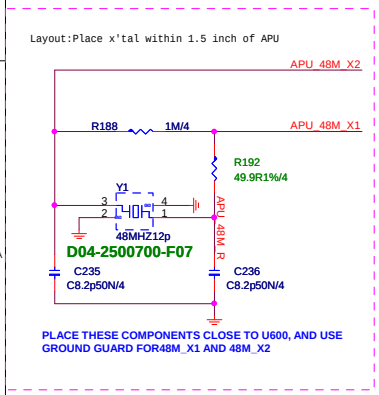


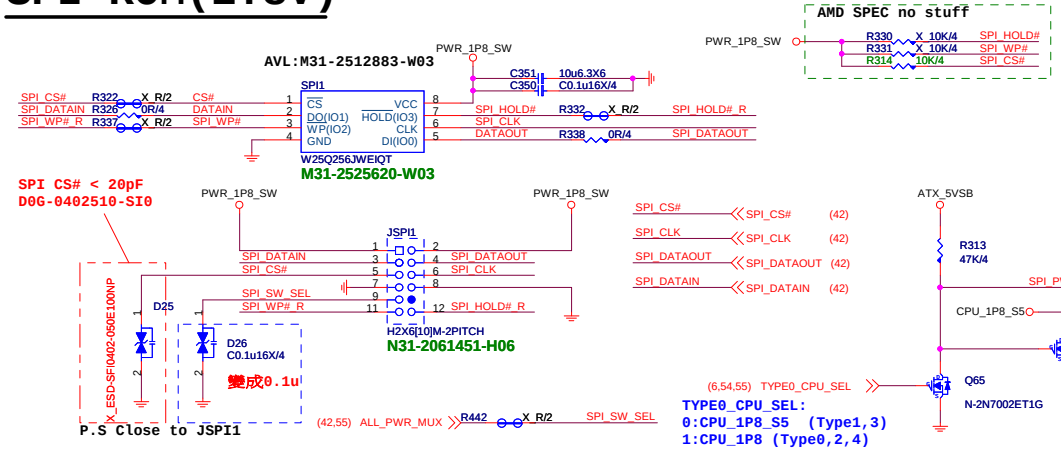
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image (Default)
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]

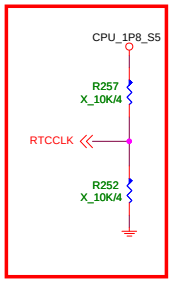


	AGPIO3	LFRAME	SYSREST#
	Only Support Type0	Support Type1/2/3/4	Support Type1/2/3/4
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

SPI ROM(1.8V)







	RTCCLK
	Only Support Type4
PULL HIGH	RTCCLK is input and is used as the bypass clock (Default)
PULL LOW	Normal Mode: Use 32Khz xtal as the source of RTC clock

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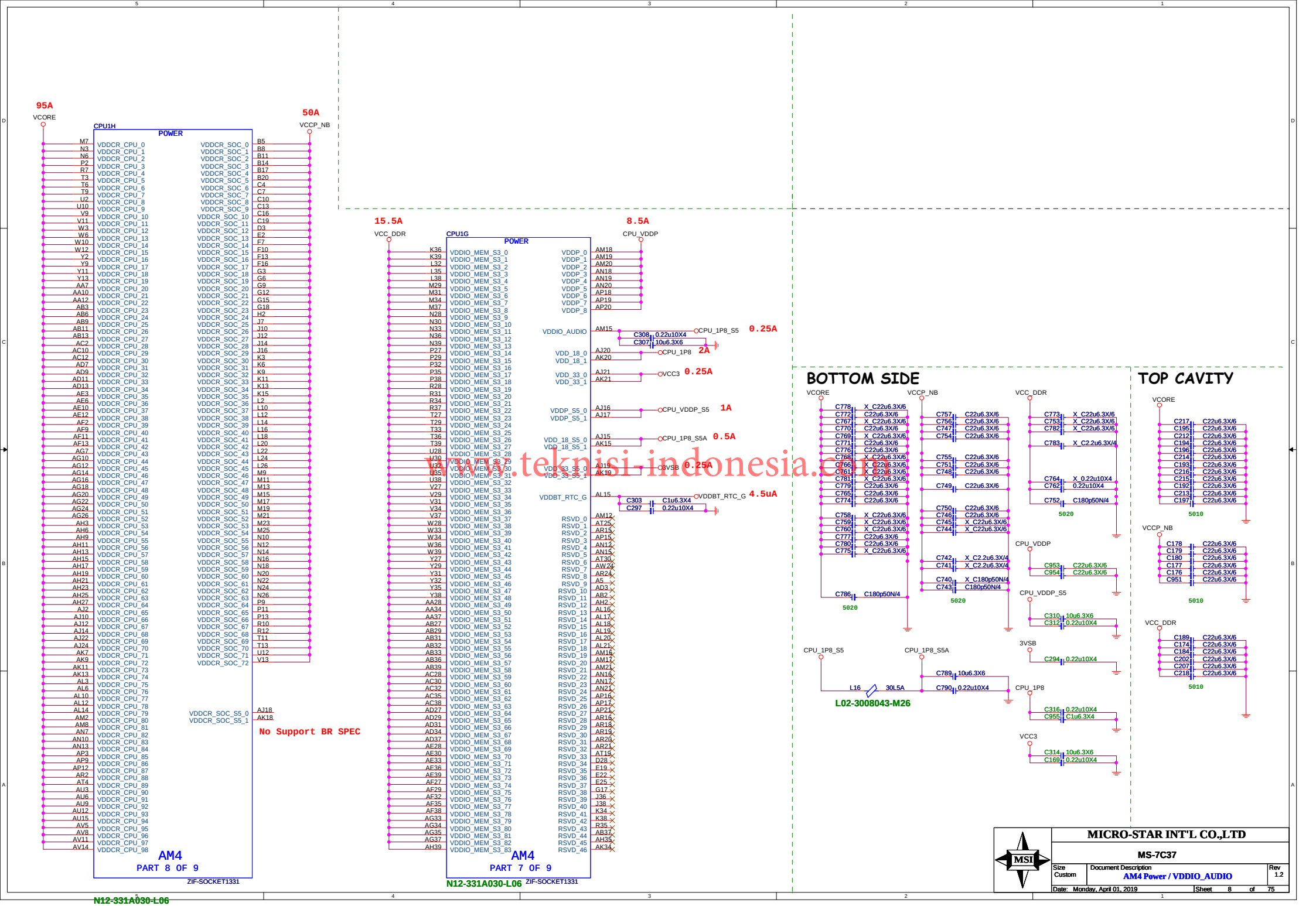

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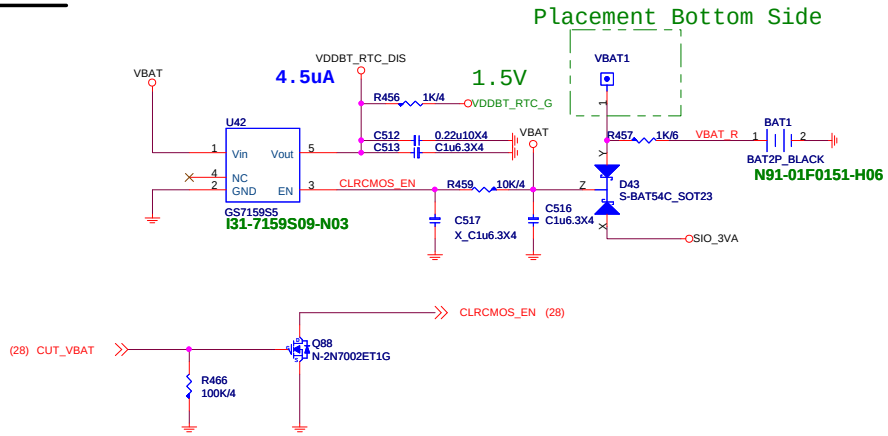
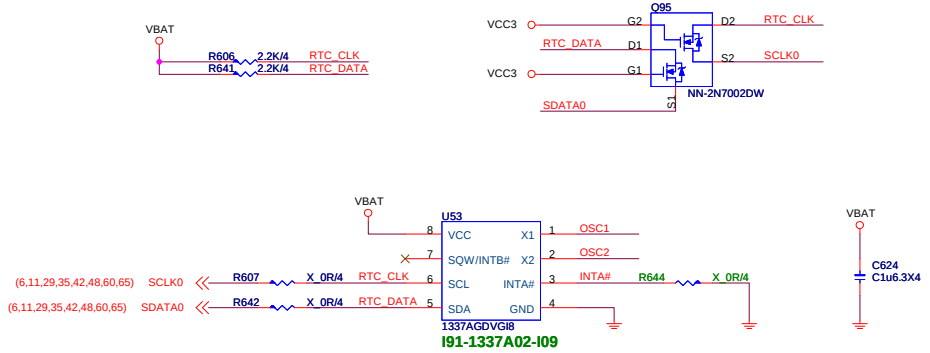
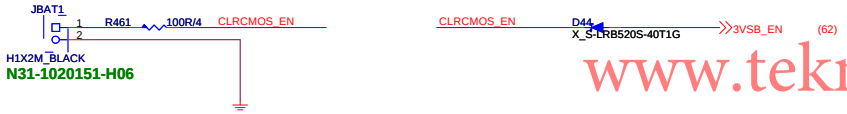
RTC & Clear CMOS Circuit

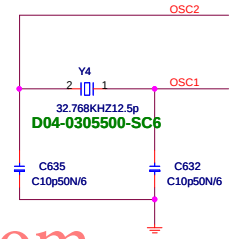


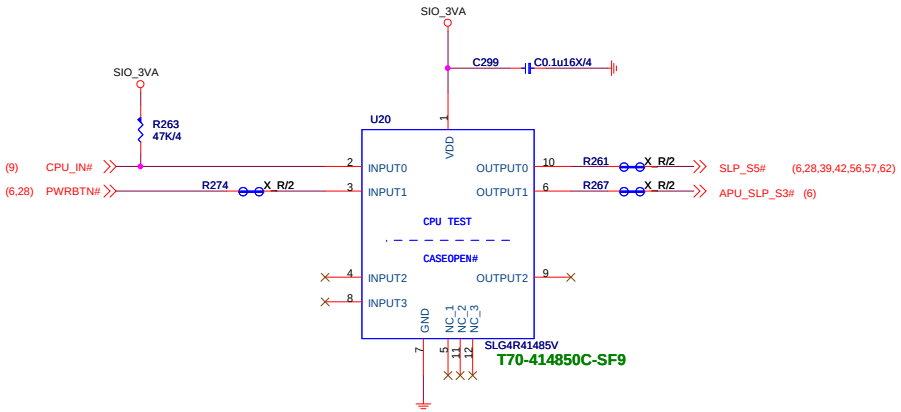
RTC Backup



Clear CMOS button







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Size: Custom | Document Description: RTC / CMOS | Rev: 1.2

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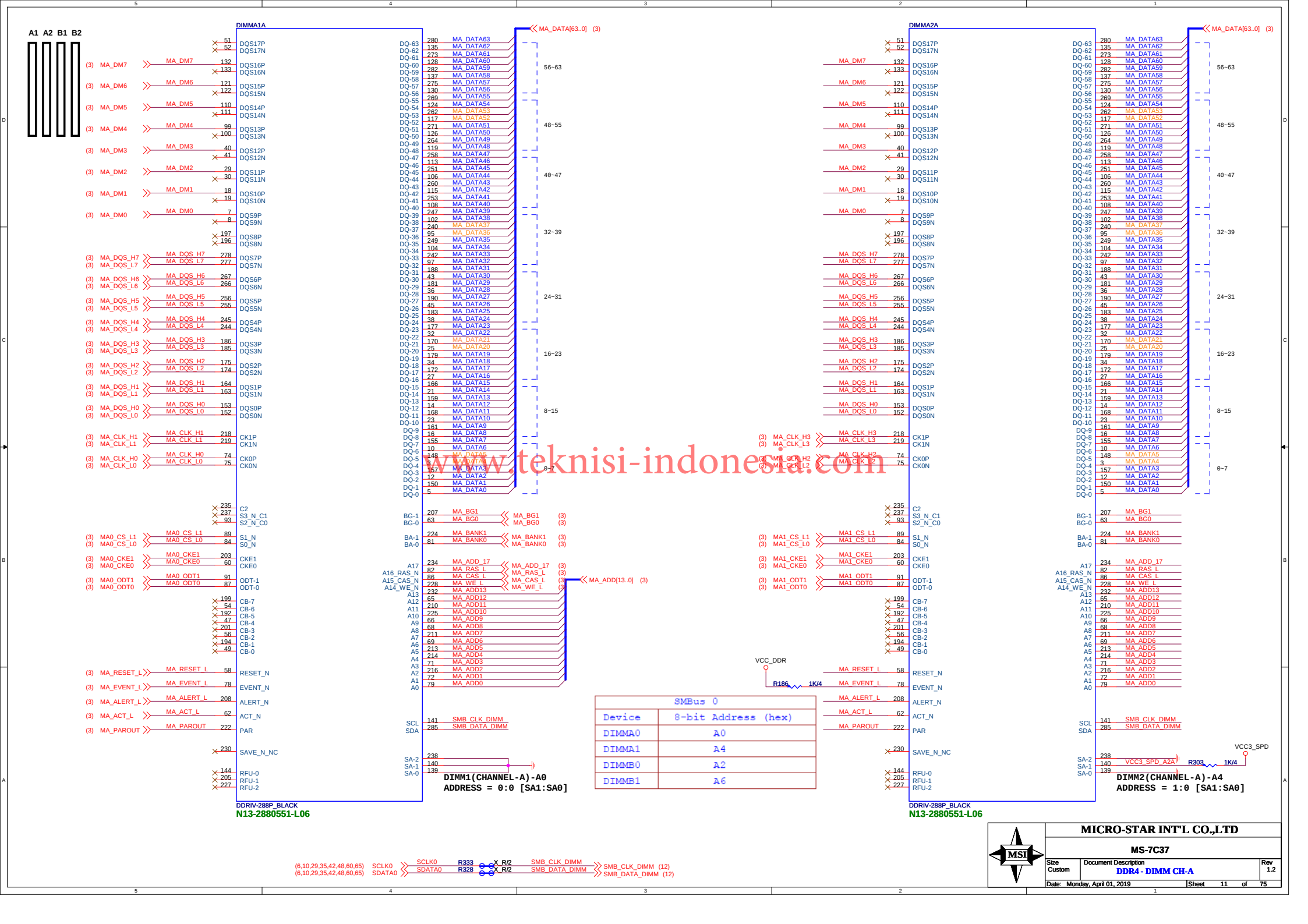

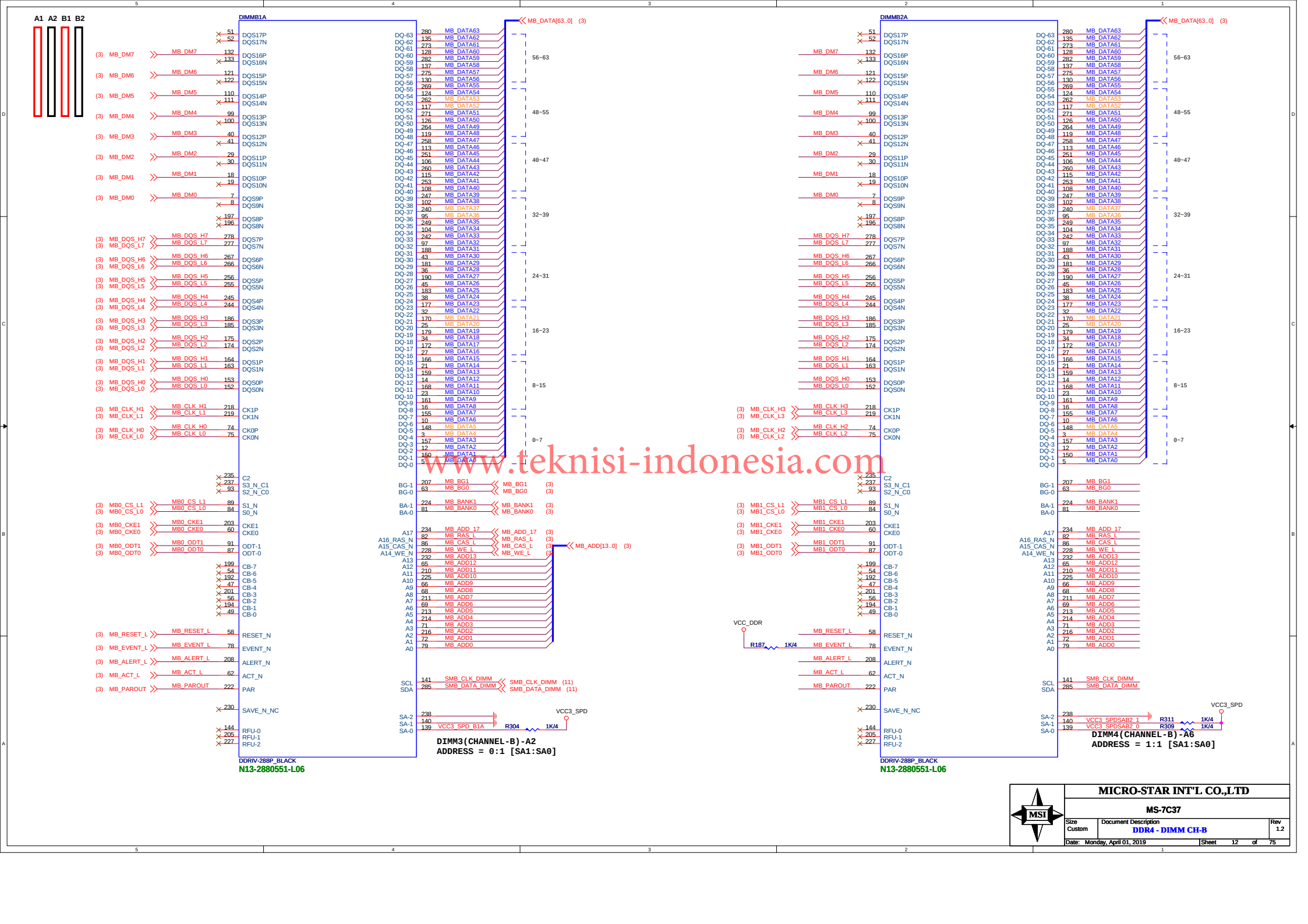
A1 A2 B1 B2
DIMMB1A
DIMMB2A
MB_DATA[63..0] (3)
MB_ADD[13..0] (3)
56~63
48~55
40~47
32~39
24~31
16~23
8~15
0~7
VCC_DDR
R187 1K/4
VCC3_SPD
R304 1K/4
R311 1K/4
R309 1K/4
DIMM3(CHANNEL-B)-A2
ADDRESS = 0:1 [SA1:SA0]
DIMM4(CHANNEL-B)-A6
ADDRESS = 1:1 [SA1:SA0]
DDRIV-288P_BLACK
N13-2880551-L06
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avl:D08-0301100-B07

F5
VCC3 1 2 VCC3_SPD
F-SPR-P260T-2.6A
D08-0301000-P16

DIMM SLOT PN BY SPEC

DIMMA1C
DDRIV-288P_BLACK
N13-2880551-L06

DIMMA2C
DDRIV-288P_BLACK
N13-2880551-L06

DDR VREF

(place resistors close to DIMMs)

DIMM_CA_VREF_A
VCC_DDR
C46 C0.1u16X/4
R50 1K1%/4
C144 C0.1u16X/4
D56 ESD-AOZ8231ADI-05
C67 C1000p50X4
C68 C0.1u16X/4
R66 1K1%/4
D0G-130050C-A68

VCC3_SPD C347 C0.1u16X/4
DIMM_CA_VREF_A C49 C2.2u6.3X/4 C55 C0.1u16X/4
VTT_DDR C182 C0.1u16X/4
VPP25 C361 C0.1u16X/4 C360 C0.1u16X/4

VCC_DDR C138 C152 C129 C130 C35 C145 C151 C150 C1u6.3X4 C0.1u16X/4

VCC3_SPD C354 C0.1u16X/4
DIMM_CA_VREF_A C62 C54 C2.2u6.3X/4 C0.1u16X/4
VTT_DDR C186 C0.1u16X/4
VPP25 C382 C362 C0.1u16X/4

VCC_DDR C146 C140 C131 C127 C1u6.3X4
C34 C154 C166 C136 C0.1u16X/4

DIMMA1B
DDRIV-288P_BLACK
N13-2880551-L06

DIMMA2B
DDRIV-288P_BLACK
N13-2880551-L06

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Size: Custom
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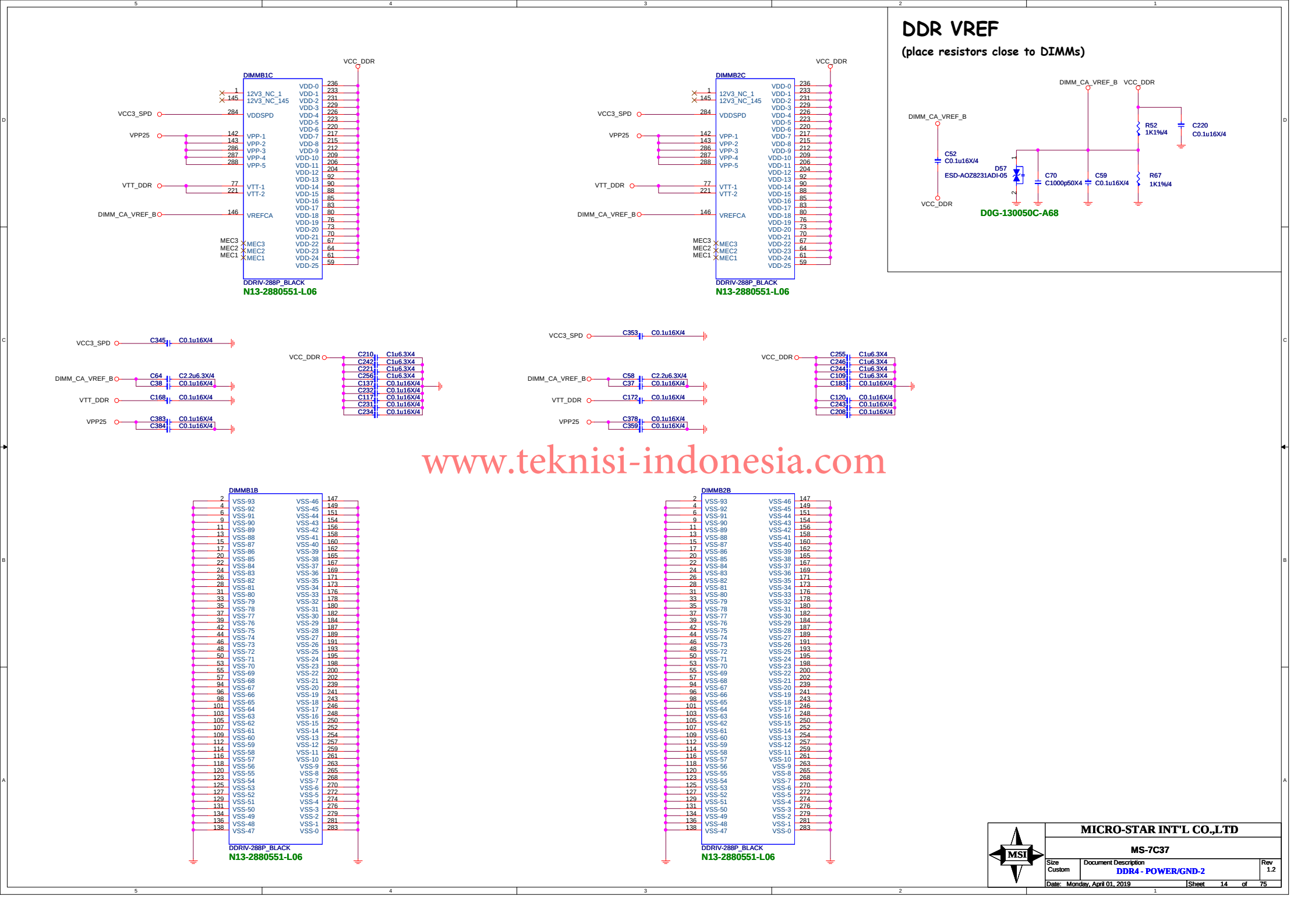
DDR VREF
(place resistors close to DIMMs)
DIMM_CA_VREF_B
VCC_DDR
C52
C0.1u16X/4
D57
ESD-AOZ8231ADI-05
C70
C1000p50X4
C59
C0.1u16X/4
R52
1K1%/4
R67
1K1%/4
C220
C0.1u16X/4
D0G-130050C-A68
DIMMB1C
DIMMB2C
VCC3_SPD
VPP25
VTT_DDR
DIMM_CA_VREF_B
MEC3
MEC2
MEC1
DDRIV-288P_BLACK
N13-2880551-L06
C345
C64
C38
C168
C383
C384
C210
C242
C221
C256
C137
C232
C117
C231
C234
C353
C58
C37
C172
C378
C359
C255
C246
C244
C109
C183
C120
C243
C208
C1u6.3X4
C2.2u6.3X/4
C0.1u16X/4
DIMMB1B
DIMMB2B
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Custom
Document Description
DDR4 - POWER/GND-2
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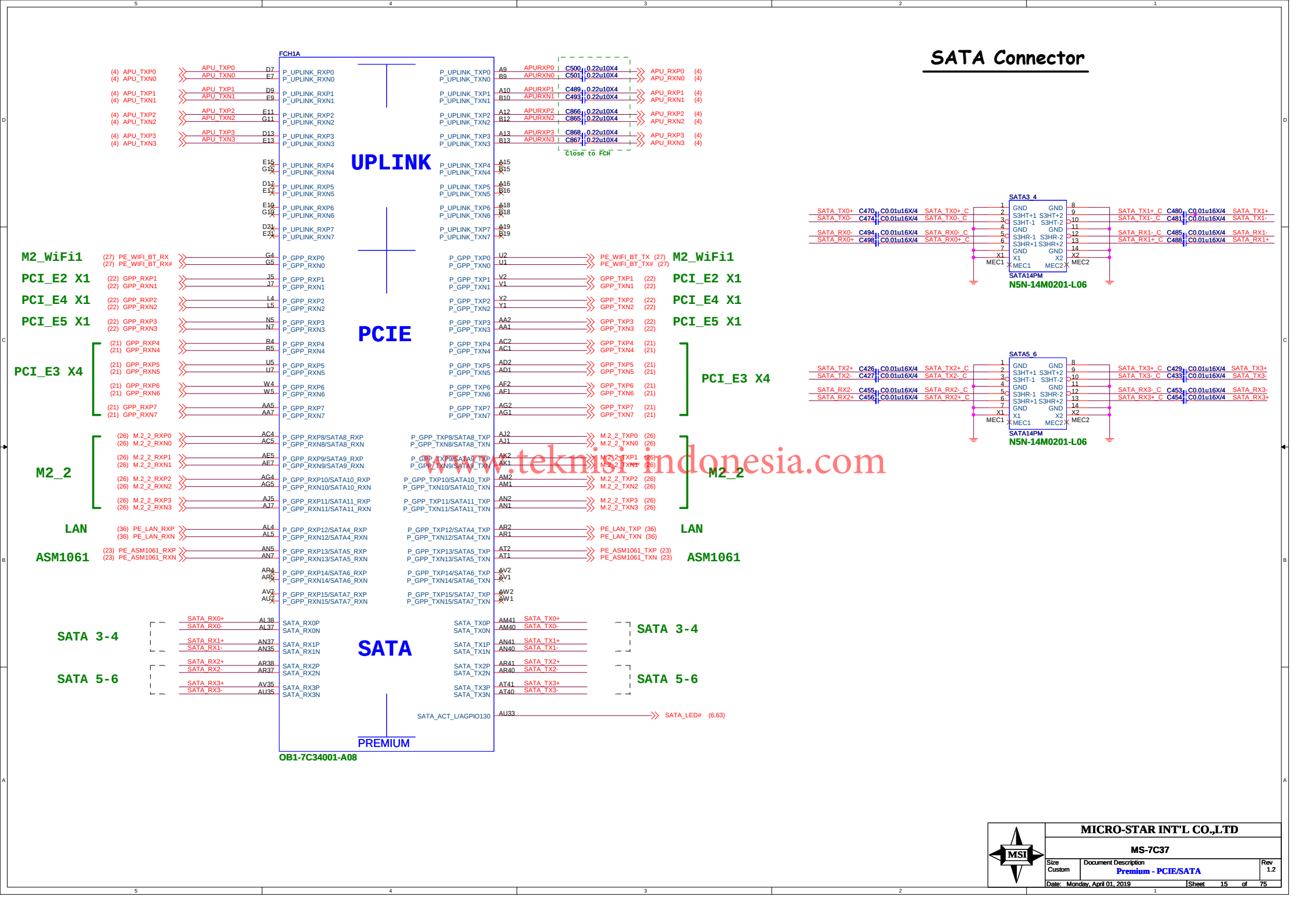
SATA Connector
FCH1A
UPLINK
PCIE
SATA
PREMIUM
Close to FCH
M2_WiFi1
PCI_E2 X1
PCI_E4 X1
PCI_E5 X1
PCI_E3 X4
M2_2
LAN
ASM1061
SATA 3-4
SATA 5-6
SATA3_4
SATA5_6
SATA14PM
N5N-14M0201-L06
OB1-7C34001-A08
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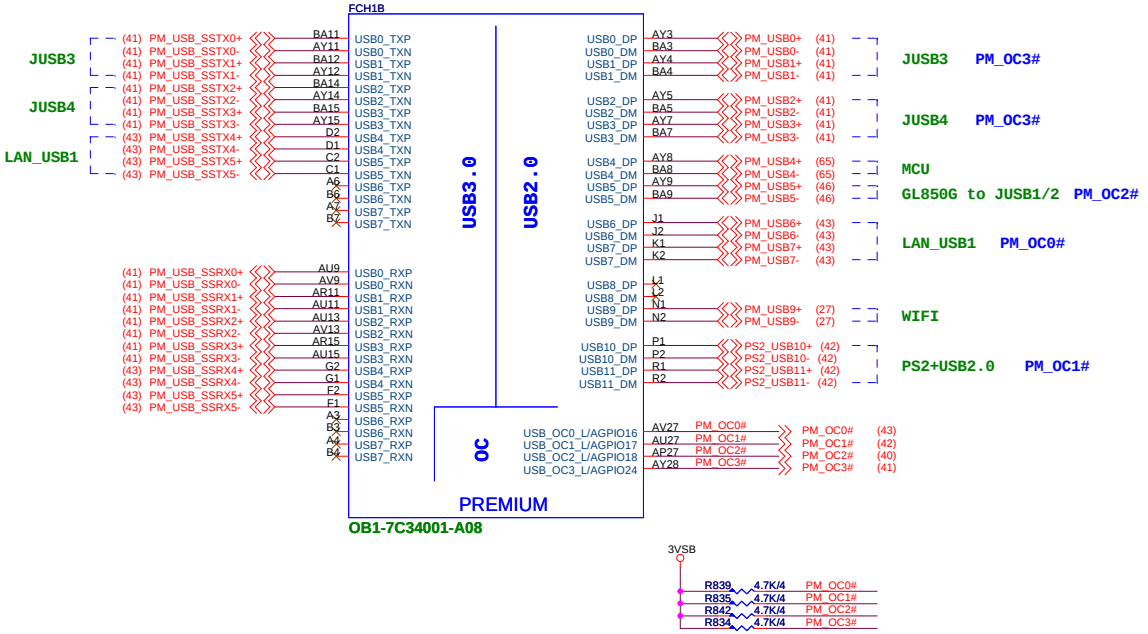

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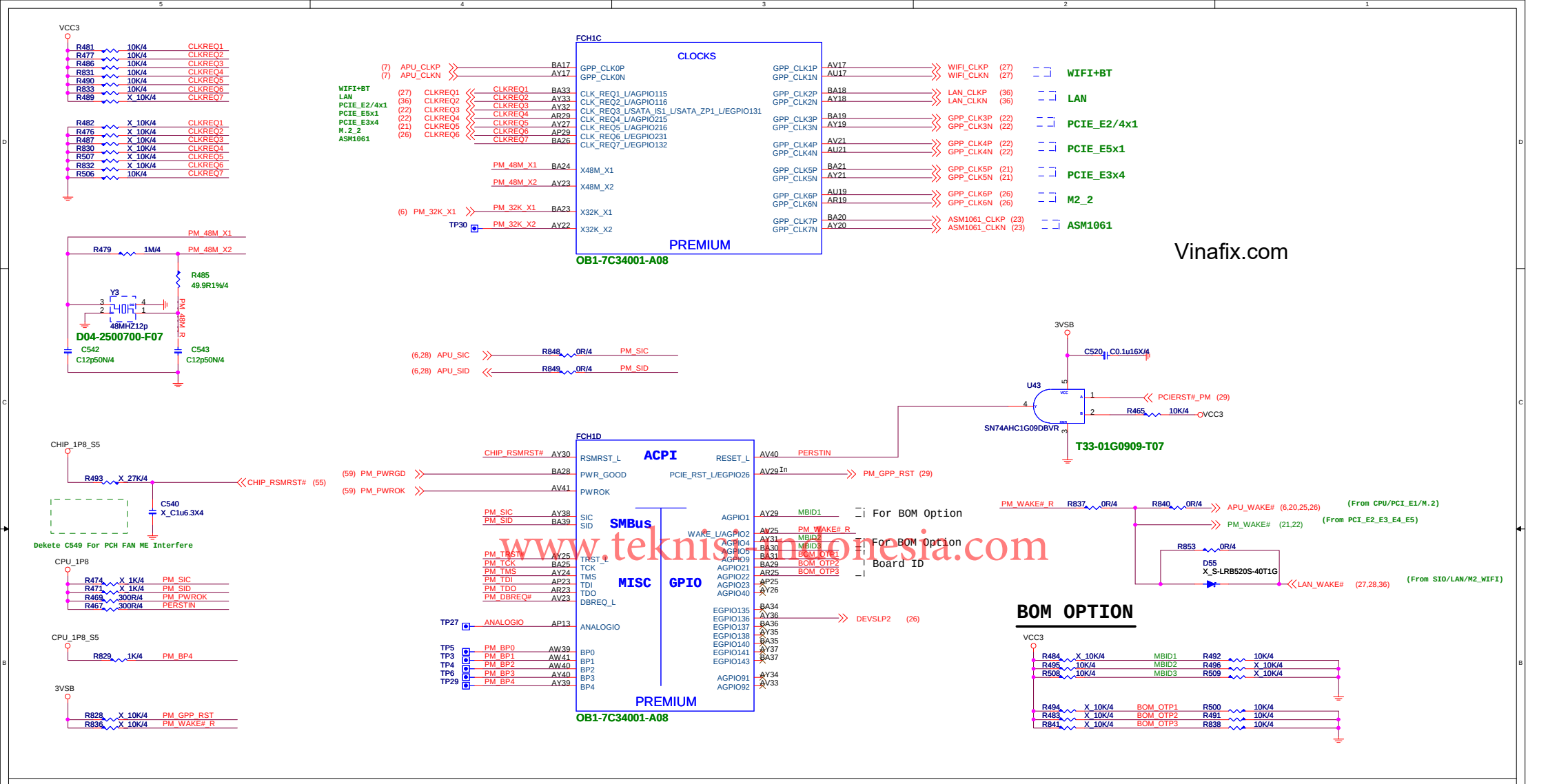
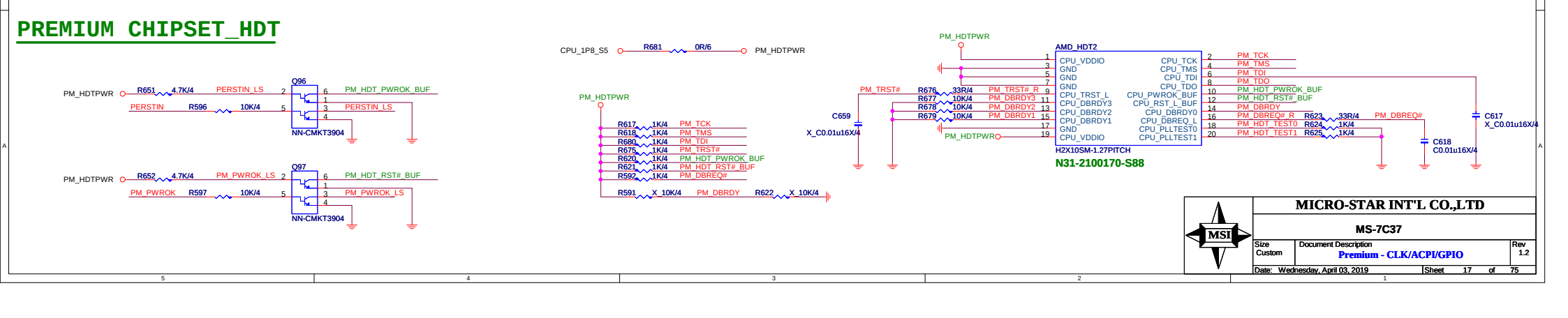


PREMIUM CHIPSET_HDT



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Size: Custom	Document Description: Premium - CLK/ACPI/GPIO
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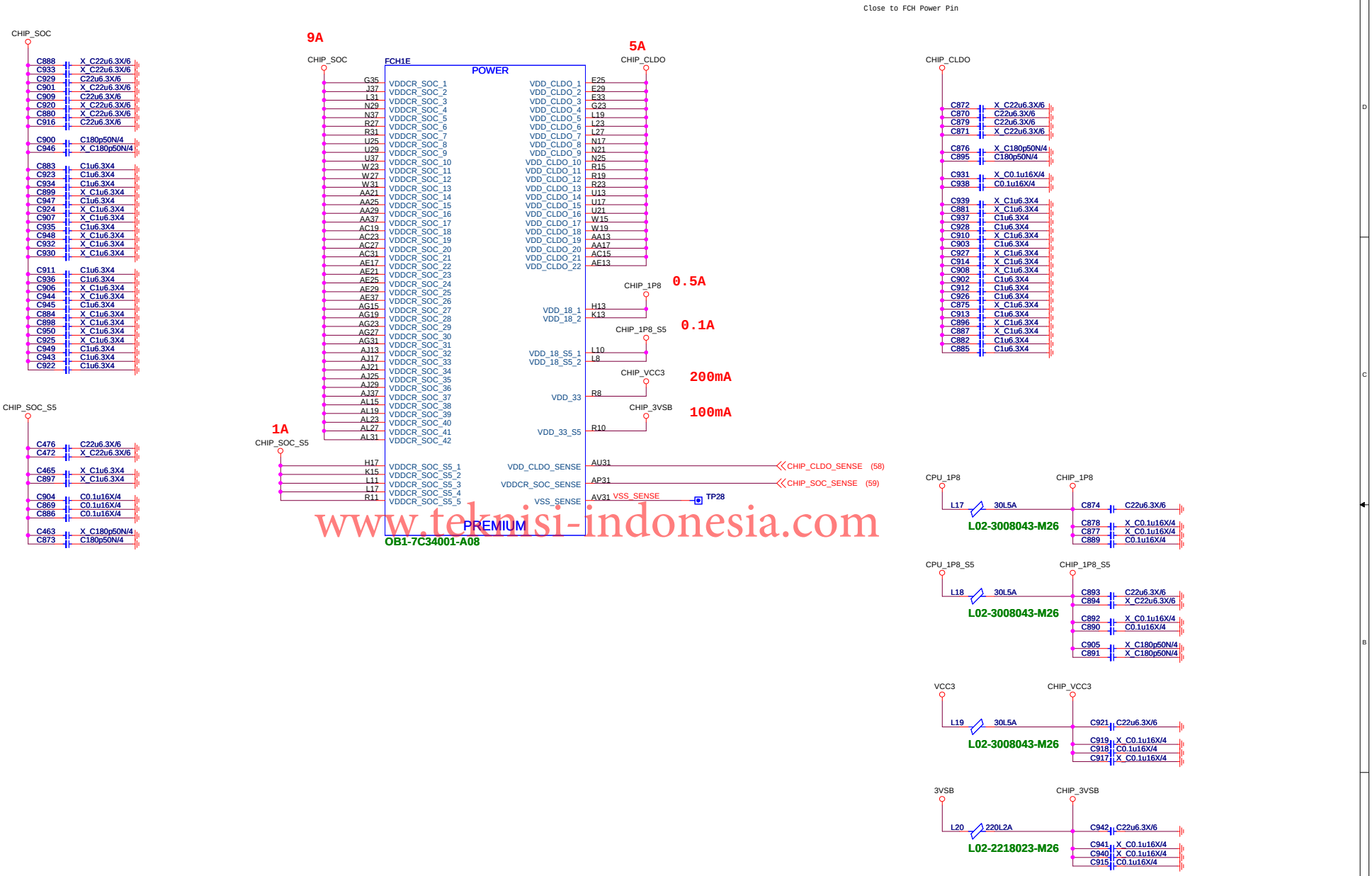

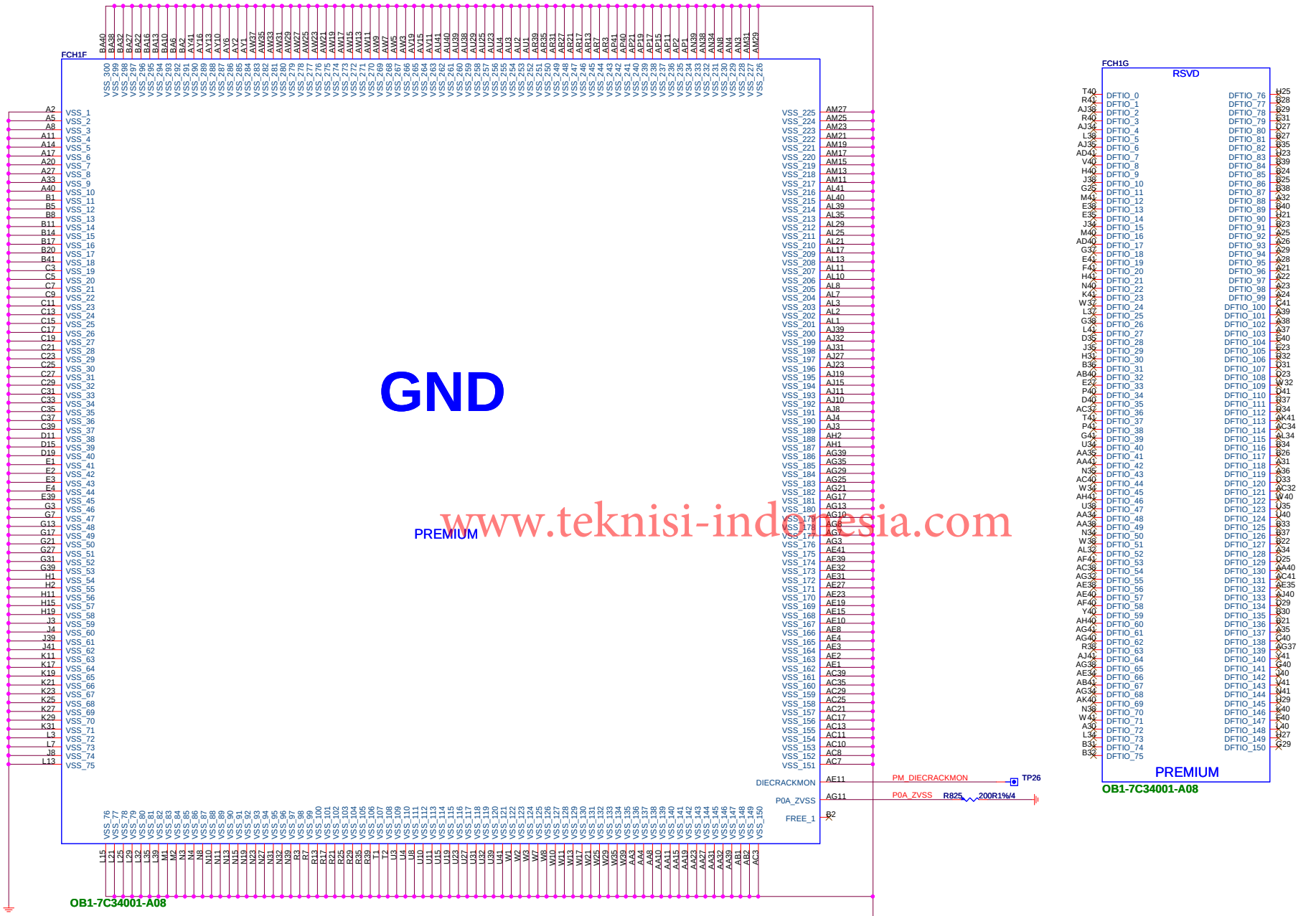

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MS-7C37		
Size: Custom	Document Description: Premium - GND	Rev: 1.2
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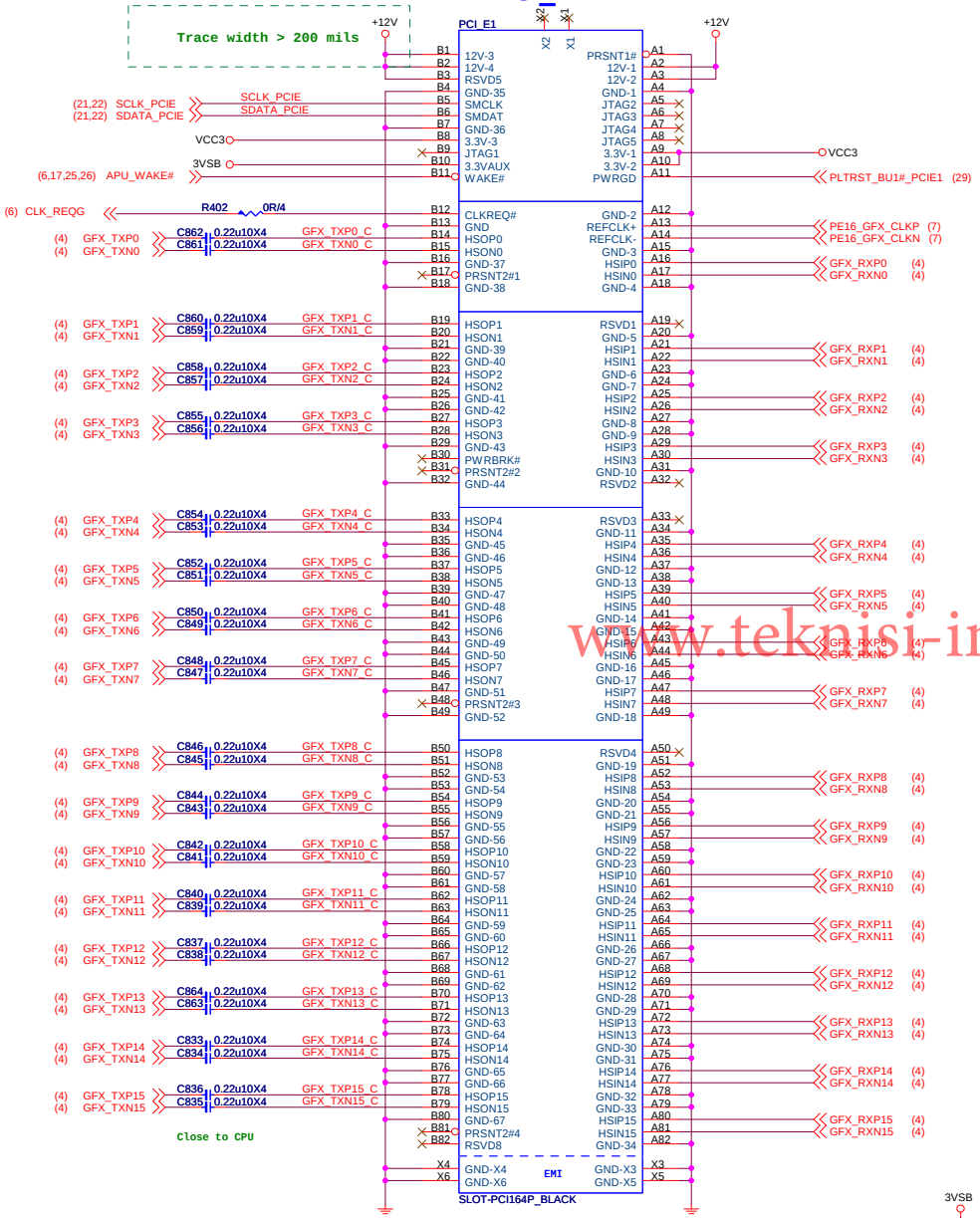
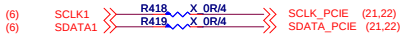
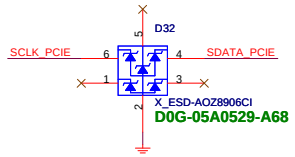
PCI EXPRESS x16 Slot

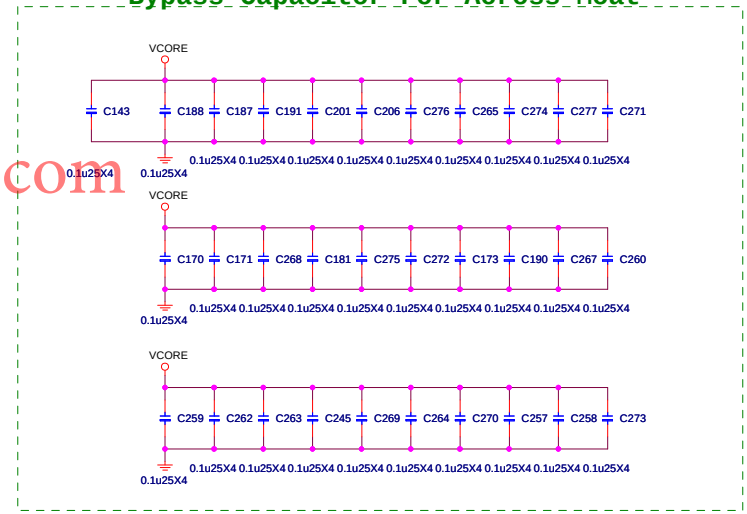
PCI_E1



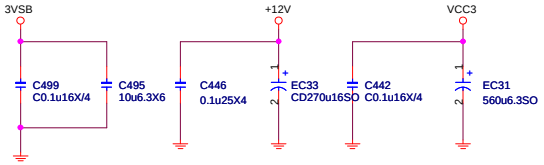




Bypass Capacitor For Across Moat



PCI Express x16 Slot		
+12V		- 5.5A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA



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Size: Custom	Document Description: PCI_E1 (X16)	Rev: 1.2
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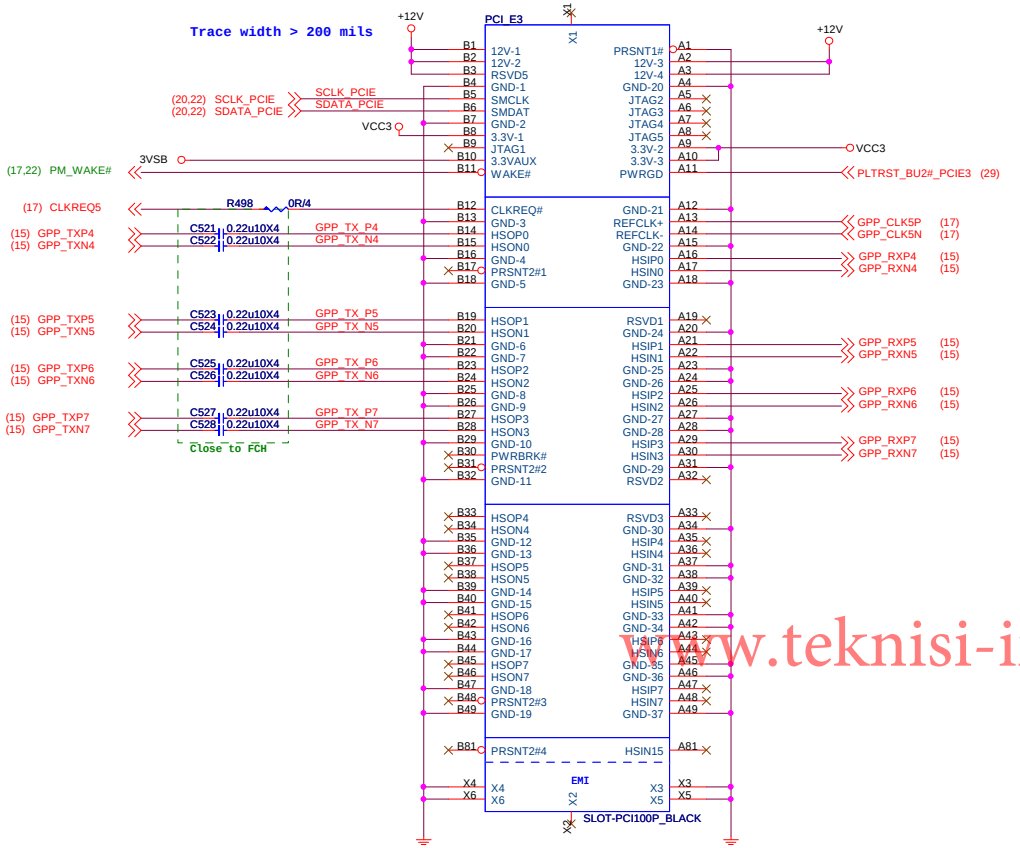
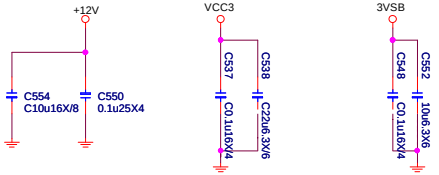
PCI_E3 X4



PCI Express x4 Slot *1		
+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA



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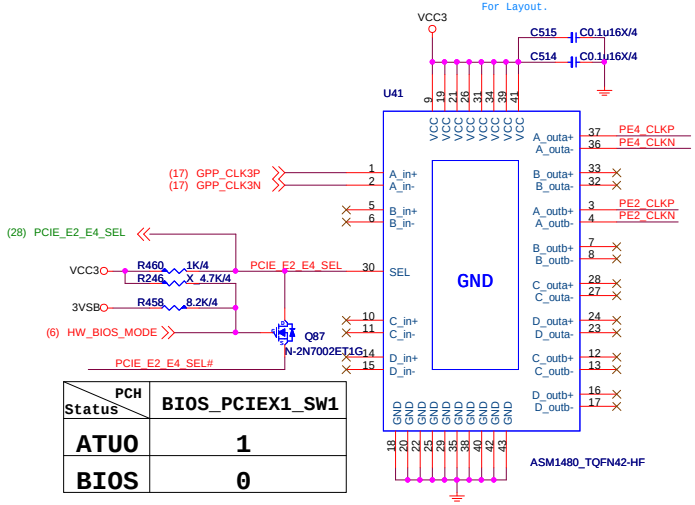
MS-7C37

Size	Document Description	Rev
Custom	PCI_E3 (X4)	1.2

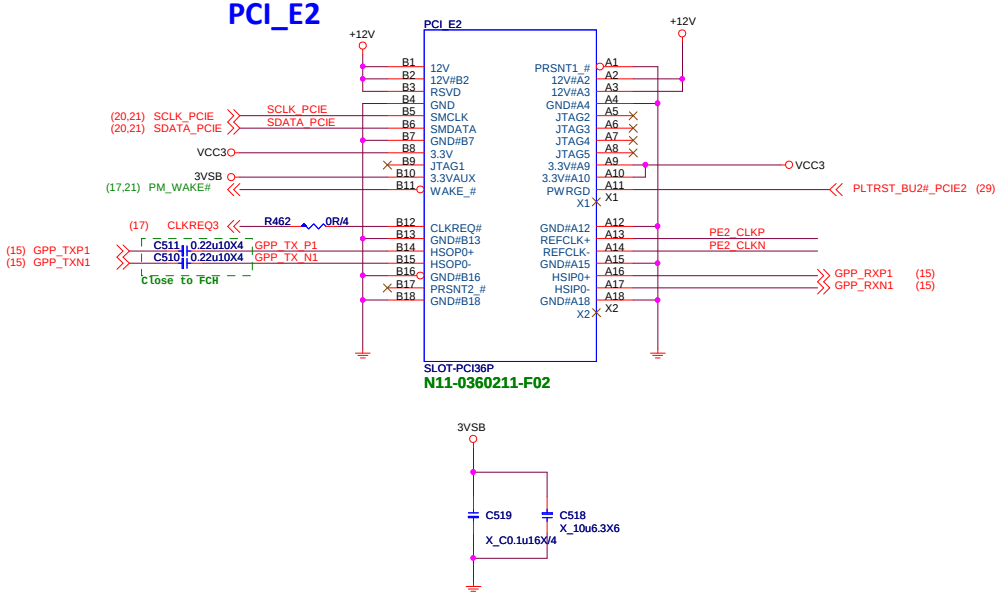
Date: Monday, April 01, 2019 Sheet 21 of 75



PCH Status	BIOS_PCIEX1_SW1
ATUO	1
BIOS	0

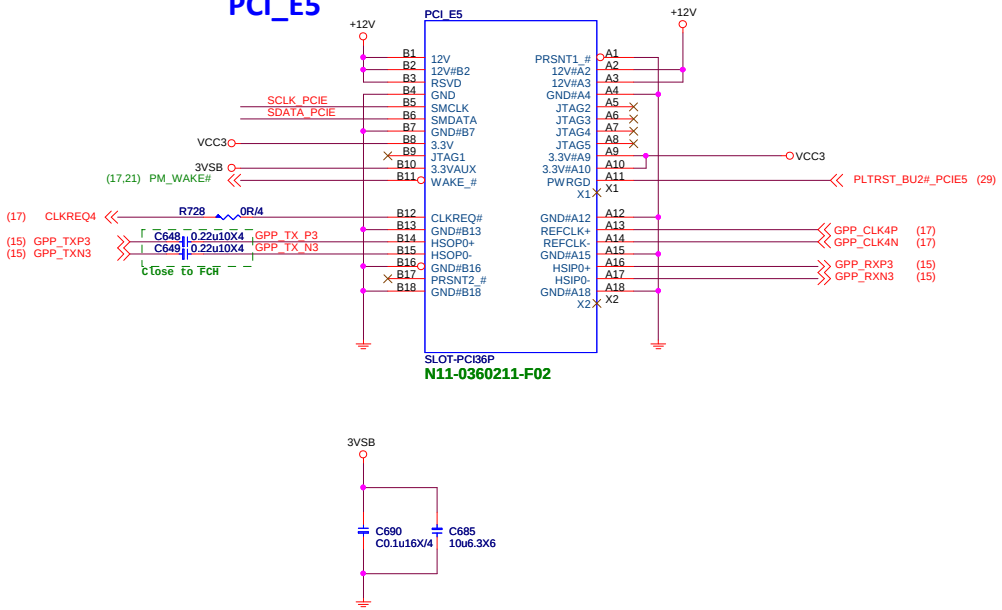
PCIE_E2_E4_SEL
L: PCI_E4
H: PCI_E2

PCI_E2

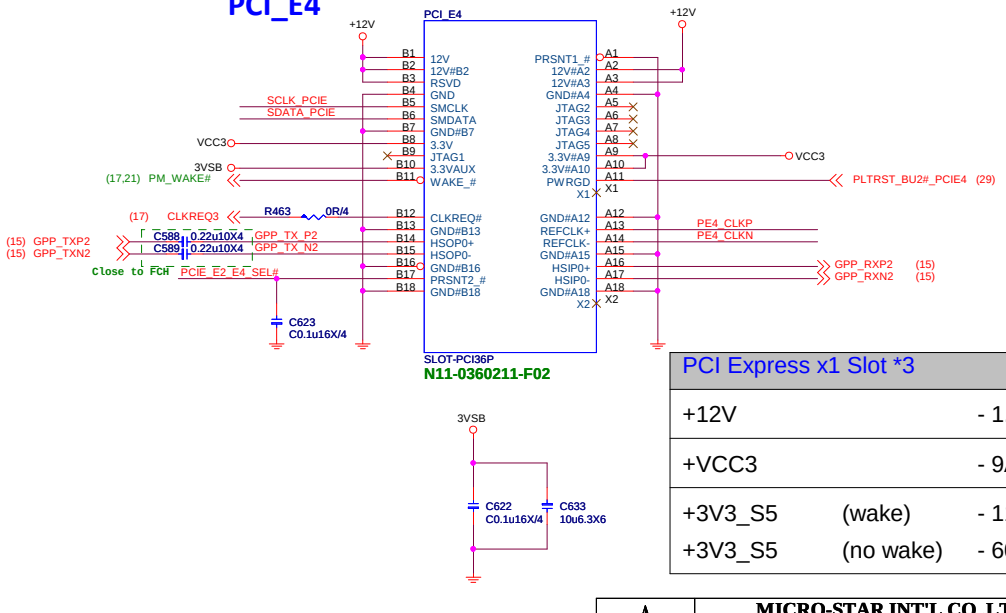


PCIE_E2 & PCIE_E4互切, PCIE_E2 & PCIE_E4同時有PCIE device 以PCIE_E4 優先

PCI_E5



PCI_E4



PCI Express x1 Slot *3		
+12V		- 1.5 A
+VCC3		- 9A
+3V3_S5	(wake)	- 1125mA
+3V3_S5	(no wake)	- 60mA

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MS-7C37

Size	Document Description	Rev
Custom	PCIE Switch PCI_E2 / E4 / E5 (X1)	1.2

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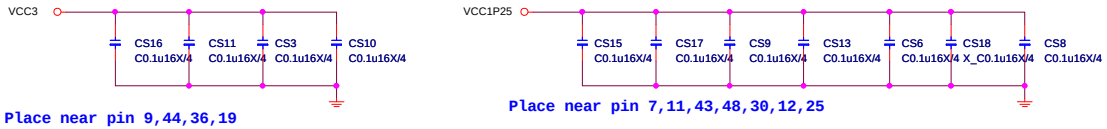
SATA Connector

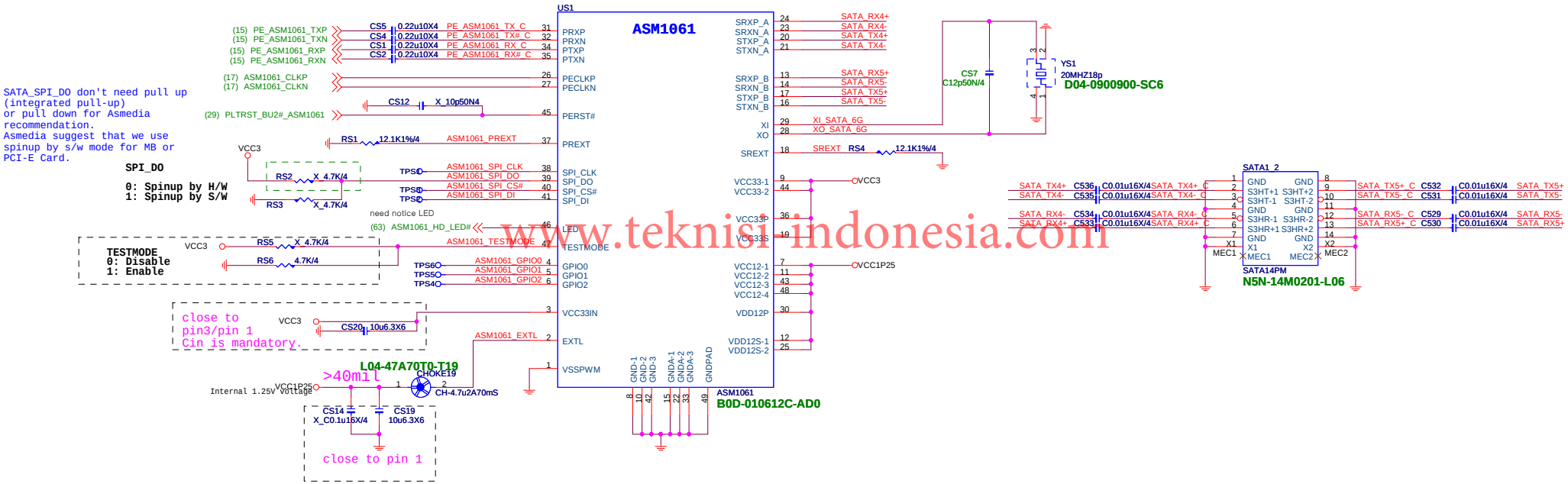
1.2V delay from 3.3V 90% > 0ms

ASM1061 POWER Consumption

	3.3V	1.25V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47



ASM1061 SATA6G



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C37	
Size: Custom	Document Description: PCIE to SATA (ASM1061)	Rev: 1.2
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MS-7C37	
Size: Custom	Document Description: PCI_E1_E3_E5 (X1)
Rev: 1.2	
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M.2_1 Connector

VCC3 4.25A
Max: 14W

Vinafix.com

22 * 110

SCREW1 SCREW E2B-7984020-H75 SCREW

RECESS1 SCREW E43-1203516-A89 CROSS RECESS

H6 H7 H5 H1 — E2B-7B05010-A89

Footprint: H_R240D173_BR189_PT

	MICRO-STAR INT'L CO.,LTD	
MSI	MS-7C37	
Size: Custom	Document Description: M2_1	Rev: 1.2
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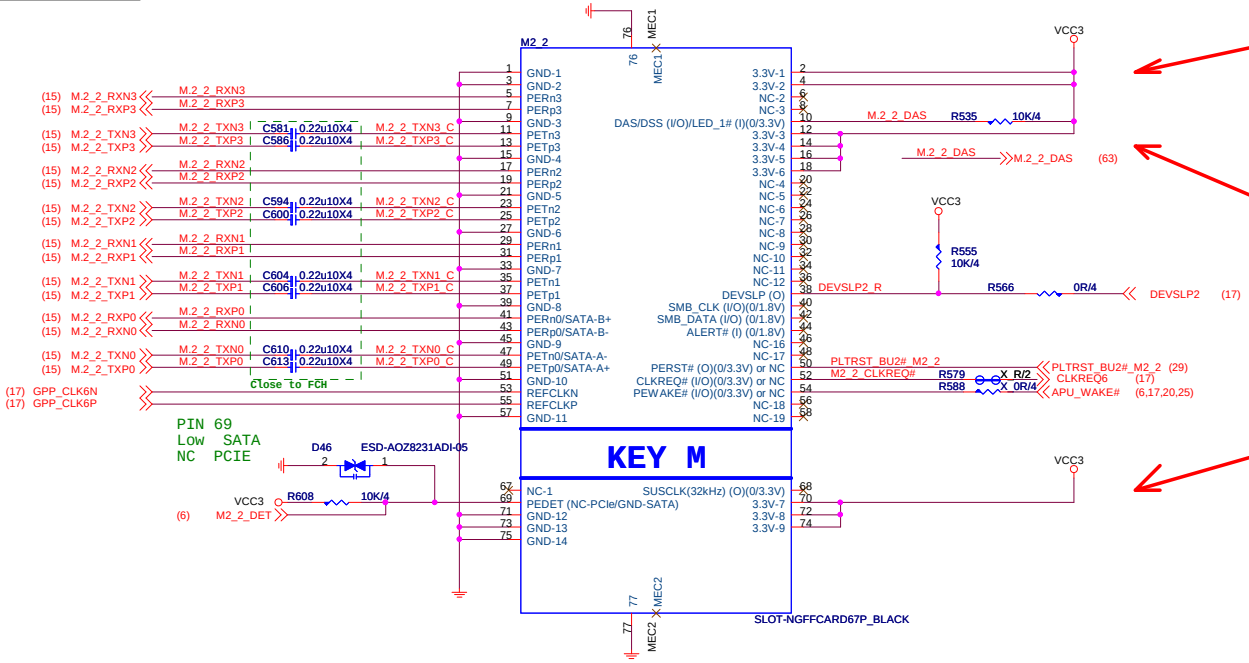
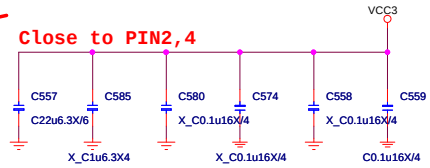
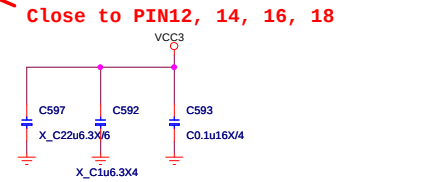
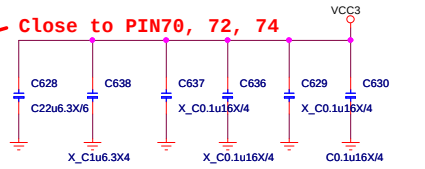
M.2_2 Connector



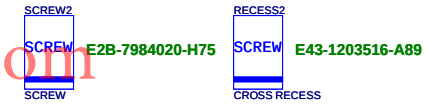
VCC3 4.25A
Max: 14W

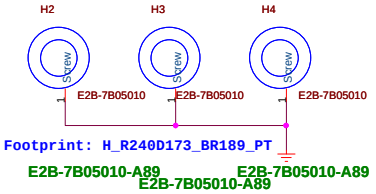






22 * 80





Support PCIE and SATA Mode

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MS-7C37	
Size: Custom	Document Description: M2_2
Rev: 1.2	
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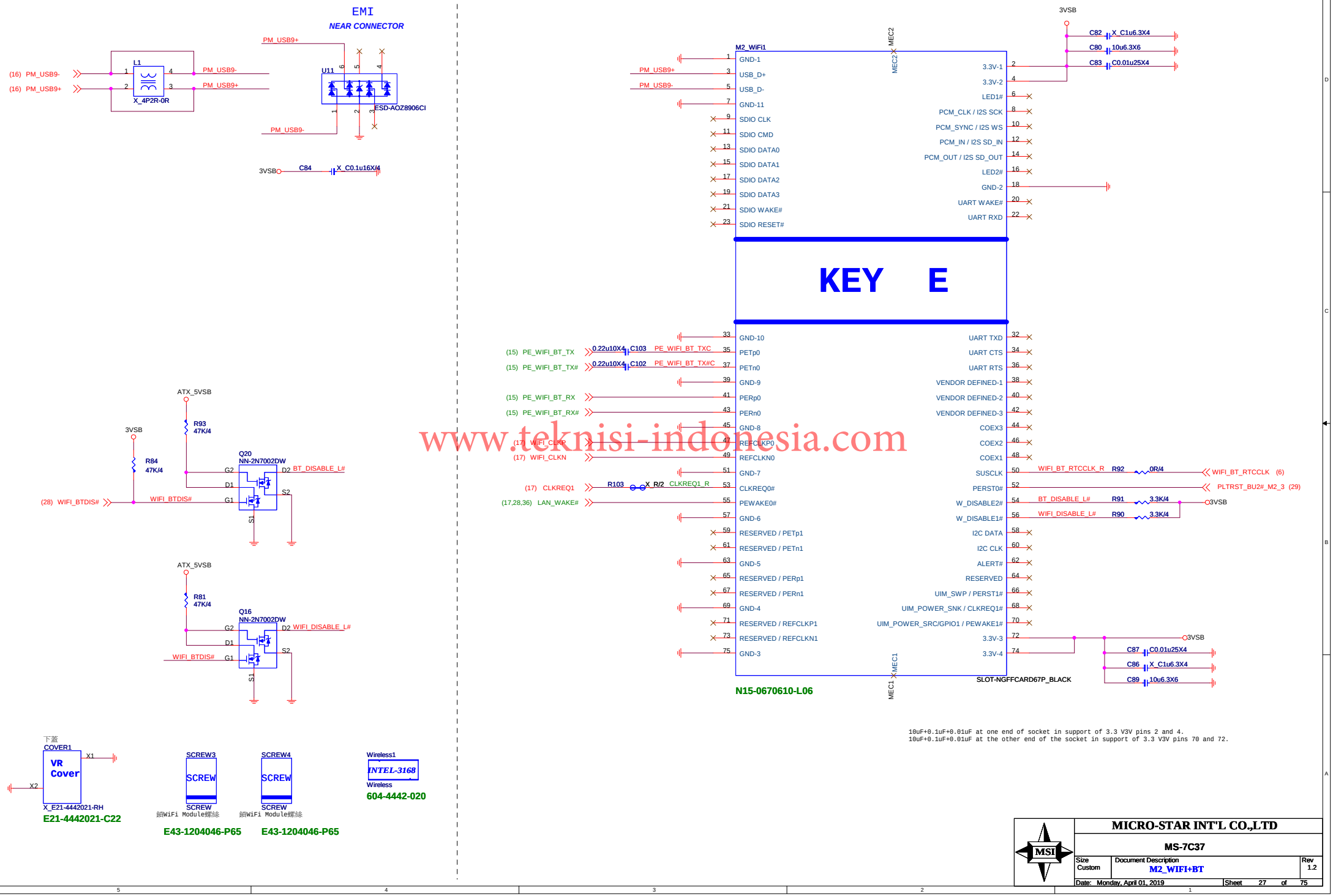

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MS-7C37	
Size: Custom	Document Description: M2_WIFI+BT
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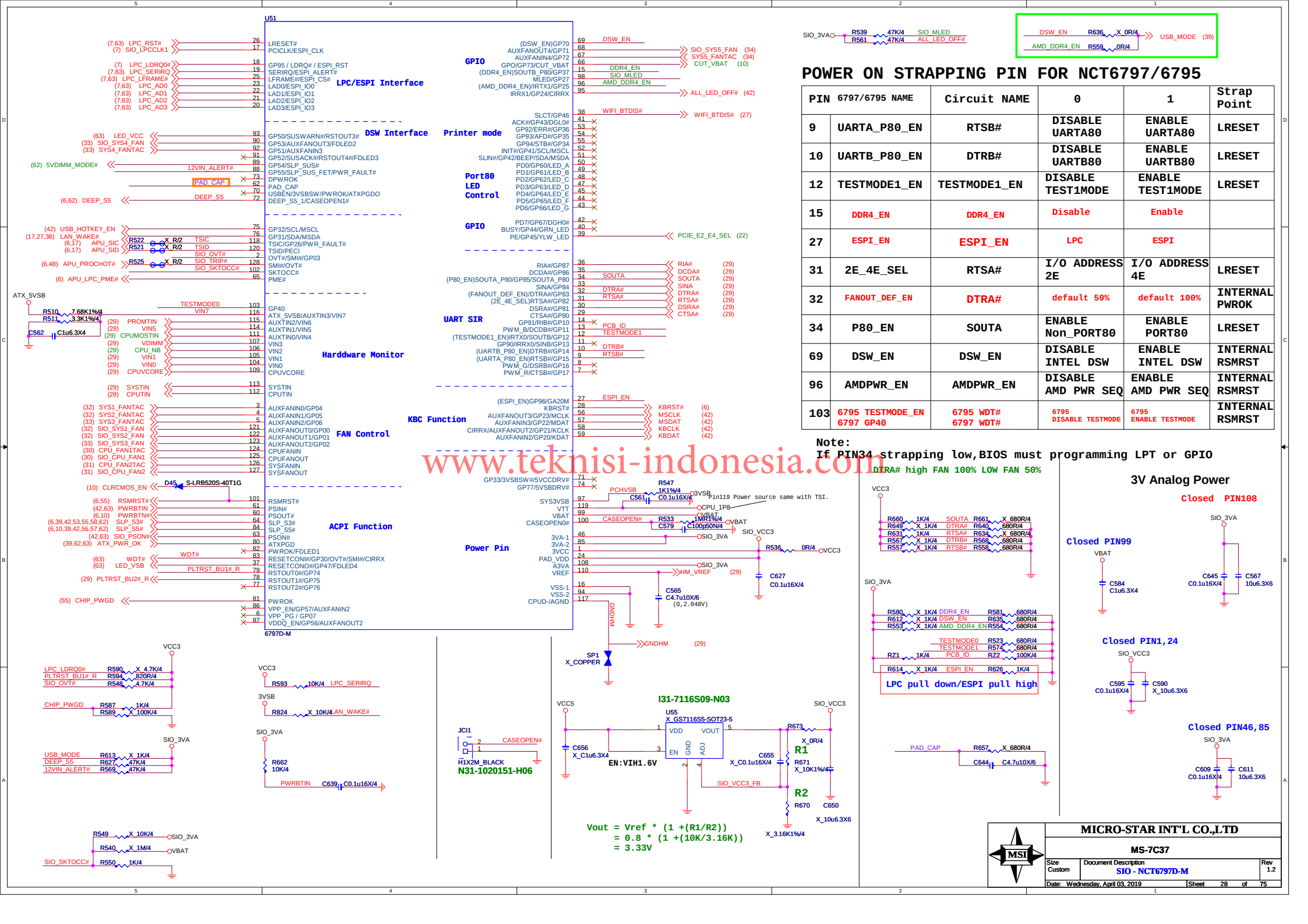

POWER ON STRAPPING PIN FOR NCT6797/6795

PIN	6797/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TESTMODE1_EN	TESTMODE1_EN	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ESPI_EN	ESPI_EN	LPC	ESPI	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DTRA#	default 50%	default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	6795 TESTMODE_EN 6797 GP40	6795 WDT# 6797 WDT#	6795 DISABLE TESTMODE	6795 ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

DTRA# high FAN 100% LOW FAN 50%

3V Analog Power

Closed PIN108

Closed PIN99

Closed PIN1,24

Closed PIN46,85

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MS-7C37	
Size: Custom	Document Description: SIO - NCT6797D-M
Rev: 1.2	
Date: Wednesday, April 03, 2019	Sheet 28 of 75

HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect

R718 Close to CPU or PWM

VCC_DDR R516 10K1%/4 (6,48) VDDCR_CPU_SENSE+ VDIMM (28) → CPU_DRAM
R517 10K1%/4
C568 10u6.3X6

VCORE1 → R718 10K1%/4 → R719 0R/4 → CPUVCORE (28) → CPU_CORE
VCORE R502 X_10K1%/4
R515 X_10K1%/4
C566 10u6.3X6

+12V R505 220K1%/4 → VIN0 (28)
R520 20K1%/4
C571 C0.1u16X/4

VCC5 R504 12K1%/4 → VIN1 (28)
R519 3K1%/4
C570 C0.1u16X/4

Power Fault detect through VIN0,VIN1,VIN2

CPU_VDDP R512 10K1%/4 → VIN5 (28) → CPU_VDDP
C563 10u6.3X6

Inform BIOS disable VIN2 with Power Fault

VCCP_NB R503 10K1%/4 → CPU_NB (28) → CPU_SOC
R518 X_10K1%/4
C569 10u6.3X6

TEMP SENSOR

For CPU

R501 10K1%/4
RT6 10KT1%/4
C547 C2200p50X/4
HM_VREF (28)
CPUTIN (28)
GNDHM (28)
Under Socket

For System

Q90
C564 C2200p50X/4
SYSTIN (28)
GNDHM
P-3906

R514 10K1%/4
RT7 10KT1%/4
C546 C2200p50X/4
HM_VREF (28)
PROMTIN (28)
GNDHM (28)
Under FCH1 BOTTOM

R513 10K1%/4
RT4 10KT1%/4
C553 C2200p50X/4
HM_VREF (28)
CPUMOSTIN (28)
GNDHM (28)
Close to CPU MOS

COM PORT

VCC3
R689 X_2.7K/4 SINA
R707 X_2.7K/4 CTSA#
R713 X_2.7K/4 RIA#
R685 X_2.7K/4 DCDA#
R694 X_2.7K/4 DSRA#
NO USE UART PORT1

C672 X_C0.1u16X/4
VCC5
U57 GD75232DBR
I95-7523212-T07
NRIA NCTSA# NDSRA# NSINA NDCDA#
RTSA# DTRA# SOUTA
+12V_COM RIA# CTSA# DSRA# SINA DCDA#
-12V_COM NDTRA NSOUTA
C670 0.1u25X4
D50 1N4148W +12V
D48 1N4148W -12V
C654 C0.1u16X/4

JCOM1 H2X5[10]M
N31-2051331-H06
CN2 X_8P4C-470p50X/6
CN1 X_8P4C-470p50X/6

PM RESET

SIO (28) PLTRST_BU2#_R → R595 X_22R1%/4 → PLTRST_BU2#
R464 100R1%/4 PLTRST_BU2#_PCIE2 (22)
R470 100R1%/4 PLTRST_BU2#_PCIE3 (21)
R537 100R1%/4 PLTRST_BU2#_PCIE4 (22)
R668 100R1%/4 PLTRST_BU2#_PCIE5 (22)
R573 100R1%/4 PLTRST_BU2#_M2_2 (26)
R83 100R1%/4 PLTRST_BU2#_M2_3 (27)
R387 100R1%/4 PLTRST_BU2#_LAN (36)
R571 100R1%/4 PLTRST_BU2#_ASM1061 (23)

3VSB
C0.1u16X/4 C784
U72 NC7SZ08M5X
PM
(28) PLTRST_BU2#_R
(17) PM_GPP_RST
VCC3
R846 4.7K/4
R845 X_0R/4
R827 0R/4
PLTRST_BU2#

NCT7718W

Near to M2_1

10u6.3X6 C421
C0.1u16X/4 C424
C425 C2200p50X/4
VCC3
U30 SNSR-NCT7718W-HF
VDD D+ D- T_CRIT# SCL SDA ALERT# GND
SCLK0 (6,10,11,35,42,48,60,65)
SDATA0 (6,10,11,35,42,48,60,65)
ALERT#
R384 14KR1%0402 VCC3
R385 18.7K1%04 TCRIT#

NCT7718W SM Bus address is 98h (1001100xb)

Default: ALERT# Output Comparator Mode

Near to PCI_E1 Slot

Q76 N-SST3904
D+
D-

Layout notice:
1. Put the C1 2200pF to close the NCT7718W.
2. Add Ground Shielding For D+ and D- Traces.
3. D+/D- Route Has to be Away From the High Noise Area.
4. The Recommended Traces Width and Ground Shielding Spacing are 10mils.

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

CPU RESET

3VSB
X_C0.1u16X/4 C544
U44 X_NC7SZ08M5X
(6) PCIE_REST#
VCC3
R499 X_4.7K/4
PCIE_RST_BUF
R473 100R1%/4 PLTRST_BU1#_PCIE1 (20)
R475 100R1%/4 PLTRST_BU1#_M2_1 (25)
R480 100R1%/4 PCIERST#_PM (17)
PCIE_REST# R478 X_R/2 PCIE_RST_BUF

teknisi indonesia

SIO_3VA

ATX_5VSB
C541 C1u6.3X4
I31-7116S09-N03
U46 GS7116S5-SOT23-5
VDD VOUT EN GND ADJ
EN:VIH1.6V
C545 X_C0.1u16X/4
R1 R497 10K1%/4
R2 R488 3.16K1%/4
3VA_FB
SIO_3VA
C551 10u6.3X6

Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V

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Size: Custom
Document Description: SIO - HW Monitor / NCT7718W
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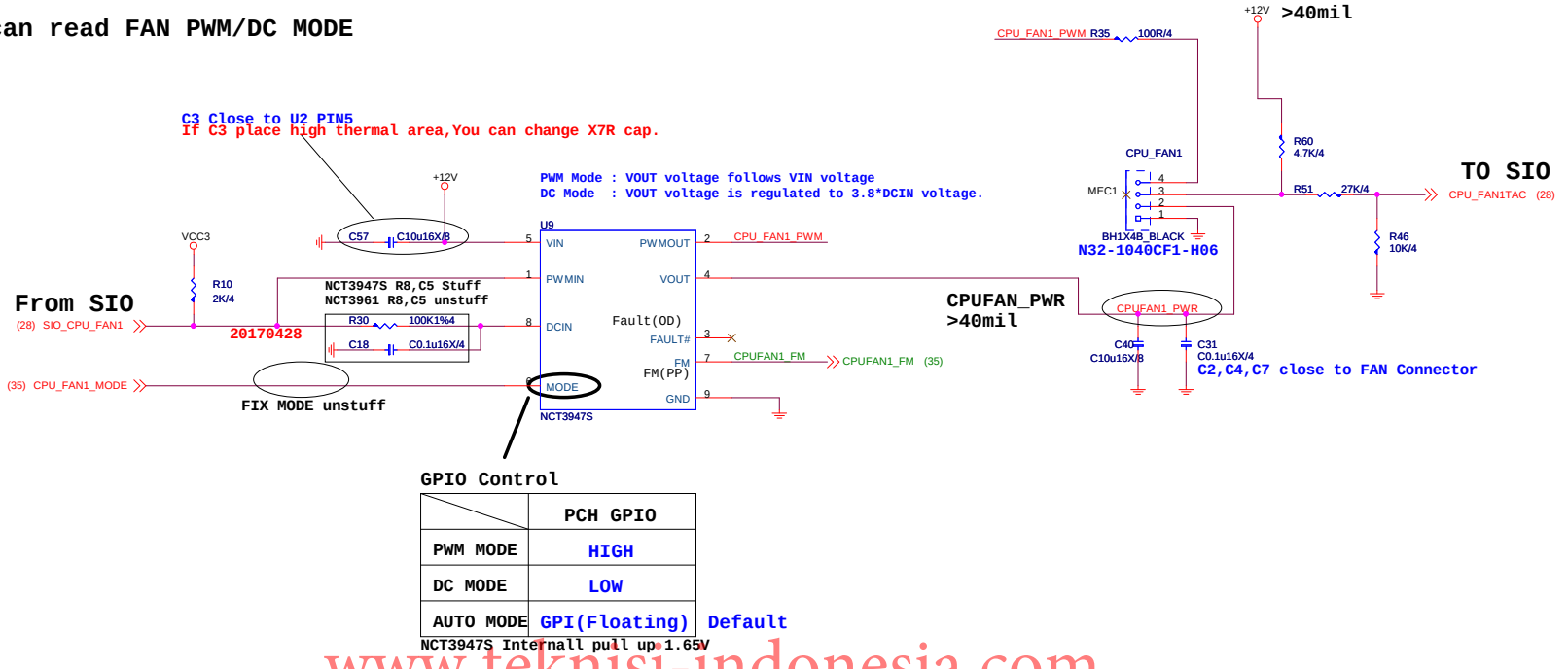
TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

CPUFAN1

1.Mode GPIO BIOS can swtich PWM/DC MODE

2.FM:BIOS can read FAN PWM/DC MODE



GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating) Default

NCT3947S Internall pull up 1.65V

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Size: Custom	Document Description: FAN TYPE-L CPUFAN1
Rev: 1.2	
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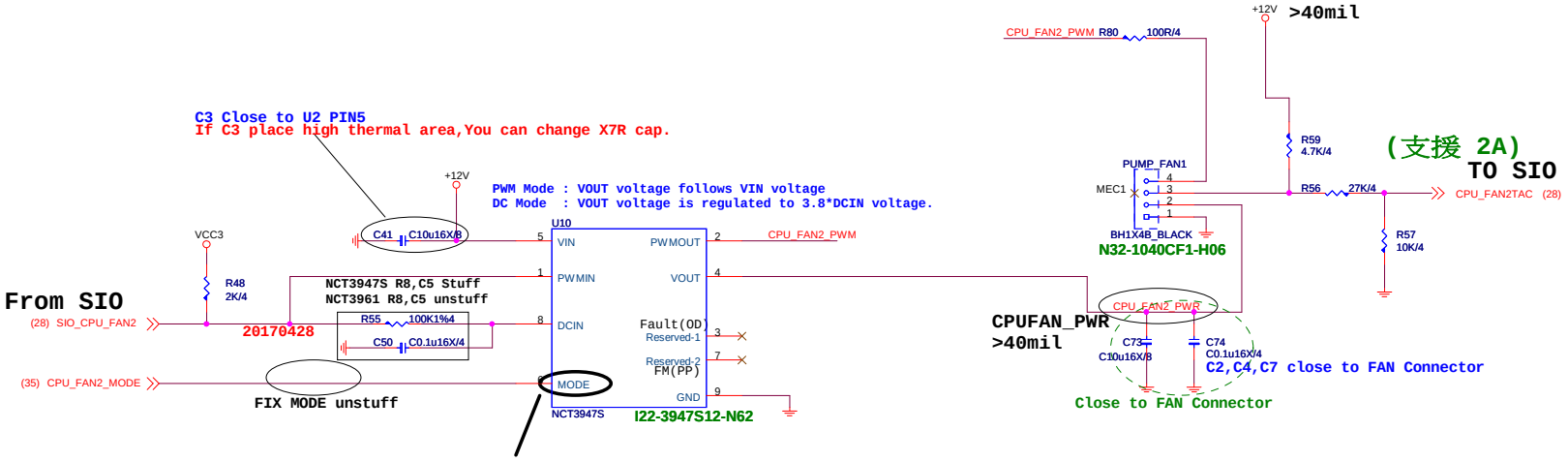
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

PUMPFAN1

1.Mode GPIO BIOS can swtich PWM/DC MODE



GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating) Default

NCT3947S Internall pull up 1.65V

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Size: Custom	Document Description: FAN TYPE-K PUMPFAN1	Rev: 1.2
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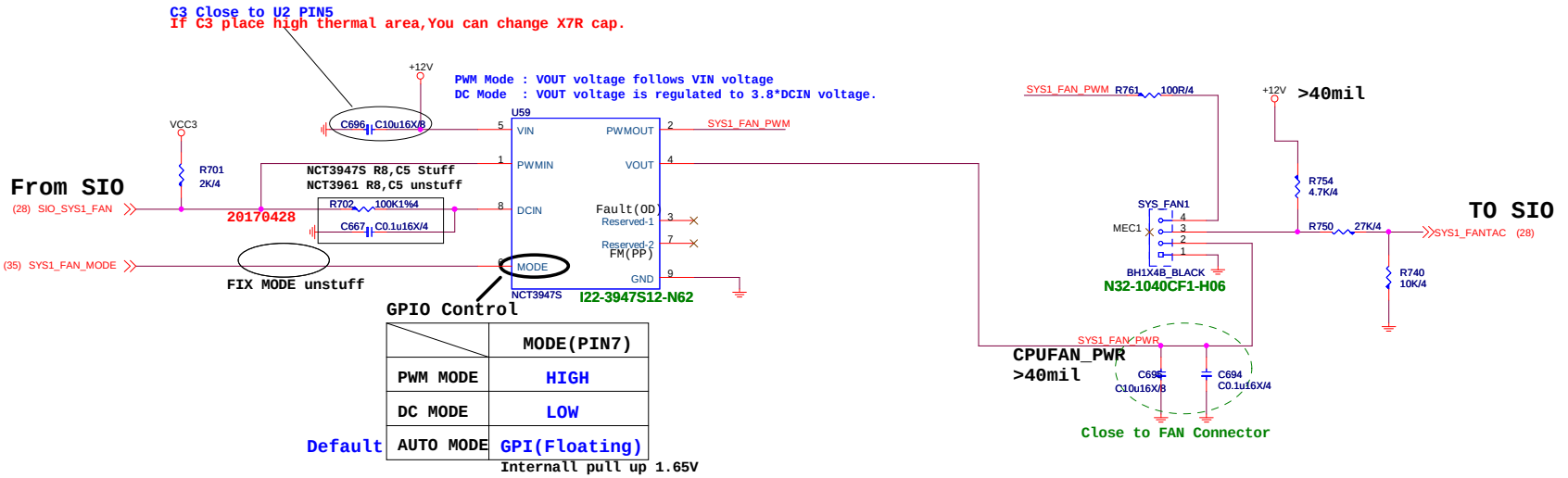
SYSFAN1

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

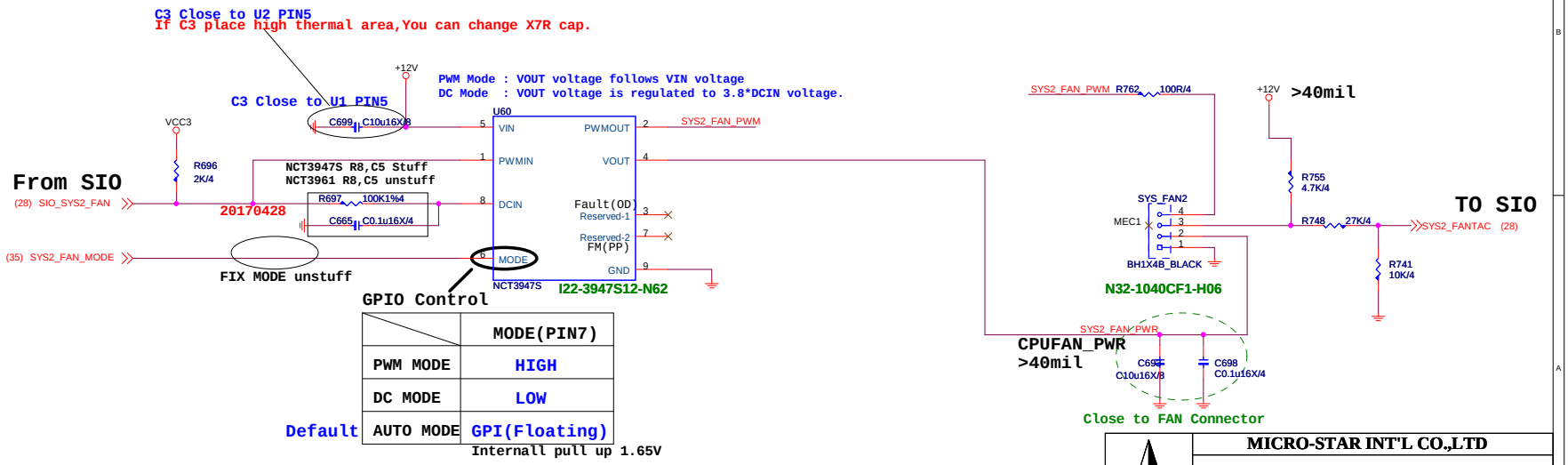
1.Mode GPIO BIOS can swtich PWM/DC MODE



SYSFAN2

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



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MS-7C37

Size	Document Description	Rev
Custom	FAN TYPE-K SYSFAN1/2	1.2

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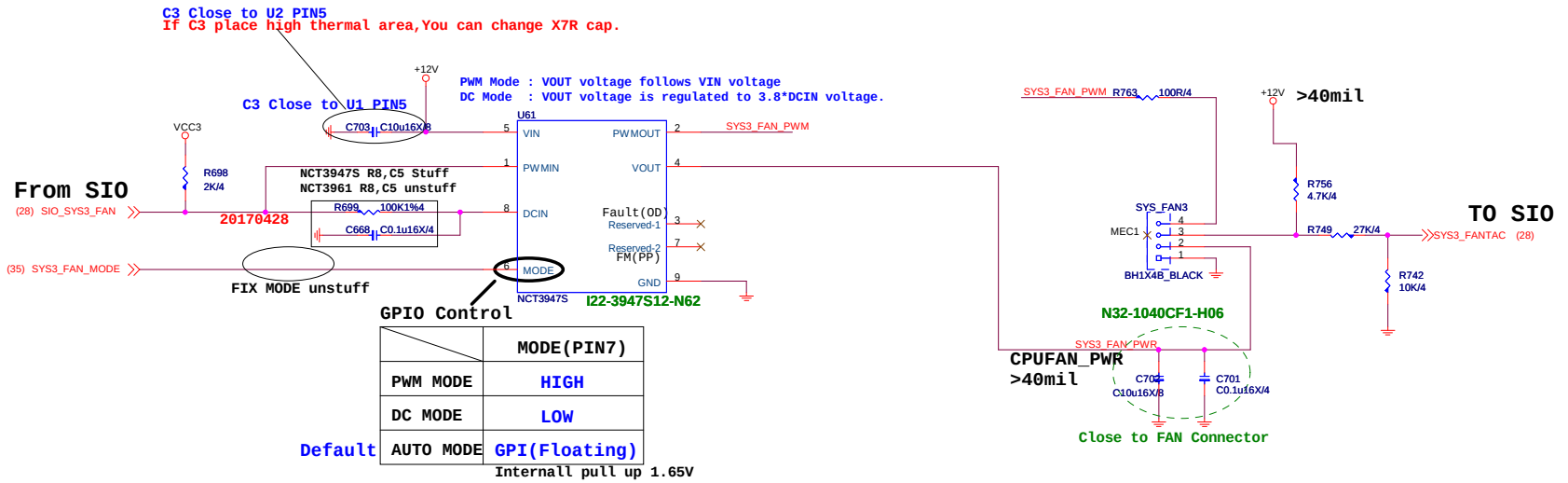
SYSFAN3

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

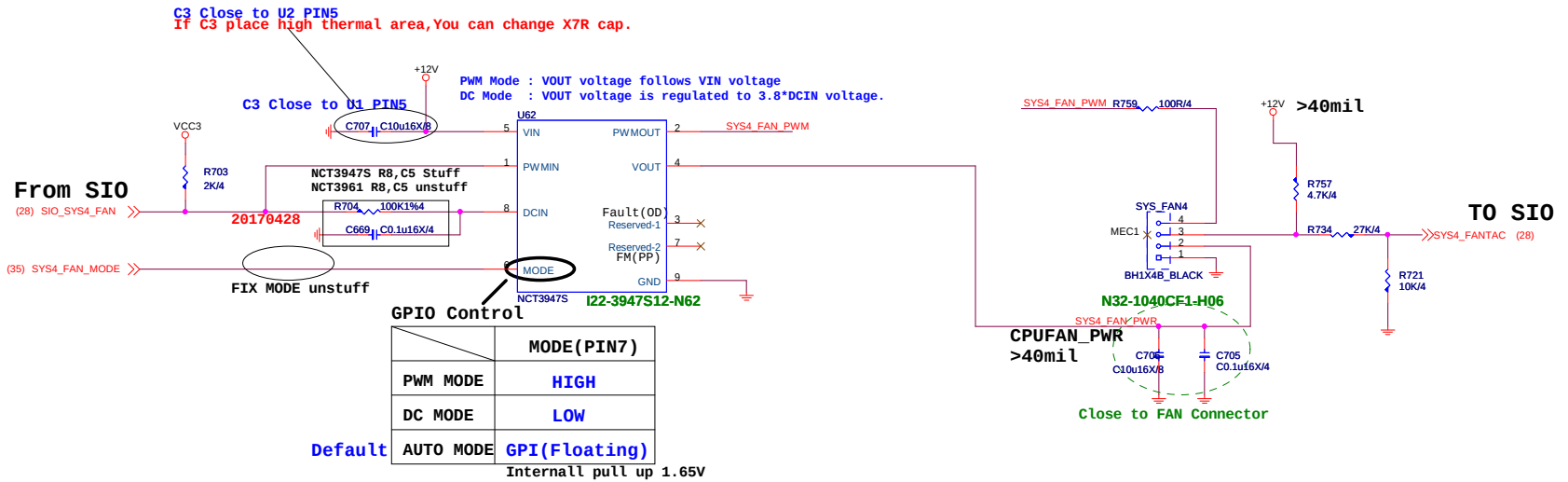
1.Mode GPIO BIOS can swtich PWM/DC MODE



SYSFAN4

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



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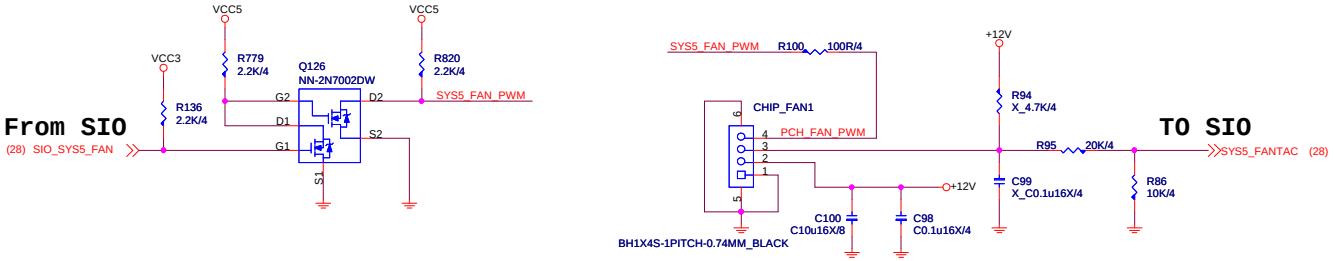
MS-7C37	
Size: Custom	Document Description: FAN TYPE-K SYSFAN3/4 — Rev: 1.2
Date: Monday, April 01, 2019	Sheet 33 of 75

PCH_FAN



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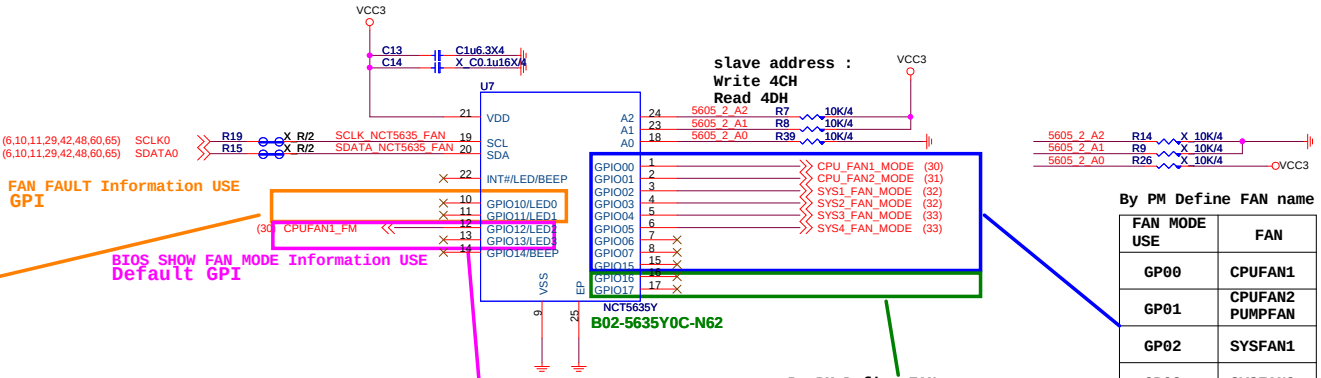
	MS-7C37	
Size: Custom	Document Description: PCH_FAN	Rev: 1.2
Date: Monday, April 01, 2019	Sheet 34 of 75	



By PM Define FAN name

SHOW FAN FAULT USE	FAN
GP10	CPUFAN1
GP11	CPUFAN2 PUMPFAN

By PM Define FAN name

SHOW FAN MODE USE	FAN
GP12	CPUFAN1
GP13	CPUFAN2 PUMPFAN

By PM Define FAN name

LED OFF BLINK	FAN
GP16	CPUFAN1
GP17	CPUFAN2 PUMPFAN

Default GPI

USE LED OFF & LED BLINK

By PM Define FAN name

FAN MODE USE	FAN
GP00	CPUFAN1
GP01	CPUFAN2 PUMPFAN
GP02	SYSFAN1
GP03	SYSFAN2
GP04	SYSFAN3
GP05	SYSFAN4
GP06	SYSFAN5
GP07	EXT_SYS FAN1
GP15	EXT_SYS FAN2

use avoid S5 leakage

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Size: Custom | Document Description: FAN GPIO NCT5635 | Rev: 1.2

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RTL8111H Giga LAN

PIN19:
AMD platform connect to PCIE_RST#,
don't connect to A-RST#.
INTEL platform connect to PLT_RST#,

VDD33 — RL5 X_1K/4 — LAN_WAKE#

Remove pull-up R if R existence on motherboard
(or SB has internal pull-up R).

VCC3 — RL8 1K1%/4 — RL6 15K/4 — ISOLATEB

VDD33@65mA

3VSB — CPL1 (20mil=1A) — 11 32 11 32 — VDD33

CL5 C0.1u16X/4, CL1 C0.1u16X/4, CL4 C4.7u10X6, CL6 C4.7u10X6

For surge improvement

VDD33 width>40mil
VDD10 width>60mil

VDD10@150mA

VDD10 — 3 22 22 24 8 30

CL2 C0.1u16X/4, CL12 C0.1u16X/4, CL13 X_C1u6.3X4, CL14 C0.1u16X/4, CL3 C0.1u16X/4, CL7 C0.1u16X/4

UL3 RTL8111H — B06-08111CC-R09

PCIE interface:
- (15) PE_LAN_TXP — CL10 0.22u10X4 PE_LAN_TXP_C — HSIP
- (15) PE_LAN_TXN — CL11 0.22u10X4 PE_LAN_TXN_C — HSIN
- HSOP — PE_LAN_RXP_C — CL16 0.22u10X4 — PE_LAN_RXP (15)
- HSON — PE_LAN_RXN_C — CL15 0.22u10X4 — PE_LAN_RXN (15)
- (17) LAN_CLKP — LAN_CLKP — REFCLK_P
- (17) LAN_CLKN — LAN_CLKN — REFCLK_N
- PERSTB — PLTRST_BU2# LAN
- CLKREQB — LAN_CLKREQ# — C422 X_C100p50N/4 — PLTRST_BU2#_LAN (29)

PM:
- (17,27,28) LAN_WAKE# — LAN_WAKE# — ISOLATEB — ISOLATEB
- LANWACKEB

Regulator & Power:
- RL1 2.49K1%/4 — RSET
- VDD33 — VDDREG, AVDD33-1, AVDD33-2
- VDD10 — REGOUT, DVDD10, AVDD10-1, AVDD10-2, AVDD10-3
- GND

Transceiver Interface:
- MDIP0/MDIN0 — TR_D0+/TR_D0-
- MDIP1/MDIN1 — TR_D1+/TR_D1-
- MDIP2/MDIN2 — TR_D2+/TR_D2-
- MDIP3/MDIN3 — TR_D3+/TR_D3-

EEPROM:
- LED0 — LED0
- LED1/GPO — LED1
- LED2 — LED2

CLOCK:
- CKXTAL1 — CLK_LANI — CL9 C22p50N4 — YL1 25MHZ18P
- CKXTAL2 — CLK_LAN0 — CL8 C22p50N4

D04-1000201-F07

Pin33: 4 via from top layer to GND layer
and make the via at the center of IC.

Pull-up resister RL9 required to either
3.3V suspend or core rail depending on
the power well of the PCH input CLKREQ# buffer.

3VSB — RL2 X_10K/4 — LAN_CLKREQ# — RL4 0R/4 — CLKREQ2 (17)
RL3 X_10K/4

next ver. CLKREQ1 neet to pull VCC3

LAN Connector

VDD33 — For EMI — RL10 100R/4 — CL18 C0.1u16X/4

LED2 — RL9 220R/4 — LED2_ACT
LED1 — RL11 220R/4 — LINK1000#
LED0 — RL12 100R/4 — LINK100#
For EMI

Main:D0G-1020530-I05
AVL:D0G-8010510-SI0
D0G-1020530-I05

DL1 CL22 C0.1u16X/4 — ESD-VPORT0603L102KV05

LAN_USB1B
YELLOW+ / YELLOW-
POWER
TD1+ TD1- TD2+ TD2- TD3+ TD3- TD4+ TD4-
GND
GREEN+/ORANGE- / GREEN-/ORANGE+
RJ45_USBX2_LEDX2

N58-32F0721-F02

For EMI

LED2_ACT — CL17 X_C100p50N/4
LINK1000# — CL19 X_C100p50N/4
LINK100# — CL20 X_C100p50N/4

ESD Protect
close to connector

D0G-0200529-A68
D0G-0100619-I05

UL1: TR_D0- TR_D0+ TR_D1- TR_D1+ — ESD-AOZ8906CI — D0G-05A0529-A68
UL2: TR_D2- TR_D2+ TR_D3- TR_D3+ — ESD-AOZ8906CI — D0G-05A0529-A68

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

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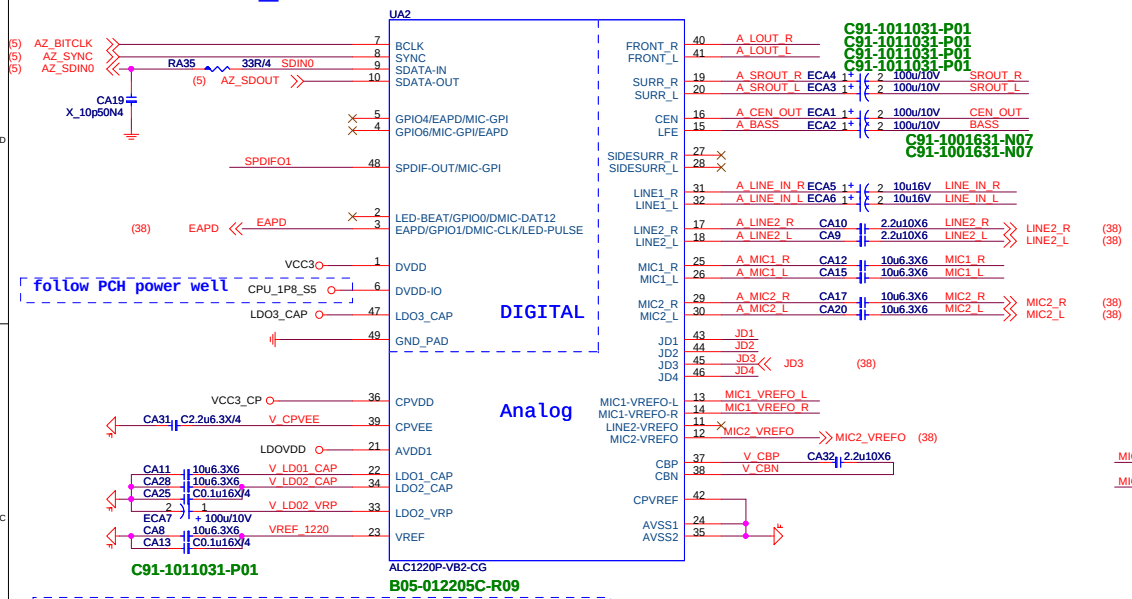
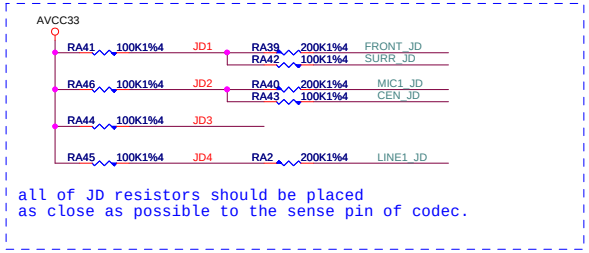
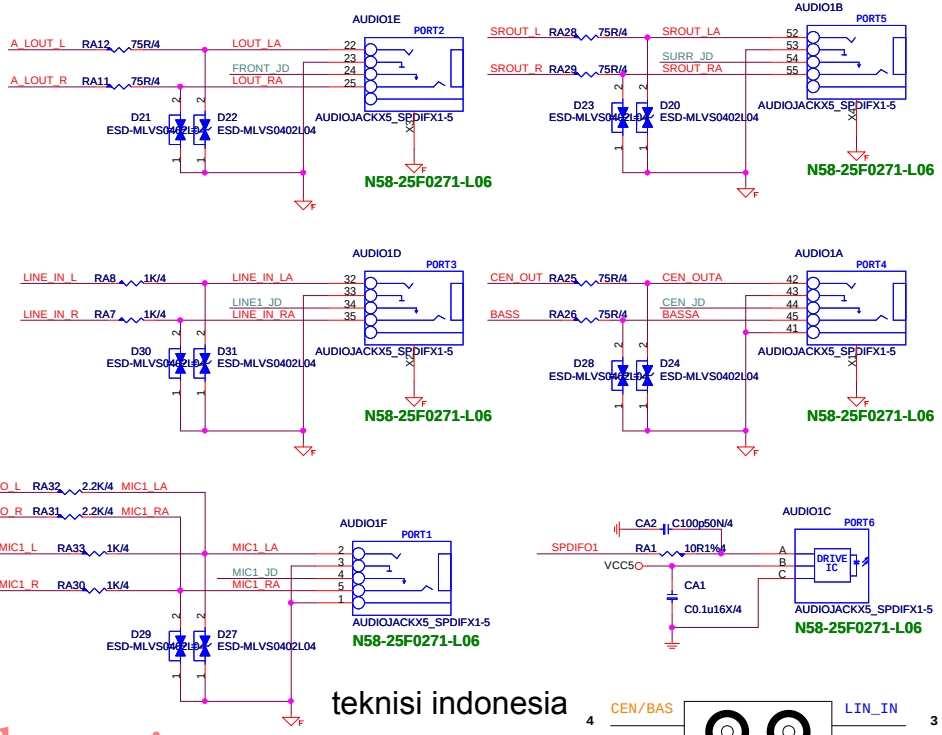
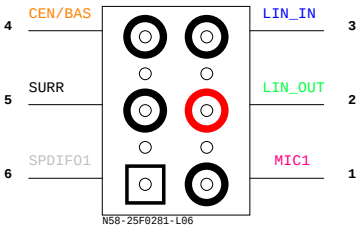
ALC1220P-VB2_48PIN

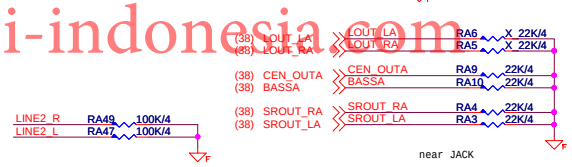


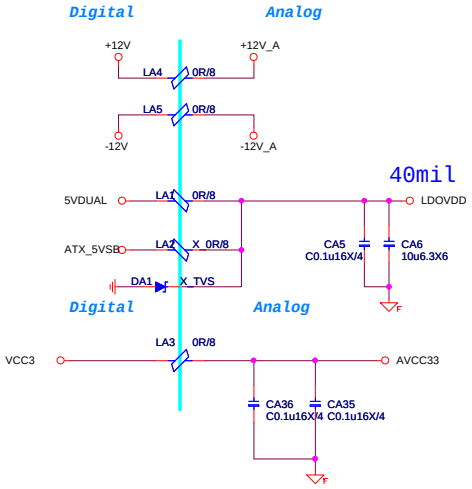


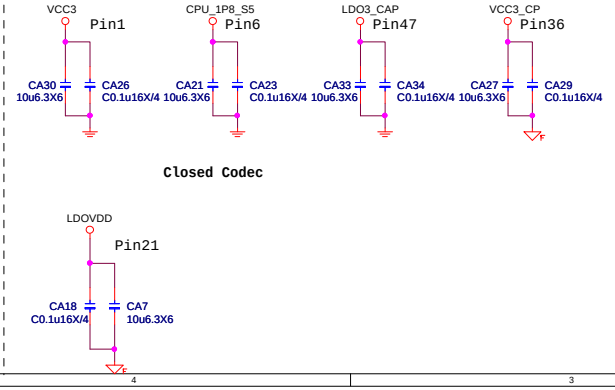


teknisi indonesia

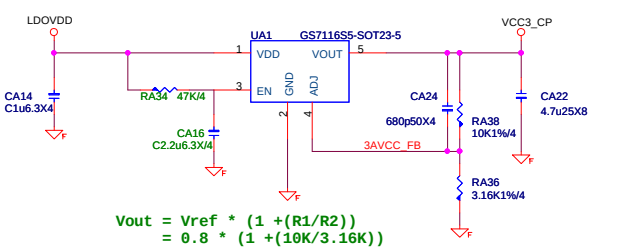








CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V



EMI

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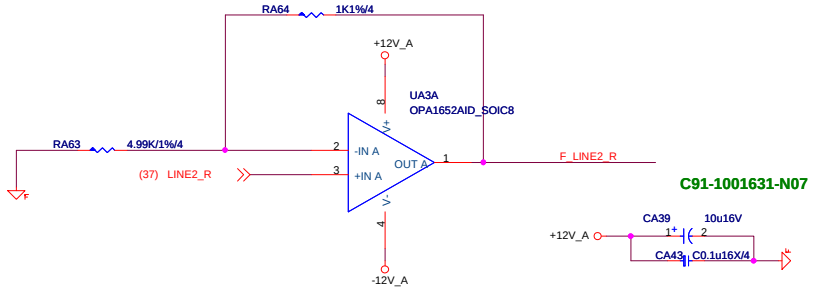
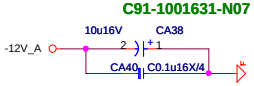
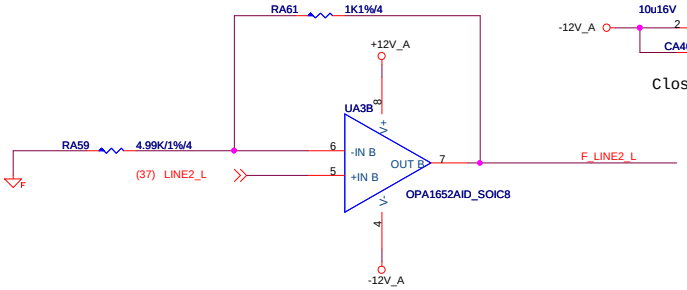


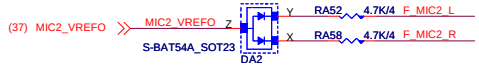
C91-1001631-N07

C91-1001631-N07

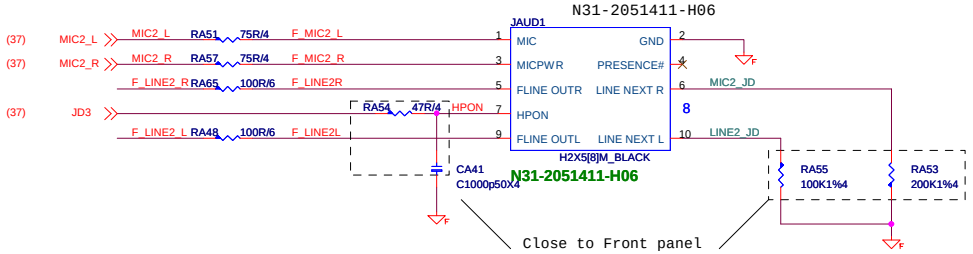


Close to U3





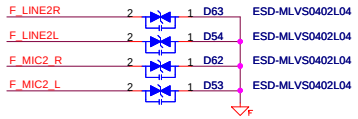
N31-2051411-H06

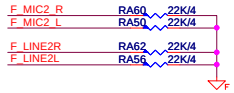


Close to Front panel
For HDA/AC97 front cable.

Close to Jack

ESD protect



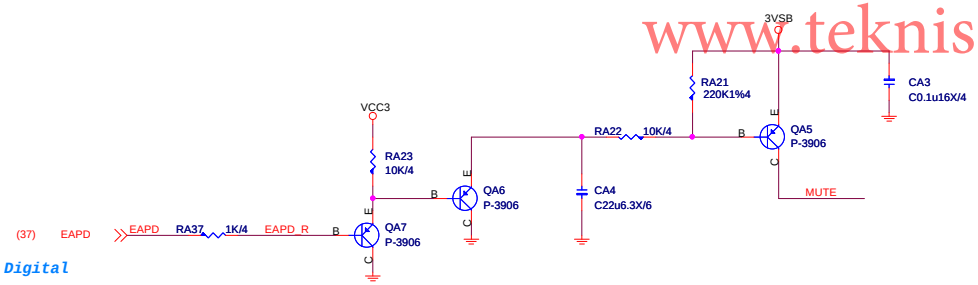


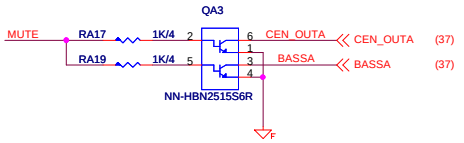
Rear Line OUT De-POP circuit

(De-pop circuit for Rear Line out & Front Headphone out)

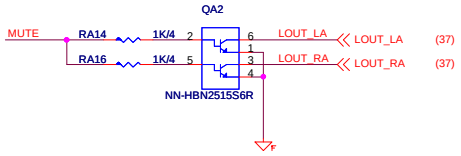
(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change SROUT_LA,SROUT_RA, CEN_OUTA, BASSA to TVS)

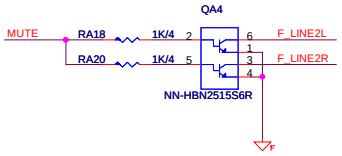
Digital

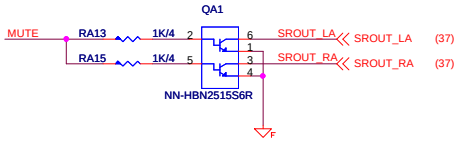




Analog







Audio moat is transparent and width 40mil

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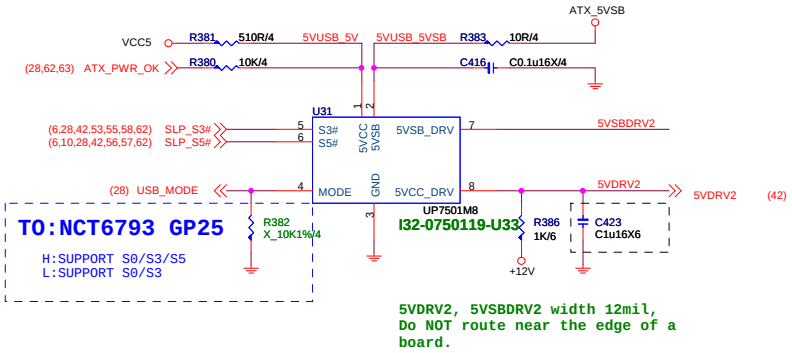
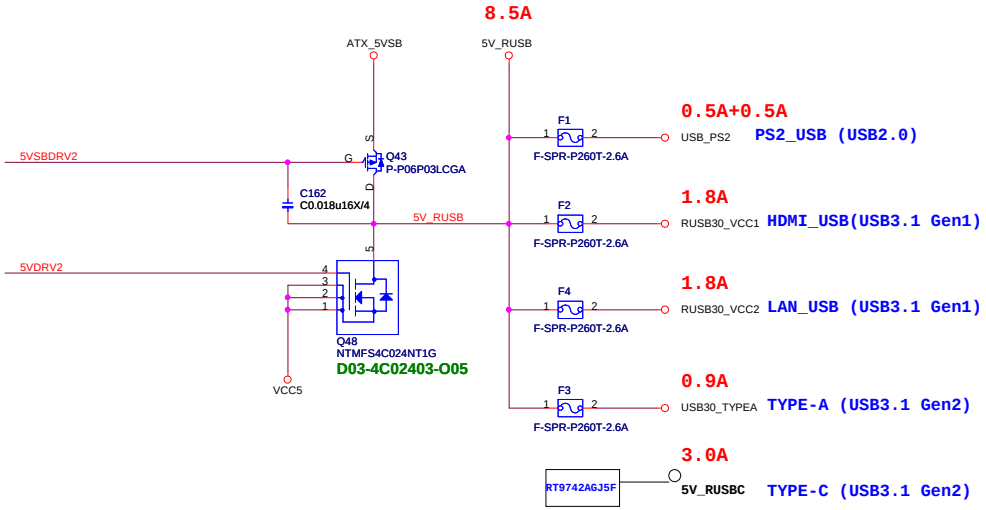
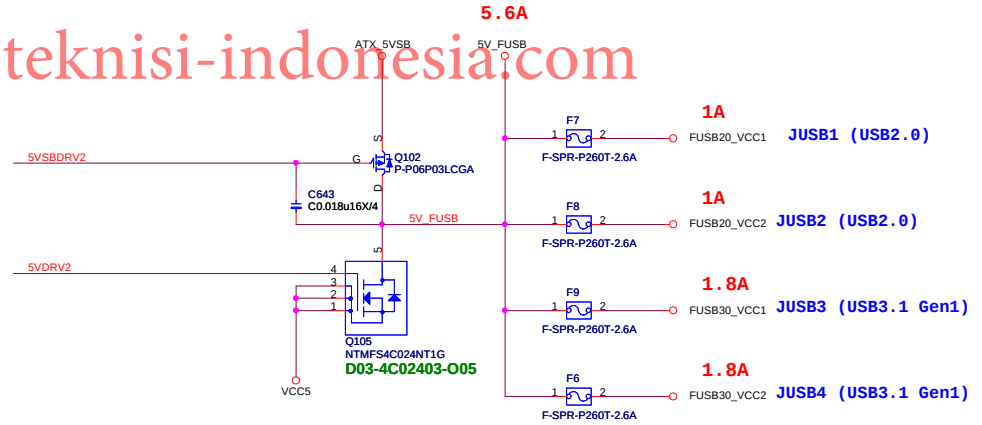
USB Power



Rear USB Port Power



Front USB Port Power



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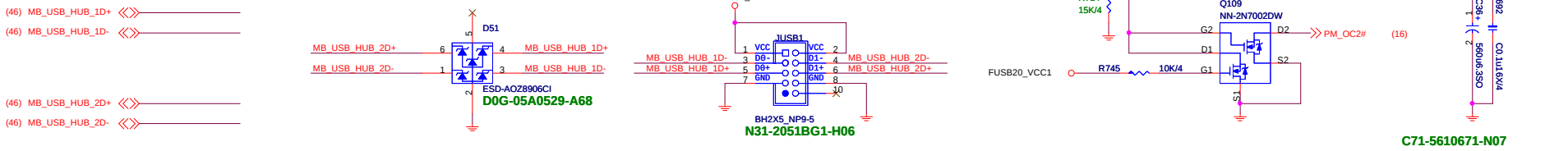
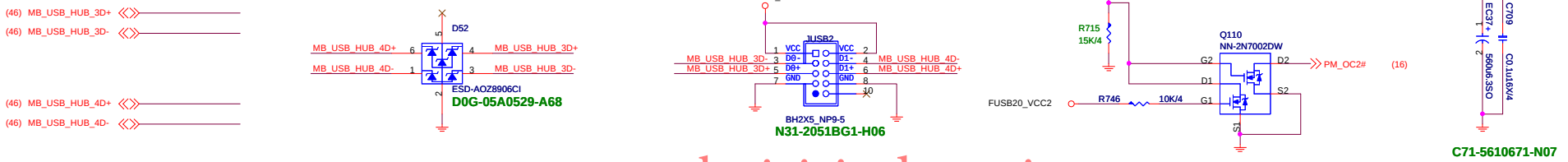
Front USB2.0(JUSB1)



Front USB2.0(JUSB2)



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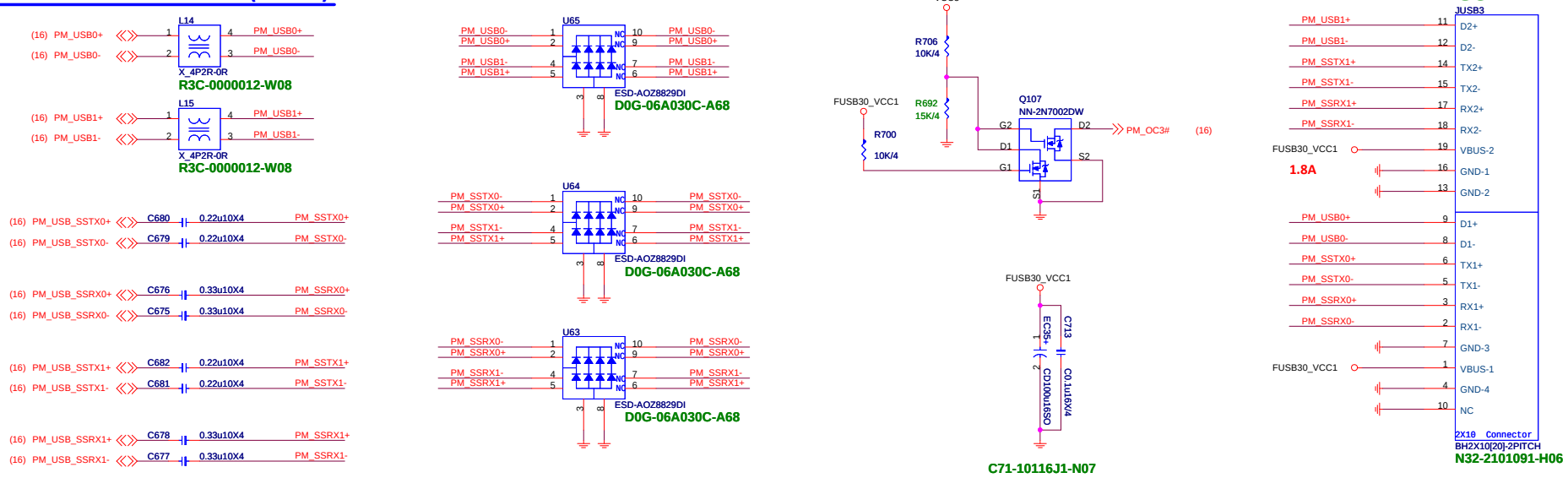
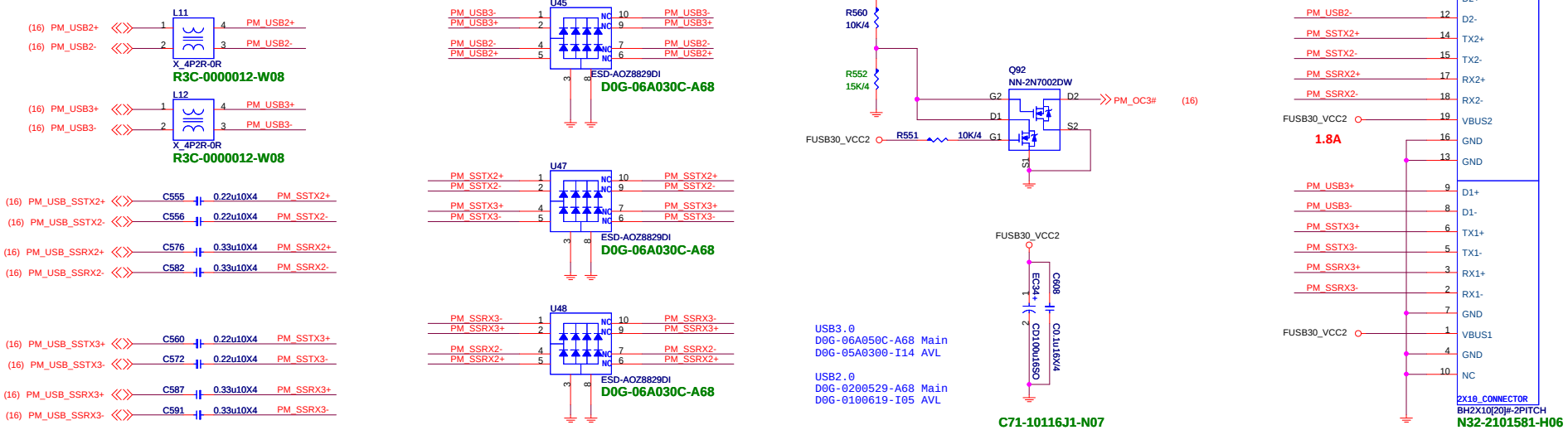
Front USB3 180° BOX Header(JUSB3)



Vinafix.com

Front USB3 90° BOX Header(JUSB4)



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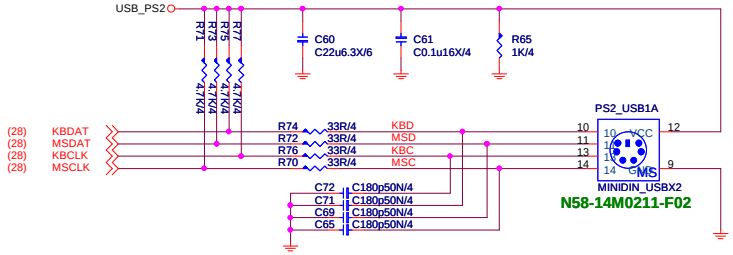
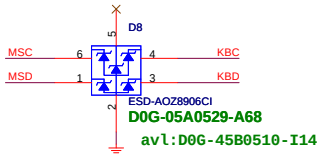
PS2

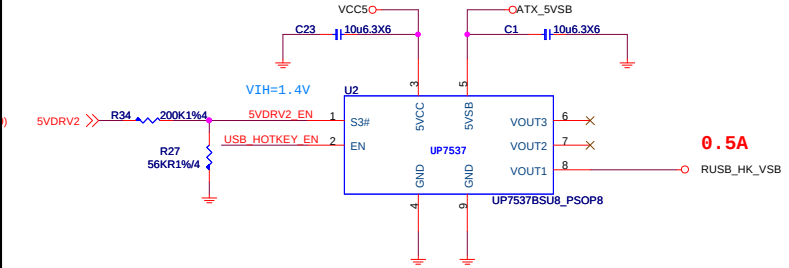
5V@1A

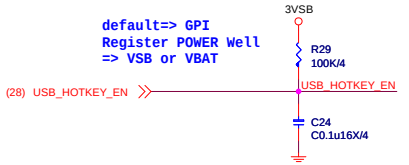
layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch





HOTKEY_POWER

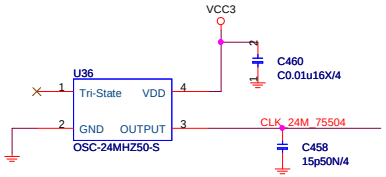


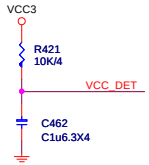


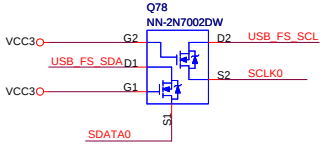
USB2.0 Flash BIOS

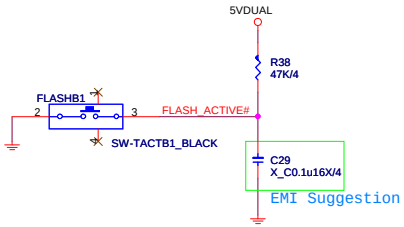
F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.

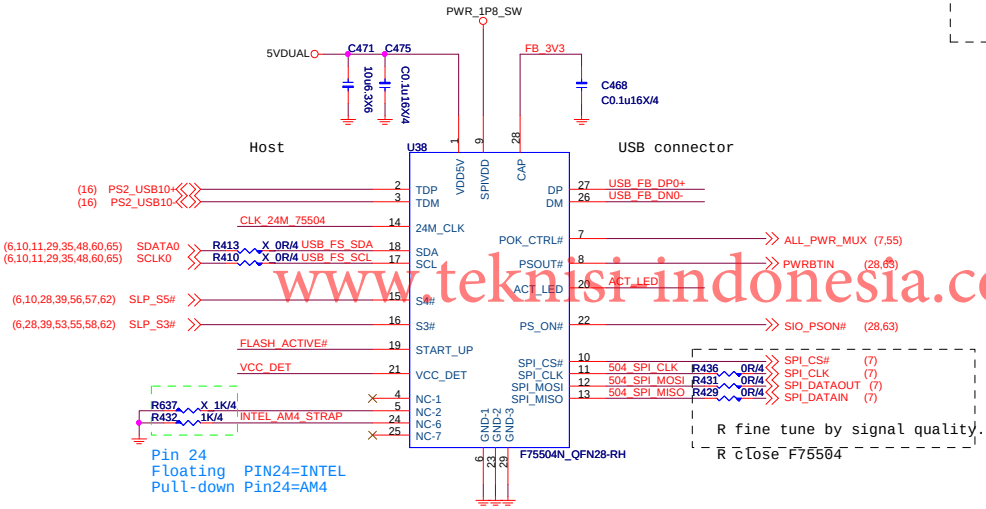
CLK running in S0,don't require in sleep

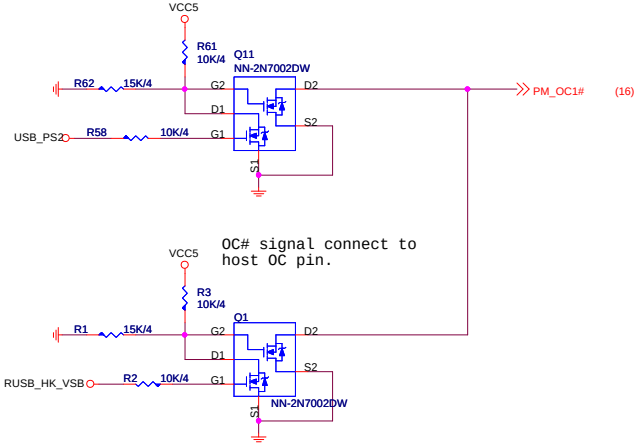


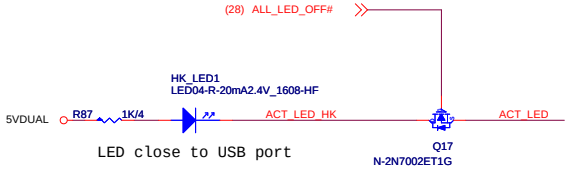


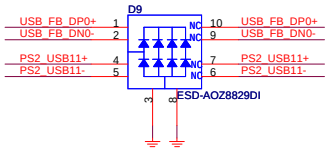


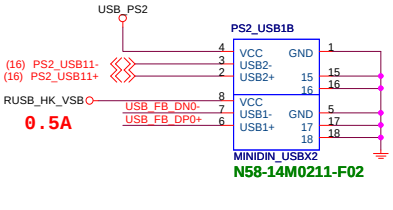


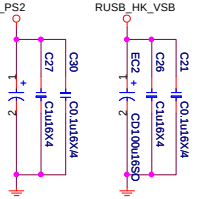












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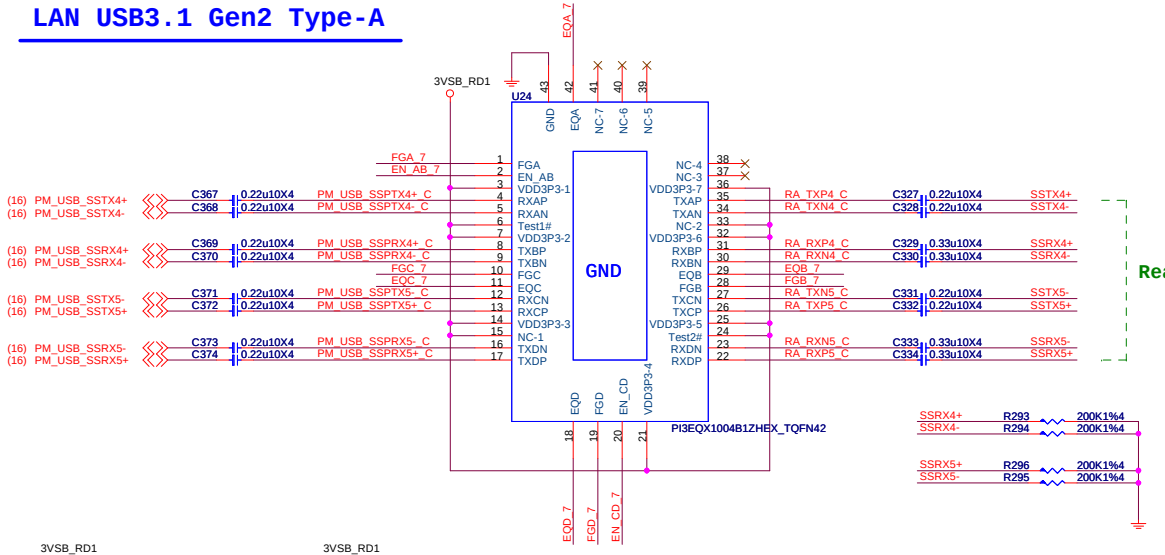
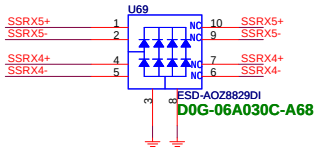
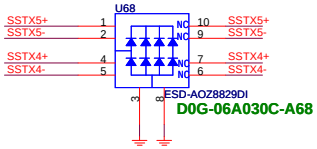
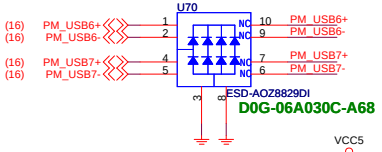
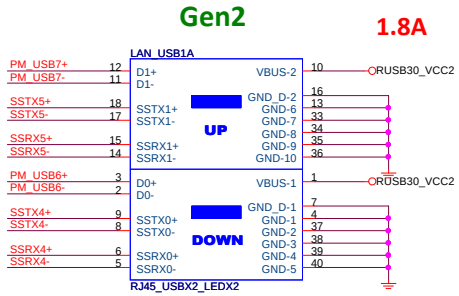
LAN USB3.1 Gen2 Type-A

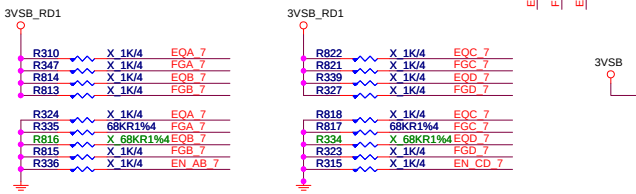


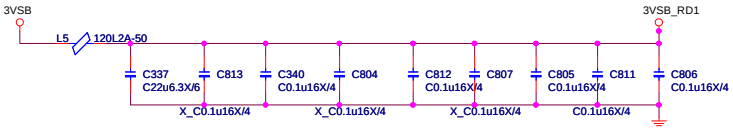


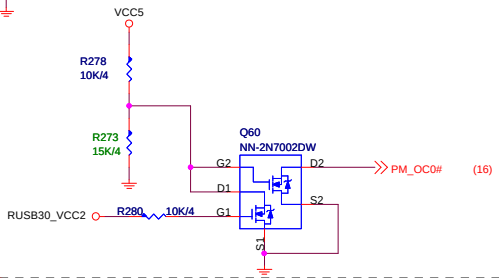




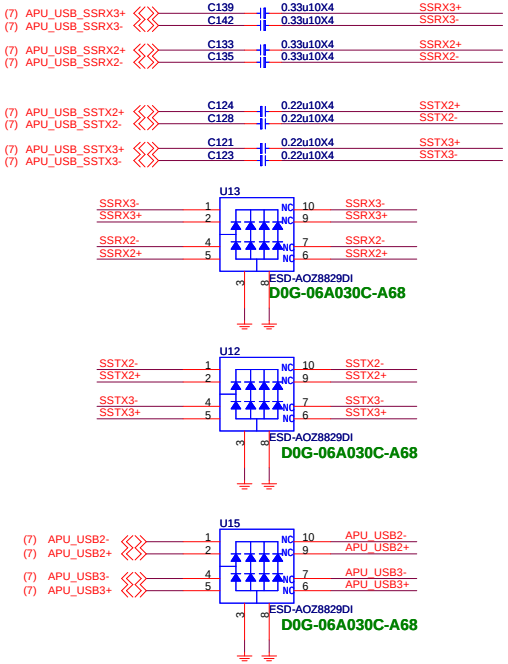


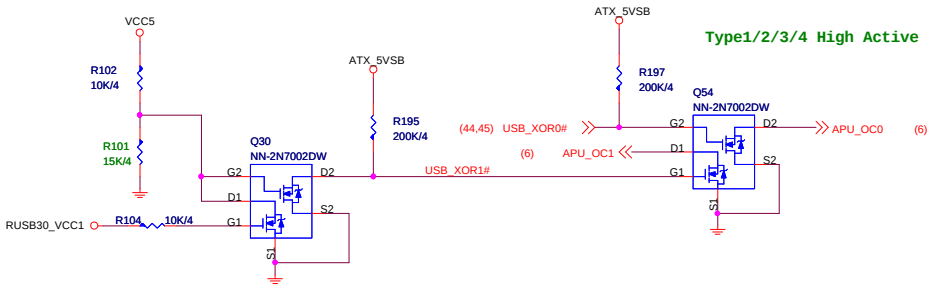


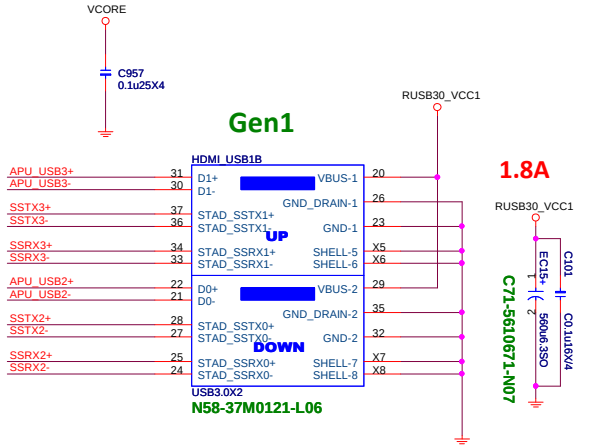




HDMI USB3.1 Gen1 Type-A







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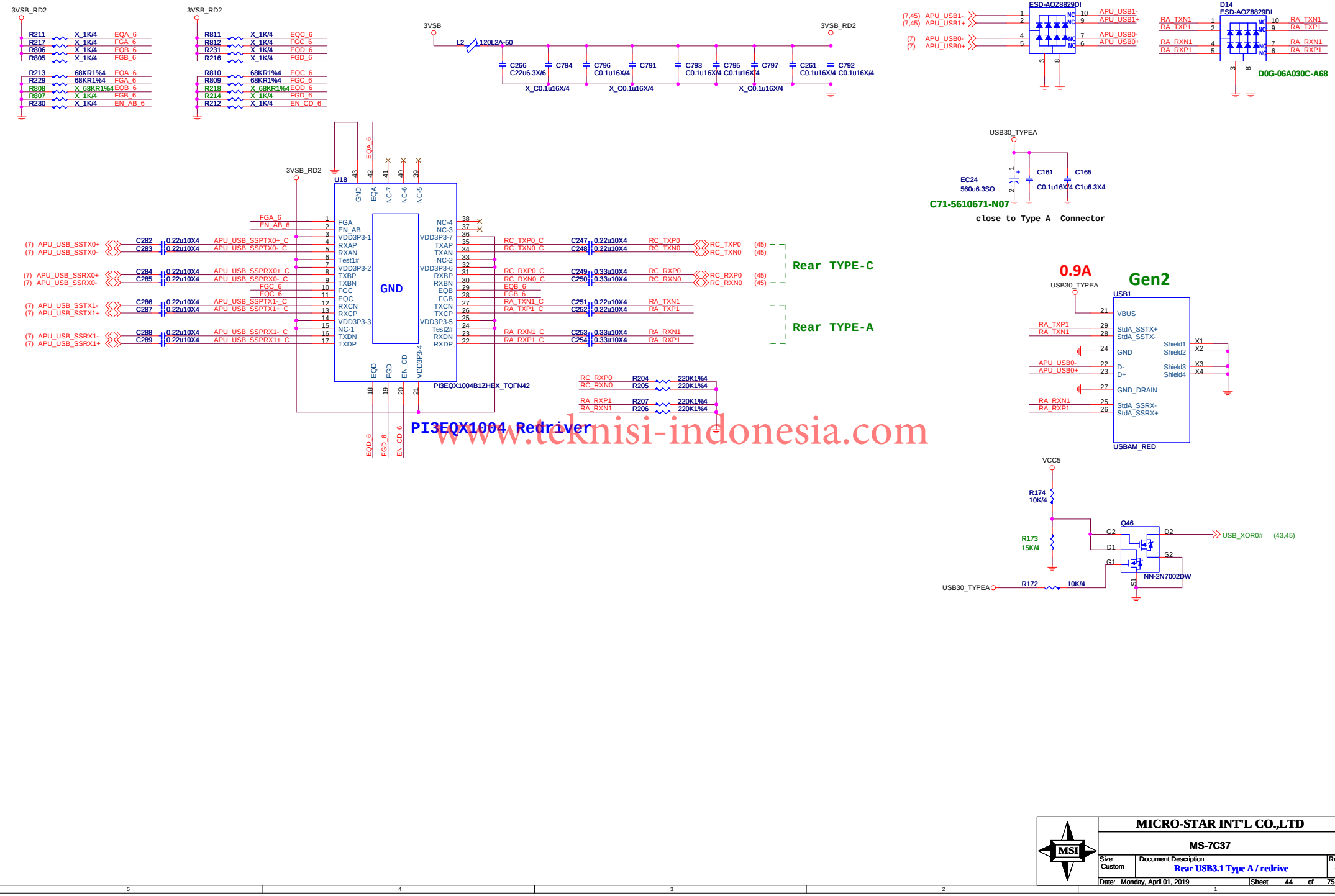
USB3.1 Gen2 Redriver + Type-A



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MS-7C37		
Size: Custom	Document Description: Rear USB3.1 Type A / redrive	Rev: 1.2
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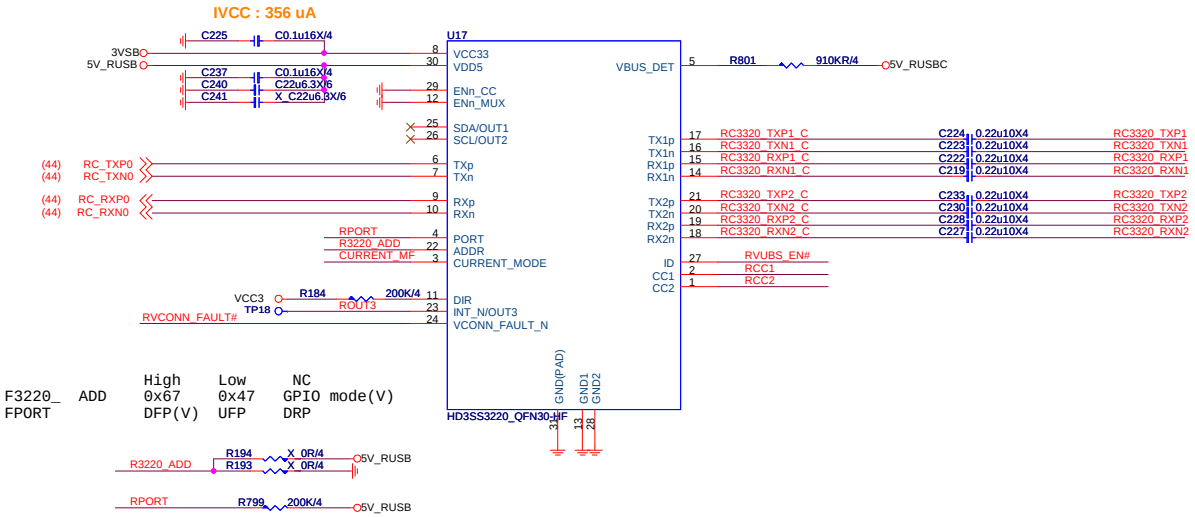
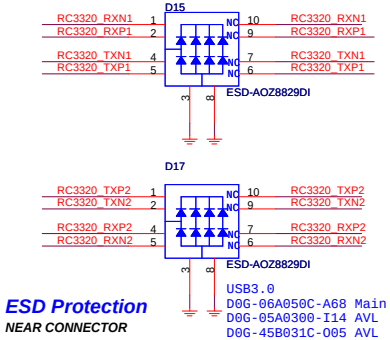
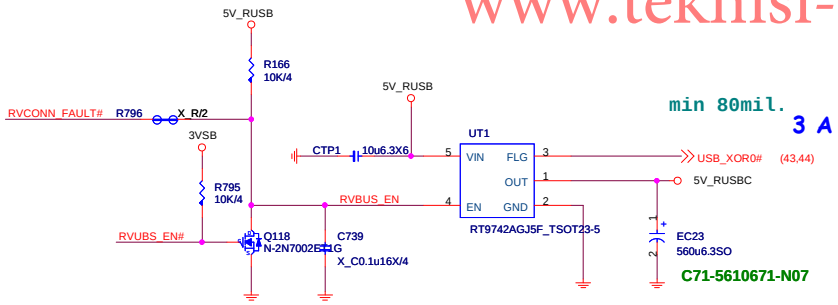
USB3.1 Gen2 Type-C

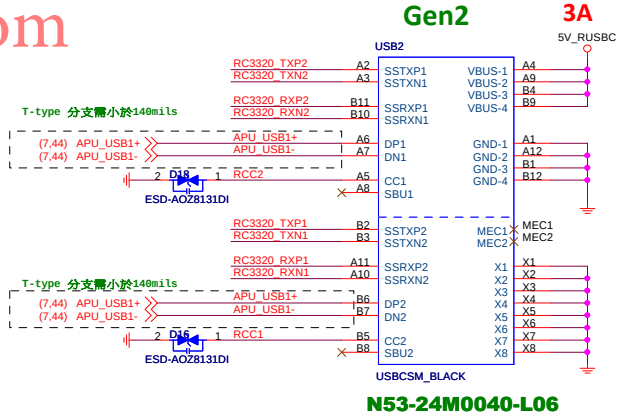
USB Type-C MUX with Configuration Channel (CC)



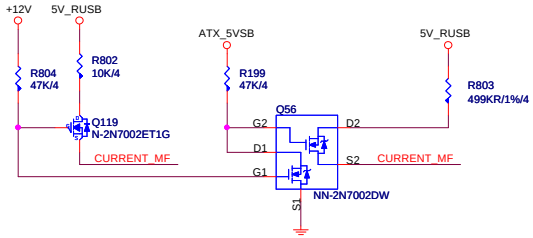


VBUS EN





Current Mode



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MS-7C37	
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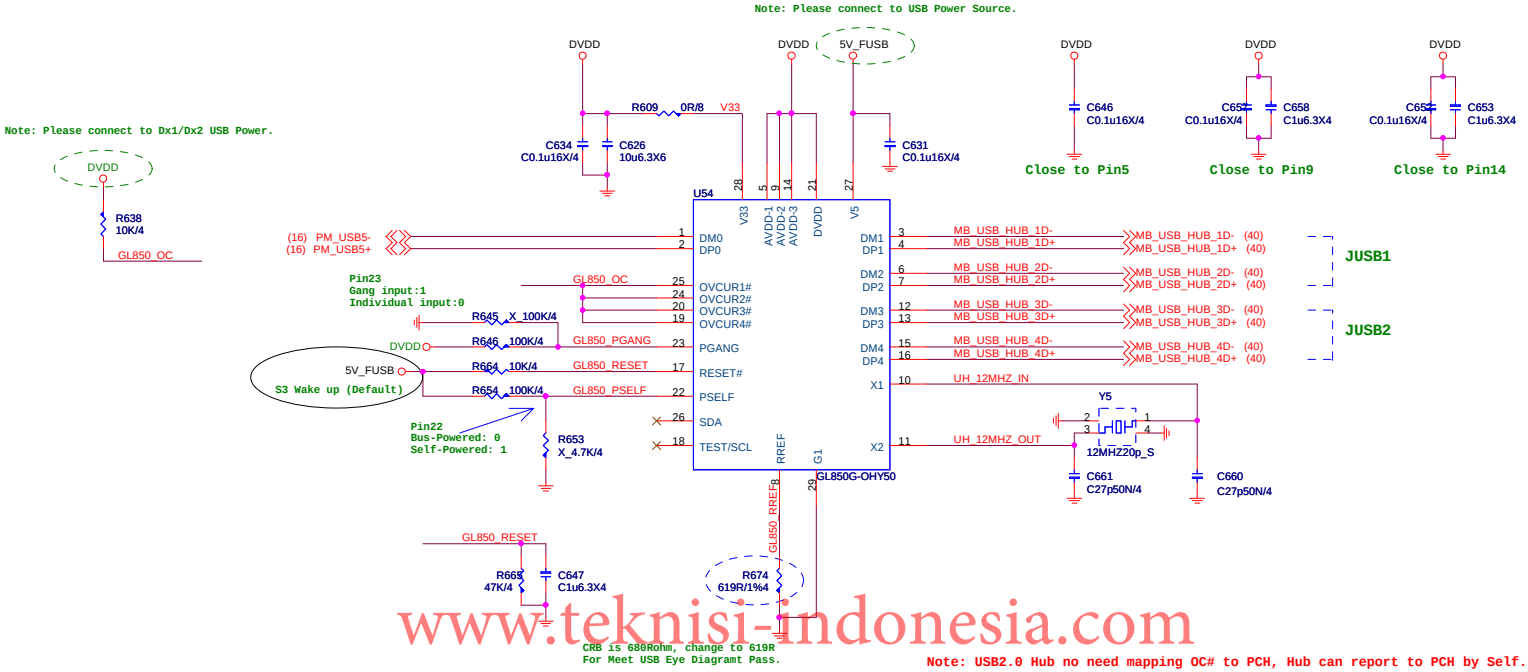
GL850G USB2.0 HUB

5V_FUSB



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Size: Custom	Document Description: GL850G	Rev: 1.2
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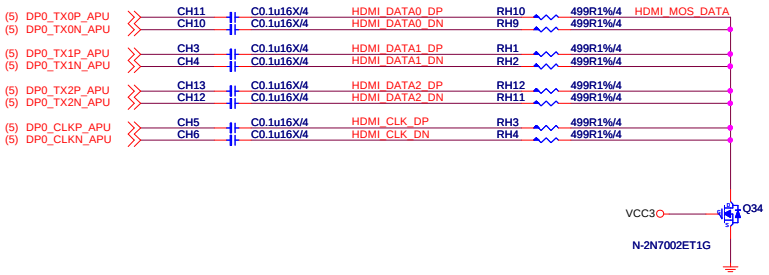
HDMI CONNECTOR

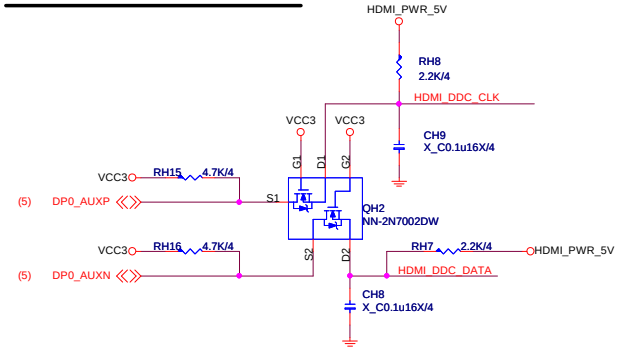
For HDMI 1.4



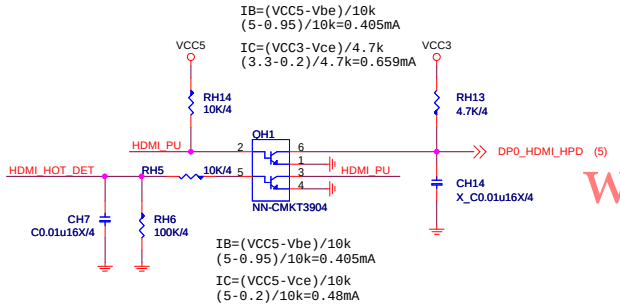
刪除RH6/RH12/RH15/RH16
For 增加VCC5寬度

For EMI

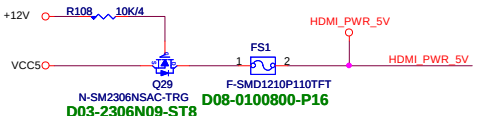
AUX Level Shifter



HPD Circuit

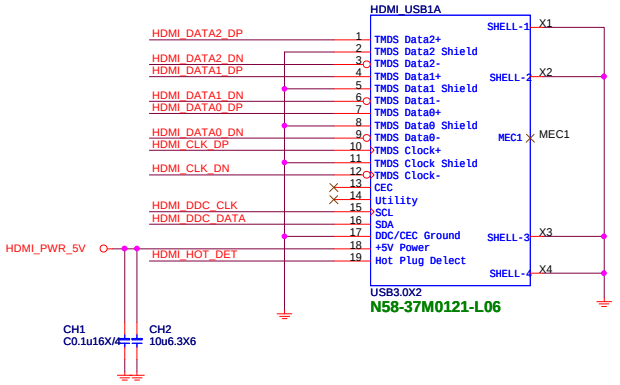


Connector Power

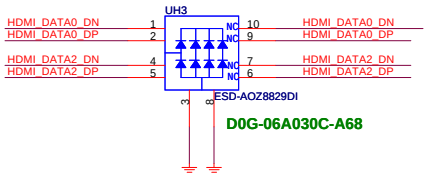


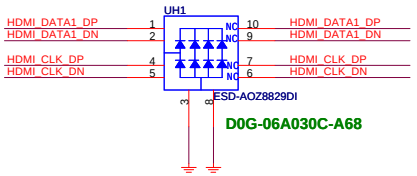
如果用DIODE_SA測試電壓會不過

Connector

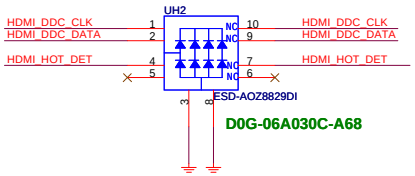


For EMI





注意:耐壓5V零件



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VCORE: ICCMax 140A
LL: 1.3mohm
OCP: 192A

SOC: ICCMax 75A
LL: 2.1ohm
OCP: 90A

燒錄打點:IC正面左上橘+金色點

Phase 1 close to CPU power pin.

RT close to Choke

RT close to Choke

0x26:RH=18K,RL=13K

Default		VR53	VR54	VC20	VR58	VR57	VR59	VR60
	Temp	6.49k	10k	100p	X	0R	X	0R
	VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X

Note:VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

SMB Address: 0X70

teknisi indonesia

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MS-7C37	
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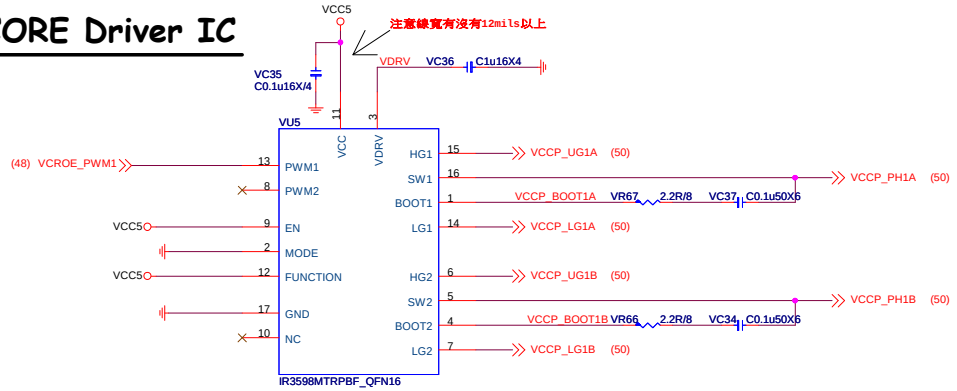
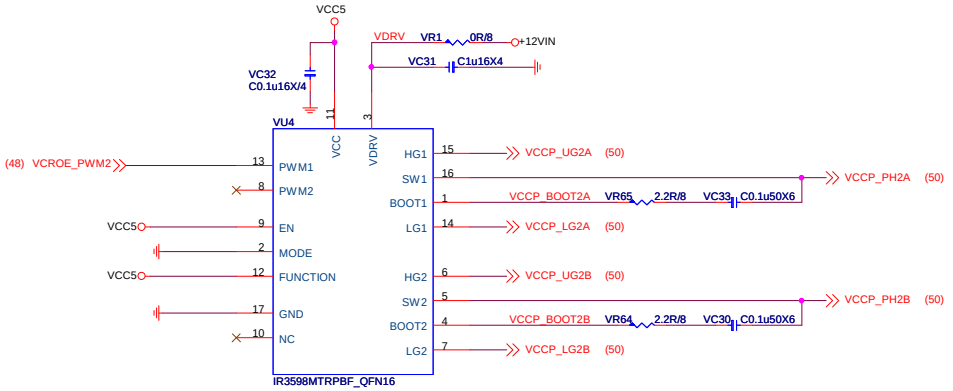
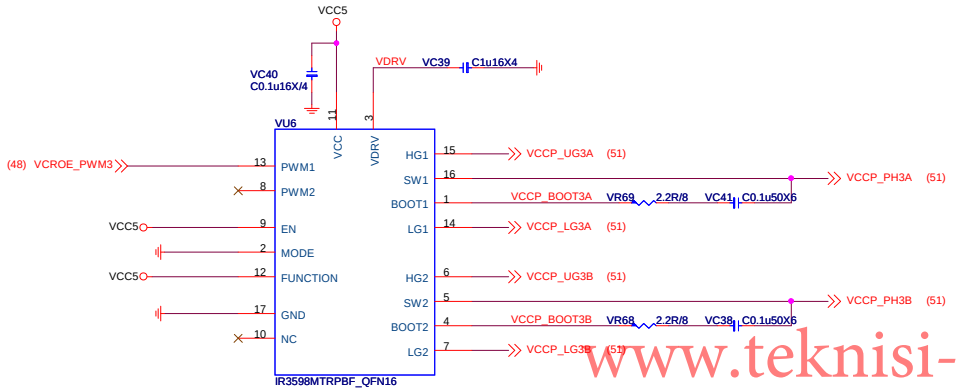
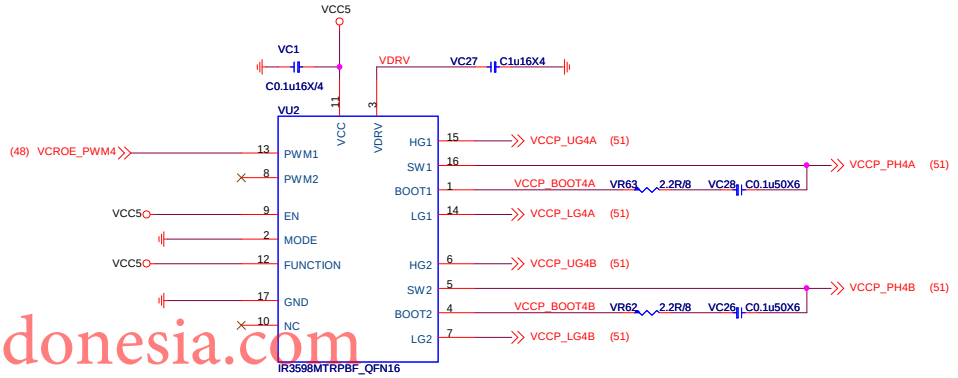
CPU_CORE Driver IC









CPU_SOC Driver IC

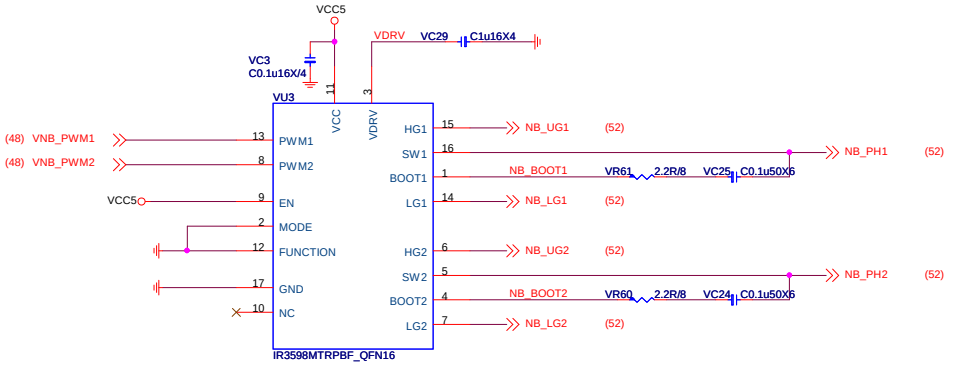


Table for IR3598				
Function	Mode	PWM Mode	Phase Mode	
0	1	IR ATL	Dual	
1	1	IR ATL	Doubler	
0	0	Tri-State	Dual	SOC
1	0	Tri-State	Doubler	Vcore

MICRO-STAR INT'L CO.,LTD

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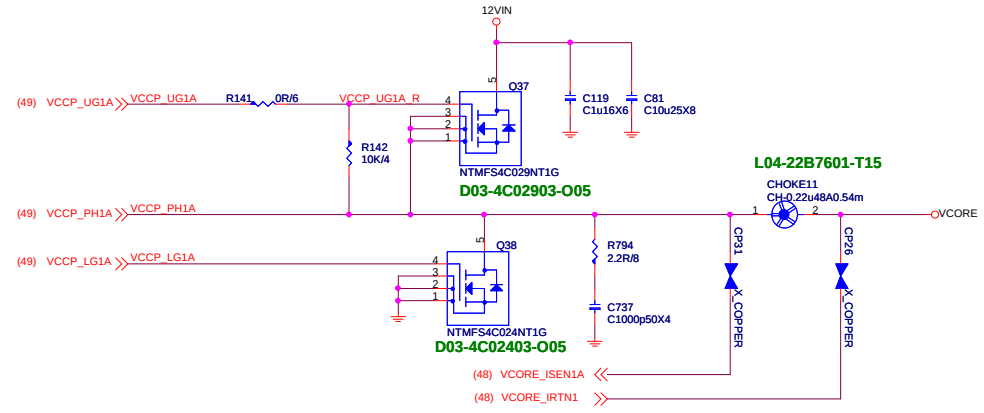
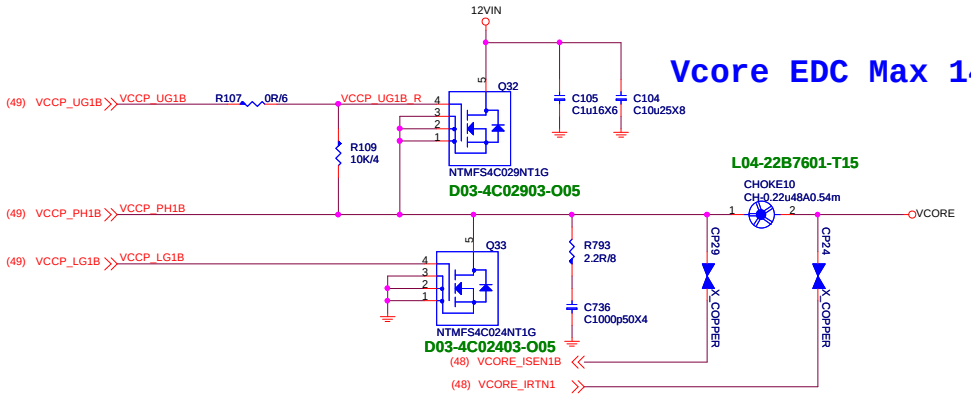
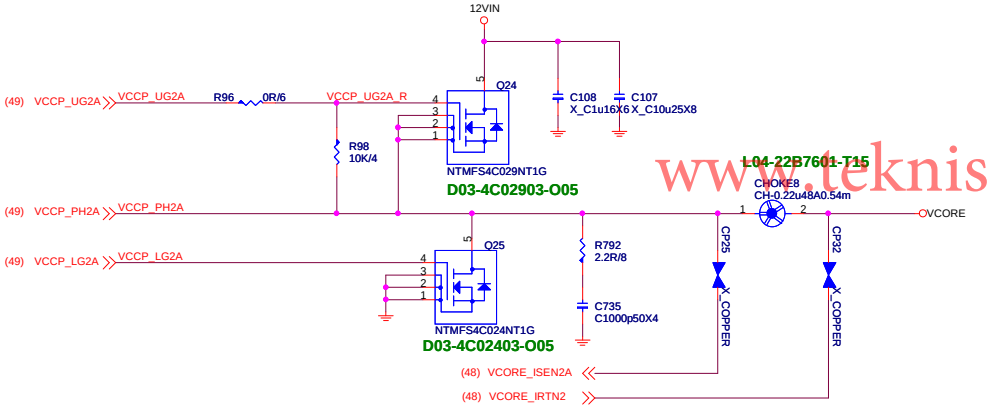
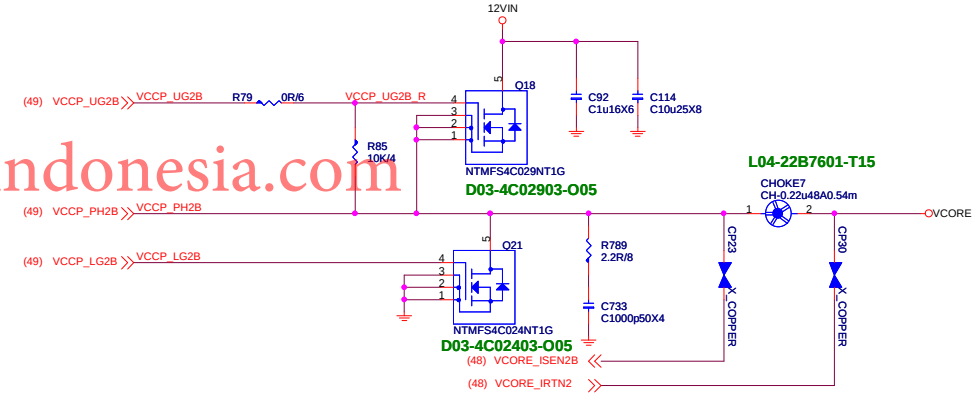
Vcore EDC Max 140A









MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C37	
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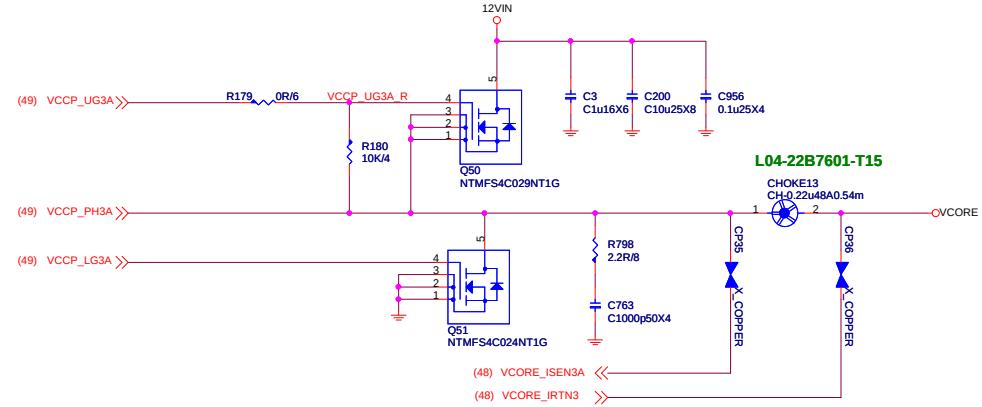

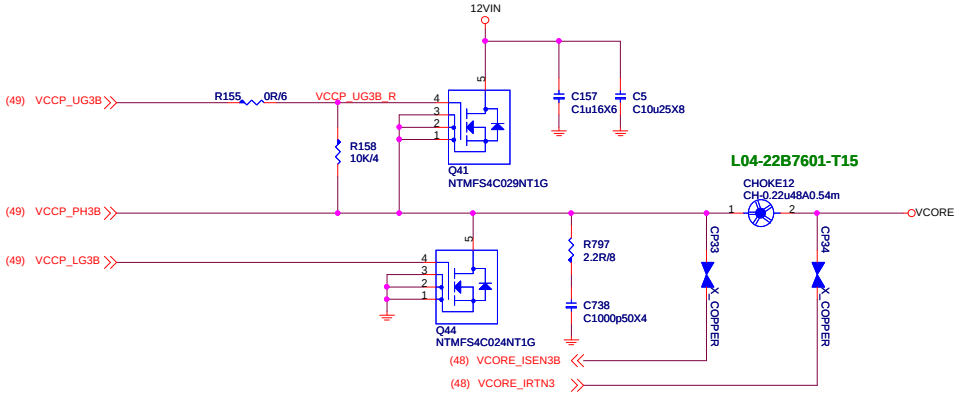

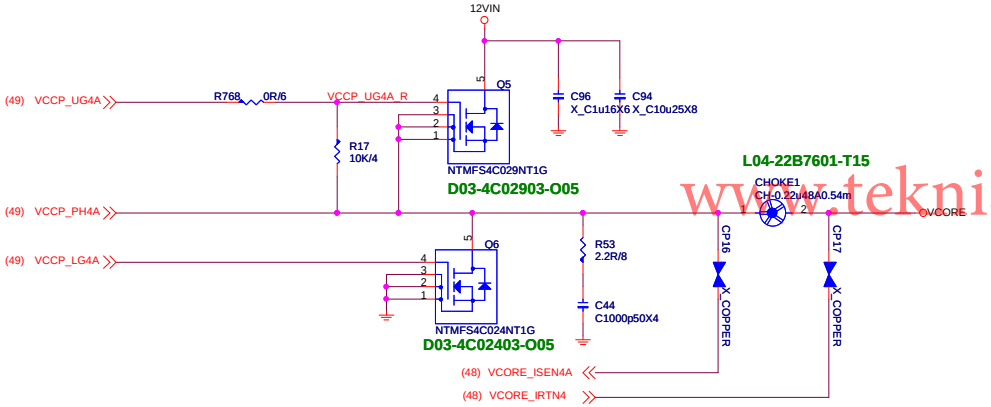

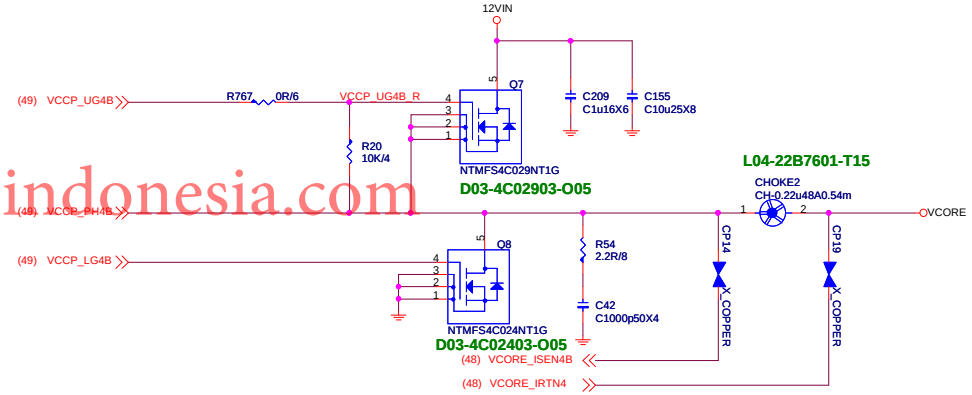

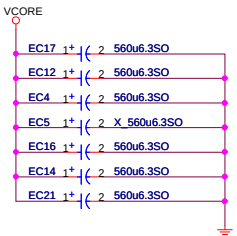

MICRO-STAR INT'L CO.,LTD

MS-7C37

Size	Document Description	Rev
Custom	CPU Power Vocre Phase 7 - 10	1.2

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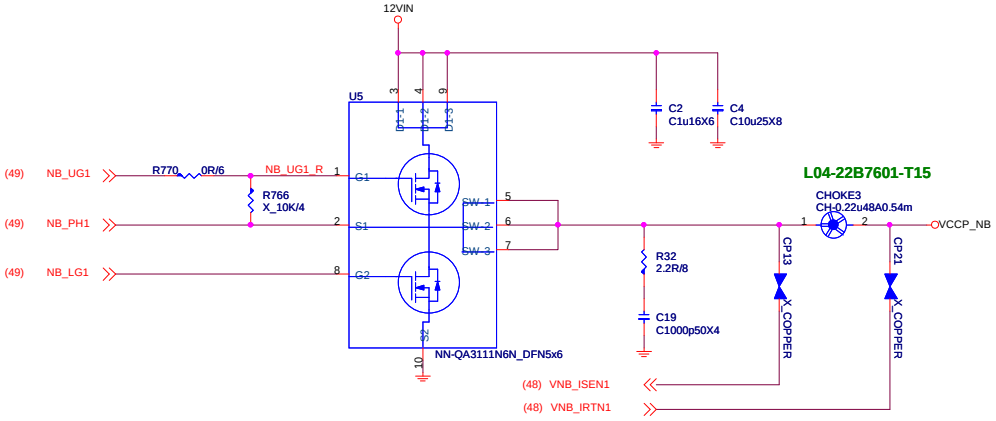
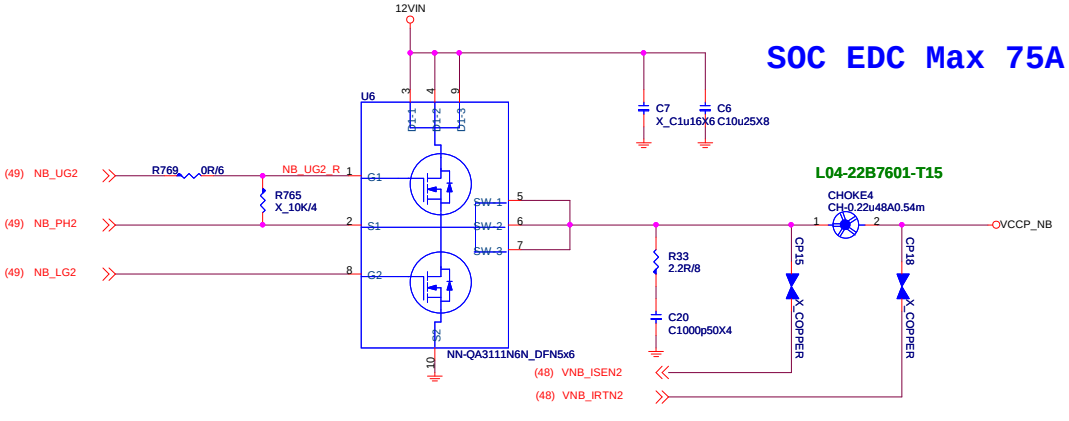
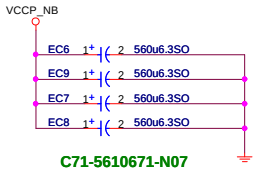




SOC EDC Max 75A



C71-5610671-N07

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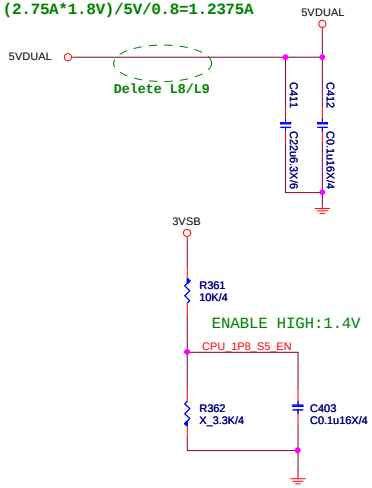
CPU_1P8V_S5

CPU: VDD_18_S5@0.5A
CPU: VDDIO_Audio@0.25A
CHIP: VDD_18_S5@0.1A

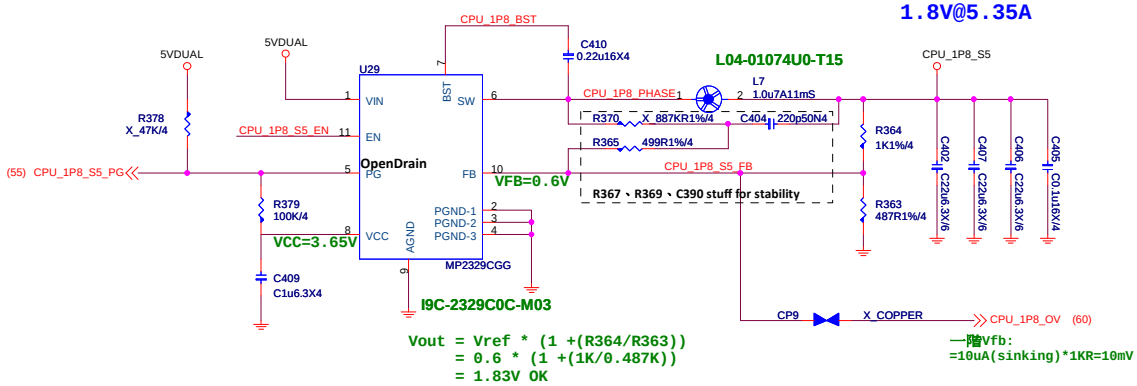
CPU_1P8: 2.5A
CPU_VDDP_S5: 1A
CHIP_SOC_S5: 1A

Input Current=
(2.75A*1.8V)/5V/0.8=1.2375A



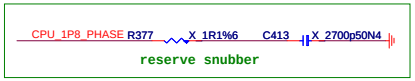
CPU_1P8_BST、CPU_1P8_BST_R >50 mils.

1.8V@5.35A



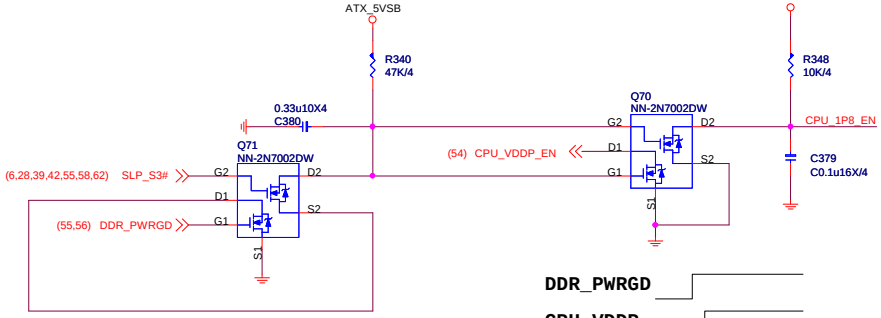
Vout = Vref * (1 +(R364/R363))
= 0.6 * (1 +(1K/0.487K))
= 1.83V OK

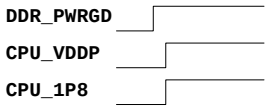
陪Vfb:
=10uA(sinking)*1KR=10mV



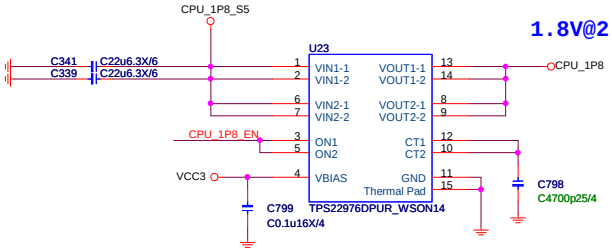
CPU_1P8V

CPU: VDD_18@2A
CHIP: VDD_18@0.5A

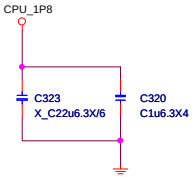




1.8V@2.5A



Adjustable Rise Time
SR = 0.42*CT+66
SR is the slew rate in (μs/V)
CT is constant value on CT pin (in pF)
The units for the constant 66 is in (μs/V)



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Size: Custom	Document Description: CPU Power 1.8_S0 / S5	Rev: 1.2
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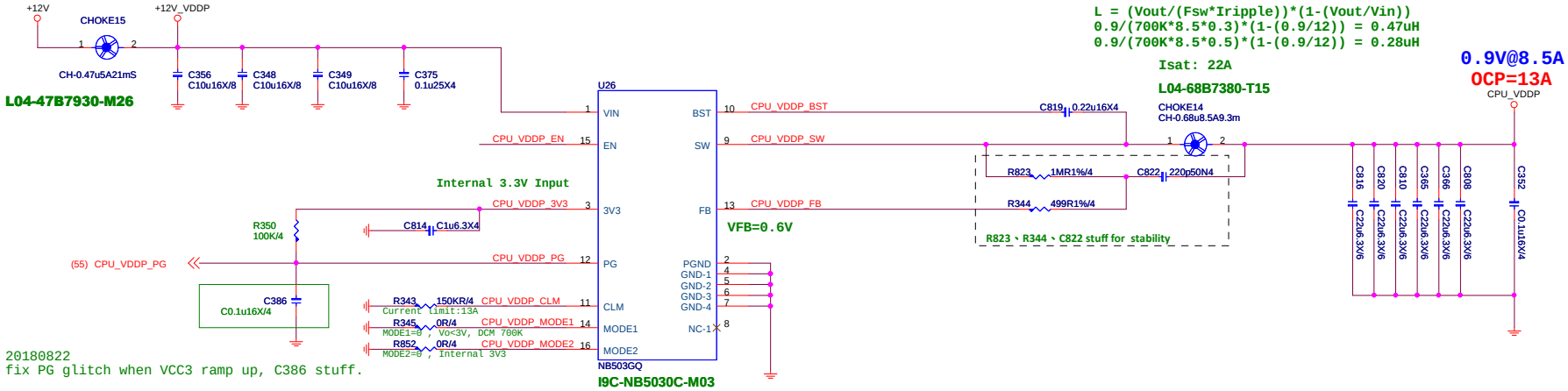
CPU_VDDP

CPU: VDDP@8.5A

```
Input Current = (8.5A*0.9V)/12V/0.8 = 0.8A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A
```

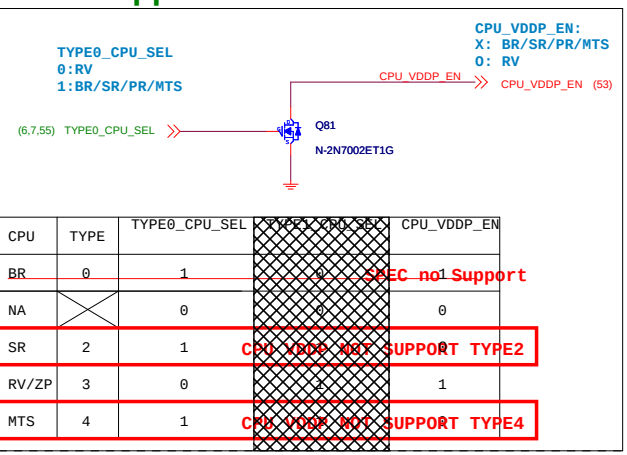



```
L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
0.9/(700K*8.5*0.3)*(1-(0.9/12)) = 0.47uH
0.9/(700K*8.5*0.5)*(1-(0.9/12)) = 0.28uH
Isat: 22A
L04-68B7380-T15
```

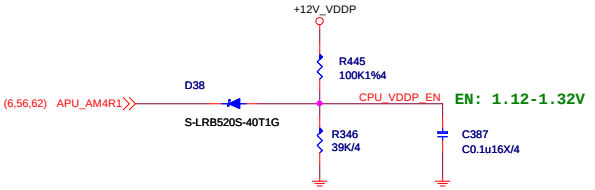
0.9V@8.5A
OCP=13A

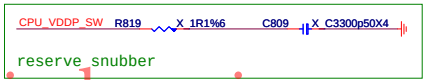
```
20180822
fix PG glitch when VCC3 ramp up, C386 stuff.
```

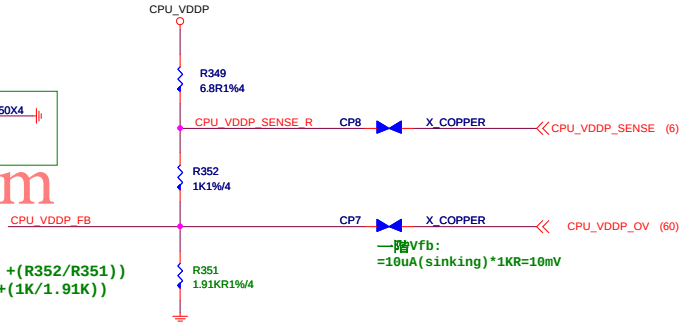
No support BR SPEC



CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN
BR	0	1	0	SPEC no Support
NA	X	0	0	0
SR	2	1	0	CPU_VDDP NOT SUPPORT TYPE2
RV/ZP	3	0	1	1
MTS	4	1	1	CPU_VDDP NOT SUPPORT TYPE4





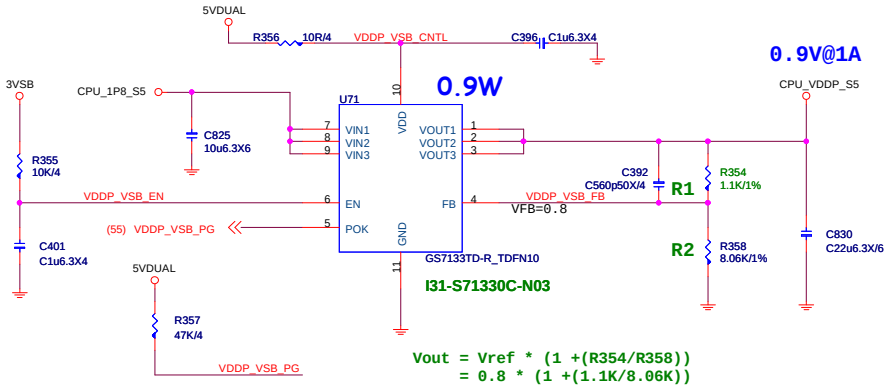



```
Vout = Vref * (1 +(R352/R351))
     = 0.6 * (1 +(1K/1.91K))
     = 0.914V OK
```

一階Vfb:
=10uA(sinking)*1KR=10mV

CPU_VDDP_S5

CPU: VDDP_S5@1A




```
Vout = Vref * (1 +(R354/R358))
     = 0.8 * (1 +(1.1K/8.06K))
     = 0.909V OK
```

MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size: Custom	Document Description: CPU Power VDDP - NB503	Rev: 1.2
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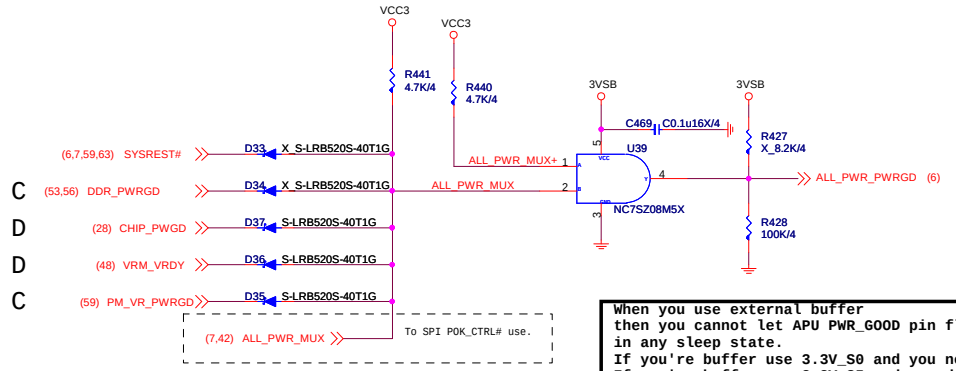
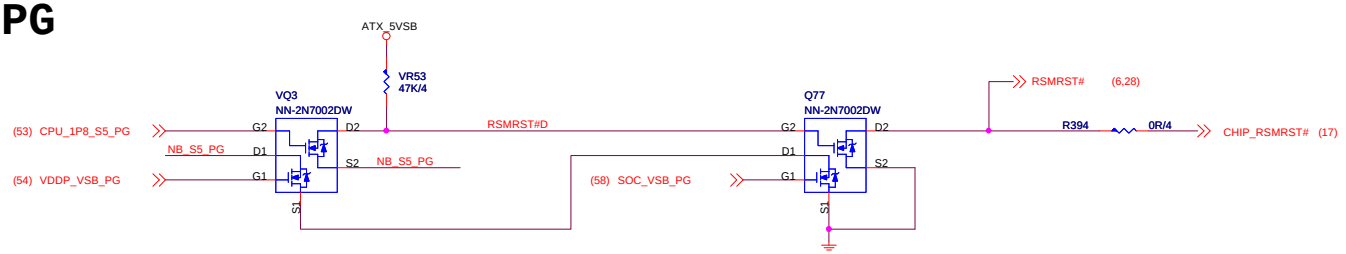
ALL POWER GOOD MUX

S0 PG

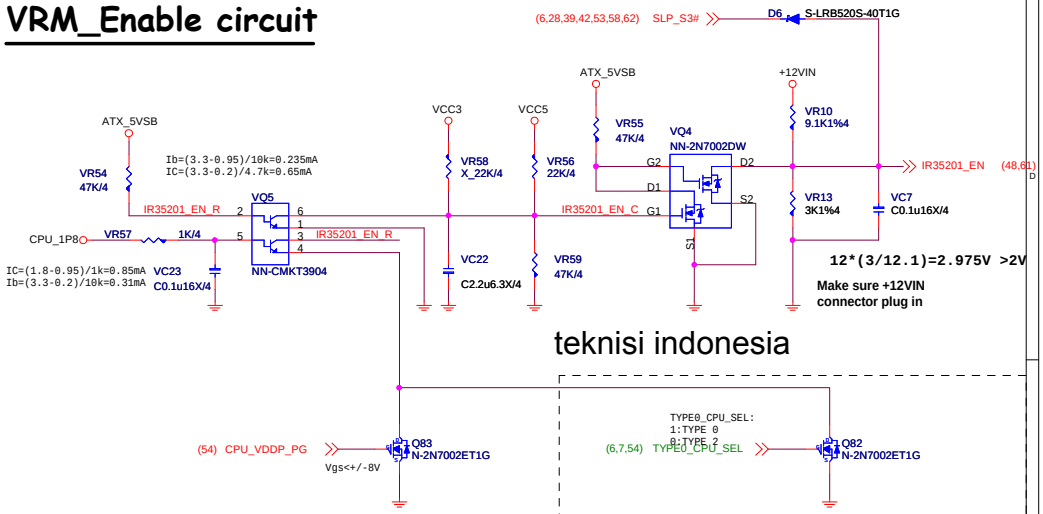



```
When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.
```

S5 PG



VRM_Enable circuit



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CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
~~BR~~	~~0~~	~~0~~	~~1~~ SPEC no Support
NA		0	0
SR	2	1 CPU VDDP NOT SUPPORT TYPE2	
RV/ZP	3	1	0
MTS	4	1 CPU VDDP NOT SUPPORT TYPE4	

MICRO-STAR INT'L CO.,LTD	
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VCC_DDR

15.5A For CPU
9.5A For 4DIMM
1.2A For DDR VTT
OCP = 39.3A; Choke Isat=42A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
R649 = 1.5 * 26.2 * 2mohm / 10uA
R649 = 7.86K

Rdson(Low Side) 5V
D03-4C02403-O05:3.3 ~ 4mohm
4mohm / 2pcs = 2mohm

$$R_{OCSET} = \frac{I_{VALLEY} \times R_{LGDS(ON)}}{I_{OCSET}}$$

OCP, MOSFET

Current Sensing
Iocset 9 10 11 µA

(6,54,62) APU_AM4R1 — D12 S-LRB520S-40T1G — DDR_EN

ATX_5VSB
R162 47K/4
Q45 NN-2N7002DW
G2 D2 D1 S2 G1 S1
(6,10,28,39,42,57,62) SLP_S5#
DDR_EN (57)

5VDIMM
R145 10R/8
DDR_VCC C132 C4.7u10X/6

5VDIMM
R152 47K/4
EN:VIH2.4V
EN pin Maimum:6.5V
(53,55) DDR_PWRGD
DDR_EN
DDR_REFOUT
DDR_REFIN

U14 RT8125EGQW
EN PGOOD REFOUT REFIN VCC GND BOOT PHASE UGATE LGATE/OCSET FB
DDR_BOOT1 DDR_PH1 DDR_UG1 DDR_LG1 DDR_FB
C122 0.1u25X4

C952 0.22u10X4
C149 C1000p50X4
R154 665R1%0402
C148 C1000p50X4

FB:0.8V
I32-8125E0C-R11
Vout = Vref * (1 + (R151/R148))
= 0.8 * (1 + (10.2K/19.1K))
= 1.227V OK

R1
R2
VCC_DDR
close to DIMM side
R156 10R/4
R151 10.2K1%/4
DDR_VSENP CP3 X_COPPER
VDDIO_MEM_S3_SENSE (6)
C147 X_0.1u25X4
R148 19.1K1%/4

CP4 X_COPPER
DDR_OV (60)

Input Current=(26.2*1.2)/5/0.8=7.86A

L04-12A7811-T15
CHOKE6 CH-1.2u15A1.7m
5VDUAL_IN_DDR
5VDIMM
C95 C1u16X6
C97 10u6.3X6
EC10 560u6.3SO
EC11 560u6.3SO
C141 C0.1u16X/4
C71-5610671-N07
C71-5610671-N07

DDR_UG1 R97 0R/6 DDR_UG1_R
Q22 NTMFS4C029NT1G D03-4C02903-O05
Q23 NTMFS4C029NT1G D03-4C02903-O05
R99 X_10K/4

L04-47B7981-T15
CHOKE9
CH-0.47u42A0.81m
1.2V@26.2A
OCP=39.3A

DDR_PH1
VCC_DDR

DDR_LG1
Q28 NTMFS4C024NT1G D03-4C02403-O05
Q27 NTMFS4C024NT1G D03-4C02403-O05
R105 7.87K1%/4
R112 2.2R/8
C106 C3300p50X4
snubber

C153 C1u6.3X4
C126 C22u6.3X/6
EC22 560u6.3SO
EC26 560u6.3SO
EC27 560u6.3SO
C71-5610671-N07
C71-5610671-N07
C71-5610671-N07

VCC_DDR
EC20 560u6.3SO
EC18 560u6.3SO
C71-5610671-N07
C71-5610671-N07

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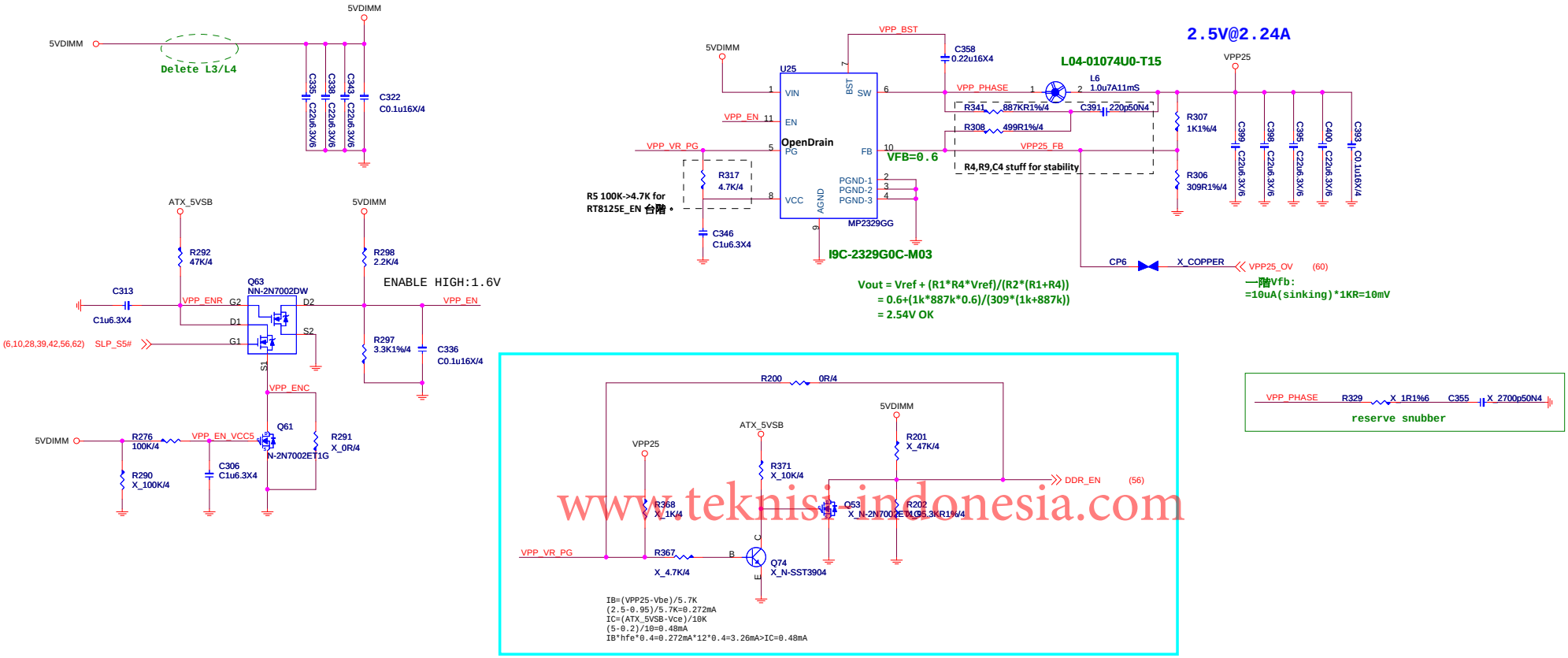
VPP25

2.5V@2.24A

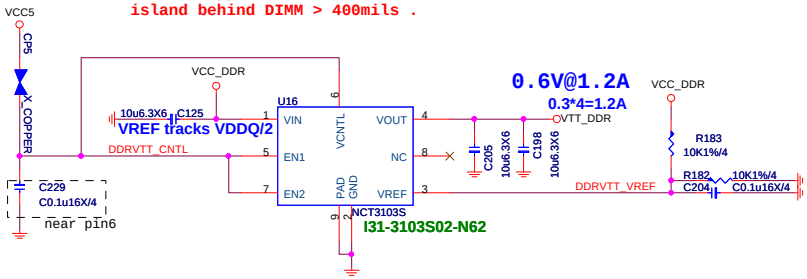
VPP_BST、VPP_BST_R >50 mils.

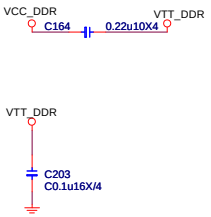


VTT_DDR

0.6V@1.2A

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .





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MS-7C37		
Size: Custom	Document Description: DDR VPP25 / VTT	Rev: 1.2
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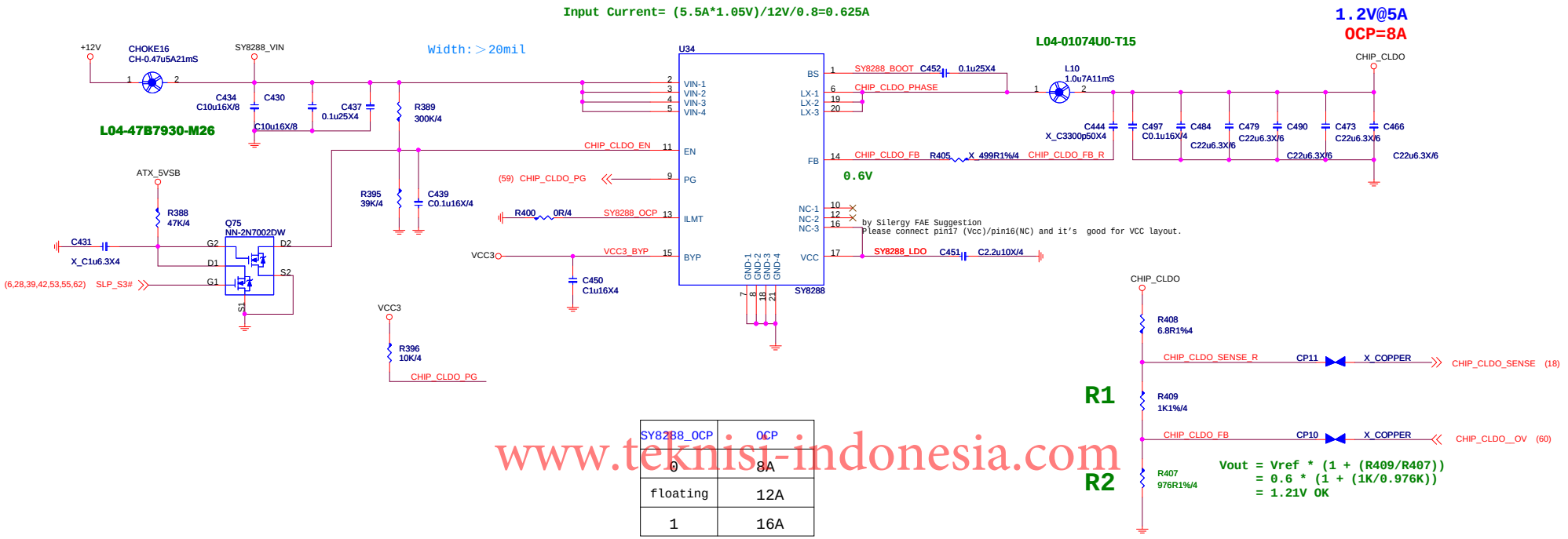
CHIP_CLDO

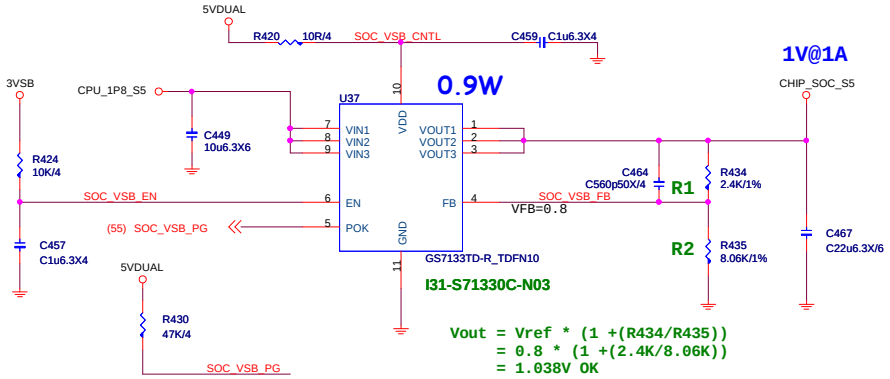
CHIP: VDD_CLDO@5A



SY8288_OCP	OCP
0	8A
floating	12A
1	16A

CHIP_SOC_S5

CHIP: VDDCR_SOC_S5@1A



MICRO-STAR INT'L CO.,LTD	
MS-7C37	
Size: Custom	Document Description: PROM - SY8288RAC / 1.05V
Rev: 1.2	
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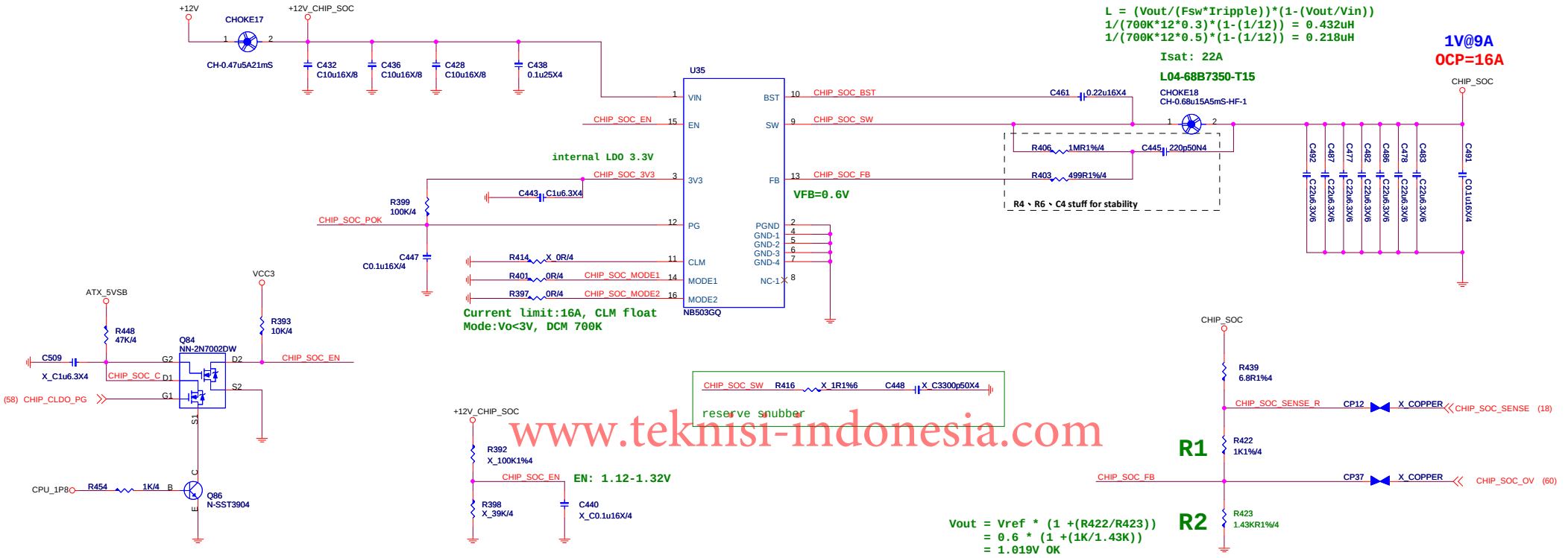
CHIP_SOC

CHIP: VDDCR_SOC@9A

Input Current = (12A*1V)/12V/0.8 = 1.25A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=12*SQRT((1/12)*(1-(1/12))) = 3.316A
Choke Irms =5 A



L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
1/(700K*12*0.3)*(1-(1/12)) = 0.432uH
1/(700K*12*0.5)*(1-(1/12)) = 0.218uH

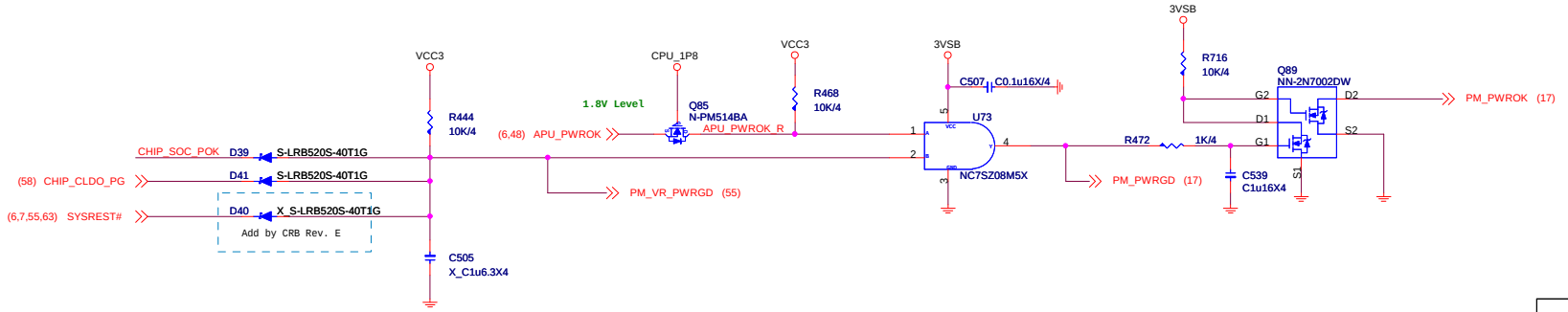
Isat: 22A

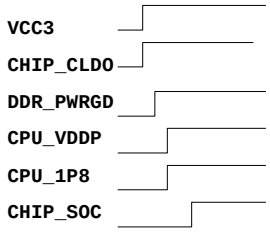
L04-68B7350-T15

1V@9A
OCP=16A

Vout = Vref * (1 +(R422/R423))
= 0.6 * (1 +(1K/1.43K))
= 1.019V OK

S0 PG





MICRO-STAR INT'L CO.,LTD	
MS-7C37	
Size: Custom	Document Description: PROM - NB503 / 1.0V
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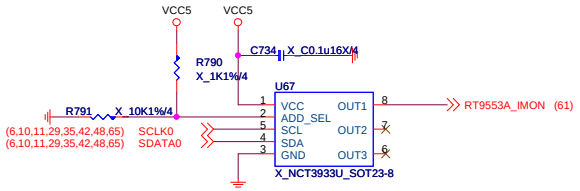
Over Voltage Control IC

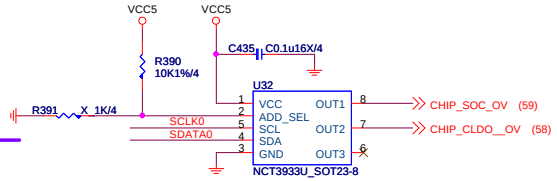
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

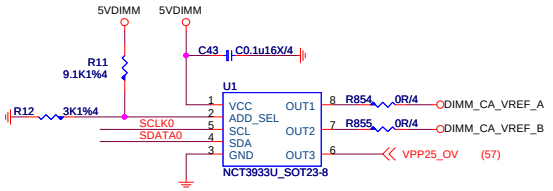
0x2A:RH=OPEN,RL=10K



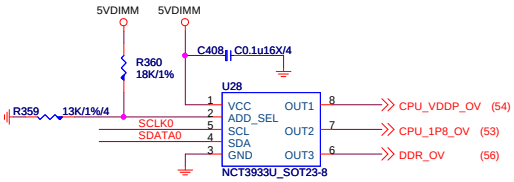
0x20:RH=10K,RL=OPEN



0x28:RH=9.1K,RL=3K



0x26:RH=18K,RL=13K



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size: Custom	Document Description: OV Control - NCT3933	Rev: 1.2
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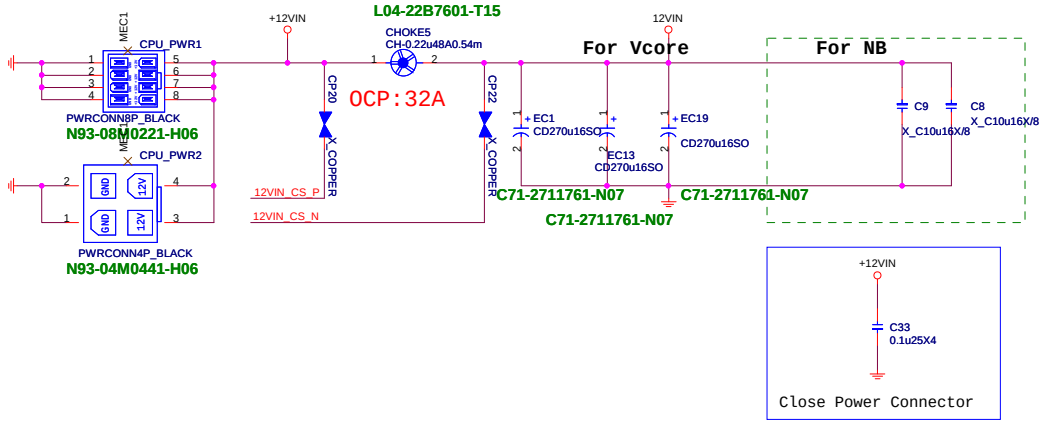
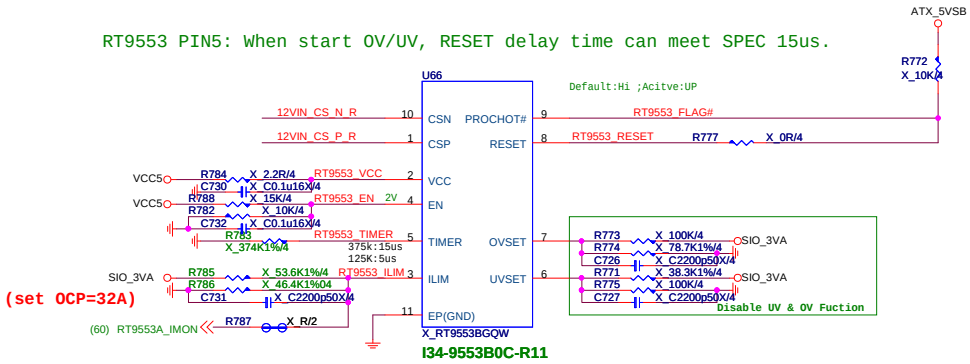
CPU POWER CONNECTOR

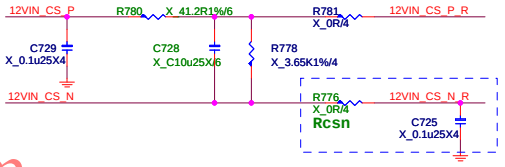


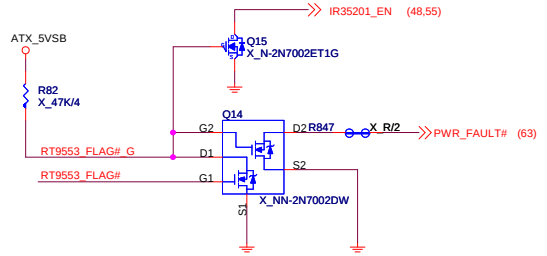
RT9553B CURRENT SENSE



Vcore			
D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	2	> output Vcore
D	=	0.166667	
I o = Icore(max)*0.8			
I core(max)	=	200	> Vcore current
I avg.	=	160	A
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	10	phase
I ripple	=	5.962848	A
How many pcs. Of Cap.			
I ripple(cap)	=	4700	m A
COE TEMP	=	1	
Input Cap.	=	2	pcs.

SOC			
D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.55	> output Vcore
D	=	0.129167	
I o = Icore(max)*0.8			
I core(max)	=	75	> Vcore current
I avg.	=	60	A
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	2	phase
I ripple	=	10.06153	A
How many pcs. Of Cap.			
I ripple(cap)	=	4700	m A
COE TEMP	=	1	
Input Cap.	=	3	pcs.





MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size: Custom	Document Description: OCP 12VIN - RT9533B	Rev: 1.2
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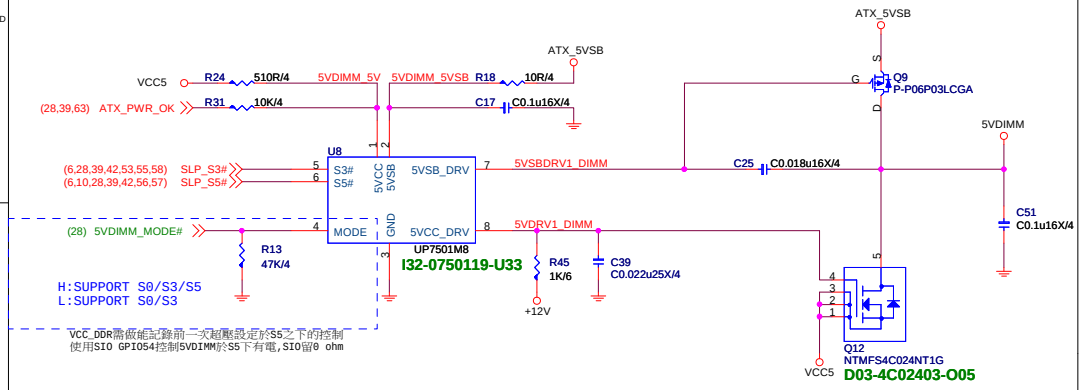
5VDIMM FOR DDR



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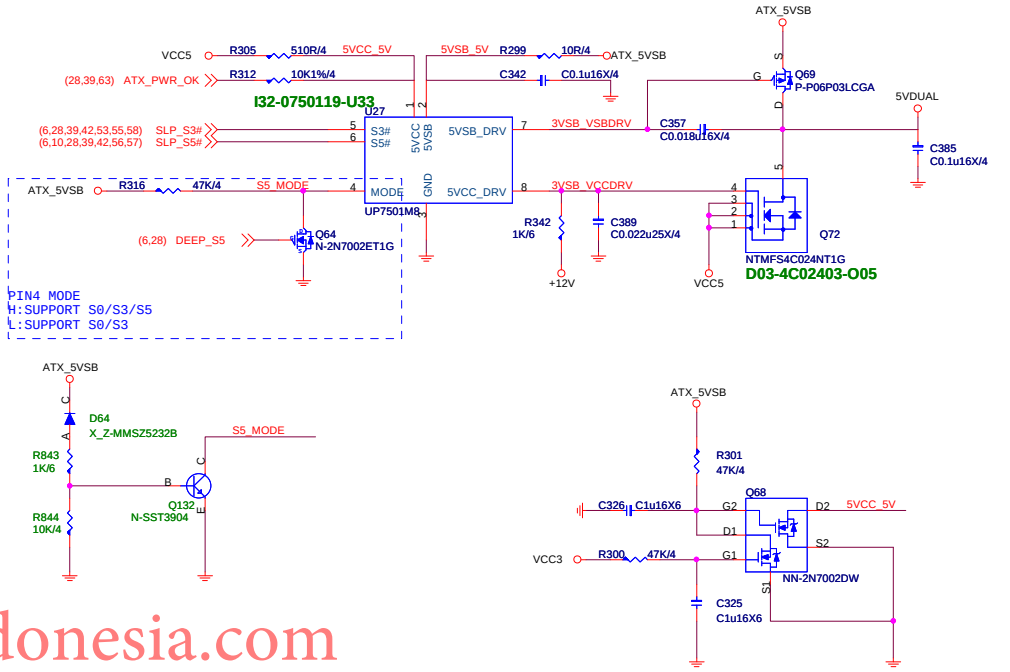
5VDUAL For 3VSB、CPU 1.8V 、VDDP

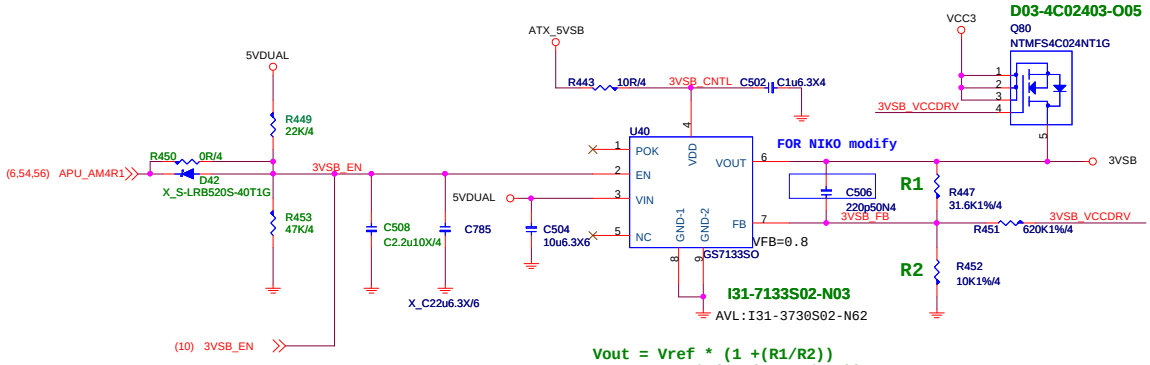


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

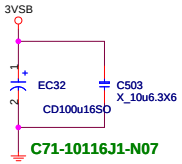
3VSB cost down

3.3V@3.363A

- CPU: VDD_33_S5@0.25A
- CHIP: VDD_33_S5@0.1A
- PCIE*4@1.5A
- M.2_WIFI@0.78A
- LAN@0.065A
- Redriver*2@0.668A
- USB TYPE-C@0.9mA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(31.6K/10K))
= 3.328V OK



MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size: Custom	Document Description: ACPI - 3VSB / 5VDIMM	Rev: 1.2
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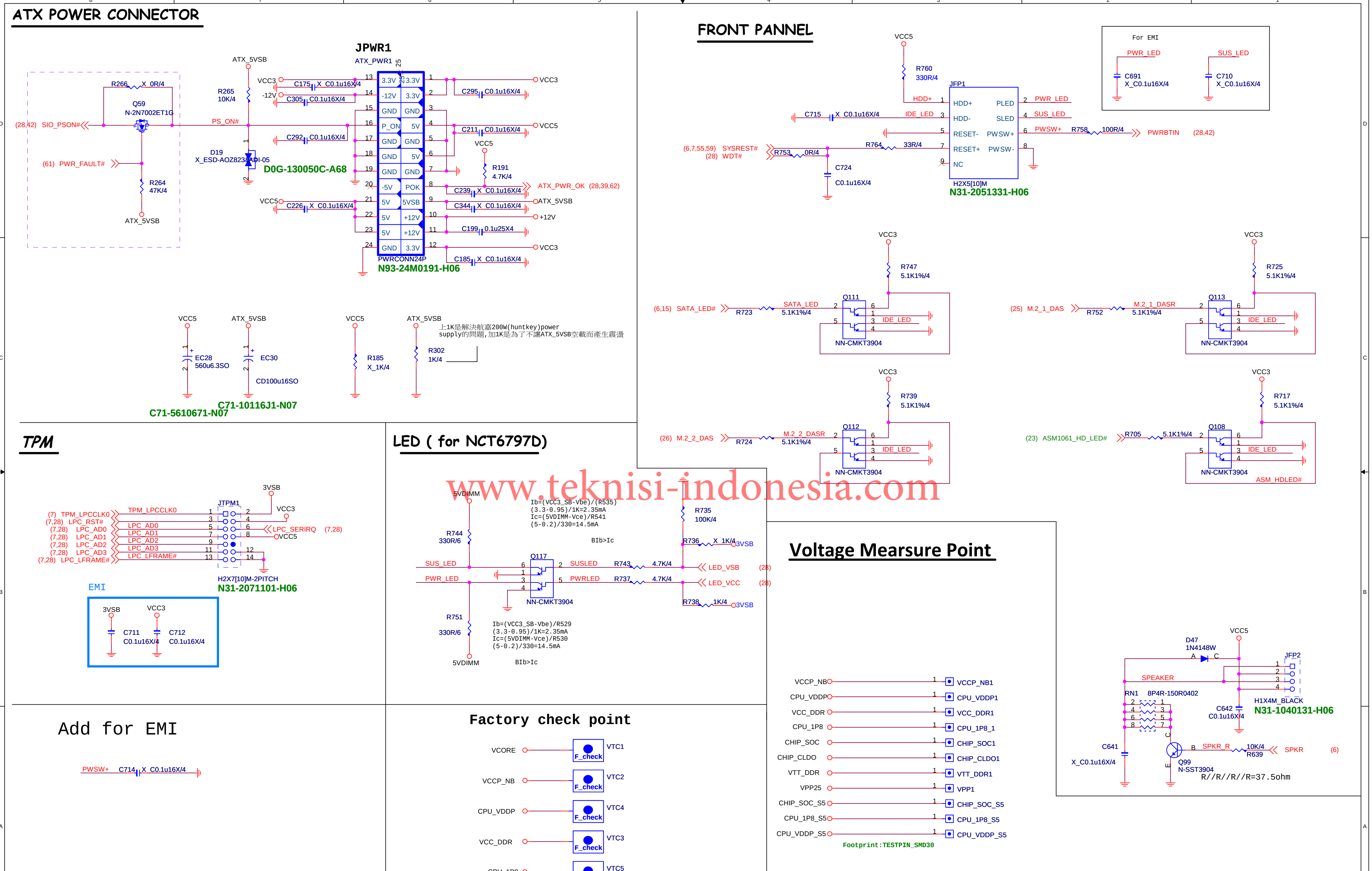

MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size: Custom	Document Description: ATX Power - FrontPanel / EMI	Rev: 1.2
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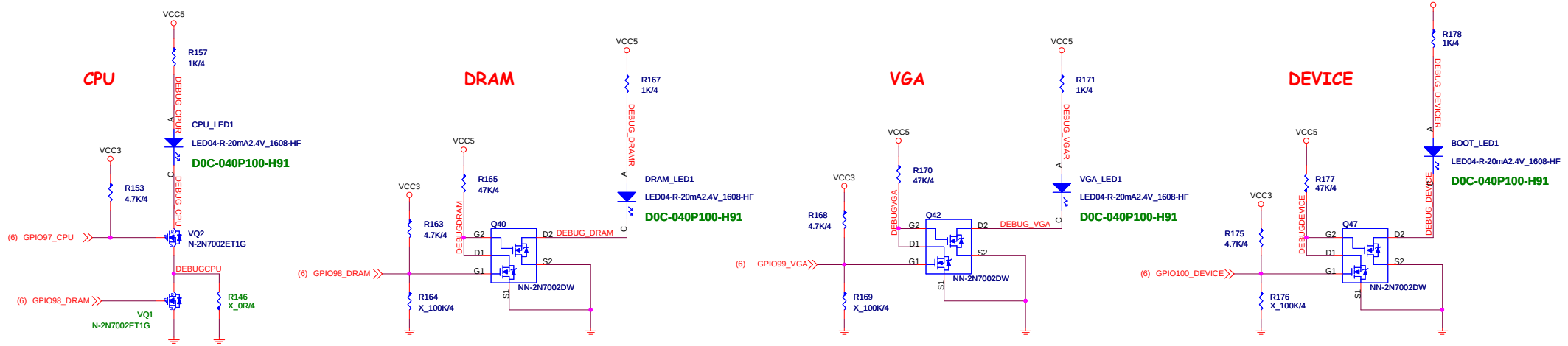
EZ Debug LED



LED\GPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

LED亮燈時同時將CPU LED關掉

AMD AMP Detect LED

MICRO-STAR INT'L CO.,LTD

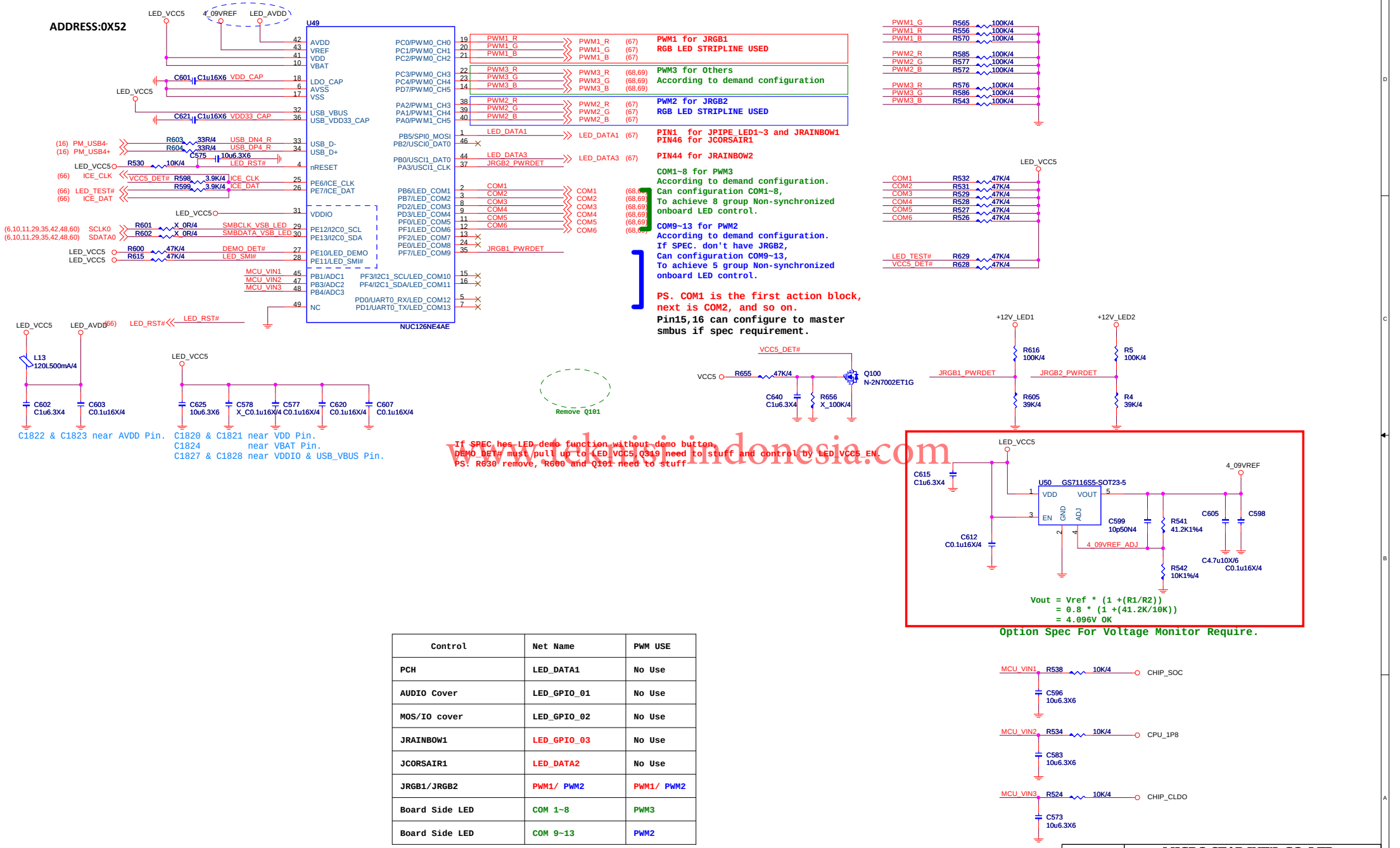
MS-7C37

Size: Custom | Document Description: LED - EZ DEBUG | Rev: 1.2

Date: Monday, April 01, 2019 | Sheet 64 of 75

48 PIN LED MCU

If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.



Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2

MICRO-STAR INT'L CO.,LTD

MS-7C37

Size: Custom | Document Description: MCU - LED Control | Rev: 1.2

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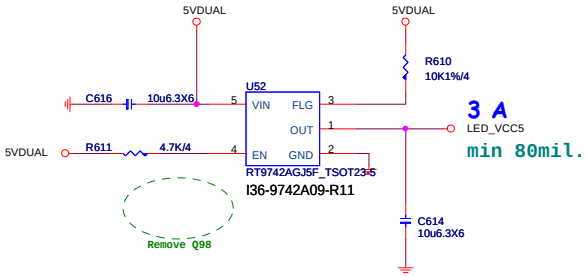
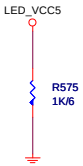
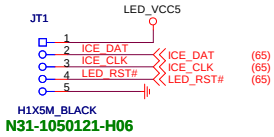
EXTERNAL POWER INPUT



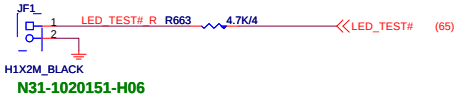


External Power

JT1 for FW update



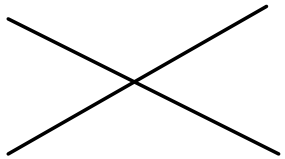
JF1 For Factory Test



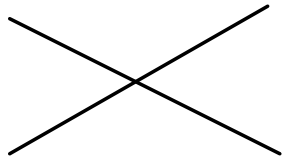
JPIPE:PIN1:output ,PIN2:input

PIN2:MCU IN
PIN1:HEATSINK OUT

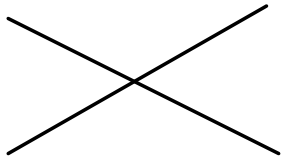
1 PCH HEATSINK LED



2 AUDIO/IO Cover LED



3 MOS HEATSINK LED



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MS-7C37		
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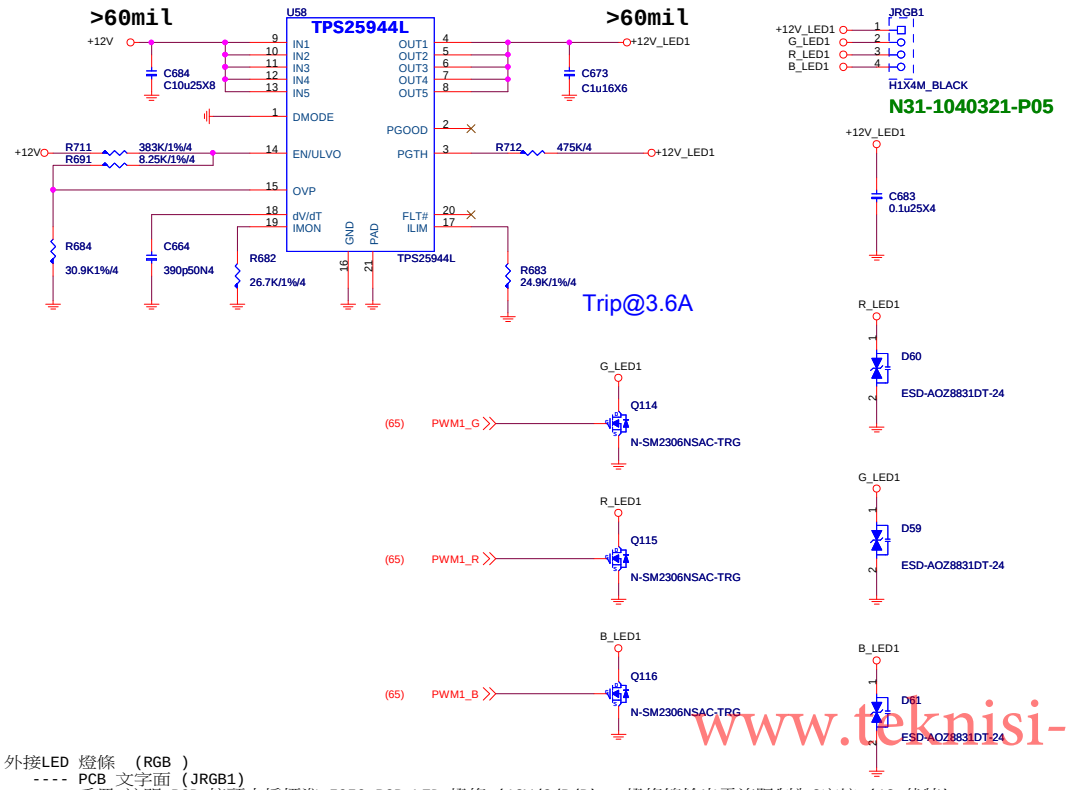
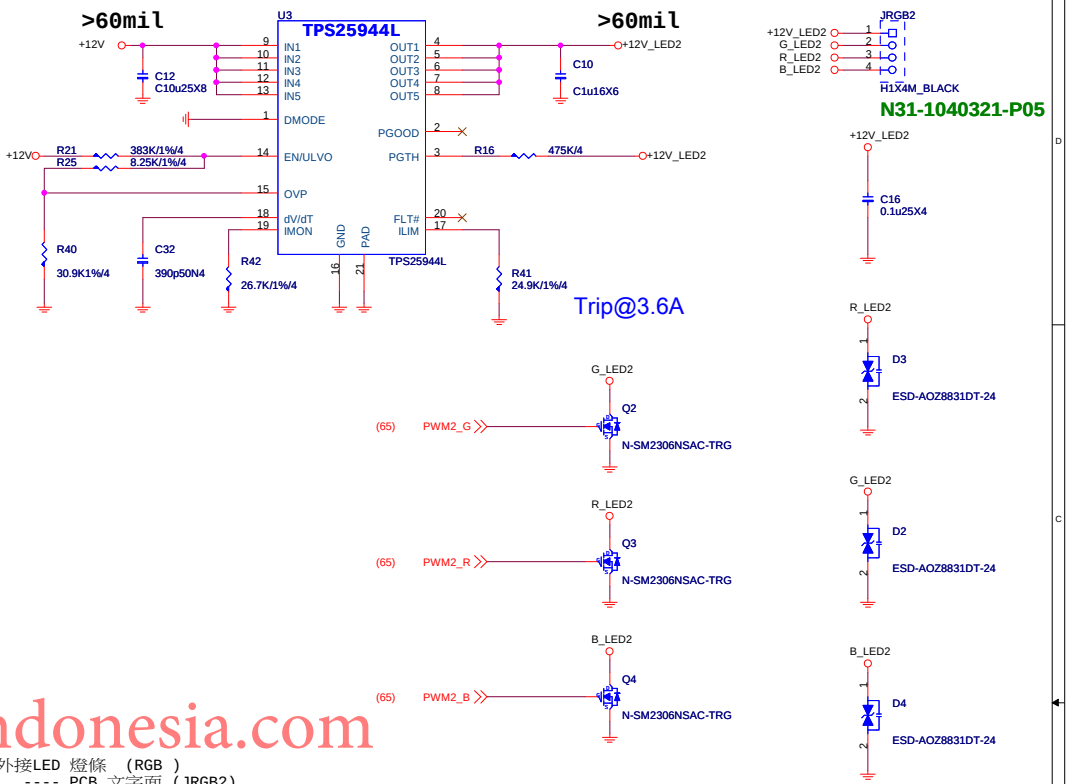
JRGB1



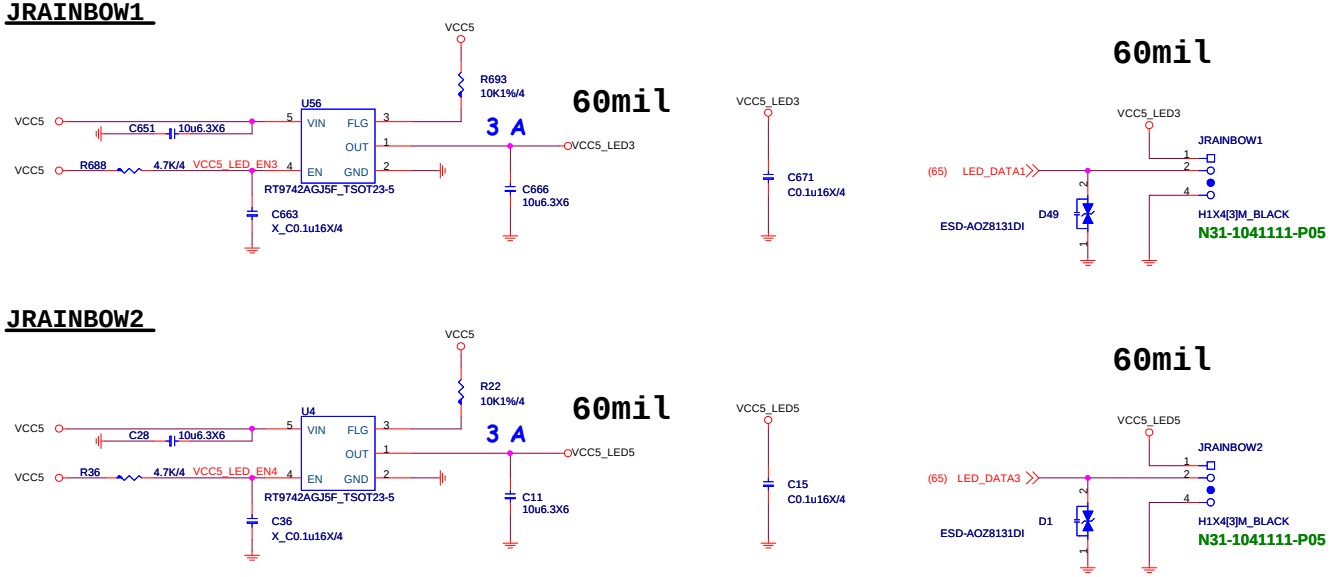
外接LED 燈條 (RGB)
---- PCB 文字面 (JRGB1)
---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

JRGB2



外接LED 燈條 (RGB)
---- PCB 文字面 (JRGB2)
---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

JRAINBOW1



JRAINBOW2

JCORSAIR1

Vinafix.com

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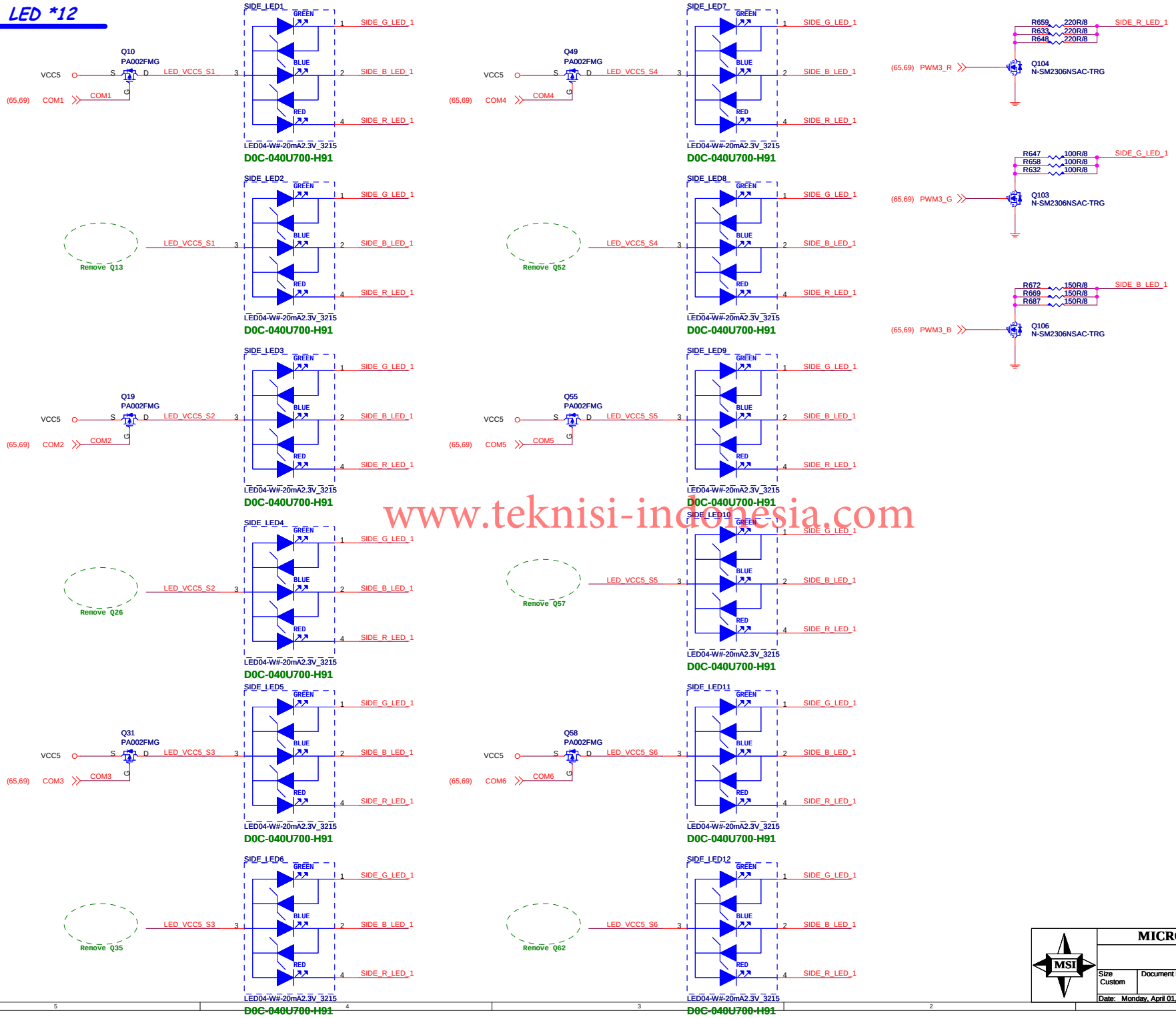
Sidebar LED *12



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MS-7C37		
Size: Custom	Document Description: LED - Sidebar LED	Rev: 1.2
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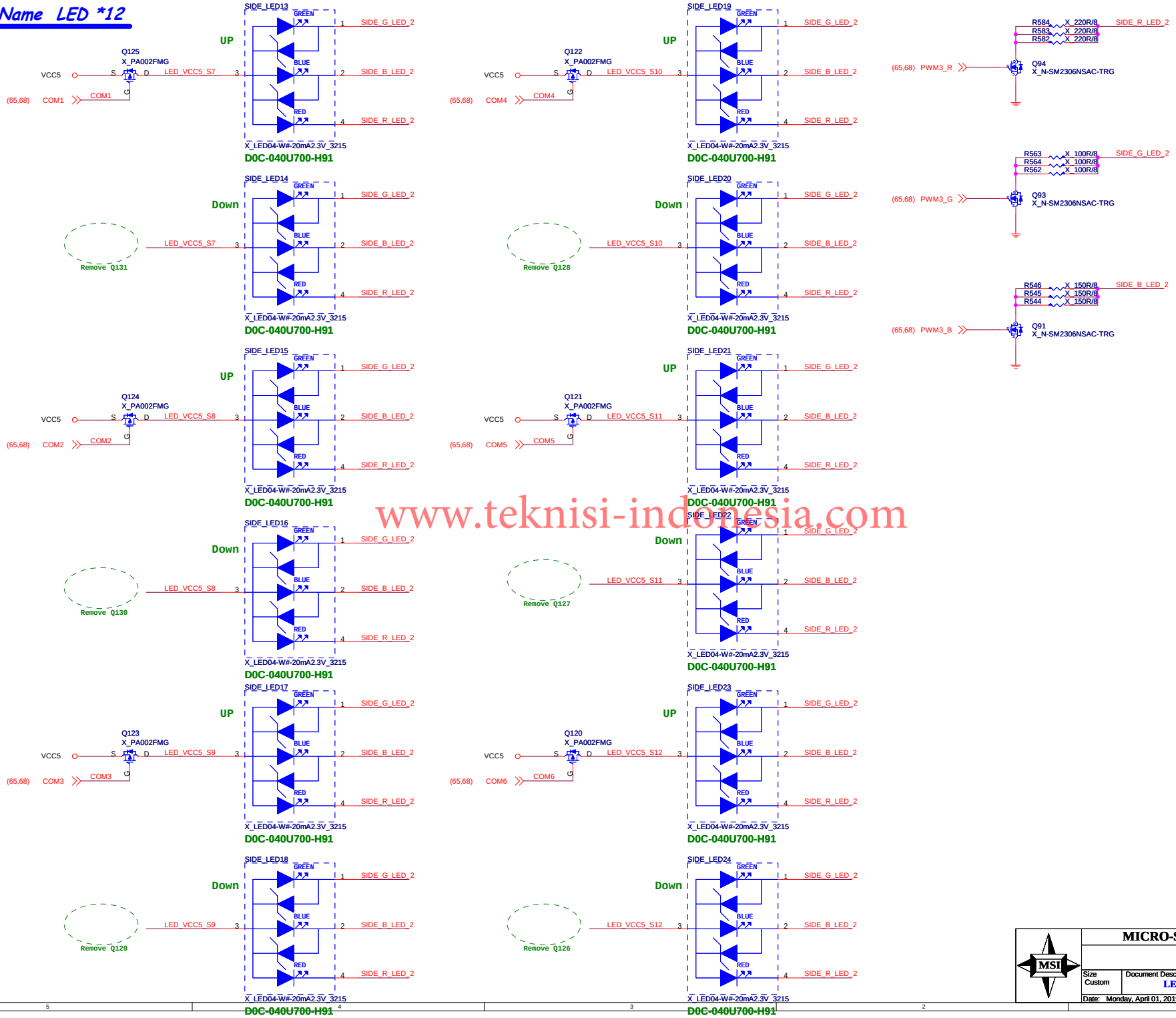
Market Name LED *12



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C37	
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CPU Socket

CPU2

E95-0000021-C22

E95-0000022-C22

Simulation

X_JS1 — SIM1 — X_PIN1*2

X_JS2 — SIM2 — X_PIN1*2

FM3, FM8, FM2, FM1, FM4, FM5, FM7, FM6 — X_FM120

Optics Orientation Holes

MH1, MH2, MH3, MH6, MH5, MH4, MH9, MH8, MH7 — X_MH001

C662 C0.1u16X/4

C674 C0.1u16X/4

MANUAL PART

UEFI1

G51-M1SPXXA-A09

G51-M1SPXXA-A09

HDMI_LA1

Label HDMI

HDMI LABEL

Y01-RHDMI03-000

NAHIMIC1 <MSI-BOM>

Y02-MU00100-NAH

Y02-MU00100-NAH

XSPLIT1 <MSI-BOM>

X_Y02-MA00401-XSP

Y02-MA00401-XSP

SSE1 <MSI-BOM>

X_Y02-MA00101-SSE

Y02-MA00101-SSE

BAT1_X1

BAT-BCR2032P

AVL:

D06-0100161-F52

D06-0100101-K26

PCB

PCB

PCB1

7C37-1.2

PD0-07C3712-E48

MOS HEATSINK

N-MOS1 — MOS_N — E31-0506240-K08

W-MOS1 — MOS_N — E31-0506250-K08

PCH HEATSINK

PCH1 — MOS_N — E32-0406700-K08

Audio COVER

COVER2 — Audio Cover — E21-7A62010-RH

E21-7A62010-A91

IO COVER

DDR COVER

MICRO-STAR INT'L CO.,LTD

MS-7C37

Size: Custom | Document Description: Manual Parts | Rev: 1.2

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