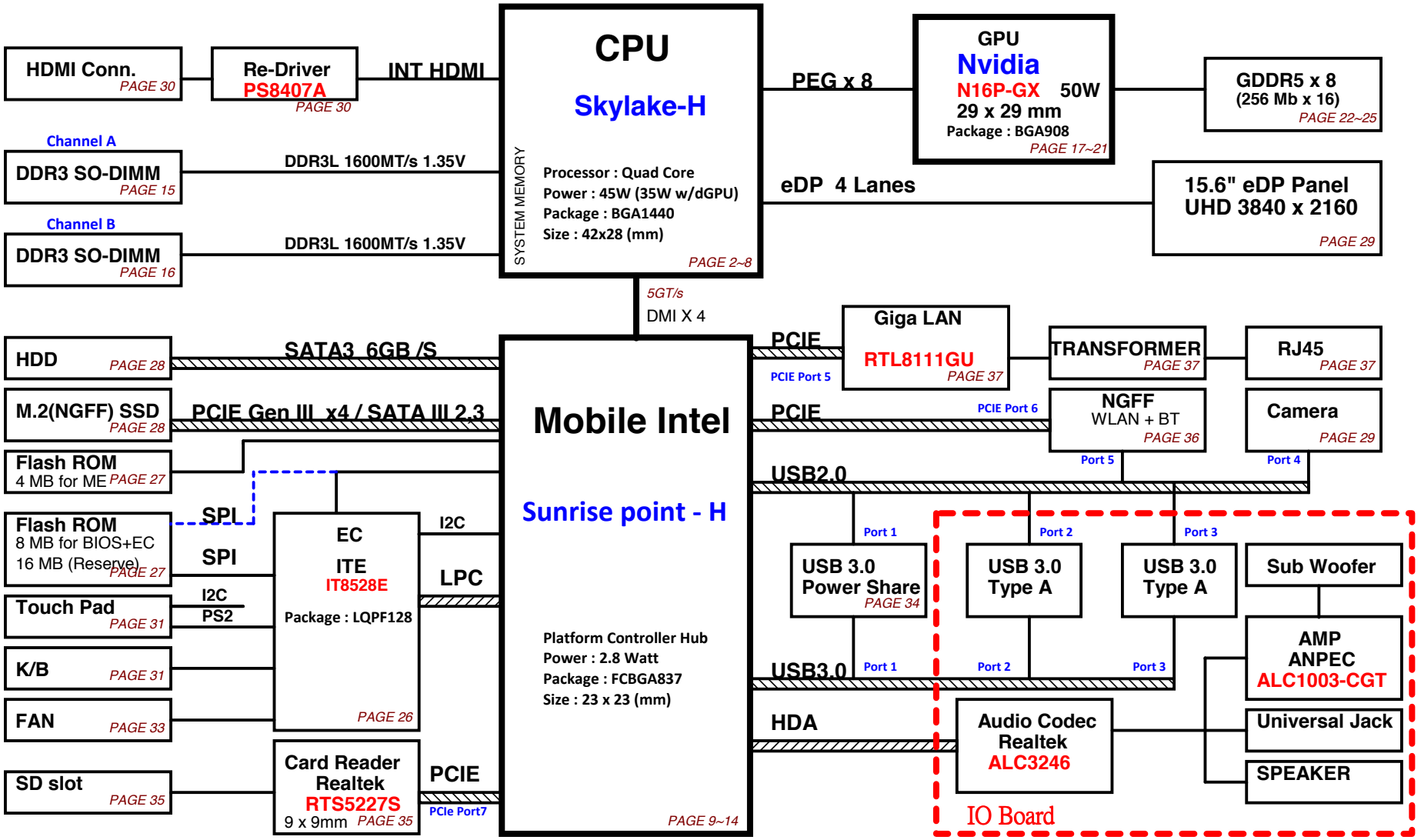
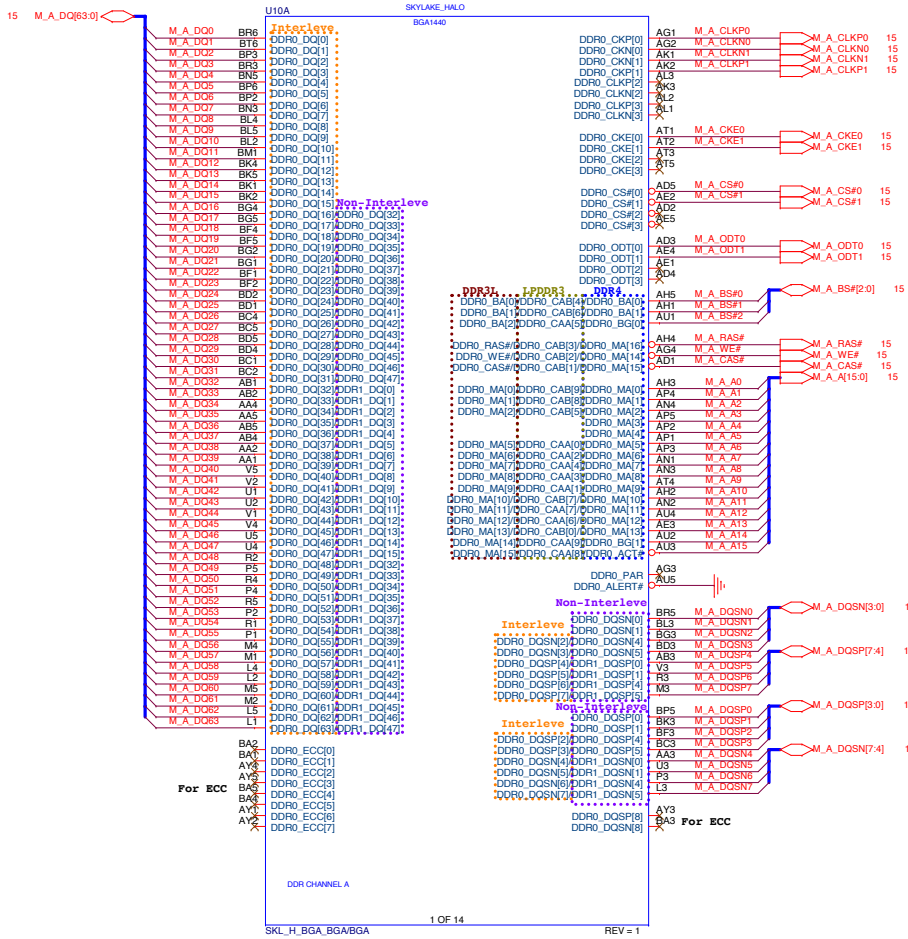
Block Diagram



Quanta Computer Inc.		
PROJECT : AM9A		
Size	Document Number: BLOCK DIAGRAM	Rev: A0
Date: Wednesday, August 19, 2015	Sheet 1 of 57	

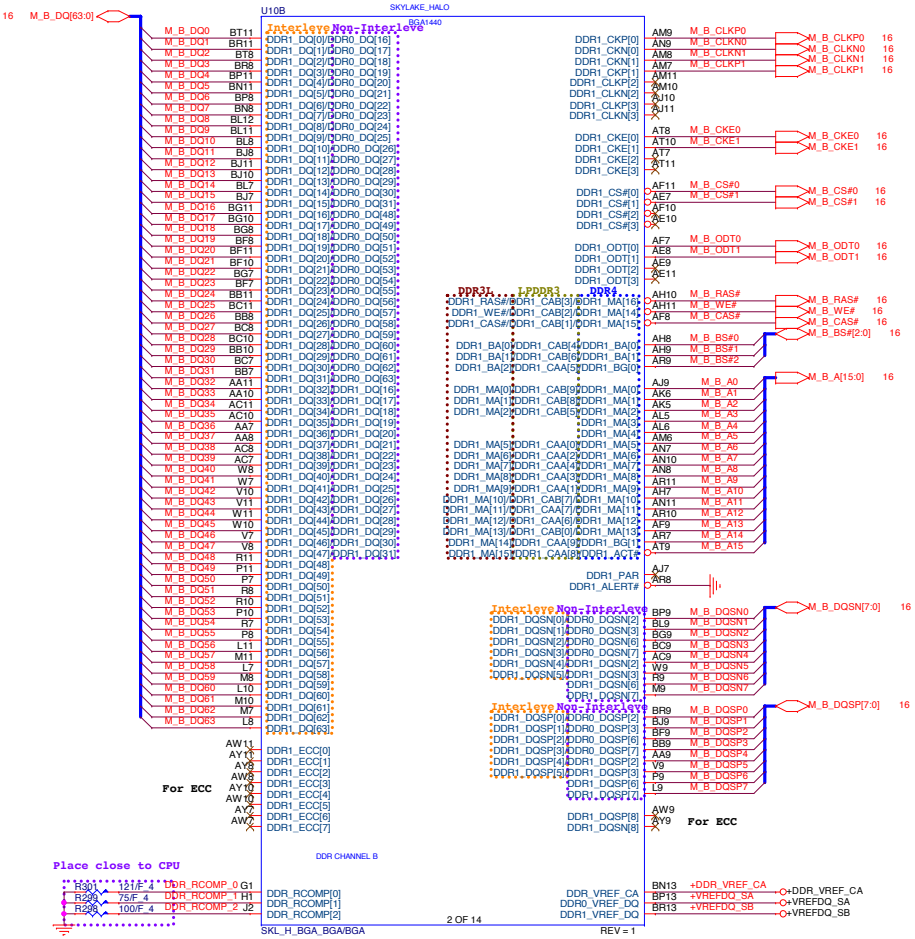
Skylake Processor (DDR3-CH-A)

SKL with DDR3L is IL memory design.



Skylake Processor (DDR3-CH-B)

SKL with DDR3L is IL memory design.



Follow SKL-H WP(V0.91) support DDR3L SO-DIMM #549401 page 26

Follow SKL-H WP(V0.91) support DDR3L SO-DIMM #549401 page 41

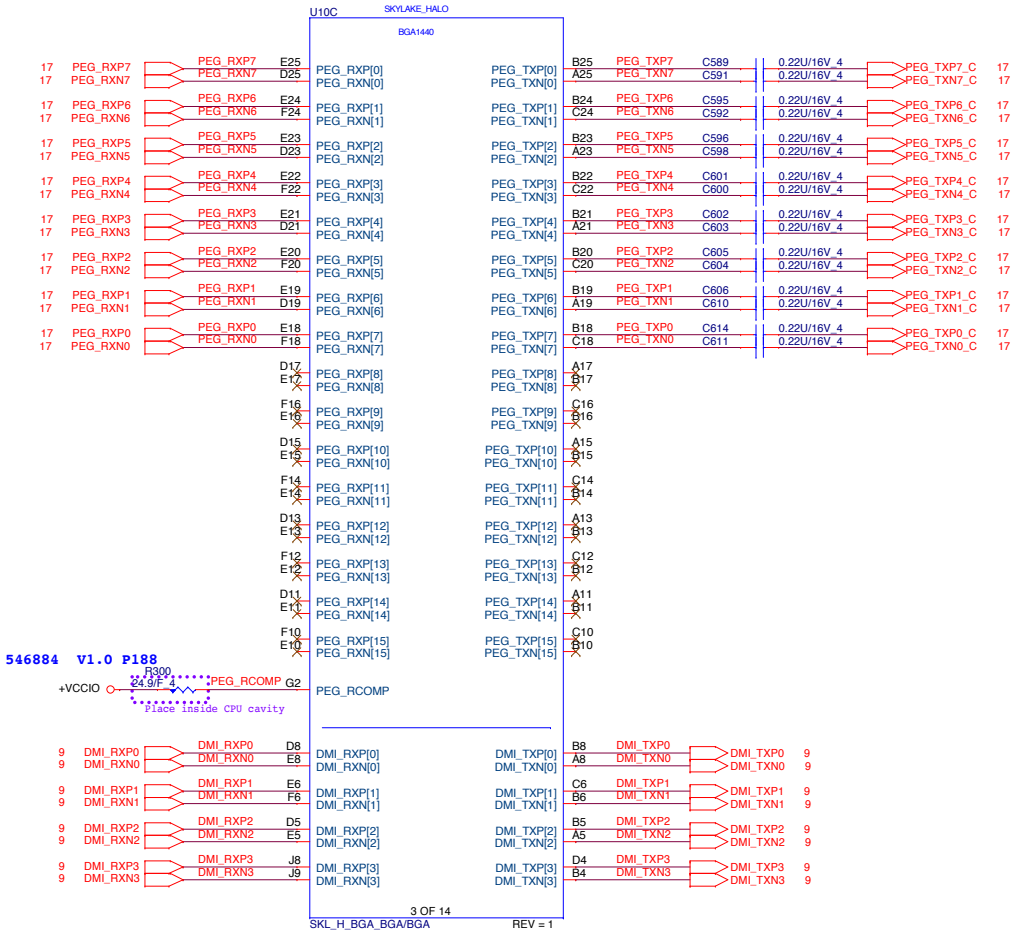
Quanta Computer Inc.

PROJECT : AM9A

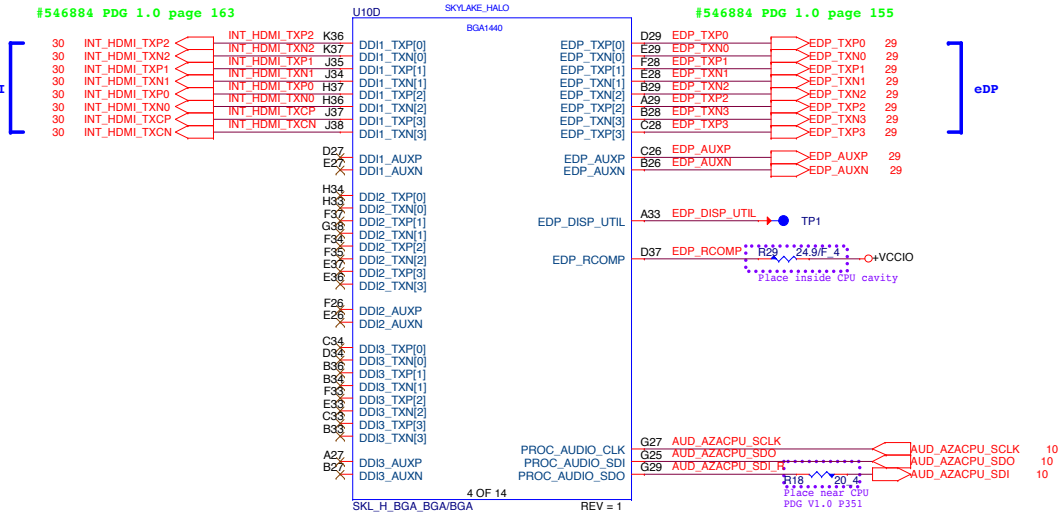
Size	Document Number	Rev
	CPU	A0

Date: Wednesday, August 19, 2015 Sheet 2 of 57

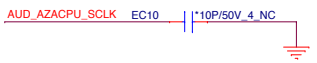
Skylake Processor (PEG, DMI)



Skylake Processor (DDI, eDP)

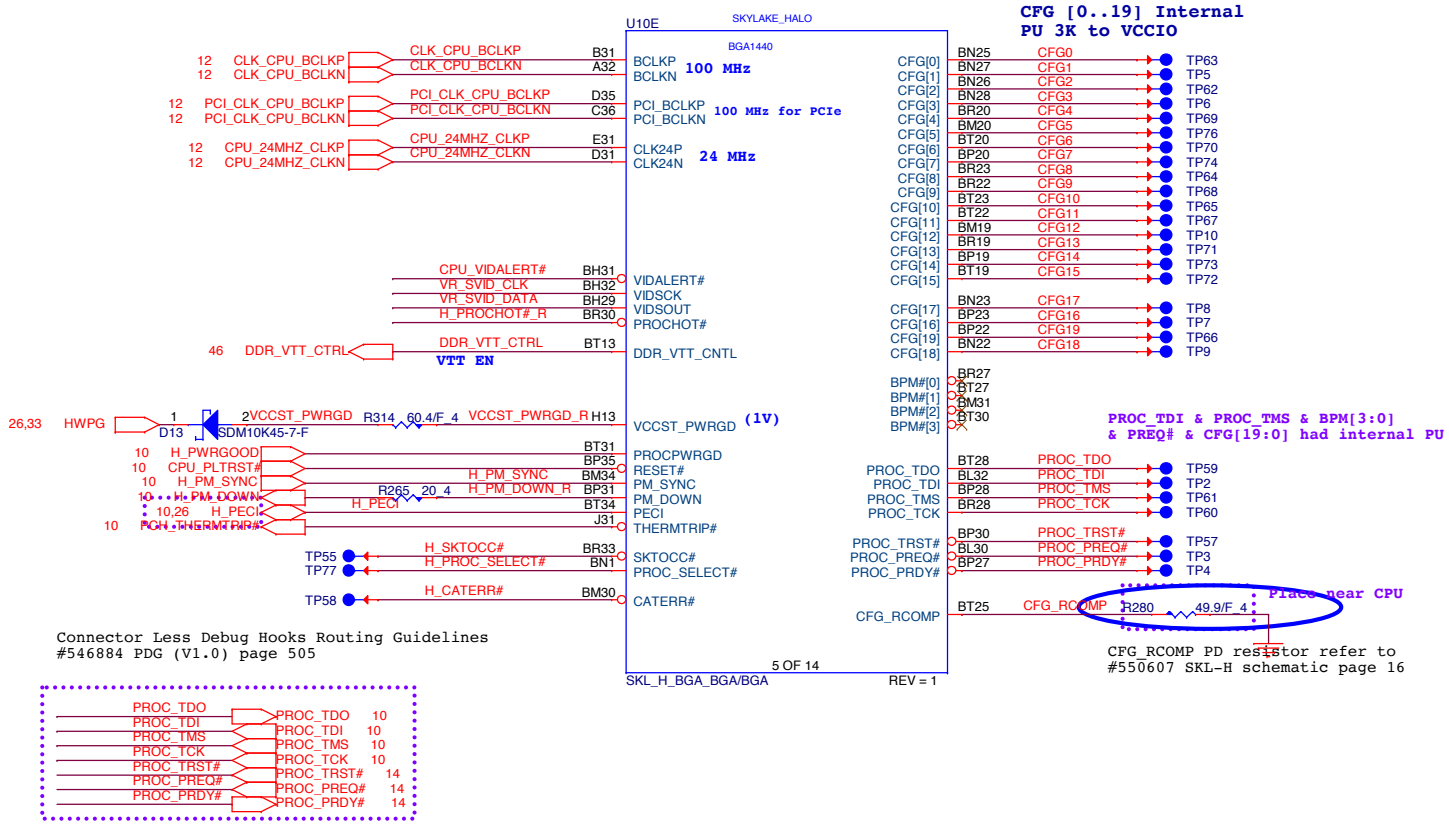


EMI



Quanta Computer Inc.			
PROJECT : AM9A			
Size	Document Number		Rev
	CPU		A0
Date: Wednesday, August 19, 2015		Sheet 3 of 57	

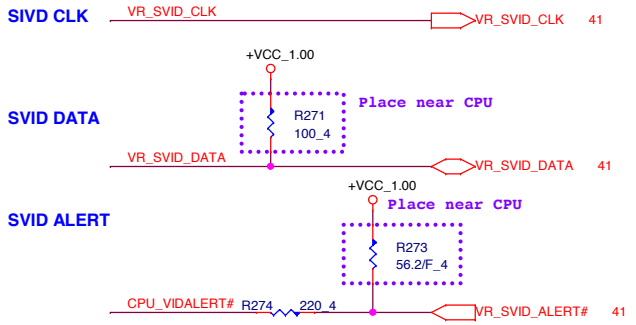
Skylake Processor (CLK, SVID, CFG)



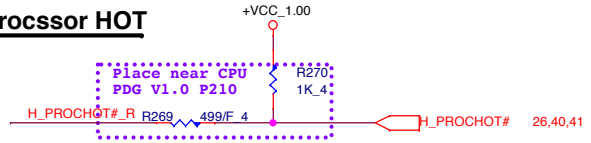
CPU STRAP PIN

Pin Name	Usage	Configuration	Circuitry
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	1 = (Default) Normal Operation; No stall. 0 = Stall.	CFG0 R281 *1K_4_NC
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal.	1 = Normal operation (Default) 0 = Lane numbers reversed.	CFG2 R279 1K_4
CFG[4]	eDP enable	1 = Disabled(Default) 0 = Enabled	CFG4 R283 1K_4
CFG[6:5]	PCI Express* Bifurcation	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express*(default)	CFG5 R288 1K_4 CFG6 R285 *1K_4_NC
CFG[7]	PEG Training	1 = PEG Train immediately following RESET# de-assertion.(default) 0 = PEG Wait for BIOS for training.	CFG7 R287 *1K_4_NC
CFG[1] CFG[3] CFG[19:8]	Reserved configuration lanes.		

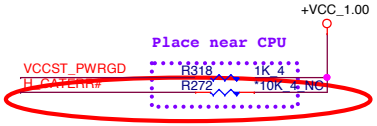
SVID



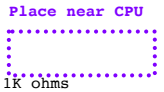
Procssor HOT



CPU PU/PD



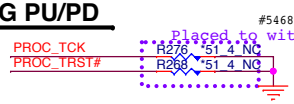
Thermtrip



Thermtrip PU 1K ohms
PDG #546884 P213

2/3 remove R186 1K_4
double PU

JTAG PU/PD



2/4 move R841 to PCH JTAG page
#546884 PDG 1.0 page 504

Quanta Computer Inc.
PROJECT : AM9A

Size	Document Number	Rev
	CPU	A0

Date: Wednesday, August 19, 2015 Sheet 4 of 57

04

PDG V1.0 #546844 page 573 VCC decoupling
47uFx4, 22uFx8, 10uFx28, 1uFx63

VCC = 60A (QC:35W+GT2)
VCC = 68A (QC:45W+GT2)

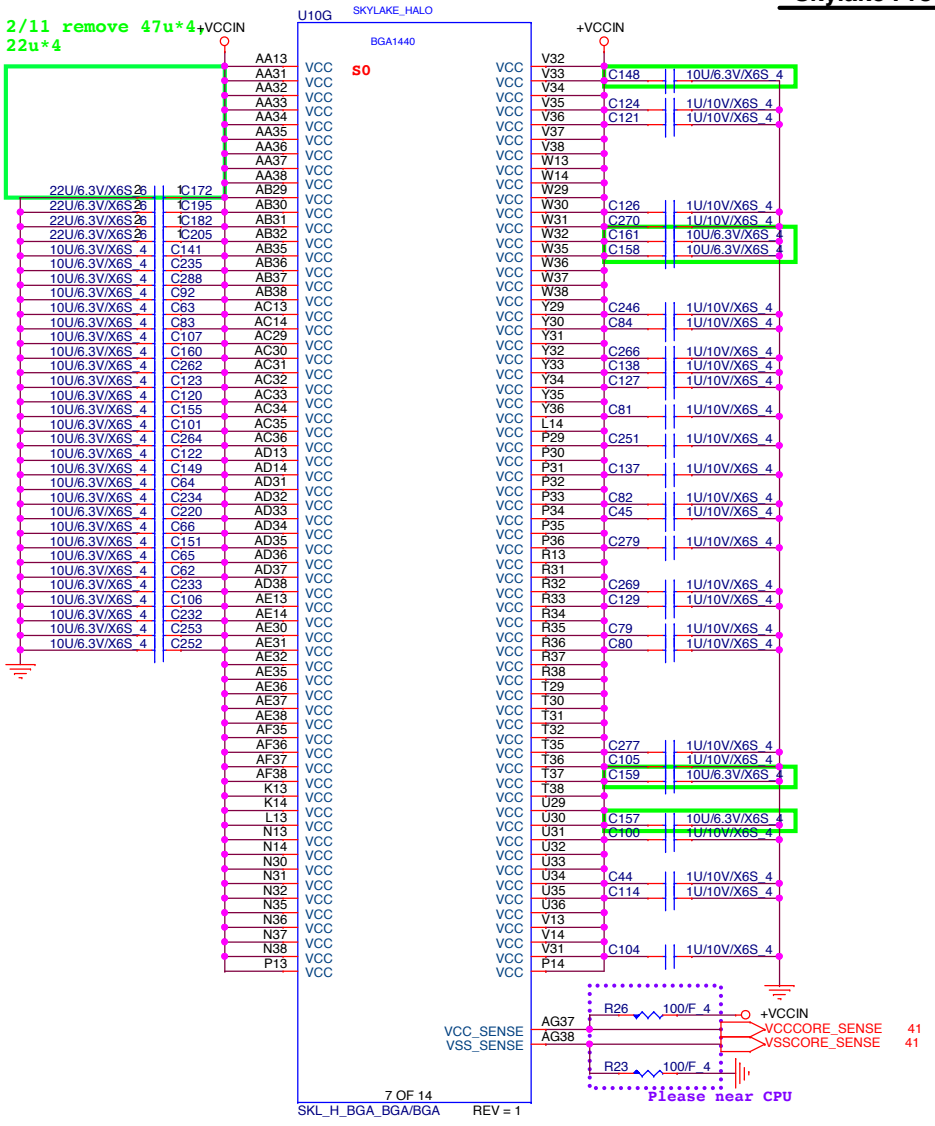
leverage other BU to optimums capacitor design

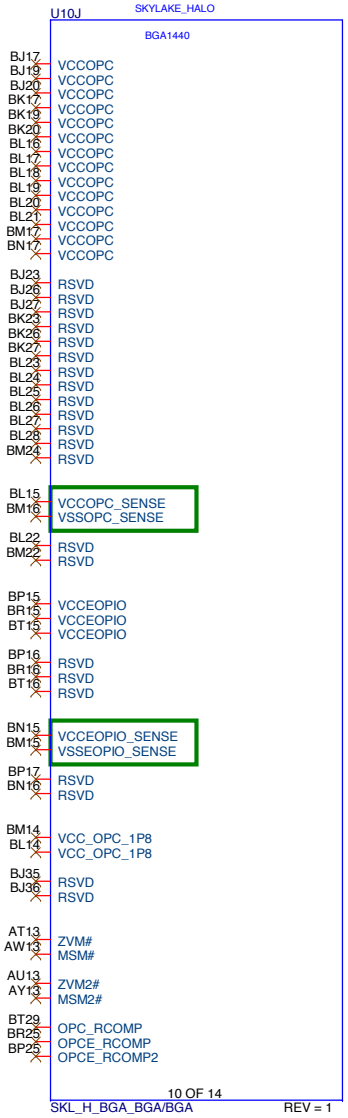
2/11 remove 47u*4
22u*4

Skylake Processor (POWER)

VCCOPC, VCCOPC_1p8, VCCEOPIO is OPC (On Package Cache)
realted power rail and used for 4+4e processor
Pandora support 4+2 Processor (w/o OPC)
Rail is unconnected for those pins w/o OPC
#544924 EDS (V0.92) page129 Note3

05





Unconnected for Processors without OPC.
#544924 EDS (V0.91) page121

Quanta Computer Inc.
PROJECT : AM9A

Size	Document Number	Rev
	CPU	A0
Date: Wednesday, August 19, 2015	Sheet 5 of 57	

PDG V1.0 #546844 page 573 & 574 decoupling capacitor
VCCSA: 220uFx1, 47uFx1, 10uFx10, 1uFx3
VCCIO: 47uFx2, 10uFx3, VDDQ: 22uFx4, 10uFx10
VDDQC: 10uFx1, VCCST:1uFx1, VCCSTG: 1uFx1
VCCPLL: 1uFx1, VCCPLL_OC: 1uFx2,

EDS V0.92 #544924 page 135~140 power rail
VDDQ: 1.35V/2.8A (DDR3L), 1.2V/2.8A (DDR4/LPDDR3)
VCCSA: 0.55~1.15V/11.1A, VCCIO: 0.95V/5.5A
VCCST: 1.0V/120mA, VCCPLL: 1.0V/145mA

06

leverage other BU to optimums capacitor design

2/11 47u*1 change to 22u*2

2/9 remove 1*10u

22uFx4 Please near VR

2/11 47u*2 change to 22u*4, 2pcs NC

2/11 22u*2 change to NC

4/31 change to 1u

Skylake Processor (POWER)

U10I SKYLAKE_HALO BGA1440

9 OF 14

SKL_H_BGA_BGA/BGA REV = 1

U10K SKYLAKE_HALO BGA1440

11 OF 14

SKL_H_BGA_BGA/BGA REV = 1

VCCPLL_OC source from VDDQ
EDS V0.92 #544924 P129 note 4 & 5

VCCSTG source from VCCST
EDS V0.92 #544924 P129 note 4 & 5

Debug pin

Place near CPU

VDDQC for SKL - U/Y series, H series left NC.
#550607 reference schematic P18

0430 add bom

Quanta Computer Inc.
PROJECT : AM9A

Size	Document Number	Rev
	CPU	A0

Date: Wednesday, August 19, 2015 Sheet 6 of 57

PDG V1.0 #546884 P573-574 decupling
47uFx6, 22uFx8, 10uFx35, 1uFx68.

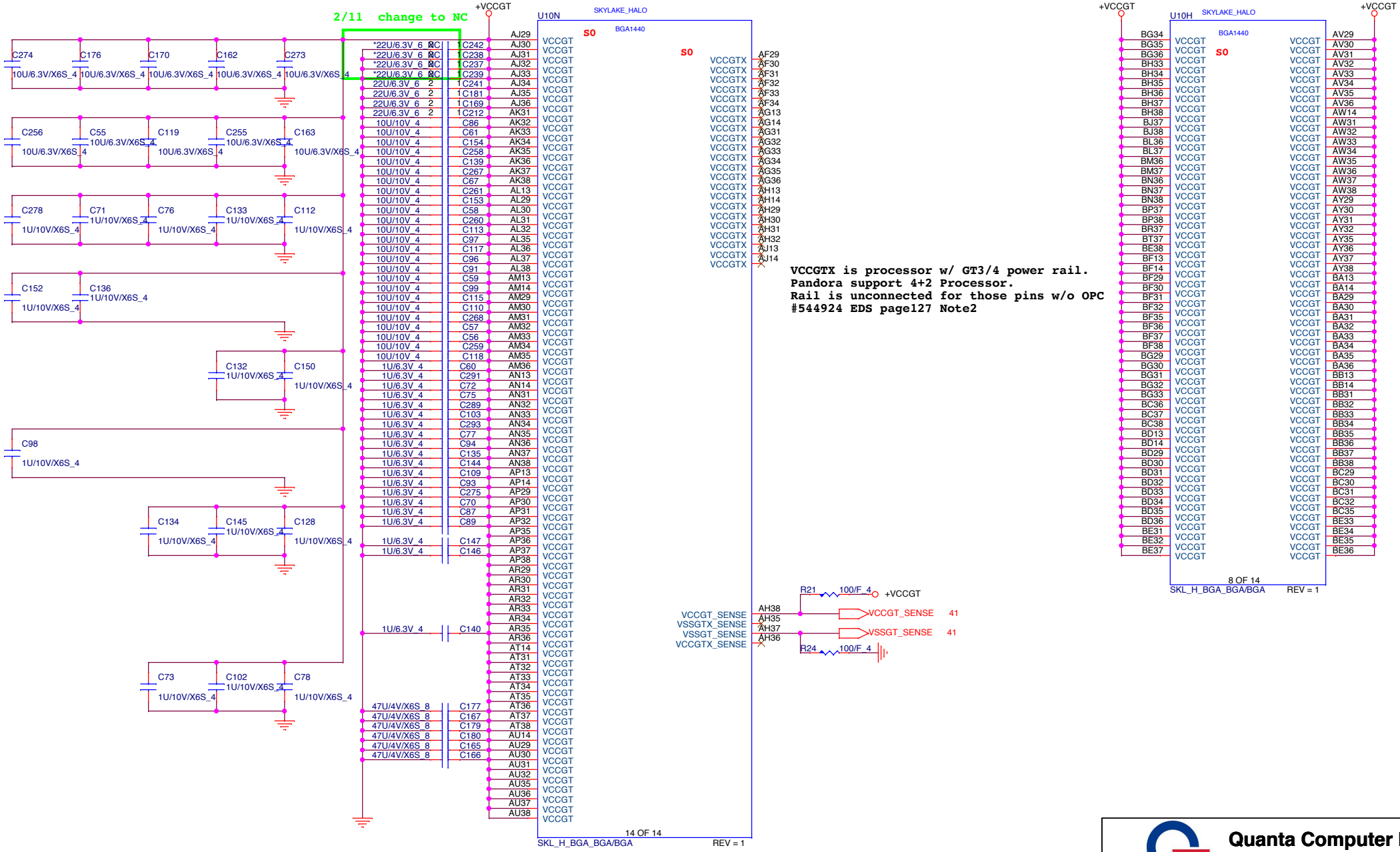
07

leverage other BU to optimums capacitor design

Skylake Processor (POWER)

VCCGT = 55A (QC+GT2)

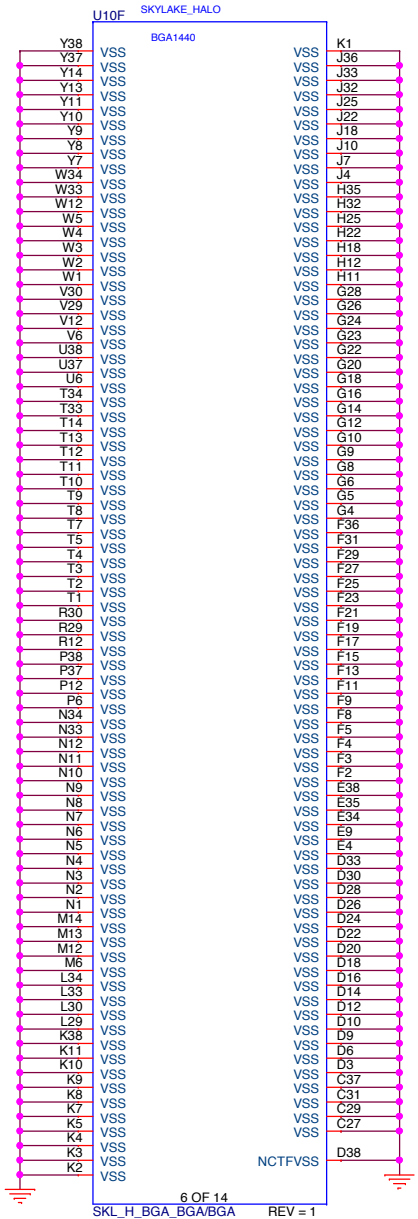
2/11 change to NC

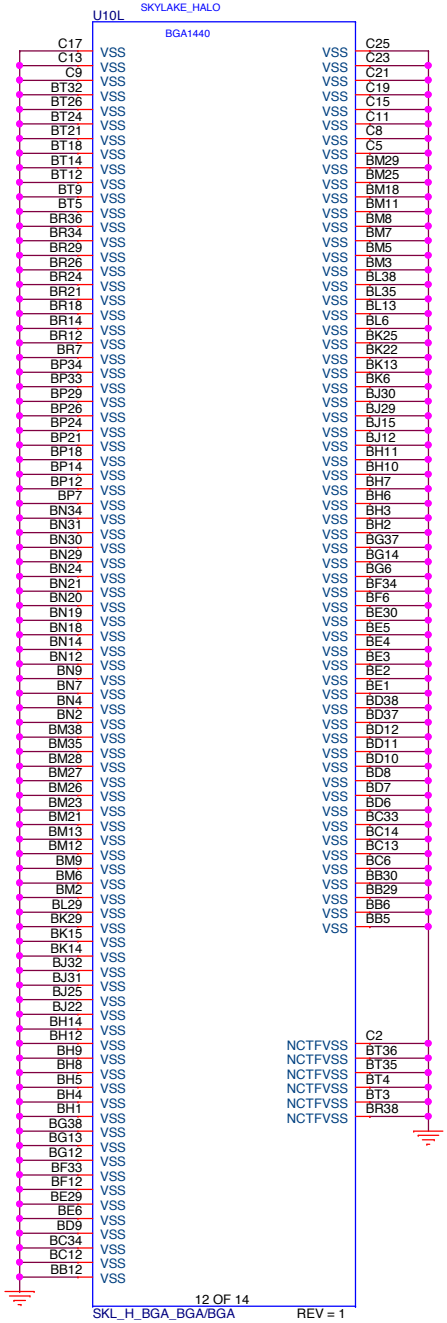


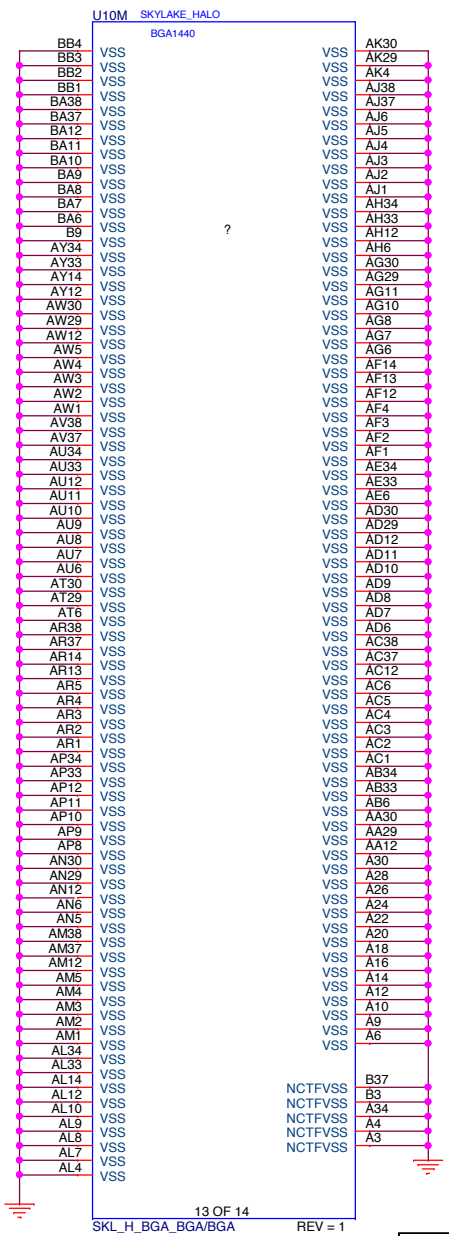
VCCGTX is processor w/ GT3/4 power rail.
Pandora support 4+2 Processor.
Rail is unconnected for those pins w/o OPC
#544924 EDS page127 Note2

Quanta Computer Inc.			
PROJECT : AM9A			
Size	Document Number: CPU		Rev: A0
Date: Wednesday, August 19, 2015	Sheet 7 of 57		

Skylake Processor (GROUND)







Quanta Computer Inc.

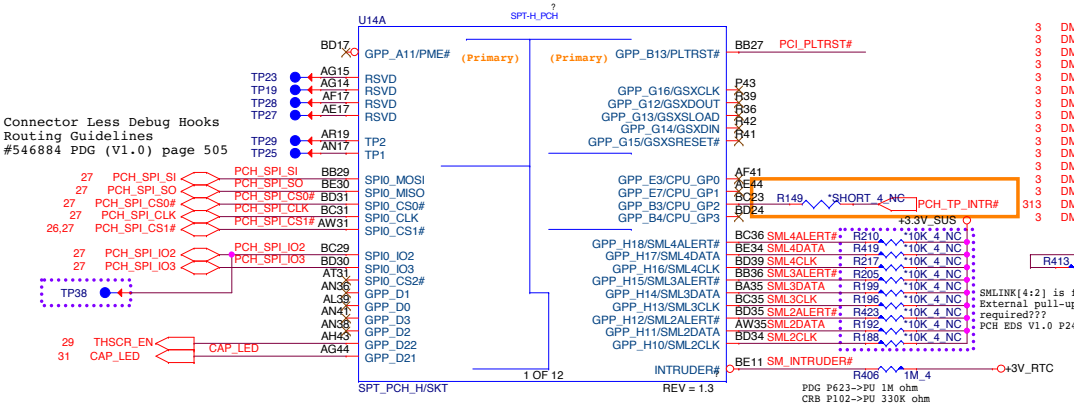
PROJECT : AM9A

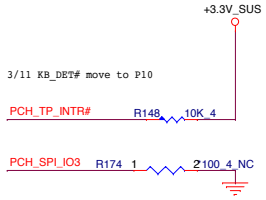
Size	Document Number	Rev
	CPU	A0
Date: Wednesday, August 19, 2015	Sheet 8 of 57	

SPT-H PCH (SPI)

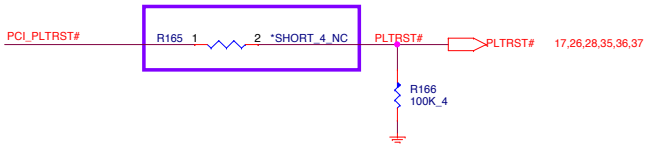
SPI_CS0# for 1st SPI device, SPI_CS1# for second SPI device, SPI_CS3# for TPM.
#546884 PDG (V1.0) page 620

Connector Less Debug Hooks Routing Guidelines
#546884 PDG (V1.0) page 505

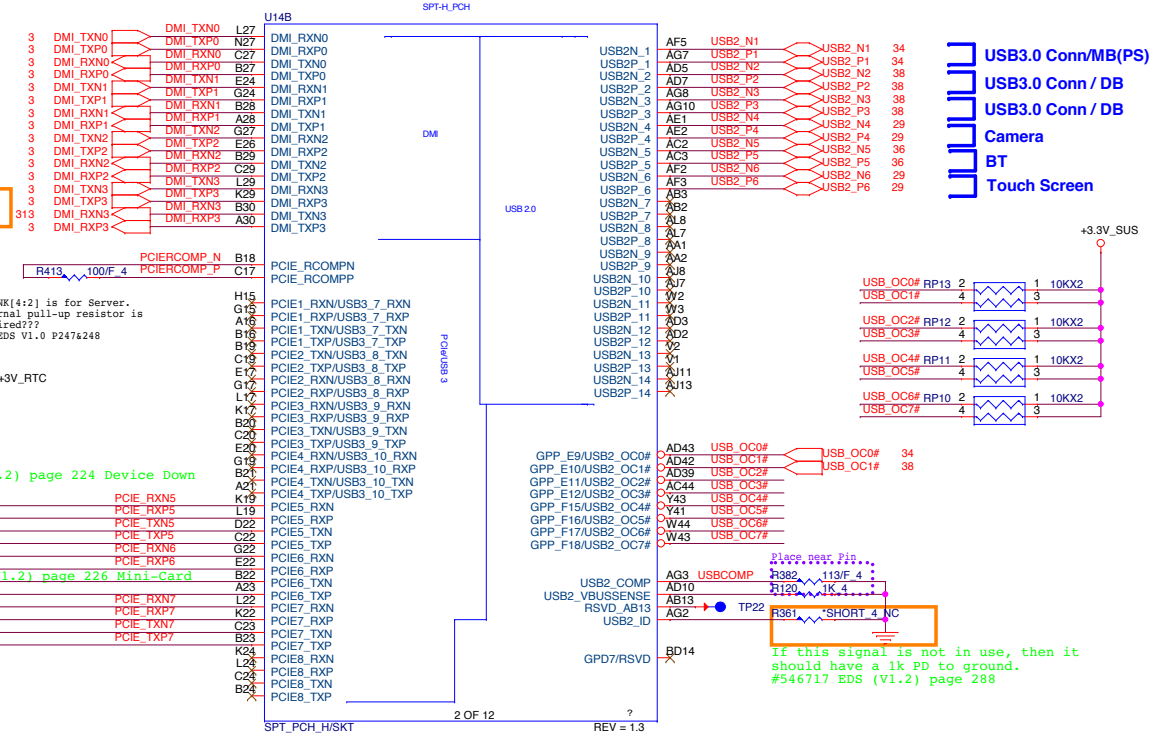


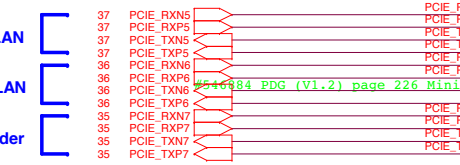


PLTRST# Buffer



SPT-H PCH (DMI/PCIE/USB3/USB2)





Quanta Computer Inc.			
PROJECT : AM9A			
Size	Document Number		Rev
	PCH		A0
Date: Wednesday, August 19, 2015		Sheet 9 of 57	

SPT-H PCH (PCIE/SATA/FAN/CLINK)

SPT-H PCH (AUDIO/SMBus/JTAG)

S0 Sleep Control: When PCH is idle and processor is in C10 state, this pin will assert to indicate VR controller can go into a light load mode. This signal can also be connected to EC for other power management related optimizations.

10

Leakage Isolation

RTC Circuitry

PCH PU/PD setting

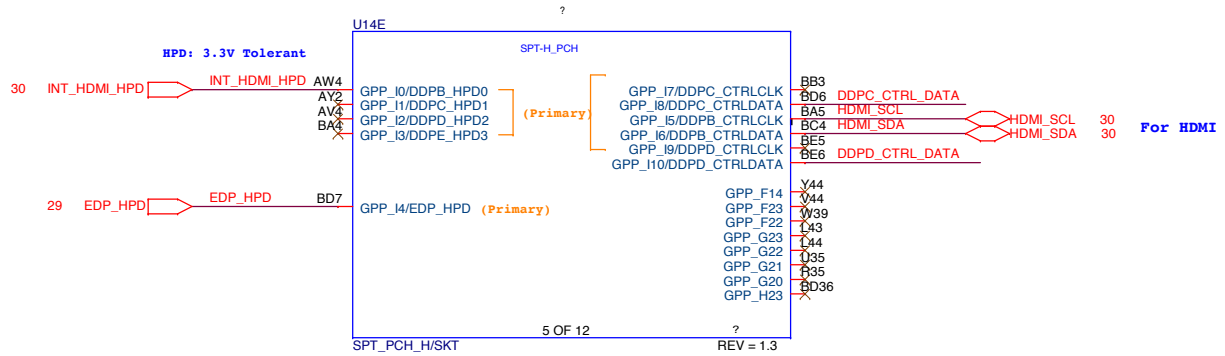
PCH STRAPING <546717 Rev0.91>

Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR / GPP_B14	Top Swap Override	PCH_PWROK	0 = Disable (Default) 1 = Enable	ACZ_SPKR R175 *1K_4_NC +3.3V_RUN
SMBALERT# / GPP_C2	TLS Confidentiality	RSMRST#	0 = Disable(Default) 1 = Enable (support IAMT and iSBA with iTLS)	SMBALERT# R219 *1K_4_NC +3.3V_SUS
SML0ALERT# / GPP_C5	eSPI or LPC	RSMRST#	0 = LPC Is selected for EC(Default) 1 = eSPI Is selected for EC.	SML0ALERT# R218 *1K_4_NC +3.3V_SUS
HDA_SDO	Flash Descriptor Security Override	PCH_PWROK	0 = Enable(Default) 1 = Disable (override)	26 PCH_MELOCK R140 1K_4 HDA_SDO_R

Quanta Computer Inc.
PROJECT : AM9A

Size	Document Number	Rev
	PCH	A0

Date: Wednesday, August 19, 2015 Sheet 10 of 57



PCH STRAPING <546717 Rev0.91>

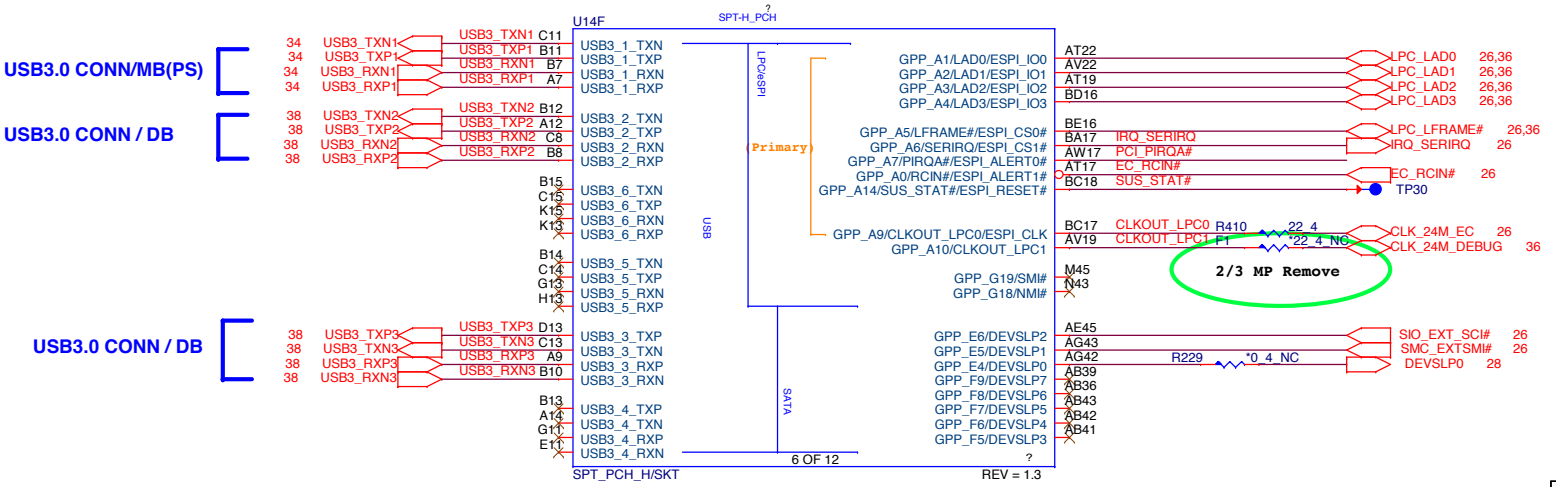
Pin Name	Usage	Sampled	Configuration	Circuitry
DDPB_CTRLDATA/GPP_I6	Display Port B Detected	PCH_PWROK	0 = Port B is not detected. (Default) 1 = Port B is detected.	#546884 PDG page170 (V1.0) HDMI_SCL 4 3 HDMI_SDA 2 1 RP8 2.2KX2 +3.3V_RUN
DDPC_CTRLDATA/GPP_I8	Display Port C Detected	PCH_PWROK	0 = Port C is not detected. (Default) 1 = Port C is detected.	DDPC_CTRL_DATA R387 *1K_4_NC +3.3V_RUN
DDPD_CTRLDATA/GPP_I10	Display Port D Detected	PCH_PWROK	0 = Port D is not detected. (Default) 1 = Port D is detected.	DDPD_CTRL_DATA R395 *1K_4_NC +3.3V_RUN

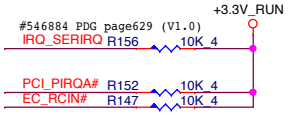
SPT-H PCH (USB3/LPC/eSPI)

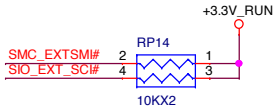
USB3.0 CONN/MB(PS)

USB3.0 CONN / DB

USB3.0 CONN / DB







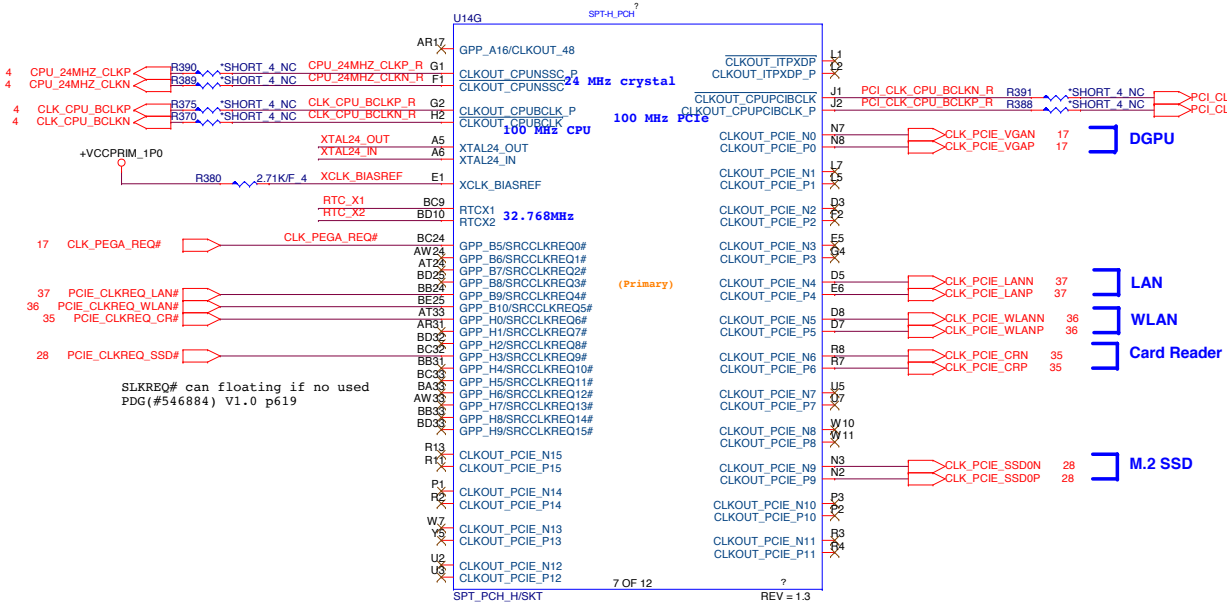
EMI

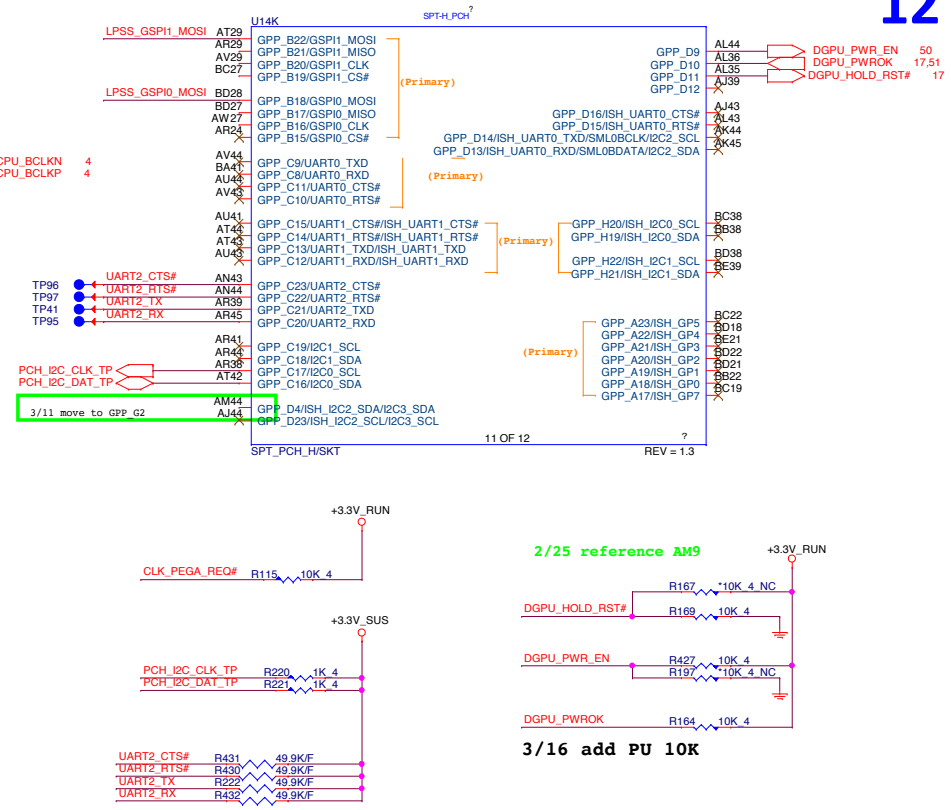
Quanta Computer Inc.

PROJECT : AM9A

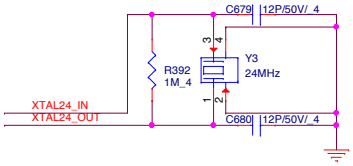
Size	Document Number	Rev
	PCH	A0
Date: Wednesday, August 19, 2015	Sheet 11 of 57	

Skylake PCH (CLOCK)

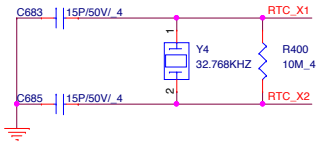




24MHz



RTC Clock 32.768KHz



PCH STRAPING <546717 Rev0.91>

Pin Name	Usage	Sampled	Configuration	Circuitry
GSPI0_MOSI/GPP_B18	No Reboot	PCH_PWROK	0 = Disable(Default) 1 = Enable	LPSS_GSPI0_MOSI R414 *1K_4_NC +3.3V_SUS
GSPI1_MOSI/GPP_B22	Boot BIOS Strap Bit BBS	PCH_PWROK	Bit6 Boot BIOS Destination 0 SPI(Default) 1 LPC	LPSS_GSPI1_MOSI R168 *1K_4_NC +3.3V_SUS

Quanta Computer Inc.

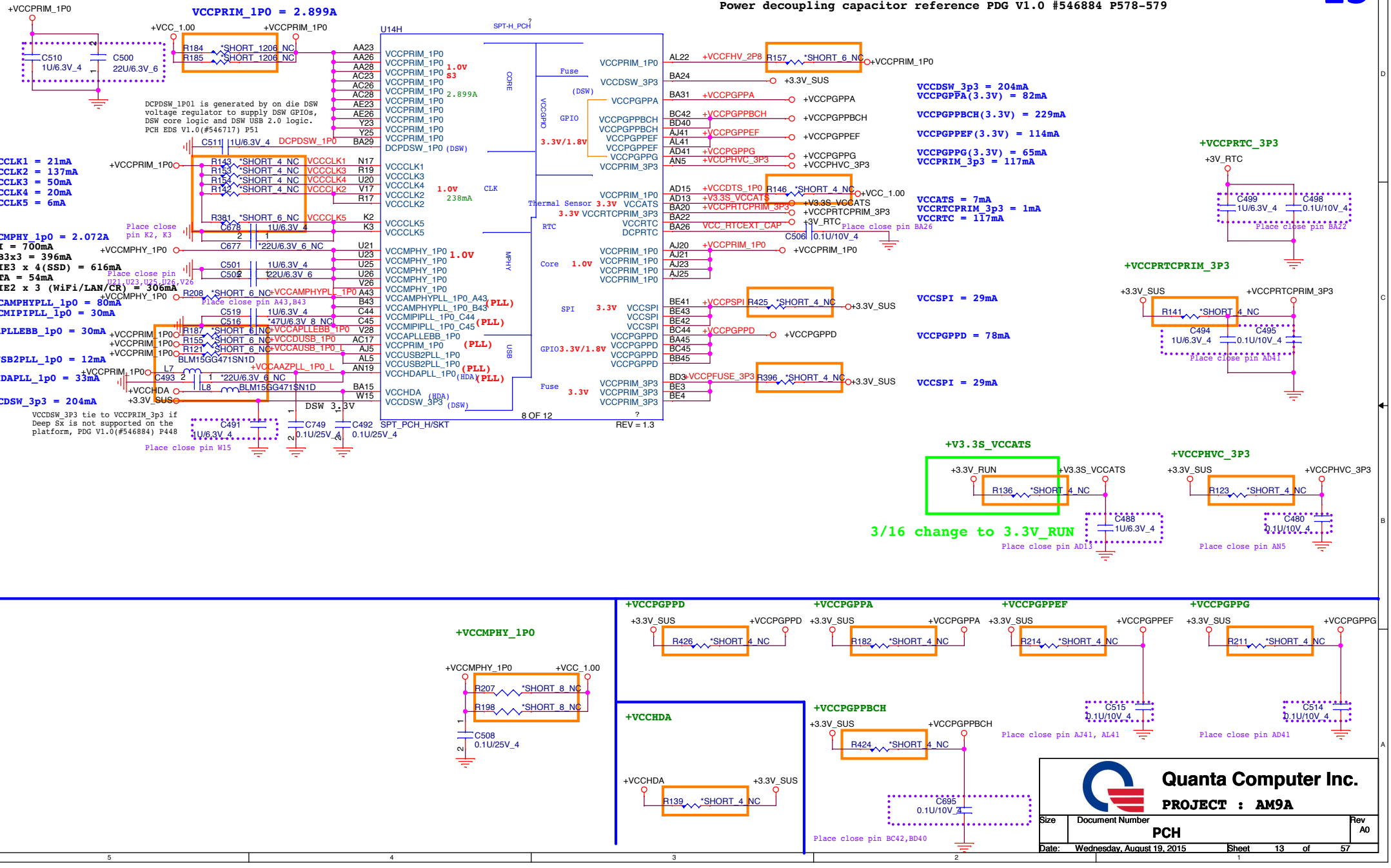
PROJECT : AM9A

Size	Document Number	Rev
	PCH	A0

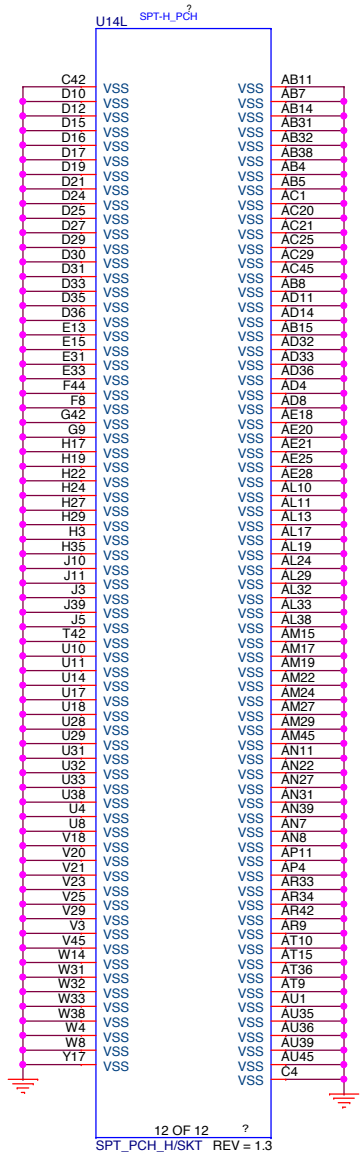
Date: Wednesday, August 19, 2015 Sheet 12 of 57

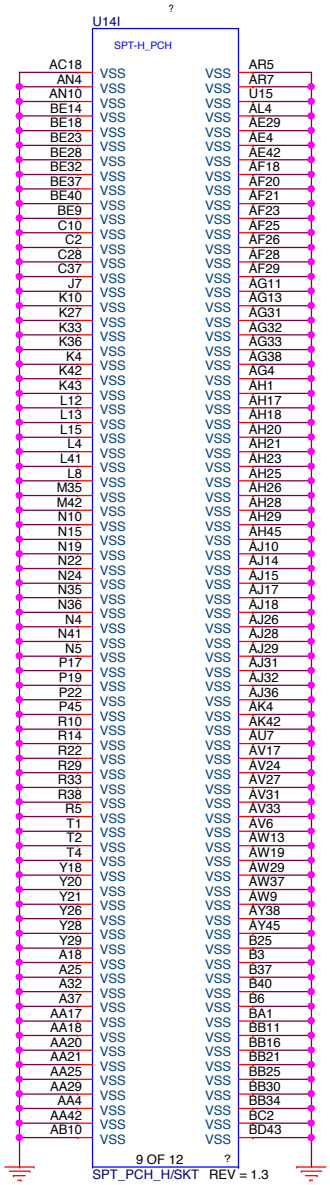
Skylake PCH (POWER)

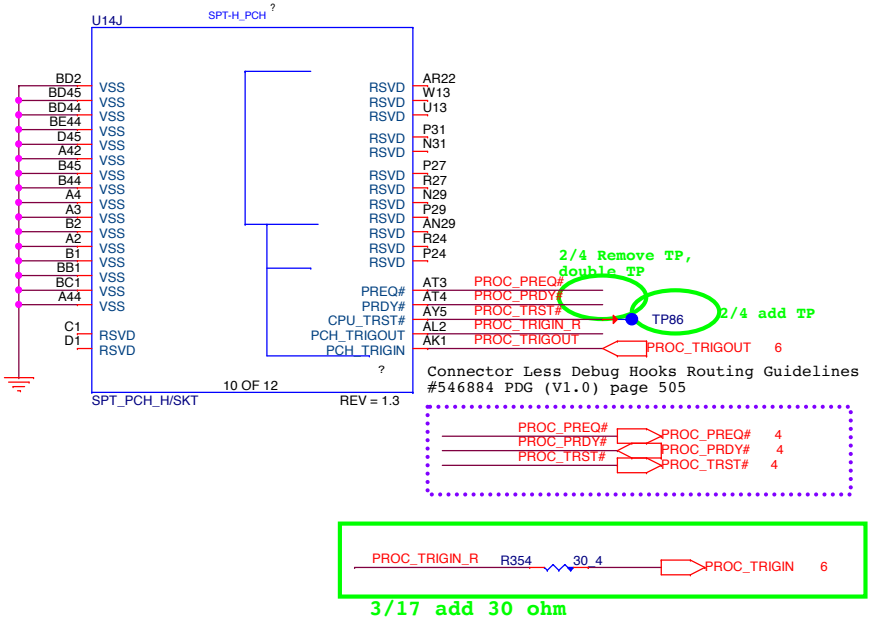
Power Rating refernce EDS V1.0 #546717 P59-60
Power decoupling capacitor reference PDG V1.0 #546884 P578-579



Quanta Computer Inc.			
PROJECT : AM9A			
Size	Document Number		Rev
	PCH		A0
Date: Wednesday, August 19, 2015		Sheet 13 of 57	

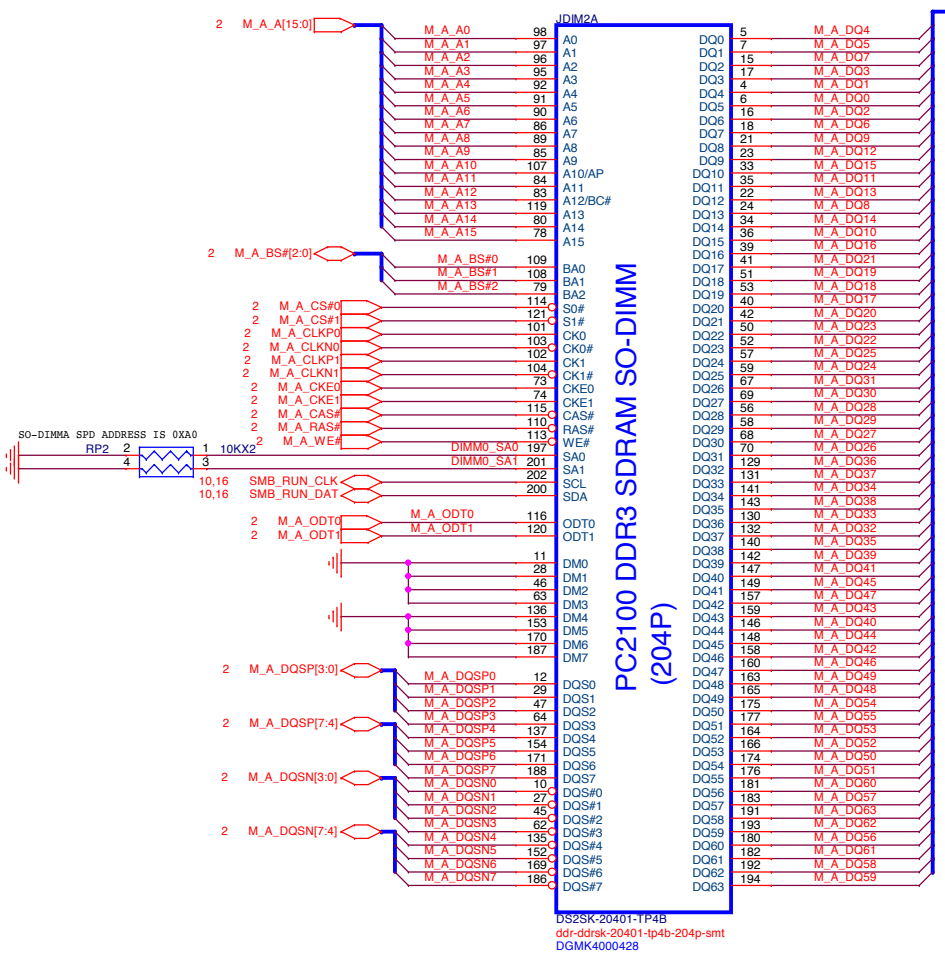




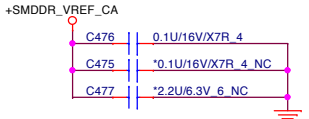


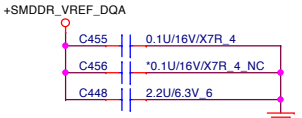
Quanta Computer Inc.		
PROJECT : AM9A		
Size	Document Number	Rev
	PCH	A0
Date: Wednesday, August 19, 2015	Sheet 14 of 57	

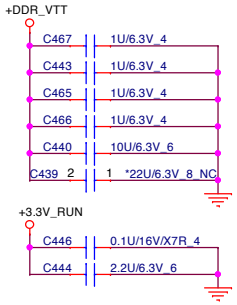
Place these Caps near So-Dimm2.

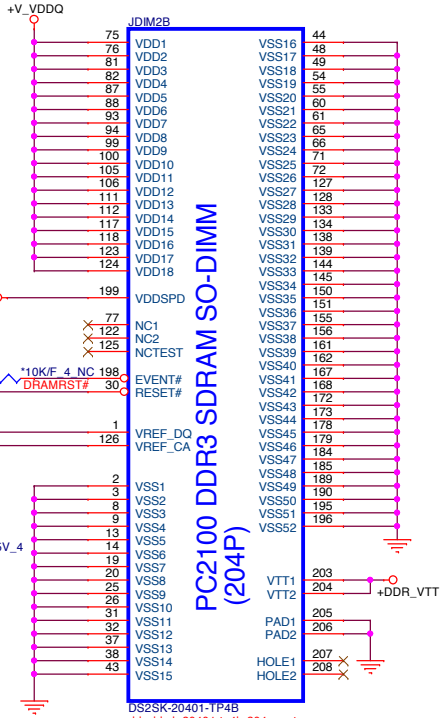


H =4.0mm

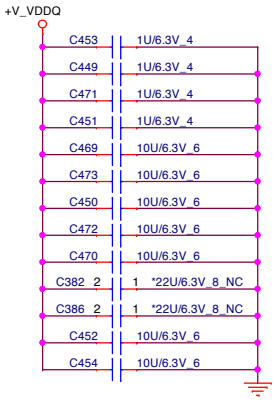




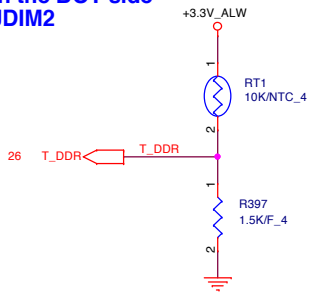


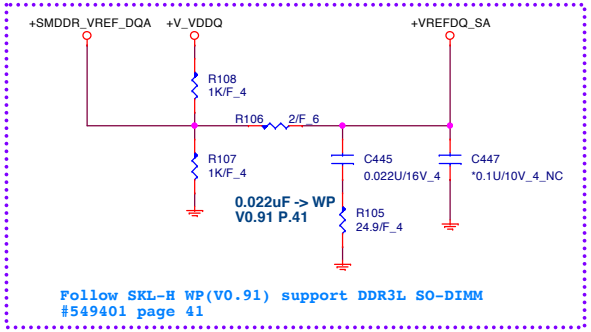


H = 4.0mm



Pleace on the BOT side
Near to JDIM2



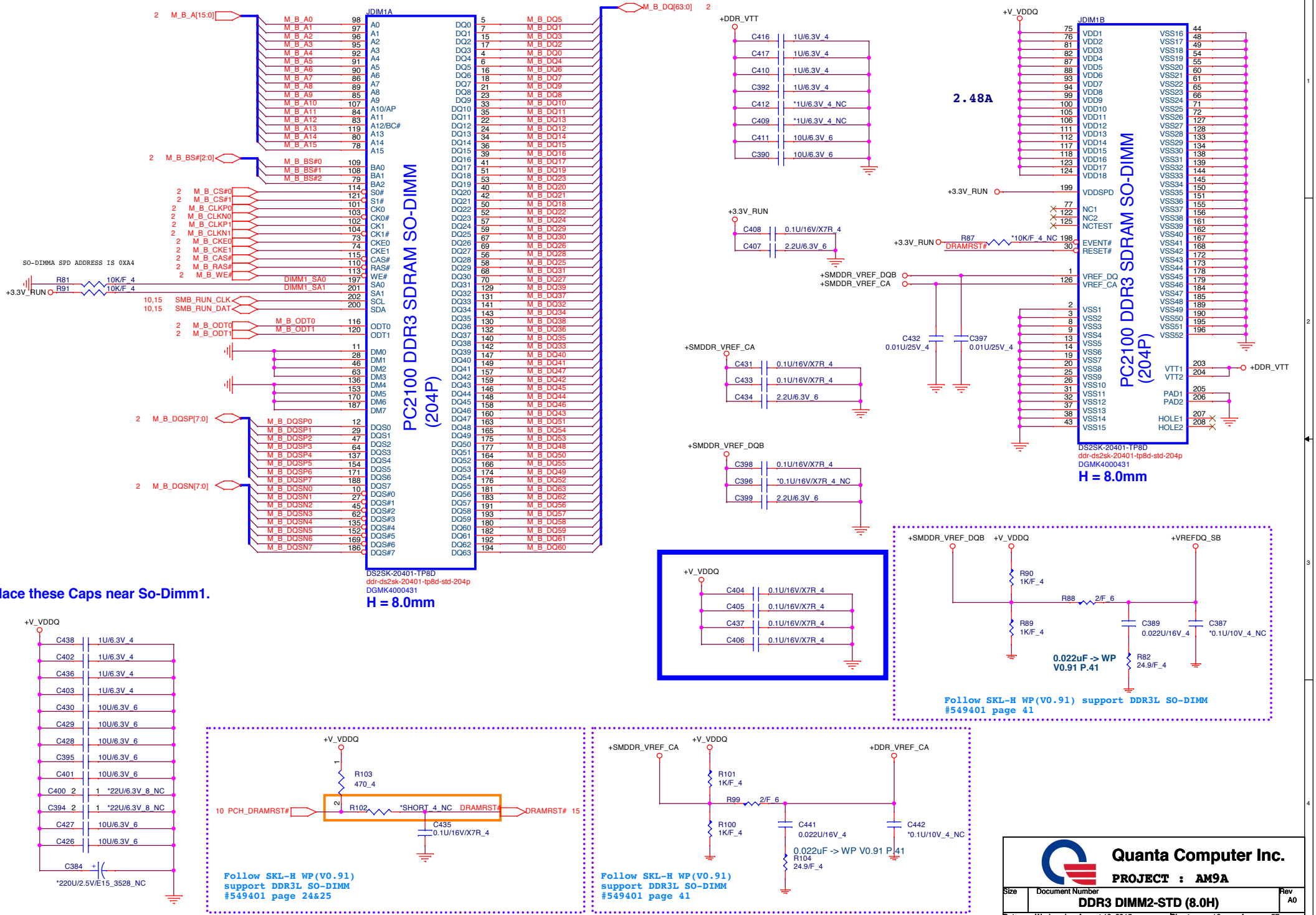


Quanta Computer Inc.

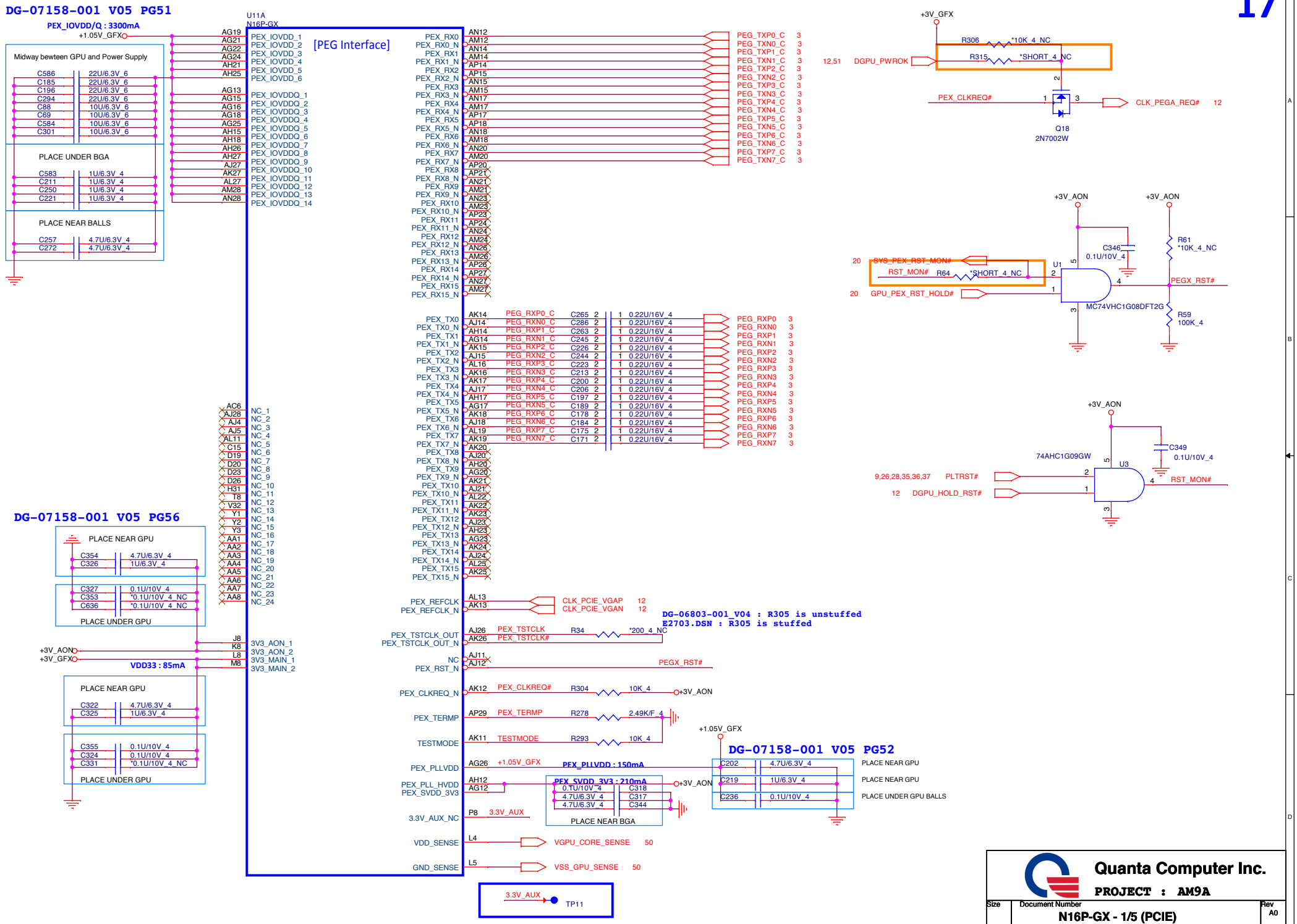
PROJECT : AM9A

Size	Document Number	Rev
	DDR3 DIMM1-STD (4.0H)	A0

Date: Wednesday, August 19, 2015 Sheet 15 of 57



Quanta Computer Inc.		
PROJECT : AM9A		
Size	Document Number: DDR3 DIMM2-STD (8.0H)	Rev: A0
Date: Wednesday, August 19, 2015	Sheet 16 of 57	


DG-07158-001 V05 PG51
PEX_IOVDD/Q : 3300mA
+1.05V_GFX
Midway bewteen GPU and Power Supply
C586 22U/6.3V_6
C185 22U/6.3V_6
C196 22U/6.3V_6
C294 22U/6.3V_6
C88 10U/6.3V_6
C69 10U/6.3V_6
C584 10U/6.3V_6
C301 10U/6.3V_6
PLACE UNDER BGA
C583 1U/6.3V_4
C211 1U/6.3V_4
C250 1U/6.3V_4
C221 1U/6.3V_4
PLACE NEAR BALLS
C257 4.7U/6.3V_4
C272 4.7U/6.3V_4
U11A
N16P-GX
[PEG Interface]
PEX_IOVDD_1
PEX_IOVDD_2
PEX_IOVDD_3
PEX_IOVDD_4
PEX_IOVDD_5
PEX_IOVDD_6
PEX_IOVDDQ_1
PEX_IOVDDQ_2
PEX_IOVDDQ_3
PEX_IOVDDQ_4
PEX_IOVDDQ_5
PEX_IOVDDQ_6
PEX_IOVDDQ_7
PEX_IOVDDQ_8
PEX_IOVDDQ_9
PEX_IOVDDQ_10
PEX_IOVDDQ_11
PEX_IOVDDQ_12
PEX_IOVDDQ_13
PEX_IOVDDQ_14
PEX_RX0
PEX_RX0_N
PEX_RX1
PEX_RX1_N
PEX_RX2
PEX_RX2_N
PEX_RX3
PEX_RX3_N
PEX_RX4
PEX_RX4_N
PEX_RX5
PEX_RX5_N
PEX_RX6
PEX_RX6_N
PEX_RX7
PEX_RX7_N
PEX_RX8
PEX_RX8_N
PEX_RX9
PEX_RX9_N
PEX_RX10
PEX_RX10_N
PEX_RX11
PEX_RX11_N
PEX_RX12
PEX_RX12_N
PEX_RX13
PEX_RX13_N
PEX_RX14
PEX_RX14_N
PEX_RX15
PEX_RX15_N
PEG_TXP0_C
PEG_TXN0_C
PEG_TXP1_C
PEG_TXN1_C
PEG_TXP2_C
PEG_TXN2_C
PEG_TXP3_C
PEG_TXN3_C
PEG_TXP4_C
PEG_TXN4_C
PEG_TXP5_C
PEG_TXN5_C
PEG_TXP6_C
PEG_TXN6_C
PEG_TXP7_C
PEG_TXN7_C
PEX_TX0
PEX_TX0_N
PEX_TX1
PEX_TX1_N
PEX_TX2
PEX_TX2_N
PEX_TX3
PEX_TX3_N
PEX_TX4
PEX_TX4_N
PEX_TX5
PEX_TX5_N
PEX_TX6
PEX_TX6_N
PEX_TX7
PEX_TX7_N
PEX_TX8
PEX_TX8_N
PEX_TX9
PEX_TX9_N
PEX_TX10
PEX_TX10_N
PEX_TX11
PEX_TX11_N
PEX_TX12
PEX_TX12_N
PEX_TX13
PEX_TX13_N
PEX_TX14
PEX_TX14_N
PEX_TX15
PEX_TX15_N
PEG_RXP0_C
PEG_RXN0_C
PEG_RXP1_C
PEG_RXN1_C
PEG_RXP2_C
PEG_RXN2_C
PEG_RXP3_C
PEG_RXN3_C
PEG_RXP4_C
PEG_RXN4_C
PEG_RXP5_C
PEG_RXN5_C
PEG_RXP6_C
PEG_RXN6_C
PEG_RXP7_C
PEG_RXN7_C
0.22U/16V_4
PEG_RXP0
PEG_RXN0
PEG_RXP1
PEG_RXN1
PEG_RXP2
PEG_RXN2
PEG_RXP3
PEG_RXN3
PEG_RXP4
PEG_RXN4
PEG_RXP5
PEG_RXN5
PEG_RXP6
PEG_RXN6
PEG_RXP7
PEG_RXN7
NC_1
NC_2
NC_3
NC_4
NC_5
NC_6
NC_7
NC_8
NC_9
NC_10
NC_11
NC_12
NC_13
NC_14
NC_15
NC_16
NC_17
NC_18
NC_19
NC_20
NC_21
NC_22
NC_23
NC_24
PEX_REFCLK
PEX_REFCLK_N
CLK_PCIE_VGAP
CLK_PCIE_VGAN
DG-06803-001_V04 : R305 is unstuffed
E2703.DSN : R305 is stuffed
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N
PEX_TSTCLK
PEX_TSTCLK#
R34
*200_4_NC
NC
PEX_RST_N
PEGX_RST#
PEX_CLKREQ_N
PEX_CLKREQ#
R304
10K_4
+3V_AON
PEX_TERMP
R278
2.49K/F_4
TESTMODE
R293
10K_4
PEX_PLLVDD
+1.05V_GFX
PEX_PLLVDD : 150mA
PEX_PLL_HVDD
PEX_SVDD_3V3
PEX_SVDD_3V3 : 210mA
3.3V_AUX_NC
3.3V_AUX
VDD_SENSE
VGPU_CORE_SENSE
GND_SENSE
VSS_GPU_SENSE
TP11
DG-07158-001 V05 PG56
PLACE NEAR GPU
C354 4.7U/6.3V_4
C326 1U/6.3V_4
C327 0.1U/10V_4
C353 *0.1U/10V_4_NC
C636 *0.1U/10V_4_NC
PLACE UNDER GPU
+3V_AON
+3V_GFX
VDD33 : 85mA
3V3_AON_1
3V3_AON_2
3V3_MAIN_1
3V3_MAIN_2
C322 4.7U/6.3V_4
C325 1U/6.3V_4
C355 0.1U/10V_4
C324 0.1U/10V_4
C331 *0.1U/10V_4_NC
DG-07158-001 V05 PG52
C202 4.7U/6.3V_4
C219 1U/6.3V_4
C236 0.1U/10V_4
PLACE NEAR GPU
PLACE NEAR GPU
PLACE UNDER GPU BALLS
C318 0.1U/10V_4
C317 4.7U/6.3V_4
C344 4.7U/6.3V_4
PLACE NEAR BGA
+3V_GFX
R306 *10K_4_NC
R315 *SHORT_4_NC
12,51 DGPU_PWROK
PEX_CLKREQ#
CLK_PEGA_REQ# 12
Q18
2N7002W
+3V_AON
C346 0.1U/10V_4
R61 *10K_4_NC
20 SYS_PEX_RST_MON#
RST_MON#
R64 *SHORT_4_NC
20 GPU_PEX_RST_HOLD#
U1
MC74VHC1G08DFT2G
PEGX_RST#
R59 100K_4
+3V_AON
C349 0.1U/10V_4
74AHC1G09GW
U3
9,26,28,35,36,37 PLTRST#
12 DGPU_HOLD_RST#
RST_MON#
Quanta Computer Inc.
PROJECT : AM9A
Size
Document Number
N16P-GX - 1/5 (PCIE)
Rev A0
Date: Wednesday, August 19, 2015
Sheet 17 of 57

U11B
N16P-GX
[MEMORY I/F A]

U11C
N16P-GX
MEMORY I/F C

GDDR5 NO USE

GDDR5 NO USE

DG-07158-001 V05 PG48

PLACE CLOSE UNDER GPU

PLACE CLOSE TO NEAE GPU

5/20 change to HCB1608KF-300T30
DG-07158-001 V05 PG50
change to CX300T30000

near to GPU
under GPU
Close to GPU BALL
near to GPU

C276 close to H17 (under GPU)

PLACE CLOSE TO GPU BALLS

1201

Quanta Computer Inc.
PROJECT : AM9A

Size	Document Number	Rev
	N16P-GX - 2/5 (Memory)	A0

Date: Wednesday, August 19, 2015 Sheet 18 of 57

U11D
N16P-GX

[IFPA/B_LVDS]
AH8 IFPAB_PLLVDD
AG8 IFPA_IOVDD
AG9 IFPB_IOVDD
AJ8 IFPAB_RSET
IFPA_TXC AM6
IFPA_TXC_N AN6
IFPA_TXD0 AP3
IFPA_TXD0_N AN3
IFPA_TXD1 AN5
IFPA_TXD1_N AM5
IFPA_TXD2 AL6
IFPA_TXD2_N AK6
IFPA_TXD3 AJ6
IFPA_TXD3_N AH6
IFPB_TXC AJ9
IFPB_TXC_N AH9
IFPB_TXD4 AP6
IFPB_TXD4_N AP5
IFPB_TXD5 AM7
IFPB_TXD5_N AL7
IFPB_TXD6 AN8
IFPB_TXD6_N AM8
IFPB_TXD7 AK8
IFPB_TXD7_N AL8

[IFPC/D_TMDS]
AF7 IFPC_PLLVDD
AG7 IFPD_PLLVDD
AF6 IFPC_IOVDD
AG6 IFPD_IOVDD
AF8 IFPC_RSET
AN2 NC
IFPD_RSET
GM107 GK107/GK208
IFPC_AUX_I2CW_SCL AG3
IFPC_AUX_I2CW_SDA_N AG2
IFPC_L0 AK1
IFPC_L0_N AJ1
IFPC_L1 AJ3
IFPC_L1_N AJ2
IFPC_L2 AH3
IFPC_L2_N AH4
IFPC_L3 AG5
IFPC_L3_N AG4
IFPD_AUX_I2CX_SCL AK3
IFPD_AUX_I2CX_SDA_N AK2
IFPD_L0 AM1
IFPD_L0_N AM2
IFPD_L1 AM3
IFPD_L1_N AM4
IFPD_L2 AL3
IFPD_L2_N AL4
IFPD_L3 AK4
IFPD_L3_N AK5

[IFPE/F_DP]
AB8 IFPEF_PLLVDD
AC7 IFPE_IOVDD
AC8 IFPF_IOVDD
AD6 IFPEF_RSET
IFPE_AUX_I2CY_SCL AB3
IFPE_AUX_I2CY_SDA_N AB4
IFPE_L0 AD2
IFPE_L0_N AD3
IFPE_L1 AD1
IFPE_L1_N AC1
IFPE_L2 AC2
IFPE_L2_N AC3
IFPE_L3 AC4
IFPE_L3_N AC5
IFPF_AUX_I2CZ_SCL AF3
IFPF_AUX_I2CZ_SDA_N AF2
IFPF_L0 AE3
IFPF_L0_N AE4
IFPF_L1 AF4
IFPF_L1_N AF5
IFPF_L2 AD4
IFPF_L2_N AD5
IFPF_L3 AG1
IFPF_L3_N AF1

[DACA/B_CRT]
AG10 DACA_VDD
AP9 DACA_VREF
AP8 DACA_RSET
DACA_RED AK9
DACA_GREEN AL10
DACA_BLUE AL9
DACA_HSYNC AM9
DACA_VSYNC AN9
I2CA_SCL R4 I2CA_SCL 1.8K/F_4 R309
I2CA_SDA R5 I2CA_SDA 1.8K/F_4 R65

[XTAL IN]
XTAL_IN H3 XTAL27_IN
XTAL_OUT H2 XTAL27_OUT
XTAL_OUTBUFF J4 XTAL_OUTBUFF RP6 2 4 1 3 10KX2
XTAL_SSIN H1 XTAL_SSIN

PLACE CLOSE TO GPU
PLACE CLOSE TO BALLS

+1.05V_GFX L3 HCB1005KF-330T30 NV_PLLVDD AD8 PLLVDD
C330 22U/6.3V_6
C338 0.1U/16V/X7R_4
PLLVDD : 200mA
PLLVDD AE8 SP_PLLVDD
C283 Close to AE8
C284 Close to AD7
+1.05V_GFX L2 HCB1005KF-181T15 AD7 VID_PLLVDD
C629 10U/6.3V_6
C631 47U/6.3V_8
C333 0.1U/16V/X7R_4
C337 0.1U/16V/X7R_4

R85 1 *0_4_NC 2
+3.3V_RUN
+3V_GFX
+3V_AON
U4 MC74VHC1G08DFT2G
3V3_MAIN_PWRGD 50,52
R86 10K/F_4
C393 0.1U/16V/X7R_4

XTAL27_IN
XTAL27_OUT R456 560_4 XTAL27_OUT_R
Y2 27MHZ +-10PPM
C649 22P/50V_4
C641 22P/50V_4

Reserve
+3V_AON
XTAL_OUTBUFF R302 *10K_4_NC

PS: DG-07158-001 V04 PG58
PLLVDD/SP_PLLVDD/VID_PLLVDD :
Trace routing for the above power rails to the GPU BGA must 12mil to 16mil wide

Quanta Computer Inc.
PROJECT : AM9A

Size	Document Number	Rev
	N16P-GX - 3/5 (Display)	A0
Date: Wednesday, August 19, 2015	Sheet 19 of 57	

4.99K/F_4: CS24992FB26 RES CHIP 4.99K 1/16W +1%(0402)
10K/F_4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)
15K/F_4: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)
24.9K/F_4: CS32492FB16 RES CHIP 24.9K 1/16W +-1%(0402)
30.1K/F_4: CS33012FB18 RES CHIP 30.1K 1/16W +-1%(0402)
34.8K/F_4: CS33482FB22 RES CHIP 34.8K 1/16W +-1% (0402)
45.3K/F_4: CS34532FB18 RES CHIP 45.3K 1/16W +-1% (0402)

Logical Strap Bit Mapping

STRAP DECODE ACCORDING TO TERMINATION RESISTANCE/VOLTAGE

TERMINATION RESISTANCE	TERMINATION VOLTAGE 3V3 [3:0]		GND [3:0]	
5K	1000	8	0000	0
10K	1001	9	0001	1
15K	1010	A	0010	2
20K	1011	B	0011	3
25K	1100	C	0100	4
30K	1101	D	0101	5
35K	1110	E	0110	6
45K	1111	F	0111	7

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			

U11E
N16P-GX

[MIOA]

[MIOB]

STRAP0
DG : STUFF 49.9KΩ PU TO 3.3V_AON

R79 49.9K/F_4 | R80 *4.99K/F_4_NC | R331 *4.99K/F_4_NC | R334 *45.3K/F_4_NC | R338 *10K/F_4_NC
R77 *4.99K/F_4_NC | R78 *4.99K/F_4_NC | R332 *4.99K/F_4_NC | R335 *4.99K/F_4_NC | R339 *45.3K/F_4_NC

STRAP0 STRAP1 STRAP2 STRAP3 STRAP4

Default: Sam 4Gb VRAM

Vendor	Q : P/N	Mfr. P/N	ROM_SI	
Hynix (1.35V)	AKG5PWUTW14	H5GC4H24AJR-R0C	0110	35K PD
Micron (1.35V)	AKG5PW0TL01	EDW4032BABG-60-F	0100	24.9K PD
Samsung (1.35V)	AKG5PGDT500	K4G41325FC-HC03	0011	20K PD

N16P-GX device ID= 0x139b		
Netname	N16P-GX	
ROM_SCLK	4.99K PD	0000
ROM_SO	4.99K PD	0000
STRAP0	49.9K PU	

Reserve PU/PD for Debug

+3V_AON
JTAG_TMS R290 *10K_4_NC
JTAG_TDI R289 *10K_4_NC
JTAG_TCK R294 *10K_4_NC
JTAG_TCK need PD 270 Ω to GND
JTAG_TRST# R291 10K_4

+3V_GFX
R327 *4.99K/F_4_NC | R68 *4.99K/F_4_NC | R76 *10K/F_4_NC
ROM_SI
ROM_SO
ROM_SCLK
R328 20K/F_4 | R69 4.99K/F_4 | R74 4.99K/F_4

GFx SMBus Isolation

+3V_AON
RP1 2.2KX2
Q10 2N7002KDW
+3V_GFX
GFX_SCL → SMBCLK3 26,33
GFX_SDA → SMBDAT3 26,33

[MISC_GPIO/I2C/JTAG/THER]

JTAG_TCK AM10
JTAG_TMS AP11
JTAG_TDI AM11
JTAG_TDO AP12
JTAG_TRST# AN11
TP75

1.8K/F_4 R67 I2CB_SCL R7
1.8K/F_4 R66 I2CB_SDA R6
1.8K/F_4 R308 I2CC_SCL R2
1.8K/F_4 R307 I2CC_SDA R3
GFX_SCL T4
GFX_SDA T3
K4 THERMDN
K3 THERMDP

GK107/GK208/GF117: NC

GPIO0 P6 → TP17 → GC6_FB_EN 10
GPIO1 M3 → TP14
GPIO2 L6 → TP16
GPIO3 P5 → TP12
GPIO4 P7 → +3V_MAIN_EN
GPIO5 L7 → +3V_MAIN_EN 50
GPIO6 M7 → GPU_EVENT# → GPU_EVENT# 10
GPIO7 N8 → TP13
GPIO8 L3 → SYS_PEX_RST_MON# 17
GPIO9 M2 ALERT
GPIO10 L1 MEM_VREF_CTL → MEM_VREF_CTL 22,23,24,25
GPIO11 M5 → DGPU_PWM_VID 50
GPIO12 N3 VGA_PWR_LEVEL → VGA_PWR_LEVEL 26
GPIO13 M4 DGPU_PSI → DGPU_PSI 50
GPIO14 N4
GPIO15 P2
GPIO16 R8
GPIO17 M6
GPIO18 R1
GPIO19 P3
GPIO20 P4
GPIO21 P1 → GPU_PEX_RST_HOLD# 17

+3V_AON
10KX2 RP7
VGA_OVT# 1
ALERT 3
2 4
GPU_EVENT# R323 10K_4
VGA_PWR_LEVEL R343 100K_4
+3V_MAIN_EN R313 10K_4
SYS_PEX_RST_MON# R319 10K_4
GPU_PEX_RST_HOLD# R310 10K_4
DGPU_PSI R316 10K_4
1.05V_GFX_PWRGD R454 10K_4

0430 add

1201 DG-07158--001 V05 PG182
MEM_VREF_CTL R311 100K_4
GC6_FB_EN R353 10K_4

[MISC2_ROM]

STRAP0 J2
STRAP1 J7
STRAP2 J6
STRAP3 J5
STRAP4 J3
MULTISTRAP_REF_GND J1
R305 40.2K/F_4

ROM_SCLK H4 → ROM_SCLK
ROM_CS_N H6
ROM_SI H5 → ROM_SI
ROM_SO H7 → ROM_SO
BUFRST_N L2 → GPU_BUFRST R312 *10K_4_NC
VGA_OVT# M1

GK107/GF117: GPIO8
GM107/GM108/GK208: OVERT

D14
GC6_FB_EN 1
52 1.05V_GFX_PWRGD
BAT54CW
3
1.35V_GFX_EN
1.35V_GFX_EN 51
R351 100K_4

GPIO	GM107/GM108	GK208/GK107
GPIO 0	GC6_FB_EN	FB_CLAMP_MON
GPIO 1	MEM_VDD_CTL	MEM_VDD_CTL
GPIO 2	LCD_BL_PWM	LCD_BL_PWM
GPIO 3	LCD_PWR_EN	LCD_PWR_EN
GPIO 4	LCD_BL_EN	LCD_BL_EN
GPIO 5	GC6_PWR_EN	DEBUG_SRVC
GPIO 6	GPU_EVENT*	FBCLAMP_TGL_REQ
GPIO 7	3D STEREO/DEBUG_SRVC	3D STEREO
GPIO 8	SYS_PEX_RST_MON*	OVERT*
GPIO 9	THERM_ALERT*/ERR_CORR	THERM_ALERT*/ERR_CORR
GPIO 10	MEM_VREF_CTL	MEM_VREF_CTL
GPIO 11	NVVDD PWM_VID	NVVDD PWM_VID
GPIO 12	AC DETECT	AC DETECT
GPIO 13	NVVDD PSI	NVVDD PSI
GPIO 14	IFPA HDP(not used for GM108)	IFA HDP/FBCLAMP_TGL_REQ
GPIO 15	IFPC HDP(not used for GM108)	IFPC HDP
GPIO 16	FRAME LOCK	FRAME LOCK
GPIO 17	IFPD HDP(not used for GM108)	IFPD HDP
GPIO 18	IFPEF HDP(not used for GM108)	IFPEF HDP(not used for GK208)
GPIO 19	IFPB HDP(not used for GM108)	IFPB HDP
GPIO 20	GC5_MODE	N/A
GPIO 21	GPU_PEX_RST_HOLD*	N/A

Quanta Computer Inc.
PROJECT : AM9A

Size	Document Number	Rev
	N16P-GX - 4/5 (MISC)	A0

Date: Wednesday, August 19, 2015 Sheet 20 of 57

VDD/XVDD : 43A

+VGACORE

U11F
N16P-GX

[GPU VDD]

AA12	VDD_001	XVDD_001	U1
AA14	VDD_002	XVDD_002	U2
AA16	VDD_003	XVDD_003	U3
AA19	VDD_004	XVDD_004	U4
AA21	VDD_005	XVDD_005	U5
AA23	VDD_006	XVDD_006	U6
AB13	VDD_007	XVDD_007	U7
AB15	VDD_008	XVDD_008	U8
AB17	VDD_009	XVDD_009	V1
AB18	VDD_010	XVDD_010	V2
AB20	VDD_011	XVDD_011	V3
AB22	VDD_012	XVDD_012	V4
AC12	VDD_013	XVDD_013	V5
AC14	VDD_014	XVDD_014	V6
AC16	VDD_015	XVDD_015	V7
AC19	VDD_016	XVDD_016	V8
AC21	VDD_017	XVDD_017	W2
AC23	VDD_018	XVDD_018	W3
M12	VDD_019	XVDD_019	W4
M14	VDD_020	XVDD_020	W5
M16	VDD_021	XVDD_021	W7
M19	VDD_022	XVDD_022	W8
M21	VDD_023	XVDD_026	Y4
M23	VDD_024	XVDD_027	Y5
N13	VDD_025	XVDD_028	Y6
N15	VDD_026	XVDD_029	Y7
N17	VDD_027	XVDD_030	Y8
N18	VDD_028		
N20	VDD_029		
N22	VDD_030		
P12	VDD_031		
P14	VDD_032		
P16	VDD_033		
P19	VDD_034		
P21	VDD_035		
P23	VDD_036		
R13	VDD_037		
R15	VDD_038		
R17	VDD_039		
R18	VDD_040		
R20	VDD_041		
R22	VDD_042		
T12	VDD_043		
T14	VDD_044		
T16	VDD_045		
T19	VDD_046		
T21	VDD_047		
T23	VDD_048		
U13	VDD_049		
U15	VDD_050		
U17	VDD_051		
U18	VDD_052		
U20	VDD_053		
U22	VDD_054		
V13	VDD_055		
V15	VDD_056		
V17	VDD_057		
V18	VDD_058		
V20	VDD_059		
V22	VDD_060		
W12	VDD_061		
W14	VDD_062		
W16	VDD_063		
W19	VDD_064		
W21	VDD_065		
W23	VDD_066		
Y13	VDD_067		
Y15	VDD_068		
Y18	VDD_069		
Y17	VDD_070		
Y20	VDD_071		
Y22	VDD_072		

+VGACORE

U11G
N16P-GX

[GPU GND]

A2	GND_1	GND_101	D2
AA17	GND_2	GND_102	D31
AA18	GND_3	GND_103	D33
AA20	GND_4	GND_104	E10
AA22	GND_5	GND_105	E22
AB12	GND_6	GND_106	E25
AB14	GND_7	GND_107	E5
AB16	GND_8	GND_108	E7
AB19	GND_9	GND_109	F28
AB2	GND_10	GND_110	F7
AB21	GND_11	GND_111	G10
A33	GND_12	GND_112	G13
AB23	GND_13	GND_113	G16
AB28	GND_14	GND_114	G19
AB30	GND_15	GND_115	G2
AB32	GND_16	GND_116	G22
AB5	GND_17	GND_117	G25
AB7	GND_18	GND_118	G28
AC13	GND_19	GND_119	G3
AC15	GND_20	GND_120	G30
AC17	GND_21	GND_121	G32
AC18	GND_22	GND_122	G33
AA13	GND_23	GND_123	G5
AC20	GND_24	GND_124	G7
AC22	GND_25	GND_125	K2
AE2	GND_26	GND_126	K28
AE28	GND_27	GND_127	K30
AE30	GND_28	GND_128	K32
AE32	GND_29	GND_129	K33
AE33	GND_30	GND_130	K5
AE5	GND_31	GND_131	K7
AE7	GND_32	GND_132	M13
AH10	GND_33	GND_133	M15
AA15	GND_34	GND_134	M17
AH13	GND_35	GND_135	M18
AH16	GND_36	GND_136	M20
AH19	GND_37	GND_137	M22
AH2	GND_38	GND_138	N12
AH22	GND_39	GND_139	N14
AH24	GND_40	GND_140	N16
AH28	GND_41	GND_141	N19
AH29	GND_42	GND_142	N2
AH30	GND_43	GND_143	N21
AH32	GND_44	GND_144	N23
AH33	GND_45	GND_145	N28
AH5	GND_46	GND_146	N30
AH7	GND_47	GND_147	N32
AJ7	GND_48	GND_148	N33
AK10	GND_49	GND_149	N5
AK7	GND_50	GND_150	N7
AL12	GND_51	GND_151	P13
AL14	GND_52	GND_152	P15
AL15	GND_53	GND_153	P17
AL17	GND_54	GND_154	P18
AL18	GND_55	GND_155	P20
AL2	GND_56	GND_156	P22
AL20	GND_57	GND_157	R12
AL21	GND_58	GND_158	R14
AL23	GND_59	GND_159	R16
AL24	GND_60	GND_160	R19
AL26	GND_61	GND_161	R21
AL28	GND_62	GND_162	R23
AL30	GND_63	GND_163	T13
AL32	GND_64	GND_164	T15
AL33	GND_65	GND_165	T17
AL5	GND_66	GND_166	T18
AM13	GND_67	GND_167	T2
AM16	GND_68	GND_168	T20
AM19	GND_69	GND_169	T22
AM22	GND_70	GND_170	AG11
AM25	GND_71	GND_171	T28
AN1	GND_72	GND_172	T32
AN10	GND_73	GND_173	T5
AN13	GND_74	GND_174	T7
AN16	GND_75	GND_175	U12
AN19	GND_76	GND_176	U14
AN22	GND_77	GND_177	U16
AN25	GND_78	GND_178	U19
AN30	GND_79	GND_179	U21
AN34	GND_80	GND_180	U23
AN4	GND_81	GND_181	V12
AN7	GND_82	GND_182	V14
AP2	GND_83	GND_183	V16
AP33	GND_84	GND_184	V19
B1	GND_85	GND_185	V21
B10	GND_86	GND_186	V23
B22	GND_87	GND_187	W13
B25	GND_88	GND_188	W15
B28	GND_89	GND_189	W17
B31	GND_90	GND_190	W18
B34	GND_91	GND_191	W20
B4	GND_92	GND_192	W22
B7	GND_93	GND_193	W28
C10	GND_94	GND_194	Y12
C13	GND_95	GND_195	Y14
C19	GND_96	GND_196	Y16
C22	GND_97	GND_197	Y19
C25	GND_98	GND_198	Y21
C28	GND_99	GND_199	Y23
C7	GND_100	GND_200	AH11
		GND_OPT_1	C16
		GND_OPT_2	W32

+VGACORE

PLACE UNDER GPU

C303	1U/6.3V_4
C230	1U/6.3V_4
C315	1U/6.3V_4
C304	1U/6.3V_4
C243	1U/6.3V_4
C201	1U/6.3V_4
C229	1U/6.3V_4
C308	1U/6.3V_4
C311	4.7U/6.3V/X6S_6
C378	4.7U/6.3V/X6S_6
C309	4.7U/6.3V/X6S_6
C379	4.7U/6.3V/X6S_6
C209	4.7U/6.3V/X6S_6
C312	4.7U/6.3V/X6S_6
C210	4.7U/6.3V/X6S_6
C207	4.7U/6.3V/X6S_6
C639	4.7U/6.3V/X6S_6
C208	4.7U/6.3V/X6S_6
C224	4.7U/6.3V/X6S_6
C314	4.7U/6.3V/X6S_6
C222	4.7U/6.3V/X6S_6
C321	4.7U/6.3V/X6S_6
C240	4.7U/6.3V/X6S_6

PLACE NEAR GPU

C376 2	1 22U/6.3V_8
C377 2	1 22U/6.3V_8
C373 2	1 22U/6.3V_8
C374 2	1 22U/6.3V_8
C372 2	1 22U/6.3V_8
C375 2	1 22U/6.3V_8
C644 2	1 22U/6.3V_6
C658	4.7U/6.3V/X6S_6
C305	4.7U/6.3V/X6S_6
C204	4.7U/6.3V/X6S_6
C214	4.7U/6.3V/X6S_6
C329	4.7U/6.3V/X6S_6

PC60 1 2 330U/2V/E9_7343

Quanta Computer Inc.

PROJECT : AM9A

Size	Document Number	Rev
	N16P-GX - 5/5 (Power)	A0

Date: Wednesday, August 19, 2015 Sheet 21 of 57

CHANNEL A: 2G/4G GDDR5

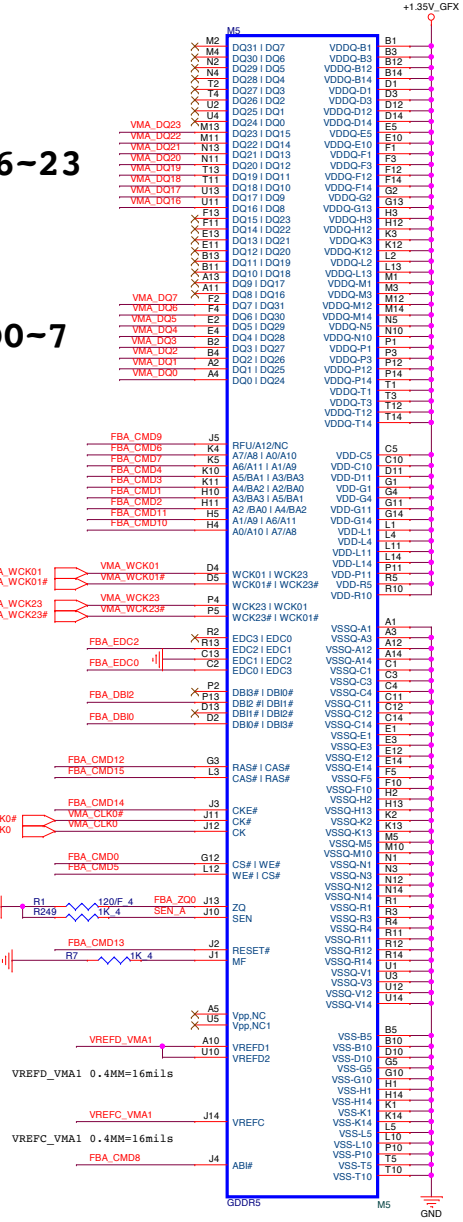
18,23 VMA_DQ[63:0] — VMA_DQ[63:0]
18,23 FBA_CMD[31:0] — FBA_CMD[31:0]
18,23 FBA_DBI[7:0] — FBA_DBI[7:0]
18,23 FBA_EDC[7:0] — FBA_EDC[7:0]

HYU 256Mx16, H5GC4H24AJR-R0C QBC PN : AKG5PWUTW14
MIC 256Mx16, EDW4032BABG-60-F QBC PN : AKG5PW0TL01
SAM 256Mx16, K4G41325FC-HC03 QBC PN : AKG5PGDT500

Channel 0 <0-7,16-23> MF=0 Non-mirrored

QD16~23

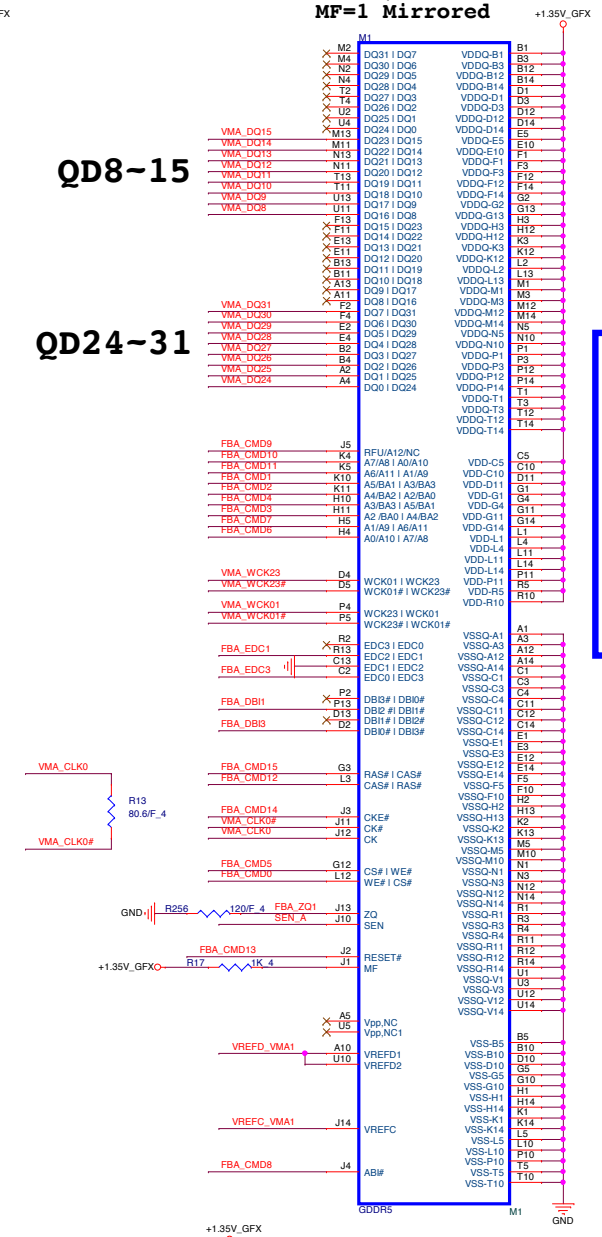
QD0~7



Channel 0 <8-15,24-31> MF=1 Mirrored

QD8~15

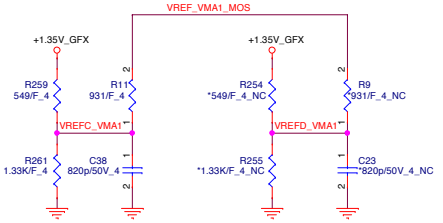
QD24~31



FBA_CMD14 R253 10K_4 +1.35V_GFX
FBA_CMD13 R8 10K_4

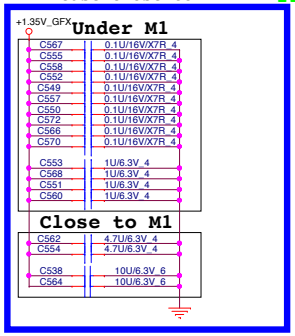
CKE* is strap pin to set ODT value of memory chip

RST PD place @ the end of daisy-chain.



DG-07158-001 V05 PG49

Please close to M1 1127



Please close to M2 1127

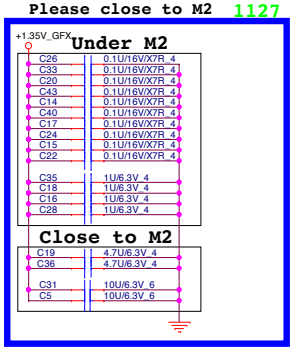


Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*

Quanta Computer Inc.
PROJECT : AM9A

Size	Document Number	Rev
	N16P-GX_GDDR5 - A1	A0

Date: Wednesday, August 19, 2015 Sheet 22 of 57

CHANNEL A: 2G/4G GDDR5

18,22 VMA_DQ[63:0] — VMA_DQ[63:0]
18,22 FBA_CMD[31:0] — FBA_CMD[31:0]
18,22 FBA_DBI[7:0] — FBA_DBI[7:0]
18,22 FBA_EDC[7:0] — FBA_EDC[7:0]

Channel 1 <32-39,48-55> MF=0 Non-mirrored

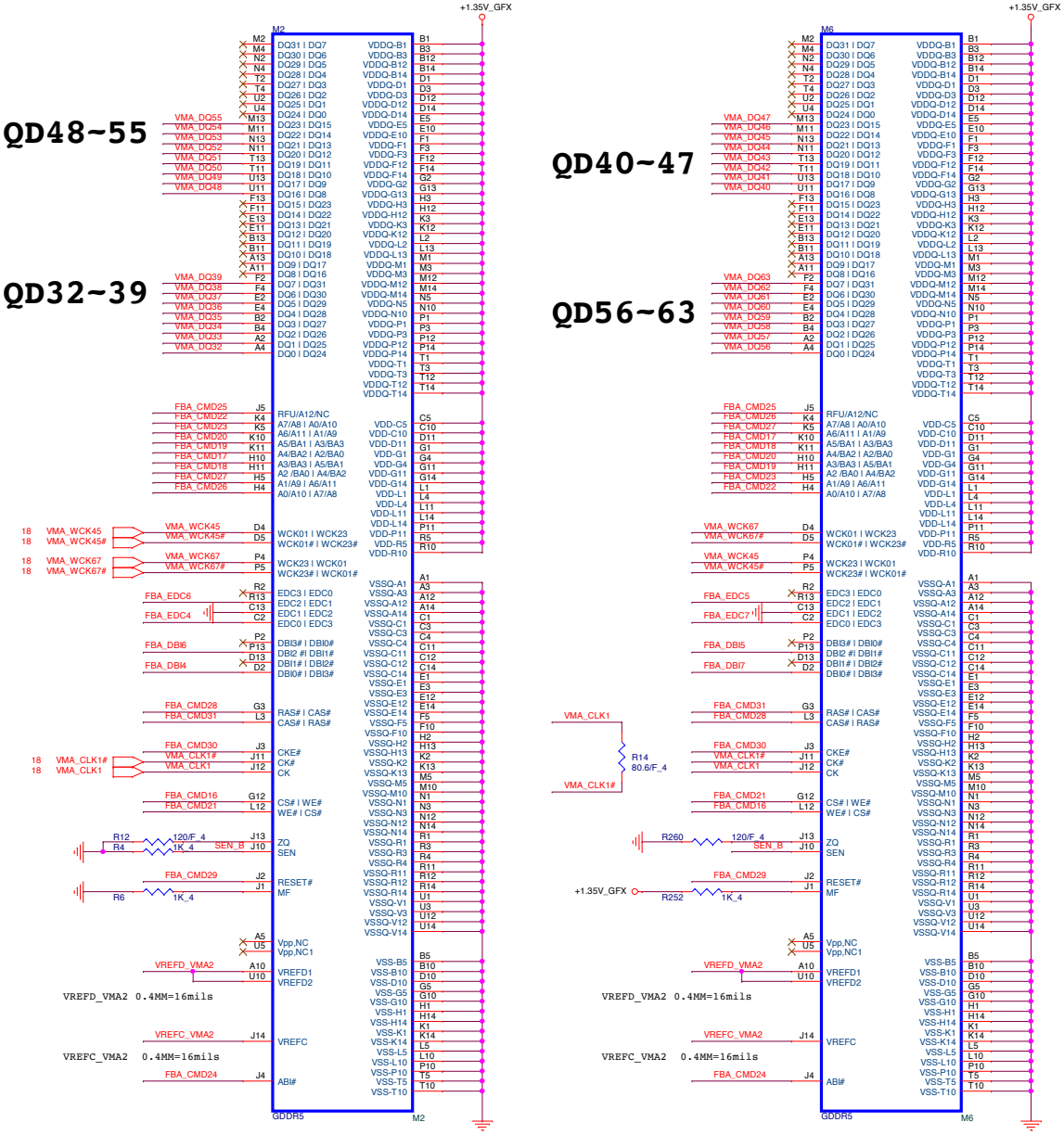
Channel 1 <40-47,56-63> MF=1 Mirrored

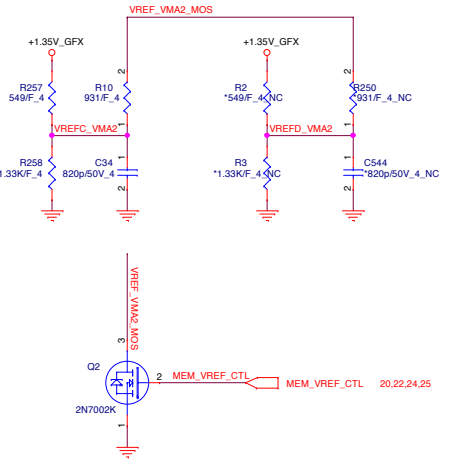
QD48~55

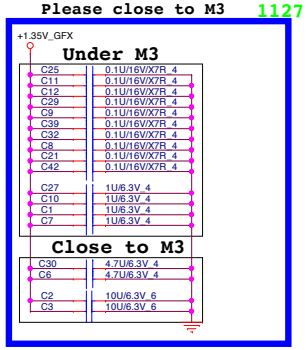
QD32~39

QD40~47

QD56~63







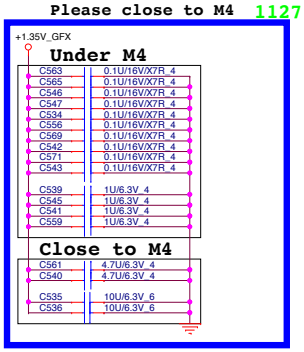
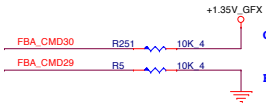


Table 4 Vendor ID to DQ mapping

Bit	7	6	5	4	3	2	1	0
MF=0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
MF=1	DQ31	DQ30	DQ29	DQ28	DQ27	DQ26	DQ25	DQ24
Feature	Revision Identification				Manufacturers Vendor Code			

Bit	15	14	13	12	11	10	9	8
MF=0	DQ23	DQ22	DQ21	DQ20	DQ19	DQ18	DQ17	DQ16
MF=1	DQ15	DQ14	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8
Feature	RFU		Density		FIFO Depth		Density	



CKE* is strap pin to set ODT value of memory chip

RST PD place @ the end of daisy-chain.

Quanta Computer Inc.
PROJECT : AM9A

Size	Document Number	Rev
	N16P-GX_ GDDR5 - A2	A0

Date: Wednesday, August 19, 2015 Sheet 23 of 57

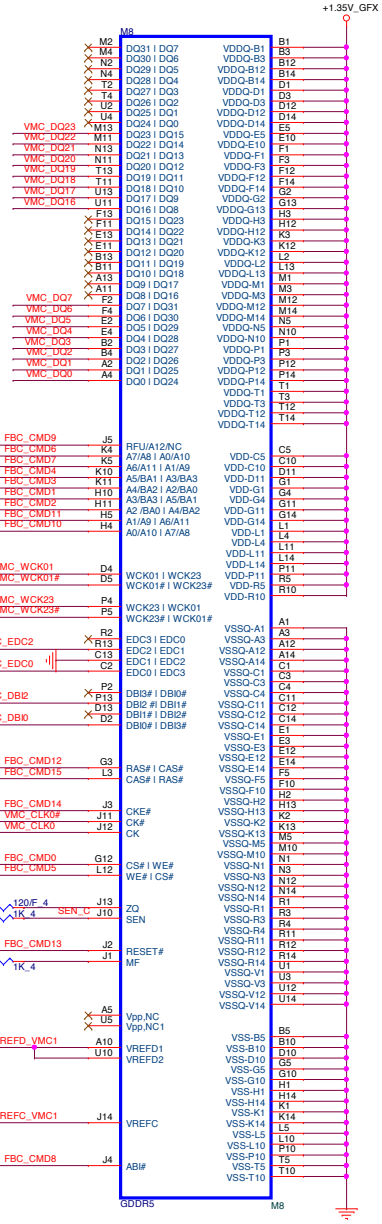
CHANNEL B: 2G/4G GDDR5

18,25 VMC_DQ[63:0] — VMC_DQ[63:0]
18,25 FBC_CMD[31:0] — FBC_CMD[31:0]
18,25 FBC_DBI[7:0] — FBC_DBI[7:0]
18,25 FBC_EDC[7:0] — FBC_EDC[7:0]

Channel 0 <0-7,16-23>
MF=0 Non-mirrored

QD16~23

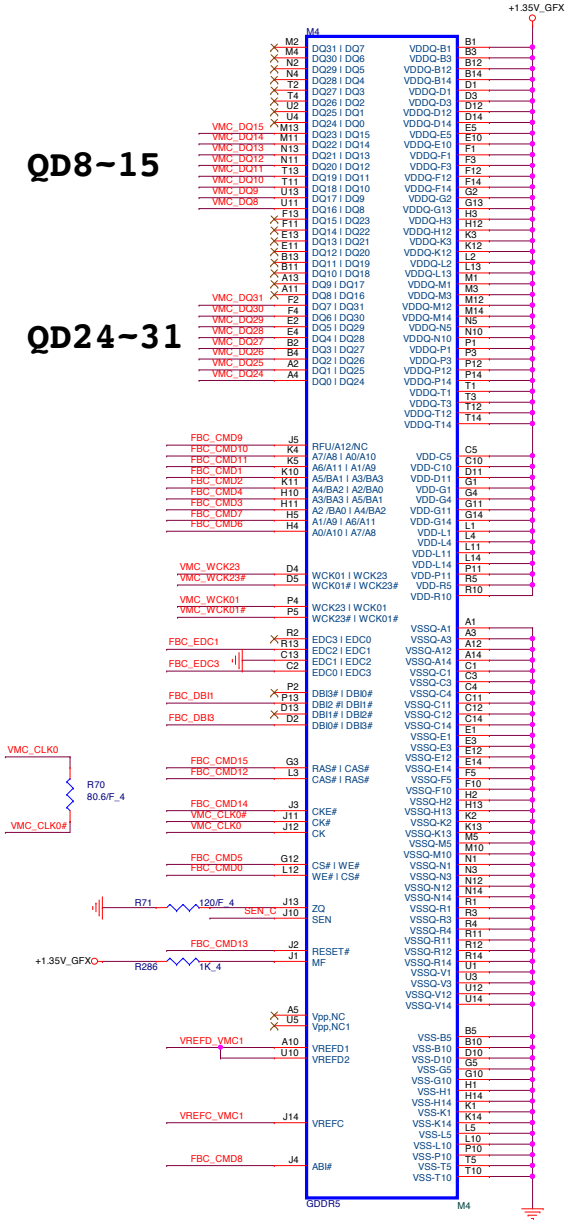
QD0~7

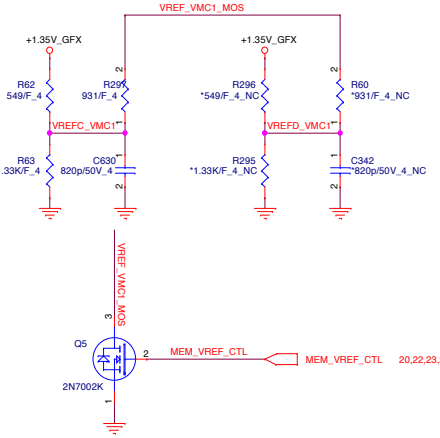


Channel 0 <8-15,24-31>
MF=1 Mirrored

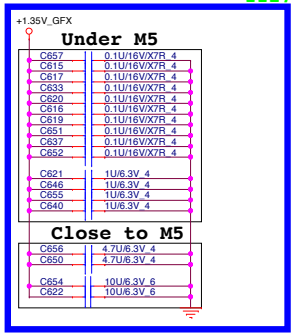
QD8~15

QD24~31

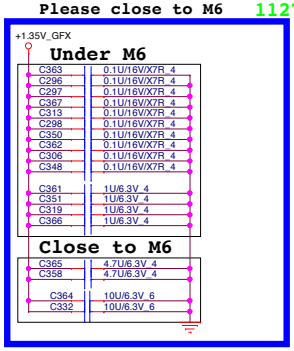




Please close to M5 1127



Please close to M6 1127



+1.35V_GFX
FBC_CMD14 R56 10K_4 — CKE* is strap pin to set ODT value of memory chip
FBC_CMD13 R292 10K_4 — RST PD place @ the end of daisy-chain.

Quanta Computer Inc.		
PROJECT : AM9A		
Size	Document Number: N16P-GX_GDDR5 - B1	Rev: A0
Date: Wednesday, August 19, 2015	Sheet 24 of 57	

CHANNEL B: 2G/4G GDDR5

18,24 VMC_DQ[63:0] — VMC_DQ[63:0]
18,24 FBC_CMD[31:0] — FBC_CMD[31:0]
18,24 FBC_DBI[7:0] — FBC_DBI[7:0]
18,24 FBC_EDC[7:0] — FBC_EDC[7:0]

Channel 1 <32-39,48-55>
MF=0 Non-mirrored

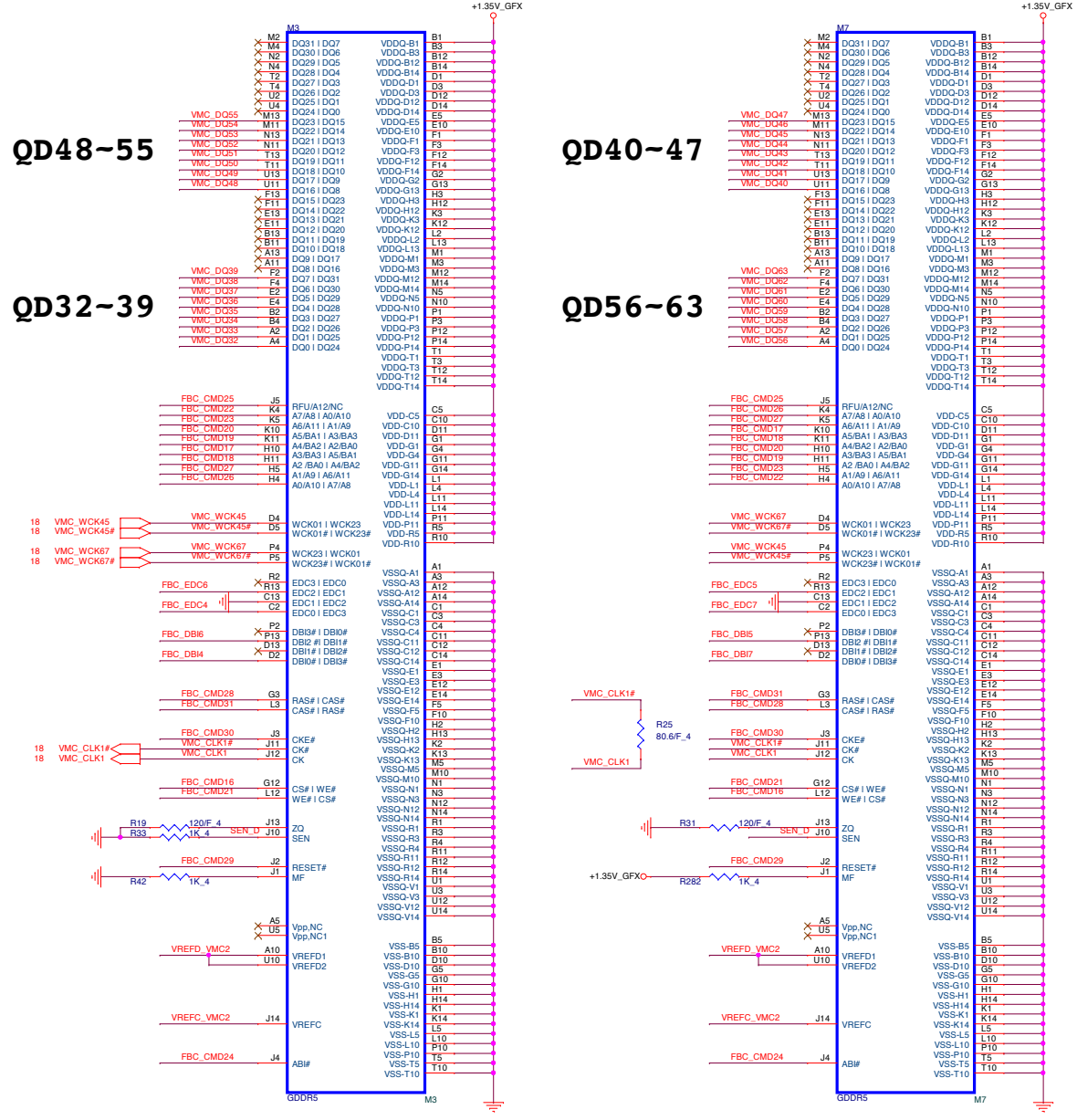
Channel 1 <40-47,56-63>
MF=1 Mirrored

QD48~55

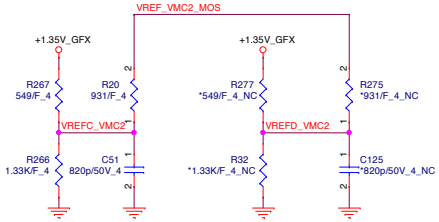
QD32~39

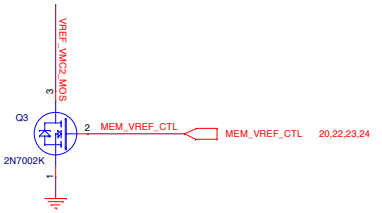
QD40~47

QD56~63

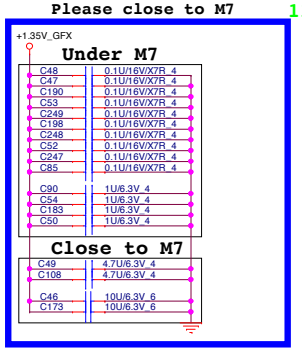


+1.35V_GFX
FBC_CMD30 R41 10K_4 — CKE* is strap pin to set ODT value of memory chip
FBC_CMD29 R284 10K_4 — RST PD place @ the end of daisy-chain.

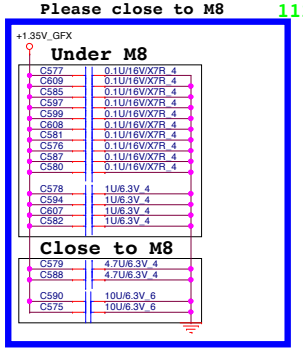




Please close to M7 1127



Please close to M8 1127



Quanta Computer Inc.
PROJECT : AM9A

Size	Document Number	Rev
	N16P-GX_GDDR5 - B2	A0

Date: Wednesday, August 19, 2015 Sheet 25 of 57

PECI

PECI:REC=33 ohms PDG-P215,
CRB P153 is 33ohms.
#546884 PDG V1.0 P615=43 ohm to EC

Place these caps close to ITE8528.

IT8528

U8
IT8528

3/17 CHANGE to EC ref AM8

3/2 modify

Thermal , GPU

Charge ,BAT
PCH

Board ID Straps

7/11 change Board ID

100K/F_4: CS41002FB28
45.3K/F_4: CS34532FB18
24.3K/F_4: CS32432FB19
12K/F_4 : CS31202FB15
6.49K/F_4: CS26492FB23
1.65K/F_4: CS21652FB29

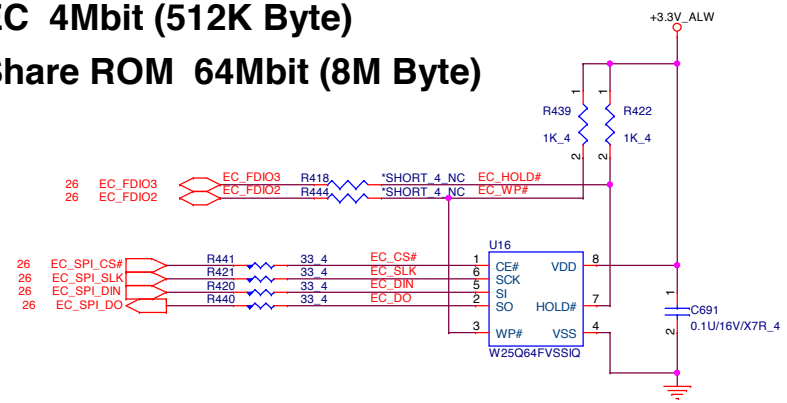
BID1		
000	0.5V PU 100K	EVT (X00)
001	1.0V PU 45.3K	DVT1 (X01)
010	1.5V PU 24.3K	DVT2 (X02)
100	2.0V PU 12K	PILOT (AOO)
101	2.5V PU 6.49K	
110	3.0V PU 1.65K	
111	0V NO PU	

It is necessary to connect this pin to the ground if "Crystal-Free" feature is activated and GPJ6 is not configured as GPI/GPO.

Quanta Computer Inc.
PROJECT : AM9A

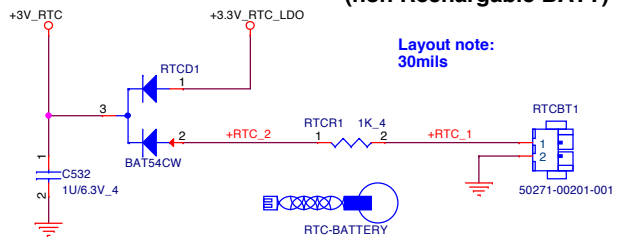
Size	Document Number	Rev
	SIO (ITE8528H)	A0
Date: Wednesday, August 19, 2015	Sheet 26 of 57	

For EC 4Mbit (512K Byte)
For Share ROM 64Mbit (8M Byte)



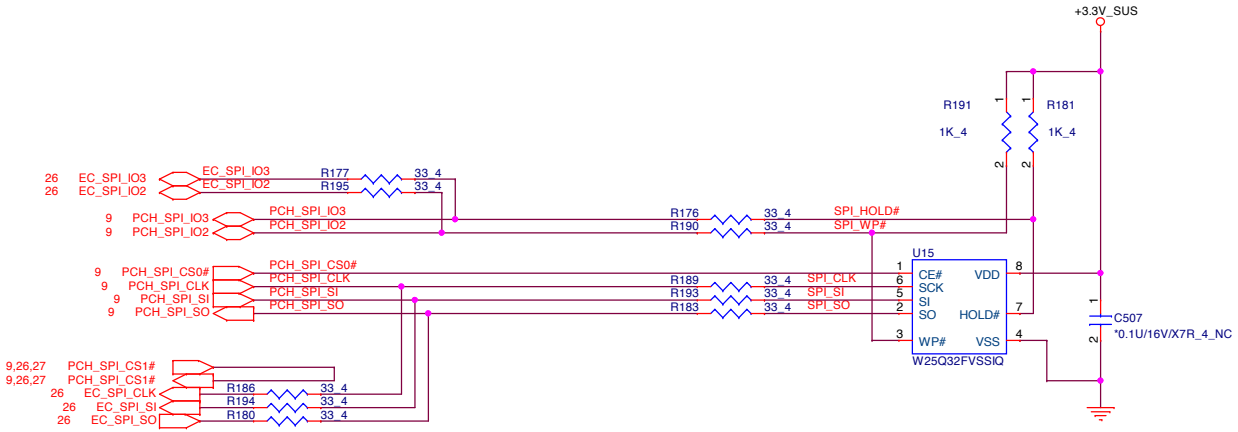
RTC BATTERY

(non Rechargable BATT)



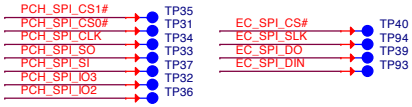
Follow JWA battery QPN

For PCH ME 32Mbit (4M Byte)

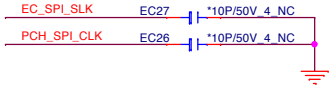


EDS #546884 P330
Use one 33- series-resistor per device if using two SPI devices and place it close to the devices.
15- series-resistor required if a single device is used.

TP for ICT flash BIOS process



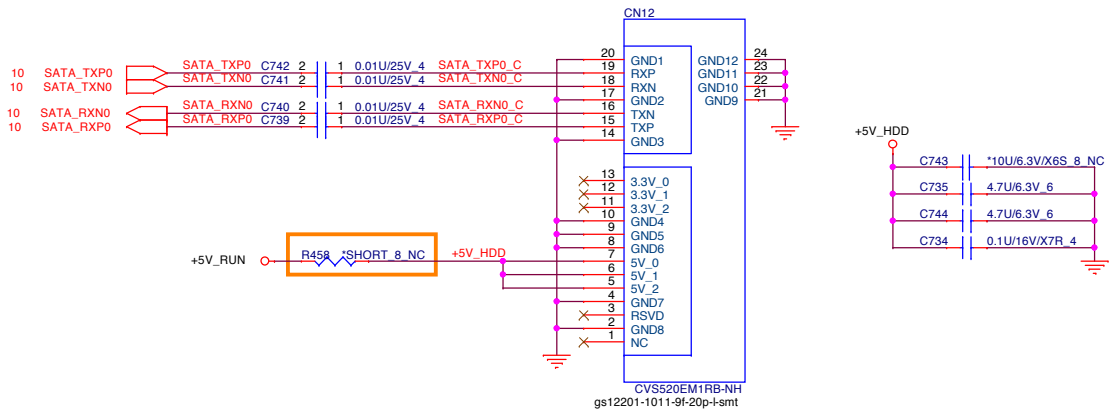
EMI



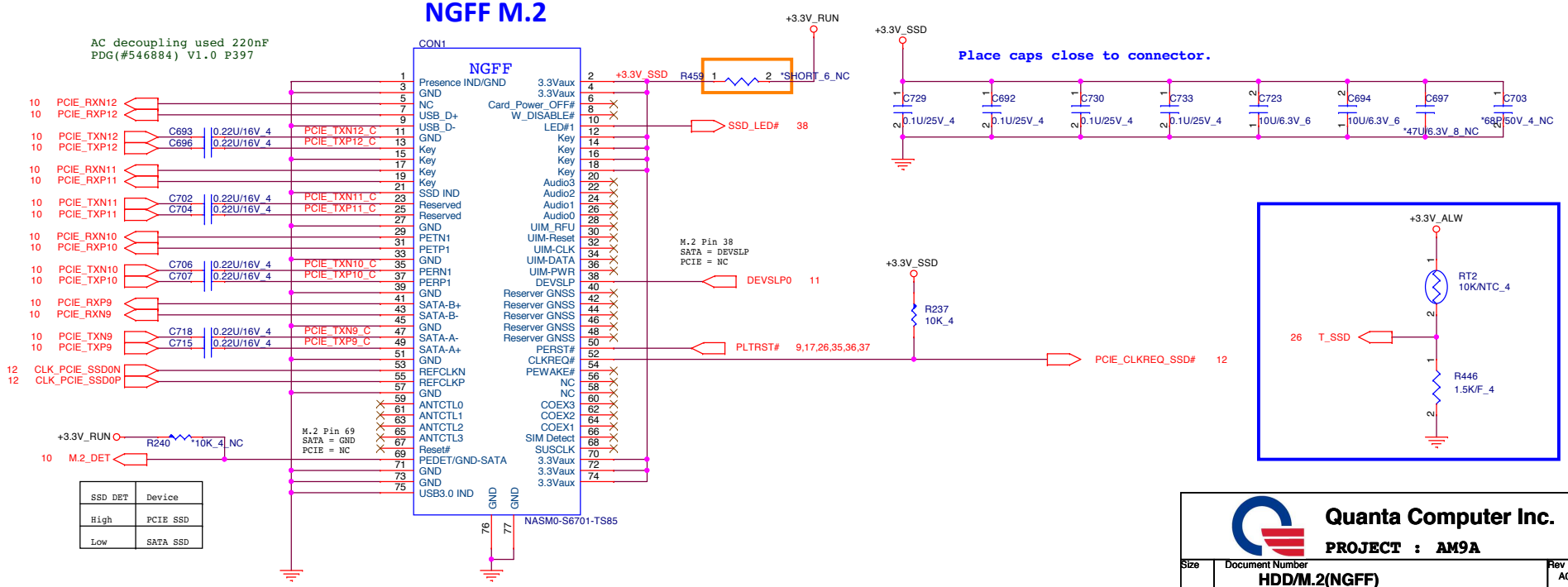
Quanta Computer Inc.		
PROJECT : AM9A		
Size	Document Number: FLASH / RTC	Rev: A0
Date: Wednesday, August 19, 2015	Sheet 27 of 57	

SATA HDD Connector

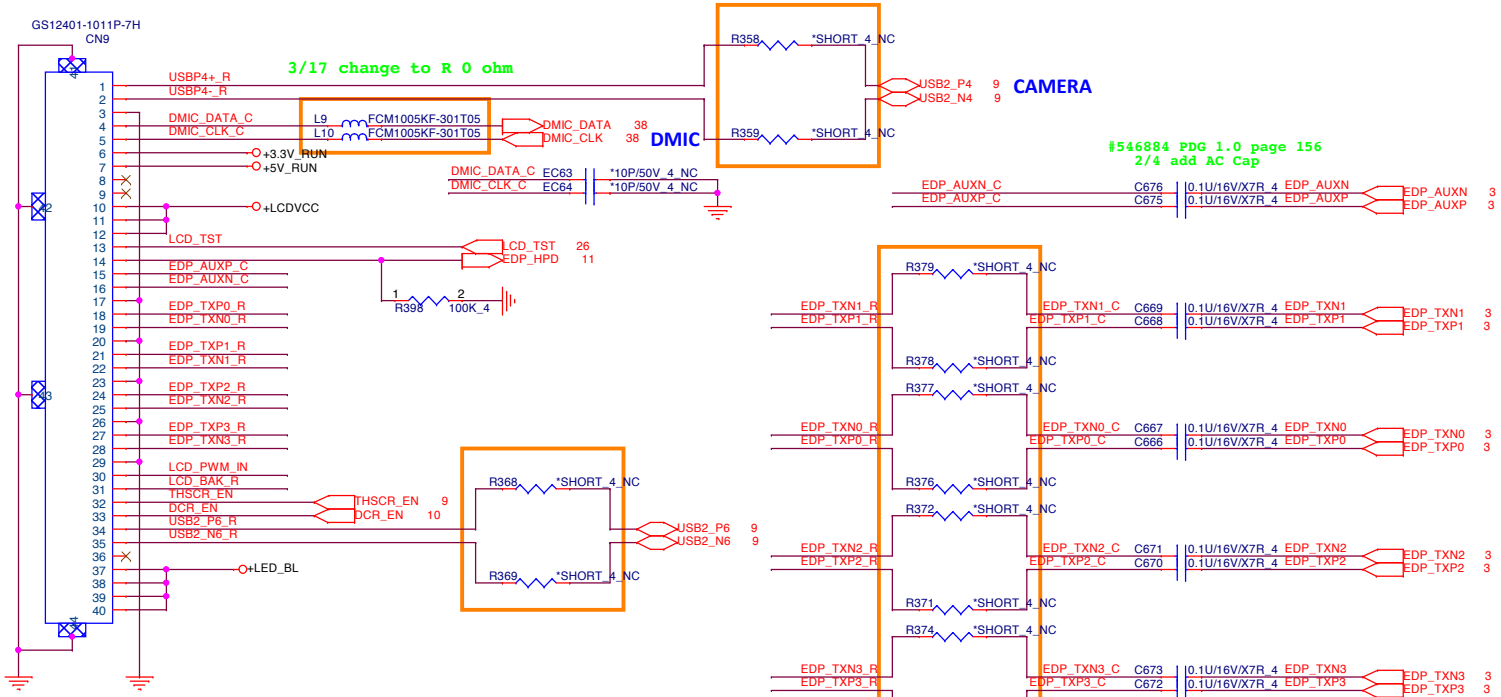
DG: Place TX cap close to connector



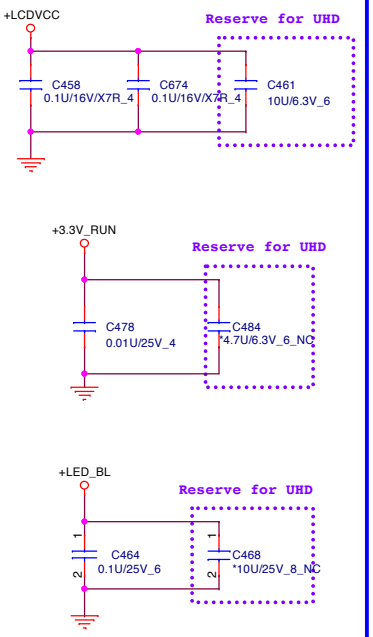
NGFF M.2



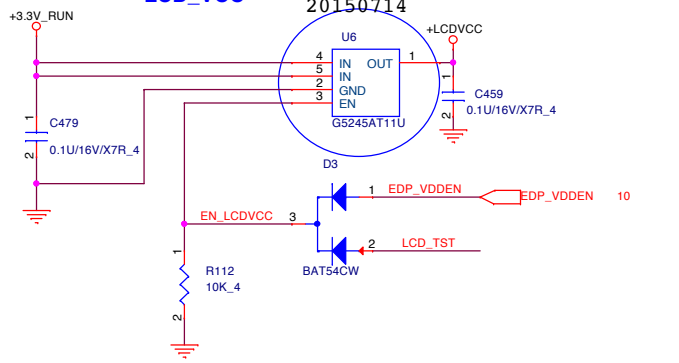
Quanta Computer Inc.			
PROJECT : AM9A			
Size	Document Number		Rev
	HDD/M.2(NGFF)		A0
Date:	Wednesday, August 19, 2015	Sheet 28 of 57	



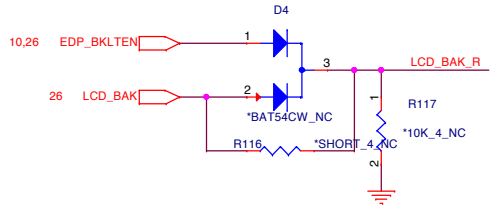
Close to CN4



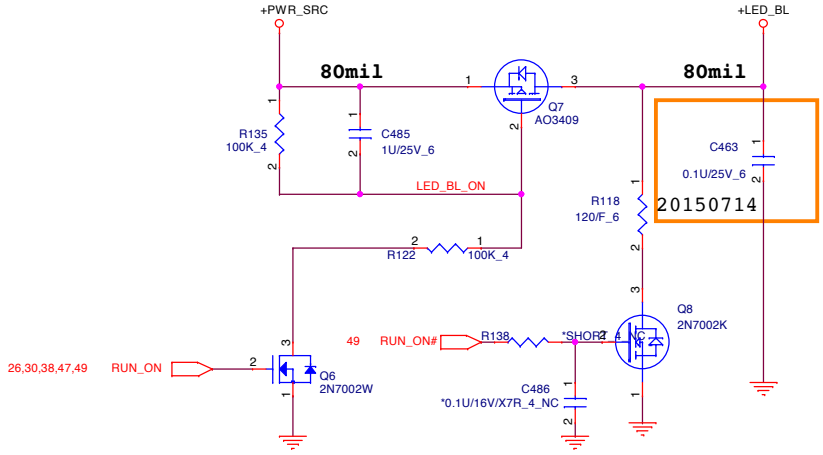
LCD_VCC



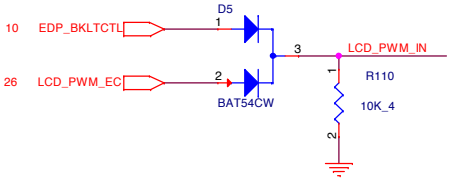
BAK_EN



Brightness Power

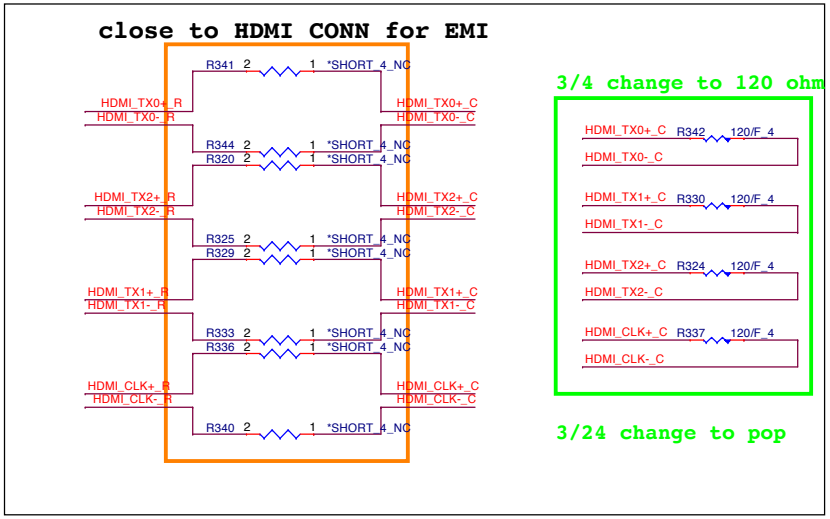


Brightness Control



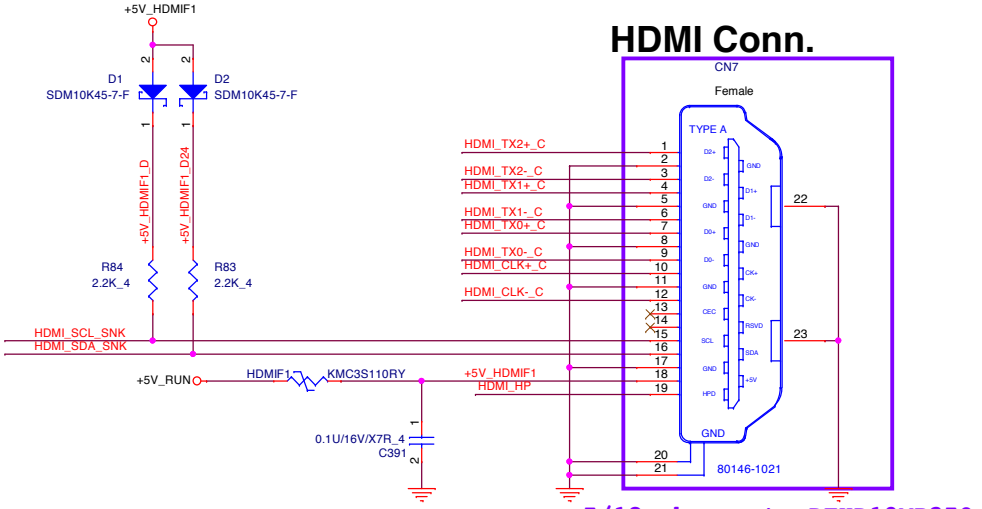
Quanta Computer Inc.
PROJECT : AM9A

Size	Document Number	Rev
	EDP/CCD	A0
Date: Wednesday, August 19, 2015	Sheet 29 of 57	



3/4 change to 120 ohm

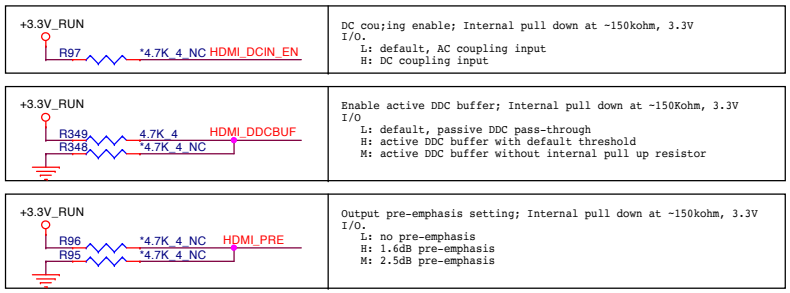
3/24 change to pop

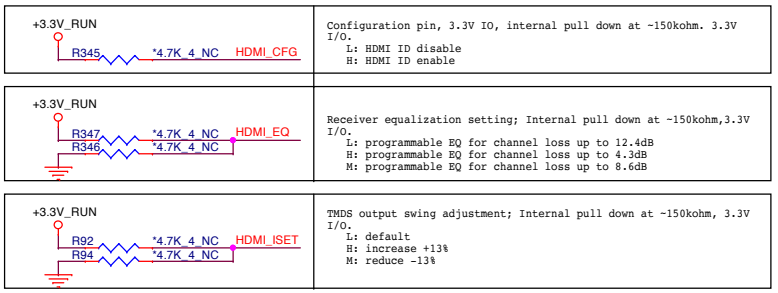


HDMI Conn.

5/18 change to DFHD19MR250

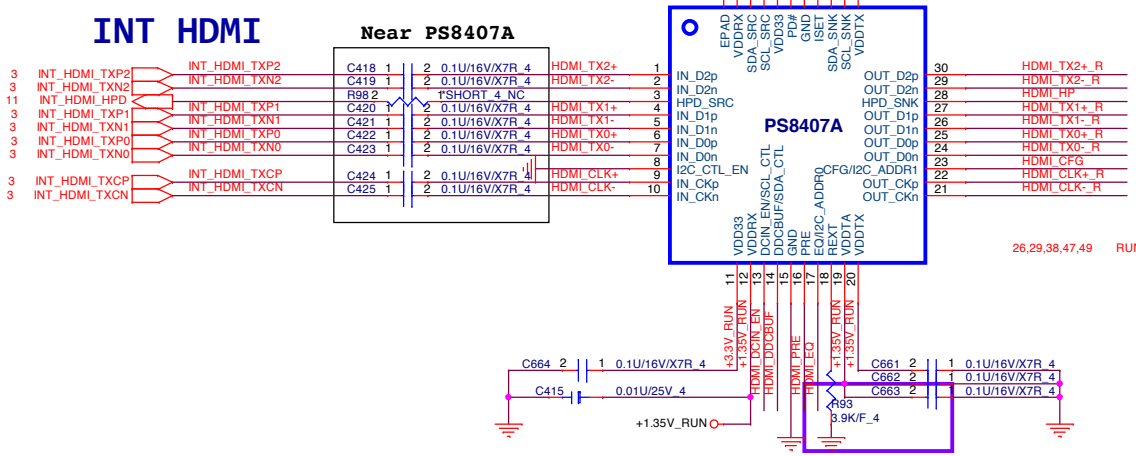
HDMI HPD :
1. PS8407A internal PD 150kohm
2. PS8407A has implement level shifter





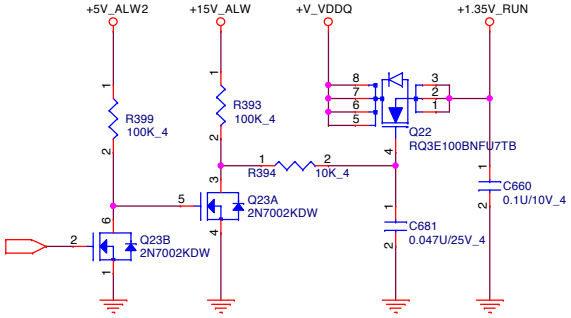
INT HDMI

Near PS8407A



5/16 change to 3.9K ohm

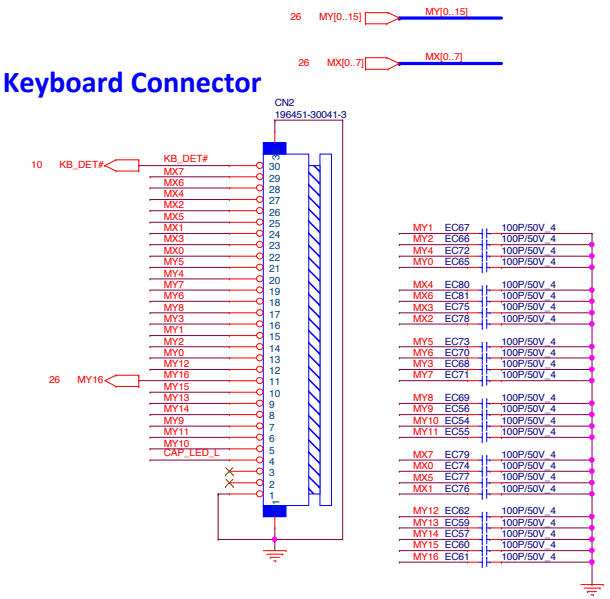
VDDRX, VDDTX, VDDTA change to 1.35V because SKL hadn't 1.5V power rail.



Quanta Computer Inc.
PROJECT : AM9A

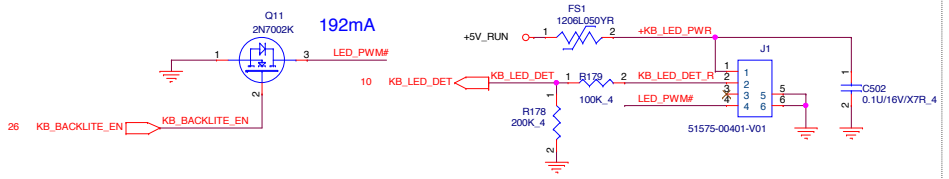
Size	Document Number	Rev
	HDMI/Re-driver	A0
Date: Wednesday, August 19, 2015	Sheet 30 of 57	

Keyboard Connector

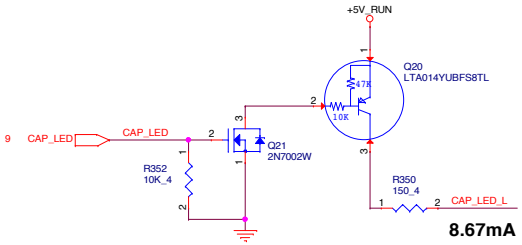


Key board illumination

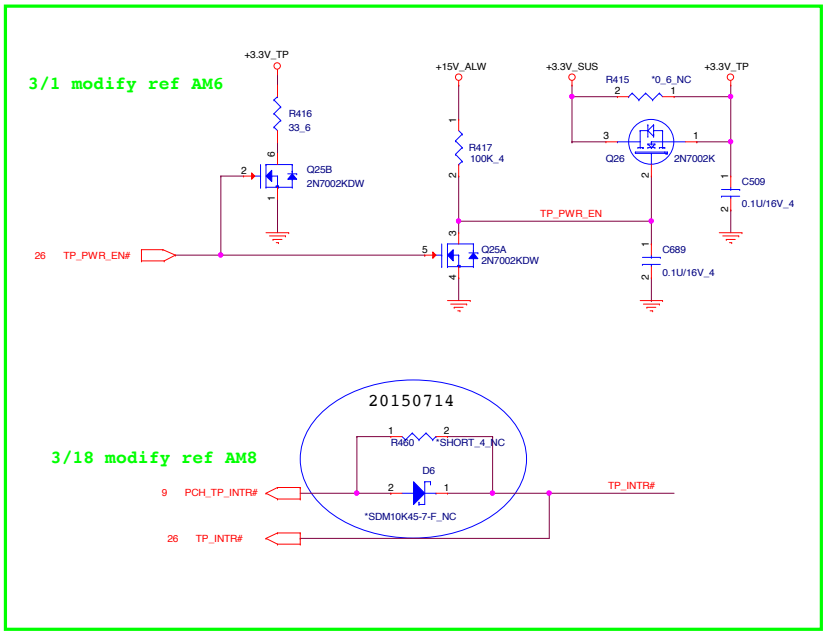
+KB_LED power trace width >10 mil



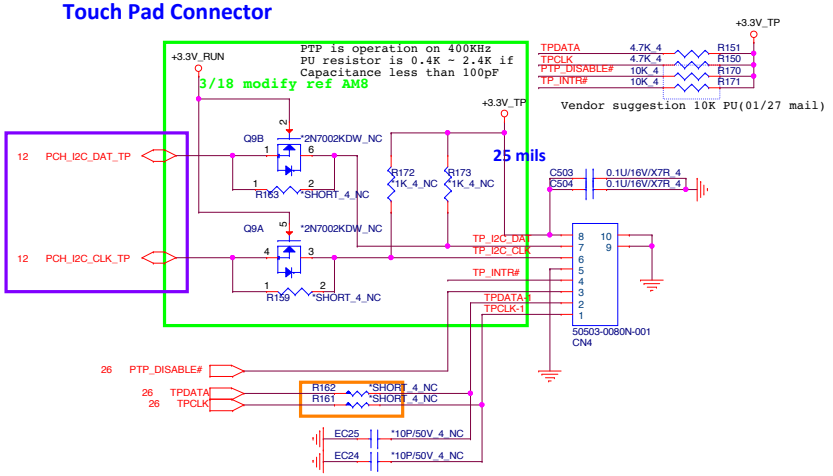
Vi(on_max)= -1.4V
Vi(off_min)=-0.3



Based on EEIG to add TP power controller circuity



Touch Pad Connector

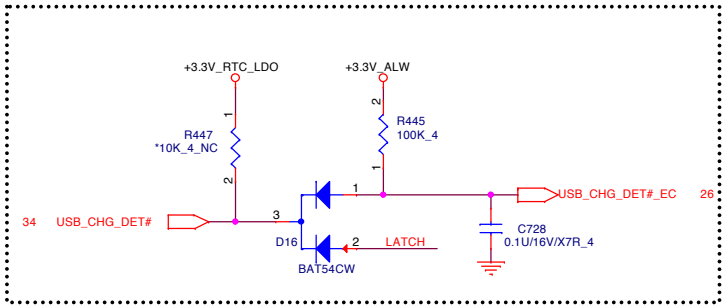


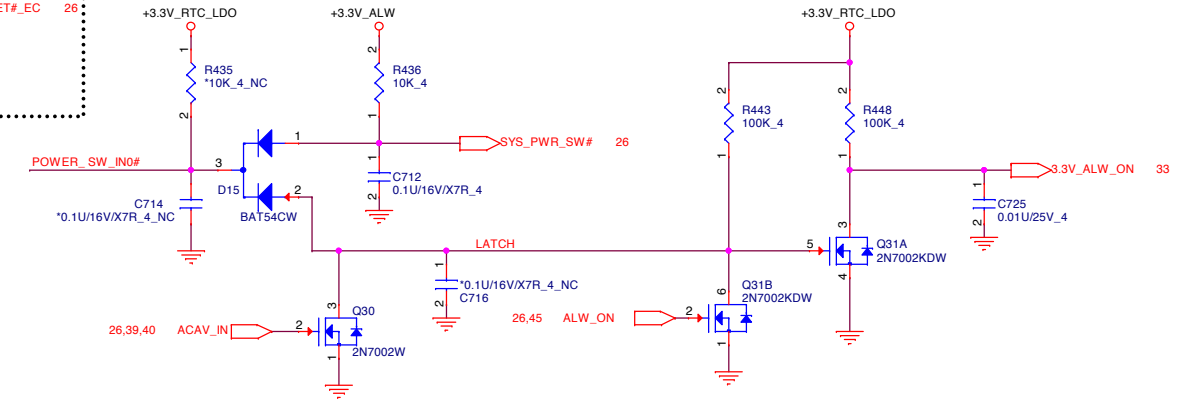
Quanta Computer Inc.

PROJECT : AM9A

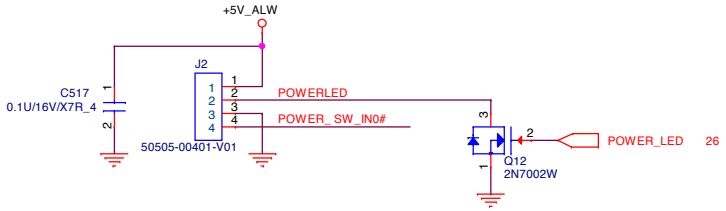
Size	Document Number	Rev
	KB/TP	A0
Date: Wednesday, August 19, 2015	Sheet 31 of 57	

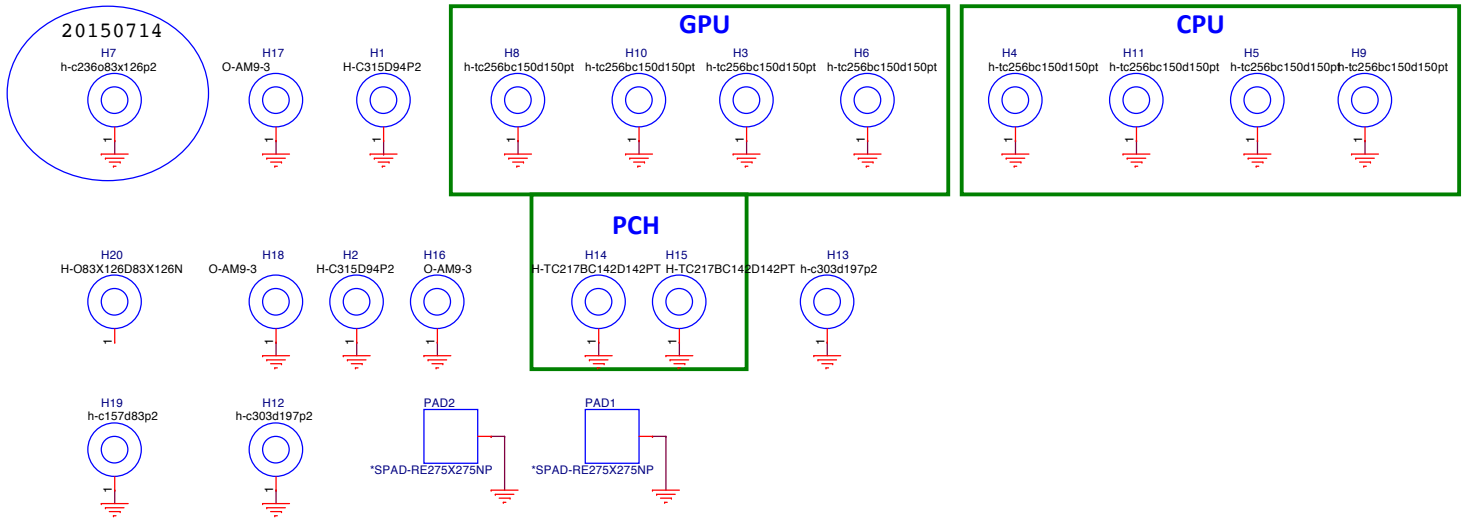
3VALW_ON POWER LOGIC





POWER BOARD CONN





Quanta Computer Inc.

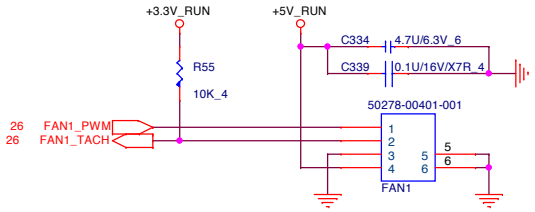
PROJECT : AM9A

Size	Document Number	Rev
	3VALW ON POWER LOGIC	A0

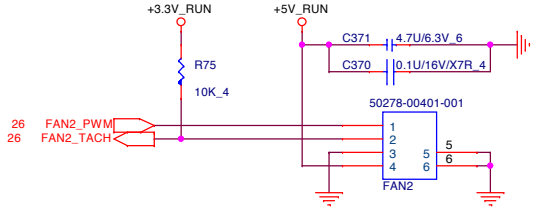
Date: Wednesday, August 19, 2015 Sheet 32 of 57

CPU FAN1 CONN

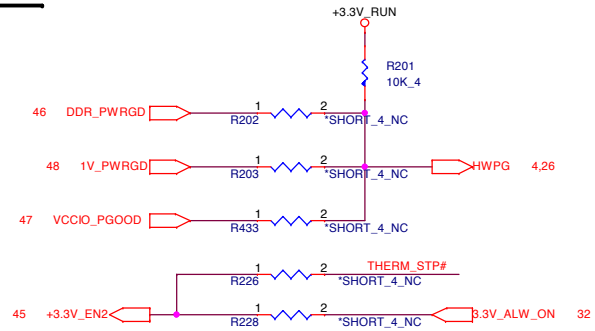
+5V_FAN
Max Current : 400 mA



GPU FAN2 CONN



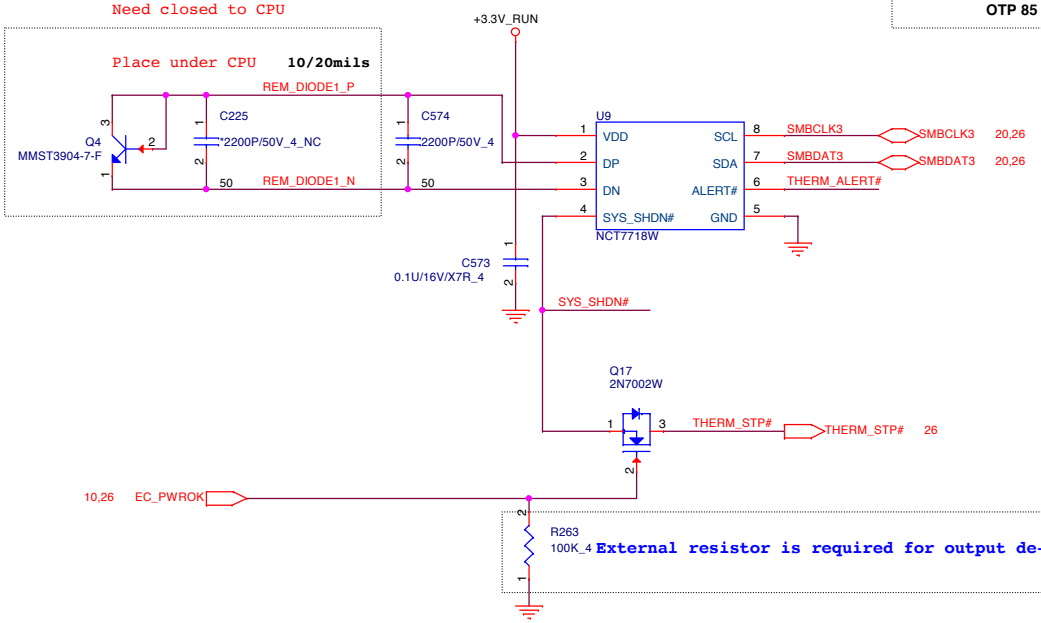
HWPG



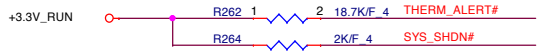
THERMAL IC

Need closed to CPU

Place under CPU **10/20mils**



OTP 85 degree C



OTP 85 degree : R526= 18.7K, R527= 2K

SYS_SHD# / ALERT#	2K	7.5K	10.5K	14K	18.7K
2K	77'C	87'C	97'C	107'C	117'C
7.5K	79'C	89'C	99'C	109'C	119'C
10.5K	81'C	91'C	101'C	111'C	121'C
14K	83'C	93'C	103'C	113'C	123'C
18.7K	85'C	95'C	105'C	115'C	125'C

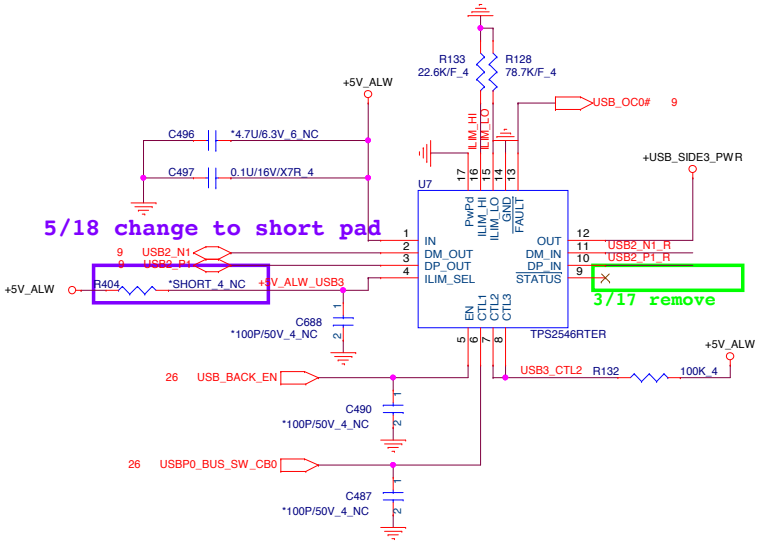
Quanta Computer Inc.
PROJECT : AM9A

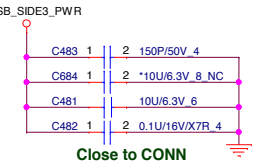
Size	Document Number	Rev
	FAN & THERMAL	A0
Date: Wednesday, August 19, 2015	Sheet 33 of 57	

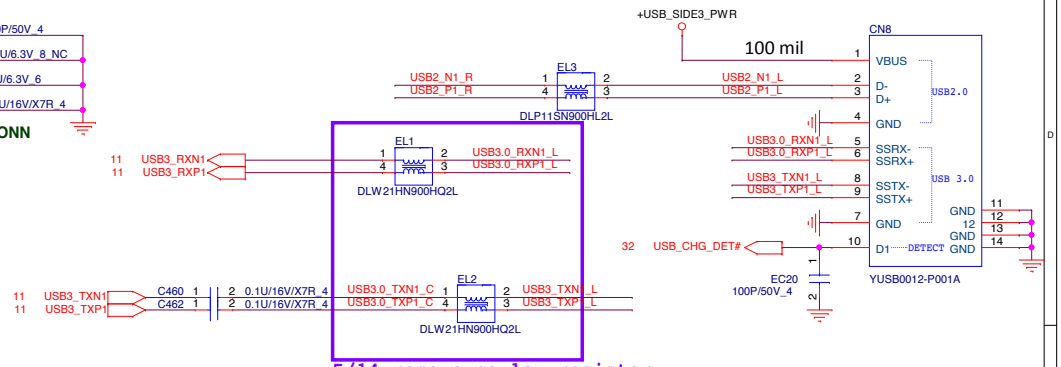
USB Power share

USB3.0/2.0 COMBO X 1

USBP0_BUS_SW_CB0	Mode	Operating at
High	CDP	S0, 1.5 A
Low	DCP, Auto-detect	S3/S4/S5, 2.1/1.5 A

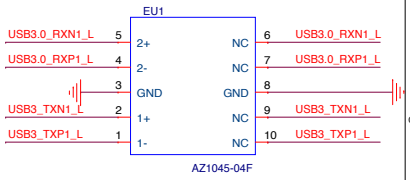






	R89	mA
OC limitation	22.6k ohm	2224
	23.2k ohm	2167

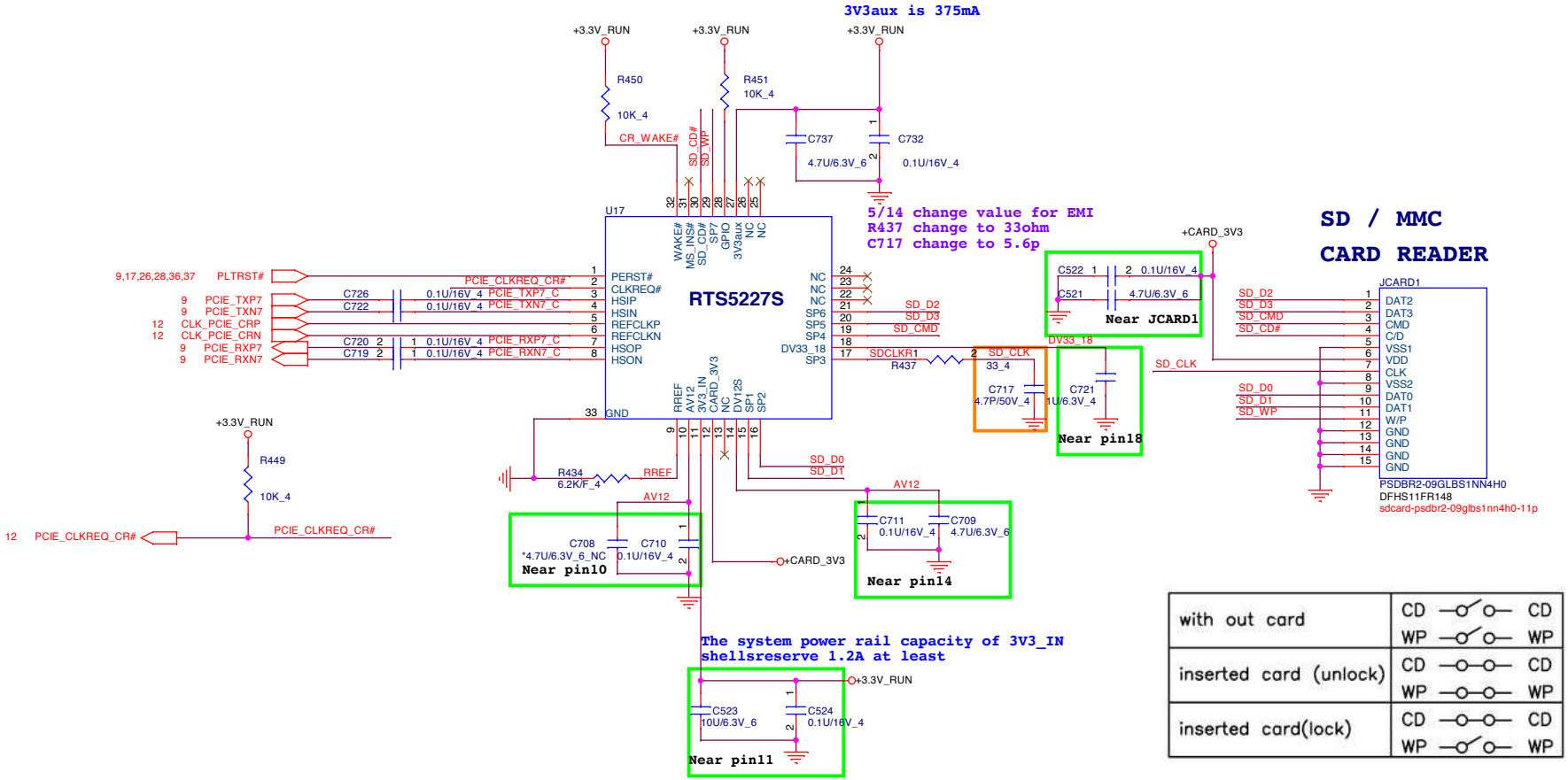
Need closed to CN9



Quanta Computer Inc.

PROJECT : AM9A

Size	Document Number	Rev
	USB3/USB Charger	A0
Date: Wednesday, August 19, 2015	Sheet 34 of 57	



with out card	CD — CD WP — WP
inserted card (unlock)	CD — CD WP — WP
inserted card(lock)	CD — CD WP — WP

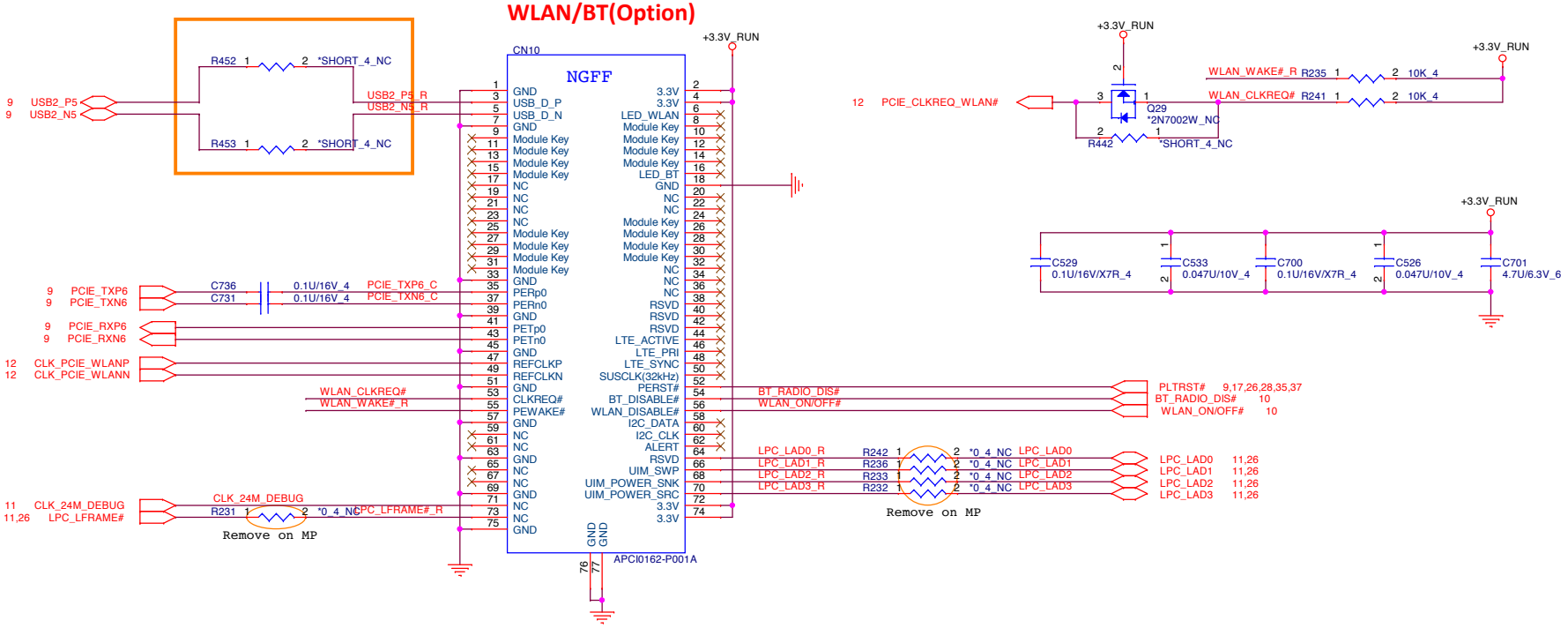
Quanta Computer Inc.

PROJECT : AM9A

Size	Document Number	Rev
	Card Reader RTS5227S	A0

Date: Wednesday, August 19, 2015 Sheet 35 of 57

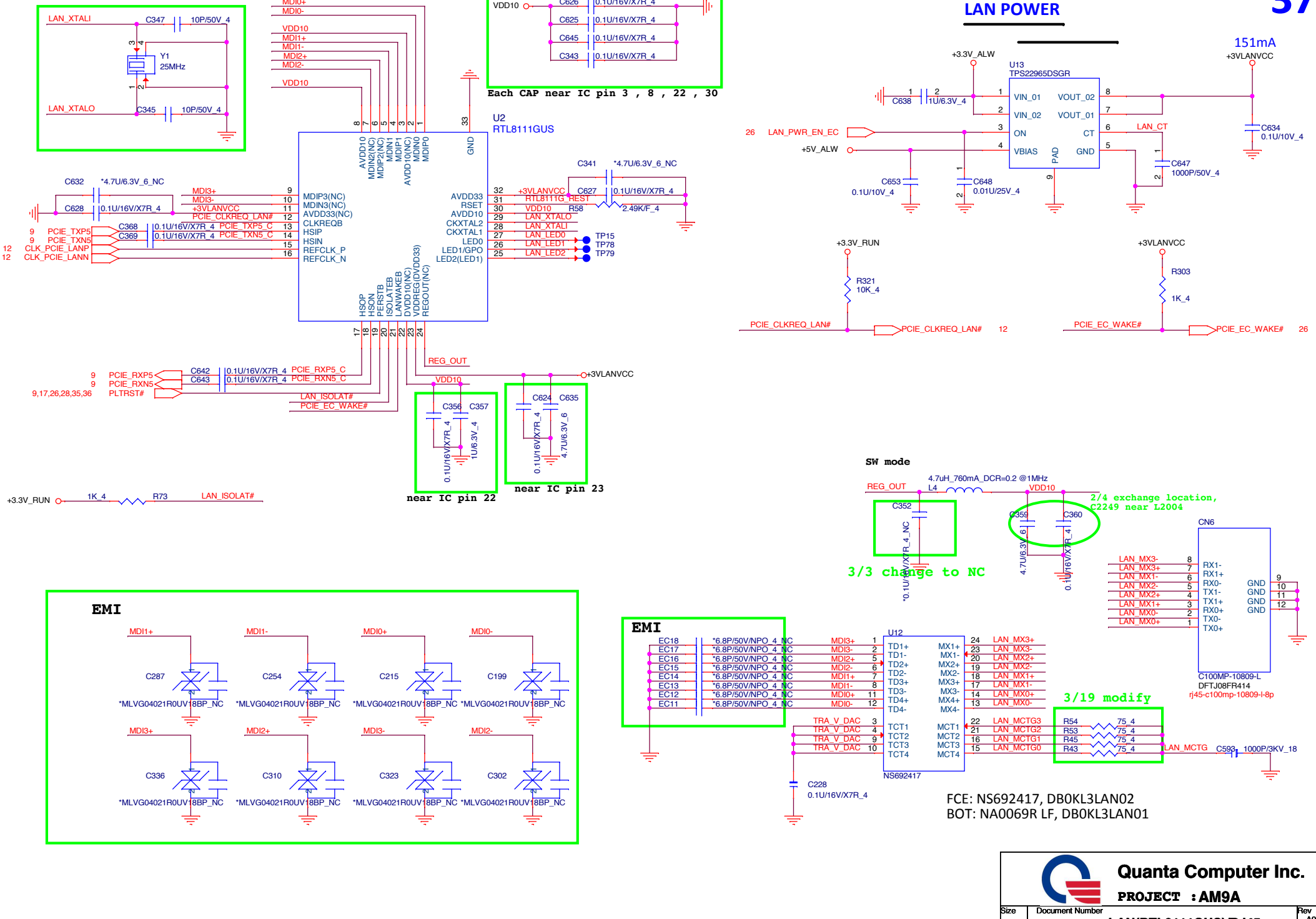
M.2 (NGFF) A-KEY WLAN/BT(Option)



Quanta Computer Inc.			
PROJECT : AM9A			
Size	Document Number: WLAN/BT		Rev: A0
Date: Wednesday, August 19, 2015	Sheet 36 of 57		

LAN POWER

151mA



SW mode

EMI

EMI

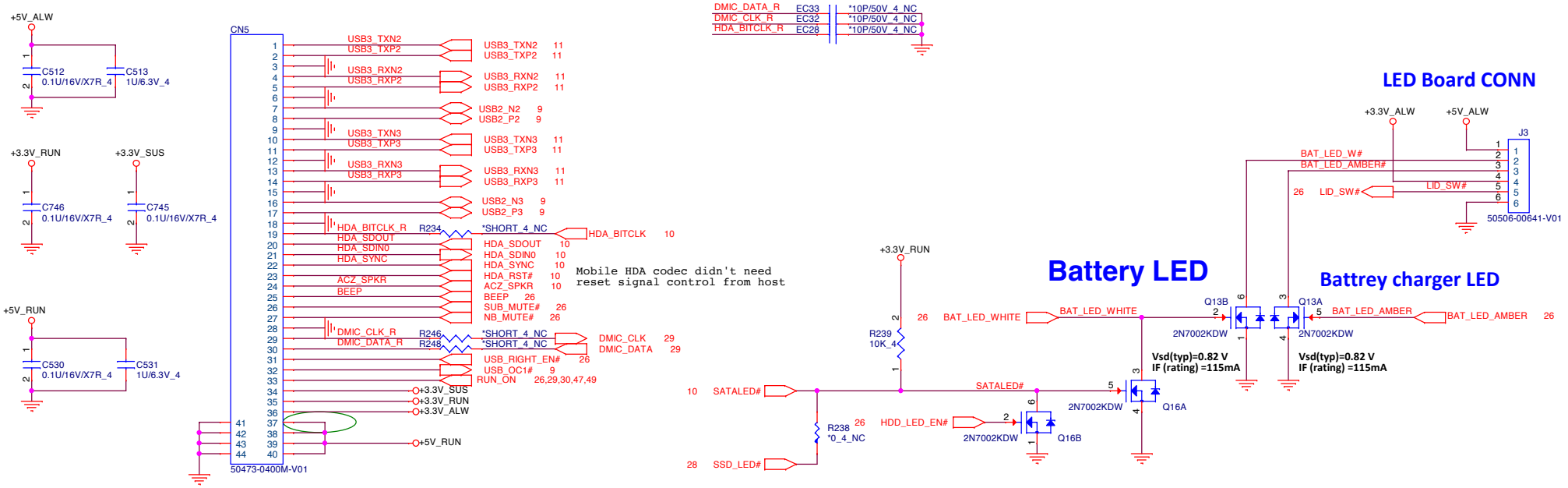
FCE: NS692417, DB0KL3LAN02
BOT: NA0069R LF, DB0KL3LAN01

Quanta Computer Inc.

PROJECT : AM9A

Size	Document Number	Rev
	LAN(RTL8111GUS)/RJ45	A0
Date: Wednesday, August 19, 2015	Sheet 37 of 57	

MB to IO Connector

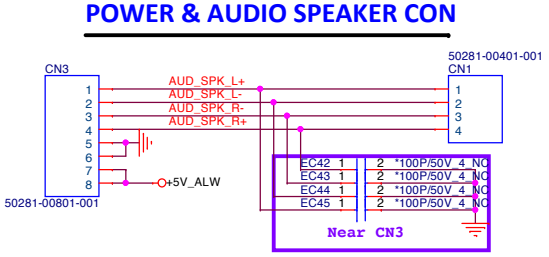


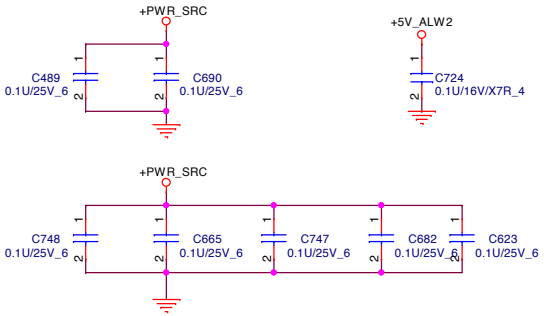
LED Board CONN

Battery LED

Battrey charger LED

POWER & AUDIO SPEAKER CON



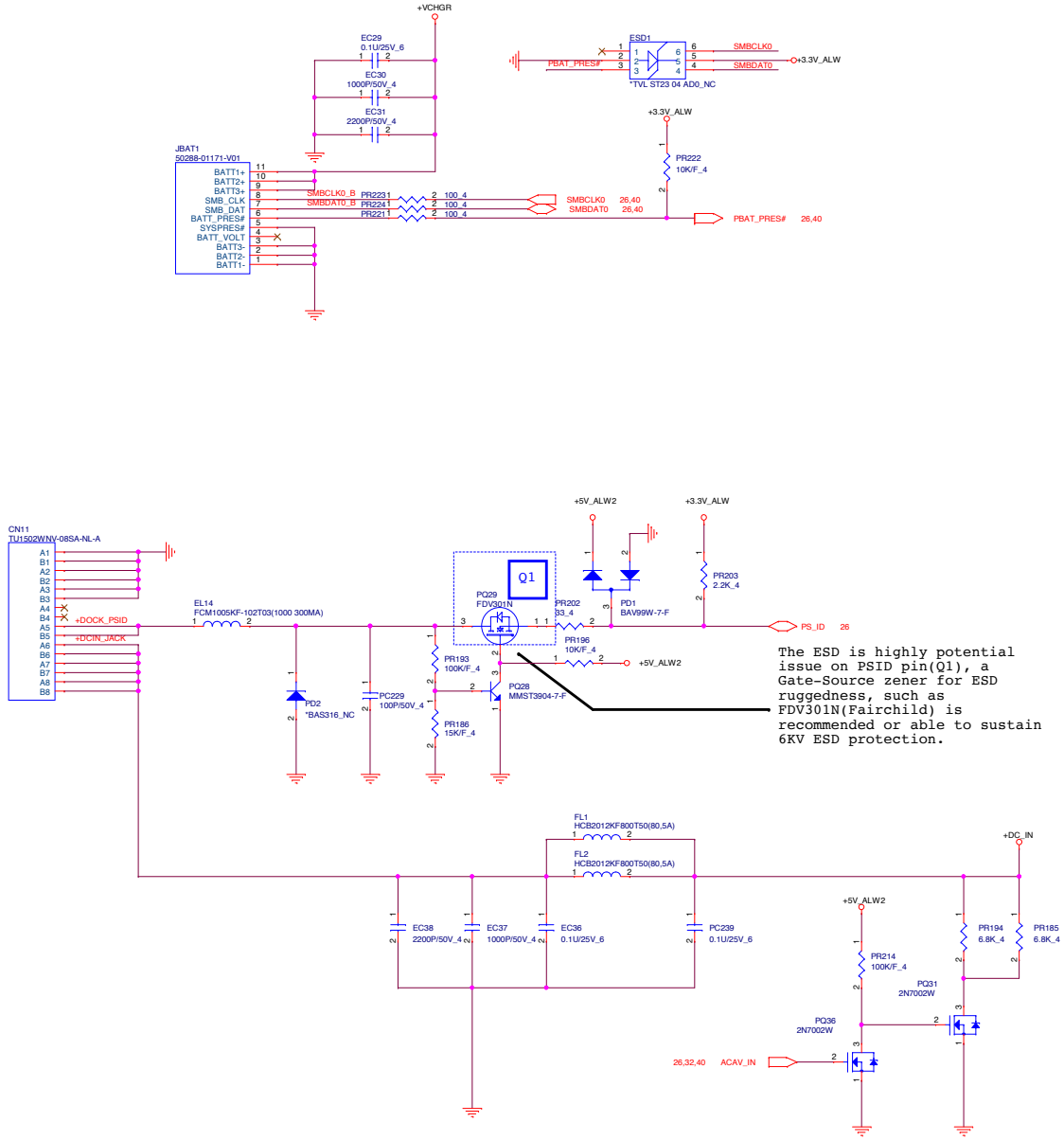


Quanta Computer Inc.

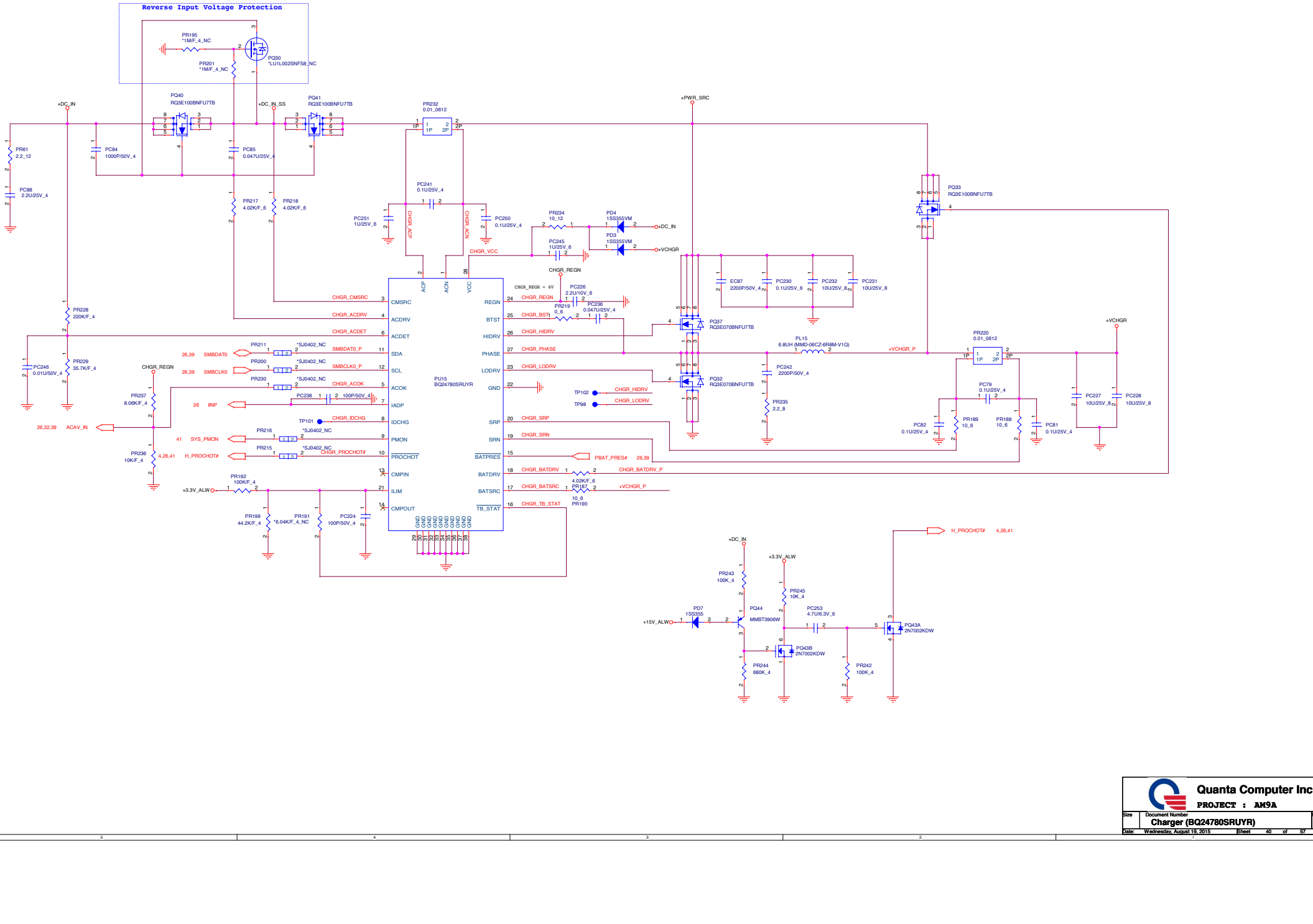
PROJECT : AM9A

Size	Document Number	Rev
	IO BD CONN/LED	A0

Date: Wednesday, August 19, 2015 Sheet 38 of 57



Quanta Computer Inc.		
PROJECT : AM9A		
Size	Document Number: DCin & Bat	Rev: A
Date: Wednesday, August 19, 2015	Sheet 39 of 58	

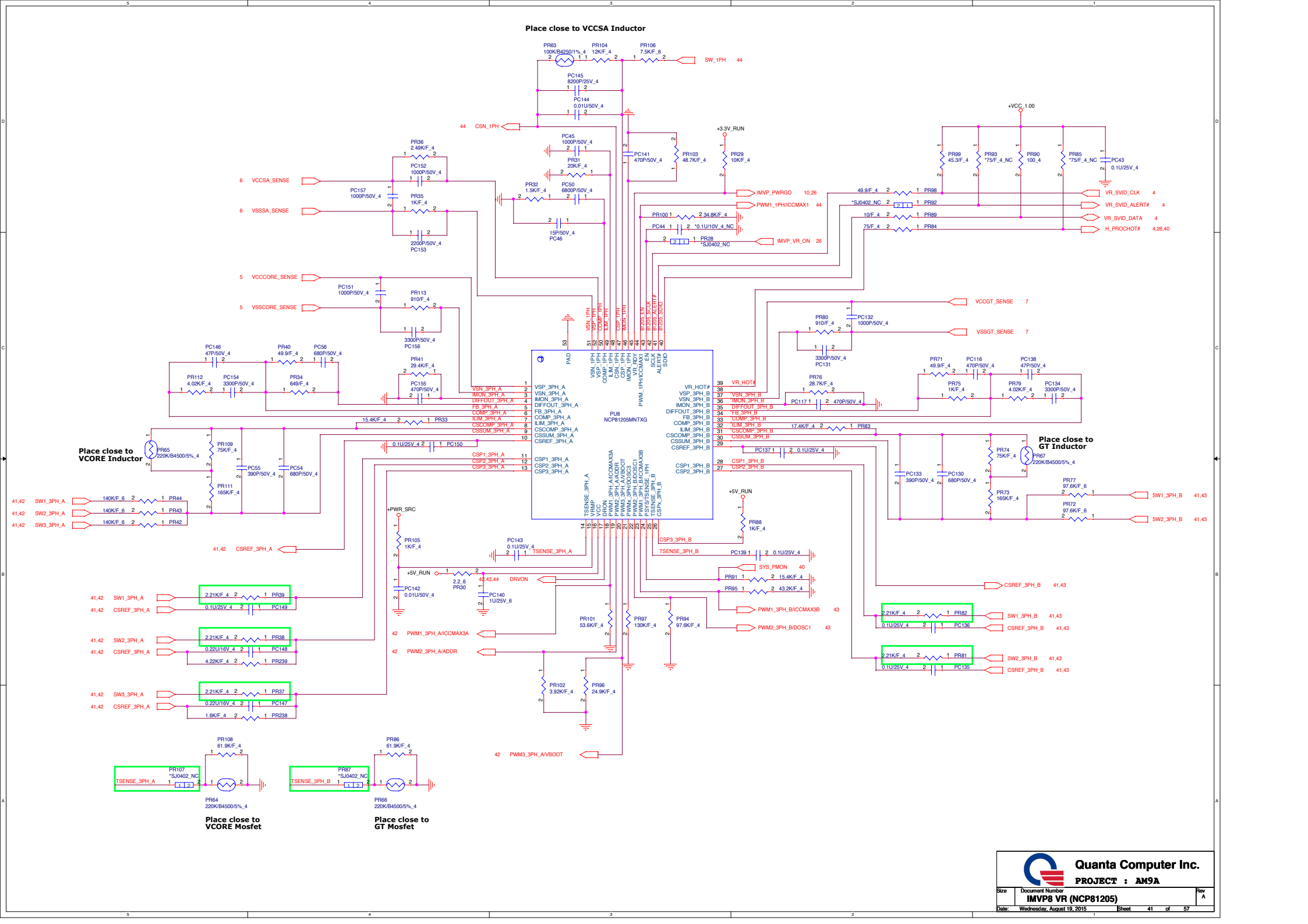


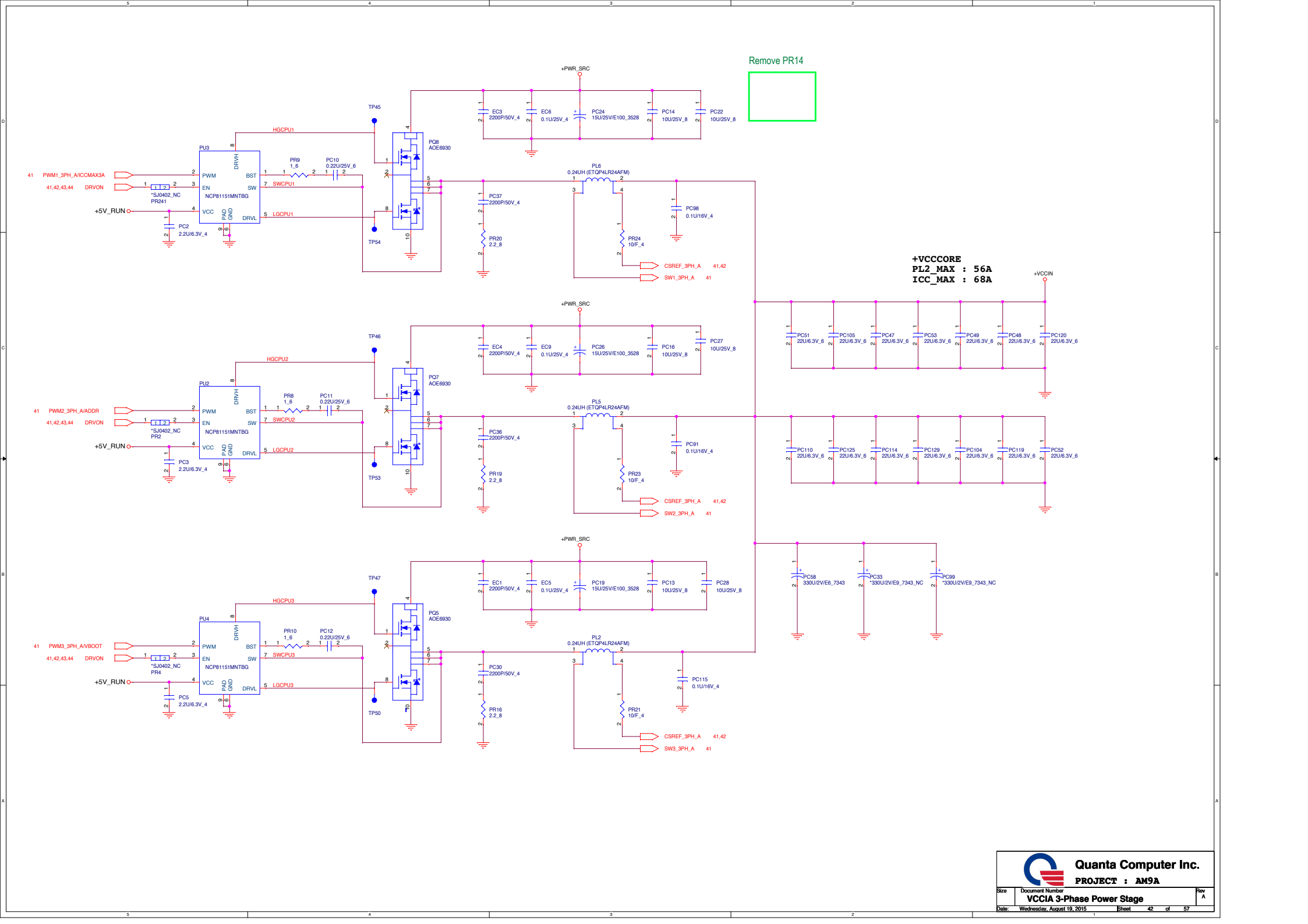
Quanta Computer Inc.

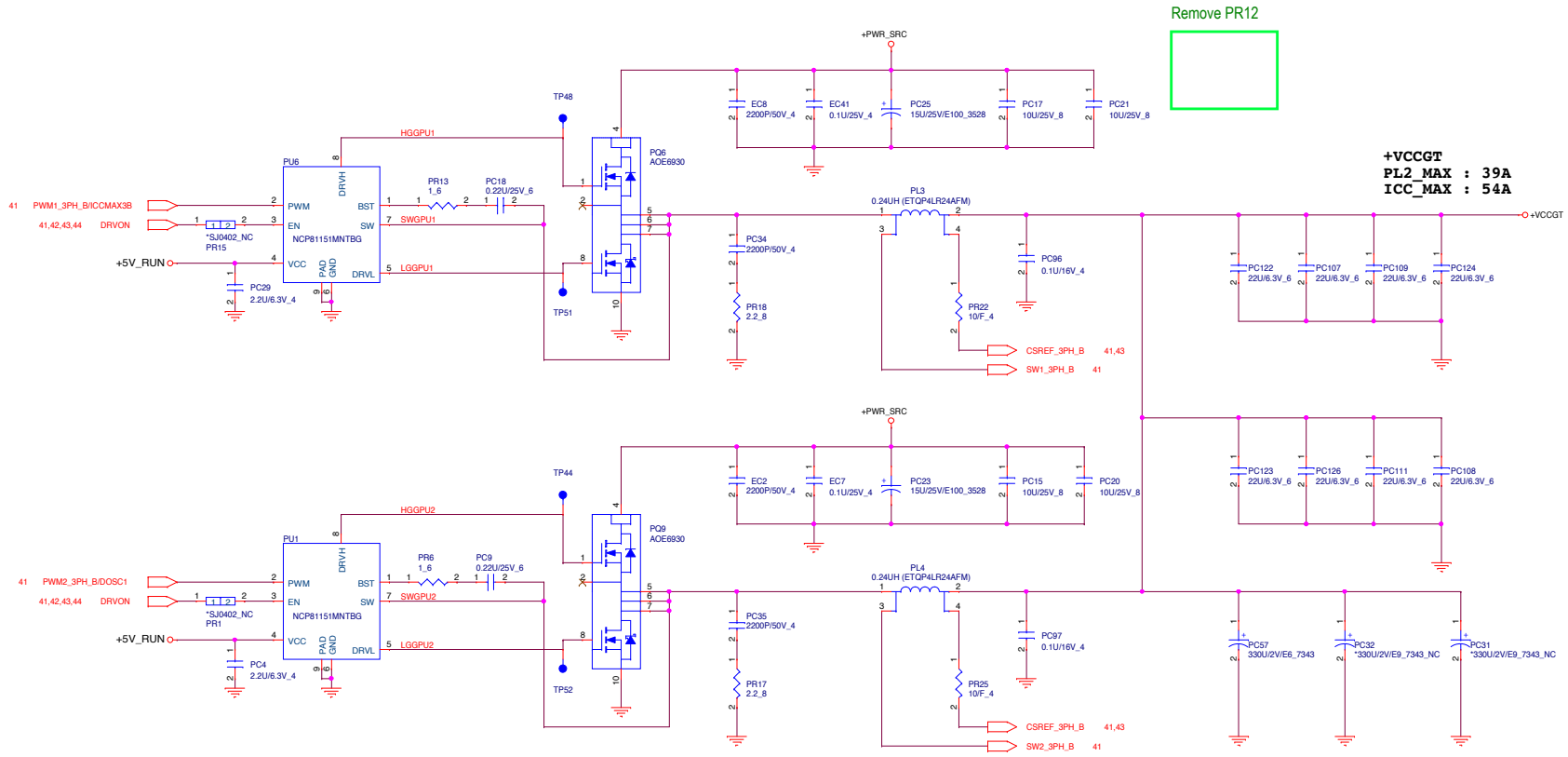
PROJECT : AM9A

Size	Document Number	Rev
	Charger (BQ24780SRUYR)	A

Date: Wednesday, August 19, 2015 Sheet 40 of 57


Place close to VCCSA Inductor
PR63 100K/B4250/1%_4
PR104 12K/F_4
PR106 7.5K/F_6
SW_1PH 44
PC145 8200P/25V_4
PC144 0.01U/50V_4
44 CSN_1PH
PC45 1000P/50V_4
PR31 20K/F_4
PC141 470P/50V_4
PR103 48.7K/F_4
+3.3V_RUN
PR29 10K/F_4
PR36 2.49K/F_4
PC152 1000P/50V_4
6 VCCSA_SENSE
PC157 1000P/50V_4
PR35 1K/F_4
6 VSSSA_SENSE
2200P/50V_4 PC153
PR32 1.5K/F_4
PC50 6800P/50V_4
15P/50V_4 PC46
IMVP_PWRGD 10,26
PWM1_1PH/ICCMAX1 44
PR100 2.34.8K/F_4
PC44 *0.1U/10V_4_NC
PR28 *SJ0402_NC
IMVP_VR_ON 26
+VCC_1.00
PR99 45.3/F_4
PR93 *75/F_4_NC
PR90 100_4
PR85 *75/F_4_NC
PC43 0.1U/25V_4
49.9/F_4 PR98
*SJ0402_NC PR92
10/F_4 PR89
75/F_4 PR84
VR_SVID_CLK 4
VR_SVID_ALERT# 4
VR_SVID_DATA 4
H_PROCHOT# 4,26,40
5 VCCCORE_SENSE
PC151 1000P/50V_4
5 VSSCORE_SENSE
PR113 910/F_4
3300P/50V_4 PC156
VSN_1PH
VSP_1PH
COMP_1PH
ILIM_1PH
CSP_1PH
IMON_1PH
PAD
PR80 910/F_4
PC132 1000P/50V_4
3300P/50V_4 PC131
VCCGT_SENSE 7
VSSGT_SENSE 7
PC146 47P/50V_4
PR40 49.9/F_4
PC56 680P/50V_4
PR112 4.02K/F_4
PC154 3300P/50V_4
PR34 649/F_4
PR41 29.4K/F_4
PC155 470P/50V_4
VSN_3PH_A
IMON_3PH_A
DIFFOUT_3PH_A
FB_3PH_A
COMP_3PH_A
ILIM_3PH_A
CSCOMP_3PH_A
CSSUM_3PH_A
CSREF_3PH_A
PU8
NCP81205MNTXG
VSP_3PH_A
PWM1_1PH/ICCMAX1
EN
SCLK
ALERT#
SDIO
VR_HOT#
VSP_3PH_B
VSN_3PH_B
IMON_3PH_B
DIFFOUT_3PH_B
FB_3PH_B
COMP_3PH_B
ILIM_3PH_B
CSCOMP_3PH_B
CSSUM_3PH_B
CSREF_3PH_B
PR71 49.9/F_4
PC116 470P/50V_4
PC138 470P/50V_4
PR76 28.7K/F_4
PR75 1K/F_4
PR79 4.02K/F_4
PC134 3300P/50V_4
PC117 470P/50V_4
15.4K/F_4 PR33
17.4K/F_4 PR83
PC137 0.1U/25V_4
Place close to VCORE Inductor
PR65 220K/B4500/5%_4
PR109 75K/F_4
PR111 165K/F_4
PC55 390P/50V_4
PC54 680P/50V_4
0.1U/25V_4 PC150
CSP1_3PH_A
CSP2_3PH_A
CSP3_3PH_A
CSP1_3PH_B
CSP2_3PH_B
Place close to GT Inductor
PR67 220K/B4500/5%_4
PR74 75K/F_4
PR73 165K/F_4
PC133 390P/50V_4
PC130 680P/50V_4
PR77 97.6K/F_6
PR72 97.6K/F_6
SW1_3PH_B 41,43
SW2_3PH_B 41,43
41,42 SW1_3PH_A
41,42 SW2_3PH_A
41,42 SW3_3PH_A
140K/F_6 PR44
140K/F_6 PR43
140K/F_6 PR42
+PWR_SRC
PR105 1K/F_4
+5V_RUN
2.2_6 PR30
PC142 0.01U/50V_4
PC140 1U/25V_6
PC143 0.1U/25V_4
TSENSE_3PH_A
TSENSE_3PH_B
CSP3_3PH_B
+5V_RUN
PR88 1K/F_4
SYS_PMON 40
PR91 15.4K/F_4
PR95 43.2K/F_4
PWM1_3PH_B/ICCMAX3B 43
PWM2_3PH_B/DOSC1 43
CSREF_3PH_B 41,43
41,42 CSREF_3PH_A
42,43,44 DRVON
PR101 53.6K/F_4
PR97 130K/F_4
PR94 97.6K/F_4
42 PWM1_3PH_A/ICCMAX3A
42 PWM2_3PH_A/ADDR
42 PWM3_3PH_A/VBOOT
PR102 3.92K/F_4
PR96 24.9K/F_4
2.21K/F_4 PR39
0.1U/25V_4 PC149
2.21K/F_4 PR38
0.22U/16V_4 PC148
4.22K/F_4 PR239
2.21K/F_4 PR37
0.22U/16V_4 PC147
1.6K/F_4 PR238
2.21K/F_4 PR82
0.1U/25V_4 PC136
2.21K/F_4 PR81
0.1U/25V_4 PC135
PR108 61.9K/F_4
PR107 *SJ0402_NC
PR64 220K/B4500/5%_4
Place close to VCORE Mosfet
PR86 61.9K/F_4
PR87 *SJ0402_NC
PR66 220K/B4500/5%_4
Place close to GT Mosfet
Quanta Computer Inc.
PROJECT : AM9A
Size
Document Number
IMVP8 VR (NCP81205)
Rev A
Date: Wednesday, August 19, 2015
Sheet 41 of 57


Remove PR14
+VCCCORE
PL2_MAX : 56A
ICC_MAX : 68A
+PWR_SRC
+VCCIN
+5V_RUN
PU3
PU2
PU4
NCP81151MNTBG
PWM1_3PH_A/ICCMAX3A
PWM2_3PH_A/ADDR
PWM3_3PH_A/VBOOT
DRVON
HGCPU1
HGCPU2
HGCPU3
SWCPU1
SWCPU2
SWCPU3
LGCPU1
LGCPU2
LGCPU3
TP45
TP46
TP47
TP54
TP53
TP50
PQ8 AOE6930
PQ7 AOE6930
PQ5 AOE6930
PL6 0.24UH (ETQP4LR24AFM)
PL5 0.24UH (ETQP4LR24AFM)
PL2 0.24UH (ETQP4LR24AFM)
CSREF_3PH_A
SW1_3PH_A
SW2_3PH_A
SW3_3PH_A
Quanta Computer Inc.
PROJECT : AM9A
VCCIA 3-Phase Power Stage
Wednesday, August 19, 2015
Sheet 42 of 57



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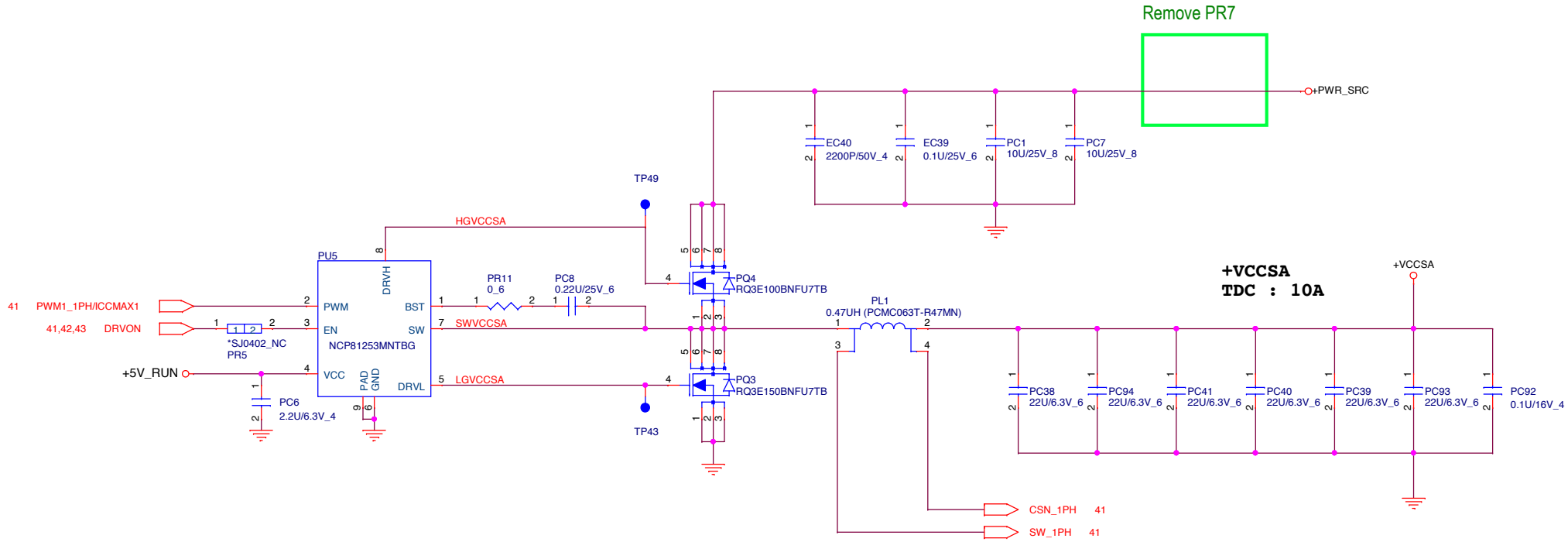
PROJECT : AM9A

Size	Document Number	Rev
	VCCGT 2-Phase Power Stage	A

Date: Wednesday, August 19, 2015 Sheet 43 of 57



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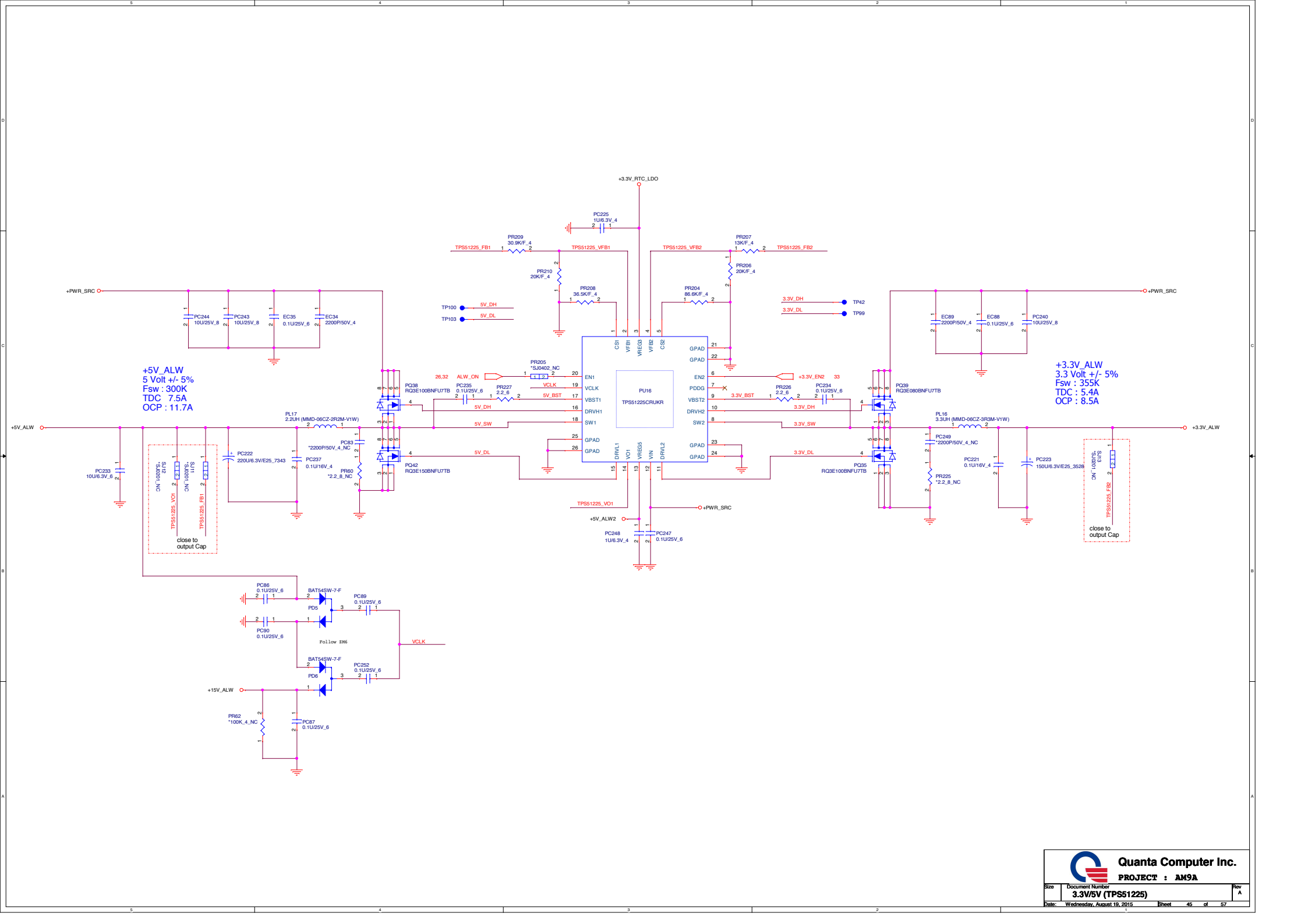
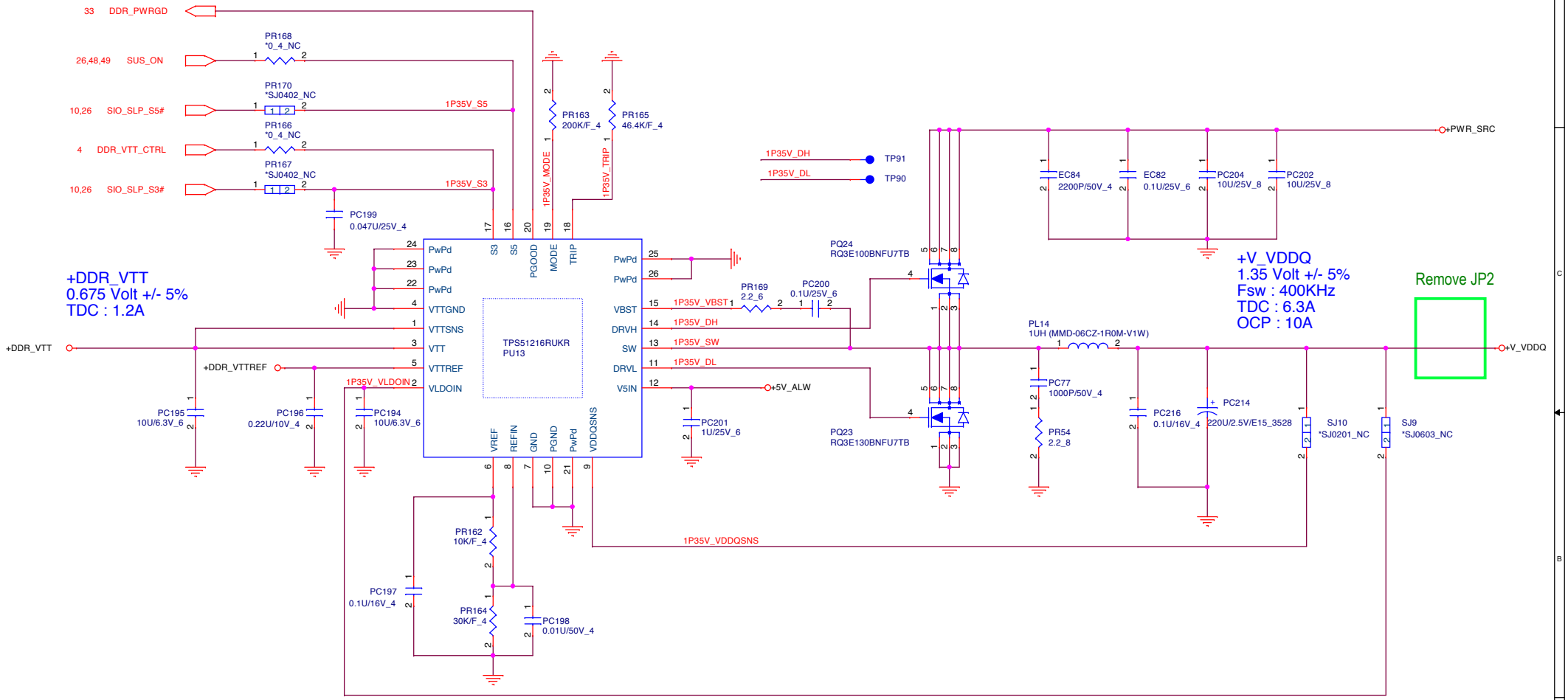
PROJECT : AM9A

Size	Document Number	Rev
	VCCSA 1-Phase Power Stage	A

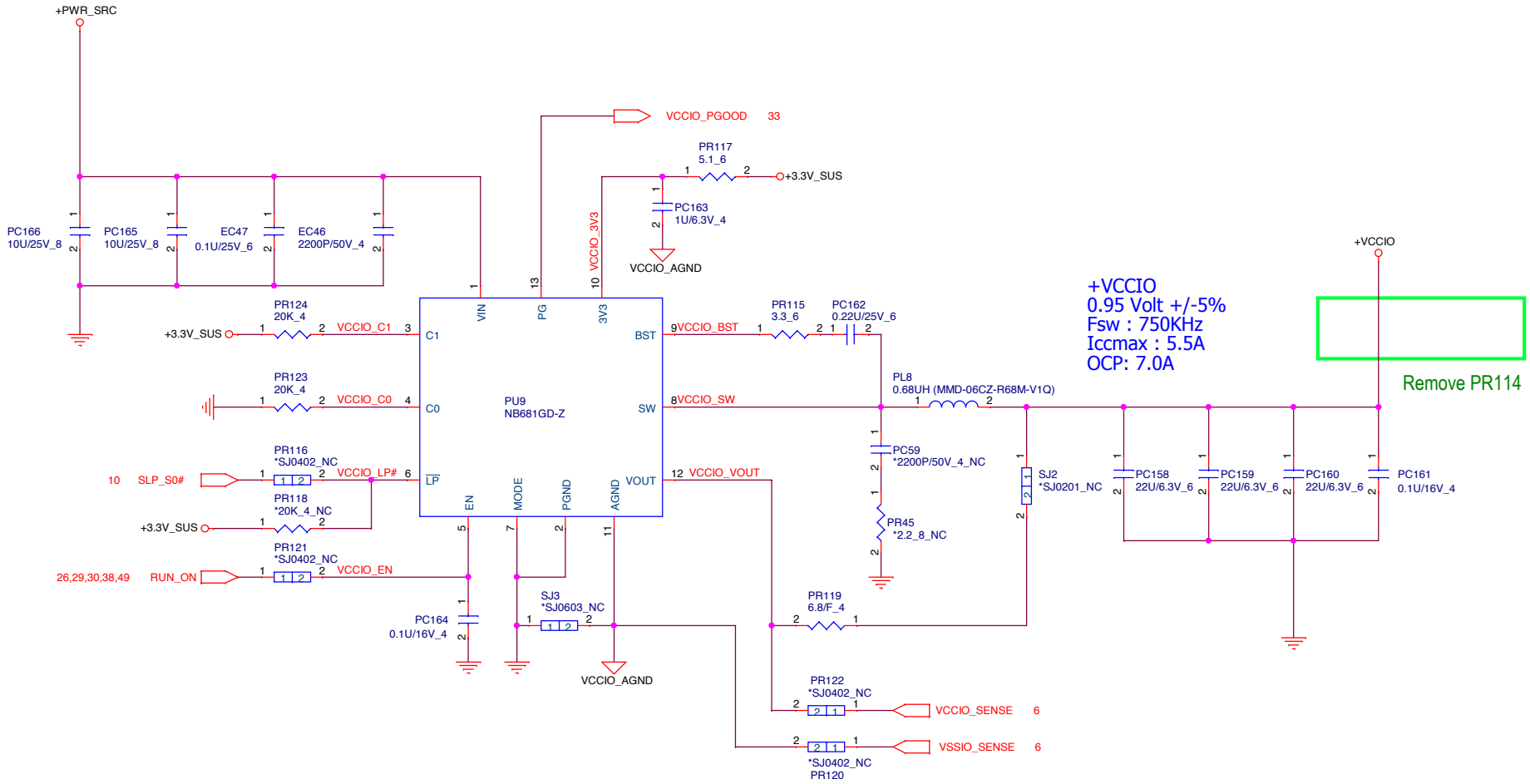
Date: Wednesday, August 19, 2015 Sheet 44 of 57



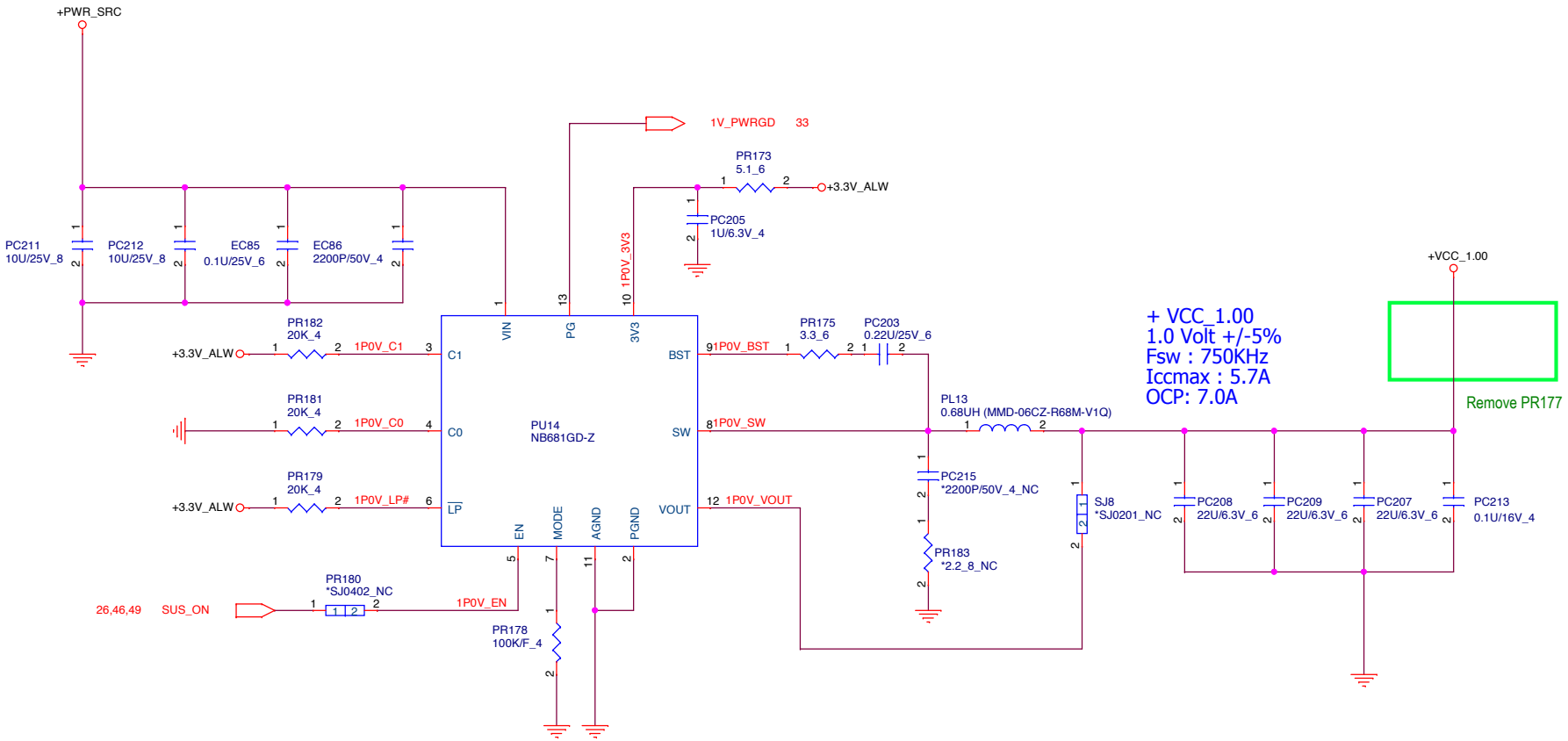
Quanta Computer Inc.			
PROJECT : AM9A			
Size	Document Number		Rev
	3.3V/5V (TPS51225)		A
Date: Wednesday, August 19, 2015	Sheet 45 of 57		



Quanta Computer Inc.		
PROJECT : AM9A		
Size	Document Number: 1.35V_DDR/0.675V(TPS51216)	Rev: A
Date: Wednesday, August 19, 2015	Sheet 46 of 57	

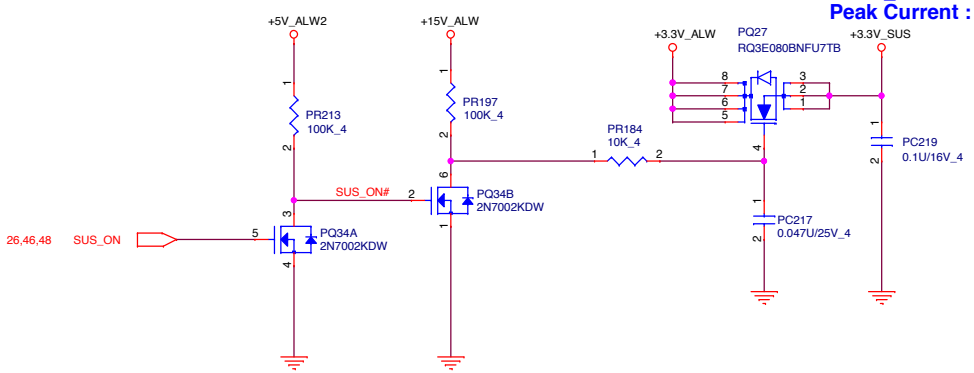


Quanta Computer Inc.		
PROJECT : AM9A		
Size	Document Number: VCCIO (NB681GD-Z)	Rev: A
Date: Wednesday, August 19, 2015	Sheet 47 of 57	

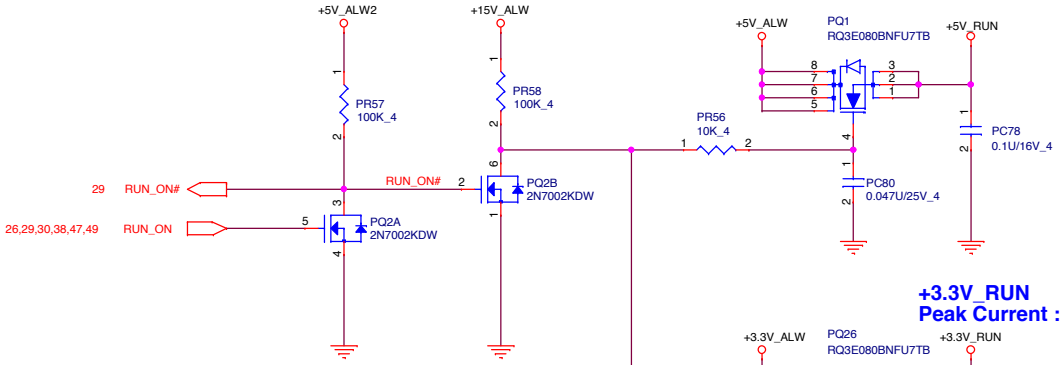


Quanta Computer Inc.		
PROJECT : AM9A		
Size	Document Number: VCC_1.00 VCCIO (NB681GD-Z)	Rev: A
Date: Wednesday, August 19, 2015	Sheet 48 of 57	

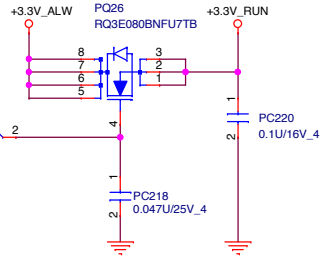
+3.3V_SUS
Peak Current : 1.1A



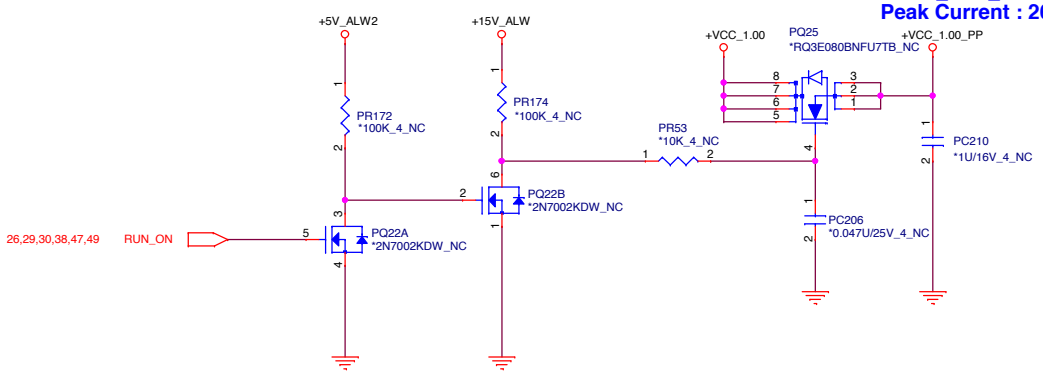
+5V_RUN
Peak Current : 6.5A



+3.3V_RUN
Peak Current : 4.7A



+VCC_1.00_PP
Peak Current : 265mA



Quanta Computer Inc.

PROJECT : AM9A

Size	Document Number	Rev
	SUS_RUN Power Switch	A
Date: Wednesday, August 19, 2015	Sheet 49 of 57	

Remove PR161

+VGACORE
EDP : 51.1A
EDP-Peak : 87A
OCP : 100A
Fsw : 300KHz

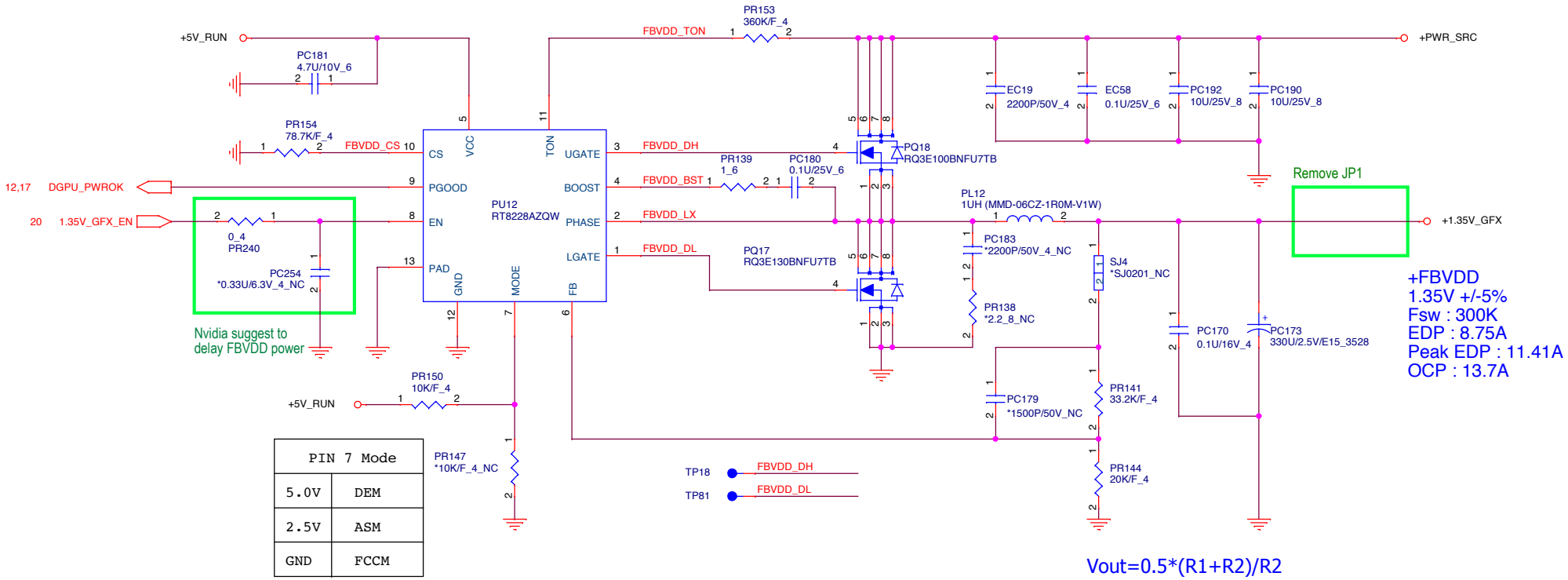
PU11
RT8813CGQW

+3V_GFX
Peak Current : 170mA

+3V_AON
Peak Current : 170mA

PU10
RT9610BZQW

Quanta Computer Inc.			
PROJECT : AM9A			
Size	Document Number		Rev
	dGPU CORE (RT8813C)		A
Date: Wednesday, August 19, 2015	Sheet 50 of 57		



PIN 7 Mode	
5.0V	DEM
2.5V	ASM
GND	FCCM

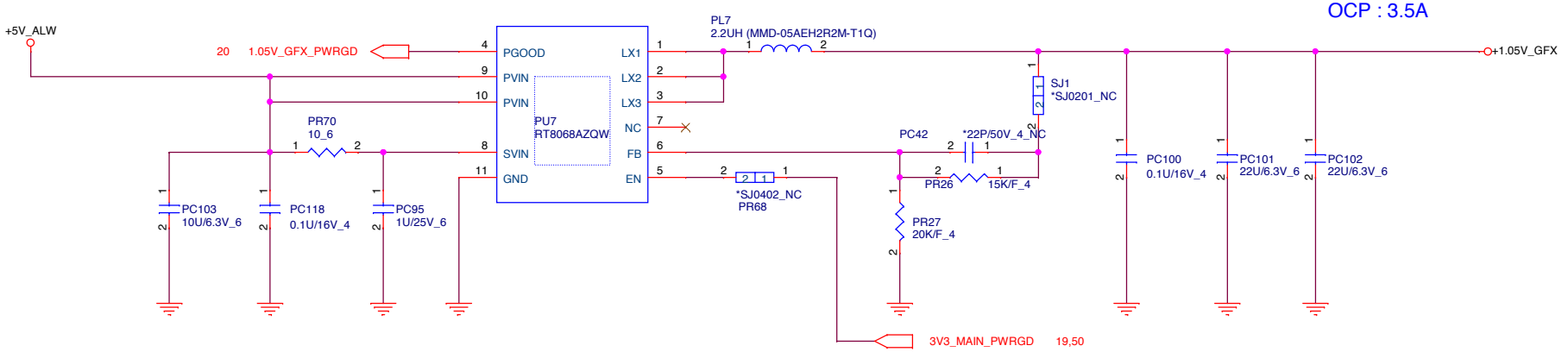
Quanta Computer Inc.

PROJECT : AM9A

Size	Document Number	Rev
	FBVDD_GPU(RT8228AZ)	A

Date: Wednesday, August 19, 2015 Sheet 51 of 57

+1.05V_GFX
1.05 Volt +/- 5%
TDC : 2.9A
OCP : 3.5A



Vout=0.6*(R1+R2)/R2

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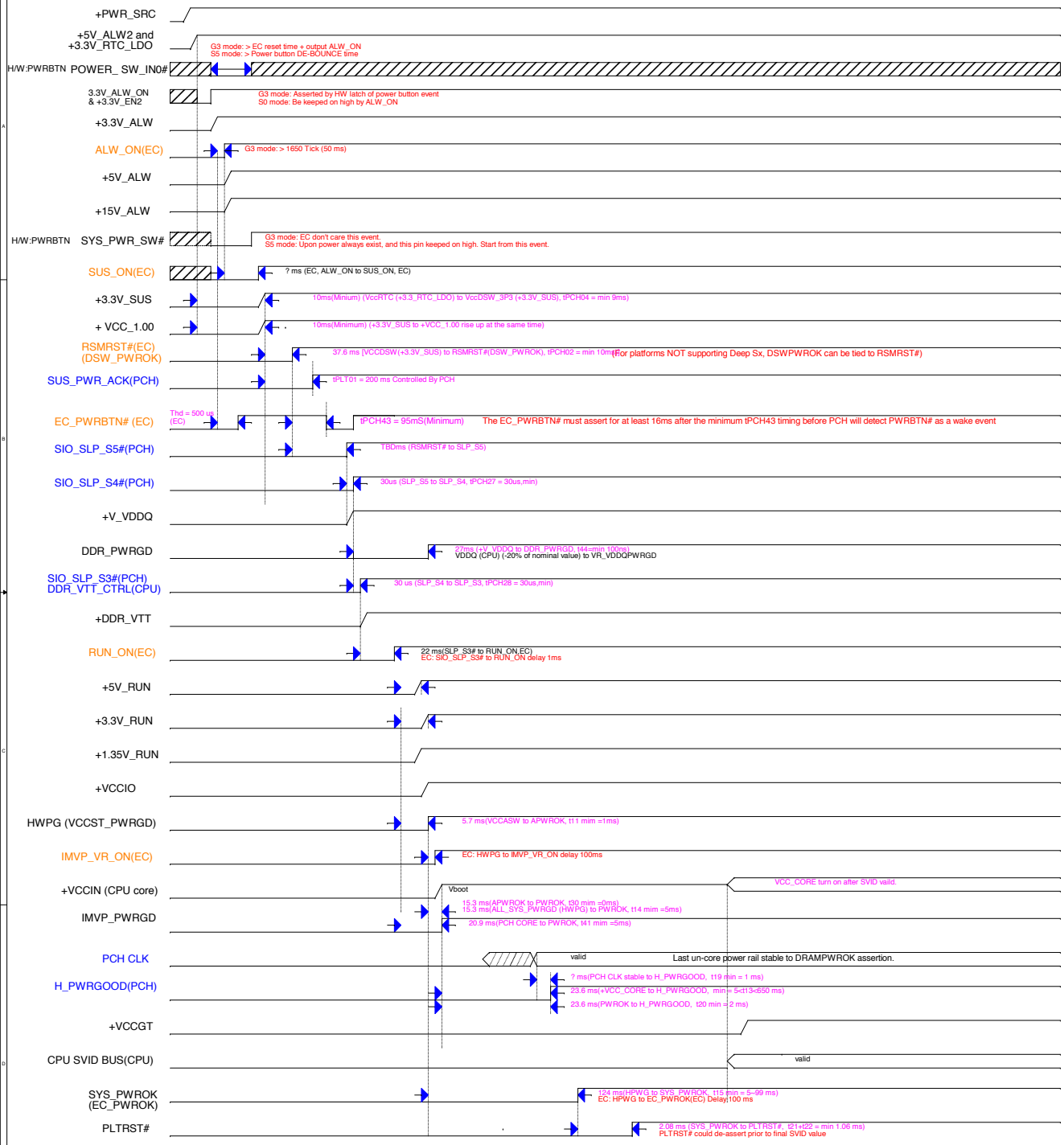
PROJECT : AM9A

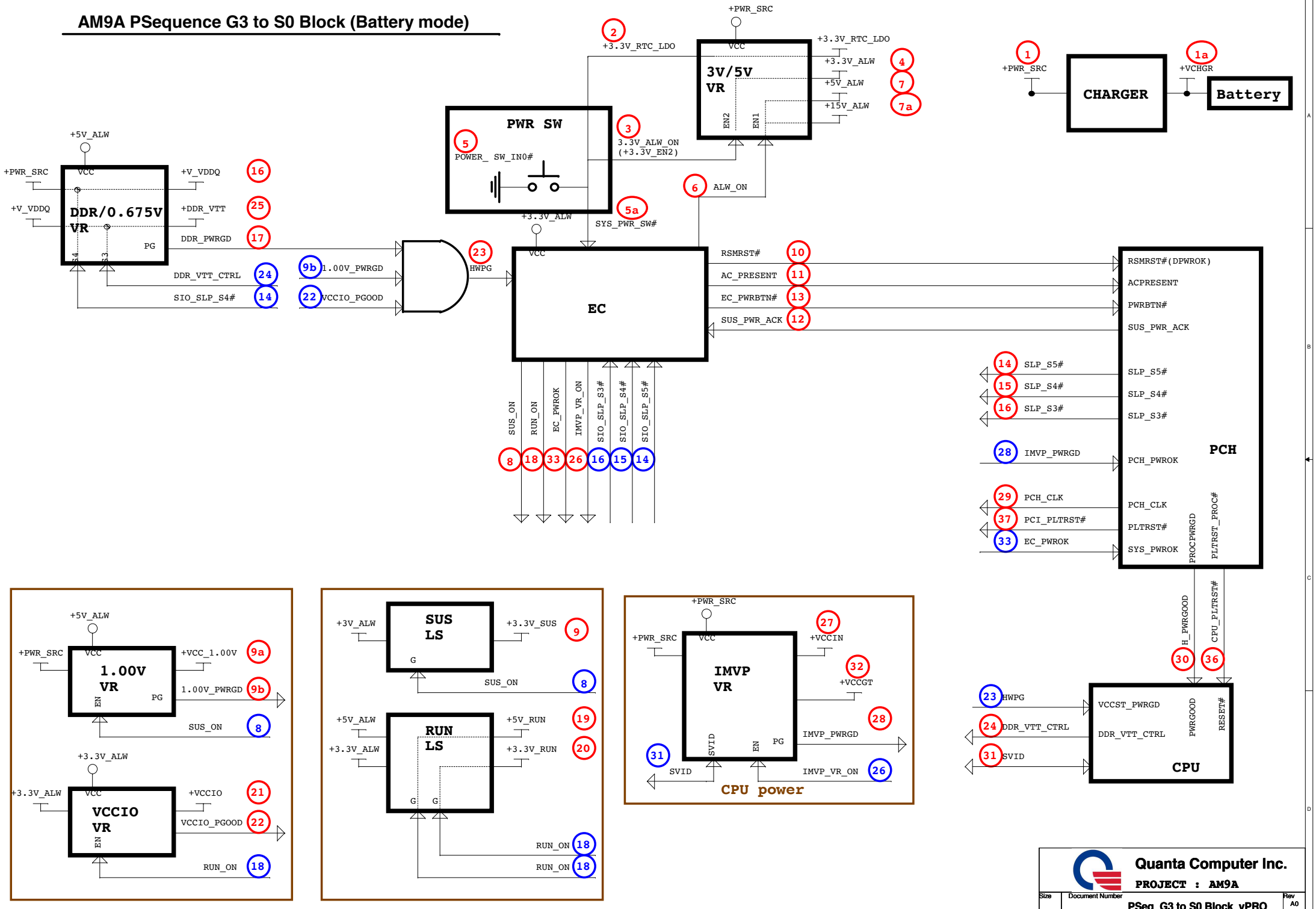
Size	Document Number	Rev
	1.05V_GFX (RT8068AZQW)	A
Date: Wednesday, August 19, 2015	Sheet 52 of 57	

AM9A PSequence G3 to S0



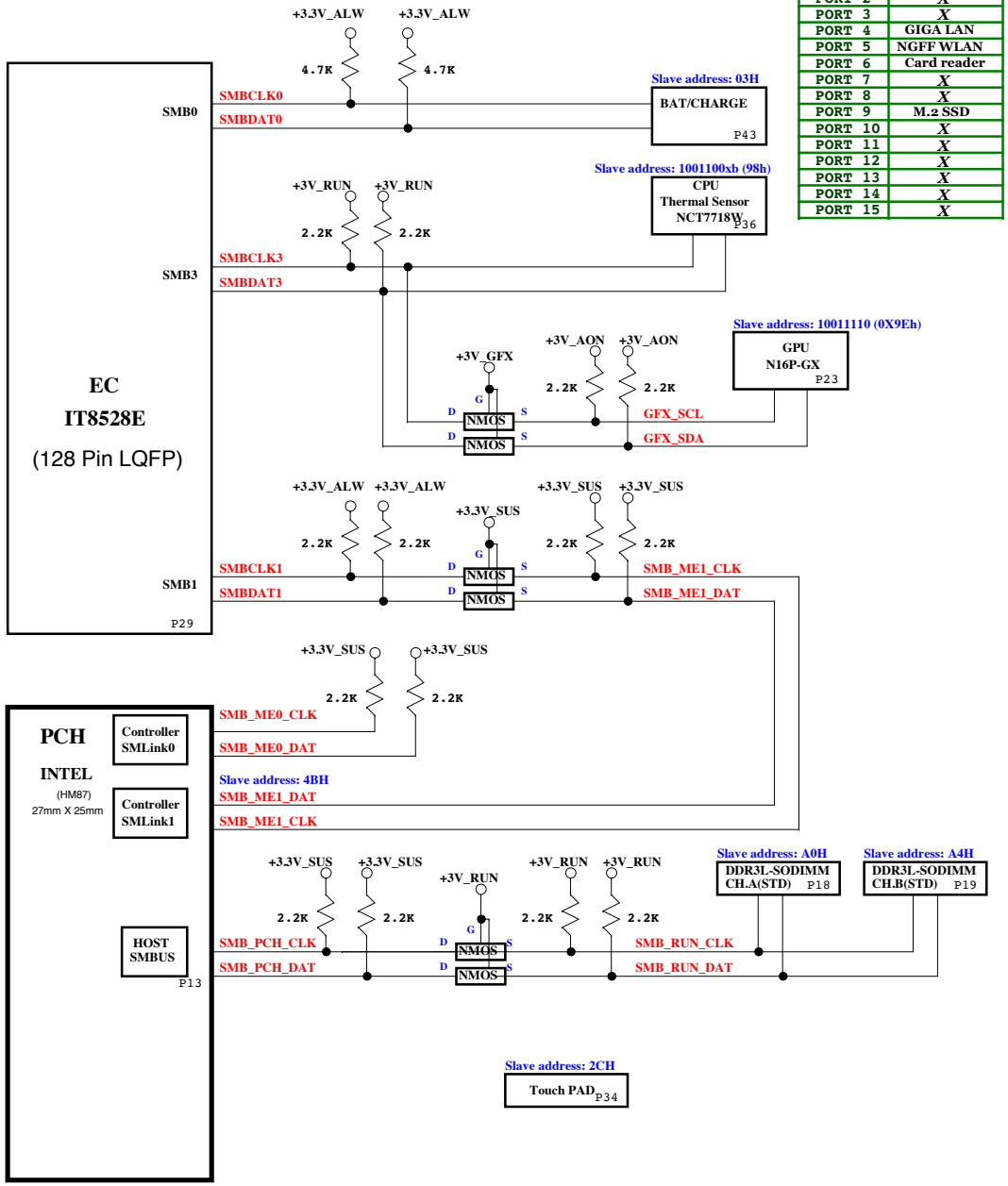
Quanta Computer Inc.		
PROJECT : AM9A		
Size	Document Number: 06 PS_G3 to S0	Rev: A0
Date: Wednesday, August 19, 2015	Sheet 53 of 57	

AM9A PSequence G3 to S0 Block (Battery mode)



Quanta Computer Inc.			
PROJECT : AM9A			
Size	Document Number		Rev
	PSeq_G3 to S0 Block_vPRO		A0
Date: Wednesday, August 19, 2015		Sheet 54 of 57	

SMBus Block



PCIe CLKOUT	
PORT 0	DGPU
PORT 1	X
PORT 2	X
PORT 3	X
PORT 4	GIGA LAN
PORT 5	NGFF WLAN
PORT 6	Card reader
PORT 7	X
PORT 8	X
PORT 9	M.2 SSD
PORT 10	X
PORT 11	X
PORT 12	X
PORT 13	X
PORT 14	X
PORT 15	X

HSIO Port	SKL H		AM9A
PORT 1	USB3.0 PORT1		USB 3.0 CONN MB(PS)
PORT 2	USB3.0 PORT2		USB 3.0 CONN DB
PORT 3	USB3.0 PORT3		USB 3.0 CONN DB
PORT 4	USB3.0 PORT4		X
PORT 5	USB3.0 PORT5		X
PORT 6	USB3.0 PORT6		X
PORT 7	USB3.0 PORT7	PCIe* Port 1	X
PORT 8	USB3.0 PORT8	PCIe* Port 2	X
PORT 9	USB3.0 PORT9	PCIe* Port 3	X
PORT10	USB3.0 PORT10	PCIe* Port 4	X
PORT11		PCIe* Port 5	GIGA LAN
PORT12		PCIe* Port 6	NGFF WLAN
PORT13		PCIe* Port 7	Card Reader
PORT14		PCIe* Port 8	X
PORT15	SATA 6Gb/s Port 0	PCIe* Port 9	M.2(NGFF)SSD
PORT16	SATA 6Gb/s Port 1	PCIe* Port10	
PORT17		PCIe* Port11	
PORT18		PCIe* Port12	
PORT19	SATA 6Gb/s Port 0	PCIe* Port13	SATA HDD
PORT20	SATA 6Gb/s Port 1	PCIe* Port14	X
PORT21	SATA 6Gb/s Port 2	PCIe* Port15	X
PORT22	SATA 6Gb/s Port 3	PCIe* Port16	X
PORT23	SATA 6Gb/s Port 4	PCIe* Port17	X
PORT24	SATA 6Gb/s Port 5	PCIe* Port18	X
PORT25		PCIe* Port19	X
PORT26		PCIe* Port20	X

USB 2.0			
EHCI #1		EHCI #2	
PORT 1	USB3.0 CONN/MB(PS)	PORT 9	X
PORT 2	USB3.0 Conn / DB	PORT 10	X
PORT 3	USB3.0 CONN / DB	PORT 11	X
PORT 4	Camera	PORT 12	X
PORT 5	BT	PORT 13	X
PORT 6	Touch Screen	PORT 14	X
PORT 7	X		
PORT 8	X		

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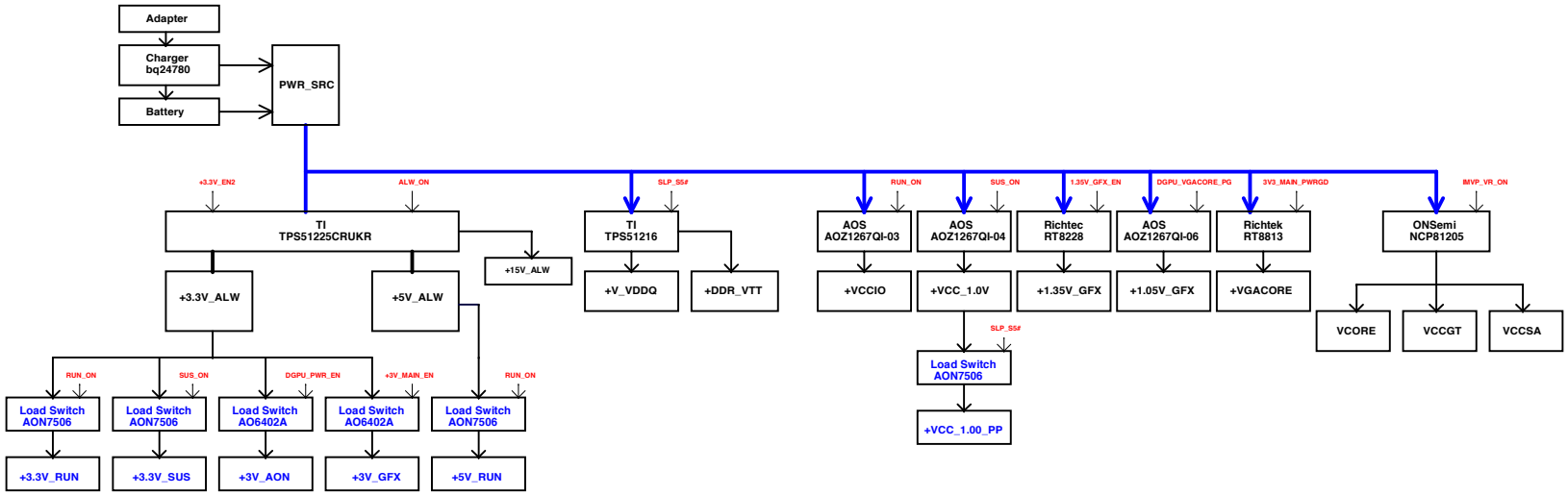
PROJECT : AM9A
Size | Document Number | Rev A0
SMBus Block
Date: Wednesday, August 19, 2015 | Sheet 55 of 57



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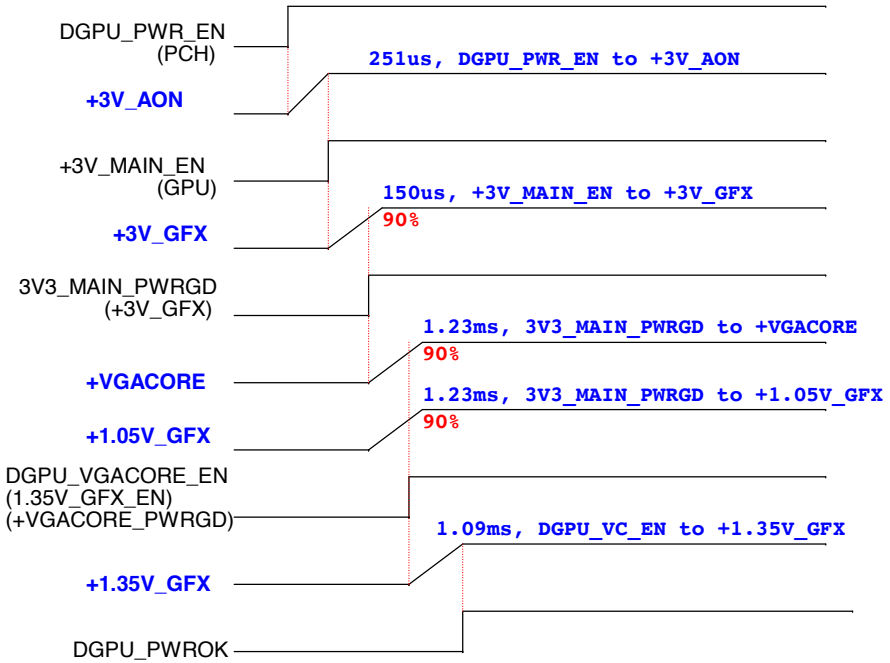
PROJECT : AM9A

Size | Document Number | Rev

Power Block Diagram | Cb

Date: Wednesday, August 19, 2015 | Sheet 56 of 57

AM9 GPU Power UP sequence

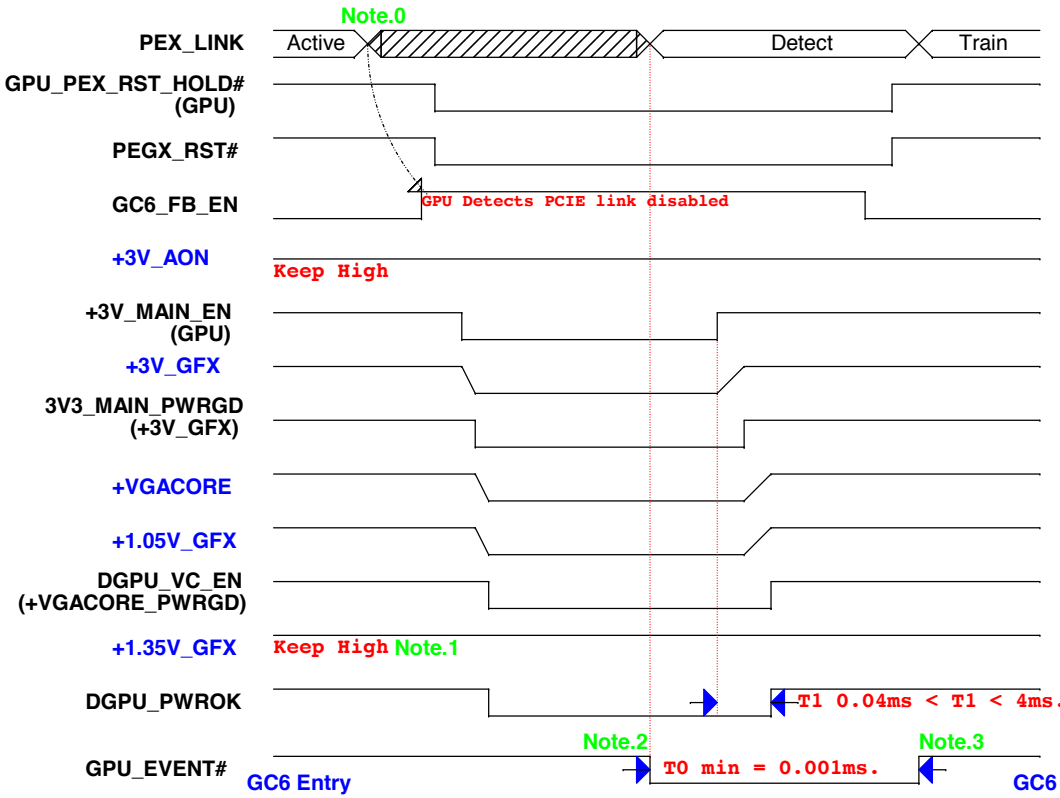


- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- A VDD33 must ramp up to 90% before NVVDD and PEXVDD in sequence can start ramping up. NVVDD must ramp up to 90% before FBVDD/Q in sequence can start ramping up

3.10.2.2 Power-Down Sequence

There is no specific power down sequence required. However, residual voltage from power down should not disrupt the power-up sequence when back to back GPU power-down and power-up take place.

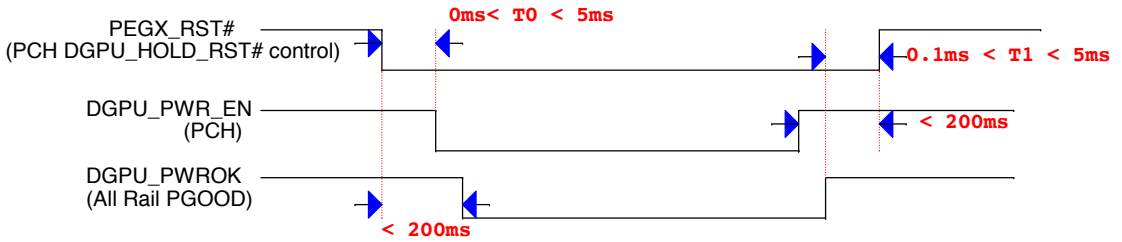
AM9 GPU GC62.0 Entry/Exit sequence



Note.0 : GPU driver ACPI call SBIOS to disables PCIE link.
Note.1 : When GC6 2.0 mode, +1.35V_GFX enabled by GC6_FB_EN
Note.2 : GPU driver ACPI call SBIOS then confirm entry complete by sensing GC6_FB_EN =1, Enable PCIE Link. Then PCH asserts GPU_EVENT#
Note.3 : SBIOS detects GC6_FB_EN =0, then De-asserts GPU_EVENT#
P.S. The entire entry and exit sequence must complete within 200 ms

AM9 Optimus GPU On/Off sequence

T0 = 220 us, PEGX_RST# to DGPU_PWR_EN
2.21 ms, DGPU_PWR_EN to DGPU_PWROK



P.S. The entire entry and exit sequence must complete within 200 ms

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PROJECT : AM9A
Size | Document Number: GPU Sequence | Rev A0
Date: Wednesday, August 19, 2015 | Sheet 57 of 57