MS-7877 Ver: 11 mini-ITX : 170 * 170 mm

SOC:

Intel - Bay Trail-D(J1750 Celeron)

OnBoard Chipset:

HD Audio Codec:ALC887VD

LAN:RTL 8106E 10/100 , Co-lay 8111G 10/100/1000

SIO:Fintek 71808A

Flash ROM: 64Mb SPI (SOC)

Main Memory:

DDRIII SO-DIMM(1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X1) Slot * 1

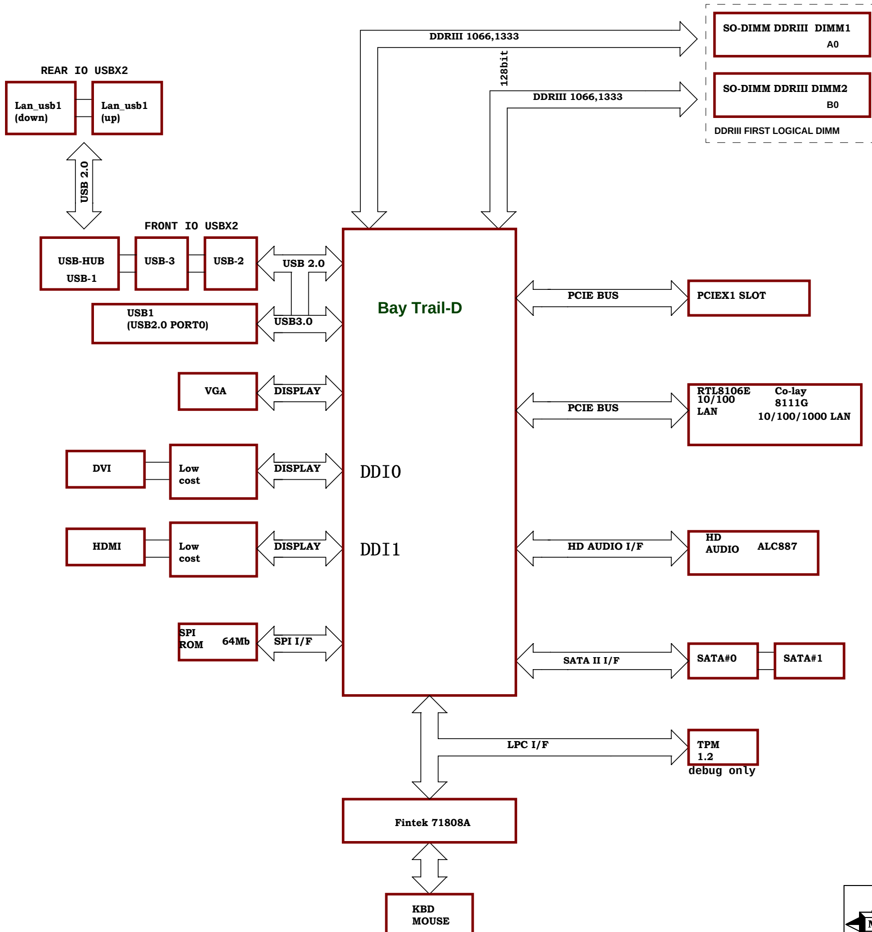
PWM:

CPU+GPU: Intersil / ISL95833 1+1 Phase
DDR: ISL6341 1-Phase
SOC V1P0S: MP2143

Other:

SATA2.0 x2
USB2.0 RearX2 Front x2
USB3.0 RearX1
D-SUB/DVI*1/HDMI*1
TPM Header *1

INTEL CONFIDENTIAL



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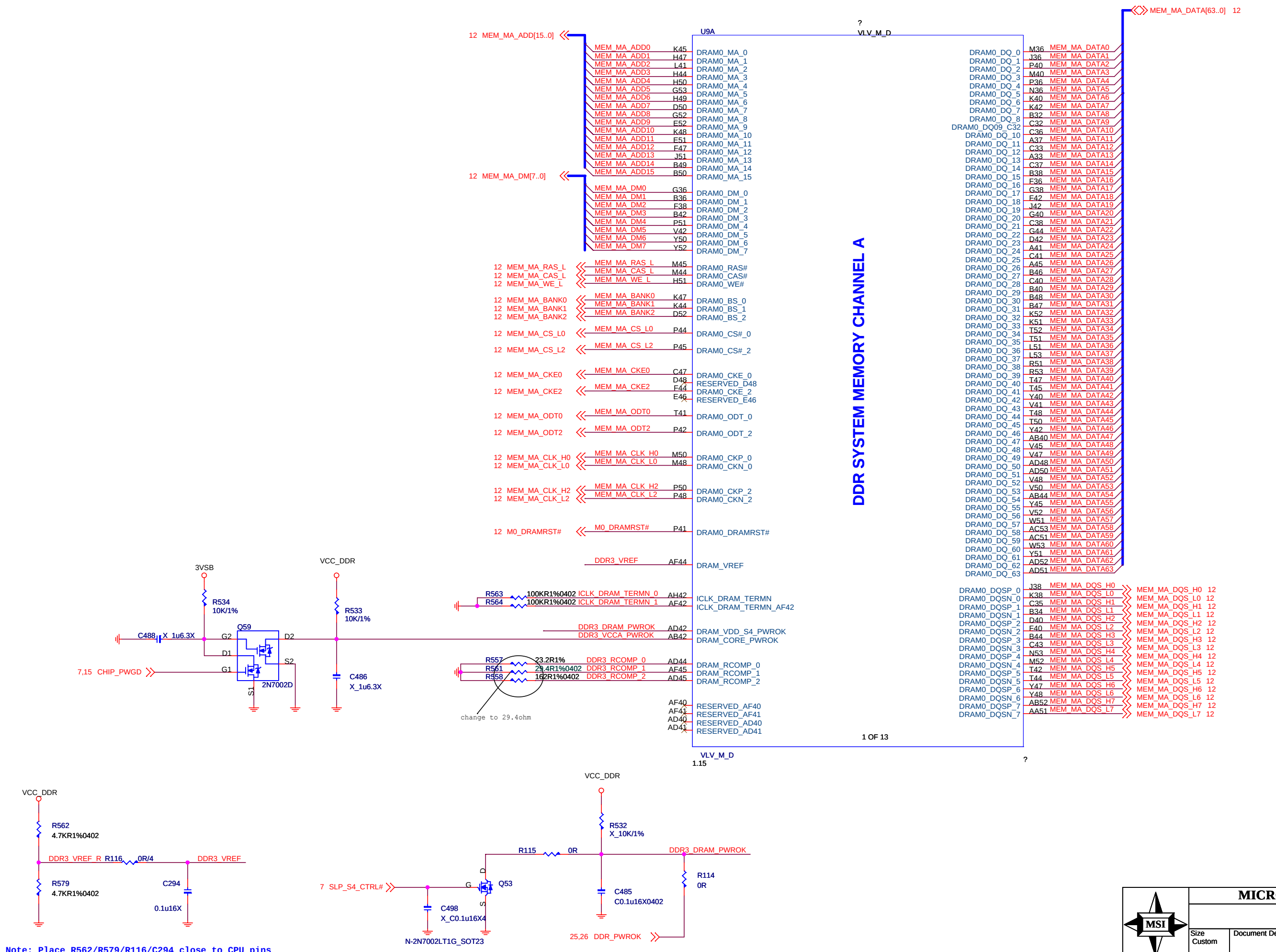
MS-7877		
Size: Custom	Document Description: Block Diagram	Rev: 11
Date: Thursday, November 14, 2013	Sheet 2 of 33	

SOC -1 DDR0



Note: Place R562/R579/R116/C294 close to CPU pins

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Custom	SOC - DIMM	11

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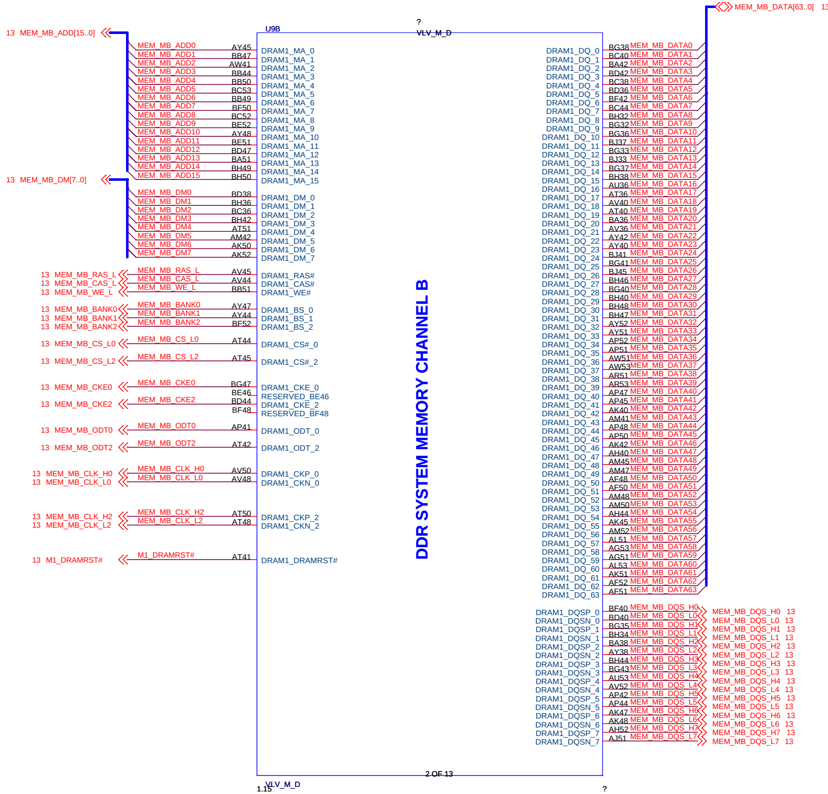
SOC -2 DDR1



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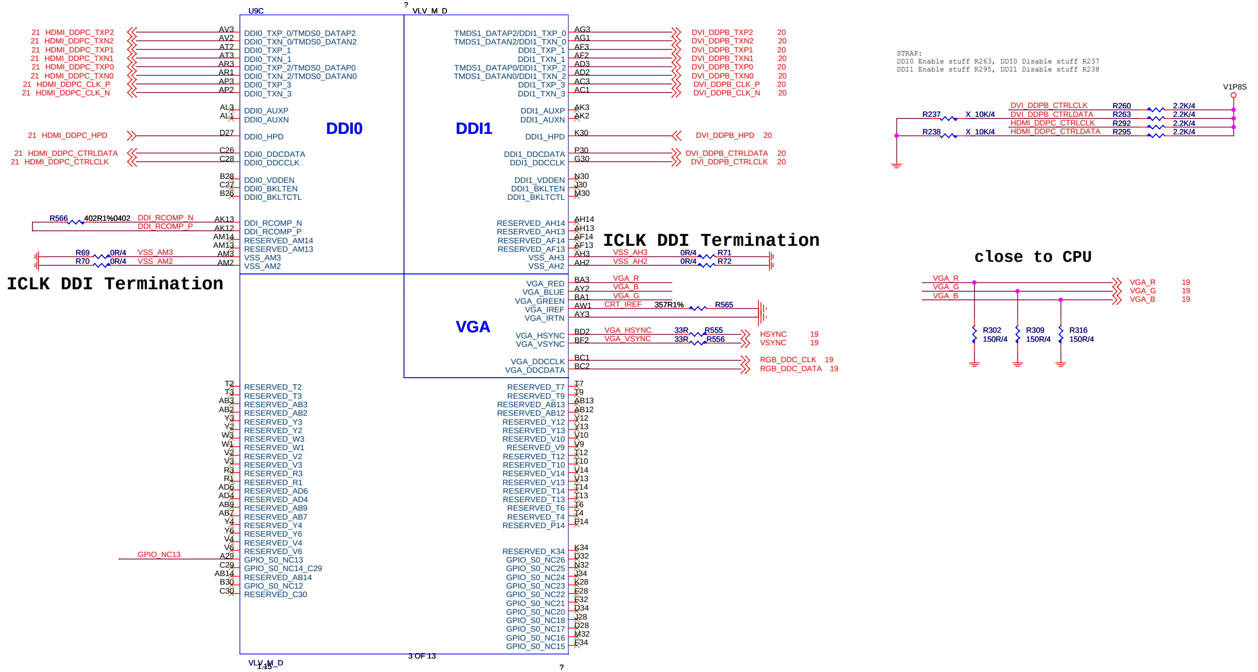
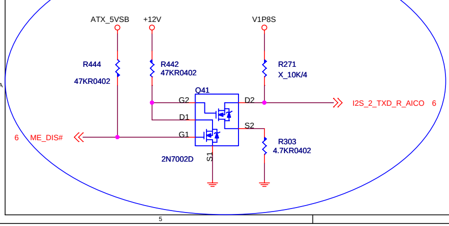
Size: Custom	Document Description: SOC - DIMM	Rev: 11
Date: Thursday, November 14, 2013	Sheet 4 of 33	

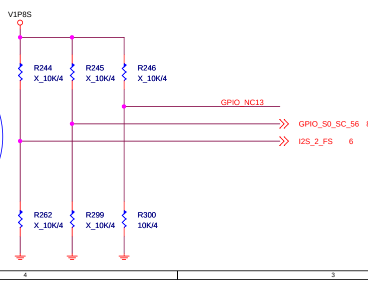
- DDCDATA must be routed same length or longer than DDCCLK within 1000 mils (25.4 mm). The total delay on DDCDATA should be longer than DDCCLK.



SOC Strap

ver 1.0 add txe disable circuit by gpio control.



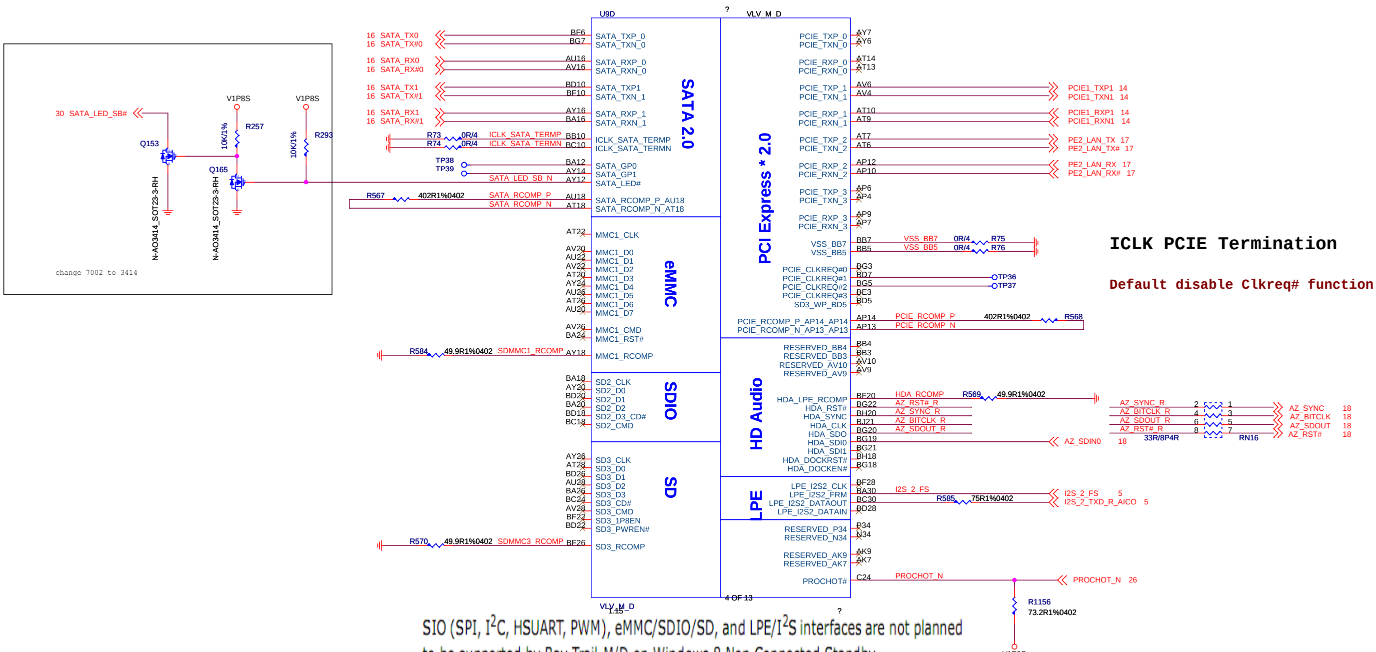


2.25 Hardware Straps

All straps are sampled on the rising edge of PMC_CORE_PWROK.

Table 36. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[056]	Legacy	1b	PMC_CORE_PWROK de-asserted	Top Swap (A16 Override) 0 = Top address bit is unchanged 1 = Top address bit is inverted
GPIO_S0_SC[063]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[065]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected



SIO (SPI, I²C, HSUART, PWM), eMMC/SDIO/SD, and LPE/I²S interfaces are not planned to be supported by Bay Trail-M/D on Windows 8 Non Connected Standby.

ICLK PCIE Termination

Default disable Clkreq# function.

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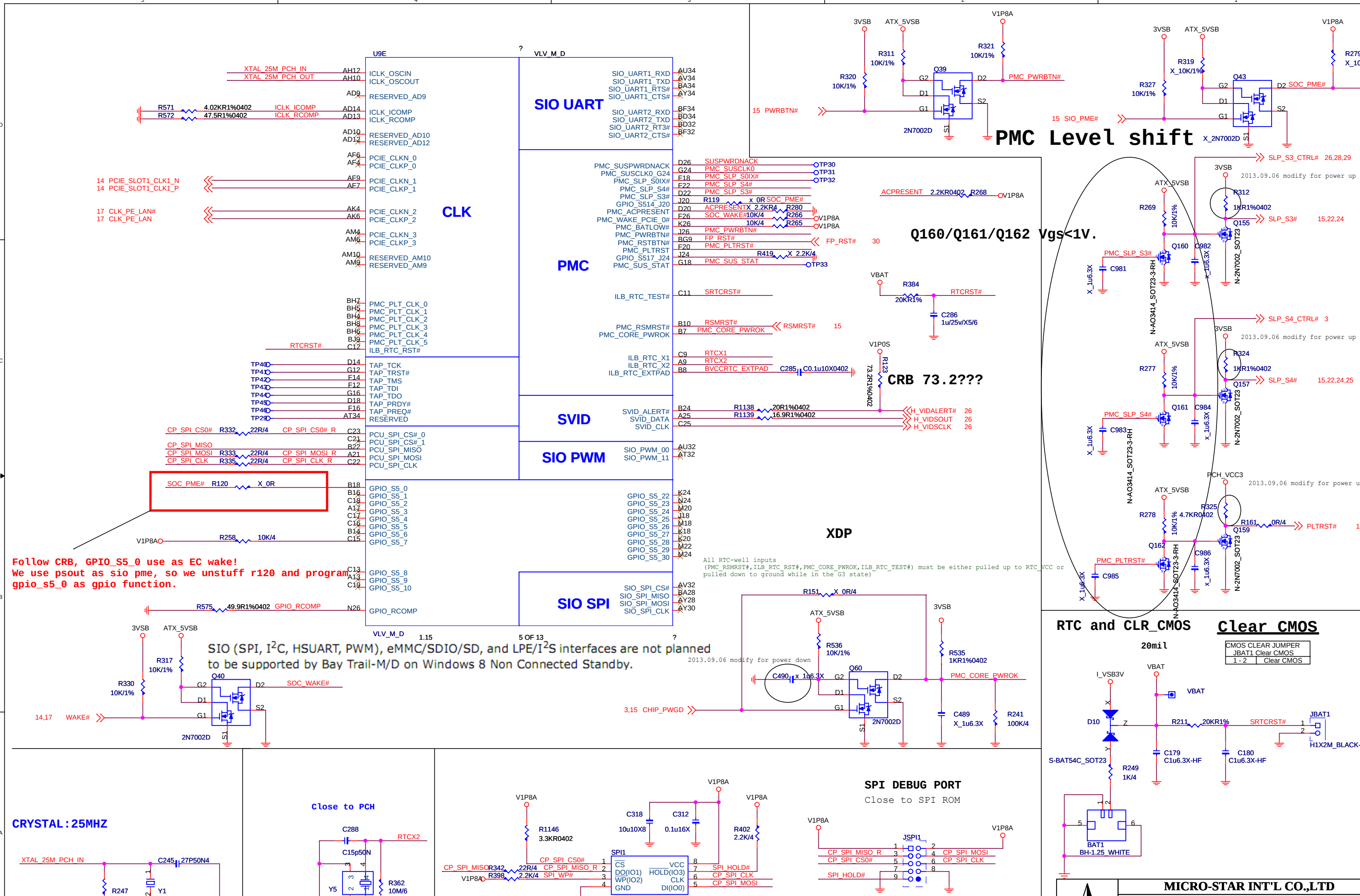

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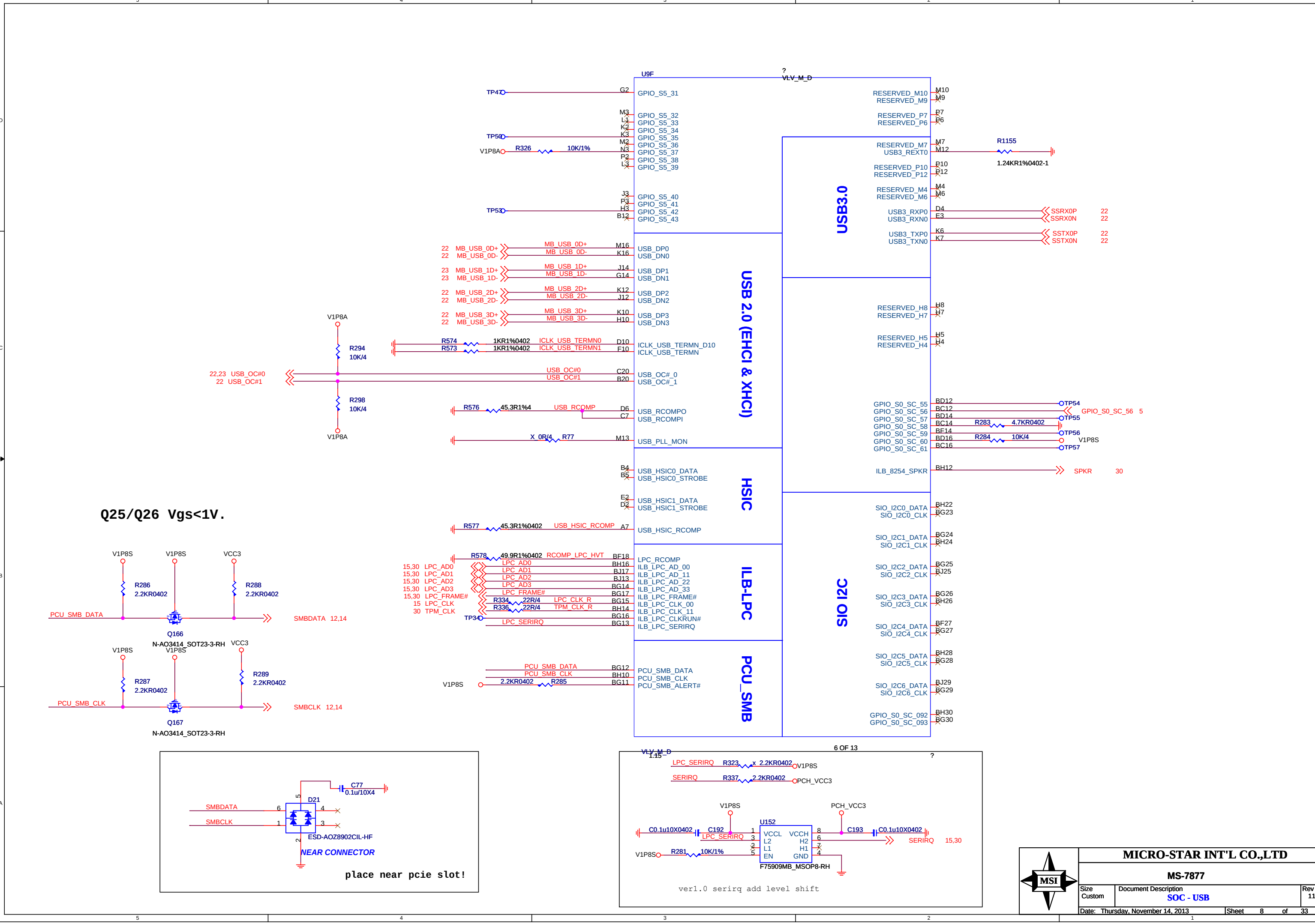
Size	Document Description	Rev
Custom	SOC - CLK	11

Date: Thursday, November 14, 2013 Sheet 7 of 33



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Size	Document Description	Rev
Custom	SOC - USB	11

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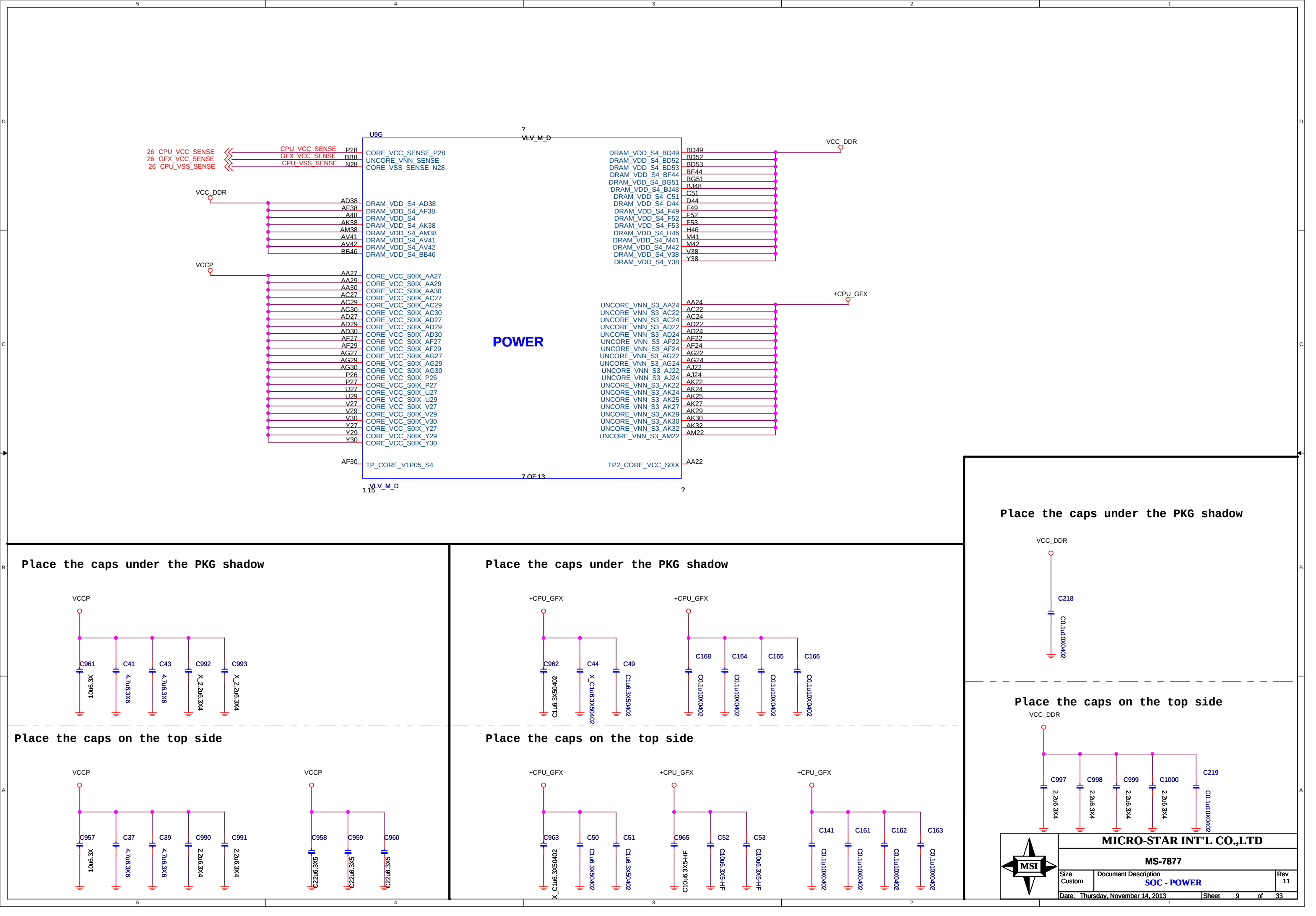
U9G
VLV_M_D
POWER
7 OF 13
26 CPU_VCC_SENSE
26 GFX_VCC_SENSE
26 CPU_VSS_SENSE
CPU_VCC_SENSE P28 CORE_VCC_SENSE_P28
GFX_VCC_SENSE BB8 UNCORE_VNN_SENSE
CPU_VSS_SENSE N28 CORE_VSS_SENSE_N28
VCC_DDR
AD38 DRAM_VDD_S4_AD38
AF38 DRAM_VDD_S4_AF38
A48 DRAM_VDD_S4
AK38 DRAM_VDD_S4_AK38
AM38 DRAM_VDD_S4_AM38
AV41 DRAM_VDD_S4_AV41
AV42 DRAM_VDD_S4_AV42
BB46 DRAM_VDD_S4_BB46
VCCP
AA27 CORE_VCC_S0IX_AA27
AA29 CORE_VCC_S0IX_AA29
AA30 CORE_VCC_S0IX_AA30
AC27 CORE_VCC_S0IX_AC27
AC29 CORE_VCC_S0IX_AC29
AC30 CORE_VCC_S0IX_AC30
AD27 CORE_VCC_S0IX_AD27
AD29 CORE_VCC_S0IX_AD29
AD30 CORE_VCC_S0IX_AD30
AF27 CORE_VCC_S0IX_AF27
AF29 CORE_VCC_S0IX_AF29
AG27 CORE_VCC_S0IX_AG27
AG29 CORE_VCC_S0IX_AG29
AG30 CORE_VCC_S0IX_AG30
P26 CORE_VCC_S0IX_P26
P27 CORE_VCC_S0IX_P27
U27 CORE_VCC_S0IX_U27
U29 CORE_VCC_S0IX_U29
V27 CORE_VCC_S0IX_V27
V29 CORE_VCC_S0IX_V29
V30 CORE_VCC_S0IX_V30
Y27 CORE_VCC_S0IX_Y27
Y29 CORE_VCC_S0IX_Y29
Y30 CORE_VCC_S0IX_Y30
AF30 TP_CORE_V1P05_S4
DRAM_VDD_S4_BD49 BD49
DRAM_VDD_S4_BD52 BD52
DRAM_VDD_S4_BD53 BD53
DRAM_VDD_S4_BF44 BF44
DRAM_VDD_S4_BG51 BG51
DRAM_VDD_S4_BJ48 BJ48
DRAM_VDD_S4_C51 C51
DRAM_VDD_S4_D44 D44
DRAM_VDD_S4_F49 F49
DRAM_VDD_S4_F52 F52
DRAM_VDD_S4_F53 F53
DRAM_VDD_S4_H46 H46
DRAM_VDD_S4_M41 M41
DRAM_VDD_S4_M42 M42
DRAM_VDD_S4_V38 V38
DRAM_VDD_S4_Y38 Y38
+CPU_GFX
UNCORE_VNN_S3_AA24 AA24
UNCORE_VNN_S3_AC22 AC22
UNCORE_VNN_S3_AC24 AC24
UNCORE_VNN_S3_AD22 AD22
UNCORE_VNN_S3_AD24 AD24
UNCORE_VNN_S3_AF22 AF22
UNCORE_VNN_S3_AF24 AF24
UNCORE_VNN_S3_AG22 AG22
UNCORE_VNN_S3_AG24 AG24
UNCORE_VNN_S3_AJ22 AJ22
UNCORE_VNN_S3_AJ24 AJ24
UNCORE_VNN_S3_AK22 AK22
UNCORE_VNN_S3_AK24 AK24
UNCORE_VNN_S3_AK25 AK25
UNCORE_VNN_S3_AK27 AK27
UNCORE_VNN_S3_AK29 AK29
UNCORE_VNN_S3_AK30 AK30
UNCORE_VNN_S3_AK32 AK32
UNCORE_VNN_S3_AM22 AM22
TP2_CORE_VCC_S0IX AA22
Place the caps under the PKG shadow
VCCP
C961 10u6.3X
C41 4.7u6.3X6
C43 4.7u6.3X6
C992 X_2.2u6.3X4
C993 X_2.2u6.3X4
Place the caps on the top side
VCCP
C957 10u6.3X
C37 4.7u6.3X6
C39 4.7u6.3X6
C990 2.2u6.3X4
C991 2.2u6.3X4
VCCP
C958 C22u6.3X5
C959 C22u6.3X5
C960 C22u6.3X5
Place the caps under the PKG shadow
+CPU_GFX
C962 C1u6.3X50402
C44 X_C1u6.3X50402
C49 C1u6.3X50402
+CPU_GFX
C168 C0.1u10X0402
C164 C0.1u10X0402
C165 C0.1u10X0402
C166 C0.1u10X0402
Place the caps on the top side
+CPU_GFX
C963 X_C1u6.3X50402
C50 C1u6.3X50402
C51 C1u6.3X50402
+CPU_GFX
C965 C10u6.3X5-HF
C52 C10u6.3X5-HF
C53 C10u6.3X5-HF
+CPU_GFX
C141 C0.1u10X0402
C161 C0.1u10X0402
C162 C0.1u10X0402
C163 C0.1u10X0402
Place the caps under the PKG shadow
VCC_DDR
C218 C0.1u10X0402
Place the caps on the top side
VCC_DDR
C997 2.2u6.3X4
C998 2.2u6.3X4
C999 2.2u6.3X4
C1000 2.2u6.3X4
C219 C0.1u10X0402
MSI
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MS-7877
Size Custom
Document Description
SOC - POWER
Rev 11
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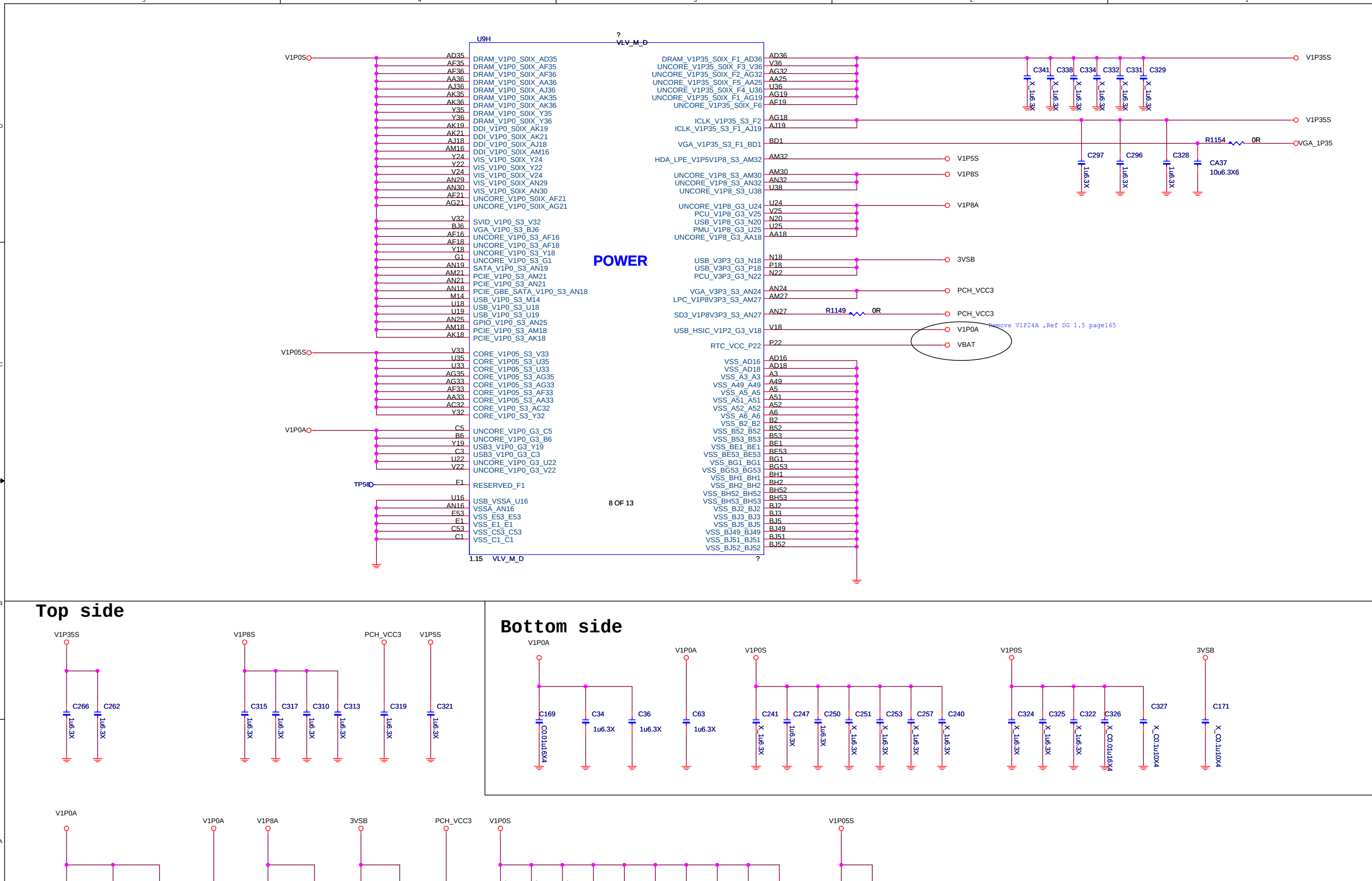
Sheet 9 of 33



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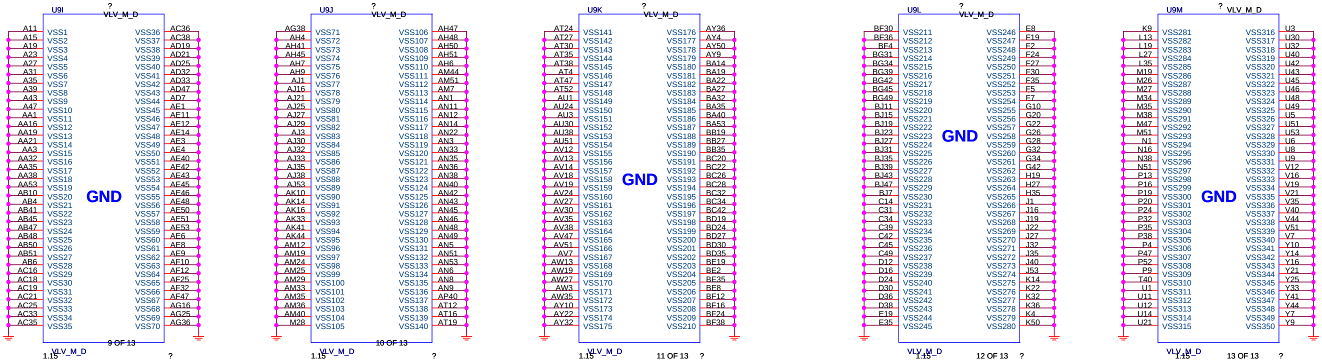

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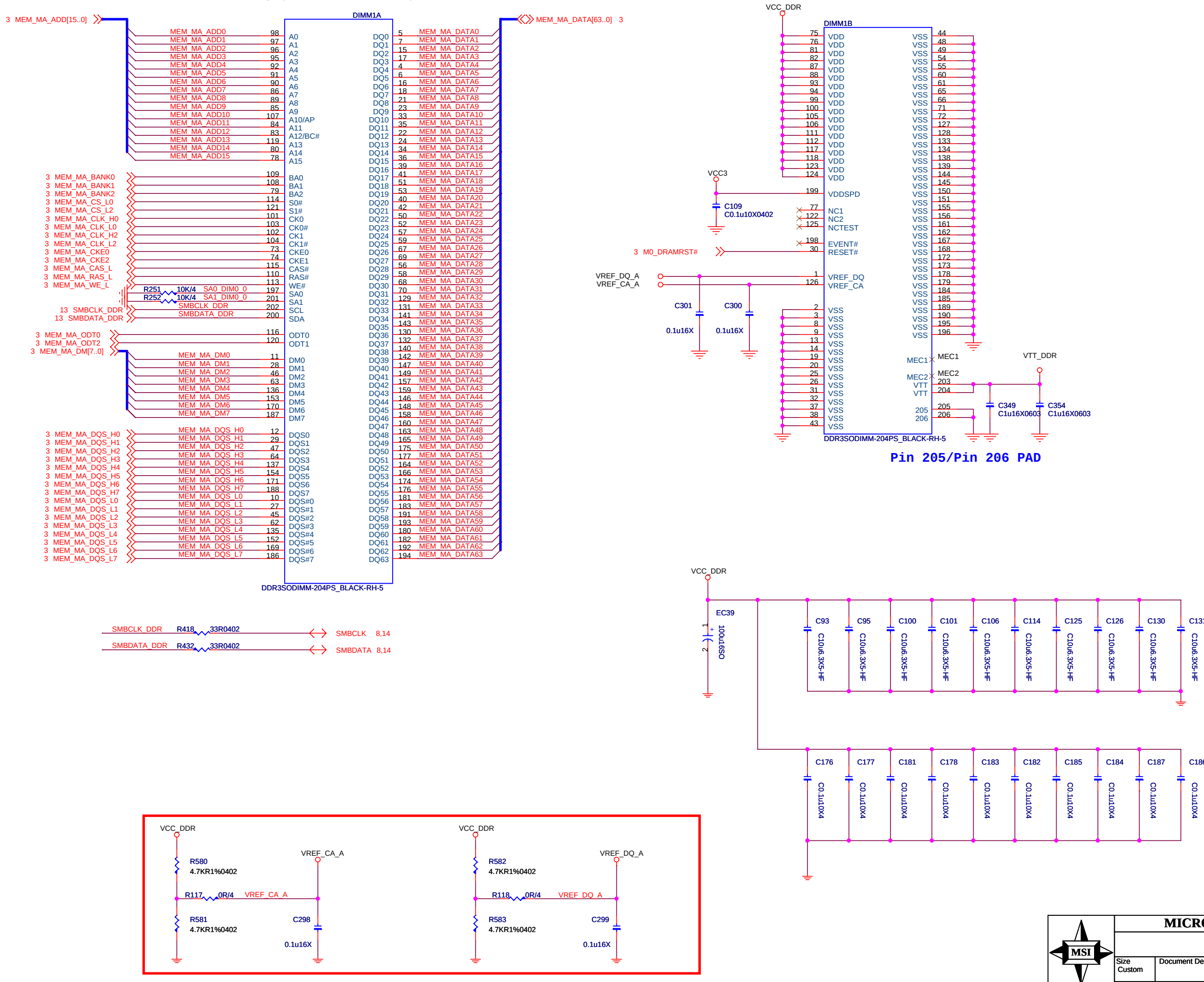
SODIMM #A0 (STD) N13-2040080-L41 9.2H



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Size: Custom	Document Description: DIMM Channel A		Rev: 11
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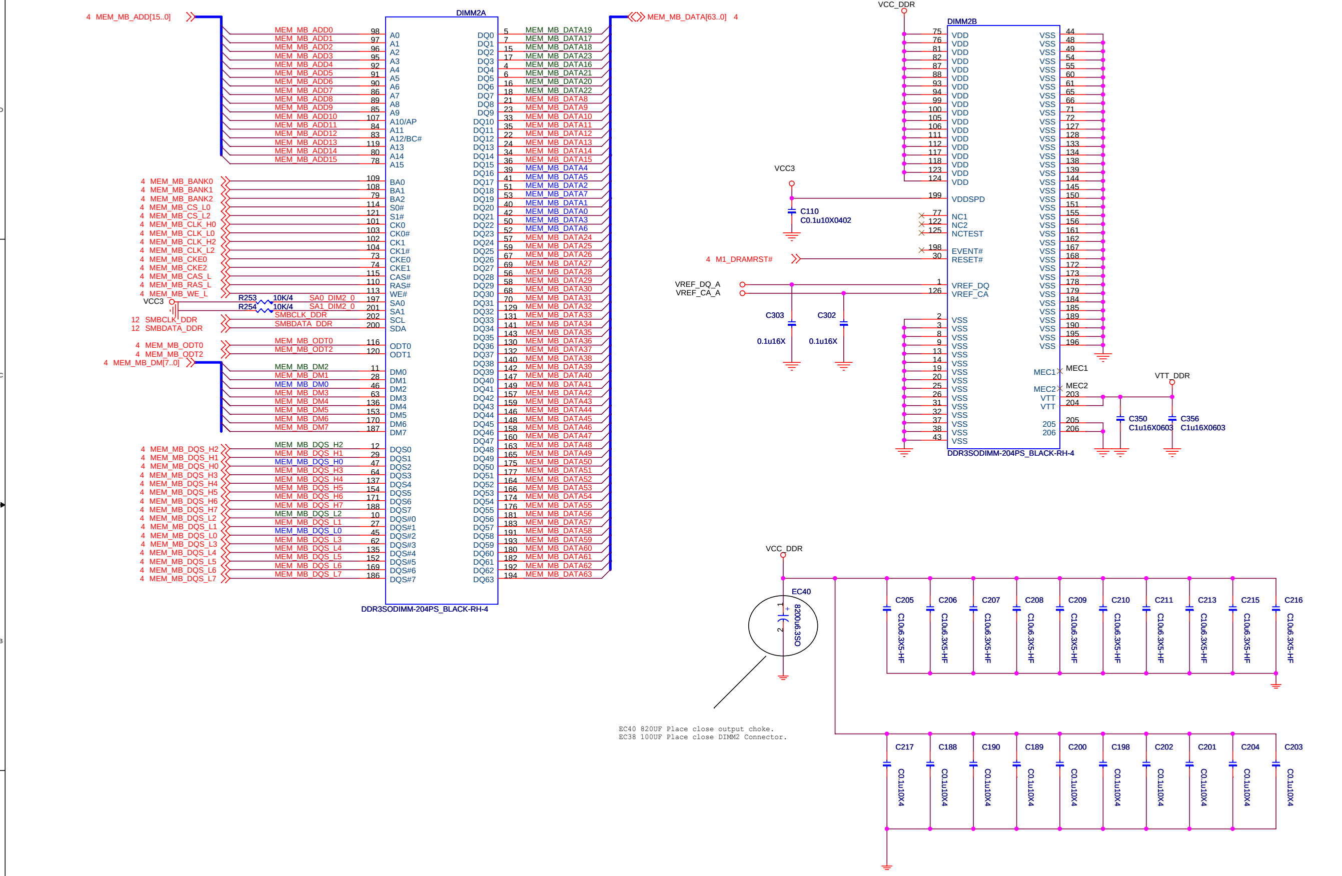
SODIMM #A2 (Reverse) N13-2040070-L41 9.2H



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Size: Custom	Document Description: DIMM Channel B		Rev: 11
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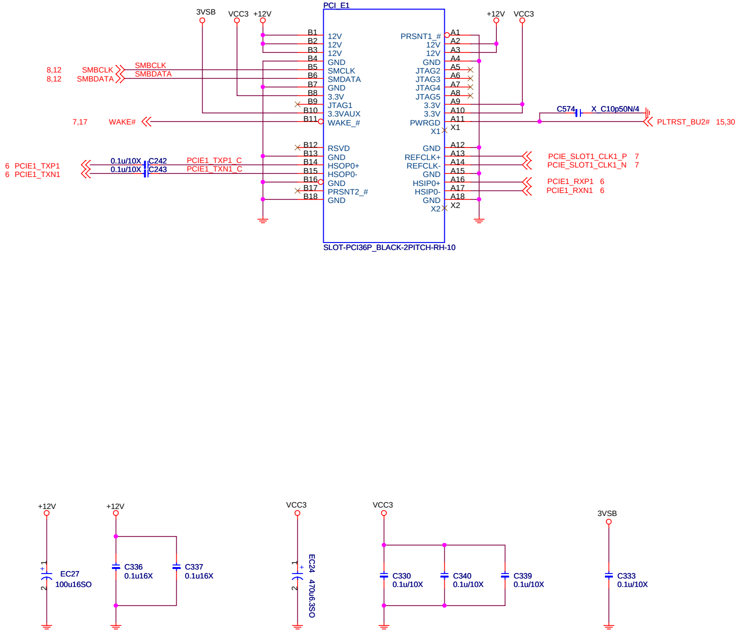
PCI EXPRESS x1-PORT



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Size: Custom	Document Description: PCIE X1 SLOT	Rev: 11
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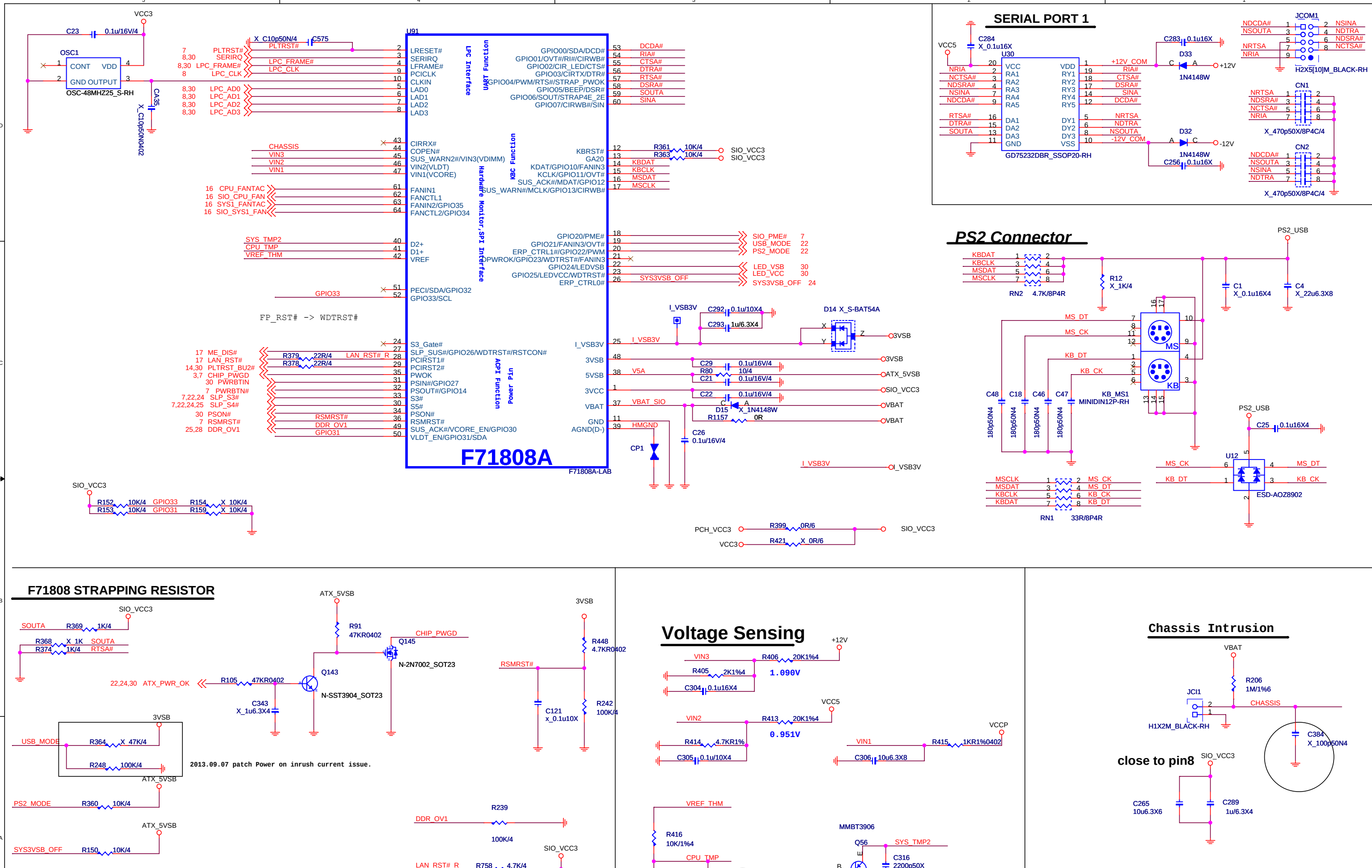

PIN	Function	NET Name	HI	LO
59	STRAP4E_2E	SOUTA	4E(DEFAUL)	2E
57	STRAP_PWOK	RTSA#	AMD (DEFAUL)	INTEL

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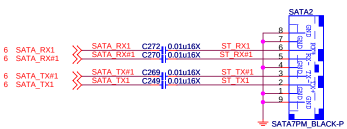
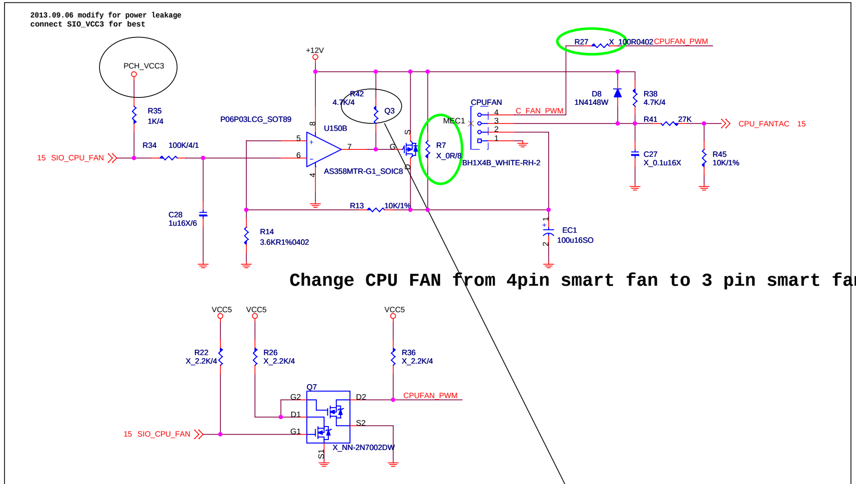
SATA 3G

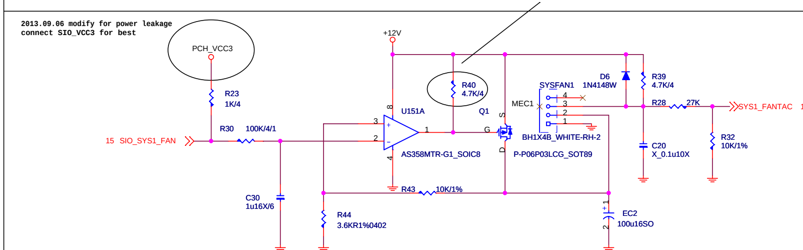
SATA1,SATA2



FAN-COUNTROL CIRCUIT



Fix next version



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	MS-7877		
	Size: Custom	Document Description: SATA & FAN	Rev: 11
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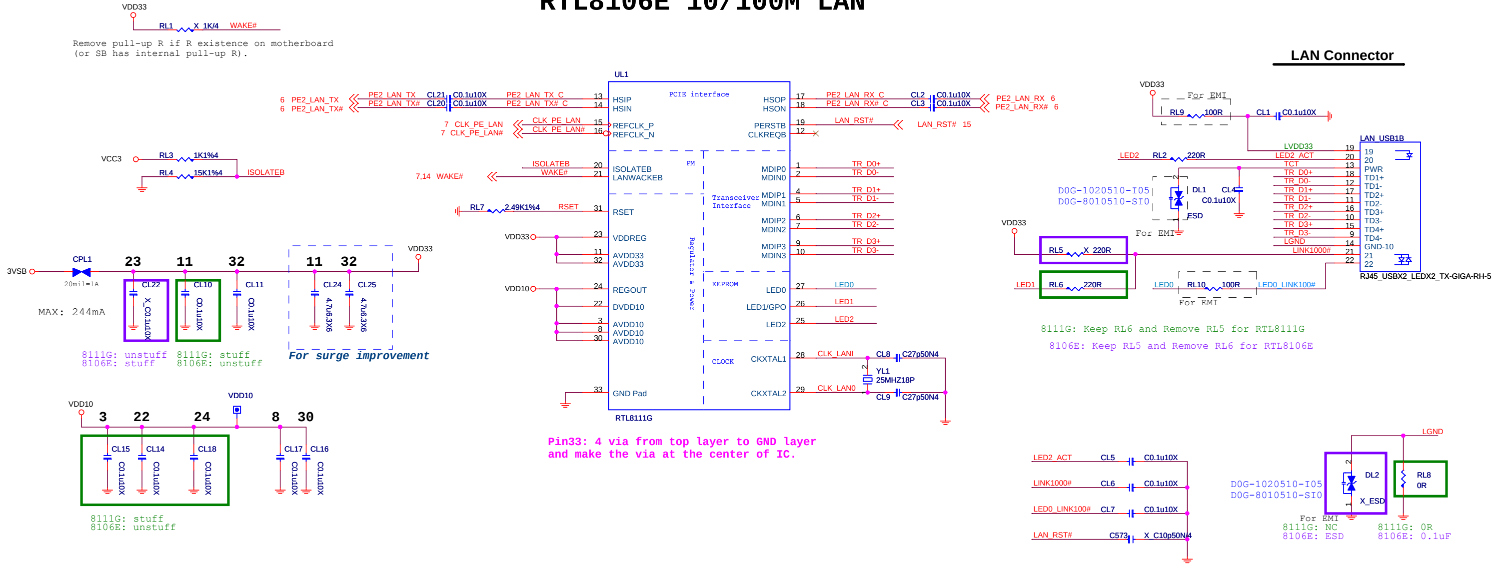
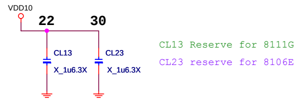
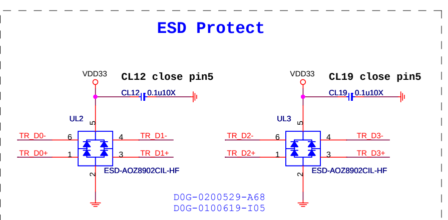
RTL8111G Giga LAN

RTL8106E 10/100M LAN







8106E POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	15/94	49.5/310.2
100 M Idle/TxRx	52/105	171.6/346.5
S0 ALDPS	4	13.2

8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

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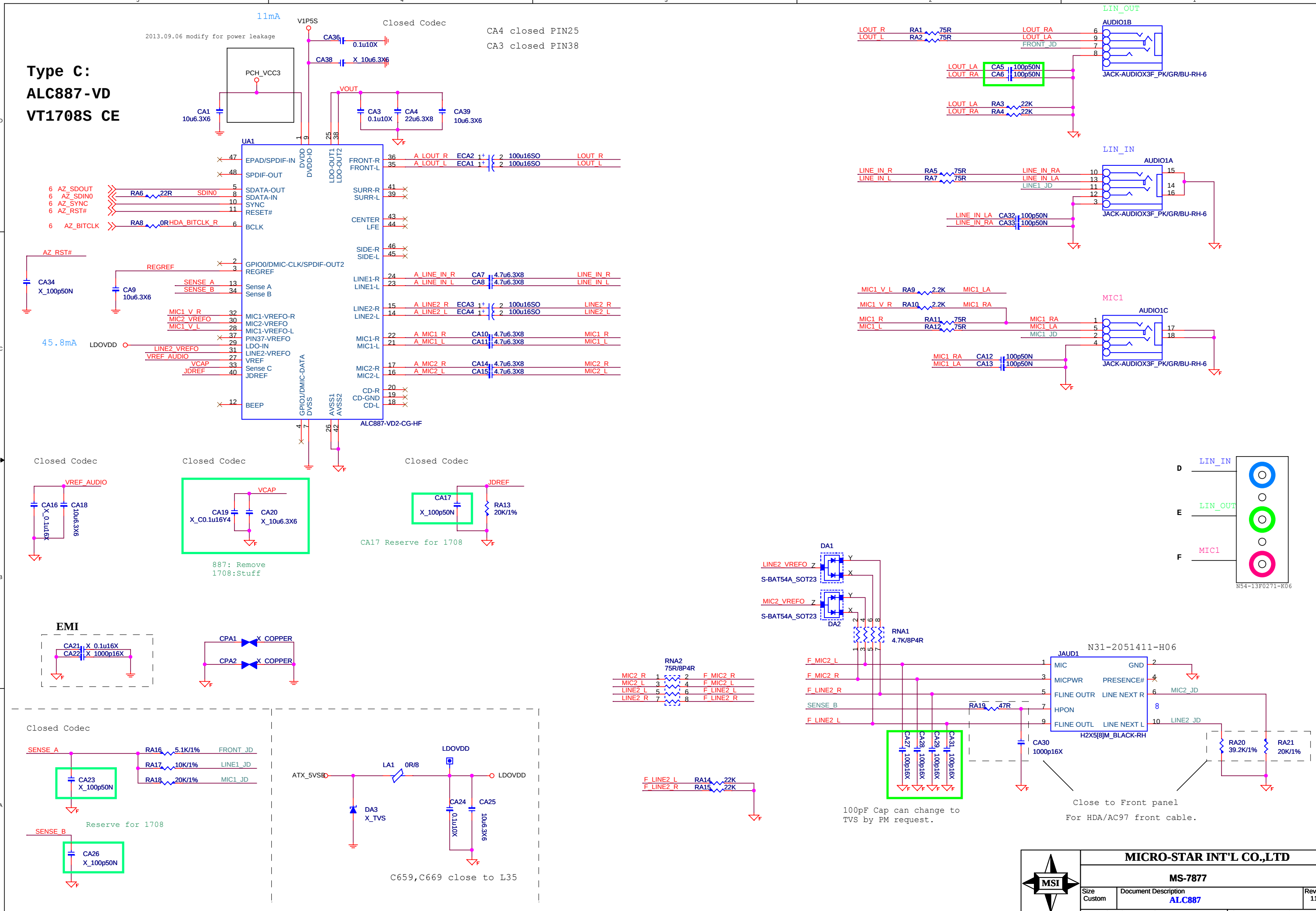
Size: Custom | Document Description: LAN-RTL8111G & 8106E | Rev: 11


Type C:
ALC887-VD
VT1708S CE
11mA
2013.09.06 modify for power leakage
V1P5S
Closed Codec
CA4 closed PIN25
CA3 closed PIN38
CA36 0.1u10X
CA38 X_10u6.3X6
PCH_VCC3
CA1 10u6.3X6
VOUT
CA3 0.1u10X
CA4 22u6.3X8
CA39 10u6.3X6
UA1
EPAD/SPDIF-IN
SPDIF-OUT
SDATA-OUT
SDATA-IN
SYNC
RESET#
BCLK
DVDD
DVDD-IO
LDO-OUT1
LDO-OUT2
FRONT-R
FRONT-L
SURR-R
SURR-L
CENTER
LFE
SIDE-R
SIDE-L
LINE1-R
LINE1-L
LINE2-R
LINE2-L
MIC1-R
MIC1-L
MIC2-R
MIC2-L
CD-R
CD-GND
CD-L
GPIO0/DMIC-CLK/SPDIF-OUT2
REGREF
Sense A
Sense B
MIC1-VREFO-R
MIC2-VREFO
MIC1-VREFO-L
PIN37-VREFO
LDO-IN
LINE2-VREFO
VREF
Sense C
JDREF
BEEP
GPIO1/DMIC-DATA
DVSS
AVSS1
AVSS2
ALC887-VD2-CG-HF
6 AZ_SDOUT
6 AZ_SDIN0
6 AZ_SYNC
6 AZ_RST#
6 AZ_BITCLK
RA6 22R SDIN0
RA8 0R HDA_BITCLK_R
AZ_RST#
CA34 X_100p50N
REGREF
CA9 10u6.3X6
SENSE_A
SENSE_B
MIC1_V_R
MIC2_VREFO
MIC1_V_L
45.8mA
LDOVDD
LINE2_VREFO
VREF_AUDIO
VCAP
JDREF
A_LOUT_R ECA2 100u16SO LOUT_R
A_LOUT_L ECA1 100u16SO LOUT_L
A_LINE_IN_R CA7 4.7u6.3X8 LINE_IN_R
A_LINE_IN_L CA8 4.7u6.3X8 LINE_IN_L
A_LINE2_R ECA3 100u16SO LINE2_R
A_LINE2_L ECA4 100u16SO LINE2_L
A_MIC1_R CA10 4.7u6.3X8 MIC1_R
A_MIC1_L CA11 4.7u6.3X8 MIC1_L
A_MIC2_R CA14 4.7u6.3X8 MIC2_R
A_MIC2_L CA15 4.7u6.3X8 MIC2_L
LIN_OUT
AUDIO1B
LOUT_R RA1 75R LOUT_RA
LOUT_L RA2 75R LOUT_LA
FRONT_JD
LOUT_LA CA5 100p50N
LOUT_RA CA6 100p50N
JACK-AUDIOX3F_PK/GR/BU-RH-6
LOUT_LA RA3 22K
LOUT_RA RA4 22K
LIN_IN
AUDIO1A
LINE_IN_R RA5 75R LINE_IN_RA
LINE_IN_L RA7 75R LINE_IN_LA
LINE1_JD
LINE_IN_LA CA32 100p50N
LINE_IN_RA CA33 100p50N
MIC1_V_L RA9 2.2K MIC1_LA
MIC1_V_R RA10 2.2K MIC1_RA
MIC1
AUDIO1C
MIC1_R RA11 75R MIC1_RA
MIC1_L RA12 75R MIC1_LA
MIC1_JD
MIC1_RA CA12 100p50N
MIC1_LA CA13 100p50N
Closed Codec
VREF_AUDIO
CA16 X_0.1u16X
CA18 10u6.3X6
VCAP
CA19 X_C0.1u16Y4
CA20 X_10u6.3X6
887: Remove
1708:Stuff
JDREF
CA17 X_100p50N
RA13 20K/1%
CA17 Reserve for 1708
D LIN_IN
E LIN_OUT
F MIC1
N54-13F0271-K06
DA1
LINE2_VREFO
S-BAT54A_SOT23
DA2
MIC2_VREFO
S-BAT54A_SOT23
RNA1 4.7K/8P4R
EMI
CA21 X_0.1u16X
CA22 X_1000p16X
CPA1 X_COPPER
CPA2 X_COPPER
RNA2 75R/8P4R
MIC2_R F_MIC2_R
MIC2_L F_MIC2_L
LINE2_L F_LINE2_L
LINE2_R F_LINE2_R
N31-2051411-H06
JAUD1
F_MIC2_L MIC
F_MIC2_R MICPWR
F_LINE2_R FLINE OUTR
SENSE_B RA19 47R HPON
F_LINE2_L FLINE OUTL
GND
PRESENCE#
LINE NEXT R MIC2_JD
LINE NEXT L LINE2_JD
H2X5[8]M_BLACK-RH
CA27 100p16X
CA28 100p16X
CA29 100p16X
CA31 100p16X
CA30 1000p16X
RA20 39.2K/1%
RA21 20K/1%
100pF Cap can change to
TVS by PM request.
Close to Front panel
For HDA/AC97 front cable.
Closed Codec
SENSE_A
RA16 5.1K/1% FRONT_JD
RA17 10K/1% LINE1_JD
RA18 20K/1% MIC1_JD
CA23 X_100p50N
Reserve for 1708
SENSE_B
CA26 X_100p50N
ATX_5VSB
LA1 0R/8
LDOVDD
DA3 X_TVS
CA24 0.1u10X
CA25 10u6.3X6
C659,C669 close to L35
F_LINE2_L RA14 22K
F_LINE2_R RA15 22K
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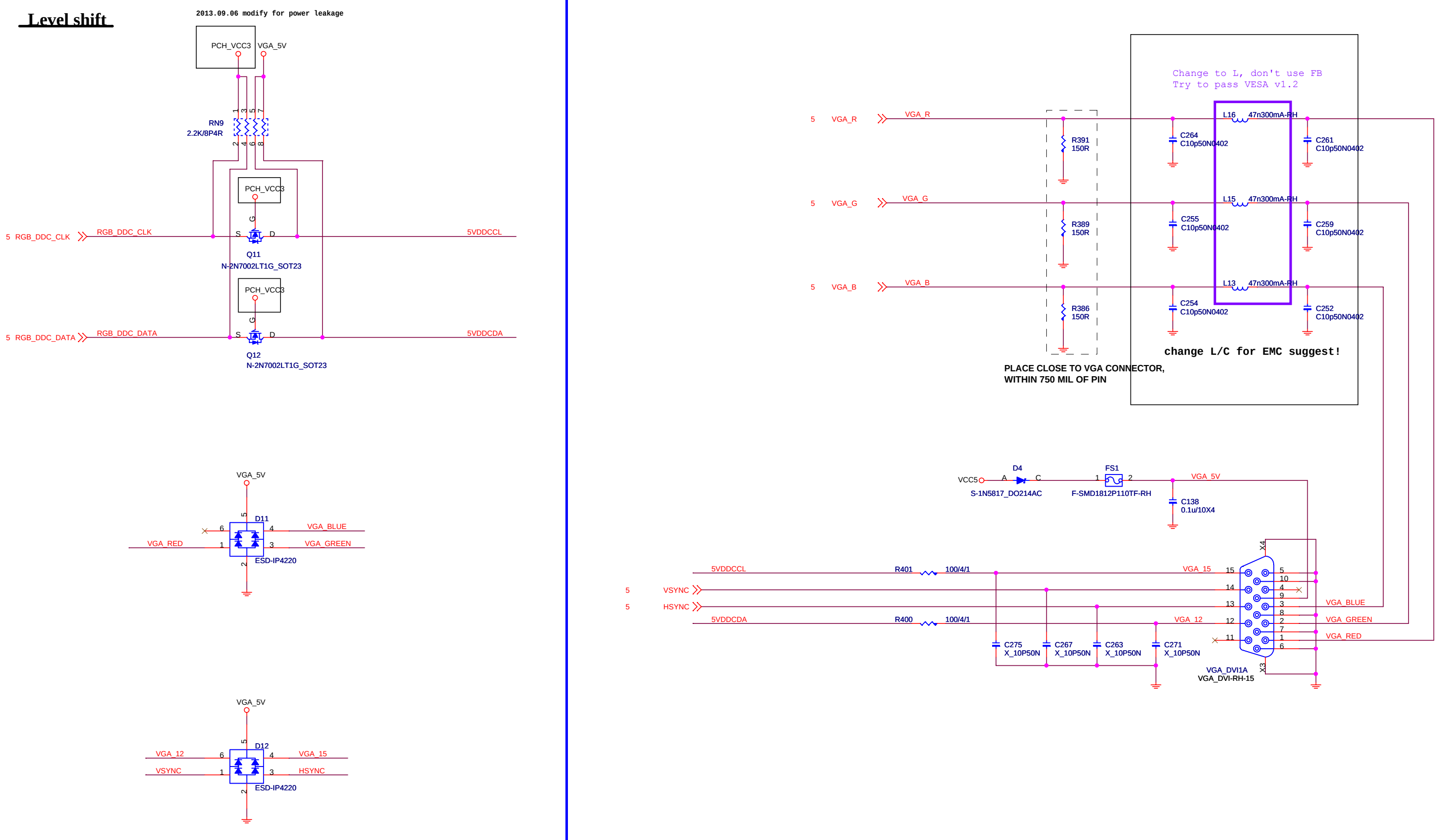
D-Sub



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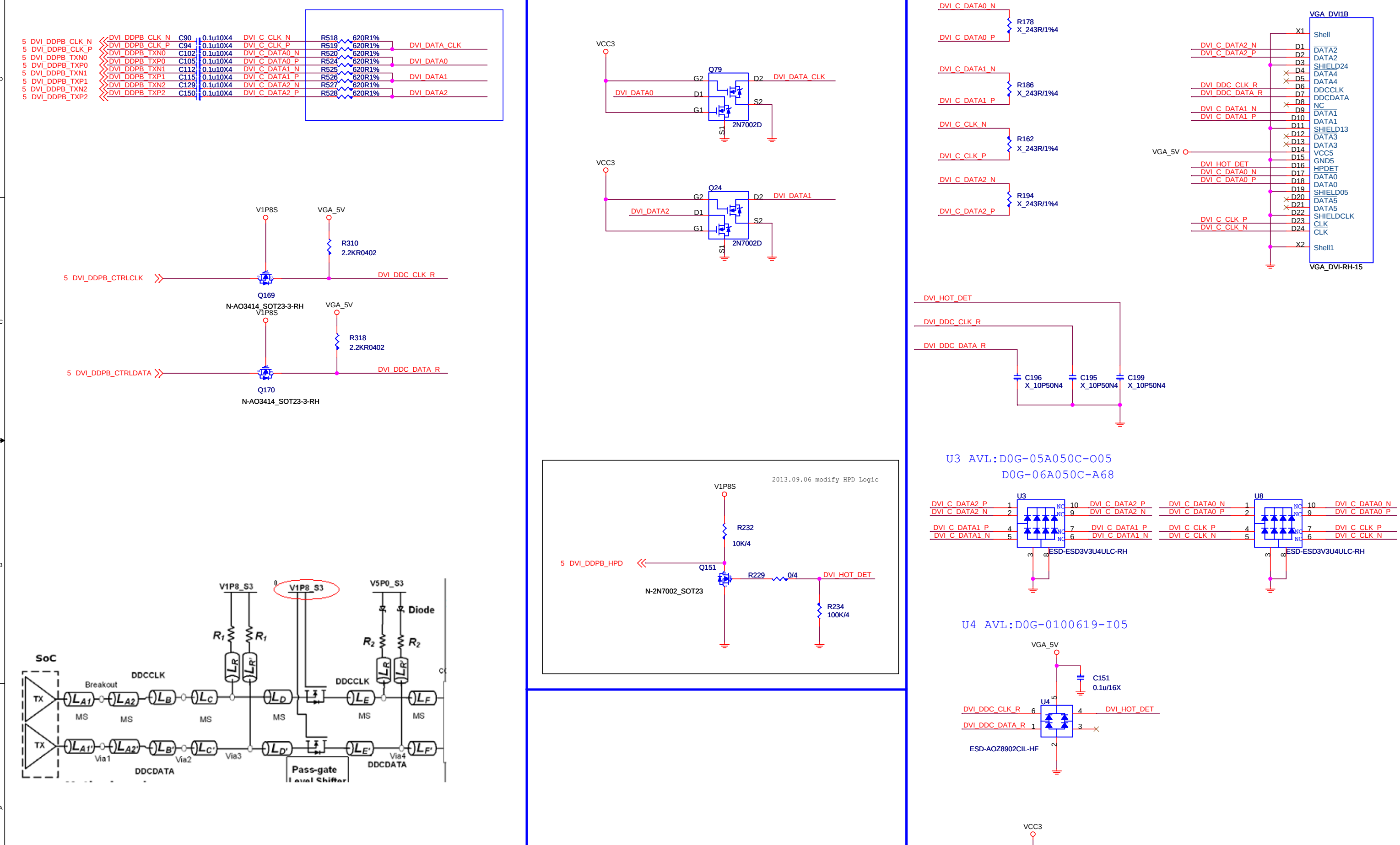
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

For EMI



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Size: Custom	Document Description: DVI MOS		Rev: 11
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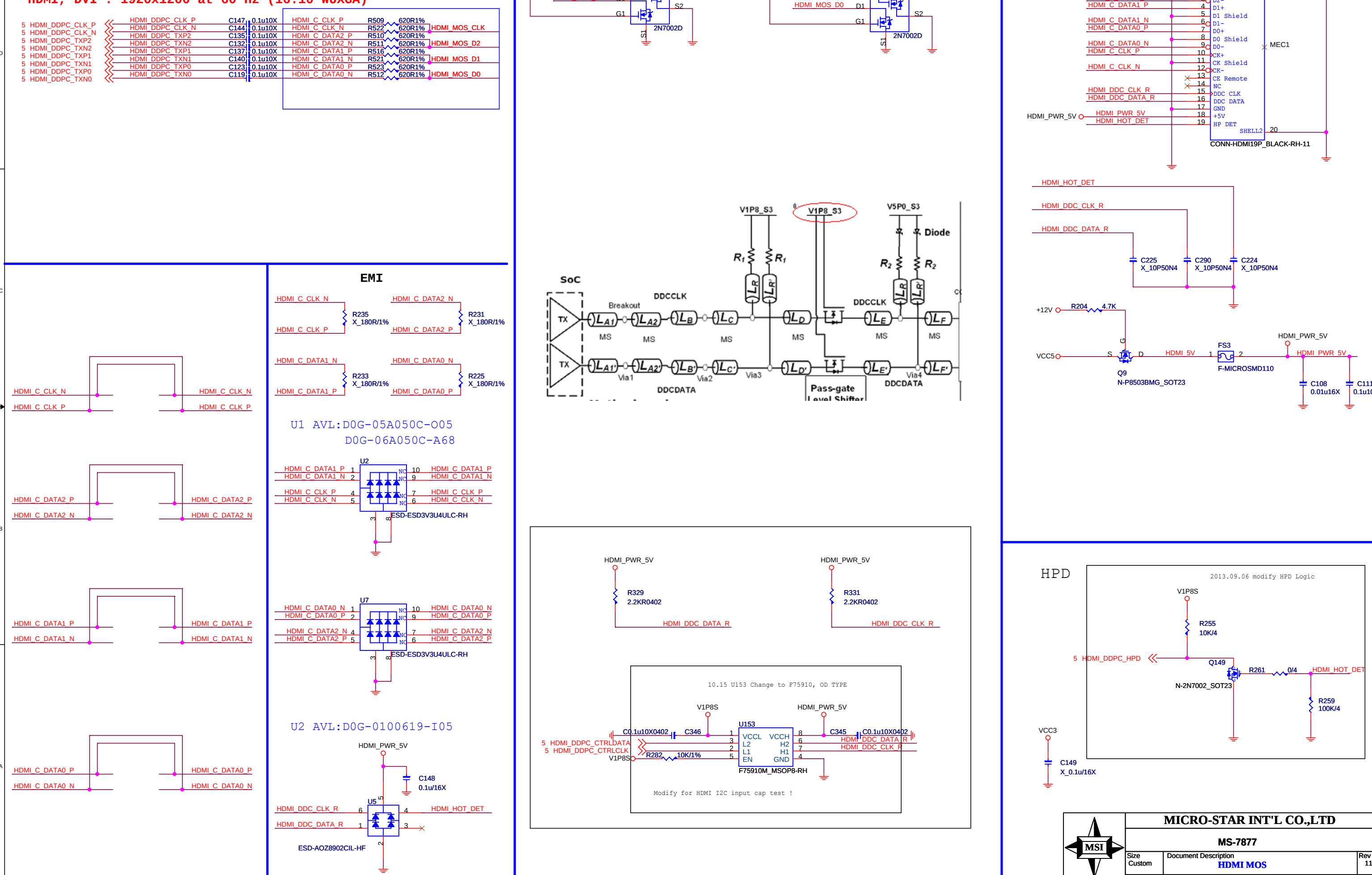
HDMI level shifter

HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



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Size: Custom	Document Description: HDMI MOS		Rev: 11
Date: Thursday, November 14, 2013		Sheet: 21	of: 9

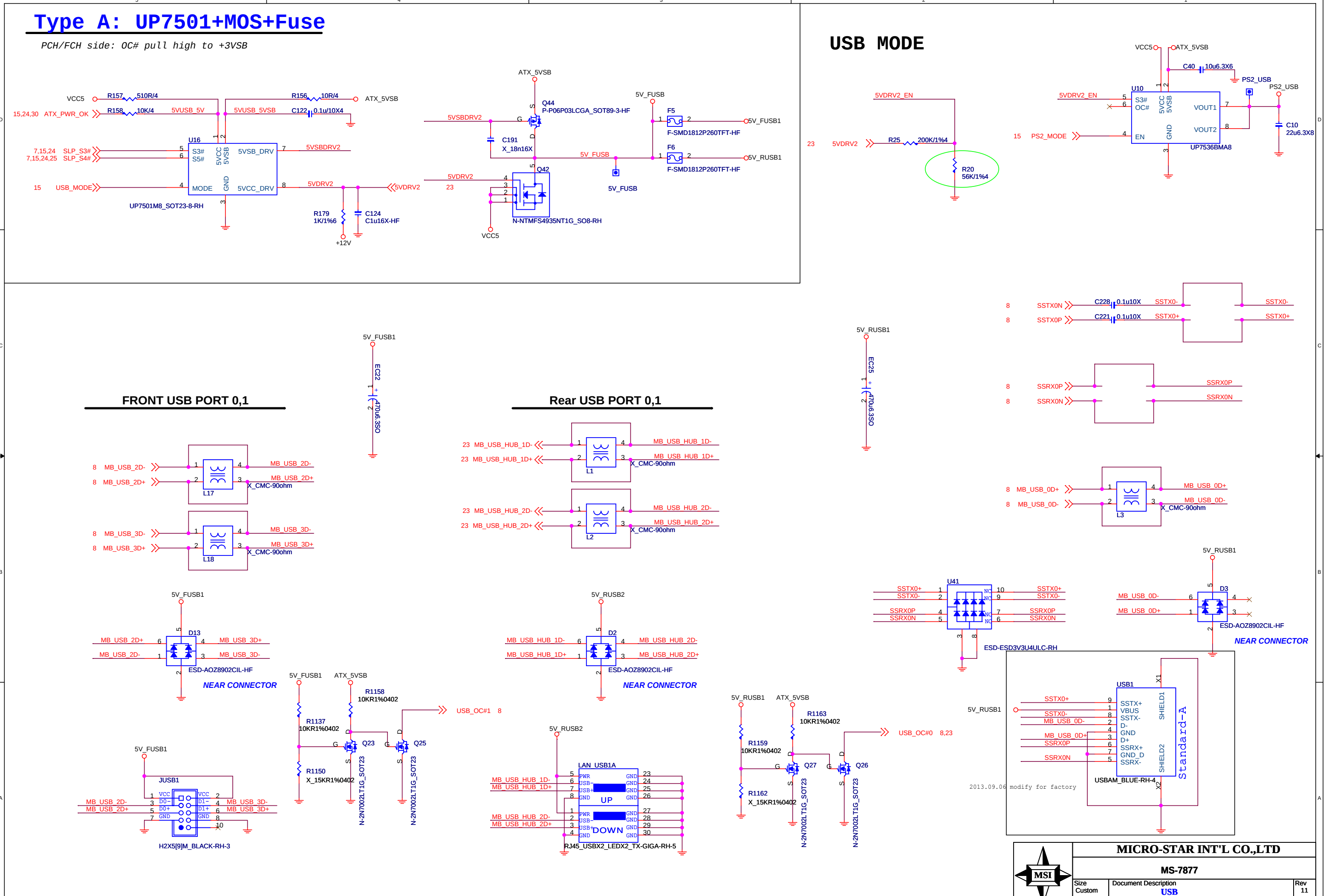
Type A: UP7501+MOS+Fuse

PCH/FCH side: OC# pull high to +3VSB

USB MODE

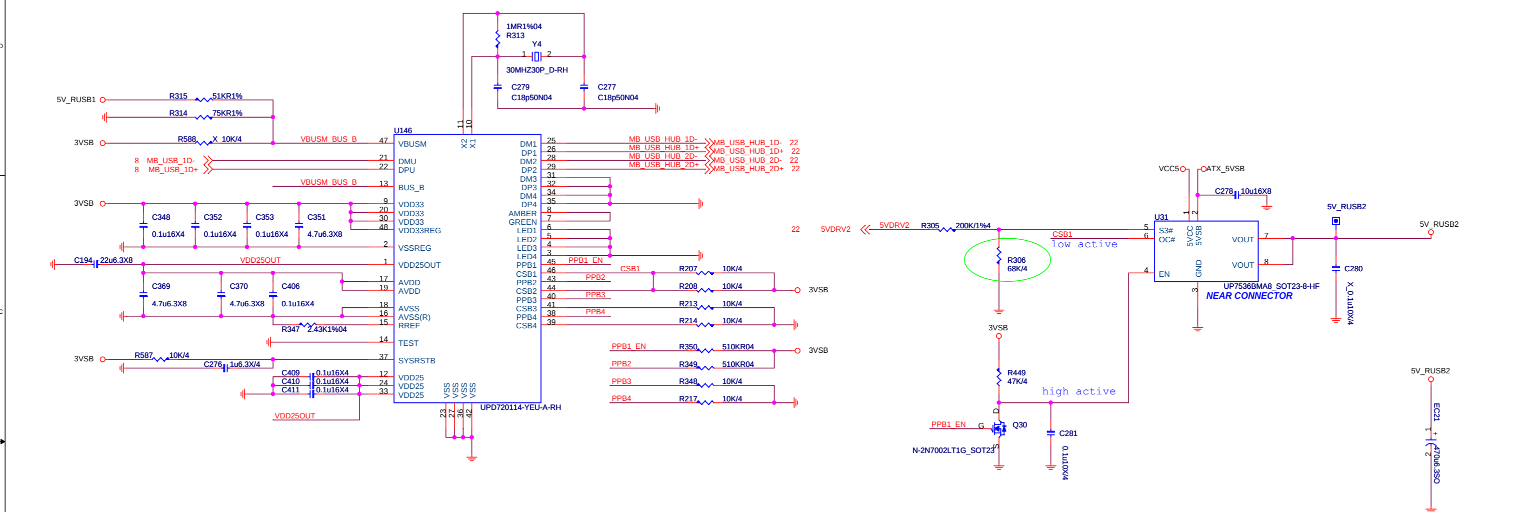
FRONT USB PORT 0,1

Rear USB PORT 0,1



MICRO-STAR INT'L CO.,LTD			
MS-7877			
Size: Custom	Document Description: USB		Rev: 11
Date: Thursday, November 14, 2013	Sheet 22 of 33		

USB HUB



MICRO-STAR INT'L CO.,LTD	
MS-7877	
Size: Custom	Document Description: USB HUB	Rev 11
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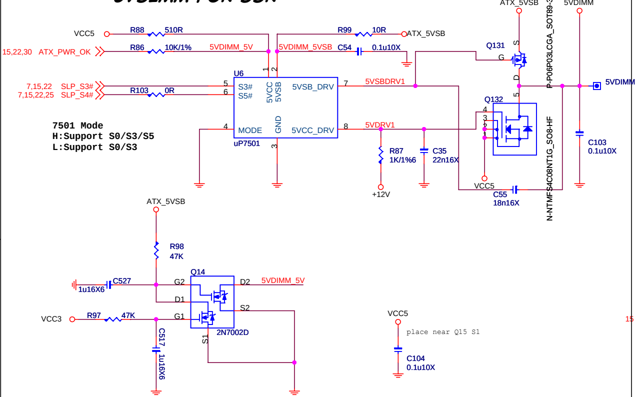
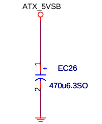
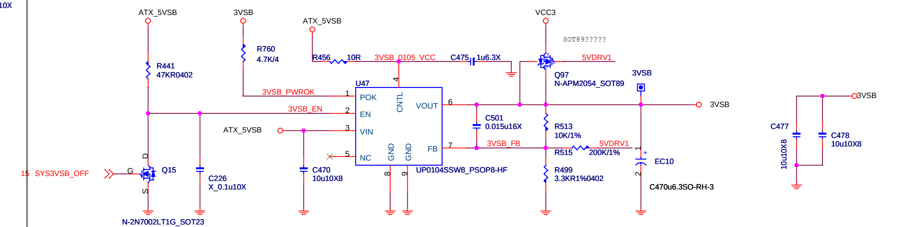
5VDIMM FOR DDR



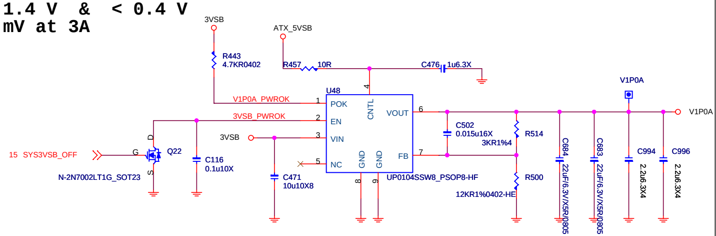
SOC Power: 3VSB
Max Power disspation:
VIN Range: 2.5 V to 5.5 V
Enable/disable: > 1.2 V & < 0.35 V
Soft stare time: 1 ms /PGOOD delay time: 1 ms(Vout >92%)



3VSB

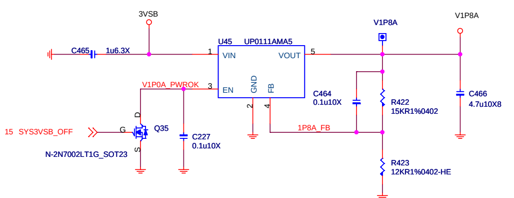


Max Power disspation: (3.3 V-1.0V)*0.35A=0.8 W
SOC Power: V1P0A 350 mA
VIN Range: 1.2 V to 5.5 V
Enable/disable: > 1.4 V & < 0.4 V
Drop voltage: 300 mV at 3A

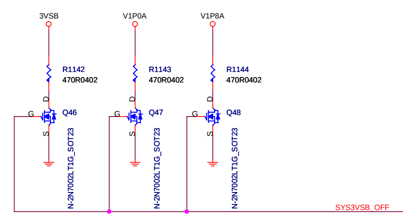


Remove V1P24A ,Ref DG 1.5 page165

SOC Power: V1P8A 65 mA
Max Power disspation: (3.3 V-1.8V)*0.065A=0.0975 W
VIN Range: 2.5 V to 5.5 V
Enable/disable: > 1.2 V & < 0.35 V
Drop voltage: 300 mV at 600 mA



Power Discharge Circuit



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DDRIII-L Power:1.35V (Total: 5.85 A)

V1P35Sx(VSFR):	400 mA
VDD-DRAM_VDD_S4 :	1.25A
V1P05S :	1.1A
SO-DIMM:	2.6 A
VTT:	0.5A

OCP Caculation

Iocp Rds(on)=9 uA *R927*

*5.58A*2*5mohm=9 uA* R927*

R927=6.5K

OCP 12.24A

Input Cap Caculation

Duty Cycle Calculation

$$Duty = \frac{output\_voltage}{input\_voltage} \times \frac{100\%}{efficiency}$$

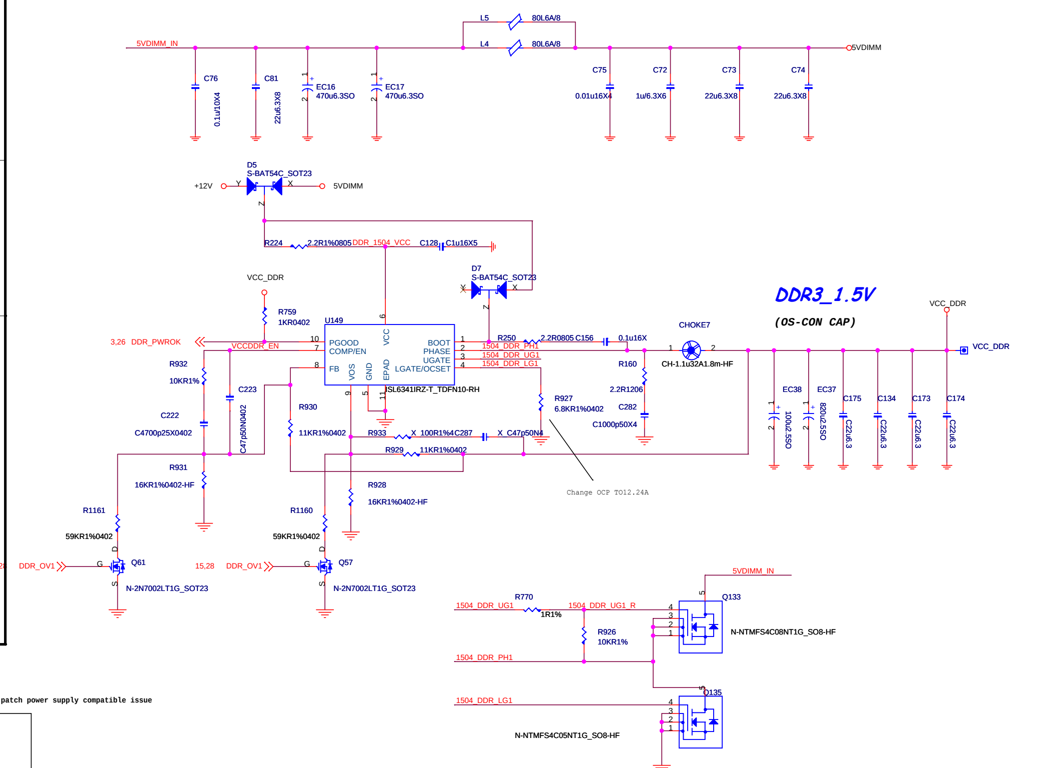
Input Ripple Current Calculation

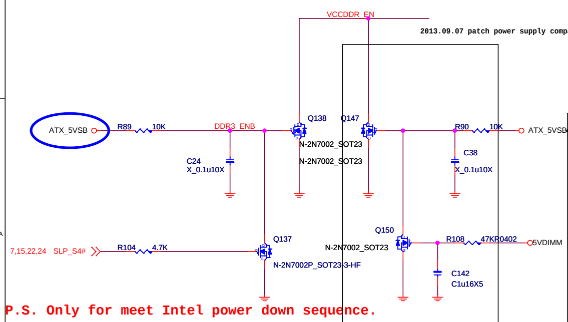
Phase Quantity: 1

$$Irms = output\_current \times \sqrt{duty \times (1 - duty)}$$

Efficiency:	80%
output :	1.5
Iripple :	5.23 A

4.7A*2 > 5.23 A

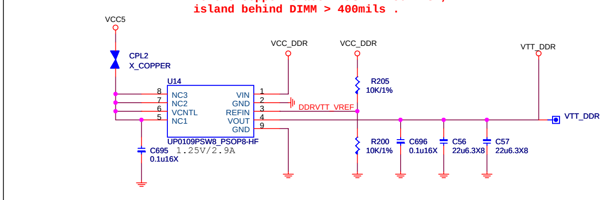




P.S. Only for meet Intel power down sequence.

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



MICRO-STAR INT'L CO.,LTD		
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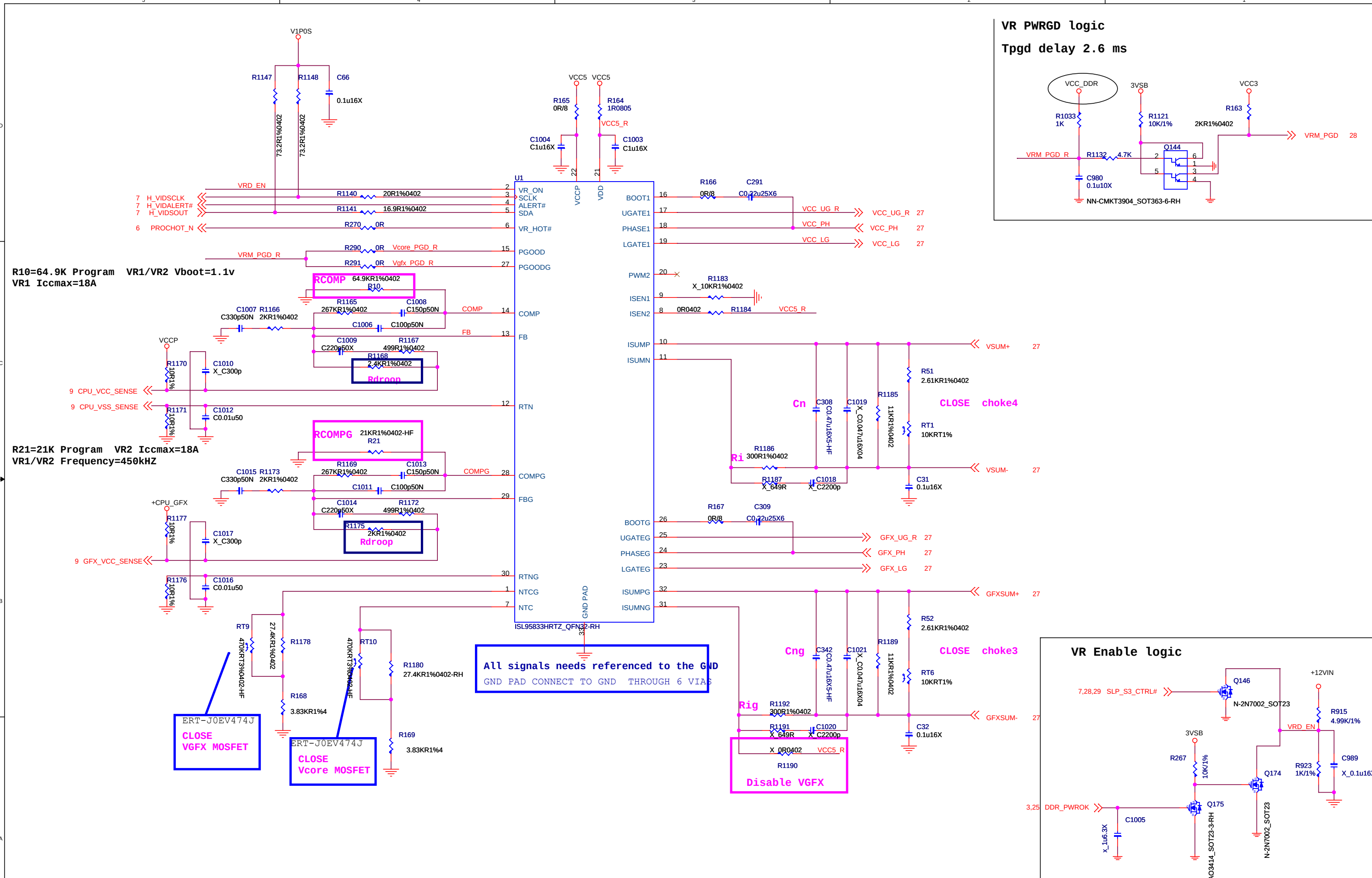
Size: Custom	Document Description: DDR Power	Rev: 11
Date: Thursday, November 14, 2013	Sheet 25 of 41	



MICRO-STAR INT'L CO.,LTD

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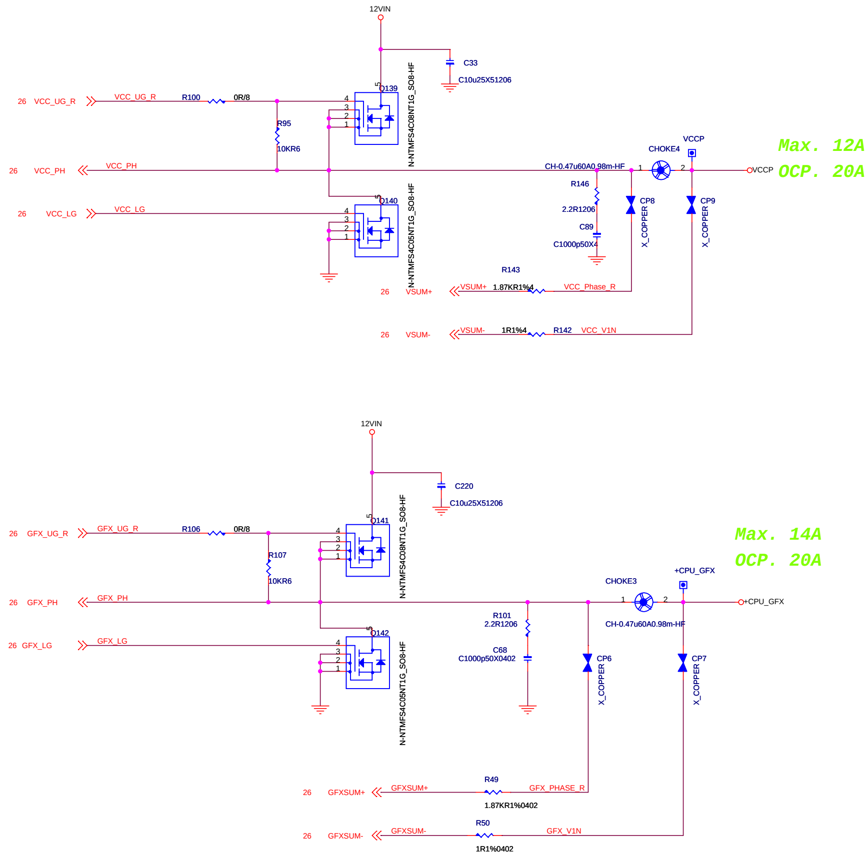
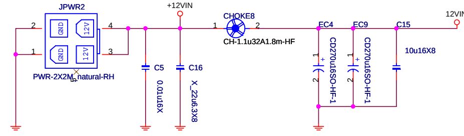
Size	Document Description	Rev
Custom	VCORE & GFX	11

Date: Thursday, November 14, 2013 Sheet 26 of 33





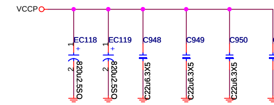


Table 4-16. Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Notes
POSCAP 330 μF	2	6 mΩ	1.8 nH	Output	1, 2
22 μF 0805 X5R	4	3 mΩ	0.6 nH	Output	

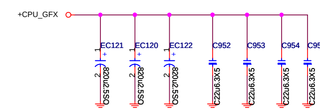


Table 4-17. UNCORE_VNN_S3 Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Notes
POSCAP 330 μF	3	6 mΩ	1.8 nH	Output	1, 2
22 μF 0805 X5R	4	3 mΩ	0.6 nH	Output	

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Custom	VCORE & GFX MOSFET	11

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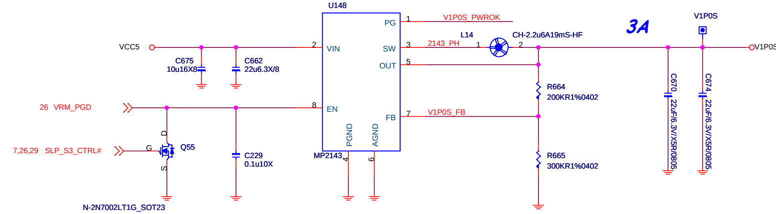
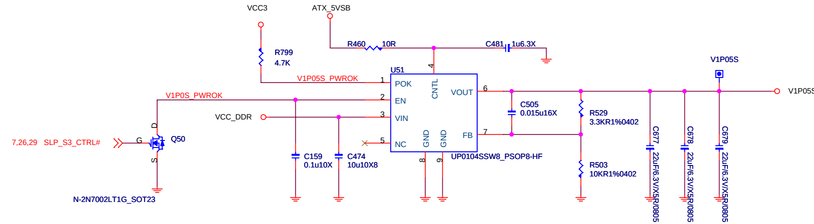
SOC Power: 1.0V 3 A

V1P0Sx: 2.1 A
V1P0S: 900 mA

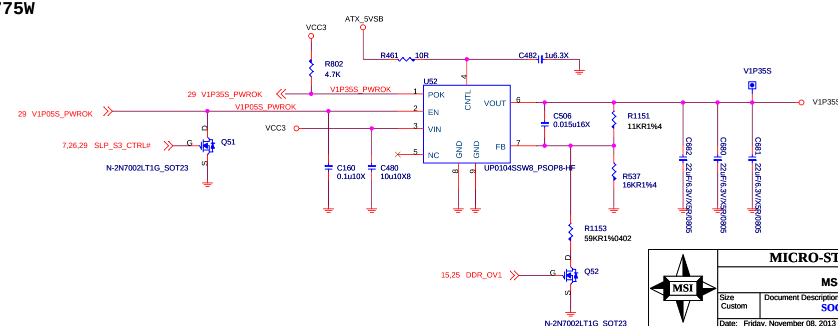
SOC Power: V1P0S 3A
VIN Range: 2.5 V to 5.5 V
Enable/disable: > 1.4 V & < 0.4 V
Guaranteed 3.0A Output Current



Max Power disspation: (1.5 V-1.05V)*1.1A=0.495W
SOC Power: V1P05S 1.1A
VIN Range: 1.2 V to 5.5 V
Enable/disable: > 1.2V & < 0.35 V
Drop voltage: 300 mV at 3A



Max Power disspation: (3.3 V-1.35V)*0.445A=0.86775W
SOC Power: V1P35S 445 mA
VIN Range: 1.2 V to 5.5 V
Enable/disable: > 1.4 V & < 0.4 V
Drop voltage: 300 mV at 3A



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Size	Document Description	Rev
Custom	SOC CORE POWER Part 1	10

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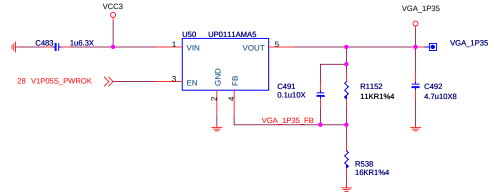
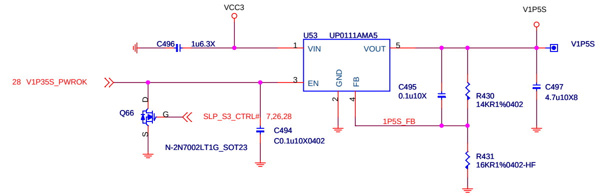
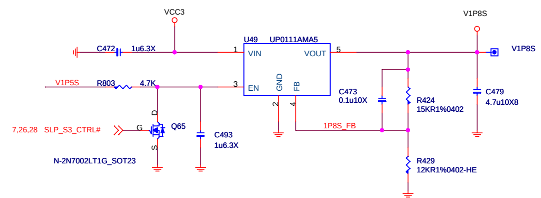
SOC Power: V1P8A 10 mA
Max Power disspation: (3.3 V-1.8V)*0.01A=0.015 W
VIN Range: 2.5 V to 5.5 V
Enable/disable: > 1.2 V & < 0.35 V
Drop voltage: 300 mV at 600 mA



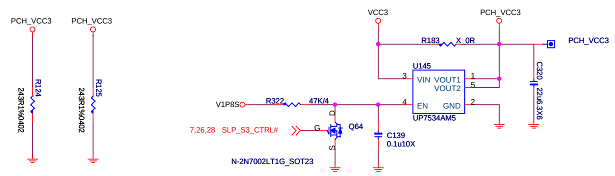
SOC Power: V1P8A 10 mA
Max Power disspation: (3.3 V-1.5V)*0.01A=0.018 W
VIN Range: 2.5 V to 5.5 V
Enable/disable: > 1.2 V & < 0.35 V
Drop voltage: 300 mV at 600 mA



SOC Power: V1P8A 10 mA
Max Power disspation: (3.3 V-1.8V)*0.01A=0.015 W
VIN Range: 2.5 V to 5.5 V
Enable/disable: > 1.2 V & < 0.35 V
Drop voltage: 300 mV at 600 mA



SOC Power: PCH_VCC3 38 mA
Continuous Load Current: 1.5A
VIN Range: 2.7V to 5.5 V
Enable/disable: > 1.4 V & < 0.4V



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Size: Custom	Document Description: SOC CORE POWER Part 2	Rev: 11
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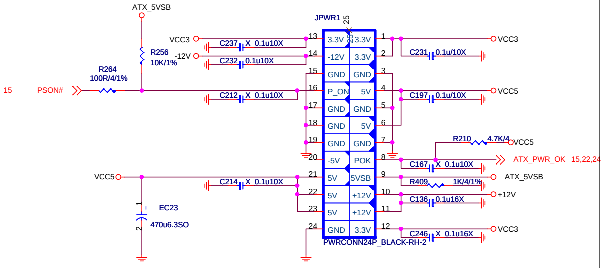
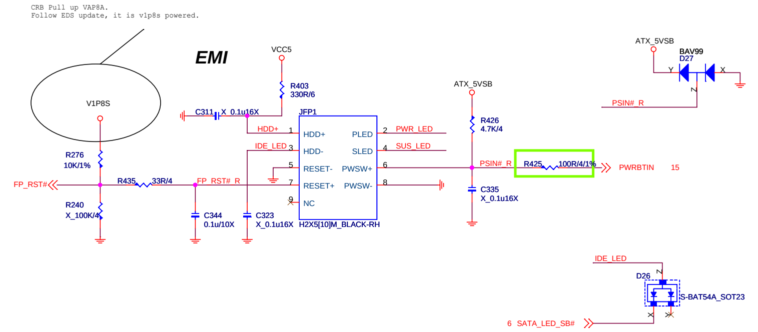
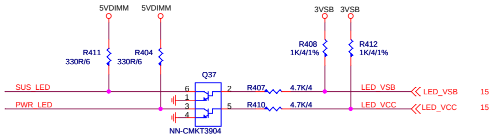
ATX POWER CONNECTOR



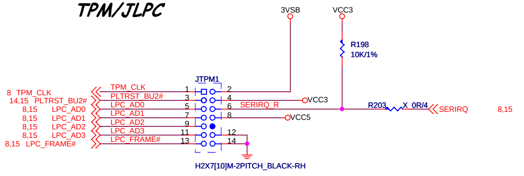
FRONT PANNEL



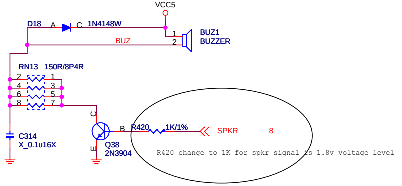
LED

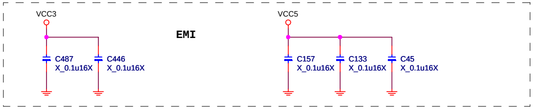


TPM/JLPC



Speaker Pin Header





MSI

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Size	Document Description	Rev
Custom	ATX F_Panel/EMI/TPM	11

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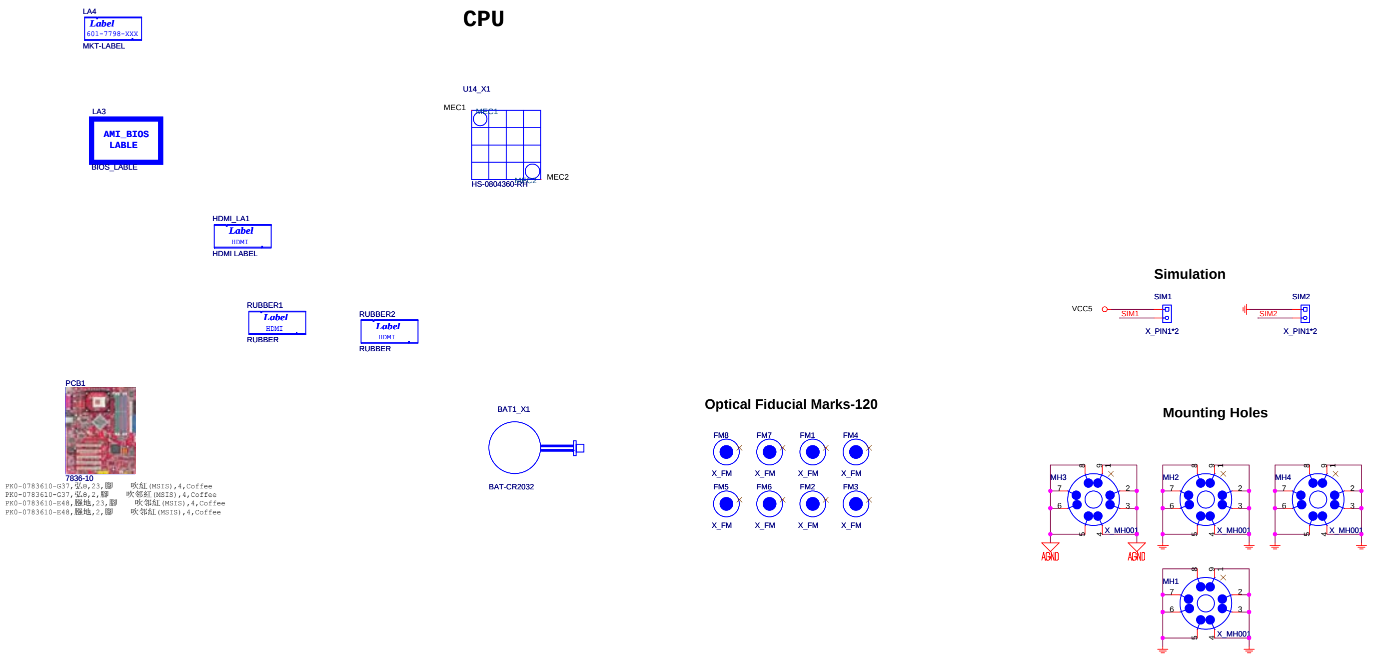

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Custom	Manual Parts	11

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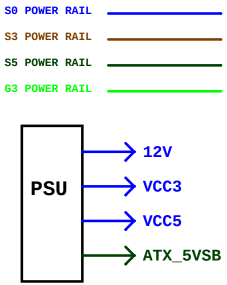
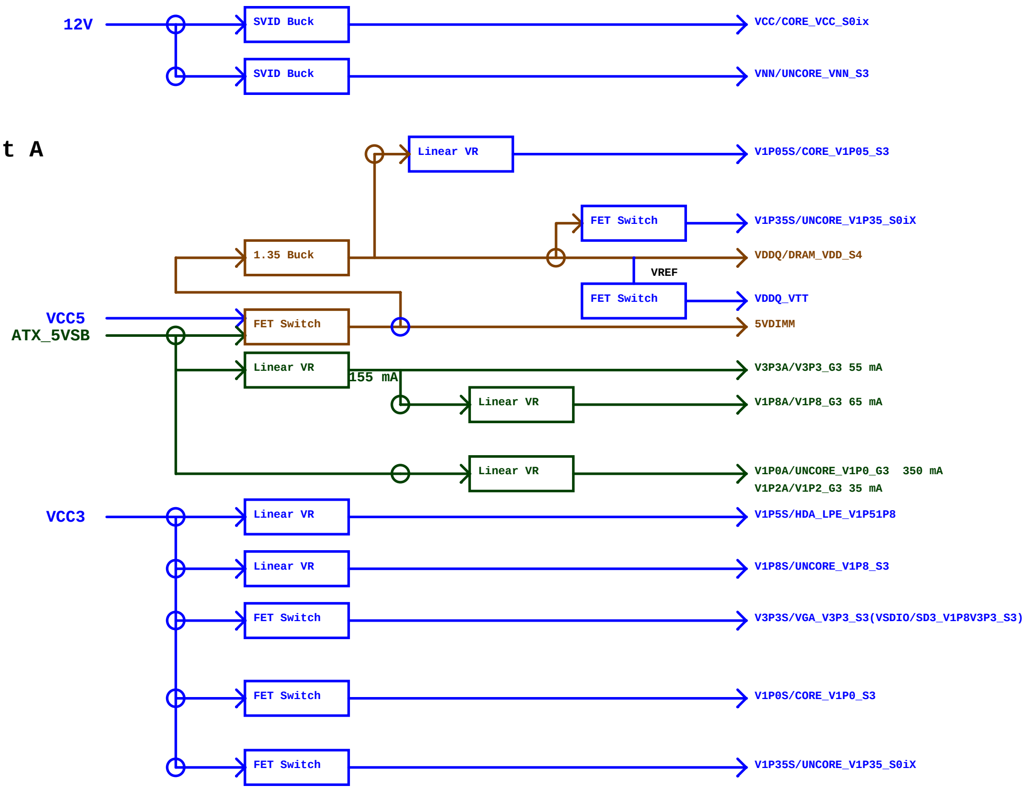


Part A



Part B

SOC	ICC
RTC_VCC	100uA
V1P0_G3	350mA
USB_HSIC_V1P24_G3	35mA
V1P8A	65mA
V3P3_G3	55mA
V1P0_S3	3A
V1P05_S3	1.1A
V1P35S	445mA
V1P8_S3	10mA
HDA_V1P5	10mA
VGA_V3P3_S3	38mA
DRAM_VDD_S4	1.25A
CORE_VCC_S3	12A
UNCORE_VNN_S3	14A

DDR3L	ICC
VDDQ(1.35V-1.5V)	
VDDQ_VTT	

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Custom	Power Map	10

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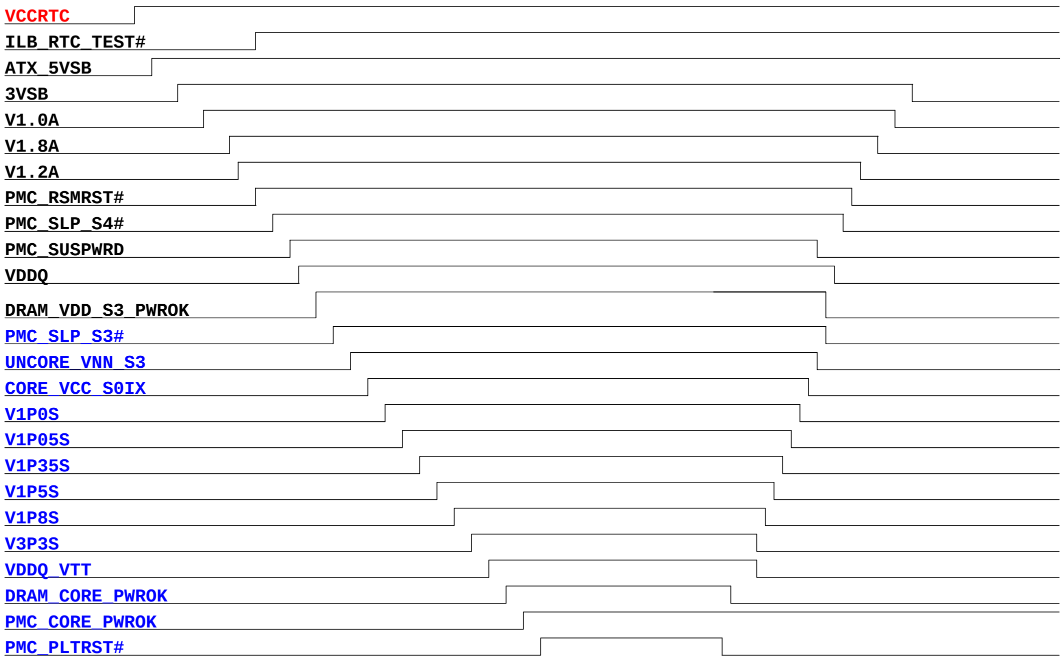

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Custom	Power Sequence	10

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BayTrail

GPIO	Power(Tolerance)	Default Term	strap	SMI/SCI	Application	S4/S5	S3	Reset	Enter S0
GPIO_S0_SC0	V1P8S	20K.L	NO	YES	NC	Off	Off	PD	PD
GPIO_S0_SC1	V1P8S	20K.L	NO	YES	NC	Off	Off	PD	PD
GPIO_S0_SC2	V1P8S	20K.H	NO	YES	SATA_LED_SB_N	Off	Off	PU	PU
GPIO_S0_SC3	V1P8S	20K.H	NO	YES	NC	Off	Off	PU	PU
GPIO_S0_SC4	V1P8S	20K.H	NO	YES	NC	Off	Off	PU	PU
GPIO_S0_SC5	V1P8S	20K.H	NO	YES	NC	Off	Off	PU	PU
GPIO_S0_SC6	V1P8S	20K.H	NO	YES	NC	Off	Off	PU	PU
GPIO_S0_SC7	V1P8S	20K.H	NO	YES	NC	Off	Off	PU	PU
GPIO_S0_SC8	VAUD	20K.L	NO	NO	AZ_RST#_R	Off	Off	PD	PD
GPIO_S0_SC9	VAUD	20K.L	NO	NO	AZ_SYNC_R	Off	Off	PD	PD
GPIO_S0_SC10	VAUD	20K.L	NO	NO	AZ_BITCLK_R	Off	Off	PD	PD
GPIO_S0_SC11	VAUD	20K.L	NO	NO	AZ_SDOUT_R	Off	Off	PD	PD
GPIO_S0_SC12	VAUD	20K.L	NO	NO	AZ_SDIN0	Off	Off	PD	PD
GPIO_S0_SC13	VAUD	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC14	VAUD	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC15	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC16	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC17	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC18	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC19	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC20	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC21	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC22	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC23	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC24	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC25	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC26	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC27	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC28	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC29	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC30	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC31	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC32	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC33	VSDIO	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC34	VSDIO	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC35	VSDIO	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC36	VSDIO	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC37	VSDIO	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC38	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC39	VSDIO	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC40	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC41	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC42	VLPC	20K.H	NO	NO	LPC_AD0	Off	Off	PU	PU
GPIO_S0_SC43	VLPC	20K.H	NO	NO	LPC_AD1	Off	Off	PU	PU
GPIO_S0_SC44	VLPC	20K.H	NO	NO	LPC_AD2	Off	Off	PU	PU
GPIO_S0_SC45	VLPC	20K.H	NO	NO	LPC_AD3	Off	Off	PU	PU
GPIO_S0_SC46	VLPC	20K.H	NO	NO	LPC_FRAME#	Off	Off		
GPIO_S0_SC47	VLPC	20K.L	NO	NO	LPC_CLK	Off	Off		
GPIO_S0_SC48	VLPC	20K.L	NO	NO	TPM_CLK	Off	Off		
GPIO_S0_SC49	VLPC	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC50	V1P8S	20K.H	NO	NO	LPC_SERIRQ	Off	Off	PU	PU
GPIO_S0_SC51	V1P8S	20K.H	NO	NO	PCU_SMB_DATA	Off	Off	PU	PU
GPIO_S0_SC52	V1P8S	20K.H	NO	NO	PCU_SMB_CLK	Off	Off	PU	PU
GPIO_S0_SC53	V1P8S	20K.H	NO	NO	PCU_SMB_ALERT# (PU 10K to V1P8S)	Off	Off	PU	PU
GPIO_S0_SC54	V1P8S	20K.H	NO	NO	SPKR	Off	Off	PU	PU
GPIO_S0_SC55	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC56	V1P8S	20K.H	YES	NO		Off	Off	PU	PU
GPIO_S0_SC57	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC58	V1P8S	20K.L	NO	NO	4.7K PD	Off	Off	PD	PD
GPIO_S0_SC59	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC60	V1P8S	20K.L	NO	NO	PU 10K to V1P8S	Off	Off	PD	PD
GPIO_S0_SC61	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC62	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC63	V1P8S	20K.H	YES	NO	NC	Off	Off	PU	PU
GPIO_S0_SC64	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC65	V1P8S	20K.H	YES	NO	NC	Off	Off	PU	PU
GPIO_S0_SC66	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC67	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC68	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC69	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC70	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC71	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC72	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC73	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC74	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC75	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC76	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC77	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC78	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC79	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC80	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC81	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC82	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC83	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC84	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC85	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC86	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC87	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC88	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC89	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC90	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC91	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC92	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC93	V1P8S	20K.H	NO	NO	NC	Off	Off	PU	PU
GPIO_S0_SC94	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC95	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC96	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC97	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC98	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC99	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC100	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_S0_SC101	V1P8S	20K.L	NO	NO	NC	Off	Off	PD	PD
GPIO_SUS_0	V1P8A	20K.H	NO	YES	NC	PU	PU	PU	PU
GPIO_SUS_1	V1P8A	20K.H	NO	YES	NC	PU	PU	PU	PU
GPIO_SUS_2	V1P8A	20K.H	NO	YES	NC	PU	PU	PU	PU
GPIO_SUS_3	V1P8A	20K.H	NO	YES	NC	PU	PU	PU	PU
GPIO_SUS_4	V1P8A	20K.L	NO	YES	NC	PD	PD	PD	PD
GPIO_SUS_5	V1P8A	20K.L	NO	YES	NC	PD	PD	PD	PD
GPIO_SUS_6	V1P8A	20K.L	NO	YES	NC	PD	PD	PD	PD
GPIO_SUS_7	V1P8A	20K.L	NO	YES	10K PU TO V1P8A	PD	PD	PD	PD
GPIO_SUS_8	V1P8A	20K.L	NO	NO	NC	PD	PD	PD	PD
GPIO_SUS_9	V1P8A	20K.L	NO	NO	NC	PD	PD	PD	PD
GPIO_SUS_10	V1P8A	20K.H	NO	NO	NC	PU	PU	PU	PU
GPIO_SUS_11	V1P8A		NO	NO	SUSPWRDNACK	0/1	0/1	0	0/1
GPIO_SUS_12	V1P8A		NO	NO	PMC_SUSCLK0	T	T	T	T
GPIO_SUS_13	V1P8A		NO	NO	PMC_SLP_S0IX#	0	0	0	0/1
GPIO_SUS_14	V1P8A		NO	NO	SOC_PME#	0	0	0	0/1
GPIO_SUS_15	V1P8A	20K.H	NO	NO	SOC_WAKE#		PU	PU	PU
GPIO_SUS_16	V1P8A	20K.H	NO	NO	PMC_PWRBTN#		PU	PU	PU
GPIO_SUS_17	V1P8A	20K.H	NO	NO	NC	PU		PU	PU
GPIO_SUS_18	V1P8A		NO	NO	PMC_SUS_STAT#	0	0	0	1
GPIO_SUS_19	V1P8A	20K.H	NO	NO	USB_OC0#	PU	PU	PU	PU
GPIO_SUS_20	V1P8A	20K.H	NO	NO	USB_OC1#	PU	PU	PU	PU
GPIO_SUS_21	V1P8A	20K.H	NO	NO	NC	PU	PU	PU	PU
GPIO_SUS_22	V1P8A	20K.L	NO	NO	NC	PD	PD	PD	PD
GPIO_SUS_23	V1P8A	20K.L	NO	NO	NC	PD	PD	PD	PD
GPIO_SUS_24	V1P8A	20K.L	NO	NO	NC	PD	PD	PD	PD
GPIO_SUS_25	V1P8A	20K.L	NO	NO	NC	PD	PD	PD	PD
GPIO_SUS_26	V1P8A	20K.L	NO	NO	NC	PD	PD	PD	PD
GPIO_SUS_27	V1P8A	20K.H	NO	NO	NC	PU	PU	PU	PU
GPIO_SUS_28	V1P8A	20K.H	NO	NO	NC	PU	PU	PU	PU
GPIO_SUS_29	V1P8A	20K.H	NO	NO	NC	PU	PU	PU	PU
GPIO_SUS_30	V1P8A	20K.H	NO	NO	NC	PU	PU	PU	PU
GPIO_SUS_31	V1P8A	20K.L	NO	NO	NC	PD	PD	PD	PD
GPIO_SUS_32	V1P8A	20K.L	NO	NO	NC	PD	PD	PD	PD
GPIO_SUS_33	V1P8A	20K.L	NO	NO	NC	PD	PD	PD	PD
GPIO_SUS_34	V1P8A	20K.L	NO	NO	NC	PD	PD	PD	PD
GPIO_SUS_35	V1P8A	20K.L	NO	NO	NC	PD	PD	PD	PD
GPIO_SUS_36	V1P8A	20K.L	NO	NO	NC	PD	PD	PD	PD
GPIO_SUS_37	V1P8A	20K.L	NO	NO	PU 10K to V1P8A	PD	PD	PD	PD
GPIO_SUS_38	V1P8A	20K.L	NO	NO	NC	PD	PD	PD	PD
GPIO_SUS_39	V1P8A	20K.L	NO	NO	NC	PD	PD	PD	PD
GPIO_SUS_40	V1P8A	20K.H	NO	NO	NC	PU	PU	PU	PU
GPIO_SUS_41	V1P8A	20K.L	NO	NO	NC	PD	PD	PD	PD
GPIO_SUS_42	V1P8A	20K.H	NO	NO	NC	PU	PU	PU	PU
GPIO_SUS_43	V1P8A	20K.L	NO	NO	NC	PD	PD	PD	PD

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SIO

GPIO	Alt Function	Power(Tolerance)	Default	strapping	Application
GPIO0	AUXFANOUT0	3VCC(3.3V)	DCD#	NO	DCDA#(COM PORT)
GPIO1	AUXFANOUT1	3VCC(3.3V)	RI#	NO	RIA#
GPIO2	AUXFANOUT2	3VCC(3.3V)	CTS#	NO	CTSA#
GPIO3	OVT#/SMI#	3VCC(3.3V)	DTR#	NO	DTRA#
GPIO4	AUXFANIN0	3VCC(3.3V)	RTS#	YES	RTSA#
GPIO5	AUXFANIN1	3VCC(3.3V)	DSR#	NO	DSRA#
GPIO6	AUXFANIN2	3VCC(3.3V)	SOUT	YES	SOUTA
GPIO7	CIRTX0	3VCC(3.3V)	SIN	NO	SINA
GPIO10	RIB#	I_VSB3V(3.3V)	KBDAT	NO	KBDAT
GPIO11	DCDB#	I_VSB3V(3.3V)	KBCLK	NO	KBCLK
GPIO12	SOUTB/IRTX0	I_VSB3V(3.3V)	MSDAT	NO	MSDAT
GPIO13	SINB/IRRX0	I_VSB3V(3.3V)	MSCLK	NO	MSCLK
GPIO14	DTRB#	I_VSB3V(3.3V)	PSOUT#	NO	PWRBTN#
GPIO15	RTSB#(UARTP80_EN)				
GPIO16	DSRB#				
GPIO17	CTSB#				
GPIO18					
GPIO19					
GPIO20	KDAT	I_VSB3V(3.3V)	GPI	NO	SIO_PME#
GPIO21	KCLK	I_VSB3V(3.3V)	GPI(default high)	NO	USB_MODE
GPIO22	MDAT	I_VSB3V(3.3V)	GPI(default Low)	NO	PS2_MODE
GPIO23	MCLK	I_VSB3V(3.3V)	WDTRST#(Internal pull	NO	NC
GPIO24	CIRRX/IRRX1	I_VSB3V(3.3V)	GPIO	NO	LED_VSB
GPIO25	IRTX1(AMDPWR_EN)/CIRTX1	I_VSB3V(3.3V)	GPIO	YES	LED_VCC
GPIO26	TSIC	I_VSB3V(3.3V)	RESETCON#	NO	NC
GPIO27	CIRRWB1/MLED	I_VSB3V(3.3V)	PSIN#	NO	PWRBTIN
GPIO28					

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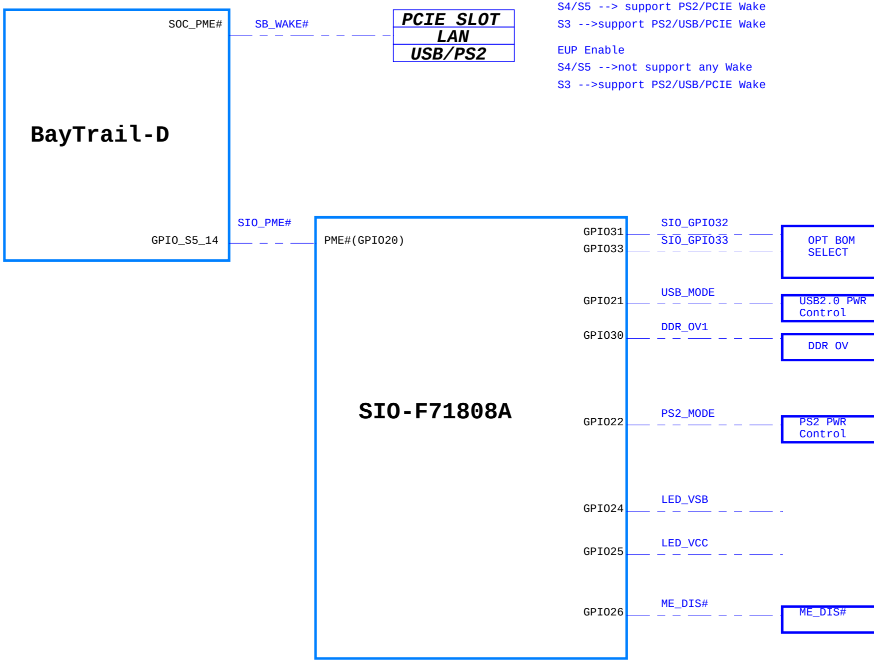
EUP Disable
S4/S5 --> support PS2/PCIE Wake
S3 -->support PS2/USB/PCIE Wake

EUP Enable
S4/S5 -->not support any Wake
S3 -->support PS2/USB/PCIE Wake



USB_MODE Status

MODE	G3	S4/S5	S0	S3
EUP Disable	0	0	1	1
EUP Enable	0	0	1	1

DDR_OV

Valtage	1.35V	1.5V
DDR_OV1	Low	High

***Default 1.5V**

PS2_MODE Status

MODE	G3	S4/S5	S0	S3
EUP Disable	0	0	1	1
EUP Enable	0	0	1	1

ME_DIS#	G3	S4/S5	S0	S3
Default	1(OD H)	1(OD H)	1(OD H)	1(OD H)
Enable	0(OD L)	0(OD L)	0(OD L)	0(OD L)

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Change to revision 1.0

1.P3: r561 change to 29.4ohm

2.P7: R312/R324 Change to 1K for signal rising quickly.

3.P7:unstuff C490 to meet pmc_core_pwrok vs ddr3_vcca_pwrok power down sequence .

4.P8:serirq change level shift .

5.P15:unstuff R364, add R248 for resolve ATX_5VSB inrush current issue.

6.C261,C259,C252,C264,C255,C254,L16,L15,L13 Changed for EMC suggested.

7.Add u153 for patch sa test hdmi i2c input cap fail issue!

8.P5: Add txe disable circuit by gpio control

9.P7: Remove PME# control circuit & use psout for ps2 wake up.

10.P10: USB_HSIC_V1P2_G3_V18 Change tied to v1p0A.

11.P15: HMGND Connect to sio pin39

12.P25: Change DDR OCP to 12.24A

13.P6: Change q163/q165 to 3414

14.P30: Change r420 to 1k for spkr signal is 1.8v voltage level.

15.P20: R229 change to 0ohm
   P21: R210 change to 0ohm

16.P7: R325 Change to 4.7K for signal rising quickly.

17.P16: Change cpu fan from 4 pin smart fan to 3 pin smart fan.

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