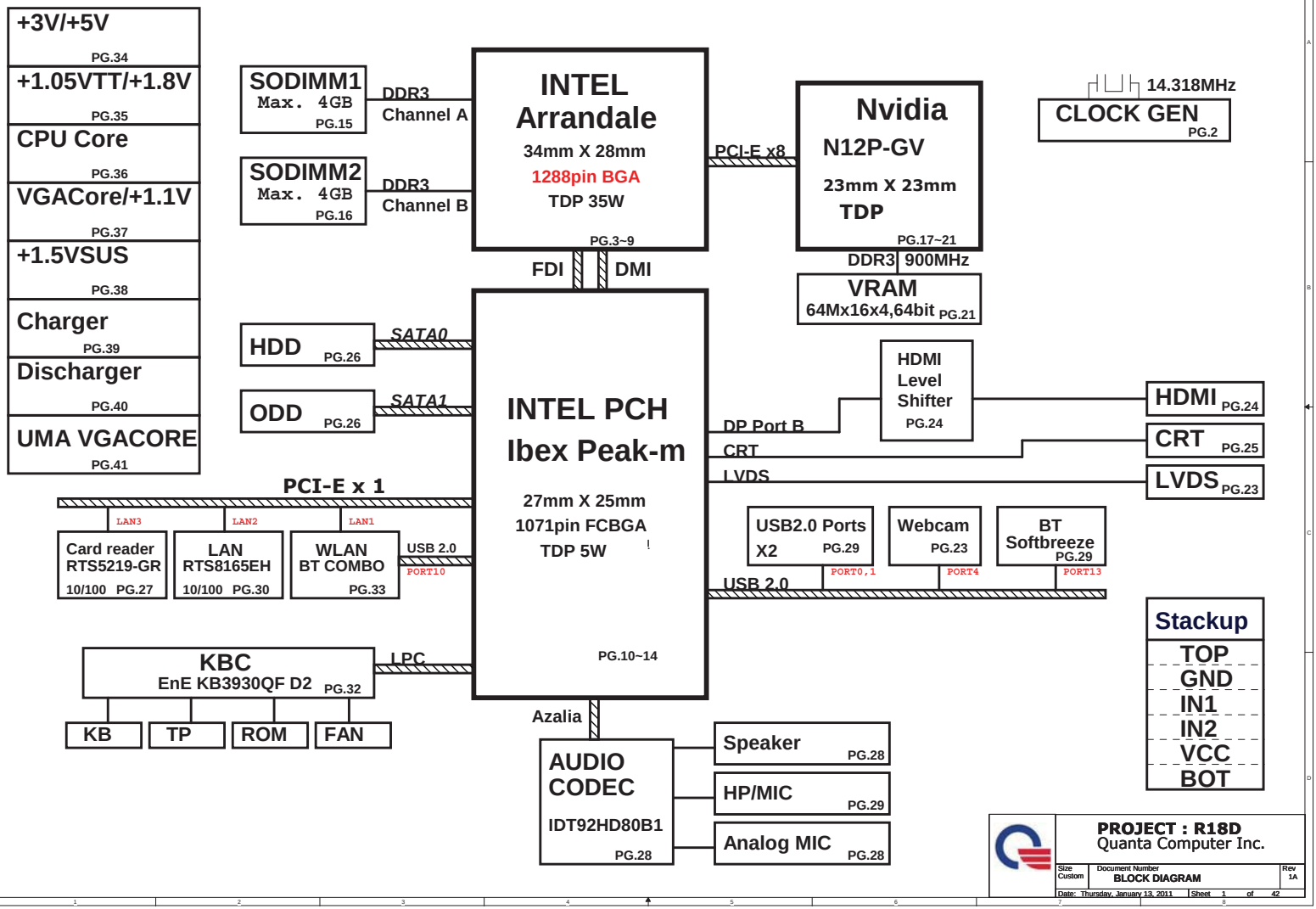
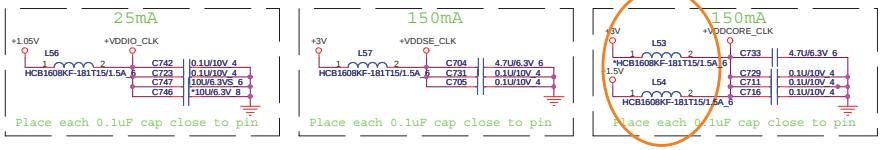
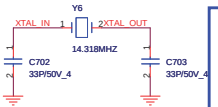
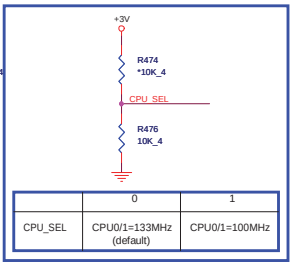
R18D INTEL UMA/DISCRETE SYSTEM DIAGRAM



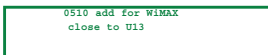
PROJECT : R18D Quanta Computer Inc.		
Size: Custom	Document Number: BLOCK DIAGRAM	Rev: 1A
Date: Thursday, January 13, 2011	Sheet 1 of 42	

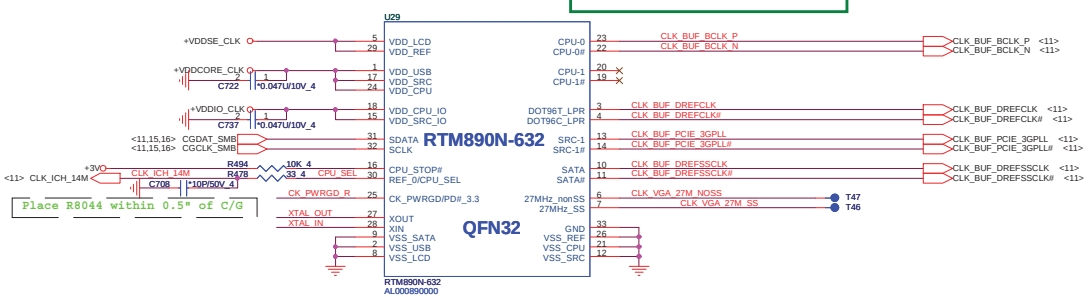


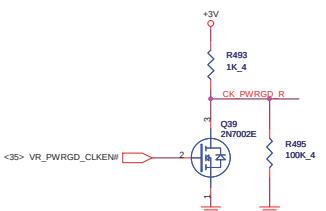




0510 add for WiMAX close to U13







Vender	Part	Part Number	Part Description
ICS	ICS9LVS3197	AL003197001	IC OTHER(32P) ICS9LVS3197AKLFT(MLF)
Realtek	RTM890N-632	AL000890000	IC OTHER(32P) RTM890N-632-GRT(QFN)
Silego	SLG8LV595VTR	AL000595000	IC OTHER(32P)SLG8LV595VTR(QFN)

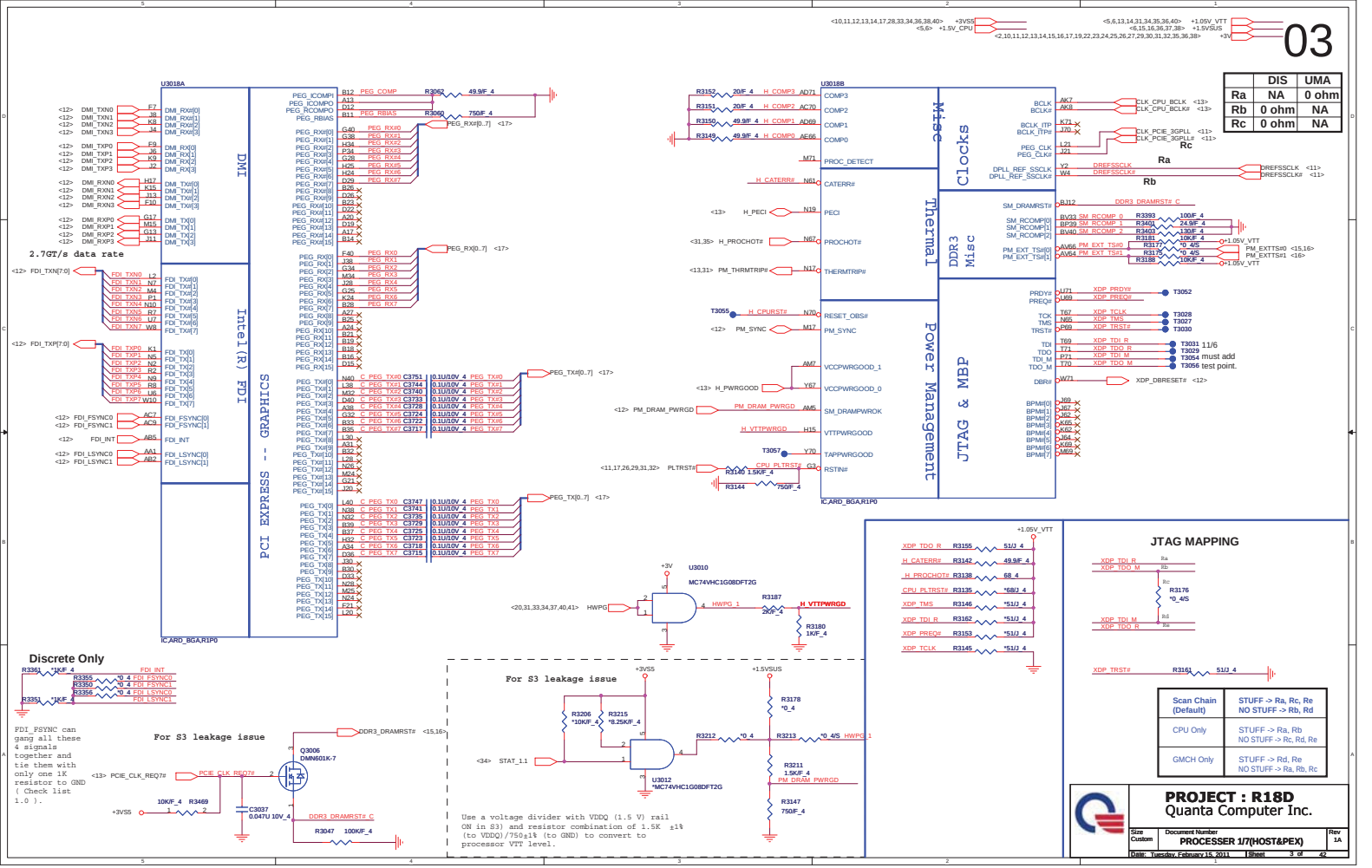
+1.05V <10,11,12,14,41>
+1.5V <6,32>
+3V <3,10,11,12,13,14,15,16,17,19,22,23,24,25,26,27,29,30,31,32,35,36,38>

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Gen(9LRS3197)	1A

Date: Tuesday, February 15, 2011 Sheet 2 of 42

	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA



Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

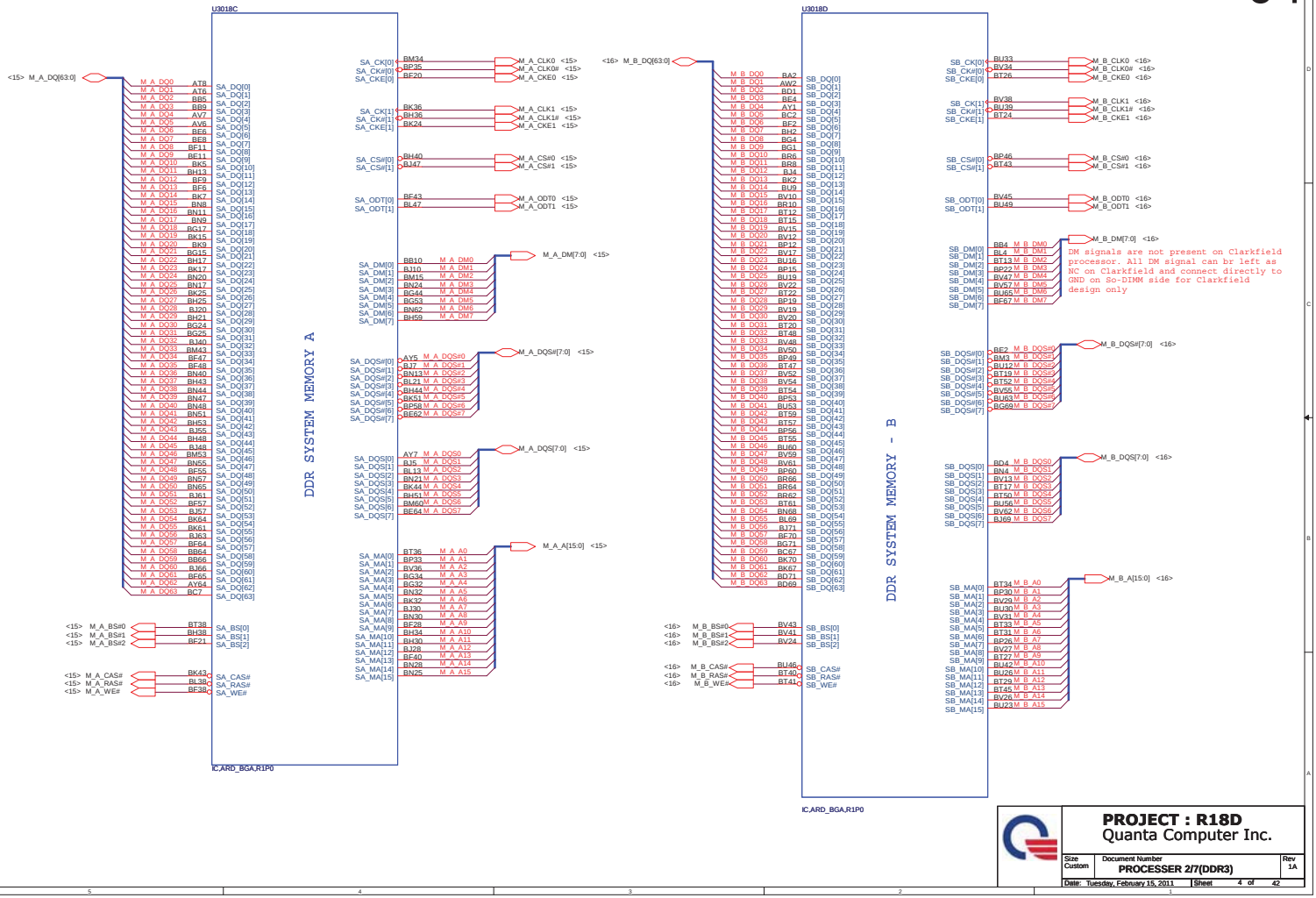
JTAG MAPPING

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 1/7(HOST&PEX)	1A

Date: Tuesday, February 15, 2011 | Sheet 3 of 42

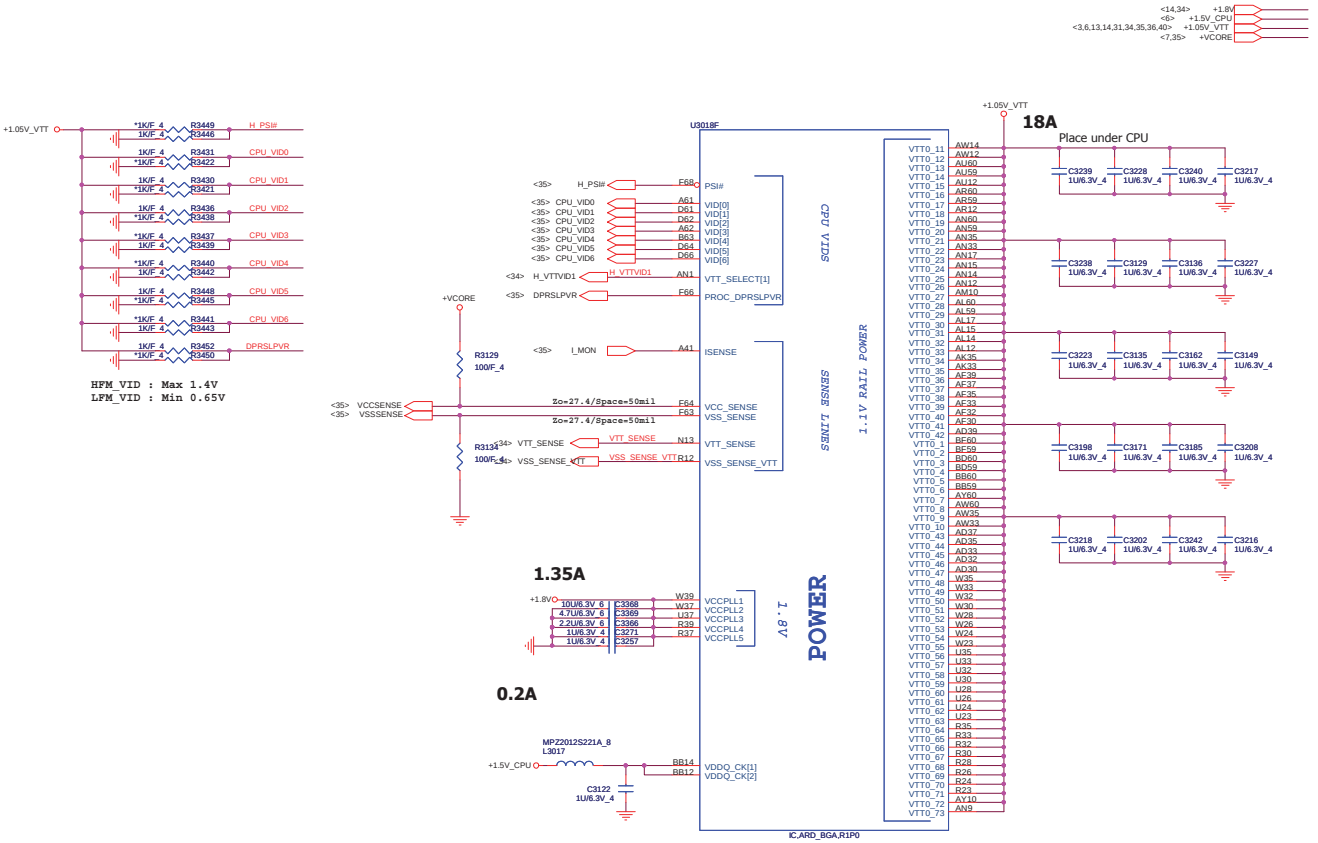
ARRANDALE/CLARKSFIELD PROCESSOR (DDR3)



PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 2/7(DDR3)	1A

Date: Tuesday, February 15, 2011 | Sheet 4 of 42

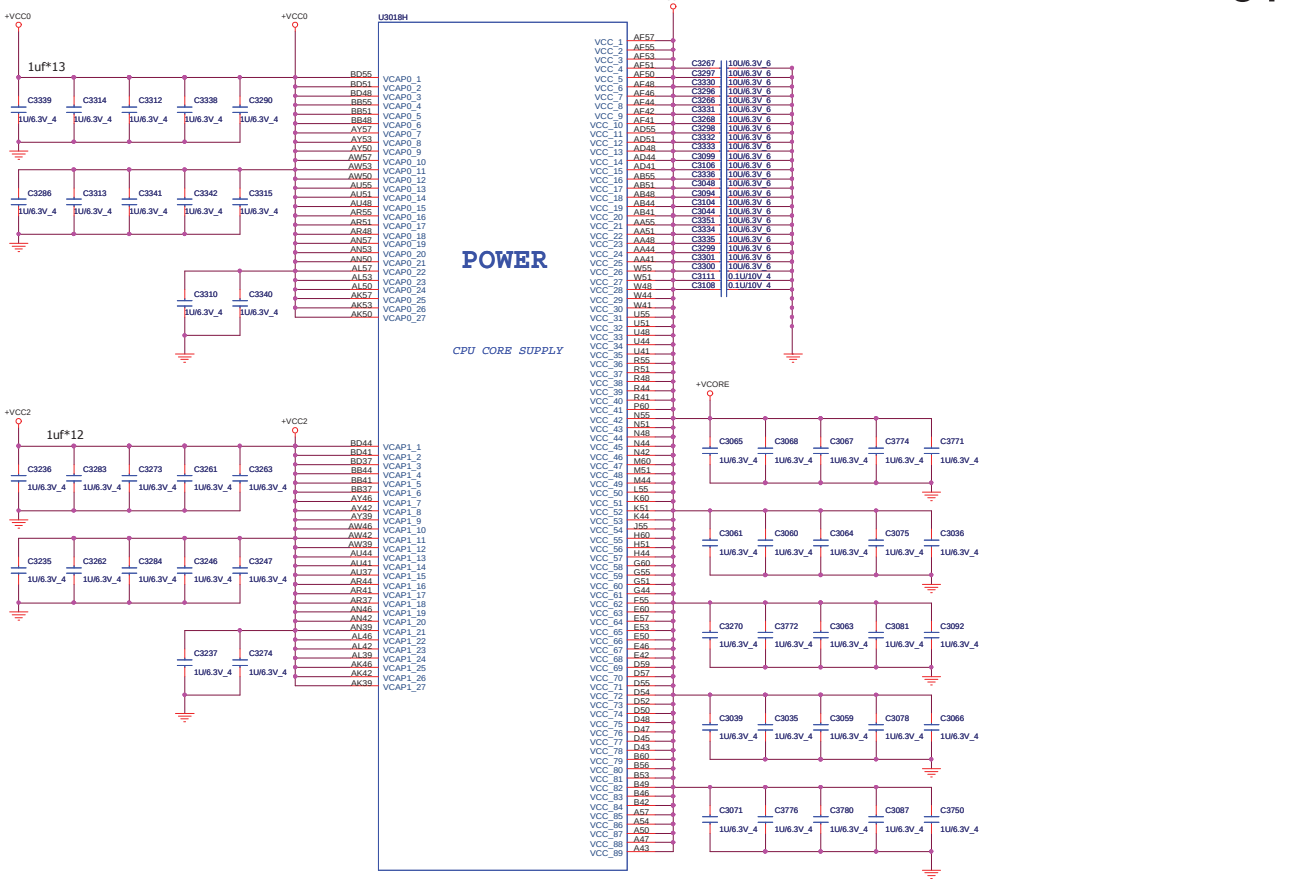


PROJECT : R18D
Quanta Computer Inc.

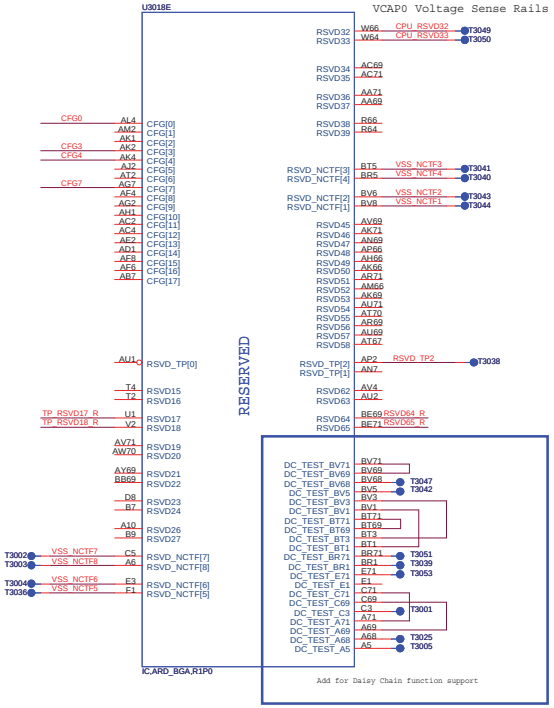
Size	Document Number	Rev
Custom	PROCESSER 3/7(POWER1)	1A

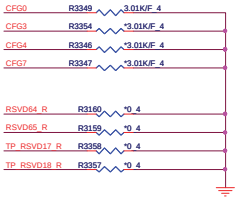
Date: Tuesday, February 15, 2011 | Sheet 5 of 42

06
Max 22A
VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V
Please note that +VCC_GFX_CORE
should be 1.05V in Arrandale
+VGACORE_IGPU
U3018G
GRAPHICS
POWER
PEG & DMI
DDR3 - 1.5V RAILS
GRAPHICS VIDs
SENSE LINES
3A
2.6A
for S3 power reduction
40mile routing
VCAP0
VCAP1
VCAP2
IC,ARD_BGA,R1P0
PROJECT : R18D
Quanta Computer Inc.
PROCESSER 4/7(POWER2)
Tuesday, February 15, 2011
6 of 42



PROJECT : R18D	
Quanta Computer Inc.	
Size: Custom	Document Number: PROCESSER 5/7(POWER3)
Rev: 1A	
Date: Tuesday, February 15, 2011	Sheet 7 of 42





CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 6/7(CFG)	1A

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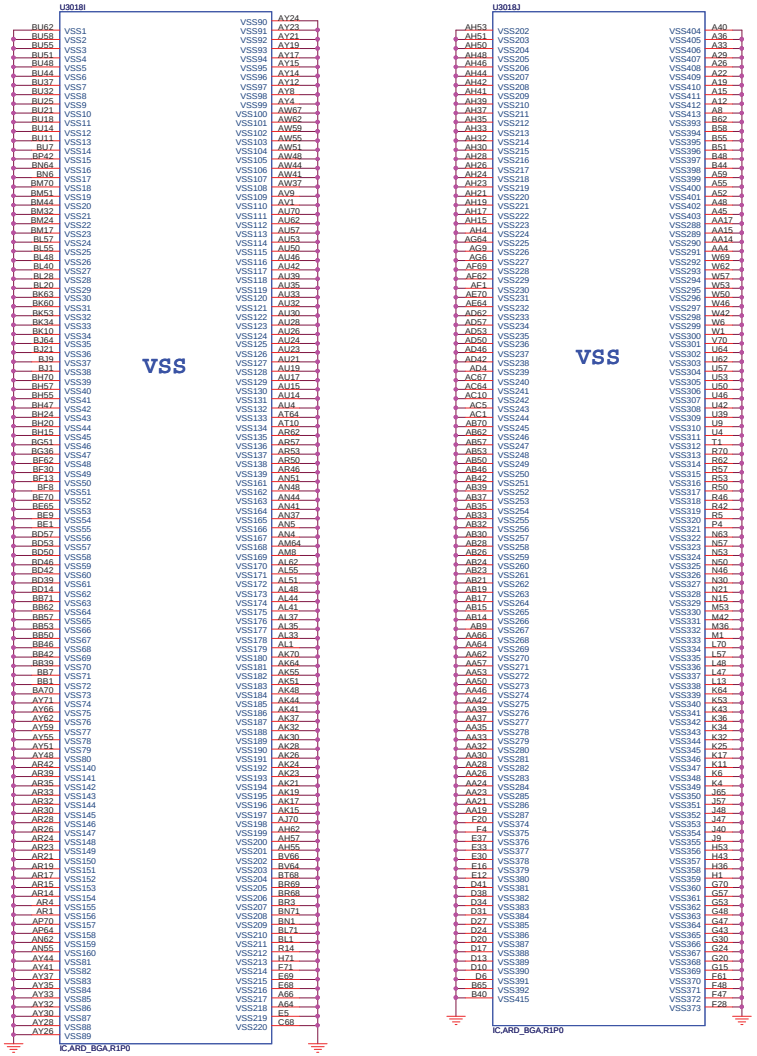
ARRANDALE PROCESSOR (GND)

09



PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 7/7(GND)	1A

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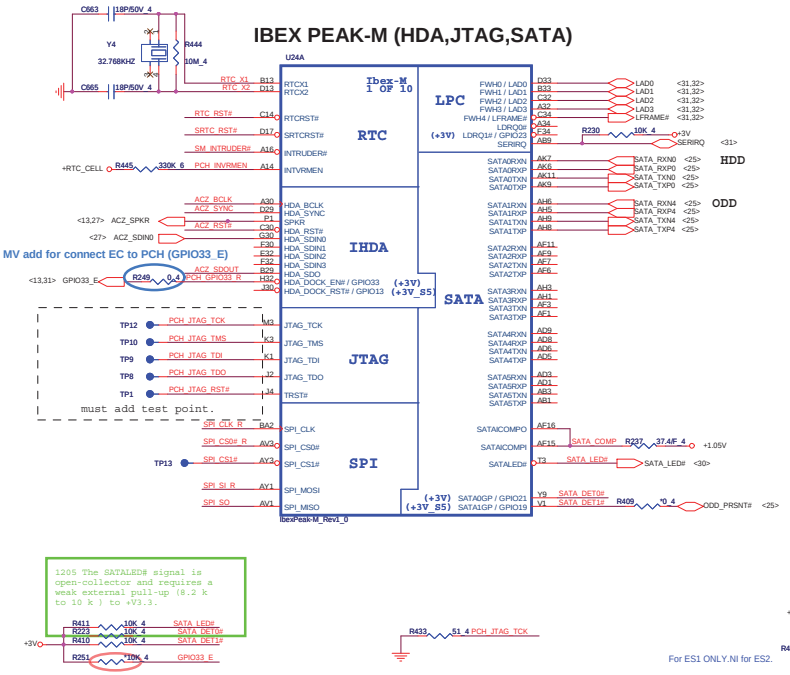
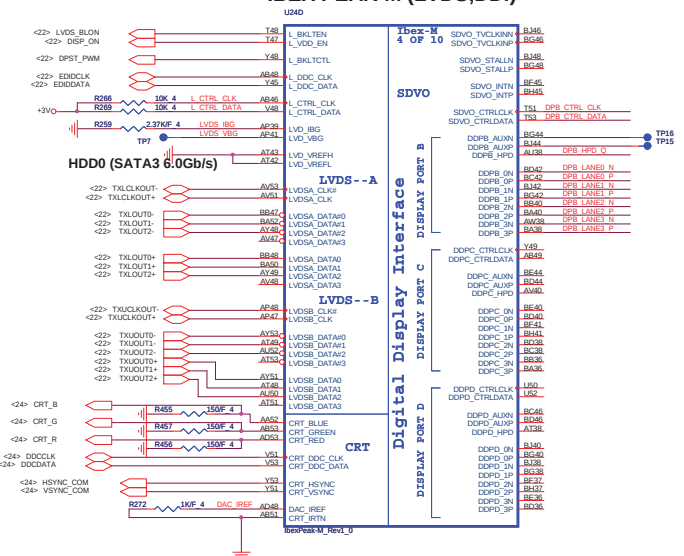
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)



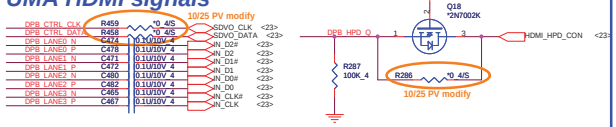
UMA CRT,LVDS&HDMI signals

IBEX PEAK-M (LVDS,DDI)



1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

UMA HDMI signals



For ES1 ONLY.NI for ES2.

For ES1 ONLY.NI for ES2.

Part
Part Number
Part Description

For AUDIO

For MDC

RTC

1mA

8/25 SI for M/E.

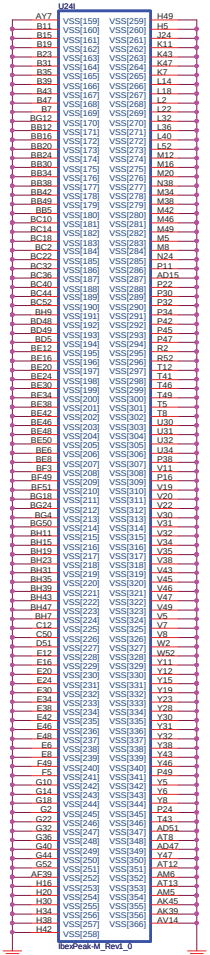
4M byte SPI ROM

W25Q32BVSSIG
AKE391P0N00
IC FLASH(8P) W25Q32BVSSIG(SOIC)

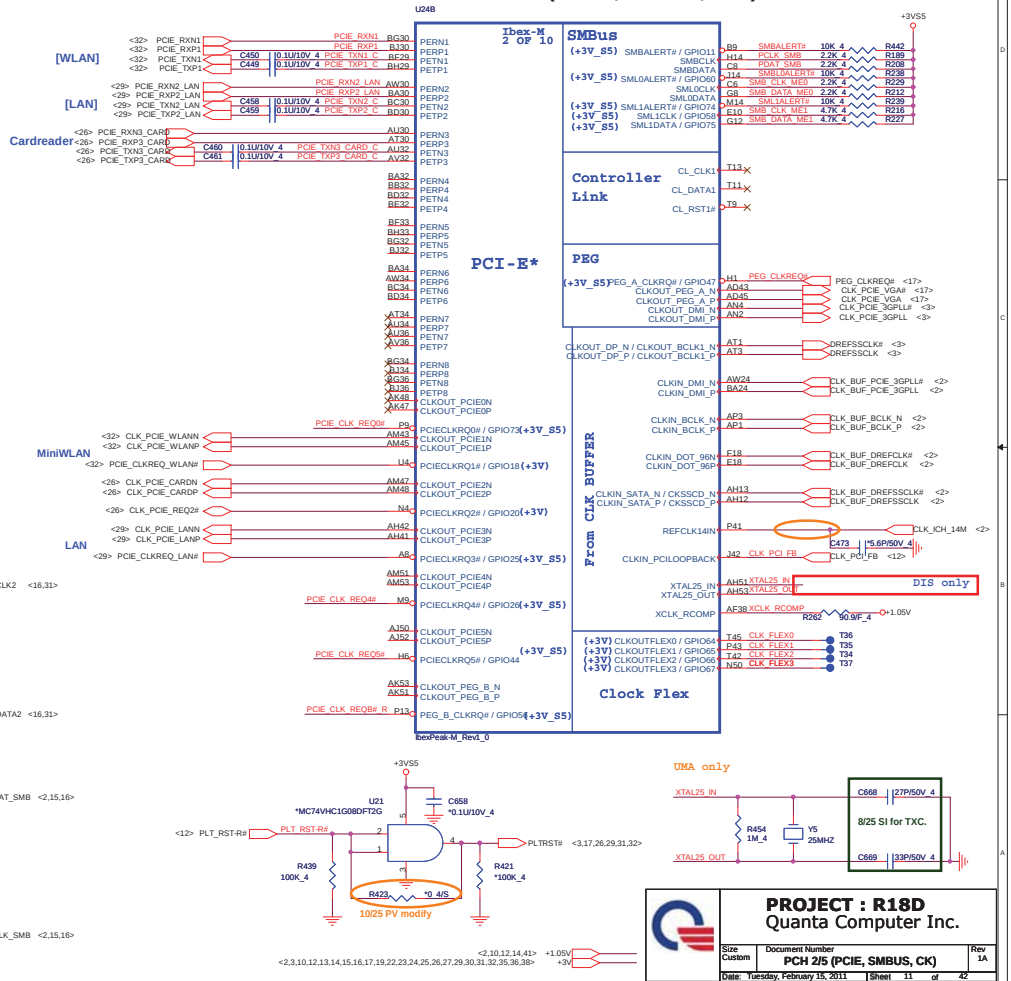
Vender
Socket DG008000031
EON - EN25F32-100HIP
AKE39FN0Q00 IC FLASH(8P) EN25F32-100HIP (SOIC)
WINBOND - W25Q32BVSSIG
AKE391P0N00 IC FLASH(8P) W25Q32BVSSIG(SOIC)

PROJECT : R18D			
Quanta Computer Inc.			
Size: Custom	Document Number: PCH 1/5 (SATA,HDA,LPC)		Rev: 1A
Date: Tuesday, February 15, 2011	Sheet 10 of 42		

IBEX PEAK-M (GND)

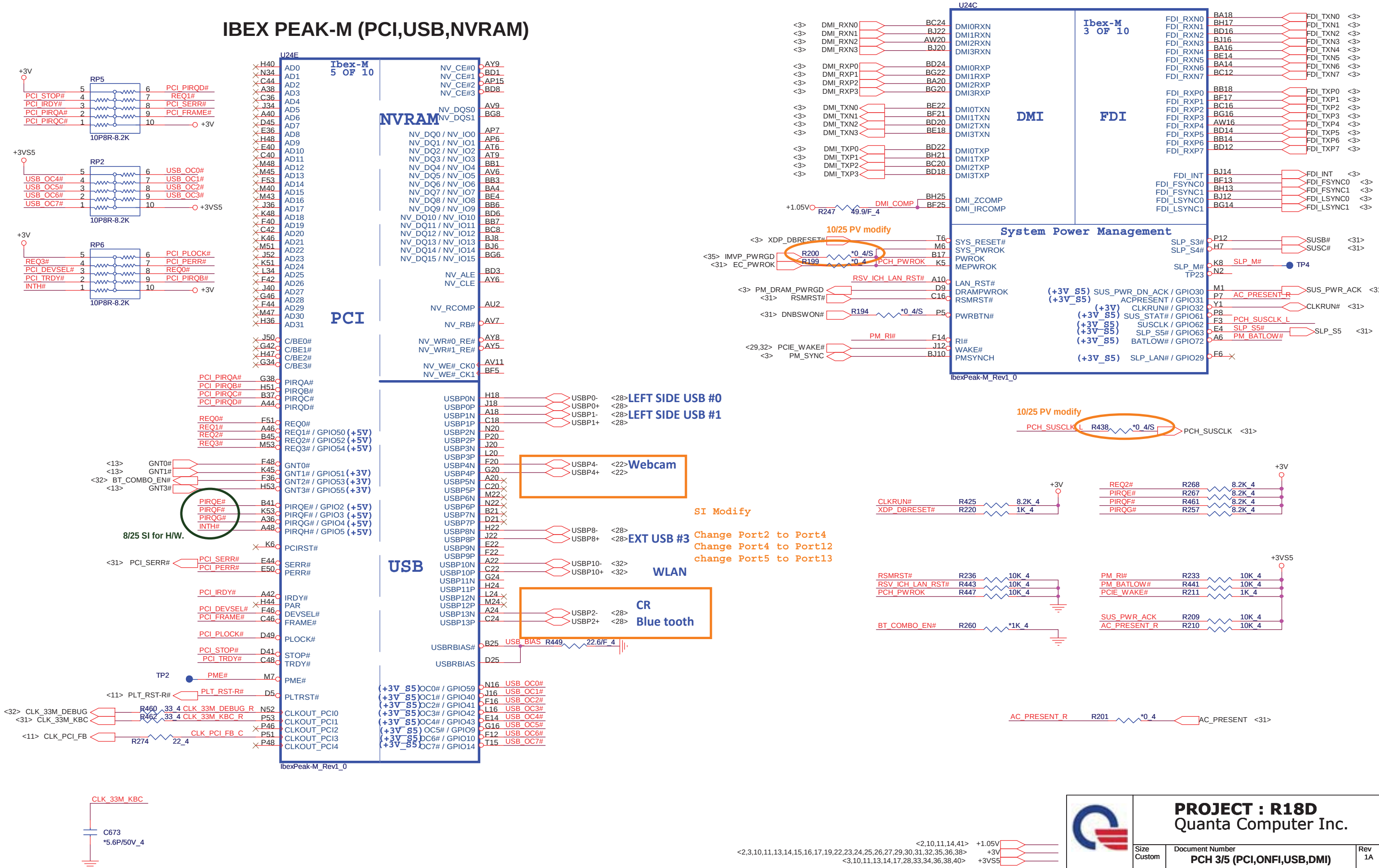


IBEX PEAK-M (PCI-E,SMBUS,CLK)



IBEX PEAK-M (DMI,FDI,GPIO)

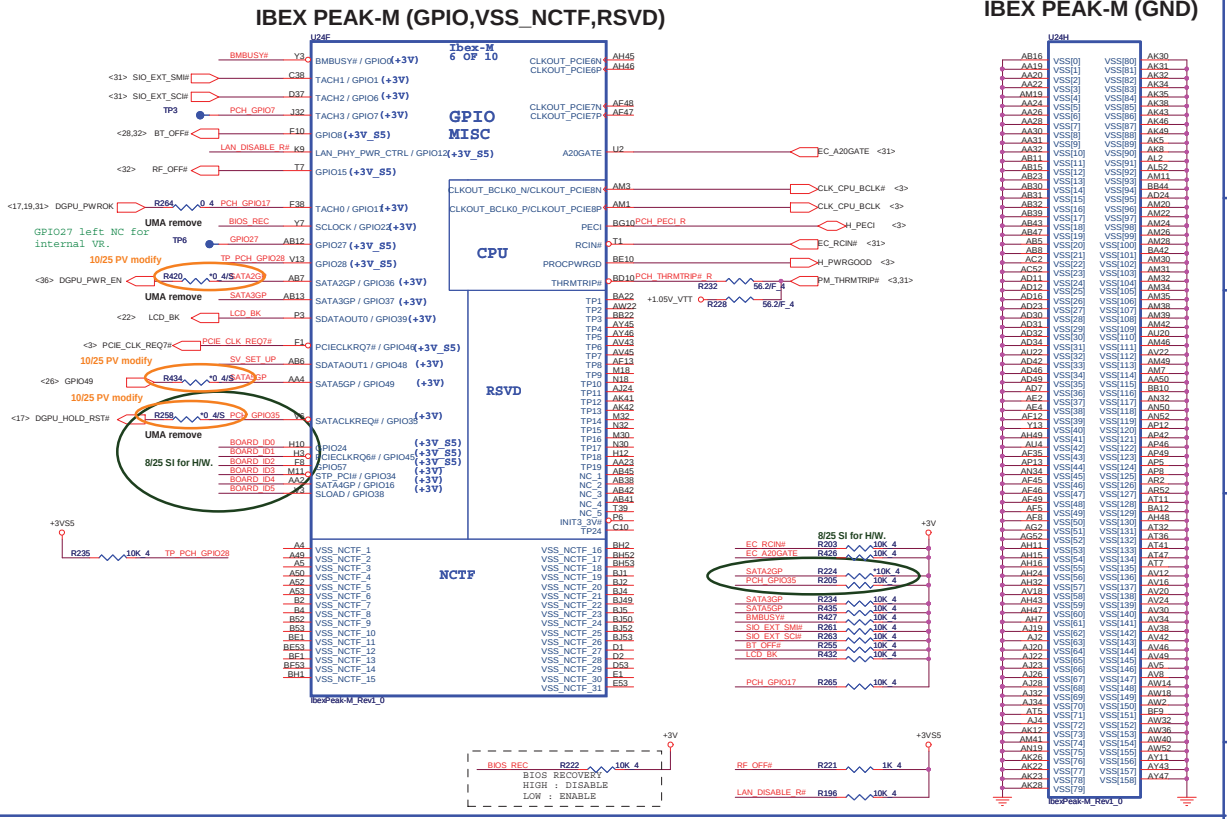
IBEX PEAK-M (PCI,USB,NVRAM)



PROJECT : R18D
Quanta Computer Inc.

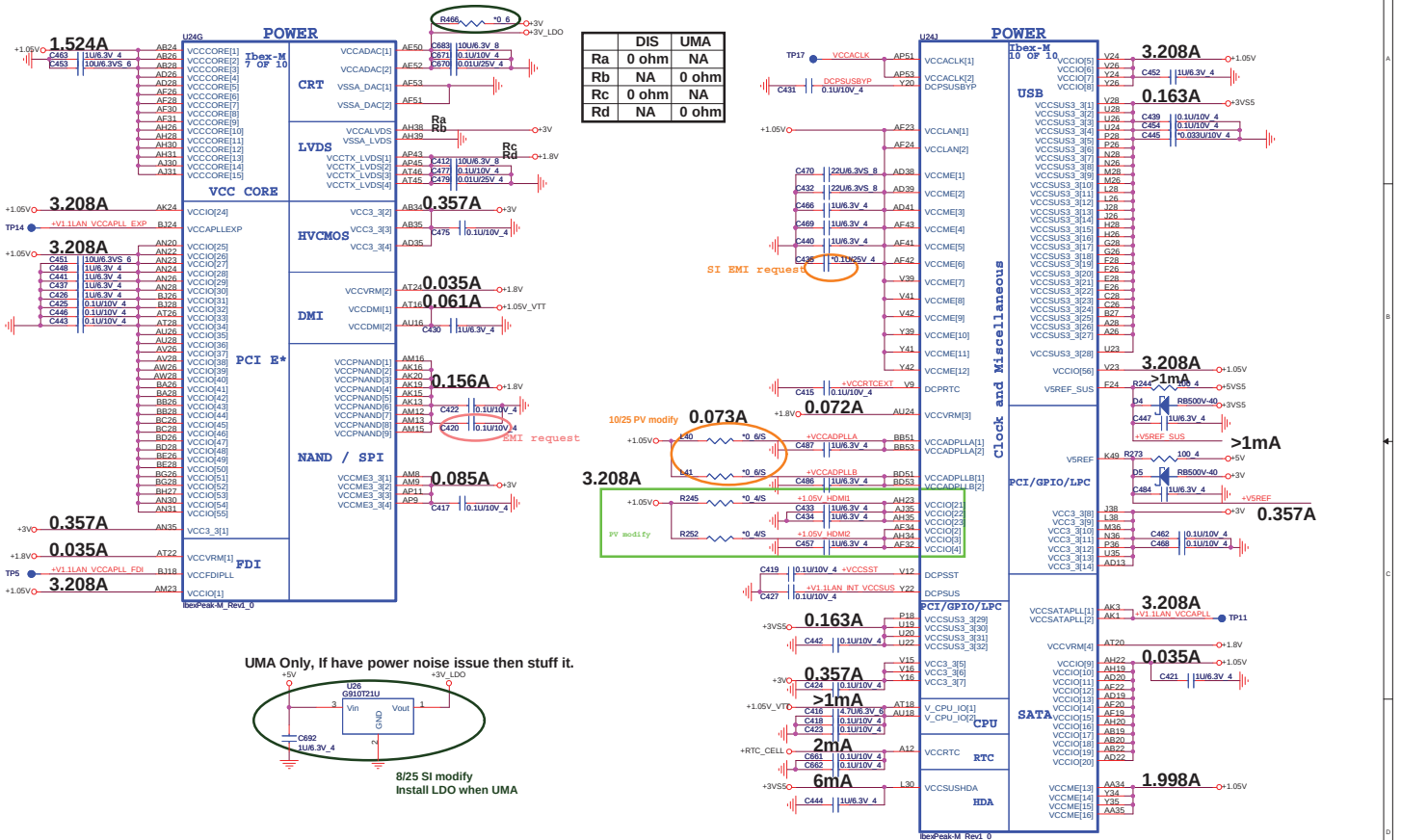
Size	Document Number	Rev
Custom	PCH 3/5 (PCI,ONFI,USB,DMI)	1A

Date: Tuesday, February 15, 2011 Sheet 12 of 42


IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)
U24F
Ibex-M
6 OF 10
GPIO MISC
CPU
RSVD
NCTF
BMBUSY# GPIO0 (+3V)
TACH1 / GPIO1 (+3V)
TACH2 / GPIO6 (+3V)
TACH3 / GPIO7 (+3V)
GPIO8 (+3V_S5)
LAN_PHY_PWR_CTRL / GPIO12 (+3V_S5)
GPIO15 (+3V_S5)
TACH0 / GPIO17 (+3V)
SCLOCK / GPIO22 (+3V)
GPIO27 (+3V_S5)
GPIO28 (+3V_S5)
SATA2GP / GPIO36 (+3V)
SATA3GP / GPIO37 (+3V)
SDATAOUT0 / GPIO39 (+3V)
PCIECLKRQ7# / GPIO46 (+3V_S5)
SDATAOUT1 / GPIO48 (+3V)
SATA5GP / GPIO49 (+3V)
SATACLKREQ# / GPIO35 (+3V)
GPIO24 (+3V_S5)
PCIECLKRQ6# / GPIO45 (+3V_S5)
GPIO67 (+3V)
STP_PCI# / GPIO34 (+3V)
SATA4GP / GPIO16 (+3V)
SLOAD / GPIO38 (+3V)
CLKOUT_PCIE6N
CLKOUT_PCIE6P
CLKOUT_PCIE7N
CLKOUT_PCIE7P
A20GATE
CLKOUT_BCLK0_N/CLKOUT_PCIEBN
CLKOUT_BCLK0_P/CLKOUT_PCIEBP
PECI
RCIN#
PROCPWRGD
THRMTRIP#
VSS_NCTF_1
VSS_NCTF_2
VSS_NCTF_3
VSS_NCTF_4
VSS_NCTF_5
VSS_NCTF_6
VSS_NCTF_7
VSS_NCTF_8
VSS_NCTF_9
VSS_NCTF_10
VSS_NCTF_11
VSS_NCTF_12
VSS_NCTF_13
VSS_NCTF_14
VSS_NCTF_15
VSS_NCTF_16
VSS_NCTF_17
VSS_NCTF_18
VSS_NCTF_19
VSS_NCTF_20
VSS_NCTF_21
VSS_NCTF_22
VSS_NCTF_23
VSS_NCTF_24
VSS_NCTF_25
VSS_NCTF_26
VSS_NCTF_27
VSS_NCTF_28
VSS_NCTF_29
VSS_NCTF_30
VSS_NCTF_31
IbexPeak-M_Rev1_0
GPIO27 left NC for internal VR.
10/25 PV modify
UMA remove
8/25 SI for H/W.
BIOS RECOVERY
HIGH : DISABLE
LOW : ENABLE
IBEX PEAK-M (GND)
U24H
VSS[0] VSS[1] VSS[2] VSS[3] VSS[4] VSS[5] VSS[6] VSS[7] VSS[8] VSS[9] VSS[10] VSS[11] VSS[12] VSS[13] VSS[14] VSS[15] VSS[16] VSS[17] VSS[18] VSS[19] VSS[20] VSS[21] VSS[22] VSS[23] VSS[24] VSS[25] VSS[26] VSS[27] VSS[28] VSS[29] VSS[30] VSS[31] VSS[32] VSS[33] VSS[34] VSS[35] VSS[36] VSS[37] VSS[38] VSS[39] VSS[40] VSS[41] VSS[42] VSS[43] VSS[44] VSS[45] VSS[46] VSS[47] VSS[48] VSS[49] VSS[50] VSS[51] VSS[52] VSS[53] VSS[54] VSS[55] VSS[56] VSS[57] VSS[58] VSS[59] VSS[60] VSS[61] VSS[62] VSS[63] VSS[64] VSS[65] VSS[66] VSS[67] VSS[68] VSS[69] VSS[70] VSS[71] VSS[72] VSS[73] VSS[74] VSS[75] VSS[76] VSS[77] VSS[78] VSS[79]
VSS[80] VSS[81] VSS[82] VSS[83] VSS[84] VSS[85] VSS[86] VSS[87] VSS[88] VSS[89] VSS[90] VSS[91] VSS[92] VSS[93] VSS[94] VSS[95] VSS[96] VSS[97] VSS[98] VSS[99] VSS[100] VSS[101] VSS[102] VSS[103] VSS[104] VSS[105] VSS[106] VSS[107] VSS[108] VSS[109] VSS[110] VSS[111] VSS[112] VSS[113] VSS[114] VSS[115] VSS[116] VSS[117] VSS[118] VSS[119] VSS[120] VSS[121] VSS[122] VSS[123] VSS[124] VSS[125] VSS[126] VSS[127] VSS[128] VSS[129] VSS[130] VSS[131] VSS[132] VSS[133] VSS[134] VSS[135] VSS[136] VSS[137] VSS[138] VSS[139] VSS[140] VSS[141] VSS[142] VSS[143] VSS[144] VSS[145] VSS[146] VSS[147] VSS[148] VSS[149] VSS[150] VSS[151] VSS[152] VSS[153] VSS[154] VSS[155] VSS[156] VSS[157] VSS[158]
IbexPeak-M_Rev1_0
R12 MB P/N
ID0 ID1 ID2 ID3 ID4 ID5
UMA
31R12MB0000 (PIM) 0 0 0 0 0 0
31R12MB0010 (PDT) 0 0 0 0 0 0
Seymour XT Hynix 512
31R12MB0020 (PIM) 1 0 0 0 0 0
31R12MB0030 (PDT) 1 0 0 0 0 0
Samsung 512
31R12MB0040 (PIM) 1 0 0 0 0 0
31R12MB0050 (PDT) 1 0 0 0 0 0
Hynix 1G
31R12MB0060 (PIM) 1 0 0 0 0 0
31R12MB0070 (PDT) 1 0 0 0 0 0
Samsung 1G
31R12MB0080 (PIM) 1 0 0 0 0 0
31R12MB0090 (PDT) 1 0 0 0 0 0
Board ID
ID0 GPIO24
ID1 GPIO45
ID2 GPIO57
ID3 GPIO34
ID4 GPIO35
ID5 GPIO38
UMA/DIS 0=UMA 1=Dis.
1.1/1.0 1=1.1 0=1.0
Reserve 0=No 1=Yes
Reserve 0=No 1=Yes
Reserve 0=No 1=Yes
Reserve 0=No 1=Yes
BOARD_ID1設成HIGH代表Rockey 1.1
RU0 RU1 RU2 RU3 RU4 RU5
RD0 RD1 RD2 RD3 RD4 RD5
BOARD_ID0 BOARD_ID1 BOARD_ID2 BOARD_ID3 BOARD_ID4 BOARD_ID5
8/25 SI for H/W.
A16 swap override Strap/Top-Block Swap Override jumper
GNT3# Low = A16 swap override/Top-Block Swap Override enabled High = Default
SV_SET_UP 1-X High = Strong (Default)
Boot BIOS Strap
PCI_GNT0# GNT#1 Boot BIOS Location
0 0 LPC
0 1 Reserved (NAND)
1 0 PCI
1 1 SPI
Danbury Technology Enabled
NV_ALE High = Enable Low = Disable
DMI Termination Voltage
NV_CLE Set to Vcc when LOW Set to Vcc/2 when HIGH
No Reboot Strap

8/25 SI modify
Uninstall on UMA
Install on DIS

	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	NA	0 ohm
Rd	NA	0 ohm



UMA Only, If have power noise issue then stuff it.

8/25 SI modify
Install LDO when UMA

<2,10,11,12,41> +1.05V
<3,5,6,13,31,34,35,36,40> +1.05V_VTT
<5,34> +1.8V
<2,3,10,11,12,13,15,16,17,19,22,23,24,25,26,27,29,30,31,32,35,36,38> +3V
<3,10,11,12,13,17,28,33,34,36,38,40> +3VS5
<23,24,25,27,30,32,38> +5V
<22,28,33,34,35,36,37,38,40,41> +5VS5

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/5 (POWER)	1A

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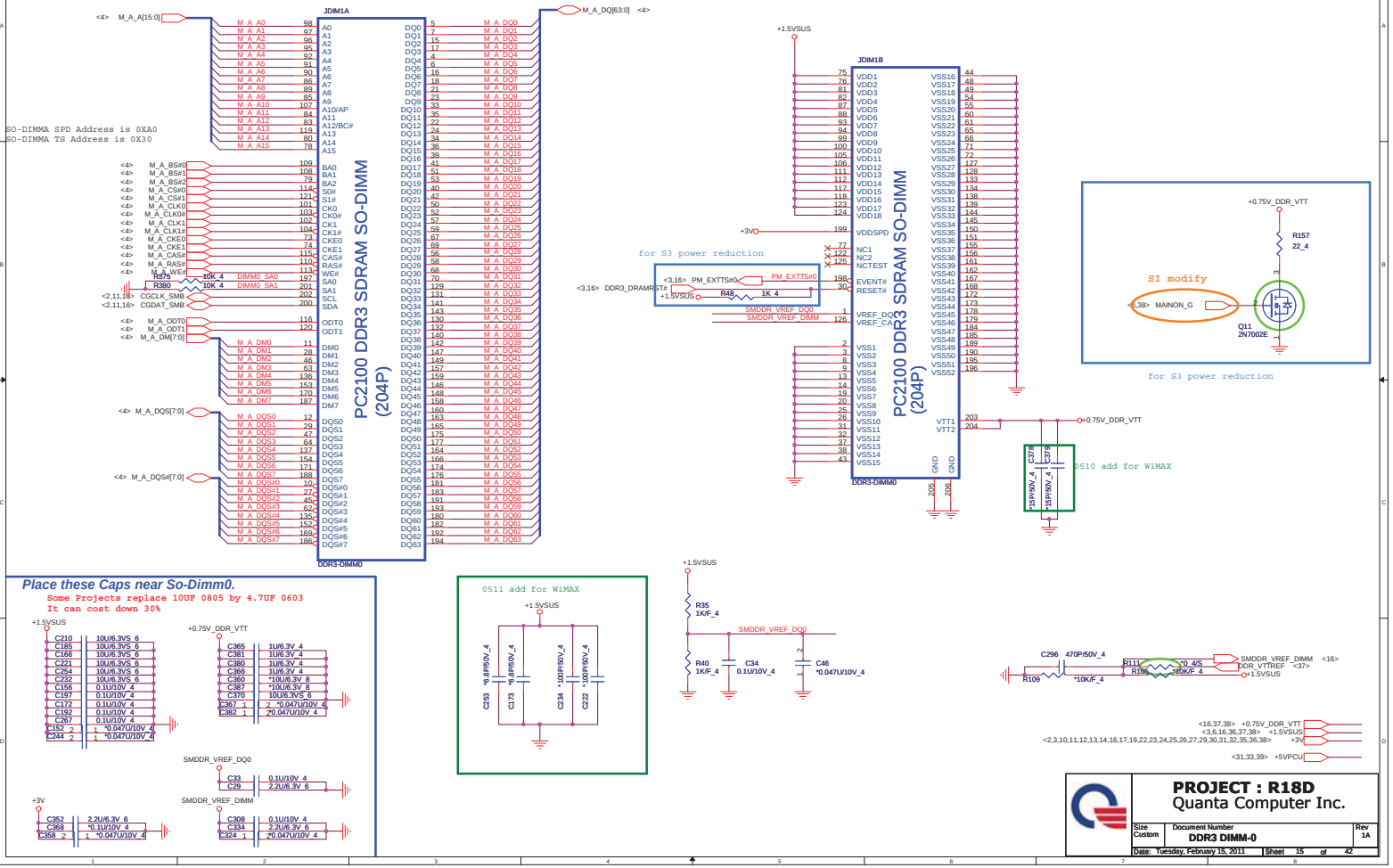
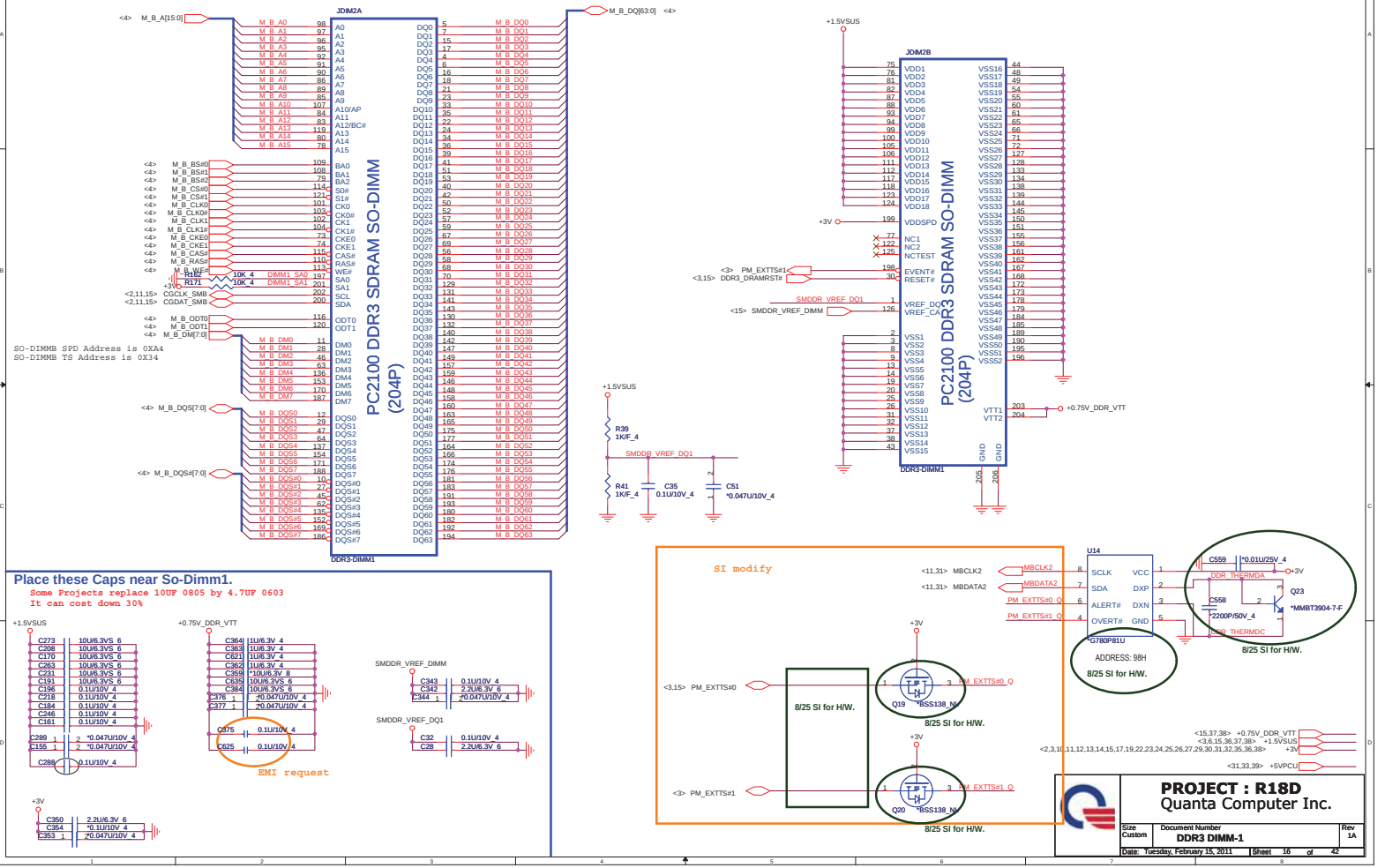
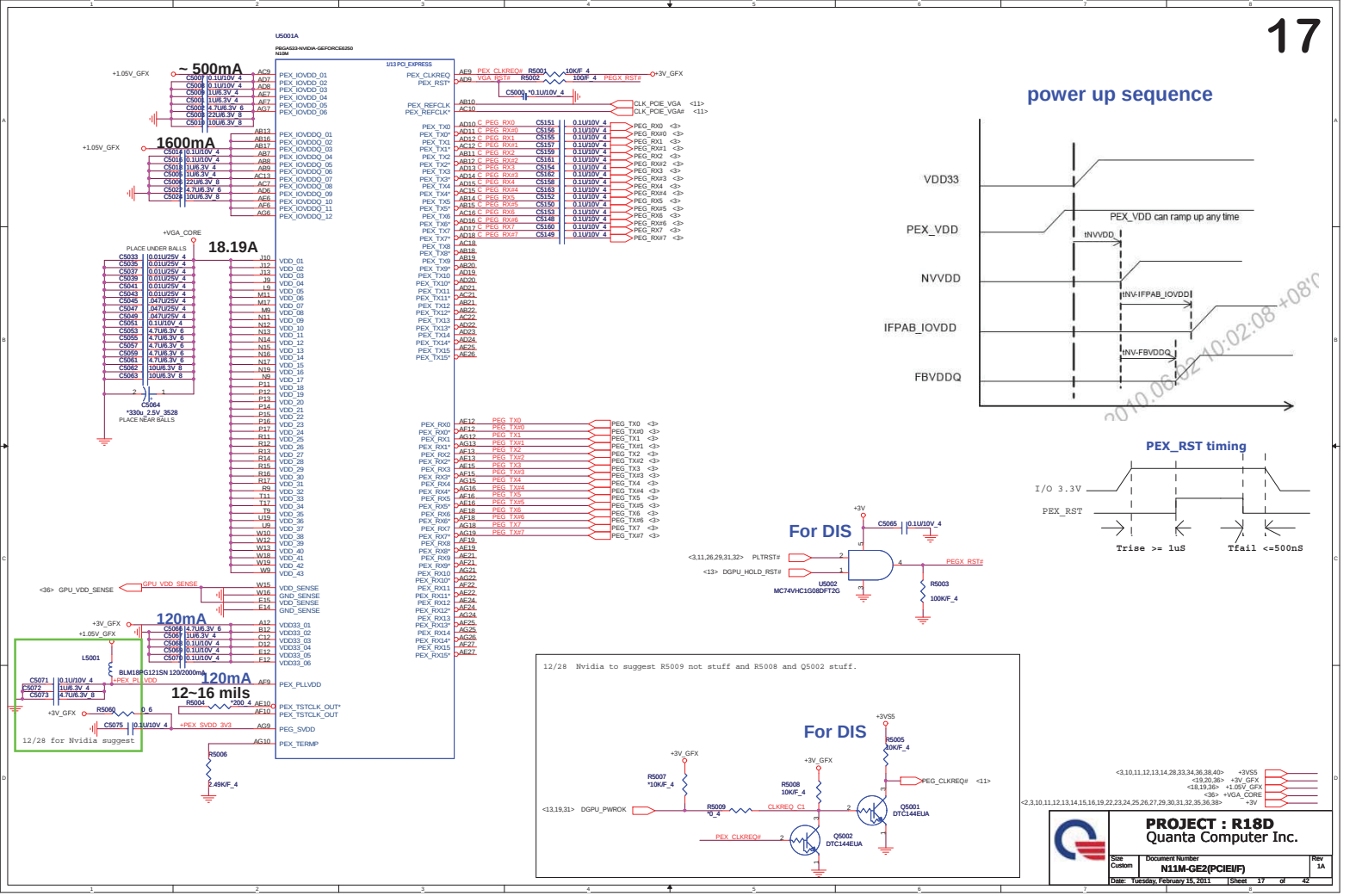
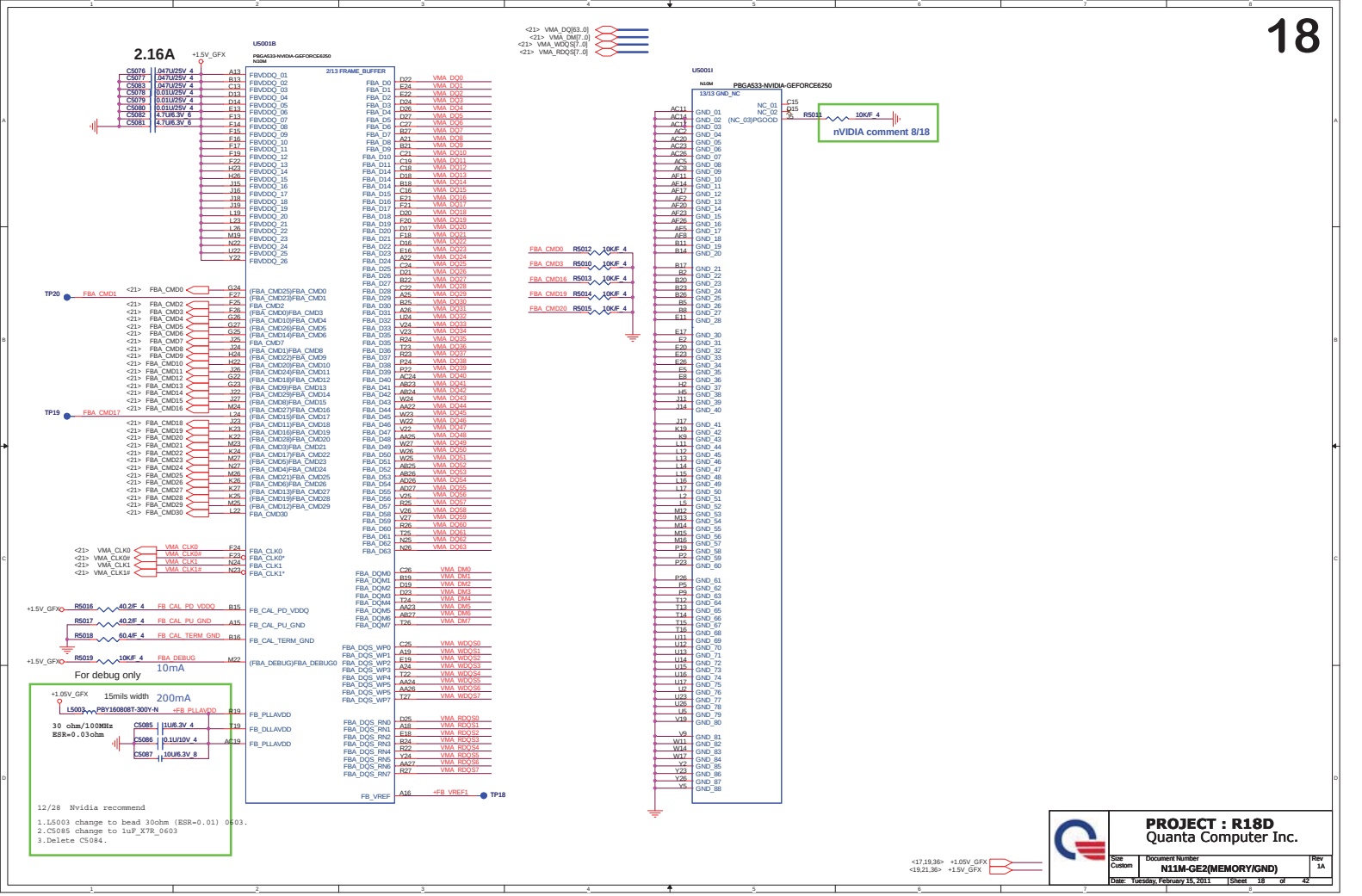


PROJECT : R18D	
Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 DIMM-0
Rev: 1A	
Date: Tuesday, February 15, 2011	Sheet 15 of 42


JDIM2A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1
JDIM2B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1
SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34
Place these Caps near So-Dimm1.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%
EMI request
SI modify
8/25 SI for H/W.
ADDRESS: 98H
U14
*G780P81U
*MMBT3904-7-F
*BSS138_NL
PROJECT : R18D
Quanta Computer Inc.
DDR3 DIMM-1
Tuesday, February 15, 2011


~ 500mA
1600mA
18.19A
120mA
120mA
12~16 mils
12/28 for Nvidia suggest
power up sequence
VDD33
PEX_VDD
NVVDD
IFPAB_IOVDD
FBVDDQ
PEX_VDD can ramp up any time
tNVVDD
tNV-IFPAB_IOVDD
tNV-FBVDDQ
PEX_RST timing
I/O 3.3V
PEX_RST
Trise >= 1uS
Tfail <=500nS
For DIS
For DIS
12/28 Nvidia to suggest R5009 not stuff and R5008 and Q5002 stuff.
PROJECT : R18D
Quanta Computer Inc.
N11M-GE2(PCIEI/F)
Tuesday, February 15, 2011


2.16A
+1.5V_GFX
U5001B
PBGA533-NVIDIA-GEFORCE6250
N10M
2/13 FRAME_BUFFER
C5076 .047U/25V_4
C5077 .047U/25V_4
C5083 .047U/25V_4
C5078 0.01U/25V_4
C5079 0.01U/25V_4
C5080 0.01U/25V_4
C5082 4.7U/6.3V_6
C5081 4.7U/6.3V_6
FBVDDQ_01 FBVDDQ_02 FBVDDQ_03 FBVDDQ_04 FBVDDQ_05 FBVDDQ_06 FBVDDQ_07 FBVDDQ_08 FBVDDQ_09 FBVDDQ_10 FBVDDQ_11 FBVDDQ_12 FBVDDQ_13 FBVDDQ_14 FBVDDQ_15 FBVDDQ_16 FBVDDQ_17 FBVDDQ_18 FBVDDQ_19 FBVDDQ_20 FBVDDQ_21 FBVDDQ_22 FBVDDQ_23 FBVDDQ_24 FBVDDQ_25 FBVDDQ_26
FBA_D0 FBA_D1 FBA_D2 FBA_D3 FBA_D4 FBA_D5 FBA_D6 FBA_D7 FBA_D8 FBA_D9 FBA_D10 FBA_D11 FBA_D12 FBA_D13 FBA_D14 FBA_D15 FBA_D16 FBA_D17 FBA_D18 FBA_D19 FBA_D20 FBA_D21 FBA_D22 FBA_D23 FBA_D24 FBA_D25 FBA_D26 FBA_D27 FBA_D28 FBA_D29 FBA_D30 FBA_D31 FBA_D32 FBA_D33 FBA_D34 FBA_D35 FBA_D36 FBA_D37 FBA_D38 FBA_D39 FBA_D40 FBA_D41 FBA_D42 FBA_D43 FBA_D44 FBA_D45 FBA_D46 FBA_D47 FBA_D48 FBA_D49 FBA_D50 FBA_D51 FBA_D52 FBA_D53 FBA_D54 FBA_D55 FBA_D56 FBA_D57 FBA_D58 FBA_D59 FBA_D60 FBA_D61 FBA_D62 FBA_D63
VMA_DQ0 VMA_DQ1 VMA_DQ2 VMA_DQ3 VMA_DQ4 VMA_DQ5 VMA_DQ6 VMA_DQ7 VMA_DQ8 VMA_DQ9 VMA_DQ10 VMA_DQ11 VMA_DQ12 VMA_DQ13 VMA_DQ14 VMA_DQ15 VMA_DQ16 VMA_DQ17 VMA_DQ18 VMA_DQ19 VMA_DQ20 VMA_DQ21 VMA_DQ22 VMA_DQ23 VMA_DQ24 VMA_DQ25 VMA_DQ26 VMA_DQ27 VMA_DQ28 VMA_DQ29 VMA_DQ30 VMA_DQ31 VMA_DQ32 VMA_DQ33 VMA_DQ34 VMA_DQ35 VMA_DQ36 VMA_DQ37 VMA_DQ38 VMA_DQ39 VMA_DQ40 VMA_DQ41 VMA_DQ42 VMA_DQ43 VMA_DQ44 VMA_DQ45 VMA_DQ46 VMA_DQ47 VMA_DQ48 VMA_DQ49 VMA_DQ50 VMA_DQ51 VMA_DQ52 VMA_DQ53 VMA_DQ54 VMA_DQ55 VMA_DQ56 VMA_DQ57 VMA_DQ58 VMA_DQ59 VMA_DQ60 VMA_DQ61 VMA_DQ62 VMA_DQ63
<21> VMA_DQ[63..0]
<21> VMA_DM[7..0]
<21> VMA_WDQS[7..0]
<21> VMA_RDQS[7..0]
TP20 FBA_CMD1
<21> FBA_CMD0 <21> FBA_CMD2 <21> FBA_CMD3 <21> FBA_CMD4 <21> FBA_CMD5 <21> FBA_CMD6 <21> FBA_CMD7 <21> FBA_CMD8 <21> FBA_CMD9 <21> FBA_CMD10 <21> FBA_CMD11 <21> FBA_CMD12 <21> FBA_CMD13 <21> FBA_CMD14 <21> FBA_CMD15 <21> FBA_CMD16
(FBA_CMD25)FBA_CMD0 (FBA_CMD23)FBA_CMD1 FBA_CMD2 (FBA_CMD0)FBA_CMD3 (FBA_CMD10)FBA_CMD4 (FBA_CMD26)FBA_CMD5 (FBA_CMD14)FBA_CMD6 FBA_CMD7 (FBA_CMD1)FBA_CMD8 (FBA_CMD22)FBA_CMD9 (FBA_CMD20)FBA_CMD10 (FBA_CMD24)FBA_CMD11 (FBA_CMD18)FBA_CMD12 (FBA_CMD9)FBA_CMD13 (FBA_CMD29)FBA_CMD14 (FBA_CMD8)FBA_CMD15 (FBA_CMD27)FBA_CMD16 (FBA_CMD15)FBA_CMD17 (FBA_CMD11)FBA_CMD18 (FBA_CMD16)FBA_CMD19 (FBA_CMD28)FBA_CMD20 (FBA_CMD3)FBA_CMD21 (FBA_CMD17)FBA_CMD22 (FBA_CMD5)FBA_CMD23 (FBA_CMD4)FBA_CMD24 (FBA_CMD21)FBA_CMD25 (FBA_CMD6)FBA_CMD26 (FBA_CMD13)FBA_CMD27 (FBA_CMD19)FBA_CMD28 (FBA_CMD12)FBA_CMD29 FBA_CMD30
TP19 FBA_CMD17
<21> VMA_CLK0 <21> VMA_CLK0# <21> VMA_CLK1 <21> VMA_CLK1#
VMA_CLK0 VMA_CLK0# VMA_CLK1 VMA_CLK1#
FBA_CLK0 FBA_CLK0* FBA_CLK1 FBA_CLK1*
FBA_DQM0 FBA_DQM1 FBA_DQM2 FBA_DQM3 FBA_DQM4 FBA_DQM5 FBA_DQM6 FBA_DQM7
VMA_DM0 VMA_DM1 VMA_DM2 VMA_DM3 VMA_DM4 VMA_DM5 VMA_DM6 VMA_DM7
+1.5V_GFX R5016 40.2/F_4 FB_CAL_PD_VDDQ
R5017 40.2/F_4 FB_CAL_PU_GND
R5018 60.4/F_4 FB_CAL_TERM_GND
+1.5V_GFX R5019 10K/F_4 FBA_DEBUG
10mA
For debug only
FB_CAL_PD_VDDQ FB_CAL_PU_GND FB_CAL_TERM_GND
(FBA_DEBUG)FBA_DEBUG0
FBA_DQS_WP0 FBA_DQS_WP1 FBA_DQS_WP2 FBA_DQS_WP3 FBA_DQS_WP4 FBA_DQS_WP5 FBA_DQS_WP6 FBA_DQS_WP7
VMA_WDQS0 VMA_WDQS1 VMA_WDQS2 VMA_WDQS3 VMA_WDQS4 VMA_WDQS5 VMA_WDQS6 VMA_WDQS7
FBA_DQS_RN0 FBA_DQS_RN1 FBA_DQS_RN2 FBA_DQS_RN3 FBA_DQS_RN4 FBA_DQS_RN5 FBA_DQS_RN6 FBA_DQS_RN7
VMA_RDQS0 VMA_RDQS1 VMA_RDQS2 VMA_RDQS3 VMA_RDQS4 VMA_RDQS5 VMA_RDQS6 VMA_RDQS7
FB_PLLAVDD FB_DLLAVDD FB_PLLAVDD
+1.05V_GFX 15mils width 200mA
L5003 PBY160808T-300Y-N +FB_PLLAVDD
30 ohm/100MHz ESR=0.03ohm
C5085 1U/6.3V_4 C5086 0.1U/10V_4 C5087 10U/6.3V_8
12/28 Nvidia recommend
1.L5003 change to bead 30ohm (ESR=0.01) 0603.
2.C5085 change to 1uF_X7R_0603
3.Delete C5084.
FB_VREF A16 +FB_VREF1 TP18
FBA_CMD0 R5012 10K/F_4
FBA_CMD3 R5010 10K/F_4
FBA_CMD16 R5013 10K/F_4
FBA_CMD19 R5014 10K/F_4
FBA_CMD20 R5015 10K/F_4
US001I
N10M
PBGA533-NVIDIA-GEFORCE6250
13/13 GND_NC
GND_01 GND_02 GND_03 GND_04 GND_05 GND_06 GND_07 GND_08 GND_09 GND_10 GND_11 GND_12 GND_13 GND_14 GND_15 GND_16 GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_25 GND_26 GND_27 GND_28 GND_30 GND_31 GND_32 GND_33 GND_34 GND_35 GND_36 GND_37 GND_38 GND_39 GND_40 GND_41 GND_42 GND_43 GND_44 GND_45 GND_46 GND_47 GND_48 GND_49 GND_50 GND_51 GND_52 GND_53 GND_54 GND_55 GND_56 GND_57 GND_58 GND_59 GND_60 GND_61 GND_62 GND_63 GND_64 GND_65 GND_66 GND_67 GND_68 GND_69 GND_70 GND_71 GND_72 GND_73 GND_74 GND_75 GND_76 GND_77 GND_78 GND_79 GND_80 GND_81 GND_82 GND_83 GND_84 GND_85 GND_86 GND_87 GND_88
NC_01 NC_02 (NC_03)PGOOD
C515 R5018 10K/F_4
nVIDIA comment 8/18
<17,19,36> +1.05V_GFX
<19,21,36> +1.5V_GFX
PROJECT : R18D
Quanta Computer Inc.
Size Custom
Document Number N11M-GE2(MEMORY/GND)
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Optimus:
All unstuff , one Cap stuff 10K ohm
Optimus:
All unstuff , one Cap stuff 10K ohm
Optimus:
All unstuff , one Cap stuff 10K ohm
12/28 for Nvidia suggest
65mA
50mA
45mA
3V: Nvidia suggest
PROJECT : R18D
Quanta Computer Inc.
N11M-GE2(DISPLAY)
Tuesday, February 15, 2011

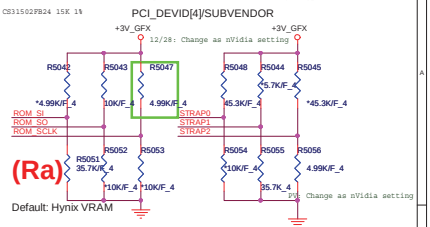
N12P-GV -> 0x17F

N12M-GE -> 0xA7A 1010 ->PU15K

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix		PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung		PD 20K
0110	DDR3 128Mx16x4, 128bit, 1GB,800MHz	Hynix		PD 35K
0111	DDR3 128Mx16x4, 128bit, 1GB,800MHz	Samsung		PD 45K
XXXX				
XXXX				

(Ra)

ROM_SI -> based on VRAM.

ROM_SO -> PU 10K

ROM_SCLK -> PU 5K

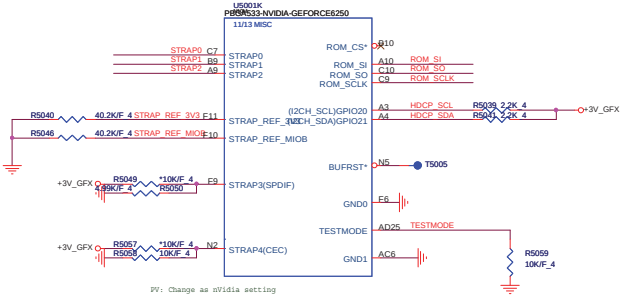
STRAP0 -> PU 45K

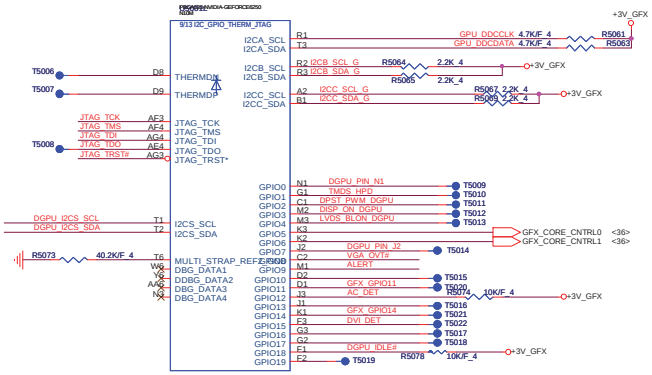
STRAP1 -> PD 35K

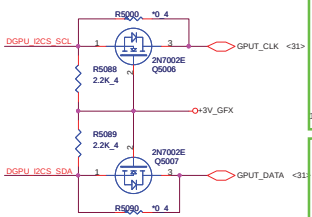
STRAP2 -> PD 5K

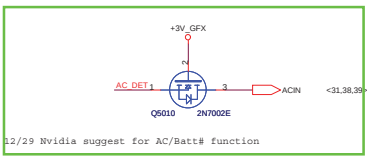
STRAP3 -> PD 5K

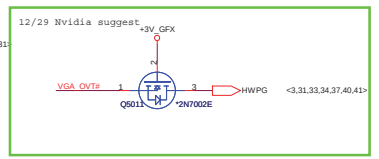
STRAP 4 -> PD 10K.

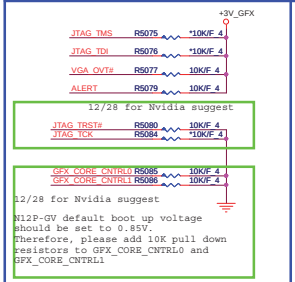












GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	Memory VREF SELECT
11	I/O	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	THERM_LOAD_STEP_DOWN
14	OUT	N/A	THERM_LOAD_STEP_UP

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	N12P-GV(GPIO/STRAPS)	1A

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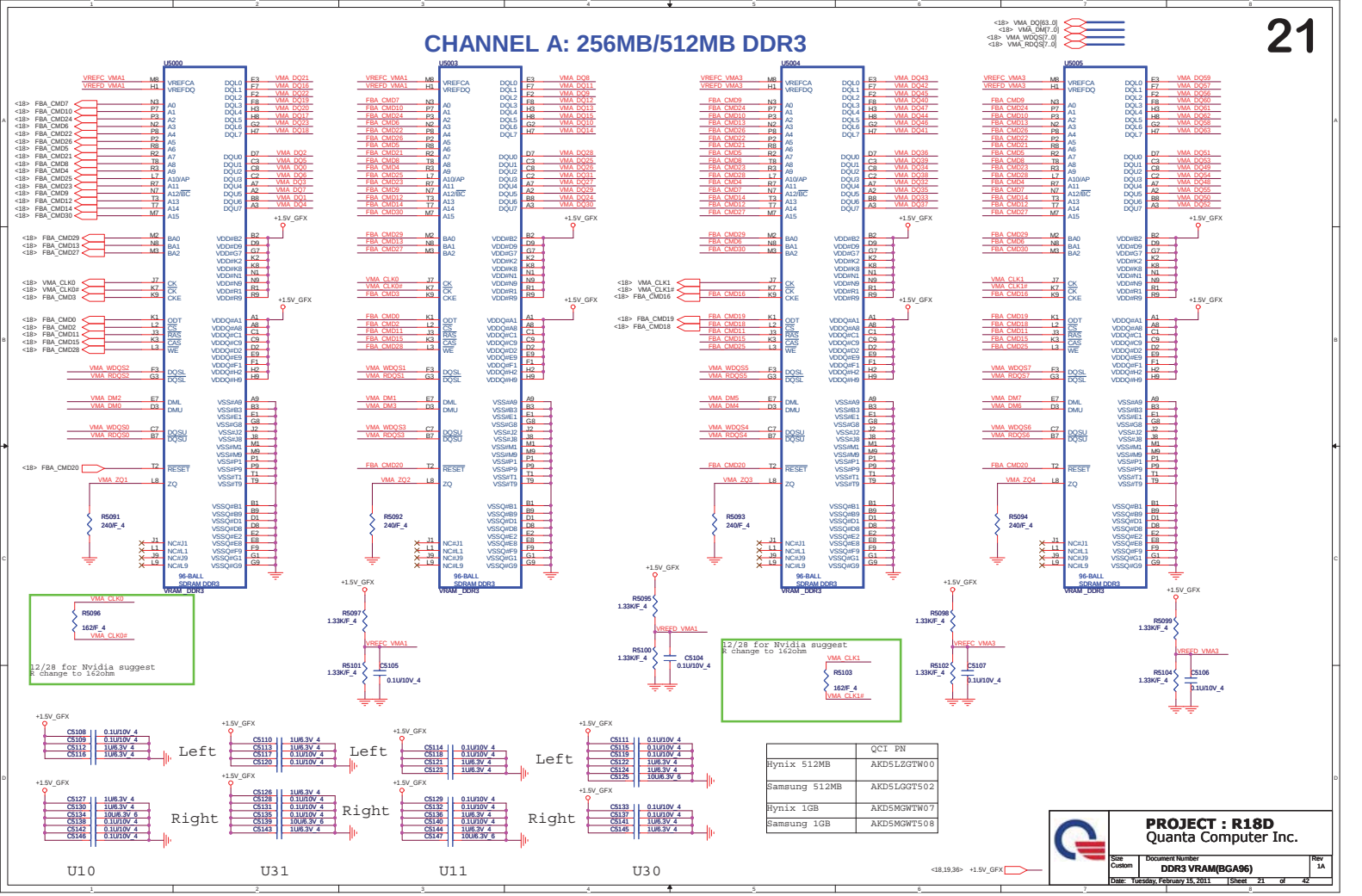
CHANNEL A: 256MB/512MB DDR3



	QCI PN
Hynix 512MB	AKD5LZGTW00
Samsung 512MB	AKD5LGGT502
Hynix 1GB	AKD5MGWTW07
Samsung 1GB	AKD5MGWT508

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 VRAM(BGA96)	1A
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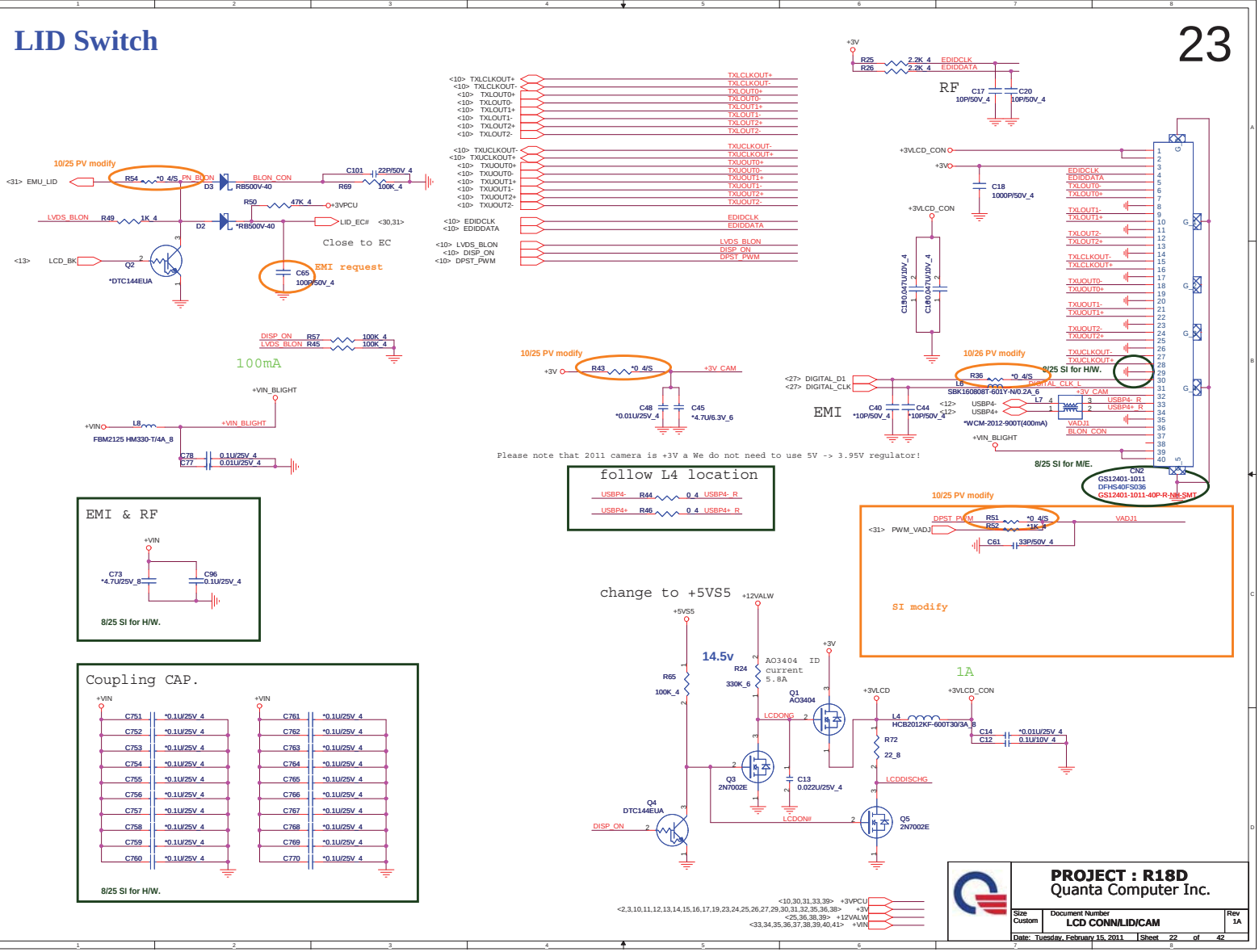
LID Switch



PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A

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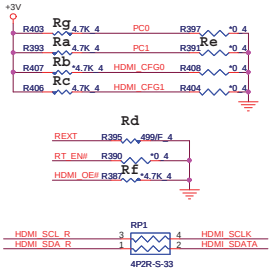
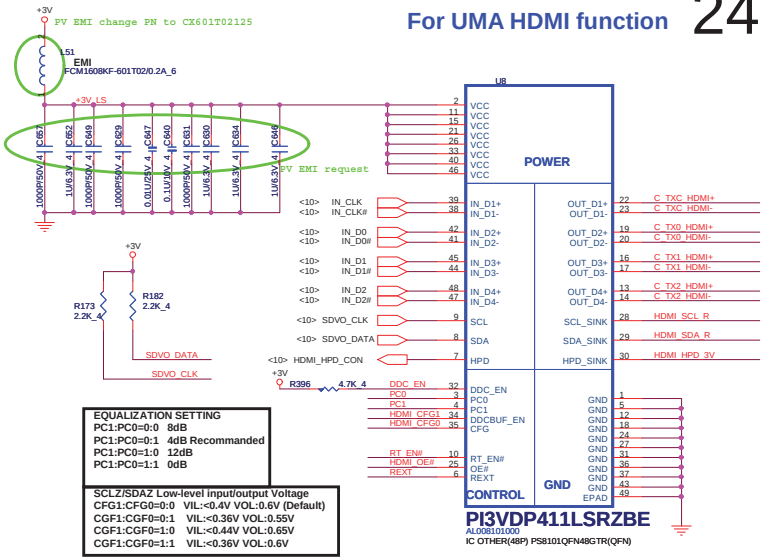
For UMA HDMI function

Signals		PDT	PIM	CHR
PC1	Ra	4.7K	4.7K	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	4.7K	1.2K
PC1	Re	NC	NC	4.7K
HDMI_OE#	Rf	NC	NC	4.7K
PC0	Rg	4.7K	4.7K	4.7K





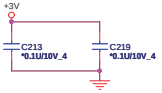
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

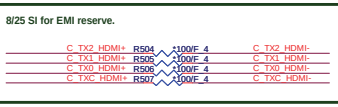
Vender	Part	Part Number	Part Description
PDT	PS8101	AL008101000	IC OTHER(48P) PS8101QFN48GTR(QFN)
PIM	PI3VDP411LSRZBE	ALP411LS004	IC OTHER(48P) PI3VDP411LSRZBE(TQFN)
CHR	CH7318C	AL007318002	IC OTHER(48P) CH7318C-BF-TR(QFN)

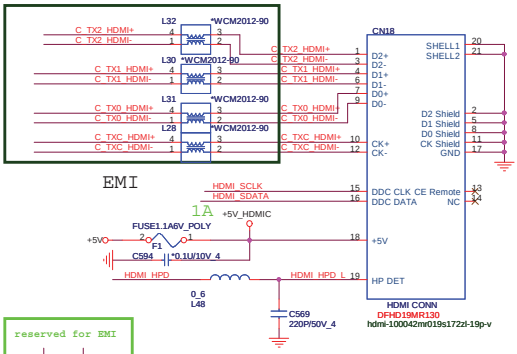
9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella

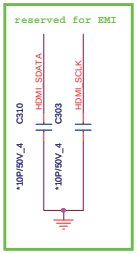
CHR : need Na R1182, add R1027 for capella

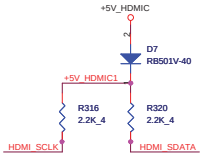


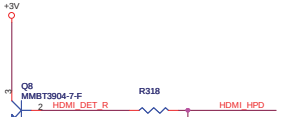
8/25 SI for EMI reserve.



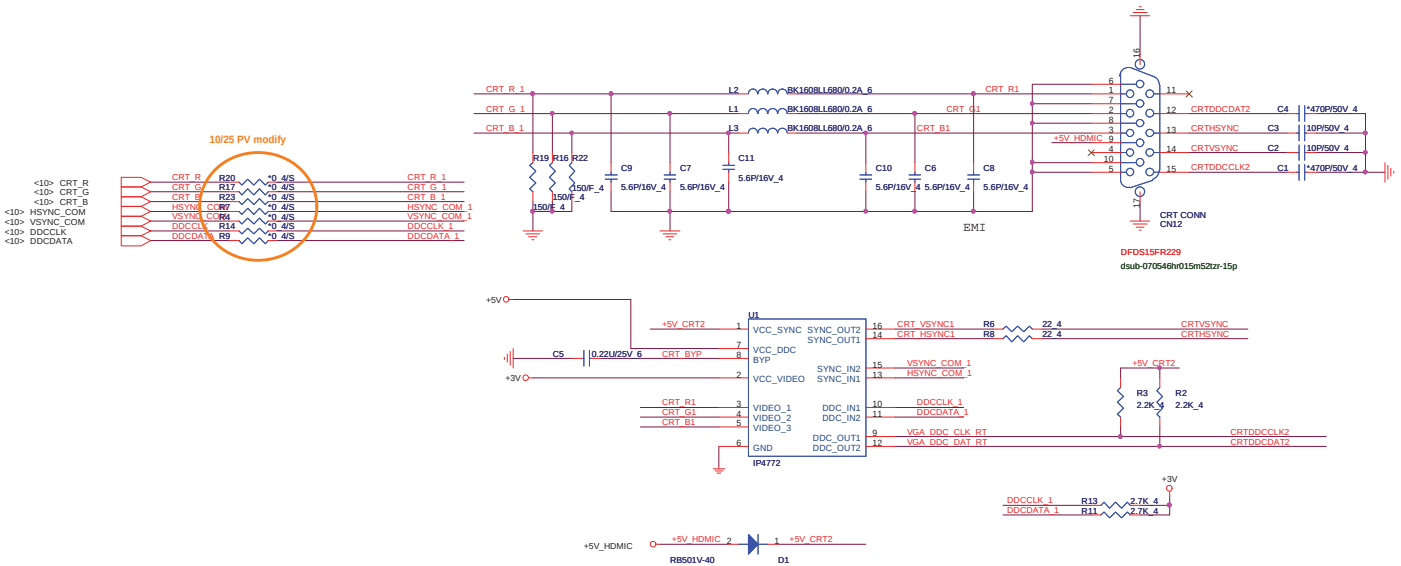




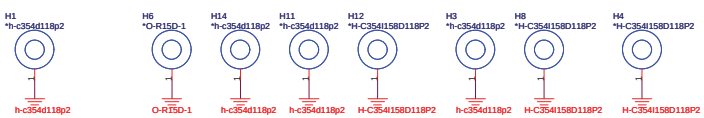




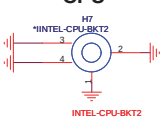
CRT PORT



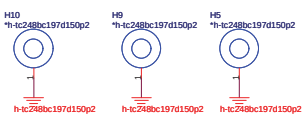
HOLE



CPU



VGA



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Quanta Computer Inc.

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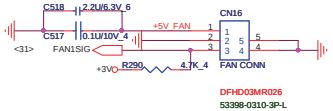
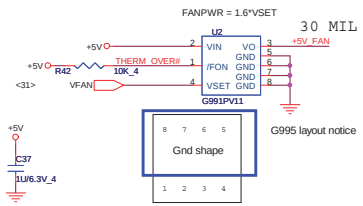
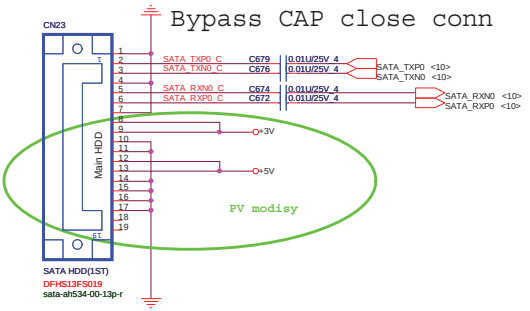
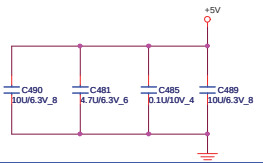
CPU FAN



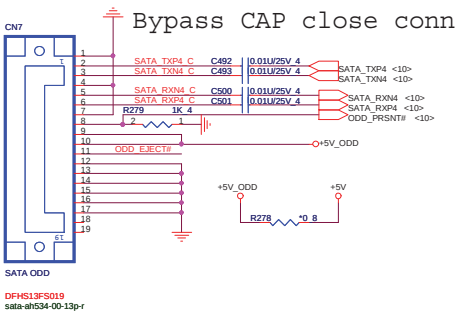


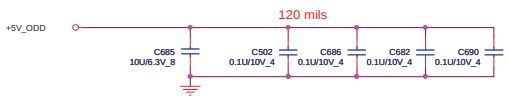
SATA HDD CONNECTOR



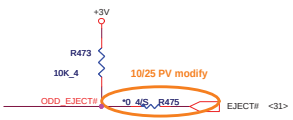


SATA ODD CONNECTOR

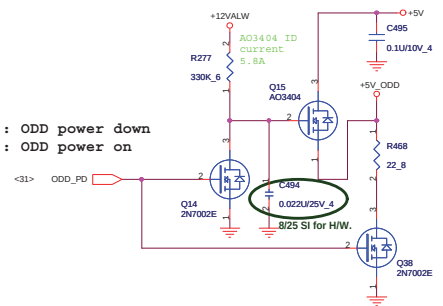




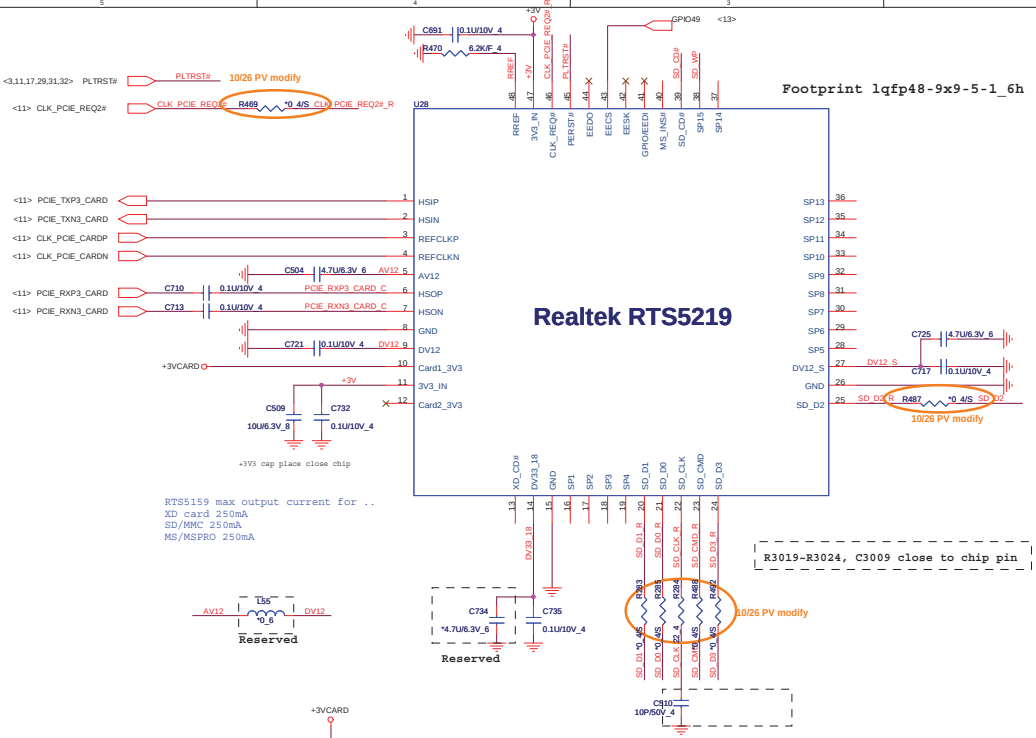
follow INTEL DG change eject PU to +3V.



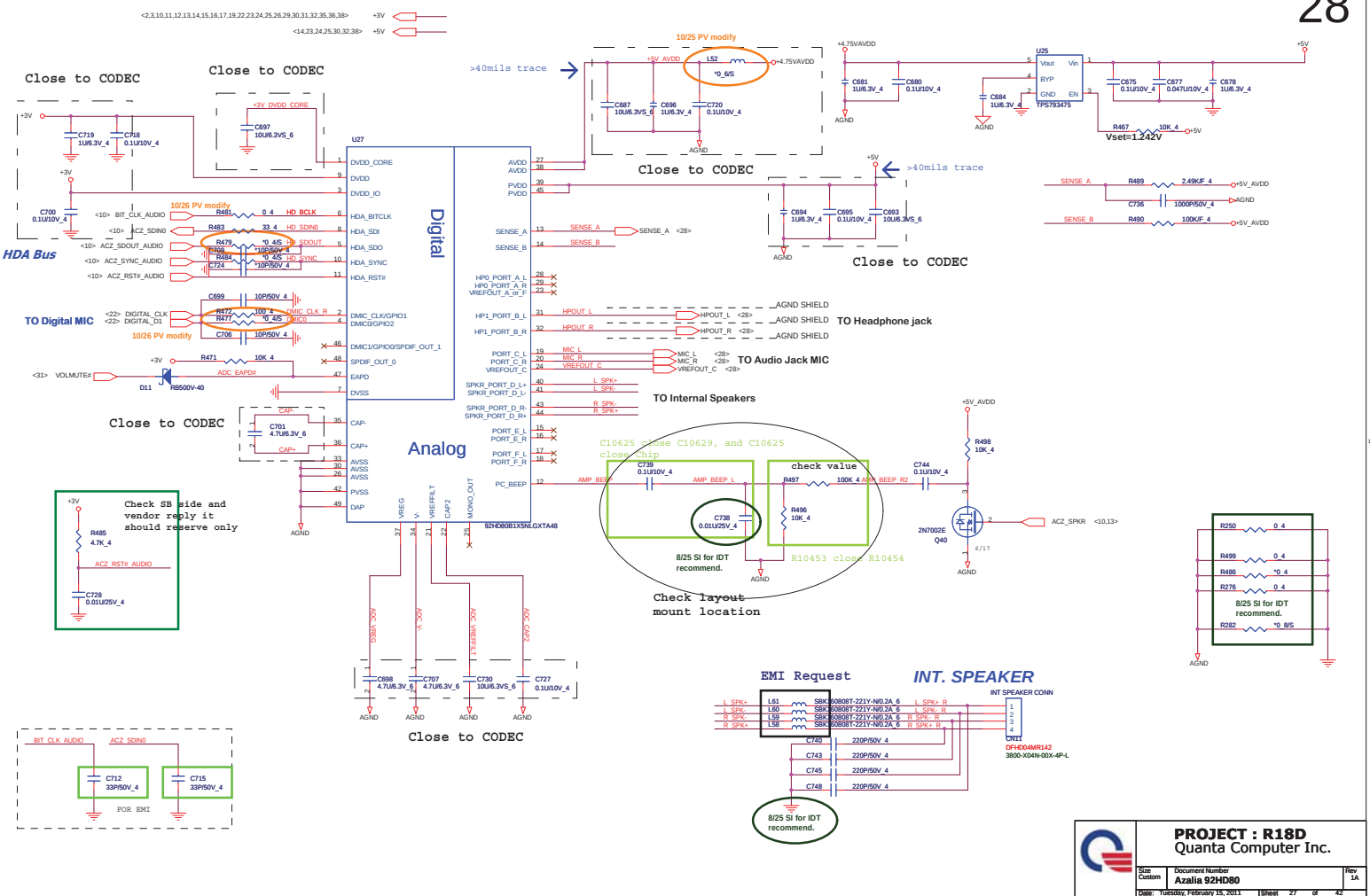
High : ODD power down
Low : ODD power on



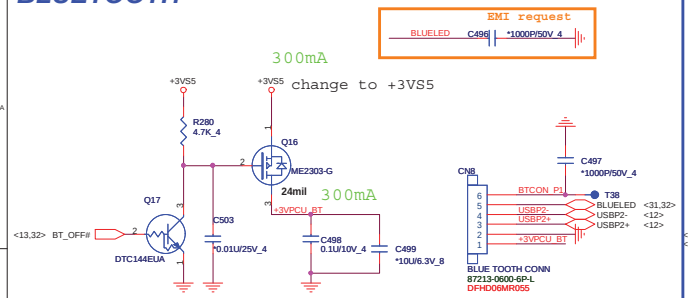
	PROJECT : R18D Quanta Computer Inc.	
Size: Custom	Document Number: HDD/ODD/FAN	Rev: 1A
Date: Tuesday, February 15, 2011	Sheet 25 of 42	



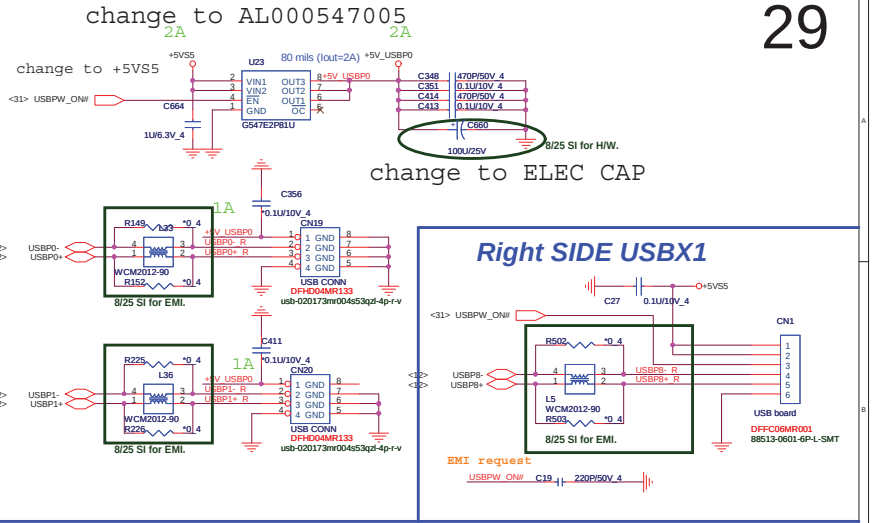
	PROJECT : R18D Quanta Computer Inc.	
Size: Custom	Document Number: RTS5219 & CR SOCKET &HOLE	Rev: 1A
Date: Tuesday, February 15, 2011	Sheet 26 of 42	


Close to CODEC
Close to CODEC
Close to CODEC
Close to CODEC
Close to CODEC
Close to CODEC
HDA Bus
TO Digital MIC
TO Headphone jack
TO Audio Jack MIC
TO Internal Speakers
Digital
Analog
U27
92HD80B1X5NLGXTA8
10/25 PV modify
10/26 PV modify
>40mils trace
Vset=1.242V
TPS793475
Check SB side and vendor reply it should reserve only
C10625 close C10629, and C10625 close chip
check value
8/25 SI for IDT recommend.
R10453 close R10454
Check layout mount location
EMI Request
INT. SPEAKER
INT SPEAKER CONN
DFHD04MR142
3800-X04N-00X-4P-L
FOR EMI
PROJECT : R18D
Quanta Computer Inc.
Azalia 92HD80
Tuesday, February 15, 2011

BLUETOOTH

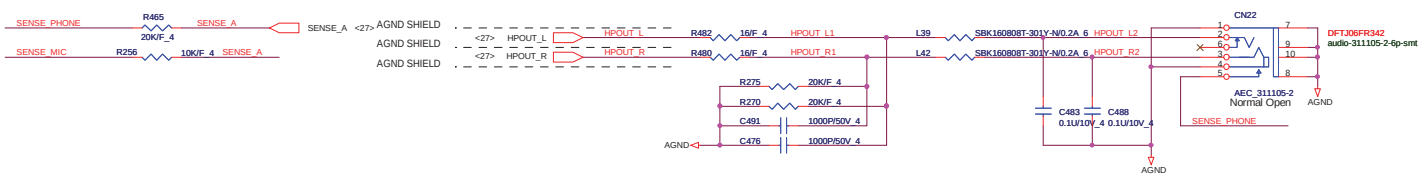


LEFT SIDE USBX2

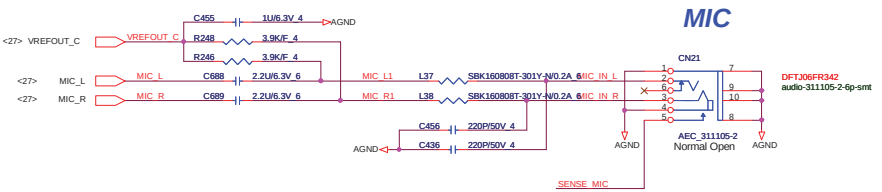


Right SIDE USBX1

Line out



MIC



	PROJECT : R18D Quanta Computer Inc.	
Size Custom	Document Number **USB/BT/Audio JacK**	Rev 1A
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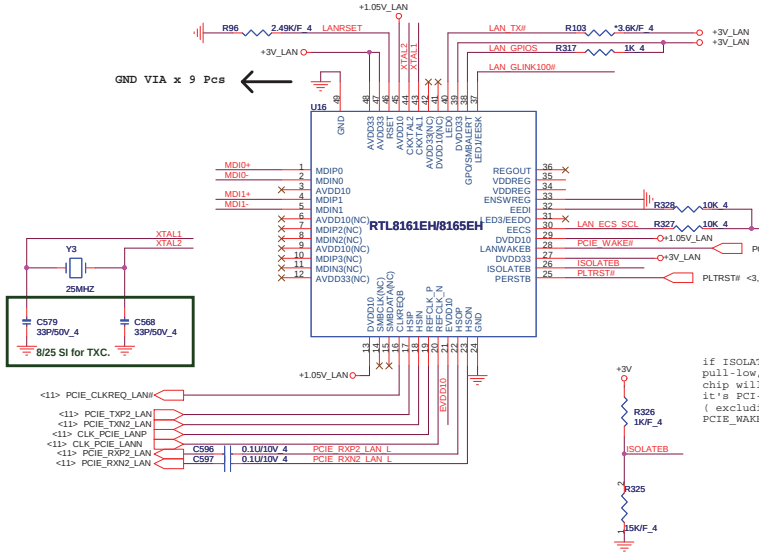
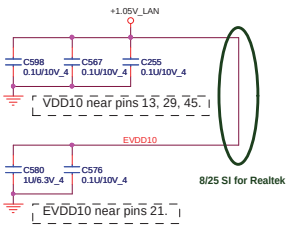


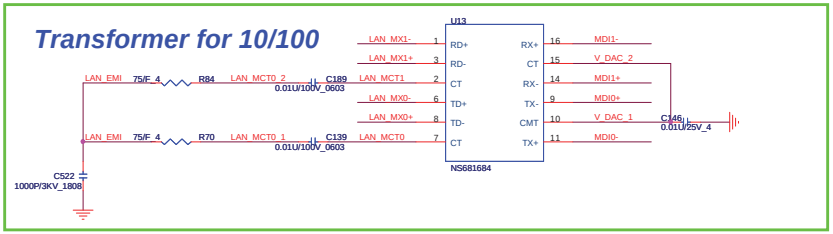
IND SMD 4.7UH +-20% 680MA(CBC2518T4R7M)
CV-4707MZ00

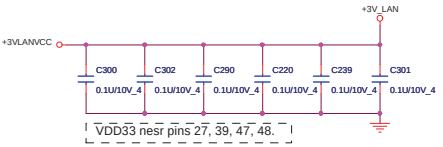
Power trace Layout 寬度> 60mil

>60mil

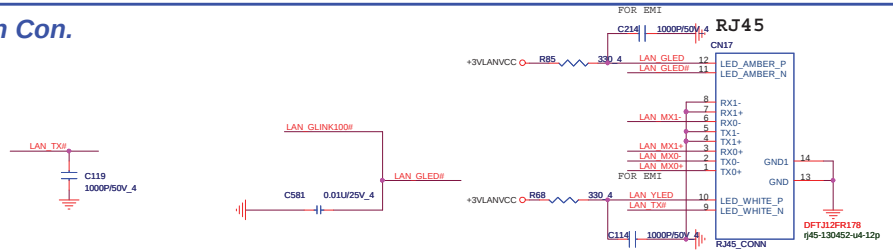


Transformer for 10/100





Lan Con.



<38> +3VLANVCC
<2,3,10,11,12,13,14,15,16,17,19,22,23,24,25,26,27,30,31,32,35,36,38> +3V

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8165EH	1A
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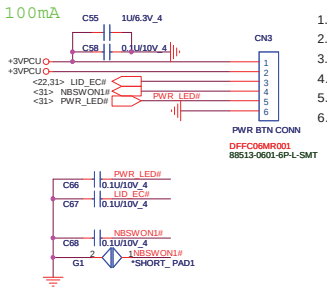
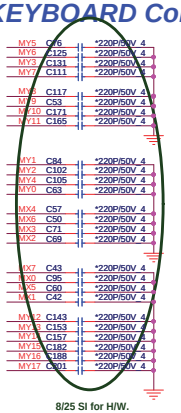
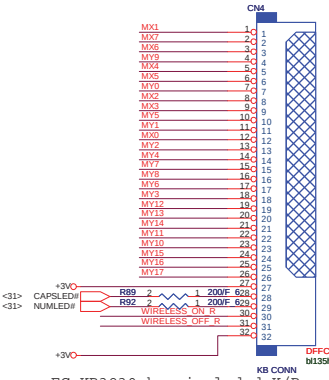
POWER BOTTON CONNECT

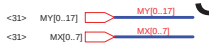


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

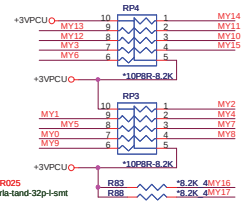
KEYBOARD Con.



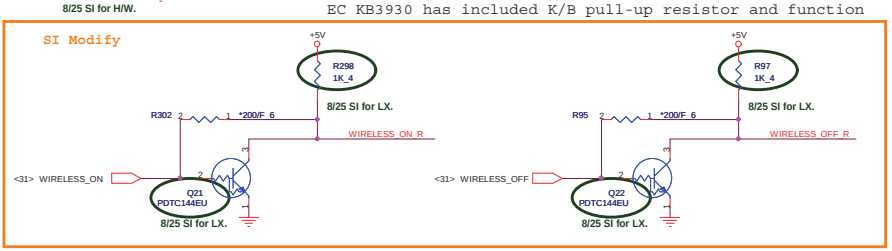




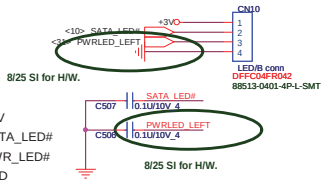
KEYBOARD PULL-UP



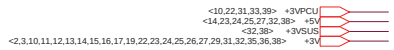
EC KB3930 has included K/B pull-up resistor and function



LED Con.

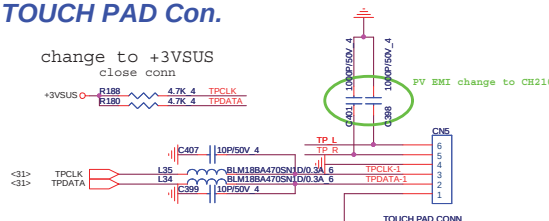


1. +3V
2. SATA_LED#
3. PWR_LED#
4.GND

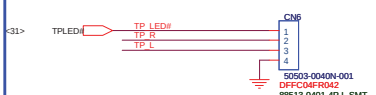


TOUCH PAD Con.

change to +3VSUS
close conn

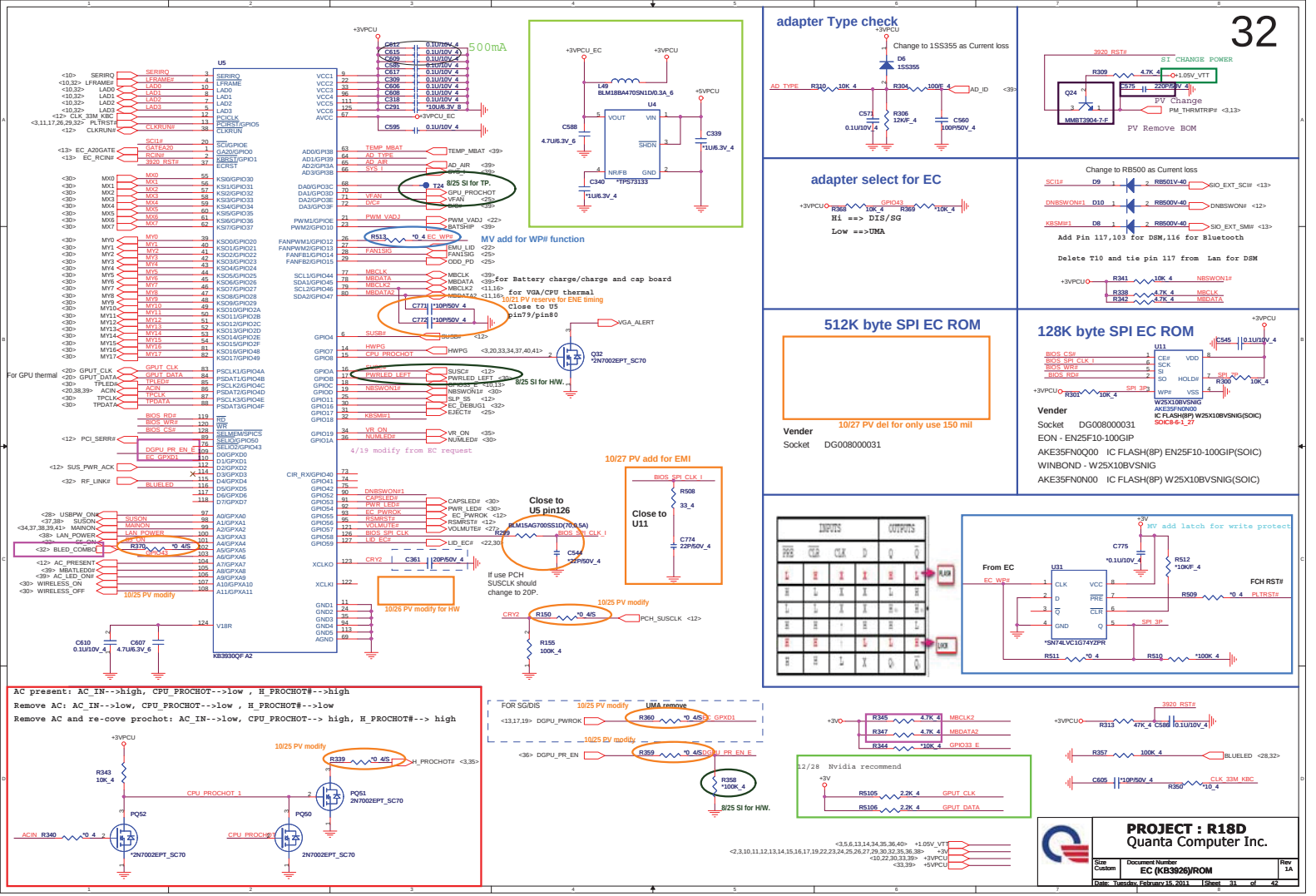


To TOUCH PAD SW board



PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KB/SW/TP	1A
Date: Tuesday, February 15, 2011	Sheet 30 of 42	


adapter Type check
Change to 1SS355 as Current loss
D6
1SS355
adapter select for EC
Hi ==> IDS/SG
Low ==>UMA
SI CHANGE POWER
PV Change
PV Remove BOM
Change to RB500 as Current loss
Add Pin 117,103 for DSM,116 for Bluetooth
Delete T10 and tie pin 117 from Lan for DSM
512K byte SPI EC ROM
10/27 PV del for only use 150 mil
Vender
Socket DG008000031
128K byte SPI EC ROM
Vender
Socket DG008000031
EON - EN25F10-100GIP
AKE35FN0Q00 IC FLASH(8P) EN25F10-100GIP(SOIC)
WINBOND - W25X10BVSNIG
AKE35FN0N00 IC FLASH(8P) W25X10BVSNIG(SOIC)
W25X10BVSNIG
AKE35FN0N00
IC FLASH(8P) W25X10BVSNIG(SOIC)
SOIC8-6-1_27
MV add for WP# function
for Battery charge/charge and cap board
for VGA/CPU thermal
10/21 PV reserve for ENE timing
Close to U5 pin79/pin80
8/25 SI for H/W.
10/27 PV add for EMI
Close to U5 pin126
Close to U11
If use PCH SUSCLK should change to 20P.
10/25 PV modify
10/26 PV modify for HW
4/19 modify from EC request
MV add latch for write protect
From EC
FCH RST#
AC present: AC_IN-->high, CPU_PROCHOT-->low , H_PROCHOT#-->high
Remove AC: AC_IN-->low, CPU_PROCHOT-->low , H_PROCHOT#-->low
Remove AC and re-cove prochot: AC_IN-->low, CPU_PROCHOT--> high, H_PROCHOT#--> high
UMA remove
12/28 Nvidia recommend
PROJECT : R18D
Quanta Computer Inc.
EC (KB3926)ROM
Size Custom
Document Number
Rev 1A
Date: Tuesday, February 15, 2011
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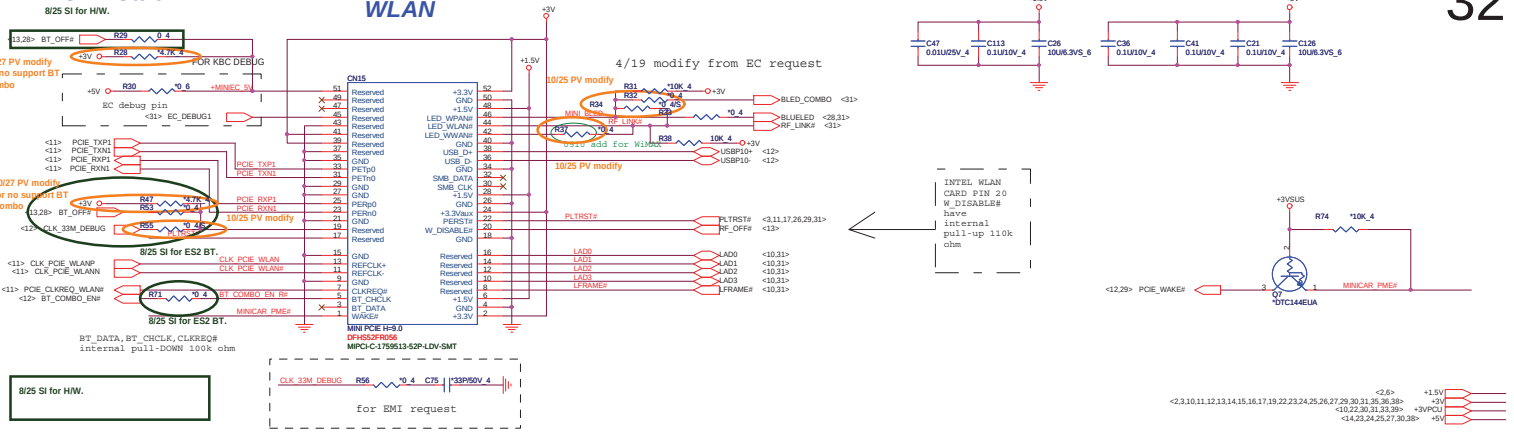
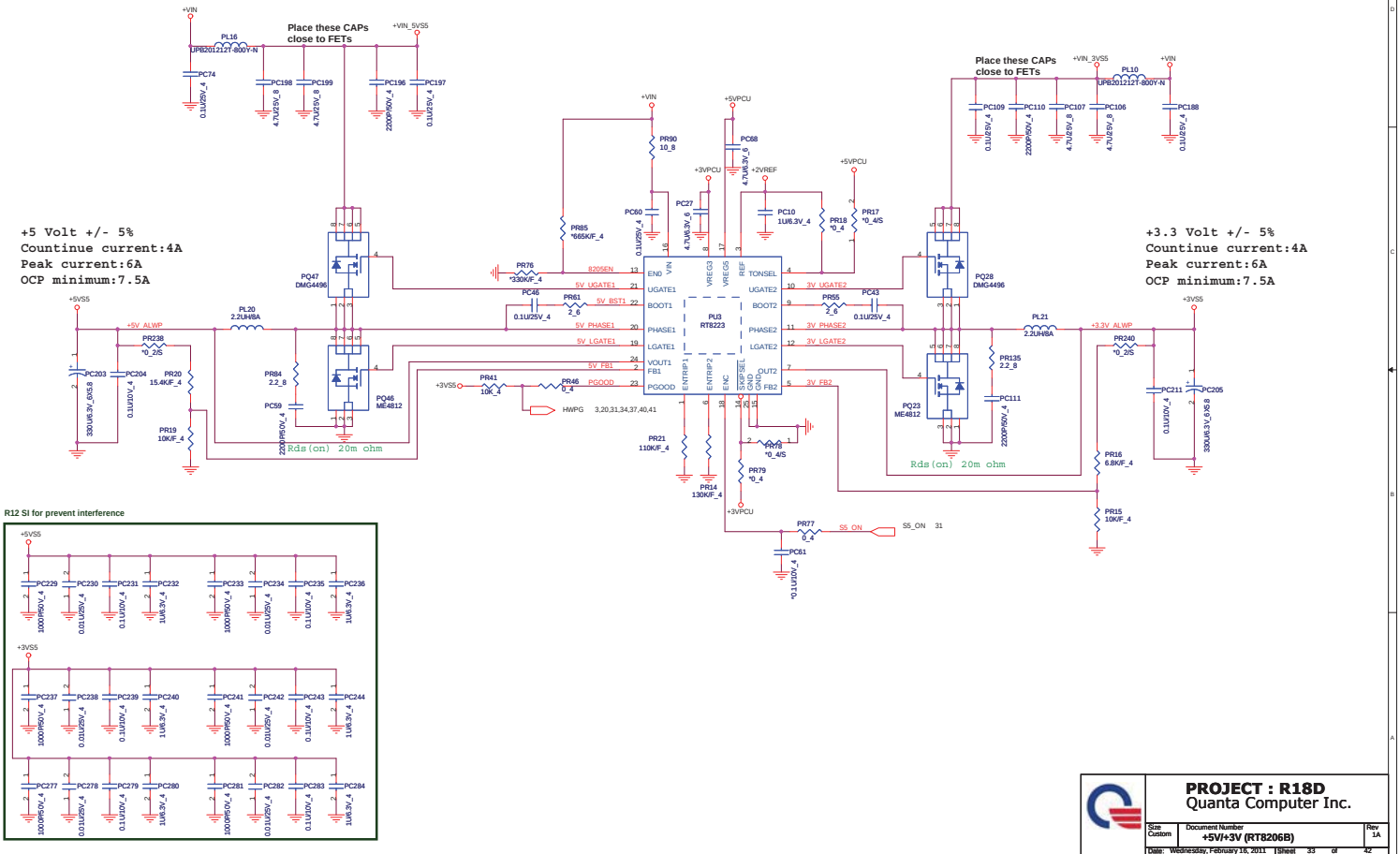
Mini PCI-E Card 1

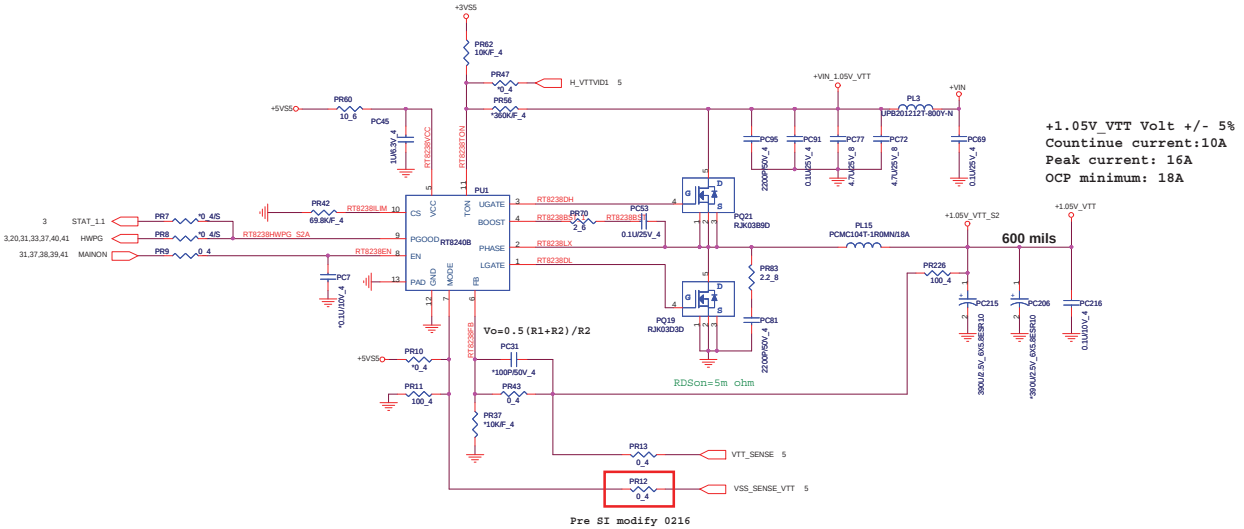
WLAN

8/25 SI for H/W.



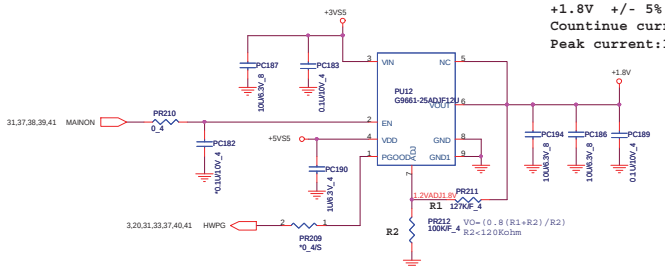
8/25 SI for H/W.


Place these CAPs close to FETs
Place these CAPs close to FETs
+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A
PU3 RT8223
Rds(on) 20m ohm
Rds(on) 20m ohm
R12 SI for prevent interference



+1.05V_VTT Volt +/- 5%
Countinue current:10A
Peak current: 16A
OCP minimum: 18A

Pre SI modify 0216



+1.8V +/- 5%
Countinue current:0.7A
Peak current:1A

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1V VTT / PCH	1A

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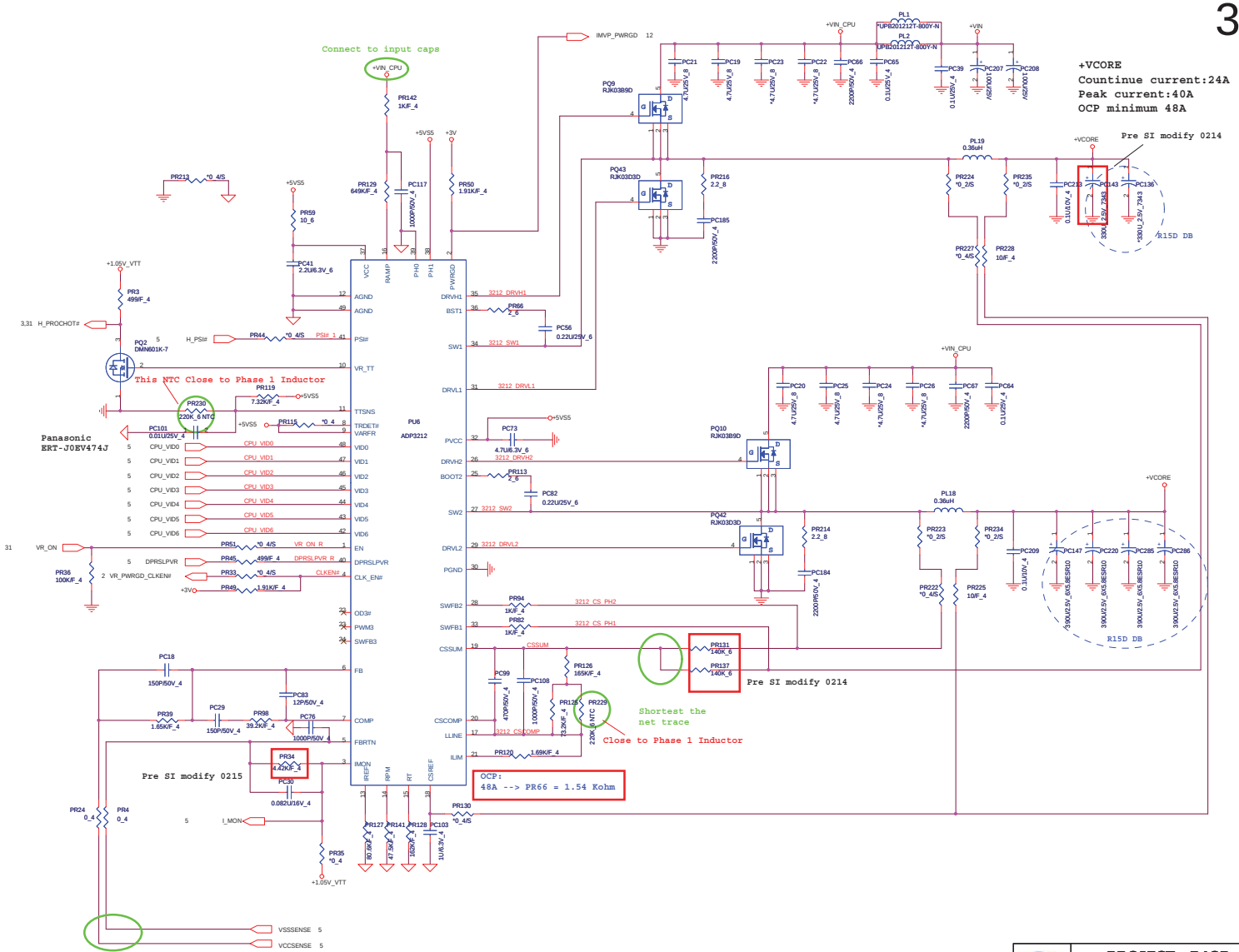
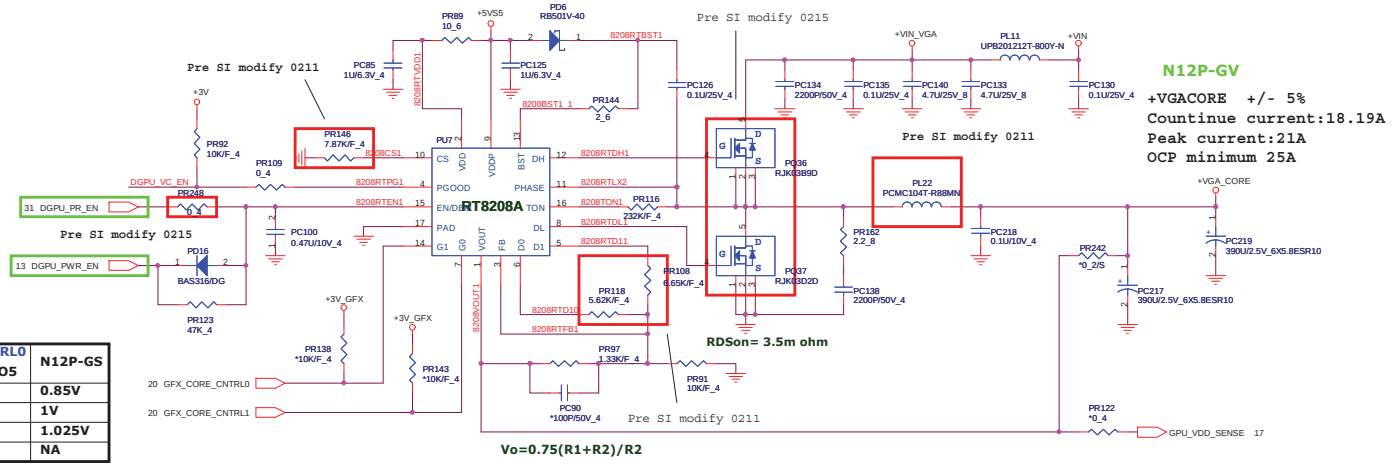
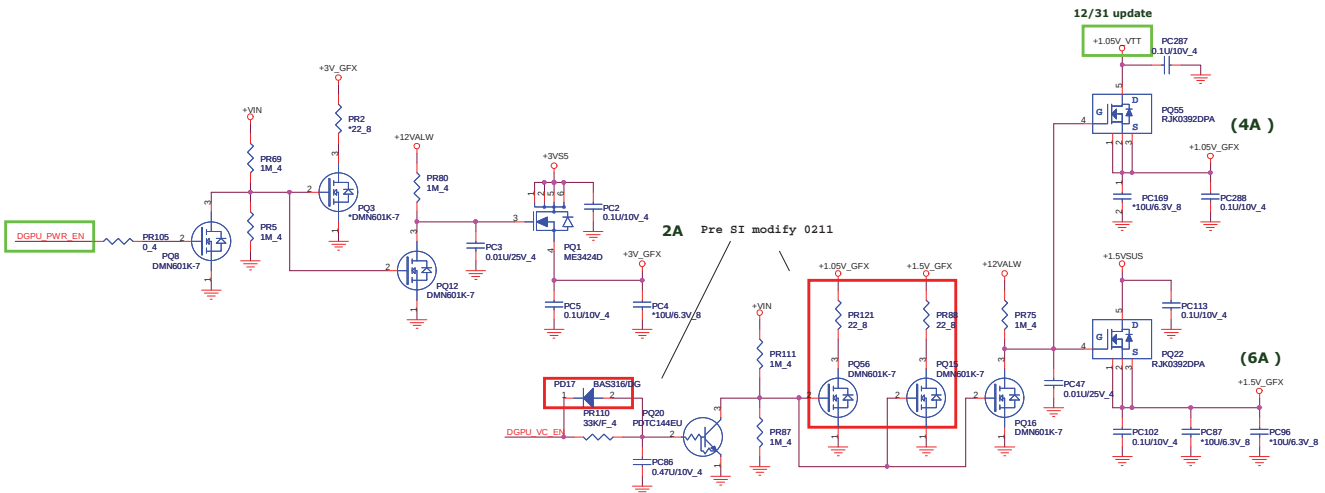


PROJECT : R18D	
Quanta Computer Inc.	
Size: Custom	Document Number: CPU Core (ADP3212)
Rev: 1A	
Date: Wednesday, February 16, 2011	Sheet 35 of 42

VGA Core



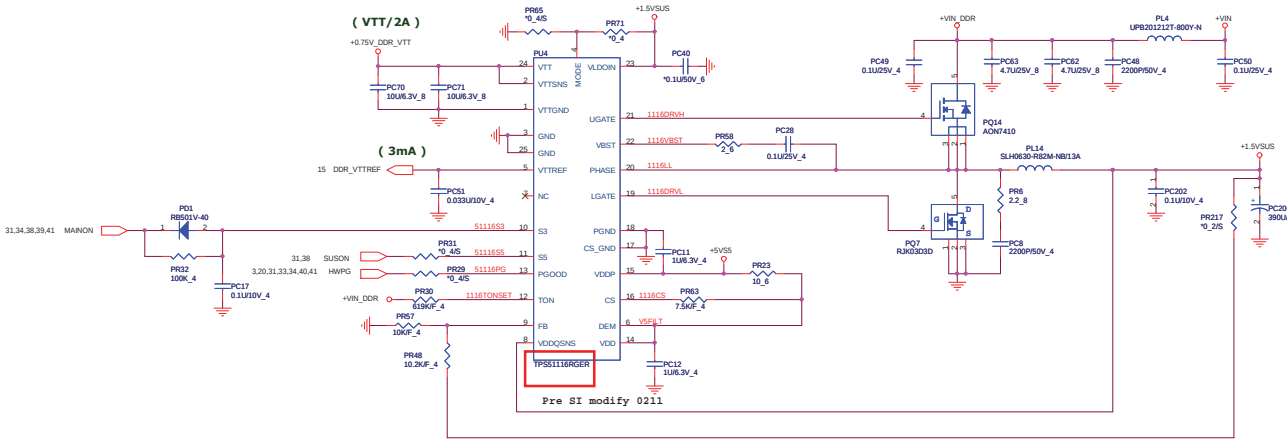
CNTRL1 GPIO6	CNTRL0 GPIO5	N12P-GS
0	0	0.85V
0	1	1V
1	0	1.025V
1	1	NA



PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8208/1.8V)	1A

Date: Wednesday, February 16, 2011 Sheet 36 of 42

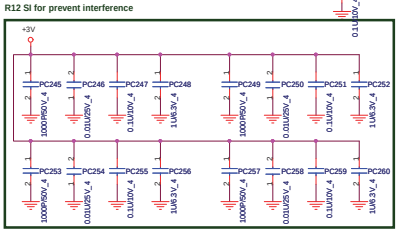


PROJECT : R18D
Quanta Computer Inc.

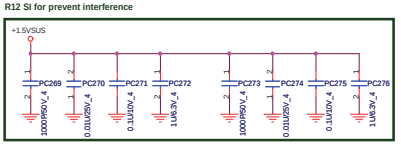
Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A

Date: Wednesday, February 16, 2011 Sheet 37 of 42

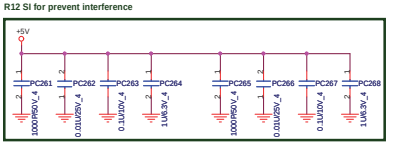
R12 SI for prevent interference



R12 SI for prevent interference



R12 SI for prevent interference



PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	1A

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DC_JACK
90W

R12 PV:
change footprint.
R12 SI:
M/E modify.

Do Not add test pad on BATDIS_G signal

R12 SI:
M/E modify.

To PWR LED

Place this ZVS close to
Diode away +VIN

Place this ZVS close to
Far-Far away +VIN

Place this cap
close to EC

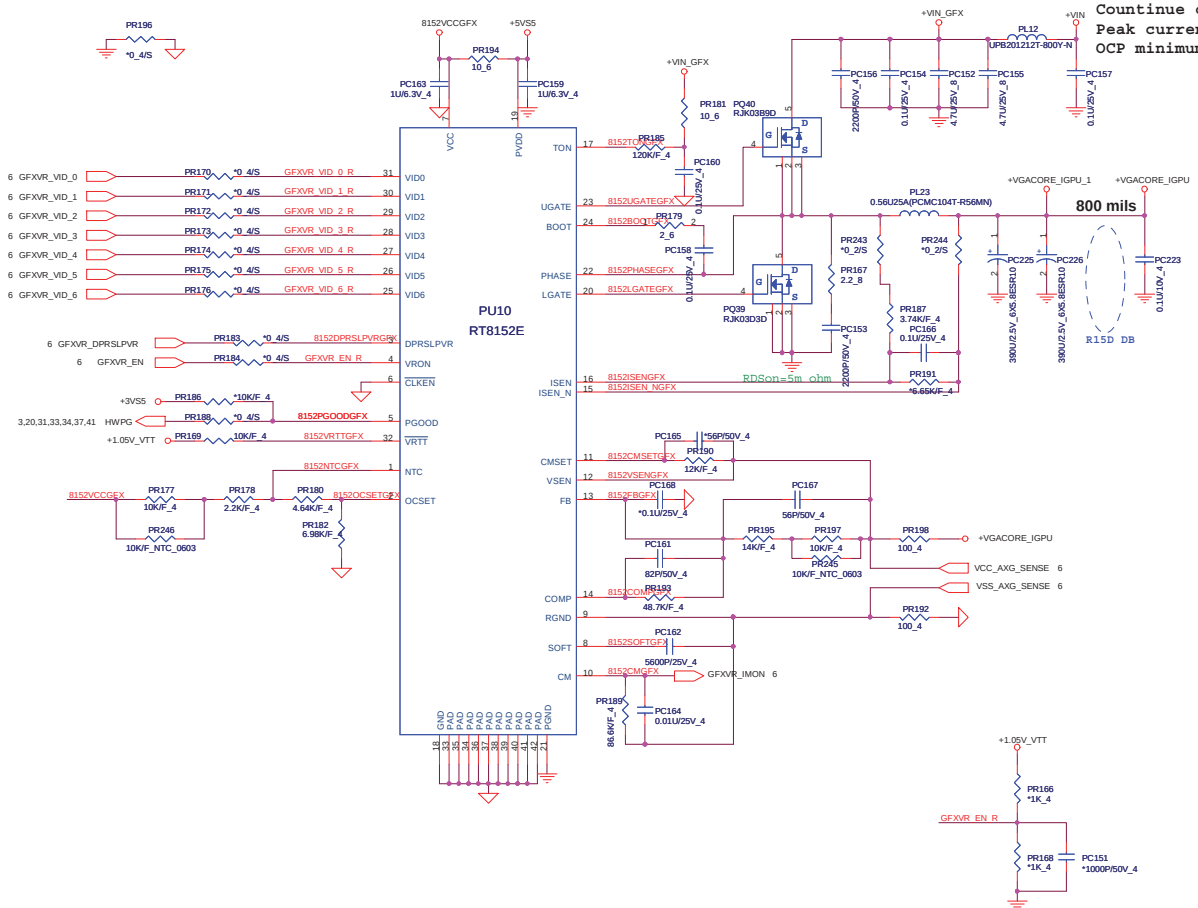
Place this cap
close to EC

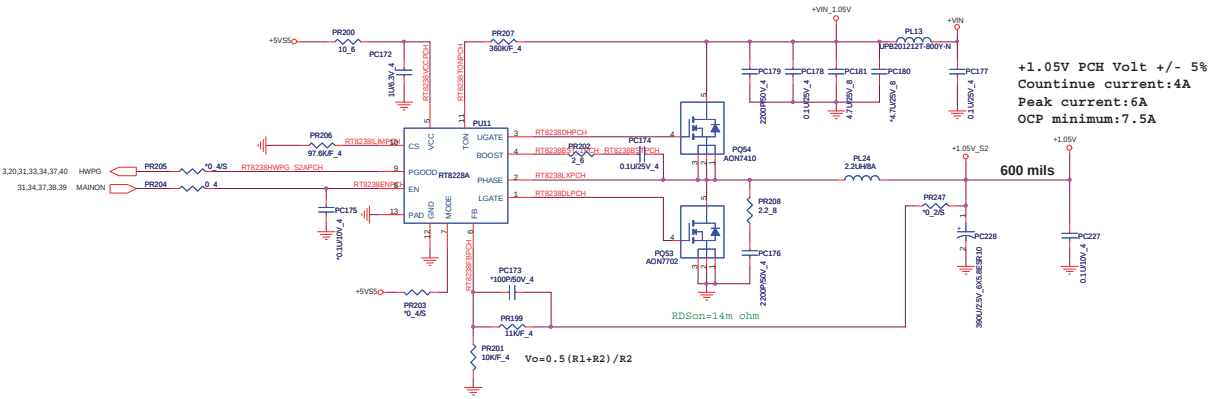
Place this cap
close to EC

PU9
OZ8681

PROJECT : R18D	
Quanta Computer Inc.	
Size: Custom	Document Number: Charger (OZ8681)
Rev: 1A	
Date: Wednesday, February 16, 2011	Sheet 39 of 42

+VGA_UMA +/- 5%
Countinue current:12A
Peak current:18A
OCP minimum 22A





	PROJECT : R18D Quanta Computer Inc.		
Size: Custom	Document Number: +1.05V (RT8238A)		Rev: 1A
Date: Wednesday, February 16, 2011	Sheet 41 of 42		

-->Pre SI

Page 19

1.Delete L5005, C5096,C5097,C5098,C5099,C5100 and connect +SP_PLLVDD to +NV_PLLVDD

2.L5004 change to bead 220ohm (ESR=0.5) 0603.
3.C5089 change to 22uF_0805

Page 11

1.delete Q35.

Page 17

1.delete L5000 and C5074.
2.connect +3V_GFX to GPU ball AG9 with a 0.1uF cap C5075.
3.New add R5060 for test

4.L5001 change to bead 120ohm@100MHz (ESR=0.18ohm) 0603.
5.C5073 should be 4.7uF_X7R_0805.
6.C5072 should be 1uF_X7R_0603.
7.C5071 should be 0.1uF_X7R_0402.

8.PCIE change to PEX_TX0~7 and PEX_RX0~7 on GPU side for X8 lane configuration
9.unstuff R5009 and R5008 Q5002 stUff for test
9.delete L5002 for NVidai recommend

Page 18

1.L5003 change to bead 30ohm (ESR=0.01) 0603.
2.C5085 change to 1uF_X7R_0603
3.Delete C5084.

Page 21

1.R5096 and R5103 change to 162ohm_1%.

Page 31

1.New add R5105 and R5106 2.2K pull up resistors to +3V for GPUT_CLK and GPUT_DATA on EC side.

2.Delete D20,Q25,D19,R500.

Page 20

1.delete R5081,R5082,R5082.

2.New add R5085 and R5086 10K pull down resistors to GFX_CORE_CNTRL0 and GFX_CORE_CNTRL1

3.Change R5047 to 5K pull up for ROM_SCLK

4.Change R5080 to 10K for JTAG_TRST# pull down.
5.R5084 can be no stuff for JTAG_TCK
6.New add Q5010 for AC/Batt# function.

7.New add Q5011.

PROJECT : R18D
Quanta Computer Inc.

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