COMPAL CONFIDENTIAL

MODEL NAME : CAP10

PCB NO : LA-E321P

BOM P/N : 451A4X31L01

GPIO MAP: Gen7 GPIO Master_XXXX

CRANE17

Kaby Lake H-type (2 chip)

REV : 1.0(A00)

2016.11.30

@ : Nopop Component

EMC@ : EMI/ESD/RF part

CONN@ : Connector Component

XDP@ : Total debug Component (pop them until ST)

TB@ : Thunderbolt function

Layout Dell logo

REV: X00
PWB: XXXXX
DATE: 1403-06

PCB 1TT LA-E321P REV1 MB

Part Number	Description
DAA000CT010	PCB 1TT LA-E321P REV1 MB

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Title: Cover Sheet

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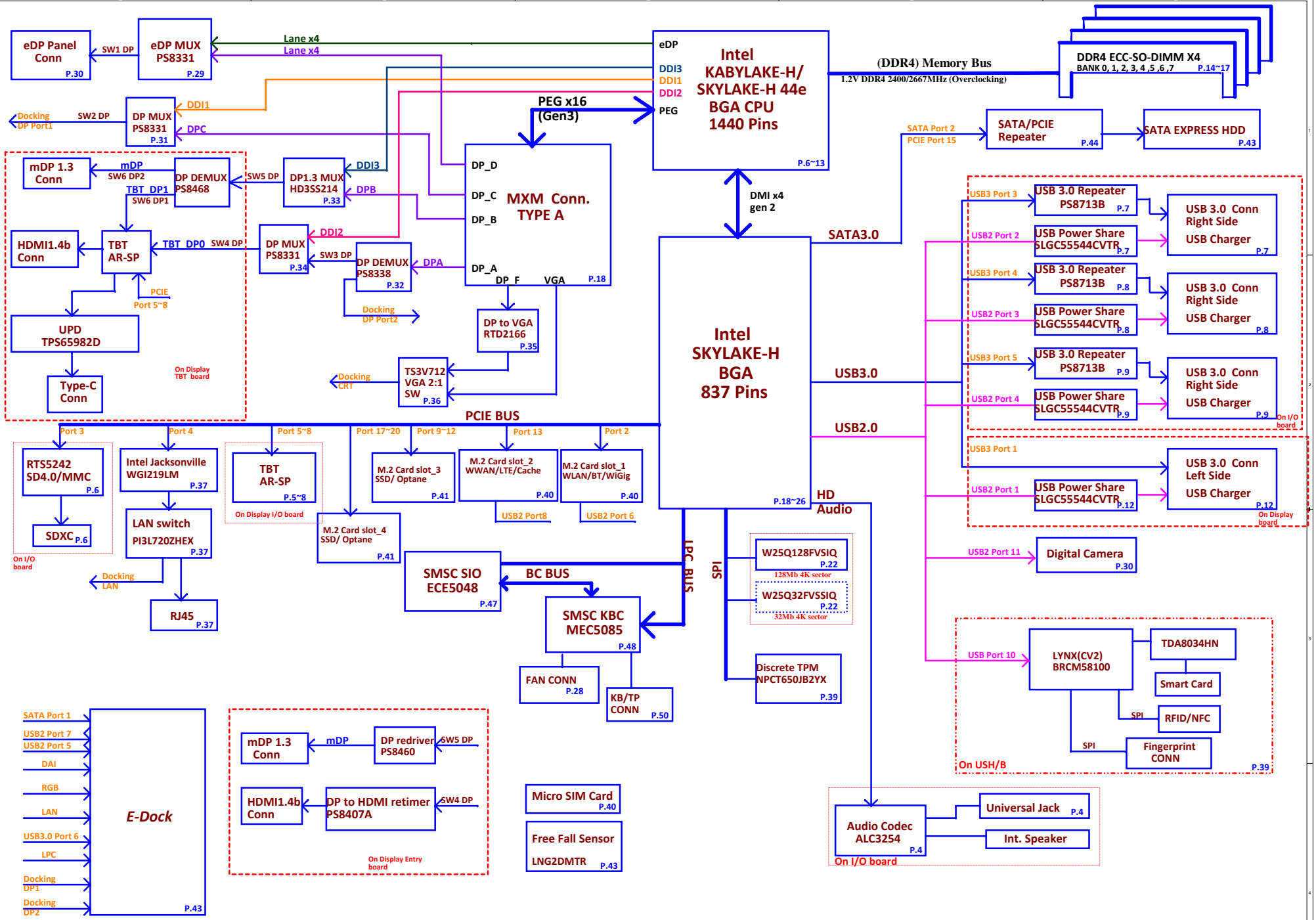
Power CKT:
0108



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Title: Block Diagram

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POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE			RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane / State	+PWR_SRC +5V_ALW +3.3V_ALW +3.3V_ALW2 +3.3V_ALW_DSW +3.3V_ALW_PCH +3.3V_RTC_LDO +1.8V_ALW +1.0V_PRIM	+3.3V_SUS +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +1.5V_RUN +0.675V_DDR_VTT +3.3V_MXM +5V_MXM +MXM_PWR_SRC		(M-OFF) +VCC_CORE +VCC_EDRAM +VCC_EOPIO +VCC_GTU +VCC_GT +1.0V_VCCSTG +VCC_SA
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

Stack up

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil
			SolderMask	IT-158
			Add Plating	
1	Top		Copper foil	0.5oz
		3.7	Prepreg	1080
2	GND/PWR		Copper foil	1oz
		3.7	Core	4mil
3	Sig 1		Copper foil	1oz
		4.1	Prepreg	2116Mx2
4	GND/PWR		Copper foil	1oz
		3.7	Core	4mil
5	Sig 2		Copper foil	1oz
		3.8	Prepreg	1080Hx2
6	Sig 3		Copper foil	1oz
		3.7	Core	4mil
7	GND/PWR		Copper foil	1oz
		4.1	Prepreg	2116Mx2
8	Sig 4		Copper foil	1oz
		3.7	Core	4mil
9	GND/PWR		Copper foil	1oz
		3.7	Prepreg	1080
10	Bottom		Copper foil	0.5oz
			Add Plating	
			SolderMask	
Overall Thickness (1.45mm ± 10%)			57.09	

SATA	DESTINATION
SATA 0	2280 SSD
SATA 1	Dock
SATA 2	
SATA 3	SATAe HDD
SATA 4	2280 SSD
SATA 5	

USB3.0	DESTINATION
Port 1	Left Side JUSB1
Port 2	M.2 Slot-2 (WWAN/LTE/Cache)
Port 3	Right Side JUSB1
Port 4	Right Side JUSB2
Port 5	Right Side JUSB3
Port 6	Docking

	USB PORT#	DESTINATION
PCH	1	Left Side JUSB1
	2	Right Side JUSB1
	3	Right Side JUSB2
	4	Right Side JUSB3
	5	Docking USB3.0
	6	M.2 Slot-1 (BT)
	7	Docking USB 2.0
	8	M.2 Slot-2 (WWAN/LTE/HCA)
	9	NA
	10	USH
	11	Camera
	12	NA
	13	NA
	14	NA

USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	NA
Lane 2	M.2 Slot-1 (WLAN/Wigig)
Lane 3	MMI(Card reader)
Lane 4	10/100/1G LOM
Lane 5~8	TBT-Alpine Ridge
Lane 9~12	SSD 2280/ Optane
Lane 13	M.2 Slot-2 (WWAN/LTE/Cache)
Lane 15~16	HDD SATA-Express
Lane 17~20	SSD 2280/ Optane

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Title: Index and Config.

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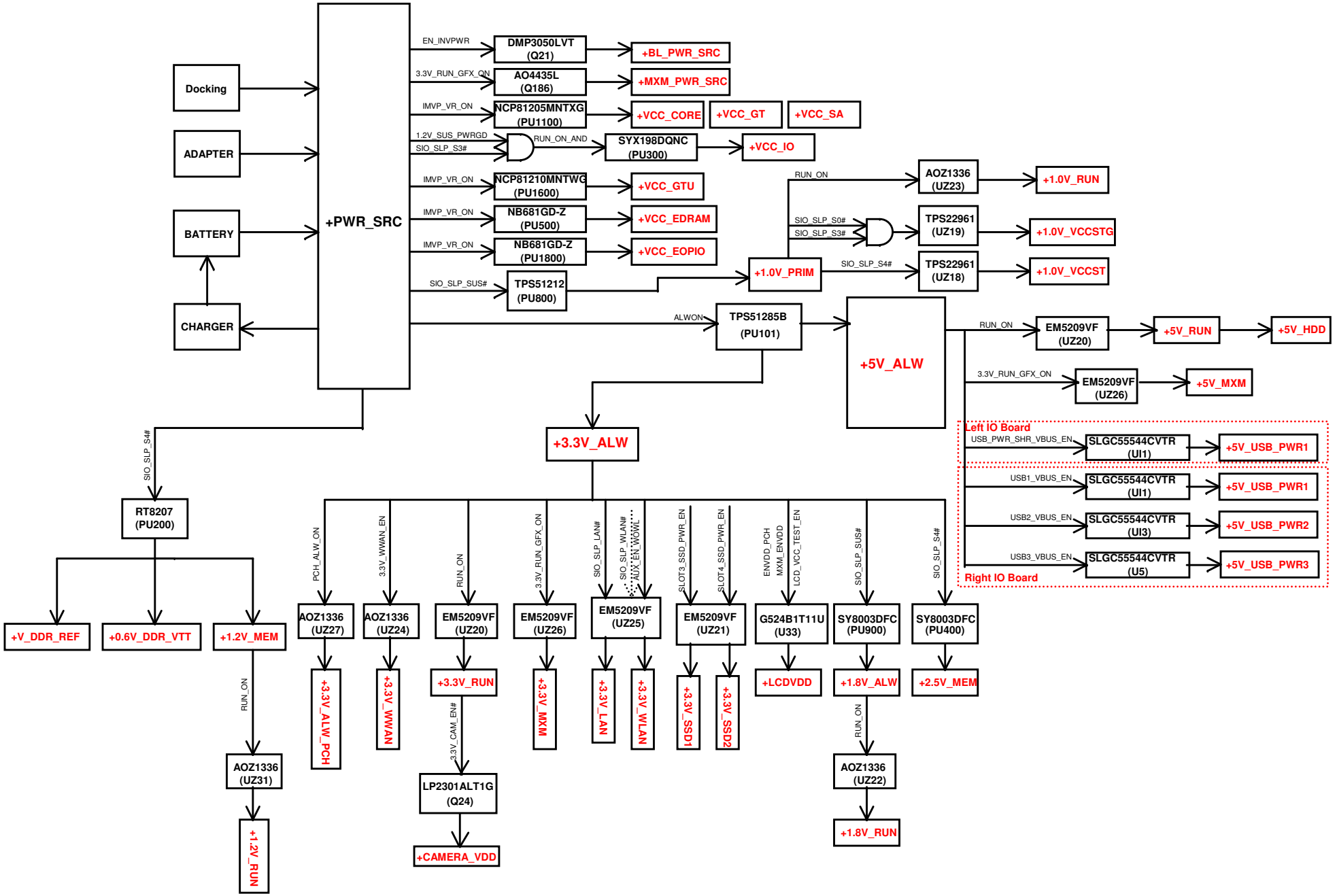

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Title	Power Rail
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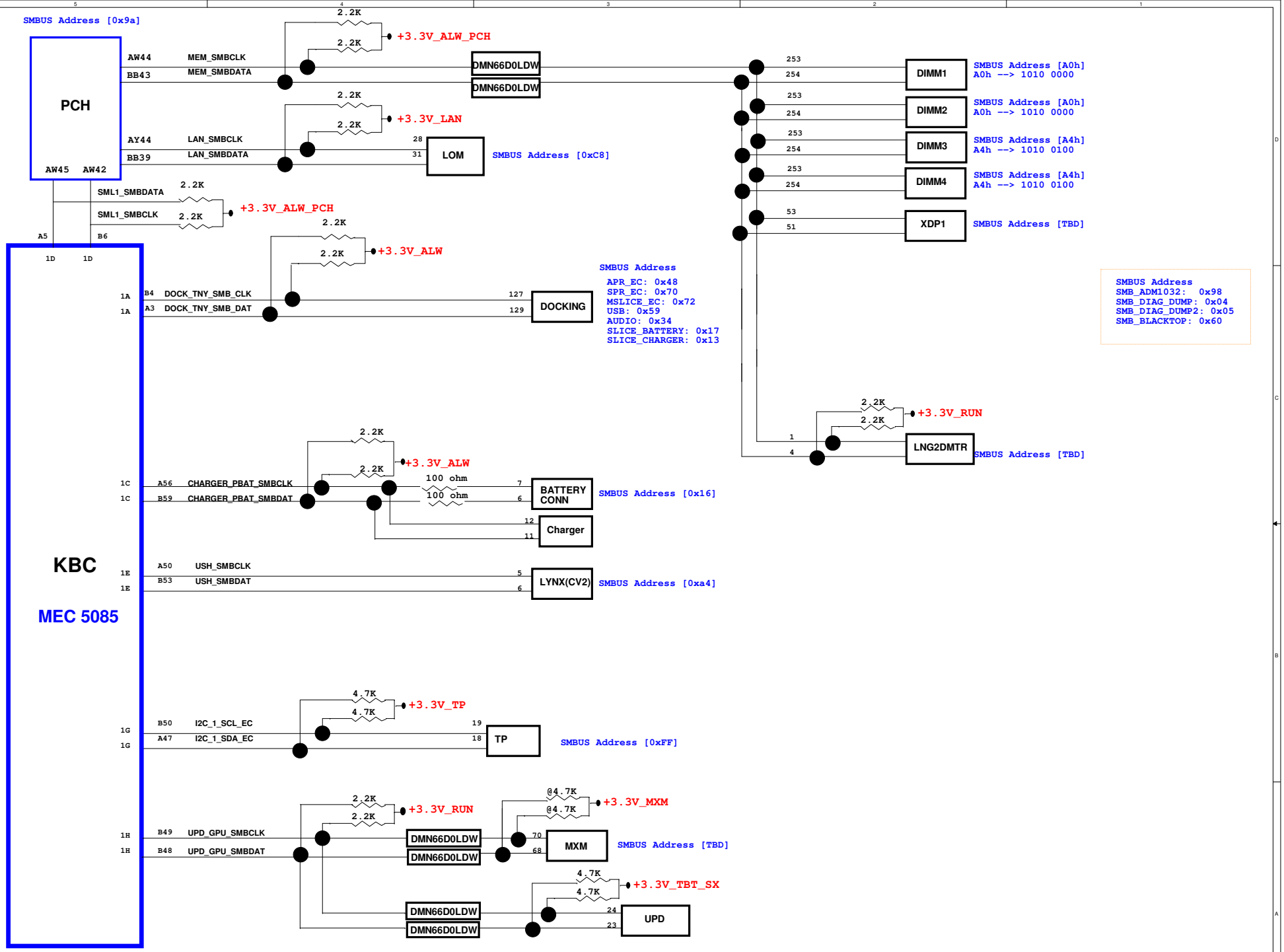

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Title	SMBUS Bolck Diagram
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CPU1C SKYLAKE_HALO Rev_1.0

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PEG_COMP G2
PEG_RCOMP

+VCC_IO
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24.9_0402_1% RC2

CAD Note:
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,Spacing=15mil
Max length= 400 mils.

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SKL-H_BGA1440

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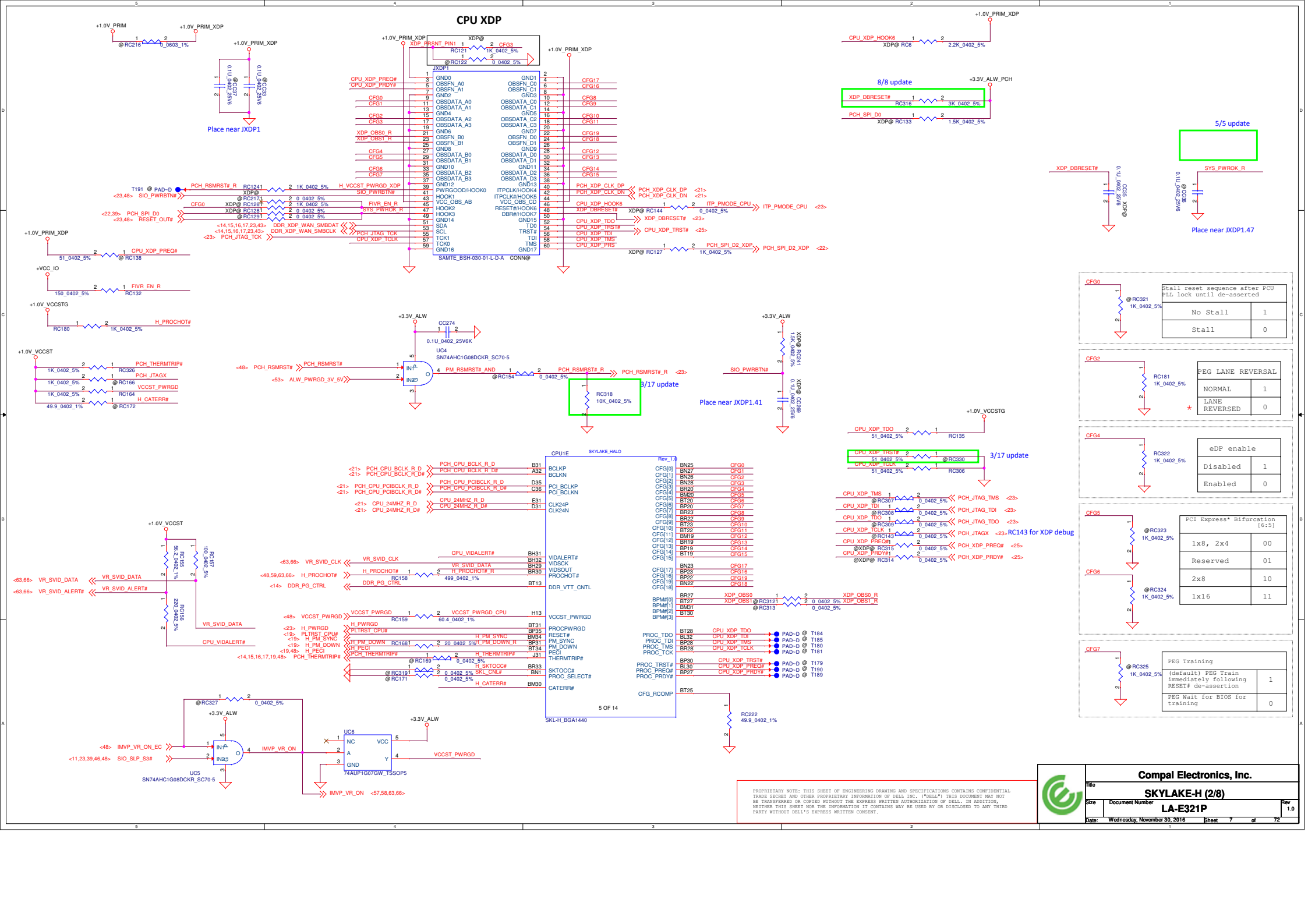
CPU XDP



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Title: SKYLAKE-H (2/8)

Size: | Document Number: LA-E321P | Rev: 1.0

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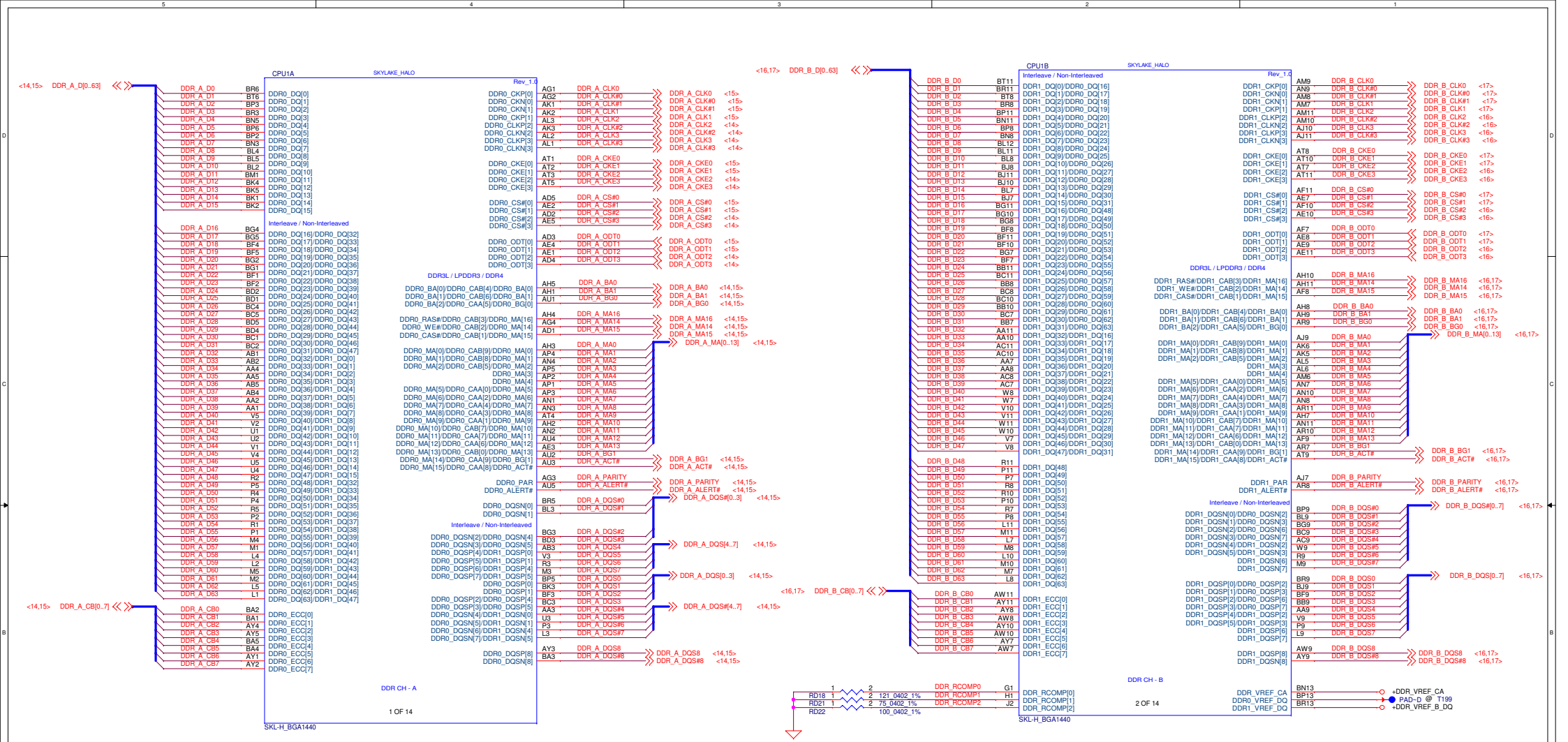

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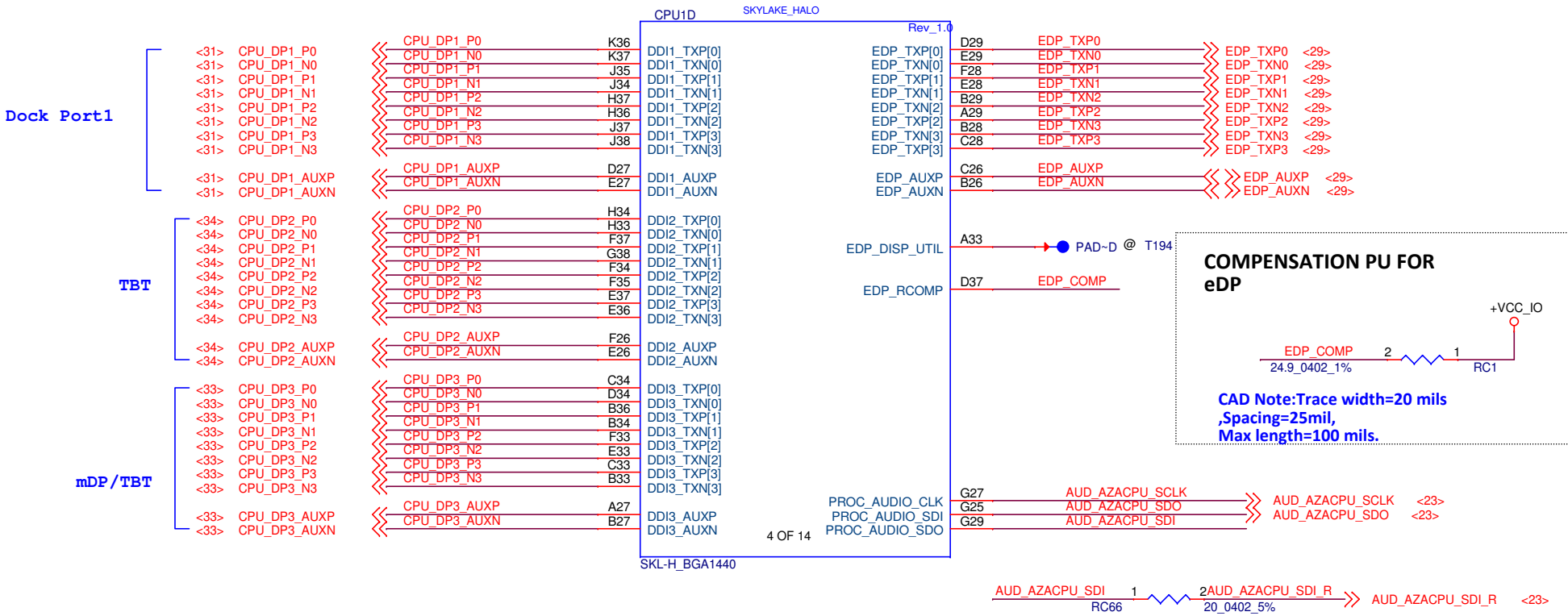

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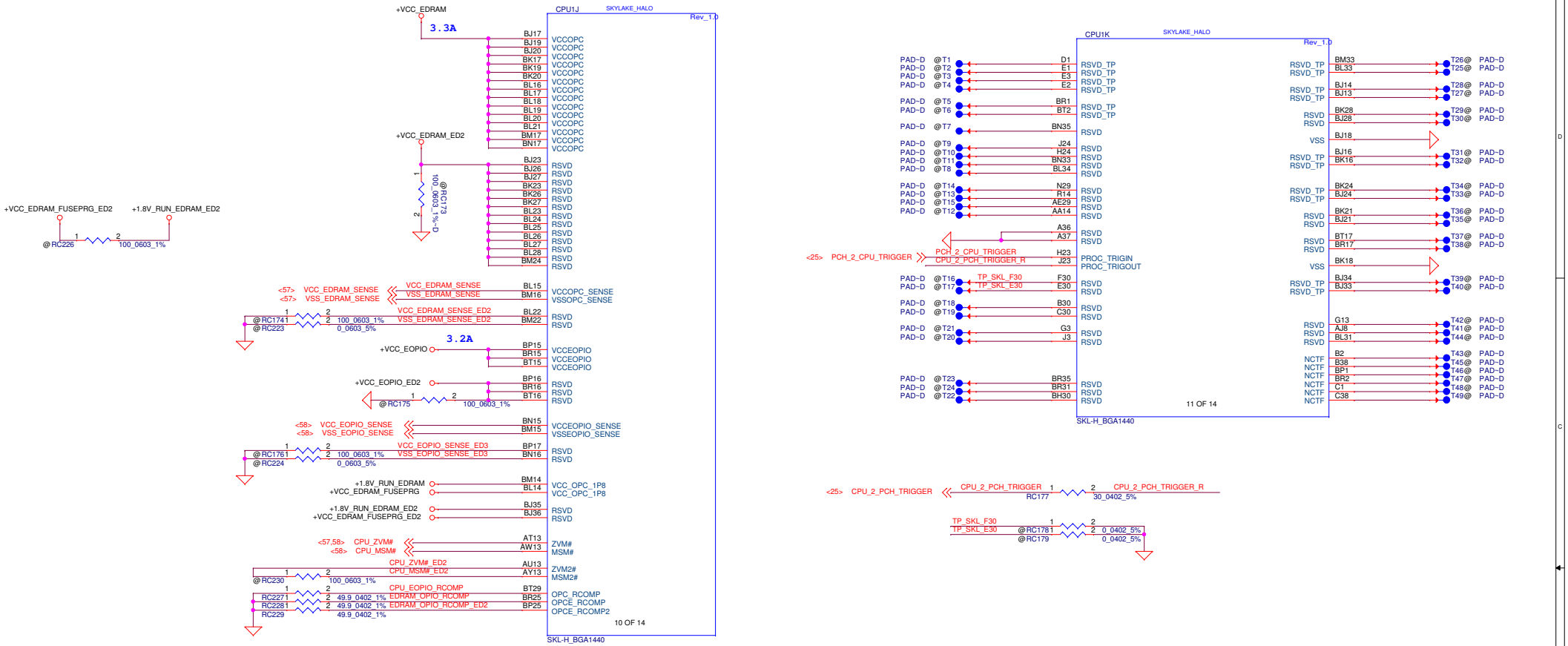

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Title: SKYLAKE-H (5/8)

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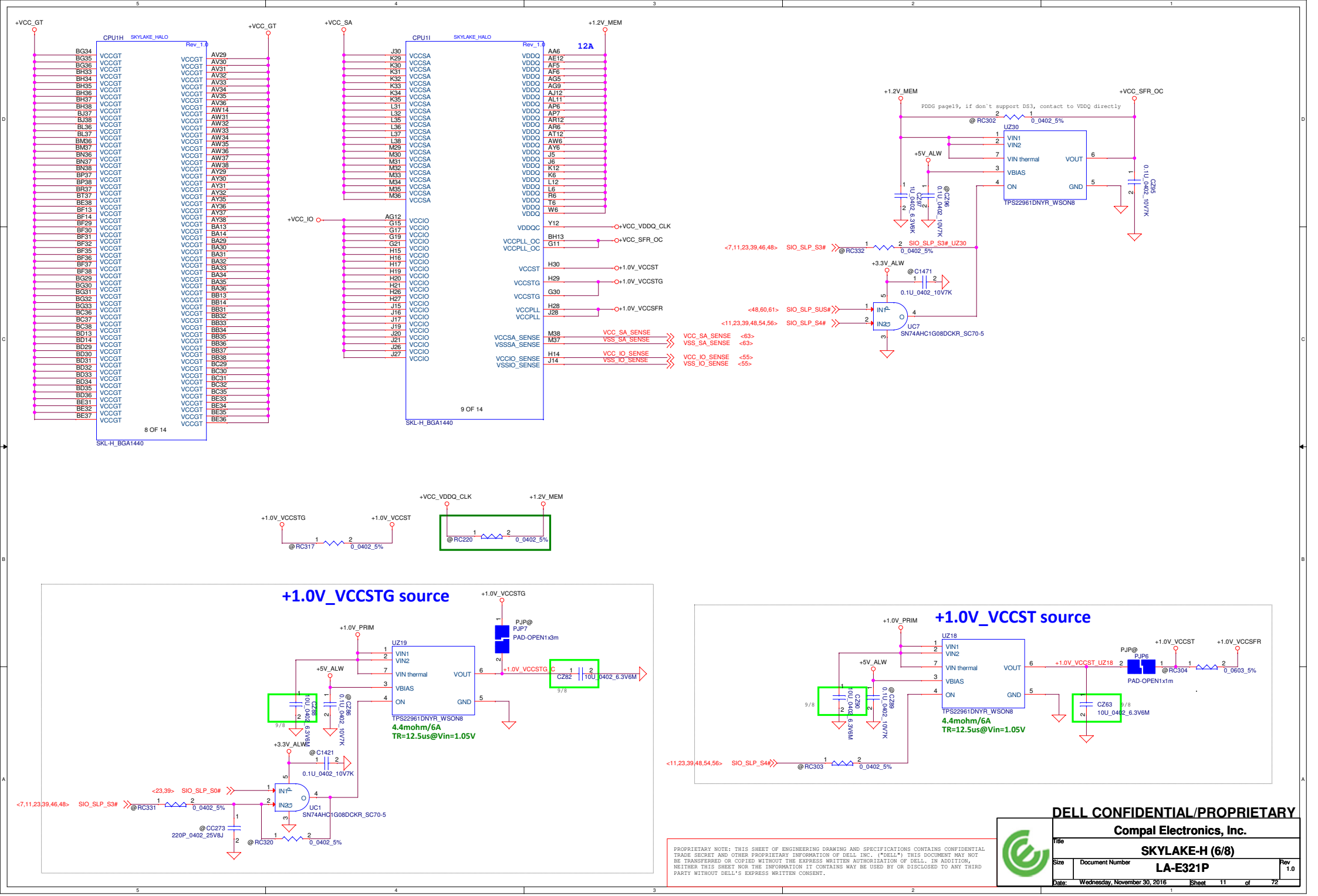

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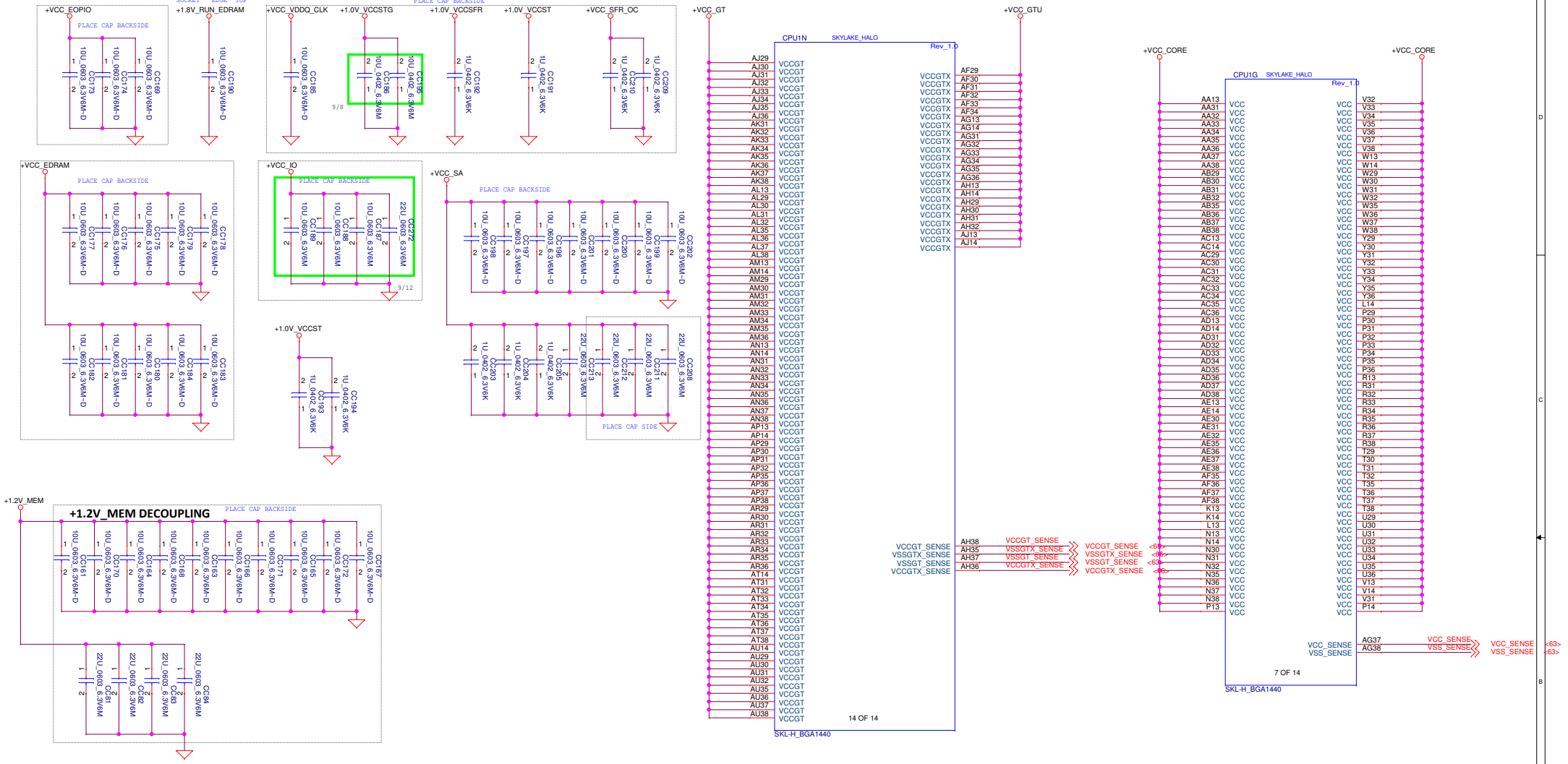

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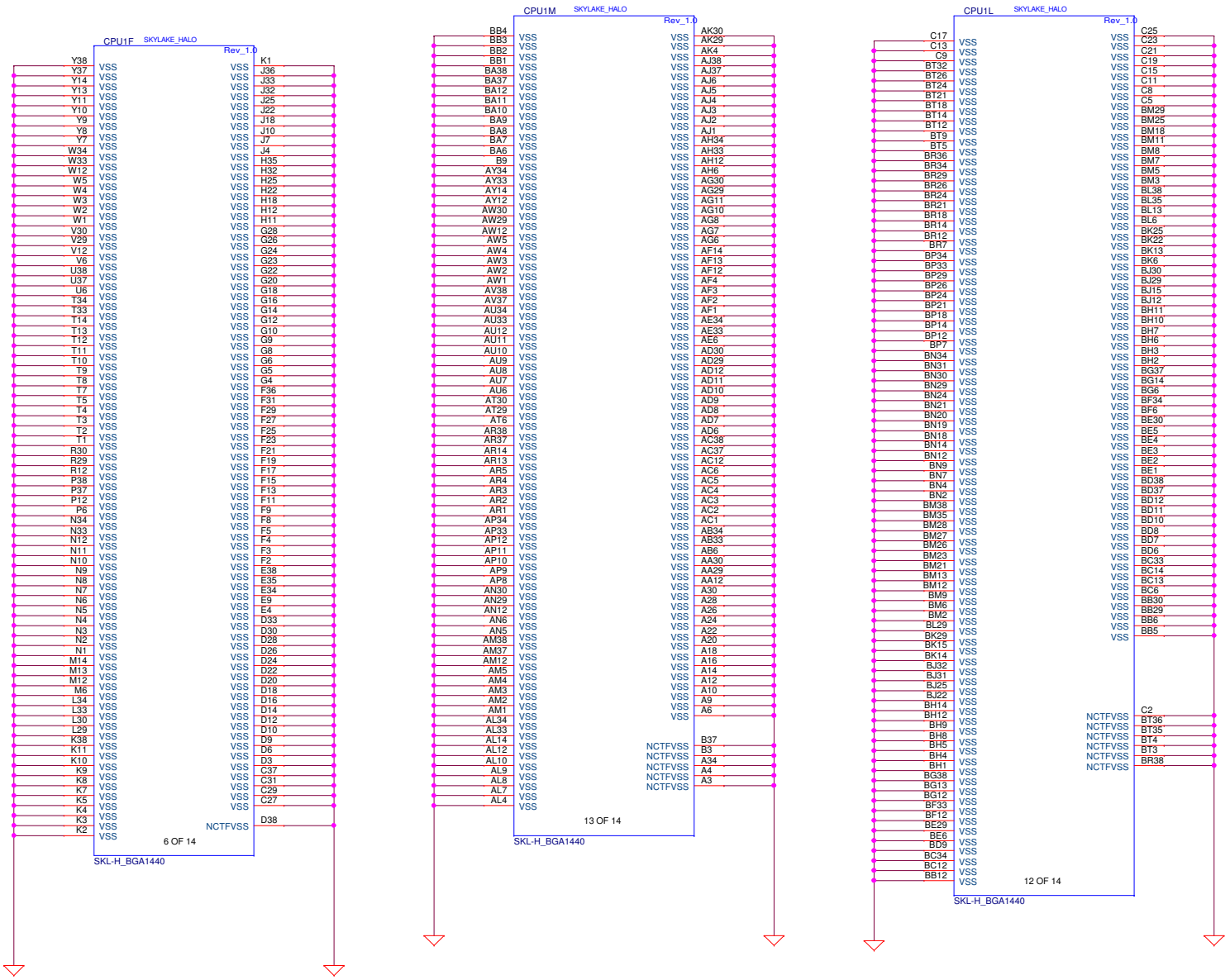

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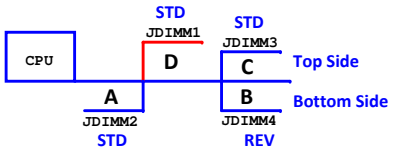
Title	SKYLAKE-H (8/8)	
Size	Document Number: LA-E321P	Rev: 1.0
Date: Wednesday, November 30, 2016	Sheet 13 of 72	

JDIMM1 STD Type H=9.2

All VREF traces should have 10 mil trace width



CD14 change to SGA20331E10

Layout Note:
Place near JDIMM1.258

DIMM Select

	SA0	SA1	SA2
DIMM2	0	0	0
DIMM4	0	1	0
* DIMM1	1	0	0
DIMM3	1	1	0

BELLW_80888-6021
CONN@

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

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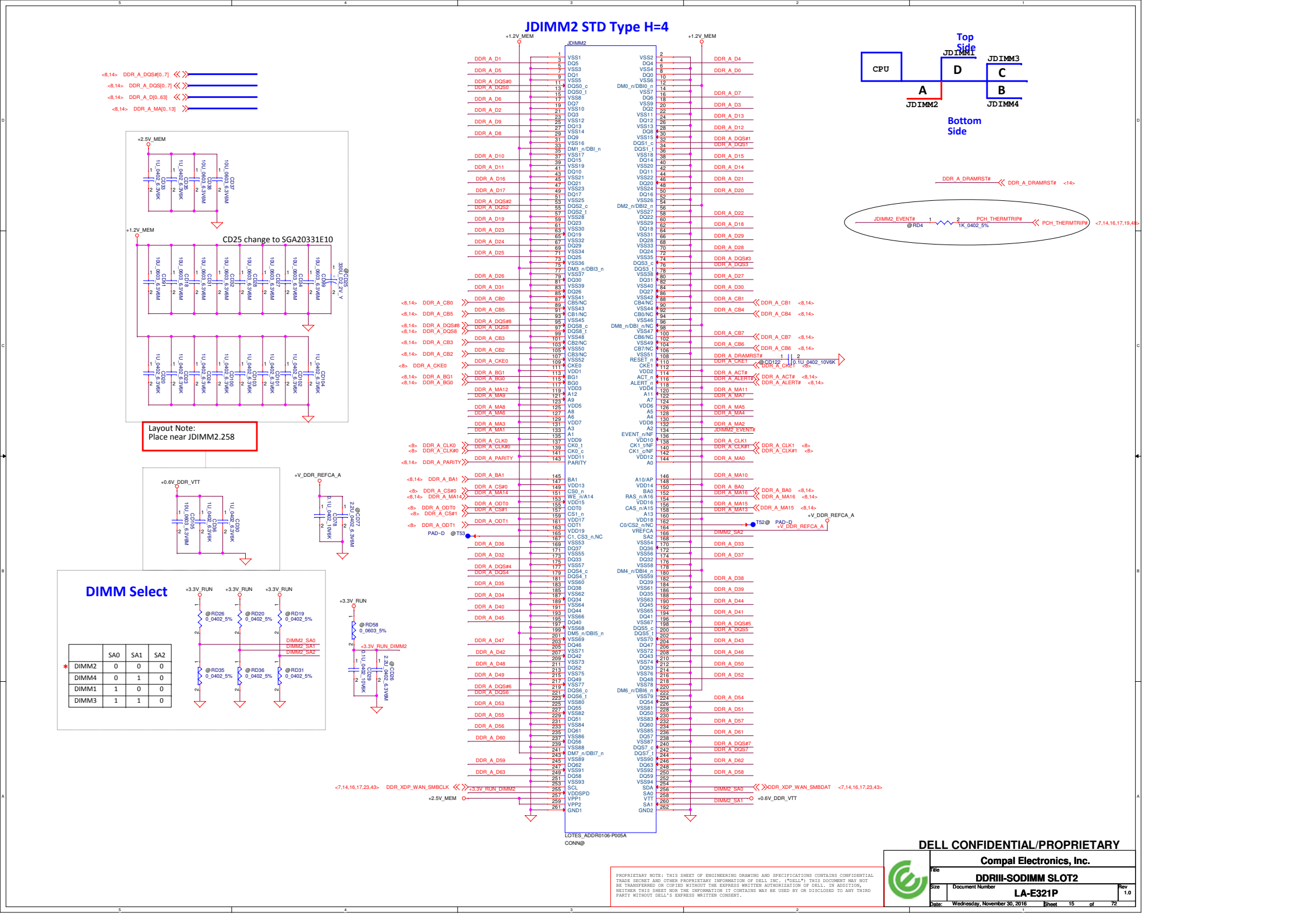
JDIMM2 STD Type H=4



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Compal Electronics, Inc.	
Title	DDRIII-SODIMM SLOT2
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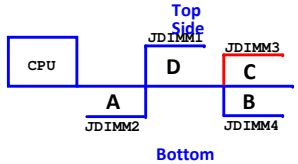
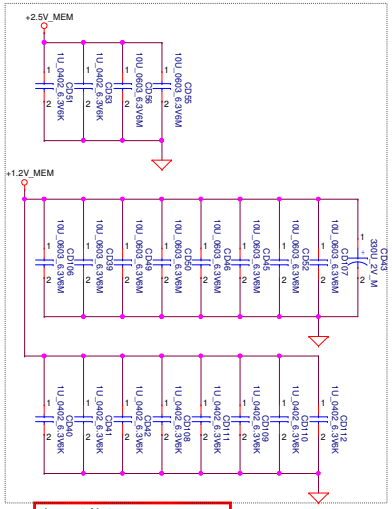
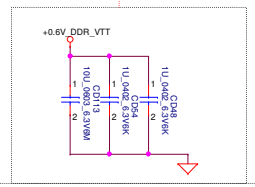
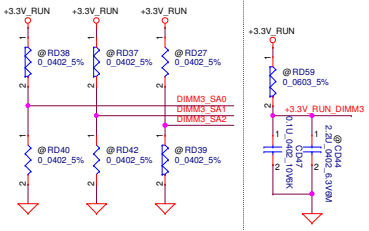
JDIMM3 STD Type H=5.2



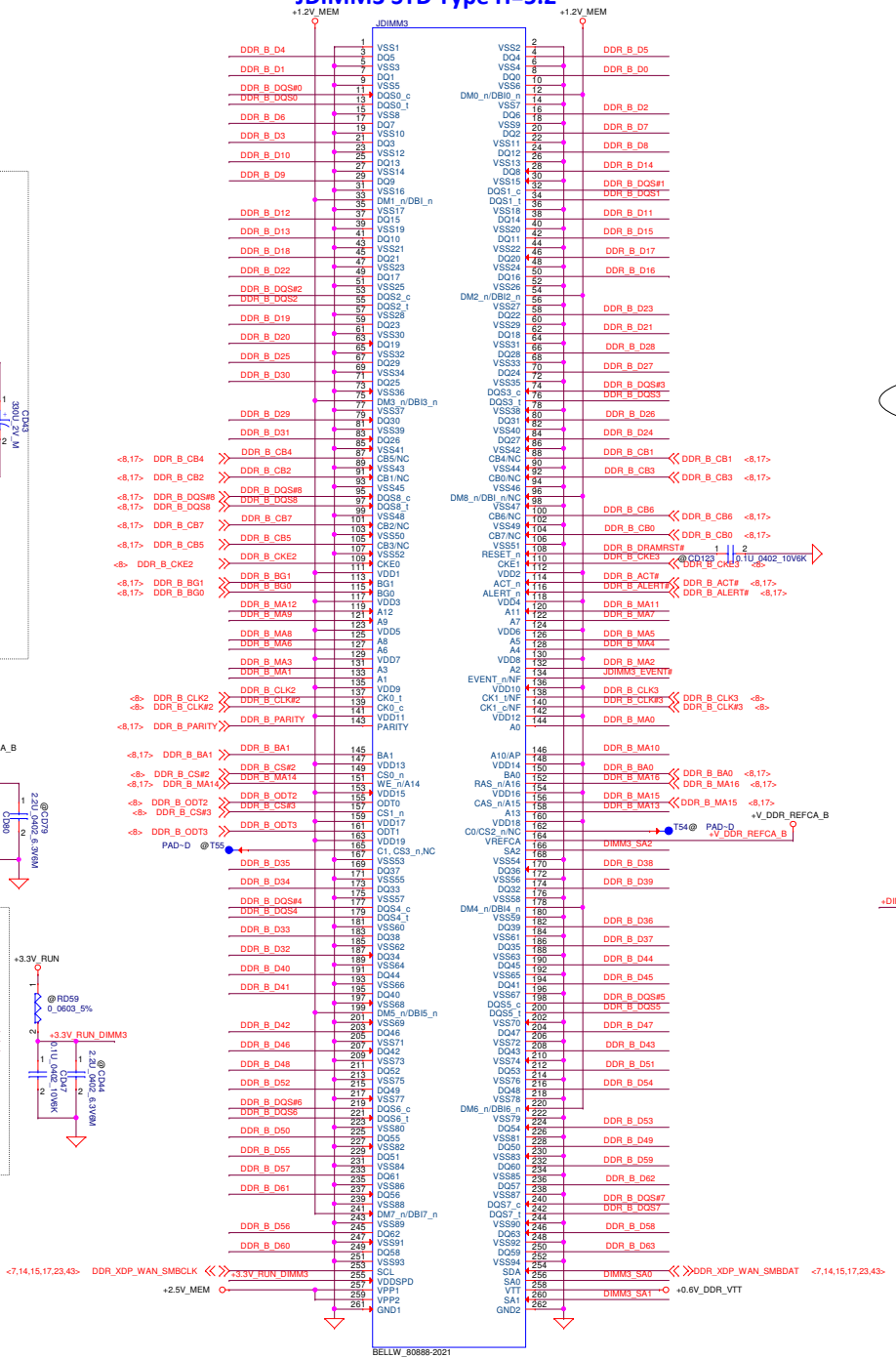


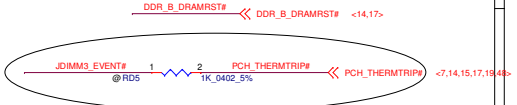


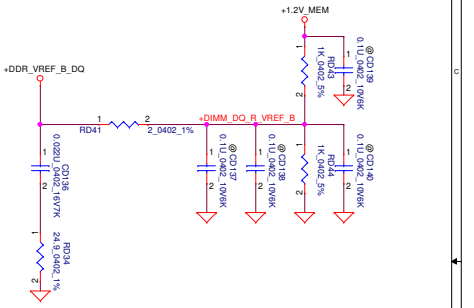
DIMM Select

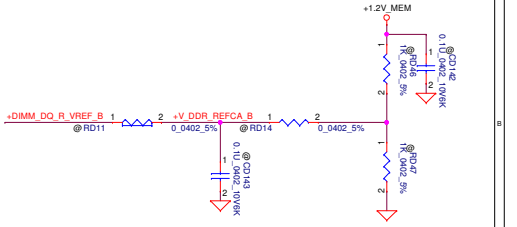


	SA0	SA1	SA2
DIMM2	0	0	0
DIMM4	0	1	0
DIMM1	1	0	0
* DIMM3	1	1	0









Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT3

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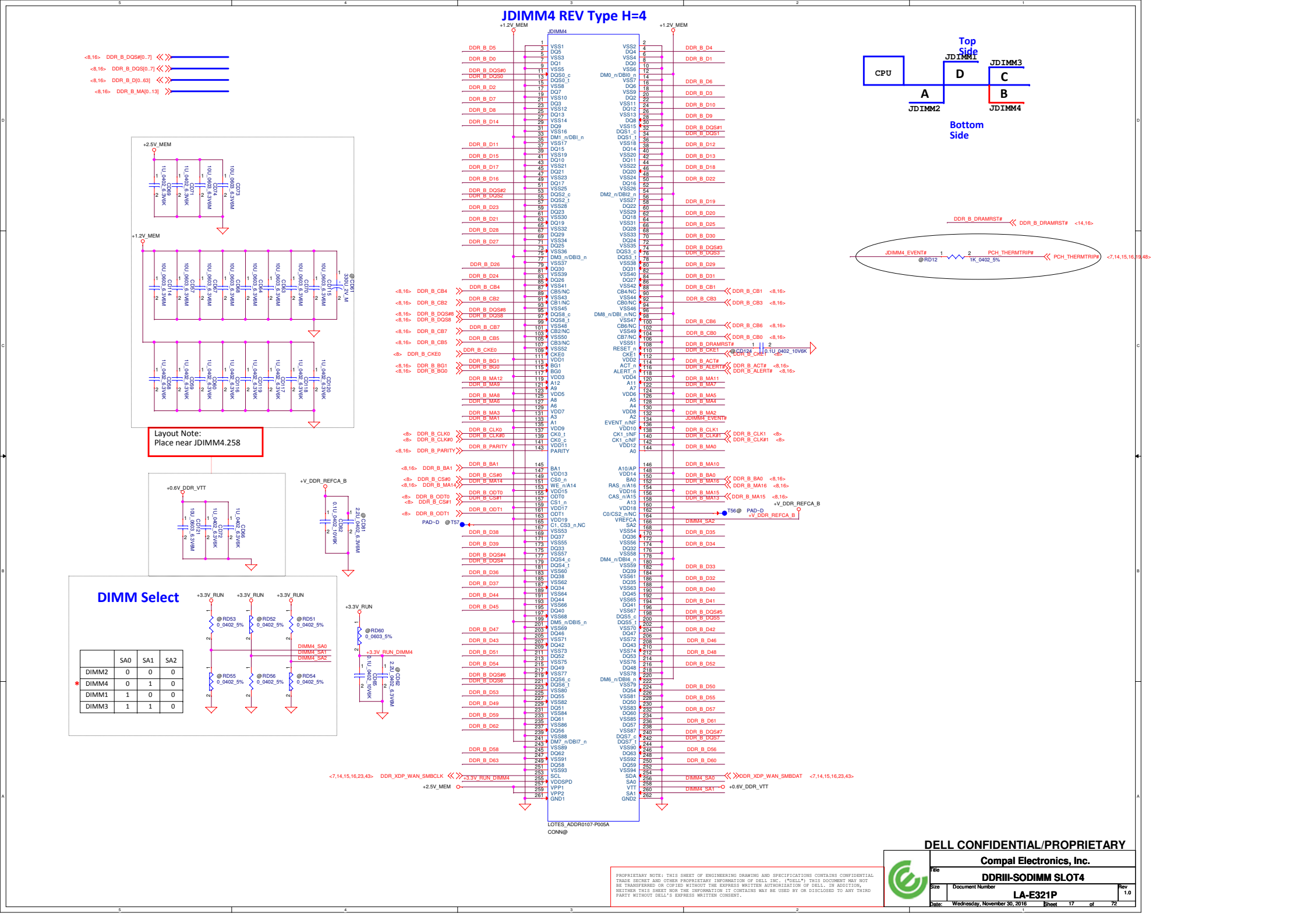
JDIMM4 REV Type H=4



	SA0	SA1	SA2
DIMM2	0	0	0
* DIMM4	0	1	0
DIMM1	1	0	0
DIMM3	1	1	0

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT4

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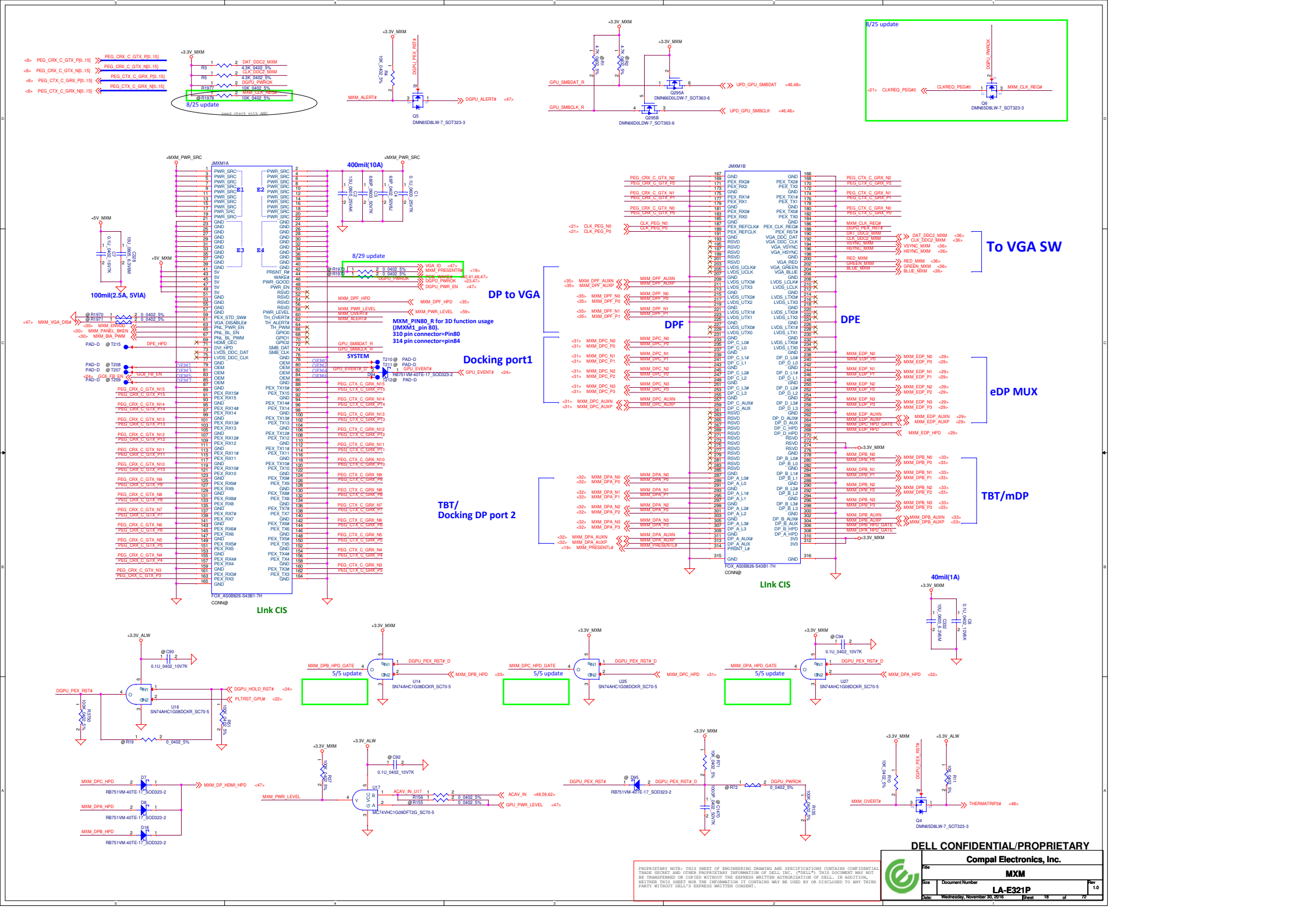
8/25 update
DGPU_PWROK
CLKREQ_PEG#0
MXM_CLK_REQ#
Q6
DMN65D8LW-7_SOT323-3
PEG_CRX_C_GTX_P[0..15]
PEG_CRX_C_GTX_N[0..15]
PEG_CTX_C_GRX_P[0..15]
PEG_CTX_C_GRX_N[0..15]
DAT_DDC2_MXM
CLK_DDC2_MXM
DGPU_PWROK
MXM_CLK_REQ#
10K_0402_5%
8/25 update
need check with AMD
MXM_ALERT#
DGPU_ALERT#
DGPU_PEX_RST#
Q5
DMN65D8LW-7_SOT323-3
GPU_SMBDAT_R
GPU_SMBCLK_R
UPD_GPU_SMBDAT
UPD_GPU_SMBCLK
Q295A
Q295B
DMN66D0LDW-7_SOT363-6
JMXM1A
JMXM1B
FOX_ASDB826-S43B1-7H
CONN@
100mil(2.5A, 5VIA)
400mil(10A)
8/29 update
VGA_ID
MXM_PRESENT#
DGPU_PWR_EN
MXM_DPF_HPD
MXM_PWR_LEVEL
MXM_OVERT#
MXM_ALERT#
MXM_PIN80_R for 3D function usage
(JMXM1_pin 80).
310 pin connector=Pin80
314 pin connector=pin84
SYSTEM
GPU_SMBDAT_R
GPU_SMBCLK_R
GPU_EVENT#
DP to VGA
Docking port1
TBT/
Docking DP port 2
DPF
DPE
To VGA SW
eDP MUX
TBT/mDP
Link CIS
Link CIS
40mil(1A)
5/5 update
U14
SN74AHC1G08DCKR_SC70-5
U16
SN74AHC1G08DCKR_SC70-5
U25
SN74AHC1G08DCKR_SC70-5
U27
SN74AHC1G08DCKR_SC70-5
U17
MC74VHC1G09DFT2G_SC70-5
RB751VM-40TE-17_SOD323-2
DGPU_HOLD_RST#
PLTRST_GPU#
ACAV_IN
GPU_PWR_LEVEL
THERMATRIP3#
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
MXM
LA-E321P
Wednesday, November 30, 2016
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6/28 update

+3.3V_ALW_PCH

1 RH366 2 TBT_CIO_PLUG_EVENT# 10K_0402_5%

5/9 update

+3.3V_ALW

1 @RH341 2 TBT_CIO_PLUG_EVENT# 10K_0402_5%

+3.3V_RUN

1 RH319 2 CAM_MIC_CBL_DET# 10K_0402_5%

1 RH317 2 MXM_PRESENTL# 10K_0402_5%

1 RH76 2 BIOS_REC 10K_0402_5%

1 RA58 2 SPK_DET# 10K_0402_5%

1 RH90 2 CONTACTLESS_DET# 10K_0402_5%

1 RH91 2 MXM_PRESENTR# 10K_0402_5%

1 RH321 2 SATA_EXP_IFDET 10K_0402_5%

1 RH323 2 SATAGP1 10K_0402_5%

1 RH324 2 HDD_DET# 10K_0402_5%

1 RH354 2 SATAGP5 10K_0402_5%

1 RH326 2 SATAGP6 10K_0402_5%

1 RH322 2 SATAGP7 10K_0402_5%

UH1C — SPT-H_PCH

CLINK

<40> PCH_CL_CLK1 — PCH_CL_CLK1 AV2 — CL_CLK
<40> PCH_CL_DATA1 — PCH_CL_DATA1 AV3 — CL_DATA
<40> PCH_CL_RST1# — PCH_CL_RST1# AW2 — CL_RST#

FAN

R44 GPP_G8/FAN_PWM_0
R45 GPP_G9/FAN_PWM_1
U36 GPP_G10/FAN_PWM_2
N42 GPP_G11/FAN_PWM_3

<30> CAM_MIC_CBL_DET# — CAM_MIC_CBL_DET# U43 — GPP_G0/FAN_TACH_0
TBT_CIO_PLUG_EVENT# U42 — GPP_G1/FAN_TACH_1
<46> TBT_CIO_PLUG_EVENT# — MXM_PRESENTL# U41 — GPP_G2/FAN_TACH_2
<18> MXM_PRESENTL# — CONTACTLESS_DET# M44 — GPP_G3/FAN_TACH_3
<39> CONTACTLESS_DET# U36 — GPP_G4/FAN_TACH_4
P44 — GPP_G5/FAN_TACH_5
<18> MXM_PRESENTR# — SPK_DET# T45 — GPP_G6/FAN_TACH_6
<46> SPK_DET# T44 — GPP_G7/FAN_TACH_7

PCIe/SATA

M.2 SSD Slot#3

<41> PCIE_PTX_DRX_P11 — PCIE_PTX_DRX_P11 B33 — PCIE11_TXP
<41> PCIE_PTX_DRX_N11 — PCIE_PTX_DRX_N11 C33 — PCIE11_TXN
<41> PCIE_PRX_DTX_P11 — PCIE_PRX_DTX_P11 K31 — PCIE11_RXP
<41> PCIE_PRX_DTX_N11 — PCIE_PRX_DTX_N11 L31 — PCIE11_RXN

Tell EC don't read GFX Temp.in GC6
High: Read; Low: Don't read

BIOS_REC AB33 — GPP_F10/SCLOCK
AB35 — GPP_F11/SLOAD
<47> GC6_THM_ON — RH342 @ 1 2 0_0402_5% — CS_CTR AA44 — GPP_F13/SDATAOUT0
AA45 — GPP_F12/SDATAOUT1

Dock

<45> SATA_PTX_DRX_N1 — SATA_PTX_DRX_N1 B38 — PCIE14_TXN/SATA1B_TXN
<45> SATA_PTX_DRX_P1 — SATA_PTX_DRX_P1 C38 — PCIE14_TXP/SATA1B_TXP
<45> SATA_PRX_DTX_N1 — SATA_PRX_DTX_N1 D39 — PCIE14_RXN/SATA1B_RXN
<45> SATA_PRX_DTX_P1 — SATA_PRX_DTX_P1 E37 — PCIE14_RXP/SATA1B_RXP

WWAN

<40> PCIE_PTX_DRX_N13 — PCIE_PTX_DRX_N13 C36 — PCIE13_TXN/SATA0B_TXN
<40> PCIE_PTX_DRX_P13 — PCIE_PTX_DRX_P13 B36 — PCIE13_TXP/SATA0B_TXP
<40> PCIE_PRX_DTX_N13 — PCIE_PRX_DTX_N13 G35 — PCIE13_RXN/SATA0B_RXN
<40> PCIE_PRX_DTX_P13 — PCIE_PRX_DTX_P13 E35 — PCIE13_RXP/SATA0B_RXP

M.2 SSD Slot#3

<41> PCIE_PTX_DRX_P12 — PCIE_PTX_DRX_P12 A35 — PCIE12_TXP
<41> PCIE_PTX_DRX_N12 — PCIE_PTX_DRX_N12 B35 — PCIE12_TXN
<41> PCIE_PRX_DTX_P12 — PCIE_PRX_DTX_P12 H33 — PCIE12_RXP
<41> PCIE_PRX_DTX_N12 — PCIE_PRX_DTX_N12 G33 — PCIE12_RXN

M.2 SSD Slot#4

<41> PCIE_PTX_DRX_P20 — PCIE_PTX_DRX_P20 J45 — PCIE20_TXP/SATA7_TXP
<41> PCIE_PTX_DRX_N20 — PCIE_PTX_DRX_N20 K44 — PCIE20_TXN/SATA7_TXN
<41> PCIE_PRX_DTX_P20 — PCIE_PRX_DTX_P20 N38 — PCIE20_RXP/SATA7_RXP
<41> PCIE_PRX_DTX_N20 — PCIE_PRX_DTX_N20 N39 — PCIE20_RXN/SATA7_RXN
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<41> PCIE_PTX_DRX_N19 — PCIE_PTX_DRX_N19 H43 — PCIE19_TXN/SATA6_TXN
<41> PCIE_PRX_DTX_P19 — PCIE_PRX_DTX_P19 L36 — PCIE19_RXP/SATA6_RXP
<41> PCIE_PRX_DTX_N19 — PCIE_PRX_DTX_N19 L37 — PCIE19_RXN/SATA6_RXN

SKL-H-PCH_BGA837 REV = 1.3 3 OF 12

PCIE9_RXN/SATA0A_RXN — G31 — PCIE_PRX_DTX_N9 — PCIE_PRX_DTX_N9 <41>
PCIE9_RXP/SATA0A_RXP — H31 — PCIE_PTX_DRX_N9 — PCIE_PRX_DTX_P9 <41>
PCIE9_TXN/SATA0A_TXN — G31 — PCIE_PTX_DRX_N9 — PCIE_PRX_DRX_N9 <41>
PCIE9_TXP/SATA0A_TXP — B31 — PCIE_PTX_DRX_P9 — PCIE_PRX_DRX_P9 <41>

M.2 SSD Slot#3

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PCIE10_RXP/SATA1A_RXP — E29 — PCIE_PTX_DRX_N10 — PCIE_PRX_DTX_P10 <41>
PCIE10_TXN/SATA1A_TXN — G32 — PCIE_PTX_DRX_N10 — PCIE_PRX_DRX_N10 <41>
PCIE10_TXP/SATA1A_TXP — B32 — PCIE_PTX_DRX_P10 — PCIE_PRX_DRX_P10 <41>

PCIE15_RXN/SATA2_RXN — F41 — PCIE_PRX_DTX_N15 — PCIE_PRX_DTX_N15 <44>
PCIE15_RXP/SATA2_RXP — E41 — PCIE_PTX_DRX_N15 — PCIE_PRX_DTX_P15 <44>
PCIE15_TXN/SATA2_TXN — B39 — PCIE_PTX_DRX_N15 — PCIE_PRX_DRX_N15 <44>
PCIE15_TXP/SATA2_TXP — A39 — PCIE_PTX_DRX_P15 — PCIE_PRX_DRX_P15 <44>

SATA Express

PCIE16_RXN/SATA3_RXN — D43 — PCIE_PRX_DTX_N16 — PCIE_PRX_DTX_N16 <44>
PCIE16_RXP/SATA3_RXP — E42 — PCIE_PTX_DRX_P16 — PCIE_PRX_DTX_P16 <44>
PCIE16_TXN/SATA3_TXN — A41 — PCIE_PTX_DRX_N16 — PCIE_PRX_DRX_N16 <44>
PCIE16_TXP/SATA3_TXP — A40 — PCIE_PTX_DRX_P16 — PCIE_PRX_DRX_P16 <44>

PCIE17_RXN/SATA4_RXN — H42 — PCIE_PRX_DTX_N17 — PCIE_PRX_DTX_N17 <41>
PCIE17_RXP/SATA4_RXP — H40 — PCIE_PTX_DRX_P17 — PCIE_PRX_DTX_P17 <41>
PCIE17_TXN/SATA4_TXN — E45 — PCIE_PTX_DRX_N17 — PCIE_PRX_DRX_N17 <41>
PCIE17_TXP/SATA4_TXP — F45 — PCIE_PTX_DRX_P17 — PCIE_PRX_DRX_P17 <41>

M.2 SSD Slot#4

PCIE18_RXN/SATA5_RXN — K37 — PCIE_PRX_DTX_N18 — PCIE_PRX_DTX_N18 <41>
PCIE18_RXP/SATA5_RXP — G37 — PCIE_PTX_DRX_P18 — PCIE_PRX_DTX_P18 <41>
PCIE18_TXN/SATA5_TXN — G45 — PCIE_PTX_DRX_N18 — PCIE_PRX_DRX_N18 <41>
PCIE18_TXP/SATA5_TXP — G44 — PCIE_PTX_DRX_P18 — PCIE_PRX_DRX_P18 <41>

GPP_E8/SATALED# — AD44 — PCH_SATA_LED# — PCH_SATA_LED# <49>
AG36 — M2_SLOT3_PEDET — M2_SLOT3_PEDET <41>
GPP_E0/SATAXPCIE0/SATAGP0 — AG35 — SATAGP1
GPP_E1/SATAXPCIE1/SATAGP1 — AG39 — HDD_DET# — HDD_DET# <43>
GPP_E2/SATAXPCIE2/SATAGP2 — AD35 — SATA_EXP_IFDET — SATA_EXP_IFDET <43,44>
GPP_F0/SATAXPCIE3/SATAGP3 — AD31 — M2_SLOT4_PEDET — M2_SLOT4_PEDET <41>
GPP_F1/SATAXPCIE4/SATAGP4 — AD38 — SATAGP5
GPP_F2/SATAXPCIE5/SATAGP5 — AC43 — SATAGP6
GPP_F3/SATAXPCIE6/SATAGP6 — AB44 — SATAGP7
GPP_F4/SATAXPCIE7/SATAGP7

BIA_PWM_PCH — W36 — BIA_PWM_PCH — BIA_PWM_PCH <30>
GPP_F21/EDP_BKLTCTL — W35 — PANEL_BKEN_PCH — PANEL_BKEN_PCH <30>
GPP_F20/EDP_BKLTEN — W42 — ENVDD_PCH — ENVDD_PCH <30,48>
GPP_F19/EDP_VDDEN

9/12 update

PCH_THERMTRIP# — AJ3 — PCH_THERMTRIP# — RH75 1 2 620_0402_5% — PCH_THERMTRIP# — PCH_THERMTRIP# <7,14,15,16,17,48>
THERMTRIP# — AL3 — PCH_PECI — RH73 1 2 13_0402_5% — H_PECI — H_PECI <7,48>
PECI — AJ4 — H_PM_SYNC_R — RH3601 2 30_0402_5% — H_PM_SYNC — H_PM_SYNC <7>
PM_SYNC — AK2 — PLTRST_CPU# — PLTRST_CPU# <7>
PLTRST_PROC# — AH2 — H_PM_DOWN — H_PM_DOWN <7>
PM_DOWN

HOST

SPSGP0	1	M2_SLOT3_PEDET	0=SATA	1=PCIE
SPSGP3	0	SATA_EXP_IFDET	0=SATA	1=PCIE
SPSGP4	0	M2_SLOT4_PEDET	0=SATA	1=PCIE

5/11 update

H_PM_DOWN — 1 @RH365 10K_0402_5% 2

PCH_PECI — 1 @RH74 10K_0402_5% 2

Compal Electronics, Inc.

Title: SKYLAKE PCH-H (1/9)

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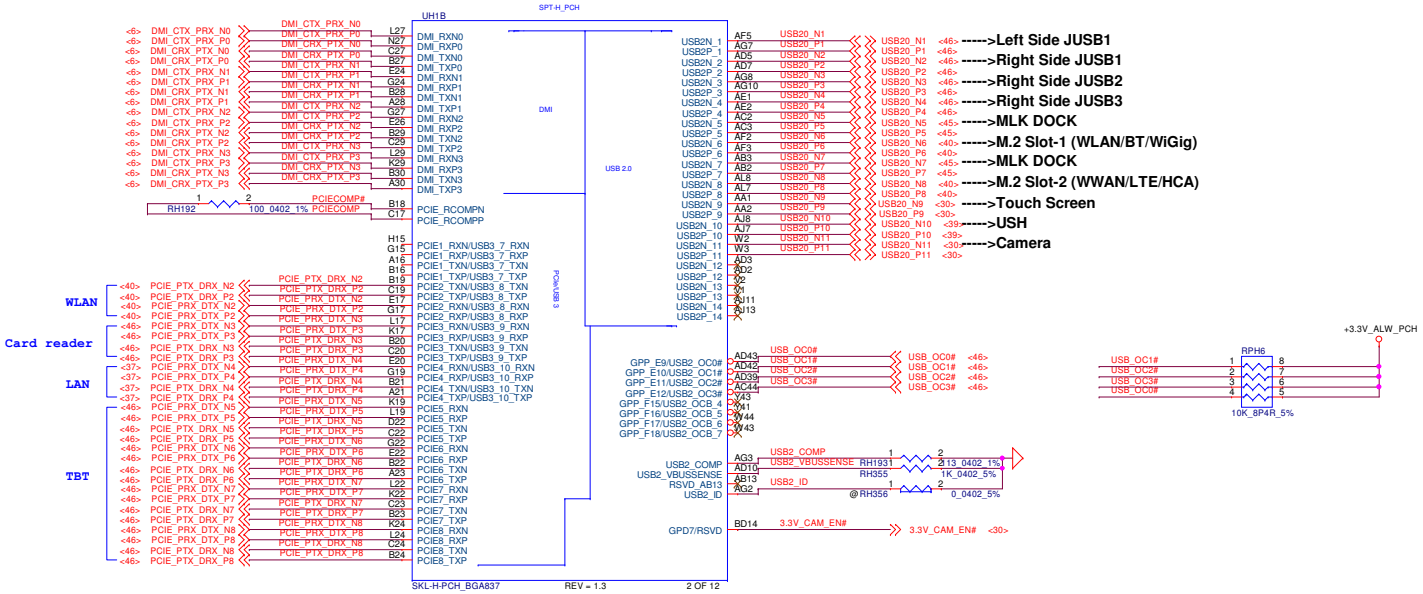
5/5 update



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Compal Electronics, Inc.

Title: SKYLAKE PCH-H (2/9)

Size | Document Number: LA-E321P | Rev: 1.0

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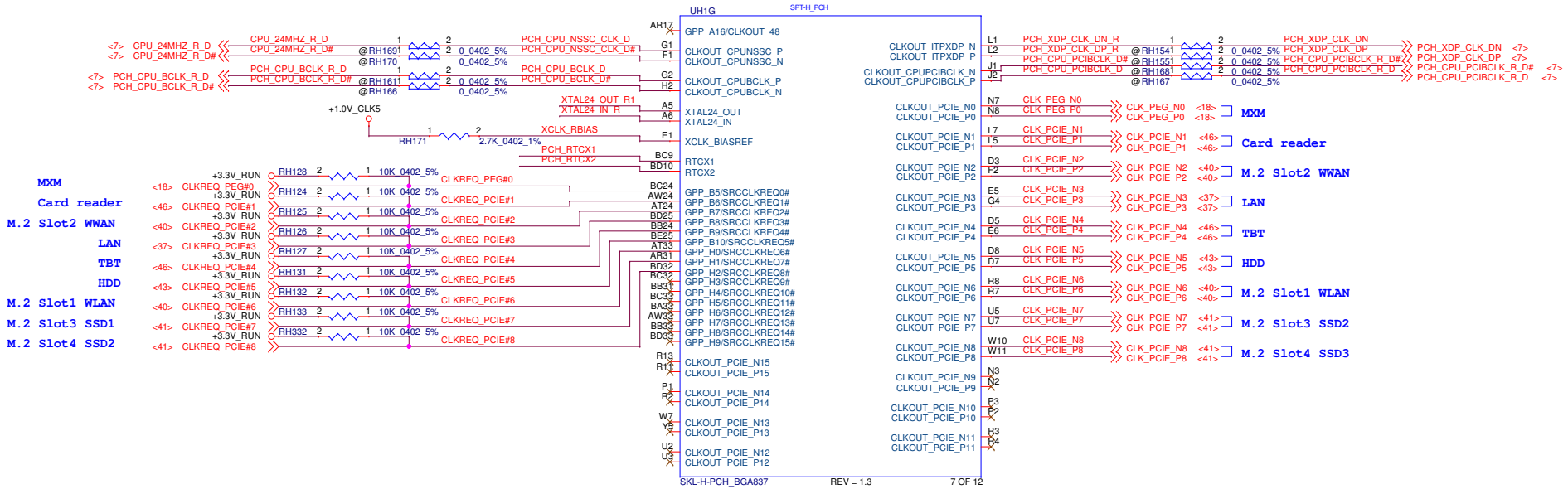
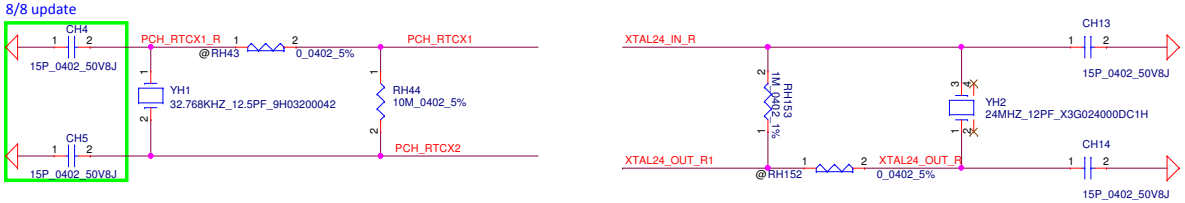


8/8 update



Compal Electronics, Inc.

Title: SKYLAKE PCH-H (3/9)

Size | Document Number: LA-E321P | Rev: 1.0

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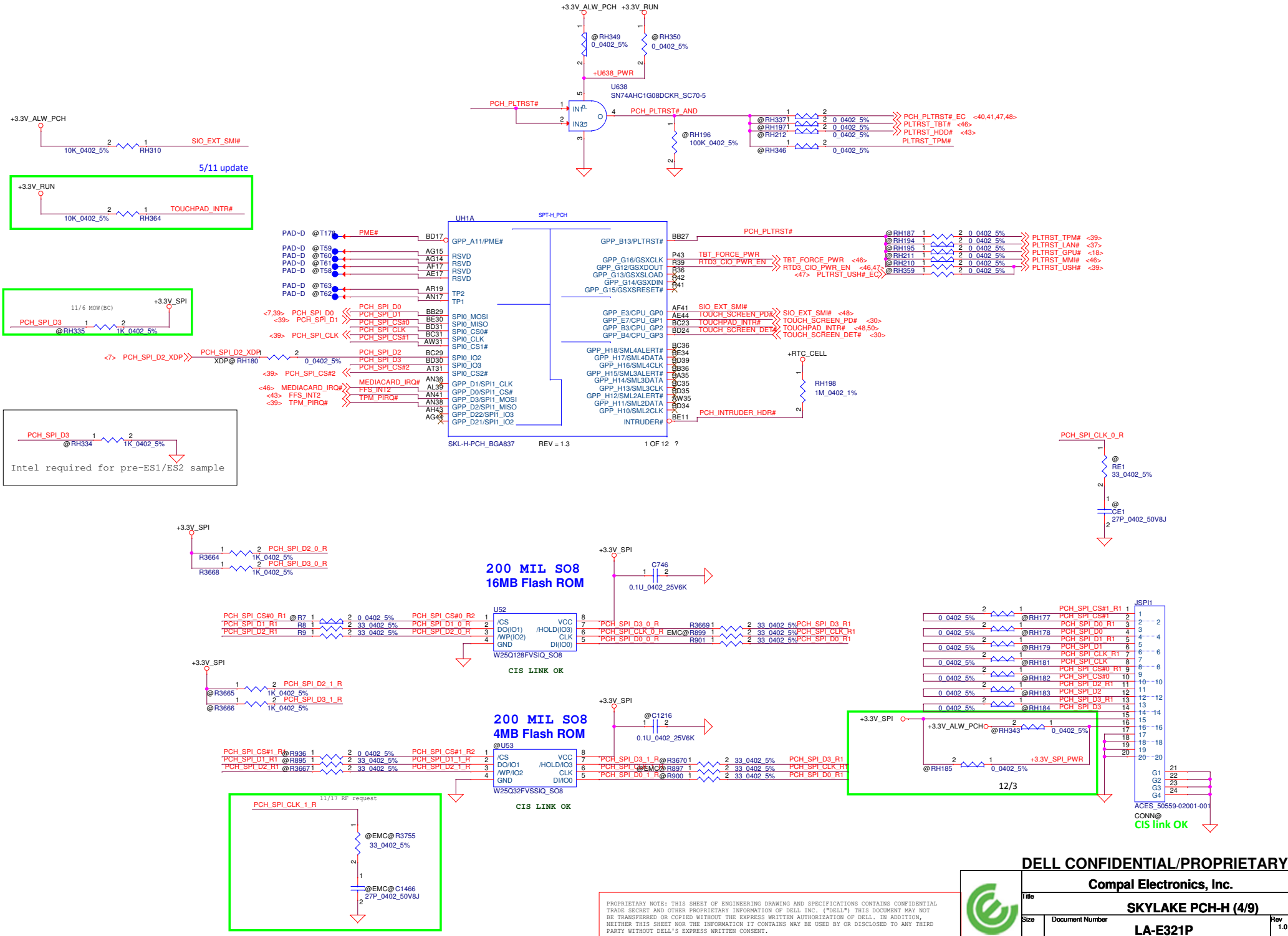
+3.3V_ALW_PCH
+3.3V_RUN
@RH349 0_0402_5%
@RH350 0_0402_5%
+U638_PWR
U638
SN74AHC1G08DCKR_SC70-5
PCH_PLTRST#
PCH_PLTRST#_AND
@RH196 100K_0402_5%
@RH3371
@RH1971
@RH212
@RH346
PCH_PLTRST#_EC <40,41,47,48>
PLTRST_TBT# <46>
PLTRST_HDD# <43>
PLTRST_TPM#
+3.3V_ALW_PCH
10K_0402_5%
RH310
SIO_EXT_SMI#
5/11 update
+3.3V_RUN
10K_0402_5%
RH364
TOUCHPAD_INTR#
UH1A
SPT-H_PCH
SKL-H-PCH_BGA837
REV = 1.3
1 OF 12
PME#
GPP_A11/PME#
RSVD
TP1
SPI0_MOSI
SPI0_MISO
SPI0_CS0#
SPI0_CLK
SPI0_CS1#
SPI0_IO2
SPI0_IO3
SPI0_CS2#
GPP_D1/SPI1_CLK
GPP_D0/SPI1_CS#
GPP_D3/SPI1_MOSI
GPP_D2/SPI1_MISO
GPP_D22/SPI1_IO3
GPP_D21/SPI1_IO2
GPP_B13/PLTRST#
GPP_G16/GSXCLK
GPP_G12/GSXDOUT
GPP_G13/GSXSLOAD
GPP_G14/GSXDIN
GPP_G15/GSXSRESET#
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
GPP_H18/SML4ALERT#
GPP_H17/SML4DATA
GPP_H16/SML4CLK
GPP_H15/SML3ALERT#
GPP_H14/SML3DATA
GPP_H13/SML3CLK
GPP_H12/SML2ALERT#
GPP_H11/SML2DATA
GPP_H10/SML2CLK
INTRUDER#
PCH_PLTRST#
TBT_FORCE_PWR
RTD3_CIO_PWR_EN
PLTRST_USH# <47>
SIO_EXT_SMI# <48>
TOUCH_SCREEN_PD#
TOUCHPAD_INTR#
TOUCH_SCREEN_DET#
PCH_INTRUDER_HDR#
+RTC_CELL
RH198 1M_0402_1%
PLTRST_TPM# <39>
PLTRST_LAN# <37>
PLTRST_GPU# <18>
PLTRST_MMI# <46>
PLTRST_USH# <39>
11/6 MOW(BC)
+3.3V_SPI
PCH_SPI_D3
@RH335 1K_0402_5%
PCH_SPI_D0
PCH_SPI_D1
PCH_SPI_CS#0
PCH_SPI_CLK
PCH_SPI_CS#1
PCH_SPI_D2
PCH_SPI_D3
PCH_SPI_CS#2
MEDIACARD_IRQ#
FFS_INT2
TPM_PIRQ#
PCH_SPI_D2_XDP
XDP@ RH180 0_0402_5%
PCH_SPI_D3
@RH334 1K_0402_5%
Intel required for pre-ES1/ES2 sample
PCH_SPI_CLK_0_R
@ RE1 33_0402_5%
@ CE1 27P_0402_50V8J
+3.3V_SPI
R3664 1K_0402_5%
R3668 1K_0402_5%
PCH_SPI_D2_0_R
PCH_SPI_D3_0_R
200 MIL SO8
16MB Flash ROM
C746 0.1U_0402_25V6K
U52
/CS
DO(IO1)
/WP(IO2)
GND
VCC
/HOLD(IO3)
CLK
DI(IO0)
W25Q128FVSIQ_SO8
CIS LINK OK
PCH_SPI_CS#0_R1
PCH_SPI_D1_R1
PCH_SPI_D2_R1
R7
R8
R9
PCH_SPI_CS#0_R2
PCH_SPI_D1_0_R
PCH_SPI_D2_0_R
R3669
R899
R901
PCH_SPI_D3_R1
PCH_SPI_CLK_R1
PCH_SPI_D0_R1
R3665 1K_0402_5%
R3666 1K_0402_5%
PCH_SPI_D2_1_R
PCH_SPI_D3_1_R
200 MIL SO8
4MB Flash ROM
@C1216 0.1U_0402_25V6K
@U53
W25Q32FVSSIQ_SO8
CIS LINK OK
PCH_SPI_CS#1_R1
PCH_SPI_D1_R1
PCH_SPI_D2_R1
@R936
@R895
@R3667
PCH_SPI_CS#1_R2
PCH_SPI_D1_1_R
PCH_SPI_D2_1_R
@R3670
@EMC@R897
@R900
PCH_SPI_D3_R1
PCH_SPI_CLK_R1
PCH_SPI_D0_R1
11/17 RF request
PCH_SPI_CLK_1_R
@EMC@R3755 33_0402_5%
@EMC@C1466 27P_0402_50V8J
JSPI1
PCH_SPI_CS#1_R1
PCH_SPI_CS#1
PCH_SPI_D0_R1
PCH_SPI_D0
PCH_SPI_D1_R1
PCH_SPI_D1
PCH_SPI_CLK_R1
PCH_SPI_CLK
PCH_SPI_CS#0_R1
PCH_SPI_CS#0
PCH_SPI_D2_R1
PCH_SPI_D2
PCH_SPI_D3_R1
PCH_SPI_D3
@RH177
@RH178
@RH179
@RH181
@RH182
@RH183
@RH184
+3.3V_ALW_PCH
@RH343 0_0402_5%
@RH185 0_0402_5%
+3.3V_SPI_PWR
12/3
ACES_50559-02001-001
CONN@
CIS link OK
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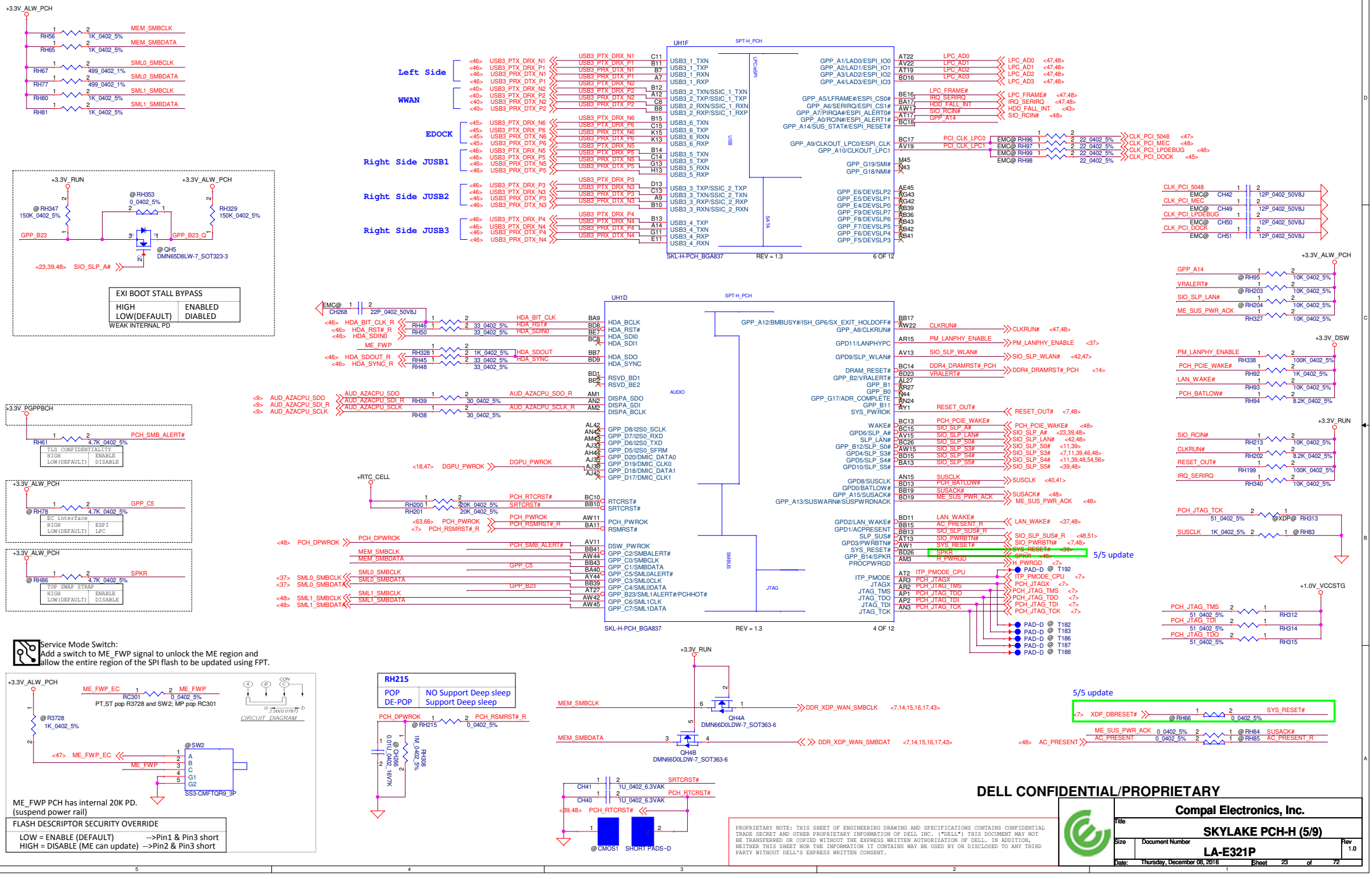
+3.3V_ALW_PCH
MEM_SMBCLK
MEM_SMBDATA
SML0_SMBCLK
SML0_SMBDATA
SML1_SMBCLK
SML1_SMBDATA
1K_0402_5%
499_0402_1%
Left Side
WWAN
EDOCK
Right Side JUSB1
Right Side JUSB2
Right Side JUSB3
UH1F
SPT-H_PCH
SKL-H-PCH_BGA837
REV = 1.3
6 OF 12
+3.3V_RUN
@RH353
0_0402_5%
@RH347
150K_0402_5%
RH329
150K_0402_5%
GPP_B23
GPP_B23_Q
@QH5
DMN65D8LW-7_SOT323-3
<23,39,48> SIO_SLP_A#
EXI BOOT STALL BYPASS
HIGH ENABLED
LOW(DEFAULT) DIABLED
WEAK INTERNAL PD
+3.3V_PGPPBCH
PCH_SMB_ALERT#
4.7K_0402_5%
TLS CONFIDENTIALITY
HIGH ENABLE
LOW(DEFAULT) DISABLE
+3.3V_ALW_PCH
@RH78
GPP_C5
EC interface
HIGH ESPI
LOW(DEFAULT) LPC
@RH86
SPKR
TOP SWAP STRAP
HIGH ENABLE
LOW(DEFAULT) DISABLE
UH1D
AUDIO
SYSPWR
JTAG
SKL-H-PCH_BGA837
REV = 1.3
4 OF 12
+RTC_CELL
RH200
RH201
20K_0402_5%
PCH_RTCRST#
SRTCRST#
RTCRST#
PCH_PWROK
PCH_RSMRST#_R
DSW_PWROK
DGPU_PWROK
PCH_DPWROK
PCH_SMB_ALERT#
MEM_SMBCLK
MEM_SMBDATA
GPP_C5
SML0_SMBCLK
SML0_SMBDATA
GPP_B23
SML1_SMBCLK
SML1_SMBDATA
HDA_BIT_CLK
HDA_RST#
HDA_SDI0
HDA_SDI1
HDA_SDOUT
HDA_SYNC
HDA_SDO
HDA_BCLK
HDA_SYNC
RSVD_BD1
RSVD_BE2
AUD_AZACPU_SDO
AUD_AZACPU_SDI_R
AUD_AZACPU_SCLK
AUD_AZACPU_SDO_R
AUD_AZACPU_SCLK_R
DISPA_SDO
DISPA_SDI
DISPA_BCLK
GPP_D8/I2S0_SCLK
GPP_D7/I2S0_RXD
GPP_D6/I2S0_TXD
GPP_D5/I2S0_SFRM
GPP_D20/DMIC_DATA0
GPP_D19/DMIC_CLK0
GPP_D18/DMIC_DATA1
GPP_D17/DMIC_CLK1
GPP_A12/BMBUSY#/ISH_GP6/SX_EXIT_HOLDOFF#
GPP_A8/CLKRUN#
GPD11/LANPHYPC
GPD9/SLP_WLAN#
DRAM_RESET#
GPP_B2/VRALERT#
GPP_B1
GPP_B0
GPP_G17/ADR_COMPLETE
GPP_B11
SYS_PWROK
WAKE#
GPD6/SLP_A#
SLP_LAN#
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
GPD8/SUSCLK
GPD0/BATLOW#
GPP_A15/SUSACK#
GPP_A13/SUSWARN#/SUSPWRDNACK
GPD2/LAN_WAKE#
GPD1/ACPRESENT
SLP_SUS#
GPD3/PWRBTN#
SYS_RESET#
GPP_B14/SPKR
PROCPWRGD
ITP_PMODE
JTAGX
JTAG_TMS
JTAG_TDO
JTAG_TDI
JTAG_TCK
CLKRUN#
PM_LANPHY_ENABLE
SIO_SLP_WLAN#
DDR4_DRAMRST#_PCH
VRALERT#
RESET_OUT#
PCH_PCIE_WAKE#
SIO_SLP_A#
SIO_SLP_LAN#
SIO_SLP_S0#
SIO_SLP_S3#
SIO_SLP_S4#
SIO_SLP_S5#
SUSCLK
PCH_BATLOW#
SUSACK#
ME_SUS_PWR_ACK
LAN_WAKE#
AC_PRESENT_R
SIO_SLP_SUS#_R
SIO_PWRBTN#
SYS_RESET#
SPKR
H_PWRGD
PAD-D @ T192
ITP_PMODE_CPU
PCH_JTAGX
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK
PAD-D @ T182
PAD-D @ T183
PAD-D @ T186
PAD-D @ T187
PAD-D @ T188
5/5 update
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
IRQ_SERIRQ
HDD_FALL_INT
SIO_RCIN#
GPP_A14
PCH_PCIE_WAKE#
PCH_LANPHY_ENABLE
SIO_SLP_WLAN#
DDR4_DRAMRST#_PCH
VRALERT#
RESET_OUT#
SIO_SLP_LAN#
SIO_SLP_S0#
SIO_SLP_S3#
SIO_SLP_S4#
SIO_SLP_S5#
SUSCLK
PCH_BATLOW#
SUSACK#
ME_SUS_PWR_ACK
LAN_WAKE#
SIO_SLP_SUS#_R
SIO_PWRBTN#
SYS_RESET#
SPKR
H_PWRGD
PCH_JTAG_TCK
PCH_JTAGX
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK
CLK_PCI_5048
CLK_PCI_MEC
CLK_PCI_LPDEBUG
CLK_PCI_DOCK
PCI_CLK_LPC0
PCI_CLK_LPC1
+3.3V_DSW
+3.3V_RUN
+1.0V_VCCSTG
Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.
+3.3V_ALW_PCH
ME_FWP_EC
RC301
0_0402_5%
PT,ST pop R3728 and SW2; MP pop RC301
CIRCUIT DIAGRAM
@R3728
1K_0402_5%
@SW2
SS3-CMFTQR9_3P
ME_FWP PCH has internal 20K PD. (suspend power rail)
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = ENABLE (DEFAULT) -->Pin1 & Pin3 short
HIGH = DISABLE (ME can update) -->Pin2 & Pin3 short
RH215
POP NO Support Deep sleep
DE-POP Support Deep sleep
@RH215
0_0402_5%
@CH326
0.01U_0402_16V7K
1M_0402_5%
RH308
SRTCRST#
PCH_RTCRST#
1U_0402_6.3V6K
@CMOS1
SHORT PADS-D
QH4A
QH4B
DMN66D0LDW-7_SOT363-6
DDR_XDP_WAN_SMBCLK
DDR_XDP_WAN_SMBDAT
5/5 update
XDP_DBRESET#
SYS_RESET#
ME_SUS_PWR_ACK
AC_PRESENT
SUSACK#
AC_PRESENT_R
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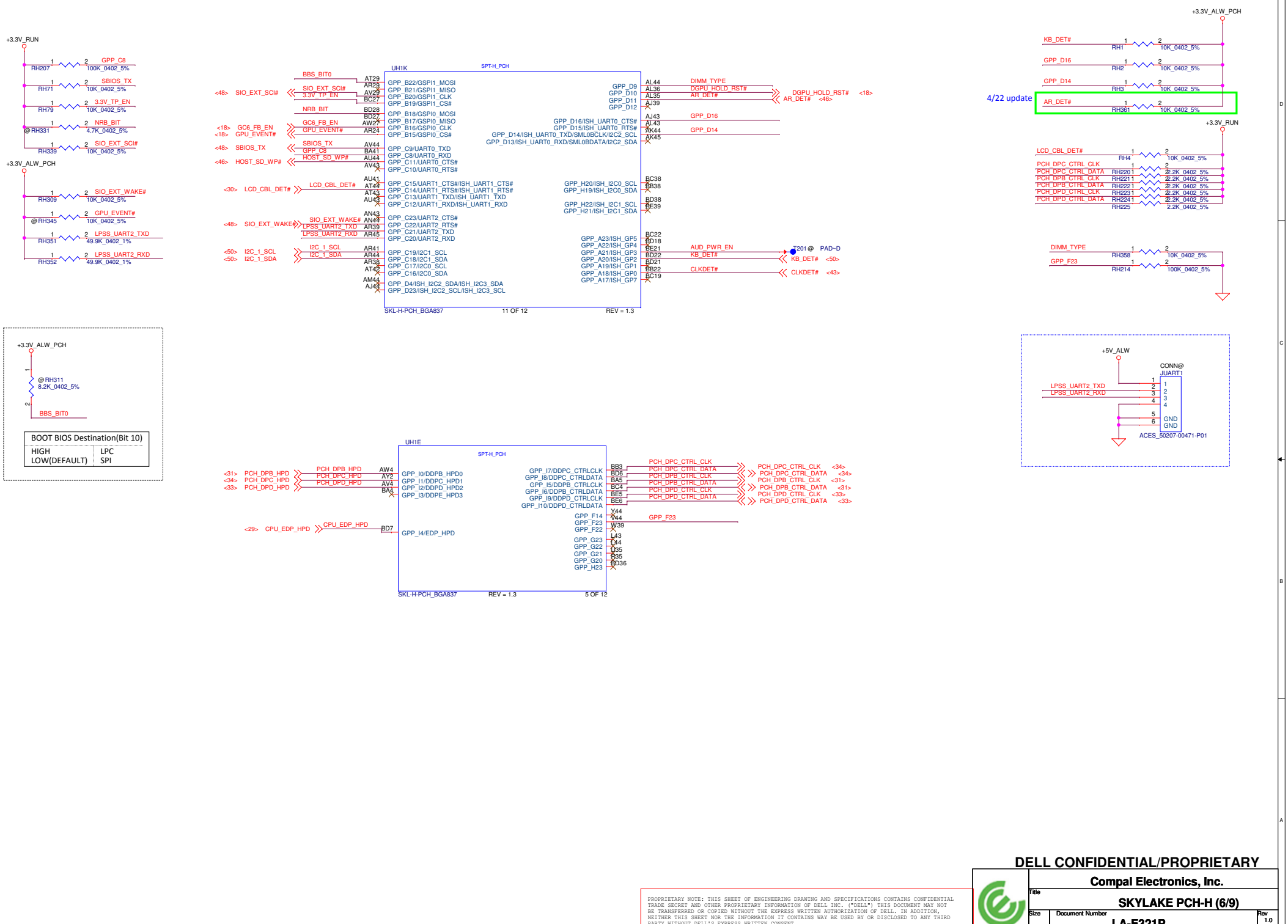
+3.3V_RUN
RH207 GPP_C8 100K_0402_5%
RH71 SBIOS_TX 10K_0402_5%
RH79 3.3V_TP_EN 10K_0402_5%
@RH331 NRB_BIT 4.7K_0402_5%
RH339 SIO_EXT_SCI# 10K_0402_5%
+3.3V_ALW_PCH
RH309 SIO_EXT_WAKE# 10K_0402_5%
@RH345 GPU_EVENT# 10K_0402_5%
RH351 LPSS_UART2_TXD 49.9K_0402_1%
RH352 LPSS_UART2_RXD 49.9K_0402_1%
UH1K
SPT-H_PCH
SKL-H-PCH_BGA837
11 OF 12
REV = 1.3
BBS_BIT0
SIO_EXT_SCI#
3.3V_TP_EN
NRB_BIT
GC6_FB_EN
GPU_EVENT#
SBIOS_TX
GPP_C8
HOST_SD_WP#
LCD_CBL_DET#
SIO_EXT_WAKE#
LPSS_UART2_TXD
LPSS_UART2_RXD
I2C_1_SCL
I2C_1_SDA
GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B20/GSPI1_CLK
GPP_B19/GSPI1_CS#
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B16/GSPI0_CLK
GPP_B15/GSPI0_CS#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_D4/ISH_I2C2_SDA/ISH_I2C3_SDA
GPP_D23/ISH_I2C2_SCL/ISH_I2C3_SCL
GPP_D9
GPP_D10
GPP_D11
GPP_D12
GPP_D16/ISH_UART0_CTS#
GPP_D15/ISH_UART0_RTS#
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C2_SCL
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C2_SDA
GPP_H20/ISH_I2C0_SCL
GPP_H19/ISH_I2C0_SDA
GPP_H22/ISH_I2C1_SCL
GPP_H21/ISH_I2C1_SDA
GPP_A23/ISH_GP5
GPP_A22/ISH_GP4
GPP_A21/ISH_GP3
GPP_A20/ISH_GP2
GPP_A19/ISH_GP1
GPP_A18/ISH_GP0
GPP_A17/ISH_GP7
DIMM_TYPE
DGPU_HOLD_RST#
AR_DET#
GPP_D16
GPP_D14
AUD_PWR_EN
KB_DET#
CLKDET#
T201@ PAD~D
DGPU_HOLD_RST# <18>
AR_DET# <46>
KB_DET# <50>
CLKDET# <43>
+3.3V_ALW_PCH
KB_DET# RH1 10K_0402_5%
GPP_D16 RH2 10K_0402_5%
GPP_D14 RH3 10K_0402_5%
AR_DET# RH361 10K_0402_5%
4/22 update
+3.3V_RUN
LCD_CBL_DET# RH4 10K_0402_5%
PCH_DPC_CTRL_CLK RH2201 2.2K_0402_5%
PCH_DPC_CTRL_DATA RH2211 2.2K_0402_5%
PCH_DPB_CTRL_CLK RH2221 2.2K_0402_5%
PCH_DPB_CTRL_DATA RH2231 2.2K_0402_5%
PCH_DPD_CTRL_CLK RH2241 2.2K_0402_5%
PCH_DPD_CTRL_DATA RH225 2.2K_0402_5%
DIMM_TYPE RH358 10K_0402_5%
GPP_F23 RH214 100K_0402_5%
+3.3V_ALW_PCH
@RH311 8.2K_0402_5%
BBS_BIT0
BOOT BIOS Destination(Bit 10)
HIGH LPC
LOW(DEFAULT) SPI
+5V_ALW
CONN@
JUART1
LPSS_UART2_TXD
LPSS_UART2_RXD
GND
GND
ACES_50207-00471-P01
UH1E
SPT-H_PCH
SKL-H-PCH_BGA837
REV = 1.3
5 OF 12
PCH_DPB_HPD
PCH_DPC_HPD
PCH_DPD_HPD
CPU_EDP_HPD
GPP_I0/DDPB_HPD0
GPP_I1/DDPC_HPD1
GPP_I2/DDPD_HPD2
GPP_I3/DDPE_HPD3
GPP_I4/EDP_HPD
GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
GPP_F14
GPP_F23
GPP_F22
GPP_G23
GPP_G22
GPP_G21
GPP_G20
GPP_H23
PCH_DPC_CTRL_CLK
PCH_DPC_CTRL_DATA
PCH_DPB_CTRL_CLK
PCH_DPB_CTRL_DATA
PCH_DPD_CTRL_CLK
PCH_DPD_CTRL_DATA
GPP_F23
<31> PCH_DPB_HPD
<34> PCH_DPC_HPD
<33> PCH_DPD_HPD
<29> CPU_EDP_HPD
PCH_DPC_CTRL_CLK <34>
PCH_DPC_CTRL_DATA <34>
PCH_DPB_CTRL_CLK <31>
PCH_DPB_CTRL_DATA <31>
PCH_DPD_CTRL_CLK <33>
PCH_DPD_CTRL_DATA <33>
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RH254 PN change to SD000017R00

+1.0V_PRIM → +1.0V_ALW_PCH : RH254 0_1206_5%

+1.0V_ALW_PCH → +1.0V_DSW : @RH255 0.0454A 0_0402_5%

+1.0V_ALW_PCH → +1.0V_CLK1 : @RH256 0.0348A 0_0402_5%

+1.0V_ALW_PCH → +1.0V_CLK3 : @RH257 0.0237A 0_0402_5%

+1.0V_ALW_PCH → +1.0V_CLK4 : @RH258 0.0327A 0_0402_5%

+1.0V_ALW_PCH → +1.0V_CLK2 : @RH259 0.205A 0_0402_5%

+1.0V_ALW_PCH → +1.0V_F24 : @RH260 0.0046A 0_0402_5%

+1.0V_ALW_PCH → +1.0V_DUSB : @RH286 0.533A 0_0402_5%

+1.0V_ALW_PCH → +2.8V_FHV : @RH287 0.0908A 0_0402_5%

+1.0V_ALW_PCH → +1.0V_DTS : @RH288 0.0061A 0_0402_5%

PJP@ PJP8 JUMP_43X79 : +1.0V_ALW_PCH → +1.0V_MPHY 2.10A

+1.0V_ALW_PCH → +1.0V_AMPHYPLL : @RH289 0.0248A 0_0402_5%

+1.0V_ALW_PCH → +1.0V_APLLEBB : @RH290 0.095A 0_0402_5%

+3.3V_ALW → +3.3V_PUSBDSW : @RH276 0_0603_5%

+RTC_CELL → +3.3V_PRTC : @RH297 0.0002A 0_0402_5%

+3.3V_ALW_PCH → +3.3V_ALW_PCHRES : @RH279 0_0603_5%

+3.3V_ALW_PCHRES → +3.3V_1.8V_GPPA : @RH291 0.0879A 0_0402_5%

+1.8V_ALW_PCHRES : @RH294 0_0402_5%

+3.3V_ALW_PCHRES → +3.3V_1.8V_AZIO : @RH292 0.075A 0_0402_5%

+1.8V_ALW_PCHRES : @RH295 0_0402_5%

+3.3V_ALW_PCHRES → +3.3V_1.8V_GPPD : @RH293 0.0395A 0_0402_5%

+1.8V_ALW_PCHRES : @RH296 0_0402_5%

+3.3V_ALW_PCH → +3.3V_PRTCPRIM : @RH298 0.0002A 0_0402_5%

+3.3V_PHVC : @RH299 0.2875A 0_0402_5%

+3.3V_1.8V_FUSE : @RH300 0.0811A 0_0402_5%

+3.3V_DSW : @RH306 0.0811A 0_0402_5%

+3.3V_ALW : @RH301 0.403A 0_0603_5%

+3.3V_RUN → +3.3V_RUN_ATS : @RH302 0.0066A 0_0402_5%

+3.3V_ALW_PCH → +3.3V_PGPPEF : @RH303 0.14107A 0_0402_5%

+3.3V_PGPPBCH : @RH304 0.27262A 0_0402_5%

+3.3V_PGPPG : @RH305 0.1318A 0_0402_5%

+1.8V_RUN → +1.8V_RUN_EDRAM : @RH252 0_0603_5%

+VCC_EDRAM_FUSEPRG : @RH253 0_0603_5%

+3.3V_ALW_PCHRES → +3.3V_1.8V_SPI : @RH246 0_0603_5%

+1.8V_ALW_PCHRES → +1.8V_ALW : @RH250 0_0603_5%

@RH247 0_0603_5%

7/5 update

+1.0V_AAZPLL → EMC@LH2 → BLM15GA750SN1D_2P → +1.0V_AAZPLL_R

+3.3V_1.8V_AZIO → EMC@LH1 → BLM15GA750SN1D_2P → +3.3V_1.8V_AZIO_R

CH12 0.1U_0201_10V6K

CH11 0.1U_0201_10V6K

7/5 update

UH1H SPT-H_PCH SKL-H-PCH_BGA837 REV = 1.3 8 OF 12

+1.0V_PRIM: AA23 AA26 AA28 AC23 AC26 AC28 AE23 AE26 Y23 Y25 BA29 DCPDSW_1P0

+1.0V_DSW: N17 R19 U20 V17 R17 VCCCLK1 VCCCLK3 VCCCLK4 VCCCLK2 VCCCLK2

+1.0V_CLK5 / +1.0V_CLK2 / +1.0V_CLK4 / +1.0V_CLK3 / +1.0V_CLK1 (NO CAP): K2 K3 VCCCLK5 VCCCLK5

+1.0V_MPHY: U21 U23 U25 U26 V26 A43 VCCMPHY_1P0 ×6

+1.0V_AMPHYPLL: B43 C44 C45 VCCMPHYPLL_1P0 VCCMPHYPLL_1P0 VCCPCIE3PLL_1P0 VCCPCIE3PLL_1P0

+1.0V_APLLEBB: V28 VCCAPLLEBB_1P0

+1.0V_DUSB: AC17 VCCPRIM_1P0

+1.0V_AUSB: AJ5 AL5 AN19 VCCUSB2PLL_1P0 VCCUSB2PLL_1P0 VCCHDAPLL_1P0

BA15 VCCHDA

+3.3V_PUSBDSW: W15 VCCDSW_3P3

VCCPRIM_1P0 ×8 VCCDSW_3P3 VCCPGPPA VCCPGPPBCH VCCPGPPBCH VCCPGPPEF VCCPGPPEF VCCPGPPG VCCPRIM_3P3 VCCPRIM_1P0 VCCATS VCCRTCPRIM_3P3 VCCRTC DCPRTC VCCPRIM_1P0 ×4 VCCSPI ×3 VCCPGPPD ×4 VCCPRIM_3P3 ×3

+2.8V_FHV: AL22

+3.3V_DSW: BA24

+3.3V_1.8V_GPPA: BA31

+3.3V_PGPPBCH: BC42 BD40

+3.3V_PGPPEF: AJ41 AL41 AD41

+3.3V_PGPPG: AN5

+3.3V_PHVC

+1.0V_DTS: AD15

+3.3V_RUN_ATS: AD13

+3.3V_PRTCPRIM: BA20

+3.3V_PRTC: BA22 BA26

+DCPRTC

+1.0V_PRIM: AJ20 AJ21 AJ23 AJ25

0.1U_0402_25V6 CH68

+3.3V_1.8V_SPI: BE41 BE43 BE42

+3.3V_1.8V_GPPD: BC44 BA45 BC45 BB45

+3.3V_1.8V_FUSE: BD3 BE3 BE4

UH1J SPT-H_PCH SKL-H-PCH_BGA837 REV = 1.3 10 OF 12

VSS: BD2 BD45 BD44 BE44 D45 A42 B45 B44 A4 A3 B2 A2 B1 BB1 BC1 A44 ×

RSVD: C1 D1

RSVD: AR22 W13 U13 P31 N31 P27 R27 N29 P29 AN29 R24 P24 AT3

PAD-D @ T66 PAD-D @ T67 PAD-D @ T68

9/7 Remove T69, T70, T71, T72, T74, T75 把top shape 補足+1.0V_MPHY

PAD-D @ T76

9/7 Remove T69, T70, T71, T72, T74, T75 把top shape 補足+1.0V_MPHY

PREQ# AT4 → PCH_XDP_PREQ# <7>

PRDY# AY5 → PCH_XDP_PRDY# <7>

CPU_TRST# AL2 → CPU_XDP_TRST# <7>

PCH_TRIGOUT AK1 → PCH_2_CPU_TRIGGER_R

PCH_TRIGIN ← CPU_2_PCH_TRIGGER <10>

PCH_2_CPU_TRIGGER_R — RH42 30_0402_5% — PCH_2_CPU_TRIGGER → PCH_2_CPU_TRIGGER <10>

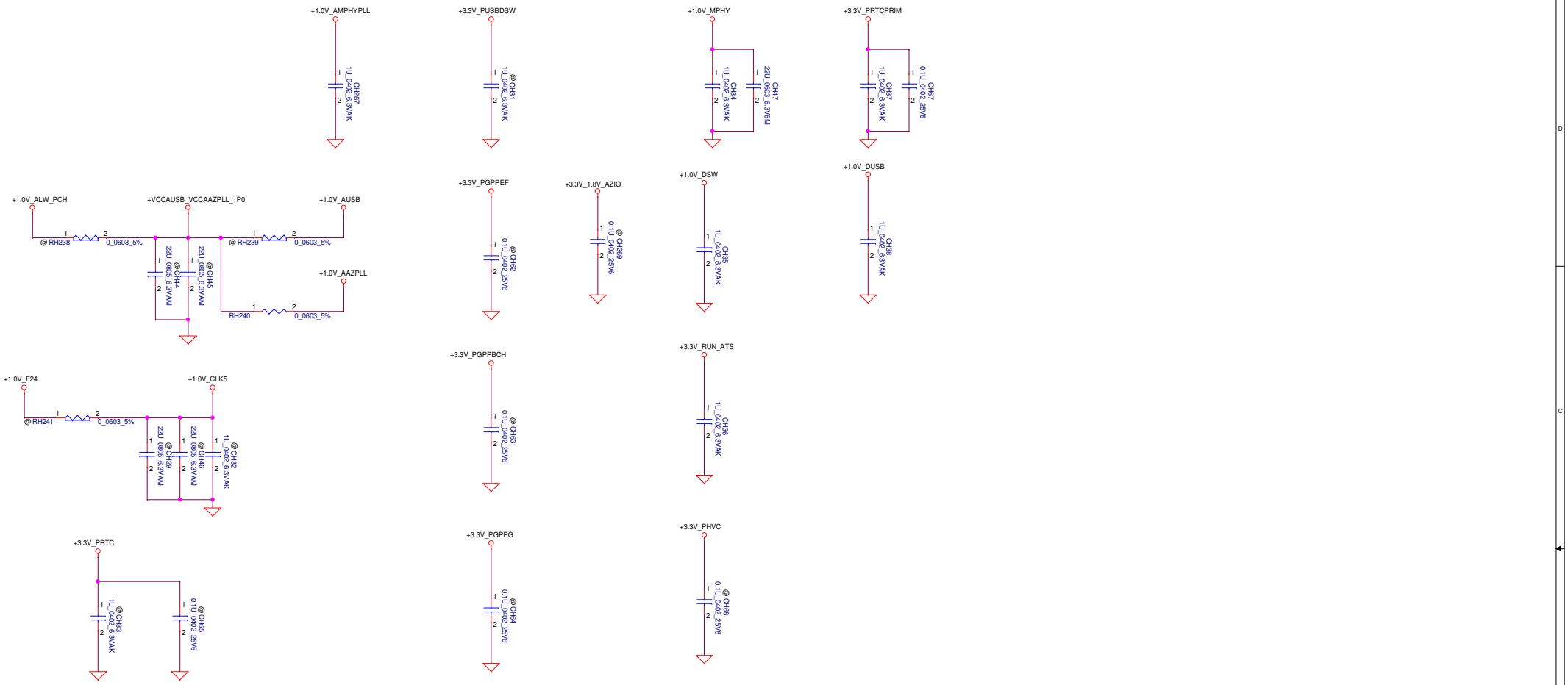
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SKYLAKE PCH-H (7/9)

Size | Document Number: LA-E321P | Rev: 1.0

Date: Thursday, December 08, 2016 | Sheet 25 of 72

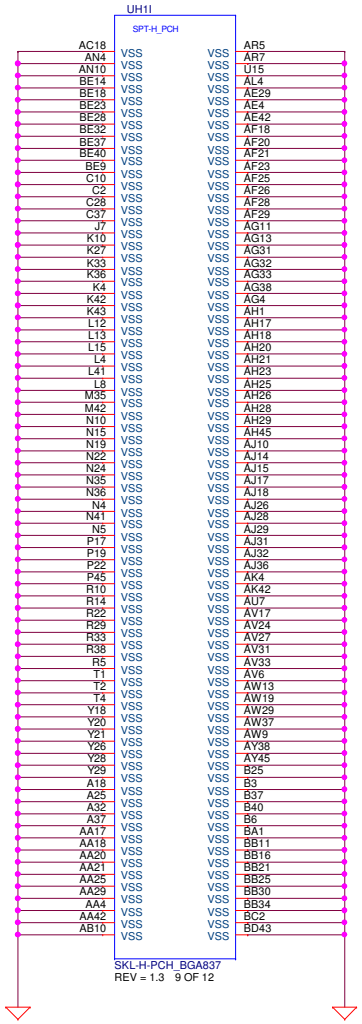


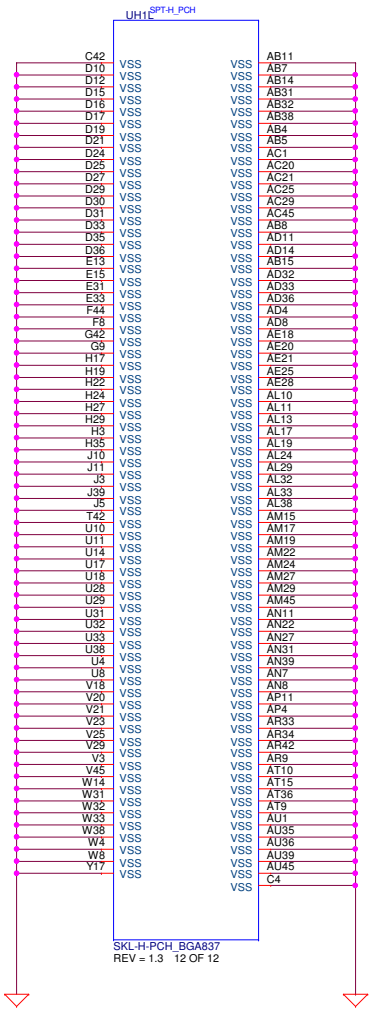
Compal Electronics, Inc.

Title: SKYLAKE PCH-H (8/9)

Size | Document Number: LA-E321P | Rev: 1.0

Date: Wednesday, November 30, 2016 | Sheet 26 of 72

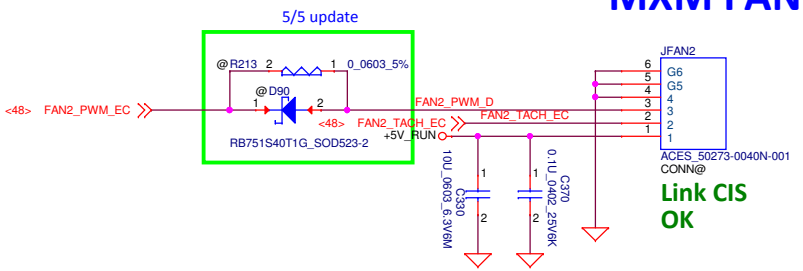




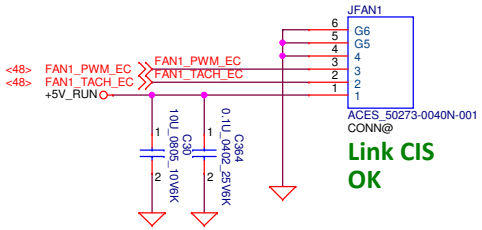
DELL CONFIDENTIAL/PROPRIETARY

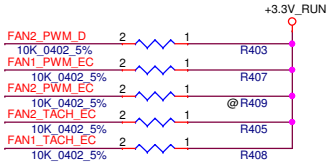
Compal Electronics, Inc.	
Title	SKYLAKE PCH-H (9/9)
Size	Document Number: LA-E321P
Rev	1.0
Date: Wednesday, November 30, 2016	Sheet 27 of 72

MXM FAN



CPU FAN



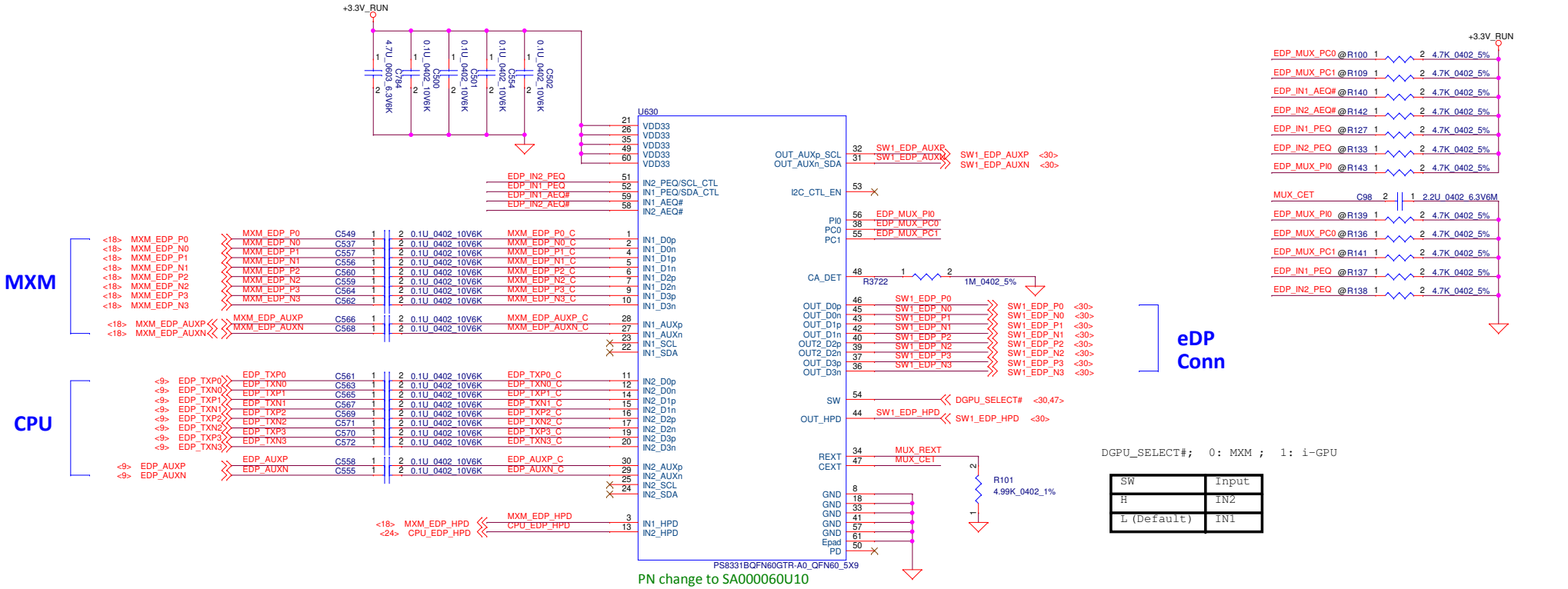


Compal Electronics, Inc.

Title: FAN control

Size | Document Number: LA-E321P | Rev: 1.0

Date: Wednesday, November 30, 2016 | Sheet 28 of 72



INy_PEQ = Programmable input equalization levels
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

INy_AEQ# = Automatic EQ disable
L: Automatic EQ enable (default)
H: Automatic EQ disable

PI0 = Auto test enable
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1 = Output swing adjustment
L: default
H: +20%
M: -16.7%

Compal Electronics, Inc.

Title: eDP MUX (PS8331)

Size | Document Number: LA-E321P | Rev: 1.0

Date: Wednesday, November 30, 2016 | Sheet 29 of 72

5/5 update

Close to JEDP1

@EMC@ D22 DMIC_CLK DMIC0 PESD5V0U2BT_SOT23-3

CONN@ ACES_50398-04041-001 JEDP1

+BL_PWR_SRC +LCDVDD +CAMERA_VDD +3.3V_RUN DMIC_CLK DMIC0 USB20_N11_R USB20_P11_R R208 @EMC@2 0_0603_5% BIA_PWM DISP_ON LCD_CBL_DET# LCD_TST SW1_EDP_HPD

CAM_MIC_CBL_DET# <19>

DMIC_CLK EMC@C1467 100P_0402_50V8J DMIC0 EMC@C1468 100P_0402_50V8J

SW1_EDP_AUXP_C SW1_EDP_AUXN_C 0.1U_0402_10V6K C371 C373 SW1_EDP_AUXP SW1_EDP_AUXN

SW1_EDP_N3_C SW1_EDP_P3_C SW1_EDP_N2_C SW1_EDP_P2_C SW1_EDP_N1_C SW1_EDP_P1_C SW1_EDP_N0_C SW1_EDP_P0_C 0.1U_0402_10V6K C374 C372 C376 C375 C378 C377 C380 C379 SW1_EDP_N3 SW1_EDP_P3 SW1_EDP_N2 SW1_EDP_P2 SW1_EDP_N1 SW1_EDP_P1 SW1_EDP_N0 SW1_EDP_P0

CIS link OK

DISP_ON R1139 100K_0402_5% D65 D64 D69 RB751VM-40TE-17_SOD323-2 PANEL_BKEN_PCH <19> MXM_PANEL_BKEN <18> PANEL_BKEN_EC <47>

60mil

+PWR_SRC Q21 DMP3050LVT-7_TSOT26-6 +BL_PWR_SRC 60mil C287 1U_1206_50V7 R422 100K_0402_5% C396 0.1U_0603_50V7K BL_PWR_SRC_ON Q22 DMN65D8LW-7_SOT323-3 C393 0.01U_0402_50V7K R423 47K_0402_5% <48> EN_INVPWR

Panel backlight power control by EC

RF require +BL_PWR_SRC EMC@C1475 22P_0402_50V8J EMC@C1476 100P_0402_50V8J

TOUCH_SCREEN_PD# TOUCH_SCREEN_DET# @R426 100K_0402_5% R382 10K_0402_5% +3.3V_RUN

Touch Screen

+BL_PWR_SRC +LCDVDD C248 0.1U_0603_50V7K C249 0.1U_0402_25V6K

Close to JEDP1

SW1_EDP_AUXN 100K_0402_5% R339 SW1_EDP_HPD 100K_0402_5% R222 SW1_EDP_AUXP 100K_0402_5% R336 +3.3V_RUN

SW1_EDP_HPD 4.7K_0402_5% R103 +LCDVDD

D66 RB751VM-40TE-17_SOD323-2 BIA_PWM_PCH <19>

<29,47> DGPU_SELECT# +3.3V_RUN C248 0.1U_0402_10V7K

BIA_PWM D68 RB751VM-40TE-17_SOD323-2 U3 TC7SH125FU_SSOP5 MXM_BIA_PWM <18> R137 10K_0402_5%

D71 RB751VM-40TE-17_SOD323-2 BIA_PWM_EC <48>

JTS1 USB20_N9_R USB20_P9_R TOUCH_SCREEN_PD# TOUCH_SCREEN_DET# +5V_RUN 140mA C310 0.1U_0402_25V6 GND GND ACES_50228-0067N-001

back to TS only

Close to JTS1

EMC@ D20 USB20_N9_R USB20_P9_R L30ESDL5V0C3-2_SOT23-3

Webcam PWR CTRL

+3.3V_RUN Q24 LP2301ALT1G_SOT23-3 +CAMERA_VDD C301 0.1U_0402_25V6K 3.3V_CAM_EN# <20> C300 10U_0603_6.3V6M C299 0.1U_0402_25V6K

<20> USB20_N9 <20> USB20_P9 MCM1012B900F06BP_4P EMC@LT1 USB20_N9_R USB20_P9_R

EMC request change main source to SM070003Z00

<20> USB20_N11 <20> USB20_P11 EMC@L10 MCM1012B900F06BP_4P USB20_N11_R USB20_P11_R @EMC@ D21 PESD5V0U2BT_SOT23-3

Close to JEDP1

LCD Power

RF require +LCDVDD EMC@C1478 100P_0402_50V8J EMC@C1477 22P_0402_50V8J

+LCDVDD C396 10U_0603_6.3V6M U33 VOUT VIN GND EN /OC +3.3V_ALW @R42 100K_0402_5% G524B1T11U_SOT23-5

D92 RB751VM-40TE-17_SOD323-2 <19,48> ENVDD_PCH <47> LCD_VCC_TEST_EN <18> MXM_ENVDD D93 BAT54CW_SOT323-3 R727 100K_0402_5%

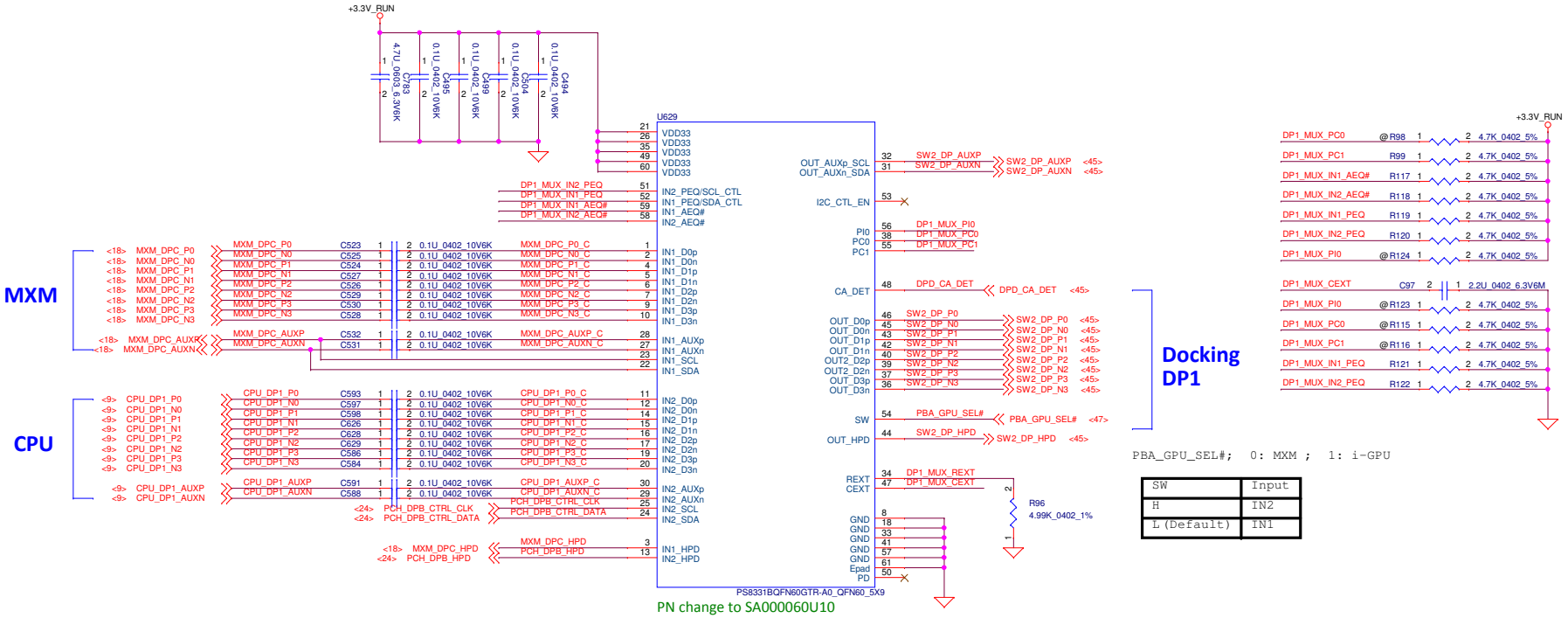
DELL CONFIDENTIAL/PROPRIETARY

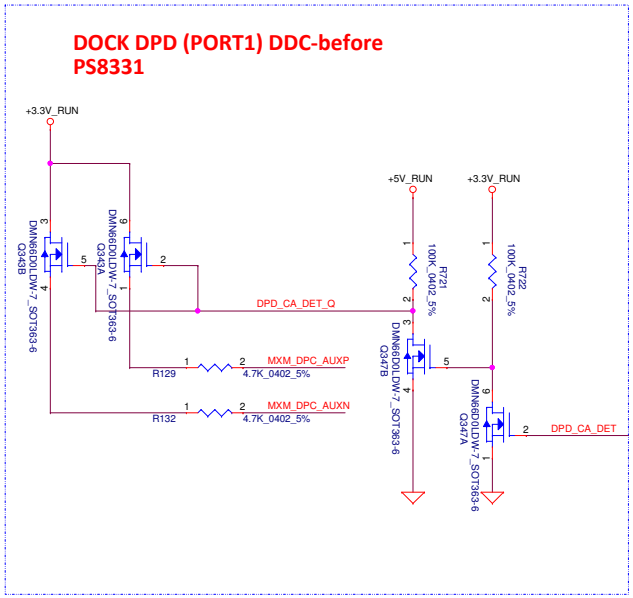
Compal Electronics, Inc.

Title: eDP / CAM / TS

Size: Document Number: LA-E321P Rev: 1.0

Date: Thursday, December 08, 2016 Sheet 30 of 72





INy_PEQ = Programmable input equalization levels
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

INy_AEQ# = Automatic EQ disable
L: Automatic EQ enable (default)
H: Automatic EQ disable

PI0 = Auto test enable
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

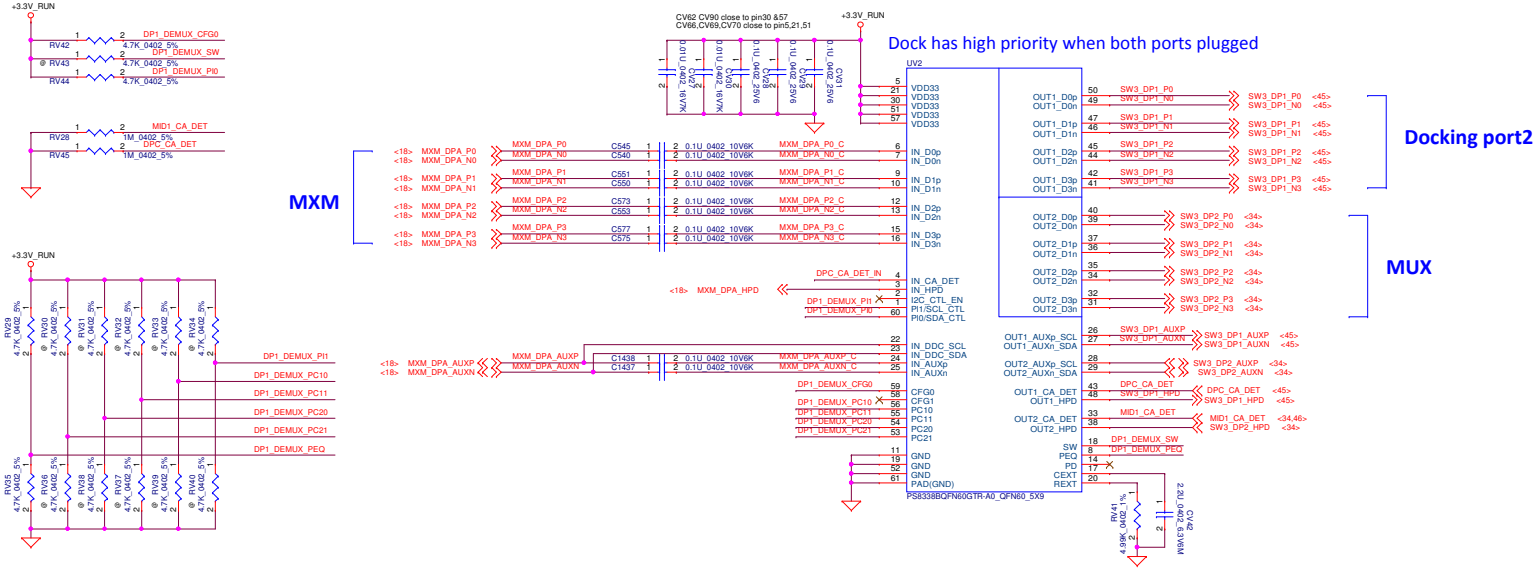
PC1 = Output swing adjustment
L: default
H: +20%
M: -16.7%

Compal Electronics, Inc.

Title: MXM/CPU MUX(PS8331)

Size | Document Number: LA-E321P | Rev: 1.0

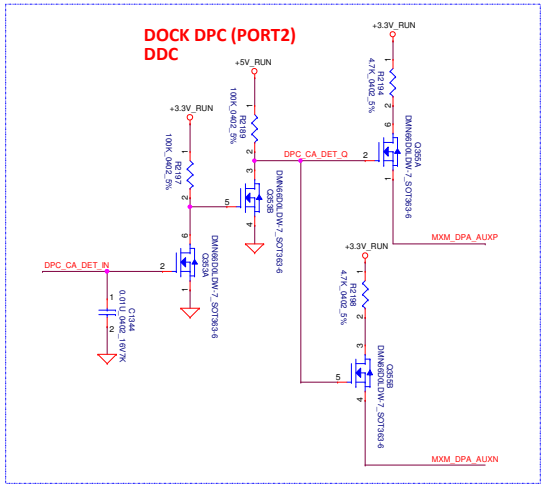
Date: Wednesday, November 30, 2016 | Sheet 31 of 72



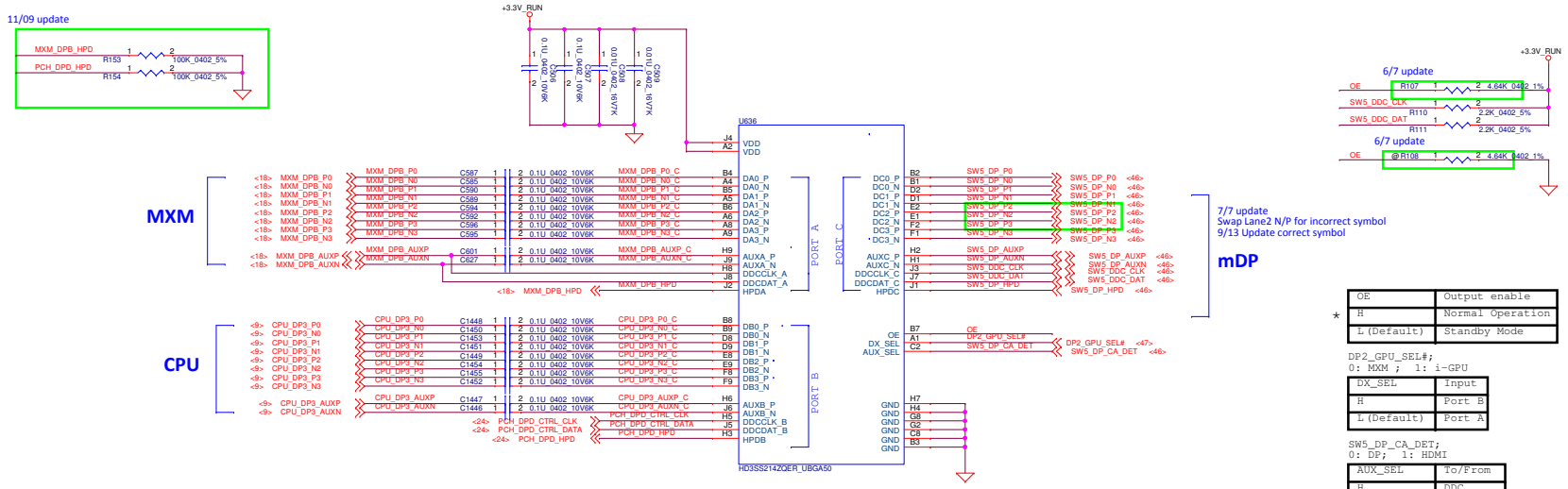
Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected (default)
SW = H: Port2 is selected

For Automatic Switching Mode (CFG0 = H): (By OUT1_HPD and OUT2_HPD)
SW = L: Port1 has higher priority when both ports are plugged (default)
SW = H: Port2 has higher priority when both ports are plugged

	H	L
CFG0	V	
SW		V



Compal Electronics, Inc.		
Title	DP DeMUX (PS8338)	
Size	Document Number: LA-E321P	Rev: 1.0
Date: Wednesday, November 30, 2016	Sheet 32 of 72	



*

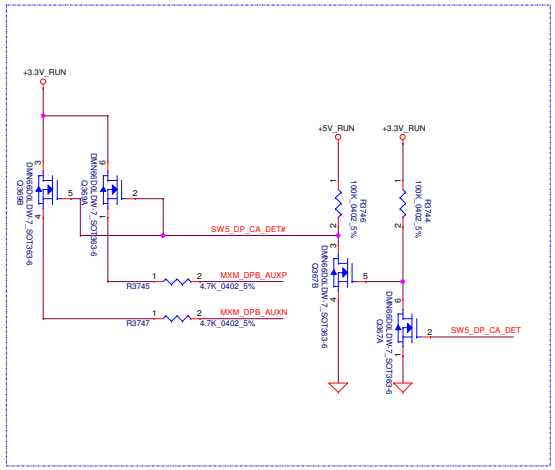
OE	Output enable
H	Normal Operation
L (Default)	Standby Mode

DP2_GPU_SEL#;
0: MXM ; 1: i-GPU

DX_SEL	Input
H	Port B
L (Default)	Port A

SW5_DP_CA_DET;
0: DP; 1: HDMI

AUX_SEL	To/From
H	DDC
L (Default)	AUX

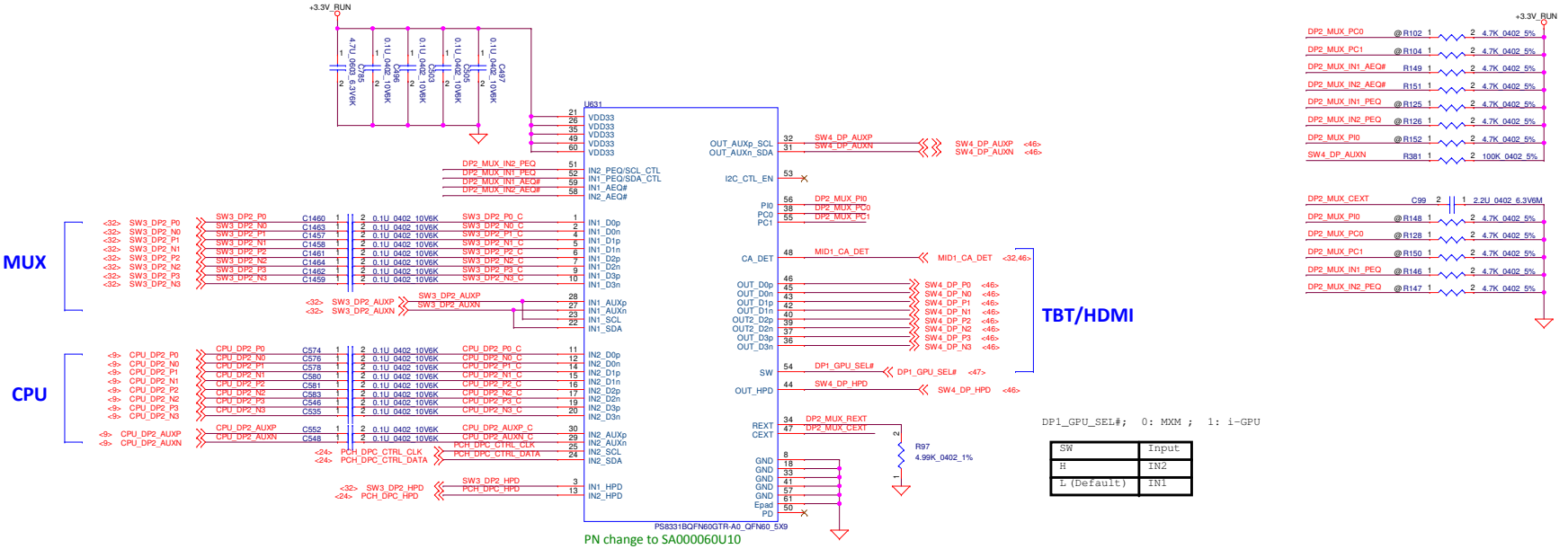


Compal Electronics, Inc.

Title: P33-mDP MB DP1.3 MUX (HD3SS214)

Size: | Document Number: LA-E321P | Rev: 1.0

Date: Wednesday, November 30, 2016 | Sheet 33 of 72



PN change to SA000060U10

DP1_GPU_SEL#; 0: MXM ; 1: i-GPU

SW	Input
H	IN2
L (Default)	IN1

INy_PEQ = Programmable input equalization levels
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

INy_AEQ# = Automatic EQ disable
L: Automatic EQ enable (default)
H: Automatic EQ disable

PI0 = Auto test enable
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1 = Output swing adjustment
L: default
H: +20%
M: -16.7%

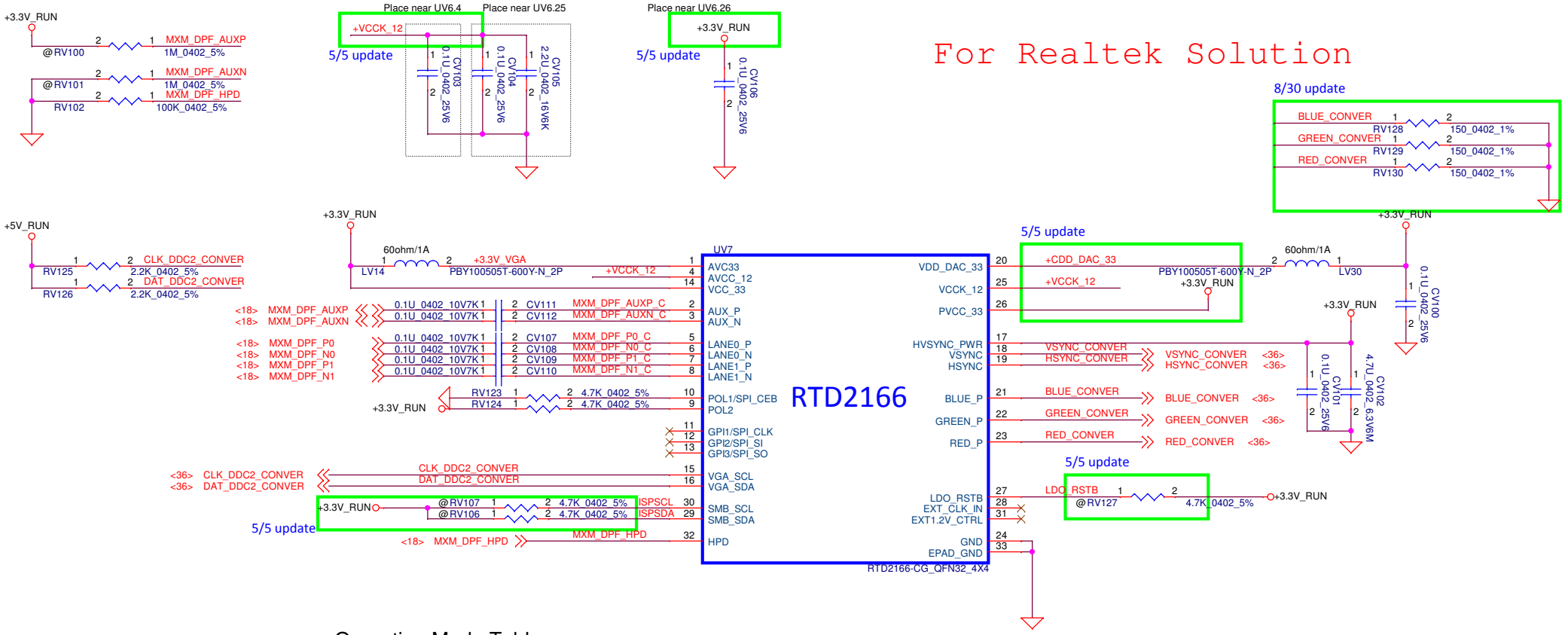
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: VGA CONN

Size: | Document Number: LA-E321P | Rev: 1.0

Date: Wednesday, November 30, 2016 | Sheet 34 of 72



Operation Mode Table

		POL1(P10)	
		0	1
POL2 (P9)	0	X	X
	1	ROM	Flash

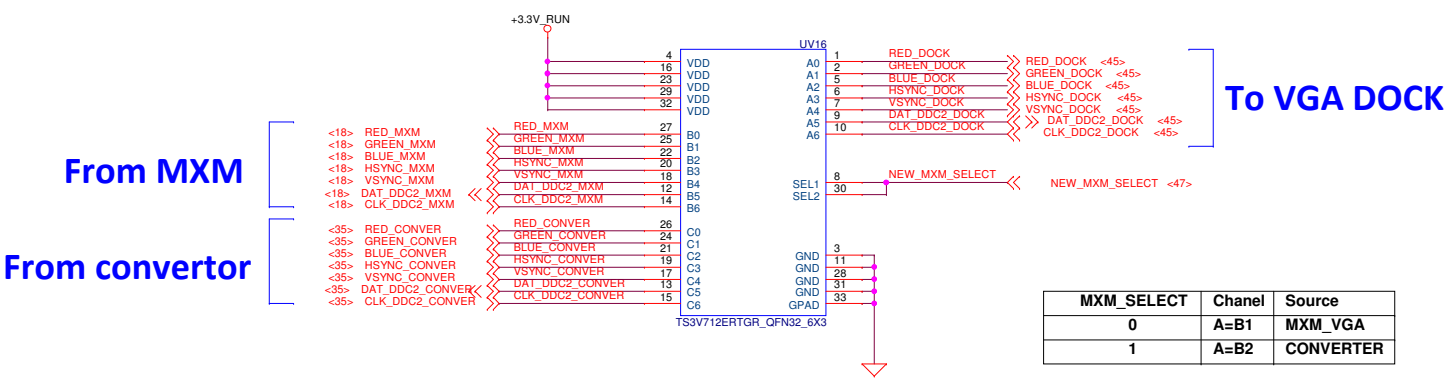
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

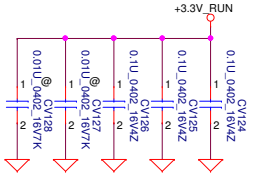
Compal Electronics, Inc.

Title: **DP to VGA**

Size: B | Document Number: **LA-E321P** | Rev: 1.0

Date: Wednesday, November 30, 2016 | Sheet 35 of 72





MXM_SELECT	Chanel	Source
0	A=B1	MXM_VGA
1	A=B2	CONVERTER

DELL CONFIDENTIAL/PROPRIETARY

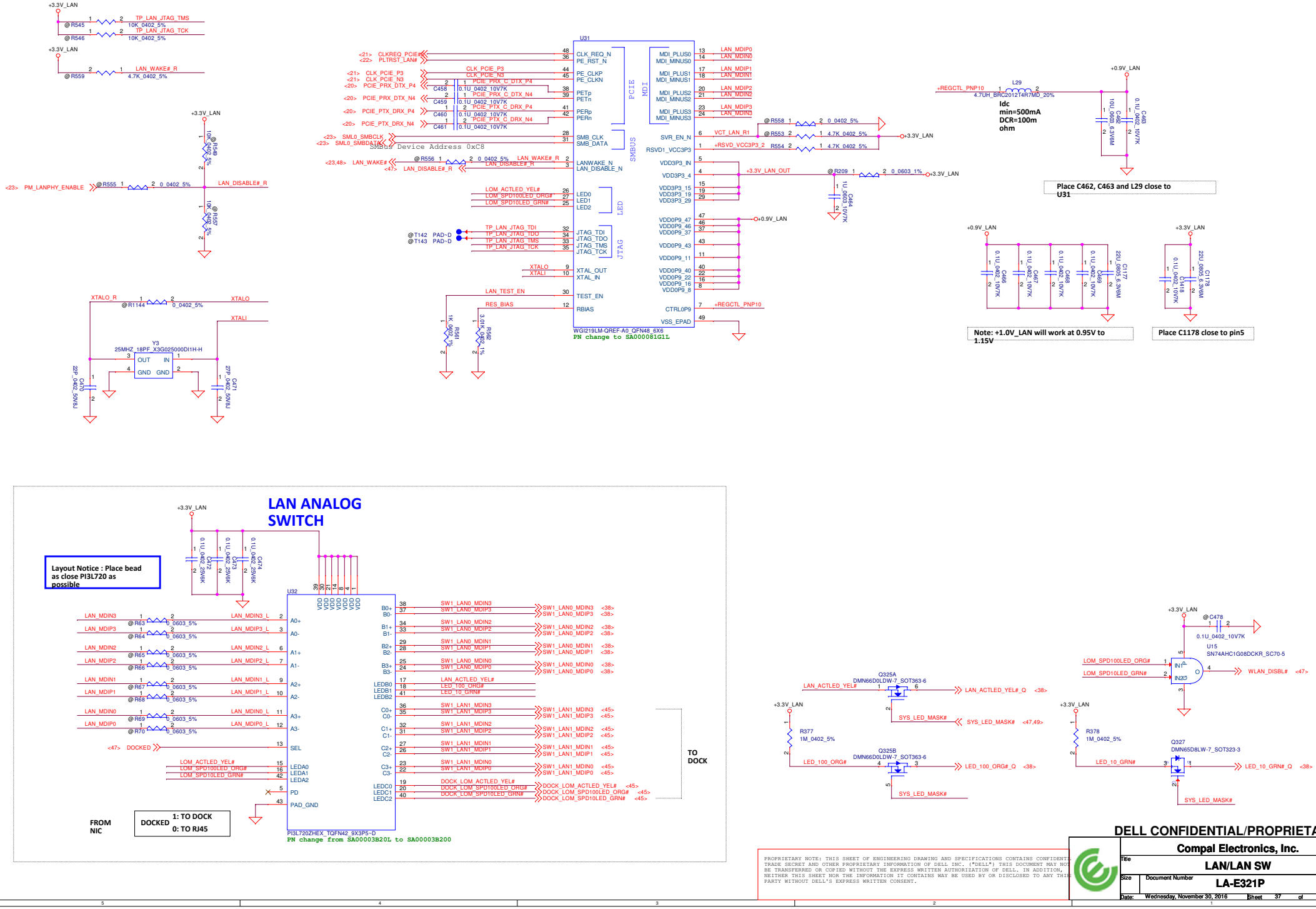
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: VGA SW

Size: Custom | Document Number: LA-E321P | Rev: 1.0

Date: Wednesday, November 30, 2016 | Sheet 36 of 72



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

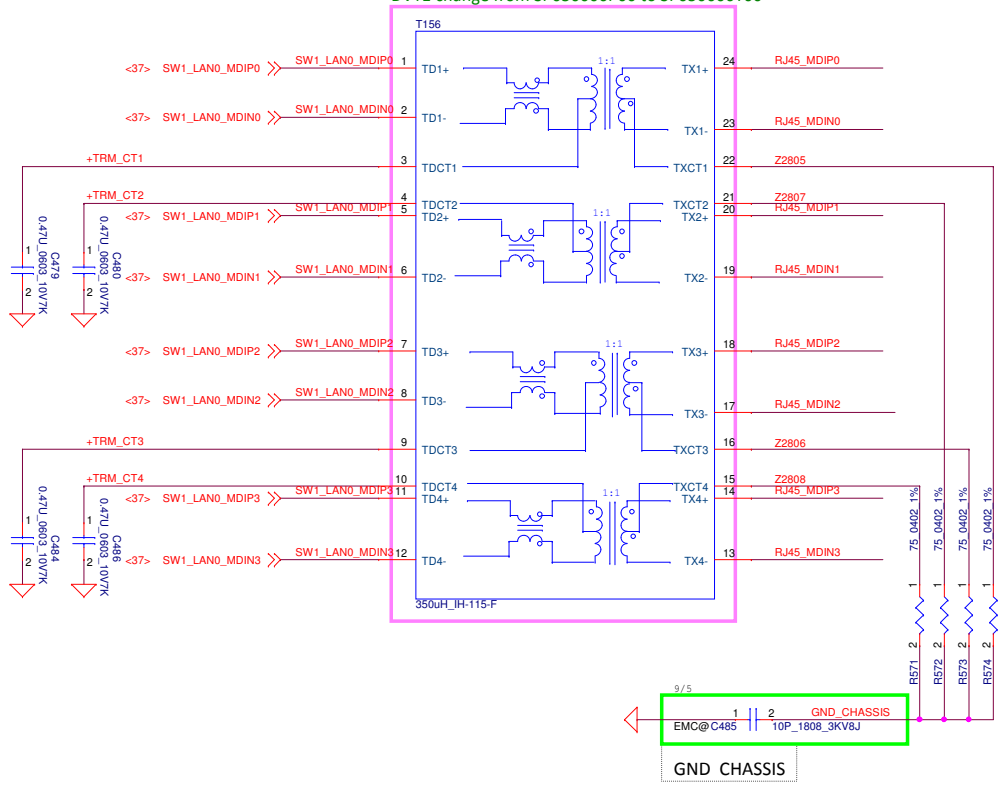
Title: LAN/LAN SW

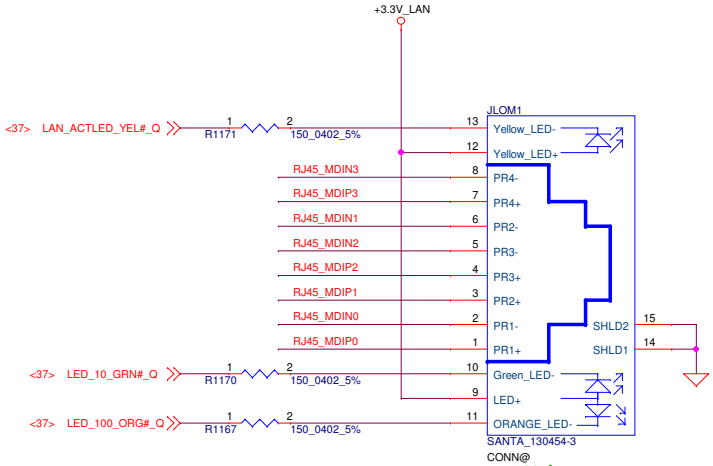
Size: | Document Number: LA-E321P | Rev: 1.0

Date: Wednesday, November 30, 2016 | Sheet 37 of 72

+3.3V_LAN/+3.3V_LAN_LOM:20mils

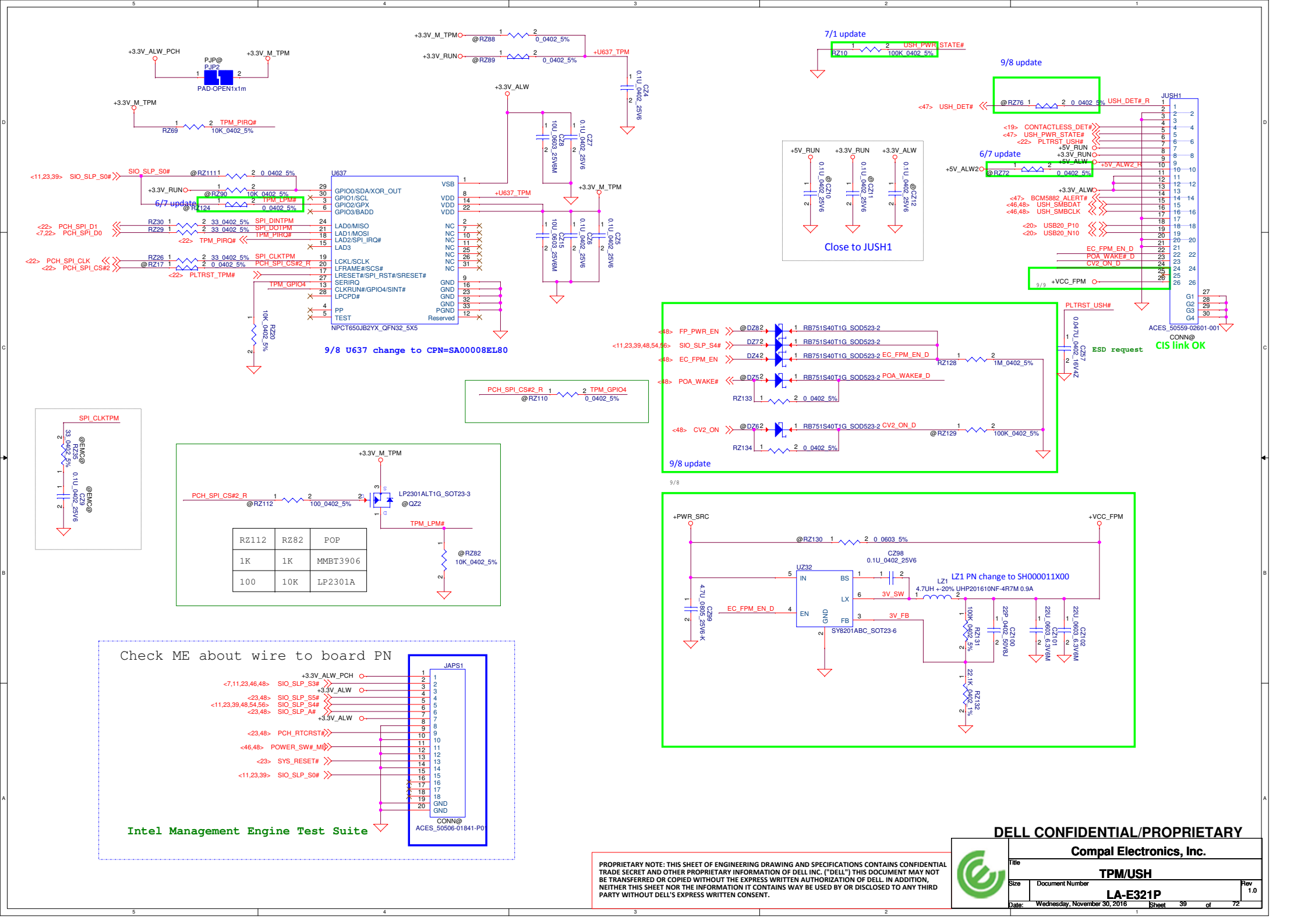
DVT1 change from SP050006P00 to SP050006Y00





DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	RJ45
Size / Document Number	LA-E321P
Rev	1.0
Date: Thursday, December 08, 2016	Sheet 38 of 72



Compal Electronics, Inc.

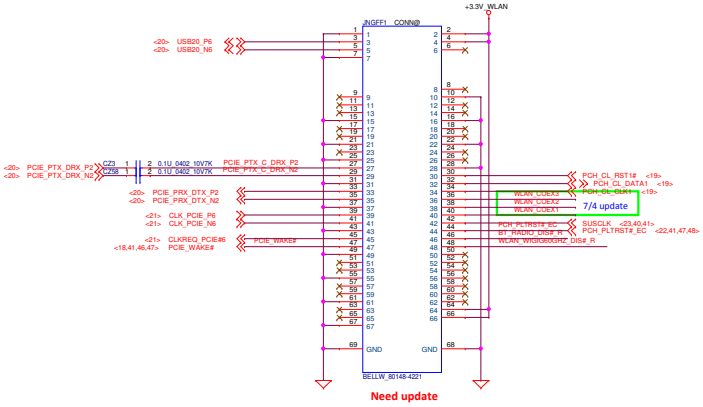
Title: TPM/USH

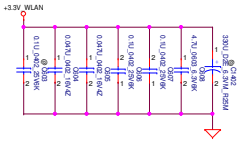
Size | Document Number: LA-E321P | Rev: 1.0

Date: Wednesday, November 30, 2016 | Sheet 39 of 72

WLAN/BT

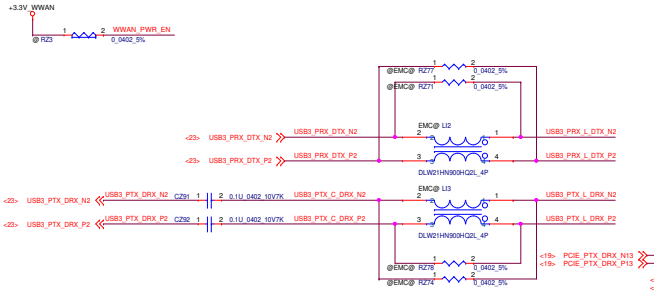
NGFF slot_1 Key A

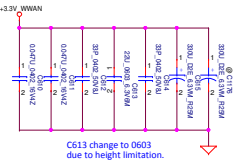




WWAN/LTE/HCA/Cache

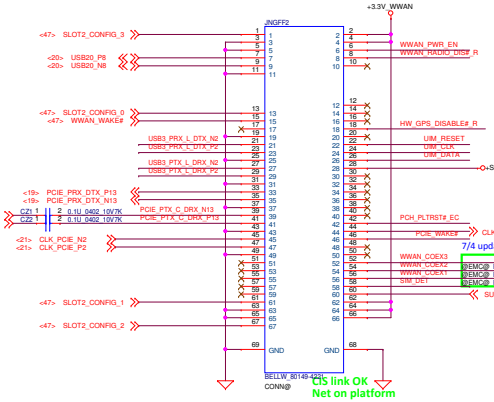
NGFF slot_2 Key B



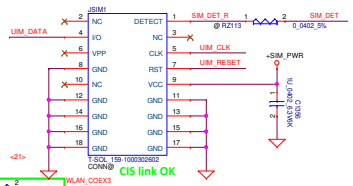


C613 change to 0603 due to height limitation.

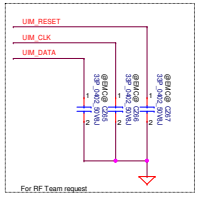
C615 footprint change to C_APXK2R5ARA331MF451



SIM Card Push-Push



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	0	0	0	0	SSD-SATA
8	1	0	0	0	WWAN
14	1	0	1	1	HCA-PCIE
15	1	1	1	1	Cache



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Compal Electronics, Inc.			
Title: M.2 Card-1/2			
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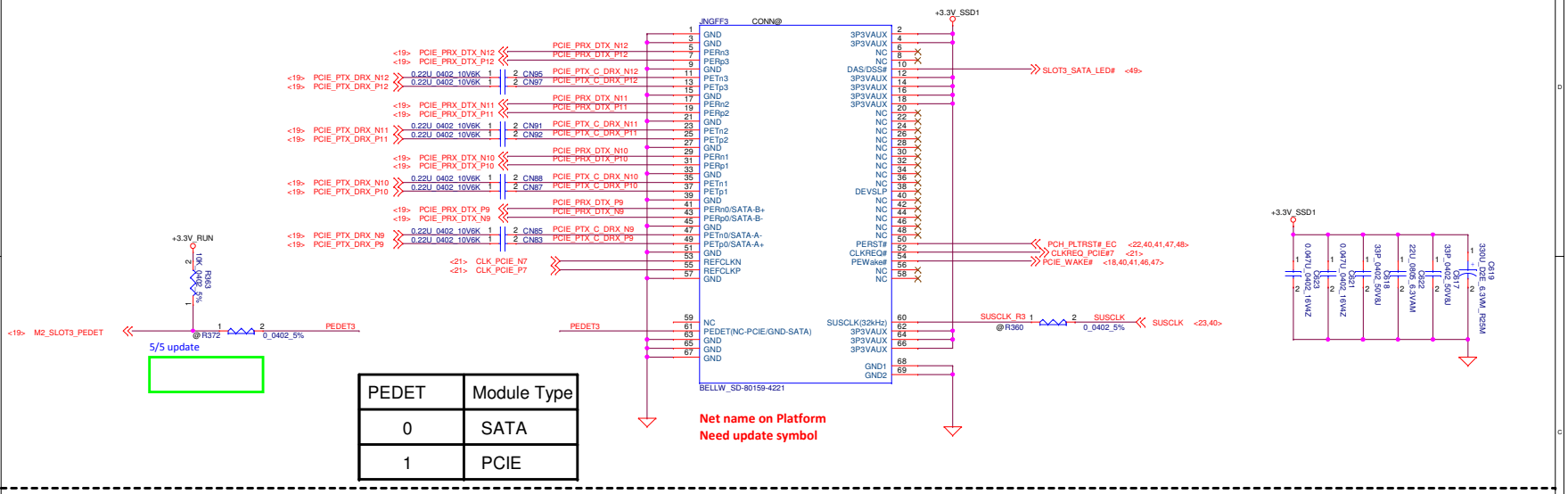
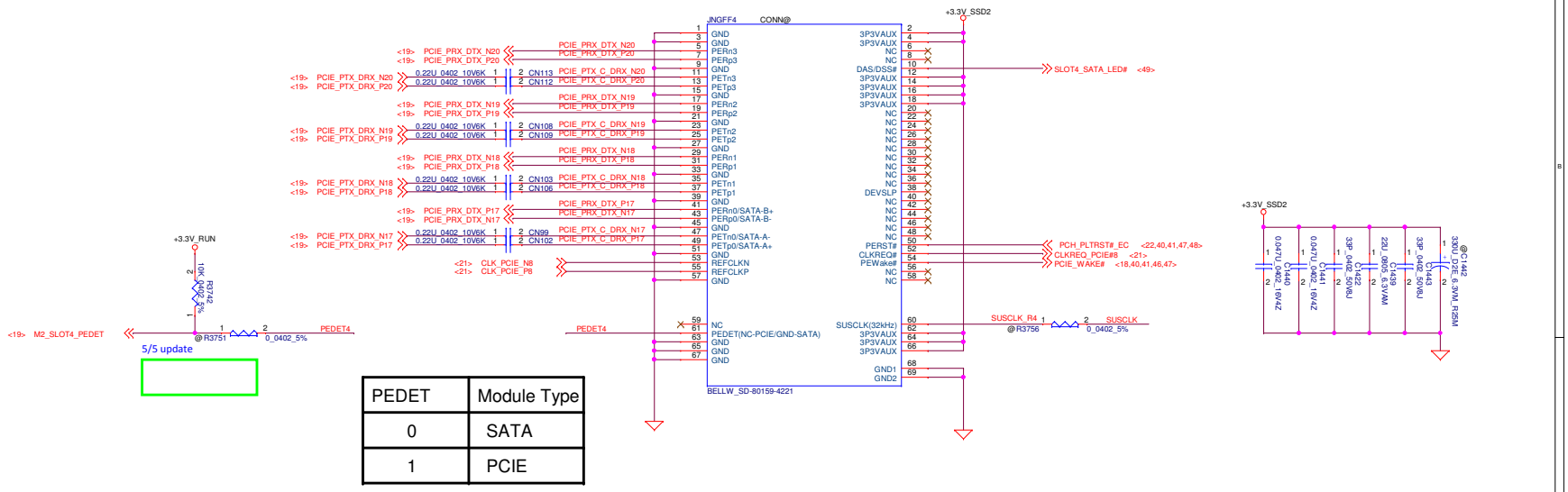
SSD
NGFF slot_3 Key M



PEDET	Module Type
0	SATA
1	PCIE

SSD
NGFF slot_4 Key M



PEDET	Module Type
0	SATA
1	PCIE

Compal Electronics, Inc.

Title: M.2 Card-2/2

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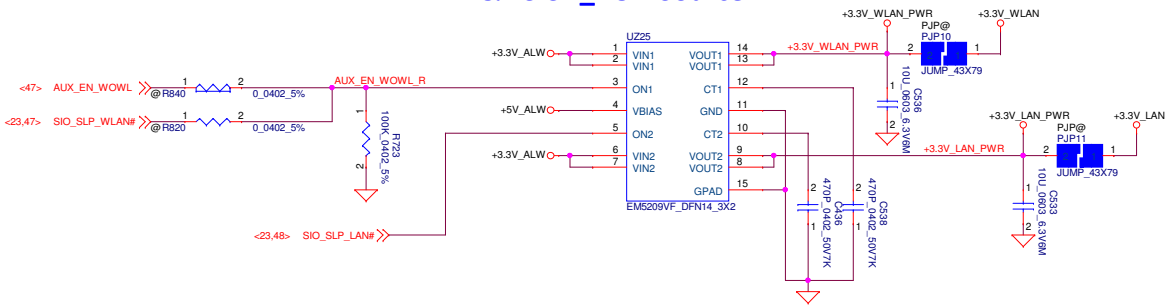
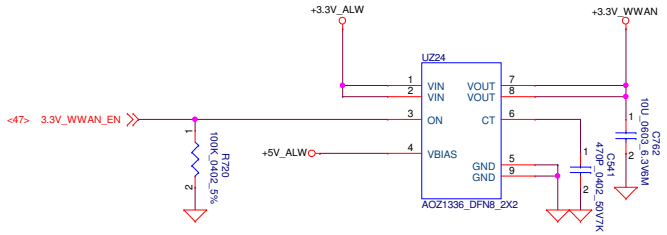
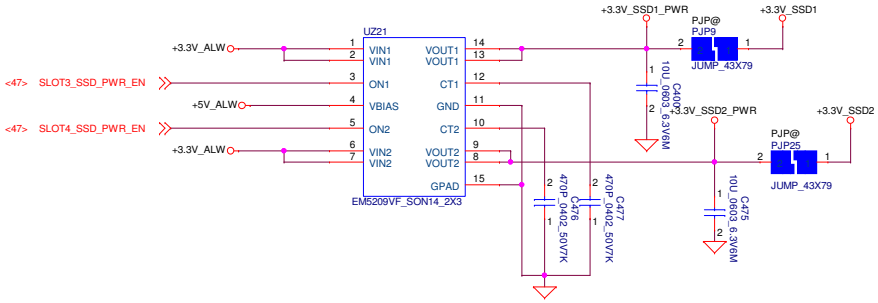
Power Control for M.2 slot 1.
& +3.3V_RUN Source



Power Control for M.2 slot 2.



Power Control for M.2 slot 3. Source
Power Control for M.2 slot 4. Source



Compal Electronics, Inc.

Title: M.2 Card PWR

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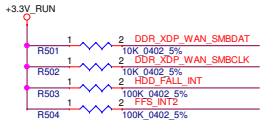
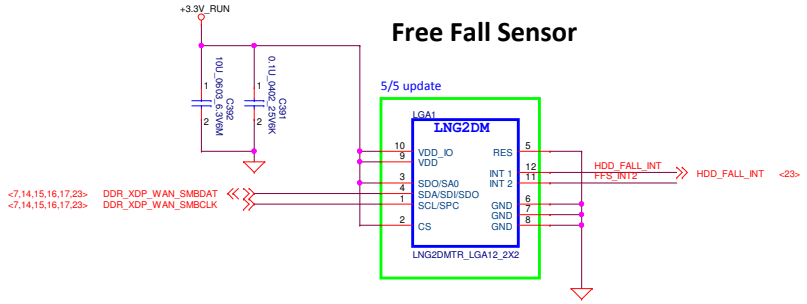
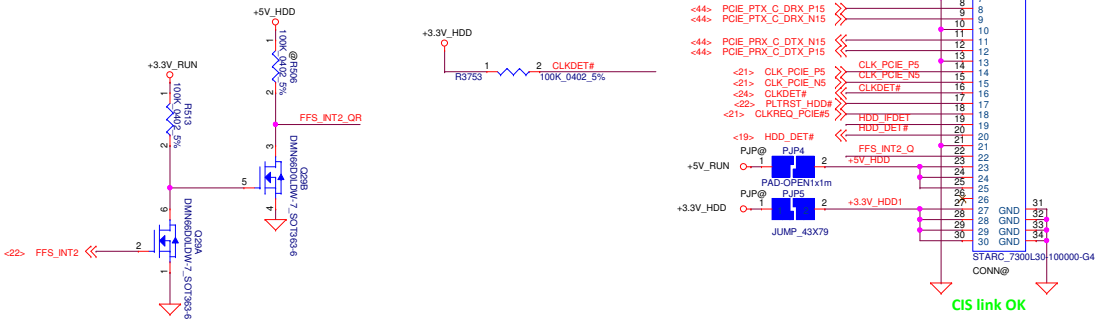
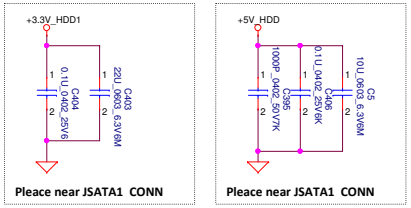




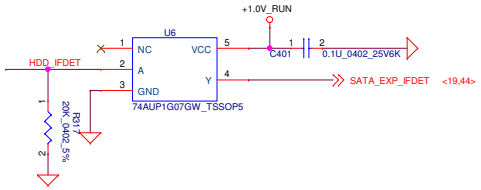


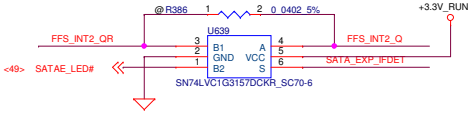


HDD_IFDET	DEVICE interface
0	SATA
1	PCIE

SATA_EXP_IFDET	DEVICE interface
0	SATA
1	PCIE

SATA_EXP_IFDET	channel on
0	A-->B1
1	A-->B2





Compal Electronics, Inc.

Title: HDD CONN

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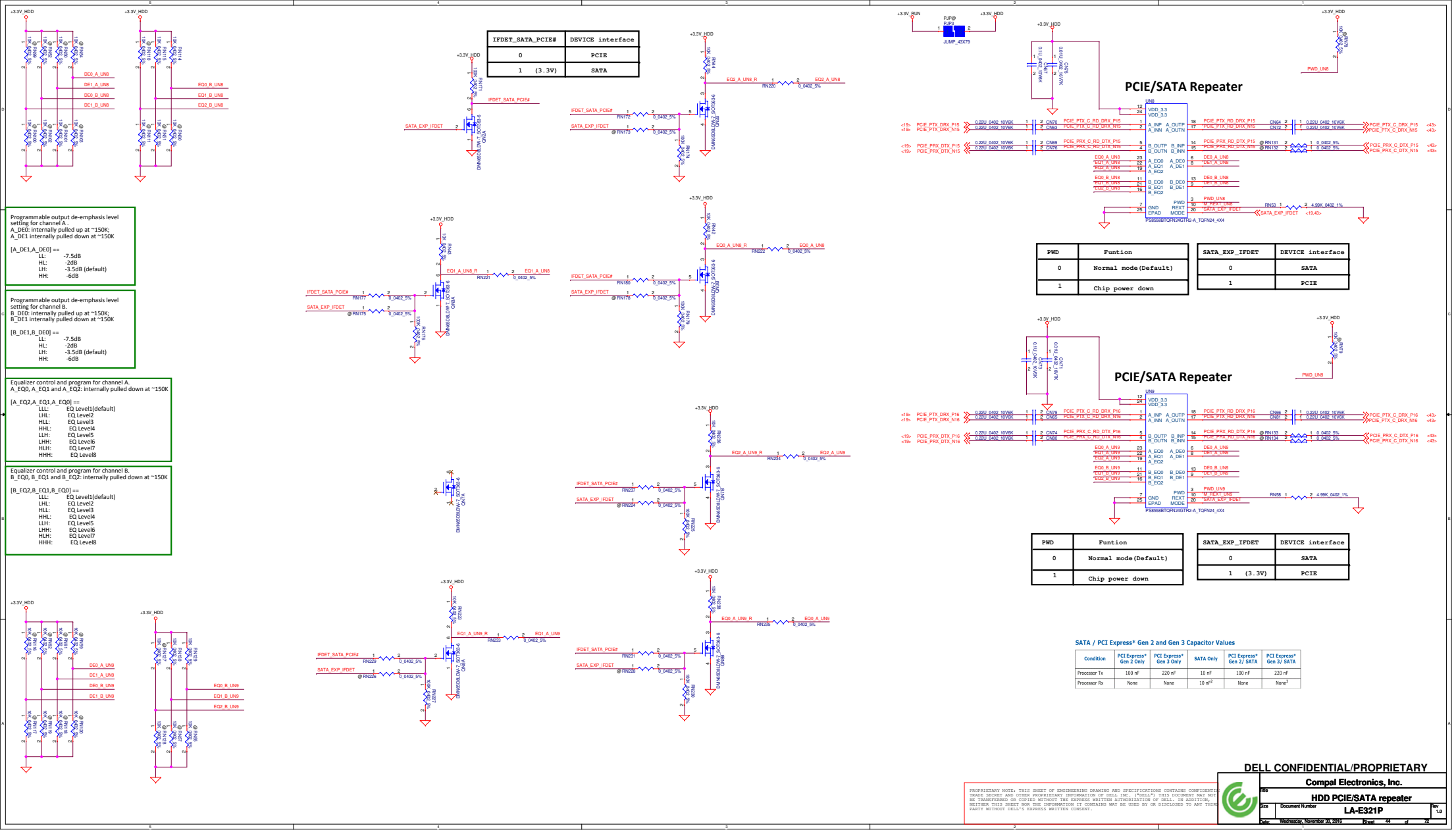

IFDET_SATA_PCIE#	DEVICE interface
0	PCIE
1 (3.3V)	SATA

PWD	Funtion
0	Normal mode(Default)
1	Chip power down

SATA_EXP_IFDET	DEVICE interface
0	SATA
1	PCIE

PWD	Funtion
0	Normal mode(Default)
1	Chip power down

SATA_EXP_IFDET	DEVICE interface
0	SATA
1 (3.3V)	PCIE

SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[2]

Compal Electronics, Inc.
HDD PCIE/SATA repeater
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EMI request add 33ohm for DOCK DVI signals.

Dock DPD (Port 1)

Dock DPC (Port 2)

DPD_CA_DET — R492 1M_0402_5%

JDOCK1

Close to DOCK
Its for Enhance ESD on dock issue.

Close to DOCK
Its for Enhance ESD on dock issue.

System hangs after hot dock.

PN change to SP0300019A0

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Compal Electronics, Inc.

Title	Docking		
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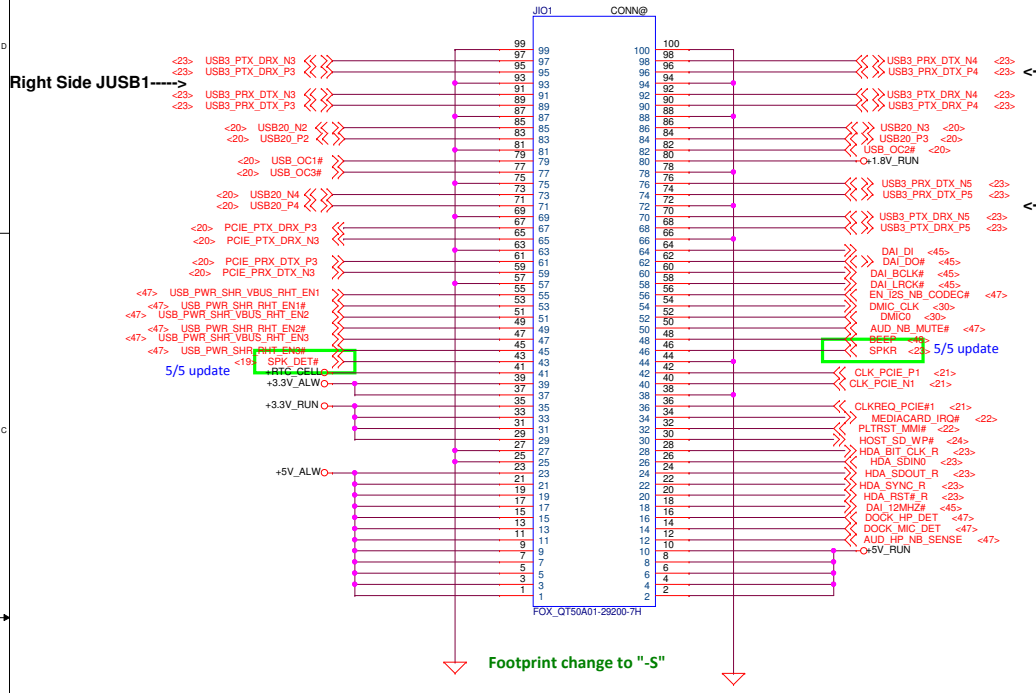
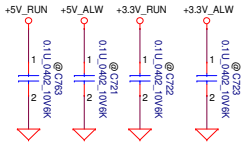
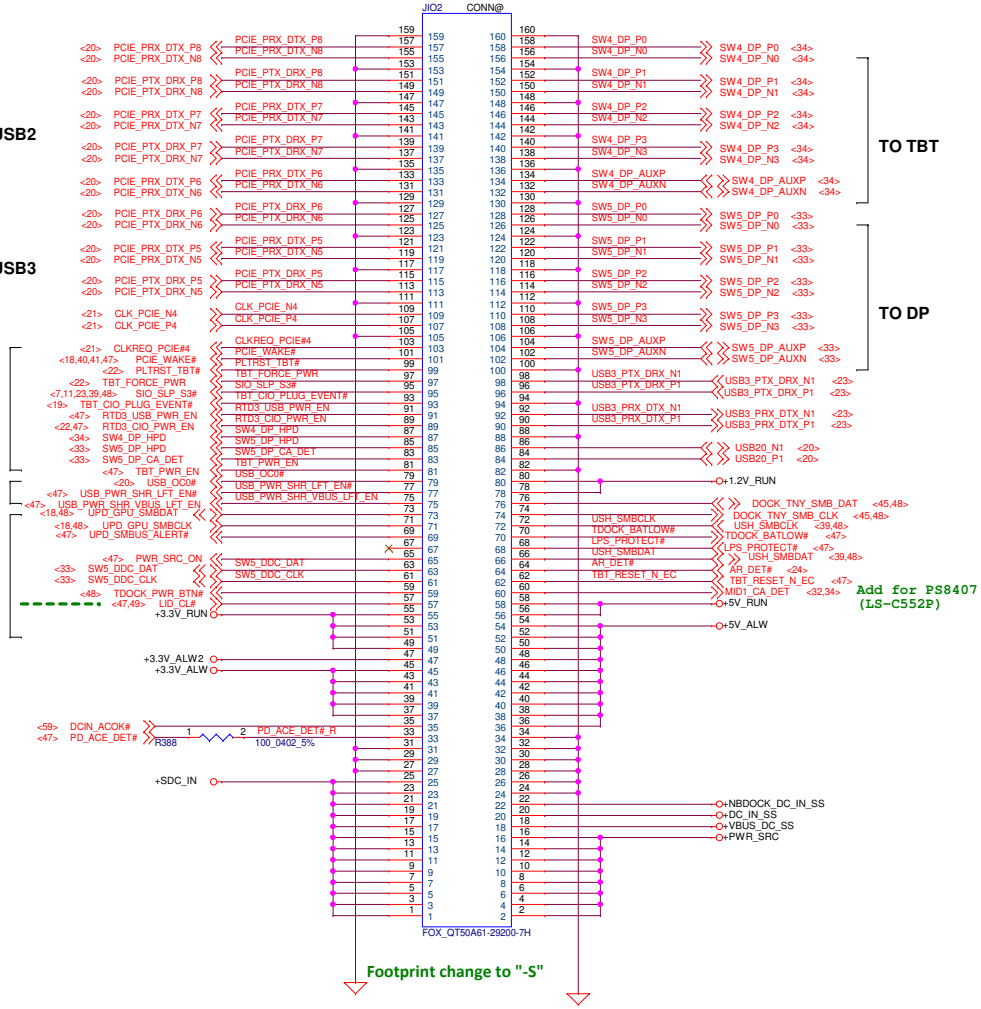
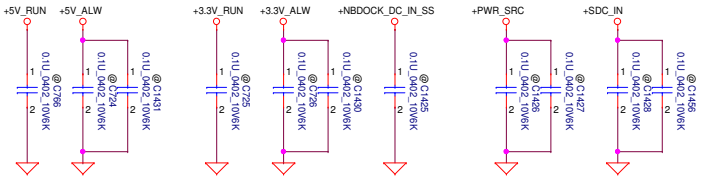
USB/Codec/Card reader IO/B



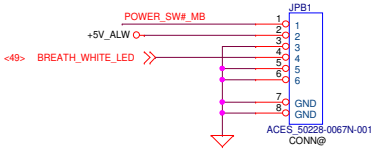


Display daughter /B

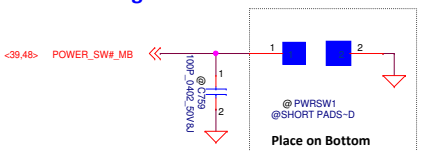


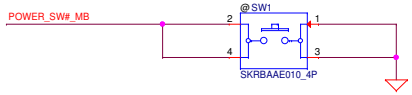


Power Button CONN



Power Switch for debug





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Compal Electronics, Inc.	
Title	IO / PWR Button
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5/9 update

RTD3_CIO_PWR_EN <22,46> — RTD3_CIO_PWR_EN — RTD3_CIO_PWR_EN_R @RE78 0_0402_5%

+3.3V_ALW

USB_PWR_SHR_LFT_EN# RE72 100K_0402_5%
USB_PWR_SHR_RHT_EN1# RE69 100K_0402_5%
USB_PWR_SHR_RHT_EN2# RE70 100K_0402_5%
USB_PWR_SHR_RHT_EN3# RE71 100K_0402_5%
WWAN_RADIO_DIS# RE14 100K_0402_5%
DOCK_TNY_SMBUS_ALRT# R763 10K_0402_5%
HW_GPS_DISABLE# R779 10K_0402_5%
SLICE_BAT_PRES# R2158 100K_0402_5%
PCIE_WAKE# R759 10K_0402_5%
WWAN_WAKE# R773 10K_0402_5%
UPD_SMBUS_ALERT# R3740 100K_0402_5%

RP9 100K_0804_8P4R_5%
SLOT2_CONFIG_0
SLOT2_CONFIG_1
SLOT2_CONFIG_2
SLOT2_CONFIG_3

USB_PWR_SHR_VBUS_LFT_EN RE73 100K_0402_5%
USB_PWR_SHR_VBUS_RHT_EN1 RE74 100K_0402_5%
USB_PWR_SHR_VBUS_RHT_EN2 RE75 100K_0402_5%
USB_PWR_SHR_VBUS_RHT_EN3 RE76 100K_0402_5%
PD_ACE_DET# RE77 100K_0402_5%
PROCHOT_GATE @R415 100K_0402_5%

+3.3V_RUN

RP3 100K_0804_8P4R_5%
D_CLKRUN#
D_SERIRQ
D_DLDRQ#
DGPU_ALERT#

GPU_PWR_LEVEL R782 100K_0402_5%
LPC_LDRQ1# R783 100K_0402_5%
M2_SLOT2_PCIE#_SATA RH318 10K_0402_5%
USH_DET# R379 10K_0402_5%
TBT_RESET_N_EC R886 100K_0402_5%

7/4 update

+3.3V_ALW_U46

0.1U_0402_25V6K C710
0.1U_0402_25V6K C715
0.1U_0402_10V7K C708
0.1U_0402_10V7K C717
0.1U_0402_10V7K C718
0.1U_0402_10V7K C719

PJP@ PJP12 PAD-OPEN1x1m — SHORT DEFALUT — +3.3V_ALW

CIS LINK OK

U46 — VCC1 (B5, A37, B30, A43, A54)

NEW_MXM_SELECT <36>	B52	GPIOA0	
RTD3_CIO_PWR_EN_R	A49	GPIOA1	
LAN_DISABLE#_R	B53	GPIOA2	
AC_DIS <52,62>	A50	GPIOA3	
LID_CL_SIO#	B54	GPIOA4	
DOCK_TNY_SMBUS_ALRT# <45,52>	A51	GPIOA5	
TBT_RESET_N_EC <46>	B55	GPIOA6	
GPU_PWR_LEVEL <18>	A52	GPIOA7	
USB_PWR_SHR_RHT_EN2# <46>	A33		
EN_I2S_NB_CODEC# <46>	B36	GPIOB0	
USH_PWR_STATE# <39>	A34	GPIOB1	
EN_DOCK_PWR_BAR <62>	B37	GPIOC2	
HW_GPS_DISABLE# <40>	A35	GPIOC3	
PANEL_BKEN_EC <30>	B38	GPIOC4	
LCD_TST <30>	A36	GPIOC5	
PSID_DISABLE# <52>	A37	GPIOC6/TACH4	
SLOT4_SSD_PWR_EN <42>	B40	GPIOC7	
DOCKED <37>	A38	GPIOD0	
DOCK_DET# <45>	B41	GPIOC1	
AUD_NB_MUTE# <46>	A39	GPIOC0	
3.3V_WWAN_EN <42>	B42	GPIOB7	
LCD_VCC_TEST_EN <30>	A40	GPIOB6	
WWAN_WAKE# <40>	B43	GPIOB5	
AUD_HP_NB_SENSE <46>	A41	GPIOB4	
USB_PWR_SHR_RHT_EN1# <46>	B44	GPIOB3	
		GPIOB2	
SLOT3_SSD_PWR_EN <42>	B32	GPIOD1	
SLICE_BAT_ON <62>	A31	GPIOD2	
SLICE_BAT_PRES# <45,52,62>	B33	GPIOD3	
TB_STAT# <59>	B15	GPIOD4	
PBA_GPU_SEL# <31>	A15	GPIOD5	
MXM_VGA_DIS# <18>	B16	GPIOD6	
USH_DET# <39>	A16	GPIOD7	
WLAN_WIGIG60GHZ_DIS# <40>	A1	GPIOE0/RXD	
EC5048_TX <48>	B2	GPIOE1/TXD	
	A2	GPIOE2/RTS#	
	B3	GPIOE3/DSR#	
	A3	GPIOE4/CTS#	
DGPU_PWR_EN <18>	B45	GPIOE5/DTR#	
DGPU_ALERT# <18>	A42	GPIOE6/RI#	
MXM_DP_HDMI_HPD <18>	B4	GPIOE7/DCD#	
	A59		
BCM5882_ALERT# <39>	B62	GPIOF0	
UPD_SMBUS_ALERT# <46>	B61	GPIOF1	
	A58	GPIOF2	
DGPU_PWROK <18,23>	A56	GPIOF3/TACH8	
VGA_ID	B59	GPIOF4/TACH7	
3.3V_RUN_GFX_ON <51>	A55	GPIOF5	
TDOCK_BATLOW# <46>	B58	GPIOF6	
	B47	GPIOF7	
M2_SLOT2_PCIE#_SATA	A45	GPIOG0/TACH5	
SYS_LED_MASK# <37,49>	B48	GPIOG1	
	A46	GPIOG2	
DP1_GPU_SEL# <34>	B49	GPIOG3	
	A47	GPIOG4	
USB_PWR_SHR_VBUS_LFT_EN <46>	B50	GPIOG5	
GC6_THM_ON <19>	A48	GPIOG6	
		GPIOG7/TACH6	
PWR_SRC_ON <46>	B13	GPIOH0	
BT_RADIO_DIS# <40>	A13	GPIOH1	
WWAN_RADIO_DIS# <40>	A53	SYSOPT1/GPIOH2	
	B57	SYSOPT0/GPIOH3	
DGPU_SELECT# <29,30>	B14	GPIOH4	
SIO_SLP_WLAN# <23,42>	A14	GPIOH5	
USB_PWR_SHR_RHT_EN3# <46>	B17	GPIOH6	
USB_PWR_SHR_VBUS_RHT_EN1 <46>	B18	GPIOH7	

	A23	GPIOI0	TBT_PWR_EN — TBT_PWR_EN <46>
	B63	GPIOI1	
PD_ACE_DET#	A60	GPIOI2/TACH0	PD_ACE_DET# <46>
PROCHOT_GATE	A61	GPIOI3	PROCHOT_GATE <59>
	B65	GPIOI4	
PLTRST_USH# _EC	A62	GPIOI5	PLTRST_USH#_EC <22>
LPS_PROTECT#	B66	GPIOI6	LPS_PROTECT# <46>
DOCK_AC_OFF_EC	A63	GPIOI7	DOCK_AC_OFF_EC <62>
AUX_EN_WOWL	B67	GPIOJ0	AUX_EN_WOWL <42>
ME_FWP_EC	A64	GPIOJ1/TACH1	ME_FWP_EC <23>
	A5	GPIOJ2/TACH2	
	B6	GPIOJ3	
GPIO_PSID_SELECT	A6	GPIOJ4	GPIO_PSID_SELECT <52>
DP2_GPU_SEL#	B7	GPIOJ5	DP2_GPU_SEL# <33>
DOCK_HP_DET	A7	GPIOJ6	DOCK_HP_DET <46>
DOCK_MIC_DET	B8	GPIOJ7	DOCK_MIC_DET <46>
USB_PWR_SHR_LFT_EN#	A8		
MASK_SATA_LED#	B9	GPIOK0	USB_PWR_SHR_LFT_EN# <46>
PCIE_WAKE#	B10	GPIOK1/TACH3	MASK_SATA_LED# <49>
LED_SATA_DIAG_OUT#	A10	GPIOK2	PCIE_WAKE# <18,40,41,46>
RTD3_USB_PWR_EN	B11	GPIOK3	LED_SATA_DIAG_OUT# <49>
USB_PWR_SHR_VBUS_RHT_EN2	A11	GPIOK4	RTD3_USB_PWR_EN <46>
SLOT2_CONFIG_0	B12	GPIOK5	USB_PWR_SHR_VBUS_RHT_EN2 <46>
USB_PWR_SHR_VBUS_RHT_EN3	A12	GPIOK6	SLOT2_CONFIG_0 <40>
		GPIOK7	USB_PWR_SHR_VBUS_RHT_EN3 <46>
	B60	GPIOL0	
	A57	GPIOL0/PWM7	
	B64	GPIOL1/PWM8	
	B68	GPIOL2/PWM0	
WLAN_DISBL#	A9	GPIOL3/PWM1	WLAN_DISBL# <37>
CCD_OFF	B1	GPIOL4/PWM3	PAD-D @T213
SLOT2_CONFIG_1	A18	GPIOL5/PWM2	PAD-D @T165
SLOT2_CONFIG_2	A44	GPIOL6	SLOT2_CONFIG_1 <40>
		GPIOL7/PWM5	SLOT2_CONFIG_2 <40>
SLOT2_CONFIG_3	B34	GPIOM1	SLOT2_CONFIG_3 <40>
	B39	GPIOM3/PWM4	
	B51	GPIOM4/PWM6	
LPC_AD0	A27		
LPC_AD1	A26	LAD0	LPC_AD0 <23,48>
LPC_AD2	B26	LAD1	LPC_AD1 <23,48>
LPC_AD3	B25	LAD2	LPC_AD2 <23,48>
LPC_FRAME#	A21	LAD3	LPC_AD3 <23,48>
PCH_PLTRST#_EC	B22	LFRAME#	LPC_FRAME# <23,48>
CLK_PCI_5048	A28	LRESET#	PCH_PLTRST#_EC <22,40,41,48>
CLKRUN#	B20	PCICLK	CLK_PCI_5048 <23>
		CLKRUN#	CLKRUN# <23,48>
LPC_LDRQ1#	A22		
IRQ_SERIRQ	B21	LDRQ1#	
CLK_SIO_14M	A32	SER_IRQ	IRQ_SERIRQ <23,48>
EC_32KHZ_ECE5048	B35	14.318MHZ/GPIOM0	PAD-D @T214
		CLK32/GPIOM2	EC_32KHZ_ECE5048 <48>
D_LAD0	B29		
D_LAD1	B28	DLAD0	D_LAD0 <45>
D_LAD2	A25	DLAD1	D_LAD1 <45>
D_LAD3	A24	DLAD2	D_LAD2 <45>
D_LFRAME#	B23	DLAD3	D_LAD3 <45>
D_CLKRUN#	A19	DLFRAME#	D_LFRAME# <45>
D_DLDRQ1#	B24	DCLKRUN#	D_CLKRUN# <45>
D_SERIRQ	A20	DLDRQ1#	D_DLDRQ1# <45>
		DSER_IRQ	D_SERIRQ <45>
BC_INT# ECE5048	A29	BC_INT#	BC_INT# ECE5048 <48>
BC_DAT ECE5048	B31	BC_DAT	BC_DAT ECE5048 <48>
BC_CLK ECE5048	A30	BC_CLK	BC_CLK_ECE5048 <48>
RUNPWROK	A4	PWRGD	RUNPWROK <48>
	B56	OUT65	
	B19	TEST_PIN	R804 1K_0402_1%
+CAP_LDO	B46	CAP_LDO	
	B27	VSS	4.7U_0603_6.3V6K C714
	C1	EP	

DB Version 0.4
ECE5048-LZY_DQFN132_11X11~D

+CAP_LDO trace width 20 mils

RP4 100K_0804_8P4R_5%
LCD_TST
SLICE_BAT_ON
MXM_DP_HDMI_HPD

GPIOL0 @R3741 100K_0402_5%
SYS_LED_MASK# R775 10K_0402_5%
PROCHOT_GATE R416 100K_0402_5%

+3.3V_ALW

Tell EC don't read GFX Temp.in GC6
High: Read; Low: Don't read

R800 100K_0402_5%
VGA_ID — VGA_ID <18>
@R803 100K_0402_5%

	VGA_ID0
Discrete	0
UMA	1

CLK_PCI_5048 — @R795 10_0402_1% — @C713 4.7P_0402_50V8C

+3.3V_ALW

R805 100K_0402_5%
LID_CL_SIO# — R807 10_0402_1% — LID_CL# <46,49>
C716 0.047U_0402_16V4Z

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SIO (ECE5048)

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Date: Wednesday, November 30, 2016 | Sheet 47 of 72

PN change from SA00006YH00 to SA00006YH90

6/8 update

5/11 update

5/5 update

Place close pin A21

Place close pin A29

32 KHz Clock

1: Channel 1 will provide Thermistor Readings
0: Channel 1 will provide Diode Readings

C1343, C1350, C1351, C1346 Place near U51

C292 Place near U51.A48

R866 close to U51 at least 250mils

Q28 change from SB000008P00 to SB00000Z500

7/1 update

CT: 3300 pF ~ 10ms delay

Reset Threshold Level 3.0V

Rest=1.33k, Tp=93degree

CIS link OK

CIS link OK

R875	C744	REV
240K	4700p	X00
130K	4700p	X01
33K	4700p	X02
4.3K	4700p	A00
2K	4700p	A01
1K	4700p	A02

R3754	C1465	REV
240K	4700p	12"
130K	4700p	14"
33K	4700p	15"
4.3K	4700p	17"
2K	4700p	***
1K	4700p	***

BOARD_ID rise time is measured from 5%~68%.

Channel	Location
DP1/DN1	CPU
DP1a/DN1a	OTP CPU
DP2/DN2	VR MXM(TOP)
DP2a/DN2a	M.2 2280
DP3/DN3	DIMM(TOP)
DP4/DN4	WWAN

DP1/DN1 for CPU OTP on Q16, place Q16 close to CPU and C273 close to Q16.

DN1a/DP1a for CPU VR on Q26, place Q26 close to CPU and C339 close to Q26

DP3/DN3 for SODIMM(TOP) on Q14, place Q14 close to SODIMM(TOP) and C272 close to Q14

DP2/DN2 for MXM(TOP side) on Q27, place Q27 close to MXM(TOP side) and C291 close to Q27.

DN2a/DP2a for M.2 2280 on Q17, place Q17 close to M.2 2280 and C340 close to Q17

DP4/DN4 for WWAN on Q15, place Q15 close to WiGig and C288 close to Q15

8/25 update

Q14, Q15, Q16, Q17, Q26, Q27 change from SB000008P00 to SB00000Z500

Compal Electronics, Inc.
Title: KBC (MEC5085)
Size: Document Number: LA-E321P
Rev: 1.0
Date: Wednesday, November 30, 2016
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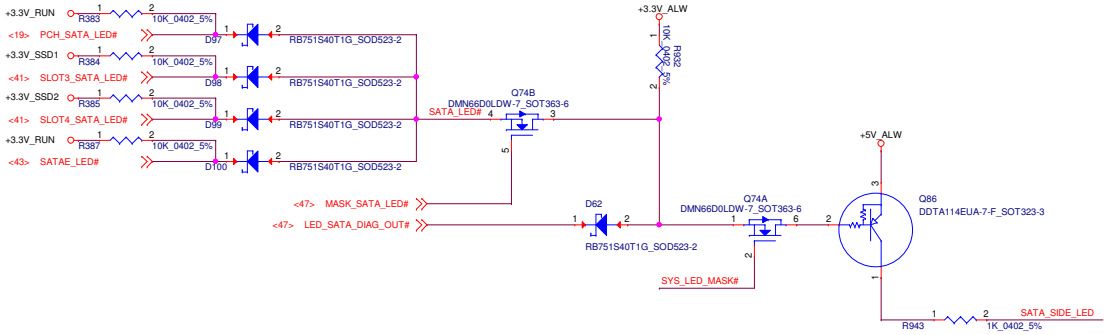
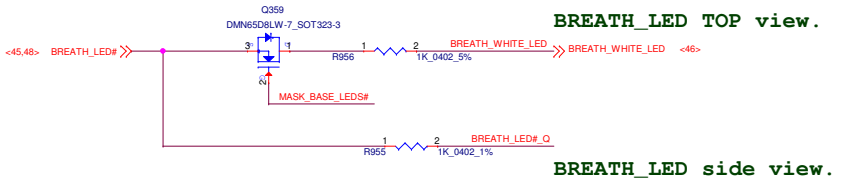
HDD LED



Breath LED

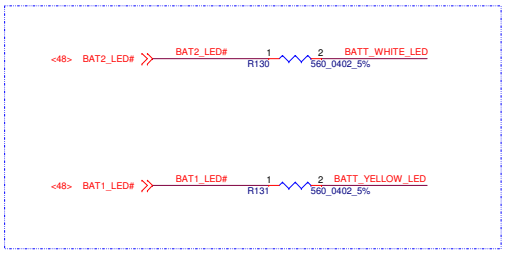


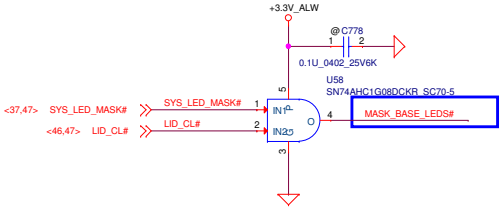
BREATH_LED TOP view.

BREATH_LED side view.

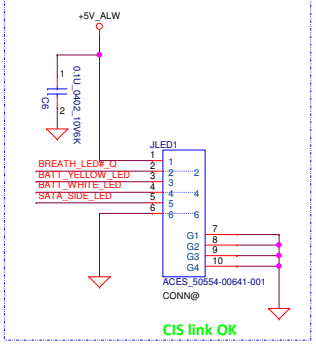
LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

BATT LED



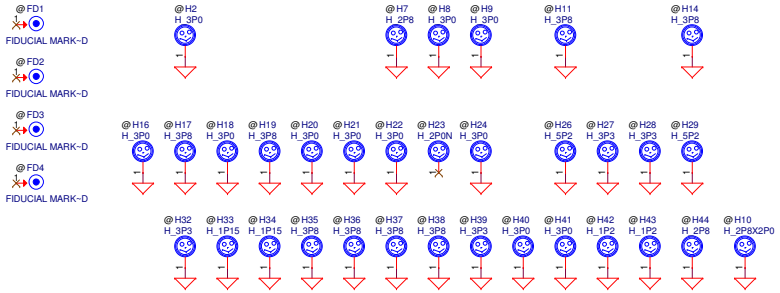


To LED/B Conn



CIS link OK

Fiducial Mark



DELL CONFIDENTIAL/PROPRIETARY

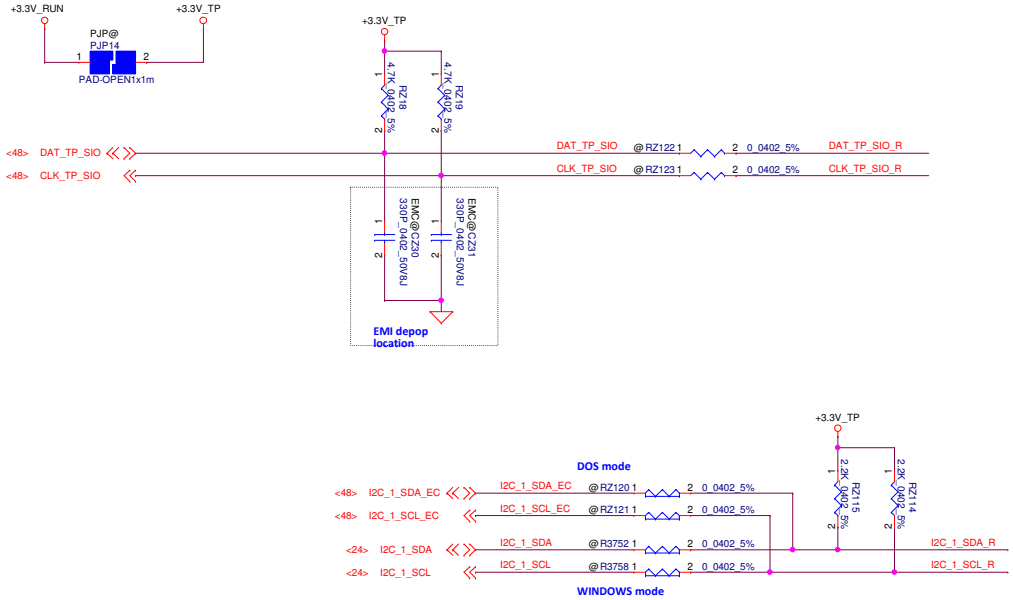
Compal Electronics, Inc.

Title: LED / Screw hole

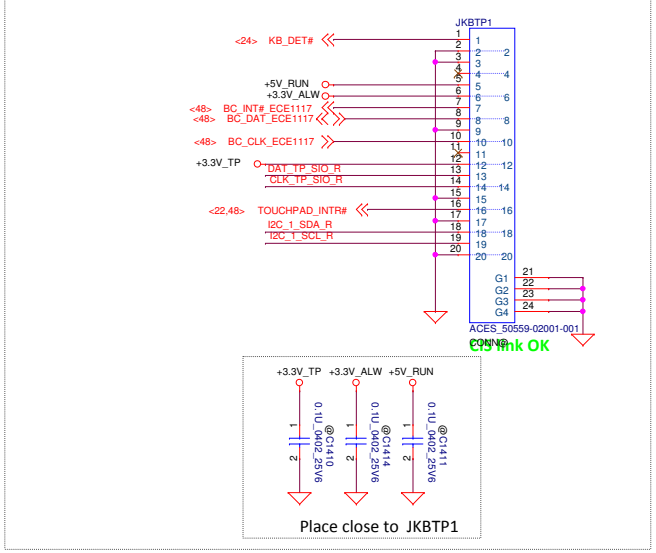
Size | Document Number: LA-E321P | Rev: 1.0

Date: Wednesday, November 30, 2016 | Sheet 49 of 72

Touch Pad



Keyboard



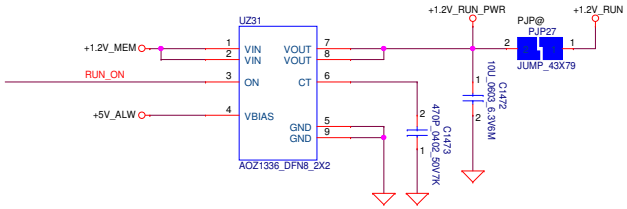
Compal Electronics, Inc.

Title: KB / TP / RSMRST#

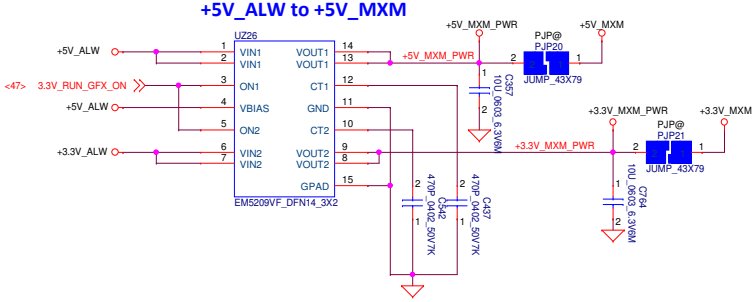
Size | Document Number: LA-E321P | Rev: 1.0

Date: Thursday, December 08, 2016 | Sheet 50 of 72

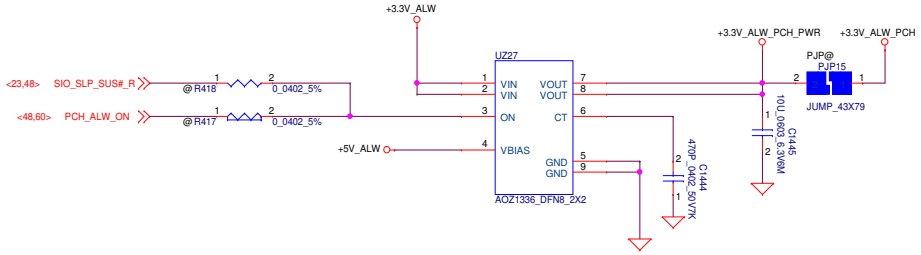
+1.2V_RUN Source



+3.3V_ALW to +3.3V_MXM
+5V_ALW to +5V_MXM

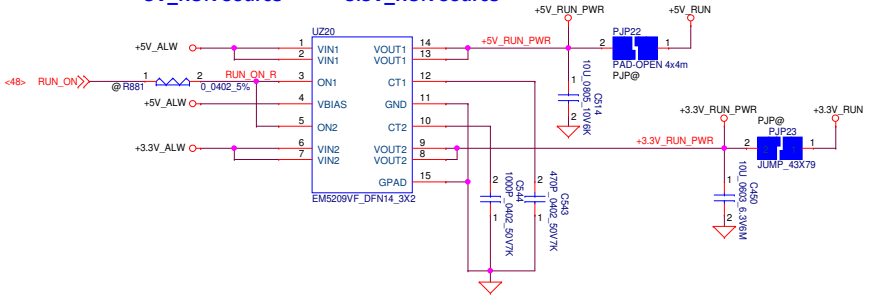


+3.3V_ALW_PCH Source

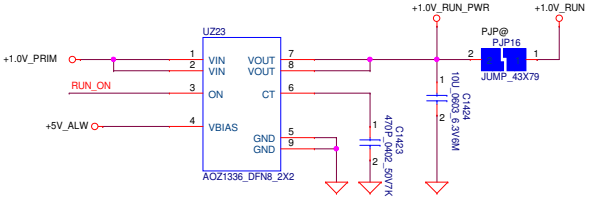


+5V_RUN Source

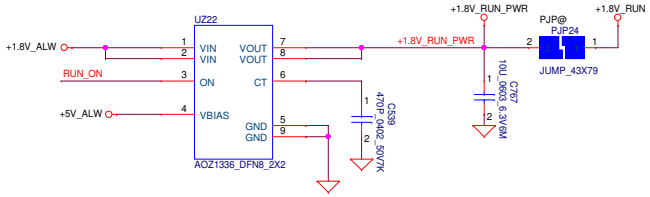
+3.3V_RUN Source



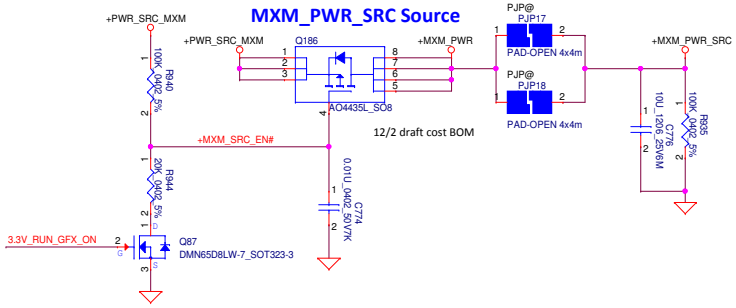
+1.0V_PRIM to +1.0V_RUN



+1.8V_RUN Source



MXM_PWR_SRC Source



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Compal Electronics, Inc.		
Title: Power Control		
Size	Document Number: LA-E321P	Rev: 1.0
Date: Wednesday, November 30, 2016	Sheet 51 of 72	

EVT change item from Miramar schematic

DVT1.0 change item

DVT2.0 change item

Pilot build change item

EMI Part (47.1)

+PWR_SRC

EMC@ PL1 SMB3025500YA_2P

+PWR_SRC_MXM

@ PC31 0.1U_0603_25V7K

@ PC30 10U_0603_25V6K

PC1 100U_25V_M

ESD Diodes

ESD (47.2)

EMC@ PD2 TVNST52302AB0_SOT523-3

EMC@ PD3 TVNST52302AB0_SOT523-3

EMI Part (47.1)

EMC@ PL2 FBMJ4516HS720NT_2P

EMC@ PL6 FBMJ4516HS720NT_2P

PBATT+_C

PBATT+

+3.3V_ALW

PR2 100K_0402_5%

Primary Battery Connector

EMI Part (47.1)

CONN@ SUYIN_200045GR009M28QZR

EMC@ PC4 2200P_0402_50V7K

Z4304

Z4305

Z4306

PR3 100_0804_8P4R_5%

GND

PBATT1

CHARGER_PBAT_SMBCLK <48,59>

CHARGER_PBAT_SMBDAT <48,59>

PBAT_PRES# <48,59>

PD5 SDMK0340L-7-F_SOD323

PQ1 AO3409_SOT23

DOCK_TNY_SMBUS_ALRT# <45,47>

<45,47,62> SLICE_BAT_PRES#

0_0402_5%

@ PR33

PC5 1500P_0402_50V7K

+3.3V_ALW

<45> DOCK_PSID

EMI Part (47.1)

@ PR7 0_0402_5%

EMC@ PL3 BLM15BX102SN1D_2P

NB_PSID

PR9 33_0402_5%

PQ2 FDV301N_G_NL_SOT23-3-D

PR8 2.2K_0402_5%

@EMC@ PD6 PESD5V0U2BT_SOT23-3

NB_PSID_TS5A63157

PU1 TS5A63157DCKR_SC70-6

GPIO_PSID_SELECT <47>

+5V_ALW

PS_ID <48>

@ PT1 PAD-D

@EMC@ PD4 PESD5V0U2BT_SOT23-3

PR10 100K_0402_1%

PR12 15K_0402_1%

PQ3 MMST3904-7-F_SOT323-3

+5V_ALW

PR11 10K_0402_1%

PR13 @ 10K_0402_5%

PSID_DISABLE# <47>

6/8 add diode for ESD team Matt request

EMI Part (47.1)

DC_IN+ Source

EMC@ PL5 SMB3025500YA_2P

EMC@ PL4 SMB3025500YA_2P

PJPDC1 ACES_50493-0110N-001

+DCIN_JACK

CONN@

PC11 1000P_0402_50V7K

@ PD8 VZ0603M260APT_0603

EMC@ PC15 1000P_0402_50V7K

PR19 @ 4.7K_0805_5%

+DC_IN

SI7149DP PQ5

0.022U_0603_50V7K

PR16 1M_0402_5%

PQ8B DCX124EK-7-F_SC74R-6

PQ8A DCX124EK-7-F_SC74R-6

PR20 10K_0402_5%

SOFT_START_GC <62>

AC_DIS <47,62>

PR22 1M_0402_5%

+DC_IN_SS

PR18 100K_0402_5%

PC14 10U_0805_25V6K

DELL CONFIDENTIAL/PROPRIETARY

COIN RTC Battery

+COINCELL

PR1 1K_0402_5%

+3.3V_RTC_LDO

Z4012

PD1 BAS40CW_SOT323-3

+RTC_CELL

PC2 1U_0603_10V4Z

Move to power schematic

CONN@ JRTC1 ACES_50271-0020N-001

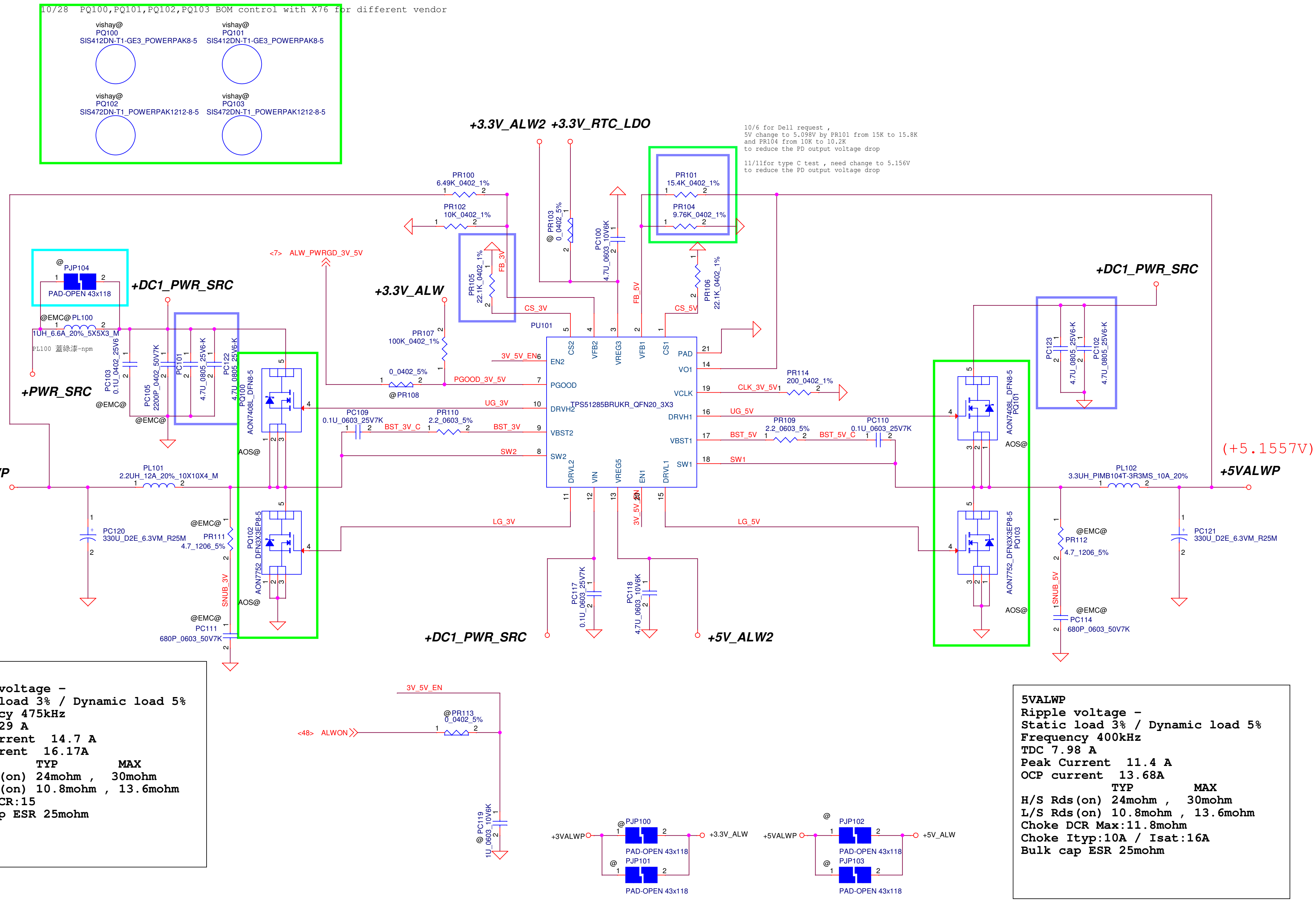
GND

Compal Electronics, Inc.

Title: +DCIN

Size: | Document Number: LA-E321P | Rev: 0.3

Date: Thursday, December 08, 2016 | Sheet 52 of 72


10/28 PQ100,PQ101,PQ102,PQ103 BOM control with X76 for different vendor
vishay@ PQ100 SIS412DN-T1-GE3_POWERPAK8-5
vishay@ PQ101 SIS412DN-T1-GE3_POWERPAK8-5
vishay@ PQ102 SIS472DN-T1_POWERPAK1212-8-5
vishay@ PQ103 SIS472DN-T1_POWERPAK1212-8-5
+3.3V_ALW2
+3.3V_RTC_LDO
10/6 for Dell request ,
5V change to 5.098V by PR101 from 15K to 15.8K
and PR104 from 10K to 10.2K
to reduce the PD output voltage drop
11/11for type C test , need change to 5.156V
to reduce the PD output voltage drop
PR100 6.49K_0402_1%
PR102 10K_0402_1%
PR101 15.4K_0402_1%
PR104 9.76K_0402_1%
PR103 0_0402_5%
PC100 4.7U_0603_10V6K
PR105 22.1K_0402_1%
PR106 22.1K_0402_1%
FB_3V
FB_5V
CS_3V
CS_5V
PJP104 PAD-OPEN 43x118
+DC1_PWR_SRC
<7> ALW_PWRGD_3V_5V
+3.3V_ALW
PR107 100K_0402_1%
PU101
TPS51285BRUKR_QFN20_3X3
EN2 PGOOD DRVH2 VBST2 SW2 DRVL2 VIN VREG5 EN1 DRVL1 CS2 VFB2 VREG3 VFB1 CS1 PAD VO1 VCLK DRVH1 VBST1 SW1
3V_5V_EN
PGOOD_3V_5V
@PR108 0_0402_5%
UG_3V
BST_3V
BST_3V_C
SW2
PC109 0.1U_0603_25V7K
PR110 2.2_0603_5%
PR114 200_0402_1%
CLK_3V_5V
UG_5V
BST_5V
BST_5V_C
PR109 2.2_0603_5%
PC110 0.1U_0603_25V7K
SW1
@EMC@ PL100 1UH_6.6A_20%_5X5X3_M
PL100 蓋錄漆-npm
+PWR_SRC
PC103 0.1U_0402_25V6
PC105 2200P_0402_50V7K
PC101 4.7U_0805_25V6-K
PC122 4.7U_0805_25V6-K
PQ100 AON7408L_DFN8-5
AOS@
+3VALWP
PL101 2.2UH_12A_20%_10X10X4_M
PC120 330U_D2E_6.3VM_R25M
@EMC@ PR111 4.7_1206_5%
SNUB_3V
PQ102 AON7752_DFN3X3EP8-5
@EMC@ PC111 680P_0603_50V7K
LG_3V
LG_5V
3V_5V_EN
PC117 0.1U_0603_25V7K
PC118 4.7U_0603_10V6K
+DC1_PWR_SRC
+5V_ALW2
PQ101 AON7408L_DFN8-5
PQ103 AON7752_DFN3X3EP8-5
PC123 4.7U_0805_25V6-K
PC102 4.7U_0805_25V6-K
(+5.1557V)
+5VALWP
PL102 3.3UH_PIMB104T-3R3MS_10A_20%
PC121 330U_D2E_6.3VM_R25M
@EMC@ PR112 4.7_1206_5%
SNUB_5V
@EMC@ PC114 680P_0603_50V7K
@PR113 0_0402_5%
<48> ALWON
@ PC119 1U_0603_10V6K
+3VALWP
@PJP100 PAD-OPEN 43x118
@ PJP101 PAD-OPEN 43x118
+3.3V_ALW
+5VALWP
@ PJP102 PAD-OPEN 43x118
@ PJP103 PAD-OPEN 43x118
+5V_ALW

3VALWP
Ripple voltage –
Static load 3% / Dynamic load 5%
Frequency 475kHz
TDC 10.29 A
Peak Current 14.7 A
OCP current 16.17A

	TYP	MAX
H/S Rds(on)	24mohm ,	30mohm
L/S Rds(on)	10.8mohm ,	13.6mohm

Choke DCR:15
Bulk cap ESR 25mohm

5VALWP
Ripple voltage –
Static load 3% / Dynamic load 5%
Frequency 400kHz
TDC 7.98 A
Peak Current 11.4 A
OCP current 13.68A

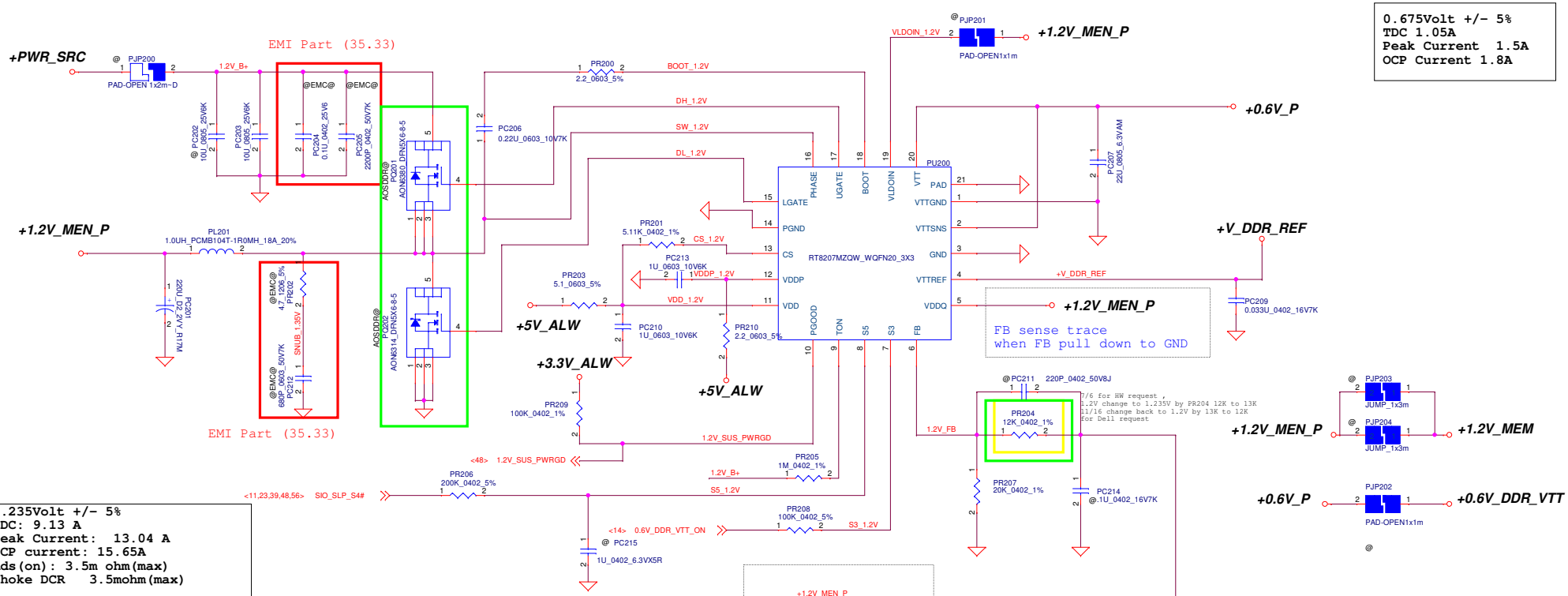
	TYP	MAX
H/S Rds(on)	24mohm ,	30mohm
L/S Rds(on)	10.8mohm ,	13.6mohm

Choke DCR Max:11.8mohm
Choke Ityp:10A / Isat:16A
Bulk cap ESR 25mohm

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title	+5V_ALW/3.3V_ALW	
Size	Document Number: LA-E321P	Rev 0.3
Date: Wednesday, November 30, 2016	Sheet 53 of 72	



0.675Volt +/- 5%
TDC 1.05A
Peak Current 1.5A
OCP Current 1.8A

1.235Volt +/- 5%
TDC: 9.13 A
Peak Current: 13.04 A
OCP current: 15.65A
Rds(on): 3.5m ohm(max)
Choke DCR 3.5mohm(max)

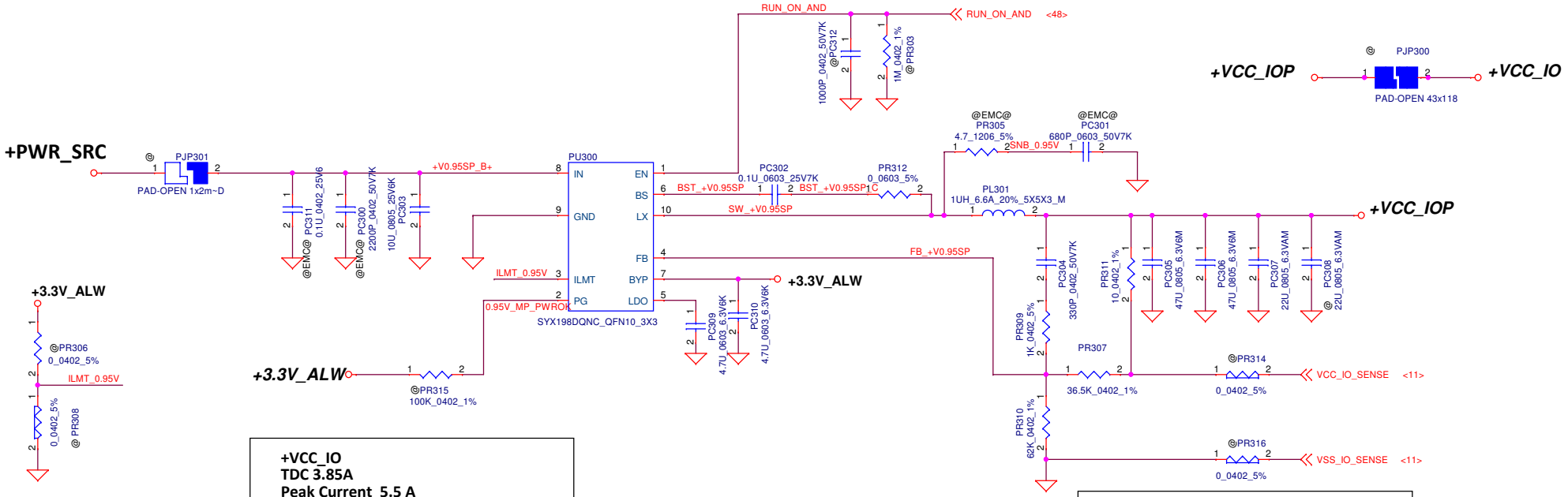
Mode	S3	S5	+1.35V_MEN	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off(Hi-Z)
S0	H	H	on	on	on

Compal Electronics, Inc.

Title: 1.2VP/0.6VSP

Size | Document Number: LA-E321P | Rev: 0.3

Date: Wednesday, November 30, 2016 | Sheet 54 of 72



+VCC_IO
TDC 3.85A
Peak Current 5.5 A
OCP Current 8 A

	TYP	MAX
Choke DCR	13.0mohm ,	14.0mohm

proximal
PR311 0 ohm PR314 10 ohm PR316 10 ohm

remote
PR311 10 ohm PR314 0 ohm PR316 0 ohm

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	+VCC_IO 0.95V
Size	Document Number: LA-E321P
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Date:	Wednesday, November 30, 2016
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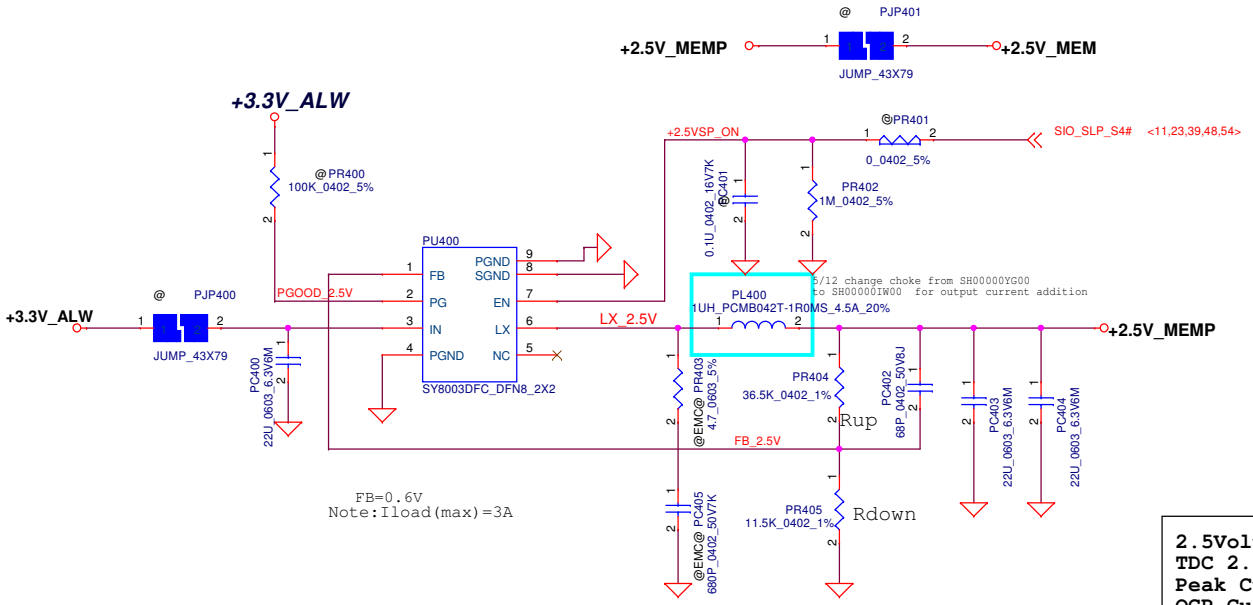

2.5Volt
TDC 2.8A
Peak Current 4A
OCP Current 4.8A

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

Compal Electronics, Inc.		
Title: +2.5V_MEM		
Size	Document Number: LA-E321P	Rev: 0.3
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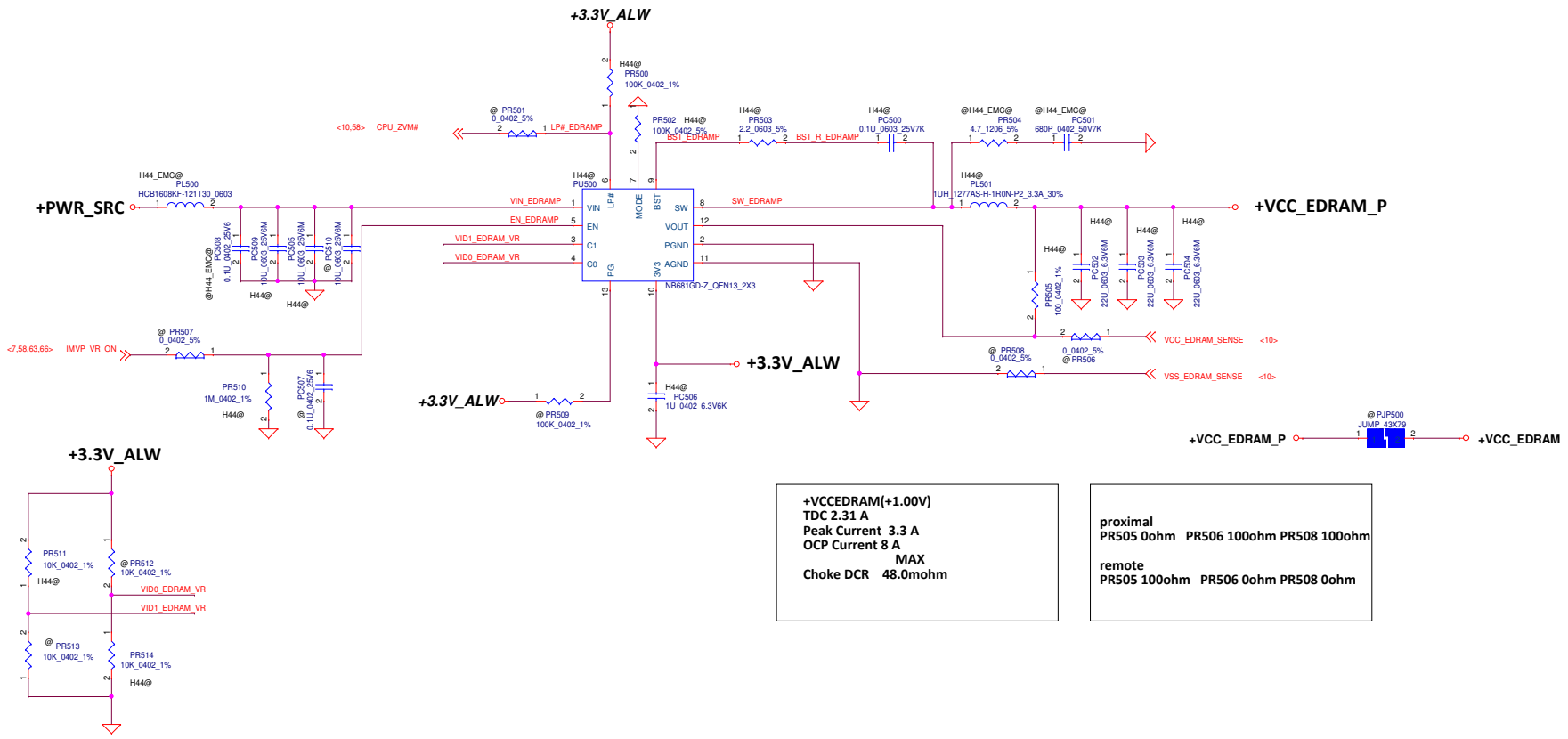
Only H44e



+VCCEDRAM(+1.00V)
TDC 2.31 A
Peak Current 3.3 A
OCP Current 8 A
MAX
Choke DCR 48.0mohm

proximal
PR505 0ohm PR506 100ohm PR508 100ohm

remote
PR505 100ohm PR506 0ohm PR508 0ohm

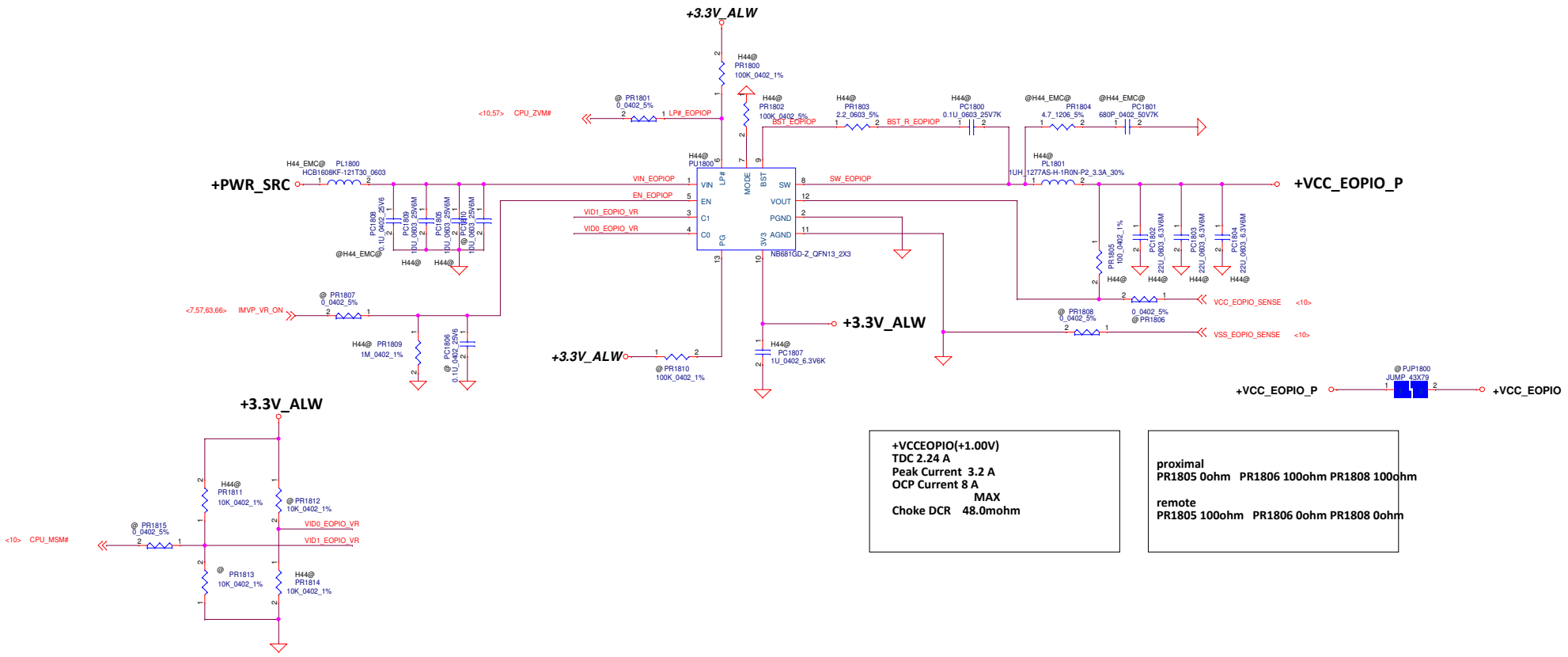
Compal Electronics, Inc.

Title: +VCCEDRAM, 1V

Size | Document Number: LA-E321P | Rev: 0.3

Date: Wednesday, November 30, 2016 | Sheet 57 of 72

Only H44e



+VCCEOPIO(+1.00V)
TDC 2.24 A
Peak Current 3.2 A
OCP Current 8 A
MAX
Choke DCR 48.0mohm

proximal
PR1805 0ohm PR1806 100ohm PR1808 100ohm

remote
PR1805 100ohm PR1806 0ohm PR1808 0ohm

Compal Electronics, Inc.

Title: +VCCEOPIO, 1V

Size | Document Number: LA-E321P | Rev: 0.3

Date: Wednesday, November 30, 2016 | Sheet 58 of 72

Iada=0~12.3A(240W)

ADP_I = 40*Iadapter*Rsense

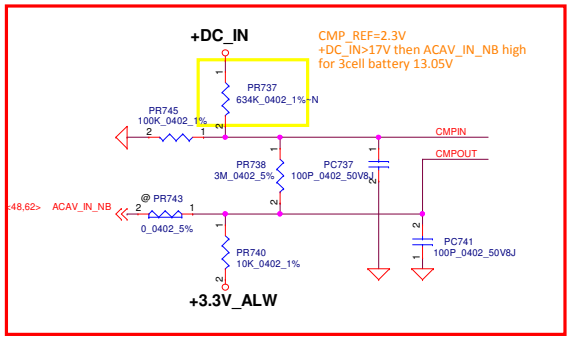
Current limit
Charger :7.8A Vilim=1.56V
6 Cell (0.8C)
Max Boost Charger :7.8A, Vilim=0.39V

AC Det (typ 2.4V)
Max:16.994V
Typ :16.540V
Min :16.098V

EMI Part (47.1)

EMI Part (35.33)

2016/7/22
For Temp voltage test ,
+DC_IN setting for ACAVIN_NB need less than 17.55V ,
so change PR737 from SD034665380
(S RES 1/16W 665K +-1% 0402) to
SD034634380(S RES 1/16W 634K +-1% 0402)



(CMP_REF=2.3V
+DC_IN>17.6V then ACAV_IN_NB high
for 4cell battery 17.4V[Miramar setting])

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Title	PWR_Charger
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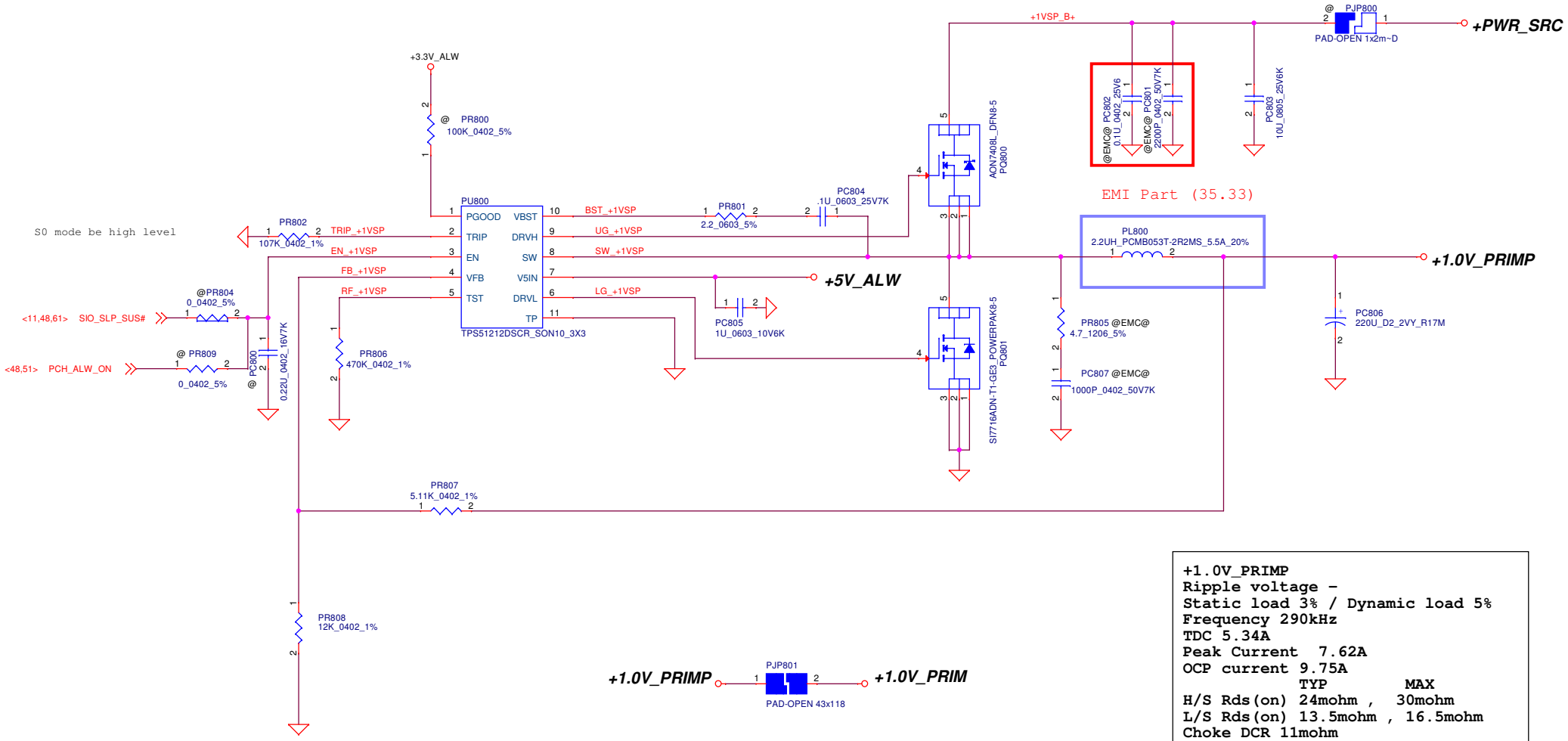

+1.0V_PRIMP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 290kHz
TDC 5.34A
Peak Current 7.62A
OCP current 9.75A

	TYP	MAX
H/S Rds(on)	24mohm ,	30mohm
L/S Rds(on)	13.5mohm ,	16.5mohm

Choke DCR 11mohm
Bulk cap ESR 17mohm

Compal Electronics, Inc.

Title: +1.0V_PRIM

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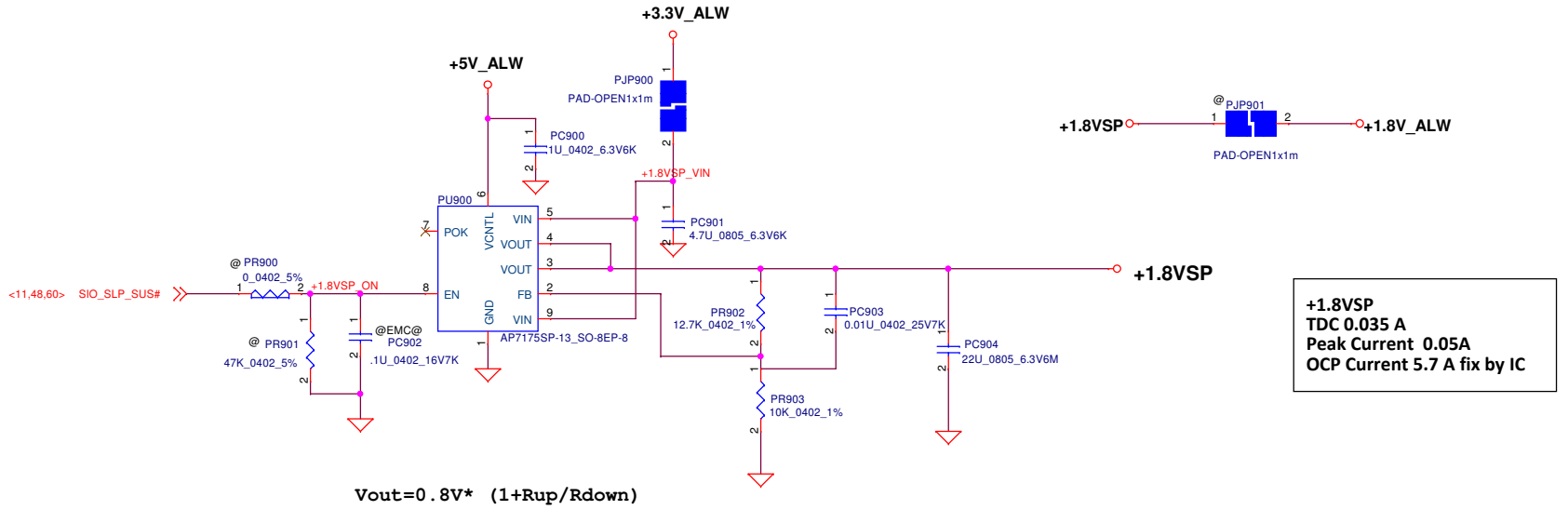

+1.8VSP
TDC 0.035 A
Peak Current 0.05A
OCP Current 5.7 A fix by IC

Compal Electronics, Inc.		
Title: +1.8V_ALW		
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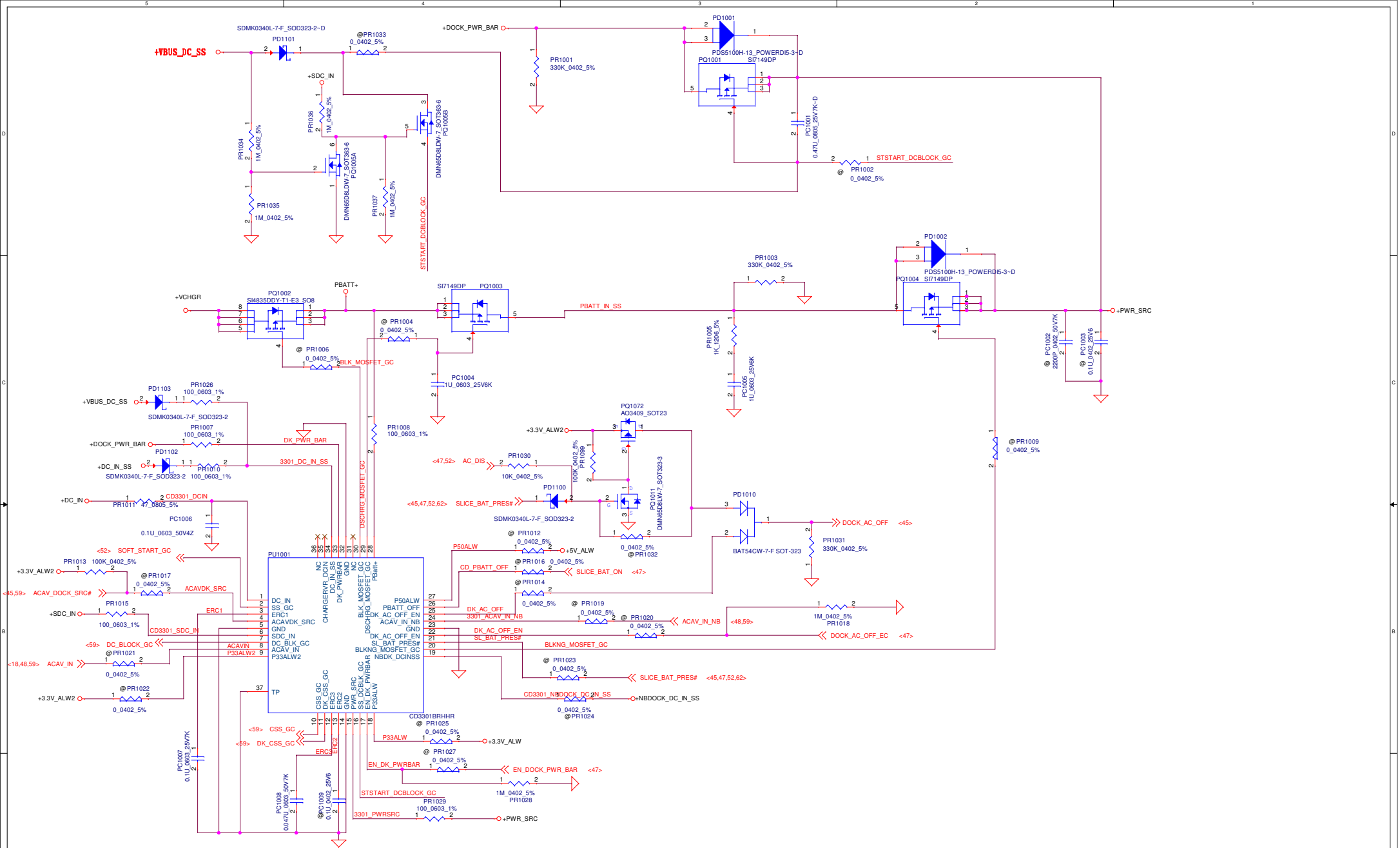

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Title: Selector

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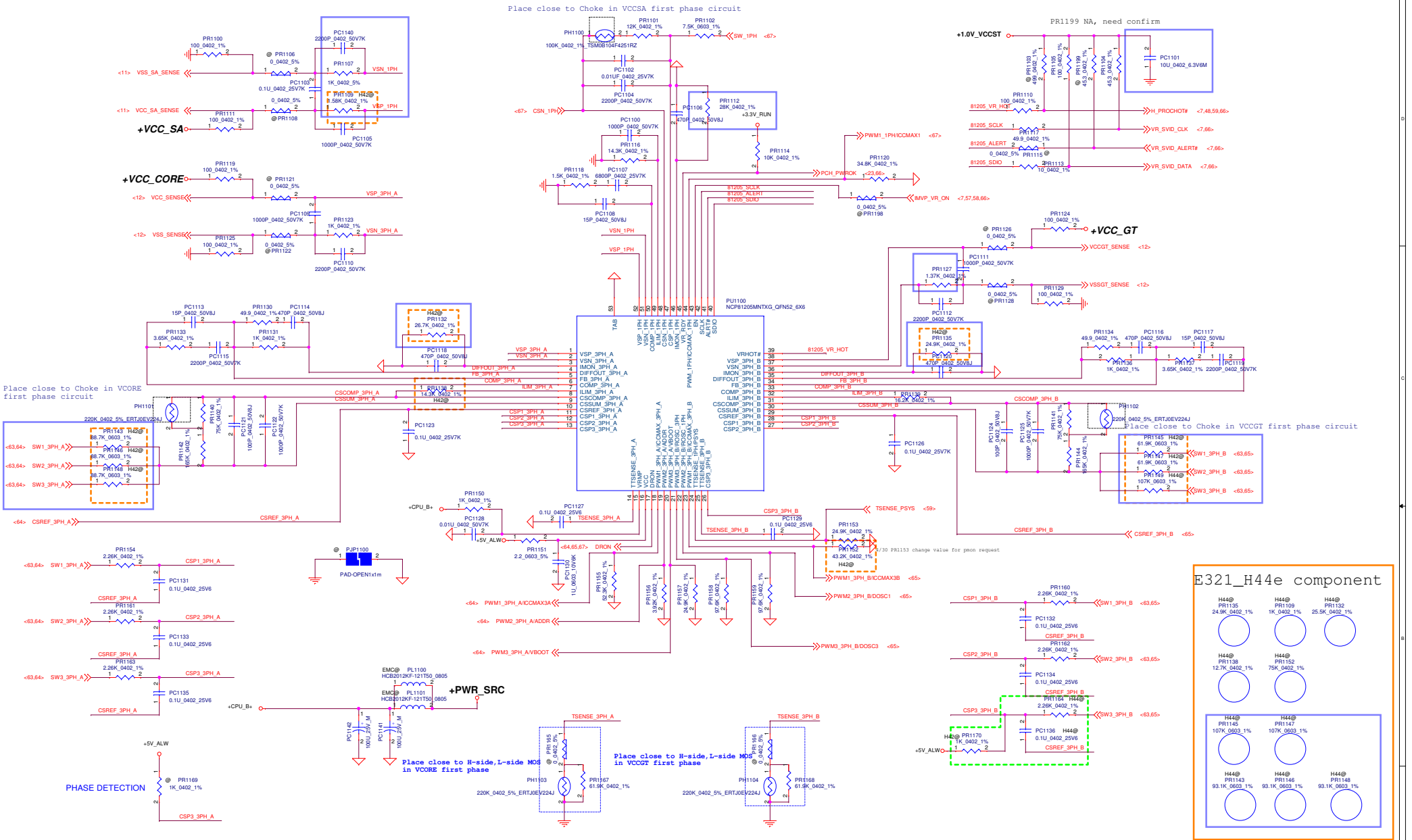
Place close to Choke in VCCSA first phase circuit
PR1199 NA, need confirm
+VCC_SA
+VCC_CORE
+VCC_GT
+1.0V_VCCST
Place close to Choke in VCORE first phase circuit
Place close to Choke in VCCGT first phase circuit
PU1100
NCP81205MNTXG_QFN52_6X6
PWM_1PH/ICCMAX_1PH
PHASE DETECTION
+PWR_SRC
Place close to H-side,L-side MOS in VCORE first phase
Place close to H-side,L-side MOS in VCCGT first phase
E321_H44e component
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Compal Electronics, Inc.
+VCORE
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Rev 0.3
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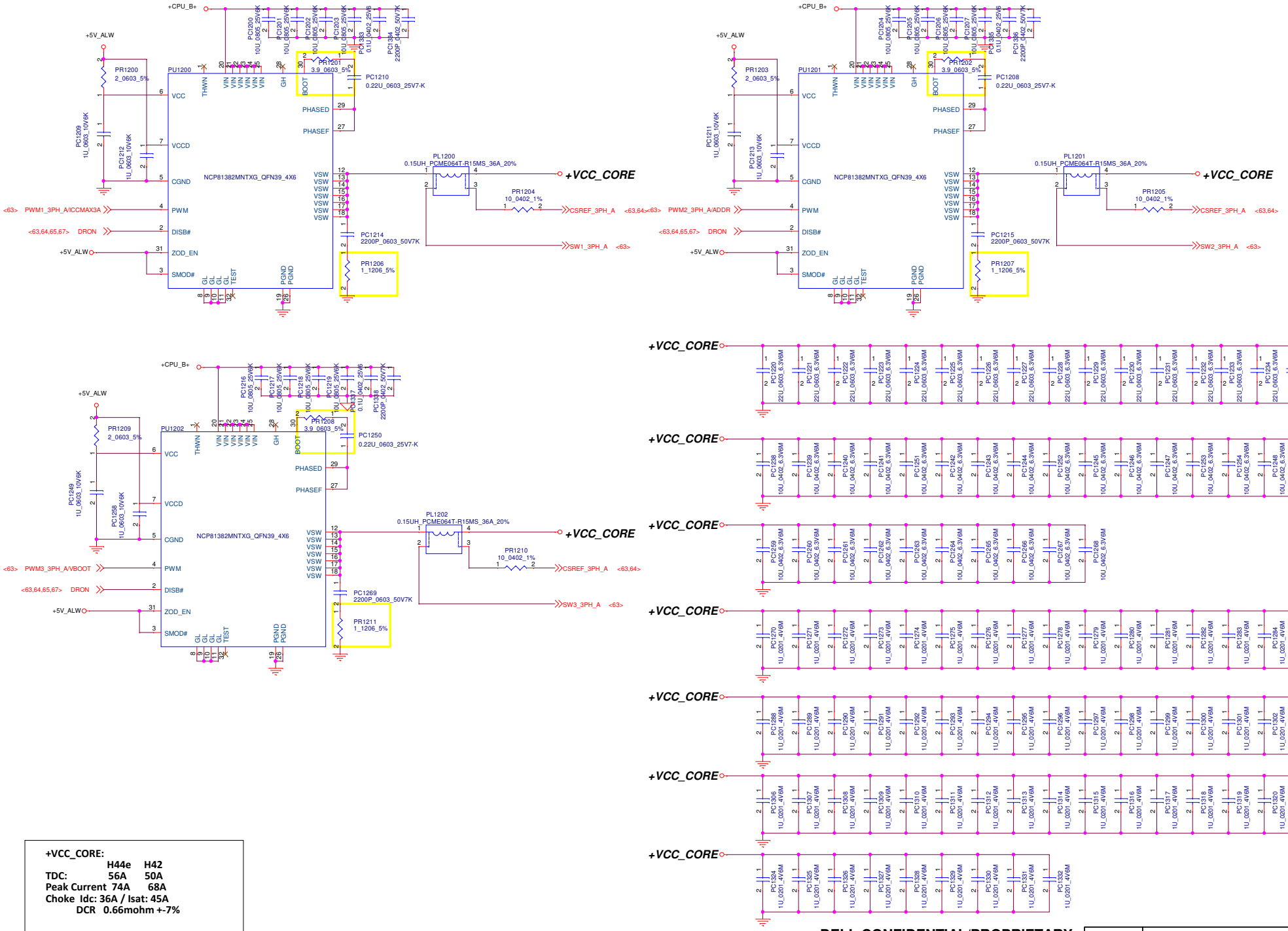

+VCC_CORE:

	H44e	H42
TDC:	56A	50A
Peak Current	74A	68A

Choke Idc: 36A / Isat: 45A

DCR 0.66mohm +-7%

Compal Electronics, Inc.	
Title	+VCC_CORE
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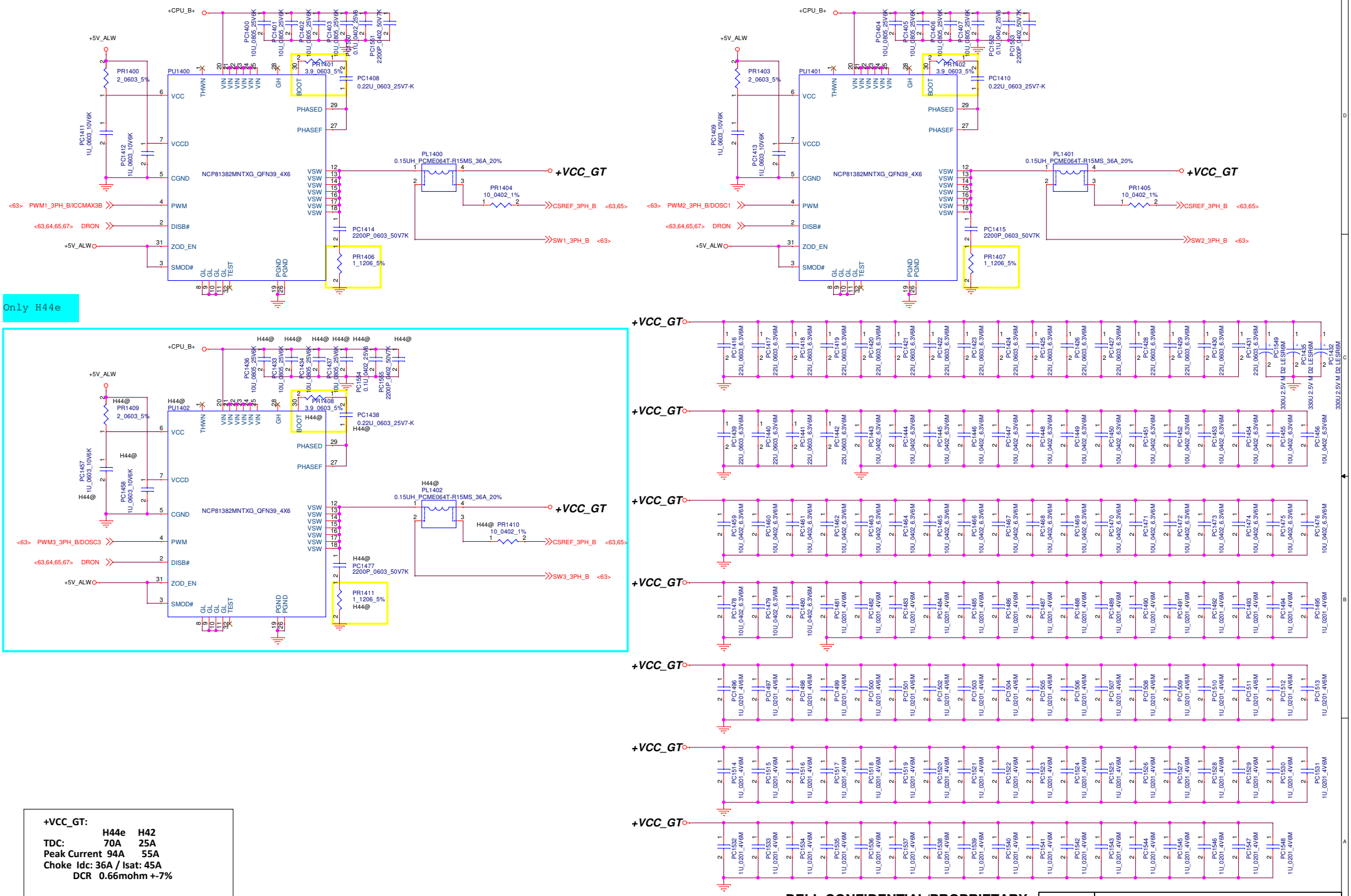

+VCC_GT:

	H44e	H42
TDC:	70A	25A
Peak Current	94A	55A

Choke Idc: 36A / Isat: 45A

DCR 0.66mohm +-7%

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Title: +VCC_GT

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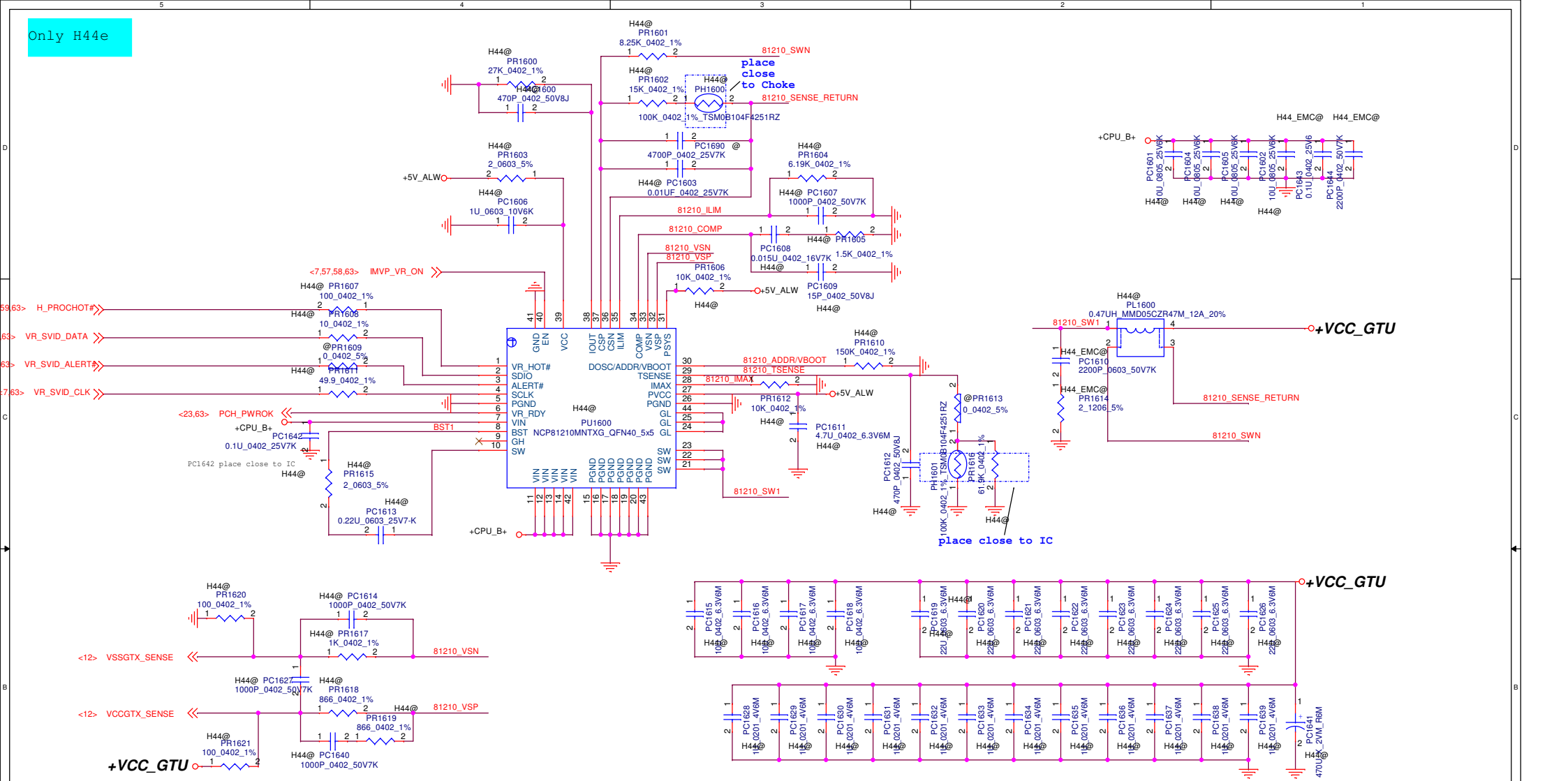

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Compal Electronics, Inc.		
Title	+VCC_GTX	
Size	Document Number LA-E321P	Rev 0.3
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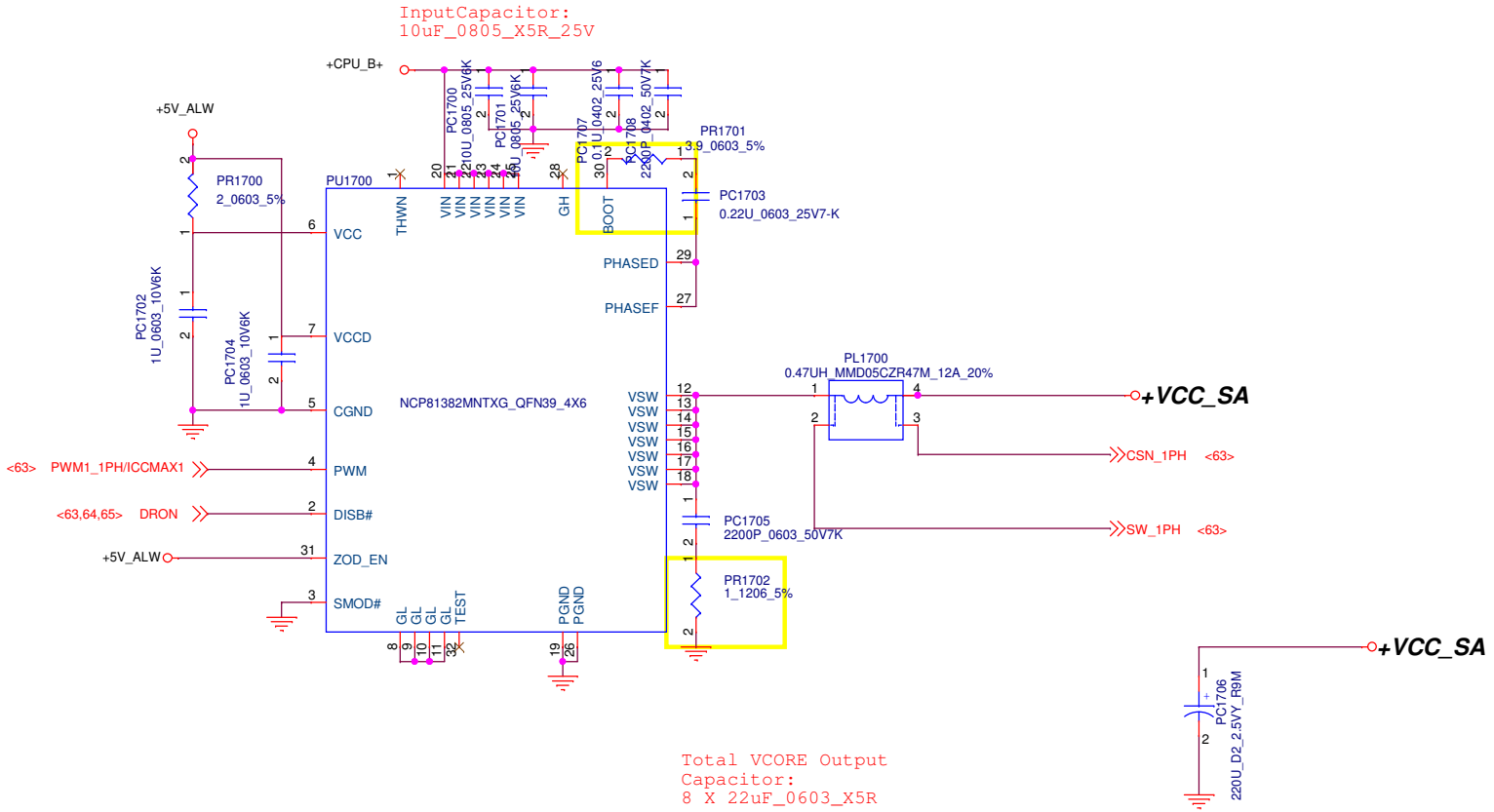

+VCC_SA
TDC 7.77A
Peak Current 11.1 A
OCP Current 13.32 A
Choke Idc: 12.2A / Isat: 16A
DCR 6.2mohm +-5%

Compal Electronics, Inc.		
Title: +VCC_SA		
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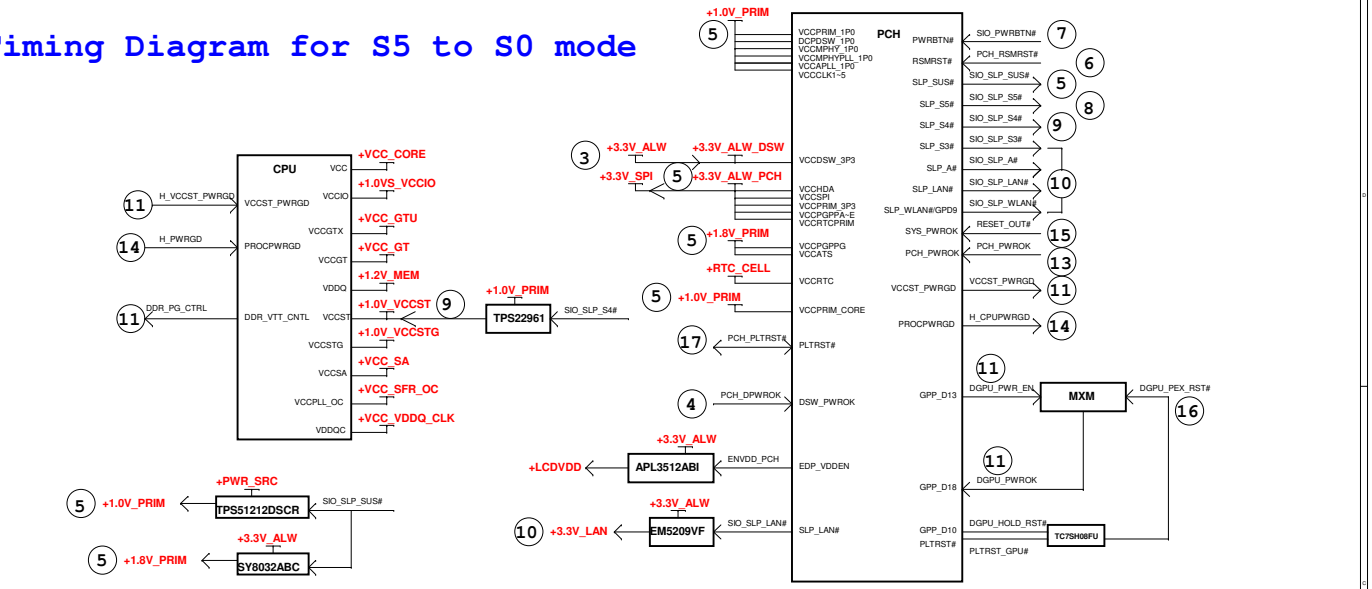
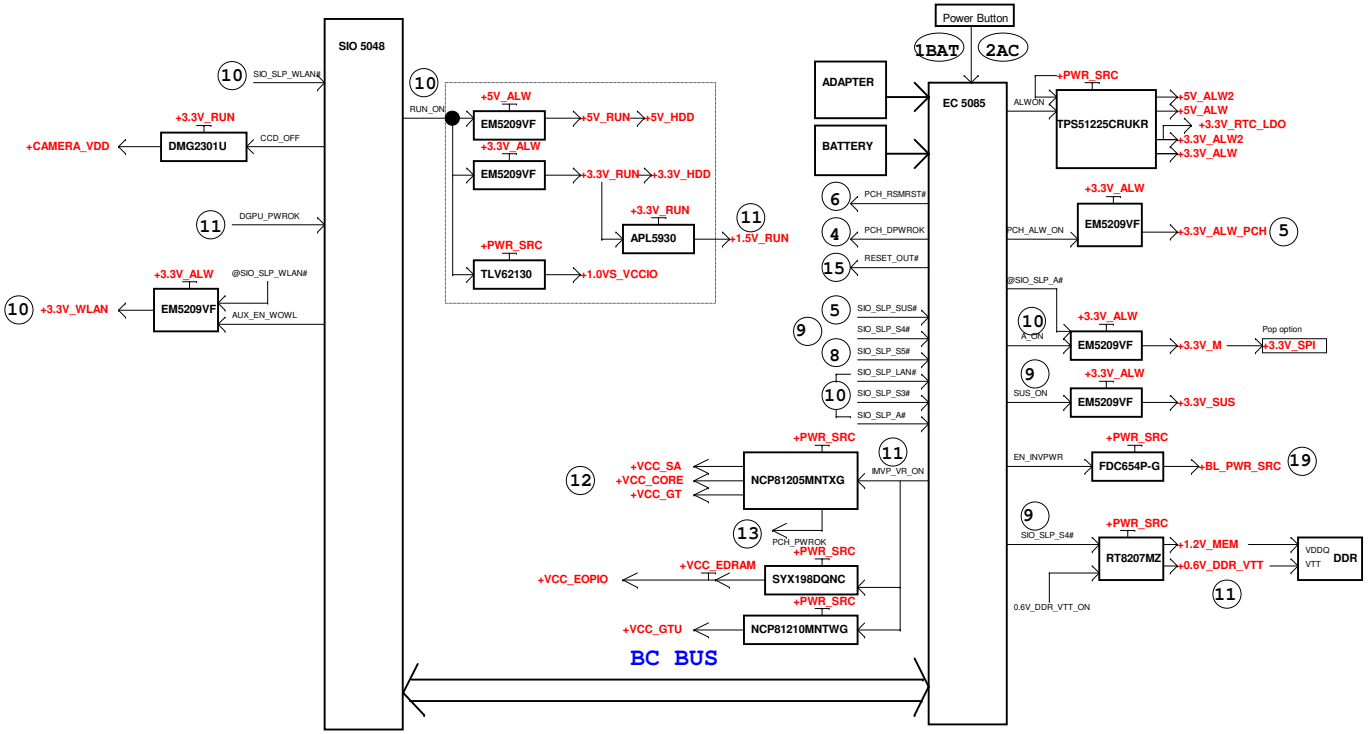
Timing Diagram for S5 to S0 mode





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Power Sequence

Document Number: LA-E321P

Rev: 1.0

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	39	HW	2016/06/07	Compal	System cannot detect USH/B	Change RZ72 to 0ohm_short for load SW power to turn on +3.3V_CV2, +3.3V_FPM	0.2(X01)
2	33	HW	2016/06/07	Compal	Mini DP can not display	Change HD3SS214 operate mode change from standy mode to normal mode, pop R107, depop R108	0.2(X01)
~~3~~	~~39~~	~~HW~~	~~2016/06/07~~	~~Compal~~	~~Reverse for version B TPM IC design~~	~~Reverse RZ124, contact from SIO_SLP_S0# to TPM_LPM#~~	~~0.2(X01)~~
4	14, 17	HW	2016/06/07	Compal	Change 330uf cap placement	Pop CD14, de-pop CD61	0.2(X01)
6	48	HW	2016/06/08	Compal	For press power button over 20 sec,EC can sent RTCRST_ON to reset RTC	add R808,R809,Q371,and connect R808.1,Q371.2 to U51.B8	0.2(X01)
7	38	HW	2016/06/08	Compal	C481 package change	Change from 0603 to 0402	0.2(X01)
8	19	HW	2016/06/28	Compal	TBT_CIO_PLUG_EVENT# pull up change from +3.3V_ALW to +3.3V_ALW_PCH for power leakage	TBT_CIO_PLUG_EVENT# add RH366 pull to +3.3V_ALW_PCH, de-pop RH341	0.2(X01)
9	46	HW	2016/06/28	Compal	To prevent damage with Miramar I/O board	Rotate JIO1 180 degree	0.2(X01)
10	48	HW	2016/07/01	Compal	Board ID resistor value change	R875 change from 240k to 130k	0.2(X01)
11	48	HW	2016/07/01	Compal	reserve for DPWROK sequence	Align BR team, add UE7, CE10, RE348, CE5	0.2(X01)
12	39	HW	2016/07/01	Compal	USH_PWR_STATE voltage level keep high	change RZ10 from 1M to 100Kohm,depop DZ3,pop RZ76	0.2(X01)
13	40	HW	2016/07/04	Compal	leverage X8-reserved 0 ohm on COEX1~3 betweem WWAN and WLAN	Add reserve RZ125, RZ126, RZ127	0.2(X01)
14	47	HW	2016/07/04	Compal	leverage X8-TBT_RESET_N_EC add R886 PD 100Kohm	Add R886	0.2(X01)
15	39	HW	2016/07/04	Compal	TPM leverage X8	change RZ111 from 0ohm-short to 0ohm,depop RZ111,RZ112,RZ82,QZ2 ,pop RZ124	0.2(X01)
16	25	RF	2016/07/05	Compal	5.76G noise mitigation	RH363 and RH362 change from 0ohm to BLM15GA750SN1	0.2(X01)
17	33	HW	2016/07/05	Compal	U636 HD3SS214ZQER footprint incorrect	Swap U636 pin E1, E2	0.2(X01)
18	7	HW	2016/08/08	Compal	Design Guide	RC316 change from 1.5k to 3k	0.3(X02)
19	50	HW	2016/08/08	Compal	Touchpad riseing time fail	Change RZ114, RZ115 from 4.7k to 2.2k	0.3(X02)
20	21	HW	2016/08/08	Compal	Crystal EA test	CH4, CH5 change from 18pf to 15pf	0.3(X02)
21	18, 21	HW	2016/08/25	Compal	add CLK_REQ# isolation for N17P/N17E MXM card	change QH3 to Q6 and connect Q6.1 to CLKREQ_PEG#0,Q6.2 to DGPU_PWROK, Q6.3 to MXM_CLK_REQ#,depop R1978	0.3(X02)
~~22~~	~~31~~	~~HW~~	~~2016/08/25~~	~~Compal~~	~~Dock port1 DP test~~	~~Depop R99~~	~~0.3(X02)~~
23	46	HW	2016/08/25	Compal	support USB3.0 wake in S3	JIO1.37 change from +3.3V_RUN to +3.3V_ALW	0.3(X02)
24	18,47	HW	2016/08/25	Compal	support UMA sku	add @R1973 between UH1.T45 and U46.B59,depop R803,pop R800	0.3(X02)
25	39	HW	2016/08/25	Compal	add USH protect circuit for EC	add DZ4,@DZ5,@DZ6,DZ7,@DZ8,RZ128,@RZ129,UZ32,@RZ130,RZ131~RZ134,CZ98~CZ102,remove @RZ70,@RZ73,change JUSH1.25 to NC,JUSH1.26 to +VCC_FPM	0.3(X02)
26	35	HW	2016/08/30	Compal	CRT impendance match to 75ohm on R,G,B	add PD 150ohm (RV128,RV129,RV130) on RED_CONVER, GREEN_CONVER, BLUE_CONVER	0.3(X02)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
27	45	HW	2016/08/31	Compal	add Docking protect circuit for EC	Add D101,@R210	0.3(X02)
28	48	HW	2016/08/31	Compal	Board ID resistor value change	R875 change from 130k to 33k	0.3(X02)
29	38	HW	2016/09/05	compal	EMI EA	change C485 from 150pF to 10pF	0.3(X02)
30	39	HW	2016/09/08	compal	leverage X8-change TPM MPN to NPCT650VB2YX	change U637 from SA00008EL70 to SA00008EL80	0.3(X02)
31	39	HW	2016/09/08	compal	remove reserve component on USH	remove DZ3,change RZ76 to 0ohm_short	0.3(X02)
32	11.12	HW	2016/09/08	compal	reduce ripple of +1.0V_VCCST,+1.0V_VCCSTG, +1.0V_PRIMP	change CZ82, CZ88, CC195,CC186,CZ63,CZ90 to 10uf_0402	0.3(X02)
33	12,19	HW	2016/09/12	INTEL	PDG1.0	change RH73 from 43ohm to 13ohm,CC187,CC188,C189 from 22uF to 10uF	0.3(X02)
34	33	HW	2016/10/14	compal	AMD MXM CARD,display icon SHOW 3 Display when plug 1monitor	Add R153,R154 PD on MXM_DPB_HPD,PCH_DPD_HPD	1.0(A00)
35	48	HW	2016/10/14	compal	Board ID change to A00	change R875 from 33Kohm to 4.3Kohm	1.0(A00)
36	48	HW	2016/10/14	compal	advance BTB connector connection	change JIO1 from QT50A01-29100-7H to QT50A01-29200-7H,JIO2 from QT50A61-29100-7H to QT50A61-29200-7H	1.0(A00)
37	18	HW	2016/10/14	compal	reserve for NV request	Add @R155 between U17.1 and U17.2,add R156 between U17.1 and ACAV_IN	1.0(A00)
38	31	HW	2016/10/14	Compal	Dock port1 DP test	Pop R99	1.0(A00)

Version Change List (P. I. R. List)Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	52 57	POWER	4/29	COMPAL	change PBAT_SMBCLK,CHARGER_SMBCLK PBAT_SMBDAT,CHARGER_SMBDAT net name for HW request	PBAT_SMBCLK,CHARGER_SMBCLK change to CHARGER_PBAT_SMBCLK; PBAT_SMBDAT,CHARGER_SMBDAT change to CHARGER_PBAT_SMBDAT	Rev.01
2	52	POWER	5/4	COMPAL	for EMC request , pop and change PC15 from 0.1U to 1000P	change PC15 from 0.1U(SE042104K80) to 1000P(SE074102K80)	Rev.01
3	52	POWER	5/4	COMPAL	for EMC request , pop and change PC15 from 0.1U to 1000P	change PC15 from 0.1U(SE042104K80) to 1000P(SE074102K80)	Rev.01
4	56	POWER	5/12	COMPAL	for DDR4 2400 current request, change output choke to support	PL400 change from SH00000YG00(S COIL 1UH +-30% 2.8A 4X4X2 FERRITE) to SH00000IW00 (S COIL 1UH +-20% PCMB042T-1R0MS 4.5A)	Rev.01
5	54	POWER	7/1	COMPAL	for RAM issue , HW request to change from 1.2V to 1.235V	change PR204 from 12K(SD034120280) to 13K(SD034130280)	Rev.02
6	64 65 67	POWER	7/1	COMPAL	For FAE check,pop Dr.MOS EMC part and change bootstrap resister to reduce the ringing of SW node	change PR1201 PR1202 PR1208 PR1401 PR1402 PR1701 from SD013200B80 (S RES 1/10W 2 +-5% 0603) to SD00000YH00 (S RES 1/10W 3.9 +-5% 0603)	Rev.02
7	64 65 67	POWER	7/11	COMPAL	For FAE check, change snubber resister to reduce the ringing of SW node	change PR1206 PR1207 PR12011 PR1406 PR1407 PR1702 from SD001200B80 (S RES 1/4W 2 +-5% 1206) to SD011100B80 (S RES 1/4W 1 +-5% 1206)	Rev.02
8	59	POWER	7/22	COMPAL	For Temp voltage test , +DC_IN setting for ACAVIN_NB need less than 17.55V , so change PR737 to achieve	change PR737 from SD034665380(S RES 1/16W 665K +-1% 0402) to SD034634380(S RES 1/16W 634K +-1% 0402)	Rev.02
9	53	POWER	9/2	COMPAL	With compal rule , need to use even part to back to back for acoustic noise improvement so add 3.3V/5V input MLCC to achieve	change PC101,PC102 from SE00000QK00(S CER CAP 10U 25V K X5R 0805 H1.25) to SE000006R80(S CER CAP 4.7U 25V K X5R 0805 H1.25) and add PC122,PC123 SE000006R80(S CER CAP 4.7U 25V K X5R 0805 H1.25)	Rev.03

Version Change List (P. I. R. List)Page 2

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
10	63	POWER	9/2	COMPAL	Change SW to controller resisters size from 0402 to 0603 to improve initial voltage for FAE suggest	change PR1143,PR1146,PR1148 from 82.5K 0402(SD000002780) to 82.5K 0603(SD014825280) and PR1145,PR1147 from 56.2K 0402(SD000001580) to 56.2K 0603(SD014562280)	Rev.03
11	60 63	POWER	9/2	COMPAL	To improve HW side +1.0V_VCCST ,+1.0V_VCCSTG and +1.0V_VCCSFR output ripple , change 1.0V_PRIM choke and VCCST MLCC	Change PL800 from SH00000Z200 (S COIL 1UH +-20% 6.6A 5X5X3 MOLDING) to SH00000R810 (S COIL 2.2UH +-20% PCMB053T-2R2MS 5.5A) and PC1101 from SE00000G880 (S CER CAP 0.1U 25V K X5R 0402) to SE00000UD00 (S CER CAP 10U 6.3V M X5R 0402)	Rev.03
12	63	POWER	9/12	COMPAL	For SA Loadline and Iout improvement , modify parameter of VR ciruit from FAE suggestion	Pop PC1140 and change from 1000P(SE074102K80) to 2200P(SE074222K80); change PR1107 from short pad to 1K(SD028100180); change PR1109 from 1.43K(SD034143180) to 1.58K(SD00000SJ80); change PR1112 from 30K(SD034300280) to 28K(SD034280280)	Rev.03
13	63	POWER	9/14	COMPAL	For IA,GT Loadline and Iout improvement , modify parameter of VR ciruit from FAE suggestion	IA part Change PR1143,PR1146,PR1148 from 82.5K(SD014825280) to 88.7K(SD014887280); change PR1132 from 24.3K to 26.7K(SD034267280); GT part Change PR1145,PR1147 from 56.2K(SD014562280) to 61.9K(SD014619280); change PR1135 from 22.6K to 24.9K(SD034249280)	Rev.03
14	53 59 60	POWER	9/20	COMPAL	For Dell request , 3.3V/5V HS and LS MOS should be used with the same vendor	High side MOS Change PQ100,PQ101,PQ800 from SB00000IA00 (S TR SIS412DN-T1-GE3 1N POWERPAK1212-8) to SB00000H800 (S TR AON7408L 1N DFN); Low side MOS Change PQ102,PQ103,PQ705 from SB00000N800 (S TR FDMC7692S 1N MLP) to SB000010U00 (S TR AON7752 1N DFN3X3EP)	Rev.03
15	53	POWER	9/26	COMPAL	For HW request , need to increase 5V output voltage from 5V to 5.08V to reduce PD output voltage drop	Change PR101 from SD034150280 (S RES 1/16W 15K +-1% 0402) to SD034154280 (S RES 1/16W 15.4K +-1% 0402)	Rev.03
16	63	POWER	9/26	COMPAL	To meet intel SPEC for GT voltage , need to modify parameter of VR circuit	Change PR1127 from SD034100180 (S RES 1/16W 1K +-1% 0402) to SD034137180 (S RES 1/16W 1.37K +-1% 0402)	Rev.03
17	53	POWER	11/11	COMPAL	For type C test , change FB resisters to rise output voltage from 5V to 5.156V	Change PR101 from SD034158280(S RES 1/16W 15.8K +-1% 0402) to SD034154280(S RES 1/16W 15.4K +-1% 0402) change PR104 from SD028102280(S RES 1/16W 10.2K +-1% 0402) to SD034976180(S RES 1/16W 9.76K +-1% 0402)	Rev.10
18	54	POWER	11/11	COMPAL	For 1.2V damage issue , upgrade high side MOS to improve	Change PQ201 from SB00000K300(S TR SIR472DP-T1-GE3 1N POWERPAK SO8) to SB00000WY00(S TR SIRA14DP-T1-GE3 1N POWERPAK SO8)	Rev.10
19	54	POWER	11/16	COMPAL	For 1.2V damage issue , change HS/LS MOS from Vishay to Magnachop and 1.235V change back to 1.2V	Change PQ201 from SB00000WY00(S TR SIRA14DP-T1-GE3 1N POWERPAK SO8)to SB00001GP00(S TR AON6380 1N DFN5X6-8): change PQ202 from SB00000WX00(S TR SIRA06DP-T1-GE3 1N POWERPAKSO-8) to SB00001GK00(S TR AON6314 1N DFN5X6-8) change PR204 from SD034130280(S RES 1/16W 13K +-1% 0402) to SD034120280S RES 1/16W 12K +-1% 0402)	Rev.10