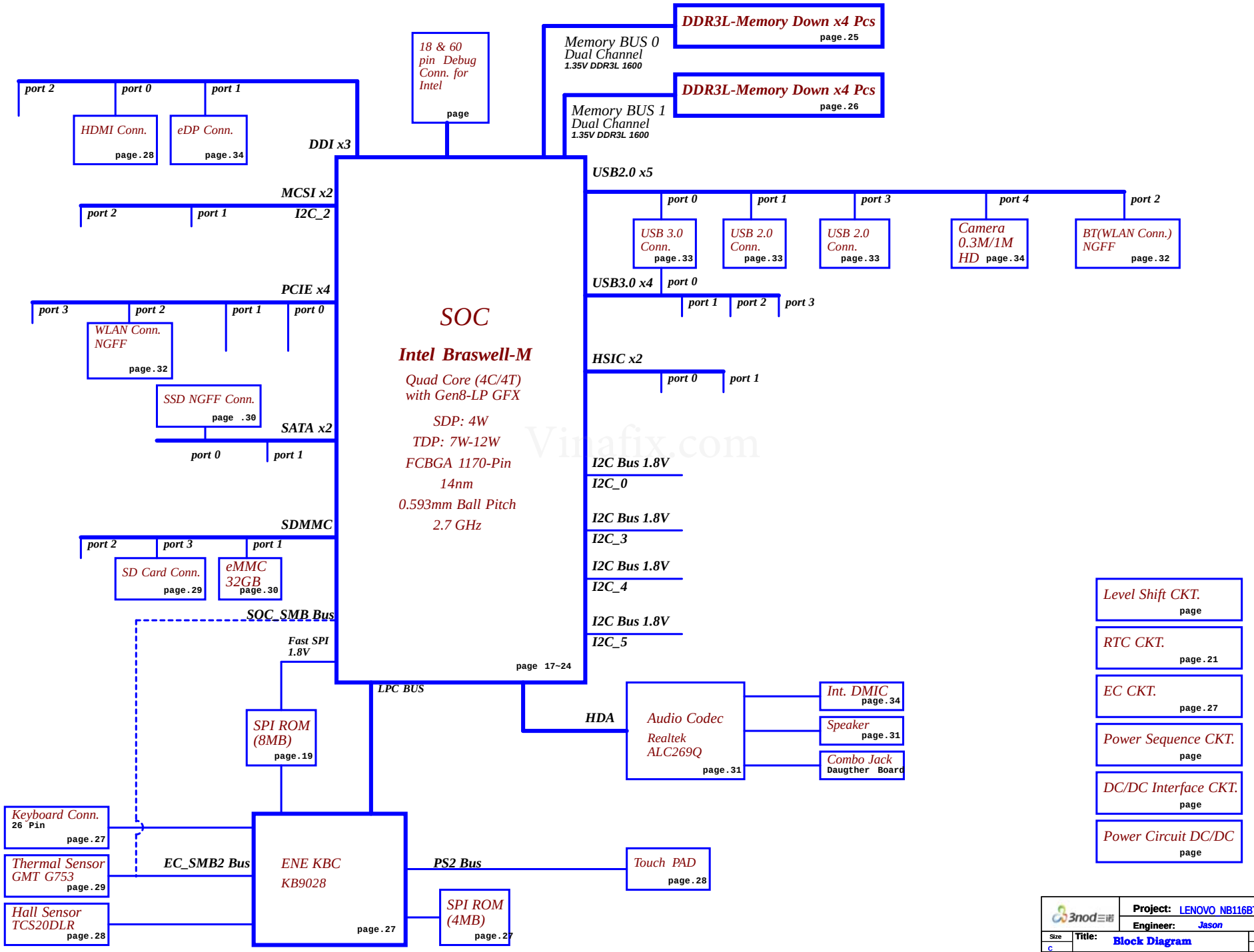
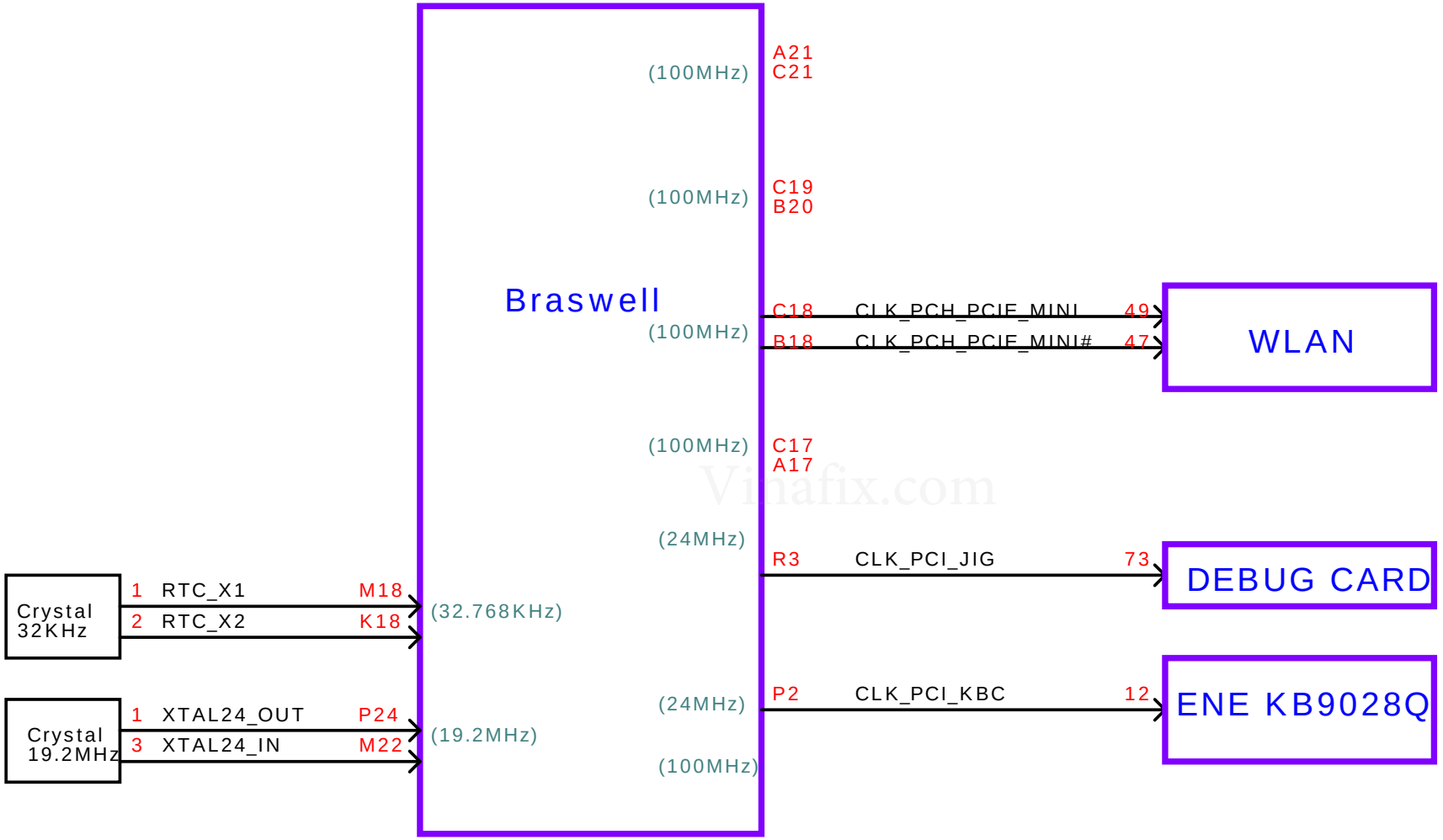
Aristotle 14"

3nod三诺	Project: LENOVO_NB116BT	
	Engineer: Jason	
Size: B	Title: Cover	Rev: V01
Date: Saturday, August 22, 2015	Sheet 1 of 37	

Block Diagram



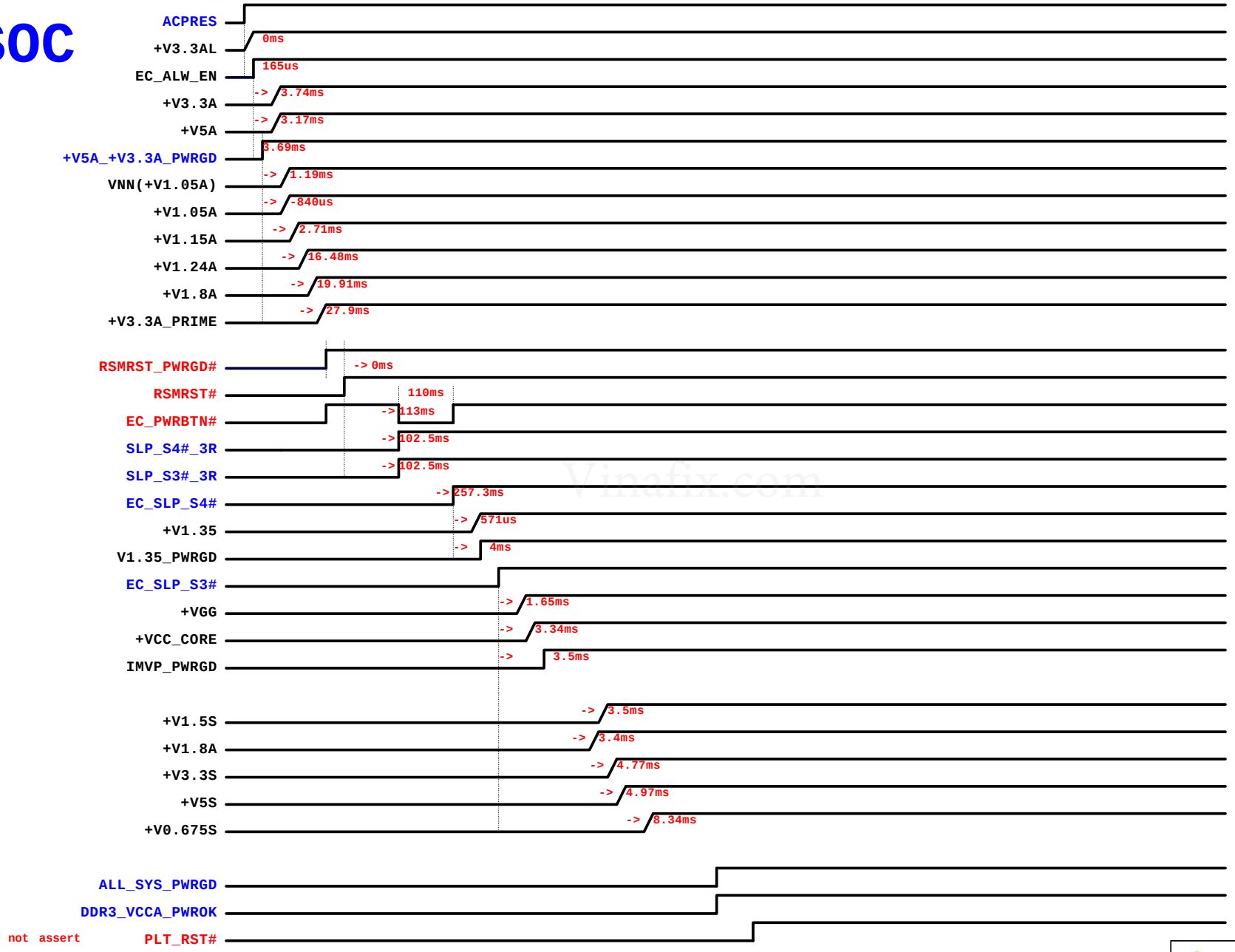
3nod三诺	Project: LENOVO NB116BT	
	Engineer: Jason	
Size: C	Title: Block Diagram	Rev: V01
Date: Saturday, August 22, 2015	Sheet 2 of 37	



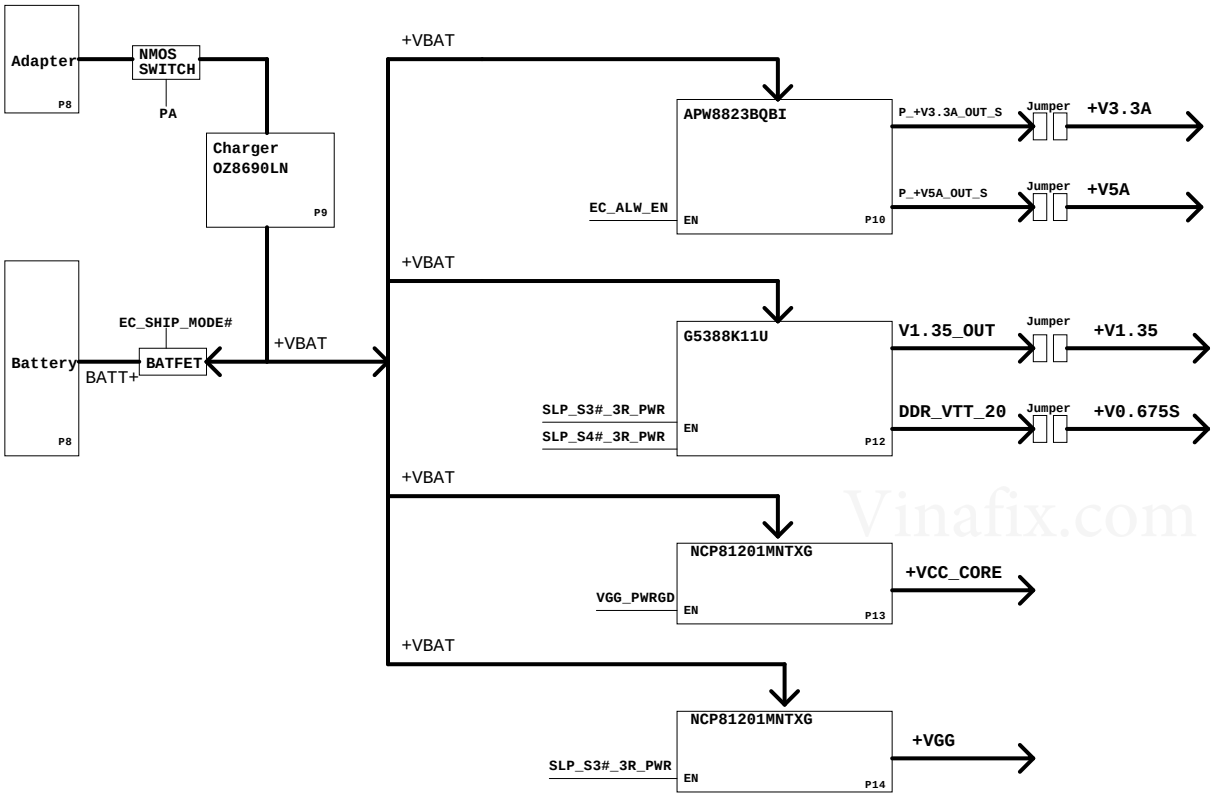
3nod三诺	Project: LENOVO_NB116BT	
	Engineer: Jason	
Size: Custom	Title: CLOCK MAP	Rev: V01
Date: Saturday, August 22, 2015	Sheet 3 of 37	

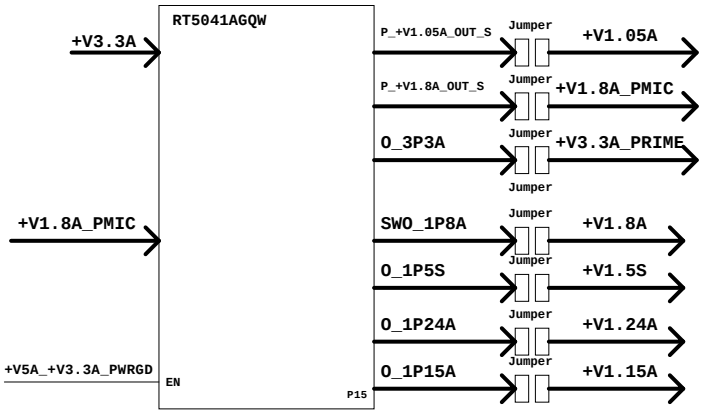
G3->S0

SOC

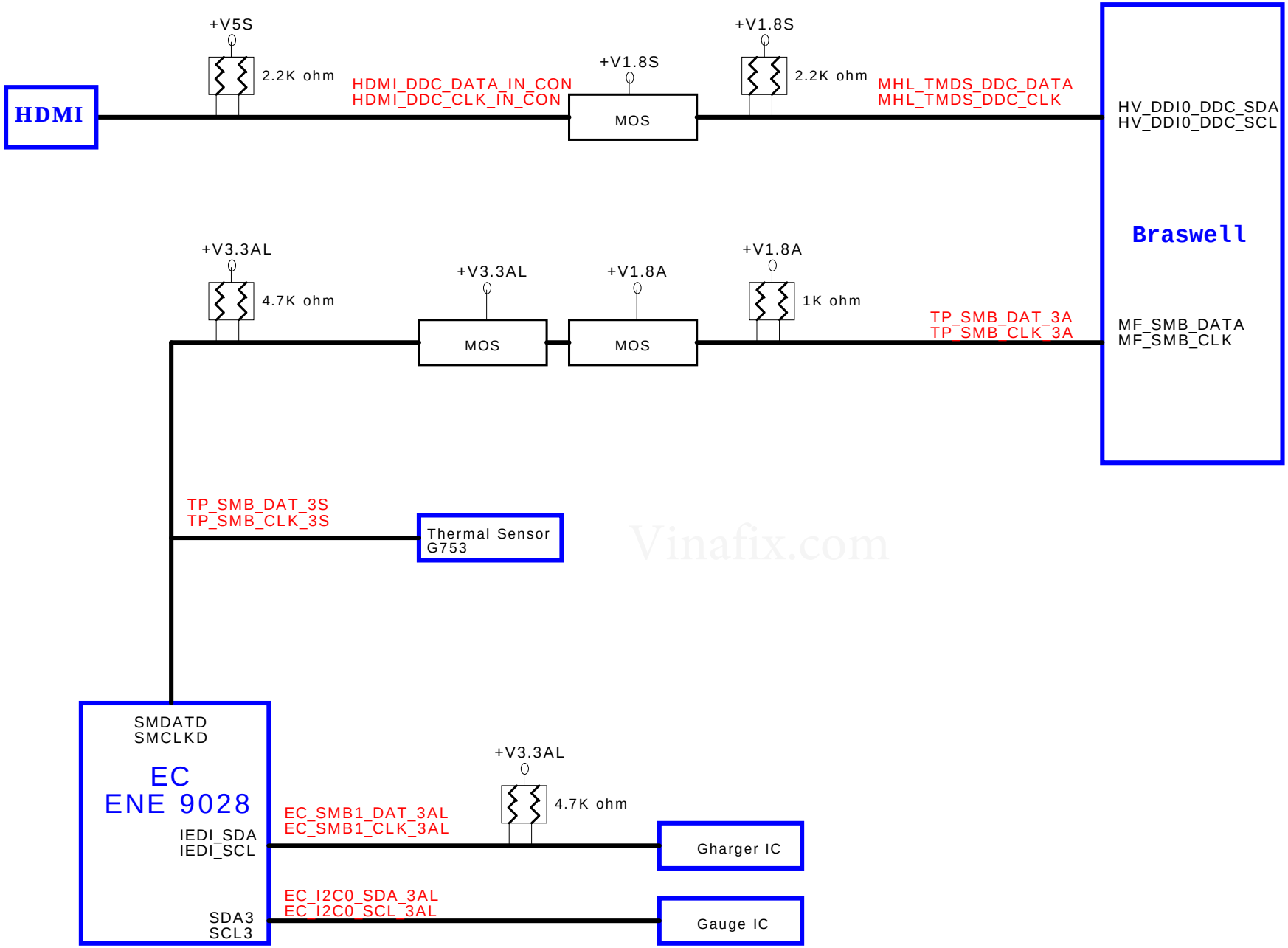


3nod三诺	Project: LENOVO_NB116BT	
	Engineer: Jason	
Size: Custom	Title: POWER SEQUENCY DIAGRAM	Rev: V01
Date: Saturday, August 22, 2015	Sheet 4 of 37	

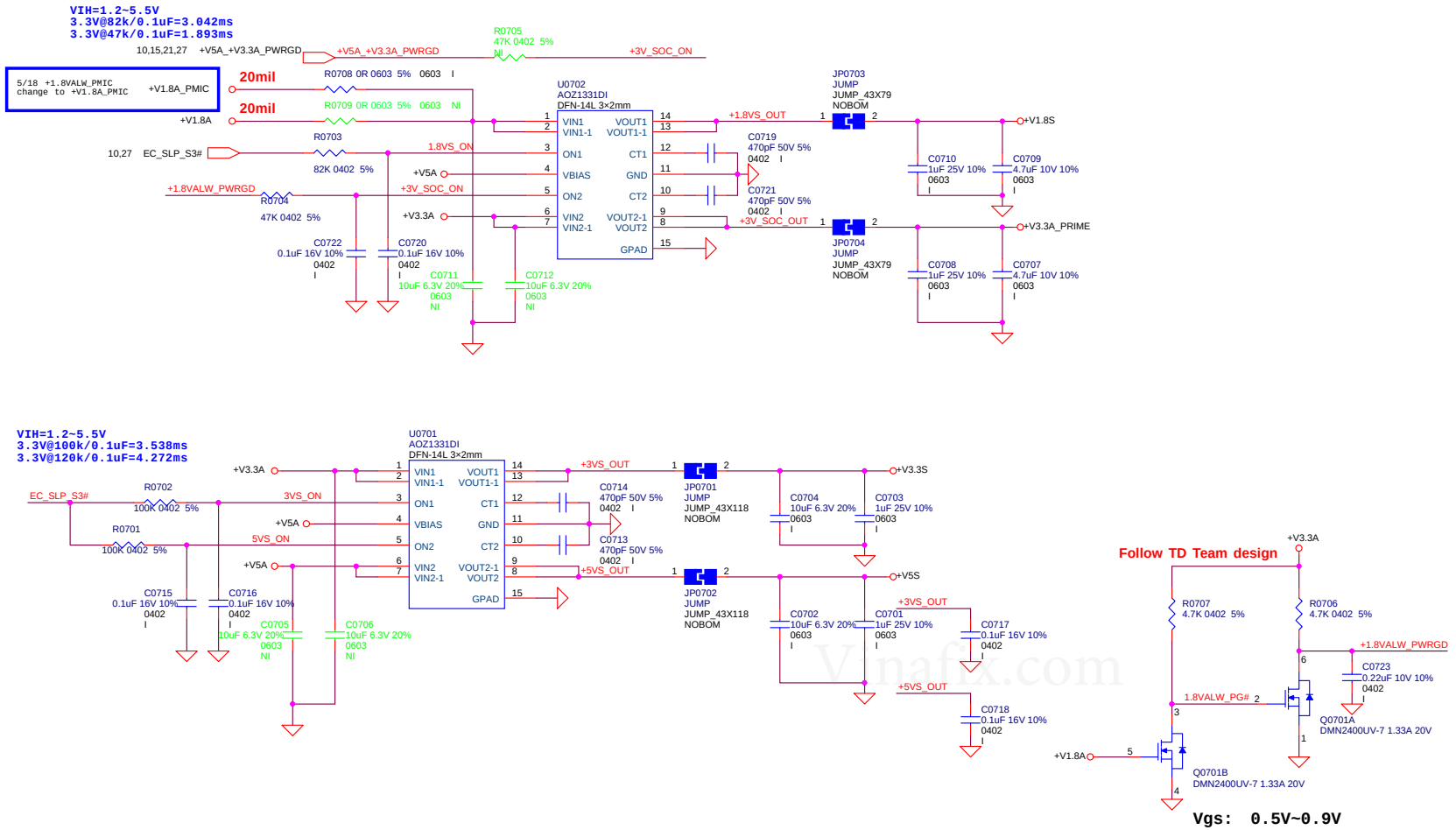




3nod三诺	Project:	LENOVO_NB116BT
	Engineer:	Jason
Size: Custom	Title:	POWER MAP
		Rev: V01
Date: Saturday, August 22, 2015	Sheet 5 of 37	



3nod三诺	Project: LENOVO NB116BT	
	Engineer: Jason	
Size: Custom	Title: SMBUS MAP	Rev: V01
Date: Saturday, August 22, 2015	Sheet 6 of 37	



+V5A +V5A 10,12,13,14,15,16,22,28,33
+V5S +V5S 28,29,31
+V3.3A +V3.3A 10,13,14,15,16,18,21,22,27,28,30,32
+V3.3A_PRIME +V3.3A_PRIME 15,23
+V3.3S +V3.3S 16,21,22,23,27,28,29,30,31,34
+V1.8A +V1.8A 15,17,19,20,21,22,23,27,28,29,30,32,34
+V1.8A_PMIC +V1.8A_PMIC 15
+V1.8S +V1.8S 17,19,23,29,30,34

3nod三诺	Project:	LENOVO_NB116BT	
	Engineer:	Jason	
Size	Title:		Rev
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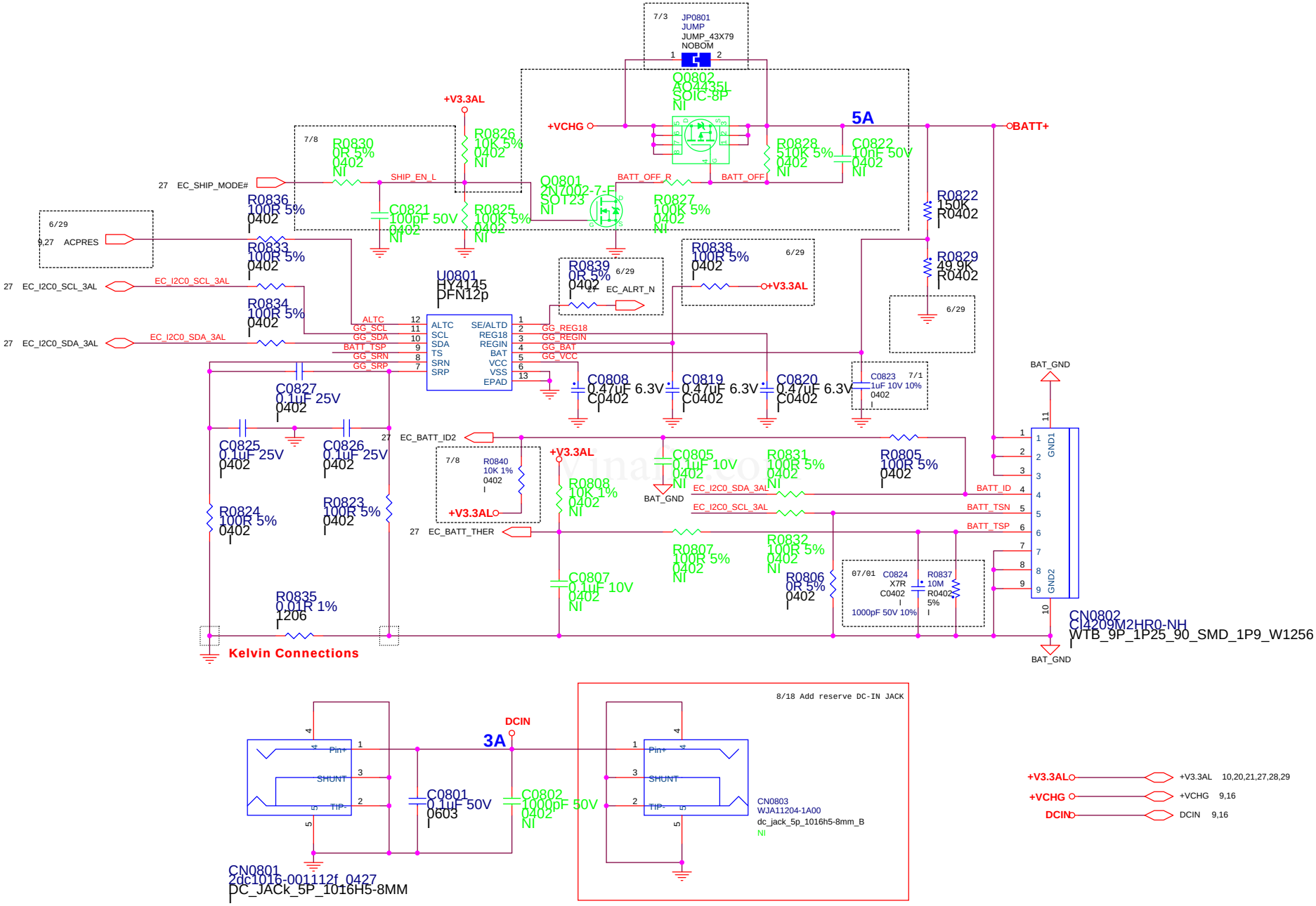
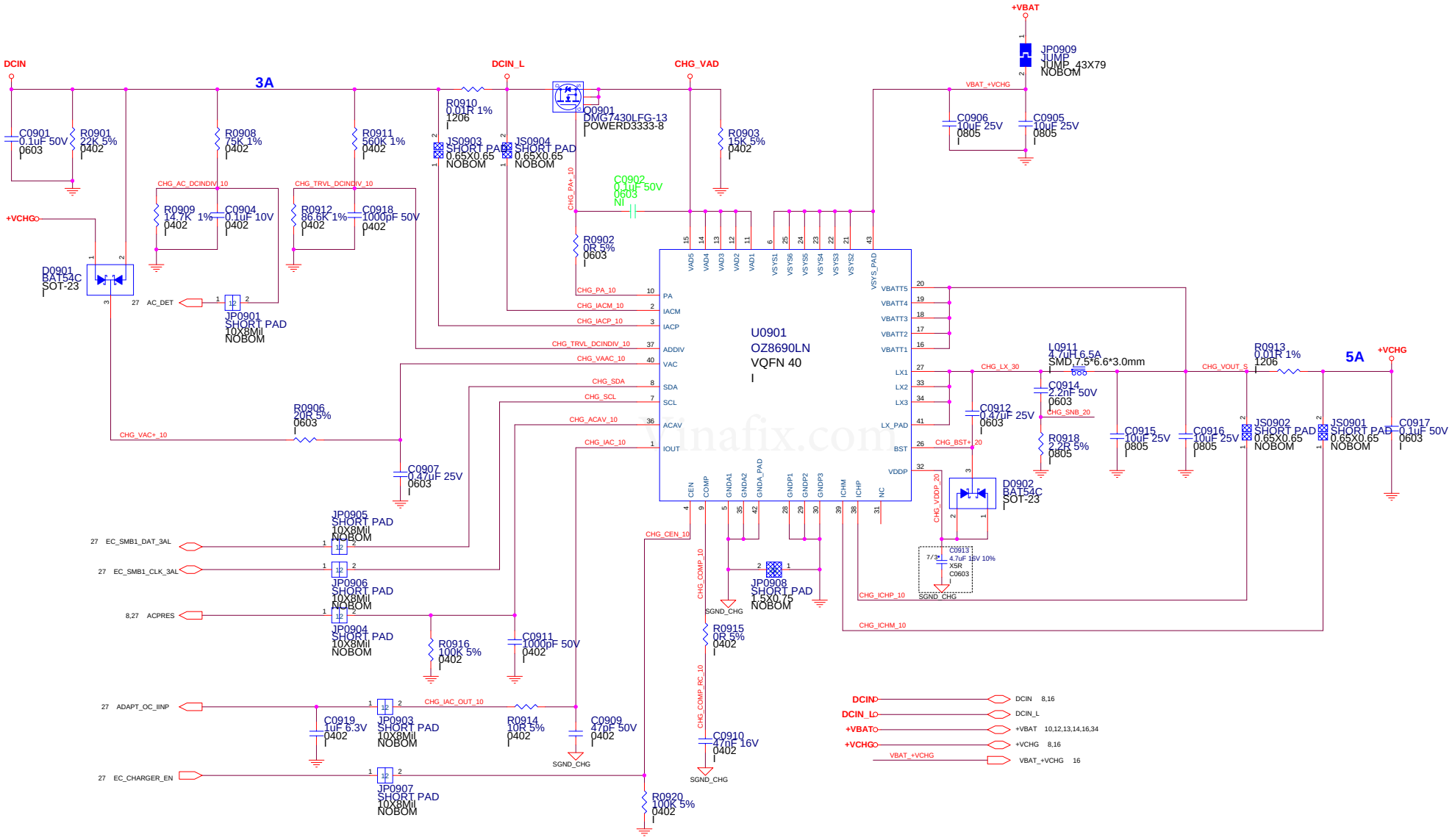
08: DC-IN & BATTERY CONNECTOR



3nod三诺	Project: LENOVO_NB116BT	
	Engineer: Frank	
Size: Custom	Title: DCIN / BATTERY CONN	Rev: V01
Date: Saturday, August 22, 2015	Sheet 8 of 37	

09: BATTERY CHARGER



3nod三诺	Project: LENOVO_NB116BT	
	Engineer: Frank	
Size: Custom	Title: Charger	Rev: V01
Date: Saturday, August 22, 2015	Sheet 9 of 37	

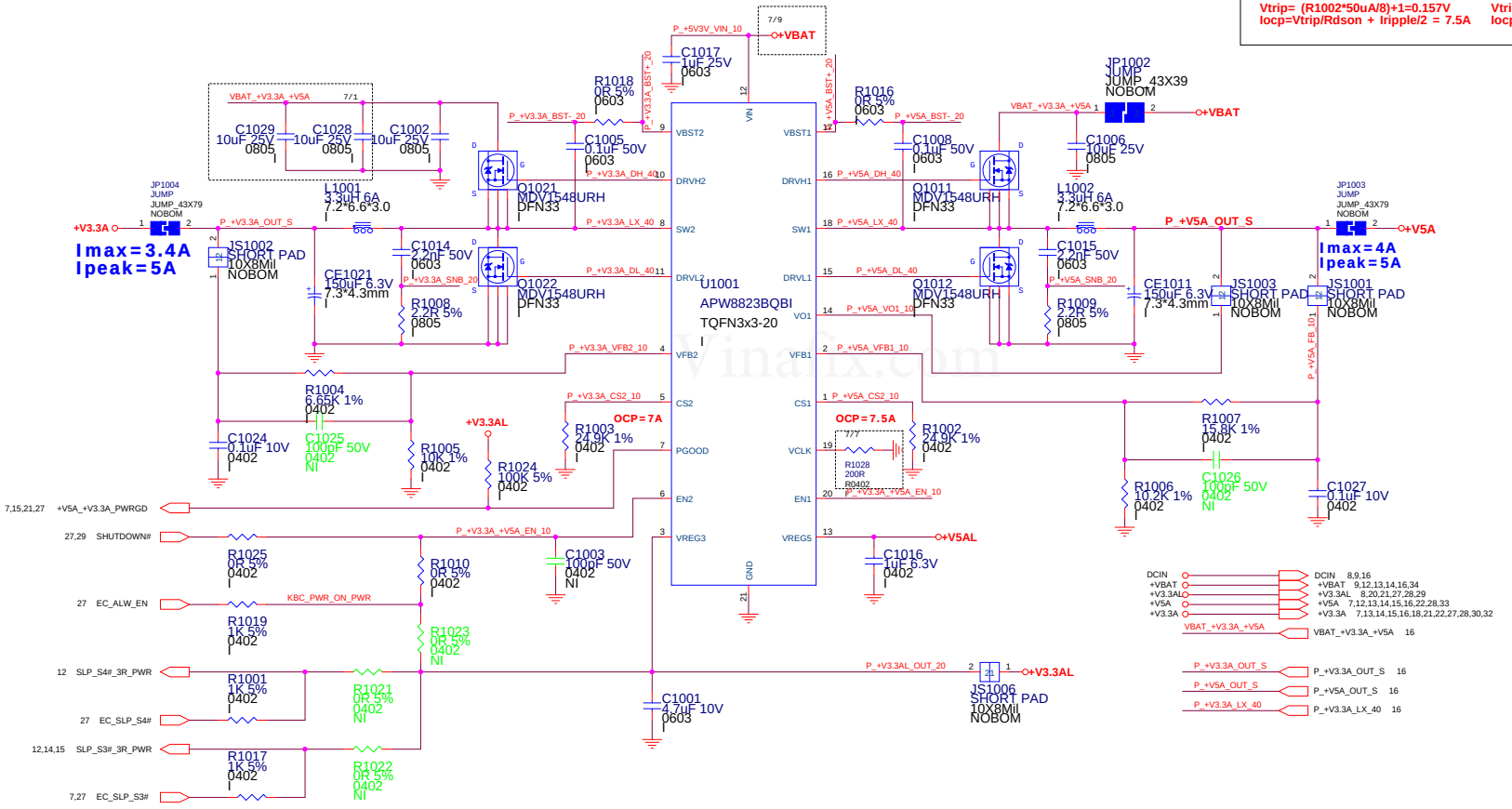
10: +V5A / +V3.3A POWER SUPPLY

+V5A:

1. **I/P Current:**
   Iin=Vo*Io/(0.75*Vin)=3.16A
2. **Ripple Current:**
   Irip=3.72A
3. **Ripple Voltage:**
   ESR/1=15mohm
   Vrip=55.8mV
4. **Inductor Spec:**
   Isat=9.3A
   Idc=6.3A
   DCR=30mohm
5. **MOSFET Spec:**
   H/L-side MOSFET: MDV1548URH
   Rds(ON)=27.8mohm (Vgs=4.5 V)
   I cont = 8.6A (T =25)
6. **Frequency:**
   F=400KHz
7. **OCP:**
   Set = R1002 to 24.9K
   Vtrip= (R1002*50uA/8)+1=0.157V
   Iocp=Vtrip/Rdson + Iripple/2 = 7.5A

+V3.3A:

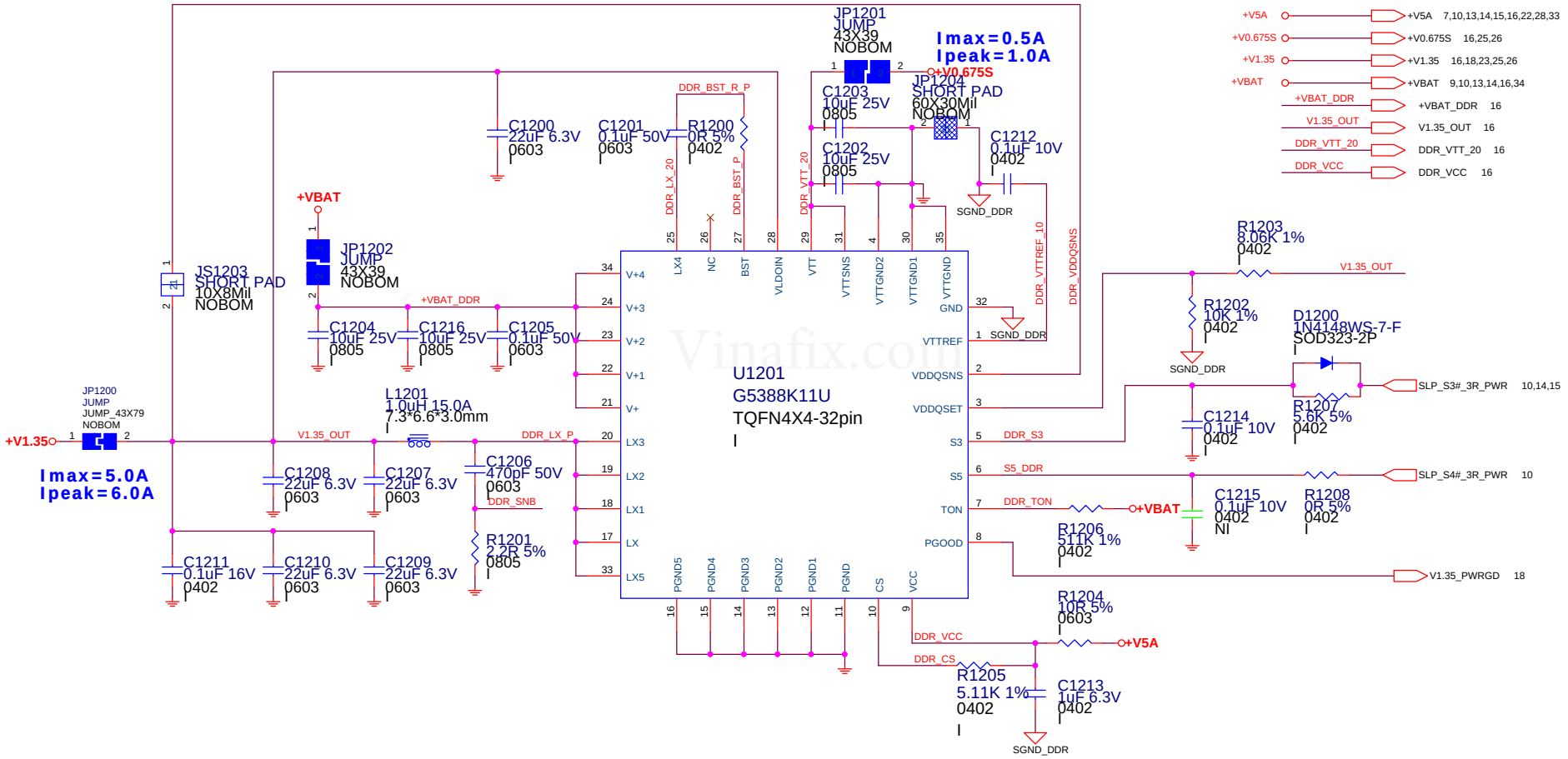
1. **I/P Current:**
   Iin=Vo*Io/(0.75*Vin)=1.22A
2. **Ripple Current:**
   Irip=2.36A
3. **Ripple Voltage:**
   ESR/1=15mohm
   Vrip=35.4mV
4. **Inductor Spec:**
   Isat=9.3A
   Idc=6.3A
   DCR=30mohm
5. **MOSFET Spec:**
   H/L-side MOSFET: MDV1548URH
   Rds(ON)=27.8mohm (Vgs=4.5 V)
   I cont = 8.6A (T =25)
6. **Frequency:**
   F=475KHz
7. **OCP:**
   Set = R1003 to 24.9K
   Vtrip= (R1003*50uA/8)+1=0.157V
   Iocp=Vtrip/Rdson + Iripple/2 = 7.0A



Project:	LENOVO NB116BT
Engineer:	Frank
Size: C	Title: System Power
Rev: V01	
Date: Saturday, August 22, 2015	Sheet 10 of 37

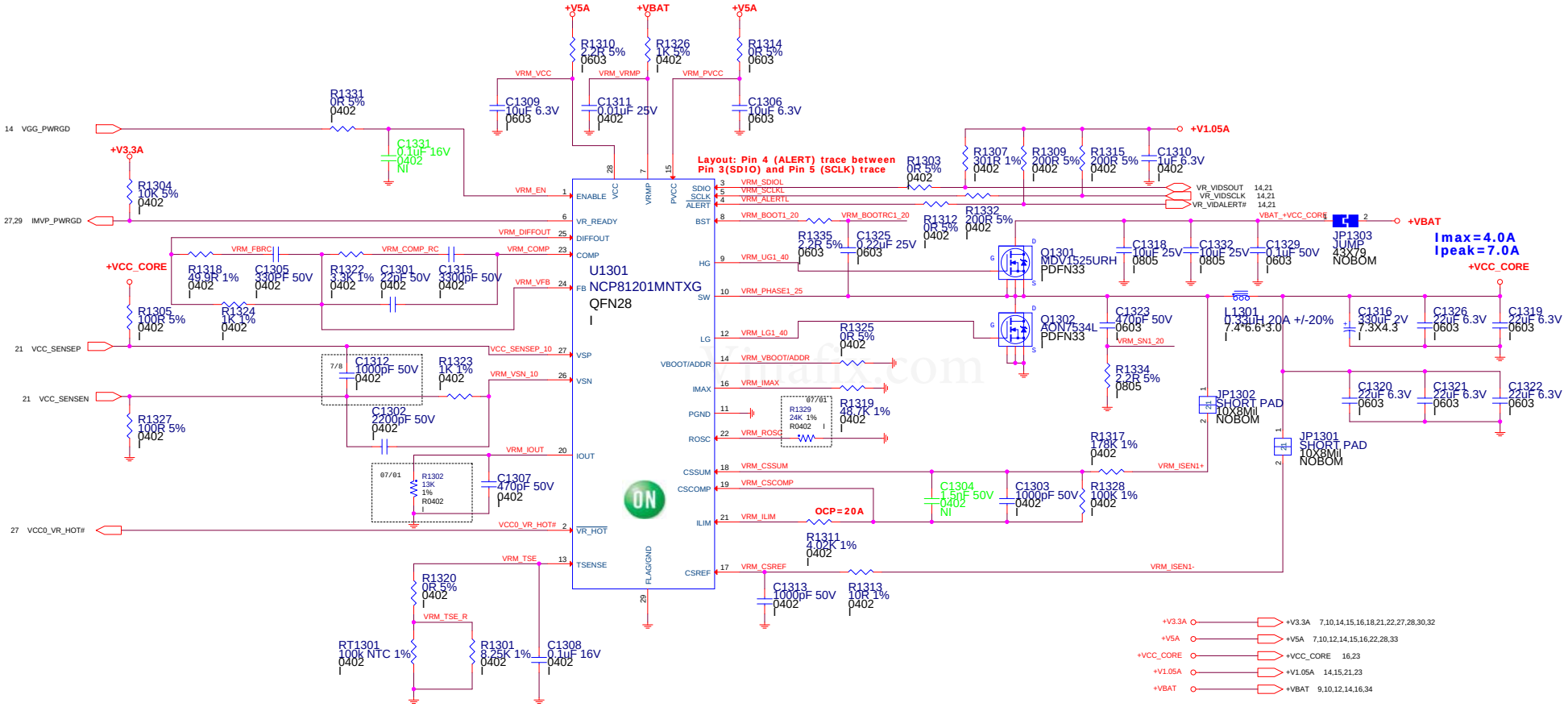
3nod三诺	Project: LENOVO_NB116BT	
	Engineer: Jason	
Size: Custom	Title: Cover	Rev: V01
Date: Saturday, August 22, 2015	Sheet 11 of 37	

12: DDR POWER SUPPLY



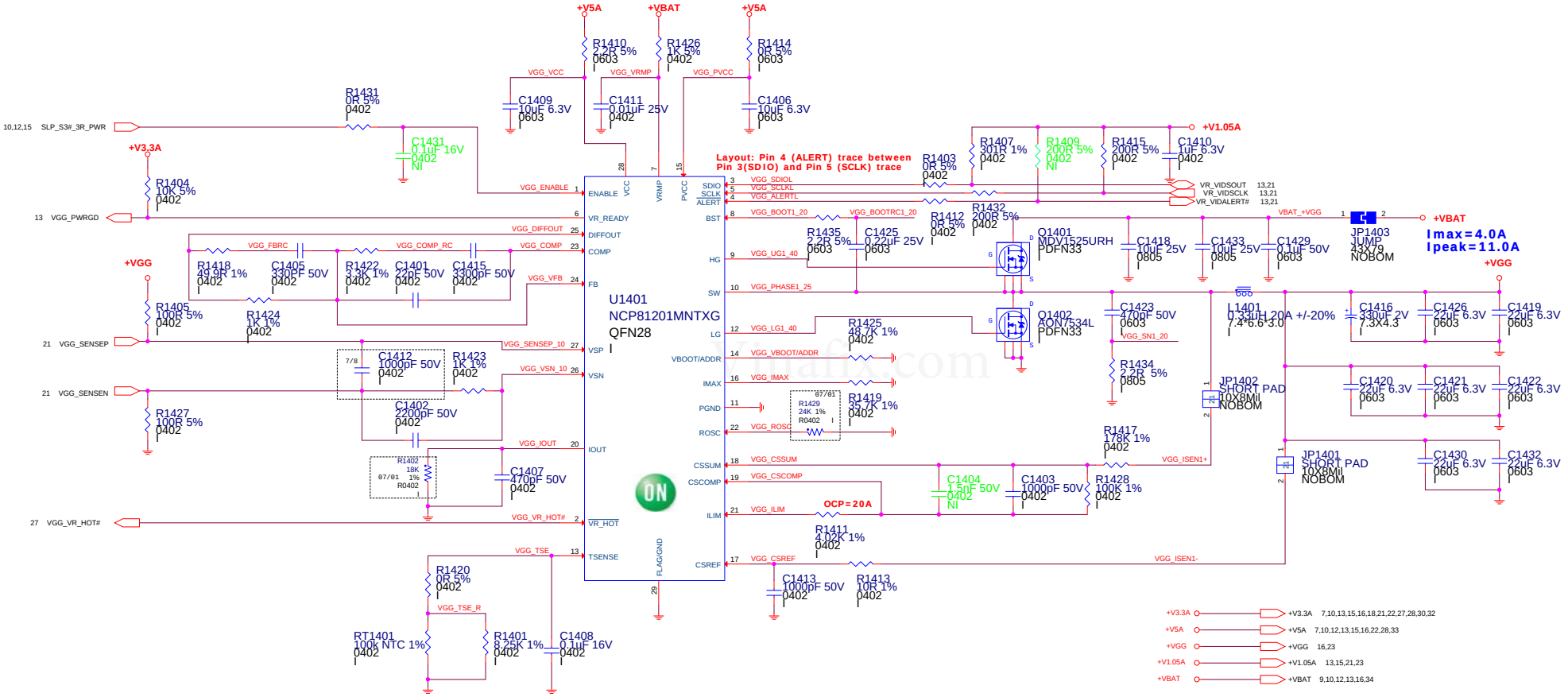
3nod三诺	Project: LENOVO_NB116BT	
	Engineer: Frank	
Size: Custom	Title: DDR Power	Rev: V01
Date: Saturday, August 22, 2015	Sheet 12 of 37	

13: VCC0&VCC1 VCORE POWER SUPPLY



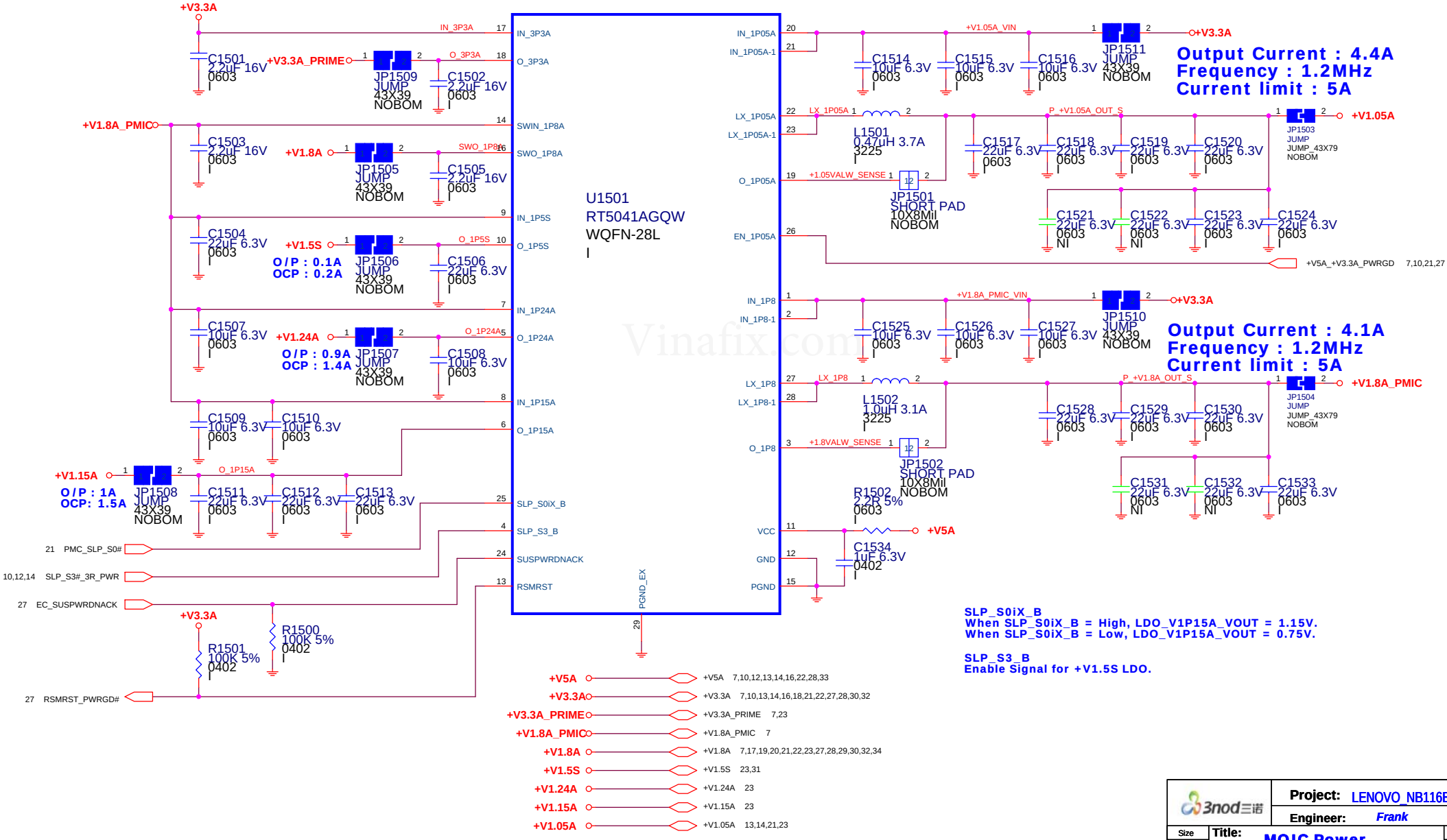
3nod三诺	Project: LENOVO NB116BT	
	Engineer: Frank	
Size: C	Title: VCORE Power	Rev: V01
Date: Saturday, August 22, 2015	Sheet 13 of 37	

14: +VGG POWER SUPPLY

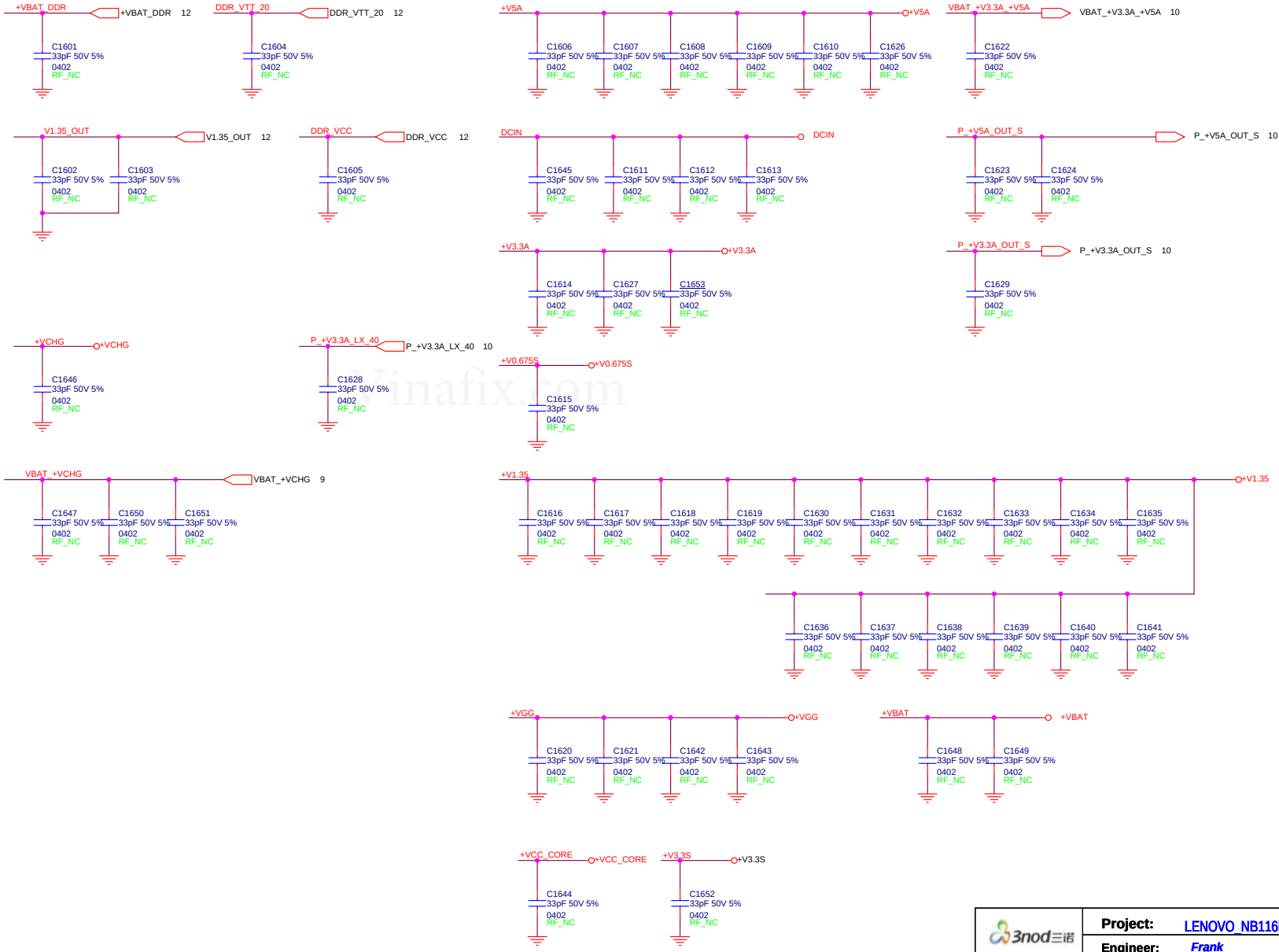


3nod三诺	Project: LENOVO NB116BT	
	Engineer: Frank	
Size: C	Title: +VGG Power	Rev: V01
Date: Saturday, August 22, 2015	Sheet 14 of 37	

15: MOIC POWER SUPPLY



16 : RF Solution

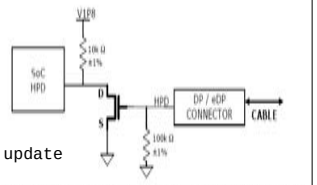


3nod三诺	Project:	LENOVO_NB116BT
	Engineer:	Frank
Size: Custom	Title:	RF Solution
	Rev:	V01
Date: Saturday, August 22, 2015	Sheet 16 of 37	

3.4.4 DDI Disable Guidelines

Pin Name	System Pull-up/ Pull-down	Schematics Notes	✓
DDIx_TXP[3:0] DDIx_TXN[3:0]		No Connect	
DDIx_AUXP DDIx_AUXN		No Connect	
DDIx_HPD DDIx_DDC_CLK DDIx_DDC_DATA		No Connect	
DDIx_BKLTEN DDIx_BKLTCTL DDIx_VDDEN		No Connect	
DDIx_RCOMP_P DDIx_RCOMP_N		402 Ω ±1%	

12/18 update



Note: It is highly recommended a passgate N-MOSFET device is selected that has Gate Threshold Voltage <=1.5V.

Note: The HPD PU resistor tolerance can be relaxed to 5%.

3.6 Storage Interfaces

3.6.1 SD Card Interface

Secure Digital Card (SD Card). If µSD is not implemented, leave them NC except RCOMP.

ESD and EMI components must be placed on board.

Pin Name	System Pull-up/ Pull-down	Series Termination	Notes	✓
SDMMC3_D[3:0]	N/A	10 Ω	Bi-directional port used to transfer data to and from SD/MMC card. By default, after power up or reset, only D[0] is used for data transfer. A wider data bus can be configured for data transfer, using D[0]-D[3].	

3.5.1 MIPI*-CSI-2 Interface—Four (x4) Lanes

If MIPI*-CSI-1 are not implemented, leave them NC.

Pin Name	System Pull-up/ Pull-down	Notes	✓
MCSI_1_CLKP MCSI_1_CLKN	N/A	Point to Point connection to rear camera.	
MCSI_1_DP[3:0] MCSI_1_DN[3:0]	N/A	Point to Point connection to rear camera.	

Pin Name	System Pull-up/ Pull-down	Notes	✓
MCSI_2_CLKP MCSI_2_CLKN	N/A	Point to Point connection to front camera.	

3.5.2 Other MIPI*-CSI and Compensation Interface

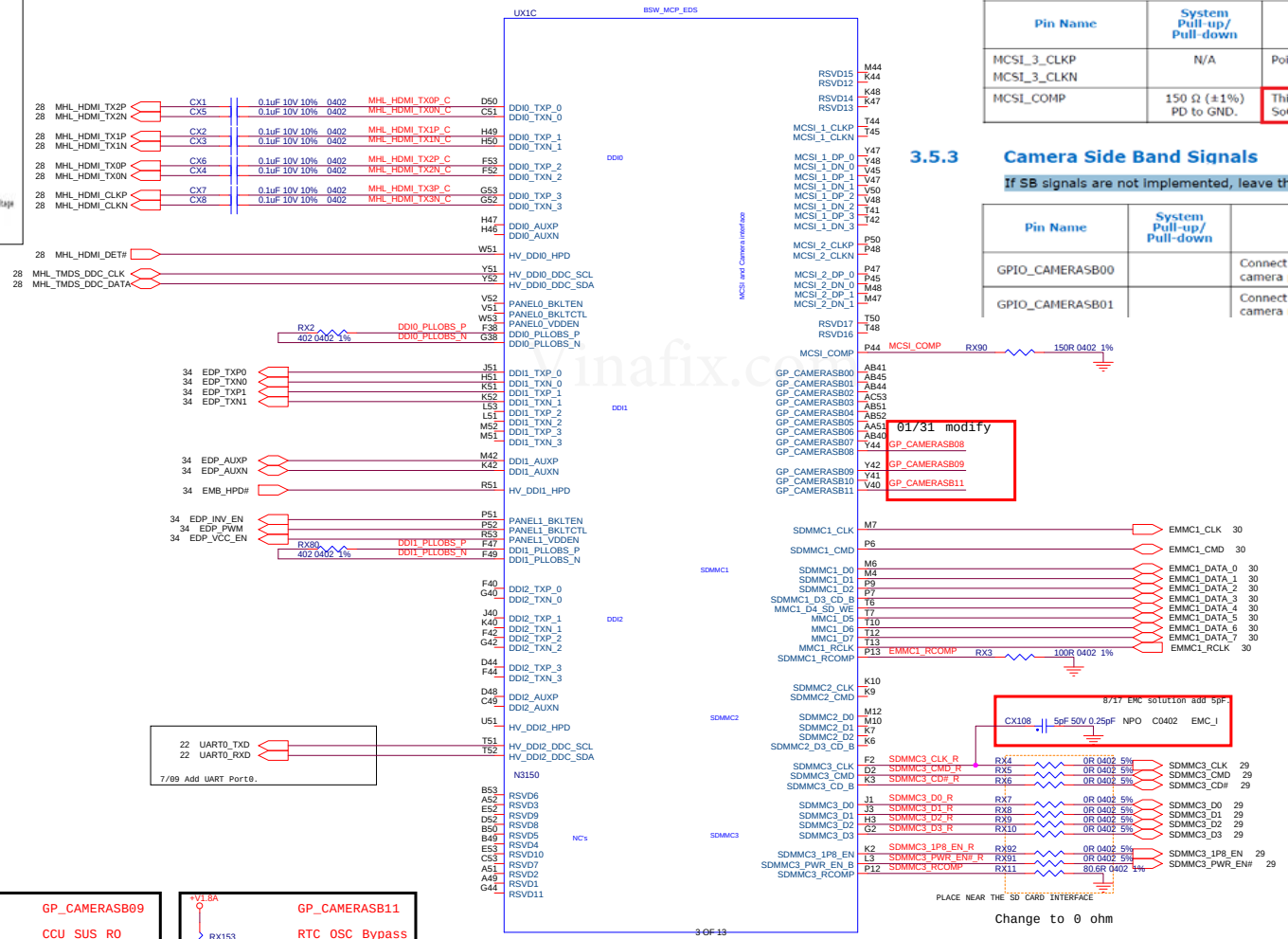
If the other MIPI*-CSI signals (exclude MCSI_COMP) are not implemented, leave them NC.

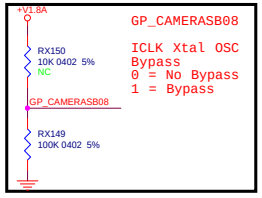
Pin Name	System Pull-up/ Pull-down	Notes	✓
MCSI_3_CLKP MCSI_3_CLKN	N/A	Point to Point connection to front camera.	
MCSI_COMP	150 Ω (±1%) PD to GND.	This resistor should be placed as close to SoC as possible.	

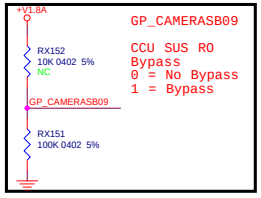
3.5.3 Camera Side Band Signals

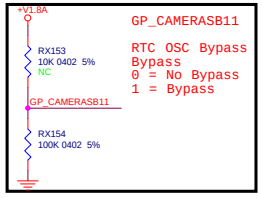
If SB signals are not implemented, leave them NC.

Pin Name	System Pull-up/ Pull-down	Notes (as example in CRB)	✓
GPIO_CAMERASB00		Connect from SoC to CAM_ACT_LED to control camera privacy LED.	
GPIO_CAMERASB01		Connect from SoC to FLASH_RESET_N at camera module.	









3nod三诺	Project: LENOVO NB116BT			
	Engineer: Jason			
Size: C	Title: BrasWell (DISPLAY)			Rev: V01
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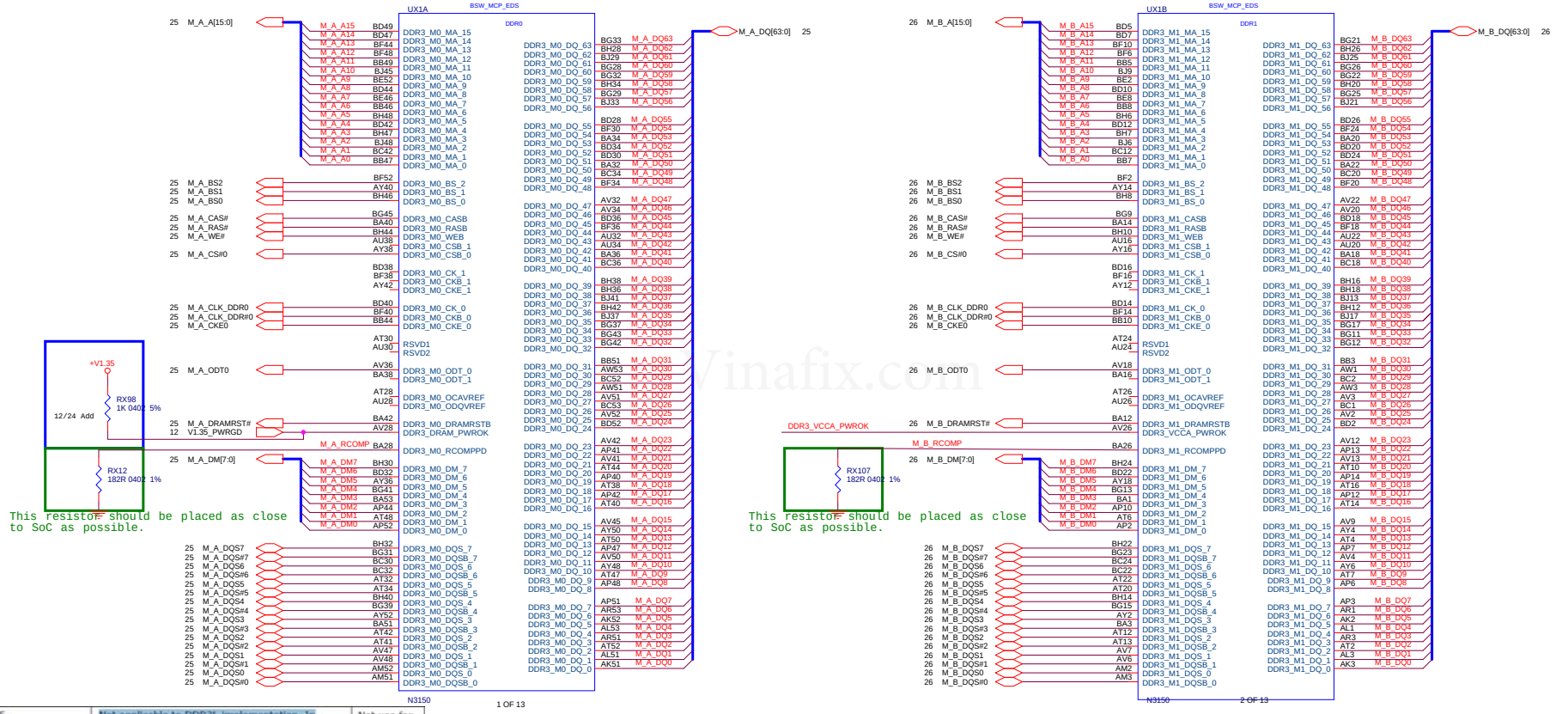

Pin Name/Description	Schematic Notes	
DDR3_M0_ODQVREF DDR3_M1_ODQVREF	Not applicable to DDR3L implementation. In DDR3L mode, these pins are No Connect on SoC Vref. External Vref circuitry needs to be given on SODIMM side. Example shown as below 0.5*VCCDDR_1P24_1P35. Use 1% resistor. Cannot go higher than 0.6*VCCDDR_1P24_1P35. Example shown as below	Not use for DDR3L design.

Pin Name/Description	Schematic Notes	
DDR3_M0_OCAVREF DDR3_M1_OCAVREF	Not applicable to DDR3L implementation. In DDR3L mode, these pins are No Connect on SoC Vref. External Vref circuitry needs to be given on SODIMM side. Example shown as below. 0.5*+VCCDDR_1P24_1P35. Use 1% resistor. Cannot go higher than 0.6*VCCDDR_1P24_1P35. Example shown as below	Not use for DDR3L design.

3nod三诺	Project: LENOVO NB116BT	
	Engineer: Jason	
Size: C	Title: BrasWell (DDR3L A/B)	Rev: V01
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PCI-E Port Table

Port	CLK	Function
Port0	Port0	Un-used
Port1	Port1	WLAN (M.2)
Port2	Port2	Un-used
Port3	Port3	WLAN (MINI)

7.2.2 Terminating Unused PCI Express* Ports
If some of the PCI Express* port(s) is not implemented on the platform:
PCIE_TXP/N [x] and PCIE_RXP/N [x] signals may be left unconnected, where x is the port number left no connect.
If no PCI Express* ports is implemented on the platform:
PCIE_TXp/n [3:0] and PCIE_RXp/n [3:0] may be left unconnected.
Pull-up PCIE_CLKREQ[3:0]_N to V1P8A with 10-K? resistor.
PCIE_RCOMP_p/n may be left unconnected
DOC:540602 VER1.2

13.2.7.3 Interface Disable Guidelines
Each signal may be left as No Connect when the interface is disabled.

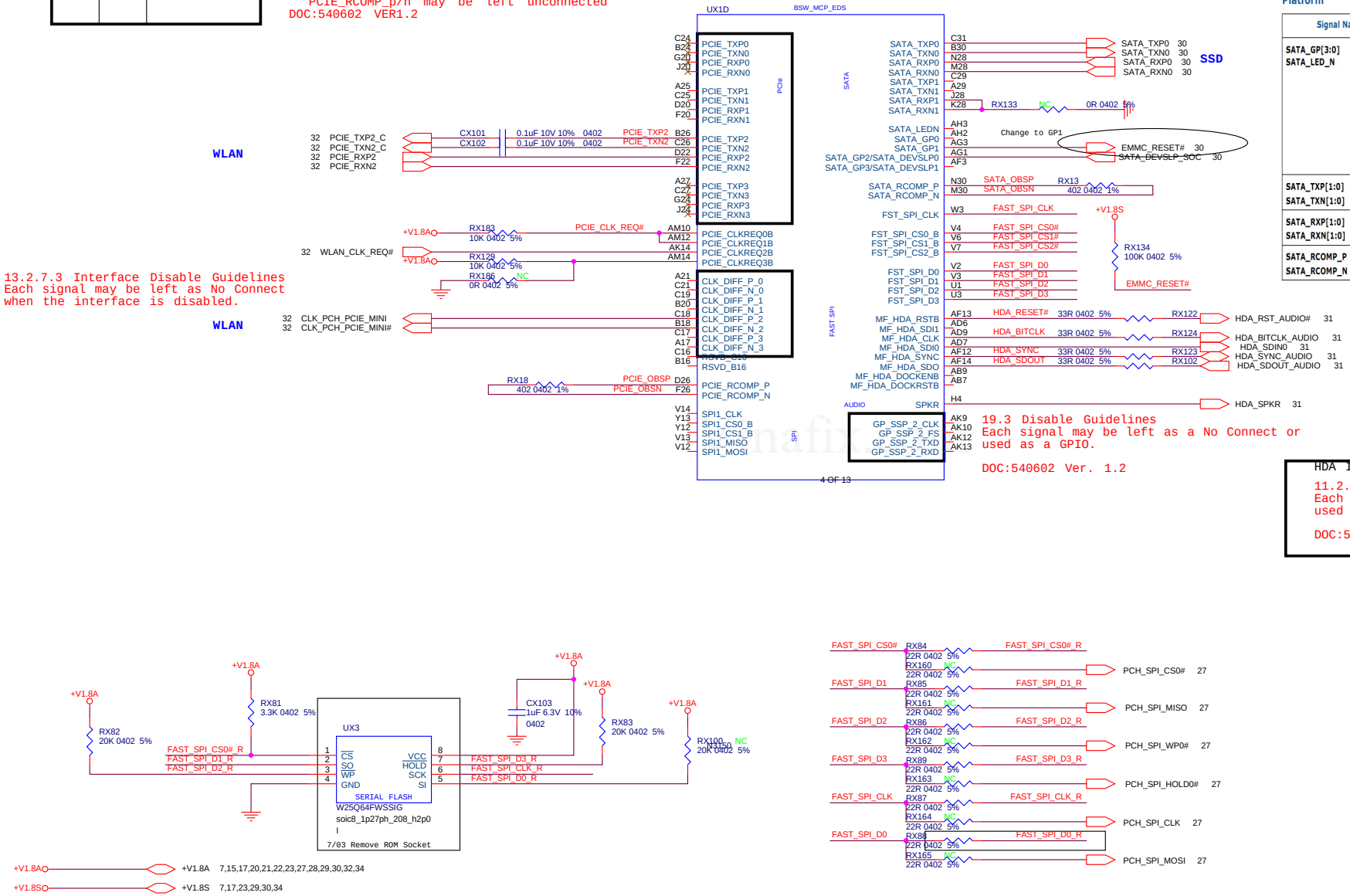
Table 9-7. Disable Guideline—If the Whole SATA interface are not Implemented on the Platform

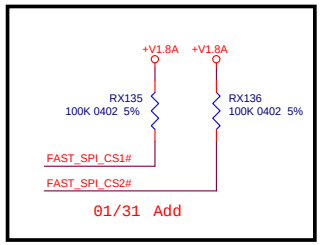
Signal Name	Disable Guideline
SATA_GP[3:0] SATA_LED_N	Each signal may be left as a No Connect or used as a GPIO. Additional considerations for each option are listed below. • No Connect: Disable the relevant interface controller via the corresponding Soft Strap listed in the Braswell SoC Family SPI Flash Programming Guide. Additionally, configure the ball to be a GPO by means of the system BIOS. See the BIOS Writers Guide for further details. • GPIO: Disable the relevant interface controller via the corresponding Soft Strap listed in the Braswell SoC Family SPI Flash Programming Guide. Additionally, configure the ball to be a GPI or GPO by means of the system BIOS. See the BIOS Writers Guide for further details.
SATA_TXP[1:0] SATA_TXN[1:0]	No-Connect.
SATA_RXP[1:0] SATA_RXN[1:0]	Connect to Ground.
SATA_RCOMP_P SATA_RCOMP_N	Connect as defined in Section 9.2.3, "SATA_RCOMP Compensation Guidelines".

19.3 Disable Guidelines
Each signal may be left as a No Connect or used as a GPIO.
DOC:540602 Ver. 1.2

HDA I/F
11.2.5 Disable Guidelines
Each signal may be left as a No Connect or used as a GPIO.
DOC:540602 Ver. 1.2

01/31 Add





Project:	LENOVO_NB116BT
Engineer:	Jason
Size	Custom
Title:	BrasWell (SPI,SATA,PCIE,AUDIO)
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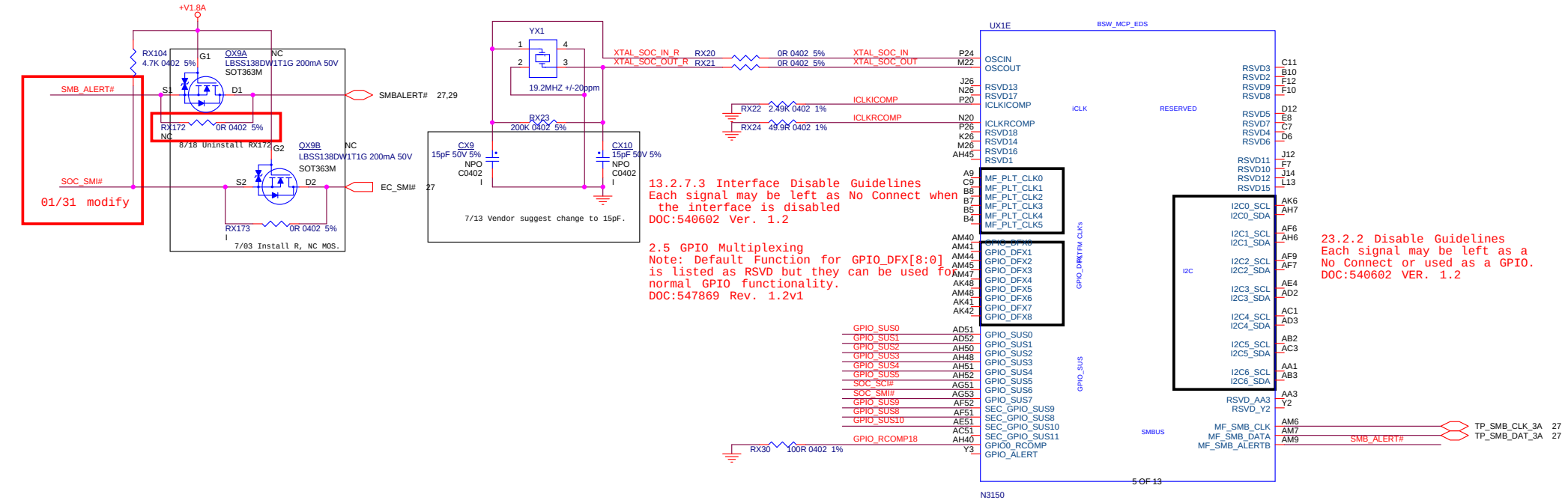
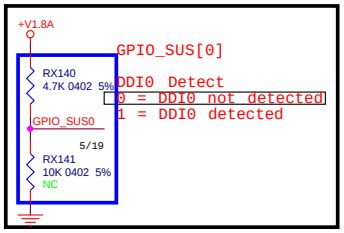
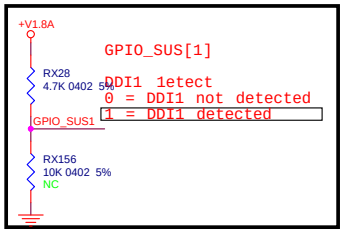
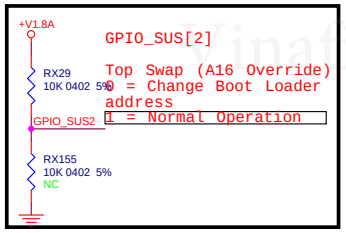
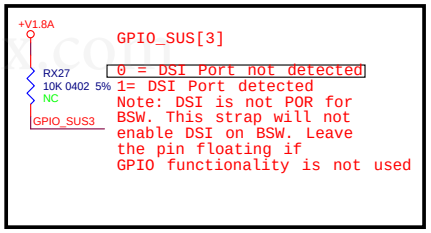
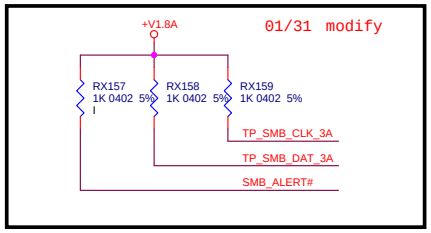


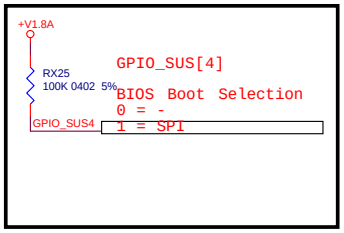


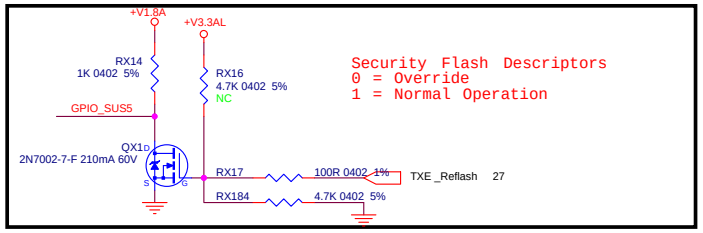


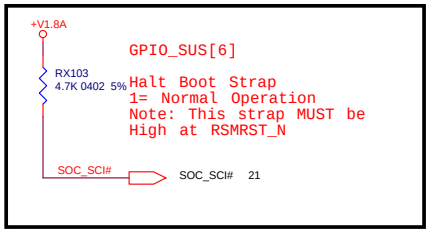


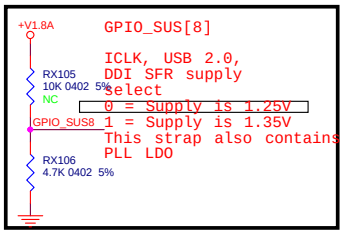


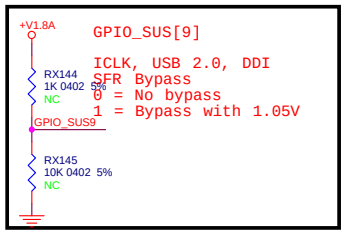


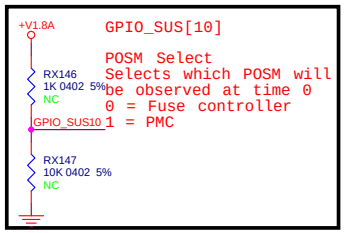


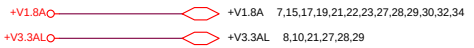




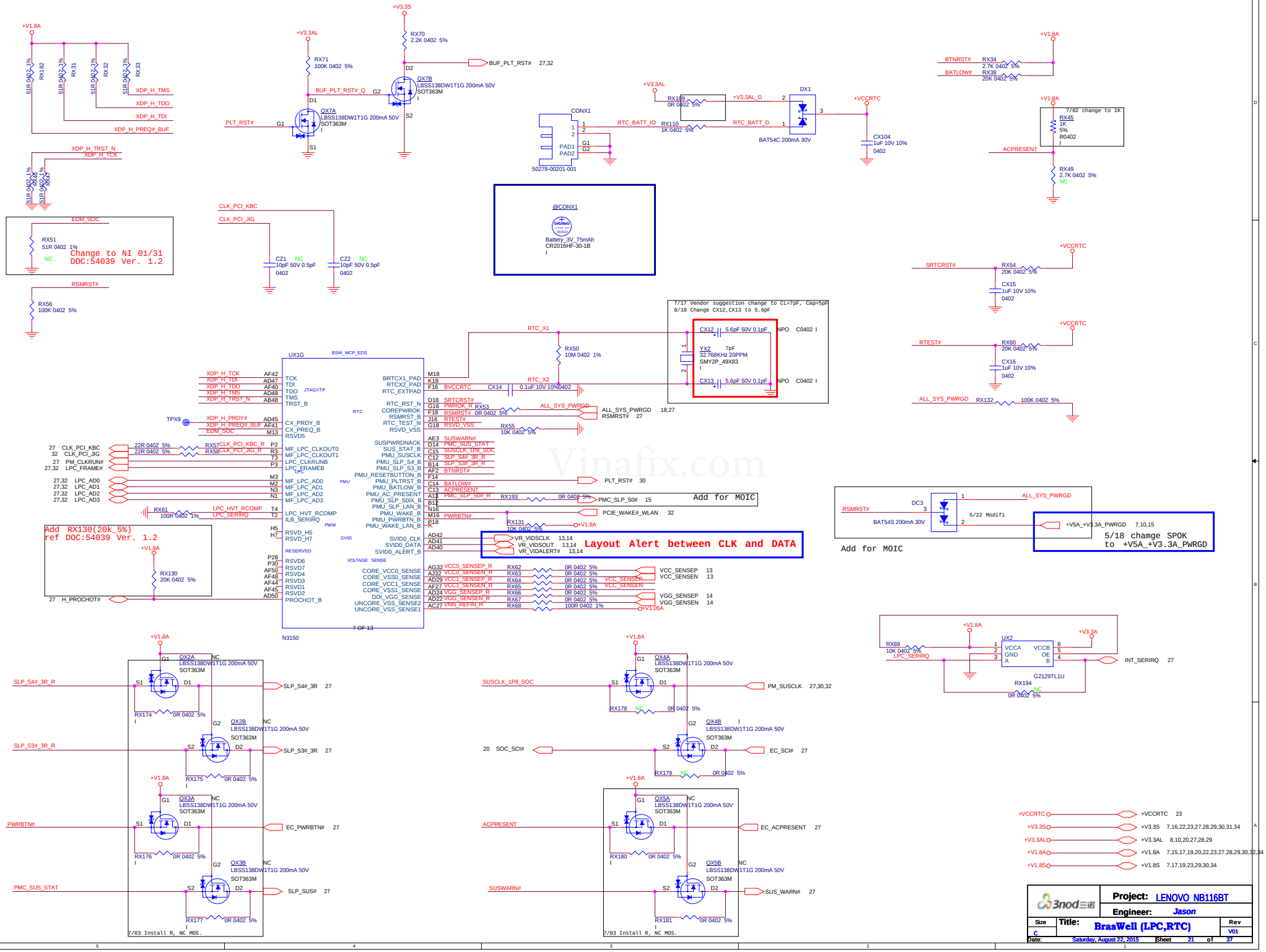








3nod三诺	Project: LENOVO_NB116BT	
	Engineer: Jason	
Size: Custom	Title: BrasWell (GPIO/I2C/CLK)	Rev: V01
Date: Saturday, August 22, 2015	Sheet 20 of 37	

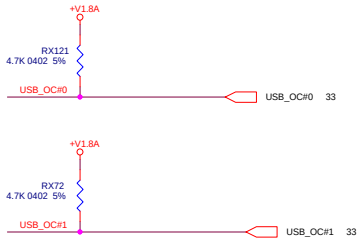

+V1.8A
+V3.3S
+V3.3AL
RX70 2.2K 0402 5%
BUF_PLT_RST# 27,32
RX71 100K 0402 5%
BUF_PLT_RST#_Q
QX7B LBSS138DW1T1G 200mA 50V SOT363M
QX7A LBSS138DW1T1G 200mA 50V SOT363M
PLT_RST#
XDP_H_TMS
XDP_H_TDO
XDP_H_TDI
XDP_H_PREQ#_BUF
XDP_H_TRST_N
XDP_H_TCK
EDM_SOC
RX51 51R 0402 1%
Change to NI 01/31
DOC:54039 Ver. 1.2
RSMRST#
RX56 100K 0402 5%
CLK_PCI_KBC
CLK_PCI_JIG
CZ1 NC 10pF 50V 0.5pF 0402
CZ2 NC 10pF 50V 0.5pF 0402
CONX1
50278-00201-001
RTC_BATT_IO
RX109 0R 0402 5%
RX110 1K 0402 5%
+3.3AL_D
RTC_BATT_D
DX1
BAT54C 200mA 30V
+VCCRTC
CX104 1uF 10V 10% 0402
@CONX1
Battery_3V_75mAh
CR2016HF-30-1B
BTNRST# RX34 2.7K 0402 5%
BATLOW# RX38 20K 0402 5%
7/02 change to 1K
RX45 1K 5% R0402
ACPRESENT
RX49 2.7K 0402 5% NC
SRTCRST# RX54 20K 0402 5%
CX15 1uF 10V 10% 0402
RTEST# RX60 20K 0402 5%
CX16 1uF 10V 10% 0402
ALL_SYS_PWRGD RX132 100K 0402 5%
7/17 Vendor suggestion change to CL=7pF, Cap=5pF
8/18 Change CX12,CX13 to 5.6pF
RTC_X1
RTC_X2
RX50 10M 0402 1%
CX12 5.6pF 50V 0.1pF NPO C0402
YX2 7pF 32.768KHz 20PPM SMY2P_49X83
CX13 5.6pF 50V 0.1pF NPO C0402
UX1G
BSW_MCP_EDS
XDP_H_TCK AF42
XDP_H_TDI AD47
XDP_H_TDO AF40
XDP_H_TMS AD48
XDP_H_TRST_N AB48
JTAG/ITP
XDP_H_PRDY# AD45
XDP_H_PREQ#_BUF AF41
EDM_SOC M13
RTC
SRTCRST# RX53
RSMRST# 0R 0402 5%
RTEST#
RX55 10K 0402 5%
ALL_SYS_PWRGD
ALL_SYS_PWRGD 18,27
RSMRST# 27
TPX9
27 CLK_PCI_KBC
32 CLK_PCI_JIG
27 PM_CLKRUN#
27,32 LPC_FRAME#
22R 0402 5%
RX57 CLK_PCI_KBC_R
RX58 CLK_PCI_JIG_R
27,32 LPC_AD0
27,32 LPC_AD1
27,32 LPC_AD2
27,32 LPC_AD3
RX61 100R 0402 1%
LPC_HVT_RCOMP
LPC_SERIRQ
Add RX130(20k_5%)
ref DOC:54039 Ver. 1.2
RX130 20K 0402 5%
27 H_PROCHOT#
PMC_SLP_S0# 15
PCIE_WAKE#_WLAN 32
RX193 0R 0402 5%
RX131 10K 0402 5%
+V1.8A
PLT_RST# 30
Add for MOIC
Layout Alert between CLK and DATA
VR_VIDSCLK 13,14
VR_VIDSOUT 13,14
VR_VIDALERT# 13,14
RSMRST#
DC3
BAT54S 200mA 30V
5/22 Modifi
ALL_SYS_PWRGD
+V5A_+V3.3A_PWRGD 7,10,15
5/18 chamge SPOK
to +V5A_+V3.3A_PWRGD
Add for MOIC
AG32 VCC0_SENSEP_R RX62 0R 0402 5% VCC_SENSEP 13
AJ32 VCC0_SENSEN_R RX63 0R 0402 5% VCC_SENSEN 13
AD29 VCC1_SENSEP_R RX64 0R 0402 5% VCC_SENSEP
AF27 VCC1_SENSEN_R RX65 0R 0402 5% VCC_SENSEN
AD24 VGG_SENSEP_R RX66 0R 0402 5% VGG_SENSEP 14
AD22 VGG_SENSEN_R RX67 0R 0402 5% VGG_SENSEN 14
AC27 VNN_REFIN_R RX68 100R 0402 1% +V1.05A
N3150
7 OF 13
RX69 10K 0402 5%
LPC_SERIRQ
UX2
G2129TL1U
RX194 NC 0R 0402 5%
INT_SERIRQ 27
SLP_S4#_3R_R
QX2A LBSS138DW1T1G 200mA 50V SOT363M
RX174 0R 0402 5%
SLP_S4#_3R 27
SLP_S3#_3R_R
QX2B LBSS138DW1T1G 200mA 50V SOT363M
RX175 0R 0402 5%
SLP_S3#_3R 27
PWRBTN#
QX3A LBSS138DW1T1G 200mA 50V SOT363M
RX176 0R 0402 5%
EC_PWRBTN# 27
PMC_SUS_STAT
QX3B LBSS138DW1T1G 200mA 50V SOT363M
RX177 0R 0402 5%
SLP_SUS# 27
7/03 Install R, NC MOS.
SUSCLK_1P8_SOC
QX4A LBSS138DW1T1G 200mA 50V SOT363M
RX178 NC 0R 0402 5%
PM_SUSCLK 27,30,32
20 SOC_SCI#
QX4B LBSS138DW1T1G 200mA 50V SOT363M
RX179 NC 0R 0402 5%
EC_SCI# 27
ACPRESENT
QX5A LBSS138DW1T1G 200mA 50V SOT363M
RX180 0R 0402 5%
EC_ACPRESENT 27
SUSWARN#
QX5B LBSS138DW1T1G 200mA 50V SOT363M
RX181 0R 0402 5%
SUS_WARN# 27
7/03 Install R, NC MOS.
+VCCRTC +VCCRTC 23
+V3.3S +V3.3S 7,16,22,23,27,28,29,30,31,34
+V3.3AL +V3.3AL 8,10,20,27,28,29
+V1.8A +V1.8A 7,15,17,19,20,22,23,27,28,29,30,32,34
+V1.8S +V1.8S 7,17,19,23,29,30,34
3nod三诺
Project: LENOVO NB116BT
Engineer: Jason
Size C
Title: BrasWell (LPC,RTC)
Rev V01
Date: Saturday, August 22, 2015
Sheet 21 of 37

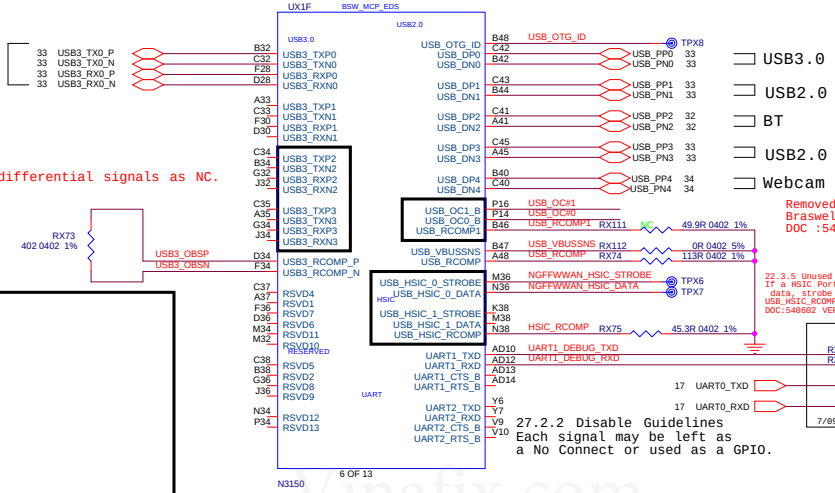
*Need setting by BIOS

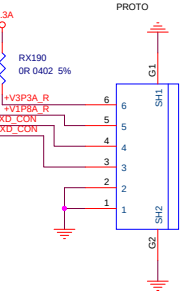
USB 3.0	USB 2.0	Function	OC#
PORT-0	PORT-0	USB2.0/3.0	OC#0
	PORT-1	USB2.0	OC#1
	PORT-2	BT	
	PORT-3	USB2.0	OC#1
	PORT-4	Webcam	

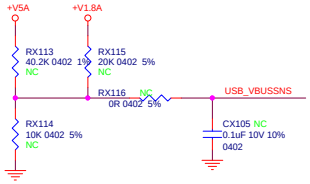
USB3.0

22.2.9 USB 3.0 Disabling and Termination Guidelines
If a USB port(s) are not implemented on the platform, USB signals can be left unconnected. OC pins require a pull-up to V1p8A with 8.2-KOhm to 10-KOhm resistors When USB OTG feature is not required, USB_OTG_ID and USB_VBUSSNS signals can be left unconnected. Additionally please refer to SPI programming Guide to set the soft strap for disabling USB OTG.
DOC::540602 Ver. 1.2





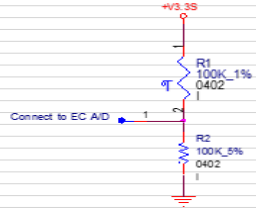


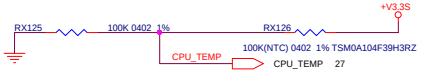


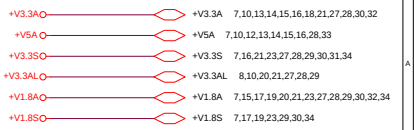
22.2.9 USB 3.0 Disabling and Termination Guidelines
If a USB port(s) are not implemented on the platform, USB signals can be left unconnected. OC pins require a pull-up to V1p8A with 8.2-KOhm to 10-KOhm resistors When USB OTG feature is not required, USB_OTG_ID and USB_VBUSSNS signals can be left unconnected. Additionally please refer to SPI programming Guide to set the soft strap for disabling USB OTG.
DOC::540602 Ver. 1.2

27.2.2 Disable Guidelines
Each signal may be left as a No Connect or used as a GPIO.

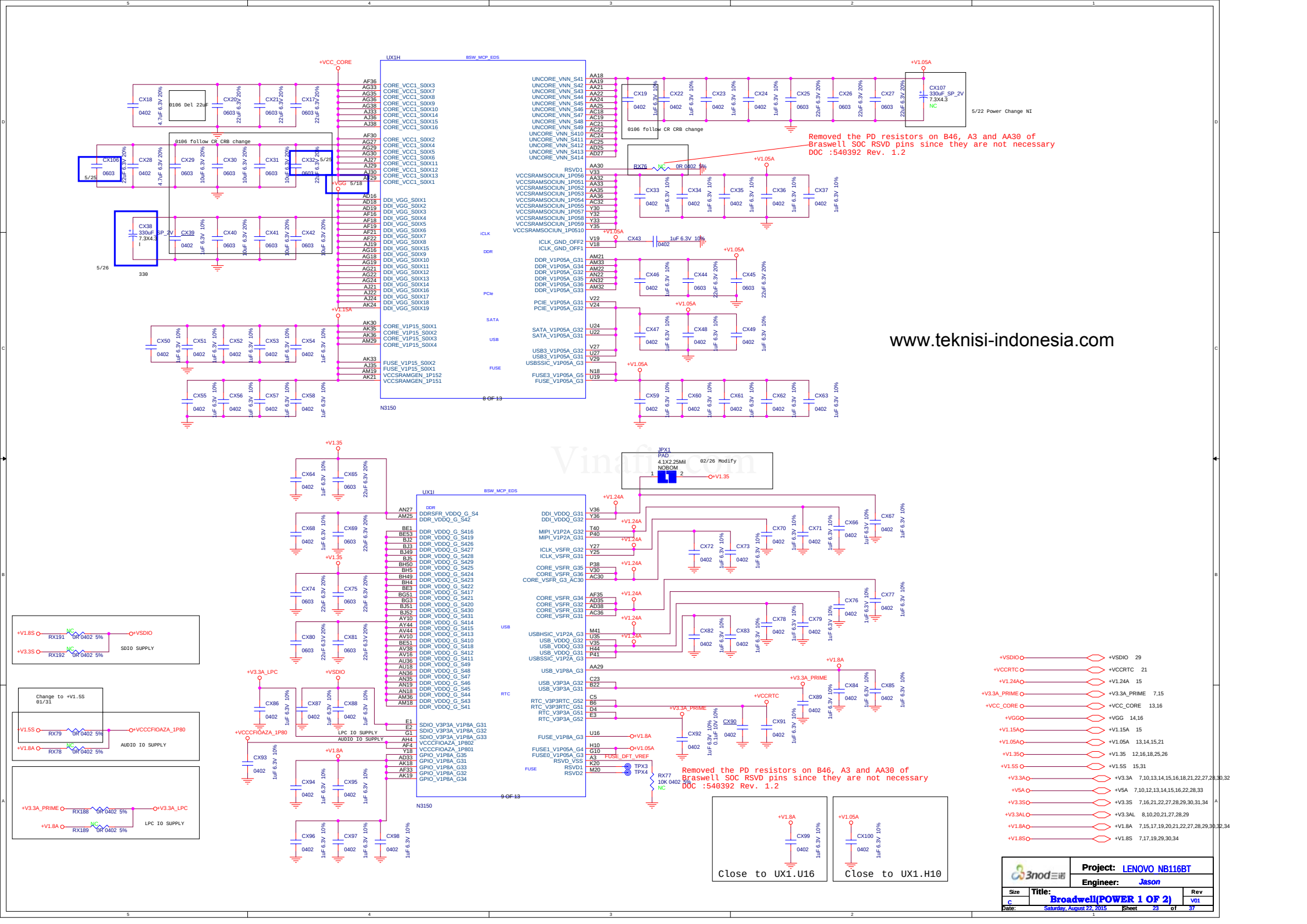
Temperature(℃)	R1(KΩ)	R2(KΩ)	Vin	EC A/D
0	328.09	100	3.3	0.770865939
1	311.75	100	3.3	0.801457195
2	296.31	100	3.3	0.832681487
3	281.73	100	3.3	0.864485369
4	267.96	100	3.3	0.896835615
5	254.94	100	3.3	0.929734503
6	242.63	100	3.3	0.963138079
7	230.98	100	3.3	0.997039096
8	219.96	100	3.3	1.031378922
9	209.53	100	3.3	1.066132524
10	199.66	100	3.3	1.101284832
11	190.29	100	3.3	1.13679424
12	181.42	100	3.3	1.172624547
13	173.02	100	3.3	1.208702659
14	165.05	100	3.3	1.245048104
15	157.49	100	3.3	1.281603169
16	150.32	100	3.3	1.31831256
17	143.51	100	3.3	1.355180482
18	137.05	100	3.3	1.392111569
19	130.91	100	3.3	1.429128232
20	125.08	100	3.3	1.466145371
21	119.55	100	3.3	1.503074471
22	114.28	100	3.3	1.540041068
23	109.28	100	3.3	1.576883462
24	104.52	100	3.3	1.613554129
25	100	100	3.3	1.65
26	95.696	100	3.3	1.686288938
27	91.6	100	3.3	1.722338205
28	87.702	100	3.3	1.758105954
29	83.99	100	3.3	1.793575738
30	80.456	100	3.3	1.828700622
31	77.089	100	3.3	1.863469781
32	73.882	100	3.3	1.897838764
33	70.826	100	3.3	1.931790243
34	67.912	100	3.3	1.965311165
35	65.135	100	3.3	1.998364974
36	62.486	100	3.3	2.030944204
37	59.96	100	3.3	2.063012754
38	57.55	100	3.3	2.094573151
39	55.25	100	3.3	2.125603862
40	53.054	100	3.3	2.156101768
41	50.958	100	3.3	2.186038501
42	48.957	100	3.3	2.215404446
43	47.045	100	3.3	2.244210956
44	45.219	100	3.3	2.272429216
45	43.473	100	3.3	2.300064336
46	41.805	100	3.3	2.327139382
47	40.211	100	3.3	2.353592662
48	38.686	100	3.3	2.379475938
49	37.227	100	3.3	2.404771571
50	35.832	100	3.3	2.4294717

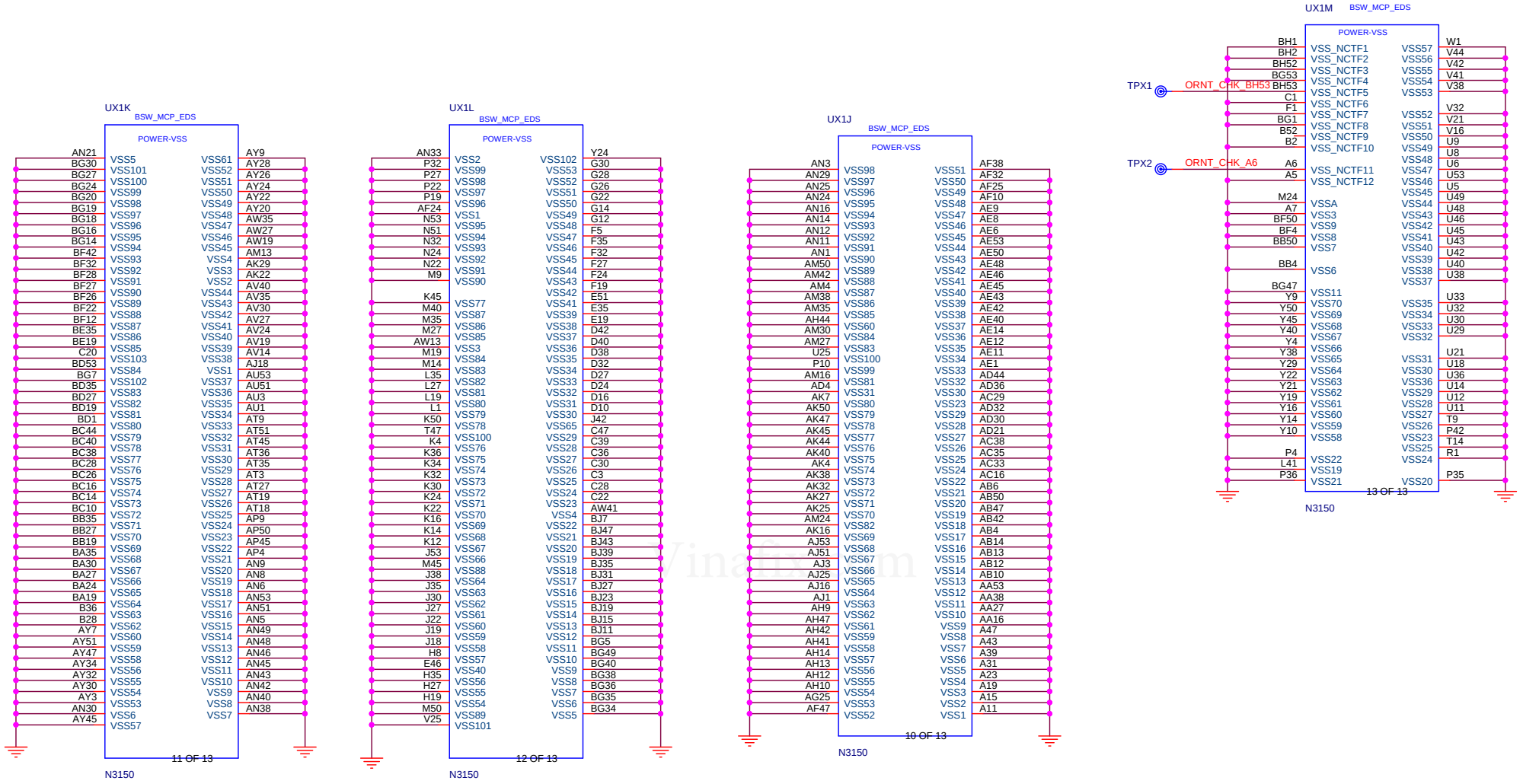






3nod三诺	Project: LENOVO NB116BT	
	Engineer: Jason	
Size: C	Title: BrasWell (USB,UART)	Rev: V01
Date: Saturday, August 22, 2015	Sheet 22 of 37	


UX1H
BSW_MCP_EDS
+VCC_CORE
CORE_VCC1_S0IX3
CORE_VCC1_S0IX7
CORE_VCC1_S0IX8
CORE_VCC1_S0IX9
CORE_VCC1_S0IX10
CORE_VCC1_S0IX14
CORE_VCC1_S0IX15
CORE_VCC1_S0IX16
CORE_VCC1_S0IX2
CORE_VCC1_S0IX4
CORE_VCC1_S0IX5
CORE_VCC1_S0IX6
CORE_VCC1_S0IX11
CORE_VCC1_S0IX12
CORE_VCC1_S0IX13
CORE_VCC1_S0IX1
DDI_VGG_S0IX1
DDI_VGG_S0IX2
DDI_VGG_S0IX3
DDI_VGG_S0IX4
DDI_VGG_S0IX5
DDI_VGG_S0IX6
DDI_VGG_S0IX7
DDI_VGG_S0IX8
DDI_VGG_S0IX15
DDI_VGG_S0IX9
DDI_VGG_S0IX10
DDI_VGG_S0IX11
DDI_VGG_S0IX12
DDI_VGG_S0IX13
DDI_VGG_S0IX14
DDI_VGG_S0IX16
DDI_VGG_S0IX17
DDI_VGG_S0IX18
DDI_VGG_S0IX19
CORE_V1P15_S0IX1
CORE_V1P15_S0IX2
CORE_V1P15_S0IX3
CORE_V1P15_S0IX4
FUSE_V1P15_S0IX2
FUSE_V1P15_S0IX1
VCCSRAMGEN_1P152
VCCSRAMGEN_1P151
8 OF 13
N3150
ICLK
DDR
PCIe
SATA
USB
FUSE
UNCORE_VNN_S41
UNCORE_VNN_S42
UNCORE_VNN_S43
UNCORE_VNN_S44
UNCORE_VNN_S45
UNCORE_VNN_S46
UNCORE_VNN_S47
UNCORE_VNN_S48
UNCORE_VNN_S49
UNCORE_VNN_S410
UNCORE_VNN_S411
UNCORE_VNN_S412
UNCORE_VNN_S413
UNCORE_VNN_S414
RSVD1
VCCSRAMSOCIUN_1P056
VCCSRAMSOCIUN_1P051
VCCSRAMSOCIUN_1P052
VCCSRAMSOCIUN_1P053
VCCSRAMSOCIUN_1P054
VCCSRAMSOCIUN_1P055
VCCSRAMSOCIUN_1P057
VCCSRAMSOCIUN_1P058
VCCSRAMSOCIUN_1P059
VCCSRAMSOCIUN_1P0510
ICLK_GND_OFF2
ICLK_GND_OFF1
DDR_V1P05A_G31
DDR_V1P05A_G34
DDR_V1P05A_G32
DDR_V1P05A_G35
DDR_V1P05A_G36
DDR_V1P05A_G33
PCIE_V1P05A_G31
PCIE_V1P05A_G32
SATA_V1P05A_G32
SATA_V1P05A_G31
USB3_V1P05A_G32
USB3_V1P05A_G31
USBSSIC_V1P05A_G3
FUSE3_V1P05A_G5
FUSE_V1P05A_G3
+V1.05A
+V1.15A
+VGG 5/18
0106 follow CR CRB change
5/22 Power Change NI
Removed the PD resistors on B46, A3 and AA30 of Braswell SOC RSVD pins since they are not necessary
DOC :540392 Rev. 1.2
RX76 NC 0R 0402 5%
www.teknisi-indonesia.com
JPX1
PAD
4.1X2.25Mil
NOBOM
02/26 Modify
+V1.35
UX1I
BSW_MCP_EDS
DDR
USB
RTC
DDRSFR_VDDQ_G_S4
DDR_VDDQ_G_S42
DDR_VDDQ_G_S416
DDR_VDDQ_G_S419
DDR_VDDQ_G_S426
DDR_VDDQ_G_S427
DDR_VDDQ_G_S428
DDR_VDDQ_G_S429
DDR_VDDQ_G_S425
DDR_VDDQ_G_S424
DDR_VDDQ_G_S423
DDR_VDDQ_G_S422
DDR_VDDQ_G_S417
DDR_VDDQ_G_S421
DDR_VDDQ_G_S420
DDR_VDDQ_G_S430
DDR_VDDQ_G_S431
DDR_VDDQ_G_S414
DDR_VDDQ_G_S415
DDR_VDDQ_G_S413
DDR_VDDQ_G_S410
DDR_VDDQ_G_S418
DDR_VDDQ_G_S412
DDR_VDDQ_G_S411
DDR_VDDQ_G_S49
DDR_VDDQ_G_S48
DDR_VDDQ_G_S47
DDR_VDDQ_G_S46
DDR_VDDQ_G_S45
DDR_VDDQ_G_S44
DDR_VDDQ_G_S43
DDR_VDDQ_G_S41
SDIO_V3P3A_V1P8A_G31
SDIO_V3P3A_V1P8A_G32
SDIO_V3P3A_V1P8A_G33
VCCCFIOAZA_1P802
VCCCFIOAZA_1P801
GPIO_V1P8A_G35
GPIO_V1P8A_G31
GPIO_V1P8A_G33
GPIO_V1P8A_G32
GPIO_V1P8A_G34
9 OF 13
N3150
DDI_VDDQ_G31
DDI_VDDQ_G32
MIPI_V1P2A_G32
MIPI_V1P2A_G31
ICLK_VSFR_G32
ICLK_VSFR_G31
CORE_VSFR_G35
CORE_VSFR_G36
CORE_VSFR_G3_AC30
CORE_VSFR_G34
CORE_VSFR_G32
CORE_VSFR_G33
CORE_VSFR_G31
USBHSIC_V1P2A_G3
USB_VDDQ_G32
USB_VDDQ_G33
USB_VDDQ_G31
USBSSIC_V1P2A_G3
USB_V1P8A_G3
USB_V3P3A_G32
USB_V3P3A_G31
RTC_V3P3RTC_G52
RTC_V3P3RTC_G51
RTC_V3P3A_G51
RTC_V3P3A_G52
FUSE_V1P8A_G3
FUSE1_V1P05A_G4
FUSE0_V1P05A_G3
RSVD_VSS
RSVD1
RSVD2
FUSE_DFT_VREF
TPX3
TPX4
RX77 10K 0402 5% NC
+V1.24A
+V3.3A_PRIME
+VCCRTC
+V1.8A
+V1.05A
Removed the PD resistors on B46, A3 and AA30 of Braswell SOC RSVD pins since they are not necessary
DOC :540392 Rev. 1.2
+V1.8S
+V3.3S
RX191 0R 0402 5%
RX192 0R 0402 5%
+VSDIO
SDIO SUPPLY
Change to +V1.5S 01/31
+V1.5S
RX79 0R 0402 5%
+VCCCFIOAZA_1P80
+V1.8A
RX78 0R 0402 5%
AUDIO IO SUPPLY
+V3.3A_PRIME
RX188 0R 0402 5%
+V3.3A_LPC
RX189 0R 0402 5%
LPC IO SUPPLY
+VSDIO 29
+VCCRTC 21
+V1.24A 15
+V3.3A_PRIME 7,15
+VCC_CORE 13,16
+VGG 14,16
+V1.15A 15
+V1.05A 13,14,15,21
+V1.35 12,16,18,25,26
+V1.5S 15,31
+V3.3A 7,10,13,14,15,16,18,21,22,27,28,30,32
+V5A 7,10,12,13,14,15,16,22,28,33
+V3.3S 7,16,21,22,27,28,29,30,31,34
+V3.3AL 8,10,20,21,27,28,29
+V1.8A 7,15,17,19,20,21,22,27,28,29,30,32,34
+V1.8S 7,17,19,29,30,34
Close to UX1.U16
Close to UX1.H10
3nod三诺
Project: LENOVO NB116BT
Engineer: Jason
Size C
Title: Broadwell(POWER 1 OF 2)
Rev V01
Date: Saturday, August 22, 2015
Sheet 23 of 37

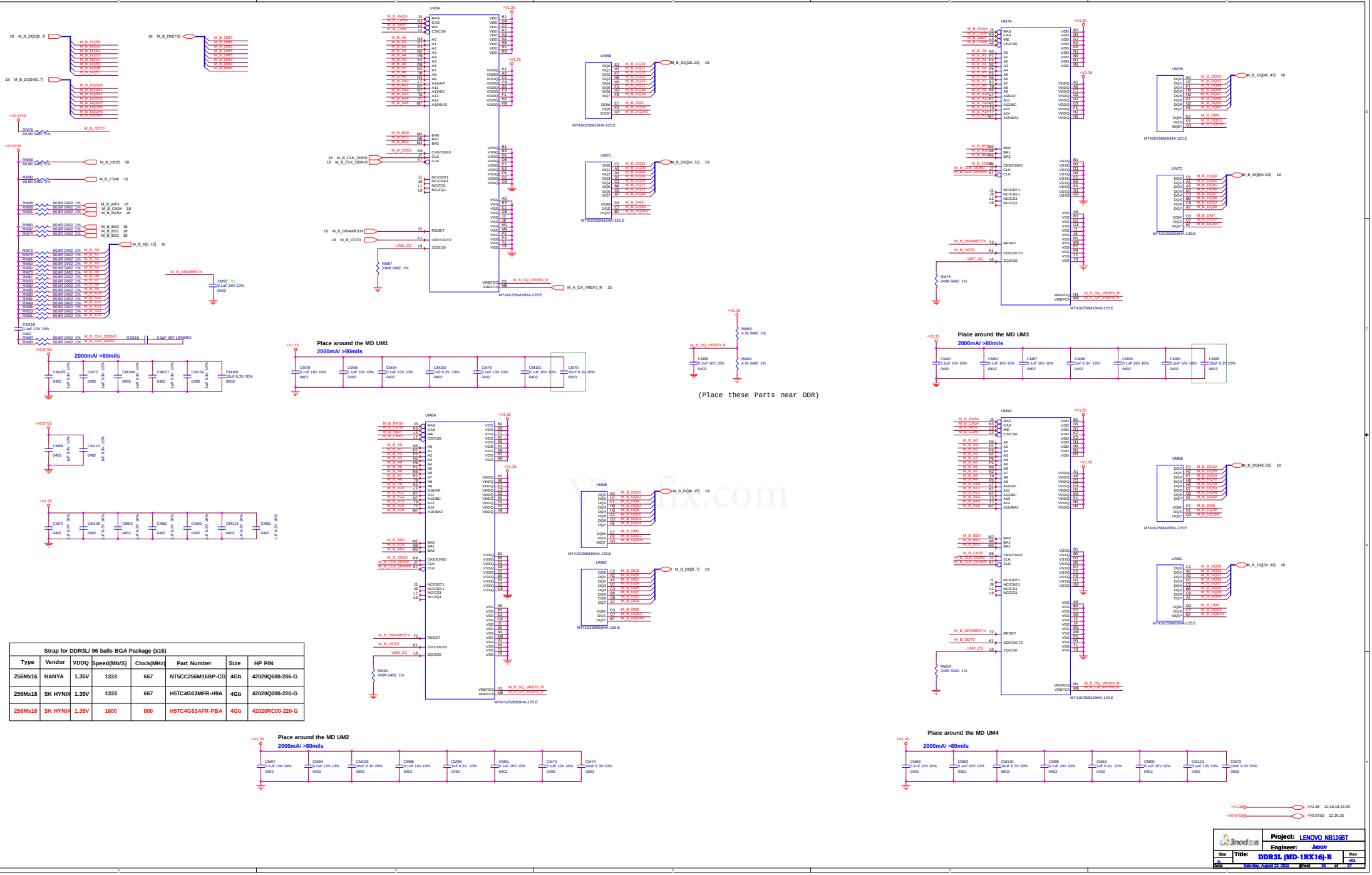


3nod三诺	Project: LENOVO_NB116BT	
	Engineer: Jason	
Size: B	Title: Broadwell(POWER 2 OF 2)	Rev: V01
Date: Saturday, August 22, 2015	Sheet 24 of 37	

Strap for DDR3L/ 96 balls BGA Package (x16)							
Type	Vendor	VDDQ	Speed(Mb/S)	Clock(MHz)	Part Number	Size	HP P/N
256Mx16	NANYA	1.35V	1333	667	NT5CC256M16BP-CG	4Gb	42020Q600-286-G
256Mx16	SK HYNIX	1.35V	1333	667	H5TC4G63MFR-H9A	4Gb	42020Q000-220-G
256Mx16	SK HYNIX	1.35V	1600	800	H5TC4G63AFR-PBA	4Gb	42020RC00-220-G

	Project:	LENOVO NB116BT	
	Engineer:	Jason	
Size	Title:	DDR3L (MD-1RX16)-A	Rev
A			V01
Date:	Saturday, August 22, 2015	Sheet 25 of 37	

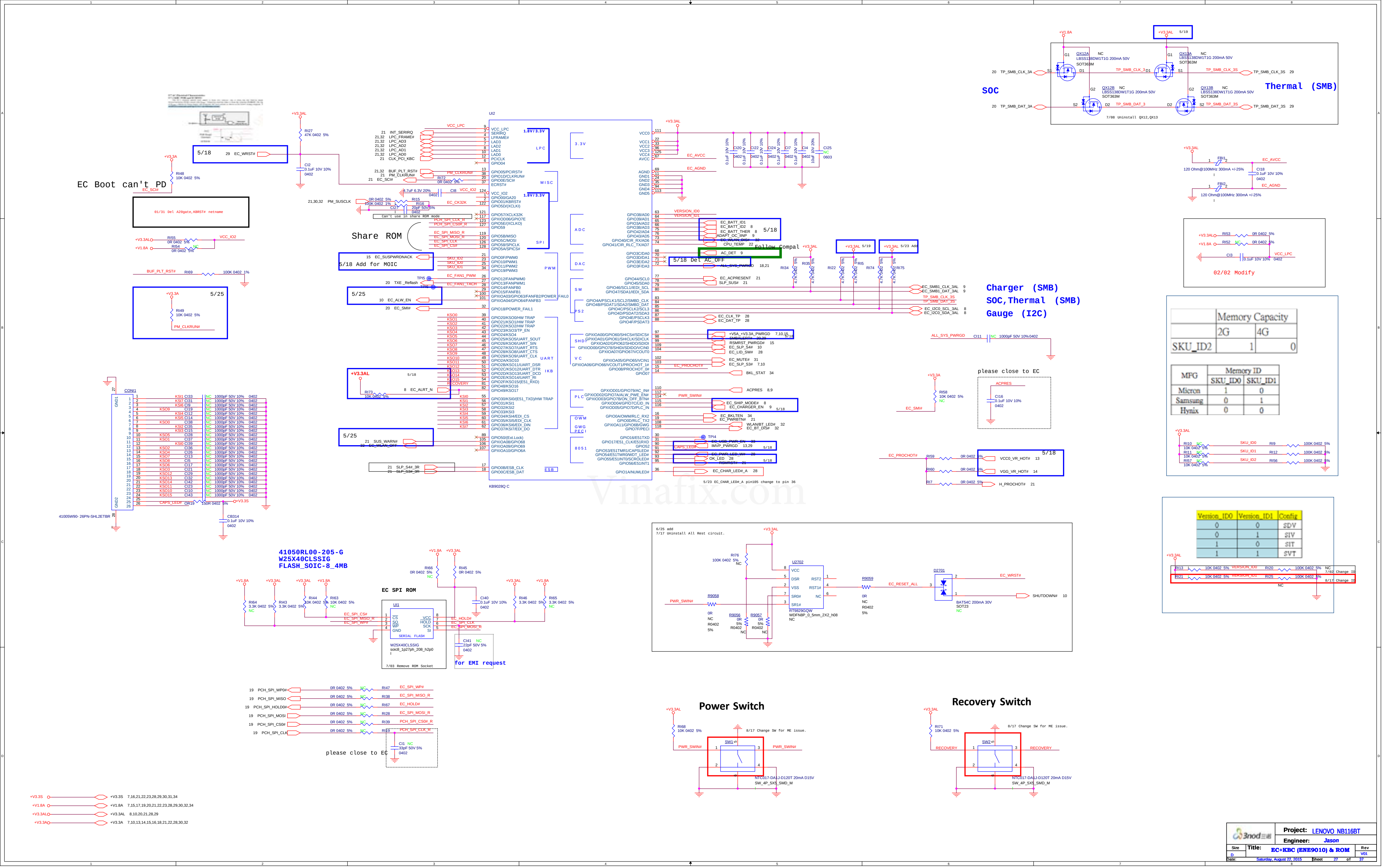
+V1.35 12,16,18,23,26
+V0.675S 12,16,26



Strap for DDR3L/ 96 balls BGA Package (x16)							
Type	Vendor	VDDQ	Speed(Mb/S)	Clock(MHz)	Part Number	Size	HP P/N
256Mx16	NANYA	1.35V	1333	667	NT5CC256M16BP-CG	4Gb	42020Q600-286-G
256Mx16	SK HYNIX	1.35V	1333	667	H5TC4G63MFR-H9A	4Gb	42020Q000-220-G
256Mx16	SK HYNIX	1.35V	1600	800	H5TC4G63AFR-PBA	4Gb	42020RC00-220-G

+V1.35 12,16,18,23,25
+V0.675S 12,16,25

Project:	LENOVO NB116BT	
Engineer:	Jason	
Size: A	Title: DDR3L (MD-1RX16)-B	Rev: V01
Date: Saturday, August 22, 2015	Sheet 26 of 37	



	Memory Capacity	
	2G	4G
SKU_ID2	1	0

MFG	Memory ID SKU_ID0	Memory ID SKU_ID1
Micron	1	0
Samsung	0	1
Hynix	0	0

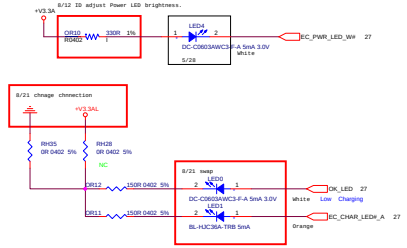
Version_ID0	Version_ID1	Config
0	0	SDV
0	1	SIV
1	0	SIT
1	1	SVT

Project:	LENOVO NB116BT
Engineer:	Jason
Title:	EC+KBC (ENE9010) & ROM
Size	D
Rev	V01
Date:	Saturday, August 22, 2015
Sheet	27 of 37

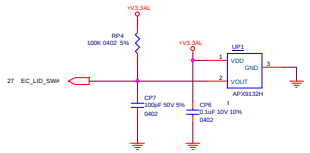
LEDS

Power on

Battery Charge



LID Switch

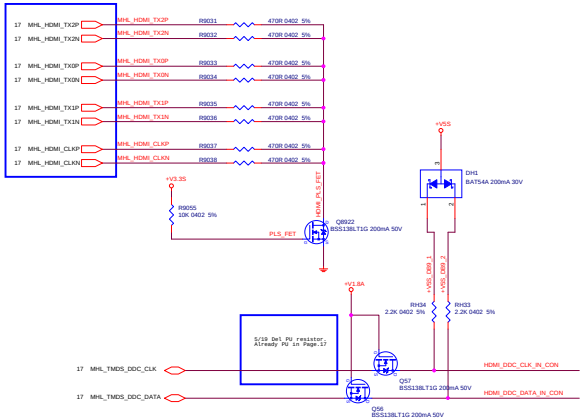


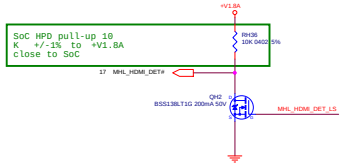
+V3.3AL: 15mils
GND: 15mils
EC_LID_SW#: 10mils
PWR_SWIN#: 10mils
EC_PWR_LED#_W: 10mils

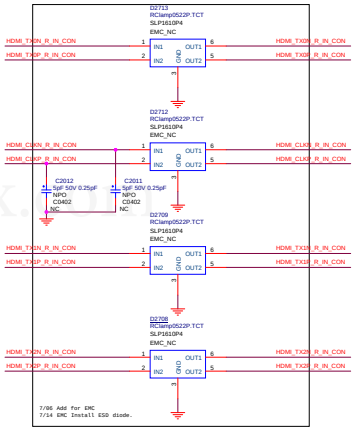
Pin	Name	I/O	Description
12	PD#	I	Chip power down. Active LOW. Internal pull up at ~150kΩ. 3.3V I/O PD# = H: Normal operation (default) L: Chip power down
8	DCIN_EN	I	DC coupling enable; Internal pull down at ~150kΩ, 3.3V I/O DCIN_EN = L: AC coupling input (default) H: DC coupling input
13	EQ	I	Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O EQ = L: Programmable EQ for channel loss up to 12.4dB @ 3.0Gbps (default) H: Programmable EQ for channel loss up to 4.3dB @ 3.0Gbps M: Programmable EQ for channel loss up to 8.6dB @ 3.0Gbps
15	PRE	I	Output pre-emphasis setting for data; Internal pull down at ~150kΩ, 3.3V I/O PRE = L: No pre-emphasis (default) H: 2.5dB pre-emphasis

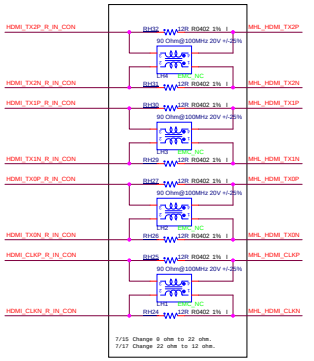
HDMI Level Shifter

Layout:Place close to capacitor Branch point

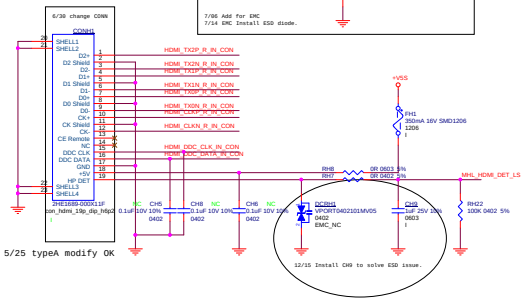




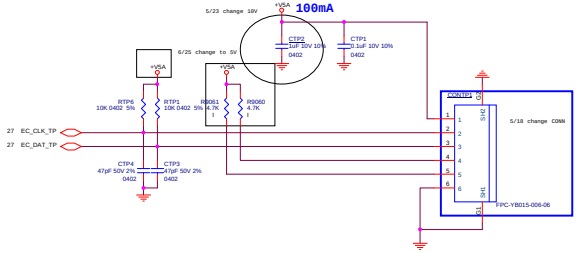




HDMI CONN

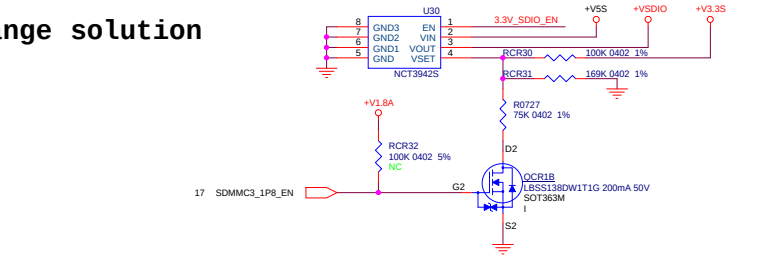


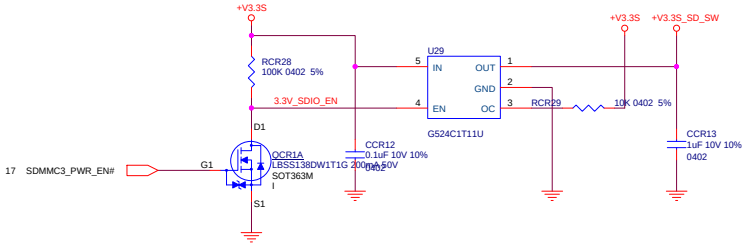
5/25 typeA modify OK



3nod三诺	Project:	LENOVO NB116BT
	Engineer:	Jason
Size: A	Title:	PWR LED/LID/TP CONN/HDMI
Date: Tuesday, December 15, 2015	Sheet 28 of 37	Rev V01

Change solution





+3V_+1.8V_VO Selection	
SDIO_3_1P8_EN	+3V_+1.8V_VOUT (V)
1	+1.8 V
0	+3.3 V

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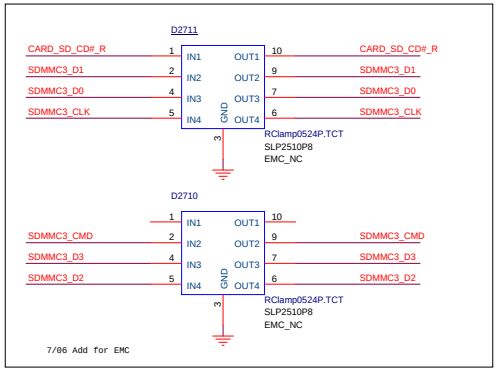
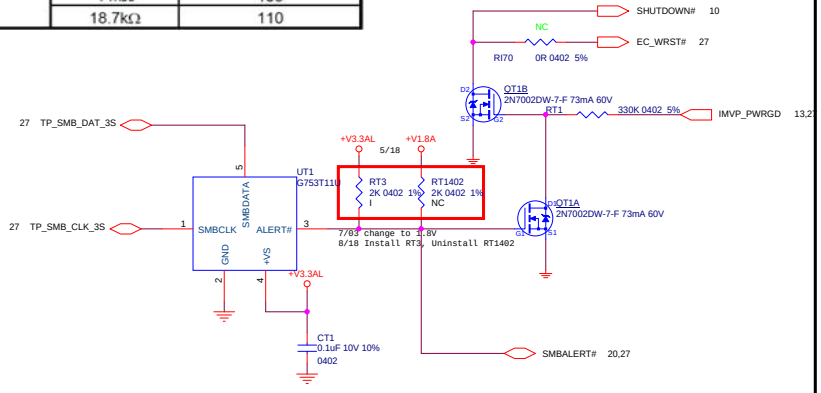


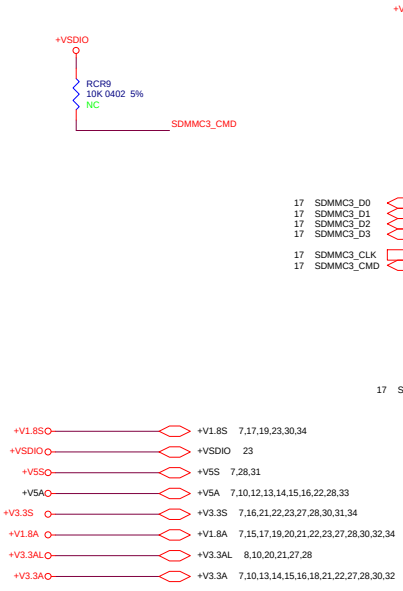
Thermal Sensor

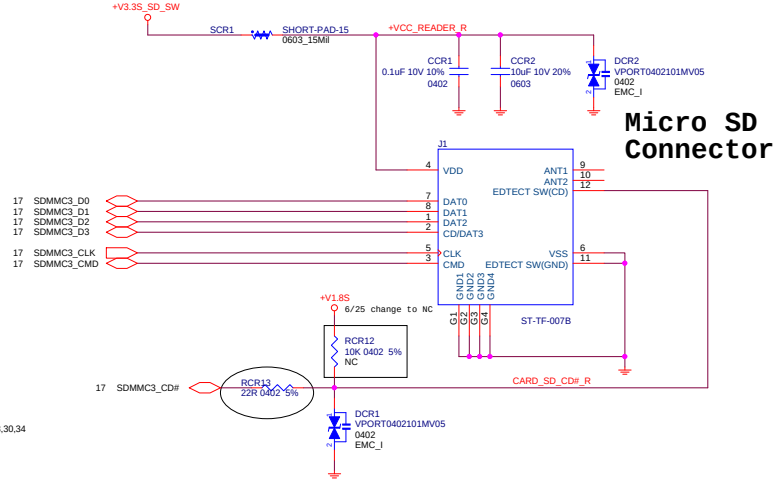
ALERT# point hardware power-on setting

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin:

PULL-UP RESISTOR		TEMPERATURE (°C)
ALERT	2kΩ	75
	7.5kΩ	90
	10.5kΩ	100
	14kΩ	105
	18.7kΩ	110

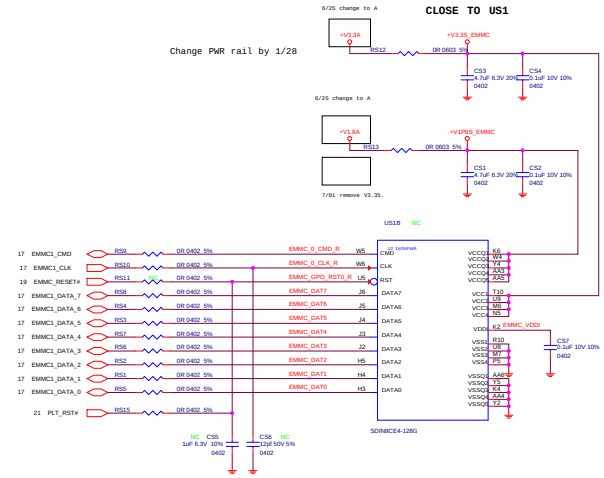




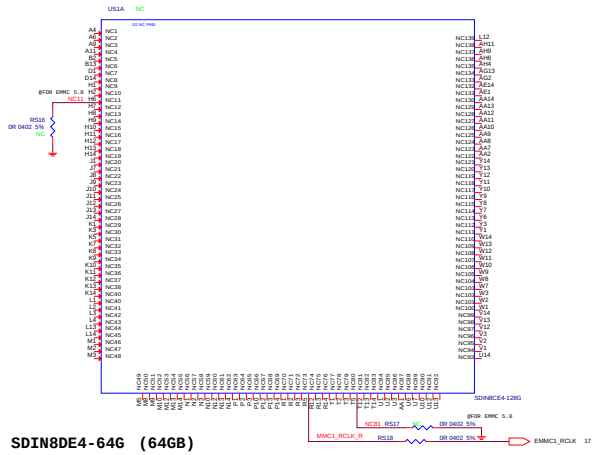


Micro SD Connector

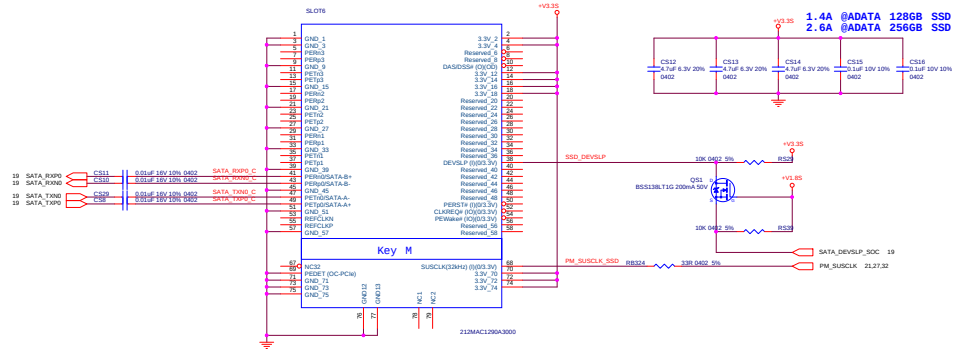
3nod三诺	Project: LENOVO NB116BT		
	Engineer: Jason		
Size: C	Title: Micro SD CONN. & Thermal		Rev: V01
Date: Monday, August 24, 2015	Sheet 29 of 37		



SDIN8CE4-128G
eMMC(169ball)

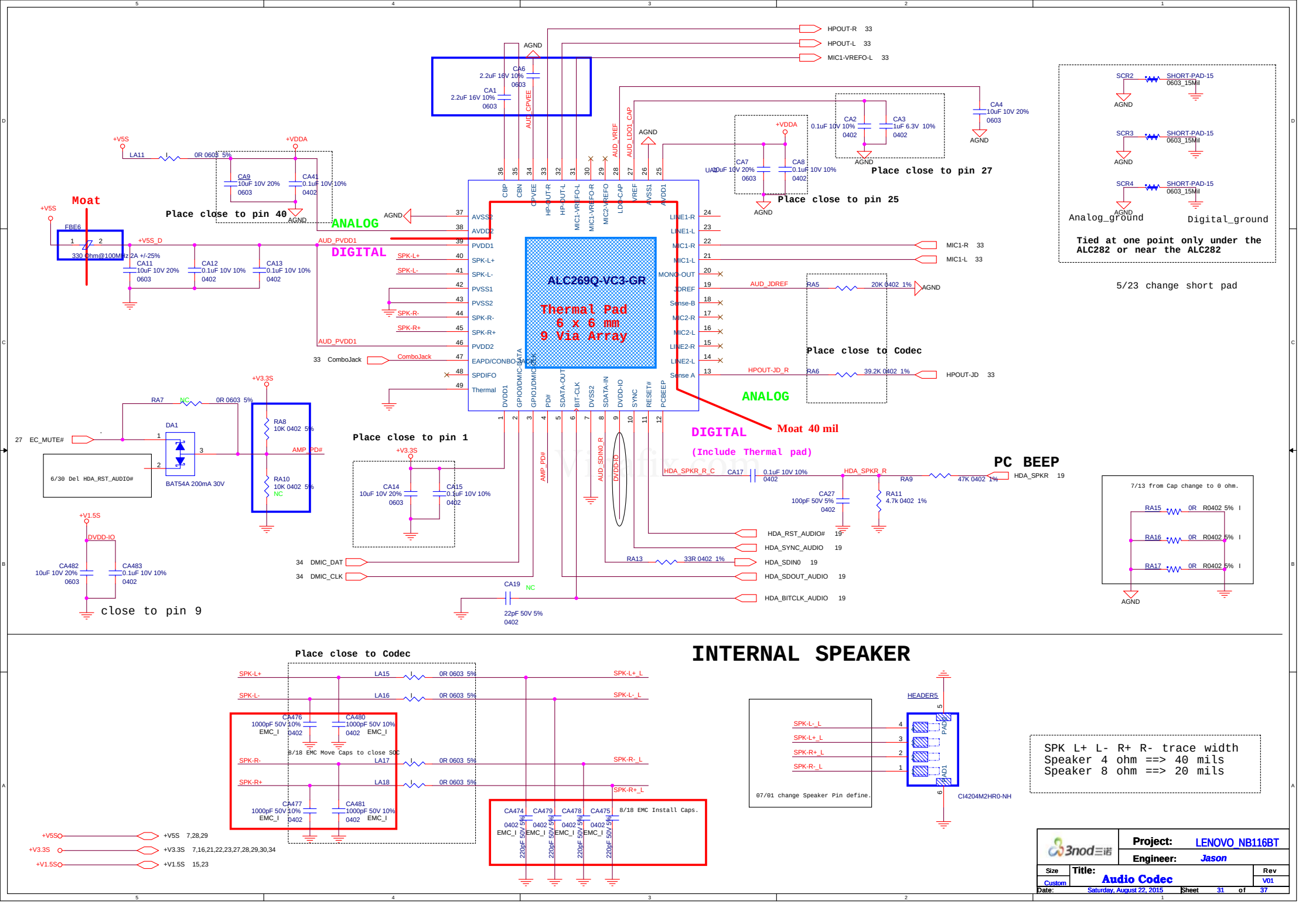


SDIN8DE4-64G (64GB)



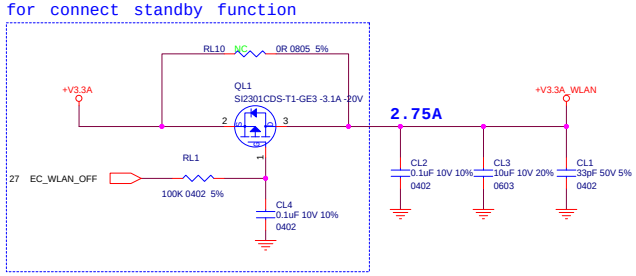
+V1.8S 7,17,19,23,29,34
+V3.3S 7,16,21,22,23,27,28,29,31,34

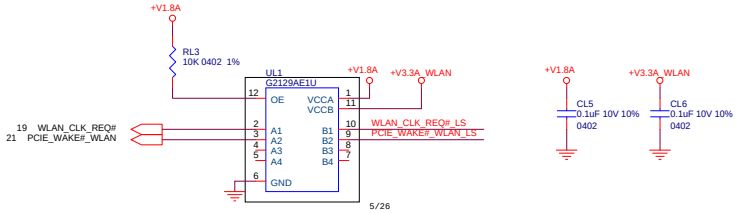
3nod三诺	Project:	LENOVO NB116BT	
	Engineer:	Jason	
Size: A	Title:	eMMC & M2 SSD	Rev: V01
Date: Saturday, August 22, 2015	Sheet 30 of 37		

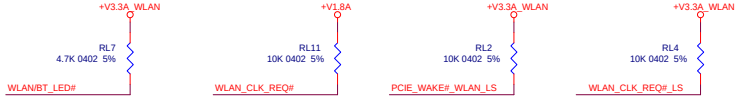

ALC269Q-VC3-GR
Thermal Pad
6 x 6 mm
9 Via Array
ANALOG
DIGITAL
Moat
Moat 40 mil
Place close to pin 40
Place close to pin 25
Place close to pin 27
Place close to pin 1
Place close to Codec
Place close to pin 9
Place close to Codec
PC BEEP
INTERNAL SPEAKER
Analog_ground
Digital_ground
Tied at one point only under the ALC282 or near the ALC282
5/23 change short pad
7/13 from Cap change to 0 ohm.
8/18 EMC Move Caps to close SOC
8/18 EMC Install Caps.
07/01 change Speaker Pin define.
SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils
6/30 Del HDA_RST_AUDIO#
Project: LENOVO_NB116BT
Engineer: Jason
Title: Audio Codec
Rev V01
Date: Saturday, August 22, 2015
Sheet 31 of 37

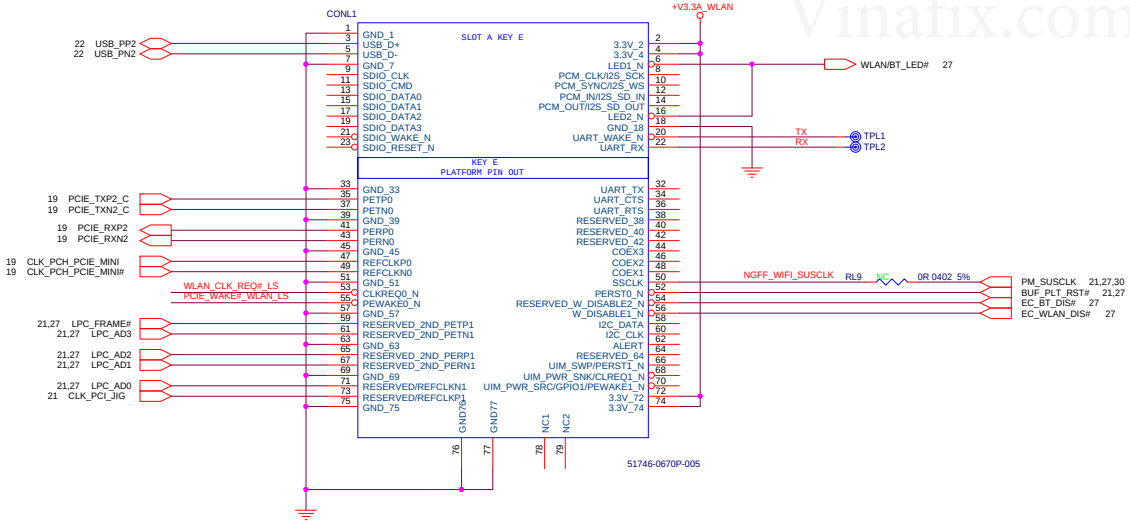
+3_3VAux=>2.75A Peak/1.1A Normal

for connect standby function

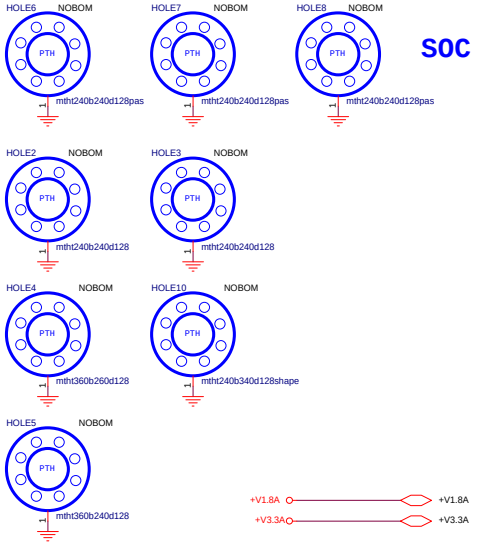








Screw Hole



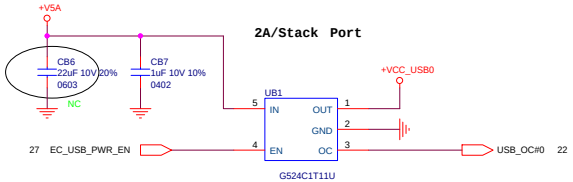
+V1.8A +V1.8A 7,15,17,19,20,21,22,23,27,28,29,30,34

+V3.3A +V3.3A 7,10,13,14,15,16,18,21,22,27,28,30

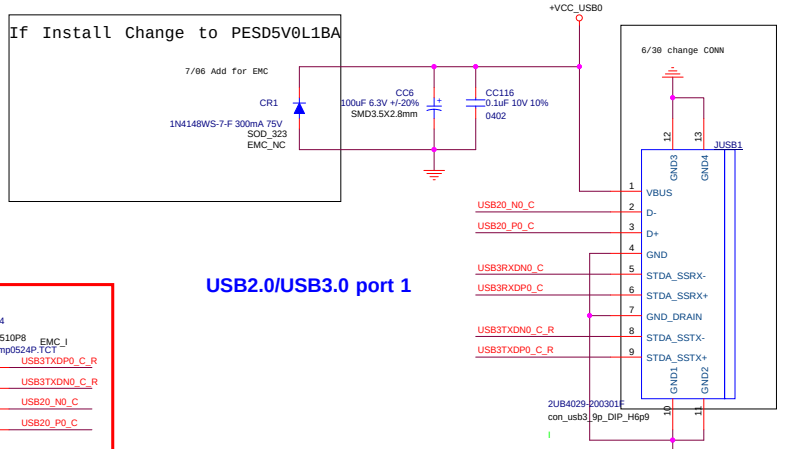
3nod三诺	Project: LENOVO NB116BT	
	Engineer: Jason	
Size: C	Title: WIFI & BT	Rev: V01
Date: Saturday, August 22, 2015	Sheet 32 of 37	

5/23 CB6 25V 0805 change 10V 0603

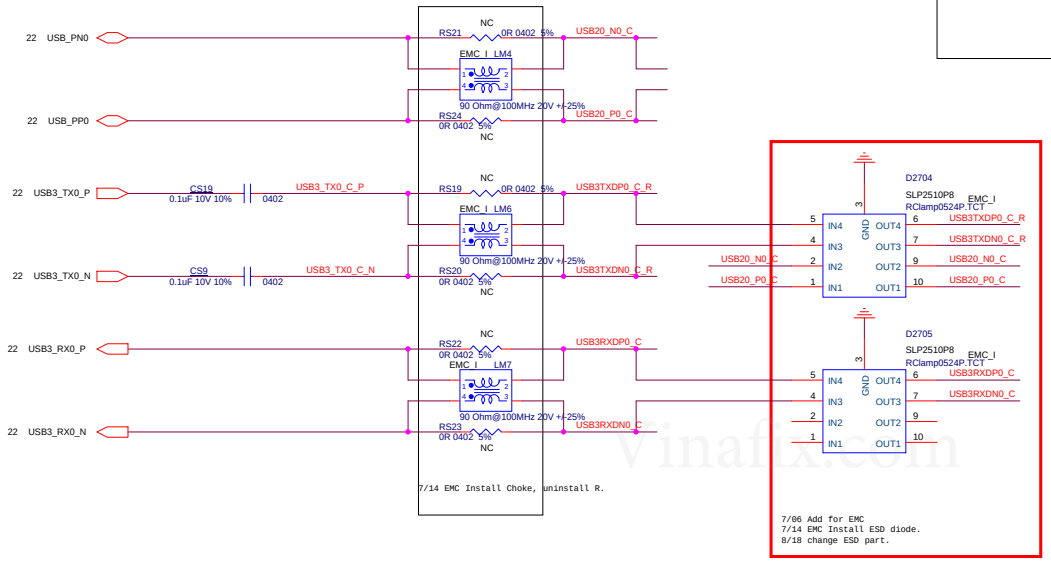
2A/Stack Port



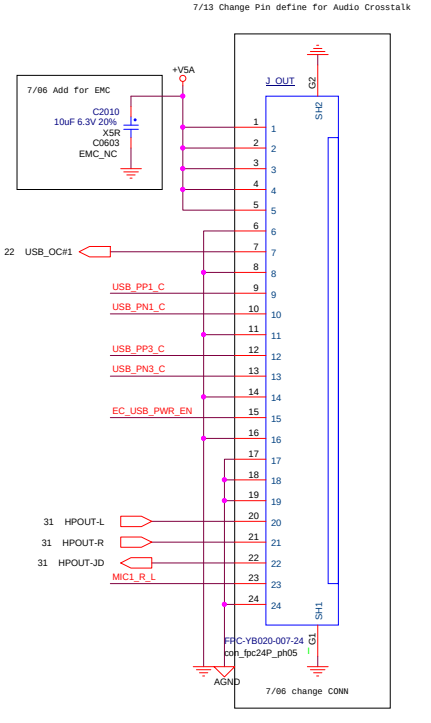
5/18 Remove Charger IC



5/23 UB1 change IC

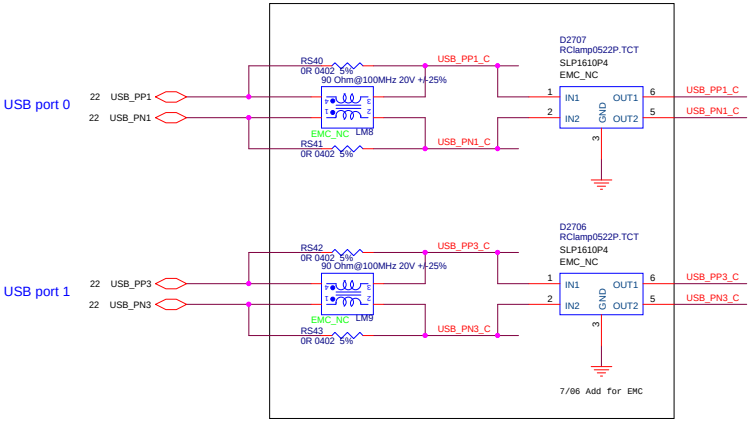


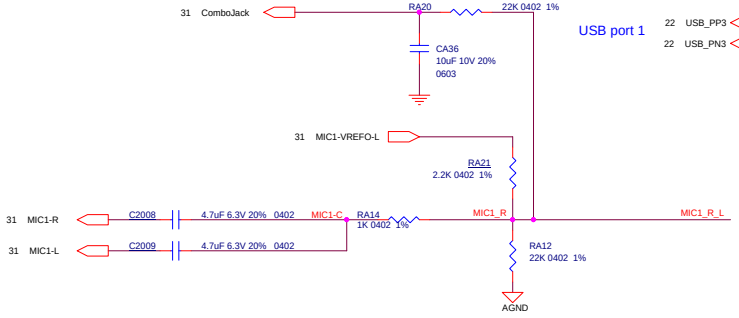
USB2.0/USB3.0 port 1



USB port 0

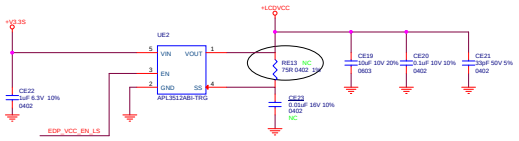
USB port 1





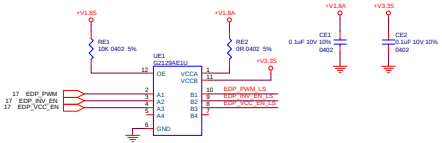
+V5A +V5A 7,10,12,13,14,15,16,22,28

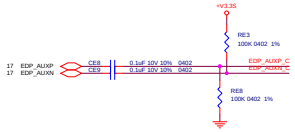
3nod三诺	Project:	LENOVO_NB116BT	
	Engineer:	Jason	
Size: C	Title:	USB 3.0/2.0 Conn	Rev: V01
Date: Saturday, August 22, 2015	Sheet 33 of 37		

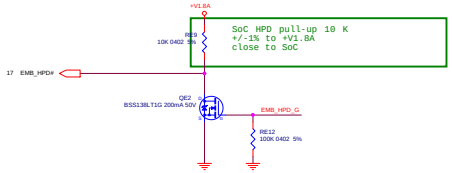


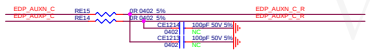
add RE13 when UB2 is NCT3521U

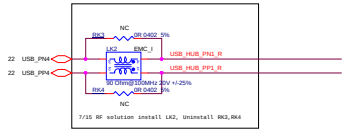
UE2	RE13
APL3512A	NI
NCT3521U	I

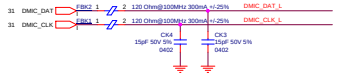




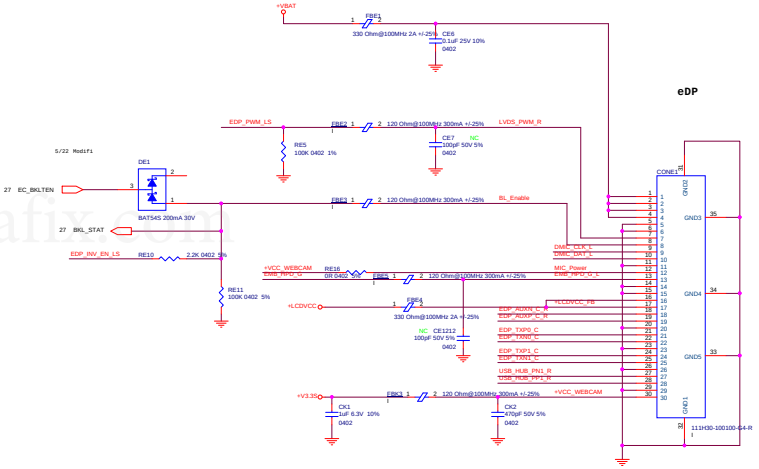








5/22 Del



BIOS_LABEL
Printed Circuit Board
BIOS_LABEL
BIOS Licence Control Label,10X10,ROHS NI

Project: LENOVO NB116BT			
Engineer: Jason			
Size: A	Title: eDP & CAM		Rev: V01
Date: Saturday, August 22, 2015	Sheet 34 of 37		

EE SDV to SIV

6/25 Page.27 Add Reset IC U2702 circuit.
6/25 Page.28 Change Touch PAD Pin define and Power(5V), follow 11" pin define.
6/25 Page.28 Reserve Touch PAD Click PU.
6/25 Page.29 Change RCR12 from PU to NC, SOC already have internal PU.
6/25 Page.30 Change eMMC Power from "S" change to "A", "S" will leak voltage.

6/30 Page.28 Change HDMI CONN, for production.
6/30 Page.33 Change USB3.0 CONN, for production.
6/30 Page.31 Del DA1 Pin.2 (HDA_RST_AUDIO#), HDA_RST_AUDIO# level(1.8V) different with Audio PD# Pin(3.3V).

7/01 Page.31 Change Speaker Pin define, follow EA pin define.
7/01 Page.30 Del eMMC reserve +V3.3S and RS14, it will not used.

7/02 Page.27 Install RI13, Uninstall RI20, for Change Version ID to SIT build.
7/02 Page.21 RX45 from 2.7K change to 1K, raise voltage level.

7/03 Page.20 Install RX172,RX173 , Uninstall QX9, change level to 1.8V.
7/03 Page.21 Install RX174,RX175,RX176,RX177,RX180,RX181 , Uninstall QX2,QX3,QX5, change level to 1.8V.
7/03 Page.19 Remove UX3 ROM Socket, on board BIOS ROM.
7/03 Page.27 Remove UI1 ROM Socket, on board EC ROM.
7/03 Page.29 Uninstall RT3, Install RT1402, for change level to 1.8V.
7/03 Change QCR1,QX2,QX3,QX4,QX5,QX7,QX9,QX11,QX12,QX13 from NX3008NBKS to LBSS138DW1T1G, follow SDV SMT part.
7/03 Page.27 Add Reserve RI76
7/03 Page.33 Change USB Daughter Board Conn to 24Pin.

7/08 Page.27 Uninstall QX12,QX13, SMB don't need connect to SOC.

7/08 Page.22 Add R9062,R9063, reserve RX166,RX167, add Port0 to UART debug.

7/13 Page.20 CX9,CX10 from 18pF Change to 15pF, reference vendor crystal test.
7/13 Page.31 CA20,CA21,CA22 from Caps Change to 0 ohm RA15,RA16,RA17, for Audio crosstalk test.
7/13 Page.33 Change J_OUT Conn pin define, For Audio Crosstalk issue.
7/13 Page.27 SKU1,2,3 Uninstall R9059, test EC control reset.

7/16 Page.18 RX170 change from 100K to 10K, follow CRB.

7/17 Page.28 RH24,RH25,RH26,RH27,RH29,RH30,RH31,RH32 change from 0 to 12 ohm, EMC solution.
7/17 Page.21 Change YX2 CL=7pF, CX12,CX13 change to 5pF, Vendor suggestion.
7/17 Page.18 RX171 Change from 0 ohm to 1K ohm, fix signal glitch.
7/17 Page.27 Uninstall Reset IC circuit, EC could support it.

EE SIV to SVOP

8/12 Page.28 OR10 change from 150 ohm to 330 ohm, for LED brightness.
8/17 Page.27 Change SW1,SW2 for ME issue.
8/17 Page.27 Install RI21, Uninstall RI25, for version ID.
8/18 Page.08 Add reserve CON0803, for SMT CONN.
8/18 Page.21 Change CX12,CX13 from 5pF to 5.6pF, Vendor suggestion.
8/18 Page.20 Uninstall RX172, for thermal shutdown.
8/18 Page.29 Install RT3, Uninstall RT1402, for thermal shutdown.
8/19 Page.18 Add RX195 o ohm.
8/21 Page.28 Change LED connection, for S5 power consumption.

Already Sent ECN To Vic

12/15 Page.28 Add CH9 (install) & DCRH1(noninstall) to circuit to solve HDMI hot plug ESD issue.

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EMC

7/06 Page.29 Add ESD D2710,D2711.
7/06 Page.28 Add ESD D2708,D2709,C2011,C2012
7/06 Page.33 Add ESD D2703,D2704,D2705,D2706,D2707,CR1,C2010,LM8,LM9,RS40,RS41,RS42,RS43

7/14 Page.33 Install D2703,D2704,D2705,LM4,LM6,LM7, Uninstall RS19,RS20,RS21,RS22,RS23,RS24.

7/15 Page.34 RF solution install LK2, uninstall RK3,RK4.
7/15 Page.28 RH24,RH25,RH26,RH27,RH29,RH30,RH31,RH32 Change from 0 ohm to 22 ohm.
Already Sent ECN To Vic

7/16 Page.16 Add reserve RF plane Caps.

8/17 Page.17 Add CX108 5pF in SDMMC3_CLK_R.
8/18 Page.33 Change D2703,D2704,D2705 ESD part, for cost.
8/18 Page.31 Move CA476,CA477,CA480,CA481 close to SOC.
8/18 Page.31 Install CA474,CA475,CA478,CA479.

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SDV to SIT

POWER CHANGE LIST

6/29 Page.8 Change Gauge IC circuit. Change CN0802 pin definition. Pin4 BATT_ID2 ==> BATT_ID. Pin5 BATT_ID1 ==> BATT_TSN Pin6 BATT_THER ==> BATT_TSP Pin7/8/9/10/11 GND ==> BAT_GND
7/1 Page.10 Add C1028/C1029 10uF 25V on VBAT_+V3.3A_+V5A.
7/1 Page.13 Change R1302 from 25.5k to 13k and R1329 from 20k to 24k.
7/1 Page.14 Change R1402 from 35.7k to 18k and R1429 from 20k to 24k.
7/3 Page.8 Add JP0801 between +VCHG and BATT+.
7/3 Page.9 Change C0913 ground from GND to SGND_CHG. Change C0913 value from 2.2uF to 4.7uF.
7/7 Page.10 Add R1028 200ohm.
7/8 Page.8 Add R0840 10k to pull high +V3.3AL on EC_BATT_ID2. Non-pop R0830,C0821,R0825,R0827,Q0801,Q0802,R0828,C0822
7/8 Page.13 Pop C1312 1000pF.
7/8 Page.14 Pop C1412 1000pF.
7/9 Page.10 Delete D1004,D1005,R1011.

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