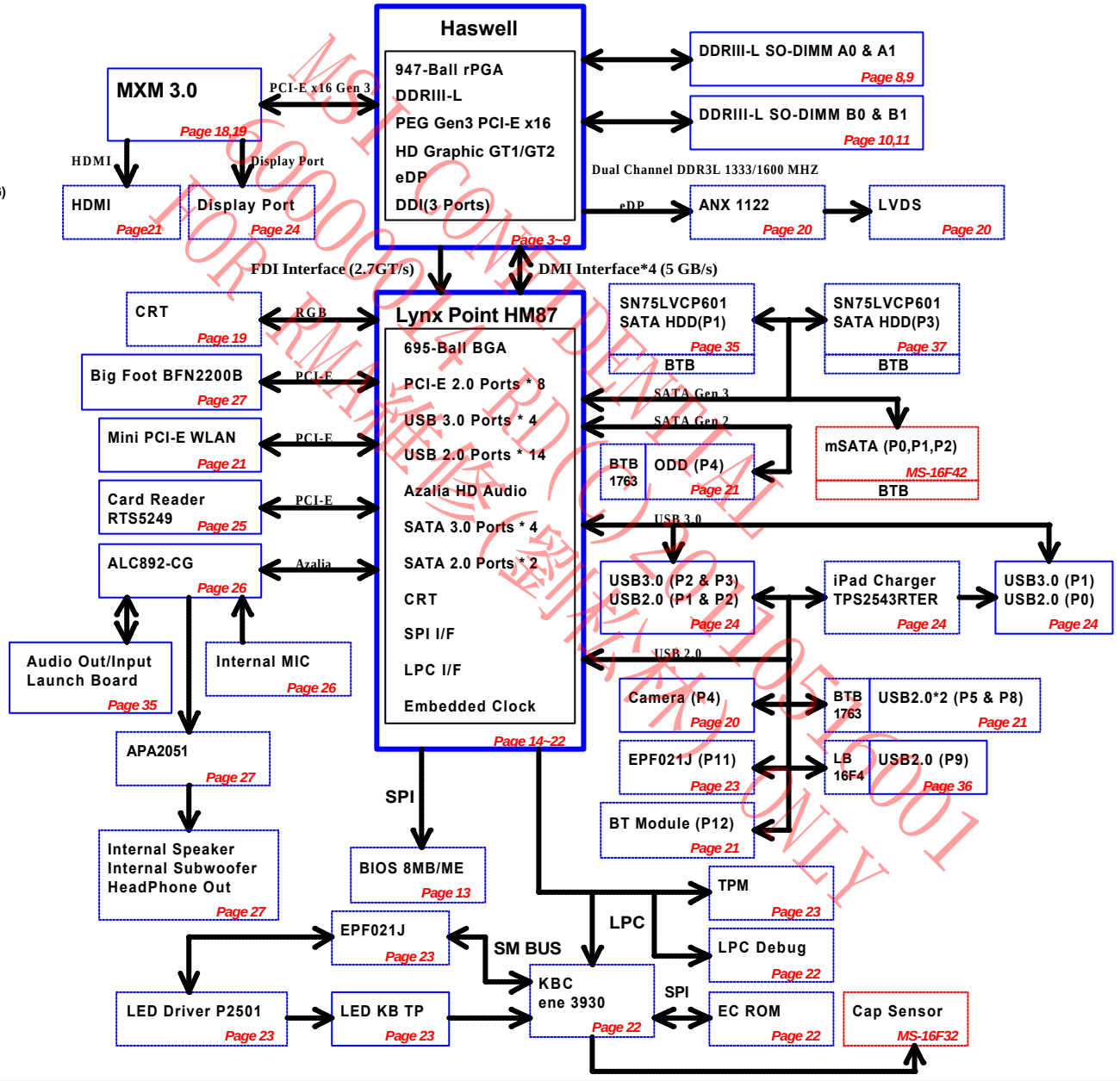
Shark Bay Platform

MS-1763 Ver.0A 2012/10/24



MICRO-STAR INT'L CO.,LTD.

Block Diagram

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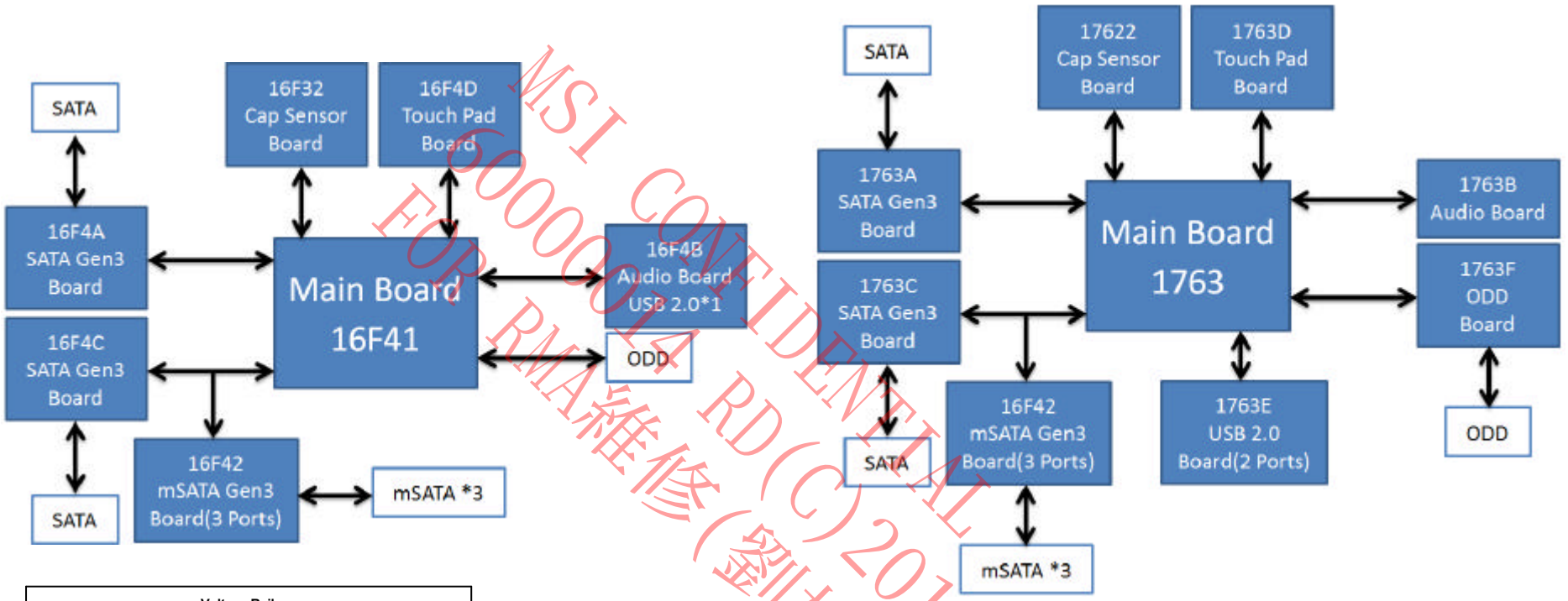
Board Diagram

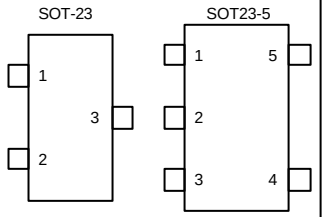


Voltage Rails			
Power Plane	**Voltage**	**Active In**	**Description**
PWR_SRC	19V or 12 V	S0, S3-S5	Power Source
+5VALW	5V	S0, S3-S5	
+3VALW	3.3V	S0, S3-S5	
+5VSUS	5V	S0, S3	
+3VSUS	3.3V	S0, S3	
+1_35VDIMM	1.35V	S0, S3	DDR3L Power
+5VRUN	5V	S0	
+3VRUN	3.3V	S0	
+1_5VRUN	1.5V	S0	PCH Power for I/O
+12V_FAN	12V	S0	Fan Power
+15V	15V	S0	LED Keyboard Power
+0_675VRUN	0.675V	S0	
+1_05VRUN	1.05V	S0	
+VCC_CORE	1.2V	S0	Processor Core Power Rail

Net Naming Conventions
Suffix
= Active Low Signal
Prefix
H = Host M = DDR Memory TP = Test Point (does not connect anywhere else)

Power States						
	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+V*SUS	+V*RUN
S0 (Full on)	**High**	**High**	**High**	**On**	**On**	**On**
S3 (Suspend to RAM)	Low	**High**	**High**	**On**	**On**	Off
S4 (Suspend to Disk)	Low	Low	**High**	**On**	Off	Off
S5 (Soft off)	Low	Low	Low	**On**	Off	Off

PCB Footprints



msi MICRO-STAR INT'L CO.,LTD.

Platform

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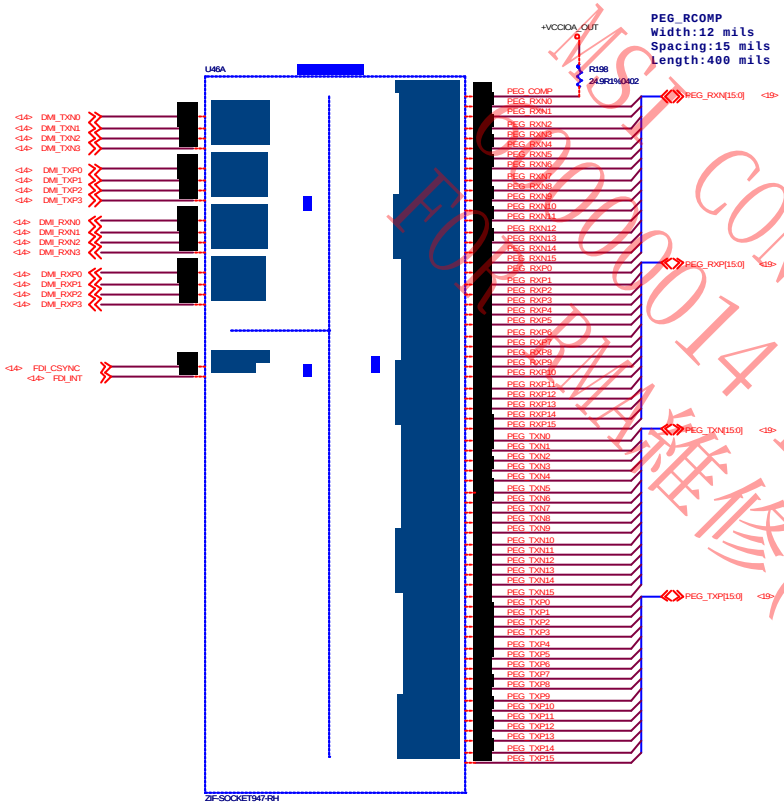
MS-17631 Change List

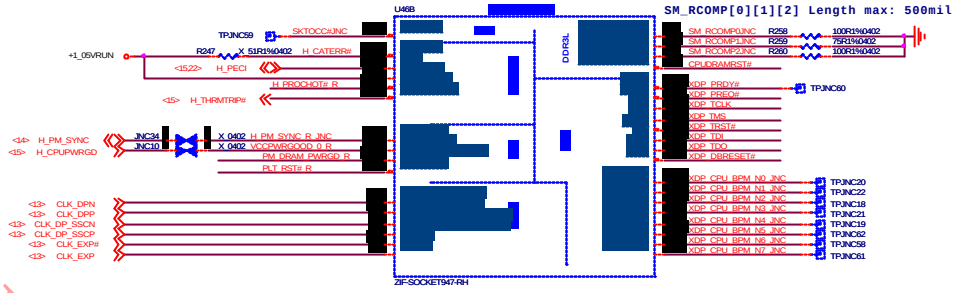
Date	Page	Description	Date	Page	Description	Date	Page	Description
2012.10.22								

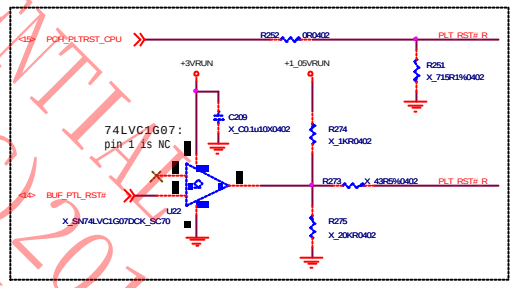
Haswell Processor (DMI,PEG,FDI)

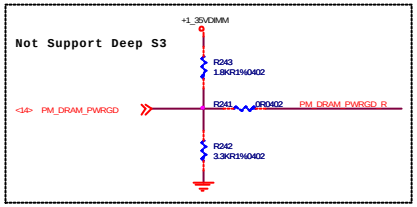


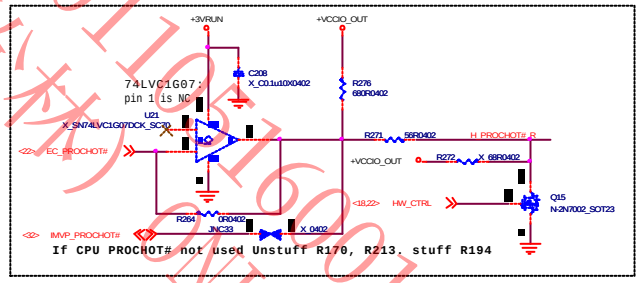
Haswell Processor (CLK,MISC,JTAG)

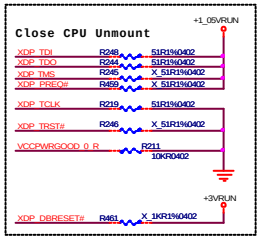
SM_RCOMP[0] Width:15mil Spacing:20mil
SM_RCOMP[1] Width:15mil Spacing:20mil
SM_RCOMP[2] Width:15mil Spacing:20mil
SM_RCOMP[0][1][2] Length max: 500mil

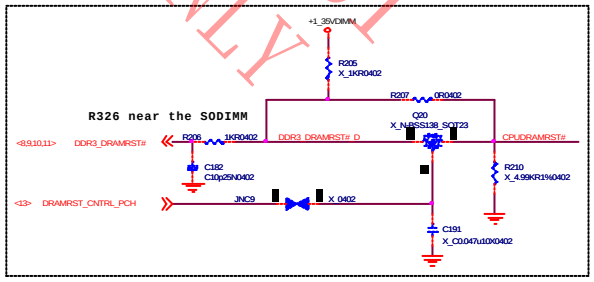












MICRO-STAR INT'L CO.,LTD.	
CPU(DMI,PEG,FDI/CLK,MISC,JTAG)	
MS-17631	0A
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Haswell Processor (DDR3)

msi	MICRO-STAR INT'L CO.,LTD.		
Processor (DDR3)			
MS-17631			0A
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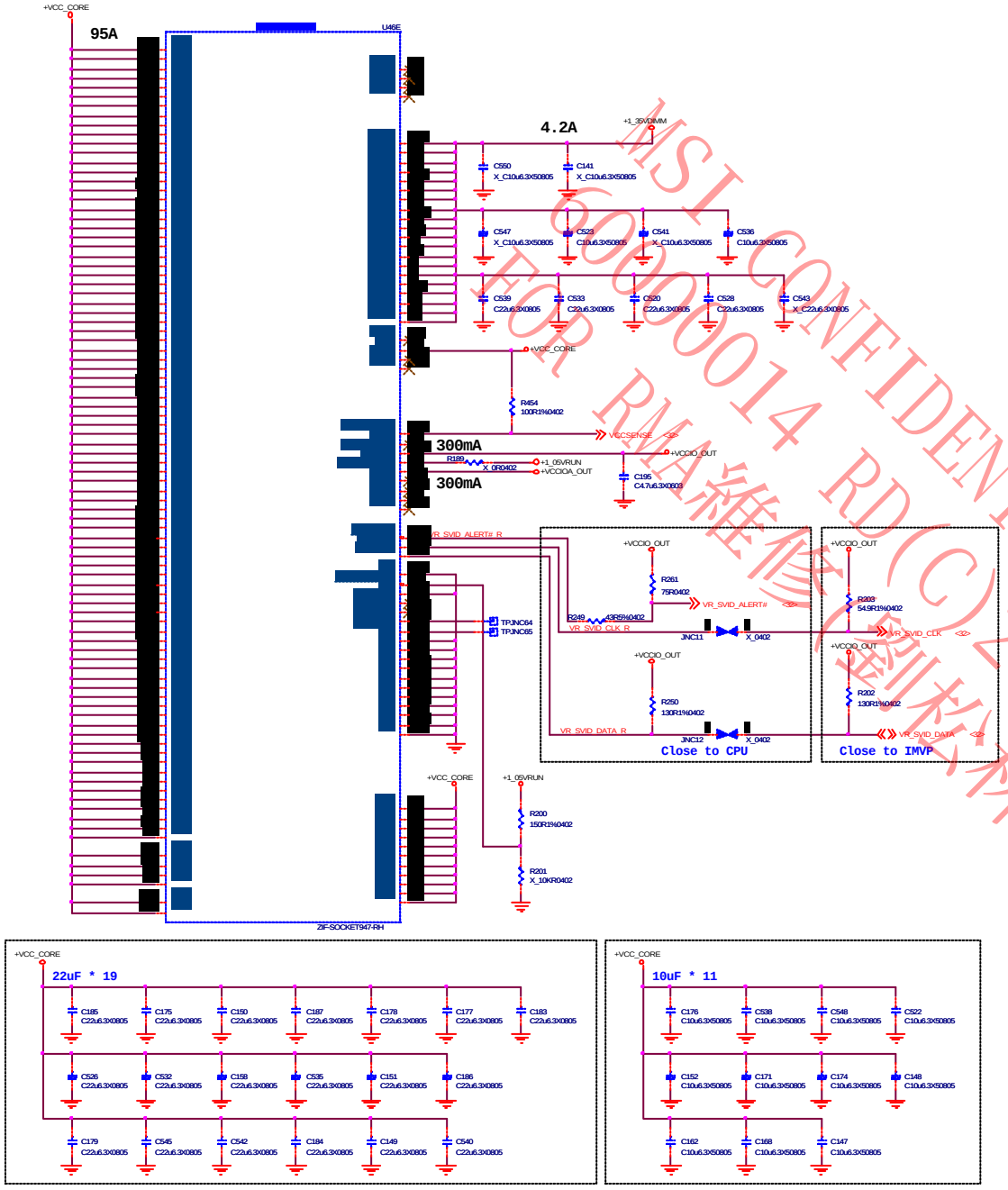
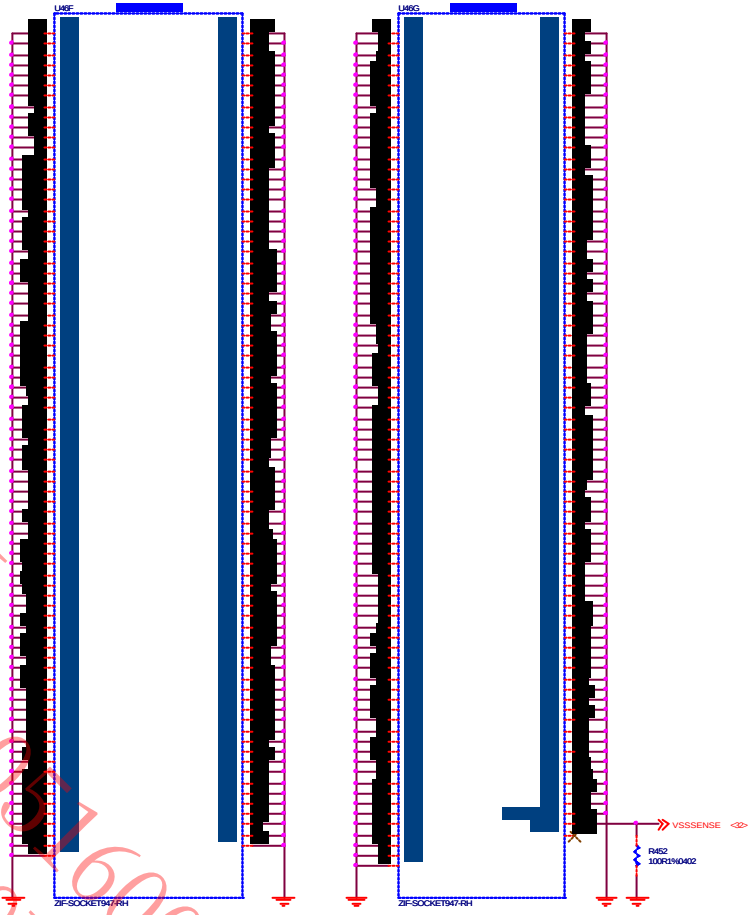
Haswell Processor (Power)



Haswell Processor (Gnd)



MICRO-STAR INT'L CO.,LTD.

Processor (Power/Gnd)

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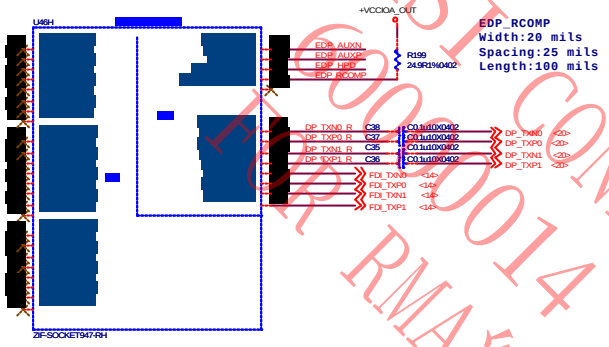
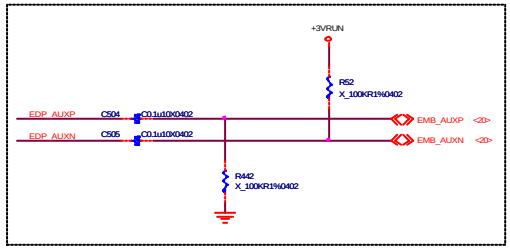
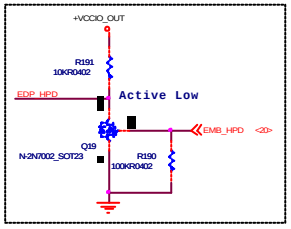
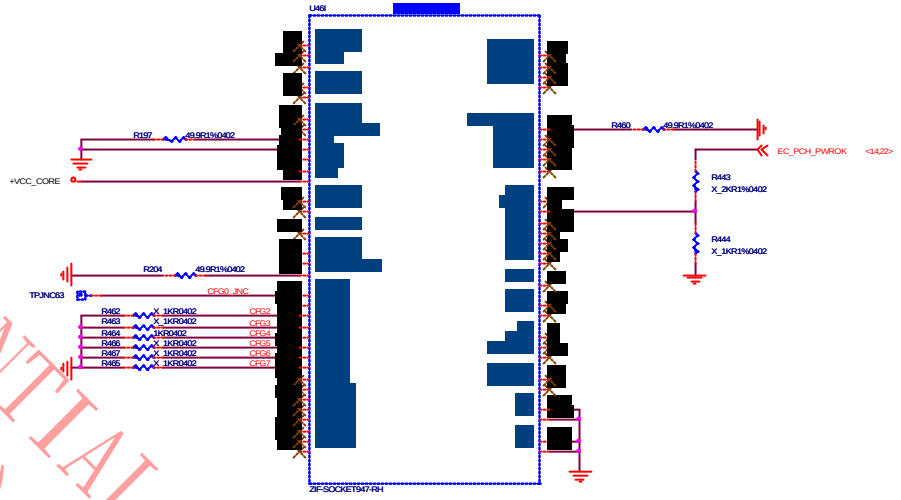
Haswell Processor (Display)







Haswell Processor (Reserved)



PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP Enable	
CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

MICRO-STAR INT'L CO.,LTD.

Processor (Display/Reserved)

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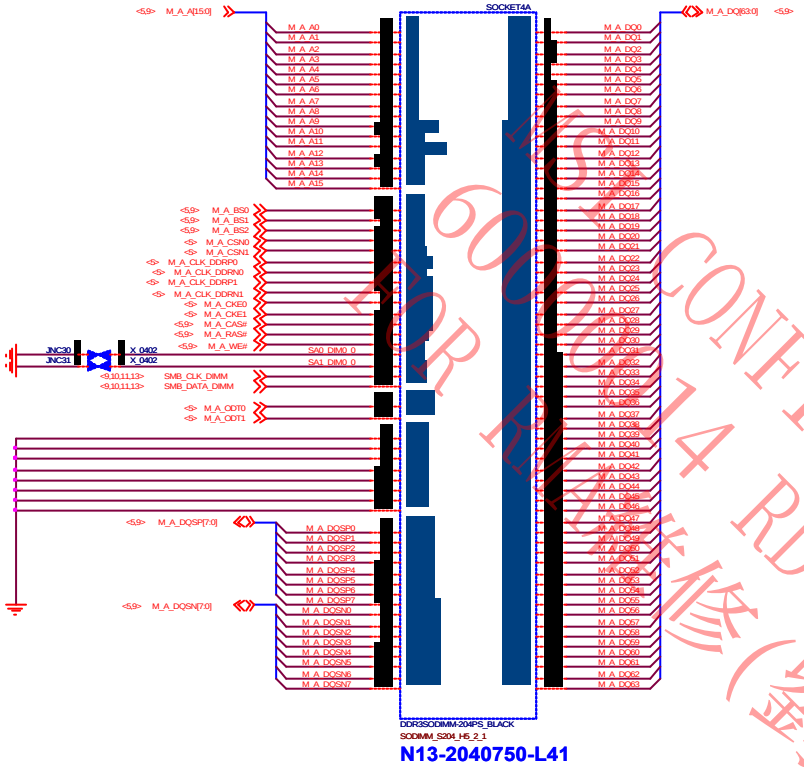
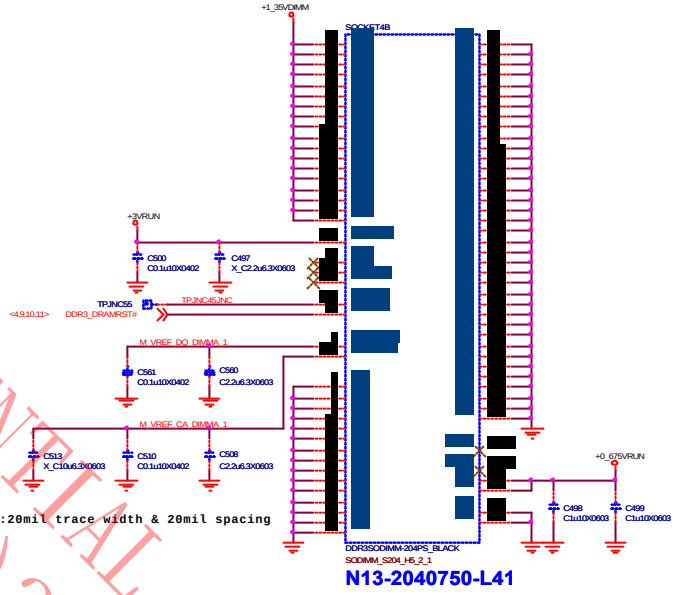
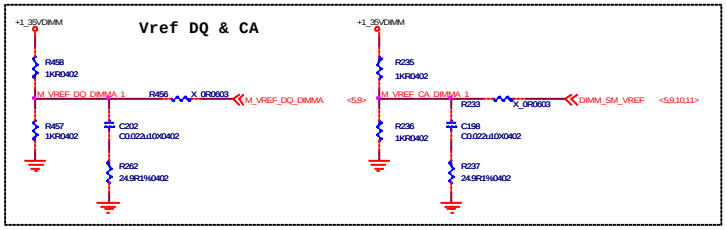
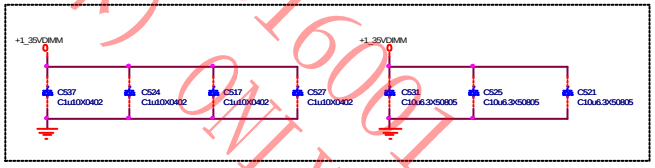
SODIMM #A0









MICRO-STAR INT'L CO.,LTD.	
DDR3 SODIMM A0	
MS-17631	0A
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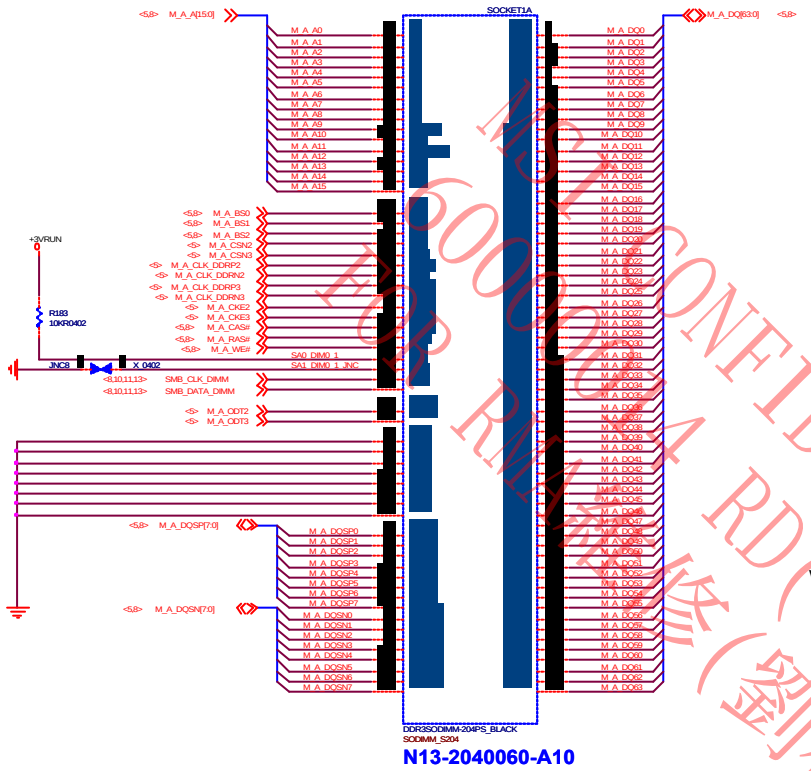
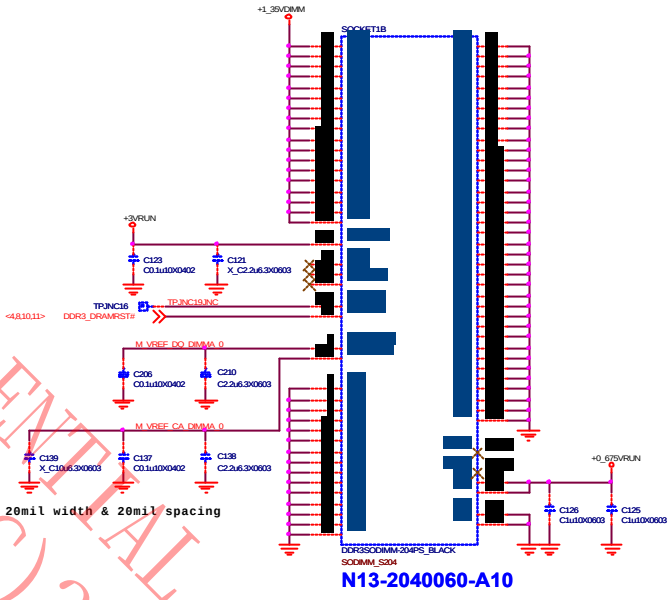
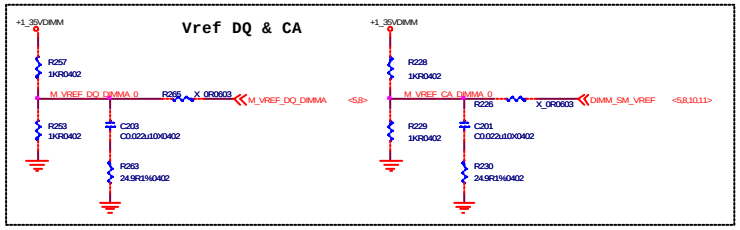
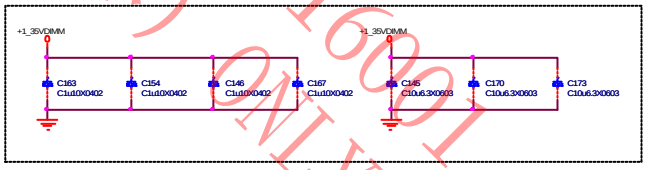
SODIMM #A1









MICRO-STAR INT'L CO.,LTD.	
DDR3 SODIMM A1	
MS-17631	0A
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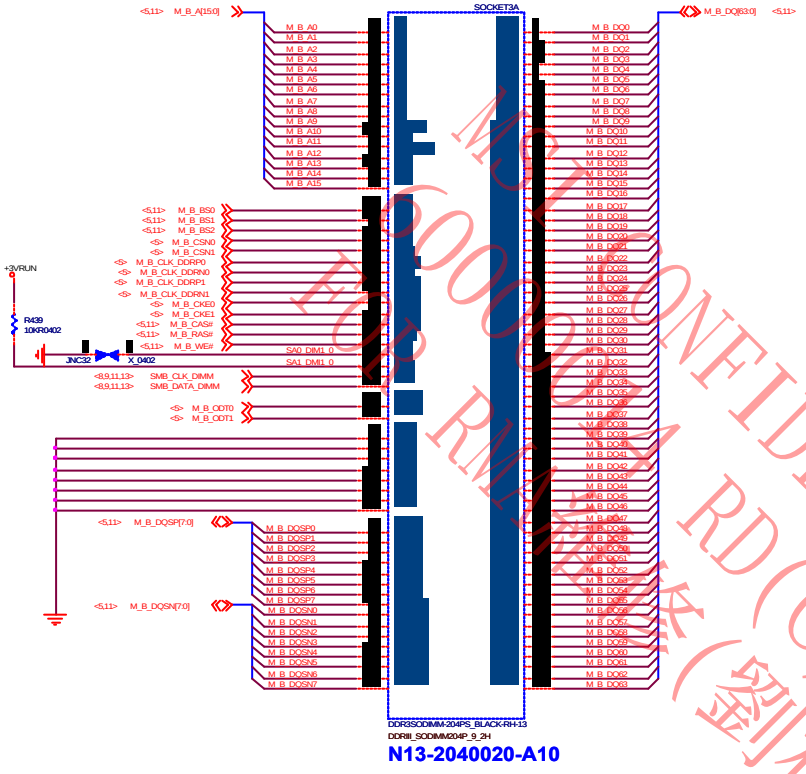
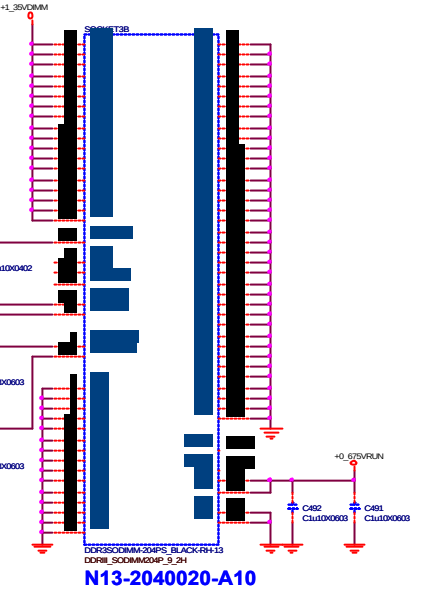
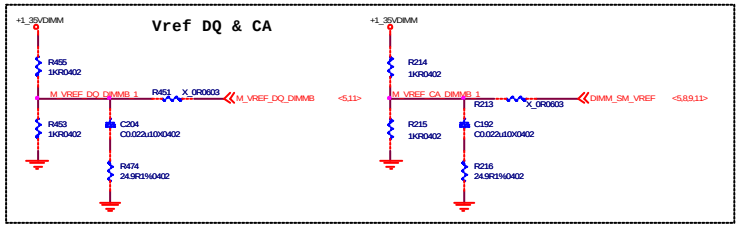
SODIMM #B0

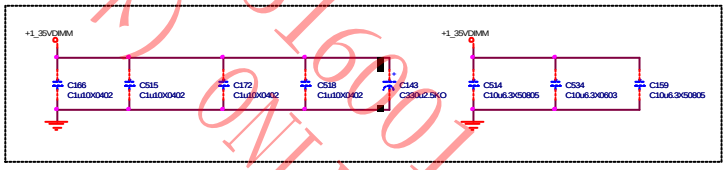


N13-2040020-A10



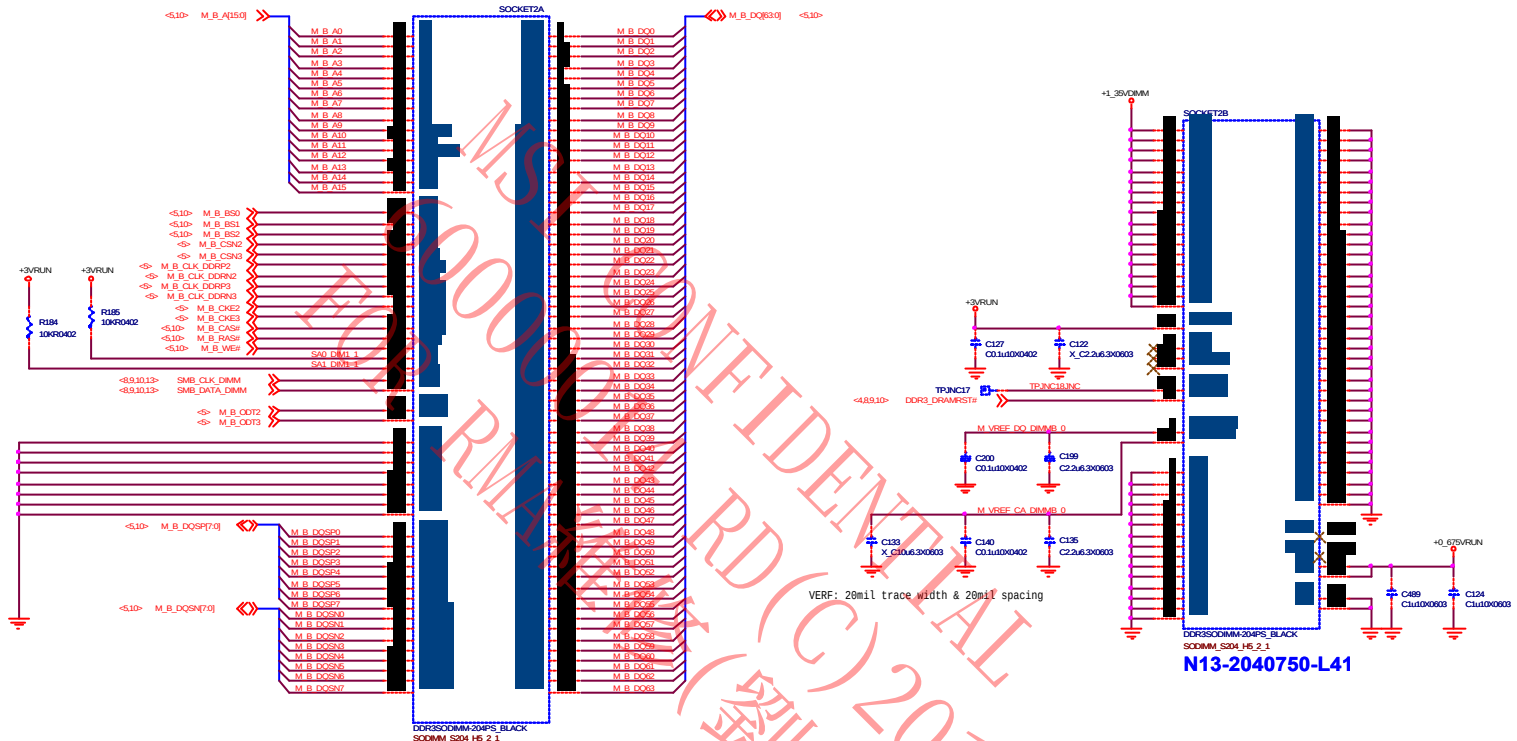
N13-2040020-A10

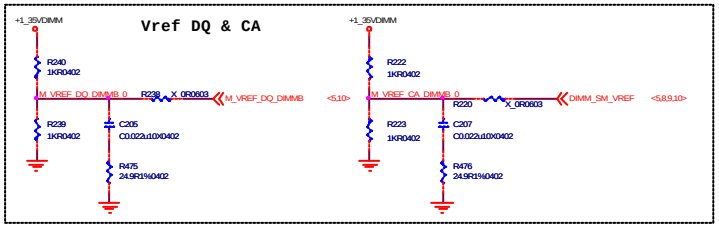


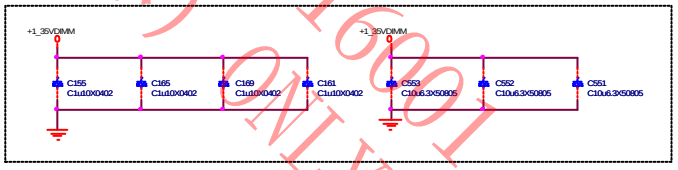


msi	MICRO-STAR INT'L CO.,LTD.
DDR3 SODIMM B0	
MS-17631	0A
Date: Tuesday, November 13, 2012	Sheet 10 of 42

SODIMM #B1







MICRO-STAR INT'L CO.,LTD.	
DDR3 SODIMM B1	
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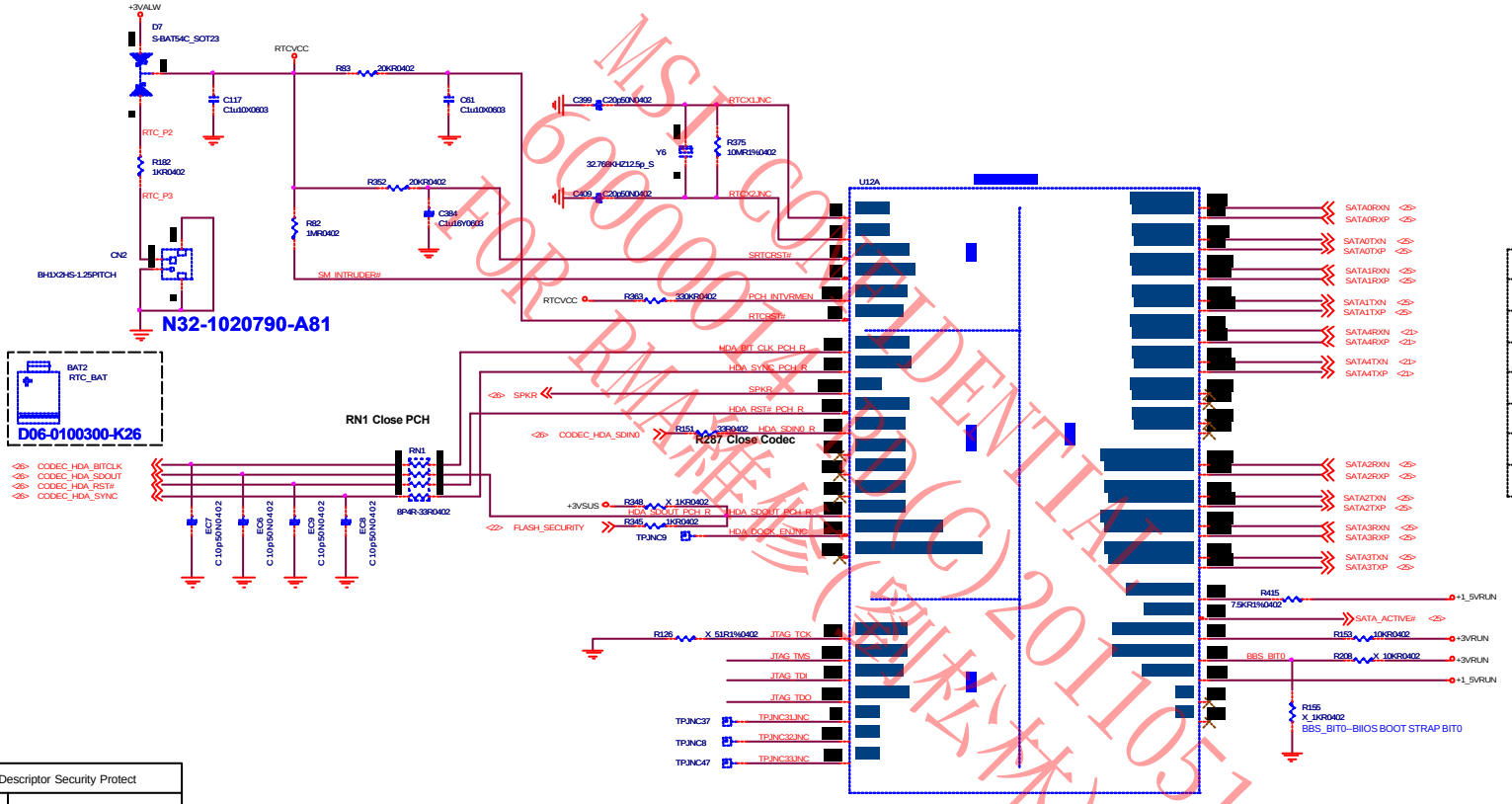
Lynx Point (HDA,JTAG,SATA)



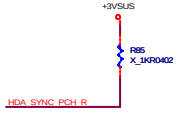
SATA	
Port	Device
0	mSATA Gen3(6Gb/s)
1	mSATA Gen3(6Gb/s)
2	ODD(Gen2)
3	NC
4	mSATA Gen3(6Gb/s)
5	To A board(Gen3)

Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

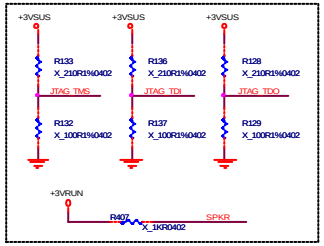
Signal has a weak internal pull-down
Note: The weak internal pull-down is disabled after PLTRST# deasserts.

SPK	The Signal has a weak internal pull-down Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)

Reserved for Codec use RUN.



HDA_SYNC signal also serves as a strap for selecting VRM voltage to the PCH.
The strap is sampled on the rising edge of RSMRST# signal.
Due to potential leakage on the codec (path to GND), the strap may not be able to achieve the Vihmin at PCH input.
Therefore, platform may need to isolate this signal from the codec during the strap
phase. The following example circuits maybe used to achieve this purpose.



MICRO-STAR INT'L CO.,LTD.
Lynx Point (HDA,JTAG,SATA)
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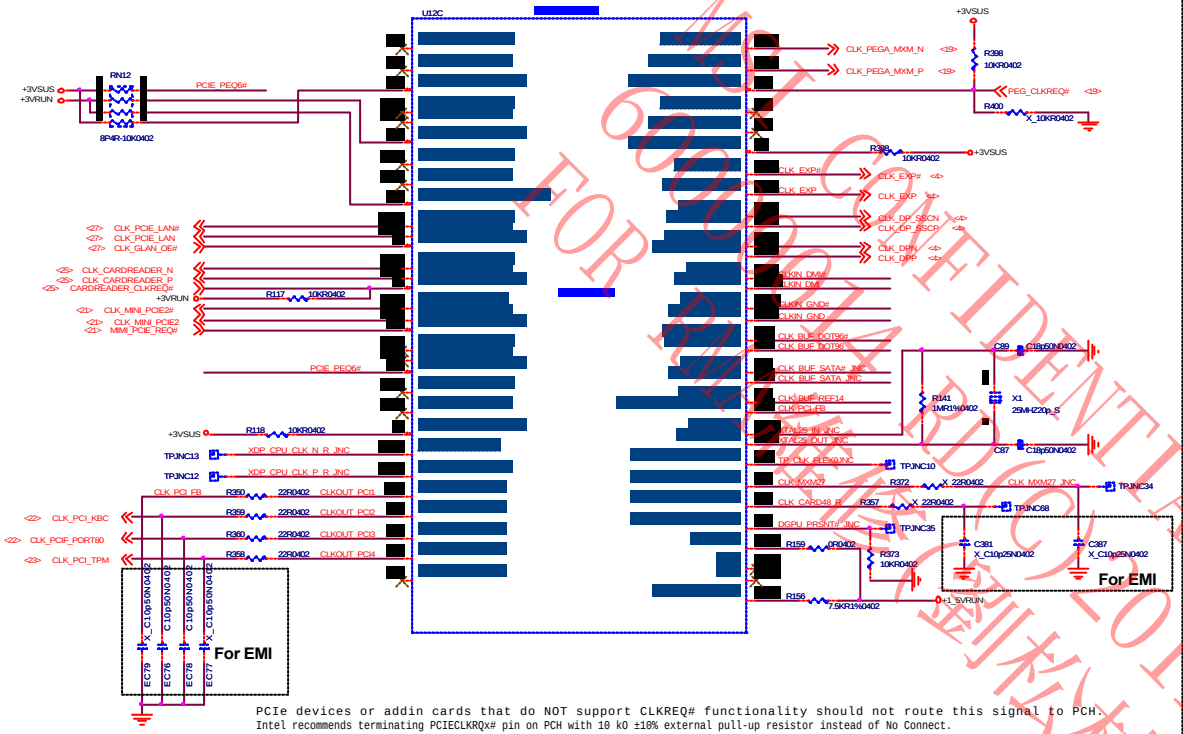
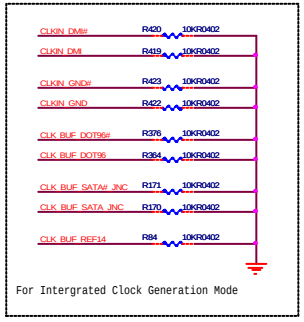
Lynx Point (Clock)

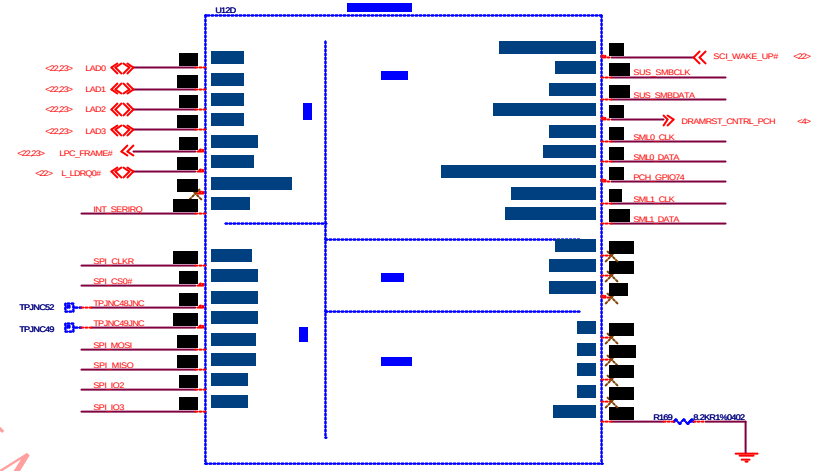


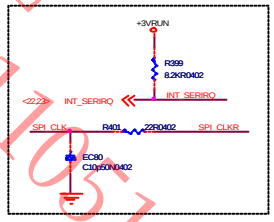
PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 kO ±10% external pull-up resistor instead of No Connect.
Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.

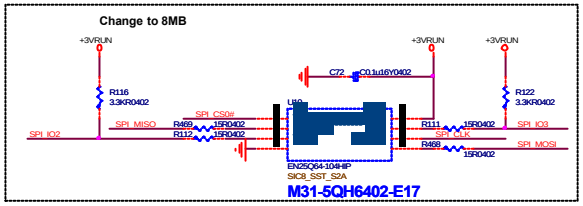
***Disable PCIE OBFF(BIOS)**

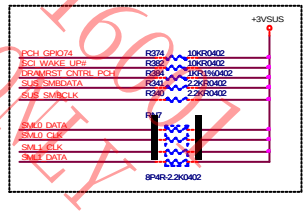


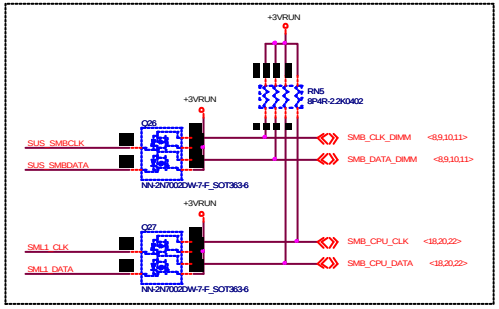
Lynx Point (LPC,SMBUS)











MICRO-STAR INT'L CO.,LTD.

Lynx Point (Clock/LPC,SMBUS)

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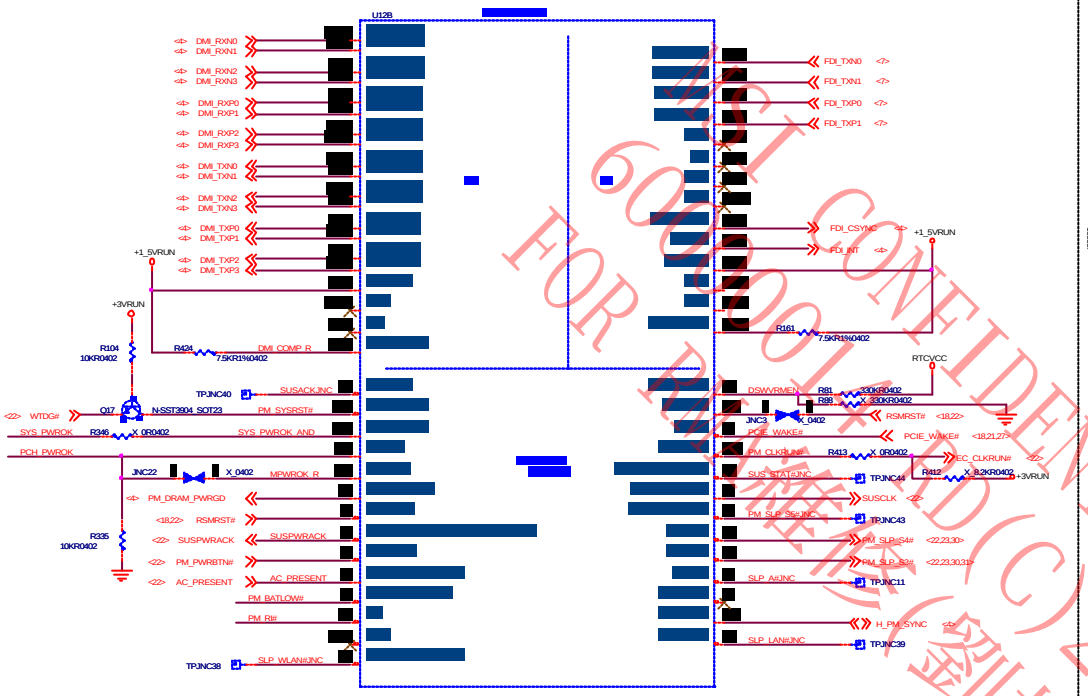
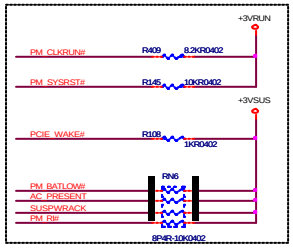
Lynx Point (DMI,FDI)





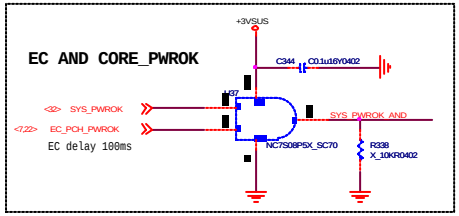
VRM (SUSCLKGPIO62)
High-Enable
Low-Disable

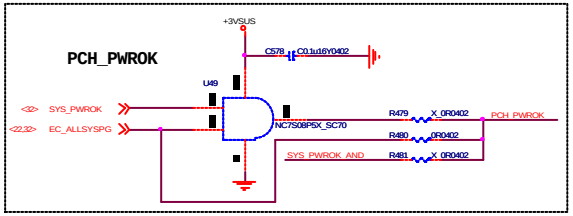
APWROK
not supporting Intel AMT
it can be connected to PWROK

GPIO31 --If not used,require pull up 3VSUS

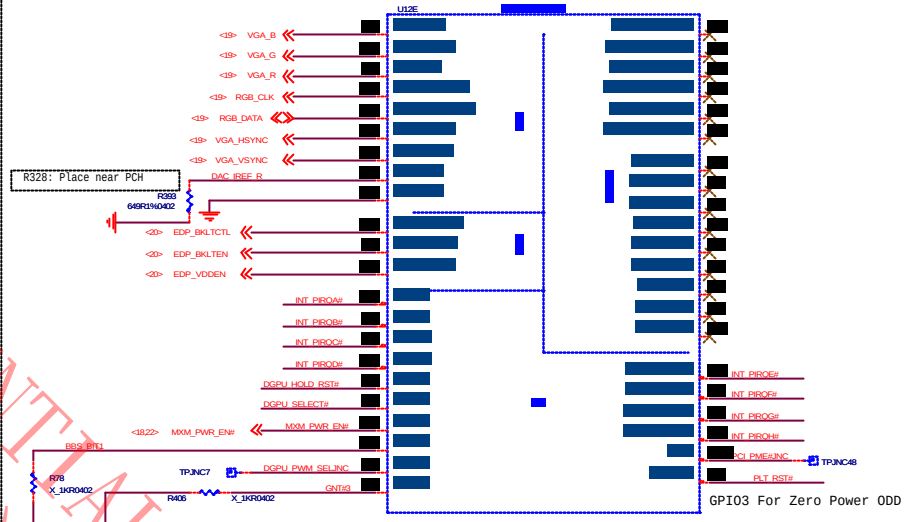
DSWODVREN - On Die DSW VR Enable
High --- Enable internal 1.05V regulator
Low --- Disable

DPWROK
Without deep s4/s5 support
tied together with RSMRST#

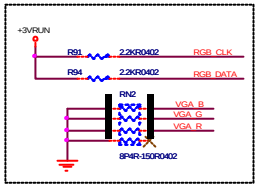


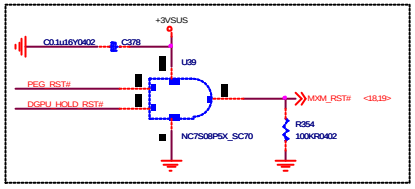


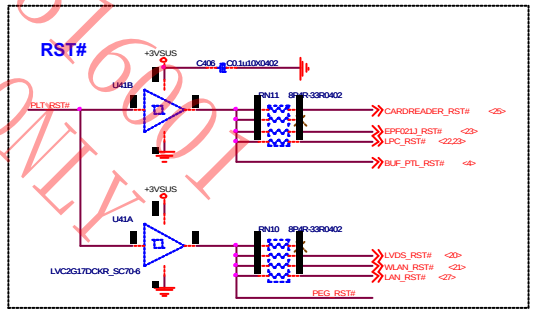
Lynx Point (PCI,DDI)

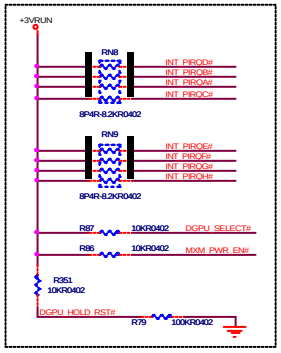


BIOS BOOT STRAP BIT		
BBS_BIT0	BBS_BIT1	BOOT BIOS LOCATION
0	0	LPC
0	1	RESERVED(NAND)
1	0	N/A
1	1	SPI









MICRO-STAR INT'L CO.,LTD.		
Lynx Point (DMI,FDI/PCI,DDI)		
MS-17631		0A
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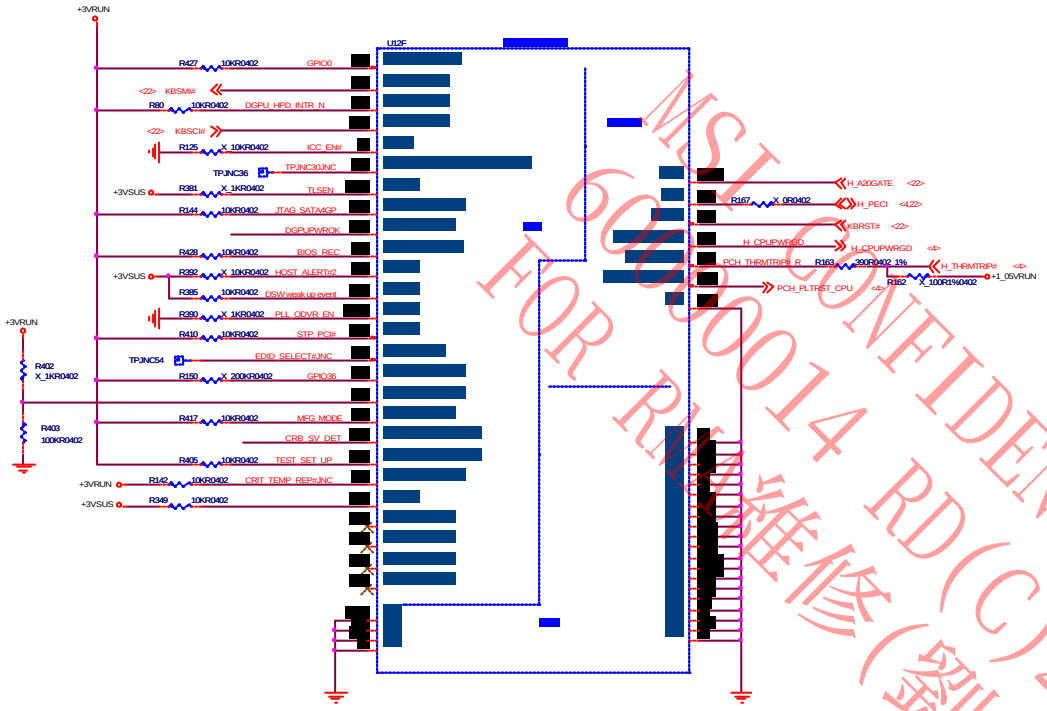
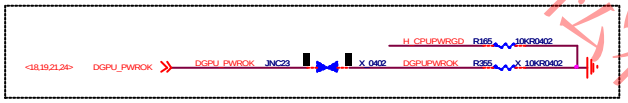
Lynx Point (GPIO,MISC)





PLL ON DIE VR_ENABLE

GPIO28	Internal pull high (Enable)
	Low: Disable

+3VSUS
R394 X_10KR0402
PLL_ODVR_EN

GPIO28 has a weak internal pull-up.
The internal pull-up is disabled after RSMRST# deasserts.

SATA3GP/GPIO37
This signal has a weak internal pull-down.
NOTE:
The internal pull-down is disabled after PLTRST# deasserts.
NOTE:
This signal should not be pulled high when strap is sampled.

No USED

+3VRUN
CRB_SV_DET
R139 X_10KR0402
R140 X_100KR0402

CRB_SV_DET	
GPIO39	High: External GFX
	Low: Internal GFX

This signal has a weak internal pull-down.
NOTE:
The internal pull-down is disabled after PLTRST# deasserts.

GPIO36 --CRB connector to 3V

GPIO36
R149 10KR0402

GPIO0 & 6 & 16 & 17 & 22 & 34 & 38 & 48 --If not used,require pull up 3VRUN

GPIO57 --If not used,require pull up 3VSUS

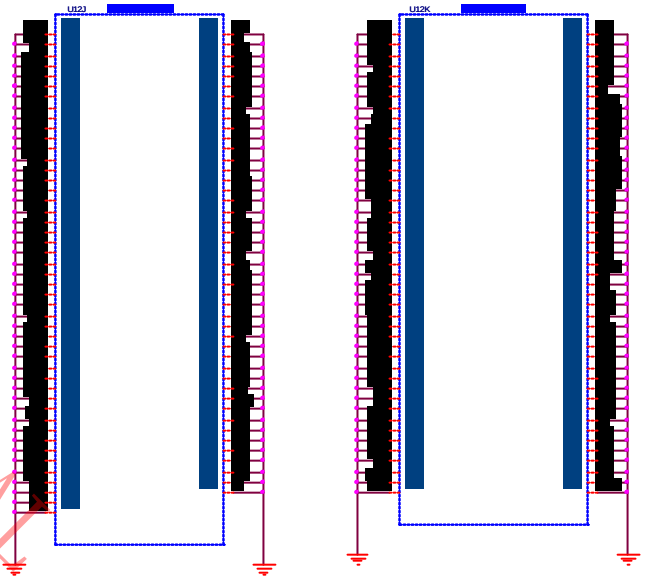
GPIO15--Not support AMT,Transport Layer Security Disable(High is support TLS,internal pull-down)

GPIO27 is deep S4 & S5 weak up event,internal pull high.& It's VCCFDIPLL internal VRM strapping pin

GPIO35 --Define to EDID Select (If not used,require pull down)

SATA2GP/GPIO36 (net name: FDI_OVRVLTG) & SATA3GP/GPIO37 (net name: SATA_ODD_PRSNT#)
Sampled at Rising edge of PWROK.
Weak internal pull-down. (weak internal pull-down is disabled after PLTRST# de-asserts)
NOTE: This signal should NOT be pulled high when strap is sampled

Lynx Point (Gnd)



MICRO-STAR INT'L CO.,LTD.

Lynx Point (GPIO,MISC/Gnd)

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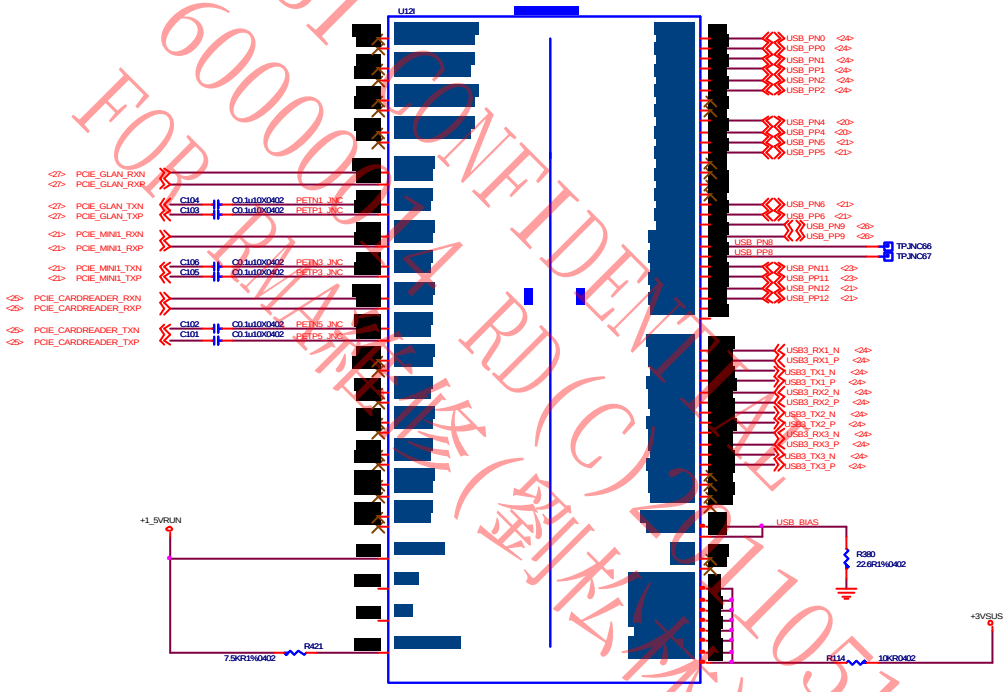
Lynx Point (PCIE,USB)

PCI-E	
Port	**Device**
3	Giga Lan
4	Mini PCIE-WLAN
5	Card Reader



USB			
USB 2.0	**USB 3.0**	**Device**	**Note**
0	1	USB 3.0 Port 1	
1	2	USB 3.0 Port 2	Debug Port
2	5	USB 3.0 Port 3	
3			NC
4		WebCam (LVDS)	
5		USB 2.0 Port 5 (1763)	
6			NC
7			NC
8		USB 2.0 Port 5 (1763)	
9		USB 2.0 Port 5 (16F4)	Debug Port
10		TestPad	
11		EPF LED (8051)	
12		Mini PCIE-BT	
13			NC
	3		NC
	4		NC
	6		NC

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Lynx Point (PCIE,USB)
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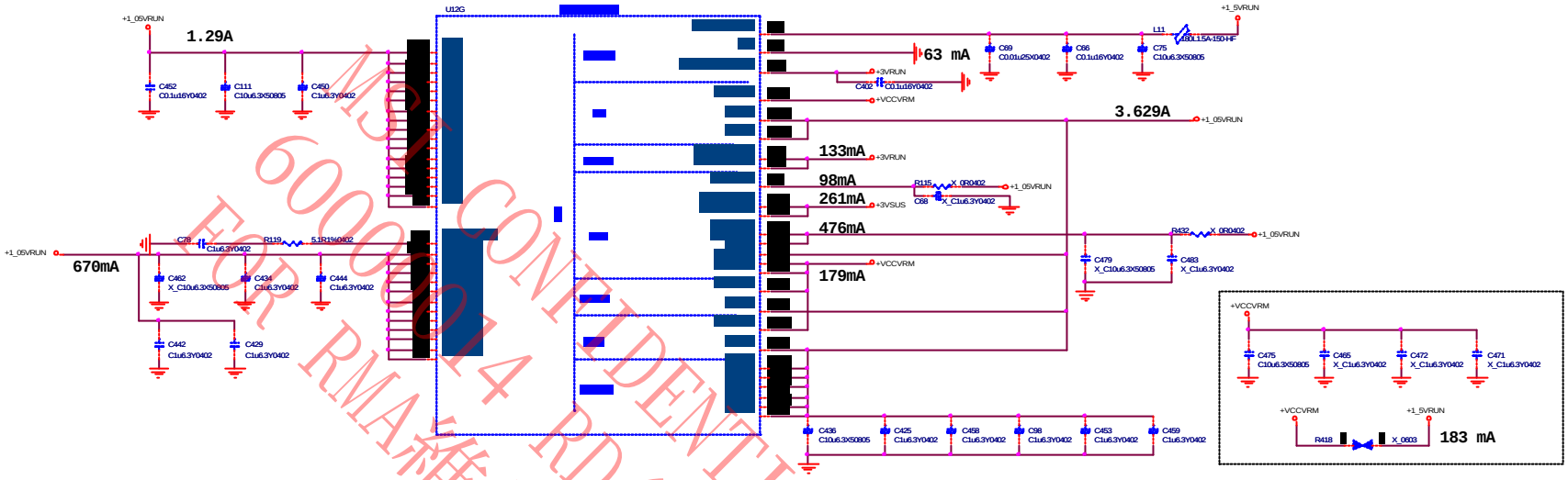
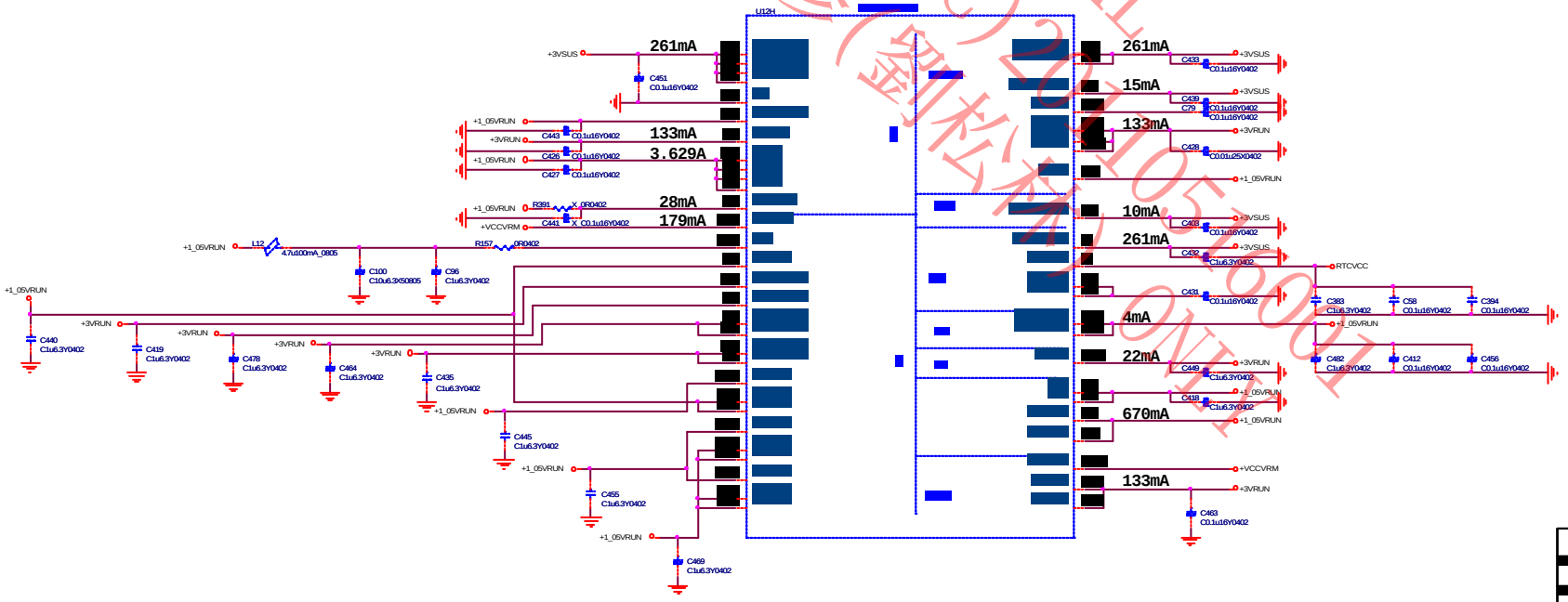
Lynx Point (Power)





MICRO-STAR INT'L CO.,LTD.

Lynx Point (Power)

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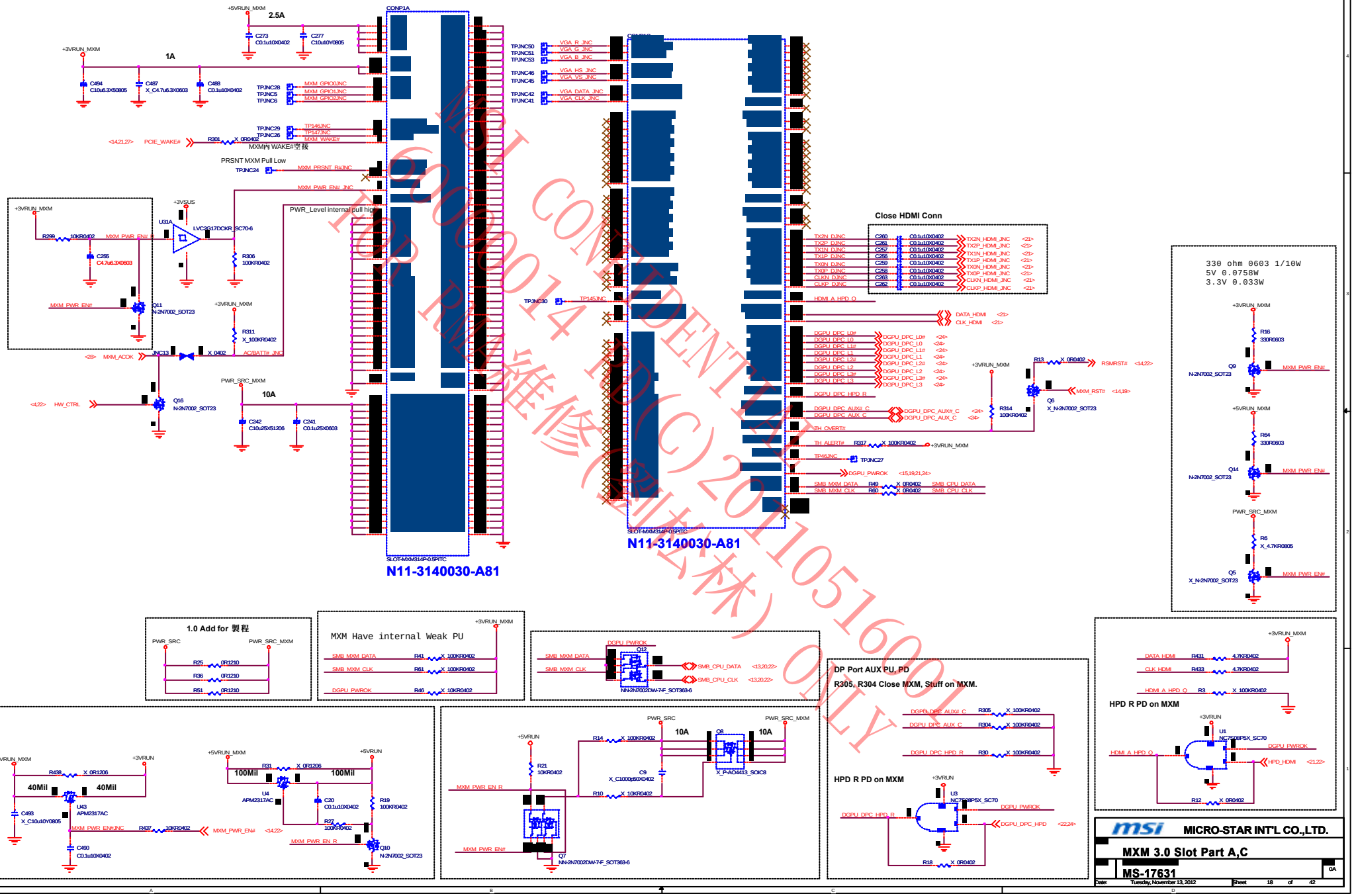
MXM 3.0 (x16 PEG Gen 3)



MICRO-STAR INT'L CO.,LTD.	
MXM 3.0 Slot Part A,C	
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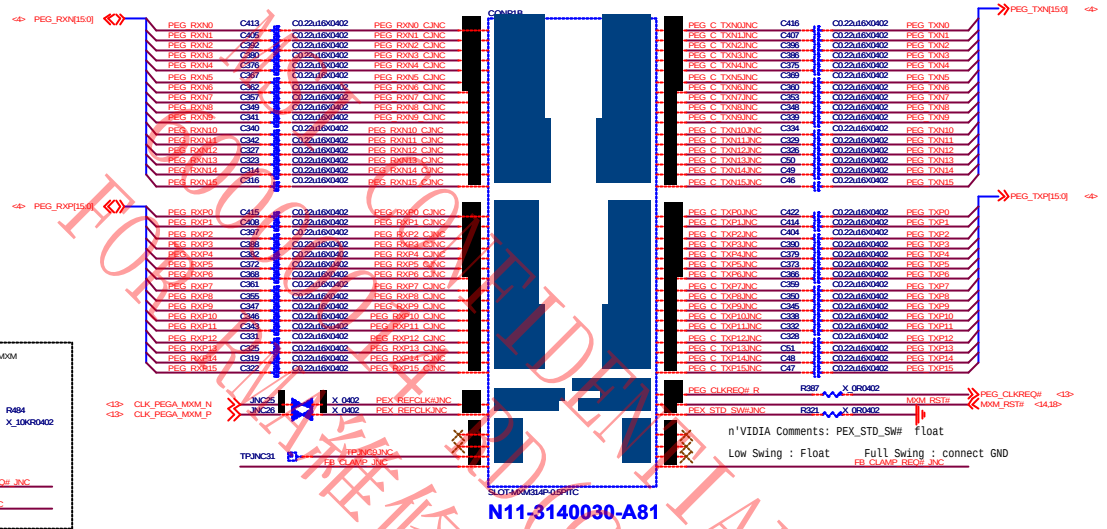
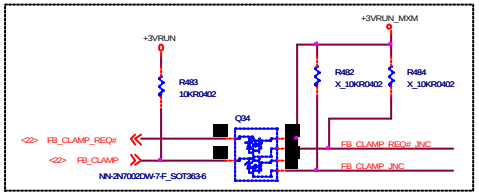
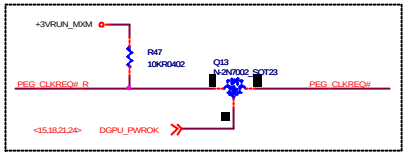
MXM 3.0 (x16 PEG Gen 3)

n'VIDIA Comments: NV11 can't support PCIE GEN3,so used 0.1uf CAP

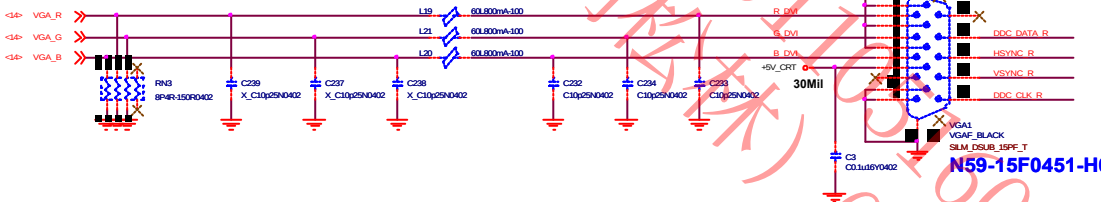
The change in AC capacitor value from 0.1uf to 0.22uf is to enable compatibility with futrue platforms having PCIE GEN3(8GT/s)

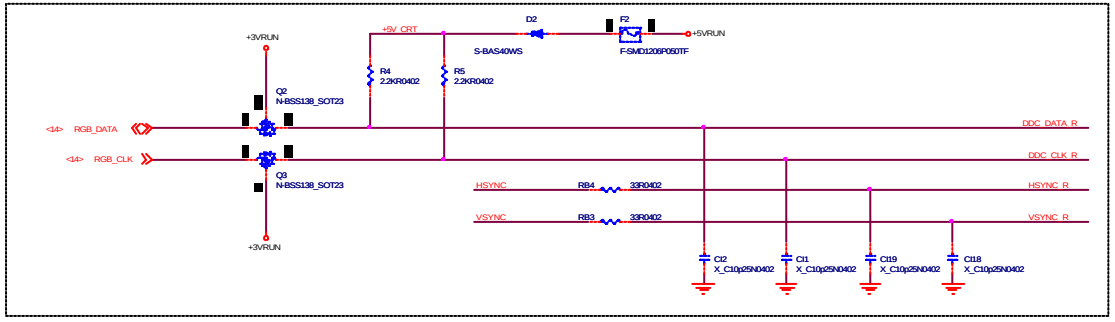


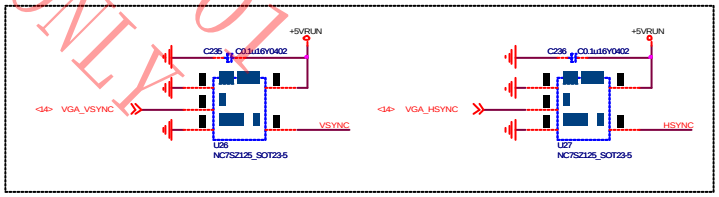




CRT







MICRO-STAR INT'L CO.,LTD.	
MXM 3.0 Slot Part B/CRT	
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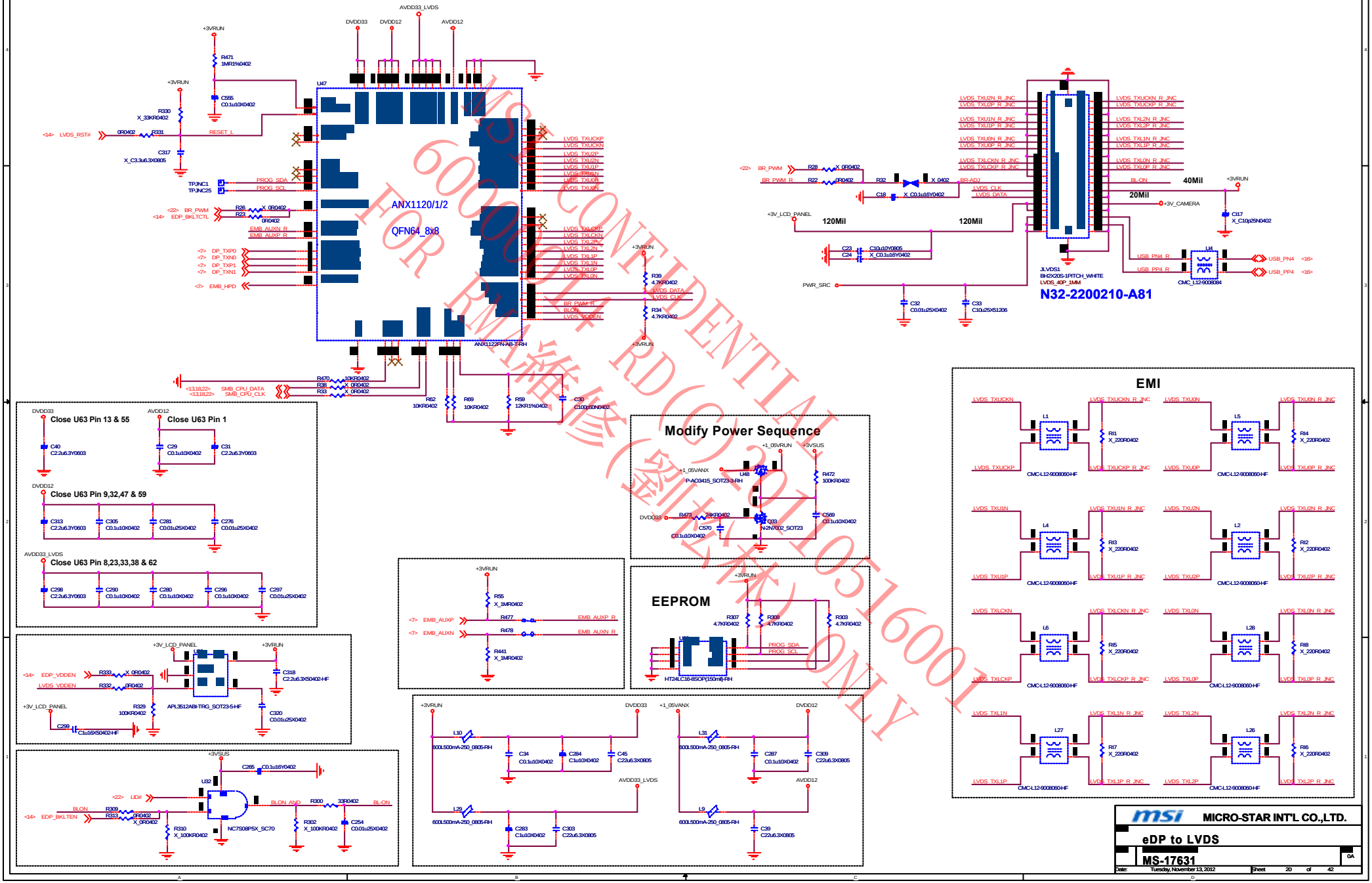
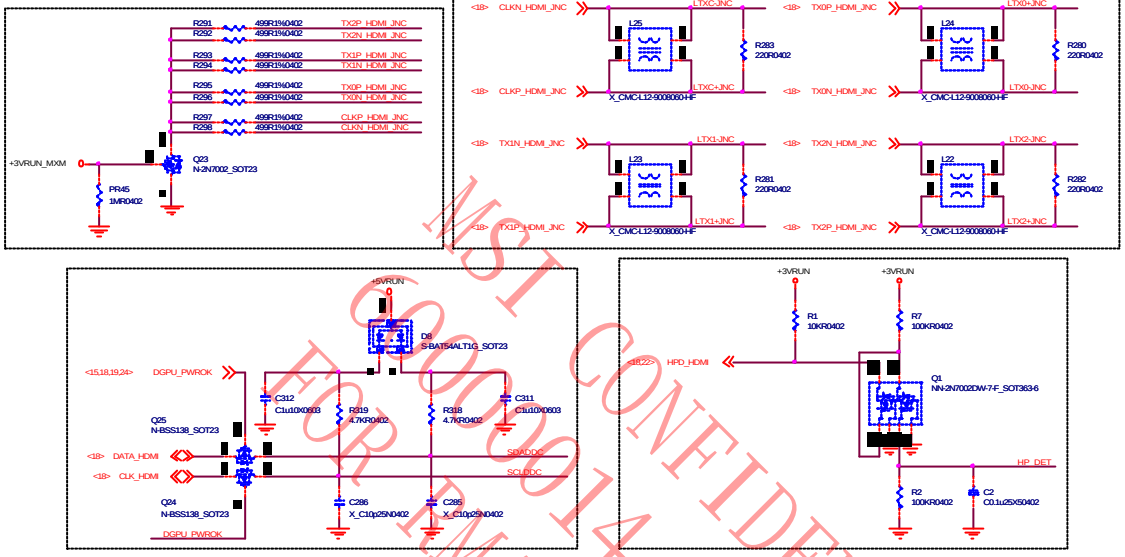
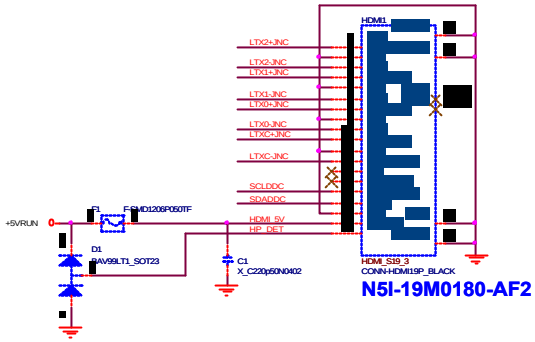
eDP to LVDS

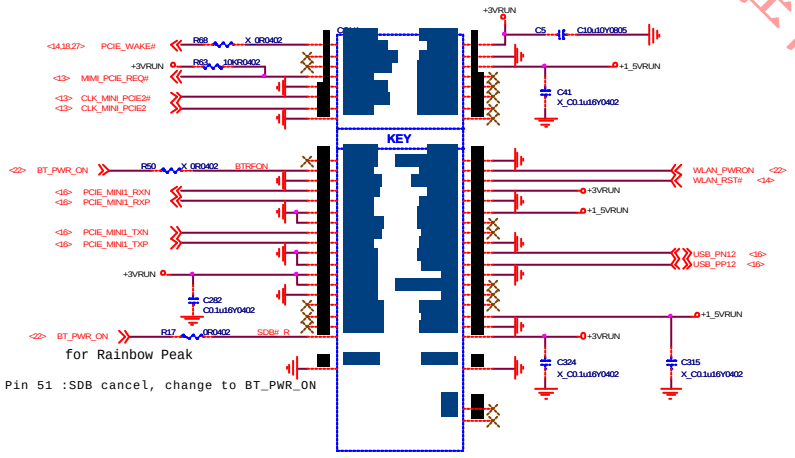


HDMI





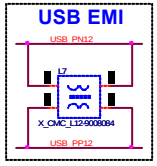
WLAN/BT



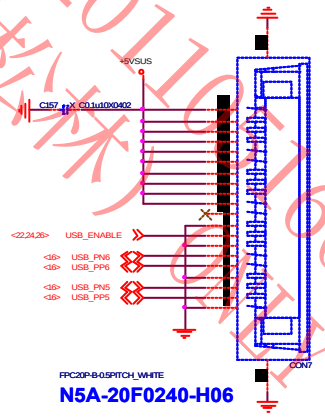
for Rainbow Peak

Pin 51 :SDB cancel, change to BT_PWR_ON

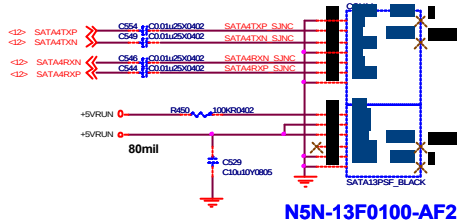
USB EMI



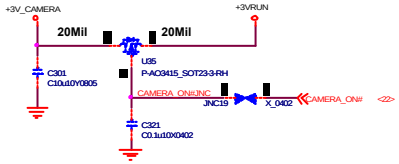
MS-1763 Co-Lay
USB Port *2



ODD



WebCAM



msi	MICRO-STAR INT'L CO.,LTD.
HDMI/WLAN/BT/USB/ODD/CAM	
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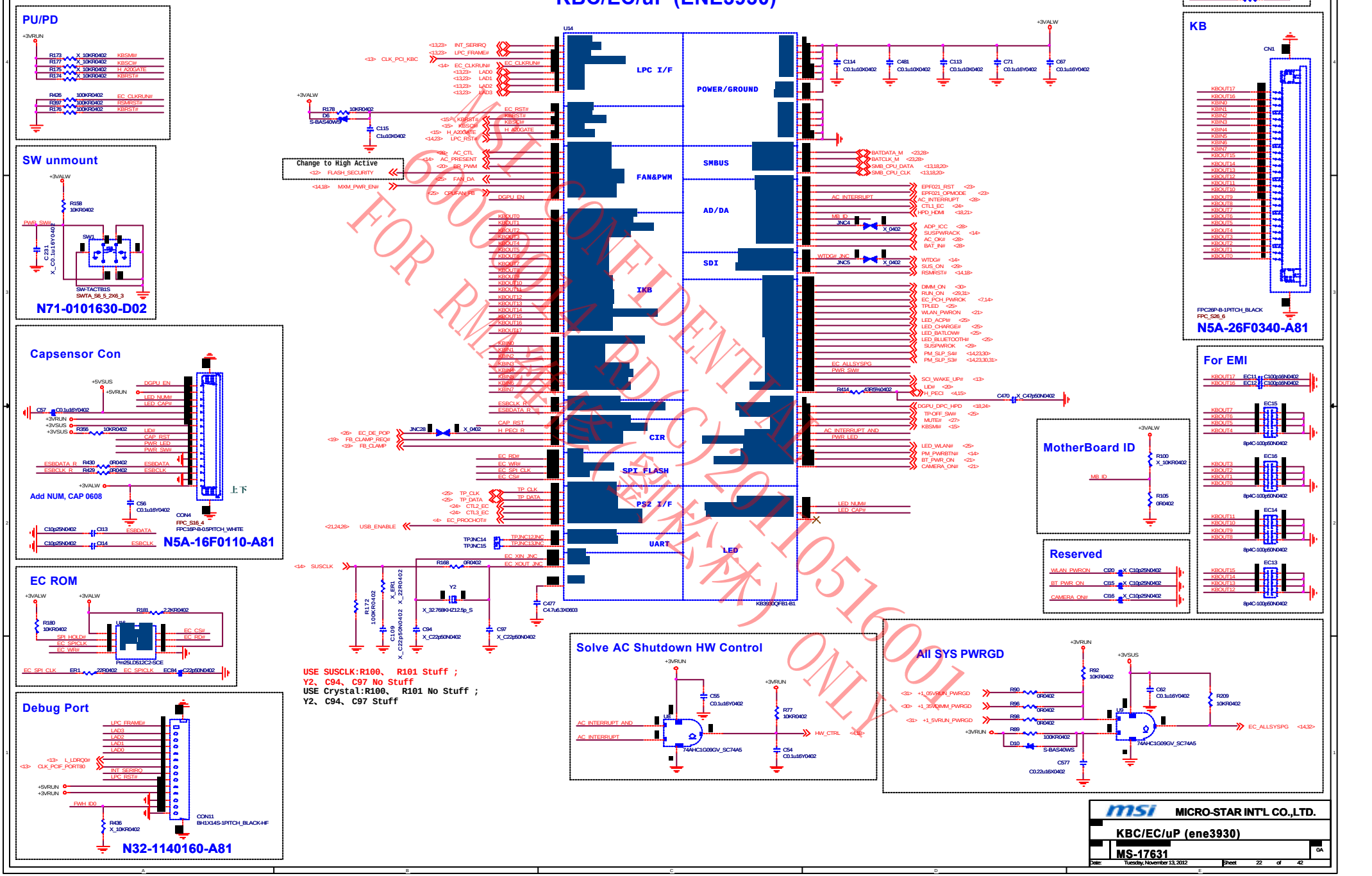
KBC/EC/uP (ENE3930)



msi	MICRO-STAR INT'L CO.,LTD.
KBC/EC/uP (ene3930)	
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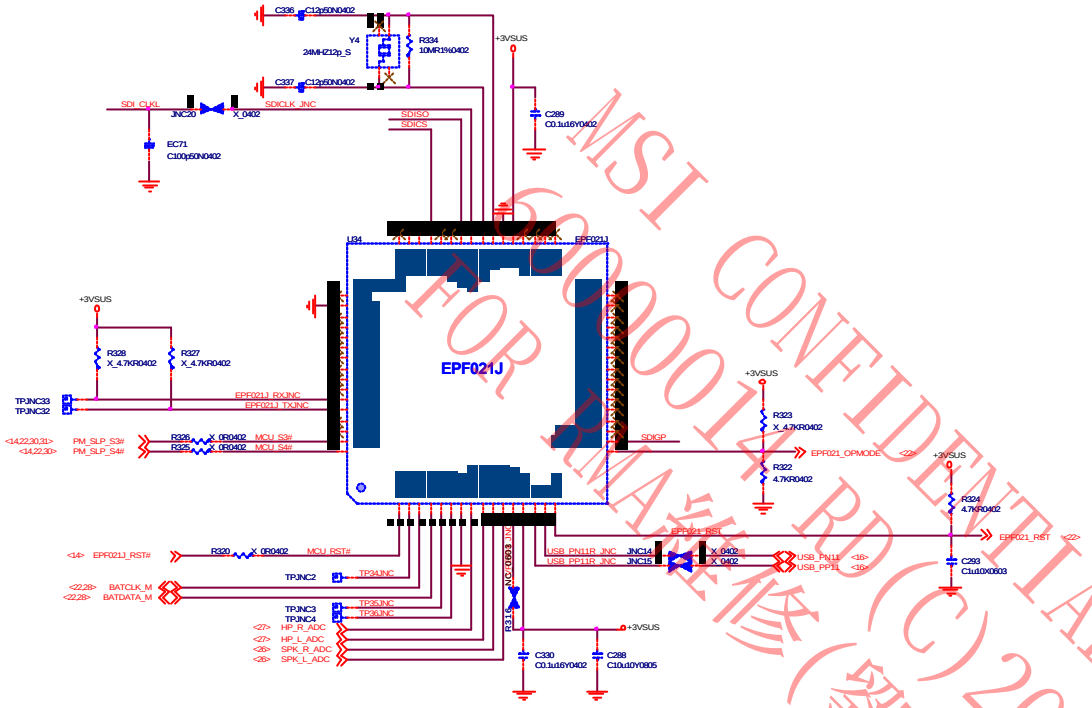
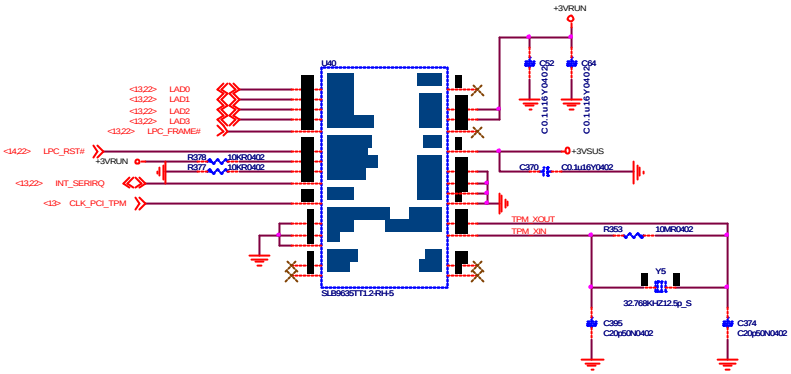
LED 8051 Controller(EPF021J)



TPM



LED Driver IC

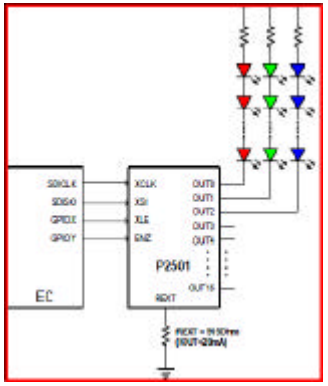
LED Forward Voltage	
R_Max	2.4V x 4 pcs = 9.6V
G_Max	3.3V x 4 pcs = 13.2V
B_Max	3.3V x 4 pcs = 13.2V

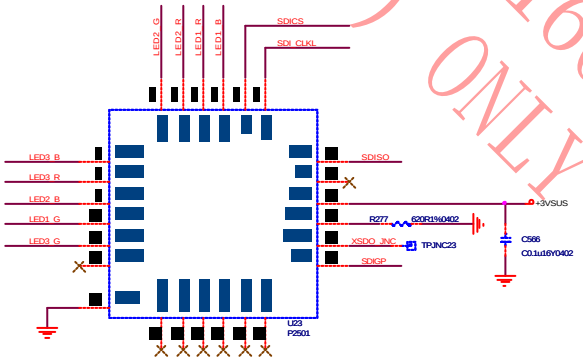
Constant current programing through the R258 resistor

IOUT=(Vrext / Rext) x 15
30mA=(1.22 / 620) x 15

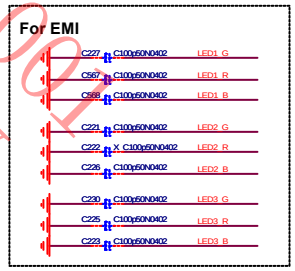
REXT		
BR1	BR0	Average_ I OUT (ON/OFF)
0	0	3.75mA
0	1	11.25mA
1	0	18.75mA
1	1	26.25mA

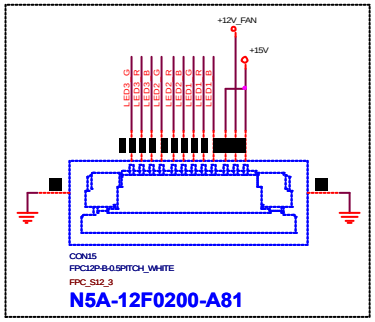
LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G





For EMI





N5A-12F0200-A81

MICRO-STAR INT'L CO.,LTD.

LED Driver IC/Controller/TPM

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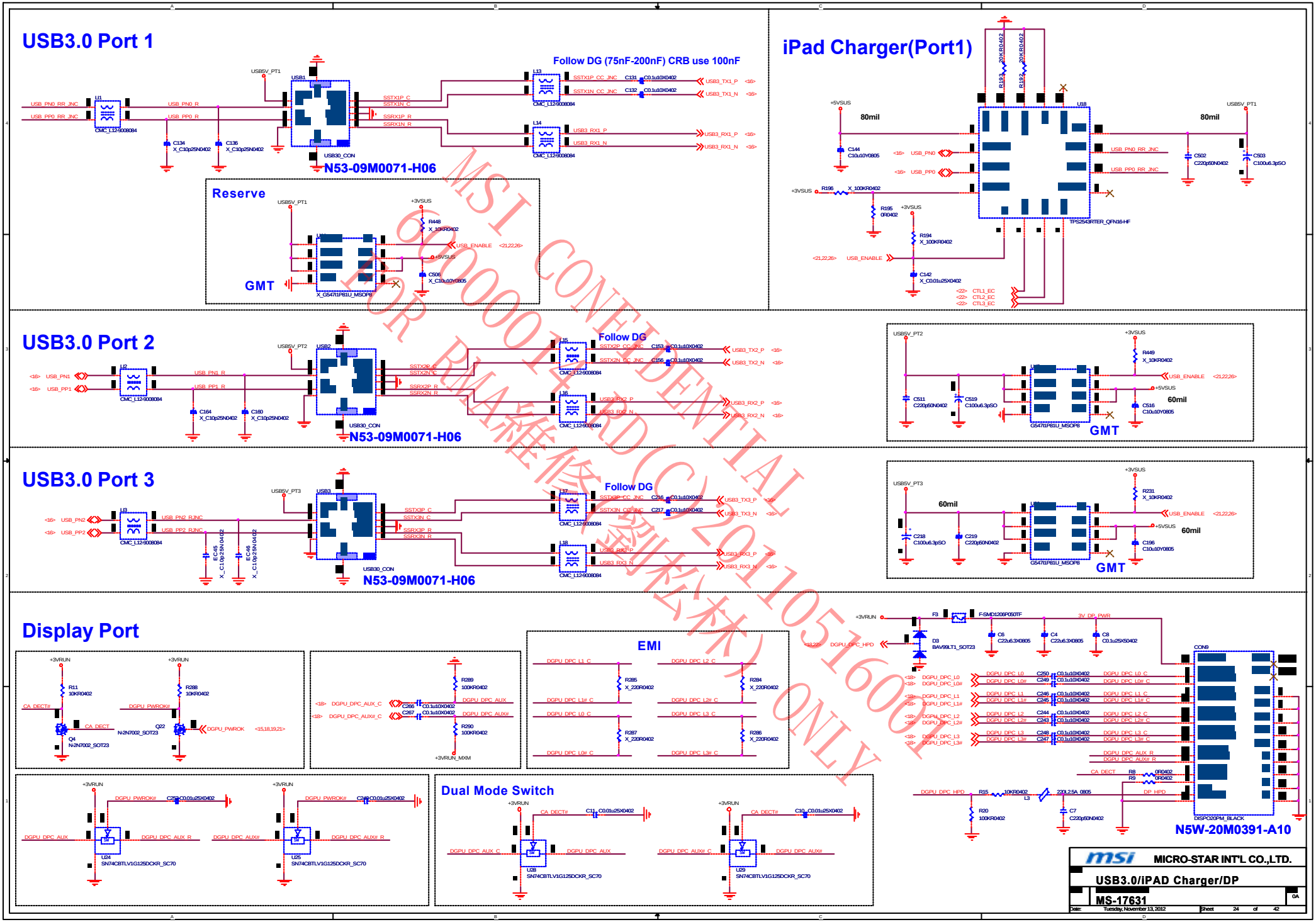
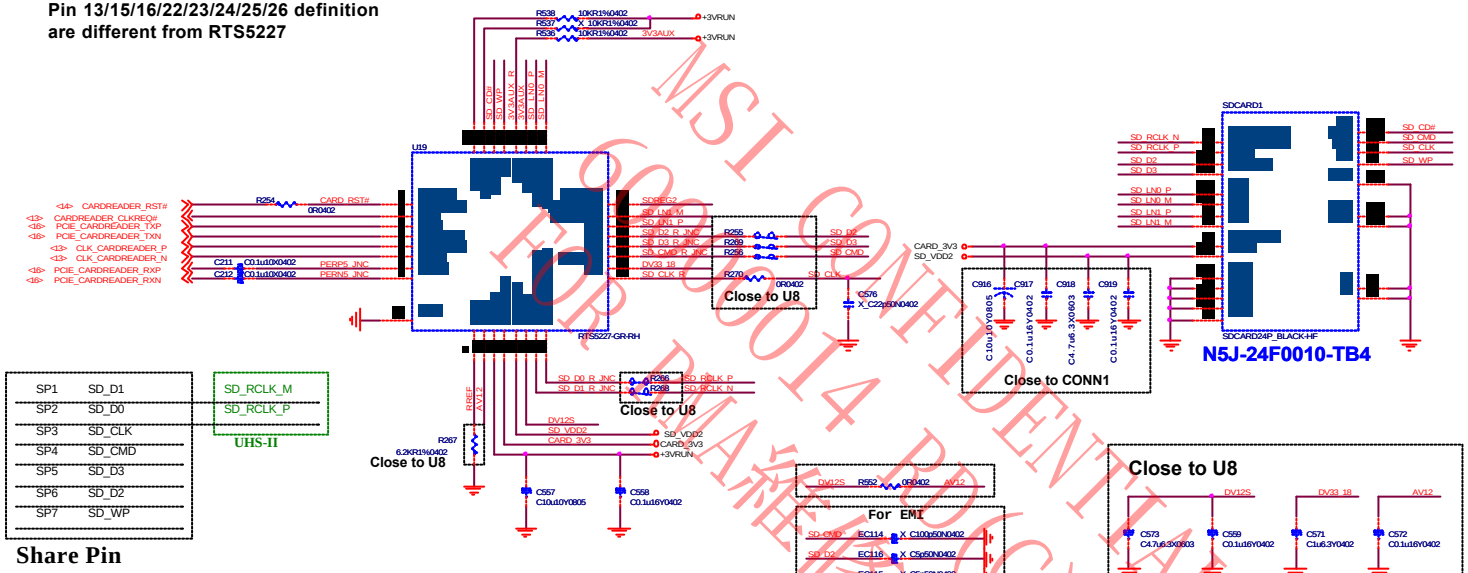
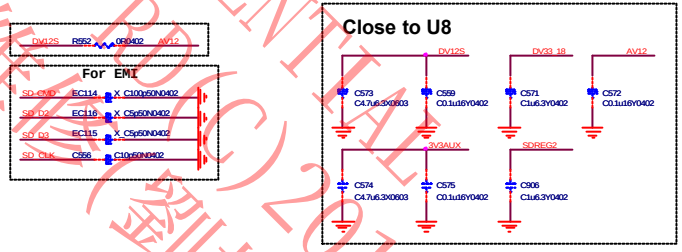


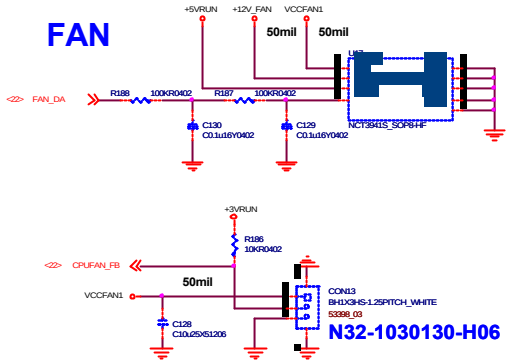
Card Reader(RTS5227)

RTS5249 Colay RTS5227
Pin 13/15/16/22/23/24/25/26 definition
are different from RTS5227

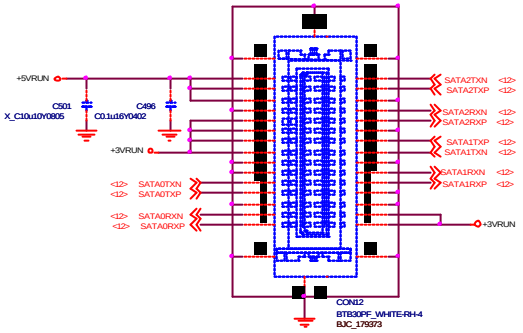




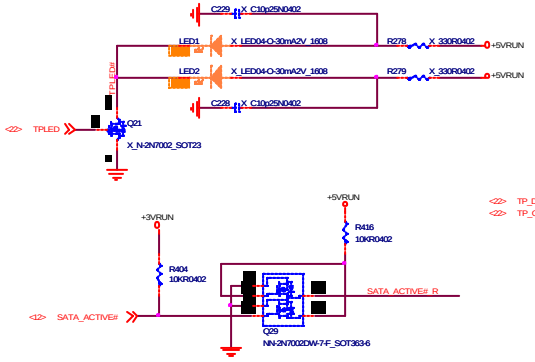
FAN

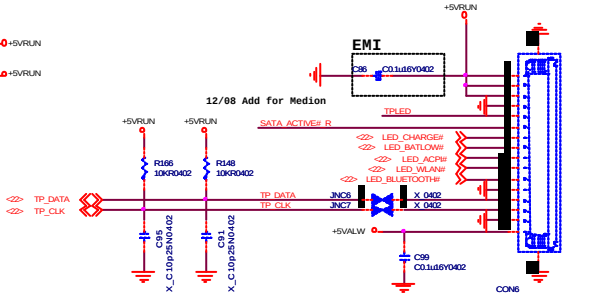


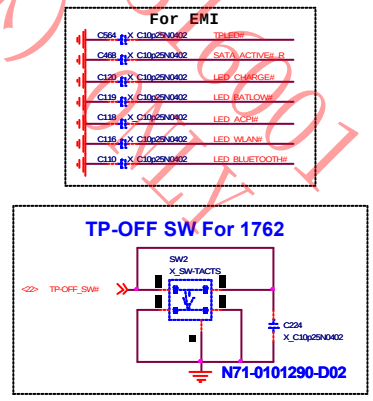
SATA HDD2 From Port 0,1,2



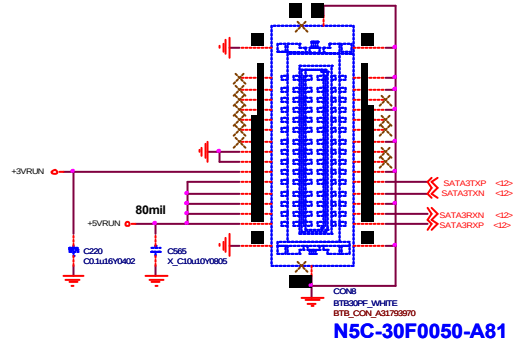
Touch Pad L/R-LED (Unmount)







SATA HDD1 From Port 3



MICRO-STAR INT'L CO.,LTD.
Card Reader/TP/HDD/FAN
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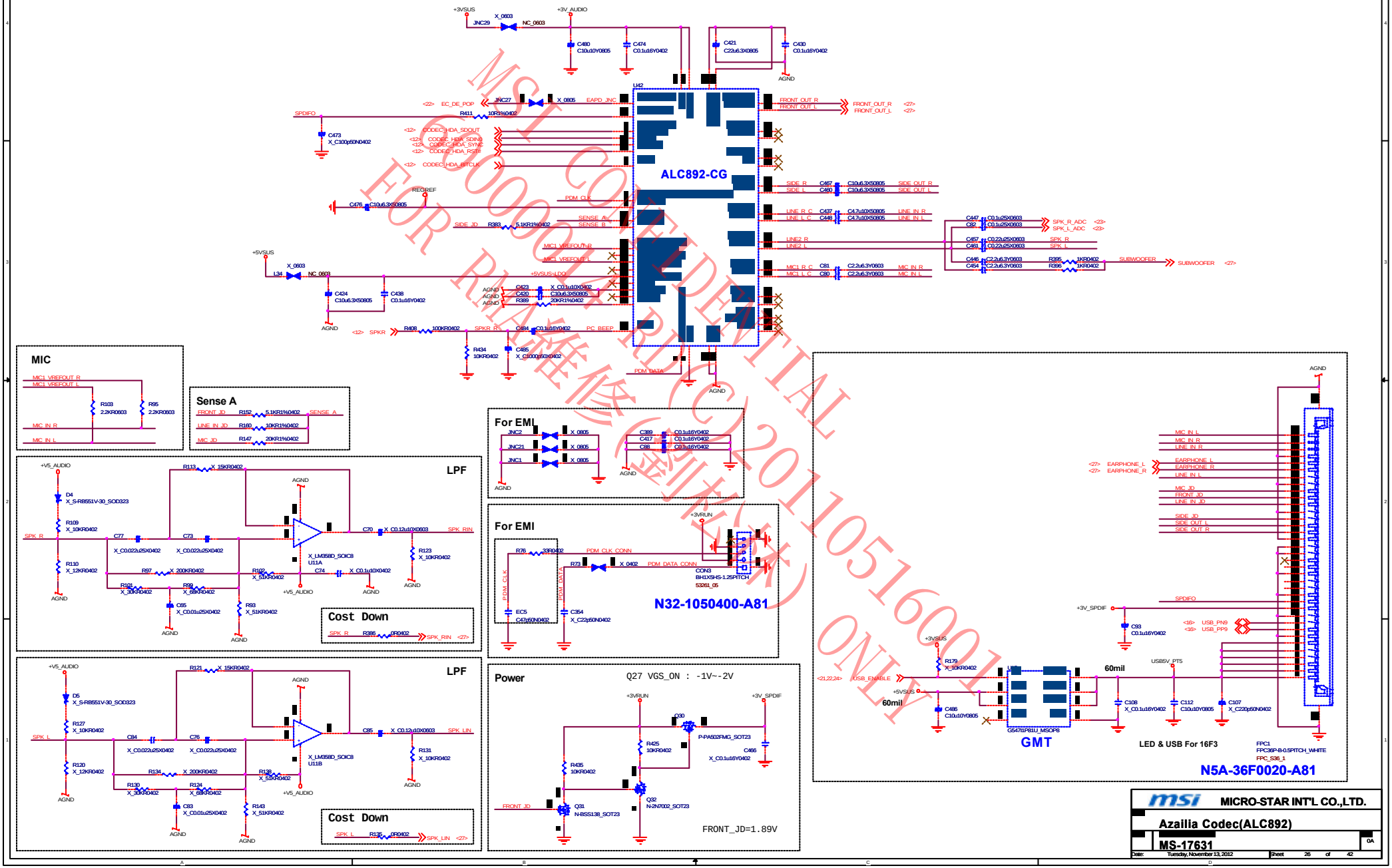
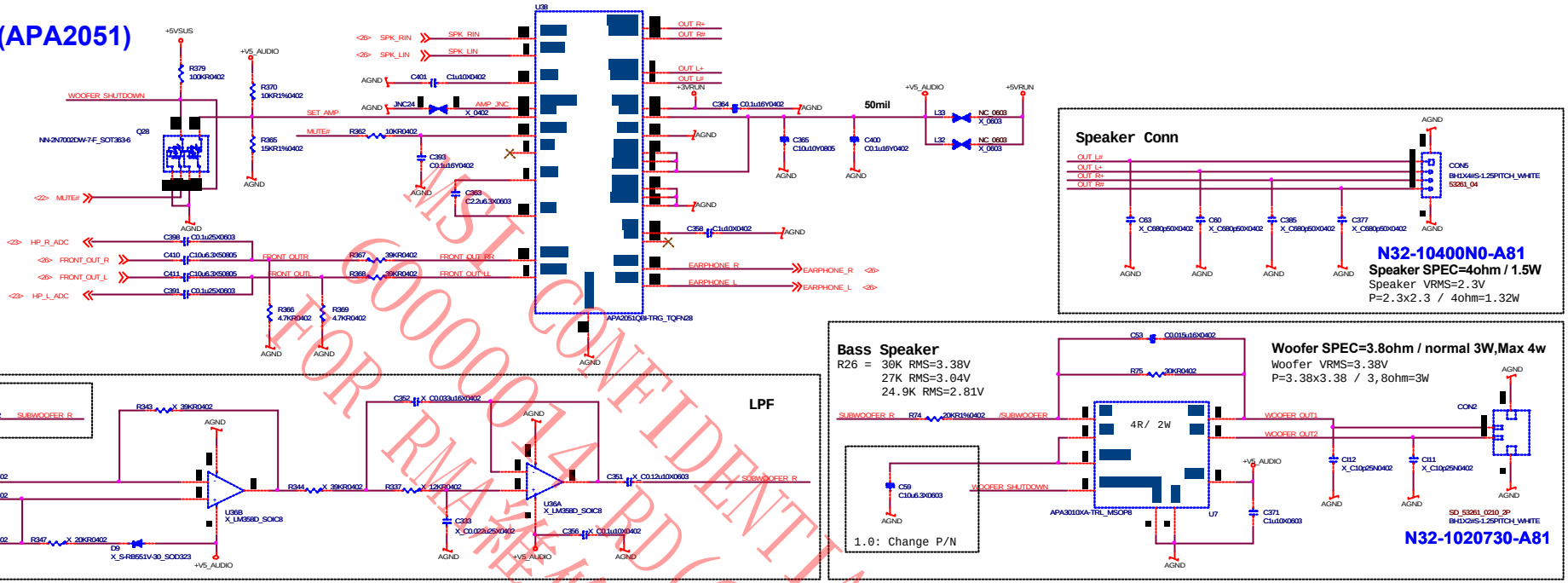
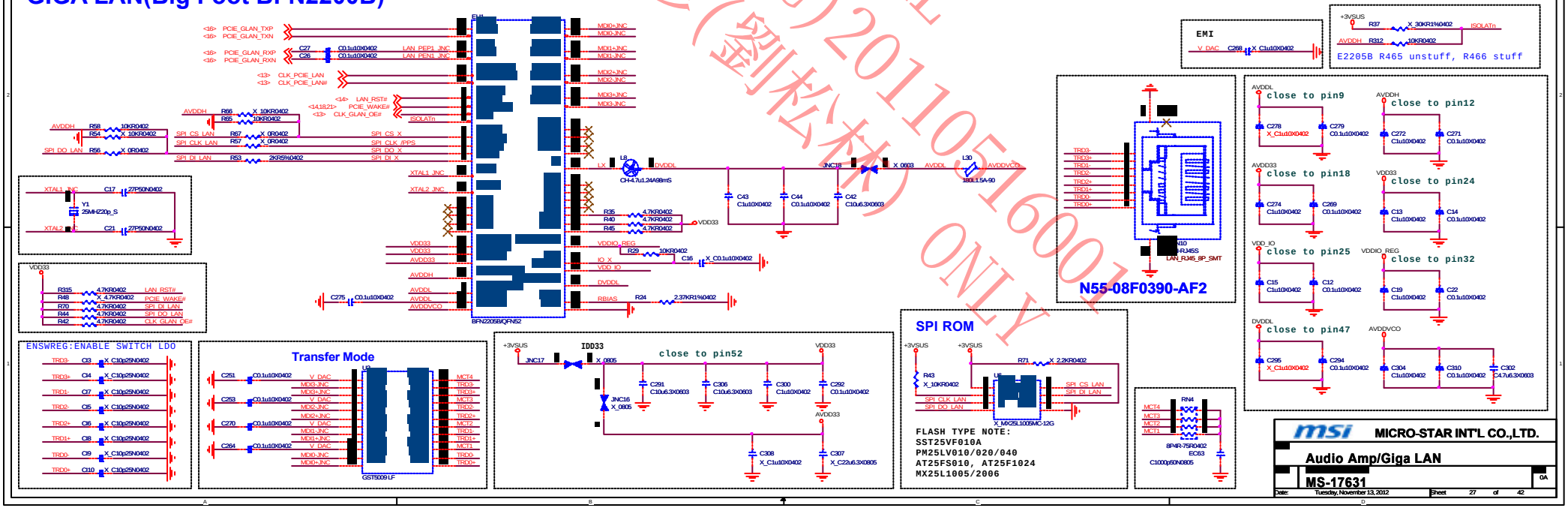
Azailia Codec(ALC892)



Audio Amp(APA2051)



GIGA LAN(Big Foot BFN2200B)



MICRO-STAR INT'L CO.,LTD.

Audio Amp/Giga LAN

MS-17631

0A

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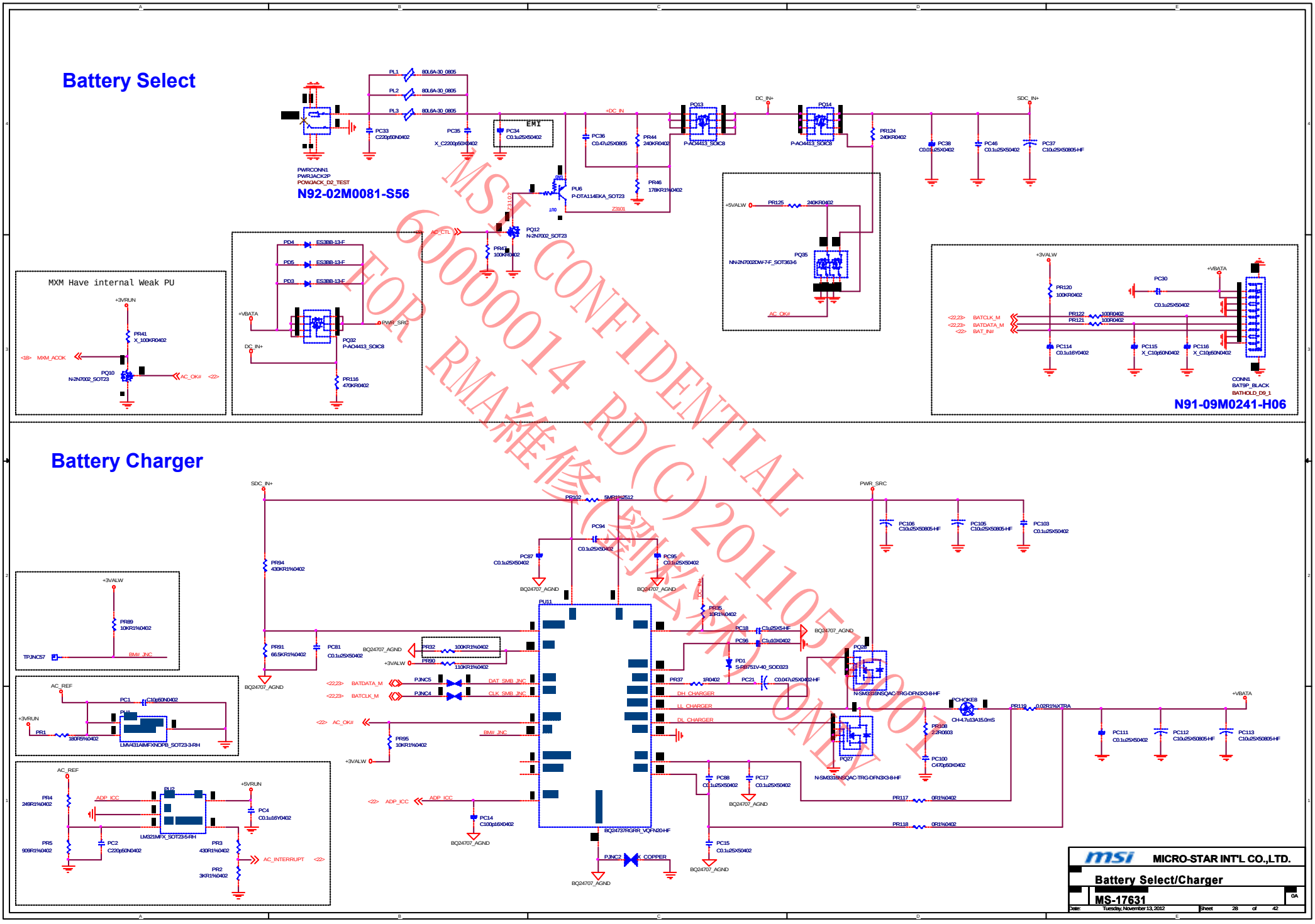
Battery Select
PWRCONN1
PWRJACK2P
POWJACK_D2_TEST
N92-02M0081-S56
MXM Have internal Weak PU
N91-09M0241-H06
Battery Charger
MICRO-STAR INT'L CO.,LTD.
Battery Select/Charger
MS-17631
Tuesday, November 13, 2012
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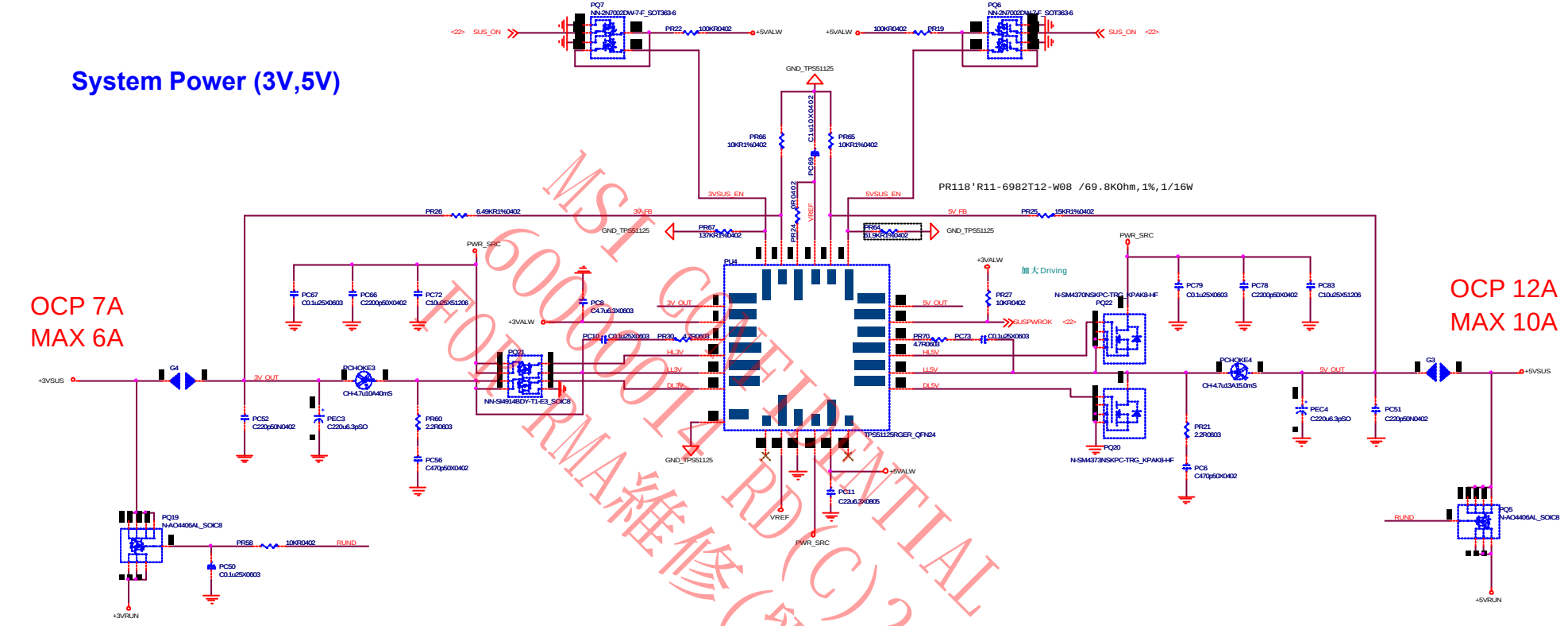
MSI CONFIDENTIAL
6000014 RD(C)20110511001
FOR RMA维修(刷机)专用 ONLY

System Power (3V,5V)

OCP 7A
MAX 6A

OCP 12A
MAX 10A



MICRO-STAR INT'L CO.,LTD.	
System Power	
MS-17631	0A
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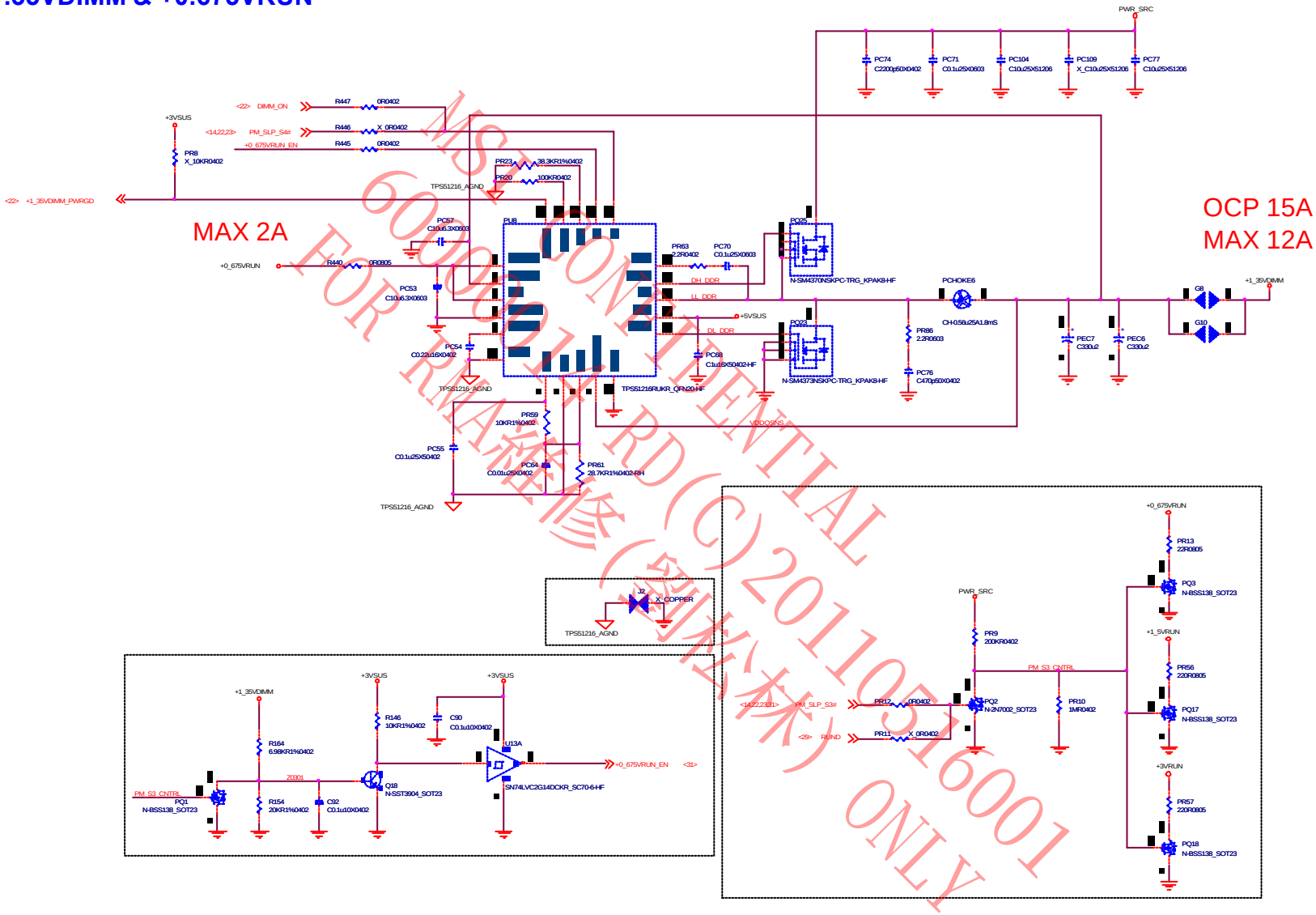
+1.35VDIMM & +0.675VRUN



MICRO-STAR INT'L CO.,LTD.	
+1.35VDIMM/+0.675VRUN	
MS-17631	0A
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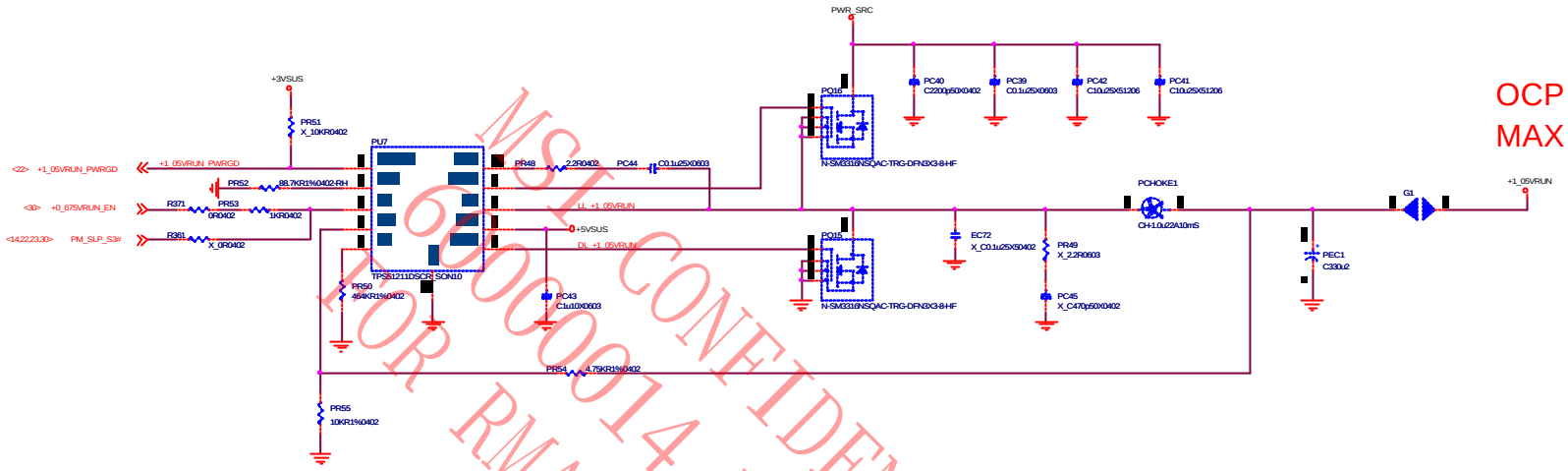
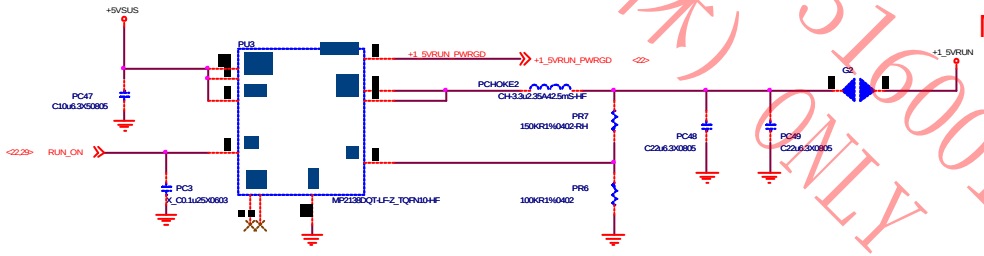
+1.05VRUN



OCP 8A
MAX 6A

+1.5VRUN



OCP 4A
MAX 1.5A

MICRO-STAR INT'L CO.,LTD.	
+1.05VRUN/+1.5VRUN	
MS-17631	0A
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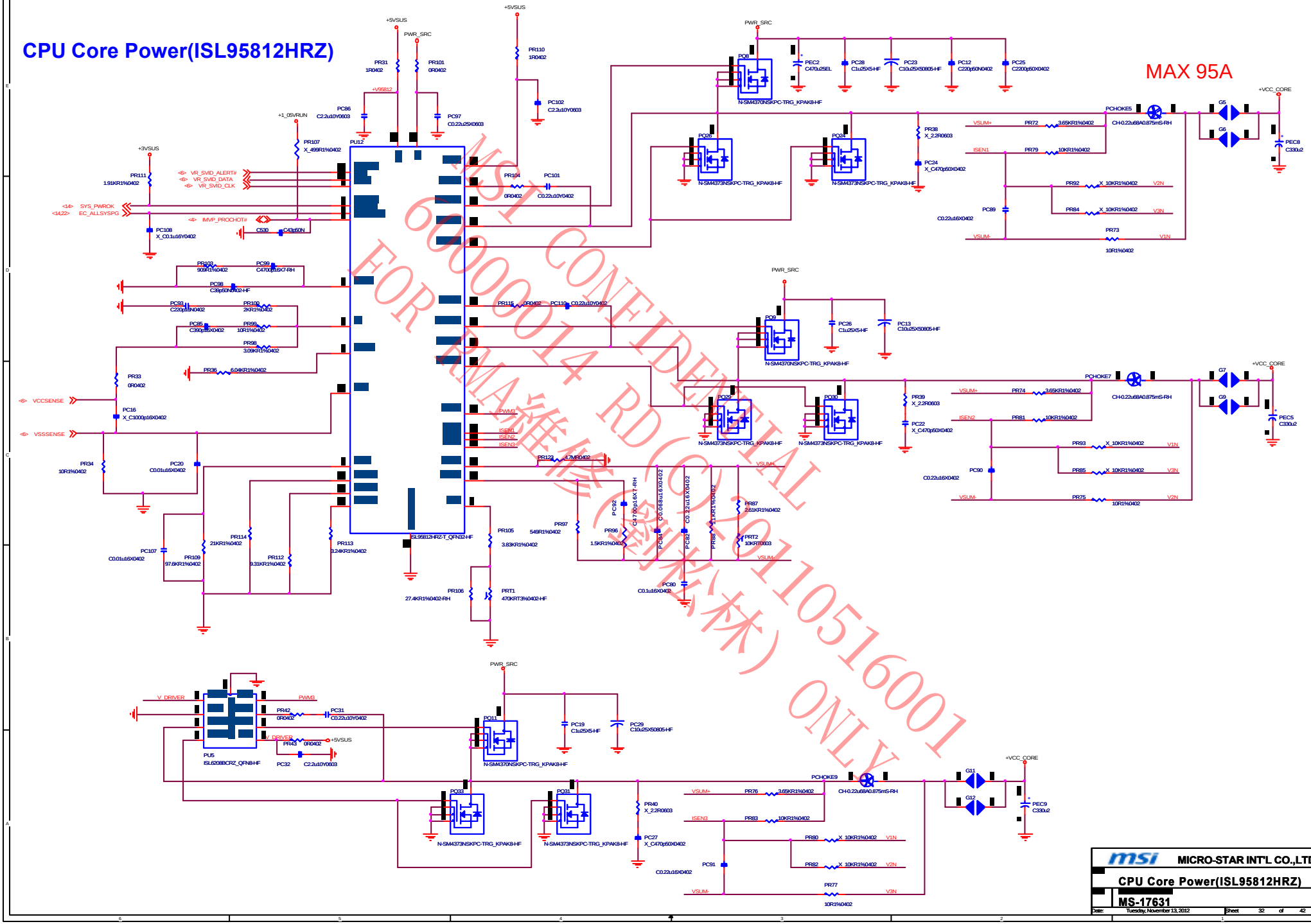
CPU Core Power(ISL95812HRZ)

MAX 95A



MICRO-STAR INT'L CO.,LTD.	
CPU Core Power(ISL95812HRZ)	
MS-17631	0A
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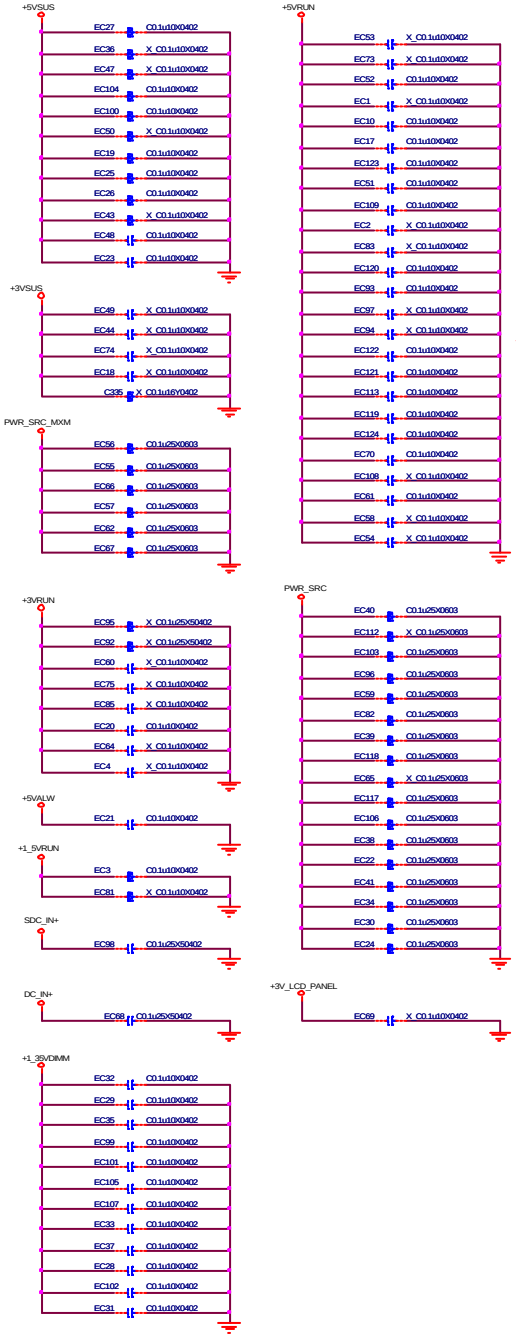
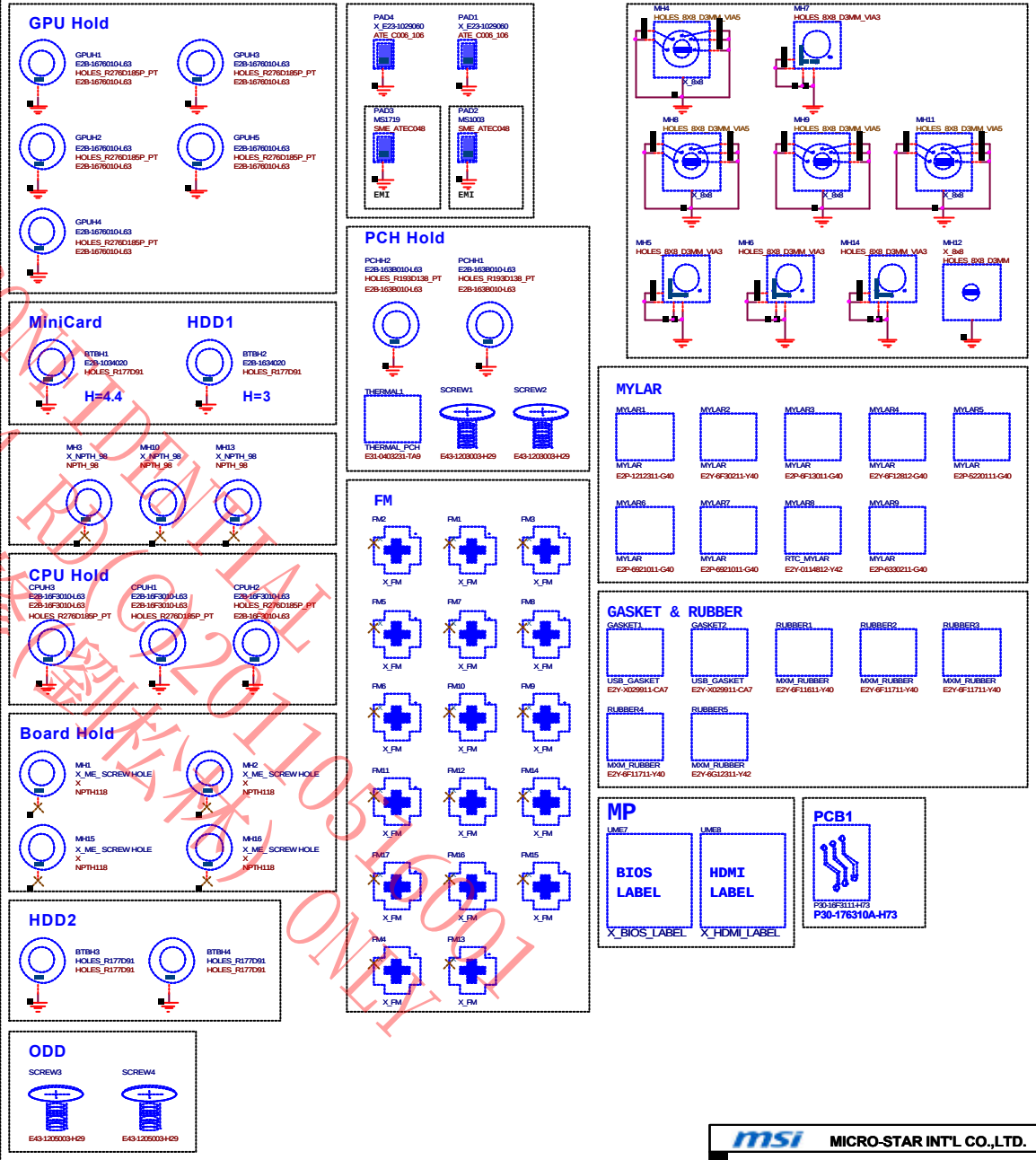
EMI



Screw



MICRO-STAR INT'L CO.,LTD.	
EMI/Screw	
MS-17631	0A
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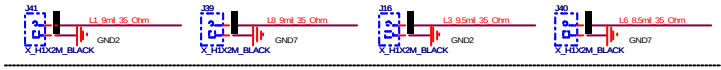
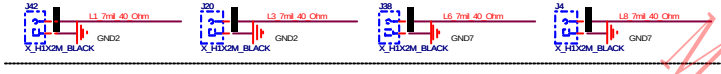
Impedance

Single End

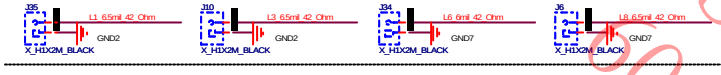
35 ohm



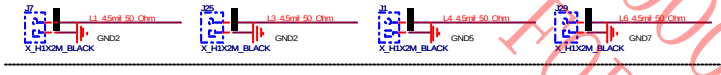
40 ohm



42 ohm

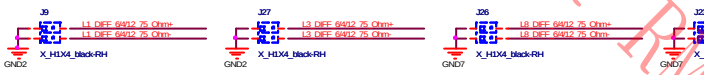


50 ohm

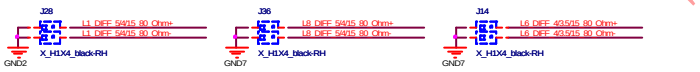


Differential

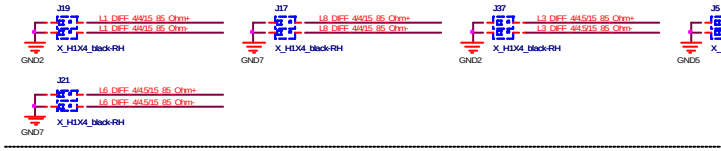
75 ohm



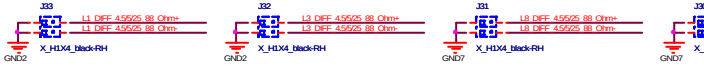
80 ohm



85 ohm

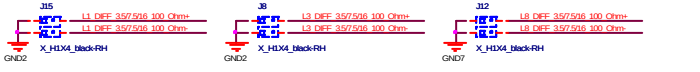


88 ohm



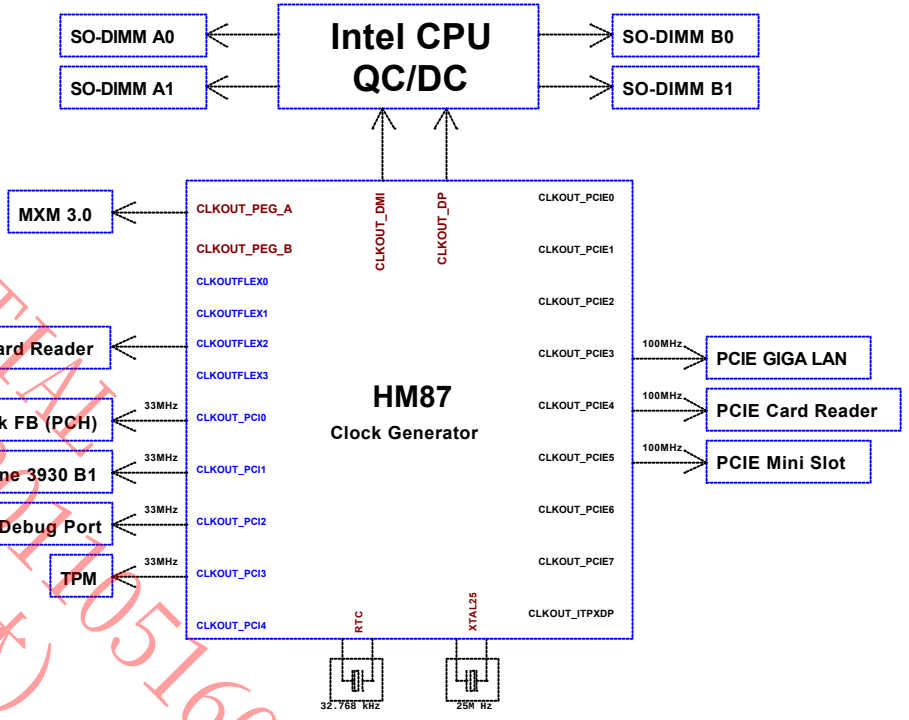
90 ohm

100 ohm



Clock Distribution

Internal Clock Mode



msi	MICRO-STAR INT'L CO.,LTD.
Impedance/Clock Distribution	
MS-17631	0A
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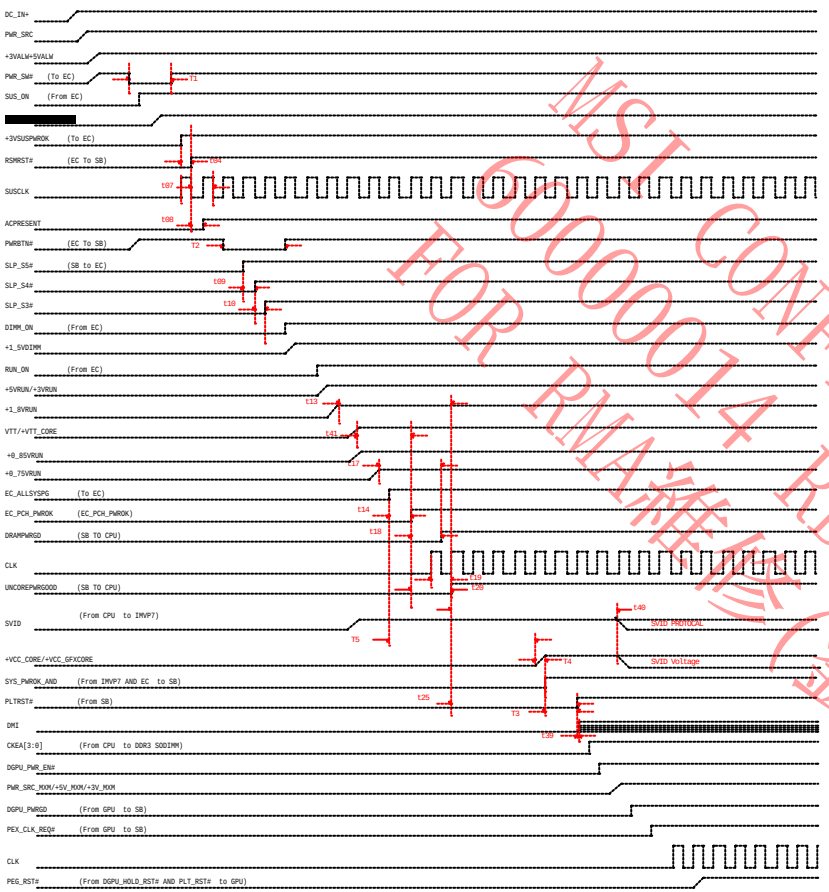
Power on Sequence

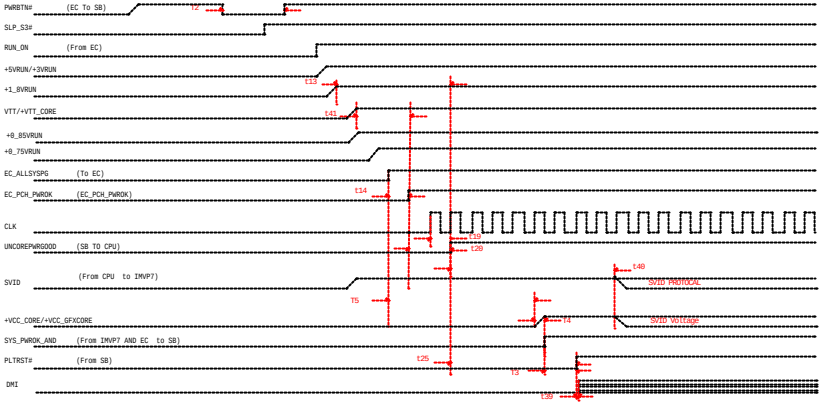
S5-S0

EC programming timing



S3-S0

EC programming timing



	Min	Max	Unit	Description
T1	150		mS	
T2	16		mS	
T3	1		mS	Timing set by PCH
t04	10		mS	
t07	100		mS	
t08		90	mS	
t09	30		uS	
t10	30		uS	
t13	5	650	mS	
t14	99		mS	EC Delay
t17	2	650	mS	
t18	1		mS	Timing set by PCH
t19	41		mS	Timing set by PCH
t20	2		mS	Timing set by PCH
t25	1	100	mS	
T5		800	uS	Follow MVP Spec
T4	2.5		mV/uS	Follow MVP Spec
t39		200	uS	
t40		500	uS	
t41	10		mS	

MICRO-STAR INT'L CO.,LTD.

Power on Sequency

MS-17631

0A

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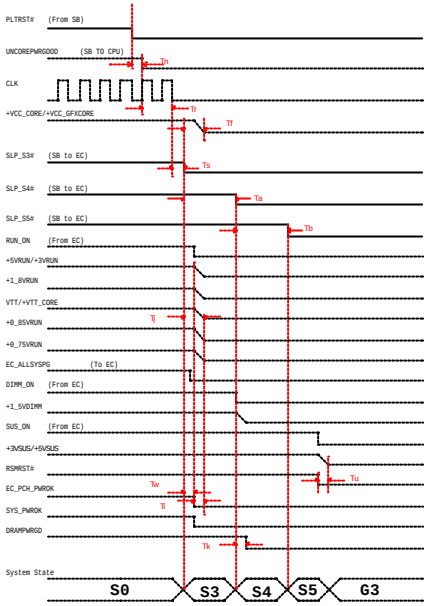
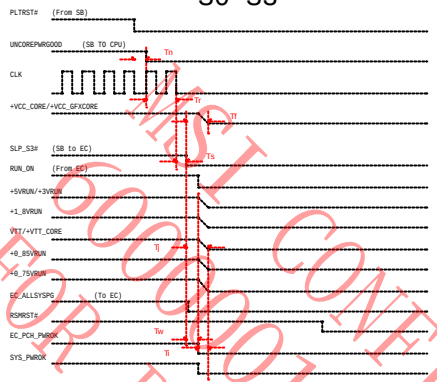
Power down Sequence

S0-S5

EC programming timing

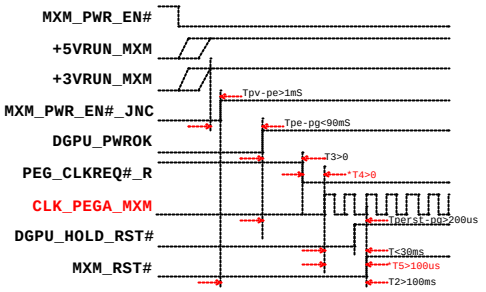


S0-S3



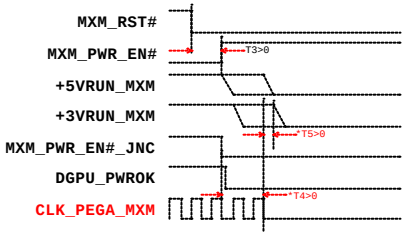
	Min	Max	Unit	Description
Ta	30		uS	
Tb	30		uS	
Tf		500	mS	
Ti	40		nS	
Tj	5		uS	
Tk	100		nS	
Tn	30		uS	
Tp	500		uS	Sx-RSMRST#
Tr	10		uS	
Ts	1		uS	
Tu	40		nS	
Tw	0		mS	

Power-Up Sequence For Optimus On MXM



P.S. Clock alway on

Power-Down Sequence For Optimus On MXM



P.S. Clock alway on

MICRO-STAR INT'L CO.,LTD.	
Power Down & MXM Sequence	
MS-17631	0A
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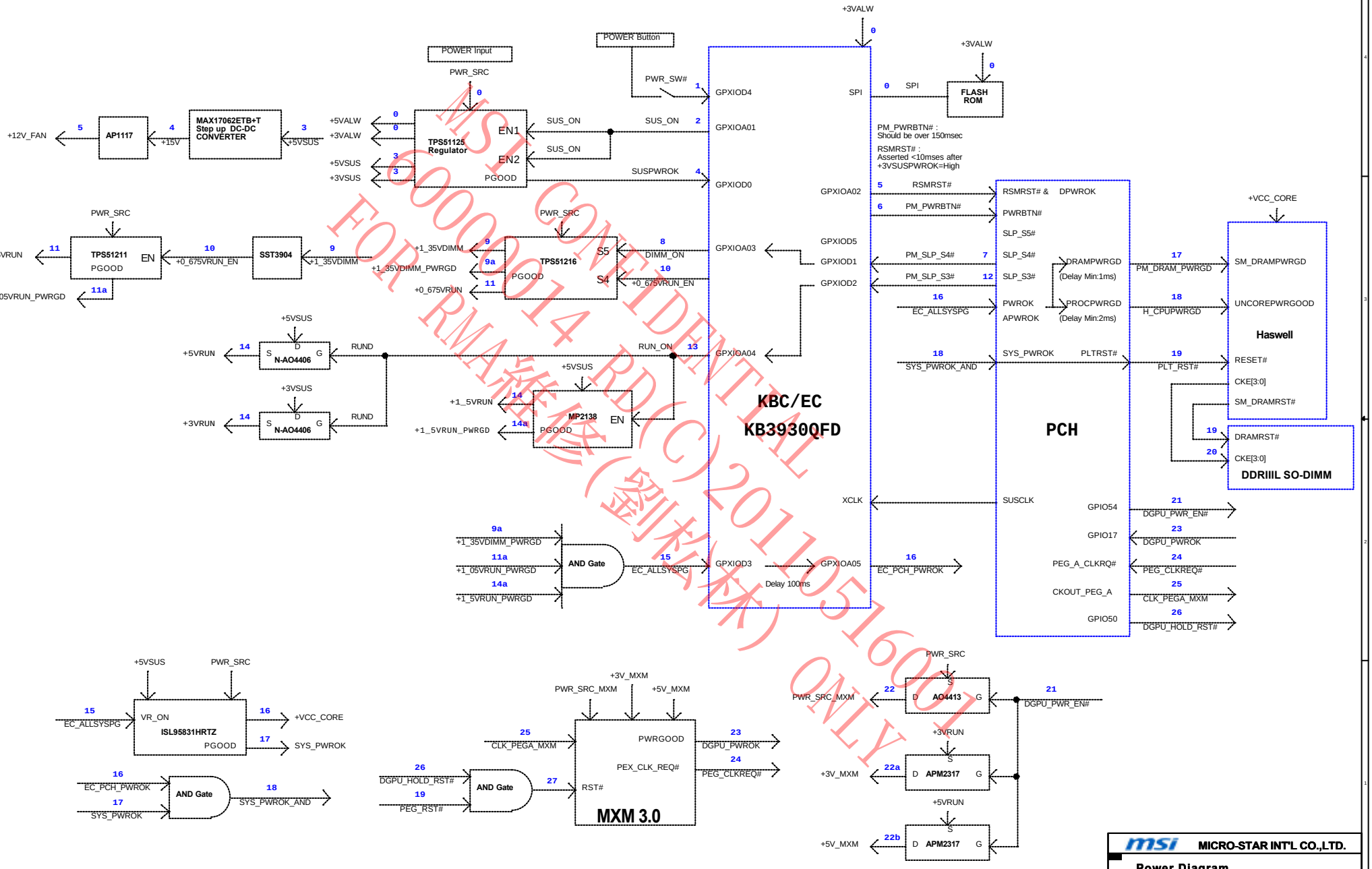
Power Diagram



MICRO-STAR INT'L CO.,LTD.	
Power Diagram	
MS-17631	0A
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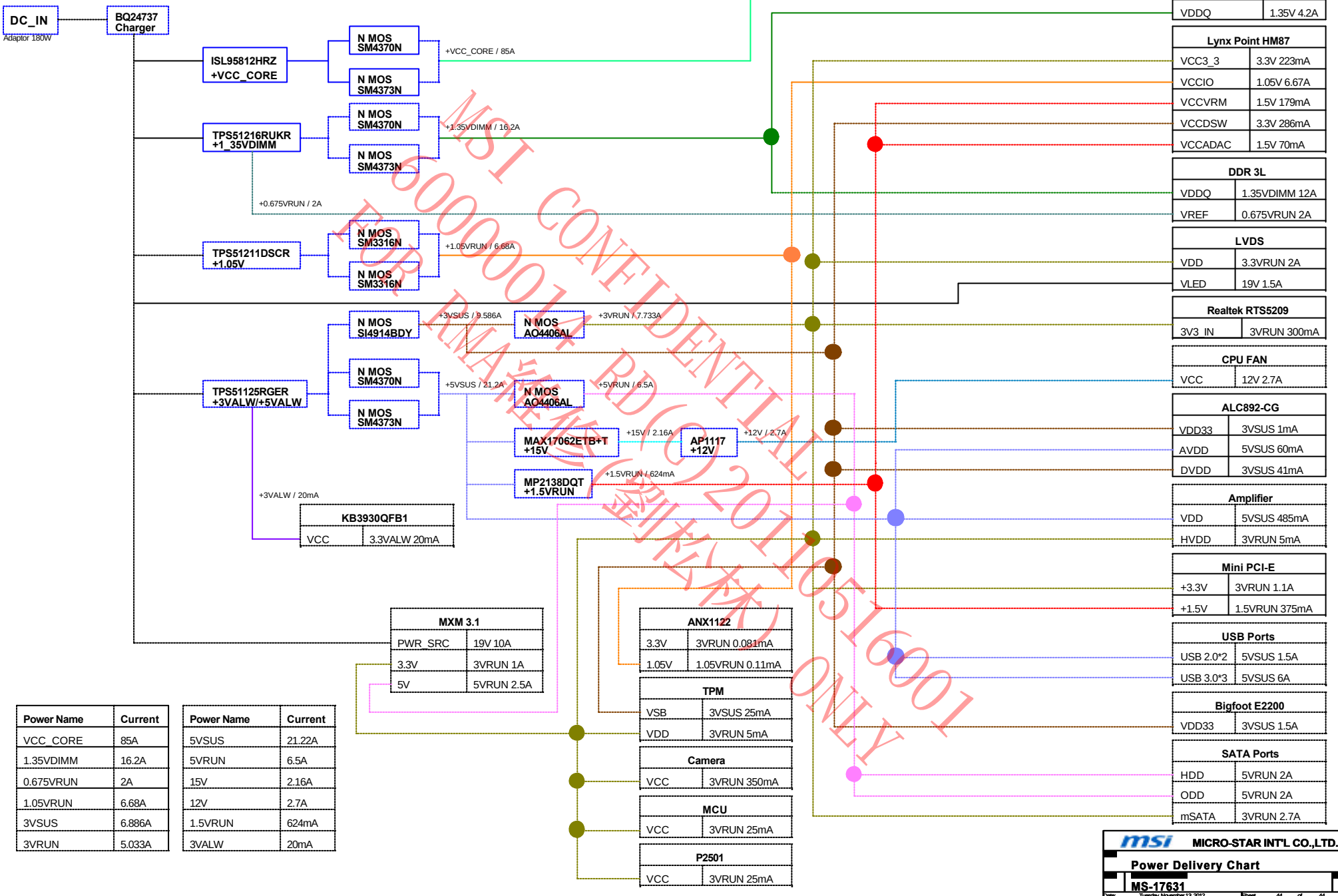

Power Name	Current
VCC_CORE	85A
1.35VDIMM	16.2A
0.675VRUN	2A
1.05VRUN	6.68A
3VSUS	6.886A
3VRUN	5.033A

Power Name	Current
5VSUS	21.22A
5VRUN	6.5A
15V	2.16A
12V	2.7A
1.5VRUN	624mA
3VALW	20mA

msi MICRO-STAR INT'L CO.,LTD.

Power Delivery Chart

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