Mockingbird-N/V 14/15_TGL & Hellcat 14/15/17_TGL Schematic

2020-08-01
REV : A00

DY : None Installed
UMA: Unified Memory Architecture
OPS: Optimal Playable Settings

<Core Design>

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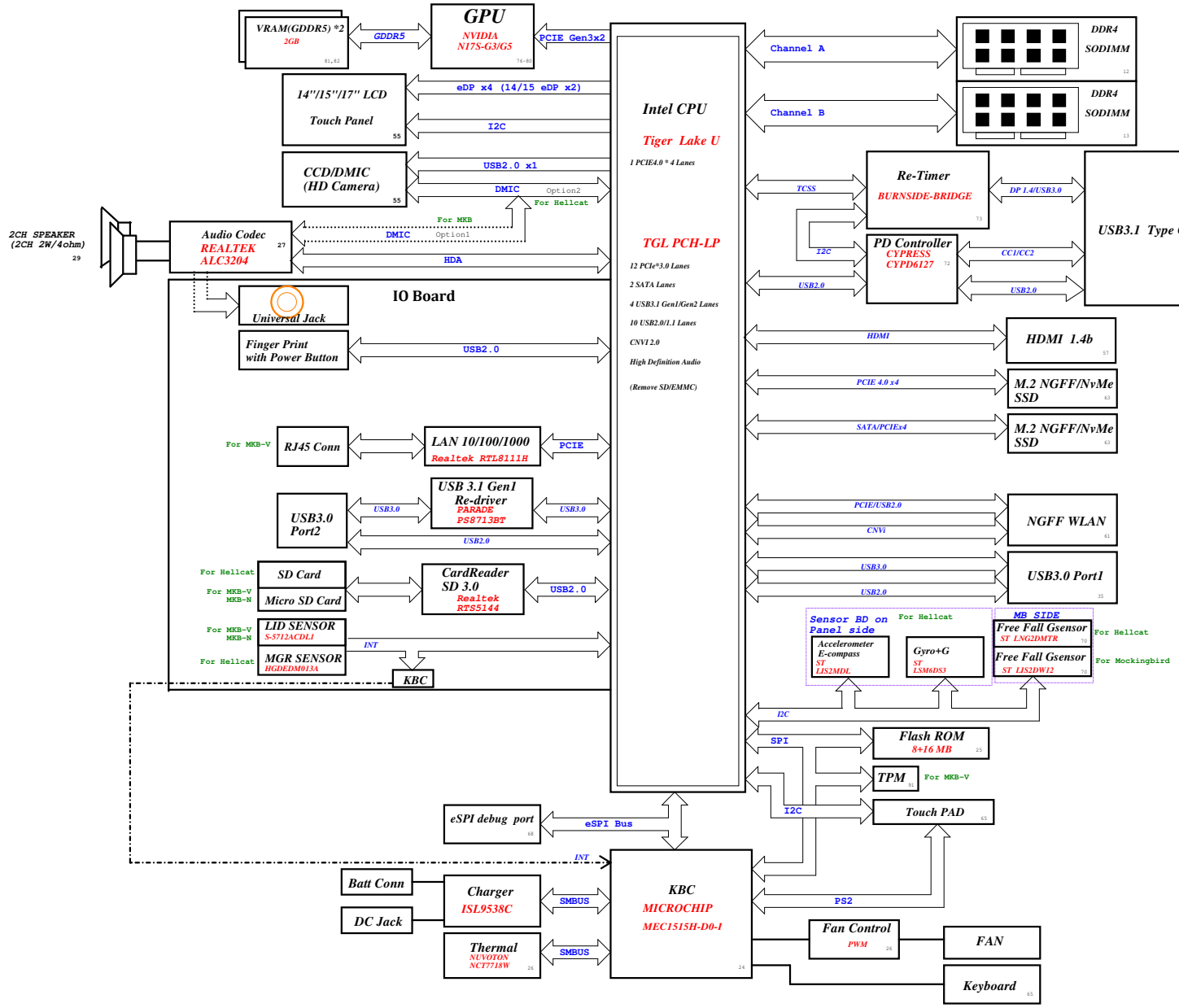
Title	Cover Page	
Size: A4	Document Number: MOCKINGBIRD_TGL	Rev: A00
Date: Saturday, August 01, 2020	Sheet 1 of 105	

Mockingbird N/V/HellCat TGL Block Diagram



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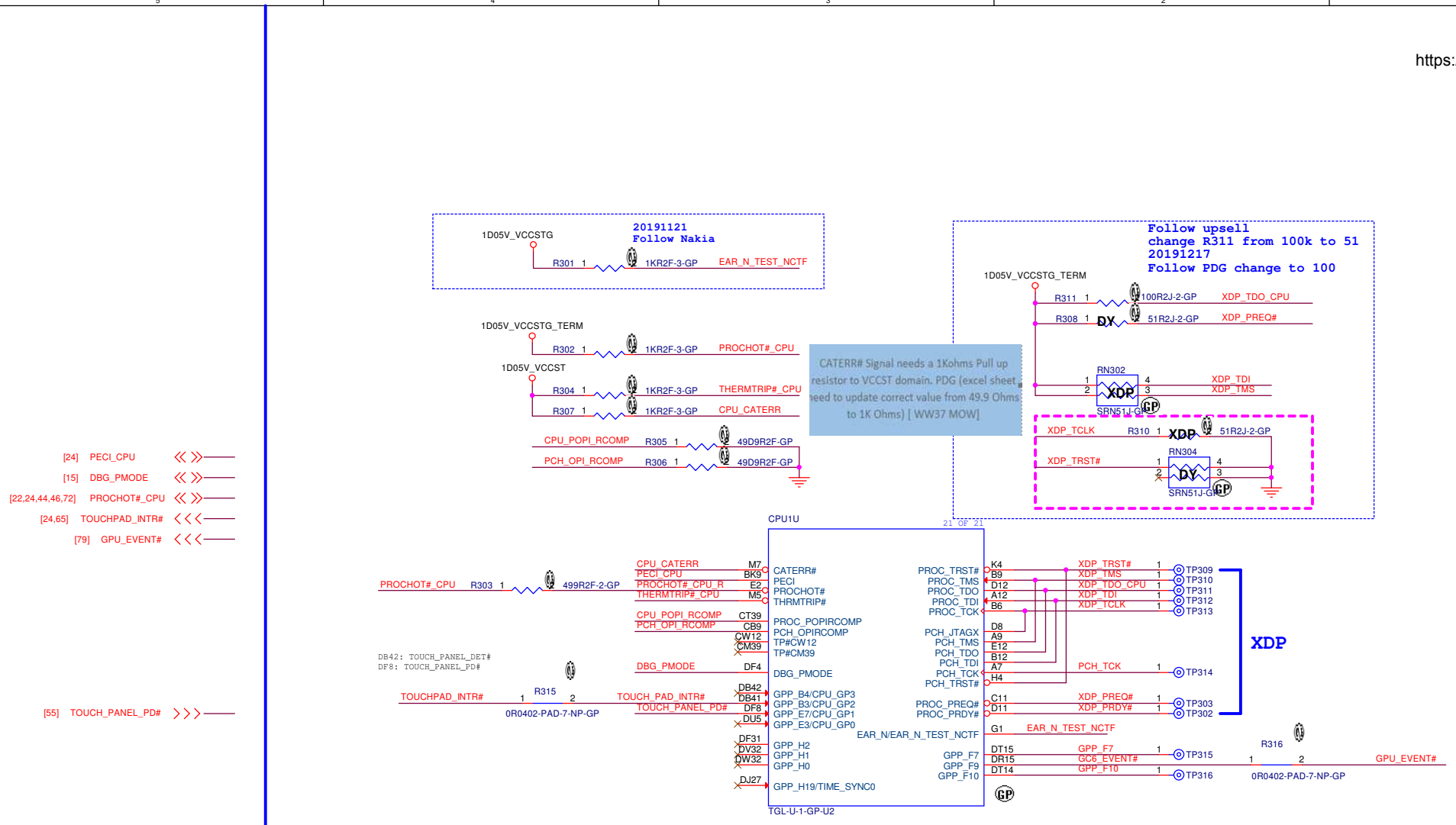
Title
Block Diagram
Size: Custom
Document Number: MOCKINGBIRD_TGL
Rev: A00
Date: Saturday, August 01, 2020
Sheet 2 of 185



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Title: CPU (THML/JTAG)

Size	Document Number	Rev
A3	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 3 of 105

eDP

[55] eDP_TX_CPU_N0
[55] eDP_TX_CPU_P0
[55] eDP_TX_CPU_N1
[55] eDP_TX_CPU_P1
[55] eDP_TX_CPU_N2
[55] eDP_TX_CPU_P2
[55] eDP_TX_CPU_N3
[55] eDP_TX_CPU_P3
[55] eDP_AUX_CPU_N
[55] eDP_AUX_CPU_P
[55] EDP_HPD
[24] L_BKLT_EN
[55] eDP_VDD_EN
[55] L_BKLT_CTRL

HDMI

[57] HDMI_DDI_TX_P3
[57] HDMI_DDI_TX_N3
[57] HDMI_DDI_TX_P0
[57] HDMI_DDI_TX_N0
[57] HDMI_DDI_TX_P1
[57] HDMI_DDI_TX_N1
[57] HDMI_DDI_TX_P2
[57] HDMI_DDI_TX_N2
[57] CPU_DPB_CTRL_CLK
[57] CPU_DPB_CTRL_DATA
[57] CPU_DISP_HPDB

TBT

[71] USB1_TCSS_TX_N0
[71] USB1_TCSS_TX_P0
[71] USB1_TCSS_TX_N1
[71] USB1_TCSS_TX_P1
[71] USB1_TCSS_RX_N0
[71] USB1_TCSS_RX_P0
[71] USB1_TCSS_RX_N1
[71] USB1_TCSS_RX_P1
[71] TBT_LSX0_TXD
[15,71] TBT_LSX0_RXD
[71] USB1_TCSS_AUX_P
[71] USB1_TCSS_AUX_N
[72] SOC_OC_FAULT

Other

[15] GPP_E21
[15] GPP_D12
[15] GPP_D10
[65] KB_DET#

USB3.2 Type-A Port2 (IO)

[66] USB_OC1#

DN4: WWAN_GPO_PERST#
DT6: WWAN_CARD_PWR_OFF#
DG47: 3.3V_CAM_EN
DF6: TBT_LSX1_TXD
DN23: SENSOR_DB_DET#
DD6: TBT_LSX1_RXD
DK23: CPU_DDP4_CTRL_CLK
DN21: CPU_DDP4_CTRL_DATA
DF47: CPU_DISP_HPD2
DH52: USB_OC1#
DK45: CPU_DISP_HPD4

CPU1A — 1 OF 21

eDP_TX_CPU_P3 AC2 — DDIA_TXP3
eDP_TX_CPU_N3 AC1 — DDIA_TXN3
eDP_TX_CPU_P2 AD2 — DDIA_TXP2
eDP_TX_CPU_N2 AD1 — DDIA_TXN2
eDP_TX_CPU_P1 AF1 — DDIA_TXP1
eDP_TX_CPU_N1 AF2 — DDIA_TXN1
eDP_TX_CPU_P0 AG2 — DDIA_TXP0
eDP_TX_CPU_N0 AG1 — DDIA_TXN0
eDP_AUX_CPU_P AJ2 — DDIA_AUX_P
eDP_AUX_CPU_N AJ1 — DDIA_AUX_N

TP401 — GPP_E23 DN4 / DT6 — GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD, GPP_E23/DDPA_CTRLDATA

EDP_HPD DR5 — GPP_E14/DDSP_HPDA/DISP_MISCA

HDMI_DDI_TX_P3 T12 — DDIB_TXP3
HDMI_DDI_TX_N3 T11 — DDIB_TXN3
HDMI_DDI_TX_P0 Y11 — DDIB_TXP2
HDMI_DDI_TX_N0 Y9 — DDIB_TXN2
HDMI_DDI_TX_P1 T9 — DDIB_TXP1
HDMI_DDI_TX_N1 P9 — DDIB_TXN1
HDMI_DDI_TX_P2 V11 — DDIB_TXP0
HDMI_DDI_TX_N2 V9 — DDIB_TXN0
AB9 / AD9 — DDIB_AUX_P / DDIB_AUX_N

CPU_DPB_CTRL_CLK DM29 / CPU_DPB_CTRL_DATA DK27 — GPP_H16/DDPB_CTRLCLK/PCIE_LNK_DOWN, GPP_H17/DDPB_CTRLDATA

CPU_DISP_HPDB DG43 — GPP_A18/DDSP_HPDB/DISP_MISCB/I2S4_RXD

20191211 for TBT
KB_DET# DG47 / DJ47 — GPP_A21/DDPC_CTRLCLK/I2S5_TXD, GPP_A22/DDPC_CTRLDATA/I2S5_RXD

TBT_LSX0_TXD DU8 — GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD
TBT_LSX0_RXD DV8 — GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD

GPP_E21 DF6 / DD6 — GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD, GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD

GPP_D10 DN23 / DM23 — GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/GSPI2_CS0#, GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/GSPI2_CLK

GPP_D12 DK23 / DN21 — GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/GSPI2_MISO, GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/GSPI2_MOSI

CPU_DISP_HPD1_R DF43 / DF45 / DF47 — GPP_A17/DISP_MISCC/I2S4_TXD, GPP_A19/DDSP_HPD1/DISP_MISC1/I2S5_SCLK, GPP_A20/DDSP_HPD2/DISP_MISC2/I2S5_SFRM

20191211 follow vendor request
USB_OC1# DH52 / SOC_OC_FAULT DK45 — GPP_A14/USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1, GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK

eDP_VDD_EN DM8 — EDP_VDDEN
L_BKLT_EN DN8 — EDP_BKLTEN
L_BKLT_CTRL DG10 — EDP_BKLTCTL

TGL-U-1-GP-U2

TBT (20191211 for TBT)
TCP0_TXRX_P1 AY2 / TCP0_TXRX_N1 AY1 / TCP0_TXRX_P0 BB1 / TCP0_TXRX_N0 BB2 / TCP0_TX_P1 AM5 / TCP0_TX_N1 AM7 / TCP0_TX_P0 AT7 / TCP0_TX_N0 AT5 / TCP0_AUX_P AP7 / TCP0_AUX_N AP5
USB1_TCSS_RX_P1 / USB1_TCSS_RX_N1 / USB1_TCSS_RX_P0 / USB1_TCSS_RX_N0 / USB1_TCSS_TX_P1 / USB1_TCSS_TX_N1 / USB1_TCSS_TX_P0 / USB1_TCSS_TX_N0 / USB1_TCSS_AUX_P / USB1_TCSS_AUX_N

TCP1_TXRX_P1 AT2 / TCP1_TXRX_N1 AT1 / TCP1_TXRX_P0 AU1 / TCP1_TXRX_N0 AU2 / TCP1_TX_P1 AD5 / TCP1_TX_N1 AD7 / TCP1_TX_P0 AH7 / TCP1_TX_N0 AH5 / TCP1_AUX_P AF7 / TCP1_AUX_N AF5

TCP2_TXRX_P1 BF1 / TCP2_TXRX_N1 BF2 / TCP2_TXRX_P0 BE2 / TCP2_TXRX_N0 BE1 / TCP2_TX_P1 BD7 / TCP2_TX_N1 BD5 / TCP2_TX_P0 AY5 / TCP2_TX_N0 AY7 / TCP2_AUX_P BB5 / TCP2_AUX_N BB7

TCP3_TXRX_P1 BK1 / TCP3_TXRX_N1 BK2 / TCP3_TXRX_P0 BJ2 / TCP3_TXRX_N0 BJ1 / TCP3_TX_P1 BM7 / TCP3_TX_N1 BM5 / TCP3_TX_P0 BH5 / TCP3_TX_N0 BH7 / TCP3_AUX_P BK5 / TCP3_AUX_N BK7

TC_RCOMP_P AN2 / TC_RCOMP_N AN1 — TCSS_RCOMP_P / TCSS_RCOMP_N — R402 1 — 2 150R2F-1-GP
DSI_DE_TE_2 M8
DDI_RCOMP AB1 — DISP_RCOMP — R401 1 — 2 150R2F-1-GP
DISP_UTILS/DSI_DE_TE_1 CE4

R403 1 — DY — 2 100KR2J-1-GP

20191129 layout Request
3D3V_S0 — RN402 — CPU_DPB_CTRL_CLK / CPU_DPB_CTRL_DATA — SRN2K2J-1-GP
R419 1 — 2 10KR2J-3-GP — KB_DET#

3D3V_S5_VCCPRIM — 20191211 Remove R422
R421 1 — 2 10KR2J-3-GP — USB_OC1#
20191224 Follow Internal review

Add RTC Gen 9 reset circuit_20170814 leakage issue
20191224 Follow Internal review

3D3V_S5_VCCPRIM — R406 10KR2J-3-GP — RTC_RST
3D3V_S5_VCCPRIM — R405 10KR2J-3-GP — RTC_RST
Q401 — CPU_DISP_HPD1_R — CPU_DISP_HPD1_P — RTC_RST — 2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C
3rd = 075.67002.007C
4th = 075.07002.0A7C

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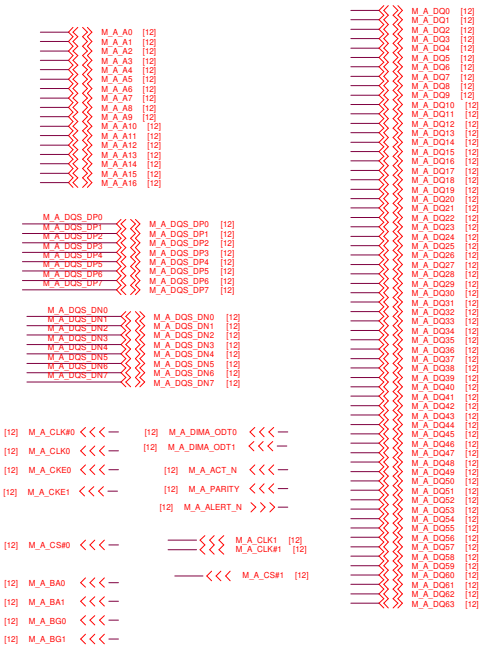
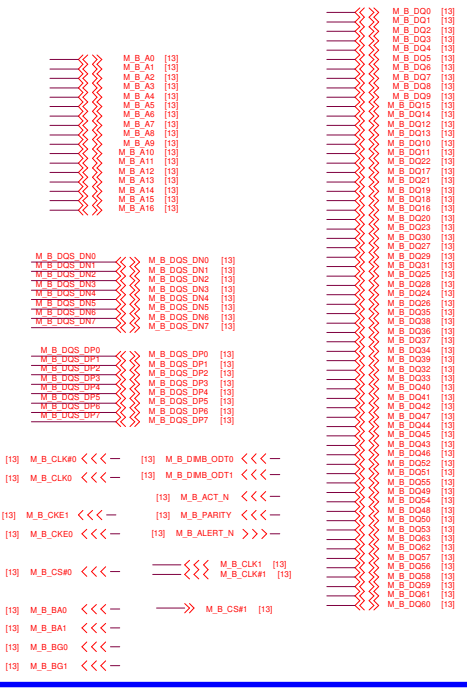
Title	CPU (DDI/EDP/TBT/TPC/)	
Size A3	Document Number MOCKINGBIRD_TGL	Rev A00
Date: Saturday, August 01, 2020	Sheet 4 of 105	

DDR4 ball type: Non-Interleaved Type

Channel A

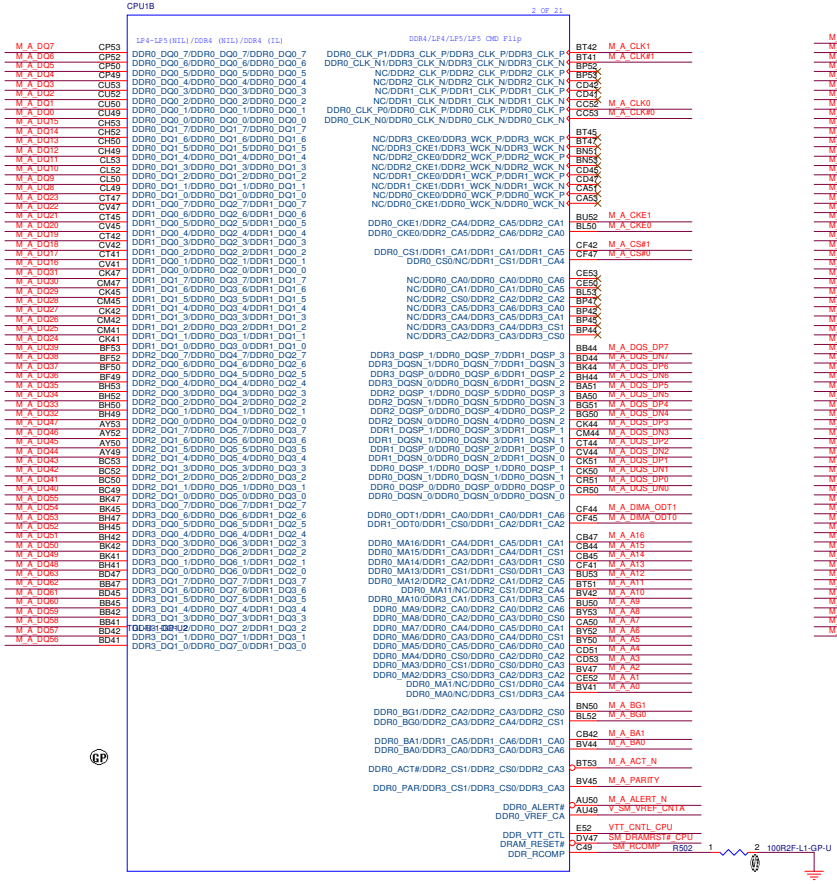


Channel B



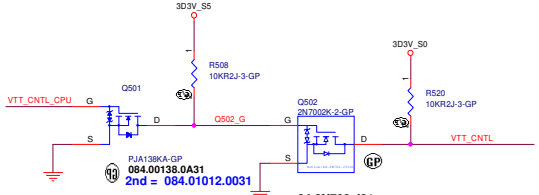
[12] V_SM_VREF_CNTA
[13] V_SM_VREF_CNTB
[51] VTT_CNTL
[12,13] DDR4_DRAMRST#

CPU1B



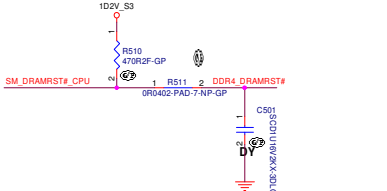
CPU1C

VTT_CNTL_CPU circuit



84.2N702.J31
2ND = 084.27002.0N31
3rd = 084.27002.0L31
4th = 084.07002.0C31

SM_DRAMRST# circuit



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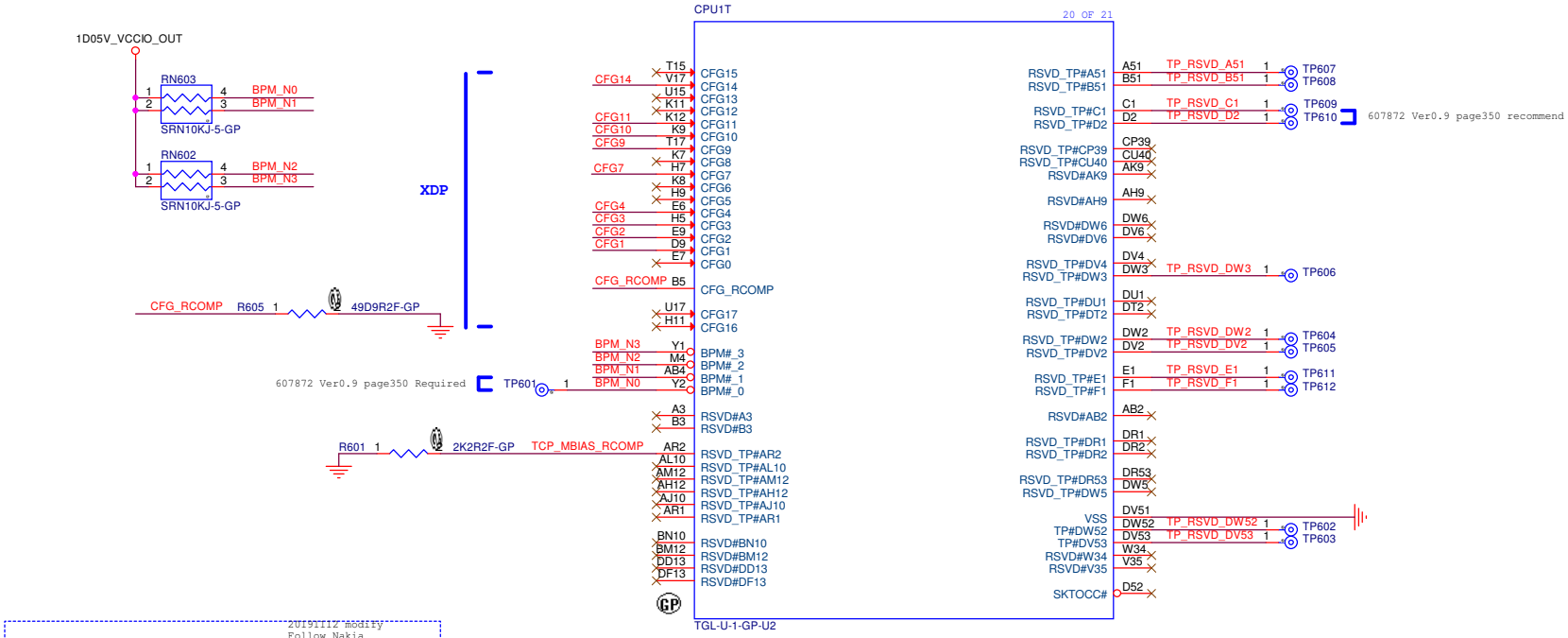
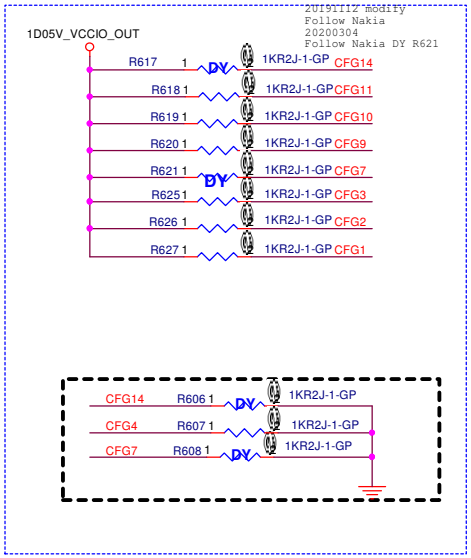
Title: CPU (DDR)

Size	Document Number	Rev
A2	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 5 of 105





607872 Ver0.9 page350 Required

CFG	Description	Termination	Resistor
EAR	Stall CPU reset sequence until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall	Pull-up to VCCSTG	1K ohm
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

Bifurcation	Link Width	CFG Signals	Lanes			
	0:6:0	CFG [14]	0	1	2	3
1x4	x4	0	0	1	2	3
1x4 **Reversed**	x4	1	3	2	1	0

Notes:
1. PCIe* Port60 is a single x4 port without bifurcation capabilities, thus bifurcation pin straps are not applicable.

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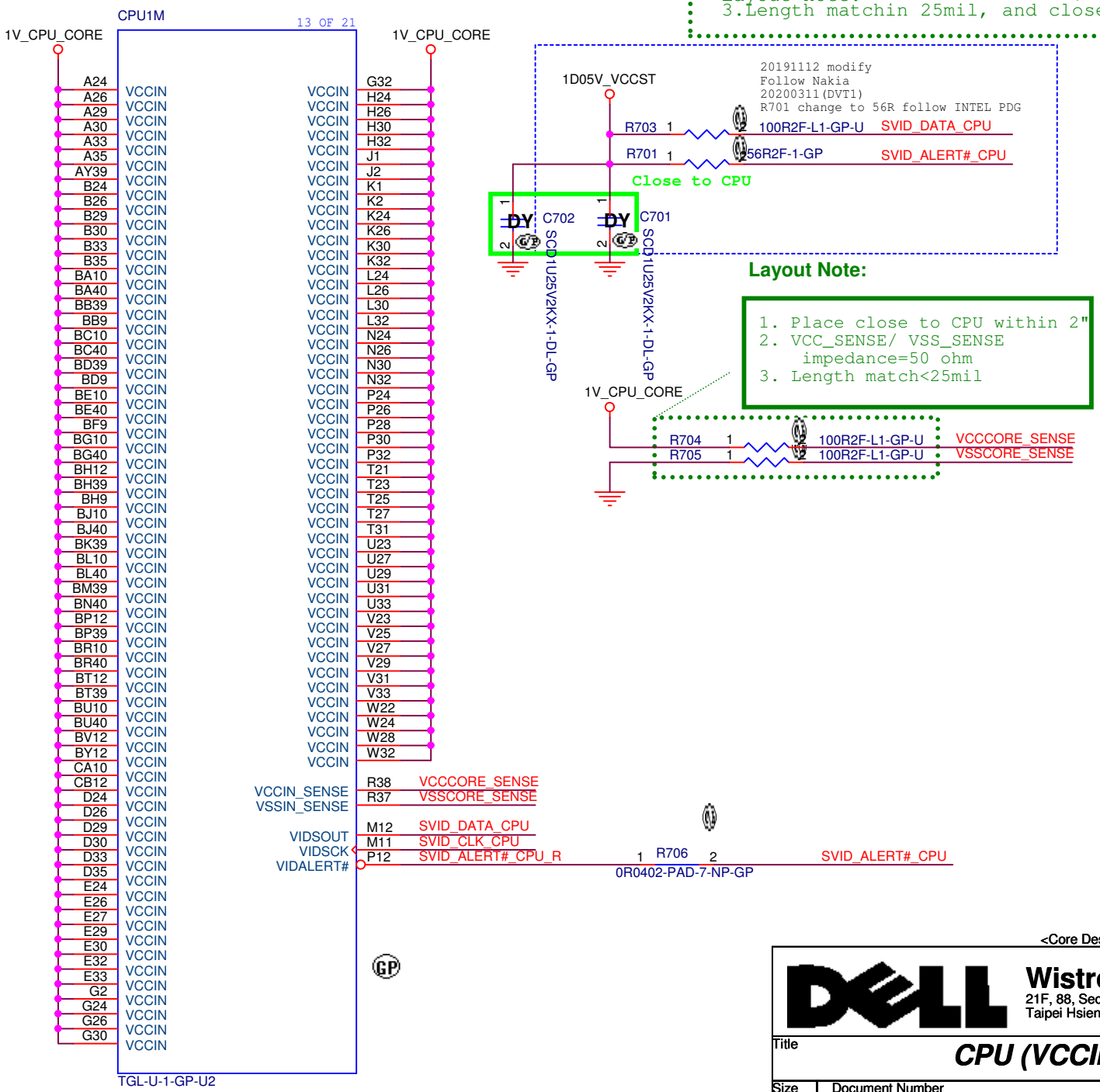
Title: ***CPU (CFG/IST)***

Size	Document Number	Rev
A3	***MOCKINGBIRD_TGL***	***A00***

Date: Saturday, August 01, 2020 Sheet 6 of 105

[46] VCCCORE_SENSE
[46] VSSCORE_SENSE
[46] SVID_ALERT#_CPU
[46] SVID_CLK_CPU
[46] SVID_DATA_CPU



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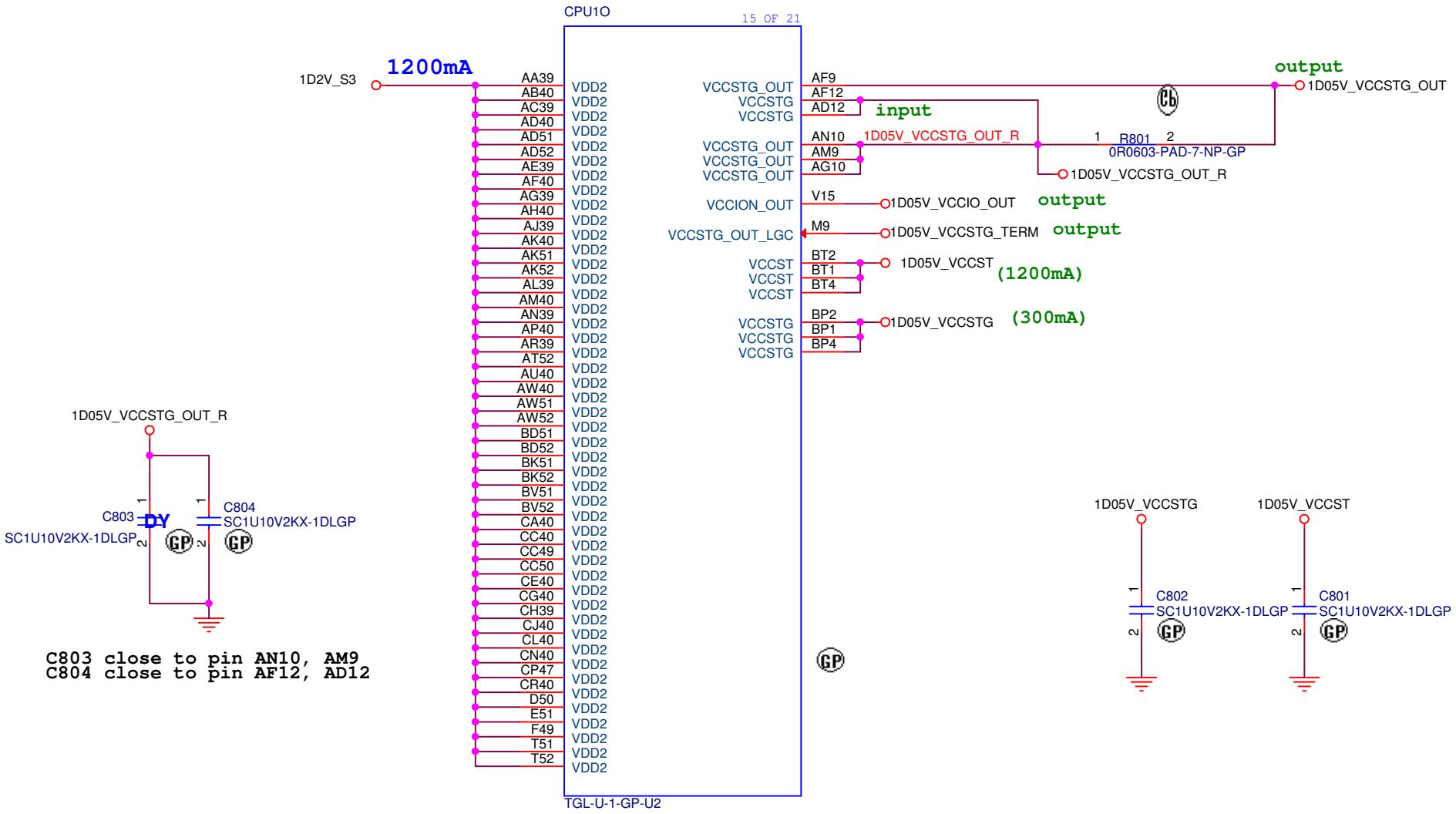
Title	CPU (VCCIN/VID)	
Size A4	Document Number MOCKINGBIRD_TGL	Rev A00
Date: Saturday, August 01, 2020	Sheet 7 of 105	

Main Func = CPU



Lack of VCCPLL_OC / VCC1P8A / VCCPLL

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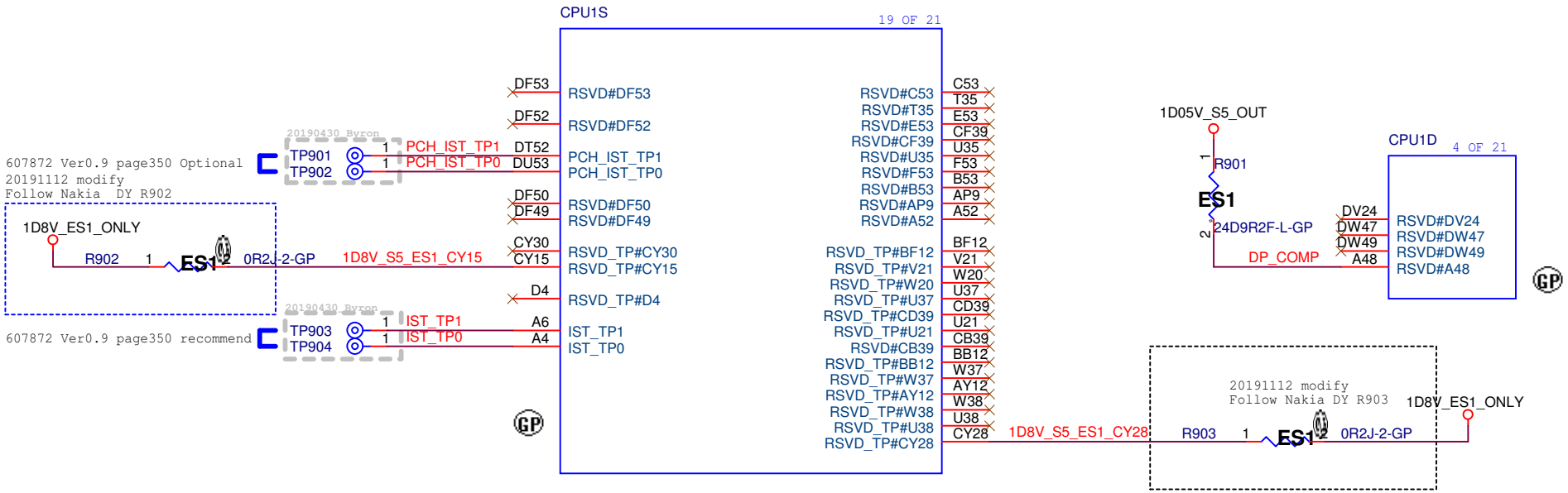
Title	CPU (VDDQ/VCC/VCCST/VCCSTG)	
Size A4	Document Number MOCKINGBIRD_TGL	Rev A00
Date: Saturday, August 01, 2020	Sheet 8 of 105	



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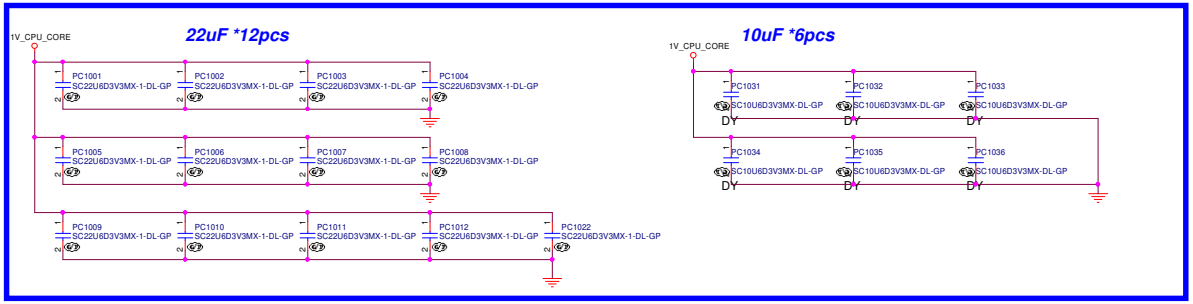
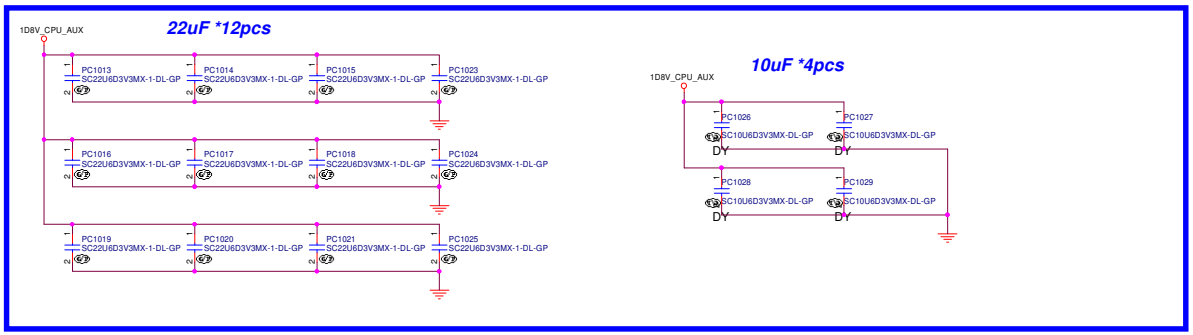
Title: ***CPU (RSVD)***

Size	Document Number	Rev
A4	***MOCKINGBIRD_TGL***	***A00***

Date: Saturday, August 01, 2020 Sheet 9 of 105

Main Func = CPU





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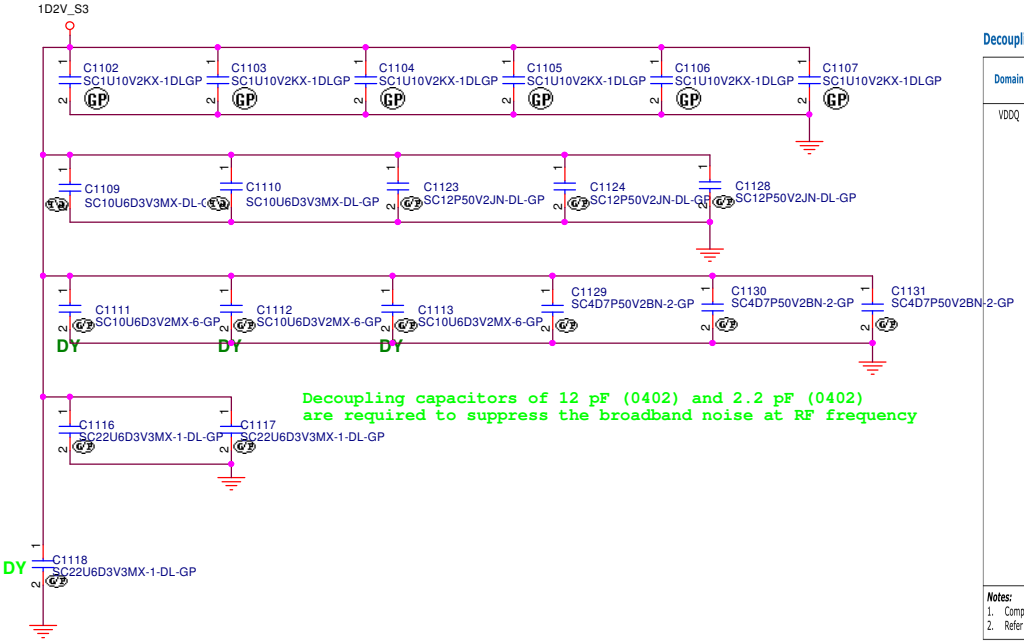
Title: CPU (CORE Power Cap1)

Size	Document Number	Rev
A2	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 10 of 105

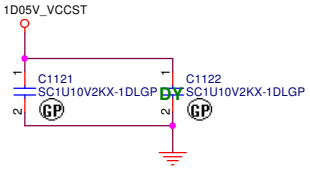
Main Func = CPU

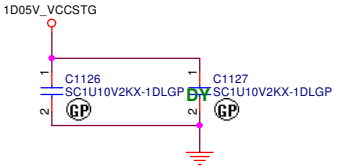


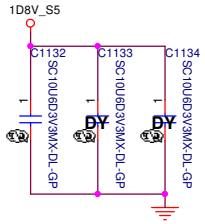
Decoupling Requirements for Ice Lake U Processor for VDDQ

Domain	Backside cap	Primary side cap	Placement guideline [3]
VDDQ	6x 1uF 0402		Place on the back side of the SoC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitor such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.
	2x 10uF 0402		Place on the back side of the SoC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitor such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.
	3x 0402 (placeholder)		Place on the back side of the SoC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitor such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.
	2x 22uF 0603		Place after the TOP DDR signal breakout. These should not be omitted on SODIMM designs, and can be removed only in Memory Down designs when the following conditions are met: 1) DRAM's are soldered down, so their decoupling is shared with the SoC. 2) DRAM's and SoC VDDQ plane copper is shared between both directly (no shorting resistors, pads or similar in the middle). 3) DRAM's are placed close to the SoC allowing that at least 5x10uF capacitors of the DRAM decoupling is within a 30mm radius from SoC Edge.
	1x 0603 (placeholder)		Place after the TOP DDR signal breakout.

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-10 for decoupling capacitor placements.







11/5 Tery Don
add 1D8V_S5 decoupling cap. follow Shuri

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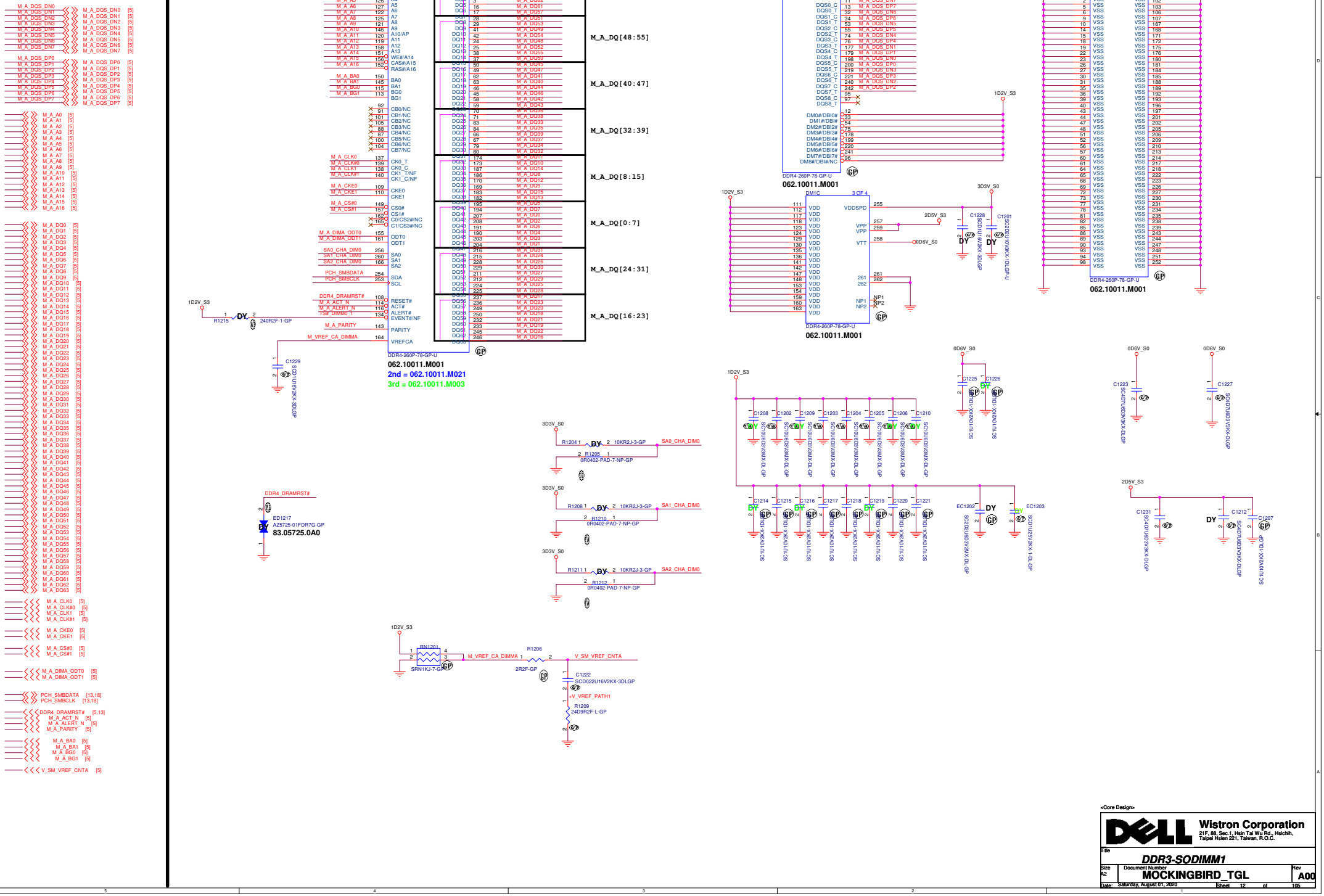
Title	CPU (Power Cap2)	
Size A3	Document Number MOCKINGBIRD_TGL	Rev A00
Date: Saturday, August 01, 2020	Sheet 11 of 105	

Main Func = MEMORY



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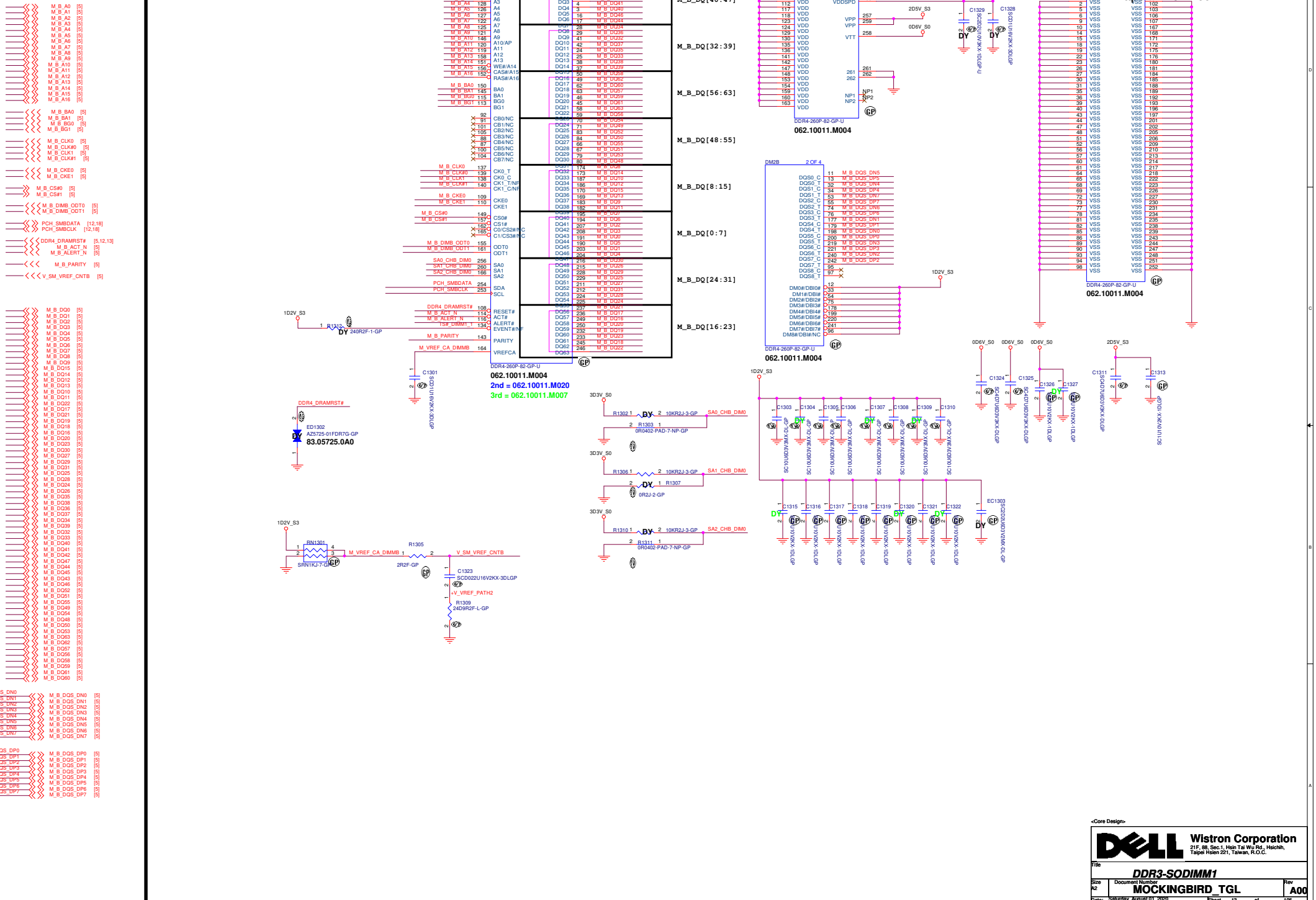
Title: DDR3-SODIMM1

Size: A2 | Document Number: MOCKINGBIRD_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 12 of 105

Main Func = MEMORY



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Title: DDR3-SODIMM1

Size: A2 | Document Number: MOCKINGBIRD_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 13 of 105

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Taipei Hsien 221, Taiwan, R.O.C.

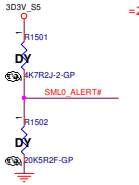
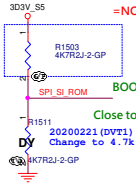
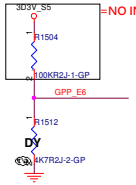
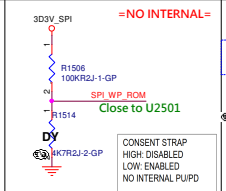
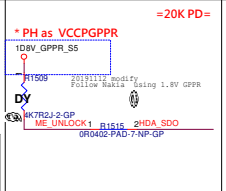
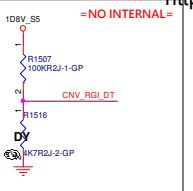
Title: ***DDR (RSVD) (DDR4-CHA1)***

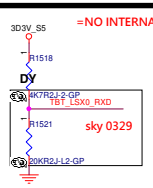
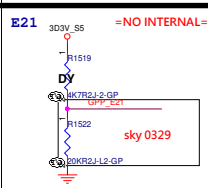
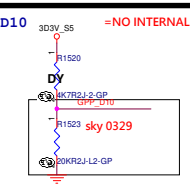
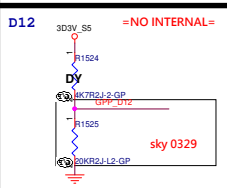
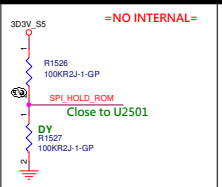
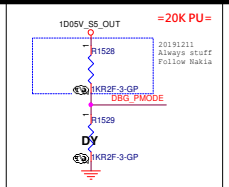
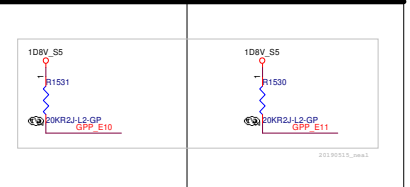
Size	Document Number	Rev
A4	***MOCKINGBIRD_TGL***	***A00***

Date: Saturday, August 01, 2020 Sheet 14 of 105

[18,24,25,91] SPI_SI_ROM
[18,24,25] SPI_WP_ROM
[18,24,25] SPI_HOLD_ROM

[21] CNV_RGI_DT
[18] SML0_ALERT#
[18] GPP_E6
[19] HDA_SDO
[4,71] TBT_LSX0_RXD
[4] GPP_D10
[3] DBG_PMODE
[4] GPP_D12
[4] GPP_E21
[18] GPP_E10
[18] GPP_E11

GPIO	GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_F2)
Schematic				=20K PD=			
High	ESPI Disable	Disable	Enable	19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)	Disable	OVERRIDEN	INTEGRATED CNVI DISABLE
Low	Enable =default=	Enable	Disable	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)	Enable	SECURITY MEASURES NOT OVERRIDEN	INTEGRATED CNVI ENABLE

GPIO	TBT LSX VCCIO conf.#0	TBT LSX VCCIO conf.#1	TBT LSX VCCIO conf.#2	TBT LSX VCCIO conf.#3	A0		GPP_E10	GPP_E11
Schematic	E19 	E21 	D10 	D12 				
High	3.3V	3.3V	3.3V	3.3V	Disable	DFXTESTMODE DISABLED (DEFAULT)		
Low	1.8V	1.8V	1.8V	1.8V	Enable	DFXTESTMODE ENABLED		

Original Ref.

GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK	M.2 CNVI MODES	TBT LSX #0
ESPI OR EC LESS HIGH: ESPI IS DISABLED LOW: ESPI SELECTED WEAK INTERNAL PD 20K	BOOT HALT HIGH - DISABLED LOW- ENABLED NO INTERNAL PU/PD	JTAG ODT DISABLE LOW: JTAG ODT DISABLED HIGH: JTAG ODT ENABLED NO INTERNAL PU/PD	CPUNSSC CLOCK FREQ HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL) LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT) WEAK INTERNAL PD 20K	CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	FLASH DESCRIPTOR SECURITY OVERRIDE HIGH: OVERRIDEN LOW: SECURITY MEASURES NOT OVERRIDEN WEAK INTERNAL PD 20K	M.2 CNVI MODES LOW-> INTEGRATED CNVI ENABLE HIGH-> INTEGRATED CNVI DISABLE NO INTERNAL PU/PD	TBT LSX #0 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD
TBT LSX #1	**TBT LSX #2**	**TBT LSX #3**	**A0**	**GPP_E10**	**GPP_E11**		
TBT LSX #1 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #2 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #3 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	A0 PERSONALITY STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD				

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)

Size	Document Number	Rev
A2	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 15 of 105

GPU
[76] GFX_PCIE_TX_P0
[76] GFX_PCIE_TX_N0
[76] GFX_PCIE_RX_P0
[76] GFX_PCIE_RX_N0

[76] GFX_PCIE_TX_P1
[76] GFX_PCIE_TX_N1
[76] GFX_PCIE_RX_P1
[76] GFX_PCIE_RX_N1

M.2 SSD1
[63] SSD_PCIE_TX_P0
[63] SSD_PCIE_TX_N0
[63] SSD_PCIE_RX_P0
[63] SSD_PCIE_RX_N0

[63] SSD_PCIE_TX_P1
[63] SSD_PCIE_TX_N1
[63] SSD_PCIE_RX_P1
[63] SSD_PCIE_RX_N1

[63] SSD_PCIE_TX_P2
[63] SSD_PCIE_TX_N2
[63] SSD_PCIE_RX_P2
[63] SSD_PCIE_RX_N2

[63] SSD_PCIE_TX_P3
[63] SSD_PCIE_TX_N3
[63] SSD_PCIE_RX_P3
[63] SSD_PCIE_RX_N3

M.2 SSD2
[63] SSD_PCIE_TX_P9
[63] SSD_PCIE_TX_N9
[63] SSD_PCIE_RX_N9
[63] SSD_PCIE_RX_P9

[63] SSD_PCIE_TX_P10
[63] SSD_PCIE_TX_N10
[63] SSD_PCIE_RX_P10
[63] SSD_PCIE_RX_N10

[63] SSD_PCIE_TX_P11
[63] SSD_PCIE_TX_N11
[63] SSD_PCIE_RX_P11
[63] SSD_PCIE_RX_N11

[63] SSD_PCIE_TX_P12
[63] SSD_PCIE_TX_N12
[63] SSD_PCIE_RX_P12
[63] SSD_PCIE_RX_N12

[63] M2_DEVSLP1
[63] M2_PEDET1

USB1
USB3.2 Type-A Port1 (MB)
[35] USB1_USB30_RX_N
[35] USB1_USB30_RX_P
[35] USB1_USB30_TX_N
[35] USB1_USB30_TX_P

[35] USB1_USB20_P
[35] USB1_USB20_N

[35] USB_OC0#

USB2
USB3.2 Type-A Port2 (IO)
[66] USB2_USB30_RX_N
[66] USB2_USB30_RX_P
[66] USB2_USB30_TX_N
[66] USB2_USB30_TX_P

[66] USB2_USB20_P
[66] USB2_USB20_N

Card Reader
[66] CARD1_USB20_P
[66] CARD1_USB20_N

Camera
[55] CCD_USB20_P
[55] CCD_USB20_N

Finger Print
[66] FP1_USB20_N
[66] FP1_USB20_P

TpyeC
[72] USB4_USB20_P
[72] USB4_USB20_N

[71,72] TBT_FORCE_PWR

PD
[17,71] PCH_TBT_PERST#

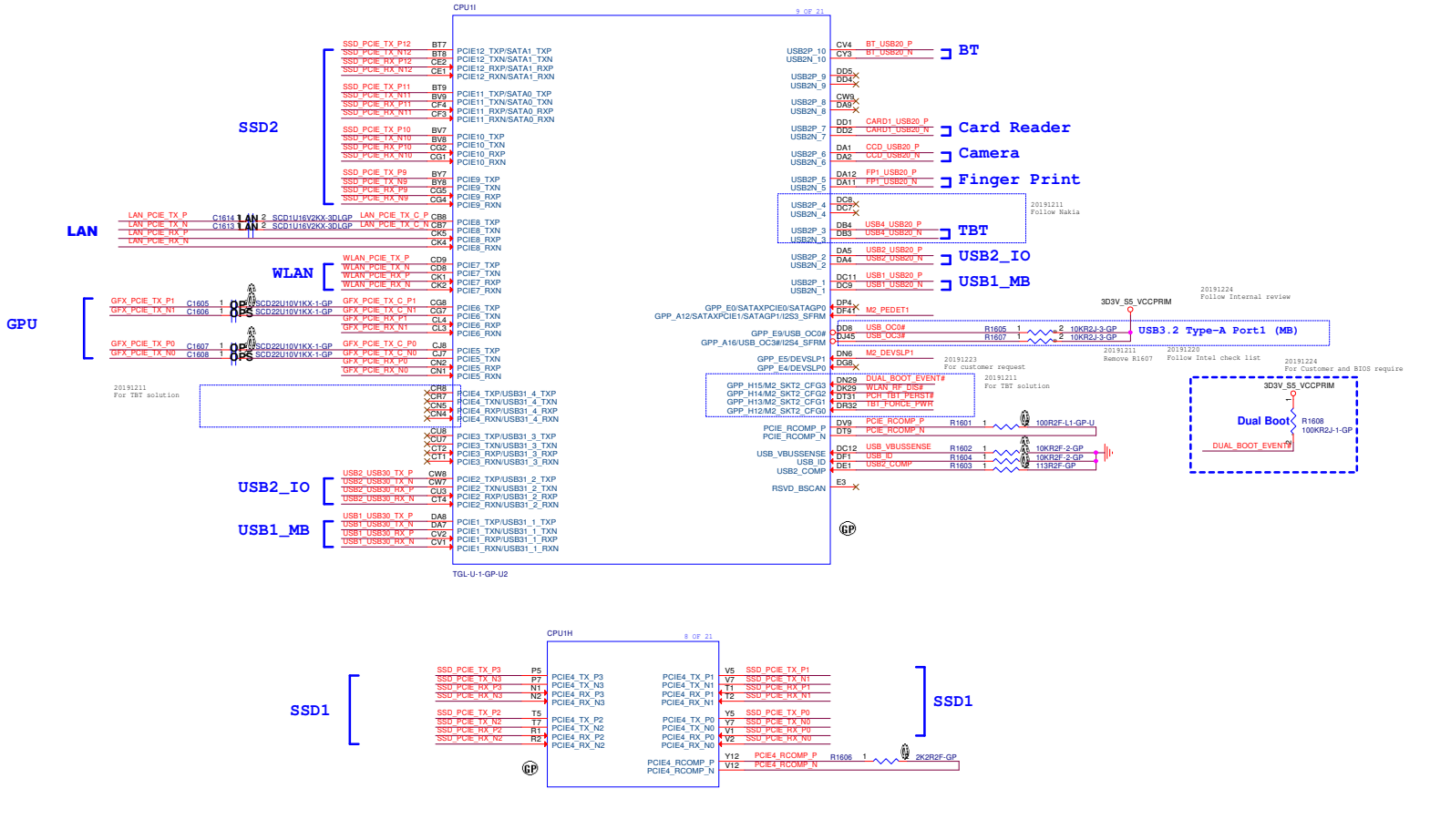
BT
[61] BT_USB20_P
[61] BT_USB20_N

WLAN
[61] WLAN_RF_DIS#

[61] WLAN_PCIE_RX_N
[61] WLAN_PCIE_RX_P
[61] WLAN_PCIE_TX_N
[61] WLAN_PCIE_TX_P

LAN
[66] LAN_PCIE_RX_N
[66] LAN_PCIE_RX_P
[66] LAN_PCIE_TX_N
[66] LAN_PCIE_TX_P

[24] DUAL_BOOT_EVENT#



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB)

Size	Document Number	Rev
A2	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 16 of 105

Power on sequence for G3 sharing

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PMU)

Size: Custom | Document Number: MOCKINGBIRD_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 17 of 105

SPI ROM

[24,25,91] SPI_CLK_ROM
[15,24,25] SPI_HOLD_ROM
[15,24,25] SPI_WP_ROM
[24,25,91] SPI_SO_ROM
[6,24,25,91] SPI_SI_ROM
[24,25] SPI_CS_ROM_N0
[24,25] SPI_CS_ROM_N1
[91] SPI_CS_ROM_N2

[17,64] PM_RSMRST#

EC

[24,68] ESPI_IO0
[24,68] ESPI_IO1
[24,68] ESPI_IO2
[24,68] ESPI_IO3

[24,68] ESPI_CS#
[24,68] ESPI_RESET#
[24,68] ESPI_CLK

Audio

[29] SPK_ID

M.2 SSD

[63] SSD_CLK_CPU_N
[63] SSD_CLK_CPU_P
[63] SSD_CLKREQ_CPU_N
[64] SATA_LED#

[63] SSD2_CLK_CPU_P
[63] SSD2_CLK_CPU_N
[63] SSD2_CLKREQ_CPU_N

GPU

[76] GFX_CLK_CPU_N
[76] GFX_CLK_CPU_P
[76] CLK_PCIE_PEG_REQ#

[76] DGPU_HOLD_RST#
[79,86] GC6_FB_EN

SMBUS

[12,13] PCH_SMBCLK
[12,13] PCH_SMBDATA

[72] SML1_SMBCLK
[72] SML1_SMBDATA
[71] SML0_SMBCLK
[71] SML0_SMBDATA

OTHER

[66] HOST_SD_WP#
[24,61] SUSCLK

HW STRAP

[15] SML0_ALERT#
[15] GPP_E6
[15] GPP_E10
[15] GPP_E11

LAN

[66] LAN_CLK_CPU_N
[66] LAN_CLK_CPU_P
[66] CLK_PCIE_LAN_REQ#

WLAN

[61] WLAN_CLK_CPU_P
[61] WLAN_CLK_CPU_N
[61] CLK_PCIE_WLAN_REQ#

[24,26,79] GPU_THM_SMBCLK
[24,26,79] GPU_THM_SMBDAT

3D3V_S0
R1821 1 2 SPK_ID
10KR2J-3-GP

20191211
Follow Intel TGL PDG
20200512
Follow Intel TGL PDG

CPU1E
5 OF 21

SPI_CLK_ROM 1 SPI_CLK_R_CPU DJ37
SPI_HOLD_ROM 1 SPI_HOLD_R_CPU DG35
SPI_WP_ROM 1 SPI_WP_R_CPU DJ39
SPI_SO_ROM 1 SPI_SO_R_CPU DJ33
SPI_SI_ROM 1 SPI_SI_R_CPU DJ35
SPI_CS_ROM_N1 2 SPI_CS_CPU_N1 DF35
SPI_CS_ROM_N0 2 SPI_CS_CPU_N0 DG37
SPI_CS_ROM_N2 DF39

R1826 0R0402-PAD-7-NP-GP
R1827 0R0402-PAD-7-NP-GP
R1828 0R0402-PAD-7-NP-GP
R1829 0R0402-PAD-7-NP-GP
R1830 0R0402-PAD-7-NP-GP
R1831 0R0402-PAD-7-NP-GP
R1832 0R0402-PAD-7-NP-GP

SPI0_CLK
SPI0_IO3
SPI0_IO2
SPI0_MISO
SPI0_MOSI
SPI0_CS1#
SPI0_CS0#
SPI0_CS2#

GPP_E11 DJ6
GPP_E10 DN5
SATA_LED# DN9
DGPU_HOLD_RST# DM6
GPP_E6 DK6
DT8
DV11
DW9

GPP_E11/SPI1_CLK/THC0_SPI1_CLK
GPP_E2/SPI1_IO3/THC0_SPI1_IO3
GPP_E1/SPI1_IO2/THC0_SPI1_IO2
GPP_E12/SPI1_MISO_IO1/THC0_SPI1_IO1
GPP_E13/SPI1_MOSI_IO0/THC0_SPI1_IO0
GPP_E10/SPI1_CS#/THC0_SPI1_CS#
GPP_E8/SPI1_CS1#/SATA_LED#
GPP_E17/THC0_SPI1_INT#
GPP_E6/THC0_SPI1_RST#

GC6_FB_EN 1 R1842 2 GC6_FB_EN_MCP DN15
0R0402-PAD-7-NP-GP SPK_ID DK13
HOST_SD_WP# DM13
DN13
DJ15
DK15
DN10
DV14
DH3
DH4
DF2

GPP_F11/THC1_SPI2_CLK
GPP_F15/GSXSRESET#/THC1_SPI2_IO3
GPP_F14/GSXDIN/THC1_SPI2_IO2
GPP_F13/GSXSLOAD/THC1_SPI2_IO1
GPP_F12/GSXDOUT/THC1_SPI2_IO0
GPP_F16/GSXCLK/THC1_SPI2_CS#
GPP_F18/THC1_SPI2_INT#
GPP_F17/THC1_SPI2_RST#

CL_CLK
CL_DATA
CL_RST#

DGPU_HOLD_RST# R1843 1 OPS 2 10KR2J-3-GP

GPP_C0/SMBCLK DK21 CPU_SMB_SCL
GPP_C1/SMBDATA DM19 CPU_SMB_SDA
GPP_C2/SMBALERT# DN19 CPU_SMB_ALERT#

GPP_C3/SML0CLK DK19 SML0_SMBCLK
GPP_C4/SML0DATA DM17 SML0_SMBDATA
GPP_C5/SML0ALERT# DN17 SML0_ALERT#

GPP_C6/SML1CLK DK17 SML1_SMBCLK
GPP_C7/SML1DATA DJ17 SML1_SMBDATA
GPP_B23/SML1ALERT#/PCHHOT#/GSPI1_CS1# CY50 SML1_ALERT#

SO-DIMM
BB
PD

GPP_A5/ESPI_CLK DN53 PCH_ESPI_CLK
GPP_A3/ESPI_IO3/SUSACK# DJ53 PCH_ESPI_IO3
GPP_A2/ESPI_IO2/SUSWARN# DH50 PCH_ESPI_IO2
GPP_A1/ESPI_IO1 DP50 PCH_ESPI_IO1
GPP_A0/ESPI_IO0 DP52 PCH_ESPI_IO0
GPP_A4/ESPI_CS# DK52 PCH_ESPI_CS#
GPP_A6/ESPI_RESET# DL50 PCH_ESPI_RESET#

GPP_B23 Strap pin can't pull High
Follow Bacchus
R1804 1 33R2F-3-GP ESPI_CLK
R1808 1 15R2F-2-GP ESPI_IO3
R1807 1 15R2F-2-GP ESPI_IO2
R1806 1 15R2F-2-GP ESPI_IO1
R1805 1 15R2F-2-GP ESPI_IO0
R1809 1 0R0402-PAD-7-NP-GP ESPI_CS#
R1810 1 0R0402-PAD-7-NP-GP ESPI_RESET#
R1814 1 75KR2F-GP
20191211
Follow Intel CRB use 1%

to EC,debug14pin

3D3V_S0
SATA_LED# R1802 1 10KR2J-3-GP
20191217
Follow HC TGL 13

3D3V_S5
RN1803 1 2 4 3 CPU_SMB_SCL CPU_SMB_SDA
SRN1KJ-7-GP

RN1807 1 2 4 3 GPU_THM_SMBCLK GPU_THM_SMBDAT
SRN1KJ-7-GP

RN1801 1 2 4 3 SML1_SMBCLK SML1_SMBDATA
SRN1KJ-7-GP

1D8V_S5
R1823 1 DX 10KR2J-3-GP CPU_SMB_ALERT#
R1824 1 10KR2J-3-GP
R1826 1 DY 10KR2J-3-GP SML1_ALERT#
20191225
Reserve for debug

3D3V_S0
RN1808 1 2 4 3 GP
SRN1KJ-7-GP
Q1802 6 5 4 1 2 3
CPU_SMB_SDA PCH_SMBDATA
PCH_SMBCLK CPU_SMB_SCL
2N7002KDW-1-GP
75.27002.F7C

CPU1K
11 OF 21

SSD2
SSD2_CLK_CPU_P CB2 CLKOUT_PCIE_P6
SSD2_CLK_CPU_N CB1 CLKOUT_PCIE_N6

SSD1
SSD_CLK_CPU_P CL7 CLKOUT_PCIE_P5
SSD_CLK_CPU_N CL8 CLKOUT_PCIE_N5

LAN
LAN_CLK_CPU_P CB4 CLKOUT_PCIE_P4
LAN_CLK_CPU_N CB5 CLKOUT_PCIE_N4

WLAN
WLAN_CLK_CPU_P BY4 CLKOUT_PCIE_P3
WLAN_CLK_CPU_N BY3 CLKOUT_PCIE_N3

GPU
GFX_CLK_CPU_P CN7 CLKOUT_PCIE_P2
GFX_CLK_CPU_N CN8 CLKOUT_PCIE_N2

CLKOUT_PCIE_P1
CLKOUT_PCIE_N1
CLKOUT_PCIE_P0
CLKOUT_PCIE_N0

R1819 1 2 60D4R2F-GP XCLK_BIASREF DJ5
TGL-U-1-GP-U2
XCLK_BIASREF

GPP_F19/SRCCLKREQ8# DU14 SSD2_CLKREQ_CPU_N
GPP_H11/SRCCLKREQ9# DG25
GPP_H10/SRCCLKREQ4# DT24 SSD_CLKREQ_CPU_N
GPP_D8/SRCCLKREQ3# DT30 CLK_PCIE_LAN_REQ#
GPP_D7/SRCCLKREQ2# DV30 CLK_PCIE_WLAN_REQ#
GPP_D6/SRCCLKREQ1# DW30 CLK_PCIE_PEG_REQ#
GPP_D5/SRCCLKREQ0#

XTAL_OUT DM1 XTAL_38D4M_X2_CPU
XTAL_IN DL1 XTAL_38D4M_X1_CPU
R1844 0R2J-2-GP XTAL_38D4M_X2
R1845 0R2J-2-GP XTAL_38D4M_X1
20200302(DVT1)
Add R1844 R1845 for EMC protect

GPD8/SUSCLK DW41 SUSCLK

RTCX2 DT47 XTL_32K_X2_CPU
RTCX1 DR47 XTL_32K_X1_CPU

RTCRST# DN37 RTC_RST#
SRTCRST# DK37 SRTC_RST#

3D3V_S0
RN1805 1 2 3 4 8 7 6 5 CLK_PCIE_LAN_REQ# CLK_PCIE_PEG_REQ# CLK_PCIE_WLAN_REQ# SSD2_CLKREQ_CPU_N
SRN10KJ-6-GP
R1801 1 2 SSD_CLKREQ_CPU_N
10KR2J-3-GP

RTC_AUX_S5
RN1802 1 2 3 4 SRTC_RST# RTC_RST#
SRN20KJ-1-GP
G1801 GAP-OPEN
C1804 SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP C1803

Layout: Place at the open door area.

20191028 Mao Lee (EVT1)
For PCIE4_0 need use #3 or #0

DJ6: TS_SPI_CLK
DN5: TS_SPI_IO3
DR9: TS_SPI_IO2
DM6: TS_SPI_SO
DK6: TS_SPI_SI
DK8: TS_SPI_CS#

DW9: DGPU_HOLD_RST#
DK13: SPK_ID
DM13: AUD_PWR_EN
DN13: HOST_SD_WP#
DJ15: WWAN_DR_DET#
DR15: USBC1_AUX_P_BIAS

DV14: USBC1_AUX_N_BIAS
DT24: CLK_PCIE_SD_REQ#
DT30: CLK_PCIE_LAN_REQ#
DK21: MEM_SMBCLK
DN19: MEM_SMBDATA
DN19: SMLB_ALERT#

XTL_32K_X2_CPU
XTL_32K_X1_CPU
R1811 1 10MR2J-L-GP
X1801 XTAL-32768KHZ-88-GP
C1802 SC5P50V2JN-4DLGP
C1801 SC5P50V2JN-4DLGP
082.30003.0191
2nd = 082.30003.0301

XTL_38D4M_X1
XTL_38D4M_X2
R1820 1 200KR2F-L-GP
X1802
XTAL-38D4MHZ-35-GP
C1806 SC10P50V2JN-4DLGP
C1805 SC10P50V2JN-4DLGP
082.30040.0221
2nd = 082.30040.0251
3rd = 082.30040.0231
20200324(DVT2)
X1802 change to common
20200413(DVT2)
BOM use 082.30040.0251 main
082.30040.0221 2nd

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SPI/LPC/SMBS/XTAL/CLK)
Size: A2
Document Number: MOCKINGBIRD_TGL
Rev: A00
Date: Saturday, August 01, 2020
Sheet 18 of 105

Audio
[27] HDA_SYNC_CODEC
[27] HDA_BITCLK_CODEC
[27] HDA_SDOUT_CODEC
[27] HDA_SDIN0_CPU
[15] HDA_SDO
[55] DMIC_PCH_CLK_Q
[55] DMIC_PCH_DATA_Q

GPU
[24,85] DGPU_PWROK
[86] DGPU_PWR_EN

G SENSOR
[70] FFS_INT2

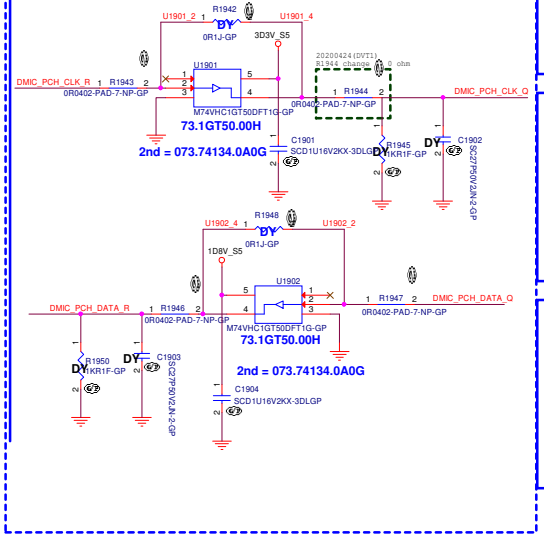
RTC
[25] RTC_DET#

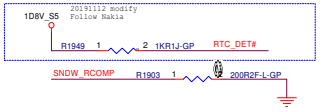
BT
[61] BT_RADIO_DIS#

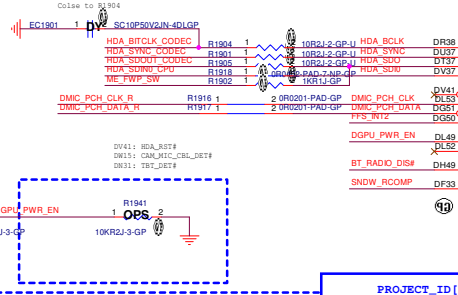
ME
[98] ME_FWP_SW

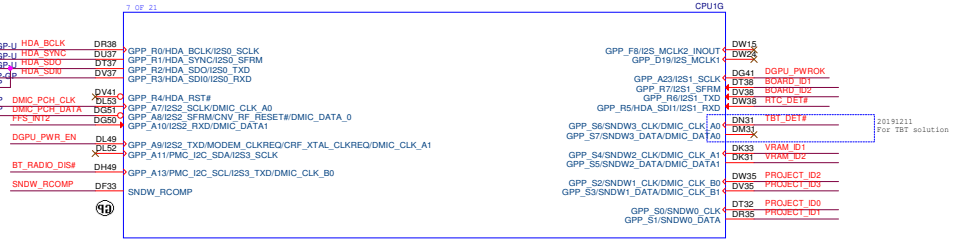
For SITP

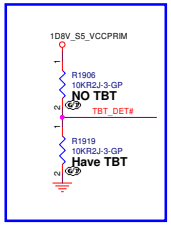
20191129
Follow ICL
20200212
no need level shift
20200331
ADD LEVEL SHIFT to Verify
20200416(DVT2)
Follow MKB AMD solution
20200508(DVT2)
Follow Nakia add DATA's Solution



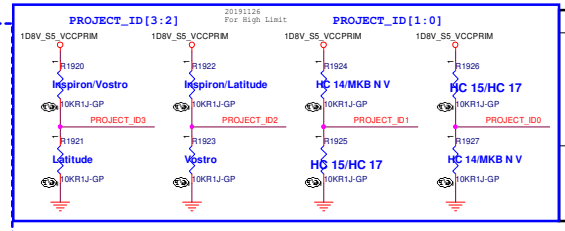




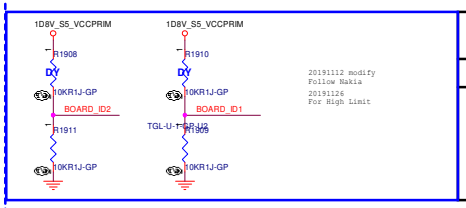




ID	Description	Setting	Mapping
TBT_DET#	TBT function detected	1	no TBT
		0	Have TBT

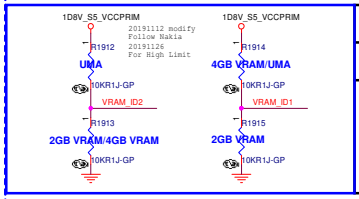


ID	Description	Setting	Mapping
PROJECT_ID[3:2]	Project Type	11	Inspiron
		10	Vostro
		01	Latitude Reseved
		00	N/A
PROJECT_ID[1:0]	Project Series	11	3000 Series
		10	5000 Series(HC 14/MKB N V)
		01	7000 Series(HC 15/HC 17)
		00	N/A



CY20 Board ID Mapping table

ID	Description	Setting	Mapping
Board ID[2:1]	Board SKU ID	11	N/A
		10	N/A
		01	TGL-UP4
		00	TGL-UP3



CY20 VRAM ID Mapping table

ID	Description	Setting	Mapping
VRAM_ID[2:1]	dGPU VRAM size	11	UMA Board
		10	N/A
		01	DIS Board with 4GB VRAM
		00	DIS Board with 2GB VRAM

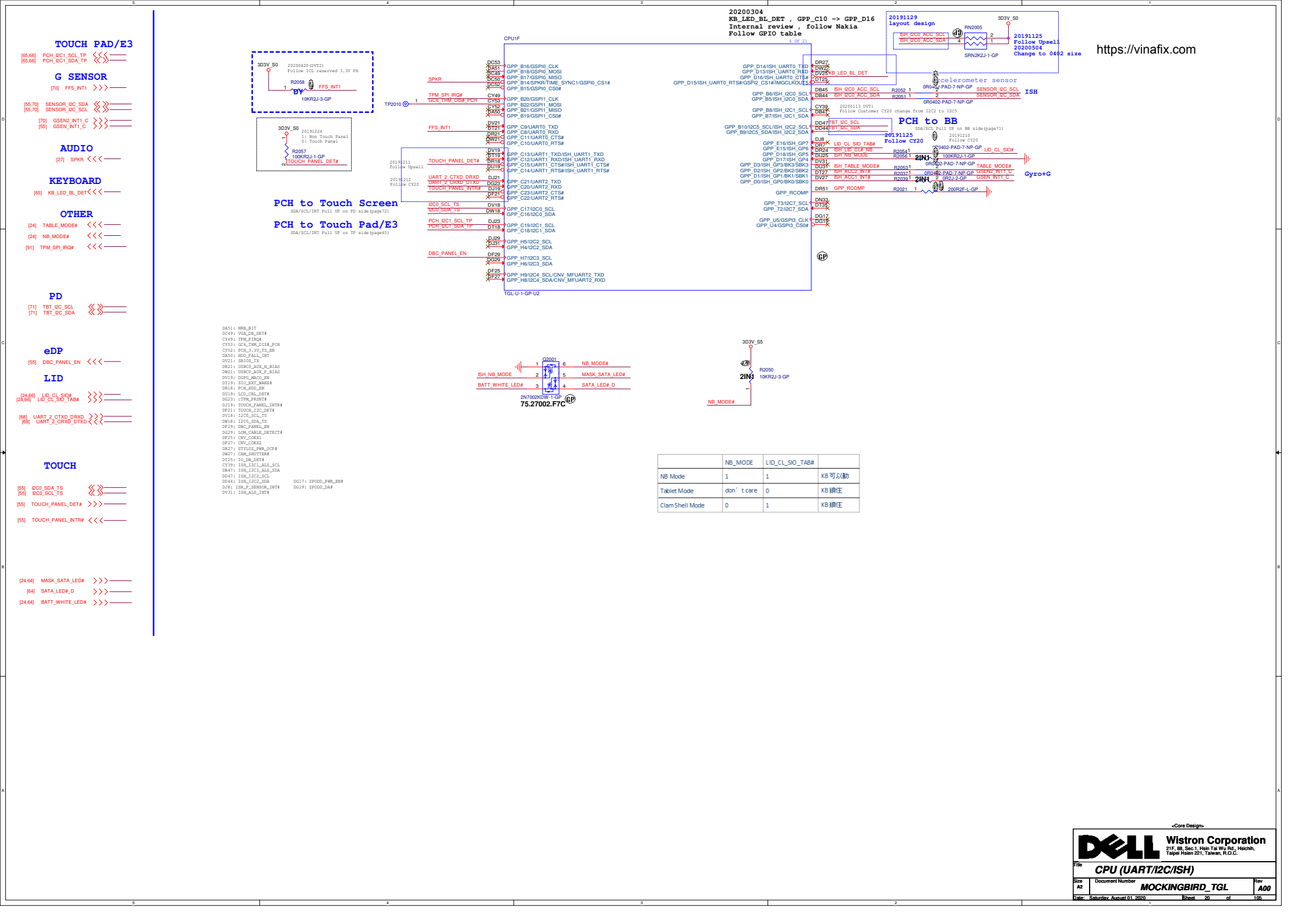
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HAD/I2S/SD/DMIC)

Size	Document Number	Rev
A2	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 19 of 105



	NB_MODE	LID_CL_SIO_TAB#	
NB Mode	1	1	KB可以動
Tablet Mode	don´t care	0	KB鎖住
Clam Shell Mode	0	1	KB鎖住

<Core Design>

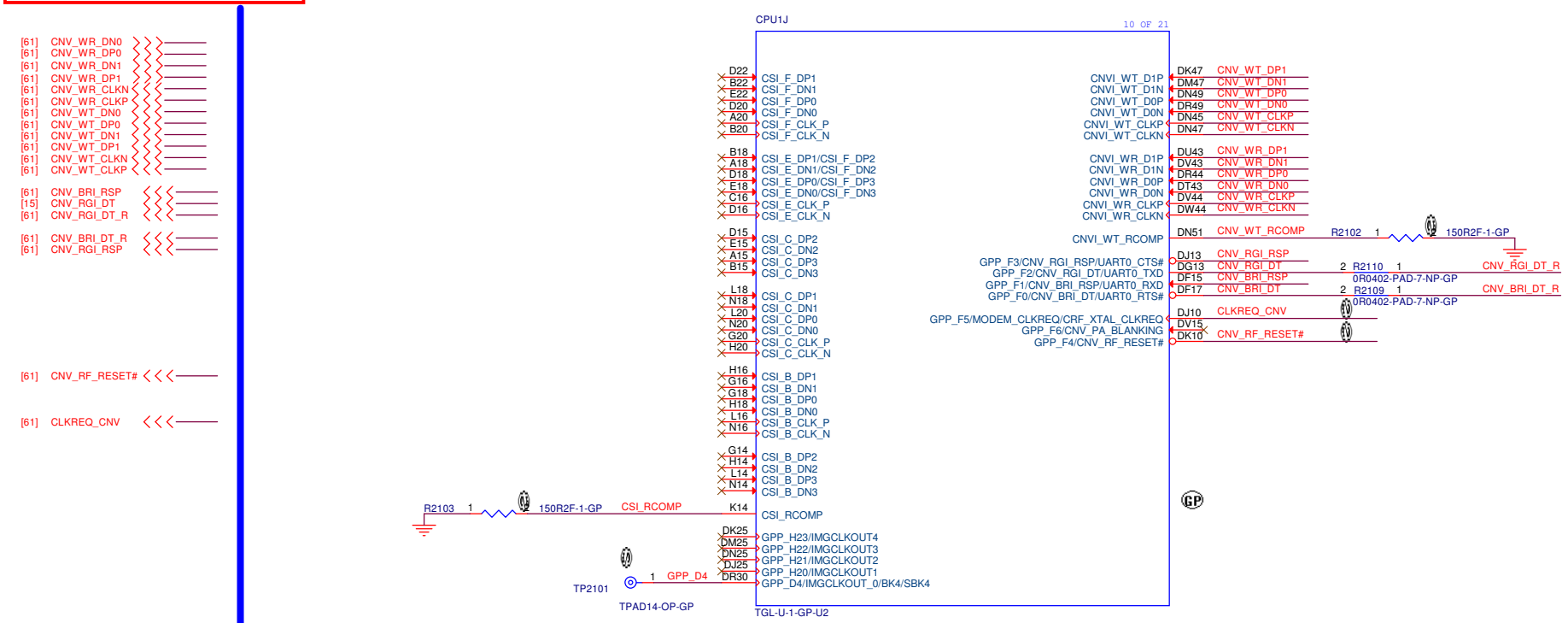
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (UART/I2C/ISH)

Size: A2 | Document Number: MOCKINGBIRD_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 20 of 105

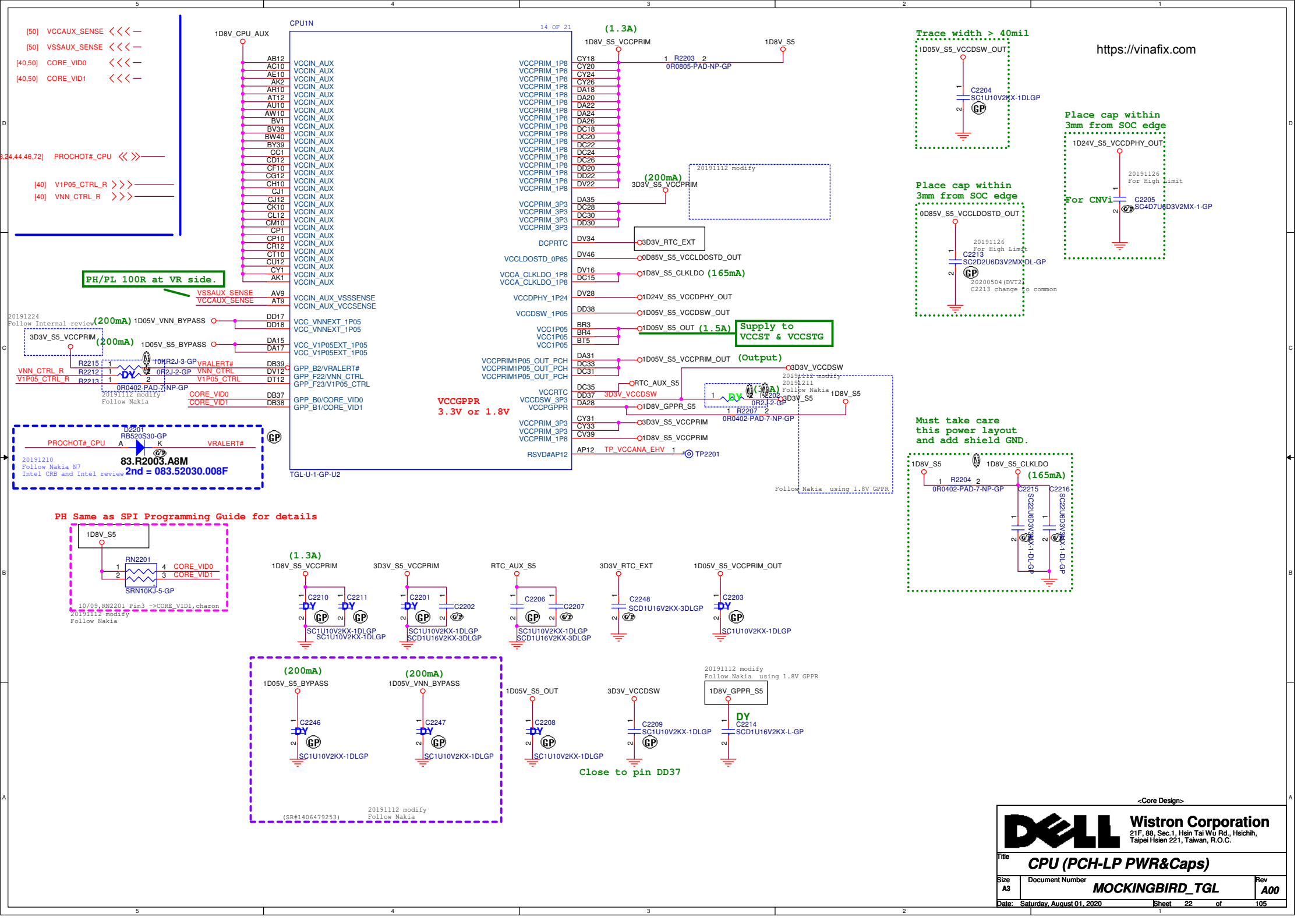
Main Func = PCH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (CSI/EMMC/CNVi)	
Size: A3	Document Number: MOCKINGBIRD_TGL	Rev: A00
Date: Saturday, August 01, 2020	Sheet 21 of 105	

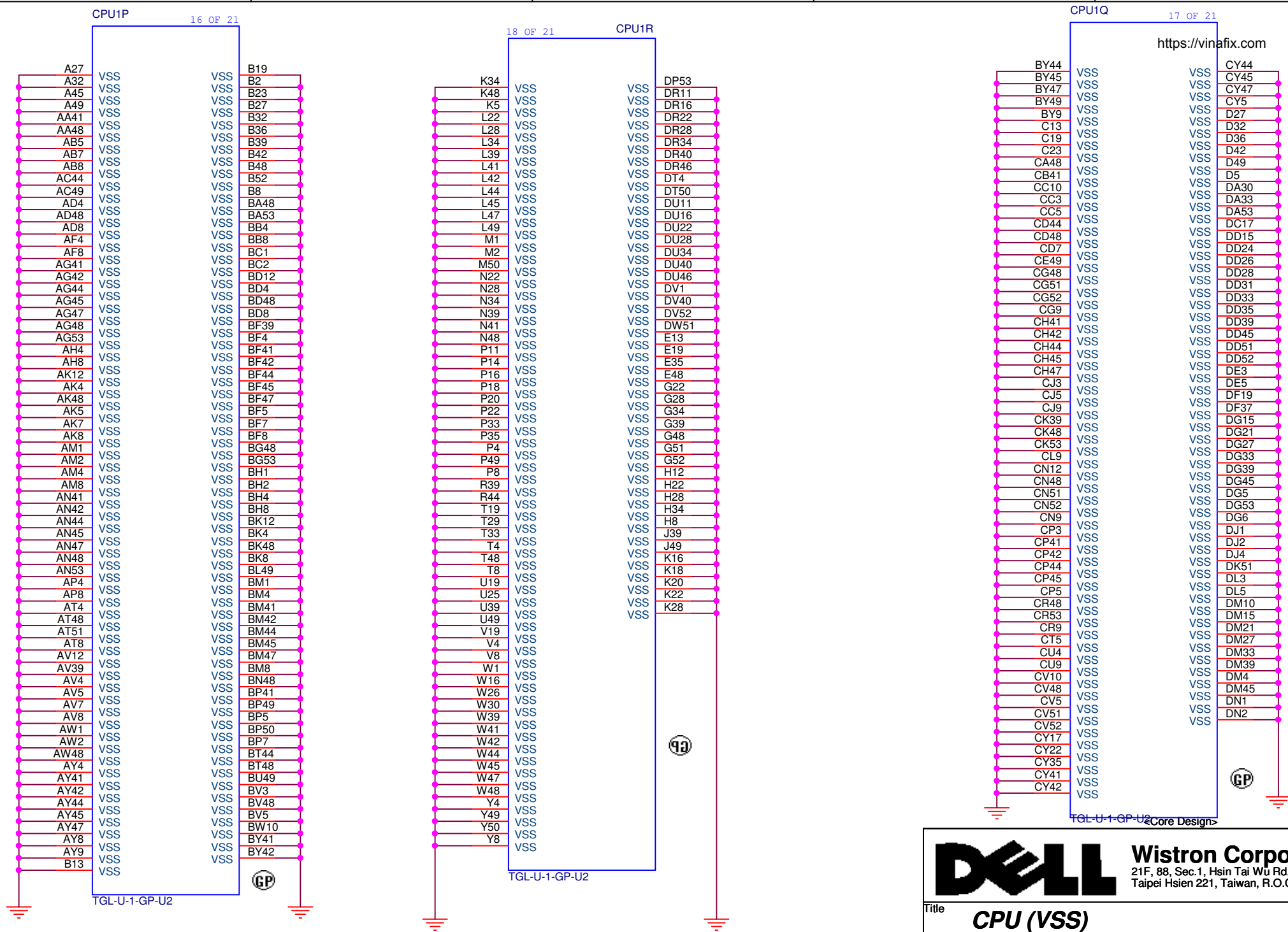


<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCH-LP PWR&Caps)

Size: A3 | Document Number: MOCKINGBIRD_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 22 of 105



DELL	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU (VSS)***	
Size A4	Document Number ***MOCKINGBIRD_TGL***	Rev ***A00***
Date: Saturday, August 01, 2020	Sheet 23 of 105	

Main Func = KBC

Hellcat

#	MODEL_ID(GPIO153)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR(R2442)	VOLTAGE	
1	14" UMA	100.0K	10.0K	3	64.10025.6DL
2		100.0K	17.8K	2.801	64.27025.6DL
3	15" MS UMA	100.0K	27.0K	2.600	
4		100.0K	37.4K	2.402	
5		100.0K	49.9K	2.201	64.64925.6DL
6	17" 2in1 UMA	100.0K	64.9K	2.001	64.82525.6DL
7	14" MS DIS	100.0K	82.5K	1.802	64.10735.6DL
8	15" MS DIS	100.0K	107K	1.594	
9		100.0K	154K	1.299	
10	17" 2in1 DIS	100.0K	200K	1.1	64.20035.6DL

20191203
Change board ID to X00
20200130
Change board ID to X01
20200330
Change board ID to X02
20200730
Change board ID to A00

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	10.0K	3
2	X01	100.0K	17.8K	2.801
3	X02	100.0K	27.0K	2.598
4	X03(reserve)	100.0K	37.4K	2.402
5	A00	100.0K	49.9K	2.201
6	A01	100.0K	64.9K	2.001
7	A02	100.0K	82.5K	1.808
8	Reserve	100.0K	107K	1.594
9	Reserve	100.0K	154K	1.299
10	Reserve	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

Mockingbird

#	MODEL_ID(GPIO153)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR(R2442)	VOLTAGE	
1	M5 14"/15" UMA	100.0K	10.0K	3	64.10025.6DL
2	V5 14"/15" UMA	100.0K	17.8K	2.801	64.17825.6DL
3		100.0K	27.0K	2.598	
4		100.0K	37.4K	2.402	
5	M5 14"/15" DIS	100.0K	49.9K	2.201	64.49925.6DL
6	V5 14"/15" DIS	100.0K	64.9K	2.001	64.64925.6DL
7		100.0K	82.5K	1.808	
8		100.0K	107K	1.594	

MODEL ID

Thermal_DGPU

Layout Note:
Place close to Mec1515

Dual Boot

For eSPI

GPIO045 (CR_STRAP)

EC G3 Flash Share

JTAG DEBUG CONN

For USB TypeC

Power on sequence for G3 sharing

Power Switch Logic(PSL)

83.R2003.A8M
2ND = 083.52030.008F

83.00751.08F
2nd = 83.R2004.G8F

75.27002.F7C

071.01515.0A03

TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO055/SHD_CS0#	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for Boot Note 2 0=Use the eSPI Flash Channel for Boot Note 1	VTR2

Note 1: If the eSPI Flash Channel is used for booting, i.e., eSPI Master Attached Flash Sharing (MAFS), the GPIO055/PWM2/SHD_CS0# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. In addition, the GPIO016/GPT-P_IN1/SHD_IO3/CT3 pin must be used as DSW_PWROK.This pin will also be driven high by the boot ROM code to support Deep Sleep Well timing requirements

2: If the Shared SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

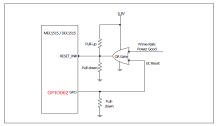
3: The comparator/op-amp is an optional feature that may be enabled in OTP to enable the Boot ROM to configure and lock the Comparator 0 pins. If the feature is enabled in OTP, and external pull-up/pull-down is required to determine the default comparator behavior. If the strap option is not enabled in OTP, the CMP_STRAP is not supported and no external pull-up or pull-down required. Application firmware may enable the comparator if supported by the specific package.

2.4.16 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

GPIO055/SHD_CS0# pin is used to determine the boot source (eSPI Flash channel or shared SPI). In addition, the GPIO055/SHD_CS0# pin is used as an indication that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the SHD_CS0# pin on the board if the Shared SPI flash interface is used so that the SPI_CS0# is detected high while RSMRST# is low.

2.14 MEC1618 / DEC1815 Shared SPI Flash Isolation Requirement



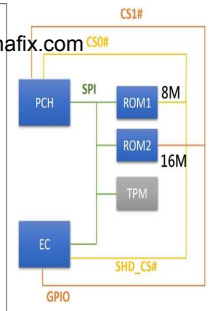
Main Func = SPI Flash

[18,24] SPI_CS_ROM_N1
[18,24] SPI_CS_ROM_N0
[18,24,91] SPI_SO_ROM
[18,24,91] SPI_CLK_ROM
[15,18,24,91] SPI_SI_ROM
[15,18,24] SPI_HOLD_ROM
[15,18,24] SPI_WP_ROM

20200421 (DVT2)
Remove SKT251

3D3V_SPI
R2501 4K7R2J-2-GP
U2501
8M
W25Q64JVSSIQ-GP
072.25Q64.0H01
2nd = 072.25647.000D
3rd = 072.02564.0H01
20191224 Follow Internal review
20200225 change to 8M
20200512 Change to 15R follow Intel PDG
R2508 4K7R2J-2-GP
U2503
16M
W25Q128JVSIQ-GP
072.25128.0B51
2nd = 072.25128.0D61
3rd = 072.25128.0F0D
3D3V_S5
C2501 DY
C2502 SCD1U16V2KX-3DLGP
R2506 0R0402-PAD-7-NP-GP
10/11 add 3D3V_SPI, follow 15 UPSELL
20200304 change R2572 R2573 to 0201
20200512 Change to 15R follow Intel PDG

Figure 217. SPI0 3-Load EC G3 Flash Sharing with FET Isolation Topology



Main Func = RTC

[19] RTC_DET#
[24] VCCDSW_EN
[24] RTCRST_ON
[17,40] SIO_SLP_SUS#
[17,45] 3V_5V_PWRGD

3D3V_AUX_S5
R2502 0R2J-2-GP
3D3V_RTC_SYS
R2503 47K7R2F-GP DY
+RTC_VCC
D2501 BAT54C-12-GP
75.00054.A7D
2nd = 75.00054.T7D
C2503 SCD47U25V3KX-1-DL-GP
R2504 10MR2J-L-GP
3D3V_RTC
Q2501
RTC_DET#
RTC_3P3_EN_G
RTC_3P3_EN_D
2N7002KDW-1-GP
75.27002.F7C
RTC_AUX_S5
Q2507 PJA3413-1-GP
RTC_RST
084.03413.0031
2nd = 084.02301.0031
3rd = 84.00513.03B
R2505 4K7R2J-2-GP
RTCRST_ON
R2567
R2518 100KR2J-1-GP
1MR2J-1-GP
C2517 SCD022U16V2KX-3DLGP

20191120 follow Nakia
3D3V_S5
R2520 100KR2J-1-GP
R2514 10KR2J-3-GP
3V_5V_PWRGD
VCCDSW_EN
D2504 BAT54A-11-GP
75.BAT54.07D
2nd = 075.00054.0A7D
3rd = 75.00054.I7D
4th = 075.00054.0Z7D
20191120
Follow ICL
High limit don't change U2502
U2502 RT9742CGJ5-GP
EN/EN#
VIN
FLG#
GND
VOUT
3D3V_VCCDSW
3D3V_S5_VCCPRIM
R2521 0R0603-PAD-7-NP-GP
074.09742.0A9F
2nd = 074.51712.009F
3rd = 074.03553.007F
4th = 074.03553.0A7F
20191224 Follow Internal review
20191111 follow Nakia
20191112 modify Follow Nakia

<Core Design>

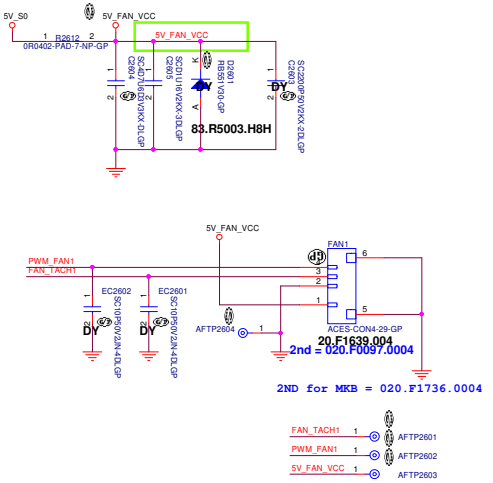
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash
Size: A2
Document Number: MOCKINGBIRD_TGL
Rev: A00
Date: Saturday, August 01, 2020
Sheet 25 of 105

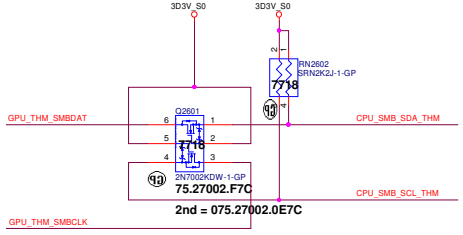
Main Func = Thermal Sensor

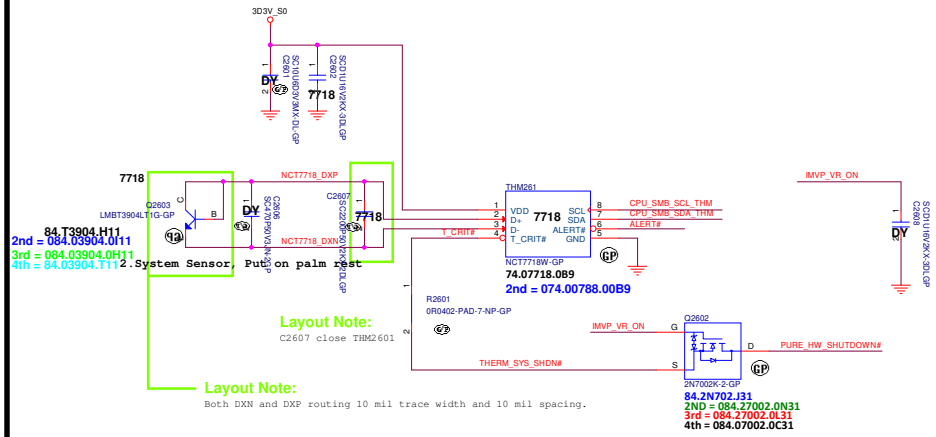
PWM FAN1

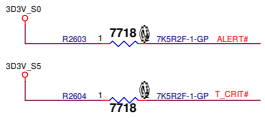
Layout Note:
Place C2602 close to FAN1 pin:
Trace width = 15mil



[18,24,79] GPU_THM_SMBDAT
[18,24,79] GPU_THM_SMBCLK
[17,24] IMVP_VR_ON
[40] PURE_HW_SHUTDOWN#
[24] PWM_FAN1
[24] FAN_TACH1







TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

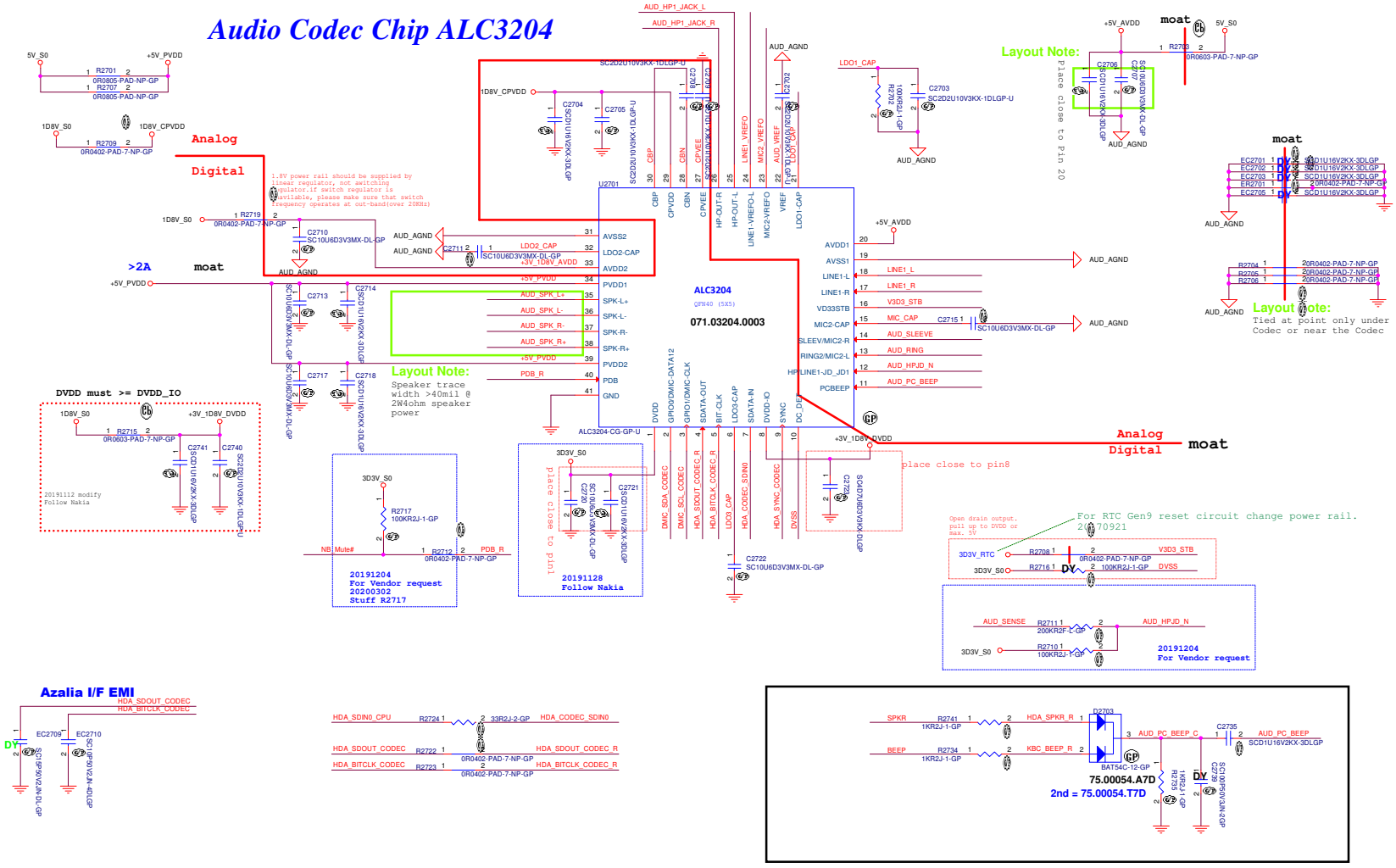
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan
Size: A2
Document Number: MOCKINGBIRD_TGL
Rev: A00
Date: Saturday, August 01, 2020
Sheet 26 of 105

Main Func = Audio

Audio Codec Chip ALC3204



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3204

Size: A2 | Document Number: MOCKINGBIRD_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 27 of 105

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<Core Design>

Wistron Corporation
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Title

(Reserved)

Size	Document Number	Rev
A4	*MOCKINGBIRD_TGL*	*A00*

Date: Saturday, August 01, 2020 Sheet 28 of 105

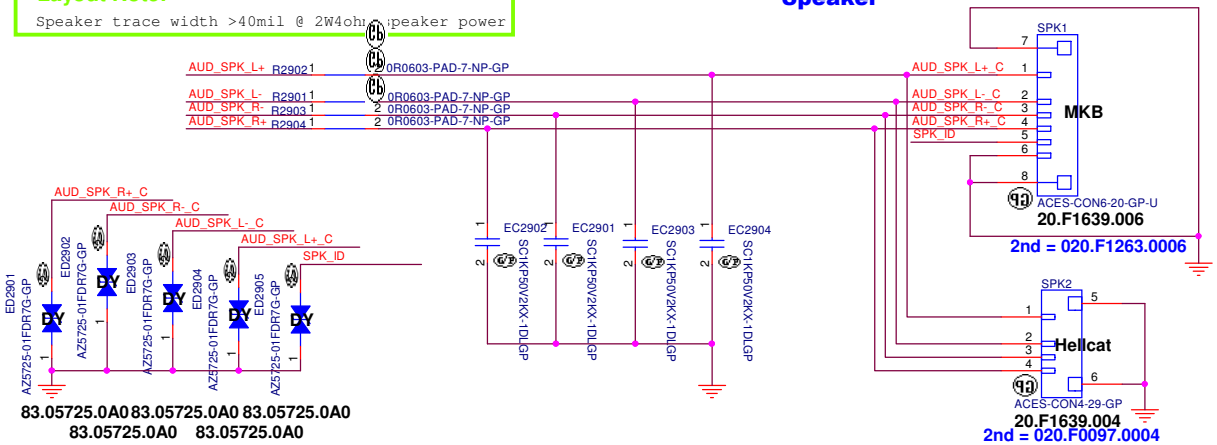
Main Func = Audio

[27] AUD_SPK_R+
[27] AUD_SPK_R-
[27] AUD_SPK_L-
[27] AUD_SPK_L+

[18] SPK_ID

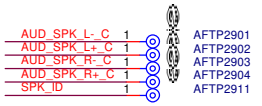
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker



CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

SPK_ID 1: VECO
0: ZY



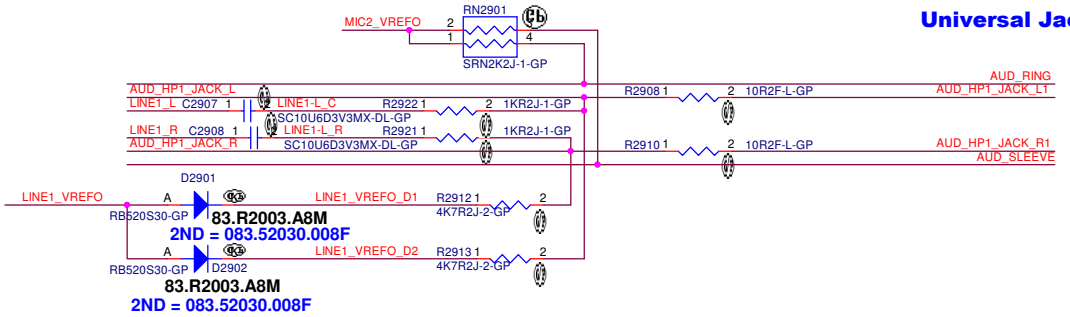
From Codec

[27] MIC2_VREFO
[27,29,66] AUD_RING
[27] AUD_HP1_JACK_L
[27] LINE1_L
[27] LINE1_R
[27] AUD_HP1_JACK_R
[27,29,66] AUD_SLEEVE
[27] LINE1_VREFO

To IO Board

[27,29,66] AUD_RING
[66] AUD_HP1_JACK_L1
[66] AUD_HP1_JACK_R1
[27,29,66] AUD_SLEEVE

Universal Jack (Moved to I/O Board)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio IO

Size	Document Number	Rev
A3	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 29 of 105

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 30 of 105

Main Func = LAN

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8106

Size: Custom | Document Number: MOCKINGBIRD_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 31 of 105

Main Func = LAN

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *XFOM&RJ45*

Size: A3 | Document Number: *MOCKINGBIRD_TGL* | Rev: *A00*

Date: Saturday, August 01, 2020 | Sheet 32 of 105

Main Func = Card Reader

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Card Reader-RTS5170

Size	Document Number	Rev
A4	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 33 of 105

Main Func = USB2.0

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB2.0 CONN

Size | Document Number: MOCKINGBIRD_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 34 of 105

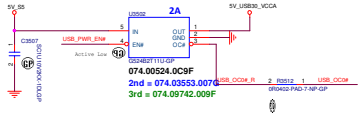
Main Func = USB3.0 Port1

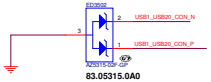
[24,65] USB_PWR_EN#

[16] USB_OC0#

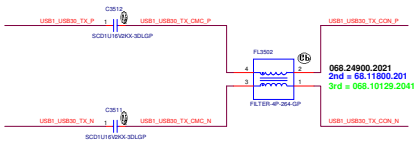
[16] USB1_USB20_N
[16] USB1_USB20_P

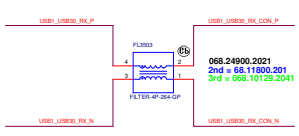
[16] USB1_USB30_TX_N
[16] USB1_USB30_TX_P
[16] USB1_USB30_RX_N
[16] USB1_USB30_RX_P

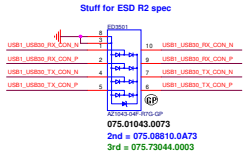


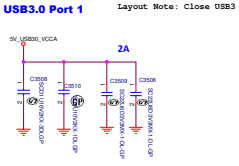


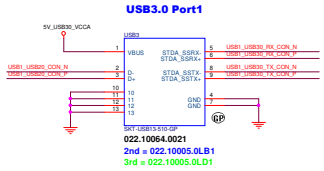
2020/02/29:swap EL3501











<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB3.0 CONN**

Size	Document Number	Rev
A1	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 35 of 156

Main Func = USB Charger

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB Charger*

Size	Document Number	Rev
Custom	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 36 of 105

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB3.0 PORT

Size	Document Number	Rev
A4	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 37 of 105

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<Core Design>

Wistron Corporation
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Title

Reserved

Size	Document Number	Rev
A4	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 38 of 105

<Core Design>

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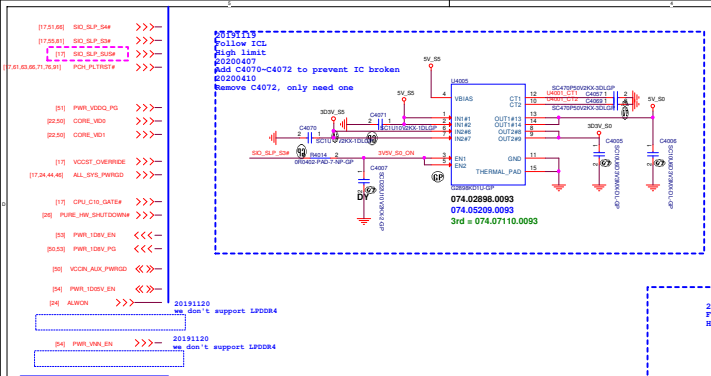
Title

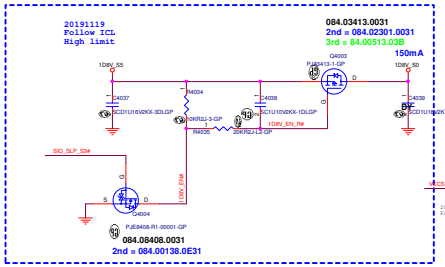
(RSVD)

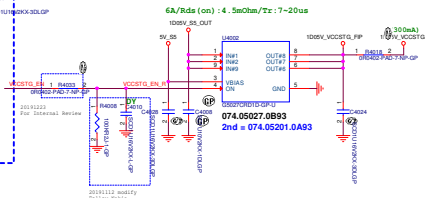
Size	Document Number	Rev
A4	***MOCKINGBIRD_TGL***	***A00***

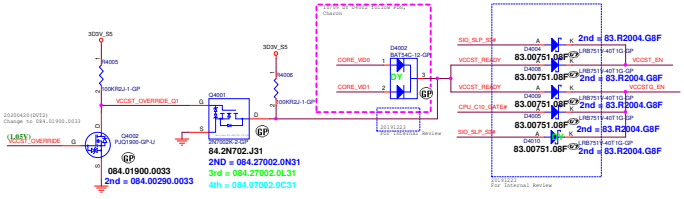
Date: Saturday, August 01, 2020 Sheet 39 of 105

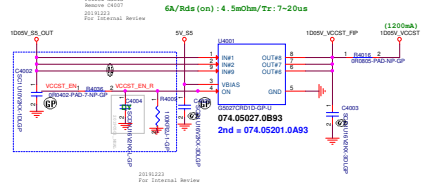
RUN Power



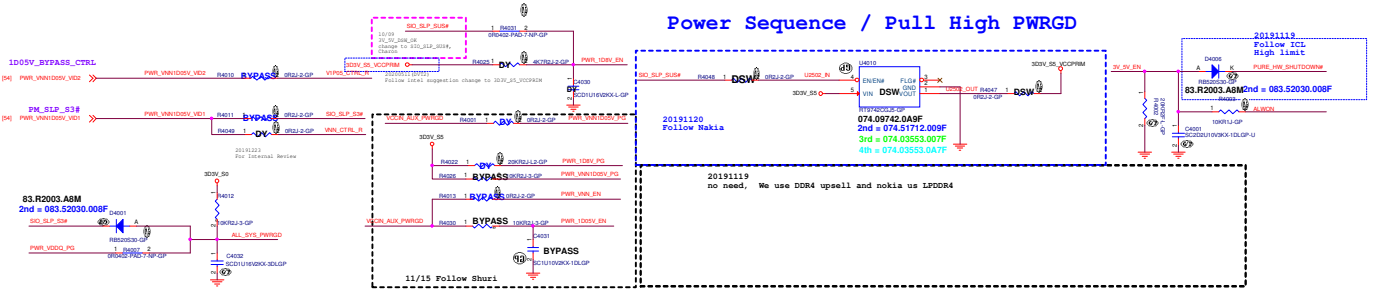




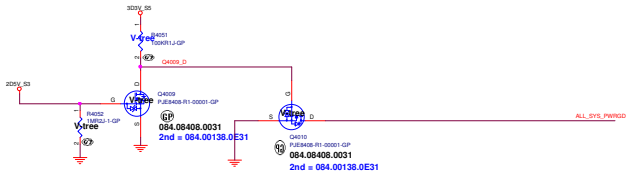


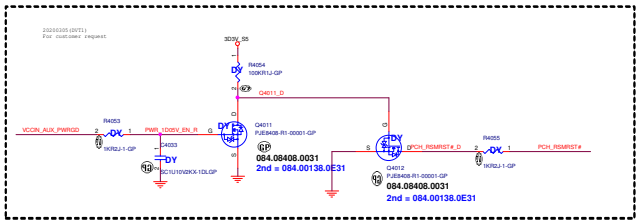


Power Sequence / Pull High PWRGD



V-tree





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«Core Design»
Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
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File: CPU (THML/JTAG)
Size: A1 | Document Number: MOCKINGBIRD_TGL | Rev: A00
Date: Saturday, August 01, 2020 | Sheet 40 of 105

<Core Design>

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Title

Connected_Standby(1/2)+DS3

Size	Document Number	Rev
A4	*MOCKINGBIRD_TGL*	*A00*

Date: Saturday, August 01, 2020 Sheet 41 of 105

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<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Connected_Standby(2/2)*		
Size: A4	Document Number: MOCKINGBIRD_TGL	Rev: A00
Date: Saturday, August 01, 2020	Sheet 42 of 105	

[24,44] AC_DIS

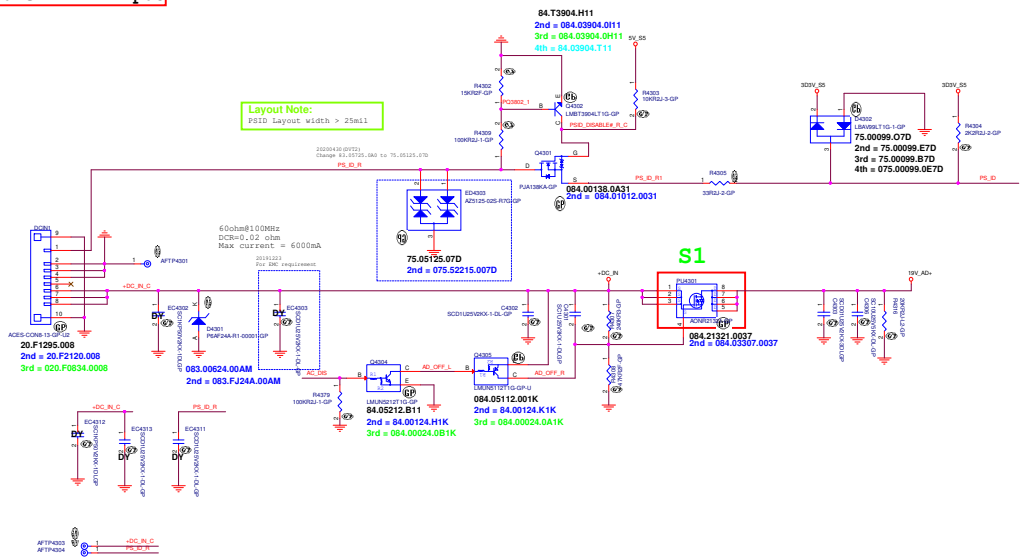
[24] PS_ID

[24,44] HW_ACAVIN_NB

[44,89] +DC_IN_C

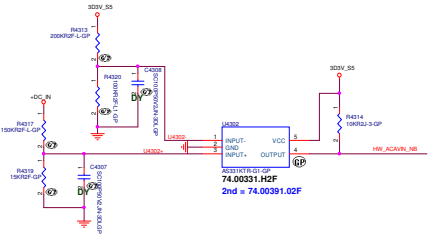
[44,89] +DC_IN

Main Func = ADT Input



https://vinafix.com

Barrel Adapter Piug-in Detect

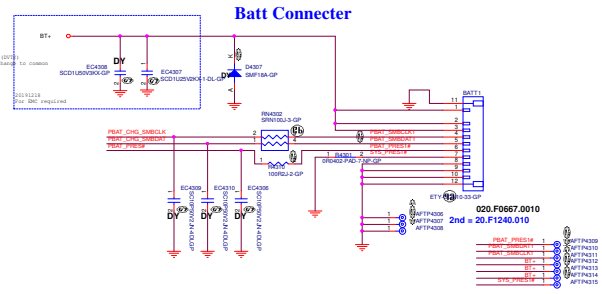


[24,44] PBAT_CHG_SMBCLK

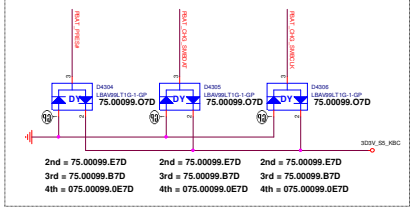
[24,44] PBAT_CHG_SMBDAT

[24,44] PBAT_PRES#

Main Func = M-BAT Input



Placement: Close to Batt Connector



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Title: DCIN
Size: A1 | Document Number: MOCKINGBIRD_TGL | Rev: A00
Date: Saturday, August 01, 2020 | Sheet 43 of 105

ISL9538C For Charger

Main Func = Charger

OFFPAGE

EE needs check it!!

- I2C form EC: PBAT_CHG_SMBDAT, PBAT_CHG_SMBCLK
- To EC: HW_ACAV_IN, AC_INF
- AC_DS
- ISL9538 AMON/BMON to EC: AD_R, PWR_CHG_IMON
- PBAT_PRES#
- From KKP ACK: VCCPD_VBUS_ACK
- HW_ACAVIN_NB
- DGPUHOT#
- CHGR_PSYS_IMVP
- PWR_IMVP_PWRGD
- ALL_SYS_PWRGD
- +DC_IN
- E3: PWR_CHG_VBATN
- PROCHOT#_CPU

S2

084.21321.0037

074.09538.0C73

084.07380.0037
2nd = 084.03323.0037
DCR=8mm~9m Ohm,
Idc=13A, Isats=16A
10.0mm x 11.5mm x 3.0mm

084.07380.0037
2nd = 084.03323.0037

083.R2003.A8M
2ND = 083.52030.008F

083.R2003.A8M
2ND = 083.52030.808F

75.27002.F7C
2nd = 075.27002.0E7C

0523

PU 3V3_AON_S0 on GPU side

84.27N22.031
2ND = 084.27002.0N31
3rd = 084.27002.0L31

PU +VCCSTG = 1.0 V on CPU side

75.27002.F7C
2nd = 075.27002.0E7C

TypeC Prochot
Follow custormer circuits.

TypeC_F

2nd = 84.2N022.031

2nd = 075.PX5D8.007C

CHECK EE
follow custormer circuits.

83.00355.H1F
2nd = 083.00016.0A1F

2nd = 084.03906.0B13

2nd = 075.PX5D8.007C

+3D3V_VDD_DCIN

75.00054.A7D
2nd = 75.00024.17D

20V>+DC_IN>4.7V

74.02204.03F
2nd = 074.02920.003F

Vout=1.24*(1+(R1/R2))

CPU_Core

Vcore_OVP

74.00331.H2F

83.00355.G1F

084.21319.0031

75.27002.F7C

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Taipei Hsien 221, Taiwan, R.O.C.

Power (Charger_ISL9538)

MOCKINGBIRD_TGL

A00

Saturday, August 04, 2007

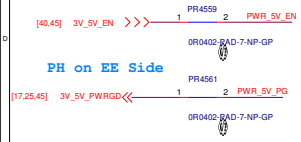
Sheet 44 of 56

TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLIm1L Reg(A)
0			1	733kHz	No	0.476
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.476
61.9				1MHz	No	0.476
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.476
105			3	733kHz	No	0.476
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476

SSID = PWR.Plane.Regulator_5V

OFFPAGE-Signal



OFFPAGE-GAP

SY8288C For 5V

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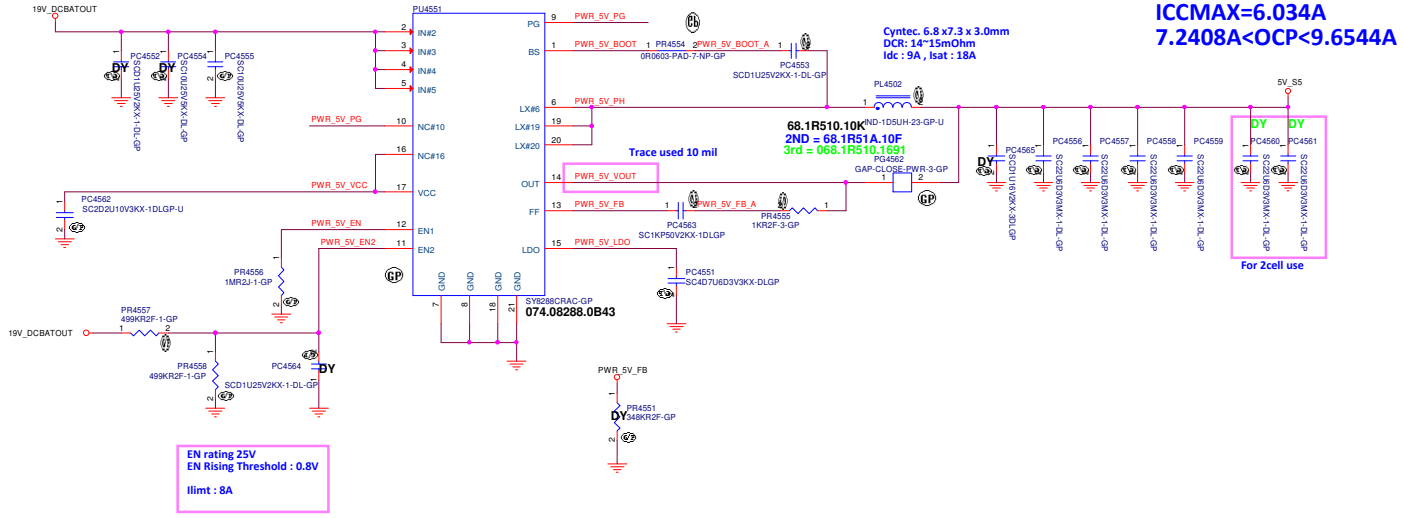
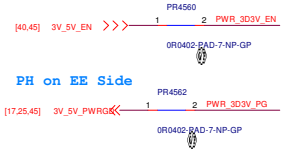


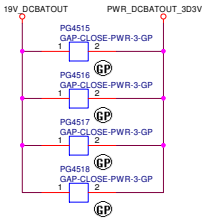
TDC=8.62A
ICCMAX=6.034A
7.2408A<OCP<9.6544A

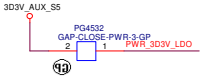
SSID = PWR.Plane.Regulator_3D3V

OFFPAGE-Signal

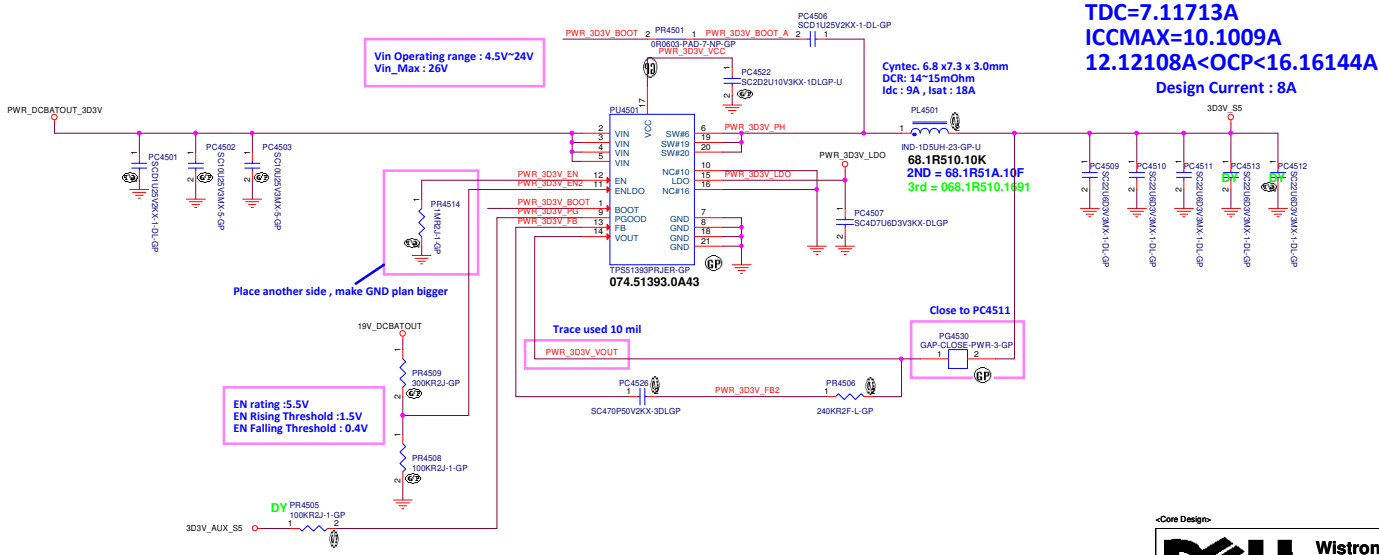


OFFPAGE-GAP





TPS51393 For 3D3V



TDC=7.11713A
ICCMAX=10.1009A
12.12108A<OCP<16.16144A
Design Current : 8A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER (SY8288_5V/3D3V)	
Size: A2	Document Number: MOCKINGBIRD_TGL	Rev: A00
Date: Saturday, August 01, 2020	Sheet 45 of 105	

Main Func = CPU_CORE

OFFPAGE

SVID

20200511(DVT2)
Remove PR4632-PR4634 to Keep away PWR_VCORE_SDIO_R to PWR_VGA_NVVDDS_LGATE1 40mil

[7] SVID_CLK_CPU
[7] SVID_DATA_CPU
[7] SVID_ALERT#_CPU

[3,22,24,44,72] PROCHOT#_CPU
[44] CHGR_PSYS_IMVP

20191119
check with Nakia need change netname to PWR_VCORE_VR_READY or not

[17,44] PWR_IMVP_PWRGD — PR4636 0R0402-PAD-7-NP-GP — PWR_VCORE_VR_READY

[17,24,40,44] ALL_SYS_PWRGD

VCORE SENSE

[7] VSSCORE_SENSE
[7] VCCCORE_SENSE

[47] PWR_VCORE_UGATE1
[47] PWR_VCORE_PHASE1
[47] PWR_VCORE_LGATE1

[47] PWR_VCORE_UGATE2
[47] PWR_VCORE_PHASE2
[47] PWR_VCORE_LGATE2

[47] PWR_VCORE_ISEN2
[47] PWR_VCORE_ISEN1
[47] PWR_VCORE_ISUMP
[47] PWR_VCORE_ISUMN

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1D05V_VCCST
1D05V_VCCSTG_TERM
3D3V_S0
5V_S5
19V_DCBATOUT
O5V_S5
O1V_CPU_CORE

Close to VR_IC
PC4626 SC1U10V2KX-1DLGP
PC4601 SCD1U25V2KX-1-DL-GP

PR4603 1KR2F-3-GP
PR4607 100R2F-L1-GP-U
PR4609 10KR2J-3-GP
PR4617 0R0402-PAD-7-NP-GP
PR4601 0R0402-PAD-7-NP-GP
PC4601 SCD22U25V2KX-4-GP
PC4613 SC1U10V2KX-1DLGP

PROCHOT#_CPU
SVID_CLK_CPU
SVID_ALERT#_CPU
SVID_DATA_CPU
PWR_VCORE_VR_READY
ALL_SYS_PWRGD

PC4612 SC4700P50V2KX-1DLGP
PR4602 12K1R2F-L1-GP
PC4609 SC330P25V1KX-GP
PR4608 90K9R2F-GP
20200221 (DVT1) changes to 90.9K
20200302(DVT1) Change PC4609 to 0201
20200313(DVT1) Change to 25V

PU4601
ISL95869HRTZ-T-GP
074.95869.0073

CHGR_PSYS_IMVP
PWR_VCORE_IMON
PWR_VCORE_NTC
PWR_VCORE_COMP
PWR_VCORE_FB
PWR_VCORE_RTN
PWR_VCORE_ISUMN1

PROG1
VBOOT:0V
F=750kHz

PR4619 78K7R2F-GP
PR4620 9K31R2F-GP
PR4621 0R0603-PAD-7-NP-GP
PC4610 SCD22U25V2KX-4-GP
PR4625 0R0402-PAD-7-NP-GP
PC4605 SC1U10V2KX-1DLGP
PR4611 0R0603-PAD-7-NP-GP
PC4611 SCD22U25V2KX-4-GP
PR4668 0R1J-GP

PR4616 10KR2F-2-GP
PWR_VCORE_NTC_N
B=4500
PR4655 27K4R2F-GP
PR4618 100K0R2F-1-GP
69.60012.0001

20200221 (DVT1) changes to 2K
20200227 (DVT1) change back to1.3K
20200522 (DVT2) changes to 1.5K

PR4615 1K5R2F-2-GP
PC4608 SC82P50V2KN-3-DL-GP
PR4614 2KR2F-3-GP
PR4613 2K49R2F-GP
PR4612 392R2F-GP
PC4607 SC1U10V2KX-1DLGP
PC4606 SC330P50V2KX-3-DL-GP
PC4604 SC820P50V2KX-1-DL-GP
PR4665 0R0402-PAD-7-NP-GP
PR4667 0R0402-PAD-7-NP-GP
PR4640 100R2F-L1-GP-U
PC4615 SCD01U25V2KX-3DLGP
PC4605 SC330P50V2KX-3-DL-GP
PC4638 SC330P50V2KX-3-DL-GP
PR4626 100R2F-L1-GP-U

PWR_VCORE_ISEN2
PWR_VCORE_ISEN1
PWR_VCORE_ISUMP
PWR_VCORE_ISUMN

PC4623 SC2200P50V2KX-2DLGP
PR4628 3K48R2F-GP
PR4627 511R2F-2-GP
PR4666 0R0402-PAD-7-NP-GP
PC4614 SCD22U16V2KX-3DLGP
PC4618 SCD22U16V2KX-3DLGP
PR4629 0R0402-PAD-7-NP-GP
PC4616 SCD22U16V2KX-3DLGP
PC4602 SCD1U16V2KX-3DLGP
PR4630 11KR2F-L-GP
PR4653 2K61R2F-1-GP
PR4650 NTC-10K-29-GP-U 69.60011.201 B=3370
PC4603 SCD01U25V2KX-3DLGP 20200212 Change to 0.1u 25V

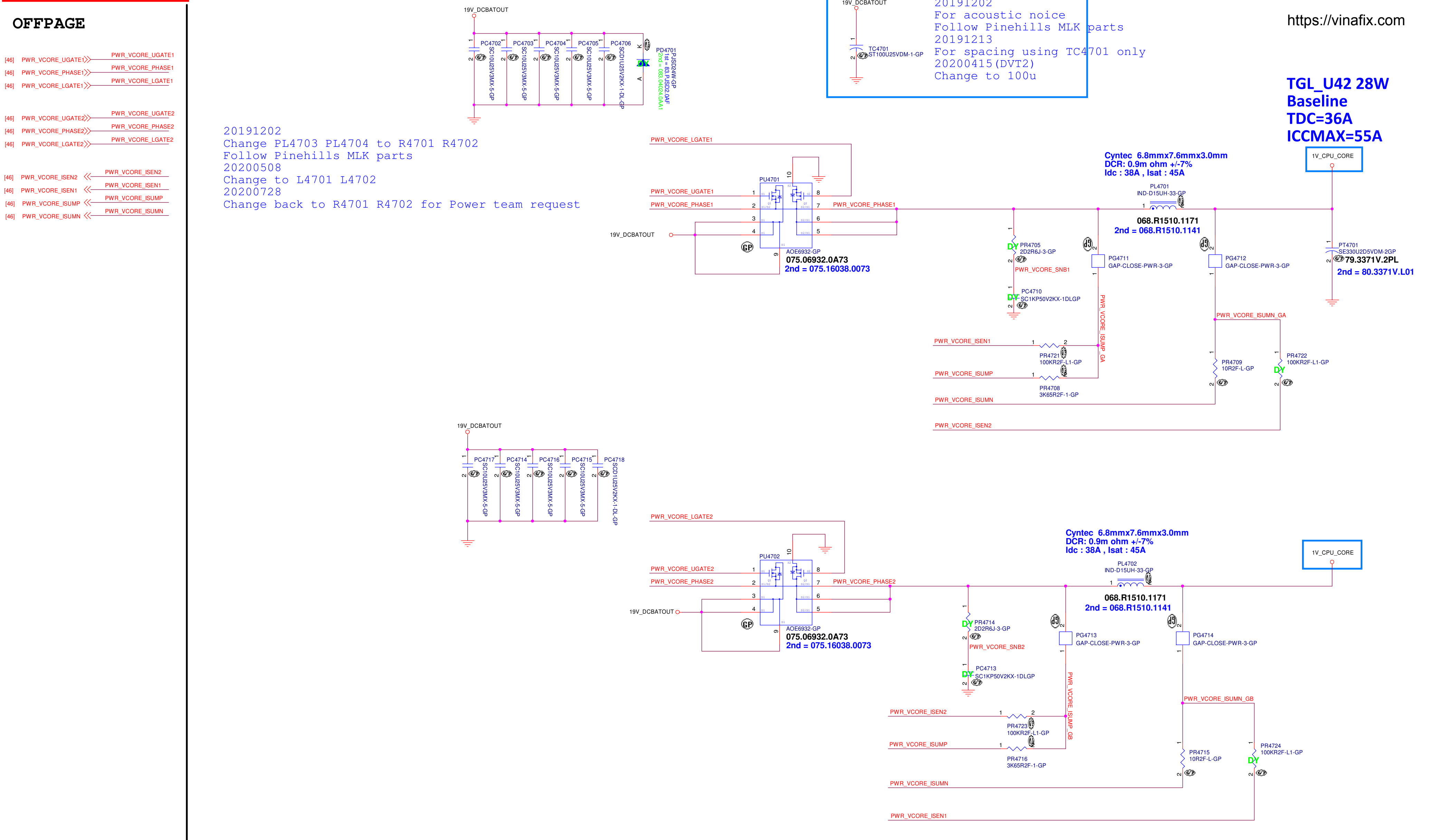
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (95869_CPUCORE(1/3))
Size: A2 | Document Number: MOCKINGBIRD_TGL | Rev: A00
Date: Saturday, August 01, 2020 | Sheet 46 of 105

Main Func = VCCIN

OFFPAGE



[46] PWR_VCORE_UGATE1 PWR_VCORE_UGATE1
[46] PWR_VCORE_PHASE1 PWR_VCORE_PHASE1
[46] PWR_VCORE_LGATE1 PWR_VCORE_LGATE1
[46] PWR_VCORE_UGATE2 PWR_VCORE_UGATE2
[46] PWR_VCORE_PHASE2 PWR_VCORE_PHASE2
[46] PWR_VCORE_LGATE2 PWR_VCORE_LGATE2
[46] PWR_VCORE_ISEN2 PWR_VCORE_ISEN2
[46] PWR_VCORE_ISEN1 PWR_VCORE_ISEN1
[46] PWR_VCORE_ISUMP PWR_VCORE_ISUMP
[46] PWR_VCORE_ISUMN PWR_VCORE_ISUMN
19V_DCBATOUT
PC4702 SC10U25V3MX-5-GP
PC4703 SC10U25V3MX-5-GP
PC4704 SC10U25V3MX-5-GP
PC4705 SC10U25V3MX-5-GP
PC4706 SCD1U25V2KX-1-DL-GP
PD4701 PJSD24W-GP
TC4701 ST100U25VDM-1-GP
PU4701
AOE6932-GP
075.06932.0A73
2nd = 075.16038.0073
Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A
PL4701 IND-D15UH-33-GP
068.R1510.1171
2nd = 068.R1510.1141
1V_CPU_CORE
PR4705 2D2R6J-3-GP
PWR_VCORE_SNB1
PC4710 SC1KP50V2KX-1DLGP
PG4711 GAP-CLOSE-PWR-3-GP
PG4712 GAP-CLOSE-PWR-3-GP
PT4701 SE330U2D5VDM-2GP
79.3371V.2PL
2nd = 80.3371V.L01
PWR_VCORE_ISUMP_GA
PWR_VCORE_ISUMN_GA
PR4721 100KR2F-L1-GP
PR4708 3K65R2F-1-GP
PR4709 10R2F-L-GP
PR4722 100KR2F-L1-GP
PC4717 SC10U25V3MX-5-GP
PC4714 SC10U25V3MX-5-GP
PC4716 SC10U25V3MX-5-GP
PC4715 SC10U25V3MX-5-GP
PC4718 SCD1U25V2KX-1-DL-GP
PU4702
AOE6932-GP
075.06932.0A73
2nd = 075.16038.0073
Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A
PL4702 IND-D15UH-33-GP
068.R1510.1171
2nd = 068.R1510.1141
1V_CPU_CORE
PR4714 2D2R6J-3-GP
PWR_VCORE_SNB2
PC4713 SC1KP50V2KX-1DLGP
PG4713 GAP-CLOSE-PWR-3-GP
PG4714 GAP-CLOSE-PWR-3-GP
PWR_VCORE_ISUMP_GB
PWR_VCORE_ISUMN_GB
PR4723 100KR2F-L1-GP
PR4716 3K65R2F-1-GP
PR4715 10R2F-L-GP
PR4724 100KR2F-L1-GP

20191202
For acoustic noice
Follow Pinehills MLK parts
20191213
For spacing using TC4701 only
20200415(DVT2)
Change to 100u

20191202
Change PL4703 PL4704 to R4701 R4702
Follow Pinehills MLK parts
20200508
Change to L4701 L4702
20200728
Change back to R4701 R4702 for Power team request

https://vinafix.com

TGL_U42 28W
Baseline
TDC=36A
ICCMAX=55A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER (95829_CPUCORE(2/3))**

Size: A2 | Document Number: **MOCKINGBIRD_TGL** | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 47 of 105

Main Func = CPU_CORE

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Size A3	Document Number	Rev A00
Date: Saturday, August 01, 2020	Sheet 48 of 105	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(RSVD)***

Size	Document Number	Rev
A	***MOCKINGBIRD_TGL***	***A00***

Date:	Sheet	of
Saturday, August 01, 2020	49	105

Main Func = VCCIN_AUX

OFFPAGE

VID

[22,40] CORE_VID0 — PR5014 0R0402-PAD-7-NP-GP — PWR_VCCIN_AUX_VID0

[22,40] CORE_VID1 — PR5015 0R0402-PAD-7-NP-GP — PWR_VCCIN_AUX_VID1

[40,53] PWR_1D8V_PG — PR5012 0R0402-PAD-7-NP-GP — PWR_VCCIN_AUX_EN_R

[40] VCCIN_AUX_PWRGD — PR5013 0R0402-PAD-7-NP-GP — PWR_VCCIN_AUX_PG

VCCIN_AUX SENSE

[22] VCCAUX_SENSE — PR5017 0R0402-PAD-7-NP-GP — PWR_VCCIN_AUX_FB_O

[22] VSSAUX_SENSE — PR5018 0R0402-PAD-7-NP-GP — PWR_VCCIN_AUX_RGND

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19V_DCBATOUT

PC5006 SC100U25V3MX-5GP

PC5007 SC100U25V3MX-5GP

PC5012 SC100U25V2MX-5GP

PC5013 SC100U25V2MX-5GP

PD5001 RLS524W-GP 30V 0.4A 2nd = 083.00024.0A01

PC5009 SC1U10V2KX-1DLGP

PWR_VCCIN_AUX_BOOT

PU5001 RT6543AGQW-GP 074.06543.0073

Pin	Net
10	BOOT
20	VSYS = 19V_DCBATOUT
11	UG = PWR_VCCIN_AUX_UG
12	PH = PWR_VCCIN_AUX_LX
13	LG = PWR_VCCIN_AUX_LG
14	PGND
2	ISENSEP = PWR_VCCIN_AUX_ISENP
3	ISENSEN = PWR_VCCIN_AUX_ISENN
8	VOUT = 1D8V_CPU_AUX
5	COMP = PWR_VCCIN_AUX_COMP
6	FB = PWR_VCCIN_AUX_FB
7	RGND = PWR_VCCIN_AUX_RGND
21	AGND
1	CS_DIS = PWR_VCCIN_AUX_CS
15	PVCC = PWR_VCCIN_AUX_VCC
16	VCC
4	PG = PWR_VCCIN_AUX_PG
19	EN = PWR_VCCIN_AUX_EN
17	VID1 = PWR_VCCIN_AUX_VID1
18	VID0 = PWR_VCCIN_AUX_VID0
9	FSWSEL = PWR_VCCIN_AUX_FSW

3D3V_S5

5V_S5

PR5002 124KR2F-GP

PR5001 2D2R2J-GP

PR5004 10KR2J-3-GP

PC5008 SC1U10V2KX-1DLGP

PR5005 2D2R2J-GP

PC5010 SC1U10V2KX-1DLGP

PR5003 DY 10KR2J-3-GP

PWR_VCCIN_AUX_EN_R

19V_DCBATOUT

PU5002 PU5003 FDMS3600-02-RJK0215-COLAY-GP 075.07321.0073 2nd = 075.34304.0073

FDMS3600-02-RJK0215-COLAY-GP 075.07321.0073

TGL_U42 28W
Baseline
TDC=14A
ICCMAX=27A
32.4A<OCP<43.2A

Cyntec. 6.8 x 7.3 x 3mm
DCR: 2.5~2.8 mOhm
Idc : 23A , Isat : 40A

PL5001 IND-D22UH-37-GP 68.R2210.10V 2nd = 068.R2210.1521

PR5021 17K8R2F-GP

PC5011 SCD1U25V2KX-1-DL-GP

PR5008 332R2F-1-GP

PR5022 634R2F-1-GP

PWR_VCCIN_AUX_RC

PR5023 NTC-10K-29-GP-U B=3370K

PR5016 0R0402-PAD-7-NP-GP

PR5007 100R2F-L1-GP-U

1D8V_CPU_AUX

PT5001 SE330U2D5VDM-2GP 79.3371V.2PL 2nd = 80.3371V.L01

PWR_VCCIN_AUX_FB_O

PC5003 SC2200P50V2KX-2DLGP

PWR_VCCIN_AUX_COMP_R

PR5011 10KR2F-2-GP

PC5002 SC470P50V2KX-3DLGP DY

PWR_VCCIN_AUX_FB_R

PR5009 1K6R2F-GP DY

PC5004 SC22P50V2JN-4DLGP

PR5010 5K62R2F-GP

PR5006 100R2F-L1-GP-U

PR5020 0R0402-PAD-7-NP-GP

<Core Design>

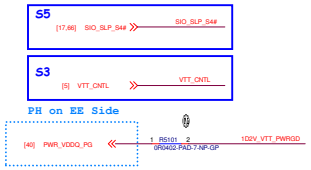
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT6543A_VCCIN_AUX

Size: A2 | Document Number | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 50 of 105

OFFPAGE



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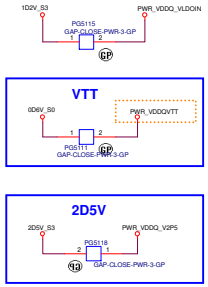


https://vinafix.com

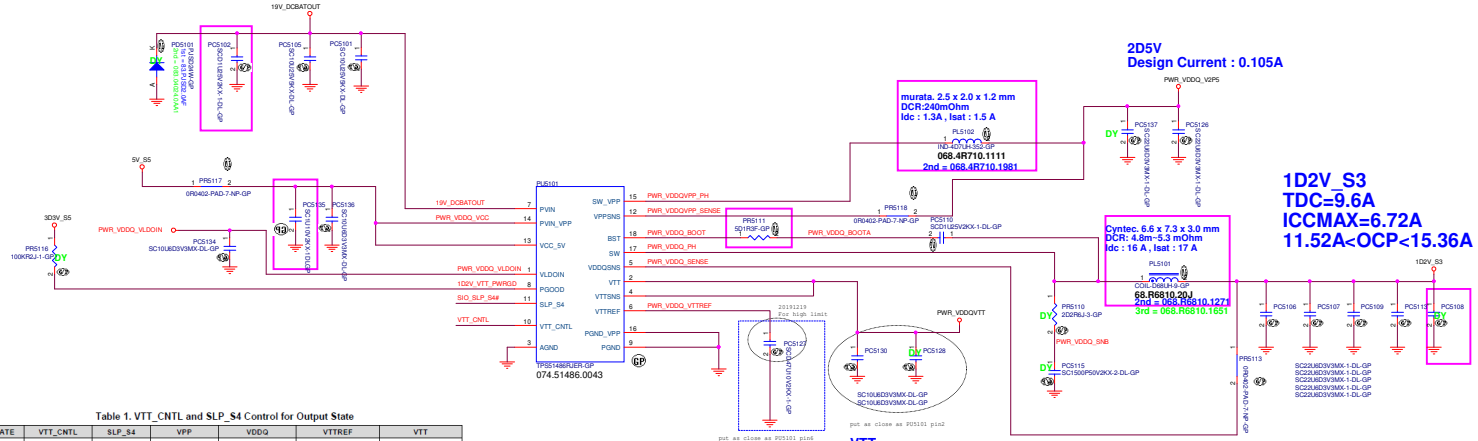


Table 1. VTT_CNTL and SLP_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 051_POWER (TPS51486R_VDDQ/VTT)

Size: Custom | Document Number: MOCKINGBIRD_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 51 of 105

SSID = PWR.Plane.Regulator_1D0V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

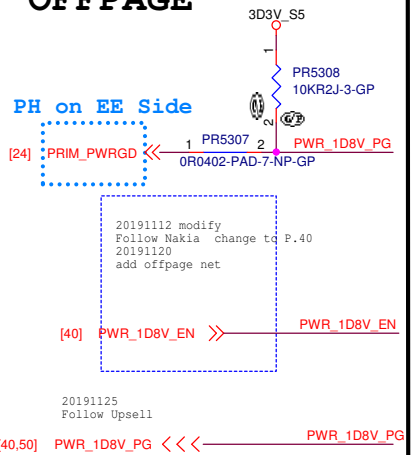
Title: POWER (AOZ2262Q_1D0V)

Size	Document Number	Rev
A3	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 52 of 105

Main Func = 1D8V/1D2V

OFFPAGE



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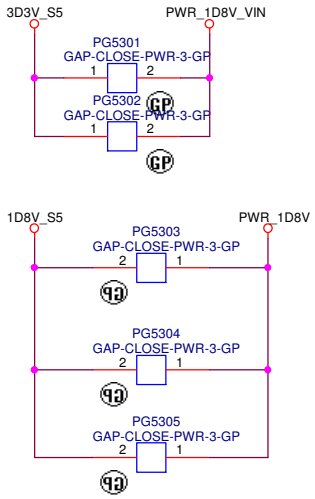
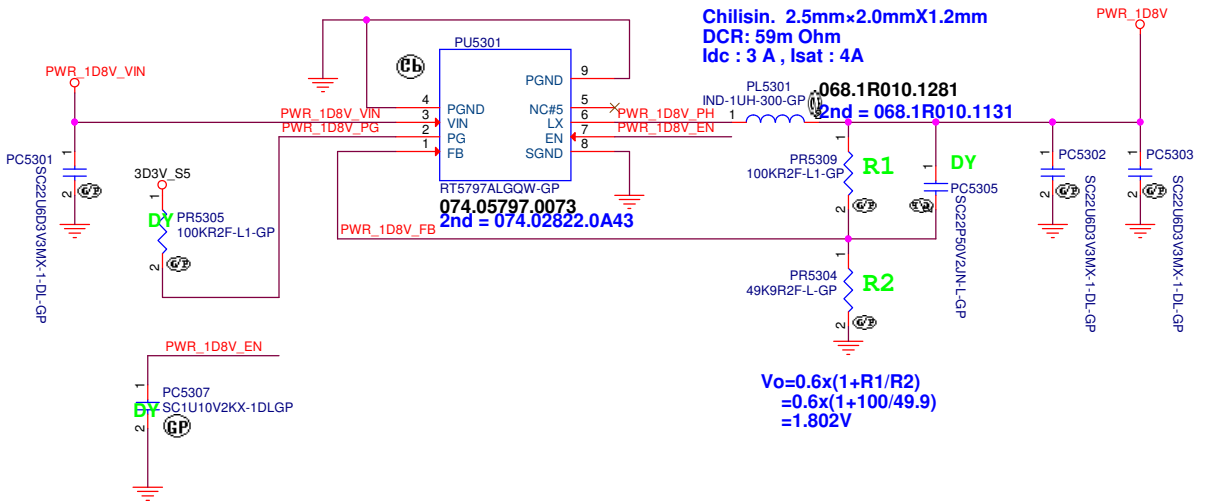


TDC=1.029A
IOCMAX=1.47A
1.764A<OCP<2.352A



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD&CAM&DMC&Touch	
Size: B	Document Number: MOCKINGBIRD_TGL	Rev: A00
Date: Saturday, August 01, 2020	Sheet 53 of 105	

Main Func = 1D05V

OFFPAGE

PH on EE Side

20191119
Check with UPSELL and Nakia follow which one

VCCIN_AUX_PWRGD
[40] PWR_VNN_EN >> PWR_VNN_EN

1D05V_BP_PWRGD
[24,40] PWR_VNN1D05V_PG >> PWR_VNN1D05V_PG

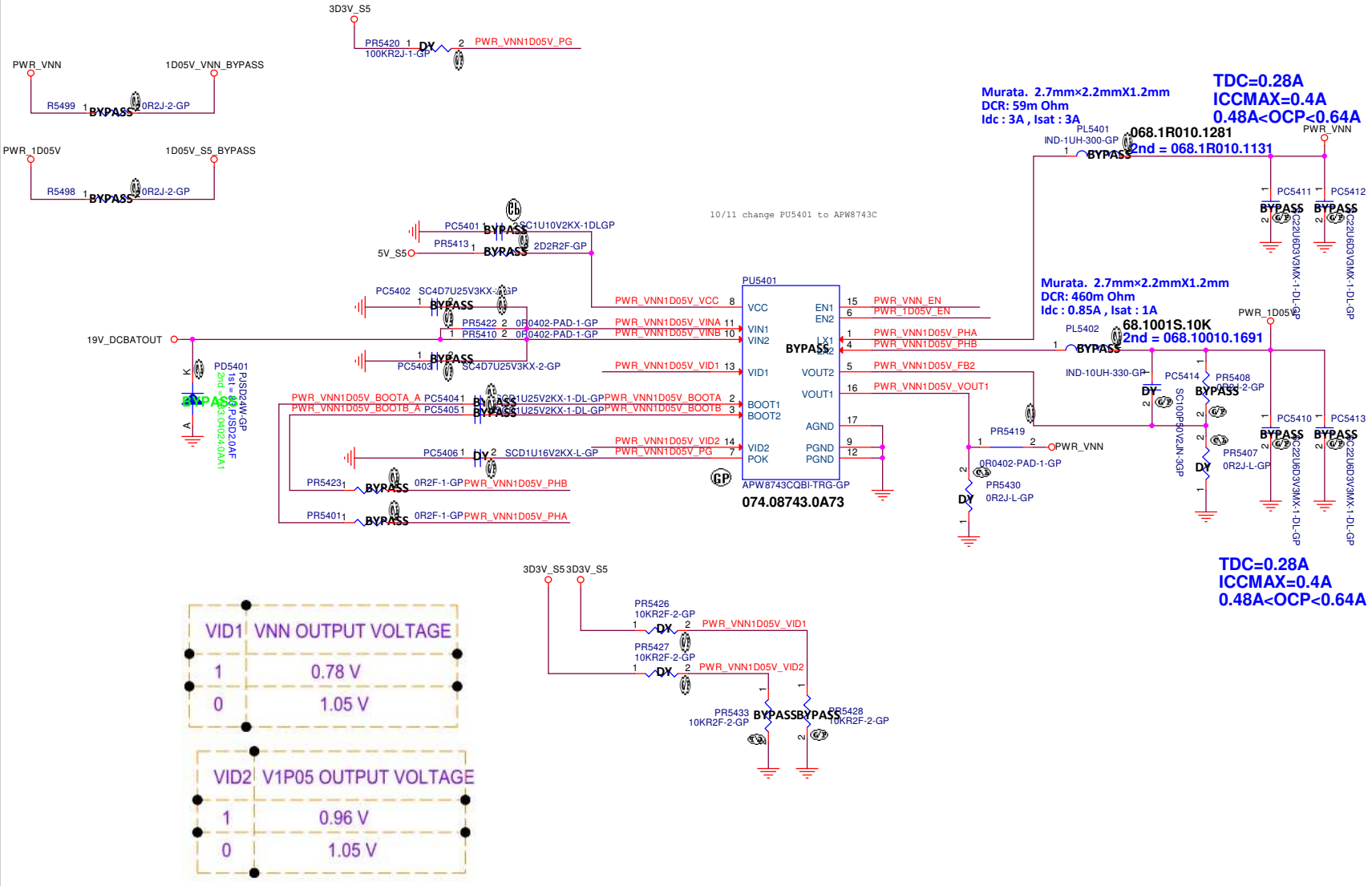
[40] PWR_1D05V_EN >> PWR_1D05V_EN

PH on EE Side

1D05V_BYPASS_CTRL
[40] PWR_VNN1D05V_VID2 >> PWR_VNN1D05V_VID2

PM_SLP_S3#
[40] PWR_VNN1D05V_VID1 >> PWR_VNN1D05V_VID1

OFFPAGE-GAP



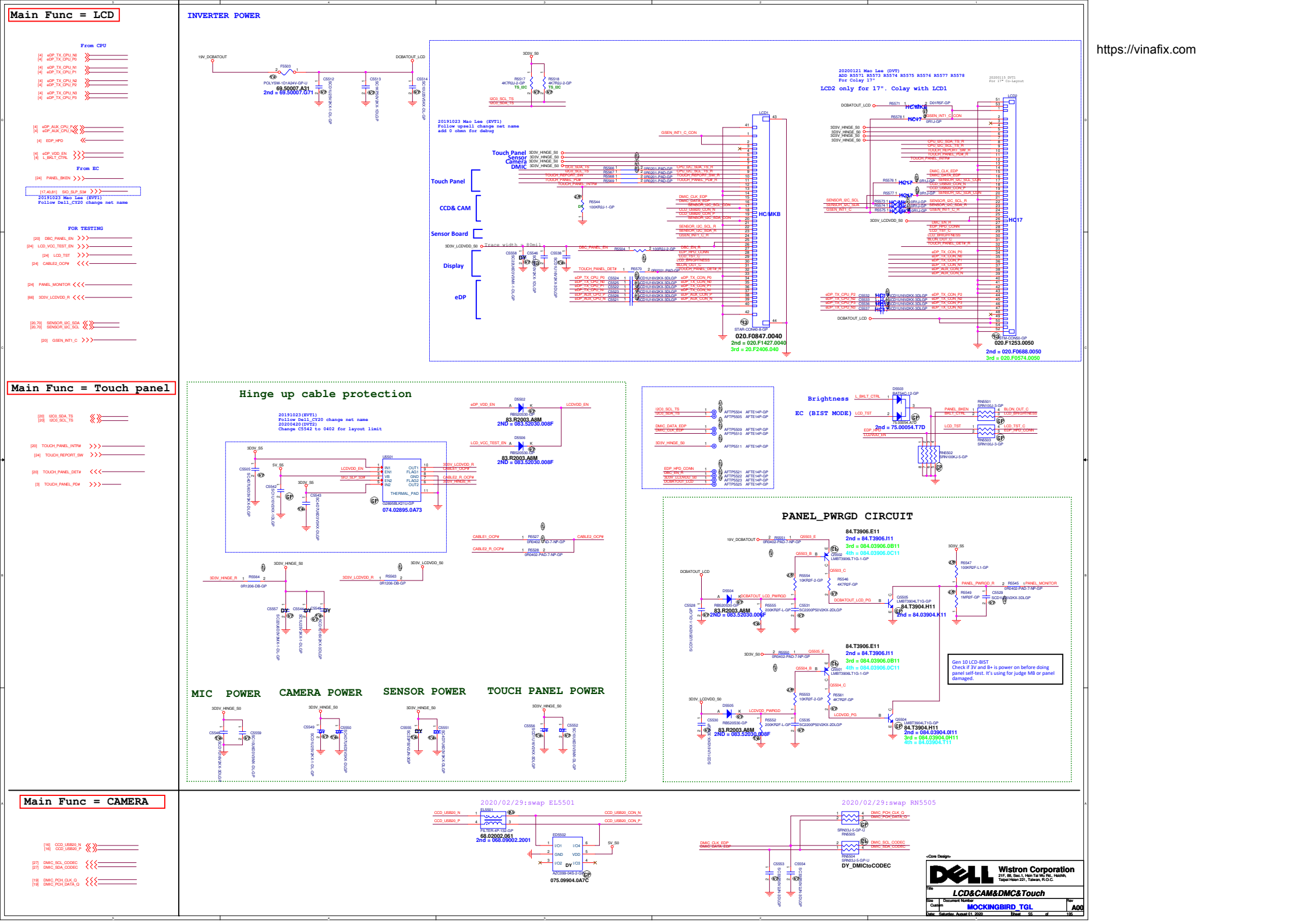
VID1	VNN OUTPUT VOLTAGE
1	0.78 V
0	1.05 V

VID2	V1P05 OUTPUT VOLTAGE
1	0.96 V
0	1.05 V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER(APW8738A_VNN1D05)
Size: A3
Document Number: MOCKINGBIRD_TGL
Rev: A00
Date: Saturday, August 01, 2020
Sheet 54 of 105



https://vinafix.com

Main Func = CRT

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CRT(Reserved)*

Size	Document Number	Rev
A3	*MOCKINGBIRD_TGL*	*A00*

Date: Saturday, August 01, 2020 Sheet 56 of 105

SSID = HDMI Level Shifter/Connector

[4] HDMI_DDI_TX_N0
[4] HDMI_DDI_TX_P0
[4] HDMI_DDI_TX_N1
[4] HDMI_DDI_TX_P1
[4] HDMI_DDI_TX_N2
[4] HDMI_DDI_TX_P2
[4] HDMI_DDI_TX_N3
[4] HDMI_DDI_TX_P3

[4] CPU_DPB_CTRL_CLK
[4] CPU_DPB_CTRL_DATA
[4] CPU_DISP_HPDB

HDMI_DDI_TX_N3 C5701 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_N3
HDMI_DDI_TX_P3 C5704 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_N0 C5705 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_N0
HDMI_DDI_TX_P0 C5703 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_N1 C5707 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_N1
HDMI_DDI_TX_P1 C5706 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_N2 C5708 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_N2
HDMI_DDI_TX_P2 C5709 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_P2

5V_S0
R57051 470R2F-GP
R57591 470R2F-GP
R57731 470R2F-GP
R57741 470R2F-GP
R57751 470R2F-GP
R57761 470R2F-GP
R57771 470R2F-GP
R57781 470R2F-GP
Q5701 PJE8408-R1-00001-GP
084.08408.0031
2nd = 084.00138.0E31
HDMI_PLL_GND

5V_S0
D5701 RB520S30-GP
83.R2003.A8M
2ND = 083.52030.008F
D5702 RB520S30-GP
83.R2003.A8M
2ND = 083.52030.008F
HDMI_SCL_R
HDMI_SDA_R
RN5702 SRN2K2J-1-GP
3D3V_S0
Part Reference = Q5702
CPU_DPB_CTRL_CLK
HDMI_SCL_CON
2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C
CPU_DPB_CTRL_DATA
HDMI_SDA_CON

HDMI_DDI_TX_CON_N0
20200420(DVT2)
Change to 180R
ER5701 180R2J-1-GP
HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CON_N1
ER5702 180R2J-1-GP
HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N2
ER5703 180R2J-1-GP
HDMI_DDI_TX_CON_P2
HDMI_DDI_TX_CON_N3
ER5704 180R2J-1-GP
HDMI_DDI_TX_CON_P3

5V_S0
F5701 POLYSW-1D1A6V-9-GP-U
69.48001.081
5V_HDMI
2ND = 69.50011.081

20191122
Follow Nakia
20191127
For High limit
change back to follow ICL

HDMI CONN

5V_HDMI
20191218
For EMC required
EC5711 SCD1U16V2KX-3DLGP
C5720 SCD1U16V2KX-3DLGP
HDMI1
HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CON_N0
HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N1
HDMI_DDI_TX_CON_P2
HDMI_DDI_TX_CON_N2
HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_CON_N3
+5V_POWER
TMDS_DATA0+
TMDS_DATA0-
TMDS_DATA1+
TMDS_DATA1-
TMDS_DATA2+
TMDS_DATA2-
TMDS_DATA0_SHIELD
TMDS_DATA1_SHIELD
TMDS_DATA2_SHIELD
TMDS_CLOCK_SHIELD
TMDS_CLOCK+
TMDS_CLOCK-
SCL
SDA
HDMI_SCL_CON
HDMI_SDA_CON
CEC
DDC/CEC_GROUND
HOT_PLUG_DETECT
RESERVED#14
GND
HDMI (A_Type)
SKT-HDMI23-235-GP
022.10025.0651
2nd = 022.10025.0701
3rd = 022.10025.0711

3D3V_S0
Q5703 LMBT3904LT1G-GP
HDMI_HPD_B R57101 150KR2F-L-GP HDMI_DET_CON
84.T3904.H11
2nd = 084.03904.0I11
3rd = 084.03904.0H11
4th = 084.03904.T11
CPU_DISP_HPDB R5712 HDMI_HPD_E
0R0402-PAD-7-NP-GP
R5709
R5711 200KR2F-L-GP

EMI Request :

HDMI_DDI_TX_CON_P0 ED5704 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF
HDMI_DDI_TX_CON_N0 ED5705 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF 2nd = 083.58017.00AF
HDMI_DDI_TX_CON_P1 ED5706 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF
HDMI_DDI_TX_CON_N1 ED5707 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF 2nd = 083.58017.00AF
HDMI_DDI_TX_CON_P2 ED5708 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF
HDMI_DDI_TX_CON_N2 ED5709 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF 2nd = 083.58017.00AF
HDMI_DDI_TX_CON_P3 ED5710 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF
HDMI_DET_CON ED5711 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF 2nd = 083.58017.00AF
HDMI_SCL_CON ED5712 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF
HDMI_SDA_CON ED5713 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF 2nd = 083.58017.00AF
ED5714 PESD5V0H1BSFYL-GP-U

2nd = 083.58017.00AF
2nd = 083.58017.00AF
2nd = 083.58017.00AF
2nd = 083.58017.00AF
2nd = 083.58017.00AF
2nd = 083.58017.00AF

<Core Design>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI
Size: Custom
Document Number: MOCKINGBIRD_TGL
Rev: A00
Date: Saturday, August 01, 2020
Sheet 57 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A4	*MOCKINGBIRD_TGL*	*A00*

Date: Saturday, August 01, 2020 Sheet 58 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A4	*MOCKINGBIRD_TGL*	*A00*

Date: Saturday, August 01, 2020 Sheet 59 of 105

Main Func = HDD

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

SATA IF_HDD/ODD

Size	Document Number	Rev
A4	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 60 of 105

Main Func = WLAN

PCIE

[16] WLAN_PCIE_TX_N
[16] WLAN_PCIE_TX_P
[16] WLAN_PCIE_RX_N
[16] WLAN_PCIE_RX_P

PCIE_CLK

[18] WLAN_CLK_CPU_N
[18] WLAN_CLK_CPU_P
[18] CLK_PCIE_WLAN_REQ#

USB2.0

[16] BT_USB20_P
[16] BT_USB20_N

Single end

[19] BT_RADIO_DIS#
[16] WLAN_RF_DIS#
[17,63,66,71,76,91] PCH_PLTRST#
[18,24] SUSCLK

Debug

Power EN (Madesimo)

[21] CNV_BRI_DT_R
[21] CNV_RGI_DT_R
[21] CLKREQ_CNV
[21] CNV_RF_RESET#
[21] CNV_WT_DN0
[21] CNV_WT_DP0
[21] CNV_WT_DN1
[21] CNV_WT_DP1
[21] CNV_WT_CLKN
[21] CNV_WT_CLKP
[21] CNV_WR_DN0
[21] CNV_WR_DP0
[21] CNV_WR_DN1
[21] CNV_WR_DP1
[21] CNV_WR_CLKN
[21] CNV_WR_CLKP
[21] CNV_BRI_RSP
[21] CNV_RGI_RSP
[24] JIO3_PCIE_WAKE#

3D3V_S5
3D3V_WLAN
R6140 2 0R0805-PAD-NP-GP
1.1A
C6110 SCD1U16V2KX-3DLGP
C6106 SC10U6D3V3MX-DL-GP
C6109 SCD1U16V2KX-3DLGP

AFTE14P-GP AFTP6104 1 3D3V_WLAN
AFTE14P-GP AFTP6105 1 CLK_PCIE_WLAN_REQ#
AFTE14P-GP AFTP6106 1 WIFI_RF_EN_R
AFTE14P-GP AFTP6107 1 BLUETOOTH_EN_R
AFTE14P-GP AFTP6108 1 PCH_PLTRST#
AFTE14P-GP AFTP6109 1 BT_USB20_CON_N
AFTE14P-GP AFTP6110 1 BT_USB20_CON_P
AFTE14P-GP AFTP6111 1 JIO3_PCIE_WAKE#

3D3V_WLAN
R6145 10KR2J-3-GP
WLAN_RF_DIS# R6144 0R0402-PAD-7-NP-GP WIFI_RF_EN_R
3D3V_WLAN
R6146 10KR2J-3-GP
BT_RADIO_DIS# R6143 0R0402-PAD-7-NP-GP BLUETOOTH_EN_R

3D3V_WLAN
R6106 DY 10KR2J-3-GP CLKIN_XTAL_LCP_R
WIFI_RF_EN_R
BLUETOOTH_EN_R
PCH_PLTRST#
SUSCLK R6135 33R2J-2-GP SUSCLK_WLAN
CNV_RGI_RSP R6109 49D9R2F-GP CNV_BRI_DT_R CNV_RGI_RSP_R CNV_RGI_DT_R
CNV_BRI_RSP R6118 49D9R2F-GP CNV_BRI_RSP_R
CLKREQ_CNV R6141 33R2J-2-GP BT_PCMOUT_CLKREQ0_R
CNV_RF_RESET# R6142 33R2J-2-GP BT_PCMFRM_CRF_RST_N
3D3V_WLAN
R6134 75KR2F-GP
R6133 DY 71K5R2F-1-GP

WLAN1

76	76	77	77
74	3_3VAUX	GND	75
72	3_3VAUX	RESERVED#73	73 CNV_WT_CLKP
70	RESERVED#70	RESERVED#71	71 CNV_WT_CLKN
68	RESERVED#68	GND	69
66	RESERVED#66	RESERVED#67/2ND_LANE_PERN1	67 CNV_WT_DP0
64	GPIO0_NFC_RESET#/MGPIO7	RESERVED#65/2ND_LANE_PERP1	65 CNV_WT_DN0
62	NFC_I2C_IRQ/MGPIO5	GND	63
60	NFC_I2C_SM_CLK	RESERVED#61/2ND_LANE_PETN1	61 CNV_WT_DP1
58	NFC_I2C_SM_DATA	RESERVED#59/2ND_LANE_PETP1	59 CNV_WT_DN1
56	W_DISABLE#1	GND	57
54	RESERVED#54/W_DISABLE#2	PEWAKE0#	55 JIO3_PCIE_WAKE#
52	PERST0#	CLKREQ0#	53 CLK_PCIE_WLAN_REQ#
50	SUSCLK_32KHZ	GND	51
48	COEX1	REFCLKN0	49 WLAN_CLK_CPU_N
46	COEX2	REFCLKP0	47 WLAN_CLK_CPU_P
44	COEX3	GND	45
42	CLINK_CLK	PERN0	43 WLAN_PCIE_RX_N
40	CLINK_DATA	PERP0	41 WLAN_PCIE_RX_P
38	CLINK_RESET	GND	39
36	UART_CTS	PETN0	37 WLAN_PCIE_TX_CON_N
34	UART_RTS	PETP0	35 WLAN_PCIE_TX_CON_P
32	UART_TX	GND	33
22	UART_RX	SDIO_RESET	23 CNV_WR_CLKP
20	UART_WAKE	SDIO_WAKE	21 CNV_WR_CLKN
18	GND	SDIO_DAT3	19
16	LED#2	SDIO_DAT2	17 CNV_WR_DP0
14	PCM_OUT	SDIO_DAT1	15 CNV_WR_DN0
12	PCM_IN	SDIO_DAT0	13
10	PCM_SYNC	SDIO_CMD	11 CNV_WR_DP1
8	PCM_CLK	SDIO_CLK	9 CNV_WR_DN1
6	LED#1	GND	7
4	3_3VAUX	USB_D-	5 BT_USB20_CON_N
2	3_3VAUX	USB_D+	3 BT_USB20_CON_P
		GND	1
NP2	NP2	NP1	NP1

NGFF_KEY_E_75P
SKT-NGFF75P-164-GP

C6107 SCD1U16V2KX-3DLGP WLAN_PCIE_TX_N
C6108 SCD1U16V2KX-3DLGP WLAN_PCIE_TX_P

062.10003.0B11
2nd = 062.10007.0371
3rd = 062.10007.0511

2020072
Remove L6101

BT_USB20_CON_P R6111 0R0402-PAD-7-NP-GP BT_USB20_P
BT_USB20_CON_N R6110 0R0402-PAD-7-NP-GP BT_USB20_N

<Core Design>

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Title: NGFF_WLAN CONN
Size: A3
Document Number: MOCKINGBIRD_TGL
Rev: A00
Date: Saturday, August 01, 2020
Sheet 61 of 105

Main Func = WWAN

<Core Design>

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Title: WWAN

Size	Document Number	Rev
A4	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 62 of 105

Main Func = M.2 SSD

[18] SSD_CLKREQ_CPU_N
[17,61,66,71,76,91] PCH_PLTRST#

[18] SSD_CLK_CPU_P
[18] SSD_CLK_CPU_N
[16] SSD_PCIE_TX_P0
[16] SSD_PCIE_TX_N0
[16] SSD_PCIE_RX_N0
[16] SSD_PCIE_RX_P0
[16] SSD_PCIE_TX_P3
[16] SSD_PCIE_TX_N3
[16] SSD_PCIE_RX_P3
[16] SSD_PCIE_RX_N3
[16] SSD_PCIE_TX_P2
[16] SSD_PCIE_TX_N2
[16] SSD_PCIE_RX_P2
[16] SSD_PCIE_RX_N2
[16] SSD_PCIE_TX_P1
[16] SSD_PCIE_TX_N1
[16] SSD_PCIE_RX_P1
[16] SSD_PCIE_RX_N1

[64] M2_PCIE_LED#

[24] SSD_SCP#

SSD M.2 CONN

SSD1
SKT-NGFF75P-224-GP
062.10003.0F31
2nd = 062.10003.0481
3rd = 062.10003.0F21
MKB

PCIE:1 SATA:0

10/9 SSD1 PCIE from CPU, not have port to detect SATA, need remove SATA function? such as DEVSLP, PEDET?

20191028 Mao Lee (EVT1)
For PCIE only

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Table 13-12.SATA / PCI Express® Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express® Gen 2 Only	PCI Express® Gen 3 Only	SATA Only	PCI Express® Gen 2/ SATA	PCI Express® Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:
1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled OOBs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and 10 nF AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled OOBs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and 10 nF AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled OOBs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines" section for the requirements for the PCIe* and SATA signals routing.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen3 devices or PCIe* Gen2 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and 10 nF AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled OOBs / Devices.**

M.2 SSD2

[16] SSD_PCIE_TX_P9
[16] SSD_PCIE_TX_N9
[16] SSD_PCIE_RX_N9
[16] SSD_PCIE_RX_P9

[16] SSD_PCIE_TX_P10
[16] SSD_PCIE_TX_N10
[16] SSD_PCIE_RX_P10
[16] SSD_PCIE_RX_N10

[16] SSD_PCIE_TX_P11
[16] SSD_PCIE_TX_N11
[16] SSD_PCIE_RX_P11
[16] SSD_PCIE_RX_N11

[16] SSD_PCIE_TX_P12
[16] SSD_PCIE_TX_N12
[16] SSD_PCIE_RX_P12
[16] SSD_PCIE_RX_N12

[18] SSD2_CLK_CPU_P
[18] SSD2_CLK_CPU_N
[18] SSD2_CLKREQ_CPU_N

[16] M2_DEVSLP1
[16] M2_PEDET1

SSD M.2 CONN

SSD2
SKT-NGFF75P-224-GP
062.10003.0F31
2nd = 062.10003.0481
3rd = 062.10003.0F21

PCIE:1 SATA:0

<Core Design>

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Title: mSATA		
Size: A2	Document Number: MOCKINGBIRD_TGL	Rev: A00
Date: Saturday, August 01, 2020	Sheet 63 of 105	

Main Func = Power BTN

NONE FINGER PRINT 才會上件

Power button

[24] KBC_PWRBTN#

[66] KBC_PWRBTN#_R

Main Func = Battery LED

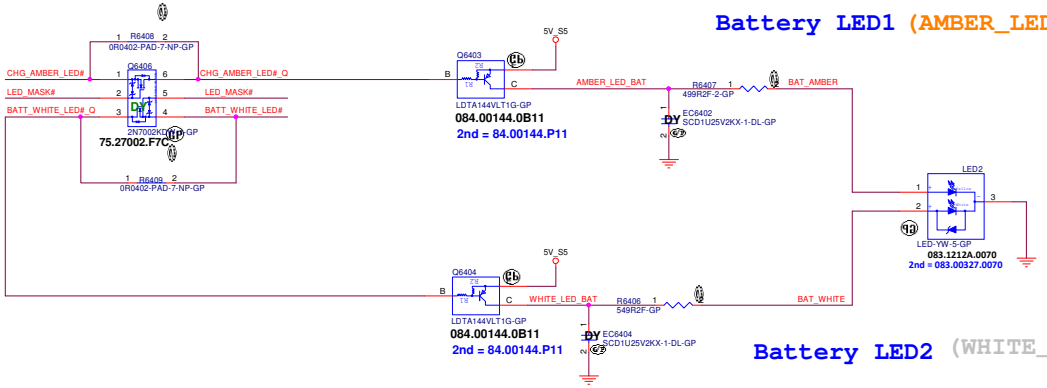
Low actived from KBC GPIO

[24] LED_MASK#

[24] CHG_AMBER_LED#

[20,24] BATT_WHITE_LED#

Battery LED1 (AMBER_LED)



Battery LED2 (WHITE_LED)

Main Func = HDD LED

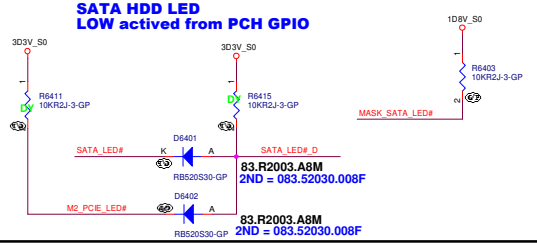
[20,24] MASK_SATA_LED#

[18] SATA_LED#

[63] M2_PCIE_LED#

[20] SATA_LED#_D

SATA HDD LED
LOW actived from PCH GPIO

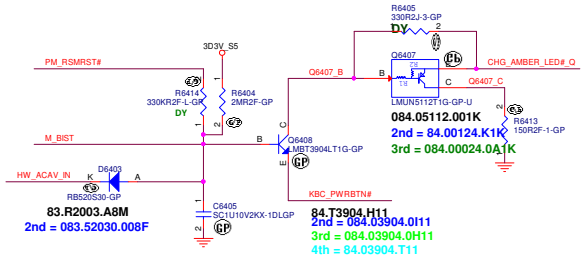


Main Func = M-BIST

[17] PM_RSMRST#

[24] M_BIST

[24,44] HW_ACAV_IN



M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by

<Core Design>

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Title: LED Board&Power Button

Size: A2 | Document Number: MOCKINGBIRD_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 64 of 105

Main Func = KB

[24] CAP_LED#_R

[4] KB_DET#

[20] KB_LED_BL_DET

[24] KB_LED_PWM

[24] KSO00
[24] KSO01
[24] KSO02
[24] KSO03
[24] KSO04
[24] KSO05
[24] KSO06
[24] KSO07
[24] KSO08
[24] KSO09
[24] KSO10
[24] KSO11
[24] KSO12
[24] KSO13
[24] KSO14
[24] KSO15
[24] KSO16

[24] KSI[0..7] — KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7

Keyboard Backlight (Reserved)

5V_S0 → F6502 POLYSW-1D1A6V-9-GP-U (69.48001.081, 2nd = 69.50011.081) → KBBL

+5V_KB_BL → KBBL

C6501 SCD1U16V2KX-3DLGP

KB_LED_BL_DET → R6503 51KR2J-1-GP → KBBL

KB_LED_PWM → R6507 100KR2J-1-GP → KBBL

KB_LED_DET_C, KB_BL_CTRL# → KBBL1 ACES-CON4-90-GP-U (020.K0298.0004, 2nd = 020.K0311.0004)

KBBL → Q6501 PJA3402-R1-00001-GP (084.03402.0031, 2nd = 084.02306.0031)

Q6501 → R6505 100KR2J-1-GP

AFTP6565

+5V_KB_BL → AFTP6506

KB_LED_DET_C → AFTP6566

KB_BL_CTRL# → AFTP6567

KB Backlight Power Consumption: 285mA max.

Internal Keyboard Connector

CAP_LED, KSO10, KSO11, KSO09, KSO14, KSO13, KSO15, KSO16, KSO12, KSO00, KSO02, KSO01, KSO03, KSO08, KSO06, KSO07, KSO04, KSO05, KSI0, KSI3, KSI1, KSI2, KSI5, KSI4, KSI7, KB_DET#

ACES-CON30-29-GP

020.K0254.0030
2nd = 020.K0274.0030
3rd = 20.K0750.030

KB_LED_DET_C → EC6501 SCD1U16V2KX-3DLGP

KB_BL_CTRL# → EC6503 SCD1U16V2KX-3DLGP

CAP LED Control

LOW actived from KBC GPIO

CAP_LED#_R → Q6502 LDTA144VLT1G-GP (084.00144.0B11, 2nd = 84.00144.P11) → R6506 1KR2J-1-GP → CAP_LED

5V_S0

Main Func = TPAD

[24] CLK_TP_SIO_I2C_DAT
[24] DAT_TP_SIO_I2C_CLK

[20,66] PCH_I2C1_SCL_TP
[20,66] PCH_I2C1_SDA_TP

[3,24] TOUCHPAD_INTR#
[24] PTP_DIS#

3D3V_S0 → R6502 0R0402-PAD-7-NP-GP → TP_VDD

Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

TP_VDD

TP side has pull high

TOUCHPAD_INTR# → R6511 10KR2J-3-GP

Support PTP

PS2

DAT_TP_SIO_I2C_CLK → R6514 20R0402-PAD-7-NP-GP
CLK_TP_SIO_I2C_DAT → R6515 20R0402-PAD-7-NP-GP

I2C

PCH_I2C1_SCL_TP → R6513 20R0402-PAD-7-NP-GP → I2C1_SCL_R
PCH_I2C1_SDA_TP → R6512 0R0402-PAD-7-NP-GP → I2C1_SDA_R

EC6504 SC33P50V2JN-3GP
EC6502 SC33P50V2JN-3GP

TP_VDD → RN6503 SRN2K2J-1-GP → I2C1_SCL_R, I2C1_SDA_R

Precision Touch Pad Connector

TP_VDD → C6505 SCD1U16V2KX-3DLGP

TP1 PTWO-CON8-16-GP (020.K0255.0008, 2nd = 020.K0151.0008)

I2C1_SDA_R, I2C1_SCL_R, TOUCHPAD_INTR#, PTP_DIS#

AFTP6531

TP_VDD → AFTP6529

I2C1_SCL_R → AFTP6528
I2C1_SDA_R → AFTP6527
TOUCHPAD_INTR# → AFTP6525
PTP_DIS# → AFTP6526

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

<Core Design>

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Title: Key Board&Touch Pad

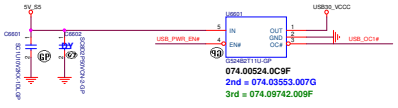
Size: A2 | Document Number: MOCKINGBIRD_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 65 of 105

Main Func = IO Connector

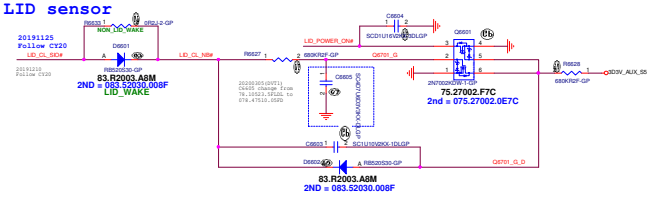
USB2.0 Power

Pin define by follow layout routing



074.00524.0C9F
2nd = 074.03553.007G
3rd = 074.09742.009F

LID sensor

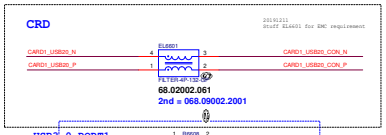


83.R2003.A8M
2ND = 083.52030.008F
LID_WAKE

75.27002.F7C
2nd = 075.27002.0E7C

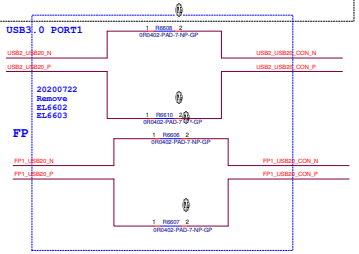
83.R2003.A8M
2ND = 083.52030.008F

CRD



68.02002.061
2nd = 068.09002.2001

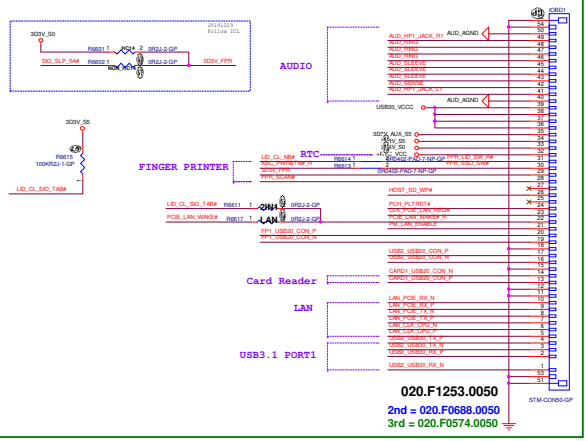
USB3.0 PORT1



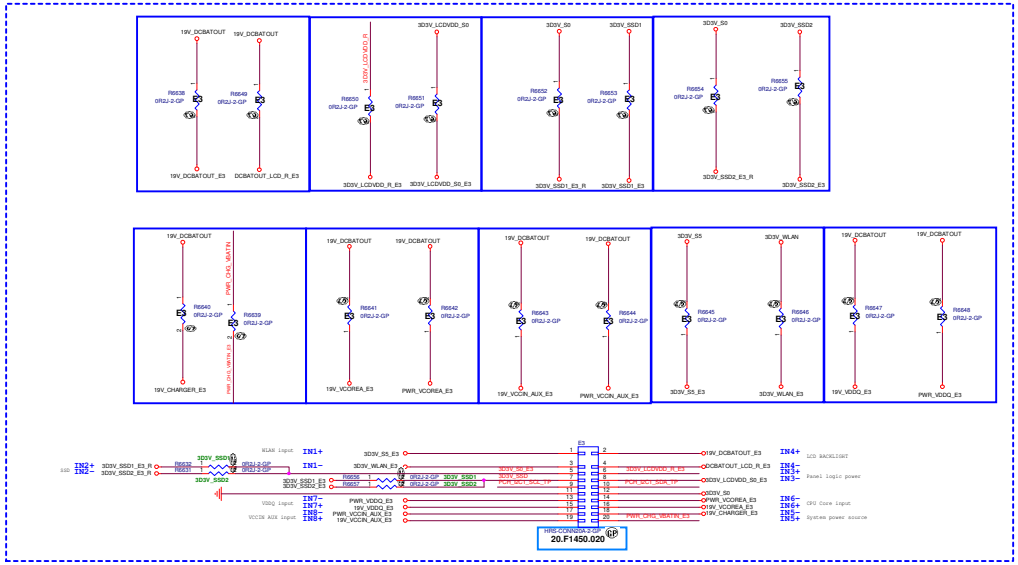
20200722
Remove
EL6602
EL6603

FP

I/O Board Connector



020.F1253.0050
2nd = 020.F0688.0050
3rd = 020.F0574.0050



20.F1450.020

AUDIO

[27,29] AUD_RING
[27,29] AUD_SLEEVE
[28] AUD_HP1_JACK_L1
[28] AUD_HP1_JACK_R1
[27] AUD_SENSE

CRD

[16] CARD1_USB20_N
[16] CARD1_USB20_P
[18] HOST_SD_WP#

USB3.0

PORT1

[16] USB2_USB30_RX_N
[16] USB2_USB30_RX_P
[16] USB2_USB30_TX_N
[16] USB2_USB30_TX_P
[16] USB2_USB20_N
[16] USB2_USB20_P

USB CONTROL

[4] USB_OC1#
[24,35] USB_PWR_EN#

LAN

[18] LAN_PCIE_RX_N
[18] LAN_PCIE_RX_P
[18] LAN_PCIE_TX_N
[18] LAN_PCIE_TX_P
[18] LAN_CLK_CPU_N
[18] LAN_CLK_CPU_P
[18] CLK_PCIE_LAN_REQ#
[24] PM_LAN_ENABLE
[24] PCIE_LAN_WAKE#

FP

[16] FP1_USB20_N
[16] FP1_USB20_P
[24] FPR_SCAN#
[64] KBC_PWRBTN#_R
[17,51] SIO_SLP_S4#

[20,24] LID_CL_SID#
[24] LID_POWER_ON#
[20,24] LID_CL_SIO_TAB#
[17,61,63,71,76,91] PCH_PLTRST#

[20,63] PCH_I2C1_SCL_TP
[20,63] PCH_I2C1_SDA_TP
[44] PWR_CH3_VBATIN
[55] 3D3V_LCDVDD_R

<Core Design>
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

File:

IO Board Connector

Size	Document Number	Rev
M	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 46 of 105

Main Func = HALL SENSOR

<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *MOCKINGBIRD_TGL* | Rev: *A00*

Date: Saturday, August 01, 2020 | Sheet 67 of 105

Main Func = Debug

ESPI

[18,24] ESPI_CLK
[18,24] ESPI_RESET#
[18,24] ESPI_CS#

[18,24] ESPI_IO0
[18,24] ESPI_IO1
[18,24] ESPI_IO2
[18,24] ESPI_IO3

UART

[24] HOST_DEBUG_TX
[20] UART_2_CTXD_DRXD
[20] UART_2_CRXD_DTXD

Follow upsell remove 3D3V_DB1

3D3V_S5
3D3V_S0
20191119
add net name

R6820 1 DY 2 0R2J-2-GP
R6821 1 DEBUG 2 0R2J-2-GP

HOST_DEBUG_TX R6801 1 DEBUG 2 0R2J-2-GP HOST_DEBUG_TX_CON
UART_2_CTXD_DRXD R6802 1 DEBUG 2 0R2J-2-GP UART_2_CTXD_DRXD_CON
UART_2_CRXD_DTXD R6803 1 DEBUG 2 0R2J-2-GP UART_2_CRXD_DTXD_CON

20191212
3D3V_S0 Follow CY20

R6804 1 DEBUG 2 51KR2J-1-GP UART_2_CTXD_DRXD
R6805 1 DEBUG 2 51KR2J-1-GP UART_2_CRXD_DTXD

ESPI Debug Connector

https://vinafix.com

DBG1
DEBUG
20.F0765.014
DM-ACES-CON14-5-GP-01
ZZ.F0765.01401

15	1		
ESPI_CLK	2	3	DEBUG
ESPI_RESET#	4	5	ESPI_CS#
ESPI_IO3	6	7	ESPI_IO2
ESPI_IO1	8	9	ESPI_IO0
3D3V_DB1	10	11	HOST_DEBUG_TX_CON
	12	13	UART_2_CTXD_DRXD_CON
UART_2_CRXD_DTXD_CON	14	16	GP

<Core Design>

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Title: ***Dubug connector***

Size	Document Number	Rev
A4	***MOCKINGBIRD_TGL***	***A00***

Date: Saturday, August 01, 2020 Sheet 68 of 105

(Blanking)

<Core Design>

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Title

Reserved

Size	Document Number	Rev
A4	*MOCKINGBIRD_TGL*	*A00*

Date: Saturday, August 01, 2020 Sheet 69 of 105

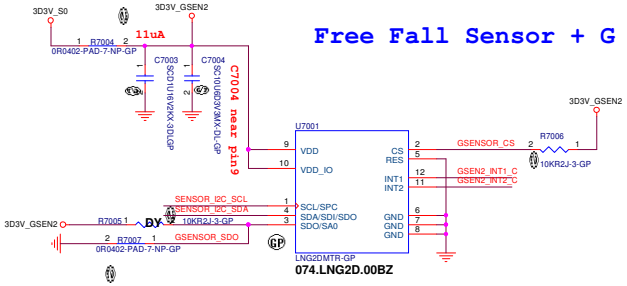
SSID = User.interface

Mantis Accelerometer for adaptive thermal and HDD protection

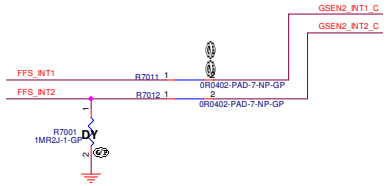
The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

[20] GSEN2_INT1_C
[20,55] SENSOR_I2C_SCL
[20,55] SENSOR_I2C_SDA
[20] FFS_INT1
[19] FFS_INT2

Free Fall Sensor + G Sensor



HellCat using 8 Bits:074.LNG2D.00BZ
Mocking Bird using 12 Bits :074.LIS2D.M002



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note:

(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

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Title: Free Fall Sensor
Size: A2 | Document Number: MOCKINGBIRD_TGL | Rev: A00
Date: Saturday, August 01, 2020 | Sheet 70 of 105

Main Func = TBT

HP team on applying, only murata have sample can meet Intel request
220nF AC cap must be placed on RX lines close to SOC side

HP team on applying ,only murata have sample can meet Intel request

Follow Hellcat15 Upsell TGL
https://vinafix.com

	WPN	DPN
TBT	071.00TBT.0F0U	M11GX
NON_TBT	071.00TBT.0D0U	7DYVG

TBT PORTS

BB
ZZ.000IC.002

BB TO PCH(TBT)

BB TO PCH(NON-TBT)

75.27002.F7C

MISC & DEBUG

BB
ZZ.000IC.002

20200221 (DVT1)
Follow reference circuits NC _a12

Power

BB
ZZ.000IC.002

GND

BB
ZZ.000IC.002

Type-C PD

BB
074.22975.0093
2nd = 74.03526.093

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EXT IO (Thunderbolt(1/3)/Type C Re-driver)

MOCKINGBIRD_TGL

A00

Follow Hellcat15 Upsell TGL

Main Func = TypeC

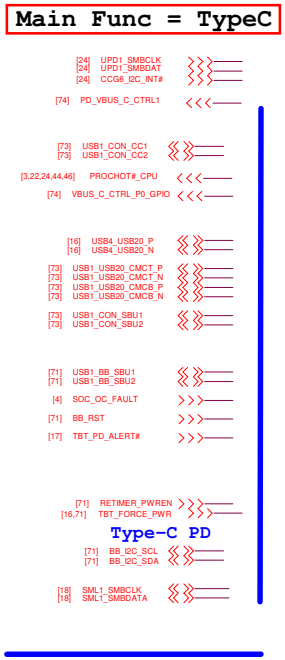
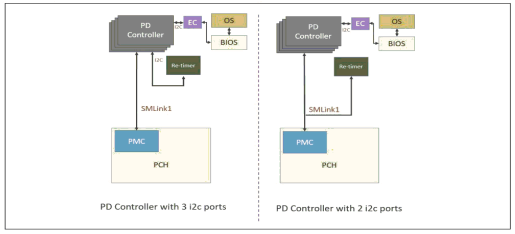


Figure 87. SMBus / SMlink Connectivity for USB Type-C PD Controller



Dell TGL Platform MOD_ID Options			
MUX	MOD_ID1	MOD_ID2	Description
BB8040R	L0	N/A	TBT Configuration w/BB Retimer
BB8010R	L2	N/A	non-TBT Configuration w/BB Retimer
TUSB546/1046	L6	L0	TUSB546 Equalizer config #1
TUSB546/1046	L6	L1 - L3	Reserved for TUSB546 Equalizer config #2,3,4 reserved

	CCG6_ID	R7216	R7218	計算值	理論值
0/8	L0	DY	64.10035.6DL (100K)	0	0
1/8	L1	064.71535.06D1 (715K)	64.10035.6DL (100K)	0.123	0.125
2/8	L2	64.30035.6DL (300K)	64.10035.6DL (100K)	0.25	0.25
3/8	L3	64.20035.6DL (200K)	64.12035.6DL (120K)	0.375	0.375
4/8	L4	64.10035.6DL (100K)	64.10035.6DL (100K)	0.5	0.5
5/8	L5	64.10035.6DL (100K)	64.20035.6DL (200K)	0.625	0.625
6/8	L6	64.22035.6DL (220K)	64.59035.6DL (590K)	0.728	0.75
7/8	L7	64.10035.6DL (100K)	064.71535.06D1 (715K)	0.877	0.875

<Core Design>
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Title: **EXT IO (Thunderbolt(2/3)/Type C CC Logic)**

Size	Document Number	Rev
A2	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 72 of 105

Main Func = TypeC

USB1

[71] USB1_SSTX_CON_P0
[71] USB1_SSTX_CON_N0
[71] USB1_SSTX_CON_P1
[71] USB1_SSTX_CON_N1

[71] USB1_SSRX_AR_P0
[71] USB1_SSRX_AR_N0
[71] USB1_SSRX_AR_P1
[71] USB1_SSRX_AR_N1

[72] USB1_USB20_CMCT_P
[72] USB1_USB20_CMCT_N
[72] USB1_USB20_CMCB_P
[72] USB1_USB20_CMCB_N

[72] USB1_CON_CC1
[72] USB1_CON_CC2

[72] USB1_CON_SBU1
[72] USB1_CON_SBU2

[71] USB1_SSTX_RC_N1
[71] USB1_SSRX_RC_P1

[71] USB1_SSRX_RC_N0
[71] USB1_SSTX_RC_N0

[71] USB1_SSRX_RC_P0
[71] USB1_SSTX_RC_P0

[71] USB1_SSRX_RC_N1
[71] USB1_SSTX_RC_P1

20V_VCCPD_VBUS

USB1

USB1_SSTX_CON_P0	A2	GND	GND	B1	
USB1_SSTX_CON_N0	A3	SSTXP1	SSTXP2	B2	USB1_SSTX_CON_P1
	A4	SSTXN1	SSTXN2	B3	USB1_SSTX_CON_N1
USB1_CON_CC1	A5	VBUS#A4	VBUS#B4	B4	
USB1_USB20_CONT_P	A6	CC1	CC2	B5	USB1_CON_CC2
USB1_USB20_CONT_N	A7	DP1	DP2	B6	USB1_USB20_CONB_P
USB1_CON_SBU1	A8	DN1	DN2	B7	USB1_USB20_CONB_N
	A9	RFU1	RFU2	B8	USB1_CON_SBU2
USB1_SSRX_AR_N1	A10	VBUS#A9	VBUS#B9	B9	
USB1_SSRX_AR_P1	A11	SSRXN2	SSRXN1	B10	USB1_SSRX_AR_N0
	A12	SSRXP2	SSRXP1	B11	USB1_SSRX_AR_P0
		GND	GND	B12	
			CHASSIS#13	13	
			CHASSIS#14	14	
			CHASSIS#15	15	
			CHASSIS#16	16	

20V_VCCPD_VBUS

20191216
For layout requirement

20191211
Follow Connector list 1210
20200416
change to the part which HC17 use

SKT-USB28-27-GP-U
062.10009.M042
2nd = 062.10009.M060

Follow Hellcat15 Upsell TGL

https://vinafix.com

20200504
Remove C7302 C7304
Change C7301 C7302 to 0402 size

20V_VCCPD_VBUS

C7301 SCD1U25V2KX-1DL-GP
C7303 SCD1U25V2KX-1DL-GP
DY C7307 SC10U25V3MX-5-GP

2020/02/29:swap EL7302/EL7301

20200722
Remove R7301
R7302 R7303 R7304

FILTER-4P-132-GP
EL7302
68.02002.061
2nd = 068.09002.2001

EL7301
FILTER-4P-132-GP
68.02002.061
2nd = 068.09002.2001

20200213
Follow EMC requestment

ED7301 PESD5V0H1BSFYL-GP-U1
ED7302 PESD5V0H1BSFYL-GP-U1
ED7303 PESD5V0H1BSFYL-GP-U1
ED7304 PESD5V0H1BSFYL-GP-U1
ED7305 PESD5V0H1BSFYL-GP-U1
ED7306 PESD5V0H1BSFYL-GP-U1
ED7307 PESD5V0H1BSFYL-GP-U1
ED7308 PESD5V0H1BSFYL-GP-U1

083.5V0H1.00AF
2nd = 083.08017.00AF

20191212
Follow Nakia

DY C7305 SCD1U50V2JN-3-LL-GP
DY C7306 SCD1U50V2JN-3-LL-GP

ED7309 PESD5V0H1BSFYL-GP-U1
ED7310 PESD5V0H1BSFYL-GP-U1
ED7311 PESD5V0H1BSFYL-GP-U1
ED7312 PESD5V0H1BSFYL-GP-U1
ED7313 PESD5V0H1BSFYL-GP-U1
ED7314 PESD5V0H1BSFYL-GP-U1
ED7315 PESD5V0H1BSFYL-GP-U1
ED7316 PESD5V0H1BSFYL-GP-U1

<Core Design>

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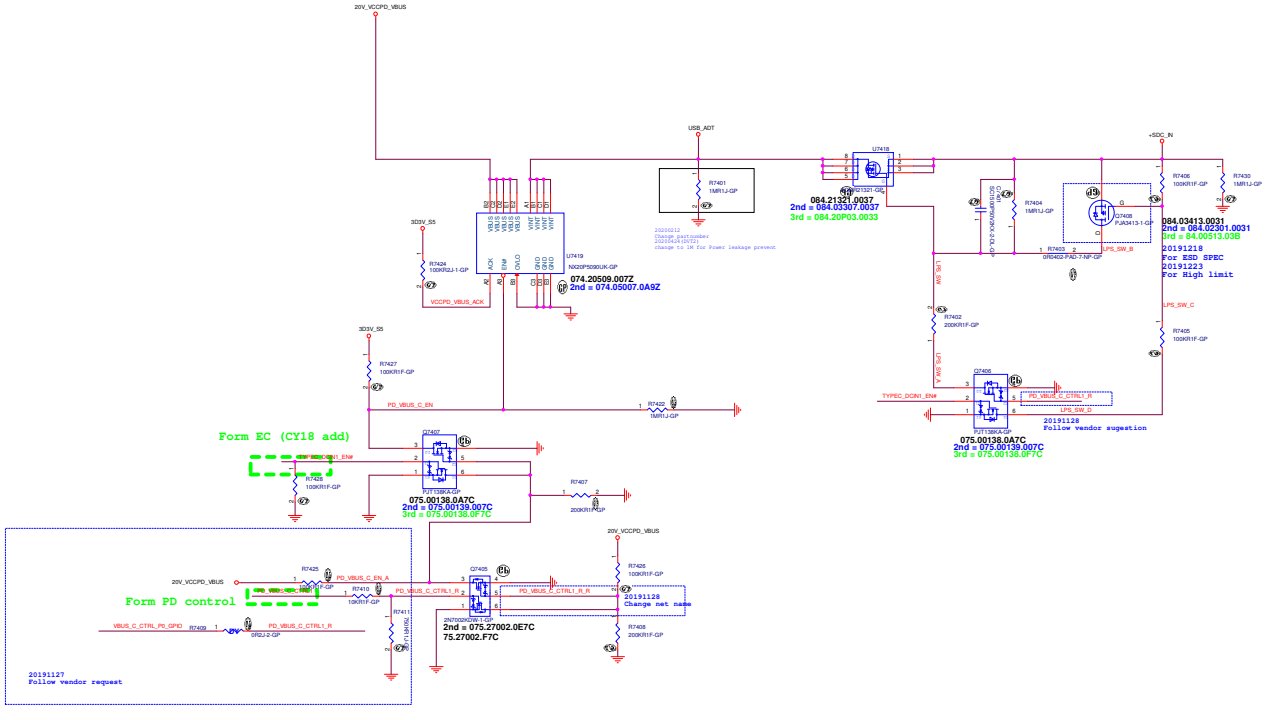
Title: EXT IO (Thunderbolt(3/3)/Type C Conn)

Size	Document Number	Rev
A3	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 73 of 105

[72] PD_VBUS_C_CTRL1
[24] TYPEC_DCIN1_EN#
[44] VCCPD_VBUS_ACK
[72] VBUS_C_CTRL_PD_GPIO



<Core Design>

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Title: GPU(2/5)DIGITALOUT
Size: A1 | Document Number: MOCKINGBIRD_TGL | Rev: A00
Date: Saturday, August 01, 2020 | Sheet 74 of 105

(Blanking)

<Core Design>

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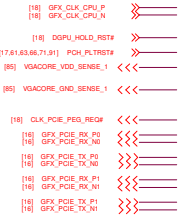
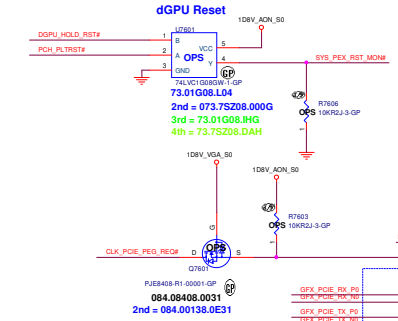
Title: *Reserved*

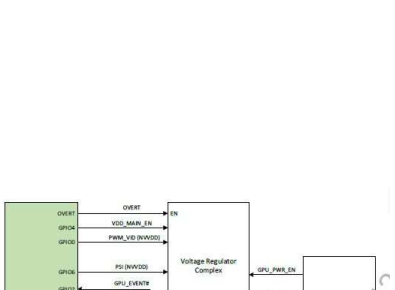
Size	Document Number	Rev
A3	*MOCKINGBIRD_TGL*	*A00*

Date: Saturday, August 01, 2020 Sheet 75 of 105

Main Func = dGPU







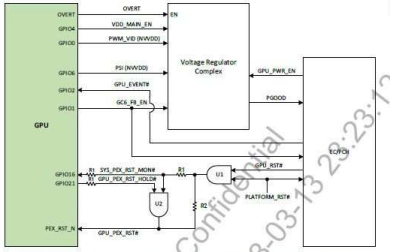
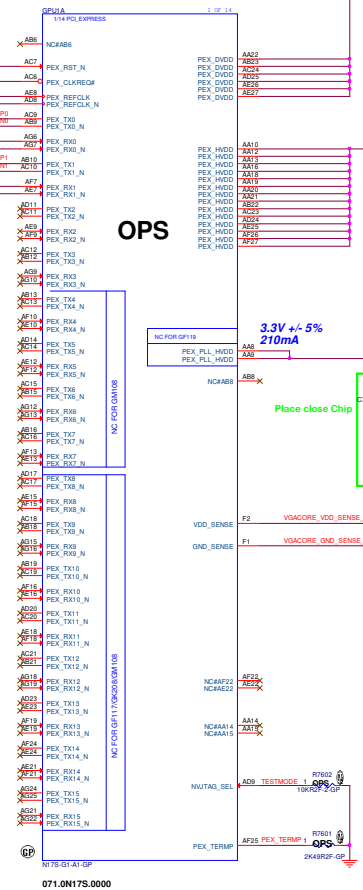


Figure 11. GC6 2.1 High-Level Signal Connections Concept (w/o GPIO Swizzling)

Note: It is critical that the GPU's OVERT output be routed directly to the voltage regulator complex enable (EN) input so that the GPU can trigger a shutdown.



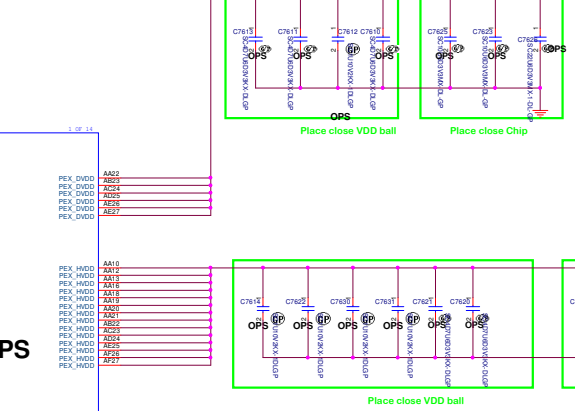


Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
PEX_PLL_HVDD Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU

<Core Design>

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Title: GPU(1/5)PEG

Size: Custom | Document Number: MOCKINGBIRD_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 76 of 105

Main Func = dGPU

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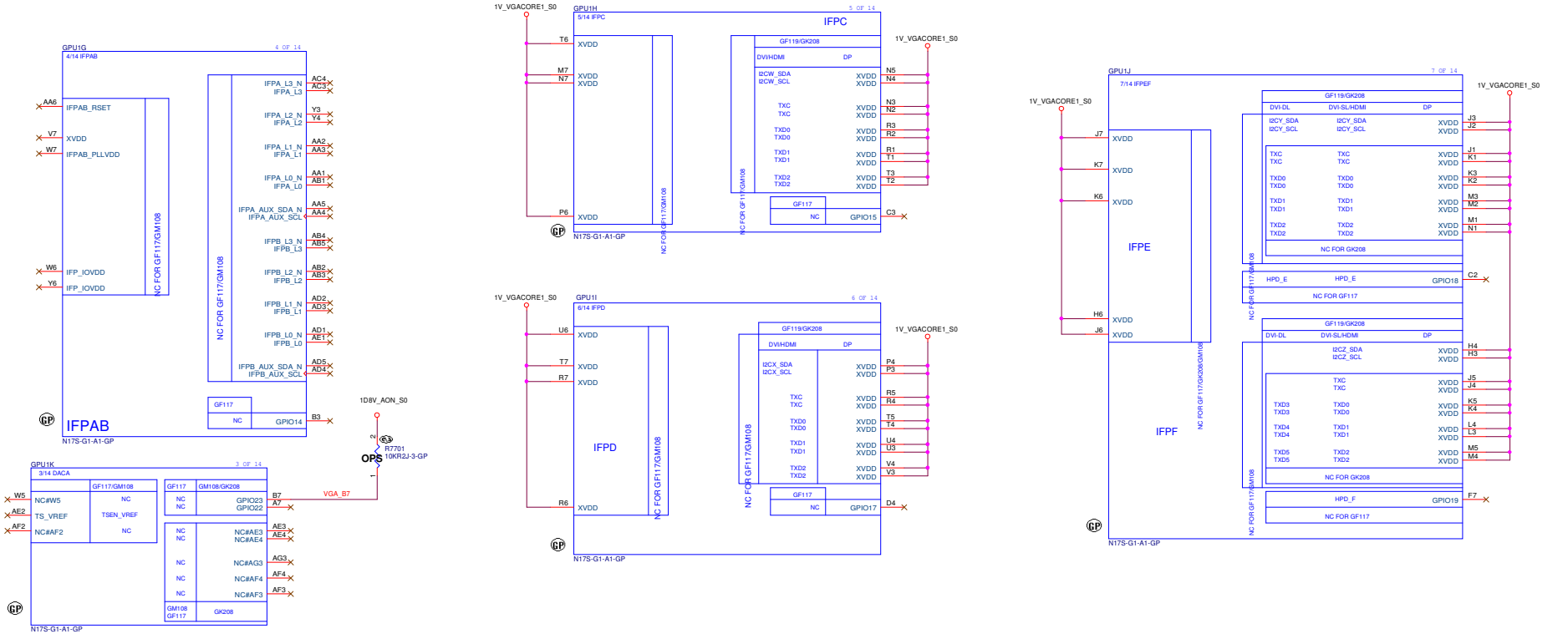

<Core Design>

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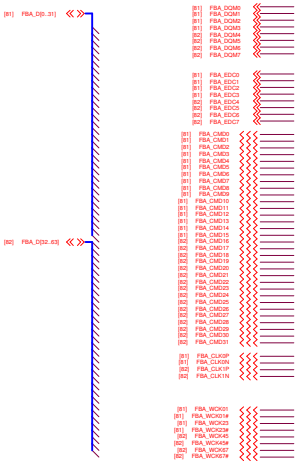
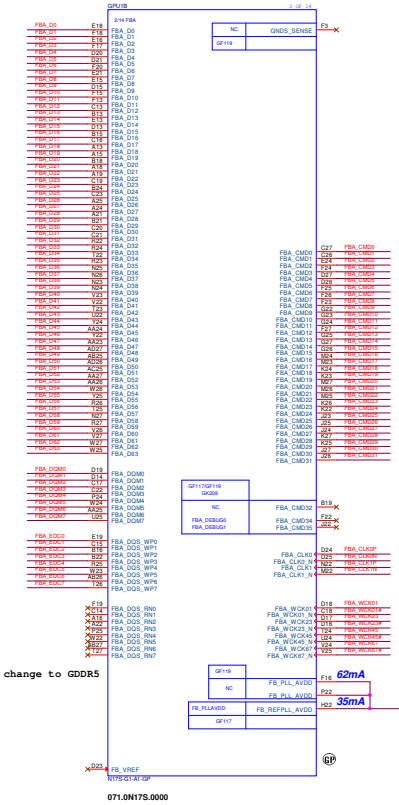
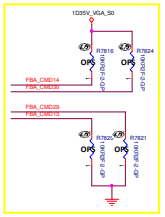
Title: *GPU(2/5)DIGITALOUT*		
Size: A2	Document Number: MOCKINGBIRD_TGL	Rev: A00
Date: Saturday, August 01, 2020	Sheet 77 of 105	

Main Func = dGPU





Modify by change to GDDR5



Note:
Reference NV-DDR5 CRB and DOH70 by GDDR5

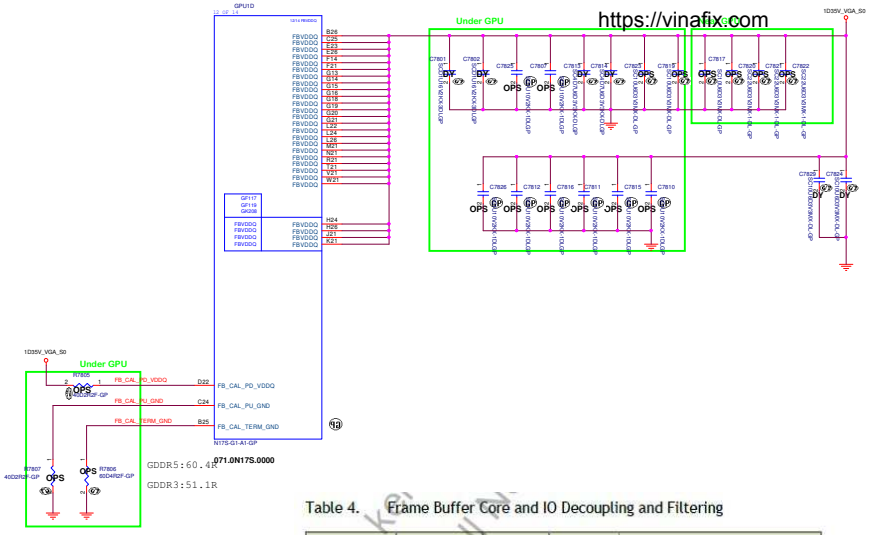


Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type				
	30 Ω (ESR=0.010 Ω)	0603	1	1	Near GPU

<Core Design>

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GPU(3/5)VRAM/F

Size	Document Number	Rev
A1	MOCKINGBIRD_TGL	A00

Date: Sheet 78 of 155

Main Func = dGPU

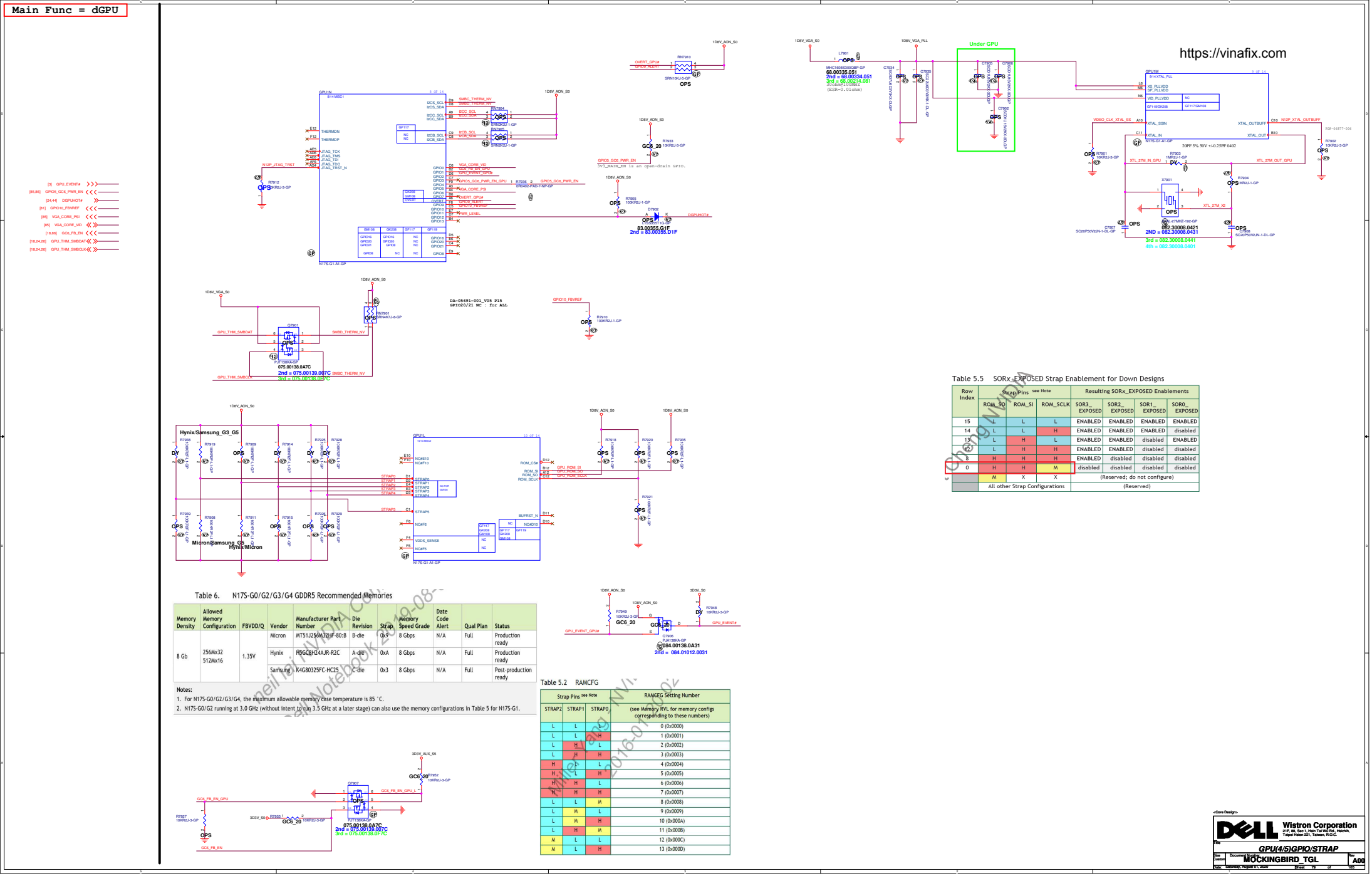

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Table 6. N17S-G0/G2/G3/G4 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FC-HC25	C-die	0x3	8 Gbps	N/A	Full	Post-production ready

Notes:
1. For N17S-G0/G2/G3/G4, the maximum allowable memory case temperature is 85 °C.
2. N17S-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations in Table 5 for N17S-G1.

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

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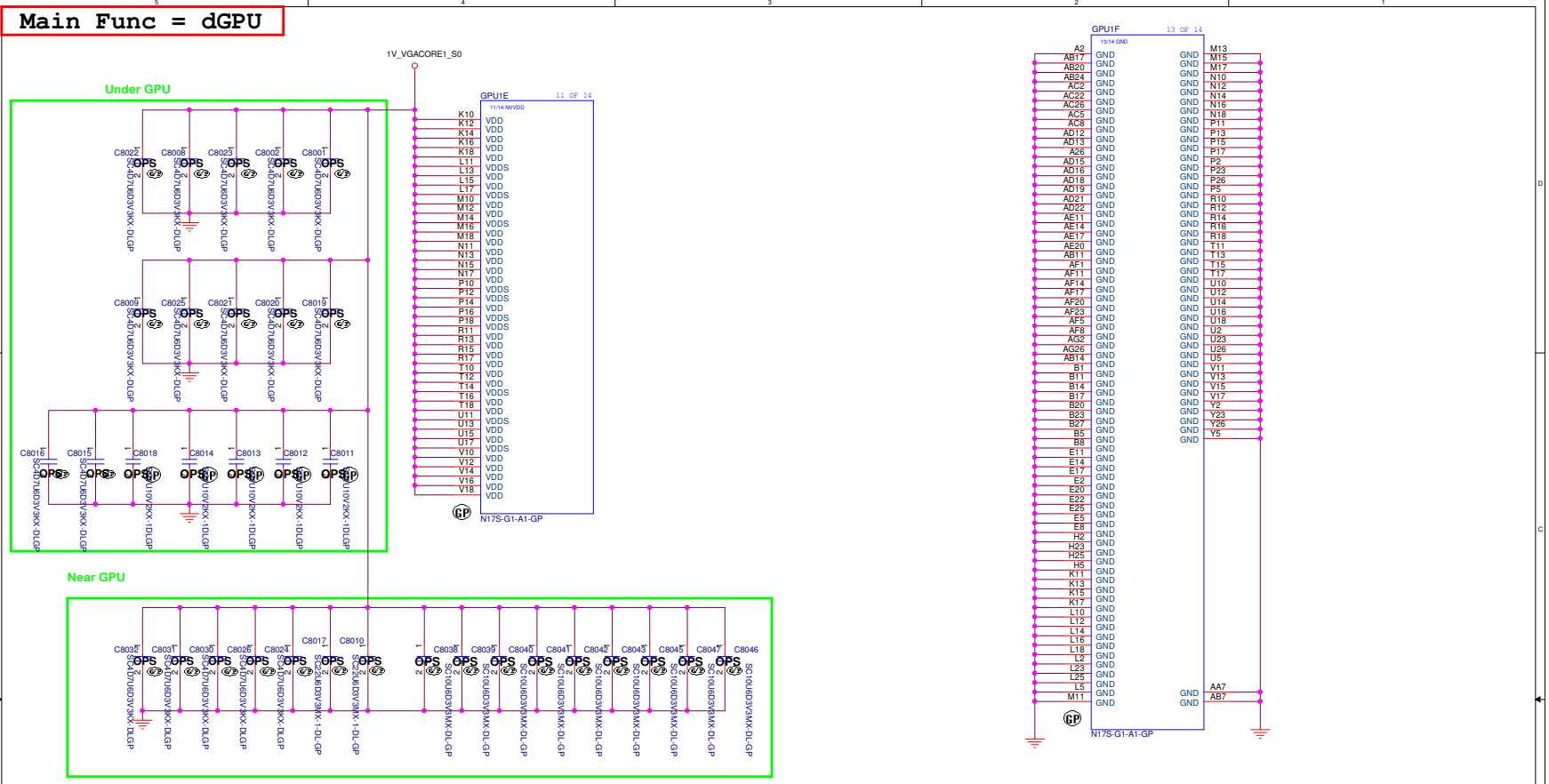
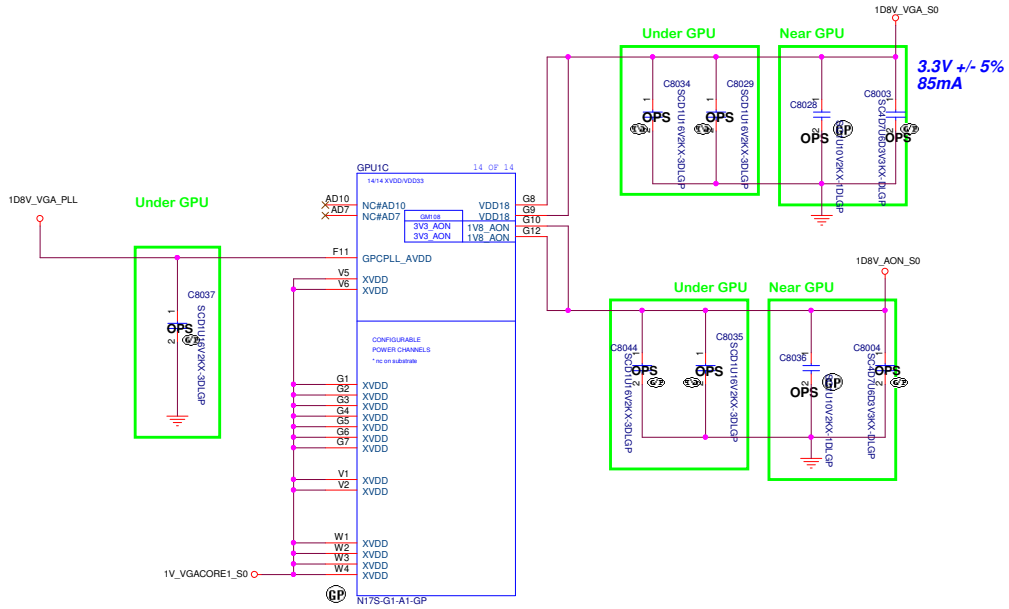
File: GPU(4/5)GPIO/STRAP

Size: Custom | Document Number: MOCKINGBIRD_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 78 of 105

Main Func = dGPU





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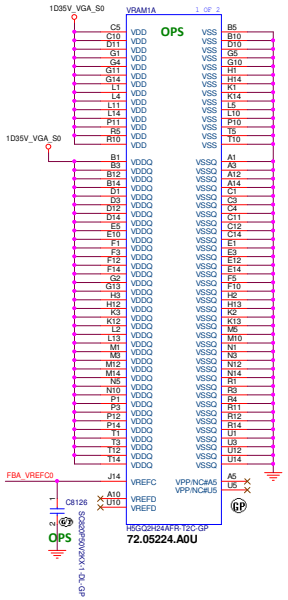
Title: GPU(5/5)PWR/GND

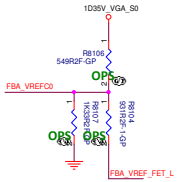
Size: Custom | Document Number: MOCKINGBIRD_TGL | Rev: A00

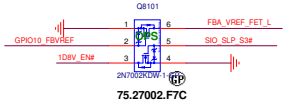
Date: Saturday, August 01, 2020 | Sheet 80 of 105

SSID = VRAM

Frame Buffer Patition A-Lower Half



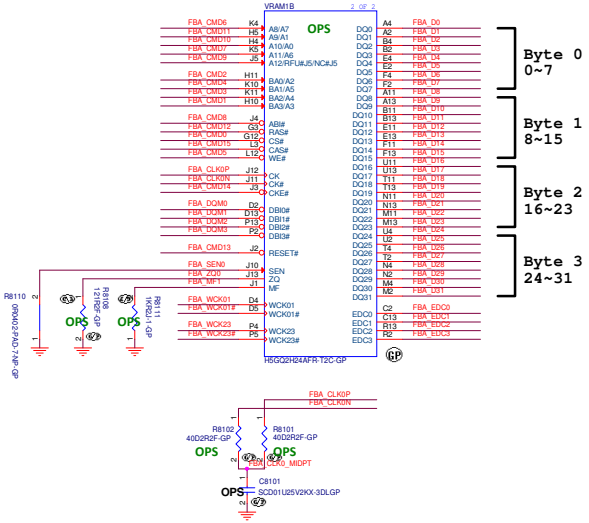




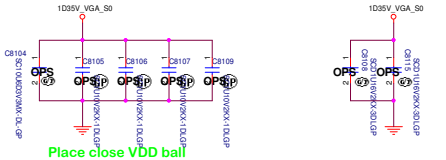
FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

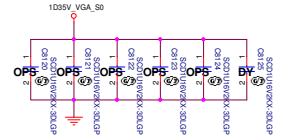
Normal(MF=0)



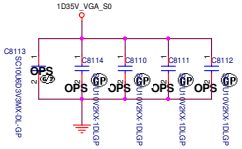
Place close VDD ball



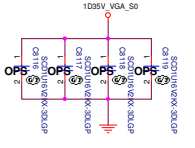
Place close VDD ball



Place close VDDQ ball



Place close VDDQ ball



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Title: **GPU-VRAM1,2 (1/4)**

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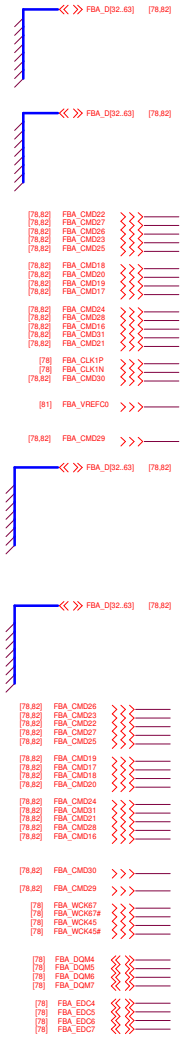
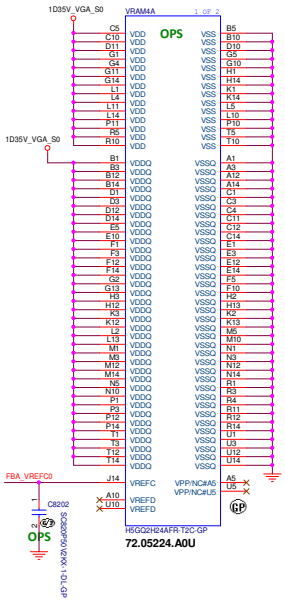
Date: Saturday, August 01, 2020 | Sheet 81 of 105

SSID = VRAM



Frame Buffer Patition A-Upper Half



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

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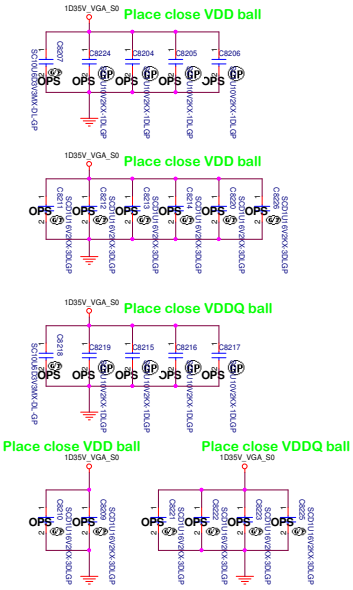
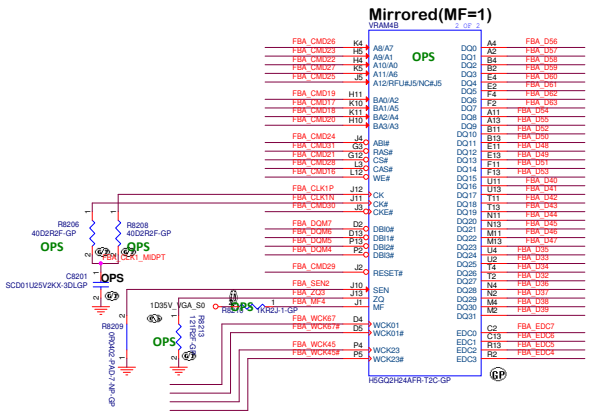


Mirrored(MF=1)



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Title: GPU-VRAM3.4 (2/4)

Size	Document Number	Rev
Custom	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 82 of 105

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Title

GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
A3	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 83 of 105

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Title

GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
A4	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 84 of 105

RT8816B For NVVDDS

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VGA : N17S-G3/G5
EDP-Peak : 69.9A

OFFPAGE-Signal

PH on EE side
1. Check EE side
2. Modify DAT

PH on EE side

EE need check

Figure 8.8 GC6 2.1 Voltage Regulator Complex Signal Connection

For VGA_CORE sequence
EE need check

OFFPAGE-GAP

Table 1	
Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

VGA : N17S-G3/G5
EDP-Peak : 69.9A
83.88A<OCP<97.86A

PU8552 PU855
For G3: 075.07321.0073
For G5: 075.07362.0073

ID:31/54A .
Rdson: 6.8~8.6/2.8~3.5m (Q1/Q2)

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 37A , Isat : 41A

OCP setting
160K ohm for OCP around 96.2A setting

SS setting

Place Near GPU (NVVDDS)
1X330uF (Poscap) - PT8511 (Page85)

<Core Design>

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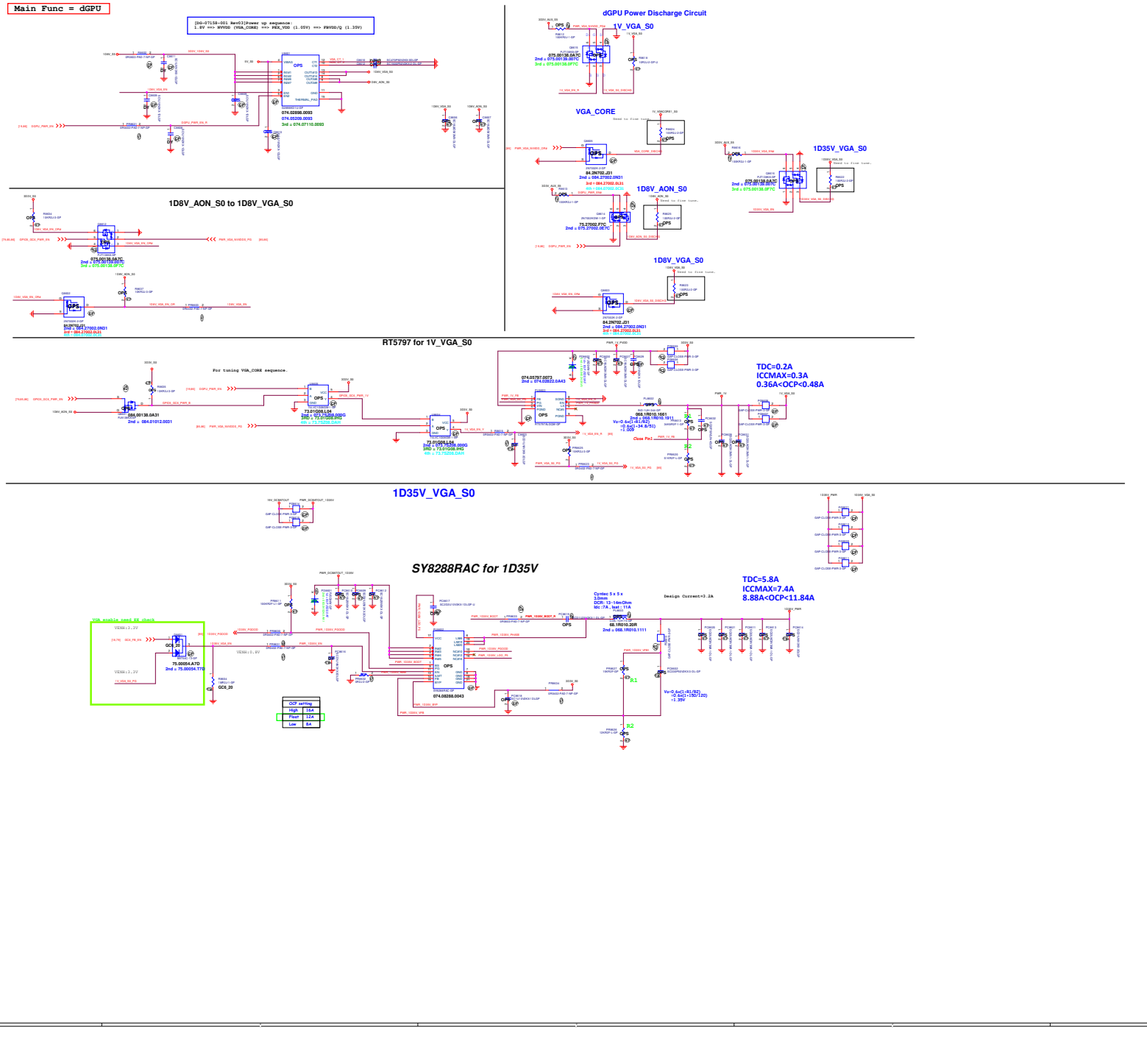
Title	GPU (RT8816A_VGA)		
Size	Document Number		Rev
A1	MOCKINGBIRD_TGL		A00
Date: Saturday, August 01, 2020	Sheet 85	of	105

Main Func = dGPU



Main Func = dGPU

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Title: *Reserved*

Size	Document Number	Rev
A3	*MOCKINGBIRD_TGL*	*A00*

Date: Saturday, August 01, 2020 Sheet 87 of 105

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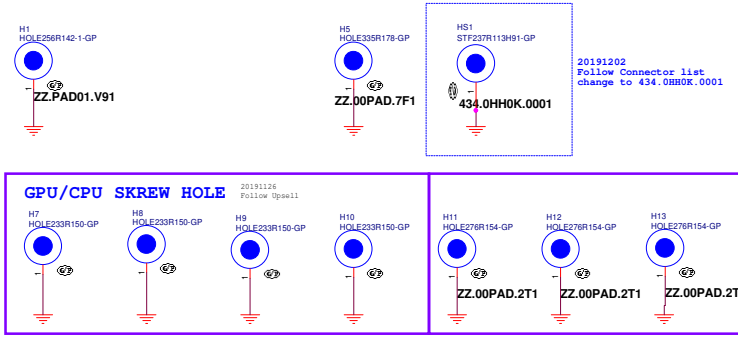
Title

Reserved

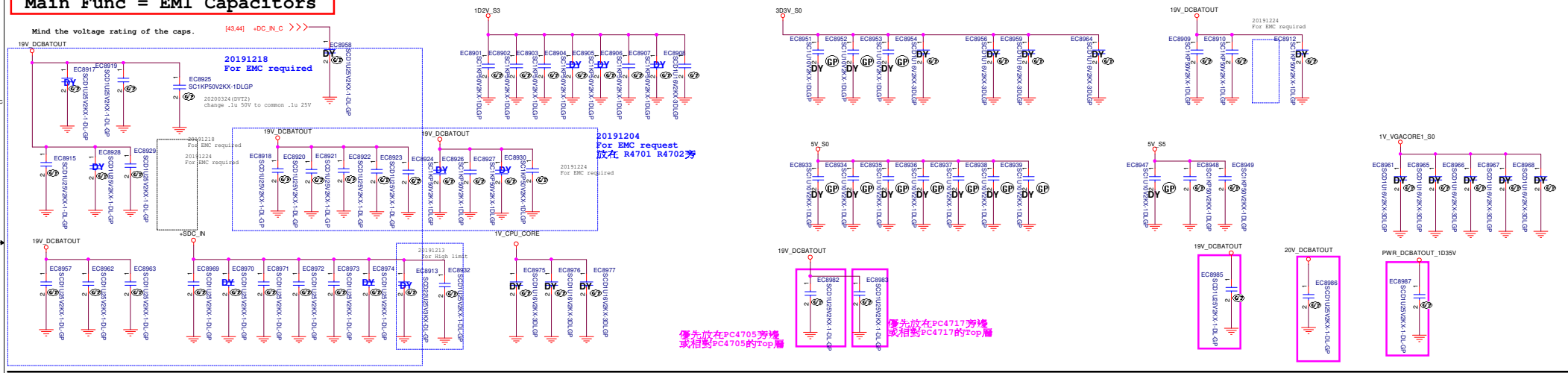
Size	Document Number	Rev
A4	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 88 of 105

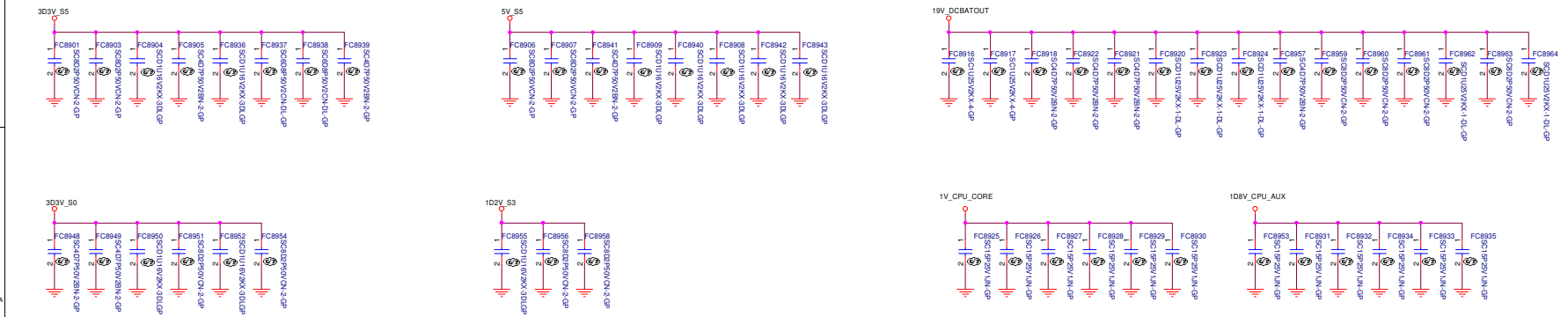
Main Func = UnusedParts



Main Func = EMI Capacitors



Main Func = RF Capacitors



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Title: *UNUSED PARTS/EMI Capacitors*

Size	Document Number	Rev
A2	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 89 of 105

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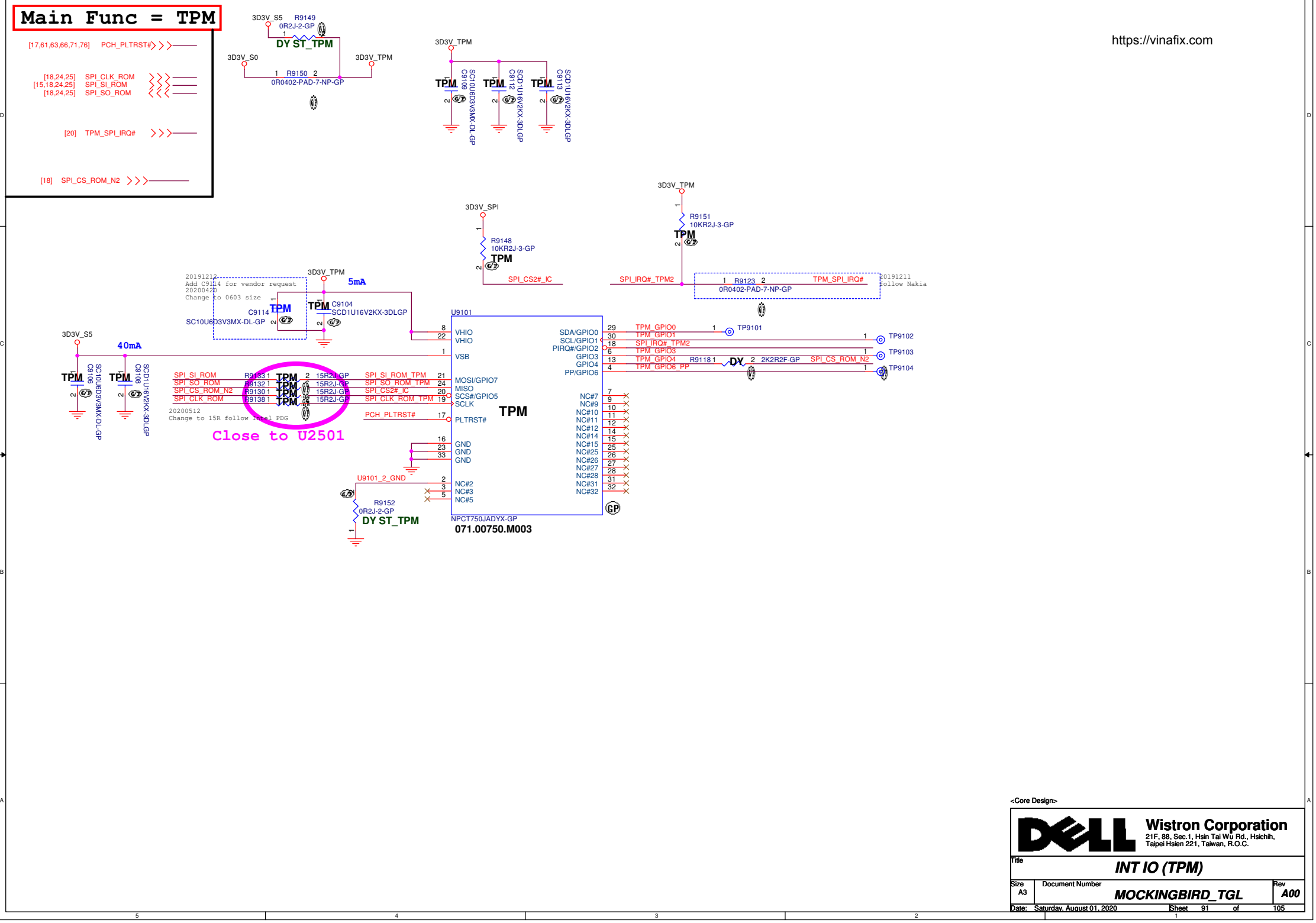
Title

Reserved

Size	Document Number	Rev
A4	***MOCKINGBIRD_TGL***	***A00***

Date: Saturday, August 01, 2020 Sheet 90 of 105

Main Func = TPM



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Title	INT IO (TPM)	
Size A3	Document Number MOCKINGBIRD_TGL	Rev A00
Date: Saturday, August 01, 2020	Sheet 91 of 105	

SSID = Finger Print

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Title
Finger Print

Size	Document Number	Rev
A4	*MOCKINGBIRD_TGL*	*A00*

Date: Saturday, August 01, 2020 Sheet 92 of 105

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<Core Design>

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Title: *(Reserved)*

Size: A3 | Document Number: *MOCKINGBIRD_TGL* | Rev: *A00*

Date: Saturday, August 01, 2020 | Sheet 93 of 105

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<Core Design>

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Date: Saturday, August 01, 2020 | Sheet 94 of 105

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Date: Saturday, August 01, 2020 | Sheet 95 of 105

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Size	Document Number	Rev
A4	*MOCKINGBIRD_TGL*	*A00*

Date: Saturday, August 01, 2020 Sheet 96 of 105

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Title

LVDS_Switch

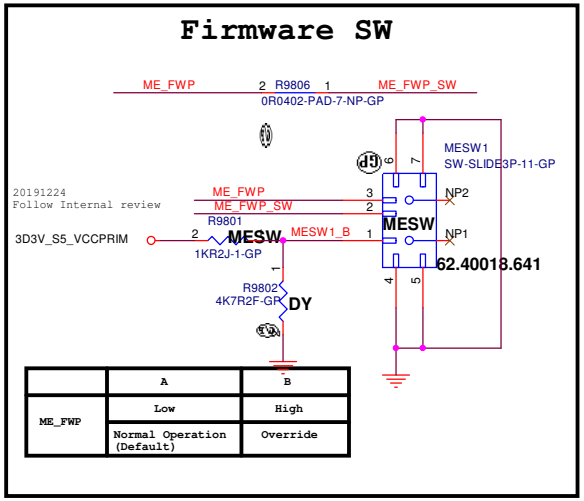
Size	Document Number	Rev
A4	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 97 of 105

Main Func = Firmware SW

[19] ME_FWP_SW
[24] ME_FWP

Firmware SW



	A	B
ME_FWP	Low	High
	Normal Operation (Default)	Override

	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

<Core Design>

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Title: CRT_Switch

Size: A3 | Document Number: MOCKINGBIRD_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 98 of 105

<Core Design>

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Title

Debug (XDP debug)

Size	Document Number	Rev
A4	*MOCKINGBIRD_TGL*	*A00*

Date: Saturday, August 01, 2020 Sheet 99 of 105

CLK Block Diagram

TBD

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Title: CLK Block Diagram		
Size: A2	Document Number: MOCKINGBIRD_TGL	Rev: A00
Date: Saturday, August 01, 2020	Sheet 100 of 105	

Change notes –

Item #	Subsystem /Component	PHASE	SCH Page #	Change Request Description	Requested By	BOM	Schematic	Layout	Reason of Change
1	EC&KBC&SIO	DVT2	24	Change R2443 to 27K	EE	V			Change Board ID to DVT2
2	PWR.3p3V_5p0V	DVT2	40	Add C4070 & C4071	EE	V	V	V	Follow Vendor's suggestion(add cap to prevent IC broken)
3	GPU.Power	DVT2	86	Add C8613	EE	V	V	V	Follow Vendor's suggestion(add cap to prevent IC broken)
4	Audio.DMIC	DVT2	19	Add U1901, C1901, C1902, R1942, R1943, R1944, R1945, R1946, R1947, R1948 Reserve C1902, R1942	EE	V	V	V	Follow DMIC Vendor's suggestion
5	Conn.WLAN	DVT2	61	Change R6109, R6118 to 49.9 ohm	EE	V			Follow Intel CNVI checklist (575882) change CNV_BRI_RSP and CNV_RGI_RSP damping resistor, from 22 to 49.9 ohm.
6	Platform.BIOS_ROM	DVT2	25	Complete reference plane for SPI signal	EE			V	For reference GND
7	EC&KBC&SIO	DVT2	24	Complete reference plane for eSPI signal	EE			V	For reference GND
8	EC&KBC&SIO	DVT2	24	Change PECI_VREF power to VCCST	EE	V	V	V	Follow Vendor's suggestion
9	IO.Type-C.TBT	DVT2	71	Q7101 , R7178 , R7179 , R7196, R7197 Change to DY	EE	V			Follow Intel TBT check list
10	GPU.Power	DVT2	85	PU8552 , PU8554 Change to 075.07362.0073 for N17s-G5	EE	V			Follow Vendor's suggestion
11	PCH	DVT2	54	premium power circuit stuff for HC15MS	EE	V			premium power circuit for 15MS only

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Title: *Change History*

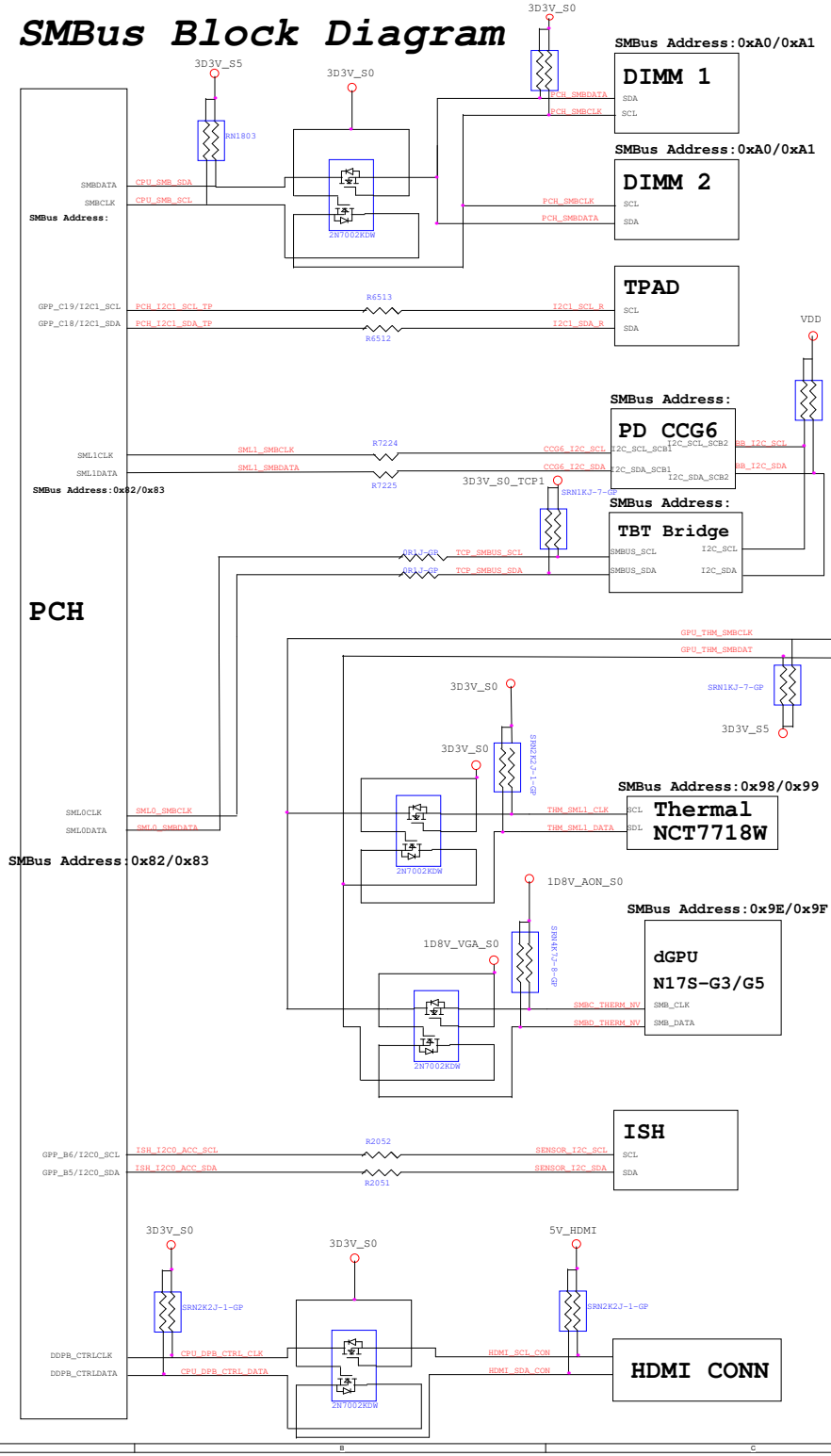
Size	Document Number	Rev
A3	*MOCKINGBIRD_TGL*	*A00*

Date: Saturday, August 01, 2020 Sheet 101 of 105

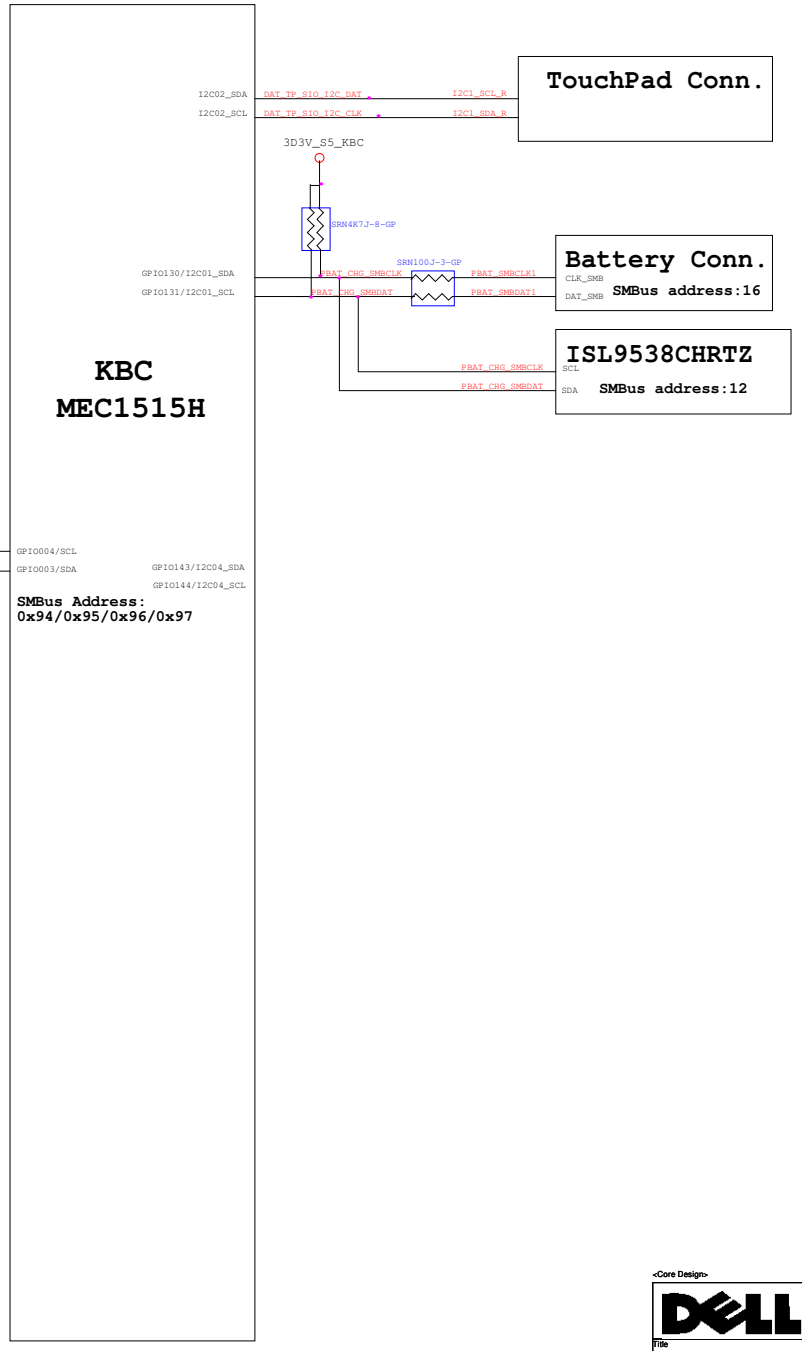
TBD

TBD

PCH SMBus Block Diagram



KBC SMBus Block Diagram



<Core Design>

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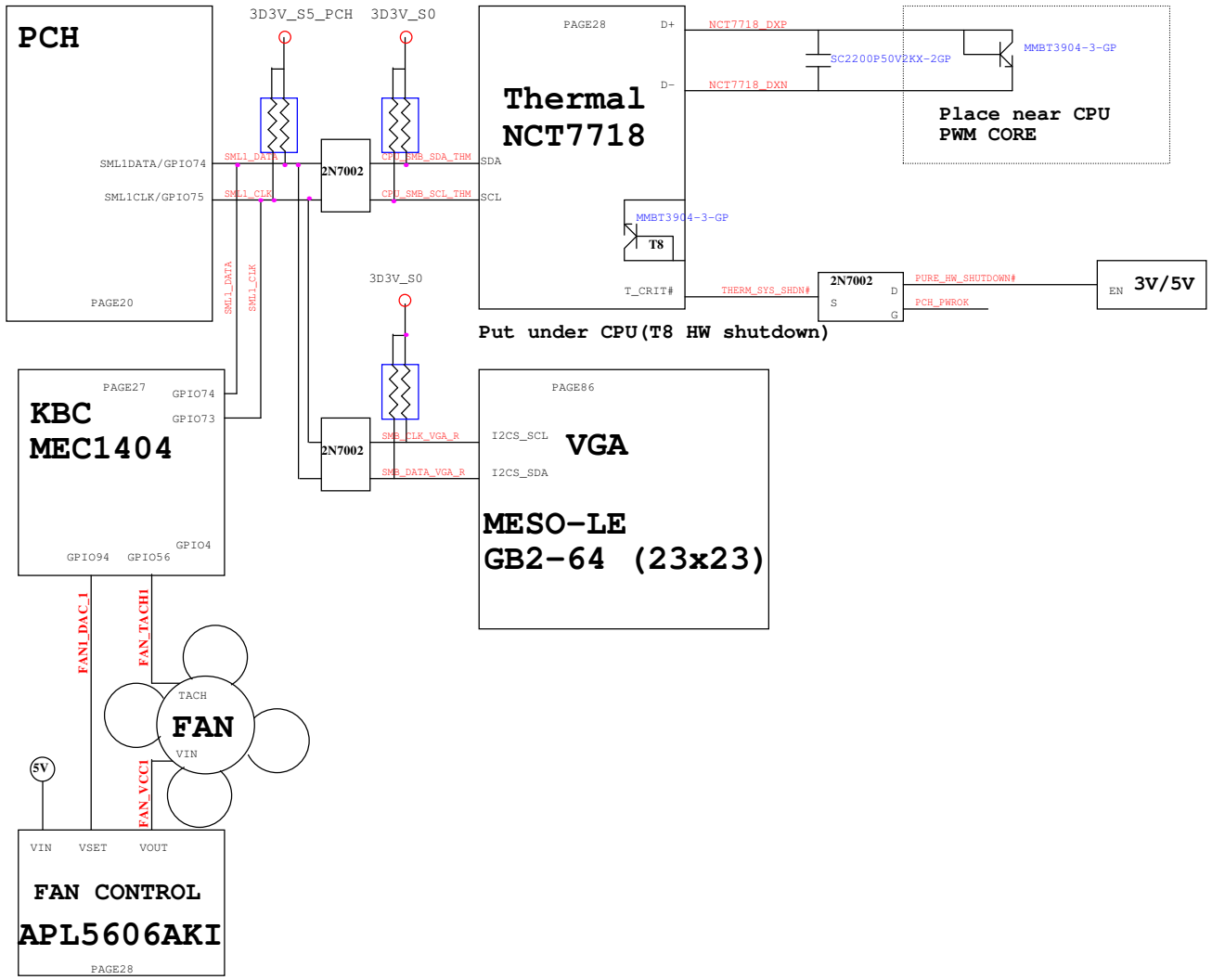
Title: SMBUS Block Diagram

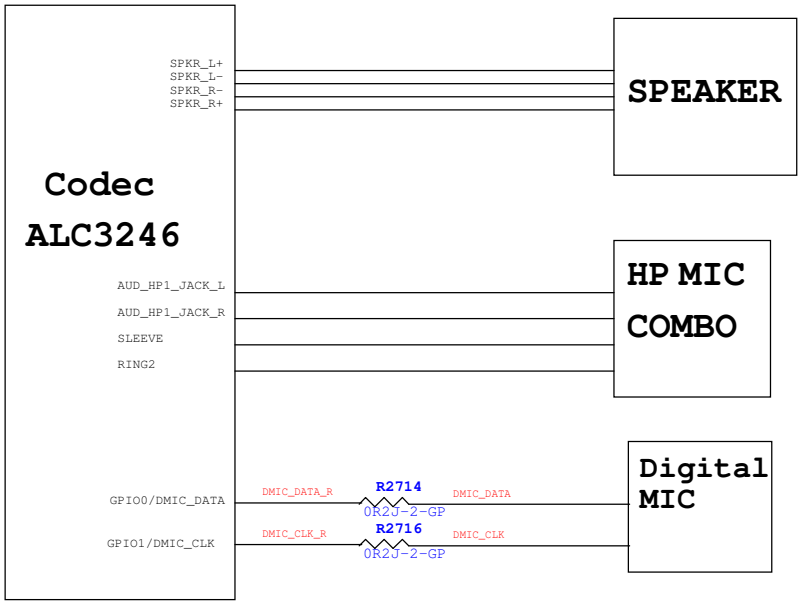
Size	Document Number	Rev
A2	MOCKINGBIRD_TGL	A00

Date: Saturday, August 01, 2020 Sheet 104 of 105

Thermal Block Diagram



Audio Block Diagram



<Core Design>

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Title: Thermal/Audio Block Diagram

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Date: Saturday, August 01, 2020 | Sheet 105 of 105