Neptune_KLS

Schematics Document

<Core Design>

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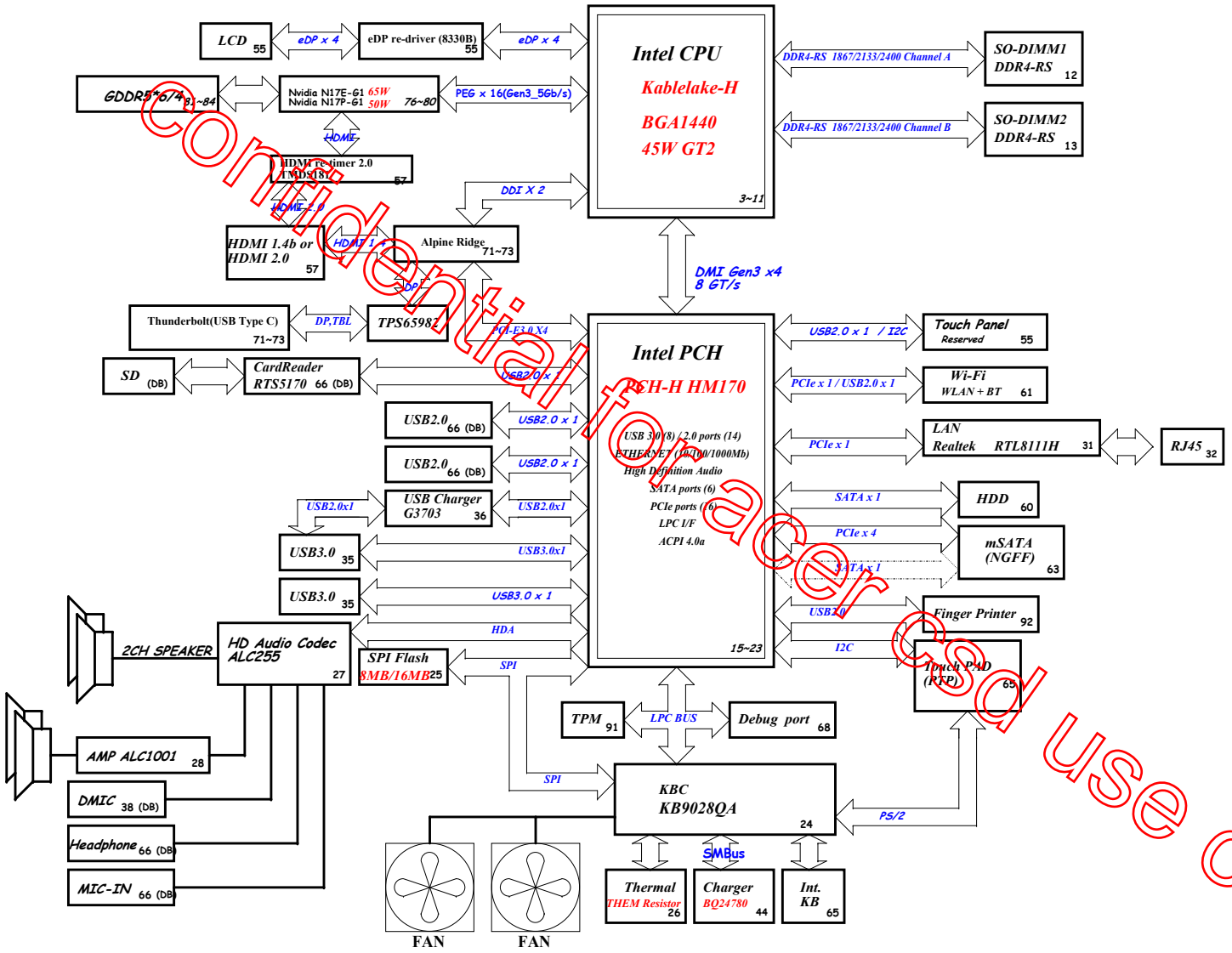
Title: **Cover Page**

Size	Document Number	Rev
A	Neptune_KLS	-1m

Date: Wednesday, May 17, 2017 Sheet 1 of 105

Neptune_KLS Board Block Diagram

Project code : 4PD0B1010001
PCB P/N : 16834
Revision : 1m



CHARGER	
BQ24780SRUYR	44
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC	
RT6575D	45
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

CPU Core Power	
ISL95855HRTZ	46,47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

DDR4 power	
APW8861QBI-TRG	51
INPUTS	OUTPUTS
DCBATOUT	1D2V_S3 2D5V_S3 0D6V_S0

1D0V_S5	
RT8231AGQW	52
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

CPU 1D8V_S0	
RT9025	53
INPUTS	OUTPUTS
3D3V_S5 5V_S5	1D5V_S0

Switches	
	40
INPUTS	OUTPUTS
5V_S5 3D3V_S5 1D0V_S5	5V_S0 3D3V_S0 0D95V_VCCIO 1V_VCCST

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Title: Block Diagram

Size	Document Number	Rev
C	Neptune_KLS	-1m

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Title: CPU (PCIE/DMI/FDI)

Size: Custom | Document Number: Neptune_KLS | Rev: -1m

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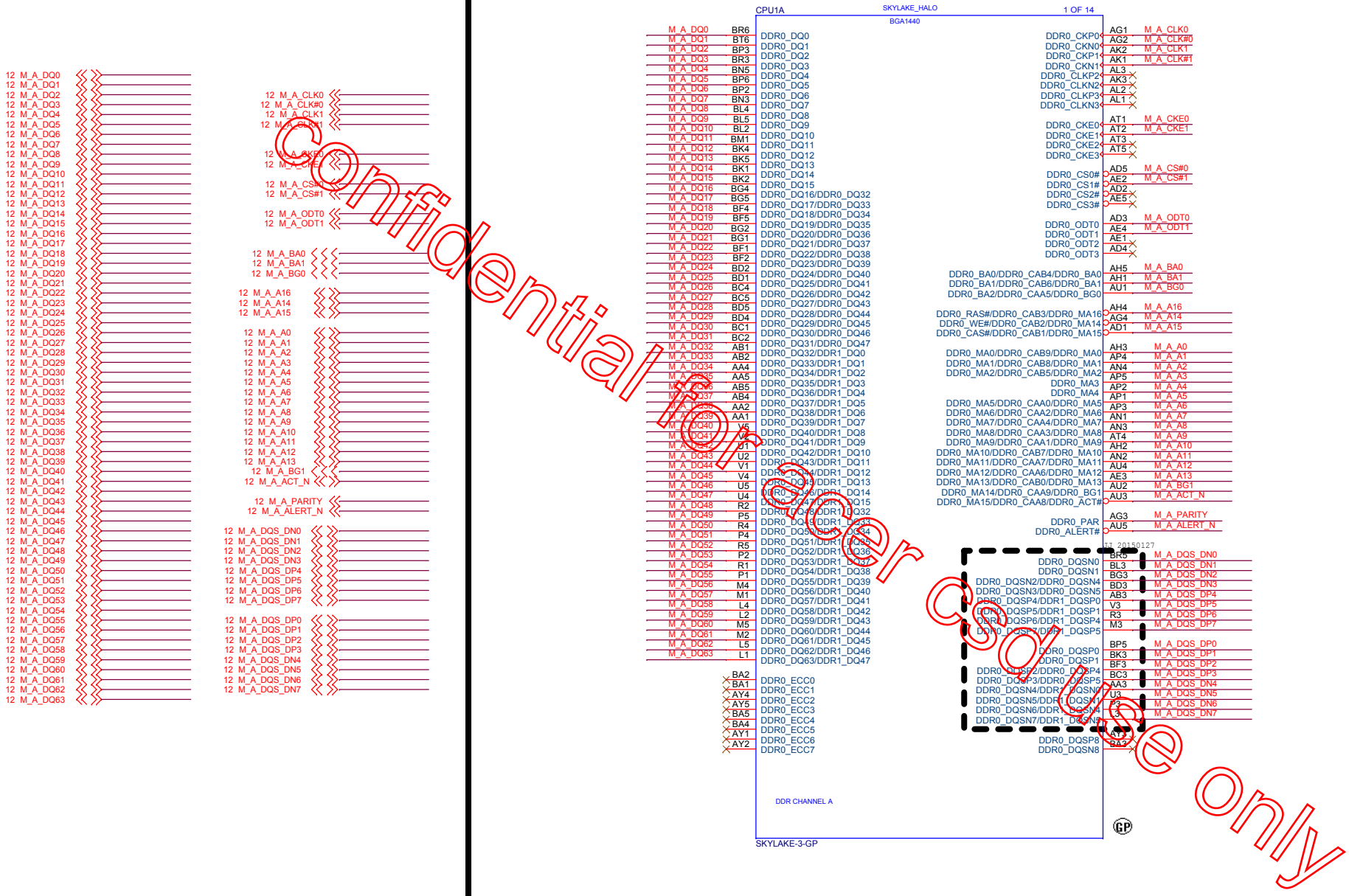

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Title: CPU_DDR_CHA

Size: A3 | Document Number: Neptune_KLS | Rev: -1m

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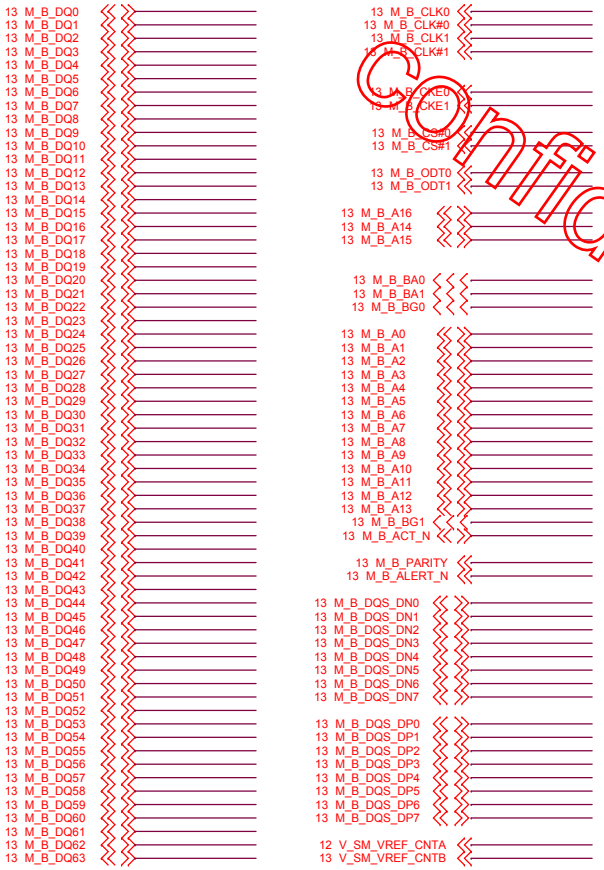
SSID = CPU



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Title: CPU_DDR_CHB

Size: A3 | Document Number: Neptune_KLS | Rev: -1m

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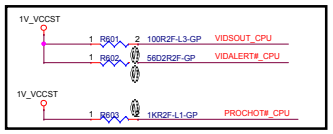
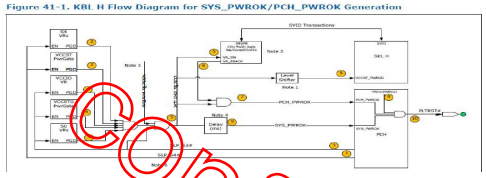
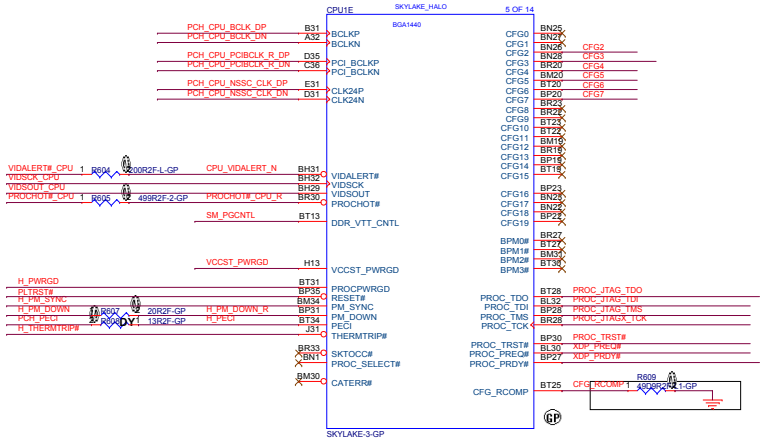
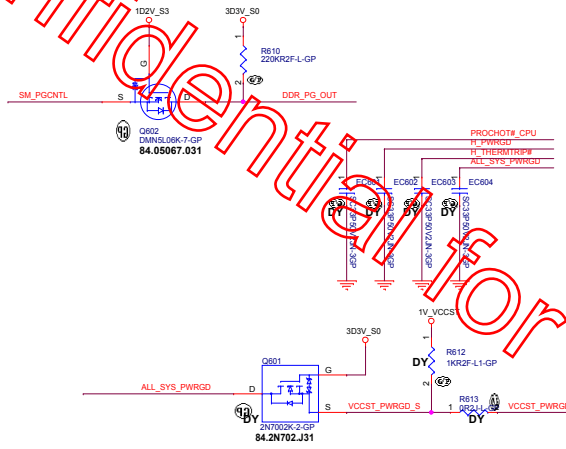
AROUND_CPU





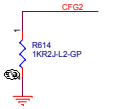


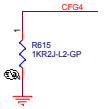


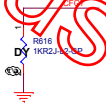
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

eDP Enable	
CFG4	1:Disable 0:Enable

PEG Training	
CFG7	1 (default) PEG Train immediately following RESET# de assertion. 0 = PEG Wait for BIOS for training.







PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM[3:0]	Pull Up	Vcc_{IO}	16-60 Ω
PREQ#	Pull Up	Vcc_{ST}	3 kΩ
PROC_TDI	Pull Up	Vcc_{STG}[1]	3 kΩ
PROC_TMS	Pull Up	Vcc_{SGT}[1]	3 kΩ
PROC_TRST#	Pull Down	-	3 kΩ
CFG[19:0]	Pull Up	Vcc_{IO}	3 kΩ

Notes:
1. For S-Processor line, it should be Vcc_{ST}

Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: – 1 = (Default) Normal Operation; No stall. – 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. – 1 = Normal operation – 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: – 1 = Disabled. – 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation – 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: – 1 = (default) PEG Train immediately following RESET# de assertion. – 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

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Title: CPU_CFG_CFG STRAP

Size: A2 | Document Number: Neptune_KLS | Rev: -1m

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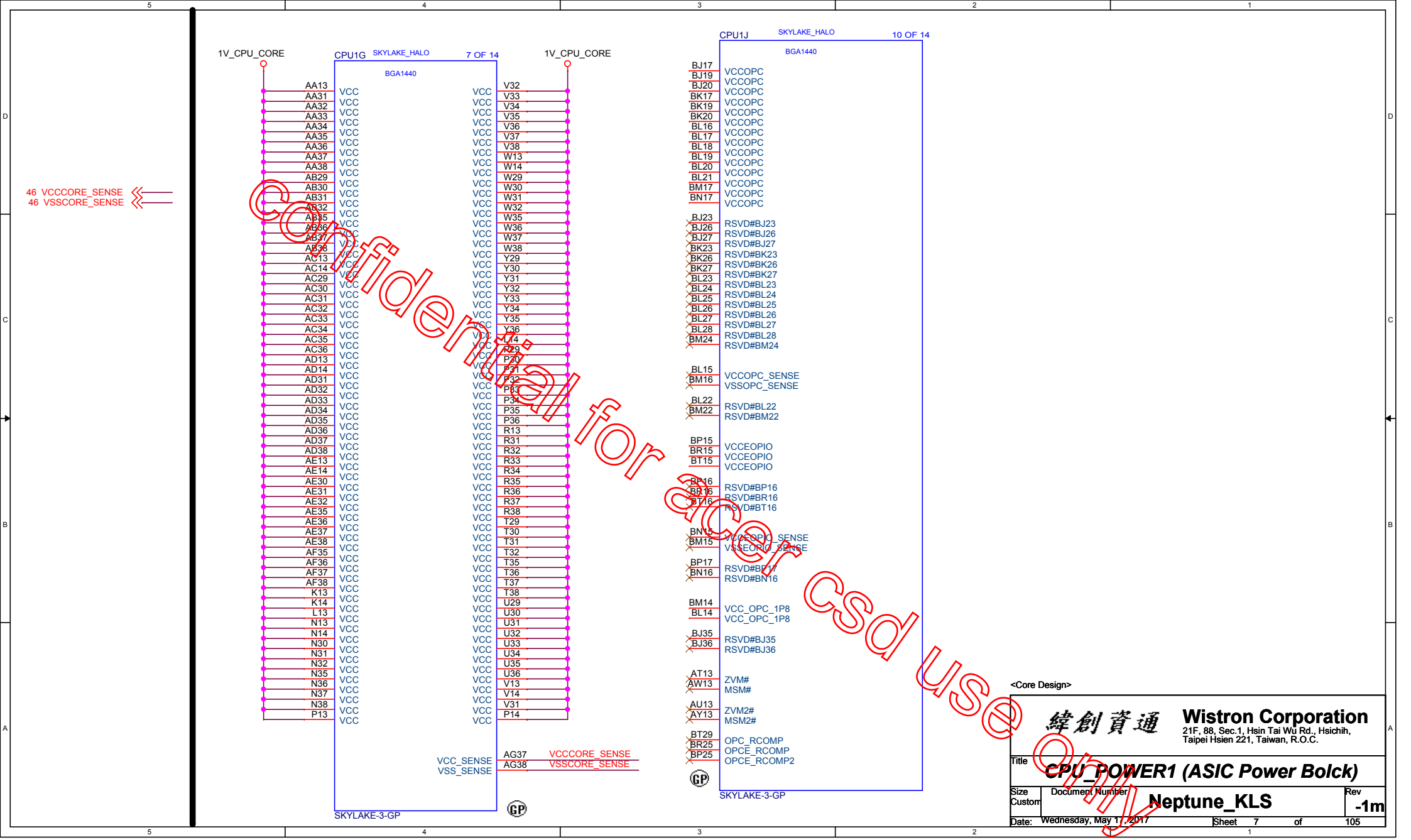
1V_CPU_CORE
CPU1G SKYLAKE_HALO 7 OF 14
BGA1440
1V_CPU_CORE
CPU1J SKYLAKE_HALO 10 OF 14
BGA1440
46 VCCCORE_SENSE
46 VSSCORE_SENSE
VCC_SENSE
VSS_SENSE
VCCCORE_SENSE
VSSCORE_SENSE
SKYLAKE-3-GP
SKYLAKE-3-GP
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Title
CPU_POWER1 (ASIC Power Bolck)
Size
Custom
Document Number
Neptune_KLS
Rev
-1m
Date: Wednesday, May 17, 2017
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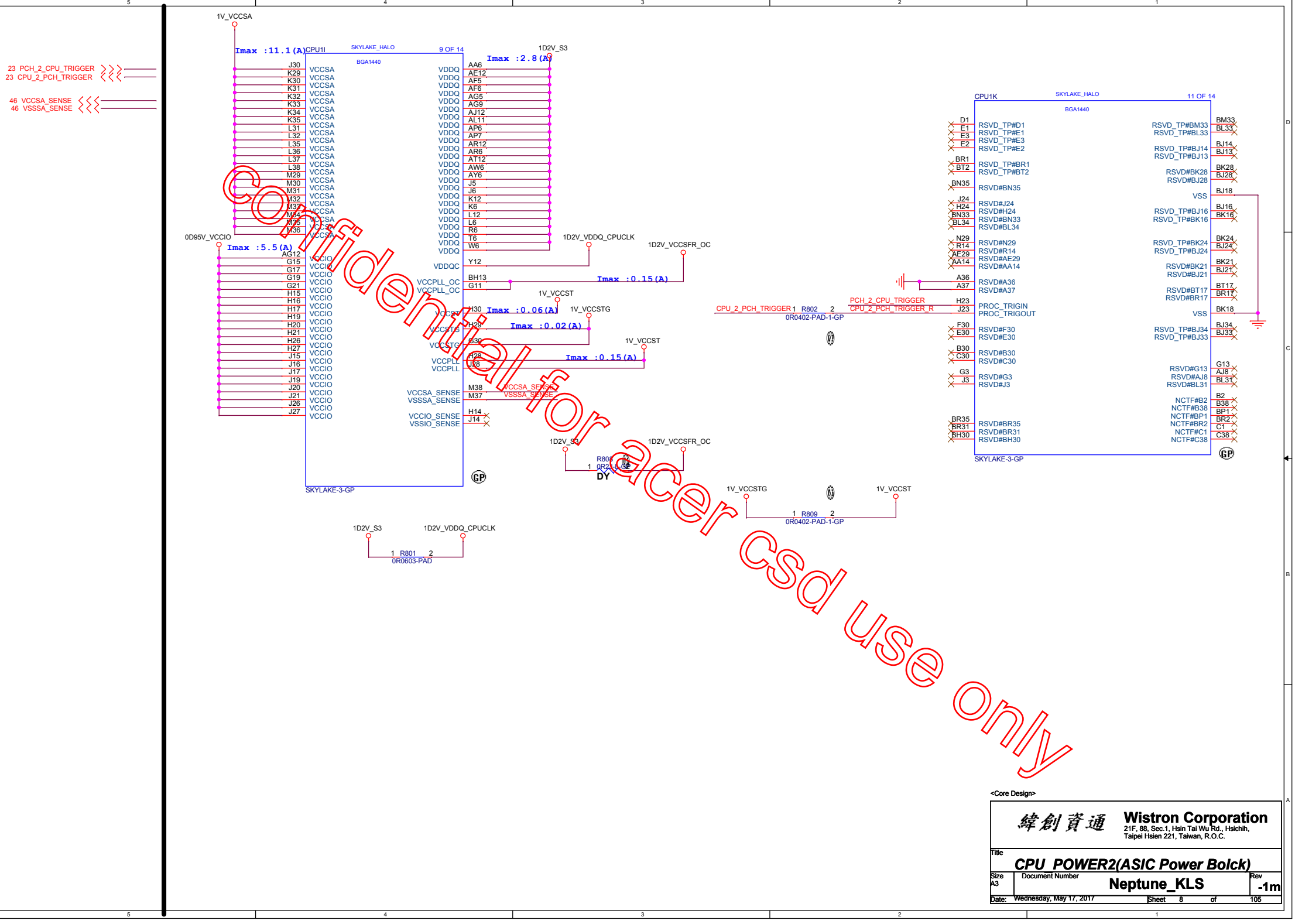
23 PCH_2_CPU_TRIGGER
23 CPU_2_PCH_TRIGGER
46 VCCSA_SENSE
46 VSSSA_SENSE
1V_VCCSA
Imax :11.1(A)
CPU1I
SKYLAKE_HALO
BGA1440
9 OF 14
SKYLAKE-3-GP
1D2V_S3
Imax :2.8(A)
0D95V_VCCIO
Imax :5.5(A)
1D2V_VDDQ_CPUCLK
1D2V_VCCSFR_OC
Imax :0.15(A)
1V_VCCST
1V_VCCSTG
Imax :0.06(A)
Imax :0.02(A)
VCCSA_SENSE
VSSSA_SENSE
R801
0R0603-PAD
R802
0R0402-PAD-1-GP
R809
CPU_2_PCH_TRIGGER_R
PCH_2_CPU_TRIGGER
DY
CPU1K
11 OF 14
PROC_TRIGIN
PROC_TRIGOUT
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Title
CPU_POWER2(ASIC Power Bolck)
Size A3
Document Number
Neptune_KLS
Rev -1m
Date: Wednesday, May 17, 2017
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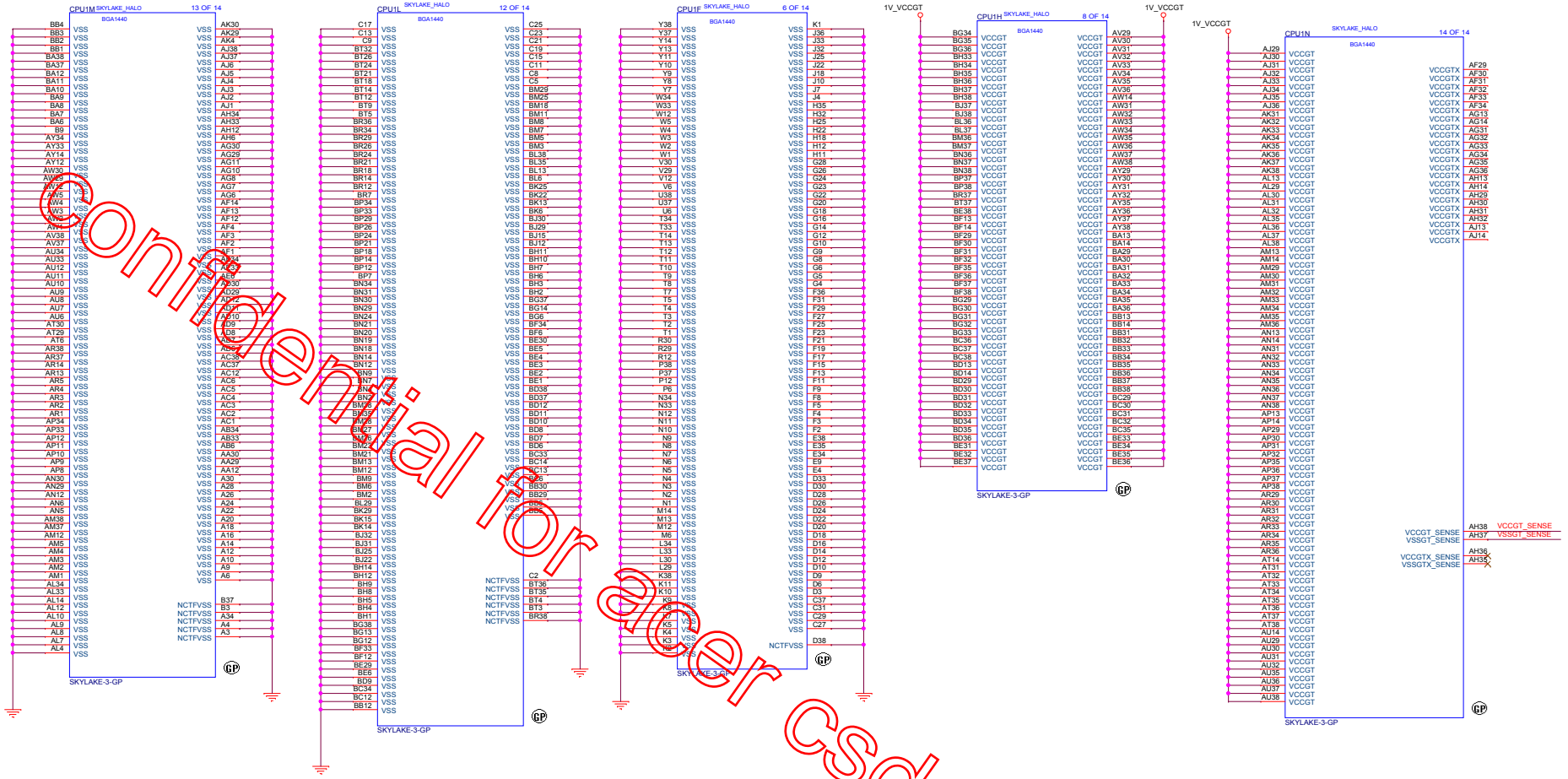
SSID = CPU



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Title: CPU_POWER3(ASIC Power Bolck)

Size: Custom | Document Number: Neptune_KLS | Rev: -1m

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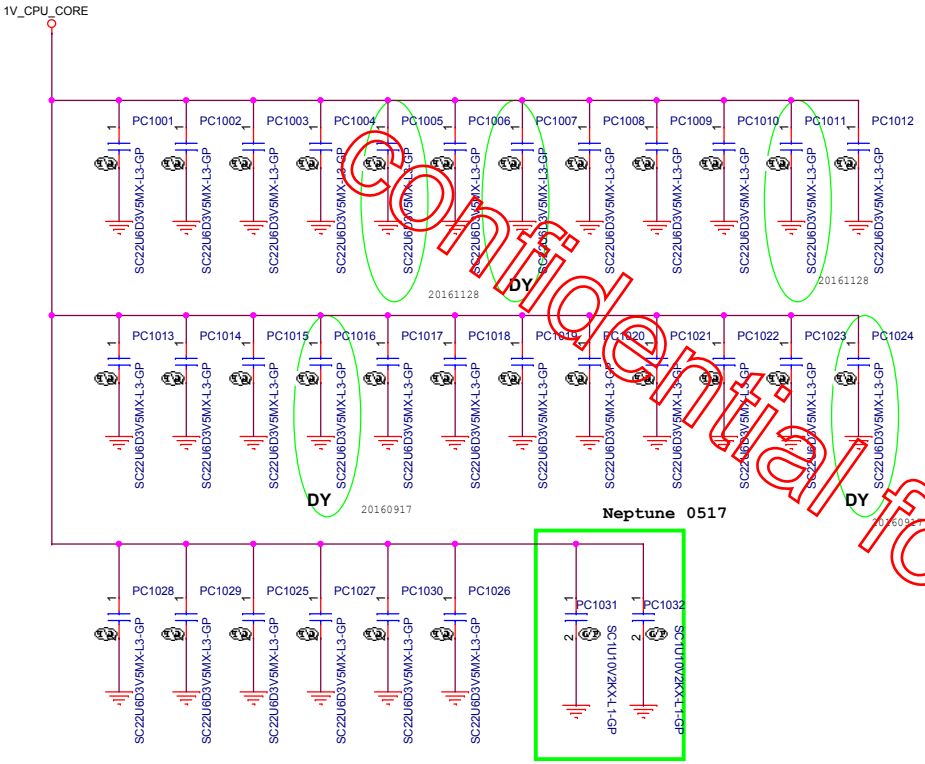
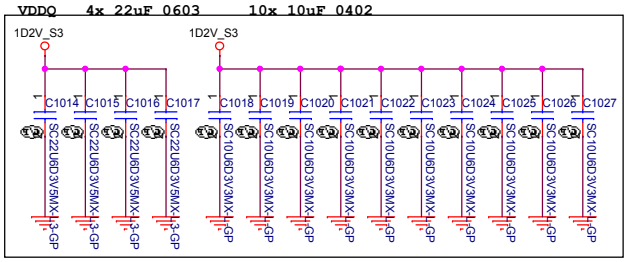
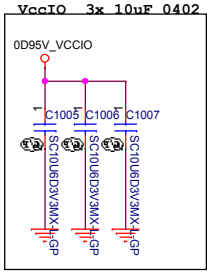
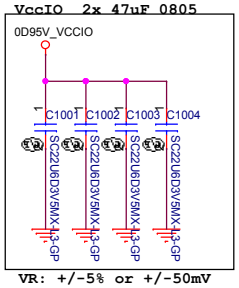
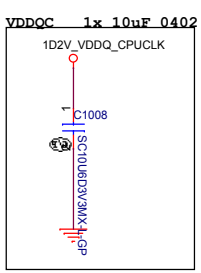
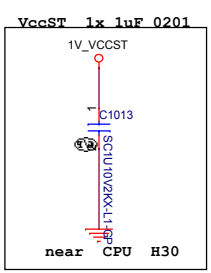




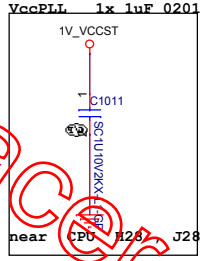


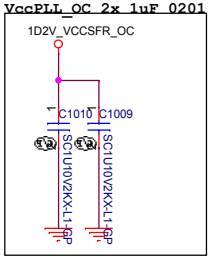






VR: +/-5% or +/-50mV
Place close to VR output





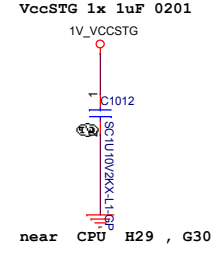


Table 49-3. Decoupling Requirements for KBL H Processor

Domain	Board Edge cap	Backside cap	Notes
Vcc	4x 47uF 0805		
		8x 22uF 0603	
		28x 10uF 0402	
		63x 1uF 0201	
Vcc_{GT}	6x 47uF 0805		
		8x 22uF 0603	
		35x 10uF 0402	
		68x 1uF 0201	
Vcc_{GTx}	8x 22uF 0603		Only needed when supporting 44e
		4x 10uF 0402	Only needed when supporting 44e
		12x 1uF 0201	Only needed when supporting 44e
Vcc_{SA}	1x 47uF 0805		
		1x 47uF 0805	
		7x 10uF 0402	
		3x 1uF 0201	
V_{DDQ}		4x 22uF 0603	
		10x 10uF 0402	
V_{DDQC}		1x 10uF 0402	
Vcc_{IO}		3x 10uF 0402	
Vcc_{ST}		1x 1uF 0201	Do not route Vcc_{GT} closest adjacent layer over any power net other than ground.
Vcc_{STG}		1x 1uF 0201	Share supply with 1.0V PCH rail
Vcc_{PLL}		1x 1uF 0201	Do not route Vcc_{PLL}, Vcc_{STG} closest adjacent layer over any power net other than ground.
Vcc_{PLL_OC}		2x 1uF 0201	Share with VDDQ. Do not route Vcc_{PLL_OC} closest adjacent layer over any power net other than ground.
Vcc_{OPC}		10x 10uF 0402	Only needed when supporting 44e VR: +/-5% or +/-50mV
Vcc_{EOPIO}		3x 10uF 0402	Only needed when supporting 44e VR: +/-5% or +/-50mV

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Title: 010_CPU (Power CAP1)

Size: A3 | Document Number: Neptune_KLS | Rev: -1m

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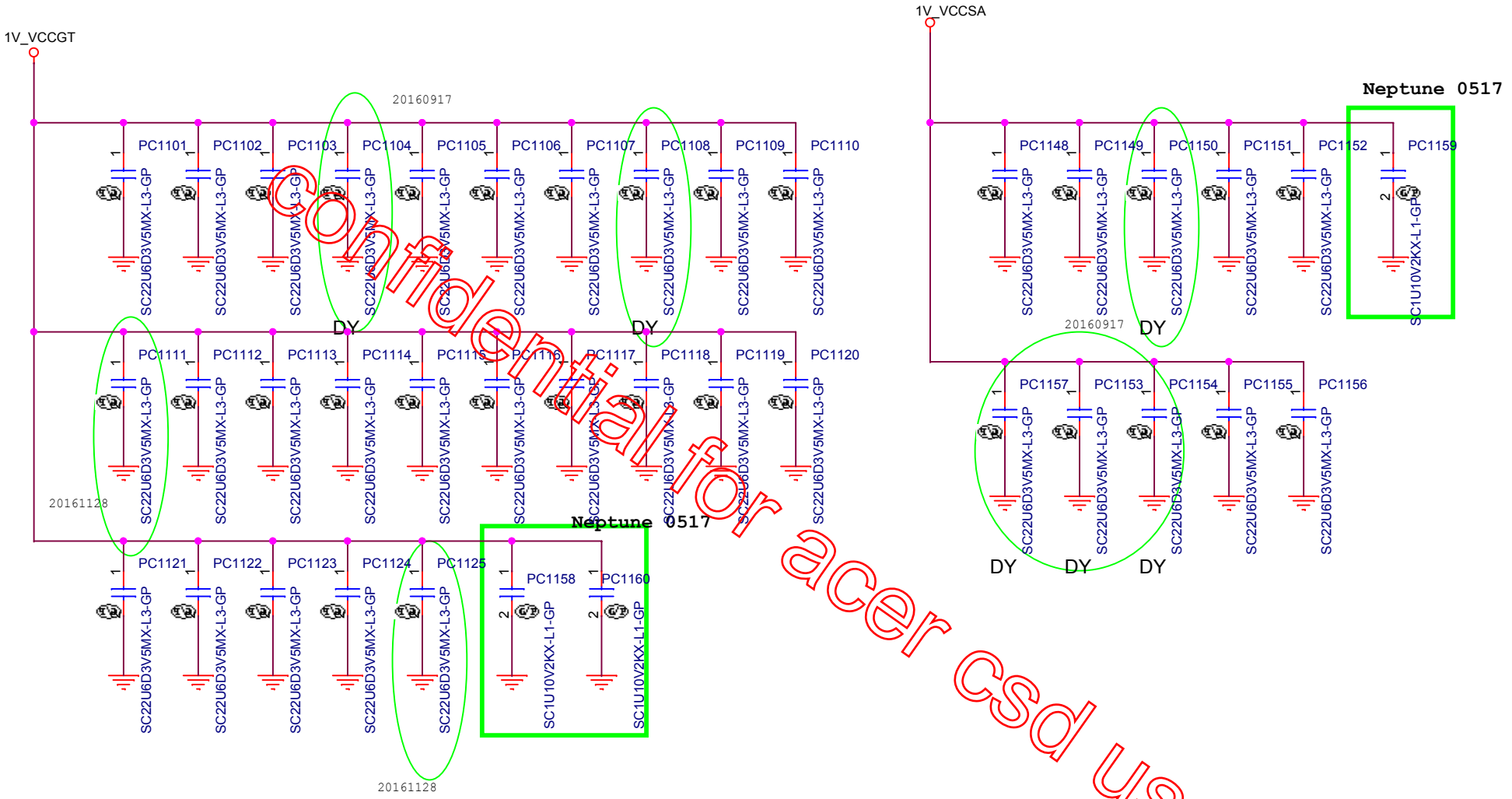

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Title: CPU (Power CAP2)

Size: A4 | Document Number: Neptune_KLS | Rev: -1m

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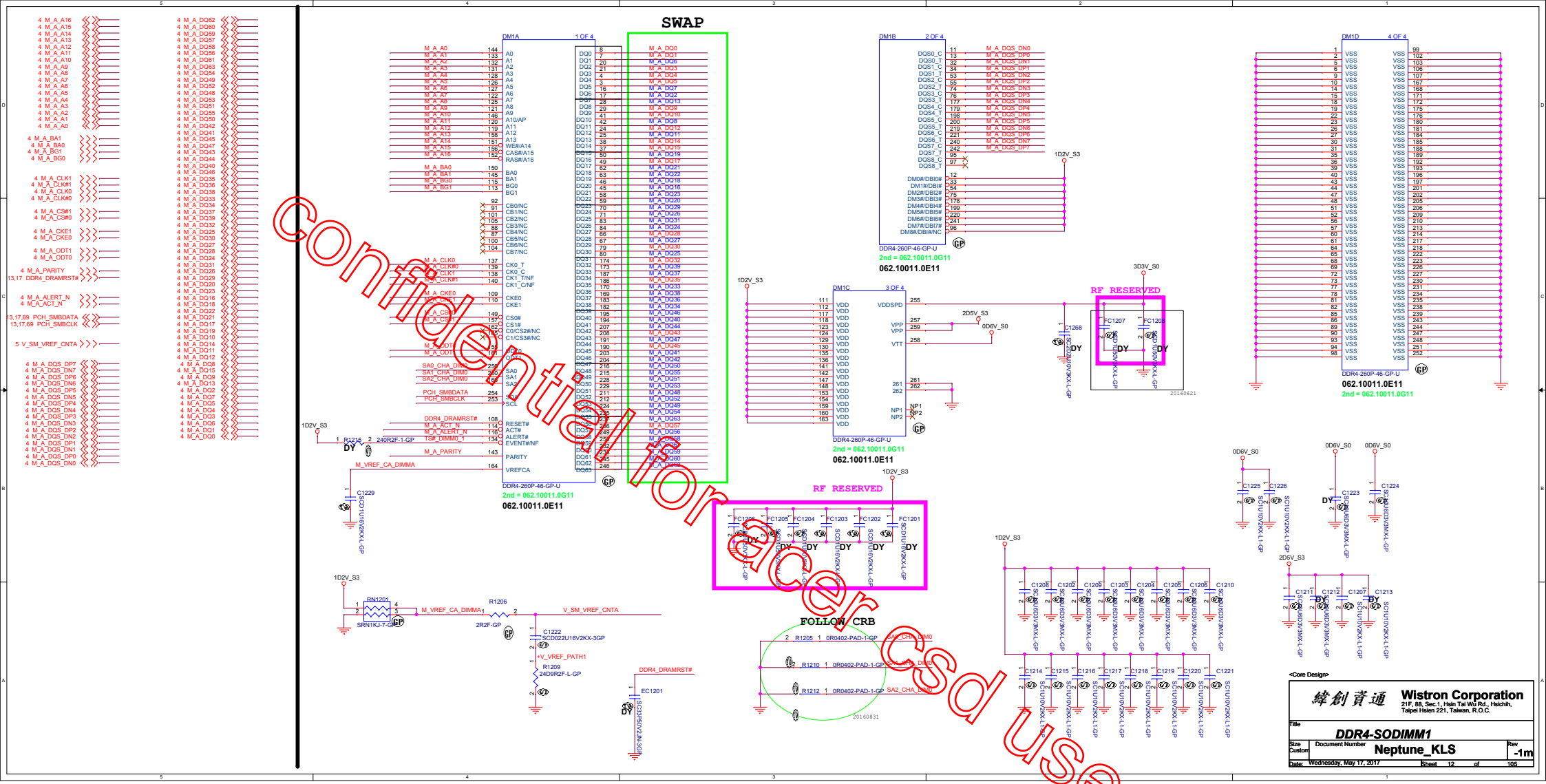

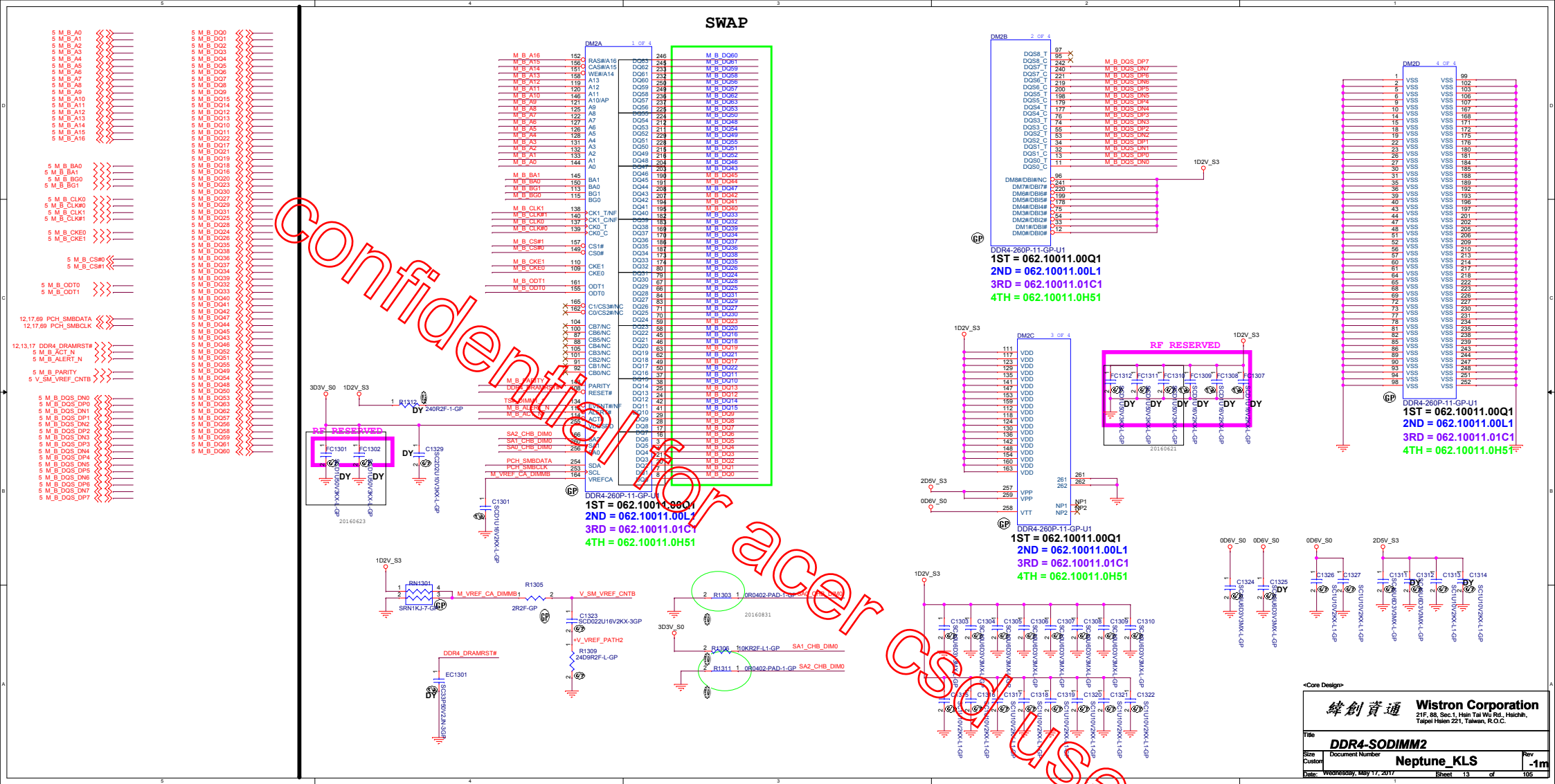
SWAP
DM2A
DM2B
DM2C
DM2D
DDR4-260P-11-GP-U1
1ST = 062.10011.00Q1
2ND = 062.10011.00L1
3RD = 062.10011.01C1
4TH = 062.10011.0H51
RF RESERVED
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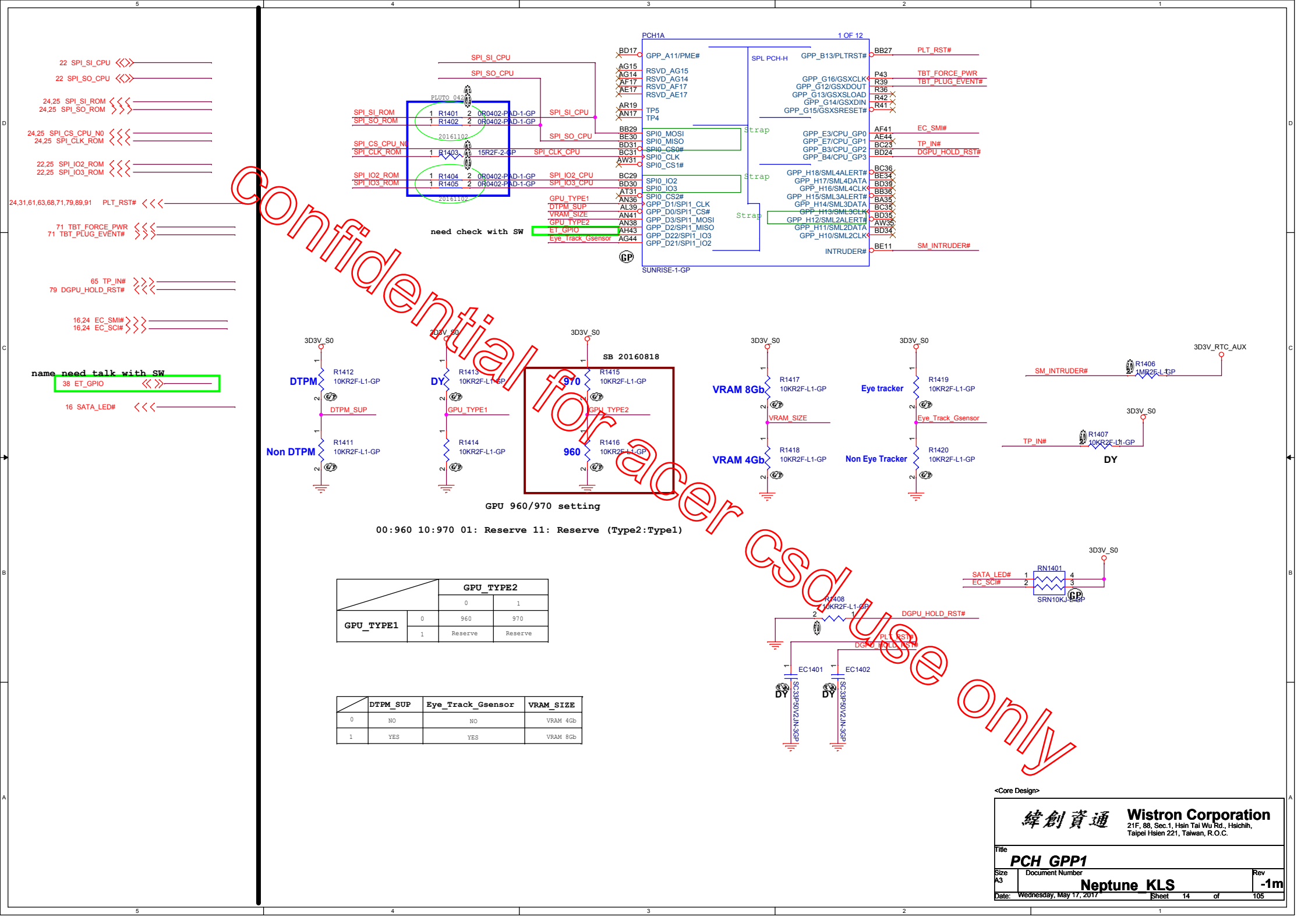

	GPU_TYPE2	
	0	1
GPU_TYPE1 0	960	970
GPU_TYPE1 1	Reserve	Reserve

	DTPM_SUP	Eye_Track_Gsensor	VRAM_SIZE
0	NO	NO	VRAM 4Gb
1	YES	YES	VRAM 8Gb

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Title: PCH_GPP1

Size: A3 | Document Number: Neptune_KLS | Rev: -1m

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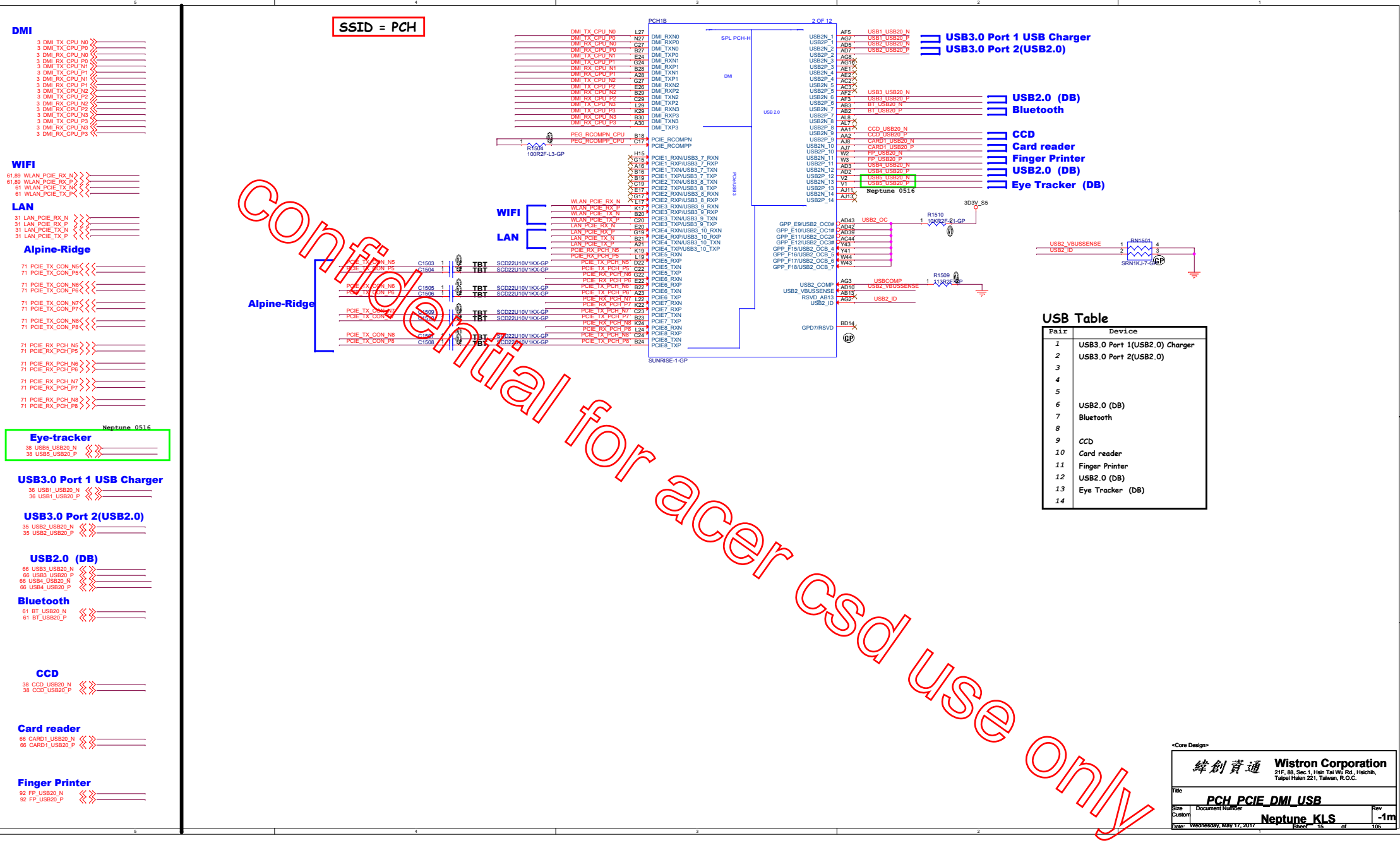
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DMI
WIFI
LAN
Alpine-Ridge
Neptune 0516
Eye-tracker
USB3.0 Port 1 USB Charger
USB3.0 Port 2(USB2.0)
USB2.0 (DB)
Bluetooth
CCD
Card reader
Finger Printer
USB2.0 (DB)
Eye Tracker (DB)
PCH1B
2 OF 12
SUNRISE-1-GP
USB Table
Pair
Device
1 USB3.0 Port 1(USB2.0) Charger
2 USB3.0 Port 2(USB2.0)
6 USB2.0 (DB)
7 Bluetooth
9 CCD
10 Card reader
11 Finger Printer
12 USB2.0 (DB)
13 Eye Tracker (DB)
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PCH_PCIE_DMI_USB
Neptune_KLS
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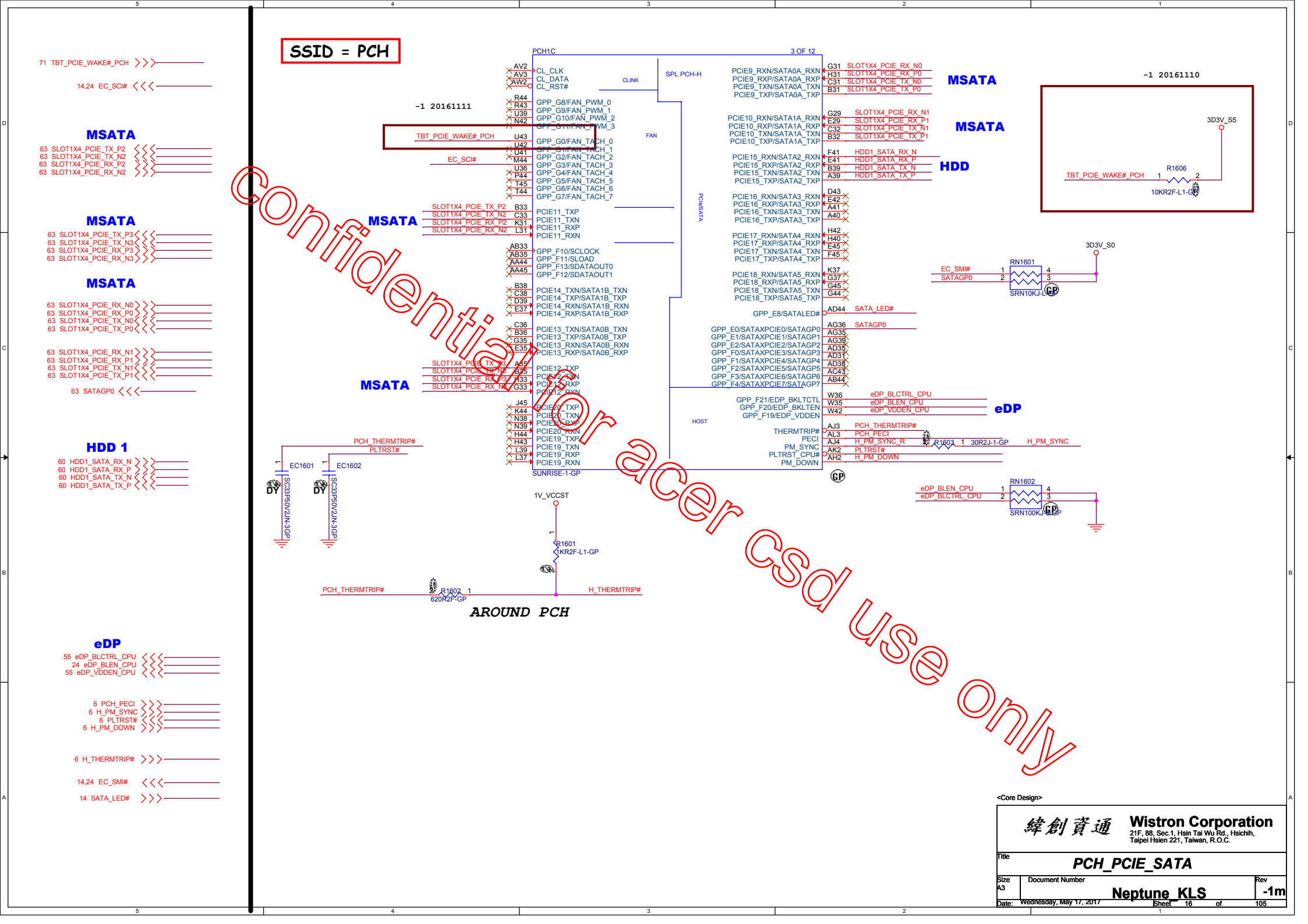
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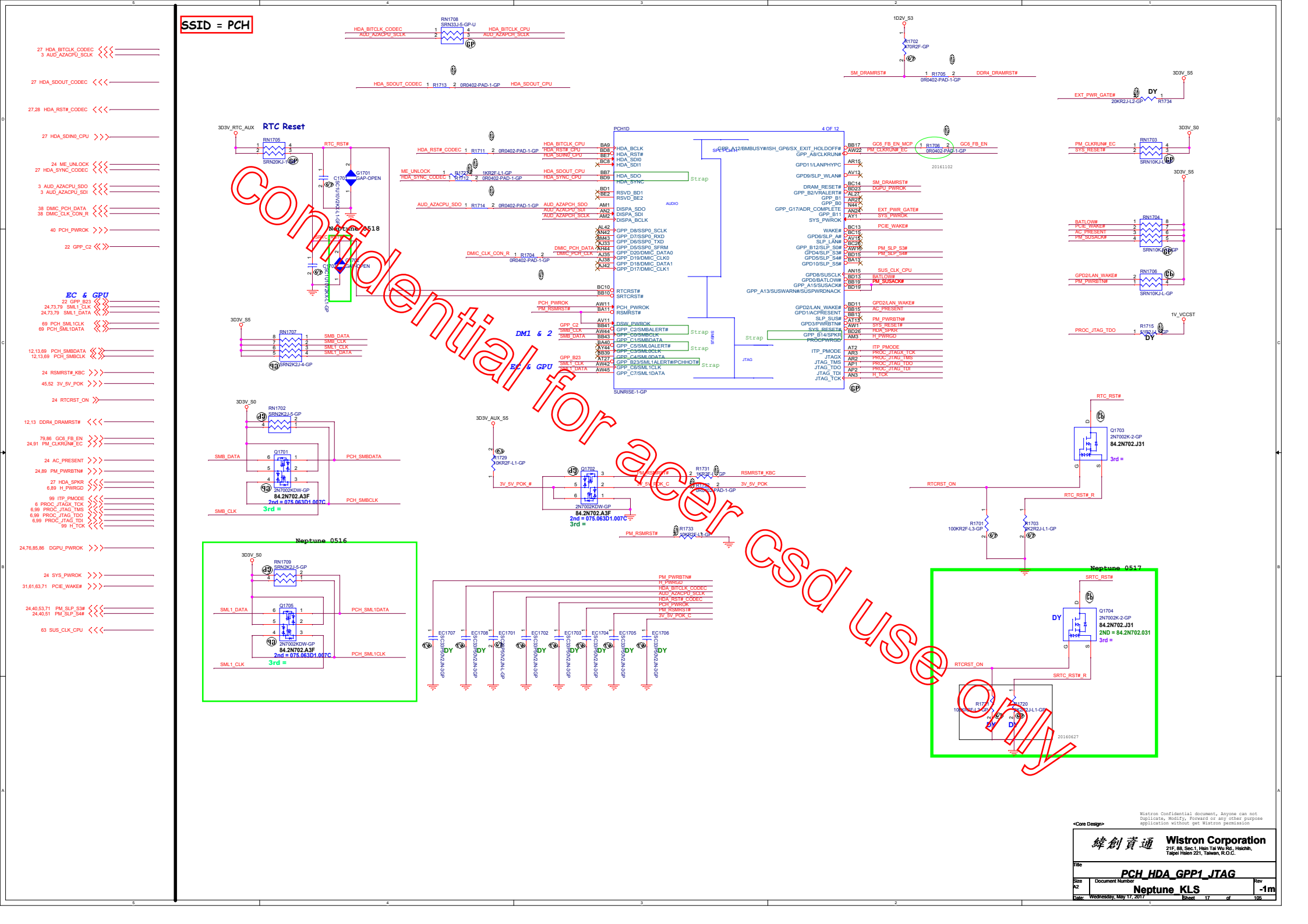
71 TBT_PCIE_WAKE#_PCH
14,24 EC_SCI#
MSATA
63 SLOT1X4_PCIE_TX_P2
63 SLOT1X4_PCIE_TX_N2
63 SLOT1X4_PCIE_RX_P2
63 SLOT1X4_PCIE_RX_N2
MSATA
63 SLOT1X4_PCIE_TX_P3
63 SLOT1X4_PCIE_TX_N3
63 SLOT1X4_PCIE_RX_P3
63 SLOT1X4_PCIE_RX_N3
MSATA
63 SLOT1X4_PCIE_RX_N0
63 SLOT1X4_PCIE_RX_P0
63 SLOT1X4_PCIE_TX_N0
63 SLOT1X4_PCIE_TX_P0
63 SLOT1X4_PCIE_RX_N1
63 SLOT1X4_PCIE_RX_P1
63 SLOT1X4_PCIE_TX_N1
63 SLOT1X4_PCIE_TX_P1
63 SATAGP0
HDD 1
60 HDD1_SATA_RX_N
60 HDD1_SATA_RX_P
60 HDD1_SATA_TX_N
60 HDD1_SATA_TX_P
eDP
55 eDP_BLCTRL_CPU
24 eDP_BLEN_CPU
55 eDP_VDDEN_CPU
6 PCH_PECI
6 H_PM_SYNC
6 PLTRST#
6 H_PM_DOWN
6 H_THERMTRIP#
14,24 EC_SMI#
14 SATA_LED#
PCH1C
3 OF 12
SUNRISE-1-GP
CLINK
SPL PCH-H
FAN
PCIe/SATA
HOST
-1 20161111
TBT_PCIE_WAKE#_PCH
EC_SCI#
MSATA
MSATA
MSATA
MSATA
HDD
eDP
-1 20161110
3D3V_S5
R1606
10KR2F-L1-GP
3D3V_S0
RN1601
SRN10KJ-L-GP
EC_SMI#
SATAGP0
RN1602
SRN100KJ-GP
eDP_BLEN_CPU
eDP_BLCTRL_CPU
PCH_THERMTRIP#
PLTRST#
EC1601
EC1602
SC33P50V2JN-3GP
1V_VCCST
R1601
1KR2F-L1-GP
R1602
620R2F-GP
H_THERMTRIP#
R1603
30R2J-1-GP
H_PM_SYNC
AROUND PCH
Confidential for acer csd use only
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH_PCIE_SATA
Size
A3
Document Number
Neptune_KLS
Rev
-1m
Date: Wednesday, May 17, 2017
Sheet 16 of 105

SSID = PCH



<Core Design>

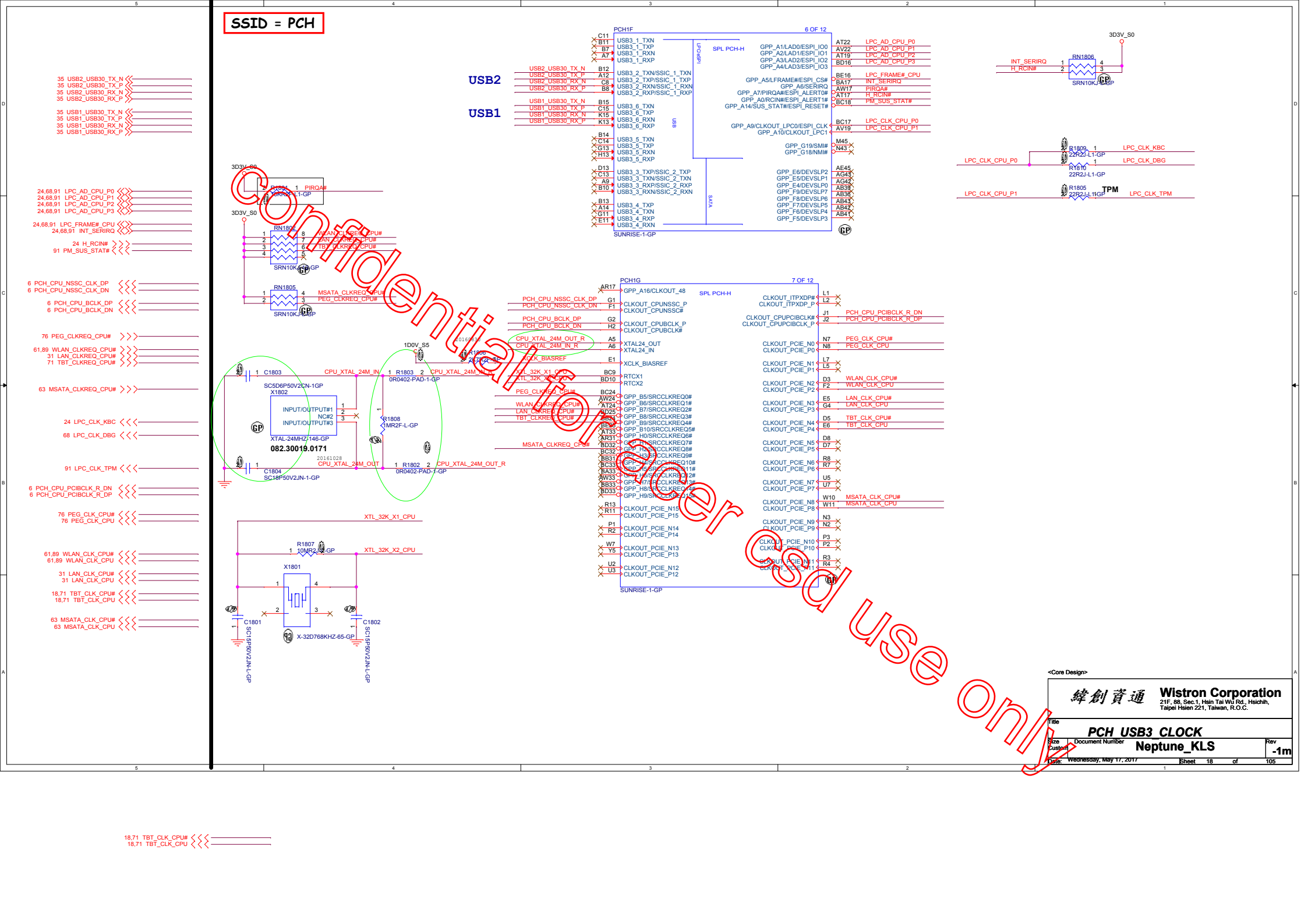
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_HDA_GPP1_JTAG

Size: A2 | Document Number: Neptune_KLS | Rev: -1m

Date: Wednesday, May 17, 2017 | Sheet 17 of 105

SSID = PCH



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	PCH_USB3_CLOCK
Size: Custom	Document Number: Neptune_KLS
Rev: -1m	
Date: Wednesday, May 17, 2017	Sheet 18 of 105

SSID = PCH

71 DDI1_TBT_HPD_CPU
71 DDI2_TBT_HPD_CPU

55 eDP_HPD_CPU
65 KB_BL_DET

22 DDI2_TBT_DATA_CPU
71 DDI1_TBT_CLK_CPU
71 DDI1_TBT_DATA_CPU

22 DDPD_DATA_CPU

22 GPP_B22/GSPI1_MOSI
86 DGPU_PWR_EN#

25 RTC_DET#

22 GPP_B18/GSPI0_MOSI
79 GPU_EVENT#

61,89 BLUETOOTH_EN
61 WIFI_RF_EN

TOUCH PAD

65 I2C1_CLK_CPU
65 I2C1_DATA_CPU

Neptune 0516
G-sensor

24 I2C2_CLK_CPU
24 I2C2_DATA_CPU
24,38,69 EYETRACKER_INT#

57 I2C0_CLK_CPU_TIMER
57 I2C0_DATA_CPU_TIMER

69 GSENSOR_INT#

68 LPSS_UART2_TXD
68 LPSS_UART2_RXD

57 VR_HDMI_DET

check

PCH1E 5 OF 12
SPL PCH-H
SUNRISE-1-GP

DDI1_TBT_HPD_CPU AW4
DDI2_TBT_HPD_CPU AY2
GPP_I0/DDPB_HPD0
GPP_I1/DDPC_HPD1
GPP_I2/DDPD_HPD2
GPP_I3/DDPE_HPD3
AV4
BA4

eDP_HPD_CPU BD7
GPP_I4/EDP_HPD

Strap GPP_I7/DDPC_CTRLCLK BB3
GPP_I8/DDPC_CTRLDATA BD6
Strap GPP_I5/DDPB_CTRLCLK BA5
GPP_I6/DDPB_CTRLDATA BC4
Strap GPP_I9/DDPD_CTRLCLK BE5
GPP_I10/DDPD_CTRLDATA BE6

DDI2_TBT_DATA_CPU
DDI1_TBT_CLK_CPU
DDI1_TBT_DATA_CPU
DDPD_DATA_CPU

GPP_F14 Y44
GPP_F23 V44
GPP_F22 W39
VR_HDMI_DET
TPM_TYPE
KB_BL_DET

GPP_G23 L43
GPP_G22 L44
GPP_G21 U35
GPP_G20 R35
GPP_H23 BD36
WIFI_RF_EN
BLUETOOTH_EN

20160816

3D3V_S0
PSW_CLR# 1 R1906 2 10KR2F-L1-GP

-1 20161025

-1 20161026

3D3V_S0
TPM2.0 R1907 10KR2F-L1-GP
TPM_TYPE
TPM1.2 R1911 10KR2F-L1-GP

1 R1904 2 10KR2F-L1-GP DGPU_PWR_EN#
1 R1905 2 10KR2F-L1-GP VR_HDMI_DET
Non-W
20160701

PSW_CLR#
Pass Word Clear
G1901
GAP-OPEN

3D3V_S5
RN1904 SRN10KJ-5-GP
RTC_DET#
GPU_EVENT#

PCH1K 11 OF 12
SPL PCH-H
SUNRISE-1-GP

GPP_B22/GSPI1_MOSI AT29
DGPU_PWR_EN# AR29
PSW_CLR# AV29
RTC_DET# BC27
GPP_B18/GSPI0_MOSI BD28
GPU_EVENT# BD27
AW27
AR24

Strap GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B20/GSPI1_CLK
GPP_B19/GSPI1_CS#
Strap GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B16/GSPI0_CLK
GPP_B15/GSPI0_CS#

GPP_C9/UART0_TXD AV44
GPP_C8/UART0_RXD BA41
GPP_C7/UART0_CTS# AU44
GPP_C6/UART0_RTS# AV43

GPP_C15/UART1_CTS#/ISH_UART1_CTS# AU41
GPP_C14/UART1_RTS#/ISH_UART1_RTS# AT44
GPP_C13/UART1_TXD/ISH_UART1_TXD AT43
GPP_C12/UART1_RXD/ISH_UART1_RXD AU43

LPSS_UART2_CTS# AN43
LPSS_UART2_RTS# AN44
LPSS_UART2_TXD AR39
LPSS_UART2_RXD AR45
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD

I2C1_CLK_CPU AR41
I2C1_DATA_CPU AR44
I2C0_CLK_CPU AR38
I2C0_DATA_CPU AT42
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA

AM44 GPP_D4/ISH_I2C2_SDA
AJ44 GPP_D23/ISH_I2C2_SCL

GPP_D9 AL44
GPP_D10 AL36
GPP_D11 AL35
GPP_D12 AJ39
HDD_Gsensor
EYETRACKER_INT#
1 TP1901

GPP_D16/ISH_UART0_CTS# AJ43
GPP_D15/ISH_UART0_RTS# AL43
GPP_D14/ISH_UART0_TXD AK44
GPP_D13/ISH_UART0_RXD AK45
I2C2_CLK_CPU
I2C2_DATA_CPU

Neptune 0516
G-sensor

GPP_H20/ISH_I2C0_SCL BC38
GPP_H19/ISH_I2C0_SDA BB38
GPP_H22/ISH_I2C1_SCL BD38
GPP_H21/ISH_I2C1_SDA BE39

GPP_A23/ISH_GP5 BC22
GPP_A22/ISH_GP4 BD18
GPP_A21/ISH_GP3 BE21
GPP_A20/ISH_GP2 BD22
GPP_A19/ISH_GP1 BD21
GPP_A18/ISH_GP0 BB22
GPP_A17/ISH_GP7 BC19
GSENSOR_INT#

Neptune 0516
3D3V_S0
RN1902 SRN2K2J-5-GP
I2C2_DATA_CPU
I2C2_CLK_CPU

3D3V_S0
RN1901 SRN2K2J-5-GP
I2C1_DATA_CPU
I2C1_CLK_CPU
20160628

TOUCH PAD
HDMI re-timer(TMDS181)

I2C0_CLK_CPU_TIMER 1 R1901 0R2J-L-GP DY
I2C0_DATA_CPU_TIMER 1 R1902 0R2J-L-GP DY

3D3V_S0
R1903 1 2 49K9R2F-L-GP LPSS_UART2_CTS#
R1908 1 2 49K9R2F-L-GP LPSS_UART2_RTS#
R1909 1 2 49K9R2F-L-GP LPSS_UART2_TXD
R1910 1 2 49K9R2F-L-GP LPSS_UART2_RXD

Neptune 0517
3D3V_S0
R1914 10KR2F-L1-GP
HDD G sensor
HDD_Gsensor
R1913 10KR2F-L-GP
Non HDD Gensor

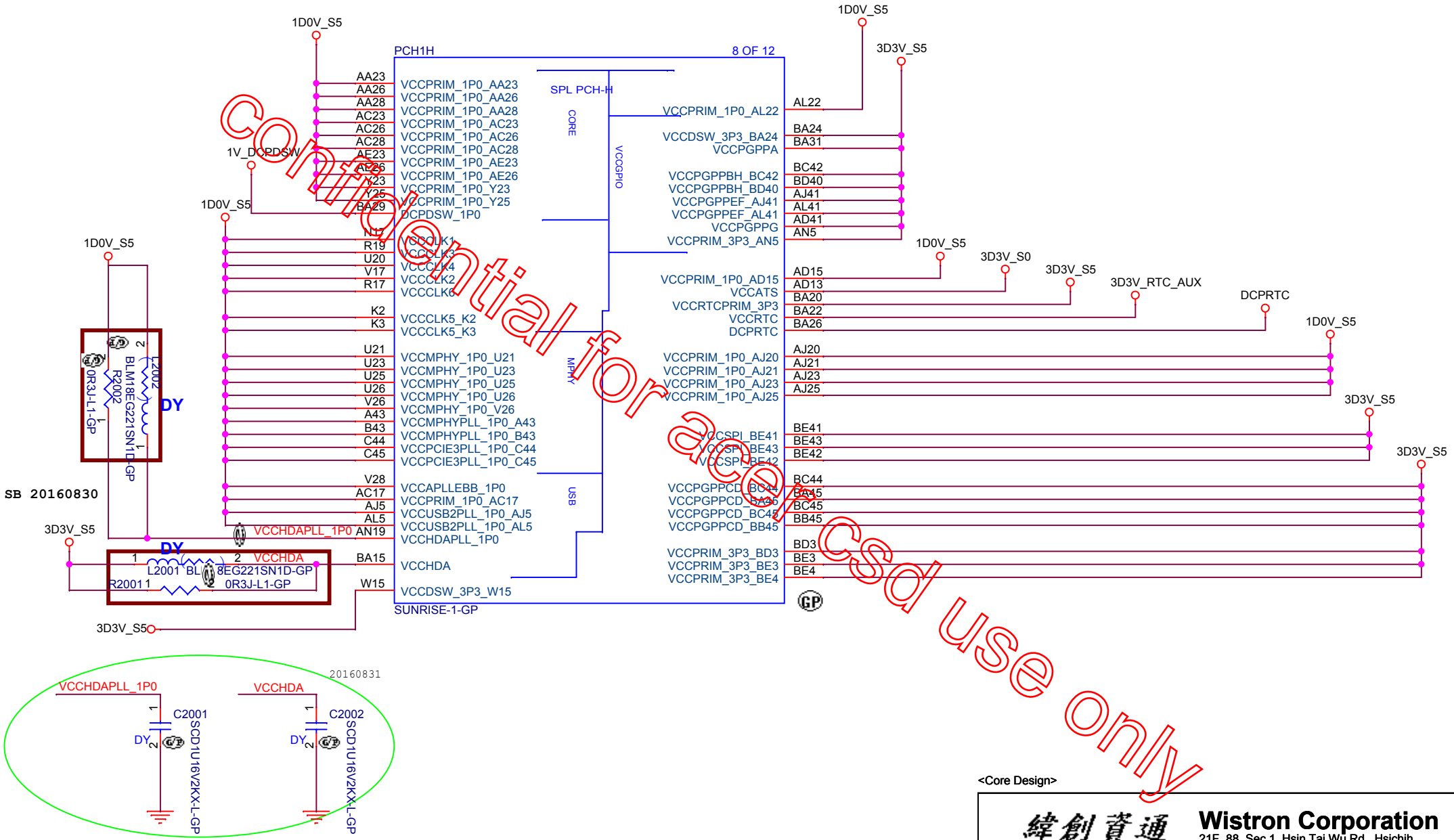
1 Support
0 no support

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_GPP2_GPP3
Size: Custom
Document Number: Neptune_KLS
Rev: -1m
Date: Wednesday, May 17, 2017
Sheet 19 of 105

SSID = PCH



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

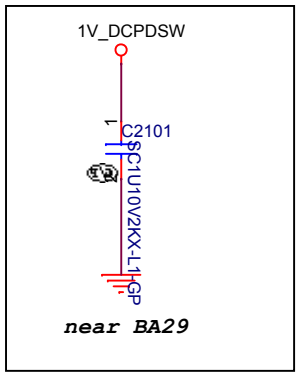
Title: PCH_POWER_VCCPRIM_VCCMPHY

Size	Document Number	Rev
A4	Neptune_KLS	-1m

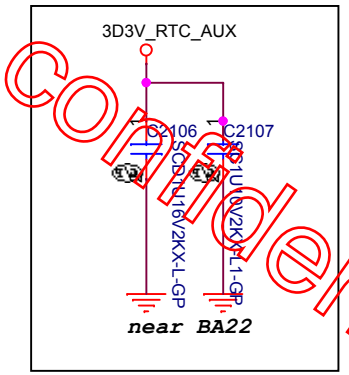
Date: Wednesday, May 17, 2017 Sheet 20 of 105

SSID = PCH

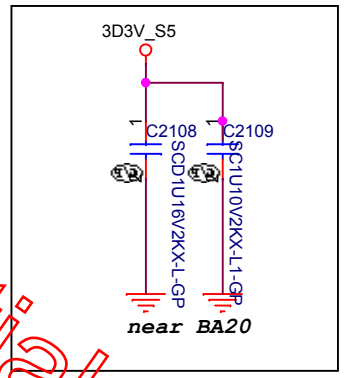
DcpDSW
1x 1uF



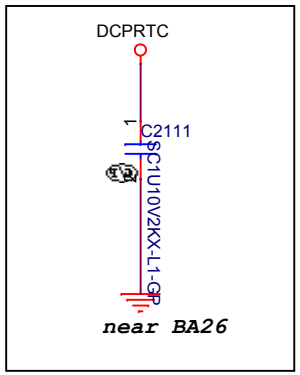
VccRTC
1x1 uF 1x0.1 uF



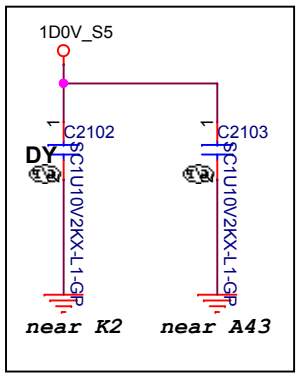
VccRTCPRIM
1x1 uF 1x0.1 uF



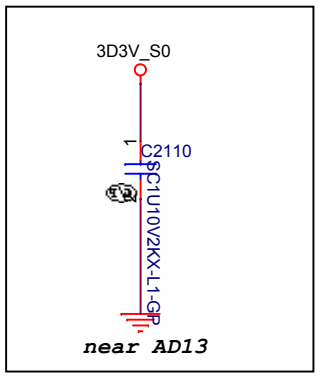
DcpRTC
1x 0.1uF



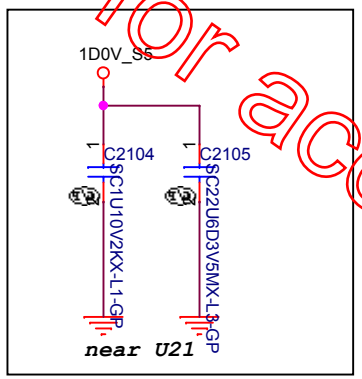
VccMPHYPLL / VccPCIE3PLL
1x1 uF



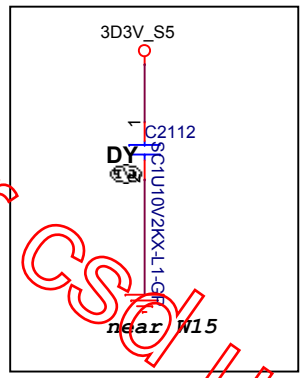
VccATS
1x1 uF



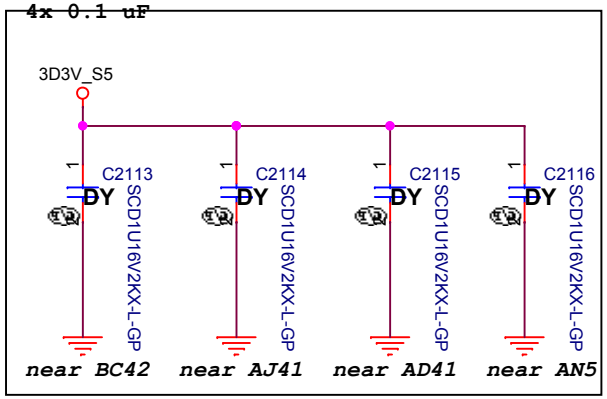
VccMPHY / VccPRIM / VccAPLLEBB
1x1 uF 1x22 uF



VccDSW
1x 1uF



VccPGPPBCH / VccPGPPEF / VccPGPPG / VccPRIM
4x 0.1 uF



Decoupling and Power Connection Requirements for SKL S/H PCH (DT / AIO) (Sheet 1 of 2)

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)umney / (E)dge	Place capacitor(s) near ball(s)
V1.0A	VccMPHY VccPRIM VccAPLLEBB	U21, U23, U25, U26, V26, AC17, V28	1 uF	0402	1	E (<3 mm)	U21
			22 uF	0805	1	E (<5 mm)	
	VccMPHYPLL VccPCIE3PLL	A43, B43, C44, C45	1 uF	0402	1	E (<5 mm)	A43
	VccCLK5	K2, K3	1 uF	0402	1	E (<5 mm)	K2 (Note 1)
	VccCLK (1,2,3,4,6)	N17, R19, U20, V17, R17	-	-	-	-	-
	VccUSB2PLL VccHDAPLL	AJ5, AL5, AN19	-	-	-	-	-
	VccPRIM	AL22	-	-	-	-	-
	VccPRIM	AD15	-	-	-	-	-
	VccPRIM	AJ20, AJ21, AJ23, AJ25	-	-	-	-	-
	VccPRIM	AA23, AA26, AA28, AC23, AC26, AC28, AE23, AE26, Y23, Y25	-	-	-	-	-
V1.0DSW	DcpDSW	BA29	1 uF	0402	1	E (<5 mm)	BA29
V1.8A/ V3.3A	VccPGPPBCH	BC42, BD40	0.1 uF	0402	1	E (<3 mm)	BC42 (Note 1)
	VccPGPPEF	AJ41, AL41	0.1 uF	0402	1	E (<3 mm)	AJ41 (Note 1)
	VccPGPPG	AD41	0.1 uF	0402	1	E (<3 mm)	AD41 (Note 1)
	VccPRIM	AN5	0.1 uF	0402	1	E (<3 mm)	AN5 (Note 1)
	VccPGPPA	BA31	-	-	-	-	-
	VccSPI	BE41, BE42, BE43	-	-	-	-	-
	VccPGPPD	BC44, BA45, BC45, BB45	-	-	-	-	-
V1.8A/ V1.8S/ V3.3S	VccATS	AD13	1 uF	0402	1	E (<5 mm)	AD13
V1.5A/ V1.8A/ V3.3A	VccHDA	BA15	-	-	-	-	-
V3.3A	VccRTCPRIM	BA20	1 uF	0402	1	E (<5 mm)	BA20
			0.1 uF	0402	1	E (<3 mm)	
	VccPRIM	BD3, BE3, BE4	-	-	-	-	-
V3.3RTC	VccRTC	BA22	1 uF	0402	1	E (<5 mm)	BA22
			0.1 uF	0402	1	E (<3 mm)	
V3.3DSW	VccDSW	W15	1 uF	0401	1	E (<3 mm)	W15 (Note 1)
	VccDSW	BA24	-	-	-	-	-
PCH Internal VRM	DcpRTC	BA26	0.1 uF	0402	1	E (<5 mm)	BA26

<Core Design>

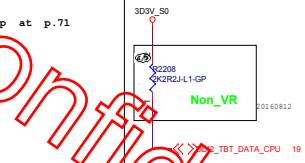
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

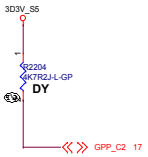
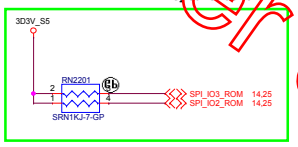
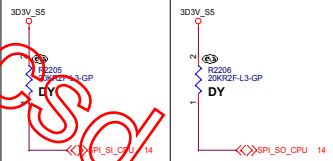
Title: **PCH_POWER_CAP1**

Size: A4 | Document Number: **Neptune_KLS** | Rev: **-1m**

Date: Wednesday, May 17, 2017 | Sheet 21 of 105

SSID = PCH

Description	Display Port B Detected	Display Port C Detected	Display Port D Detected	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	ESPI FLASH SHARING MODE
GPIO	GPP_I6	GPP_I8	GPP_I10	GPP_B18	GPP_B22	HDA_SDO	GPP_H12
Schematic							
High	Detected	Detected	Detected	Enable	LPC	Disable	1:SLAVE ATTACEHD FLASH SHARING ESPI FLASH SHARING MODE
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	0: MASTER ATTACHED FLASH SHARING
	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	eSPI or LPC	TLS Confi-dentiality	Reserved	Reserved	Reserved	Reserved	Reserved
GPIO	GPP_B14	GPP_C5	GPP_C2	SPI0_IO3	SPI0_IO2	SPI0_MOSI	SPI0_MISO	GPP_B23 / PCHHOT#
Schematic								
High	Enable	eSPI	Enable					
Low	Disable	LPC	Disable					
	internal pull-down	internal pull-down	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-up	internal pull-down

[H,S,U,Y] Pull-up Resistors on SPI_IO2 and SPI_IO3 Requirement Update

The current Skylake Platform Design Guide (PDG) states that a 1 K pull-up resistor is required on the PCH SPI_IO2 and SPI_IO3 signals.

This 1K pull up resistor is no longer needed on Skylake platforms and can be removed from the motherboard. The new guidelines will be updated in a future release of the Skylake PDG

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

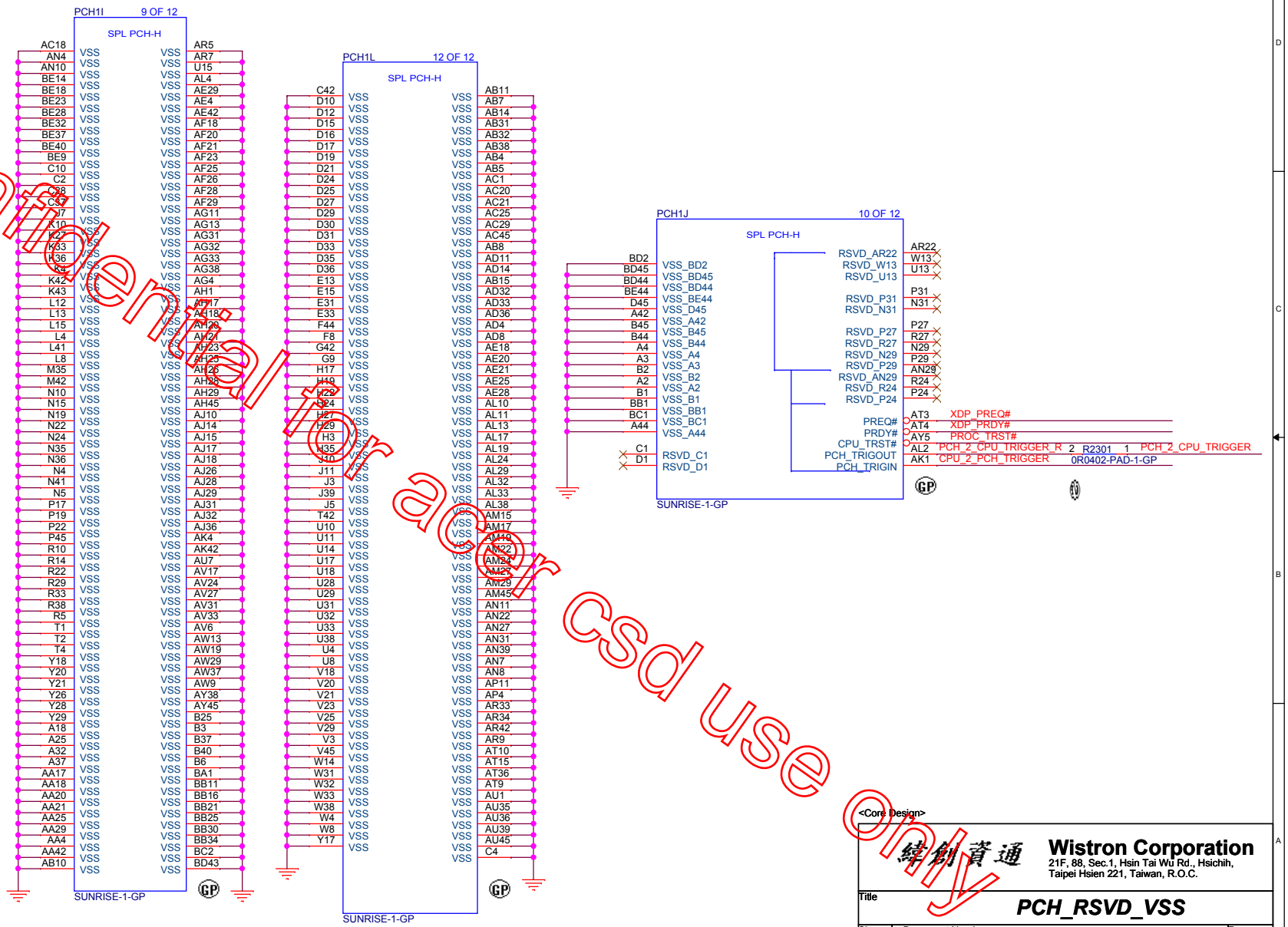
Title: PCH_STRAP

Size: A2 | Document Number: Neptune_KLS | Rev: -1m

Date: Wednesday, May 17, 2017 | Sheet 22 of 105

6,99 XDP_PREQ#
6,99 XDP_PRDY#
6,99 PROC_TRST#
8 PCH_2_CPU_TRIGGER
8 CPU_2_PCH_TRIGGER

SSID = PCH



<Core Design>

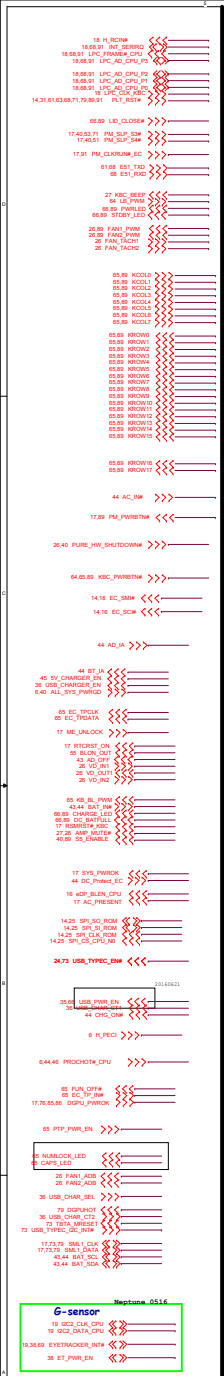
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

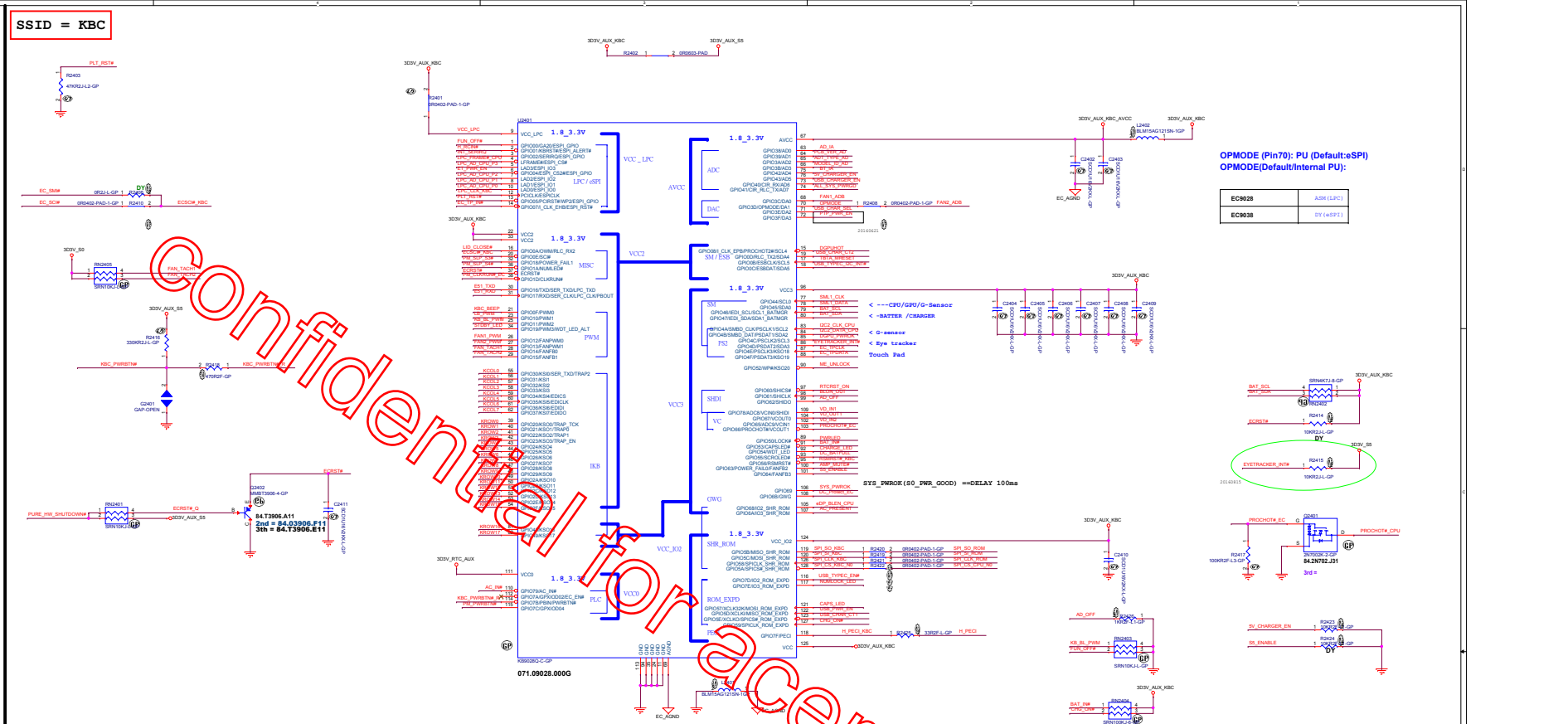
Title: PCH_RSVD_VSS

Size: B | Document Number: Neptune_KLS | Rev: -1m

Date: Wednesday, May 17, 2017 | Sheet 23 of 105

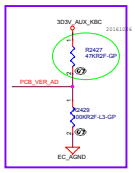
SSID = KBC



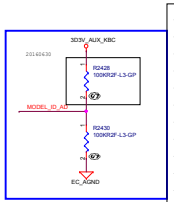


OPMODE (Pin70): PU (Default:eSPI)
OPMODE(Default/Internal PU):

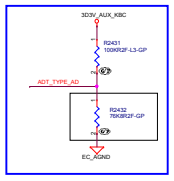
EC9028	ASM (LPC)
EC9038	DY (eSPI)



PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
5A (LAB1)	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
5B (LAB2)	100.0 K	20.0 K	2.759 V	2.759 V	>= 2.616 V	< 2.875 V
5C (ENG)	100.0 K	33.0 K	2.491 V	2.493 V	>= 2.363 V	< 2.616 V
-1 (PD)	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
-1M (MP)	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V
-1M (MP 3D SKU)	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V	< 1.934 V



MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
Pluto_N17P(G1/960)	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
Pluto_N17E(G1/970)	100.0 K	20.0 K	2.759 V	2.759 V	>= 2.616 V	< 2.875 V
	100.0 K	33.0 K	2.491 V	2.493 V	>= 2.363 V	< 2.616 V
	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V
Neptune-N17P(G1/960)	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V	< 1.934 V
Neptune-N17E(G1/970)	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.504 V	< 1.758 V
	100.0 K	143.0 K	1.358 V	1.374 V	>= 1.281 V	< 1.504 V
	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.126 V	< 1.281 V
	100.0 K	215.0 K	1.048 V	1.062 V	>= 0.524 V	< 1.126 V



ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.305 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.559 V	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.831 V	>= 0.684 V	< 0.937 V
135W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.937 V	< 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.315 V	>= 1.177 V	< 1.366 V
180W	76.8 K	100.0 K	1.433 V	1.450 V	>= 1.366 V	< 1.542 V

<Core Design>
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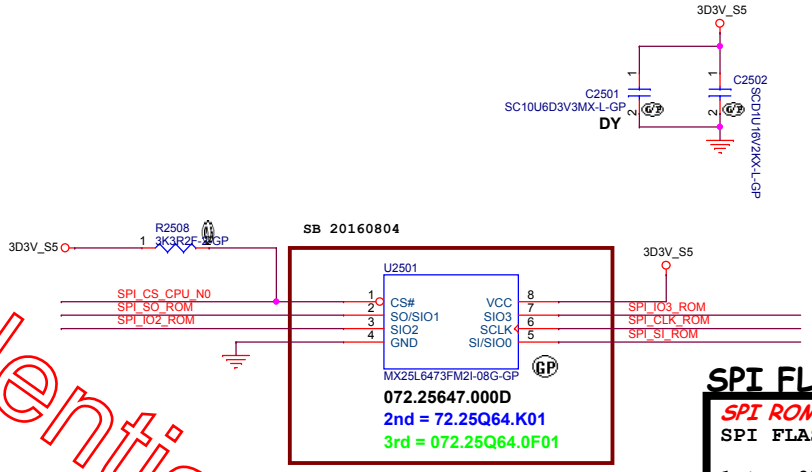
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: KBC_ENE_KB9028_KB9038
Size: Custom | Document Number: Neptune_KLS | Rev: -1m
Date: Wednesday, May 17, 2017 | Sheet 24 of 105

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH



14,24 SPI_CS_CPU_N0
14,24 SPI_SO_ROM
14,22 SPI_IO2_ROM
14,22 SPI_IO3_ROM
14,24 SPI_CLK_ROM
14,24 SPI_SI_ROM

SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil

SPI FLASH ROM (8M byte)

1st= 072.25647.000D (MXIC MX25L6473FM2I-08G)
2nd= 72.25Q64.K01 (WINBOND W25Q64FVSSIQ)
3th= 072.25Q64.0F01 (MICRON N25Q064A13ESED0F)

Main Func = RTC

19 RTC_DET#

RTC BATTERY

1st= 23.20068.001
2nd= 023.20004.0011

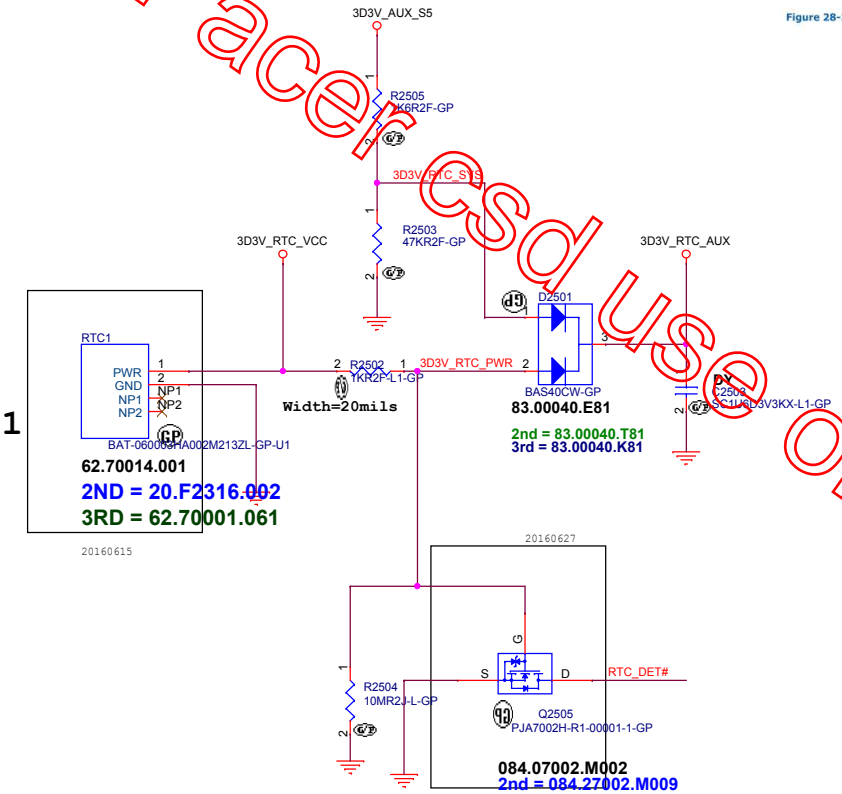
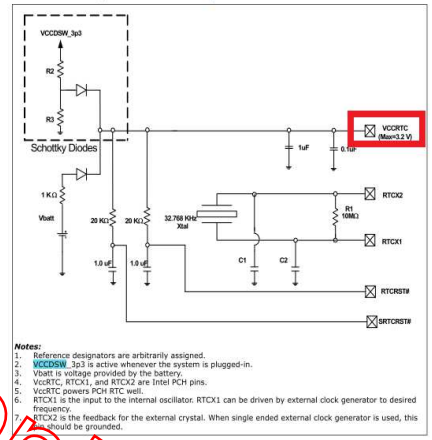


Figure 28-2. External Circuitry for the PCH RTC - Option 1



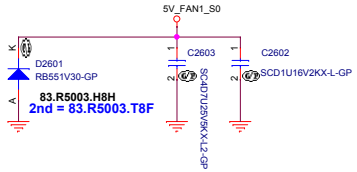
Notes:
1. Reference designators are arbitrarily assigned.
2. VCCDSW_3p3 is active whenever the system is plugged-in.
3. Vbatt is voltage provided by the battery.
4. VccRTC, RTCX1, and RTCX2 are Intel PCH pins.
5. VccRTC powers PCH RTC well.
6. RTCX1 is the input to the internal oscillator. RTCX1 can be driven by external clock generator to desired frequency.
7. RTCX2 is the feedback for the external crystal. When single ended external clock generator is used, this pin should be grounded.

<Core Design>

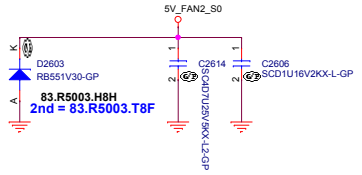
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Flash(KBC+PCH)/RTC		
Size: A3	Document Number: Neptune_KLS	Rev: -1m
Date: Wednesday, May 17, 2017	Sheet 25 of 105	

SSID = Thermal

Layout 15 mil

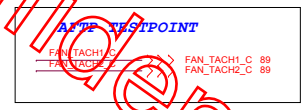


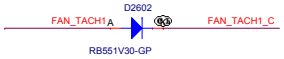
Layout 15 mil

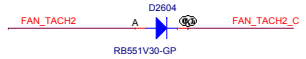


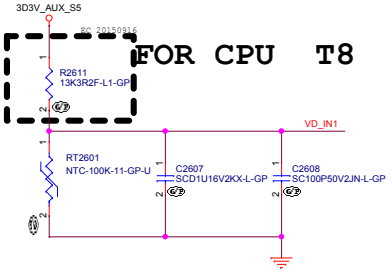
ADB (Active Dusting Blower) function

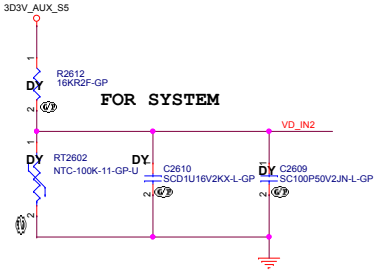
24 FAN_TACH1
24 FAN_TACH2
24,89 FAN1_PWM
24,89 FAN2_PWM
24 VD_IN1
24 VD_IN2
24 FAN1_ADB
24 FAN2_ADB
24 VD_OUT1
24,40 PURE_HW_SHUTDOWN#
40,46 IMVP_PWRGD

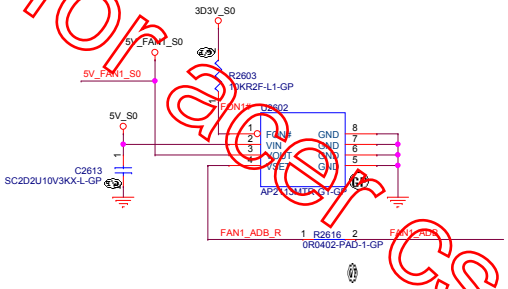


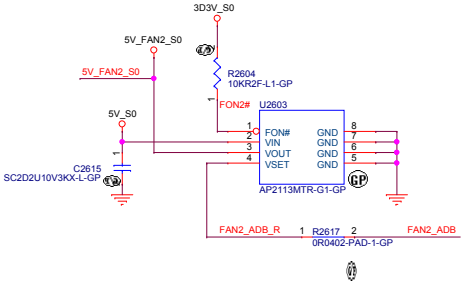


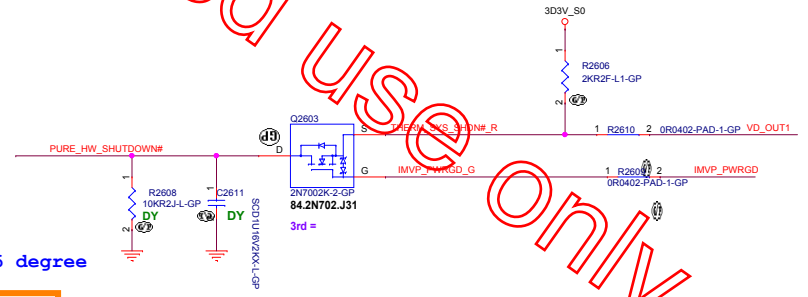






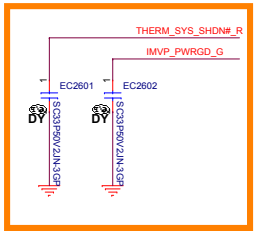






T8 = 85 degree

EMI Reserved



<Core Design>

緯創資通 Wistron Corporation
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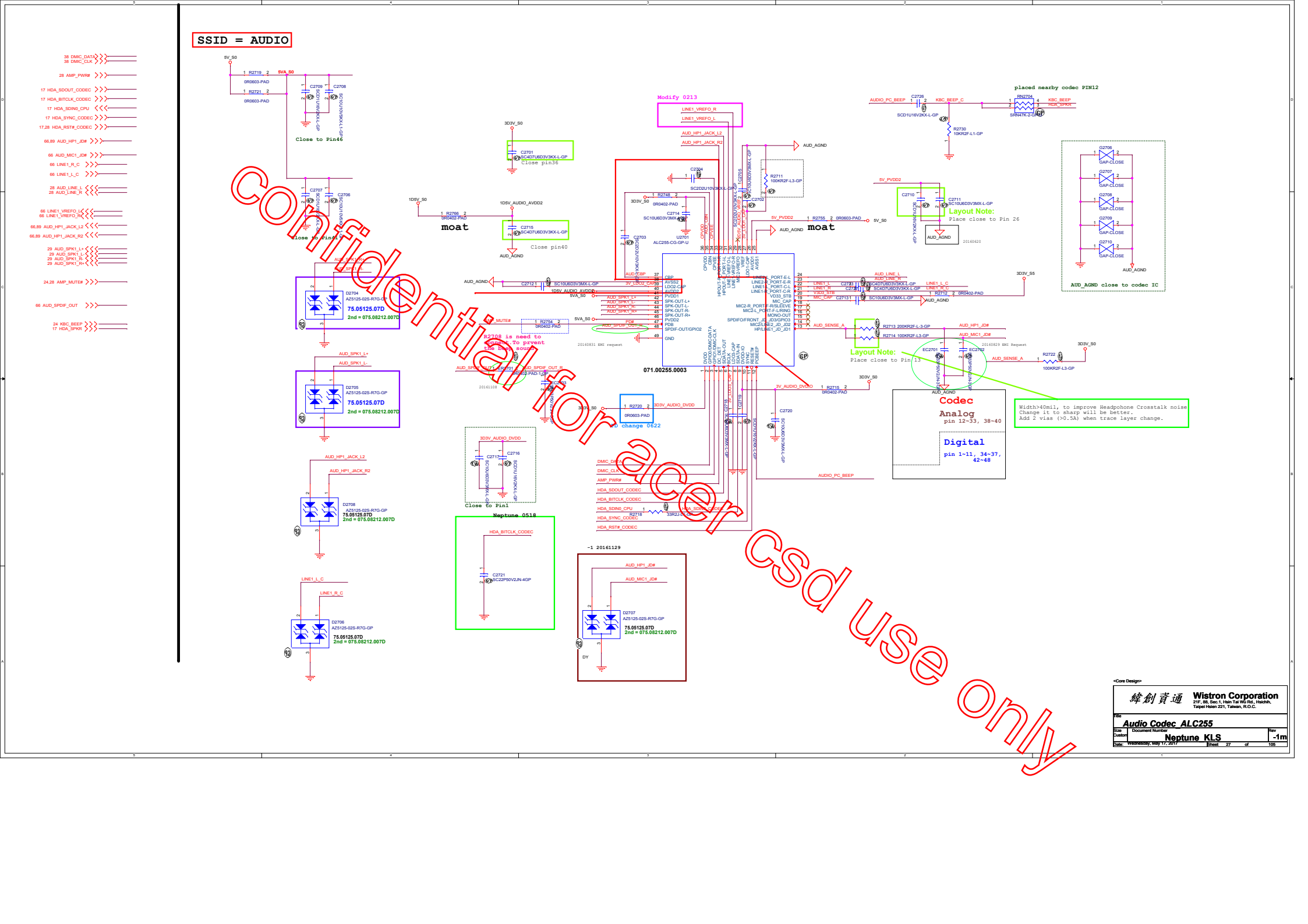
Title: Thermal T8 and FAN

Size: Custom | Document Number: Neptune_KLS | Rev: -1m

Date: Wednesday, May 17, 2017 | Sheet 26 of 105

SSID = AUDIO



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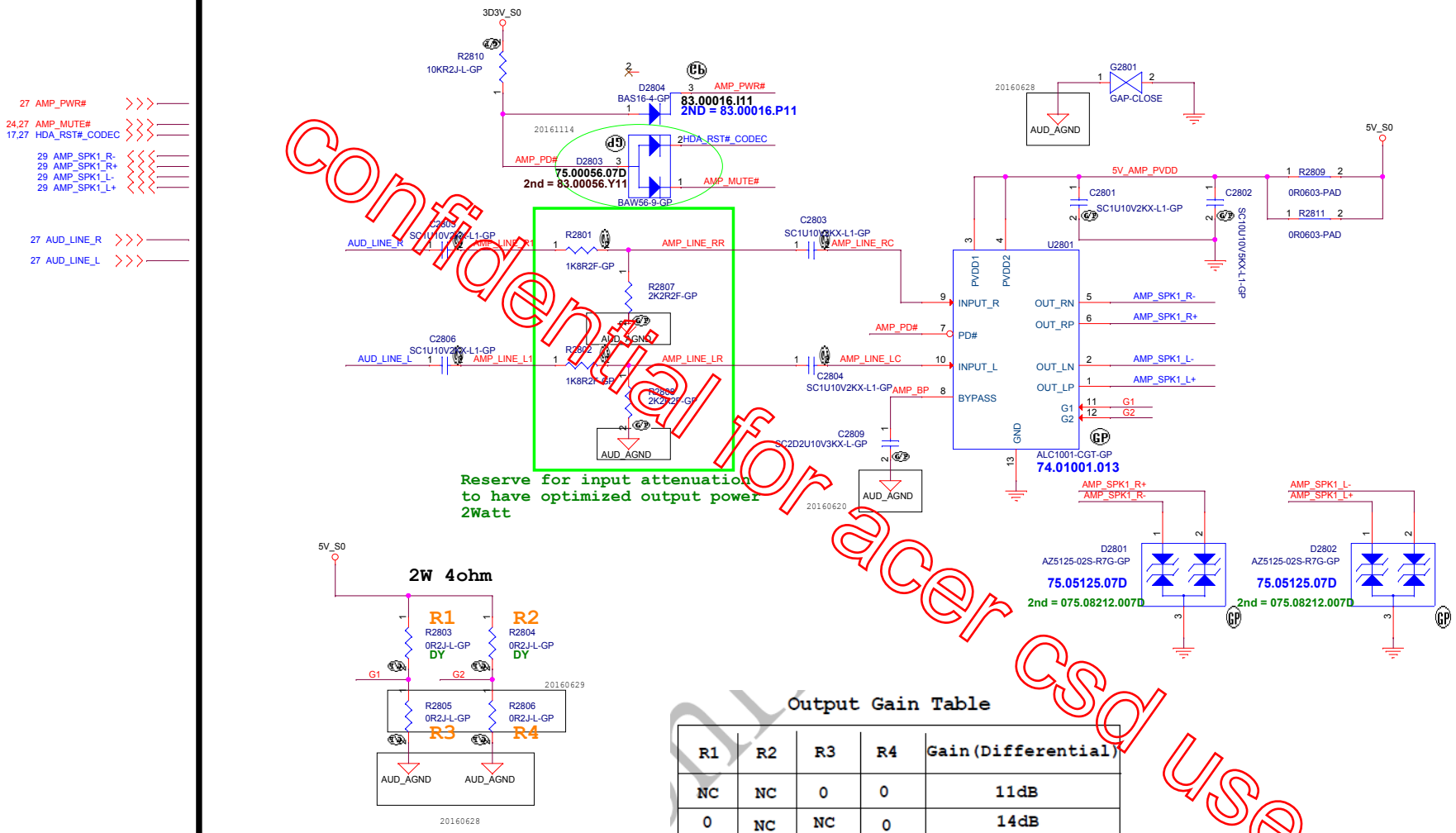
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: Audio Codec_ALC255			
Size: Custom	Document Number: Neptune_KLS		Rev: -1m
Date: Wednesday, May 17, 2017	Sheet 27 of 105		



Output Gain Table

R1	R2	R3	R4	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

<Core_Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

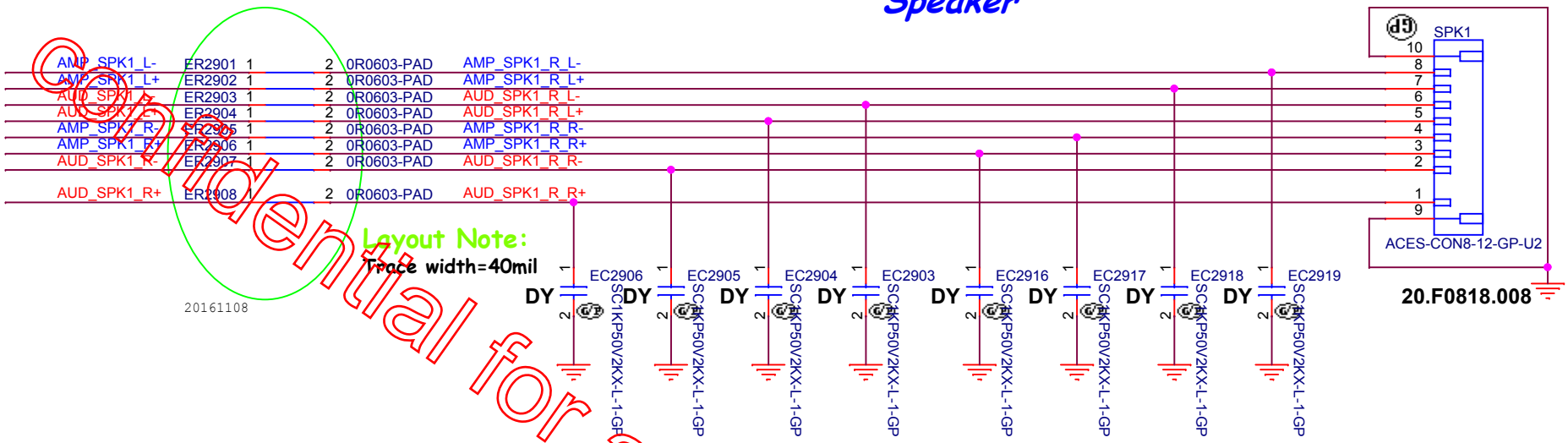
Title: AUDIO AMP_ALC1001

Size: Custom | Document Number: Neptune_KLS | Rev: -1m

Date: Wednesday, May 17, 2017 | Sheet 28 of 105

SSID = AUDIO

Speaker



28 AMP_SPK1_L-
28 AMP_SPK1_L+
27 AUD_SPK1_L-
27 AUD_SPK1_L+
28 AMP_SPK1_R-
28 AMP_SPK1_R+
27 AUD_SPK1_R-
27 AUD_SPK1_R+

AFTP TESTPOINT

89 AMP_SPK1_R_L-
89 AMP_SPK1_R_L+
89 AUD_SPK1_R_L-
89 AUD_SPK1_R_L+
89 AMP_SPK1_R_R-
89 AMP_SPK1_R_R+
89 AUD_SPK1_R_R-
89 AUD_SPK1_R_R+

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Speaker/ALC255**

Size	Document Number	Rev
A4	Neptune_KLS	-1m

Date: Wednesday, May 17, 2017 Sheet 29 of 105

<Core Design>

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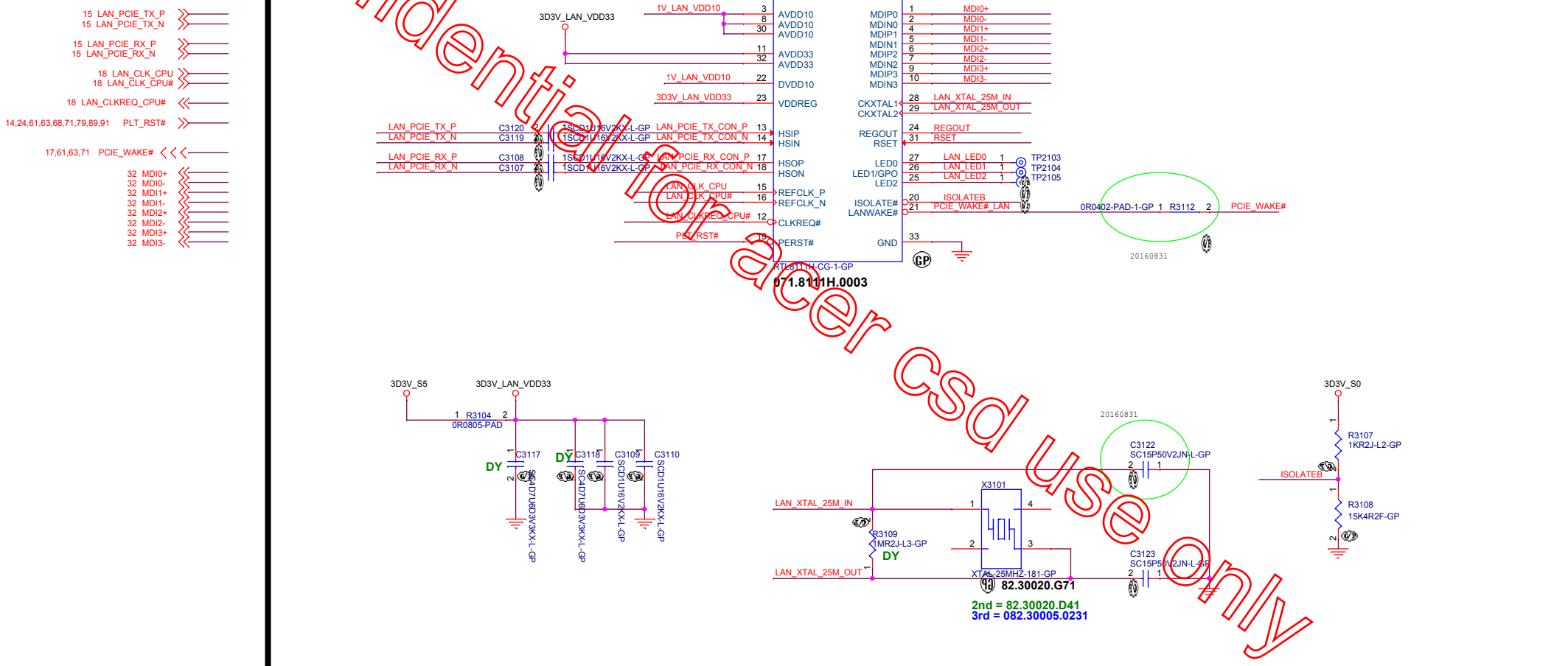
Title: ***(Reserved)***

Size	Document Number	Rev
A	Neptune_KLS	-1m

Date: Wednesday, May 17, 2017 Sheet 30 of 105



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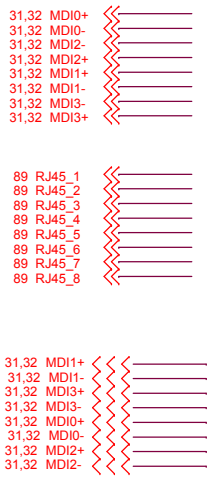
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

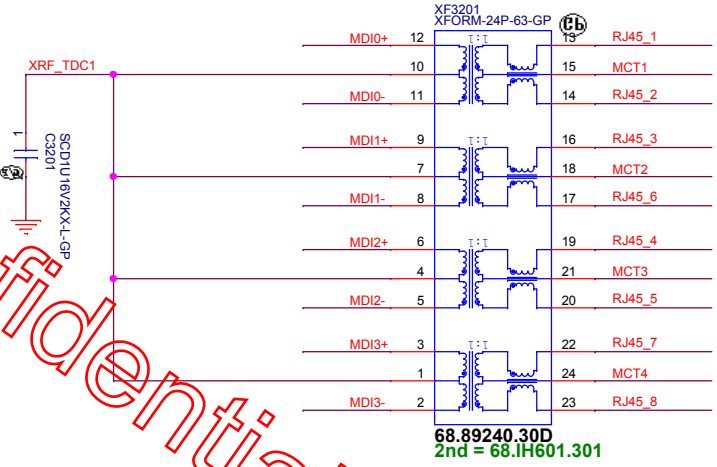
Title: LAN(RTL8111)

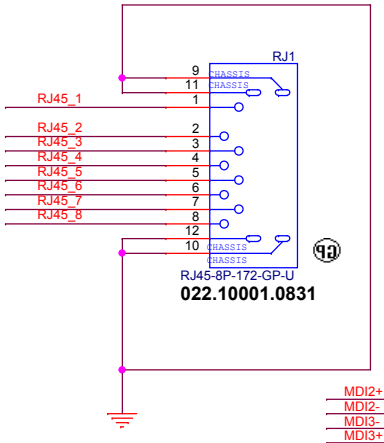
Size	Document Number	Rev
A3	Neptune_KLS	-1m

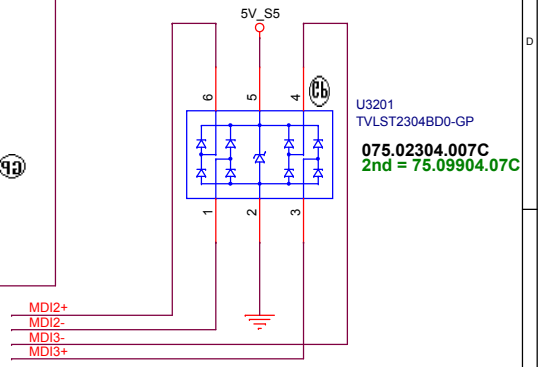
Date: Wednesday, May 17, 2017 Sheet 31 of 105

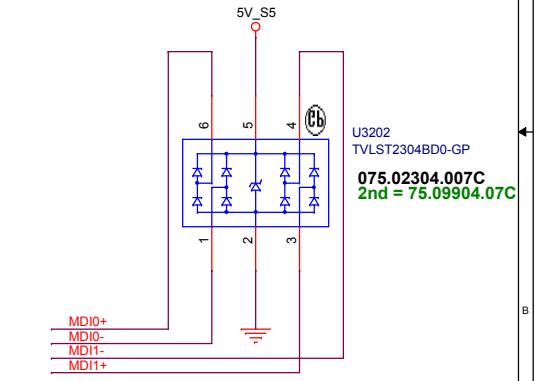
SSID = LAN

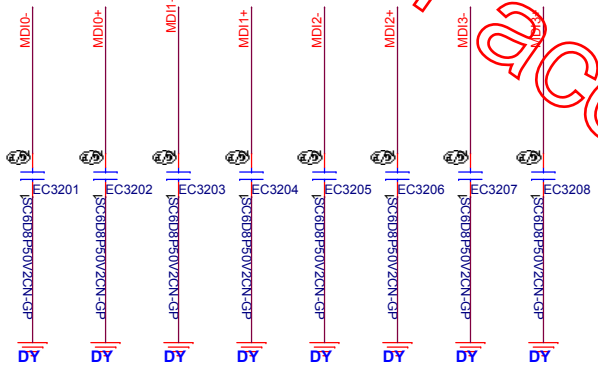


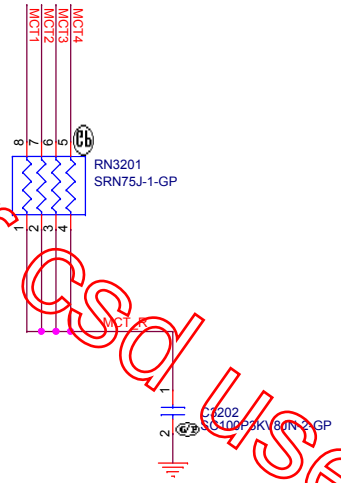












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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: RJ45+Transformer

Size	Document Number	Rev
B	Neptune_KLS	-1m

Date: Wednesday, May 17, 2017 Sheet 32 of 105

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title
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Size	Document Number	Rev
A	**Neptune_KLS**	**-1m**

Date: Wednesday, May 17, 2017 Sheet 33 of 105

<Core Design>

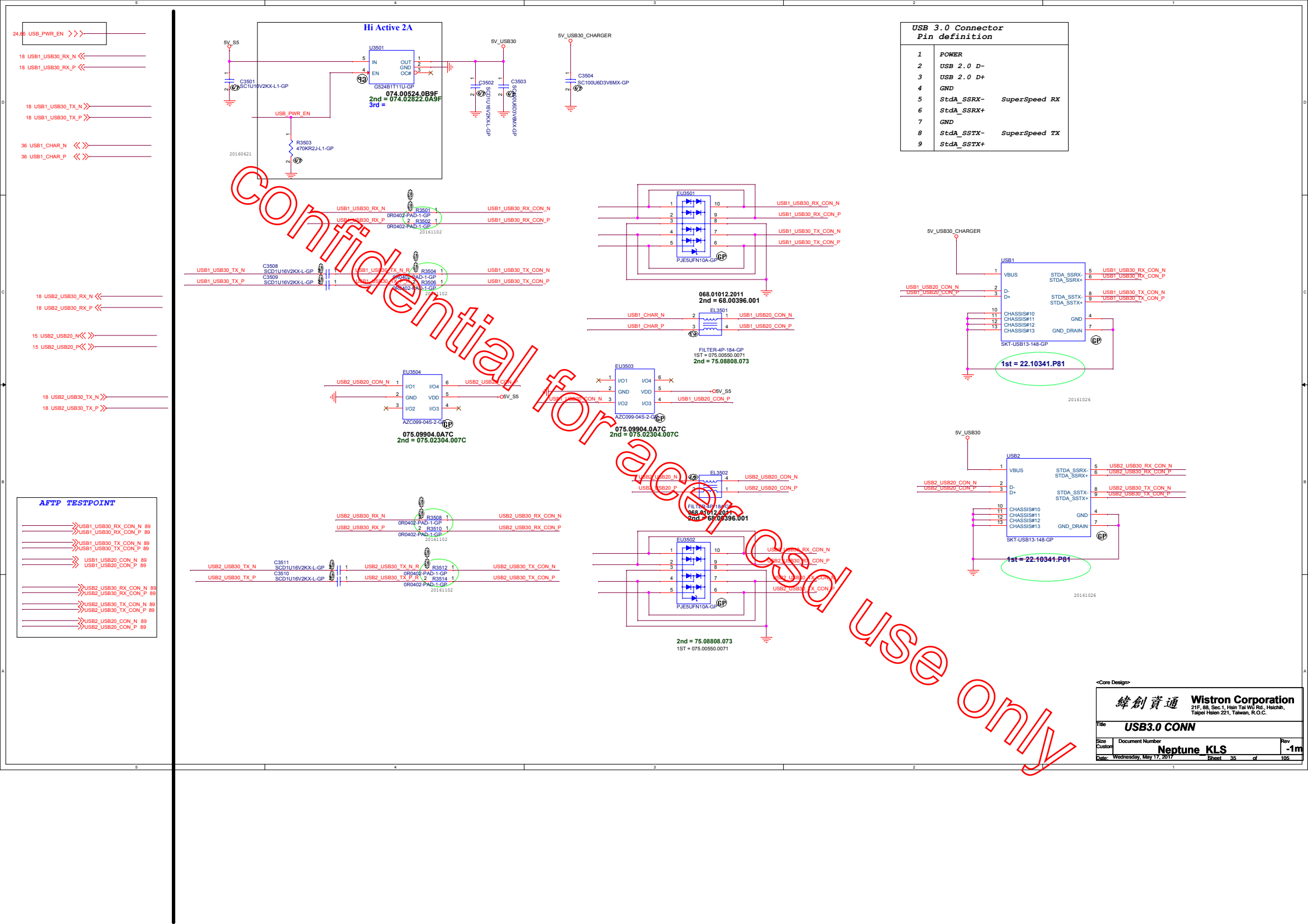
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_CFG_CFG STRAP***

Size	Document Number	Rev
A	**Neptune_KLS**	**-1m**

Date: Wednesday, May 17, 2017 Sheet 34 of 105



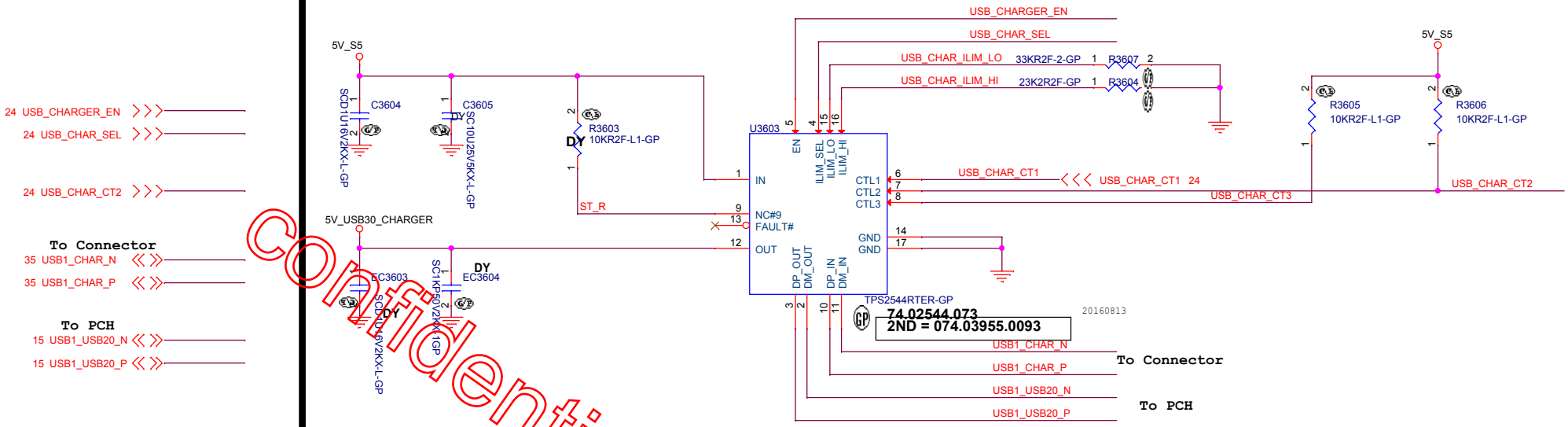


Table 2. Truth Table

CTL1	CTL2	CTL3	ILIM_ SEL	MODE	Current Limit Setting	Status Output	Notice
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data lines disconnected
0	0	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
0	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_LO	OFF	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device forced to stay in DCP BC1.2
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	Charging mode
1	0	1	0	DCP/Divider1	ILIM_LO	OFF	Device forced to stay in DCP divider1
1	0	1	1	DCP/Divider1	ILIM_HI	OFF	Charging mode
1	1	0	0	SDP1	ILIM_LO	OFF	
1	1	0	1	SDP1	ILIM_HI	OFF	Data lines connected
1	1	1	0	SDP2	ILIM_LO	OFF	
1	1	1	1	CDP	ILIM_HI	CDP	Data lines disconnected Load Detect function active

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB CHARGER

Size: B | Document Number: Neptune_KLS | Rev: -1m

Date: Wednesday, May 17, 2017 | Sheet 36 of 105

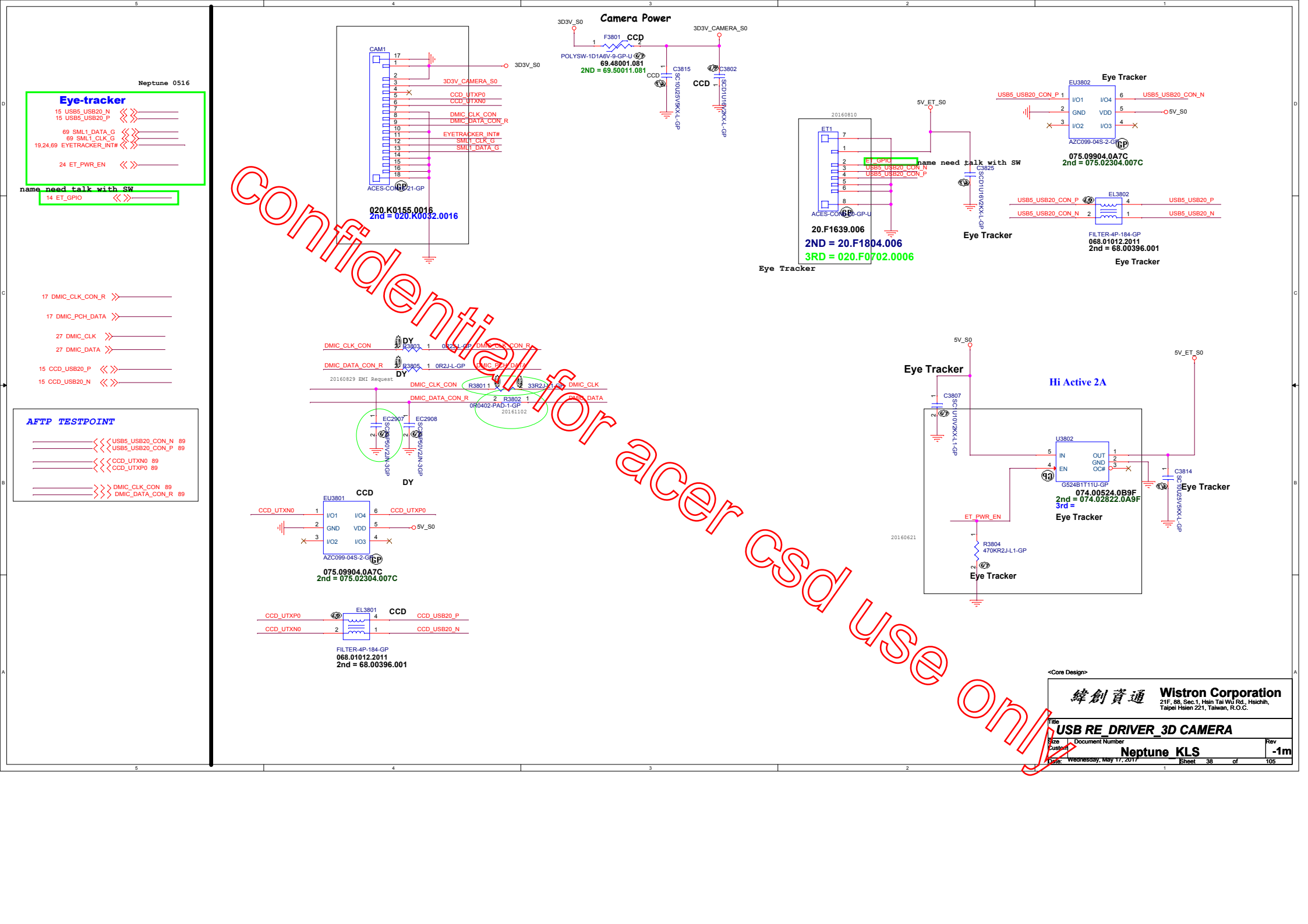
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A	Neptune_KLS	-1m

Date: Wednesday, May 17, 2017 Sheet 37 of 105



<Core Design>

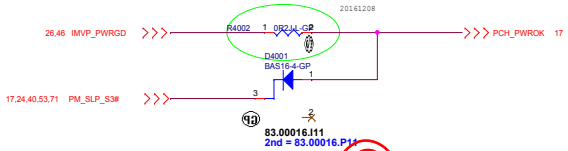
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

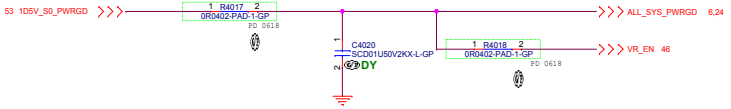
Title
(Reserved)

Size	Document Number	Rev
A	**Neptune_KLS**	**-1m**

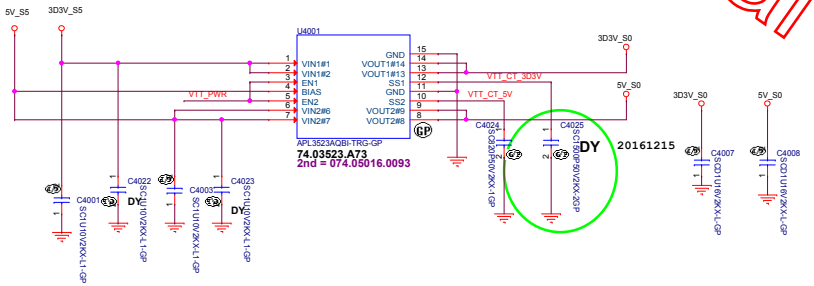
Date: Wednesday, May 17, 2017 Sheet 39 of 105

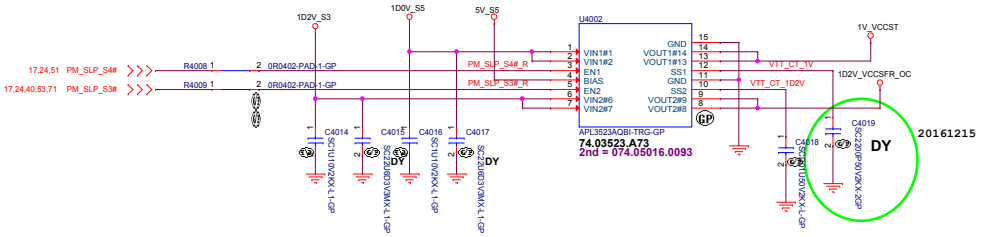
Power Sequence

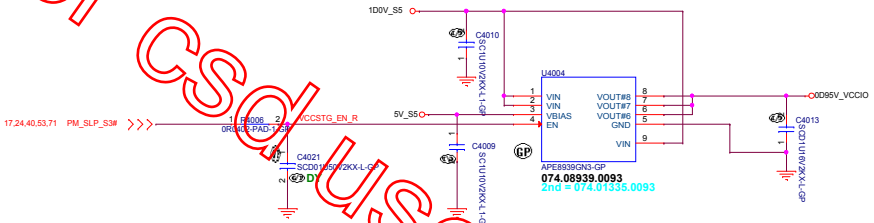


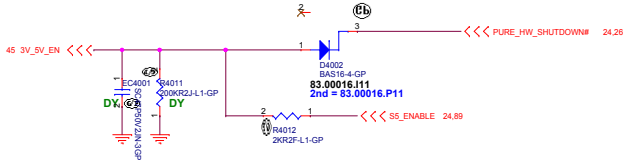


ANNIE Run Power









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Title: Power Plane Enable & SEQUENCE

Size: A2 | Document Number: Neptune_KLS | Rev: -1m

Date: Wednesday, May 17, 2017 | Sheet 40 of 105

<Core Design>

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Title: ***(Reserved)DS3***

Size	Document Number	Rev
A	**Neptune_KLS**	**-1m**

Date: Wednesday, May 17, 2017 Sheet 41 of 105

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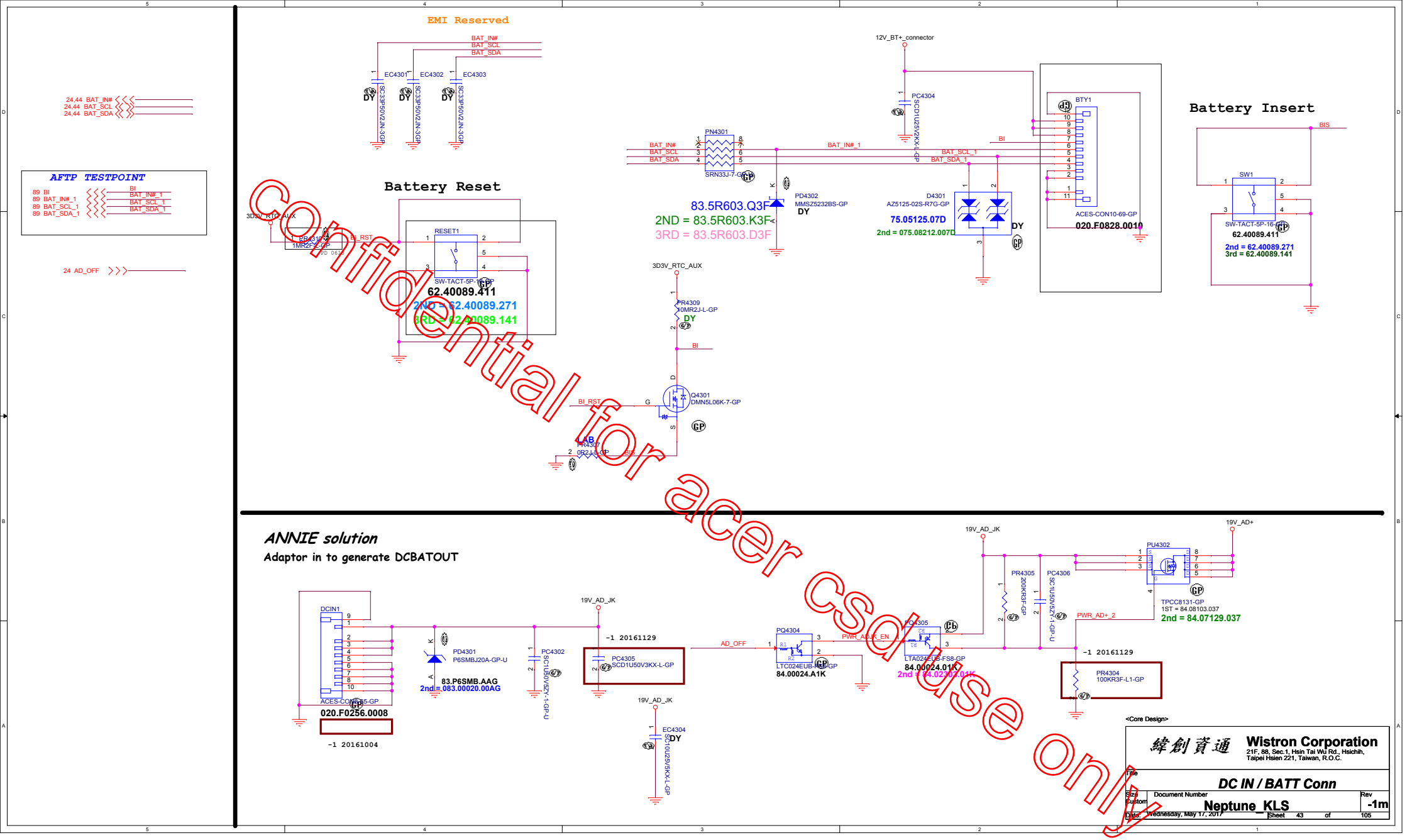
Title: ***(Reserved)***

Size	Document Number	Rev
A	**Neptune_KLS**	**-1m**

Date: Wednesday, May 17, 2017 Sheet 42 of 105


EMI Reserved
Battery Reset
Battery Insert
ANNIE solution
Adaptor in to generate DCBATOUT
DC IN / BATT Conn
Wistron Corporation
Neptune_KLS
Confidential for acer Sqa use only

SSID = Charger

Adaptor			Protect	Sense	Amplifier		R1	R2
Watt	Current	Persent	Current	Resistor	Ratio	IADP	PR4407	PR4401
135.00 W	6.92 A	110%	7.59 A	10 mOhm	20	1.52 V	24.9 K	100 K
180.00 W	9.23 A	110%	10.12 A	10 mOhm	20	2.02 V	68.1 K	100 K

Total Power Setting

SMBuS

IDCHG : Dischange detect current :
= 8 or 16 x (Vsrn - Vsrp)

IADP : AC adapter detect current :
= 20 or 40 x (Vacp - Vacn) / 10mohm

PMON : Total system power

RF RESERVED

EMI Reserved

Charger Current=1.4~3.6A

CYNTEC 7*7*3
DCR: 37~40mOhm
Idc : 5.5 A , Isat : 10A

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Title	CHARGER HPA02224
Size / Custom	Document Number: Neptune_KLS
Rev	-1m
Date: Wednesday, May 17, 2017	Sheet 44 of 105

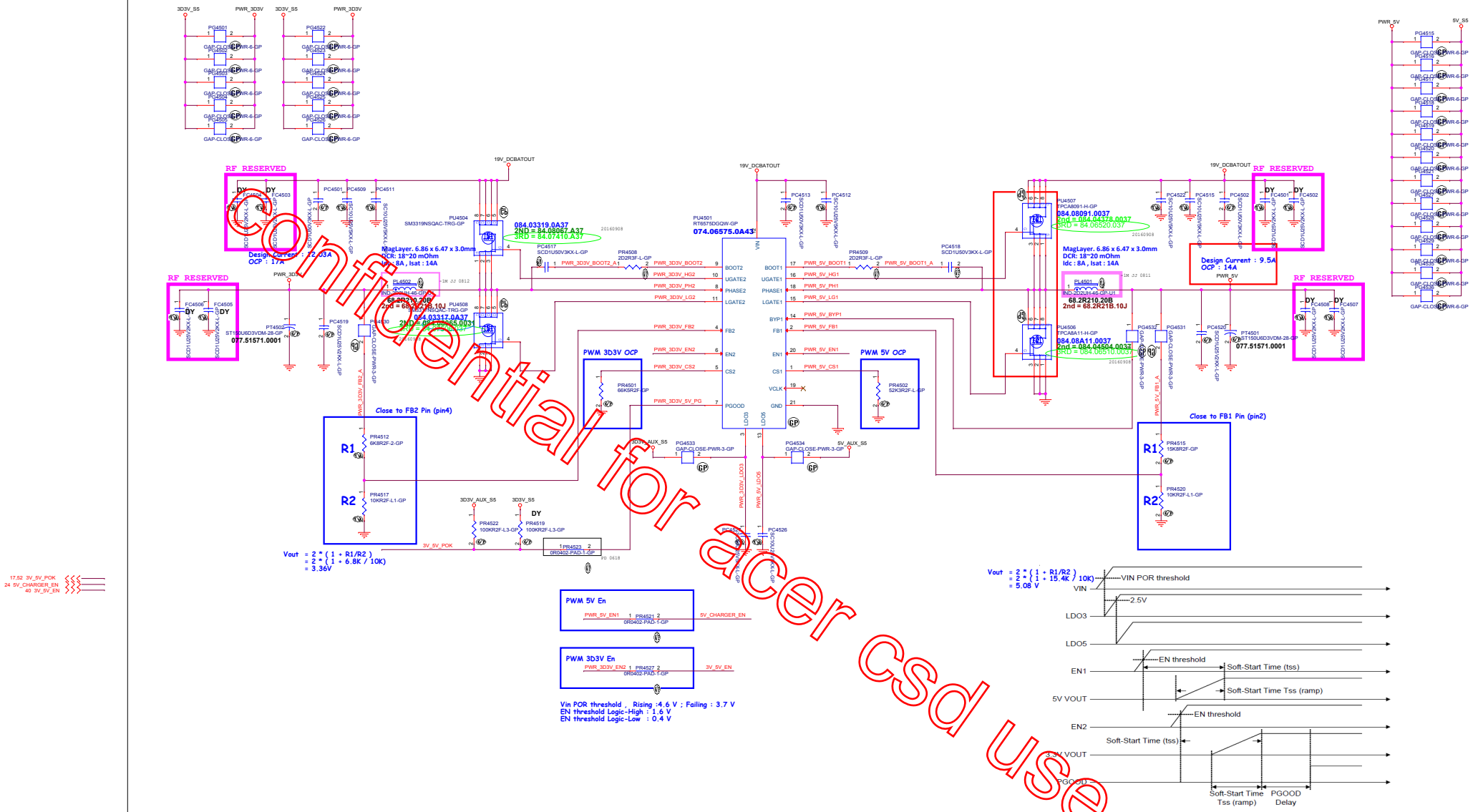

Figure 6. RT6575B Timing

<Core Design>

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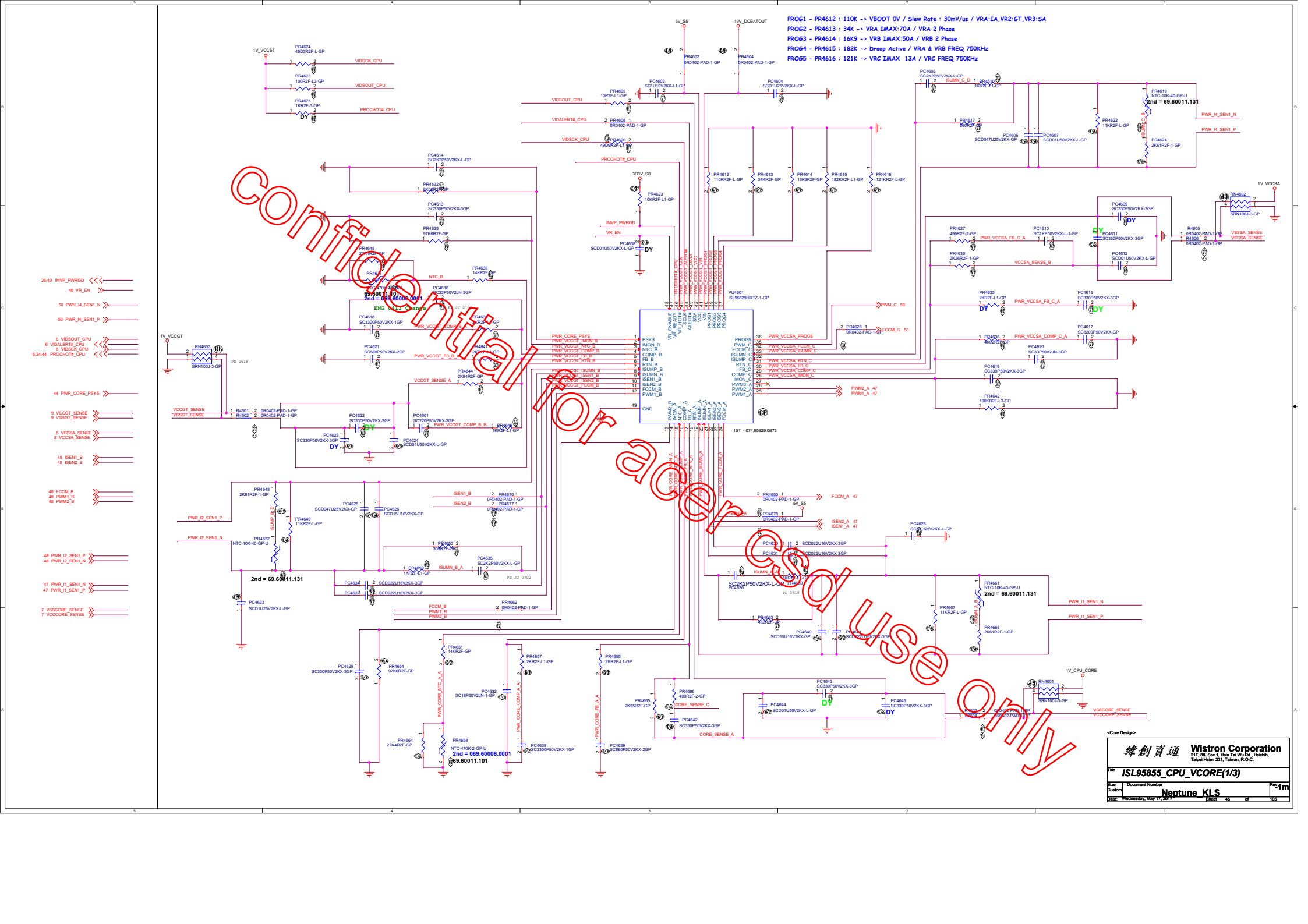
Title: RT6575D_5V/3D3V

Size: Custom | Document Number: Neptune_KLS | Rev: -1m

Date: Wednesday, May 17, 2017 | Sheet 45 of 105


PROG1 - PR4612 : 110K -> VBOOT 0V / Slew Rate : 30mV/us / VRA:IA,VR2:GT,VR3:SA
PROG2 - PR4613 : 34K -> VRA IMAX:70A / VRA 2 Phase
PROG3 - PR4614 : 16K9 -> VRB IMAX:50A / VRB 2 Phase
PROG4 - PR4615 : 182K -> Droop Active / VRA & VRB FREQ 750KHz
PROG5 - PR4616 : 121K -> VRC IMAX 13A / VRC FREQ 750KHz
PU4601 ISL95829HRTZ-1-GP
1ST = 074.95829.0B73
2nd = 69.60011.101
2nd = 069.60006.0001
69.60011.101
SC2K2P50V2KX-L-GP
PC4636
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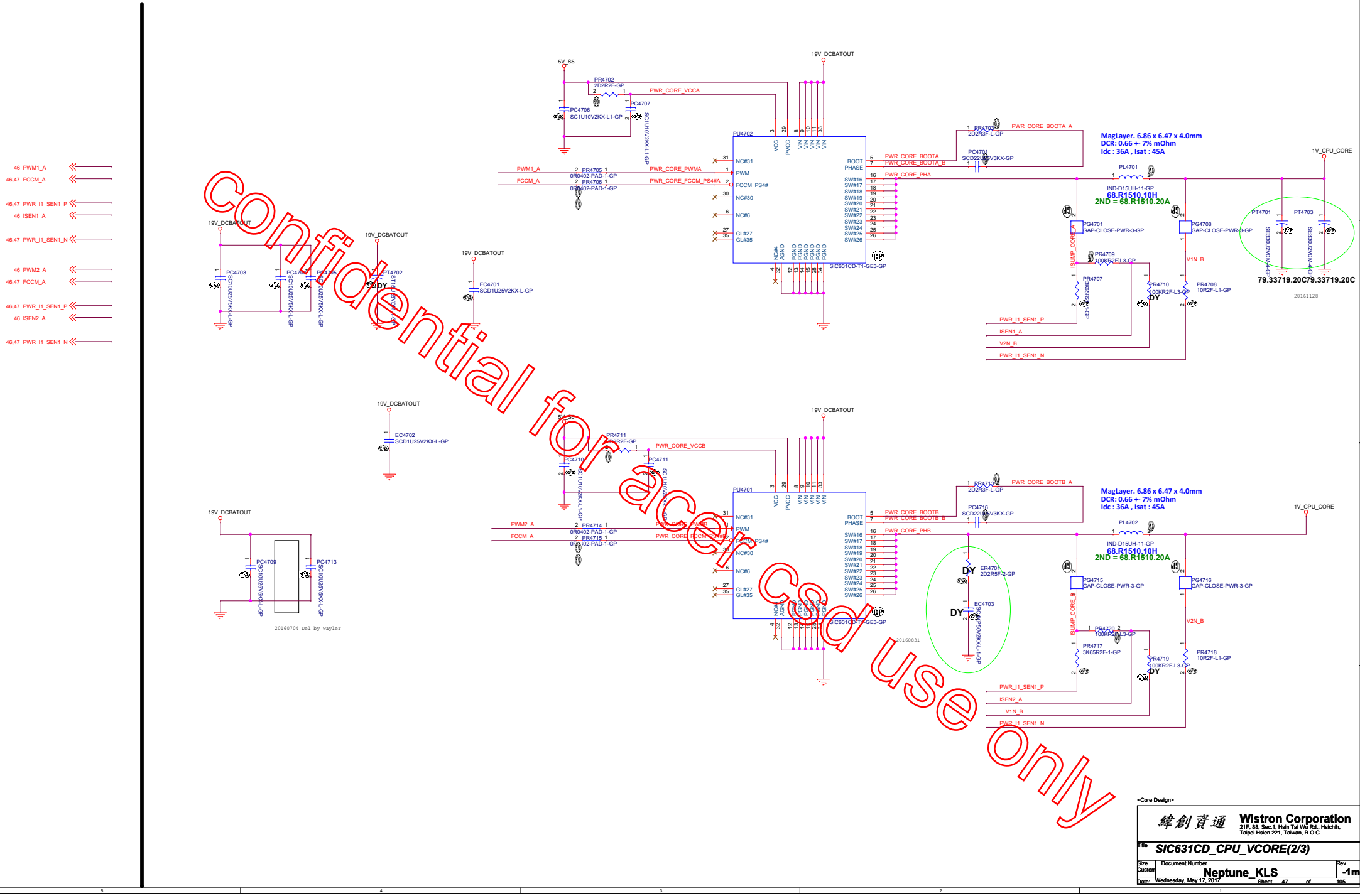
ISL95855_CPU_VCORE(1/3)
Neptune_KLS
Wednesday, May 17, 2017
Sheet 46 of 105



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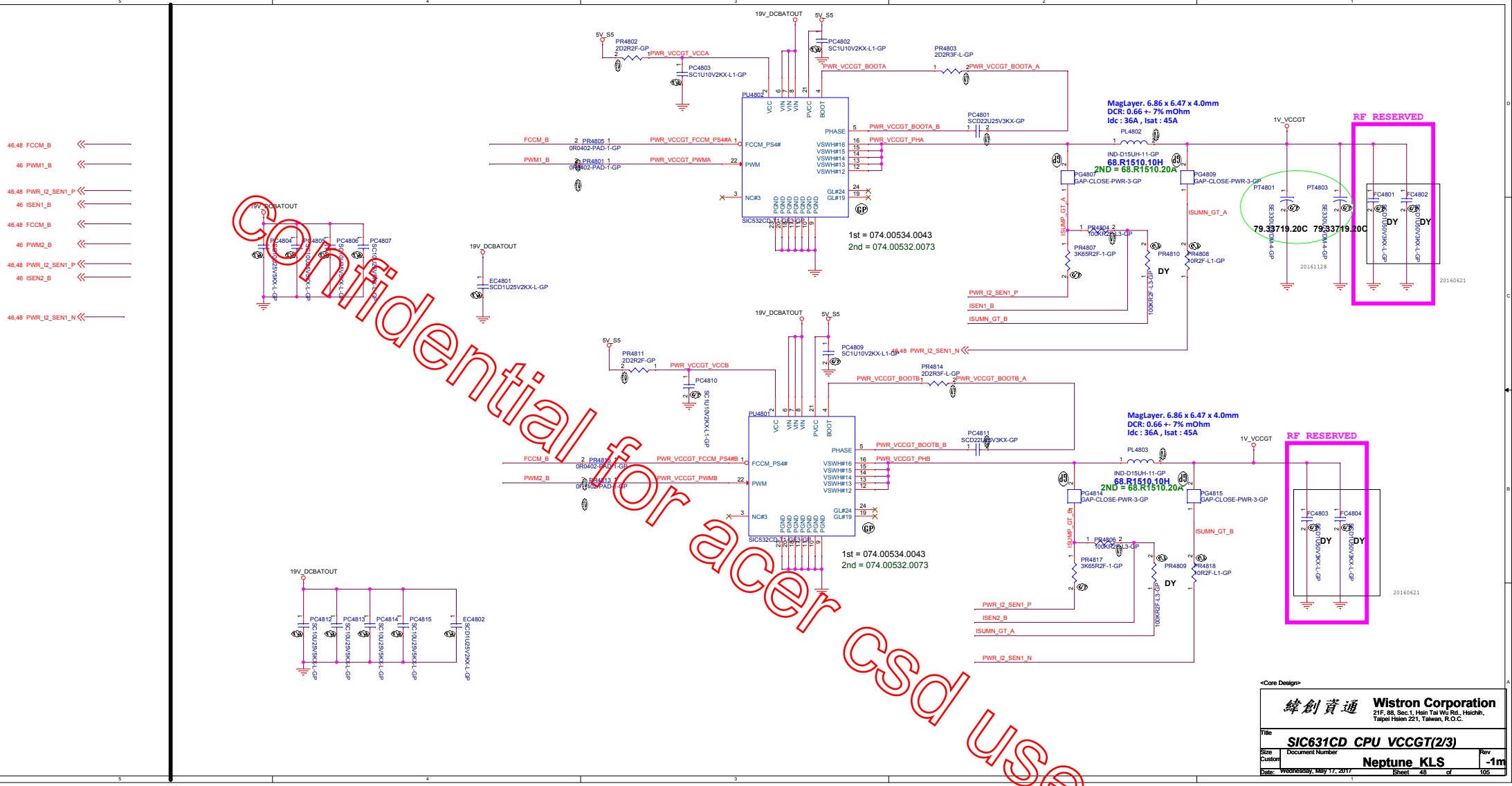
Taipei Hsien 221, Taiwan, R.O.C.

Title	SIC631CD_CPU_VCORE(2/3)	
Size: Custom	Document Number: Neptune_KLS	Rev: -1m
Date: Wednesday, May 17, 2017	Sheet 47 of 105	



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Title: SIC631CD CPU VCCGT(2/3)

Size: Custom | Document Number: Neptune_KLS | Rev: -1m

Date: Wednesday, May 17, 2017 | Sheet 48 of 105

<Core Design>

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Title: ***(Reserved)***

Size	Document Number	Rev
A	Neptune_KLS	-1m

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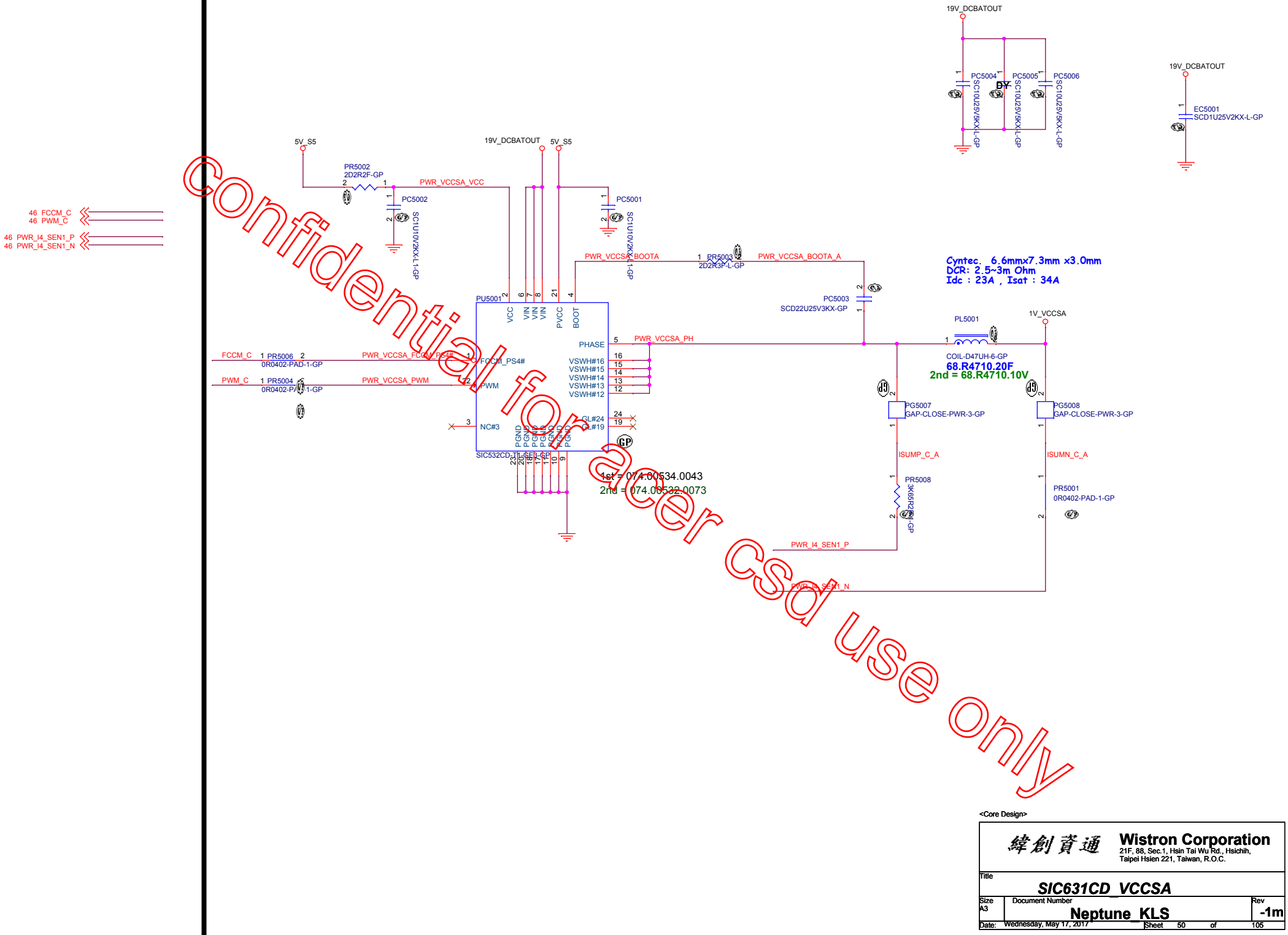

<Core Design>

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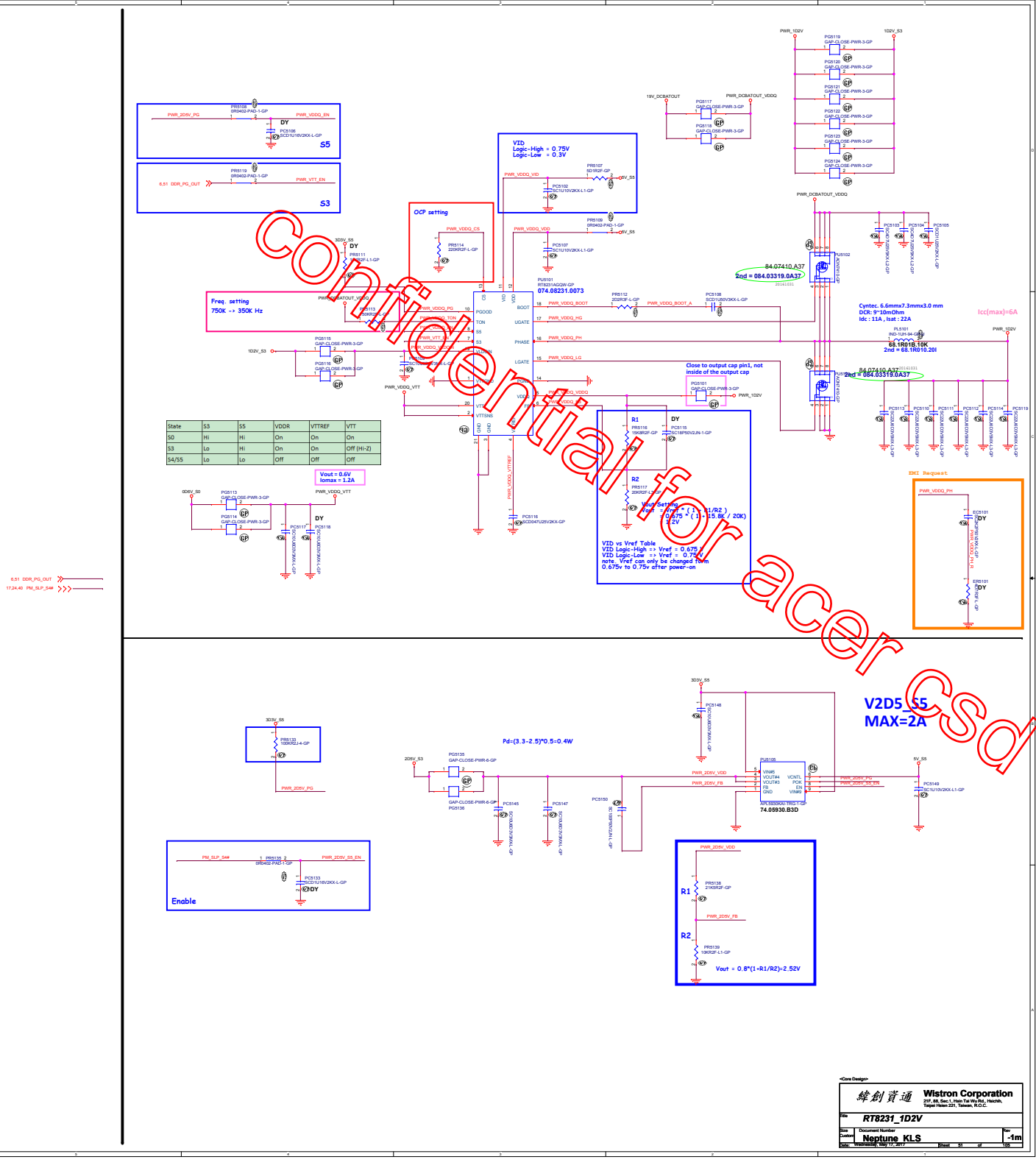
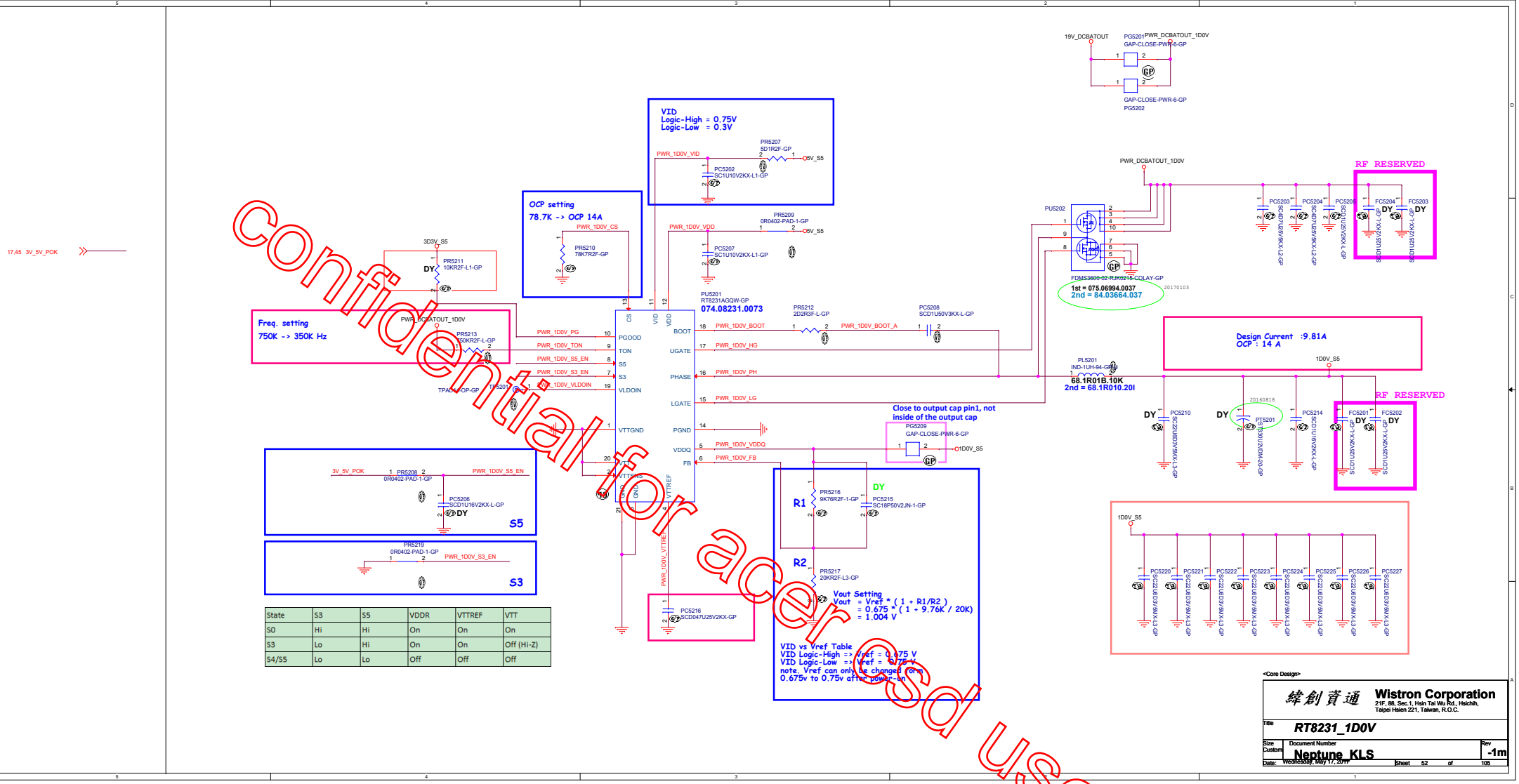
Title	SIC631CD_VCCSA	
Size A3	Document Number: Neptune_KLS	Rev: -1m
Date: Wednesday, May 17, 2017	Sheet 50 of 105	

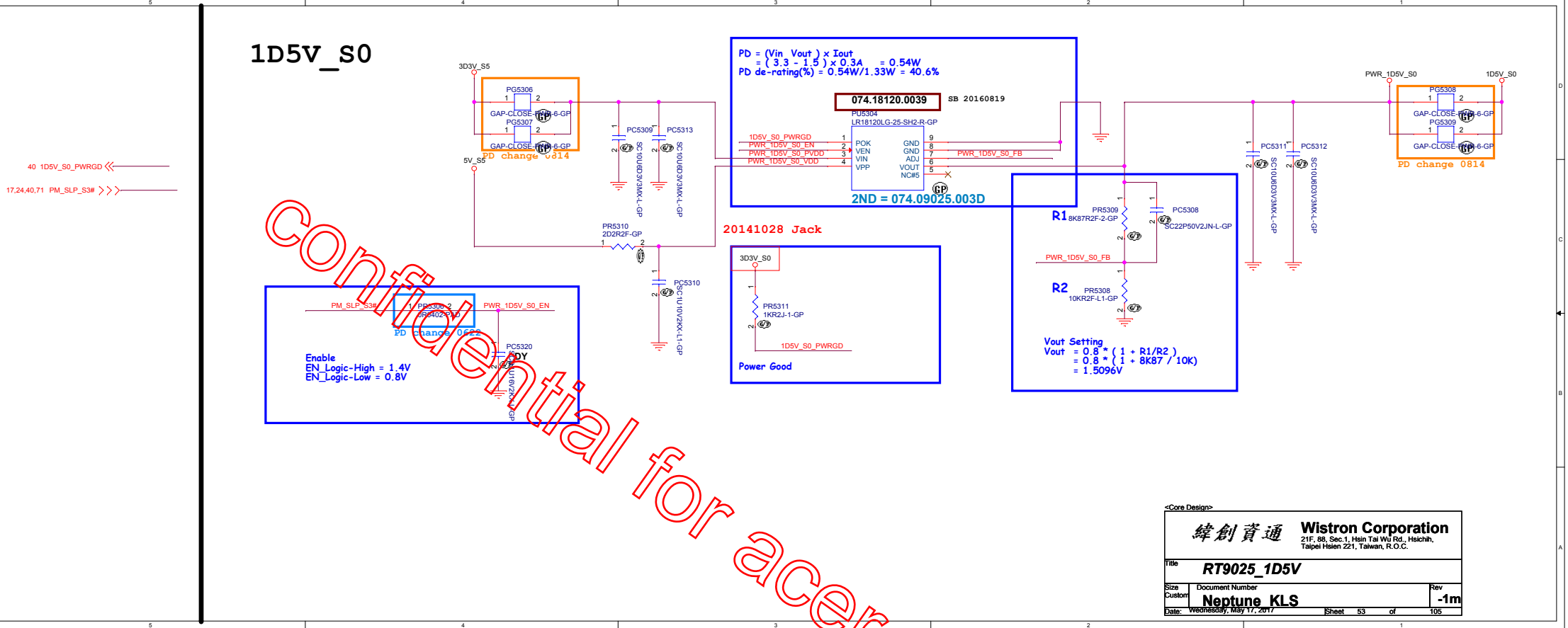


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

1D5V_S0



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Title	RT9025_1D5V	
Size: Custom	Document Number: Neptune_KLS	Rev: -1m
Date: Wednesday, May 17, 2017	Sheet 53 of 105	

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Title
(Reserved)

Size	Document Number	Rev
A	**Neptune_KLS**	**-1m**

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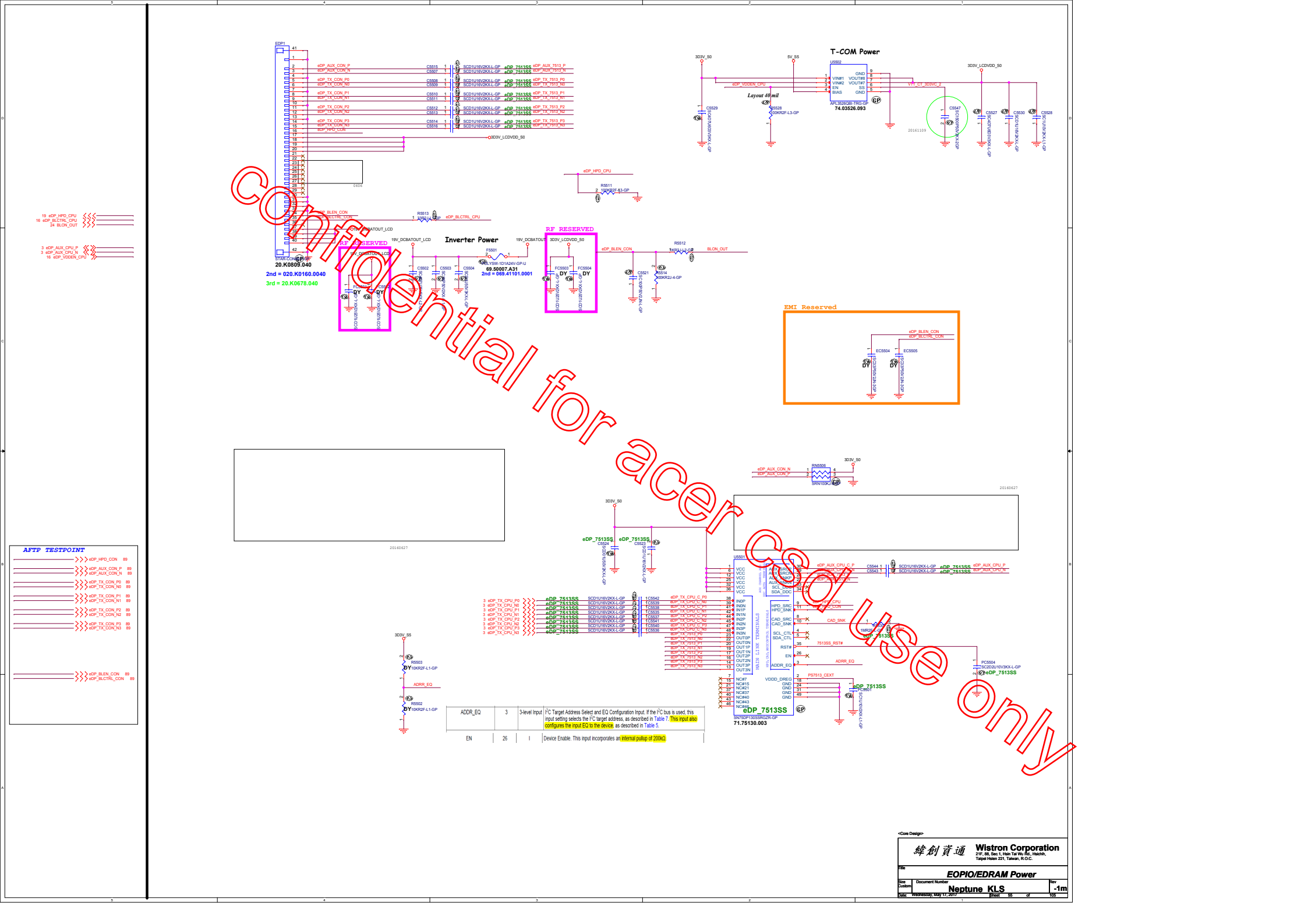

ADDR_EQ	3	3-level Input	I²C Target Address Select and EQ Configuration Input. If the I²C bus is used, this input setting selects the I²C target address, as described in Table 7. This input also configures the input EQ to the device, as described in Table 5.
EN	26	I	Device Enable. This input incorporates an internal pullup of 200kΩ.

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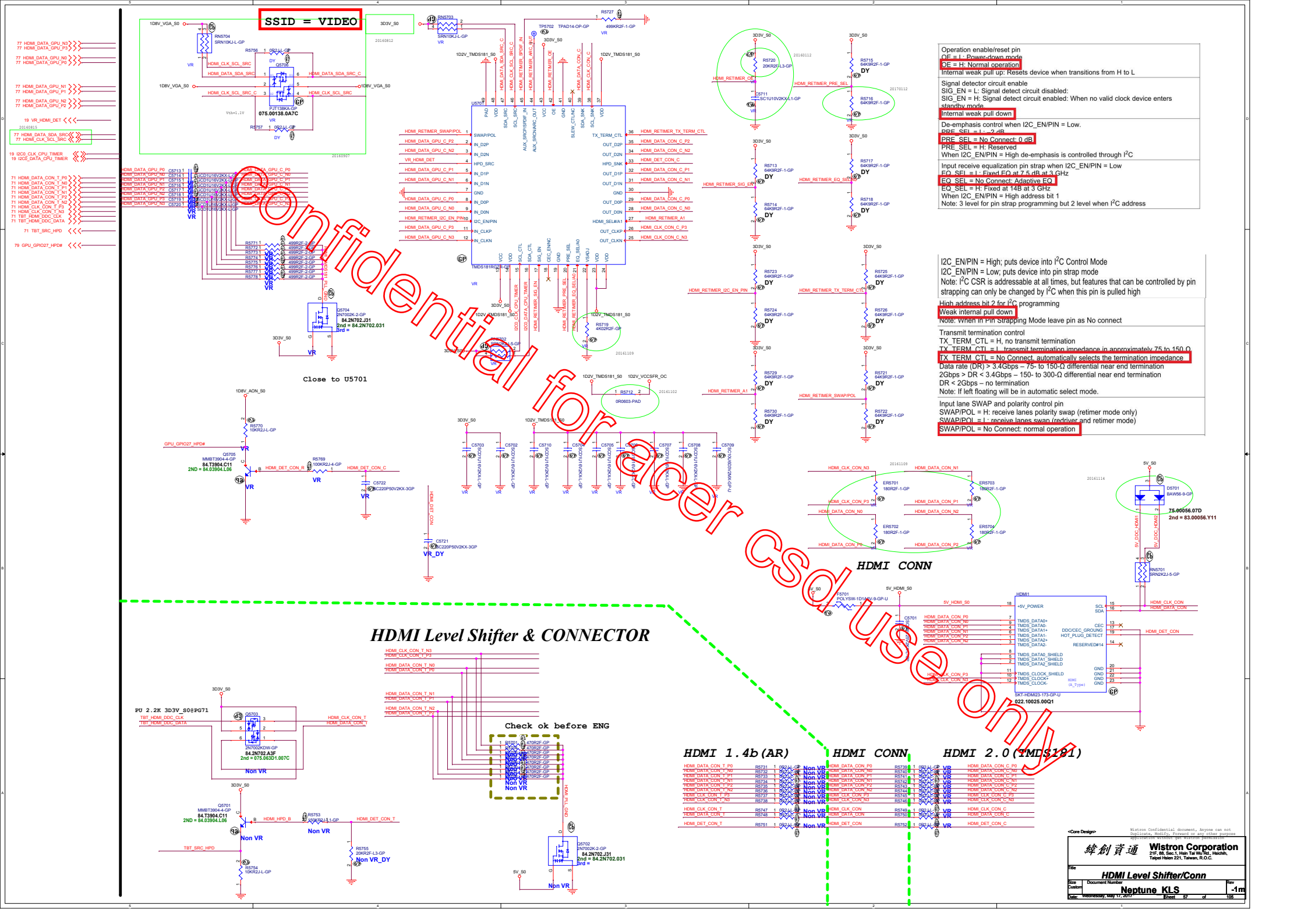
Title: ***(Reserved)***

Size	Document Number	Rev
A	Neptune_KLS	-1m

Date: Wednesday, May 17, 2017 Sheet 56 of 105


SSID = VIDEO
HDMI Level Shifter & CONNECTOR
HDMI 1.4b(AR)
HDMI CONN
HDMI 2.0(TMDS181)
Close to U5701
Check ok before ENG
Confidential for acer csq use only
Operation enable/reset pin
OE = L: Power-down mode
OE = H: Normal operation
Internal weak pull up: Resets device when transitions from H to L
Signal detector circuit enable
SIG_EN = L: Signal detect circuit disabled:
SIG_EN = H: Signal detect circuit enabled: When no valid clock device enters standby mode
Internal weak pull down
De-emphasis control when I2C_EN/PIN = Low.
PRE_SEL = L : -2 dB
PRE_SEL = No Connect: 0 dB
PRE_SEL = H: Reserved
When I2C_EN/PIN = High de-emphasis is controlled through I2C
Input receive equalization pin strap when I2C_EN/PIN = Low
EQ_SEL = L : Fixed EQ at 7.5 dB at 3 GHz
EQ_SEL = No Connect: Adaptive EQ
EQ_SEL = H: Fixed at 14B at 3 GHz
When I2C_EN/PIN = High address bit 1
Note: 3 level for pin strap programming but 2 level when I2C address
I2C_EN/PIN = High; puts device into I2C Control Mode
I2C_EN/PIN = Low; puts device into pin strap mode
Note: I2C CSR is addressable at all times, but features that can be controlled by pin strapping can only be changed by I2C when this pin is pulled high
High address bit 2 for I2C programming
Weak internal pull down
Note: When in Pin Strapping Mode leave pin as No connect
Transmit termination control
TX_TERM_CTL = H, no transmit termination
TX_TERM_CTL = L, transmit termination impedance in approximately 75 to 150 Ω
TX_TERM_CTL = No Connect, automatically selects the termination impedance
Data rate (DR) > 3.4Gbps – 75- to 150-Ω differential near end termination
2Gbps > DR < 3.4Gbps – 150- to 300-Ω differential near end termination
DR < 2Gbps – no termination
Note: If left floating will be in automatic select mode.
Input lane SWAP and polarity control pin
SWAP/POL = H: receive lanes polarity swap (retimer mode only)
SWAP/POL = L : receive lanes swap (redriver and retimer mode)
SWAP/POL = No Connect: normal operation
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HDMI Level Shifter/Conn
Neptune_KLS
-1m

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Title: ***(Reserved)***

Size	Document Number	Rev
A	Neptune_KLS	-1m

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Title: ***(Reserved)***

Size	Document Number	Rev
A	Neptune_KLS	-1m

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16 HDD1_SATA_RX_N
16 HDD1_SATA_RX_P

16 HDD1_SATA_TX_N
16 HDD1_SATA_TX_P

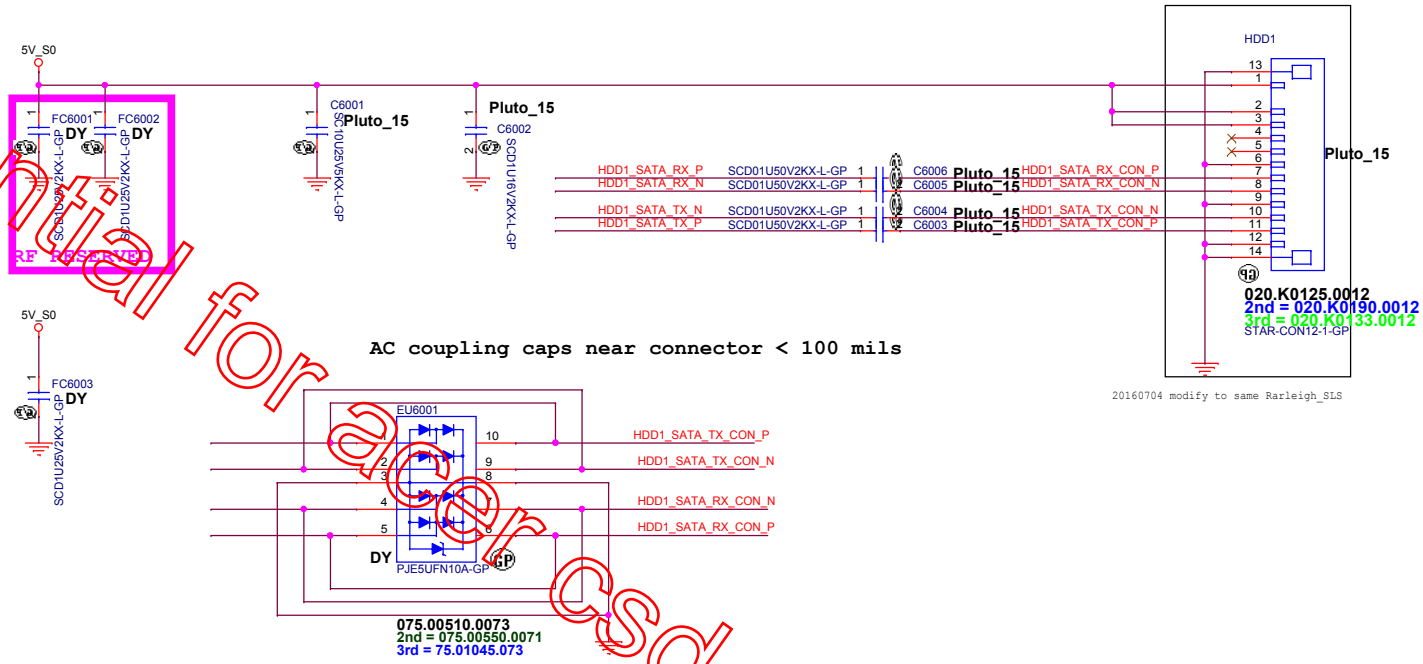
AFTP TESTPOINT

89 HDD1_SATA_TX_CON_P
89 HDD1_SATA_TX_CON_N

89 HDD1_SATA_RX_CON_P
89 HDD1_SATA_RX_CON_N

SSID = SATA

SATA HDD1 Connector



<Core Design>

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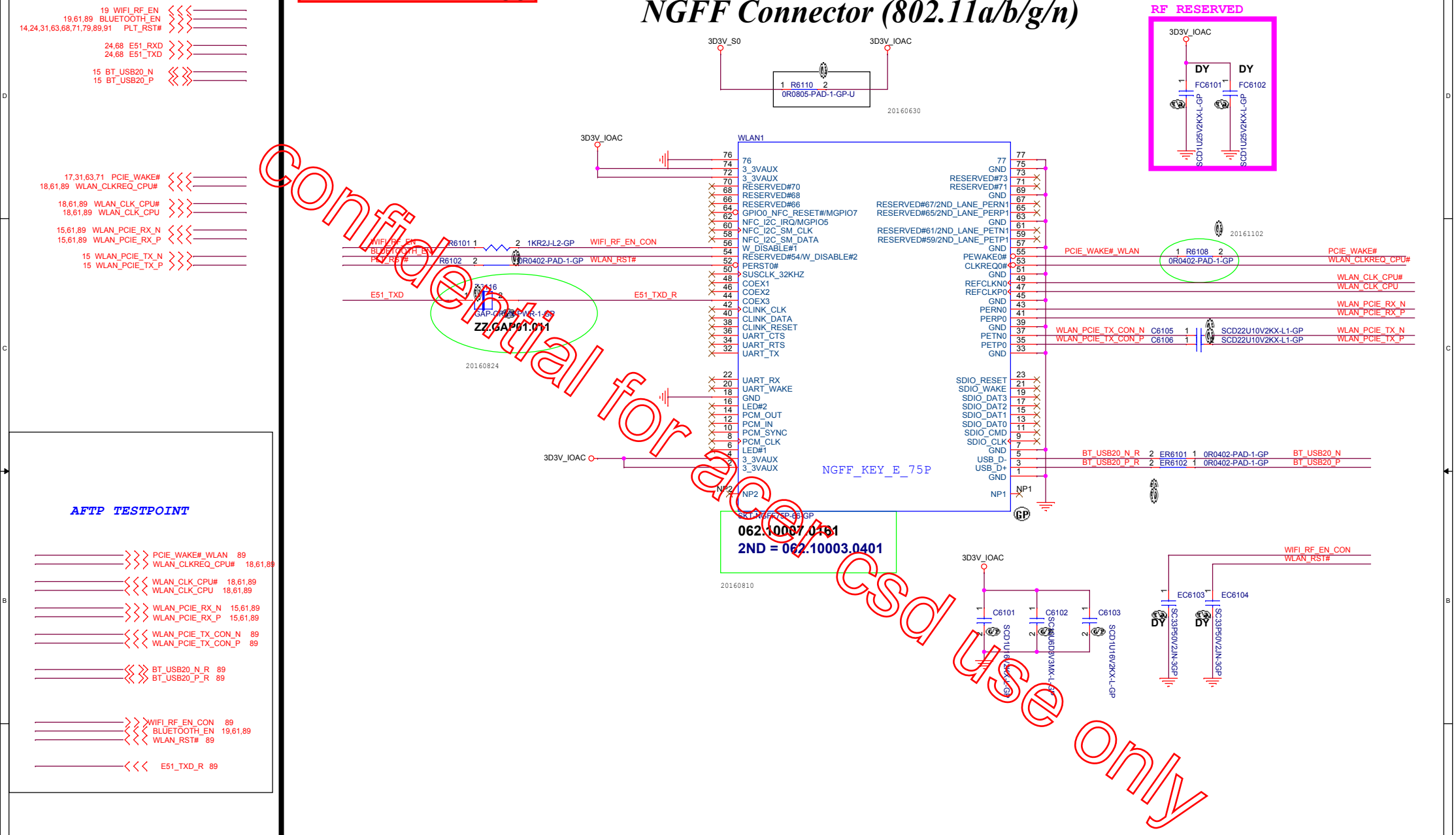
Title: HDD/ODD

Size	Document Number	Rev
Custom	Neptune_KLS	-1m

Date: Wednesday, May 17, 2017 Sheet 60 of 105

SSID = Wireless/ Wigig

NGFF Connector (802.11a/b/g/n)



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Title: Mini card-WLAN

Size: A3 | Document Number: Neptune_KLS | Rev: -1m

Date: Wednesday, May 17, 2017 | Sheet 61 of 105

SSID = Wireless

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Title: ***(Reserved)WWAN***

Size	Document Number	Rev
A	Neptune_KLS	-1m

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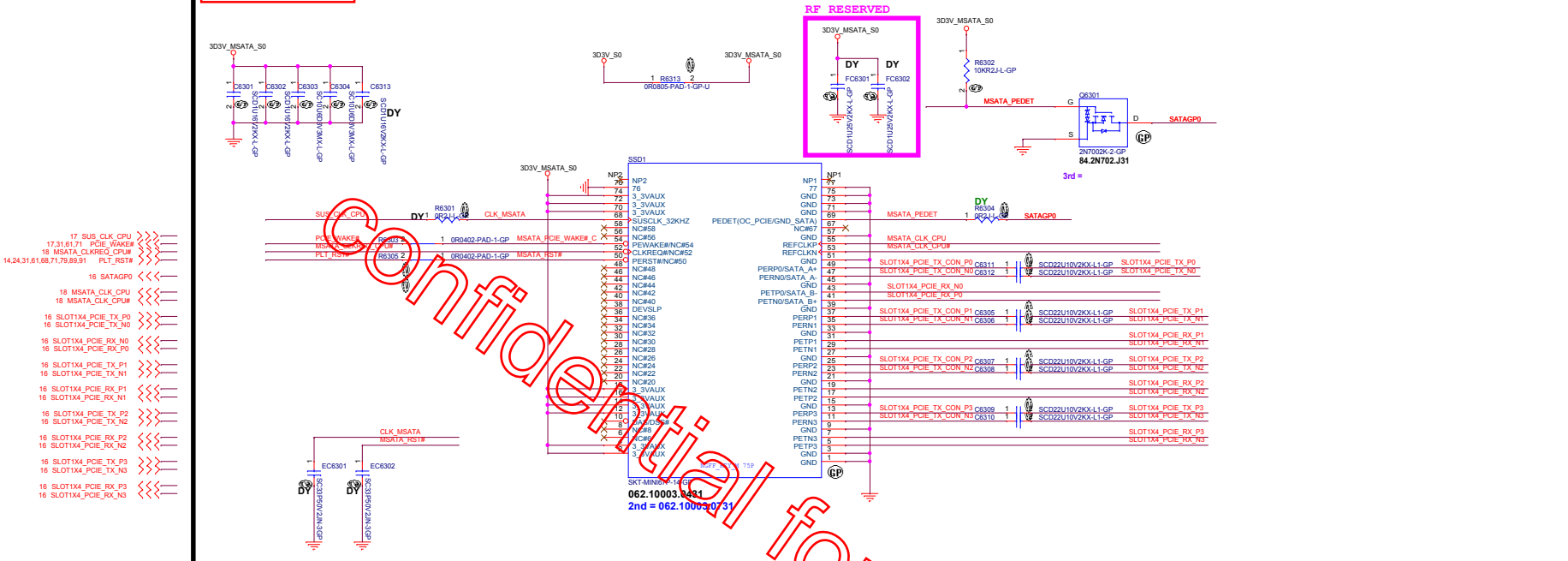
Mini Card Connector (NGFF m-SATA)

SSID = m-SATA



17 SUS_CLK_CPU
17,31,61,71 PCIE_WAKE#
18 MSATA_CLKREQ_CPU#
14,24,31,61,68,71,79,89,91 PLT_RST#
16 SATAGP0
18 MSATA_CLK_CPU
18 MSATA_CLK_CPU#
16 SLOT1X4_PCIE_TX_P0
16 SLOT1X4_PCIE_TX_N0
16 SLOT1X4_PCIE_RX_N0
16 SLOT1X4_PCIE_RX_P0
16 SLOT1X4_PCIE_TX_P1
16 SLOT1X4_PCIE_TX_N1
16 SLOT1X4_PCIE_RX_P1
16 SLOT1X4_PCIE_RX_N1
16 SLOT1X4_PCIE_TX_P2
16 SLOT1X4_PCIE_TX_N2
16 SLOT1X4_PCIE_RX_P2
16 SLOT1X4_PCIE_RX_N2
16 SLOT1X4_PCIE_TX_P3
16 SLOT1X4_PCIE_TX_N3
16 SLOT1X4_PCIE_RX_P3
16 SLOT1X4_PCIE_RX_N3

Table 34-5. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:
1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.

<Core_Design>

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Title: SSD-NGFF

Size	Document Number	Rev
A2	Neptune_KLS	-1m

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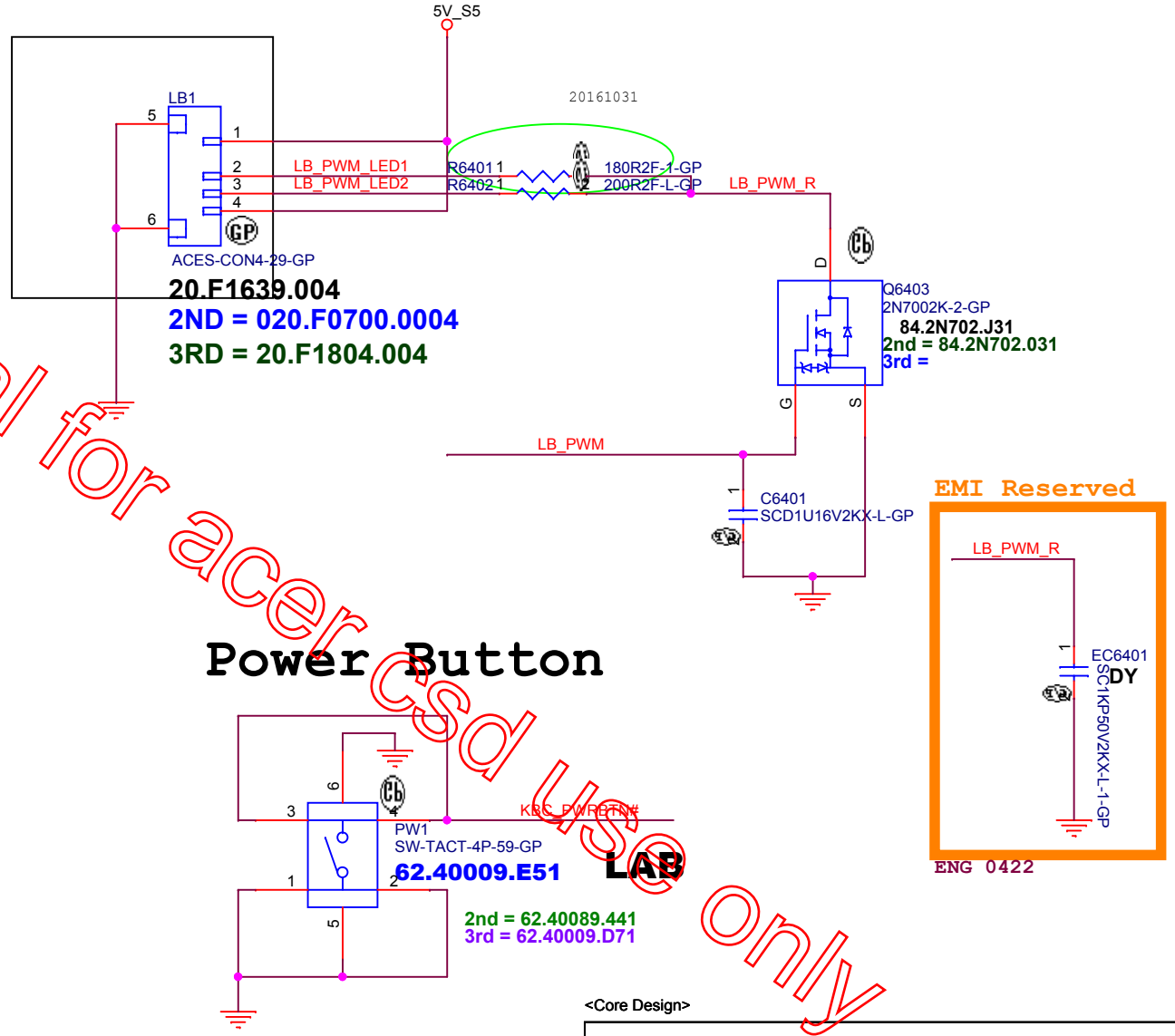
SSID = User.Interface

24 LB_PWM
24,65,89 KBC_PWRBTN#



AFTP TESTPOINT

89 LB_PWM_LED1
89 LB_PWM_LED2

<Core Design>

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Title: LED Bard/Power Button

Size	Document Number	Rev
A4	Neptune_KLS	-1m

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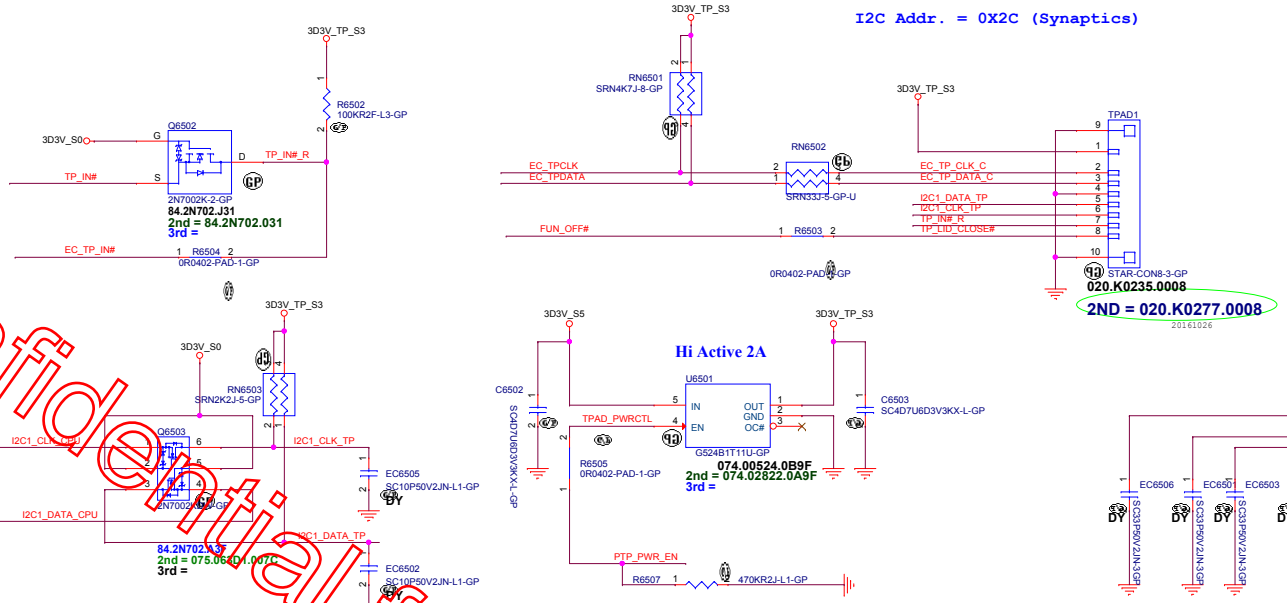
Precision Touch Pad

I2C Addr. = 0X2C (Synaptics)



14 TP_IN#
24 EC_TP_IN#
19 I2C1_CLK_CPU
19 I2C1_DATA_CPU
24 EC_TPCLK
24 EC_TPDATA
24 FUN_OFF#
24 PTP_PWR_EN
24,64,89 KBC_PWRBTN#
24 KB_BL_PWM
19 KB_BL_DET
20160623

24,89 KROW[0..17]
24,89 KCOL[0..7]
24 NUMLOCK_LED
24 CAPS_LED
20160630

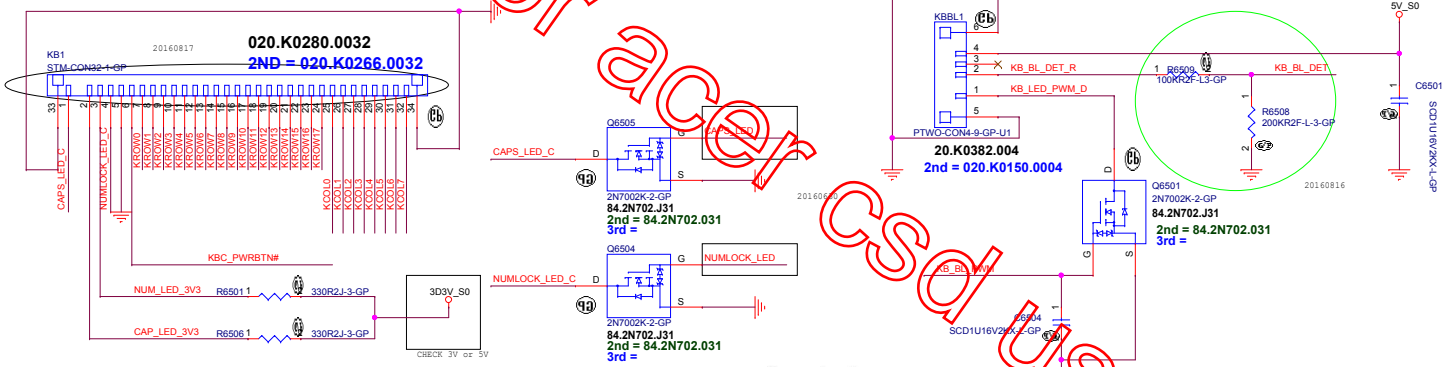
AFTP TESTPOINT

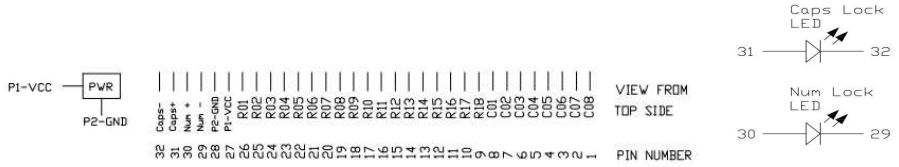
KB_BL_DET_R 89
EC_TP_CLK_C 89
EC_TP_DATA_C 89
I2C1_DATA_TP 89
I2C1_CLK_TP 89
TP_IN#_R 89
TP_LID_CLOSE# 89

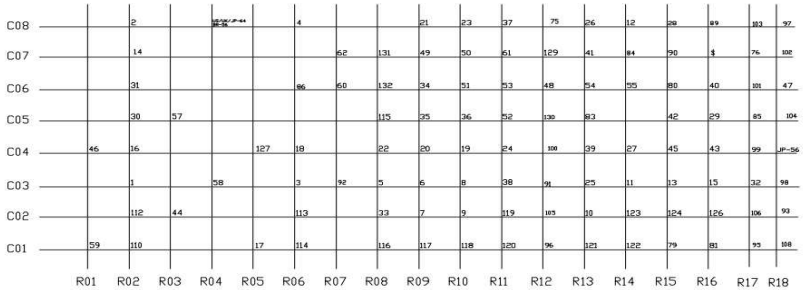
KB_LED_PWM_D 89

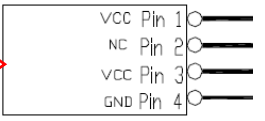
AFTP TEST POINT

Internal KeyBoard Connector









KB_LED_PWM_D
EC6507
SC33P50V2JN-3GP

<Core Design>

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Title: **LED Bard / Power Button**

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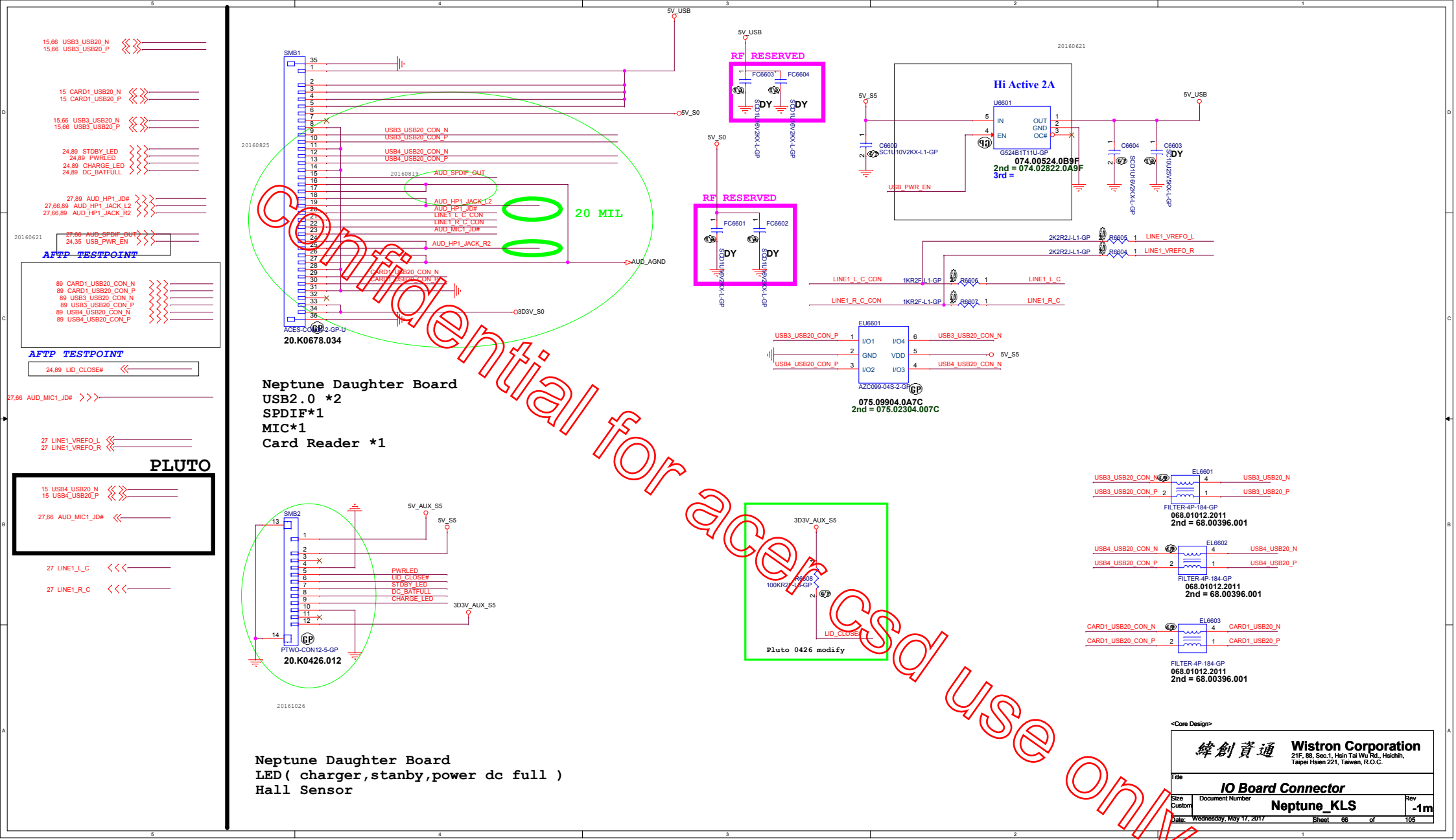
15,66 USB3_USB20_N
15,66 USB3_USB20_P
15 CARD1_USB20_N
15 CARD1_USB20_P
15,66 USB3_USB20_N
15,66 USB3_USB20_P
24,89 STDBY_LED
24,89 PWRLED
24,89 CHARGE_LED
24,89 DC_BATFULL
27,89 AUD_HP1_JD#
27,66,89 AUD_HP1_JACK_L2
27,66,89 AUD_HP1_JACK_R2
20160621
27,66 AUD_SPDIF_OUT
24,35 USB_PWR_EN
AFTP TESTPOINT
89 CARD1_USB20_CON_N
89 CARD1_USB20_CON_P
89 USB3_USB20_CON_N
89 USB3_USB20_CON_P
89 USB4_USB20_CON_N
89 USB4_USB20_CON_P
AFTP TESTPOINT
24,89 LID_CLOSE#
27,66 AUD_MIC1_JD#
27 LINE1_VREFO_L
27 LINE1_VREFO_R
PLUTO
15 USB4_USB20_N
15 USB4_USB20_P
27,66 AUD_MIC1_JD#
27 LINE1_L_C
27 LINE1_R_C
SMB1
5V_USB
5V_S0
3D3V_S0
AUD_AGND
20160825
20160819
AUD_SPDIF_OUT
AUD_HP1_JACK_L2
AUD_HP1_JD#
LINE1_L_C_CON
LINE1_R_C_CON
AUD_MIC1_JD#
AUD_HP1_JACK_R2
CARD1_USB20_CON_N
CARD1_USB20_CON_P
USB3_USB20_CON_N
USB3_USB20_CON_P
USB4_USB20_CON_N
USB4_USB20_CON_P
ACES-CON35-GP-U
20.K0678.034
20 MIL
RF RESERVED
FC6603
FC6604
FC6601
FC6602
SCD1U16V2KX-L-GP
DY
Hi Active 2A
U6601
IN
OUT
GND
EN
OC#
G524B1T11U-GP
074.00524.0B9F
2nd = 074.02822.0A9F
3rd =
C6602
C6604
C6603
SC1U10V2KX-L1-GP
SCD1U16V2KX-L-GP
SC10U25V8KX-L-GP
USB_PWR_EN
20160621
2K2R2J-L1-GP
R6605
R6604
LINE1_VREFO_L
LINE1_VREFO_R
1KR2F-L1-GP
R6606
R6607
LINE1_L_C
LINE1_R_C
EU6601
I/O1
I/O2
I/O3
I/O4
GND
VDD
5V_S5
AZC099-04S-2-GP
075.09904.0A7C
2nd = 075.02304.007C
Neptune Daughter Board
USB2.0 *2
SPDIF*1
MIC*1
Card Reader *1
SMB2
5V_AUX_S5
PWRLED
LID_CLOSE#
STDBY_LED
DC_BATFULL
CHARGE_LED
3D3V_AUX_S5
PTWO-CON12-5-GP
20.K0426.012
20161026
3D3V_AUX_S5
R6608
100KR2F-L1-GP
LID_CLOSE#
Pluto 0426 modify
EL6601
EL6602
EL6603
FILTER-4P-184-GP
068.01012.2011
2nd = 68.00396.001
Neptune Daughter Board
LED(charger,stanby,power dc full)
Hall Sensor
Confidential for acer csd use only
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
IO Board Connector
Size
Custom
Document Number
Neptune_KLS
Rev
-1m
Date: Wednesday, May 17, 2017
Sheet 66 of 105

<Core Design>

緯創資通 **Wistron Corporation**
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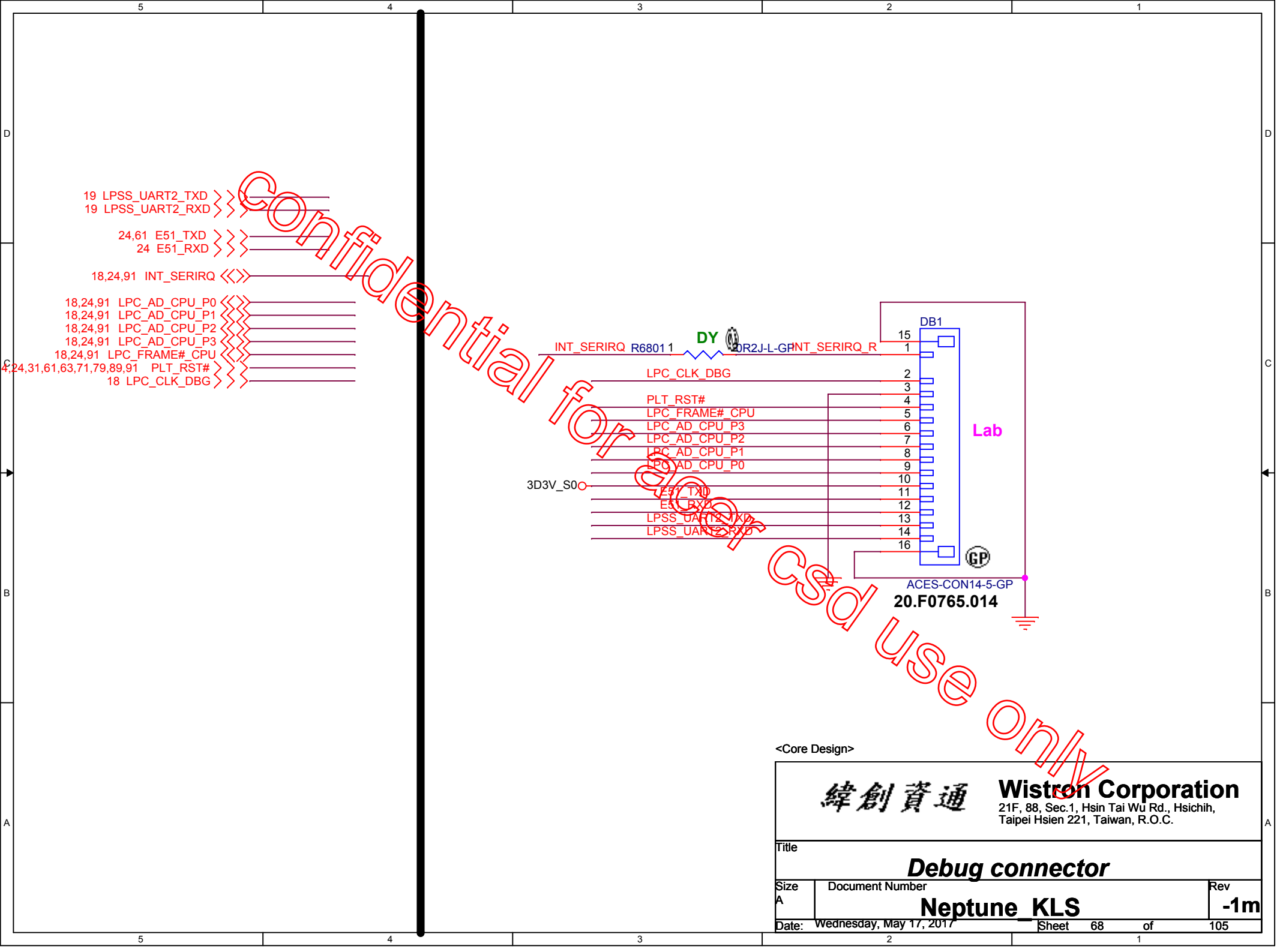
Taipei Hsien 221, Taiwan, R.O.C.

Title
Hall Sensor

Size	Document Number	Rev
A	Neptune_KLS	-1m

Date: Wednesday, May 17, 2017 Sheet 67 of 105


19 LPSS_UART2_TXD
19 LPSS_UART2_RXD
24,61 E51_TXD
24 E51_RXD
18,24,91 INT_SERIRQ
18,24,91 LPC_AD_CPU_P0
18,24,91 LPC_AD_CPU_P1
18,24,91 LPC_AD_CPU_P2
18,24,91 LPC_AD_CPU_P3
18,24,91 LPC_FRAME#_CPU
4,24,31,61,63,71,79,89,91 PLT_RST#
18 LPC_CLK_DBG
INT_SERIRQ
R68011
DY
0R2J-L-GP
INT_SERIRQ_R
DB1
15
1
2
3
4
5
6
7
8
9
10
11
12
13
14
16
LPC_CLK_DBG
PLT_RST#
LPC_FRAME#_CPU
LPC_AD_CPU_P3
LPC_AD_CPU_P2
LPC_AD_CPU_P1
LPC_AD_CPU_P0
3D3V_S0
E51_TXD
E51_RXD
LPSS_UART2_TXD
LPSS_UART2_RXD
Lab
GP
ACES-CON14-5-GP
20.F0765.014
Confidential for acer csd use only
<Core Design>
緯創資通
Wistron Corporation
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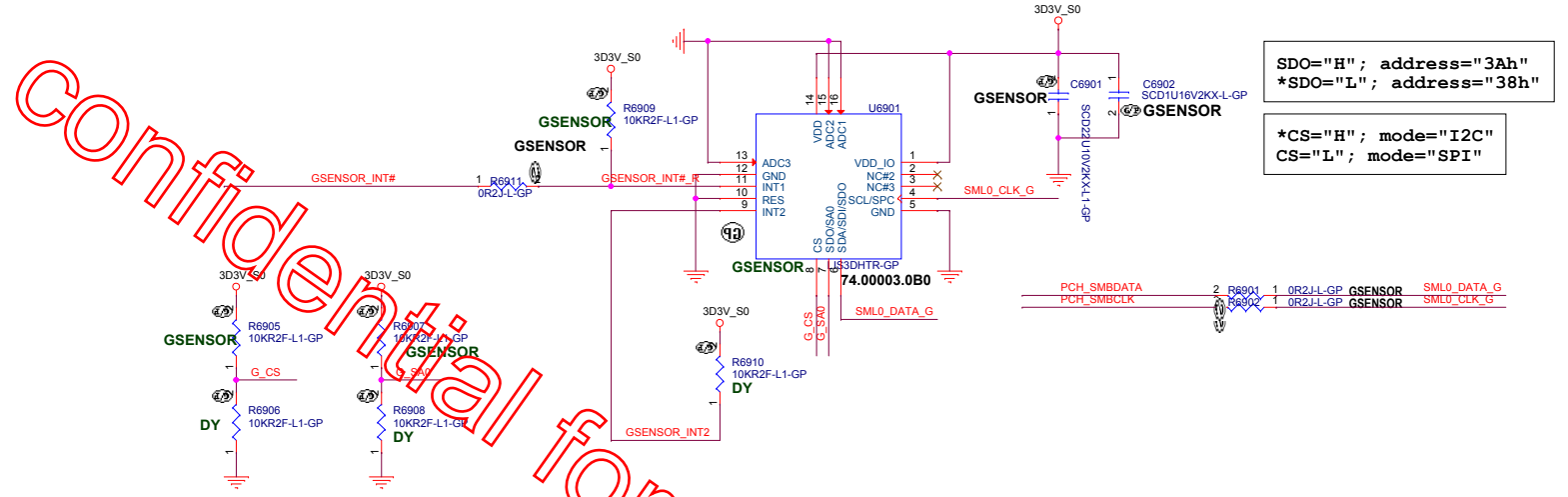
Taipei Hsien 221, Taiwan, R.O.C.
Title
Debug connector
Size
A
Document Number
Neptune_KLS
Rev
-1m
Date: Wednesday, May 17, 2017
Sheet 68 of 105

SSID = User.Interface

G Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

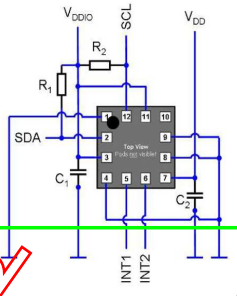
19 GSENSOR_INT#
12,13,17 PCH_SMBDATA
12,13,17 PCH_SMBCLK

Neptune_SKS 0516

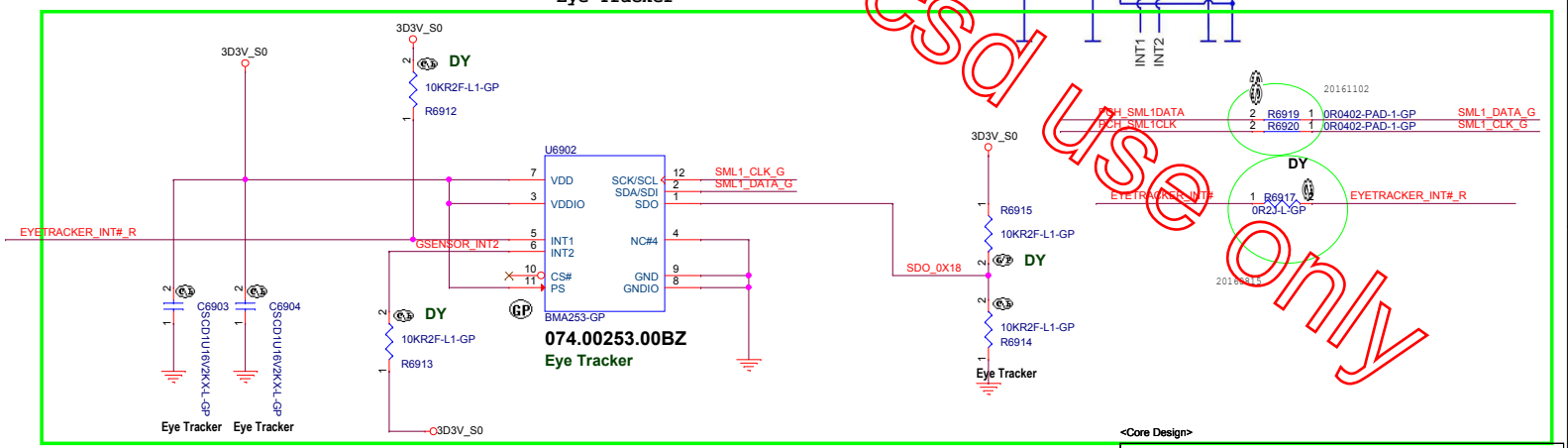
19,24,38 EYETRACKER_INT#
17 PCH_SML1CLK
17 PCH_SML1DATA
38 SML1_DATA_G
38 SML1_CLK_G

SSID = User.Interface

G Sensor
(BMA253 I2C address 0x18)



Eye Tracker



The default I²C address of the device is 0011000b (0x18). It is used if the SDO pin is pulled to 'GND'. The alternative address 0011001b (0x19) is selected by pulling the SDO pin to 'V_{DDIO}'.

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Title: G-SENSOR
Size: Custom | Document Number: Neptune_KLS | Rev: -1m
Date: Wednesday, May 17, 2017 | Sheet 69 of 105

<Core Design>

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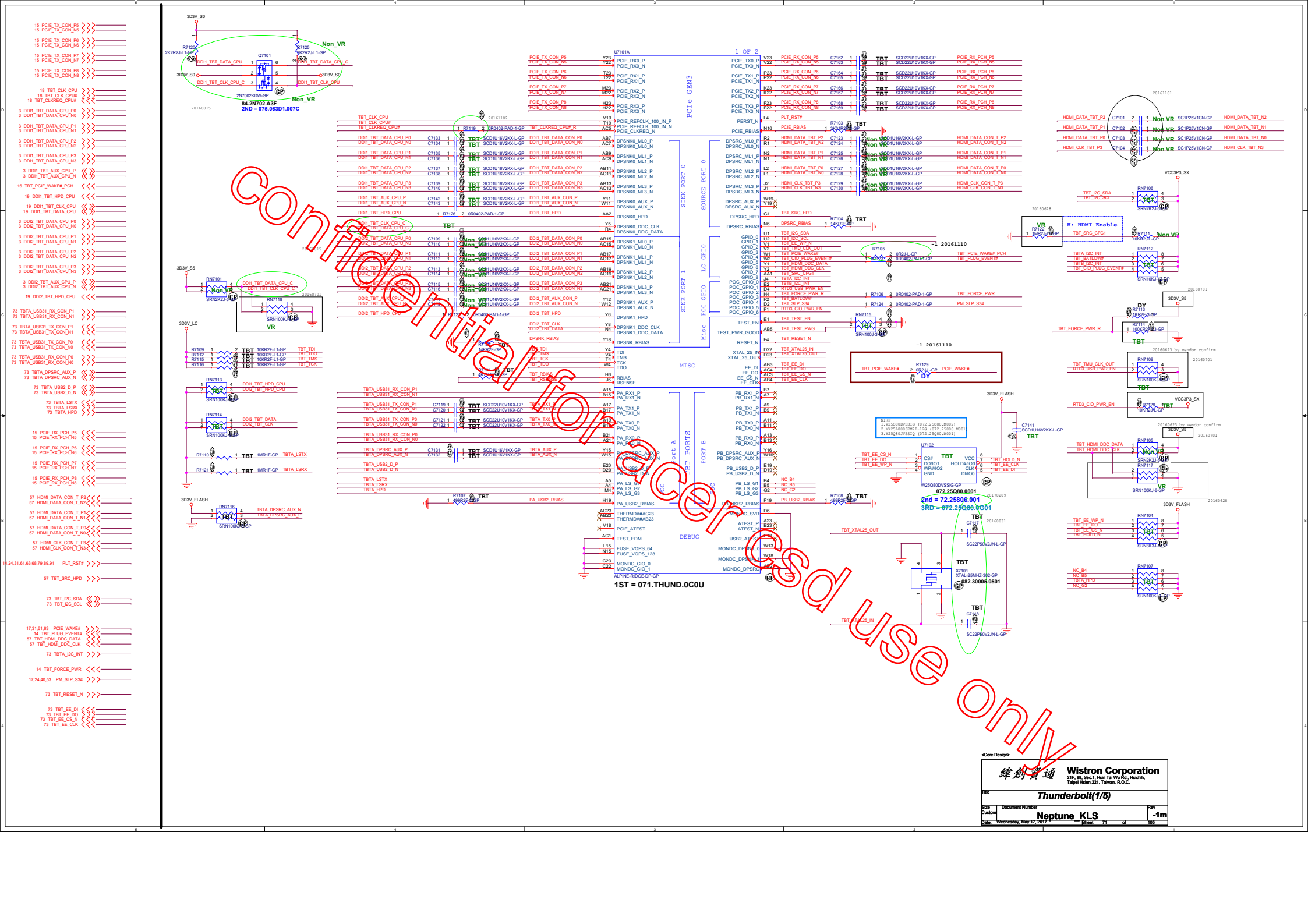
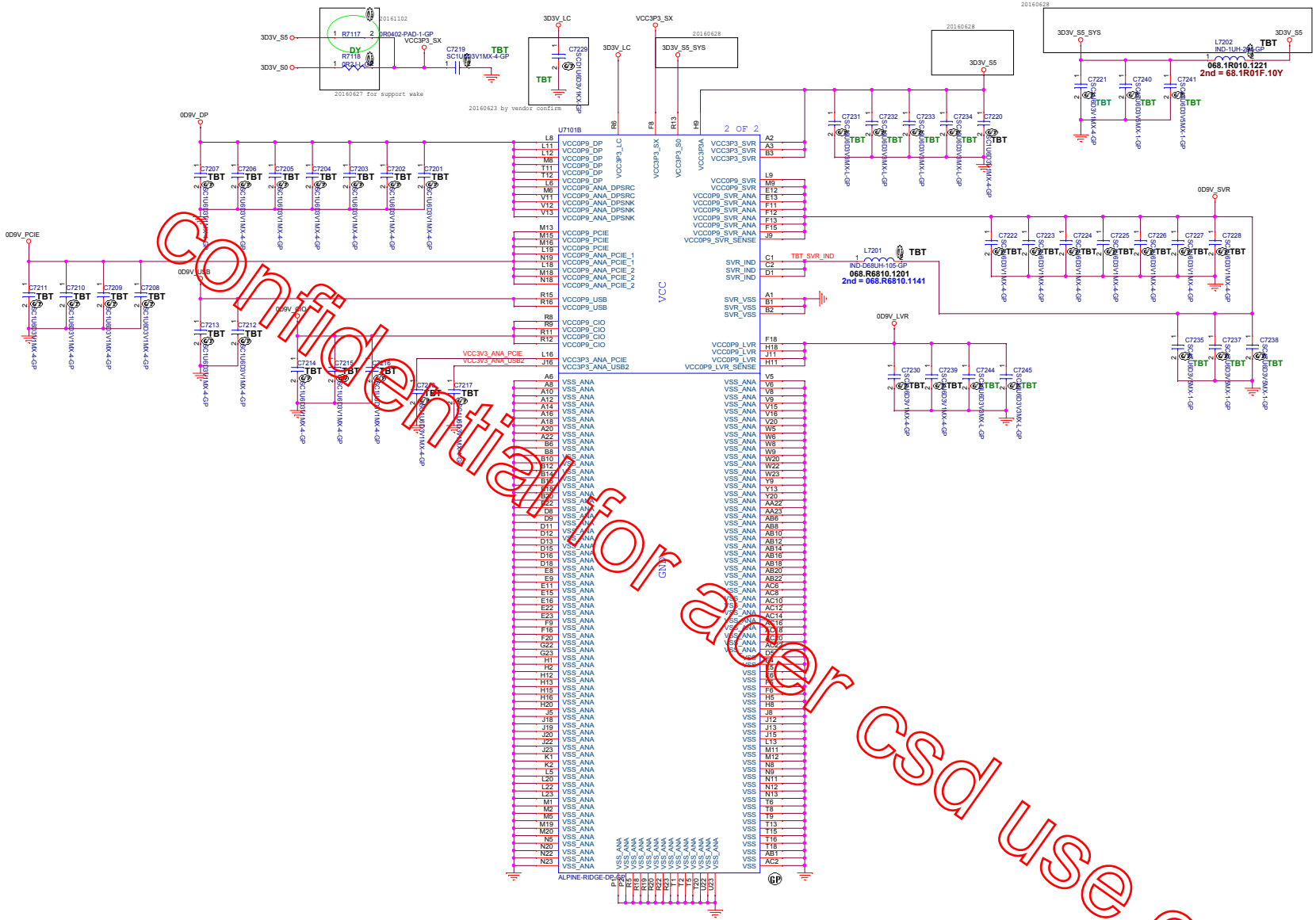
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)Free Fall Sensor

Size	Document Number	Rev
A	**Neptune_KLS**	**-1m**
Date: Wednesday, May 17, 2017	Sheet 70 of 105	





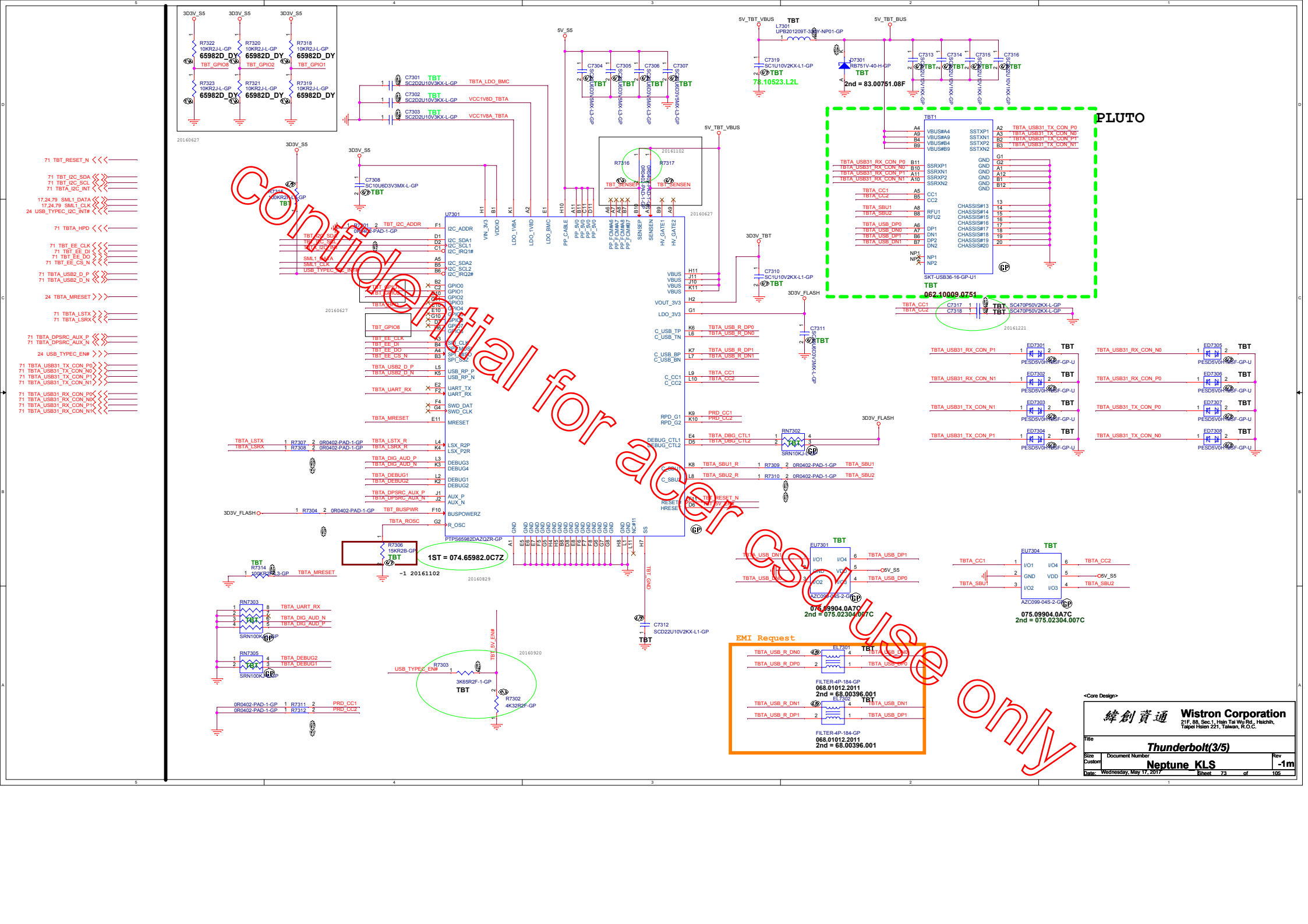
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thunderbolt(2/5)

Size: A2 | Document Number: Neptune_KLS | Rev: -1m

Date: Wednesday, May 17, 2017 | Sheet 72 of 105


PLUTO
Confidential for acer use only
EMI Request
1ST = 074.65982.0C7Z
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Thunderbolt(3/5)
Neptune_KLS
-1m
Wednesday, May 17, 2017
Sheet 73 of 105

<Core Design>

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Title

(Reserved)Thunderbolt (4/5)

Size	Document Number	Rev
A	**Neptune_KLS**	**-1m**

Date: Wednesday, May 17, 2017 Sheet 74 of 105

<Core Design>

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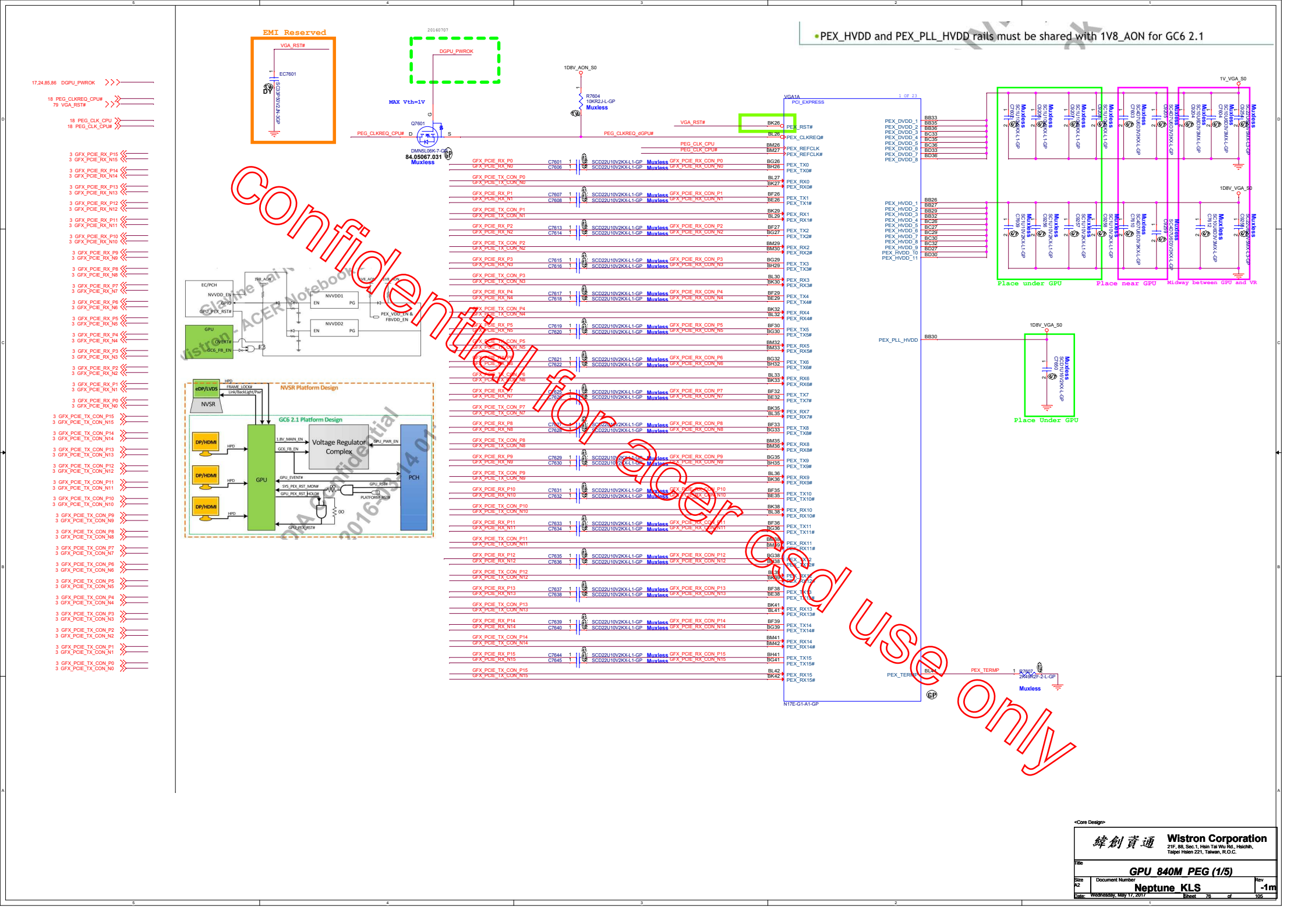
Title

(Reserved)Thunderbolt (5/5)

Size	Document Number	Rev
A	**Neptune_KLS**	**-1m**

Date: Wednesday, May 17, 2017 Sheet 75 of 105



- PEX_HVDD and PEX_PLL_HVDD rails must be shared with 1V8_AON for GC6 2.1

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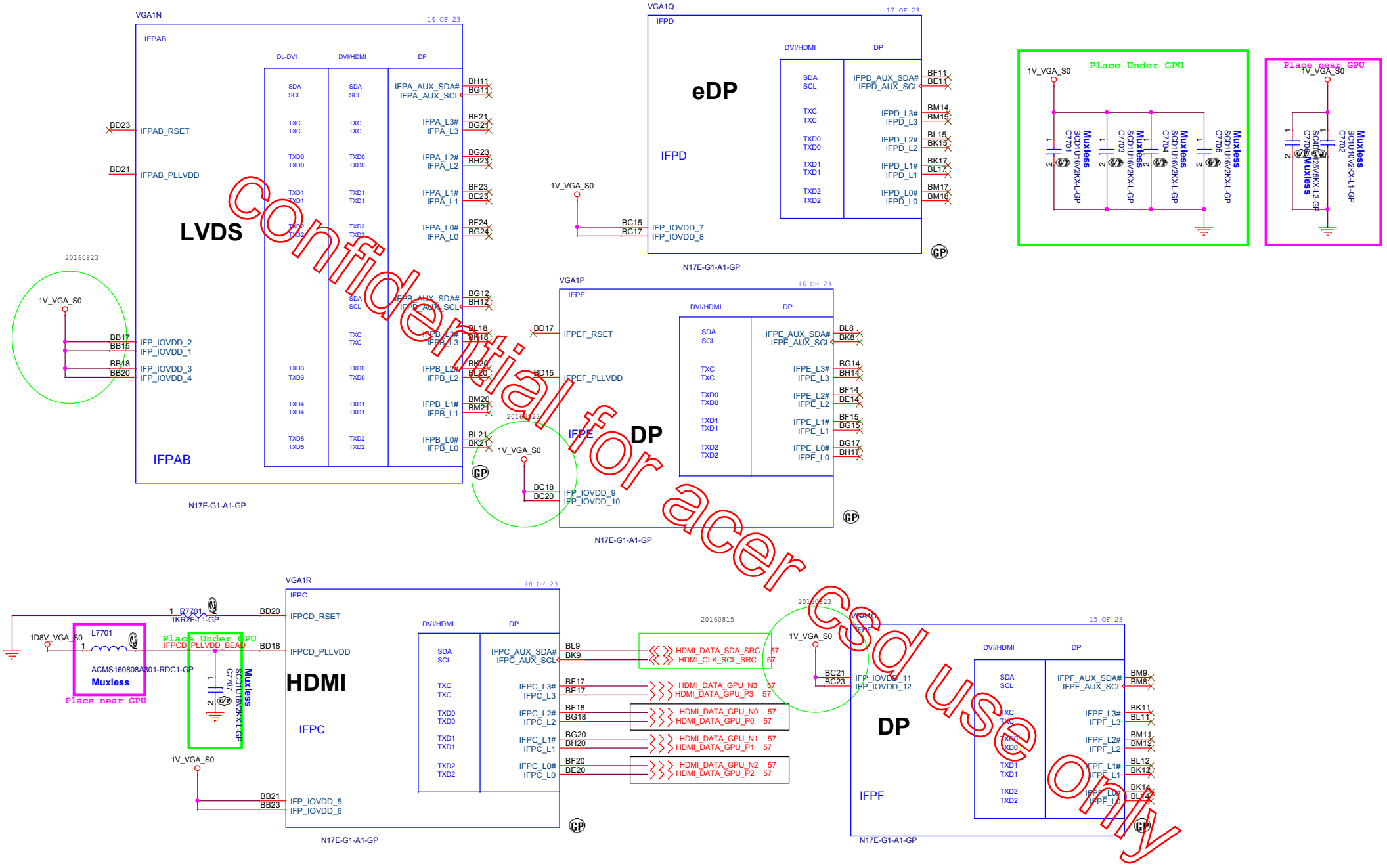
Title: GPU_840M_PEG (1/5)

Size: A2 | Document Number: Neptune_KLS | Rev: -1m

Date: Wednesday, May 17, 2017 | Sheet 78 of 105



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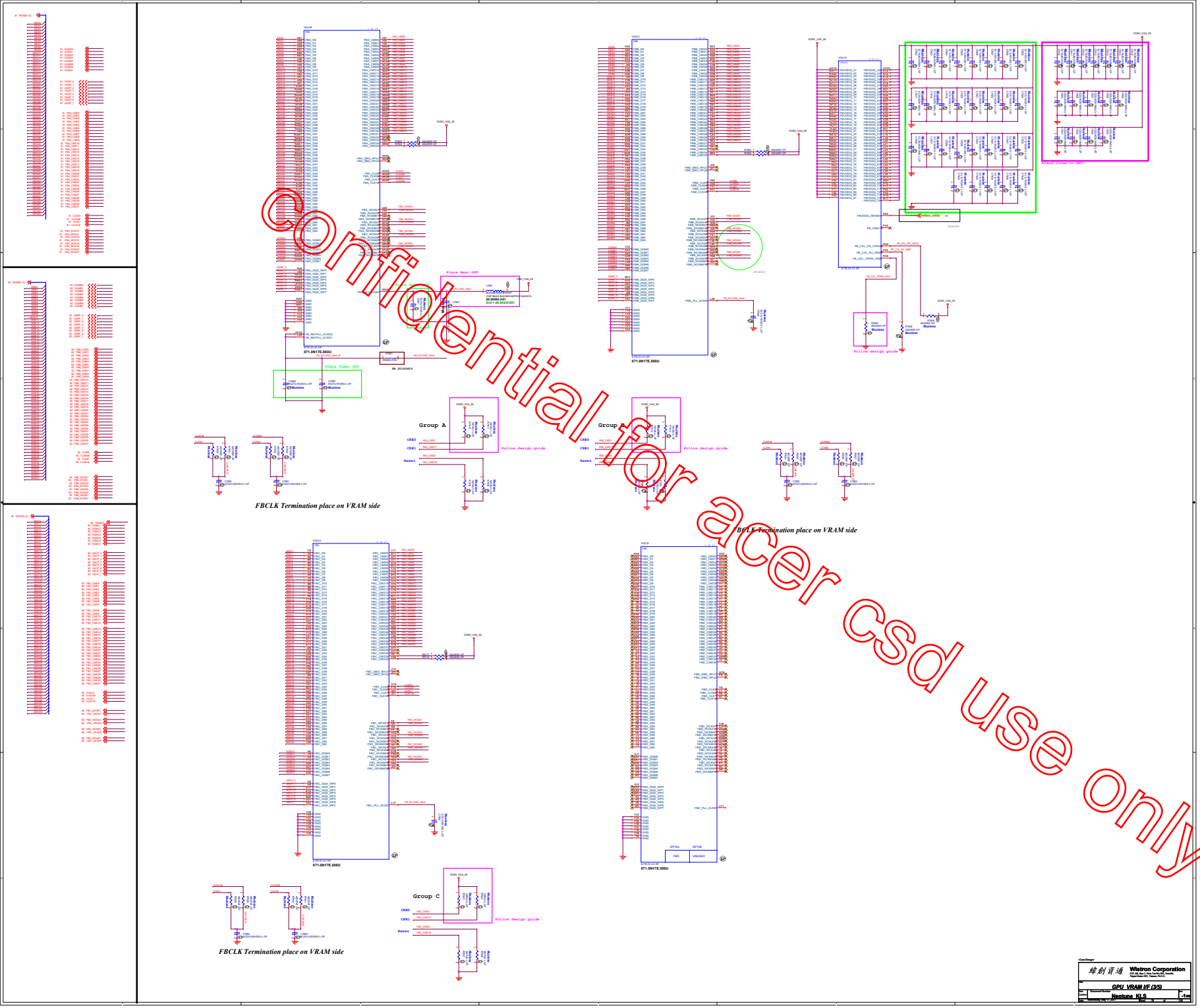
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU_DIGITALOUT (2/5)	
Size A3	Document Number Neptune_KLS	Rev -1m
Date: Wednesday, May 17, 2017	Sheet 77 of 105	


Confidential for acer csd use only
Group A
Group B
Group C
FBCLK Termination place on VRAM side
FBCLK Termination place on VRAM side
FBCLK Termination place on VRAM side
Place Near GPU
Place under GPU
Follow design guide
Wistron Corporation
GPU_VRAM I/F (3/5)
Neptune KL2

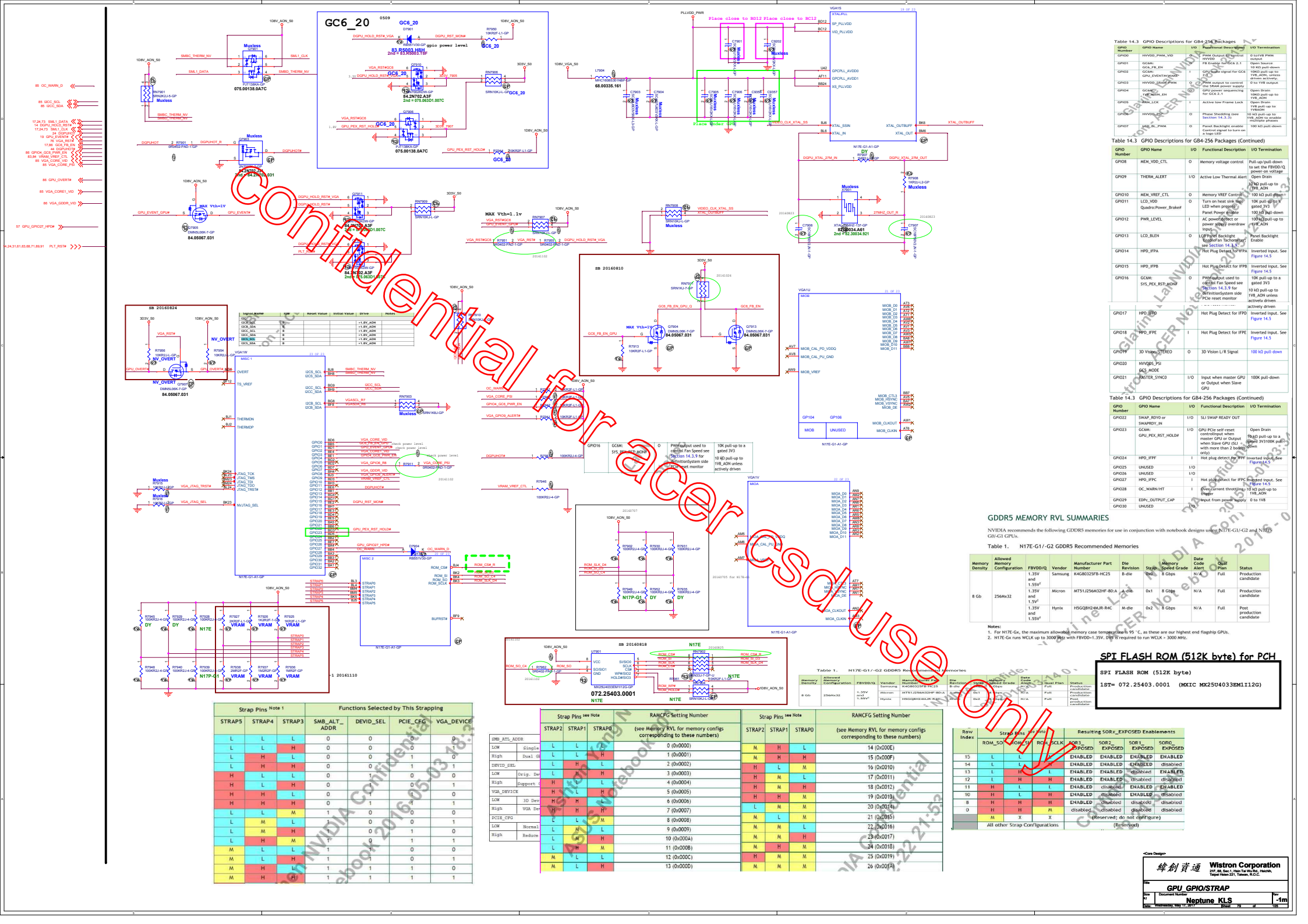


Table 14.3 GPIO Descriptions for GB4-256 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output for control NVVDD	0 to1V8 PWM output
GPIO1	GC6M: GC6_FB_EN	I	FB Enable for GC6 2.1	Open Source 10 kΩ pull-down
GPIO2	GC6M: GPU_EVENT#/WAKE-	I	GPU wake signal for GC6 2.0	10KΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	GC6M: GPU_PWR_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10KΩ pull-up to 1V8_AON
GPIO5	PMU_LCK	I	Active low Frame Lock	Open Drain 1V8 pull-up to 1V8_AON
GPIO6	NVVDD_SSC	O	Phase Shedding (see Section 14.3.3)	Open Drain 10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable Control signal to turn on a logo LED	100 kΩ pull-down

Table 14.3 GPIO Descriptions for GB4-256 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD Quadro:Power_Brake#	O	Turn on heat sink fan LED when present) Panel Power enable	10K pull-up to 3 gated 3V3 100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable/Fan Tachometer; see Section 14.3.2	Panel Backlight Enable
GPIO14	HPD_IFPA	I	Hot Plug Detect for IFPA	Inverted input. See Figure 14.5
GPIO15	HPD_IFPB	I	Hot Plug Detect for IFPB	Inverted input. See Figure 14.5
GPIO16	GC6M: SYS_PEX_RST_MON#	O	PWM output used to control Fan Speed see Section 14.3.9 for definitionSystem side PCIe reset monitor	10K pull-up to a gated 3V3 10 kΩ pull-up to 1V8_AON unless actively driven
GPIO17	HPD_IFPD	I	Hot Plug Detect for IFPD	Inverted input. See Figure 14.5
GPIO18	HPD_IFPE	I	Hot Plug Detect for IFPE	Inverted input. See Figure 14.5
GPIO19	3D Vision_STEREO	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO20	NVVDD5_PSI GC5_MODE			
GPIO21	RASTER_SYNC0	I/O	Input when master GPU or Output when Slave GPU	100K pull-down

Table 14.3 GPIO Descriptions for GB4-256 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO22	SWAP_RDY0 or SWAPRDY_IN	I/O	SLI SWAP READY OUT	
GPIO23	GC6M: GPU_PEX_RST_HOLD#	I/O	GPU PCIe self-reset controlInput when master GPU or Output when Slave GPU (SLI with more than 2 boards only)	Open Drain 10 kΩ pull-up to a gated 3V3100K pull-down
GPIO24	HPD_IFPF	I	Hot plug detect for IFPF	Inverted input. See Figure14.5
GPIO25	UNUSED	I/O		
GPIO26	UNUSED	I/O		
GPIO27	HPD_IFPC	I	Hot plug detect for IFPC	Inverted input. See Figure 14.5
GPIO28	OC_WARN/HT	I	Over-current throttling	10 kΩ pull-up to 1V8_AON
GPIO29	EDPc_OUTPUT_CAP	I	Input from power supply	0 to 1V8
GPIO30	UNUSED	I/O		

GDDR5 MEMORY RVL SUMMARIES

NVIDIA recommends the following GDDR5 memories for use in conjunction with notebook designs using N17E-G1/-G2 and N17P-G1/-G2 GPUs.

Table 1. N17E-G1/-G2 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap_ID	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.55V[2]	Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.5V[2]	Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V[2]	Hynix	H5GQBH24MJR-R4C	M-die	0x2	8 Gbps	N/A	Full	Post production candidate

Notes:
1. For N17E-Gx, the maximum allowable memory case temperature is 95 °C, as these are our highest end flagship GPUs.
2. N17E-Gx runs WCLK up to 3000 MHz with FBVDD=1.35V. DVS is required to run WCLK > 3000 MHz.

Strap Pins Note 1 / Functions Selected by This Strapping

STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

SMB_ALT_ADDR	
LOW	Single
High	Dual C
DEVID_SEL	
LOW	Orig. De
High	Support
VGA_DEVICE	
LOW	3D Dev
High	VGA De
PCIE_CFG	
LOW	Normal
High	Reduce

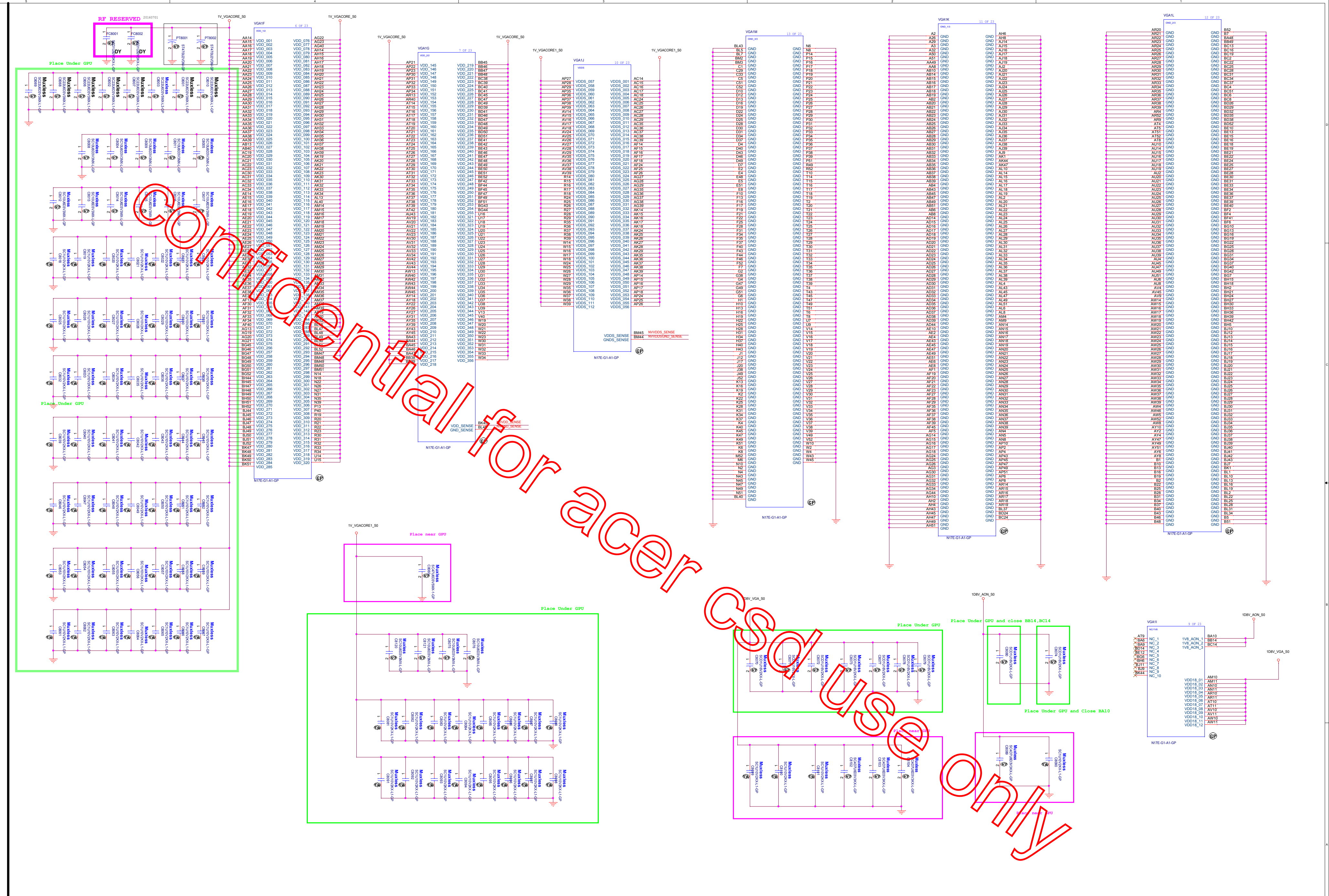
Strap Pins see Note / RAMCFG Setting Number

STRAP2	STRAP1	STRAP0	RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Strap Pins see Note / RAMCFG Setting Number

STRAP2	STRAP1	STRAP0	RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Row Index	Strap Pins			Resulting SOR_EXPOSED Enablements			
	ROM_SO	ROM_CS	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			



<Core Design>

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **GPU_POWER/GND (5/5)**		
Size: Custom	Document Number: **Neptune_KLS**	Rev: **-1m**
Date: Wednesday, May 17, 2017	Sheet 80 of 105	

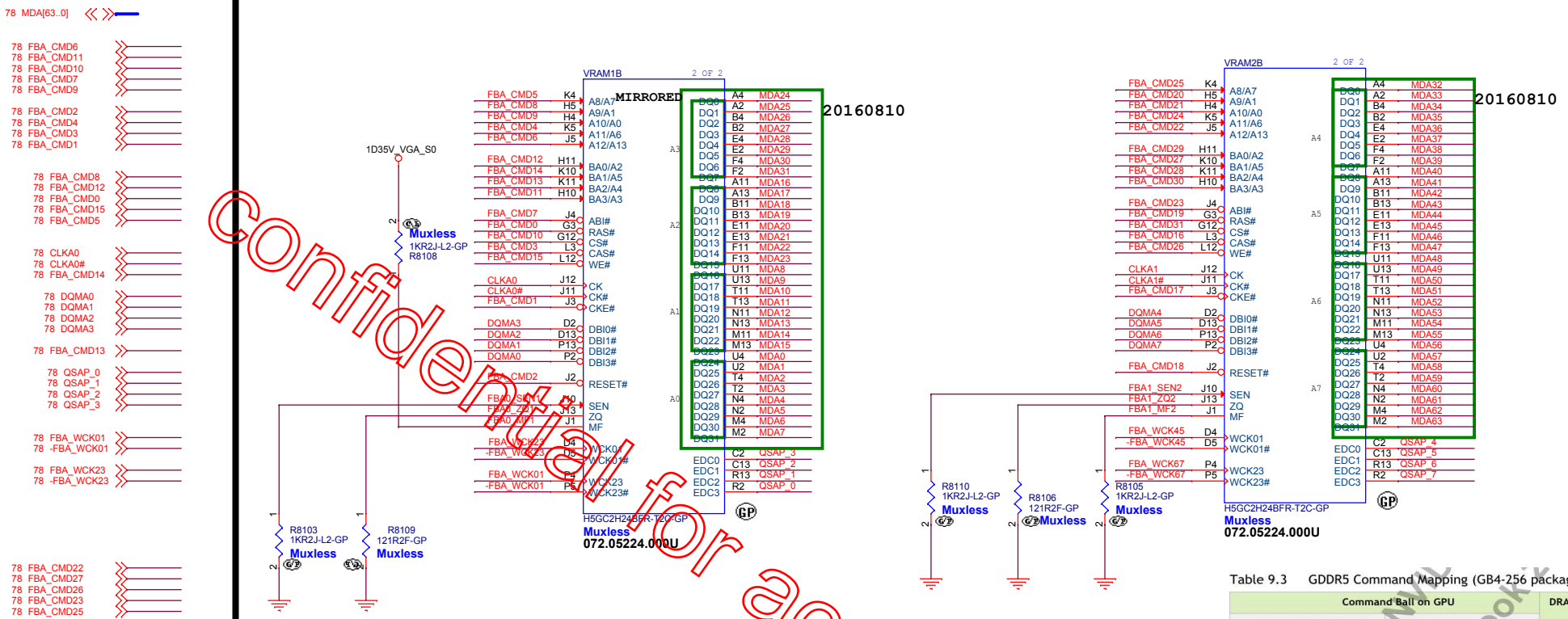


Table 9.3 GDDR5 Command Mapping (GB4-256 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CAS*
FBA_CMD1	FBA_CMD17	CKE*
FBA_CMD2	FBA_CMD18	RST*
FBA_CMD3	FBA_CMD19	RAS*
FBA_CMD4	FBA_CMD20	A1_A9
FBA_CMD5	FBA_CMD21	A0_A10
FBA_CMD6	FBA_CMD22	A12_RFU
FBA_CMD7	FBA_CMD23	ABI*
FBA_CMD8	FBA_CMD24	A6_A11
FBA_CMD9	FBA_CMD25	A7_A8
FBA_CMD10	FBA_CMD26	WE*
FBA_CMD11	FBA_CMD27	A5_BA1
FBA_CMD12	FBA_CMD28	A4_BA2
FBA_CMD13	FBA_CMD29	A2_BA0

Table 9.3 GDDR5 Command Mapping (GB4-256 packages) (Continued)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD14	FBA_CMD30	A3_BA3
FBA_CMD15	FBA_CMD31	CS*

FB CMD mapping Mode H -N15P-GX GDDR5

TABLE
GDDR5 VIDEO MEMORY 72.05224.A0U 72.20325.B0U

	HYNIX 2GBITS (64Mx32)	SAMSUNG 2GBITS (64Mx32)	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)
U91 U92 U93 U94 U95 U96 U97 U98	H5GQ2H24AFR-T2C	K4G20325FD-FC04	H5GC4H24MFR (tentative)	K4G41325FC-HC03 (tentative)

LOGIC

CHECK PM AVL

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Title: VRAM 1,2 (1/4)

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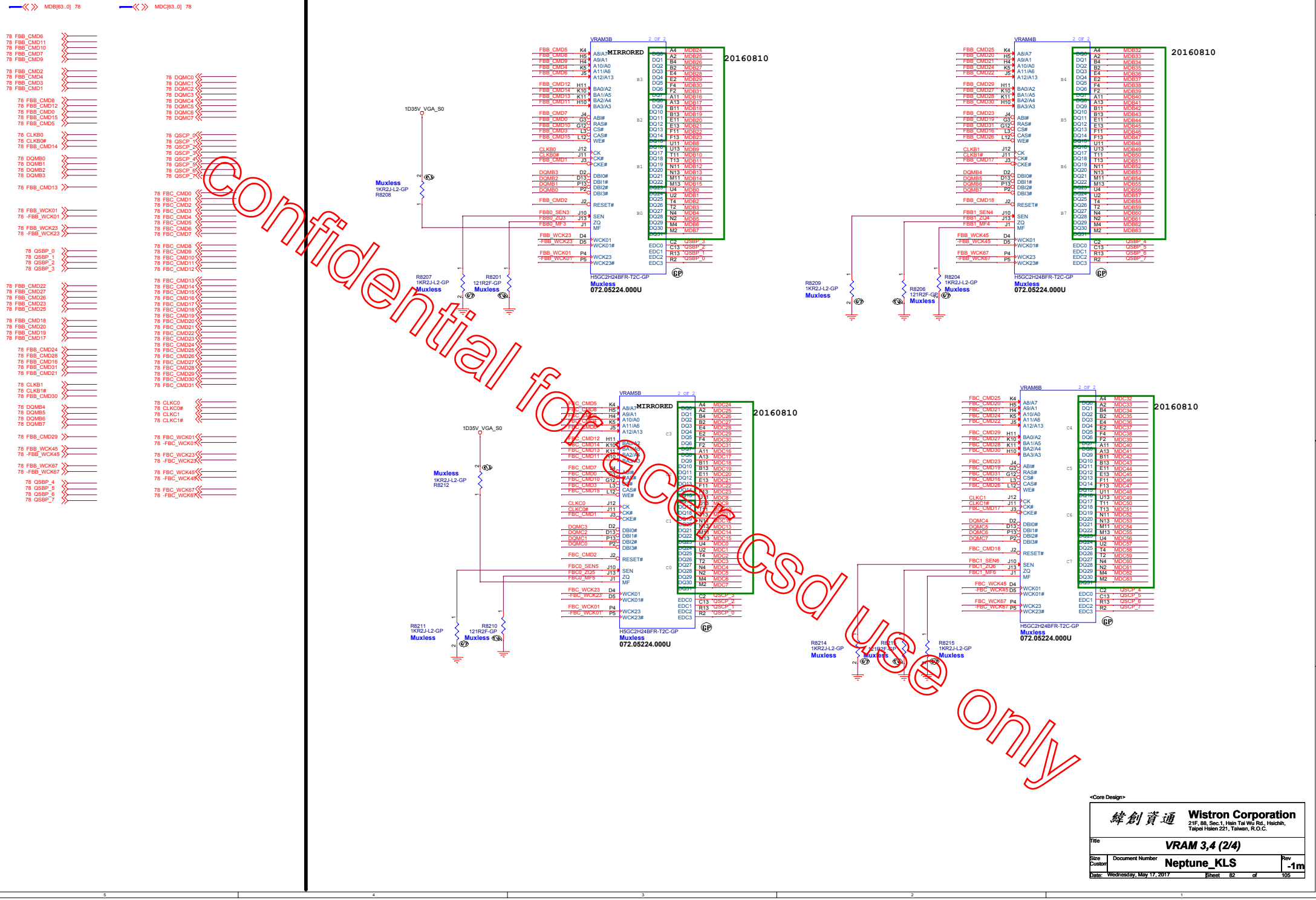

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Title: VRAM 3,4 (2/4)

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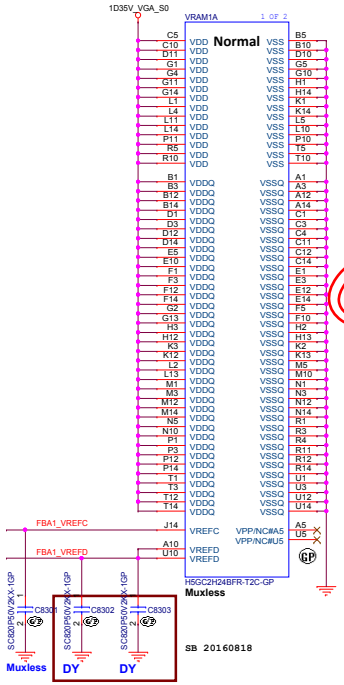

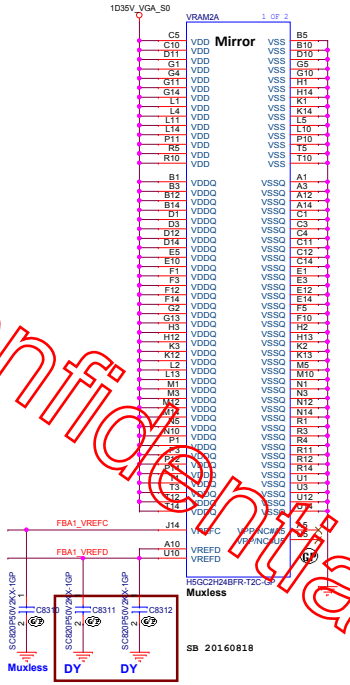

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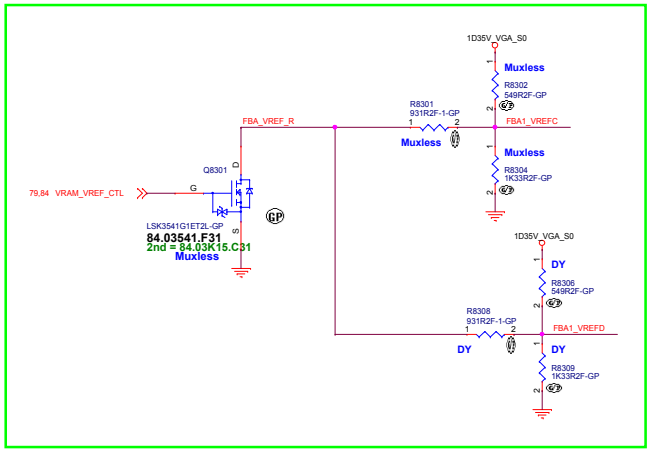

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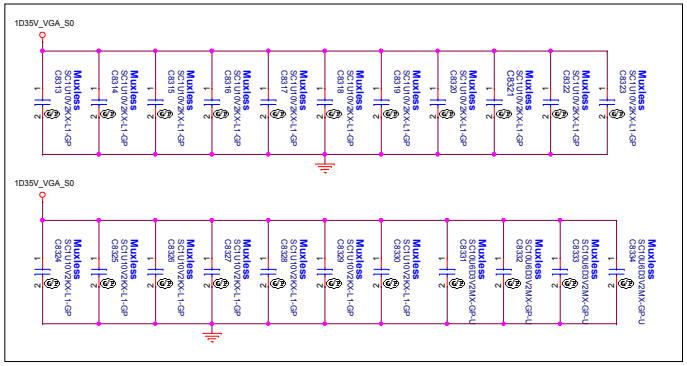

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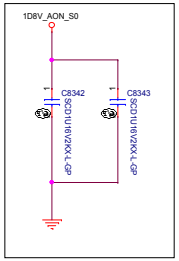

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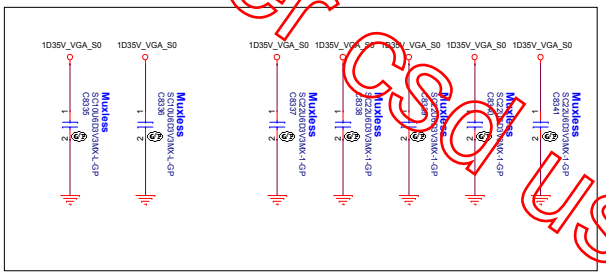
FOR VRAM1/ VRAM2



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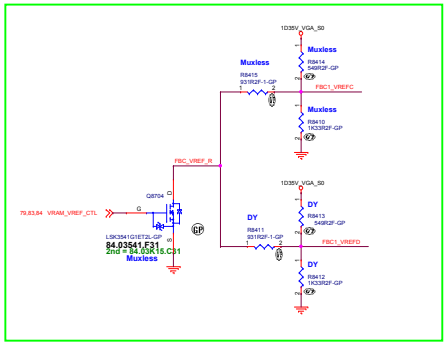

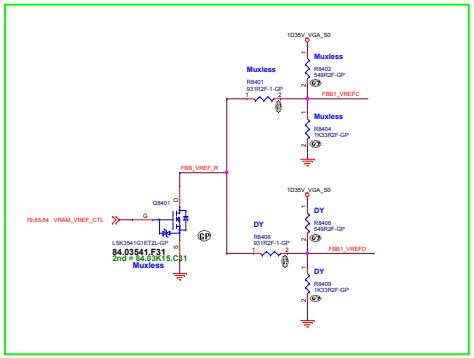

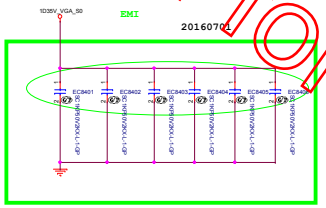

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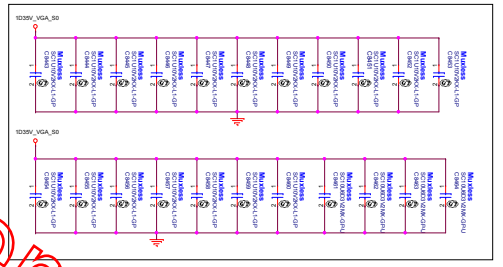

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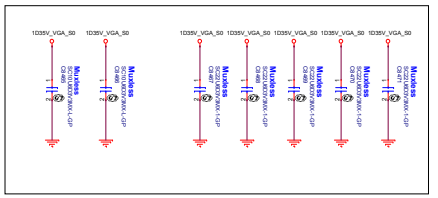

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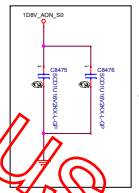

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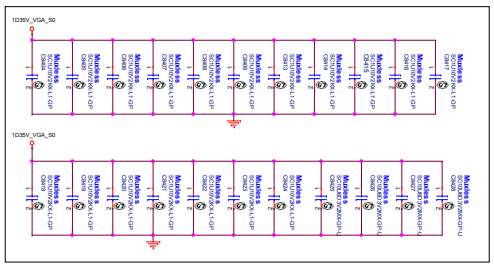
FOR VRAM3/ VRAM4



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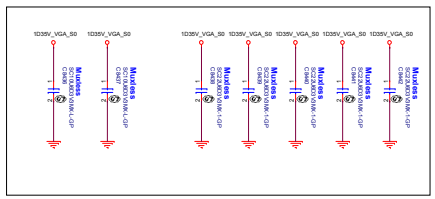

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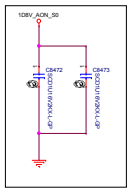

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Title: VGA Power A

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VGA : N17E-G1
Config : B
EDP-Continuous : 58A
EDP-Peak : 136A

CHECK SPEC

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification		
	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.309
C	nF	4.7

RT8816A For NVVDDS

VGA : N17E-G1 / NVVDDS
EDP-Continuous : 28A
EDP-Peak : 74A

N17 E-G1
EDP-Continuous : 62 A
EDP-Peak : 164 A
N17 P-G1
EDP-Continuous : 47 A
EDP-Peak : 90 A

N17 E-G1
EDP-Continuous : 21 A
EDP-Peak : 49 A
N17 P-G1
EDP-Continuous : 16 A
EDP-Peak : 35 A

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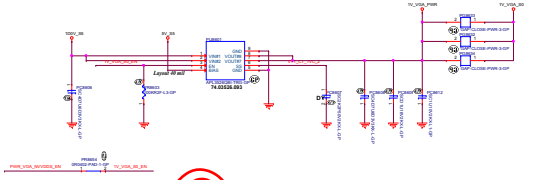
VGA Power 8
Neptune_KLS

APL3526QB for 1V_VGA_S0



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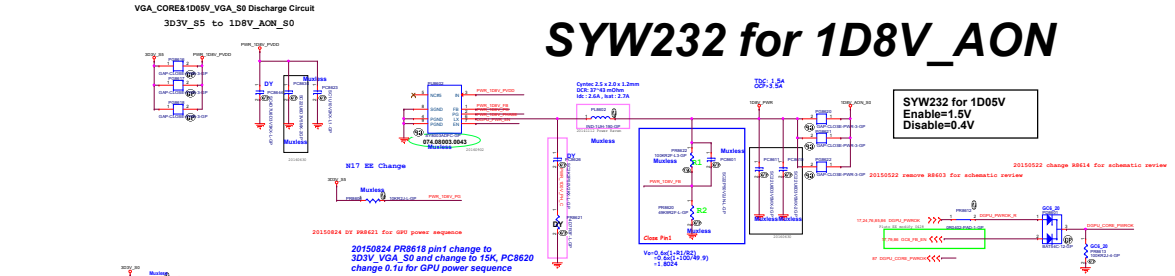

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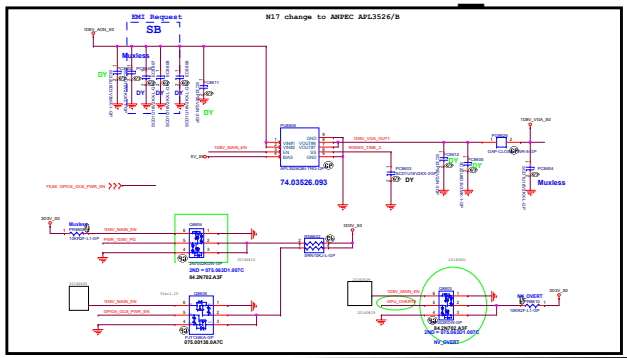


RT8816A for PWR_VGA_GDDR

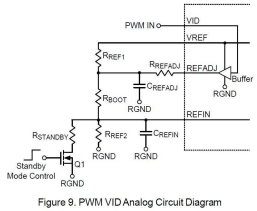


Figure 9. PWM VID Analog Circuit Diagram

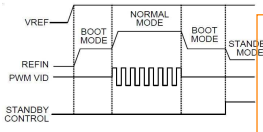
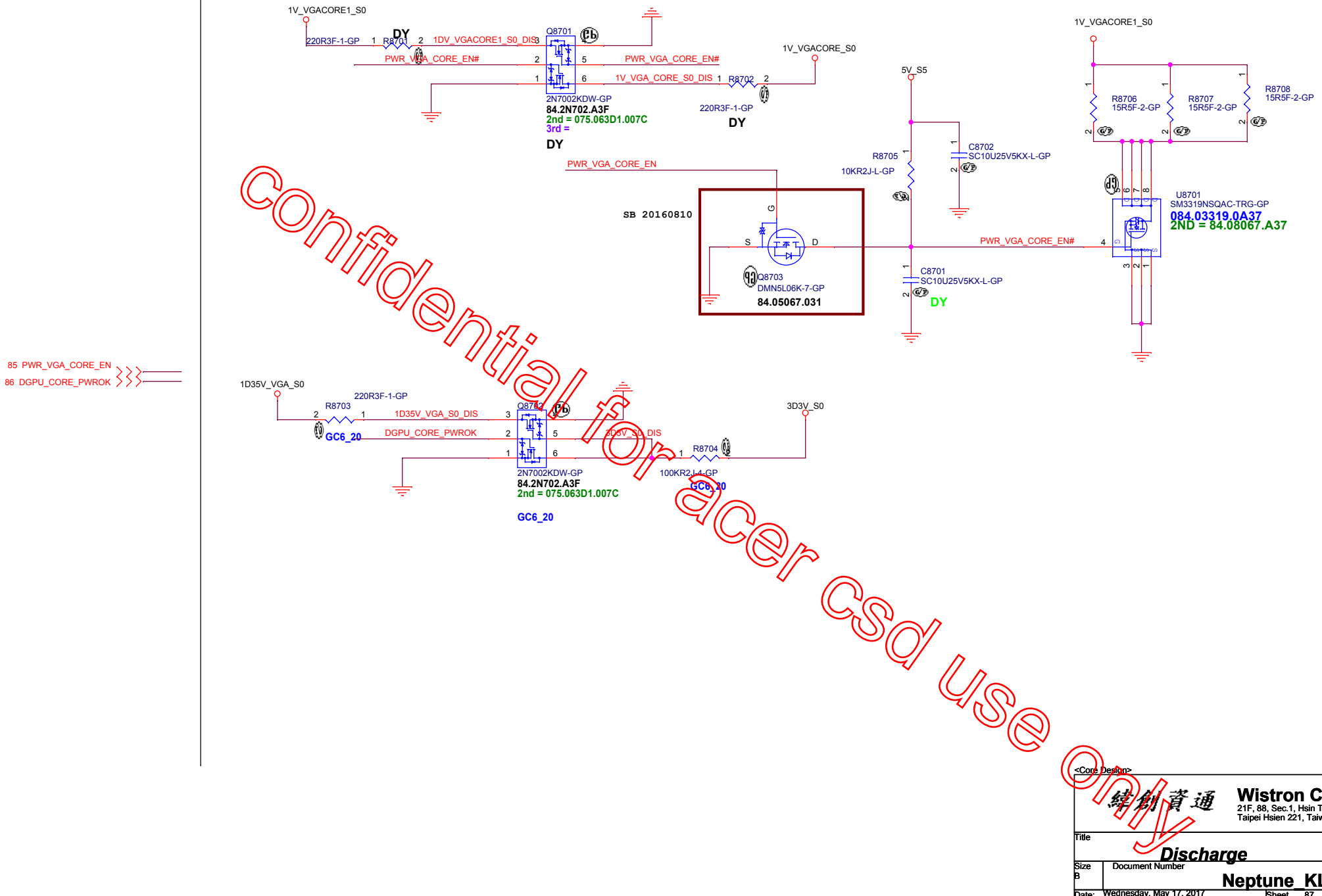


Figure 10. PWM VID Time Diagram

$$V_{BOOT} = V_{VREF} \times \left(\frac{R_{REF2}}{R_{REF1} + R_{REF2} + R_{BOOT}} \right)$$

$$V_{STANDBY} = V_{VREF} \times \frac{R_{REF2} \,//\, R_{STANDBY}}{R_{REF1} + R_{BOOT} + (R_{REF2} \,//\, R_{STANDBY})}$$



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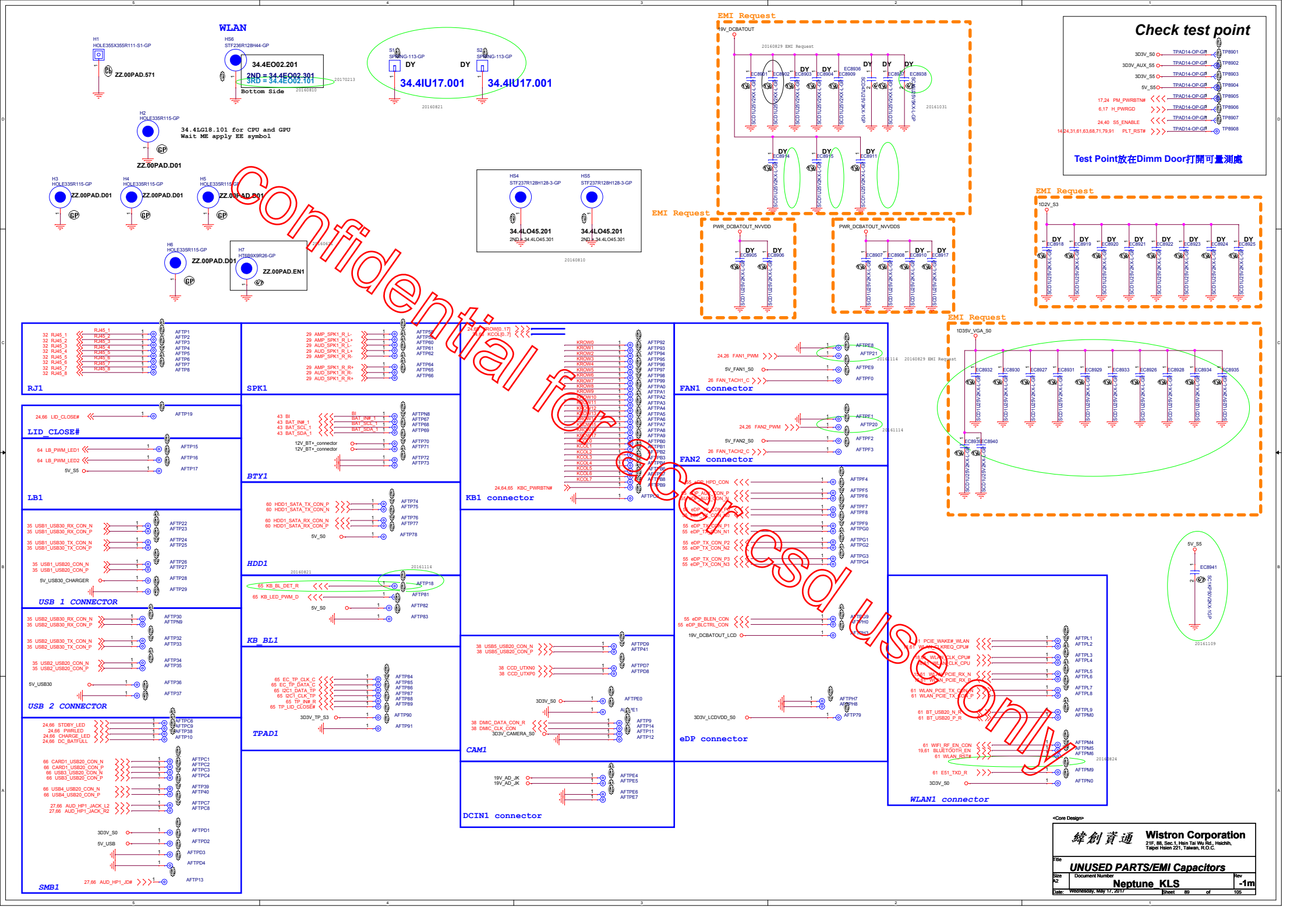

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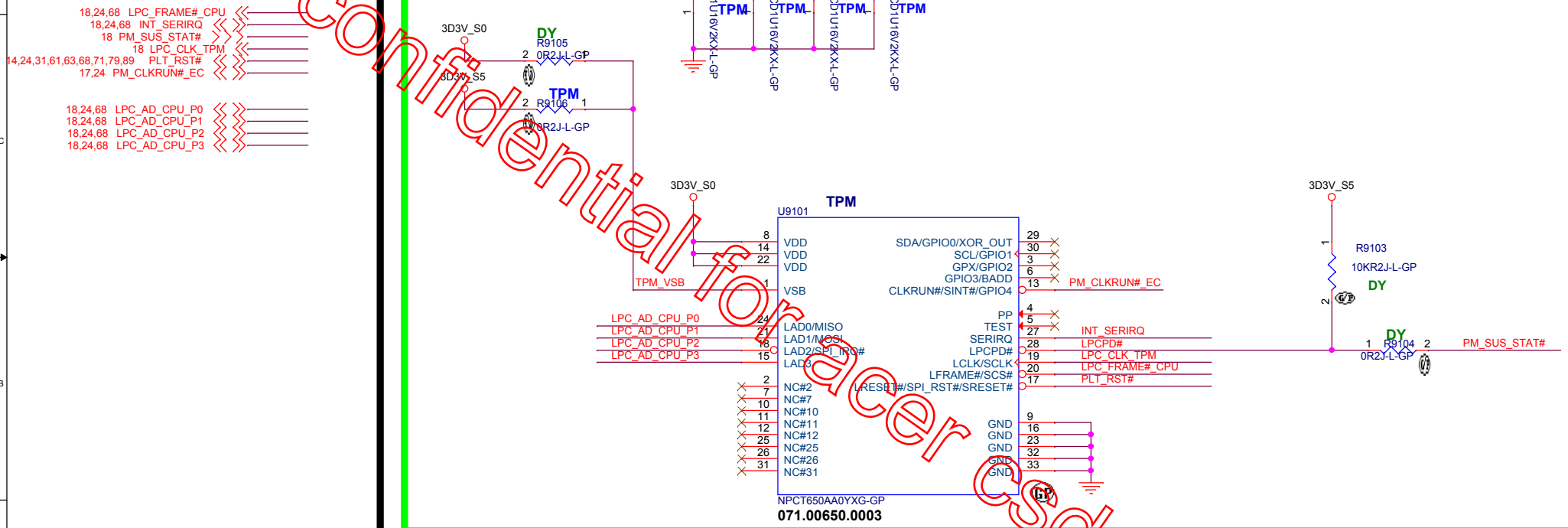
PLUTO



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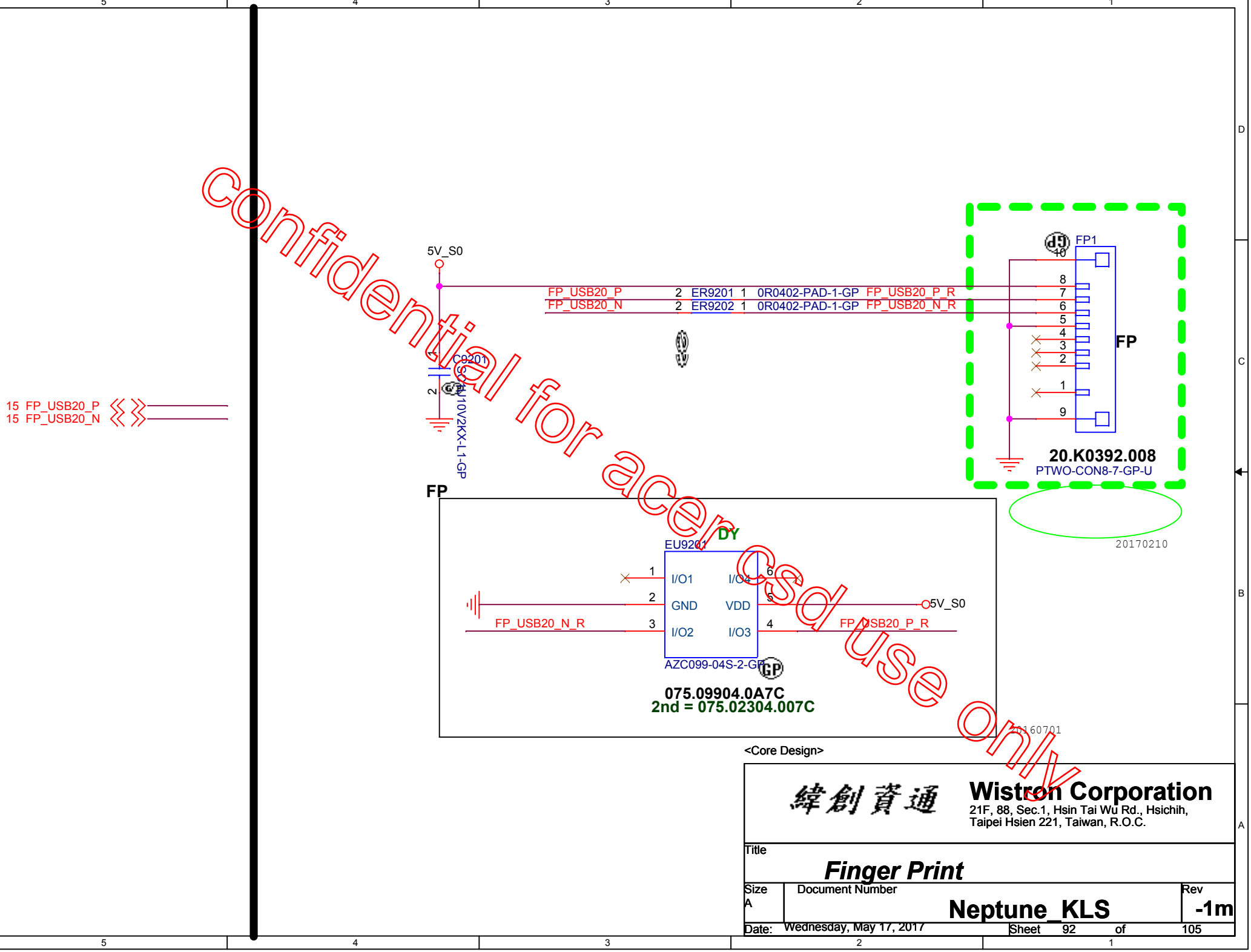

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Title: ***CPU_CFG_CFG STRAP***

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Change History

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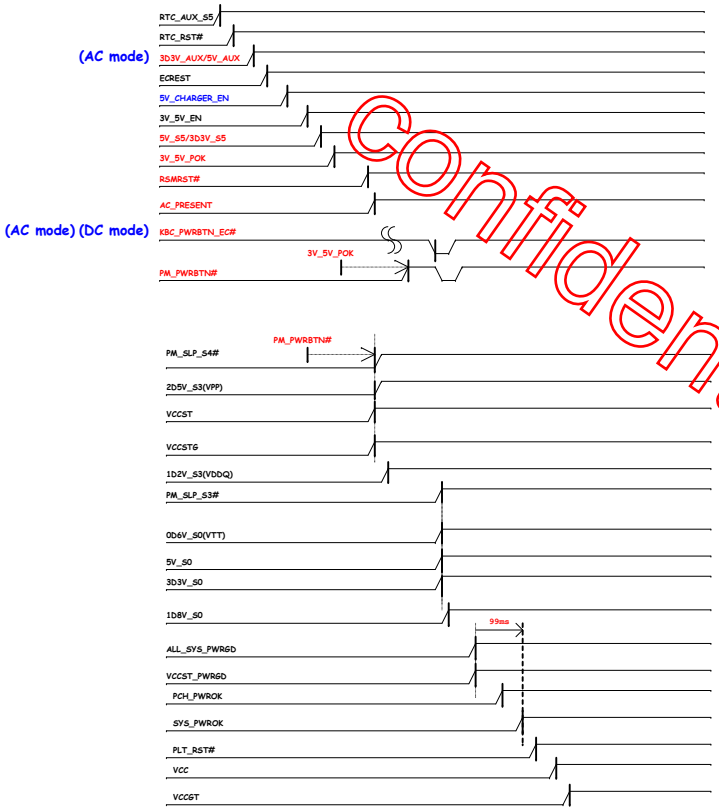
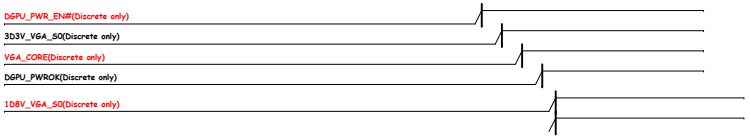
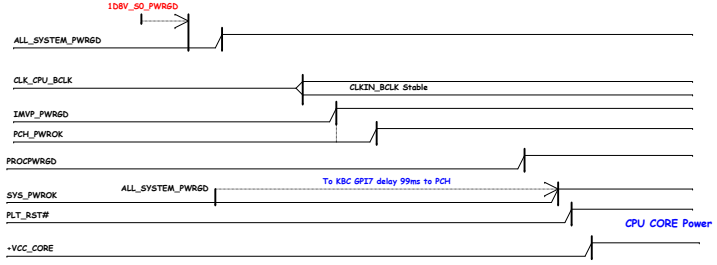
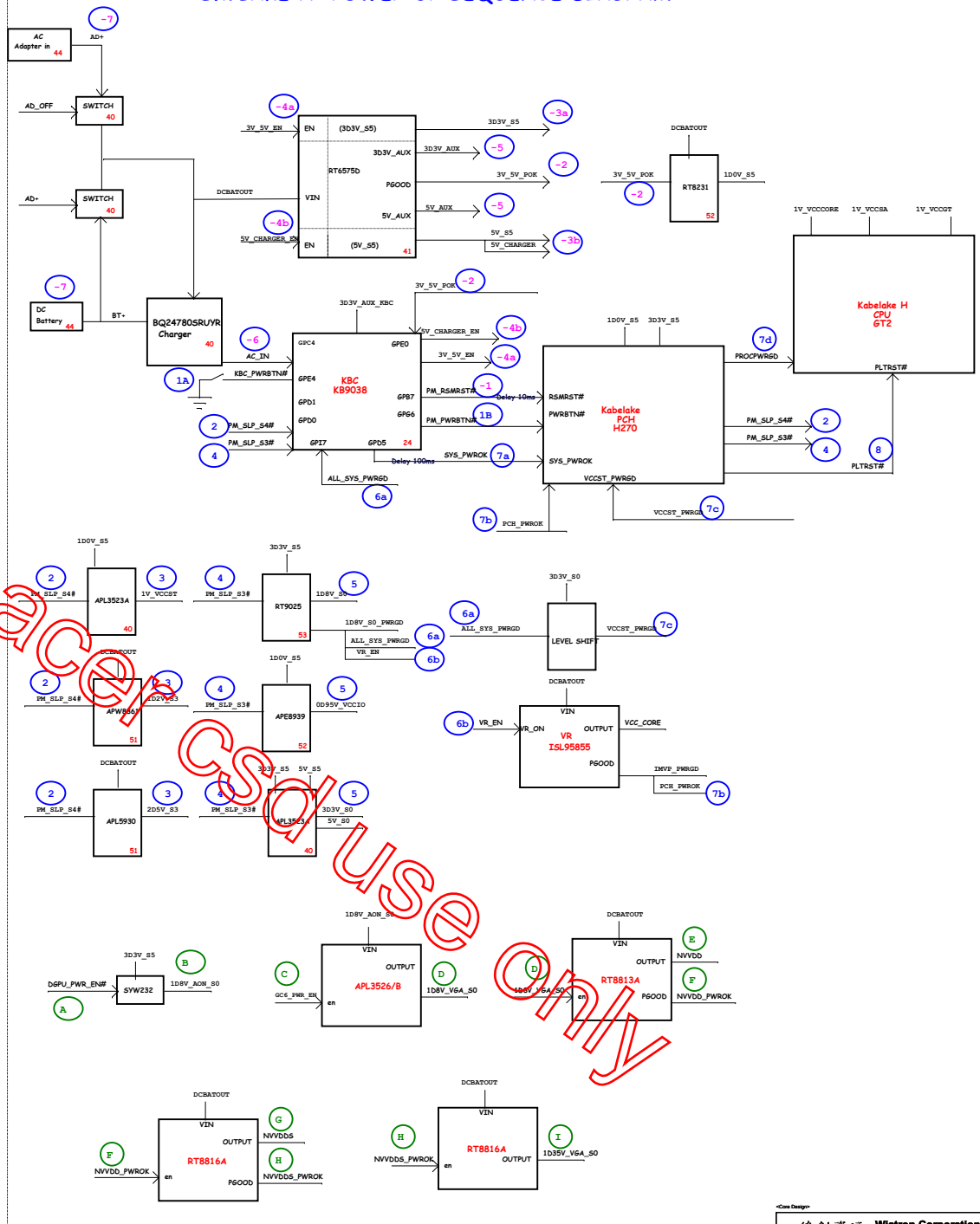
Intel-Power Up Sequence







SKYLAKE H POWER UP SEQUENCE DIAGRAM



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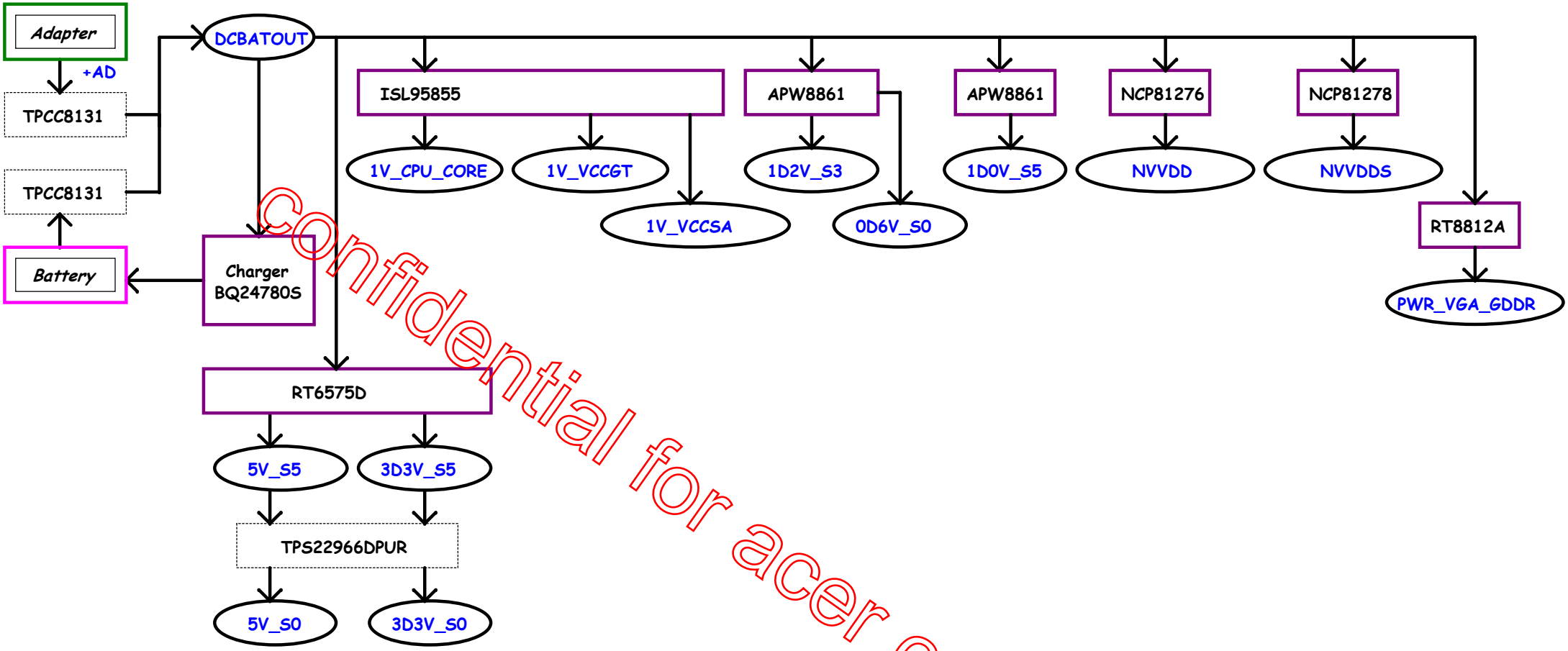

Regulator | LDO | Switch

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Title: **Power Block Diagram**

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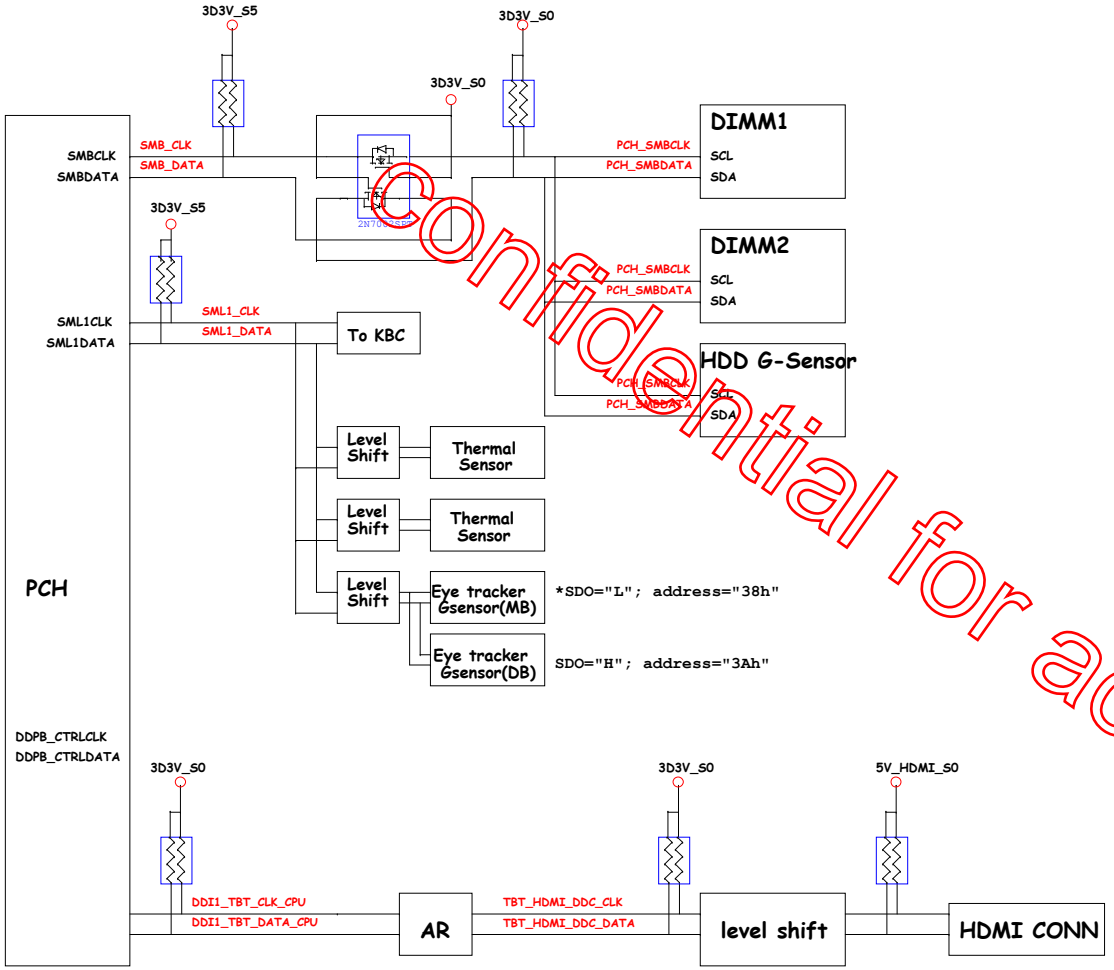
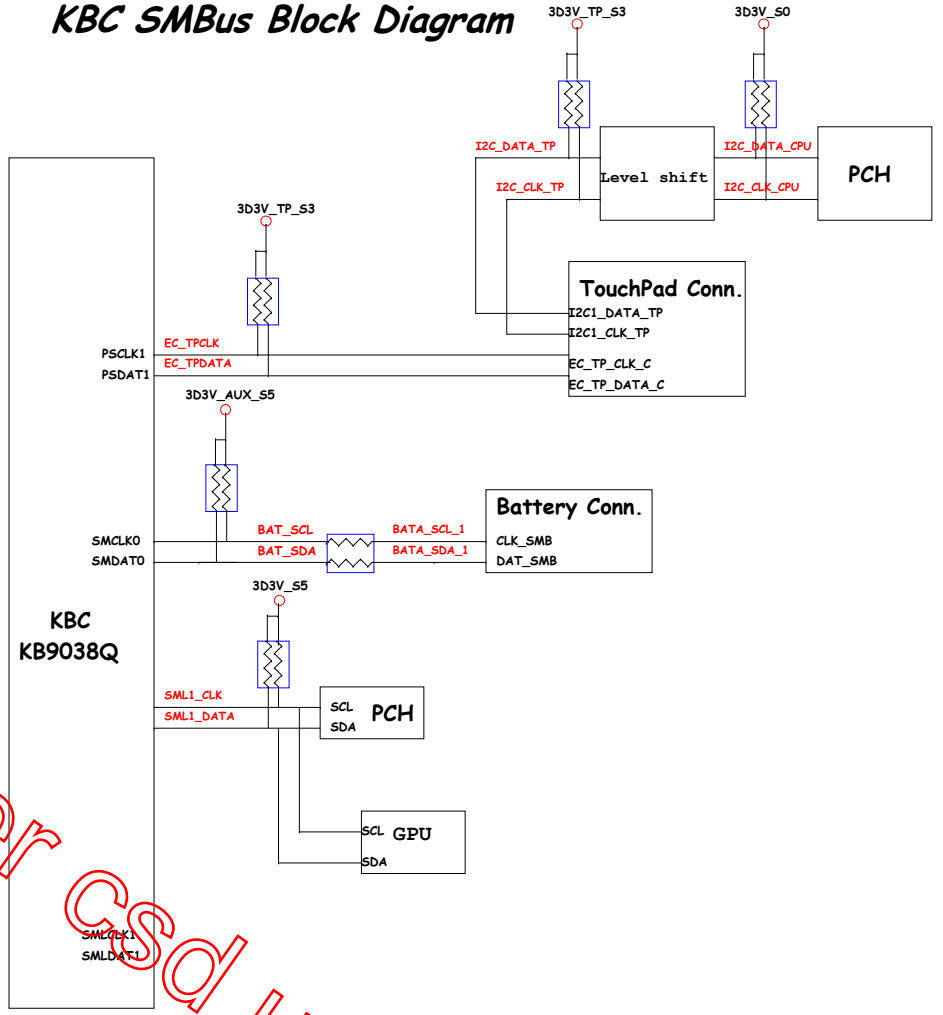
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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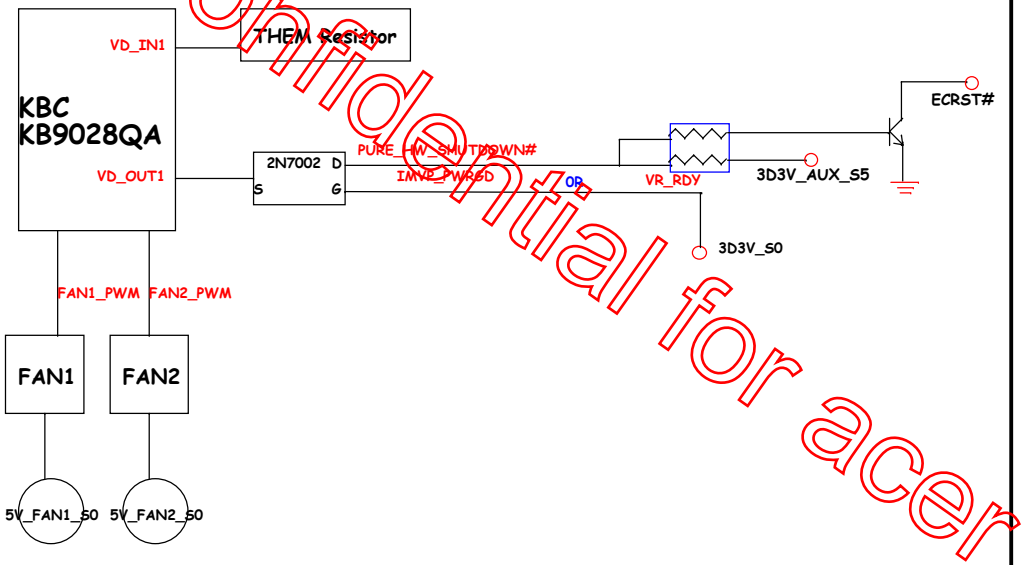
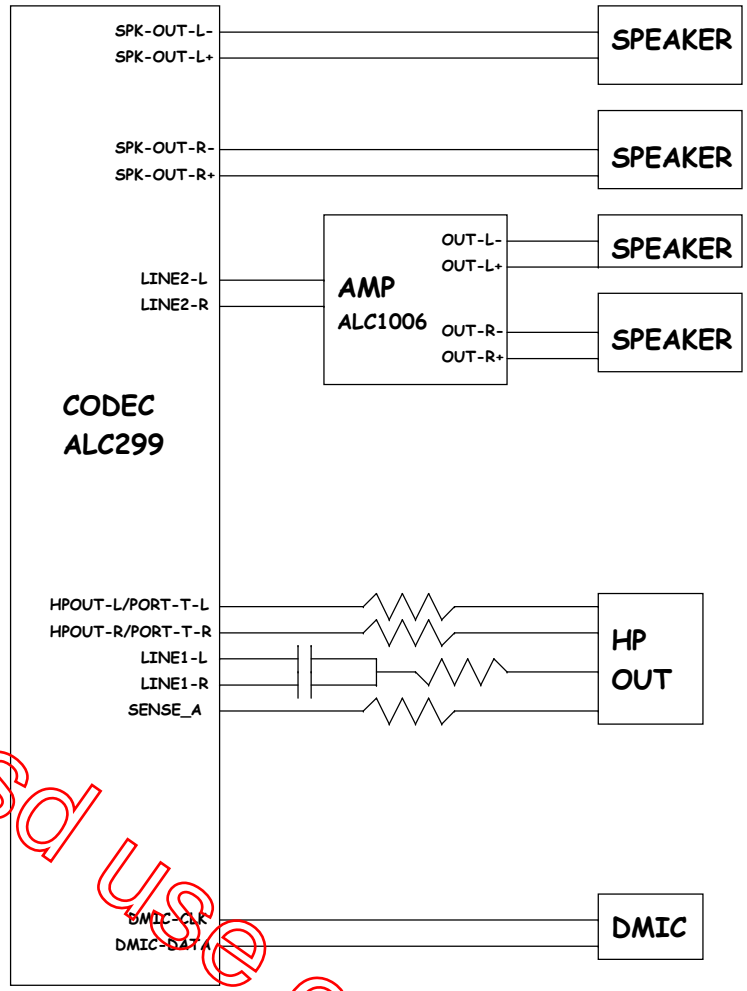
Thermal Block Diagram



Audio Block Diagram



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