MS-7970

ATX

Ver:
1.1

Intel -Skylake plamform
Z170

CPU:

Skylake-S

System Chipset:

Z170 TOMAHAWK
B150 TOMAHAWK
Z170A G43

Onboard Chip:

HD Audio Codec:ALC892

LAN:RTL 8111H

SIO:Nuvoton 6793D

Flash ROM: SPI 64MB /128MB(For H170/B150)

Main Memory:

*DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)*

ACPI:

NIKO/UPI

PWM:

IMVP8 -ISL95858

Expansion Slots:

*PCI Express (X16) Slot *1*
*PCI Express (X4) Slot * 1*
*PCI Express (X1) Slot * 3*
*PCI Slot * 3*
*M2 * 1*

Other:

SATA3.0 x6 (PCH)
*REAR USB2.0 *2*
*FRONT USB2.0 *4*
*FRONTUSB3.0 *4*
*REAR USB3.0 *2*
*REAR USB3.1 *2*

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Size	Document Description	Rev
Custom	Cover Sheet	1.1

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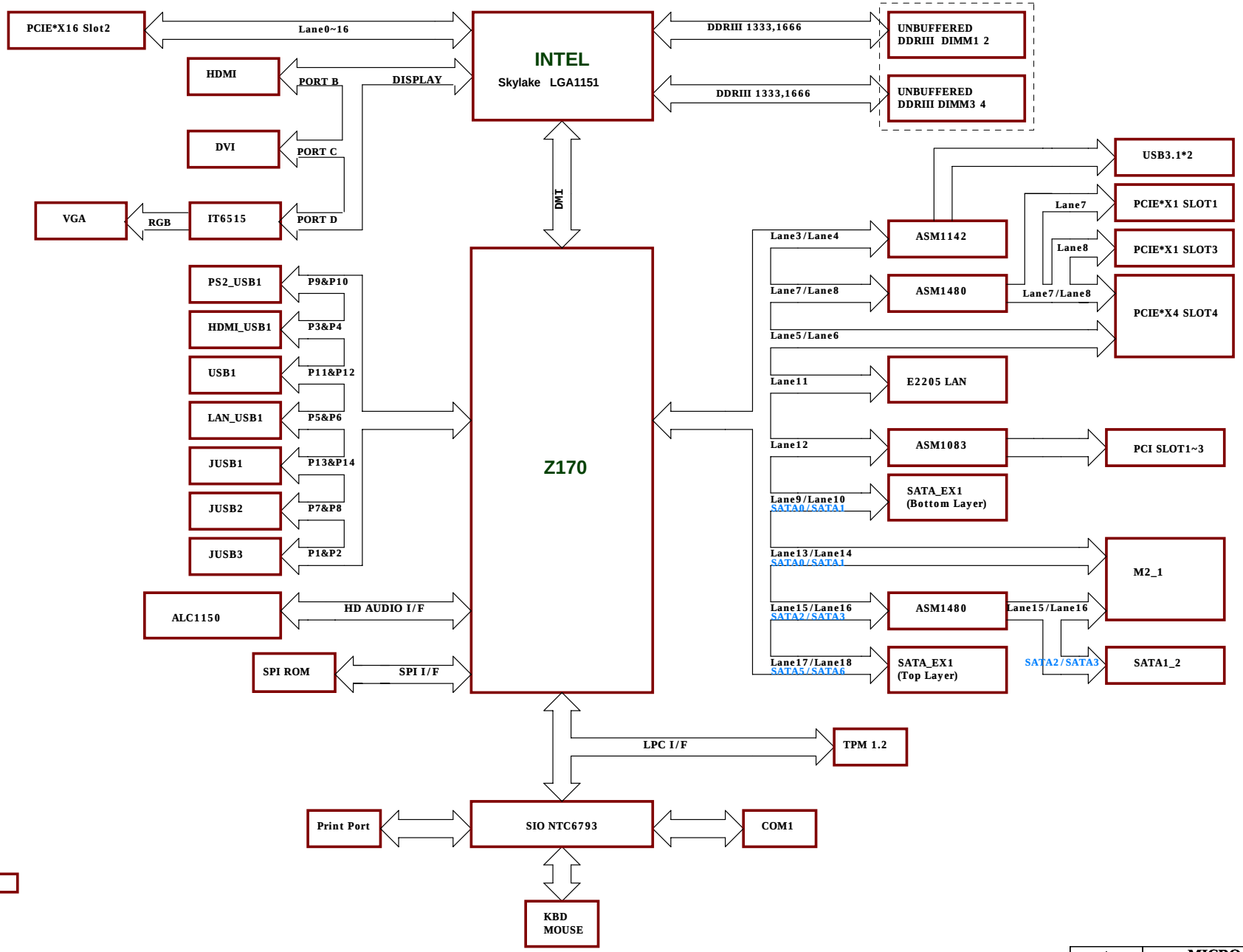
MS-7978 Block Diagram



Slot Sequence:

- PCIE X1
- PCIE X16
- PCIE X1
- PCIE X1
- PCIE X4
- PCI
- PCI

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MS-7970		
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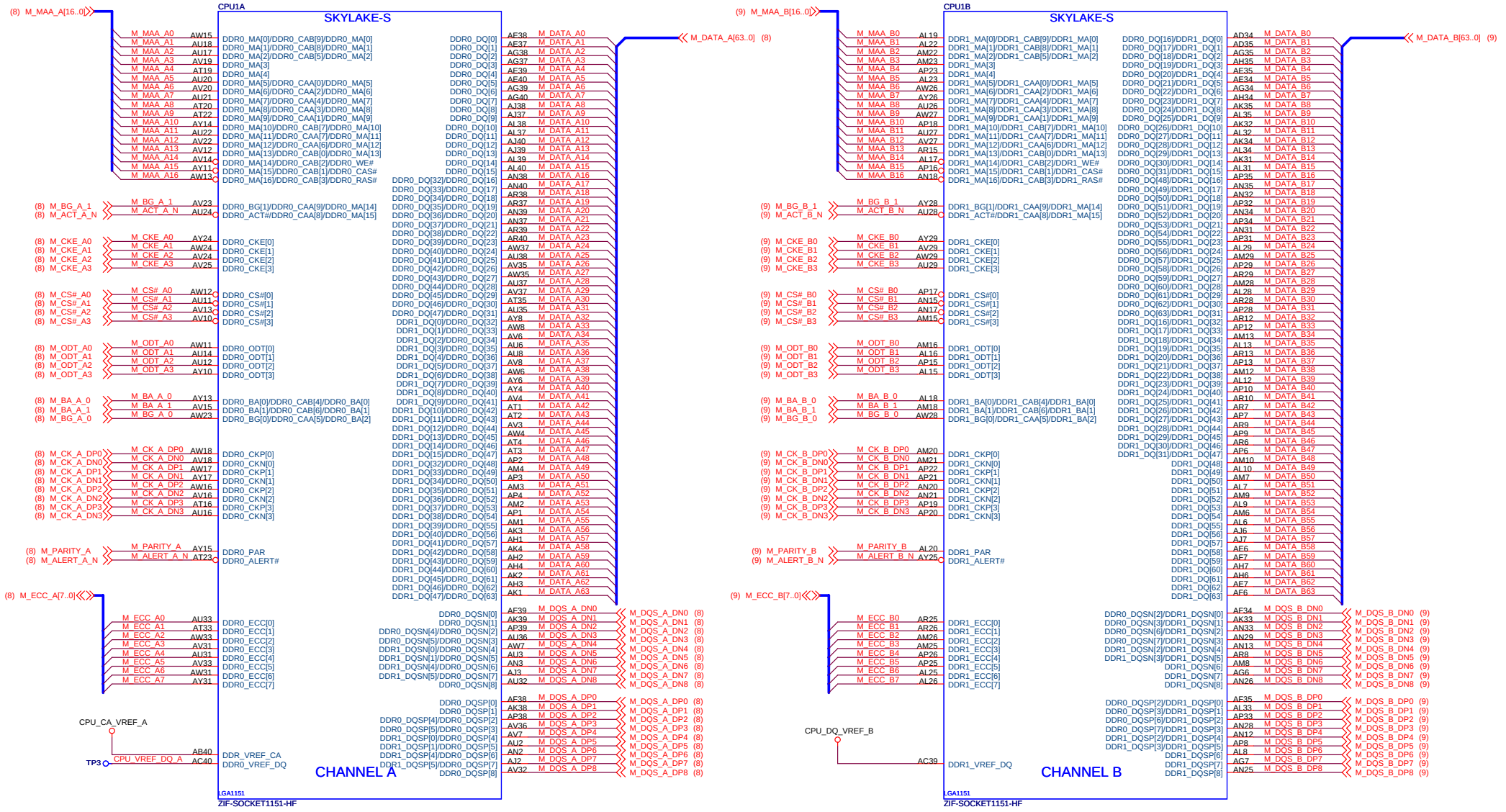
SOCKET PN N12-151A010-L06



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Size: Custom	Document Description: CPU-Memory
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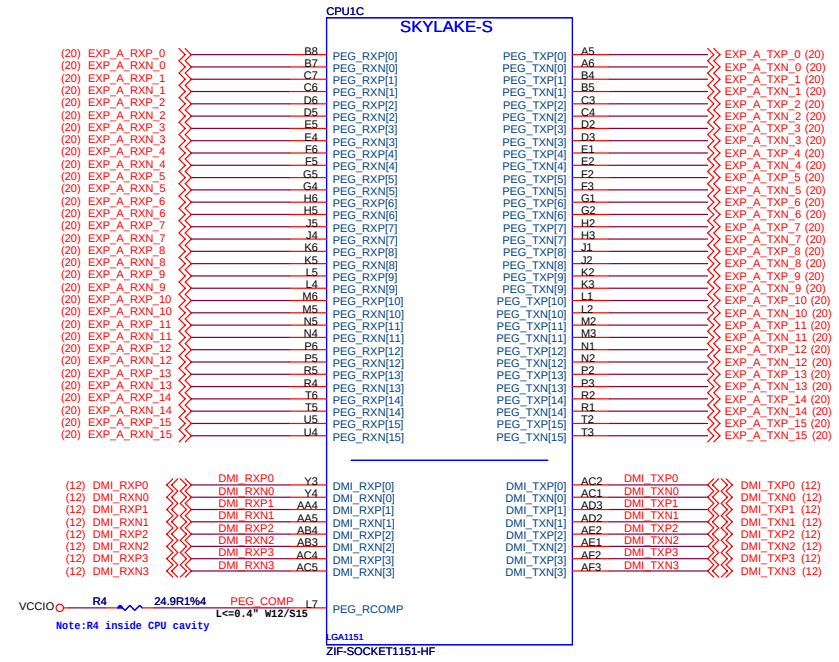

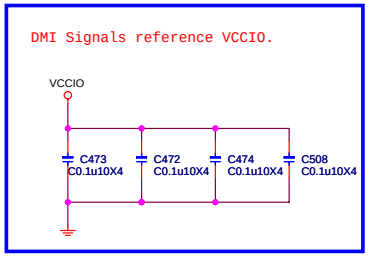

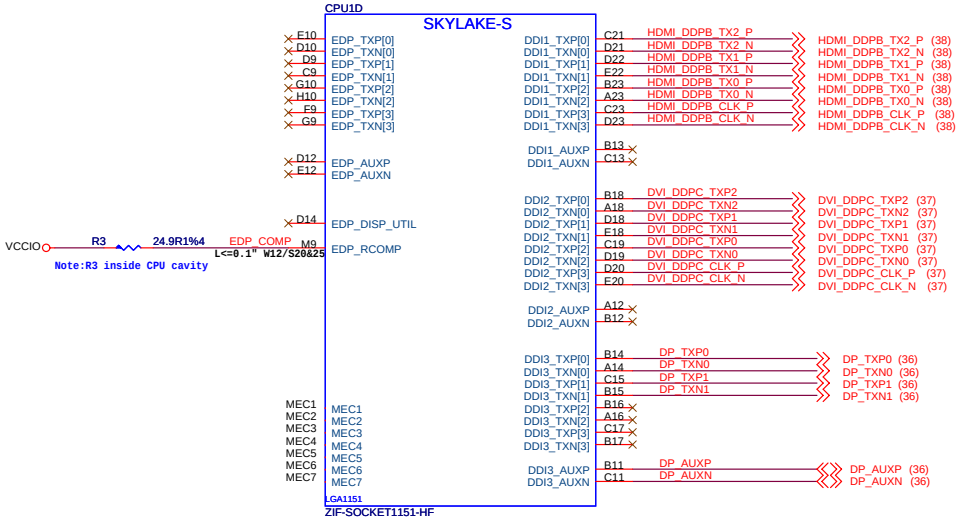

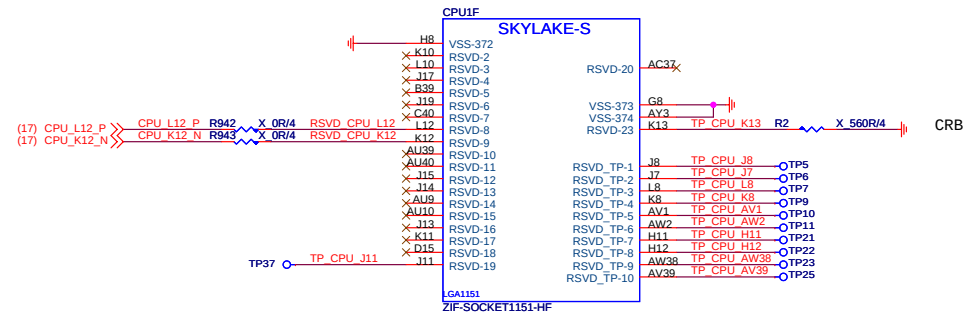

CPU Socket MEC5 Hole top layer add Soldermask,bot layer not add Soldermask.
1.MEC5 connect to GND.
2.Add CPU1L.
3.Footprint change to ZIF_SOCK1151_TEST_7978.

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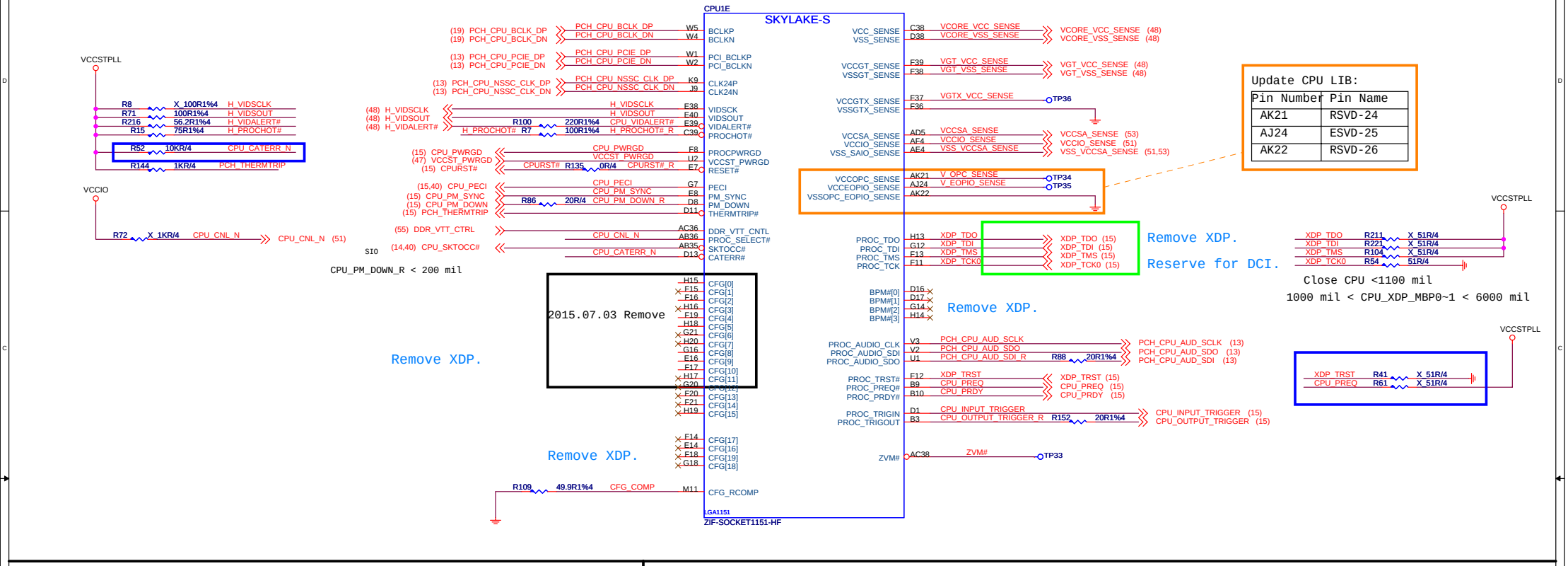


The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.

EN# X8	SLOT2	SLOT5
0	X8	X8
1	X16	X0

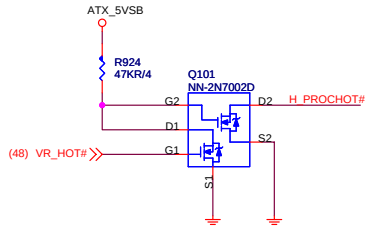
CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

2015.04.23 Remove

NOTE: This CPU LIB only for MS-7978 and MS-7984,other desginer please make sure need it



MICRO-STAR INT'L CO.,LTD

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Size: Custom | Document Description: CPU-Control/MISC/CFG/Audio | Rev: 1.1

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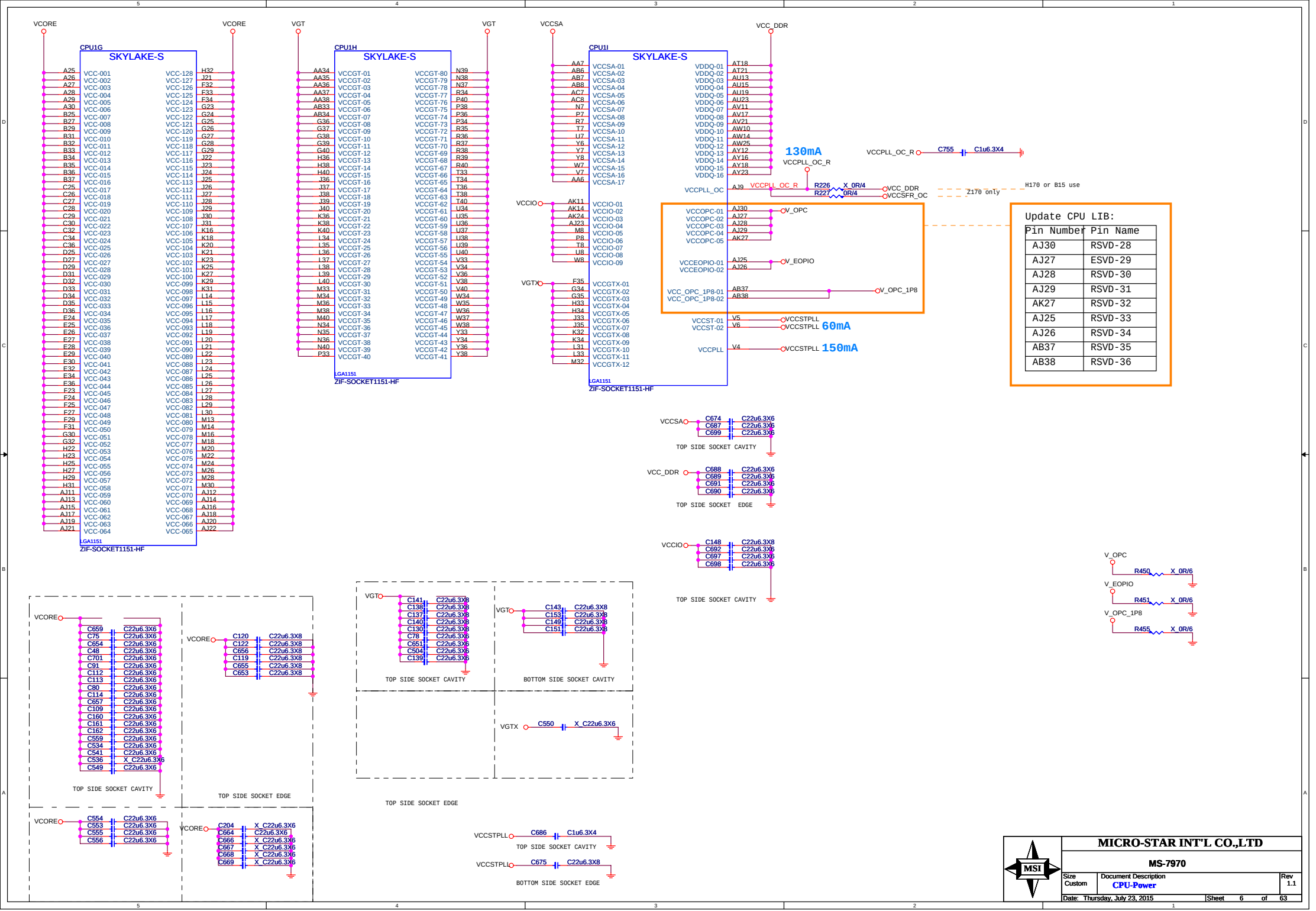

MICRO-STAR INT'L CO.,LTD	
MS-7970	
Size: Custom	Document Description: CPU-Power
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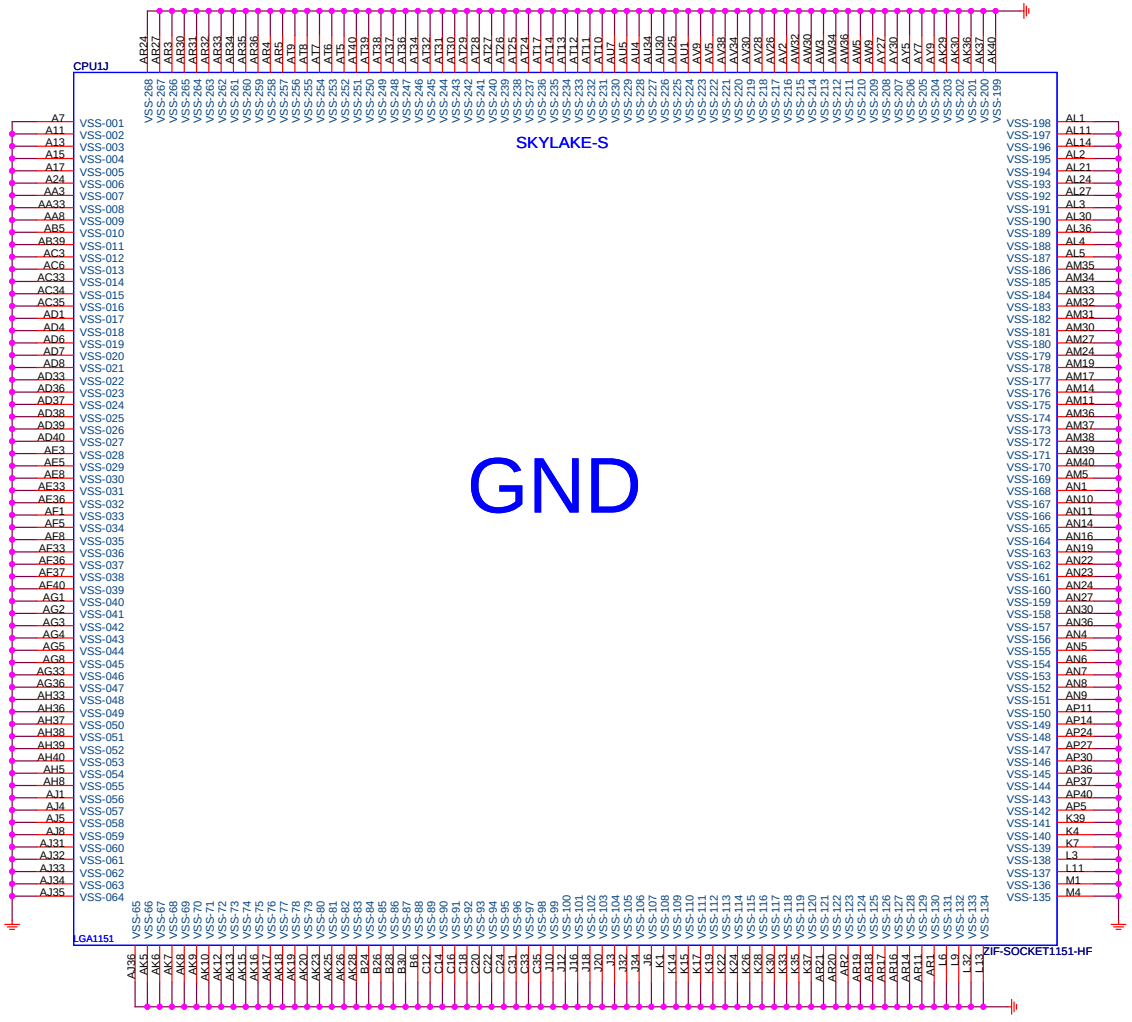

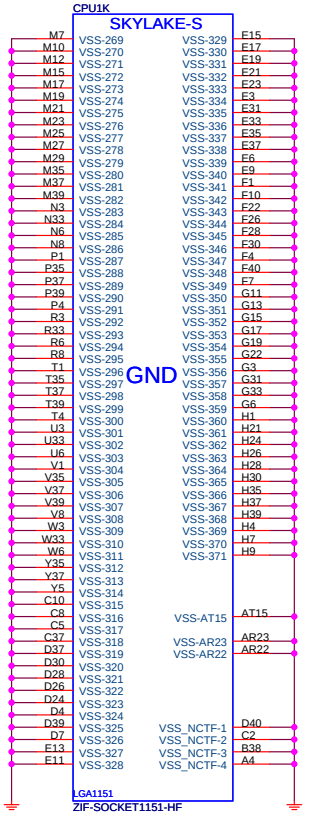

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: CPU-GND	Rev: 1.1
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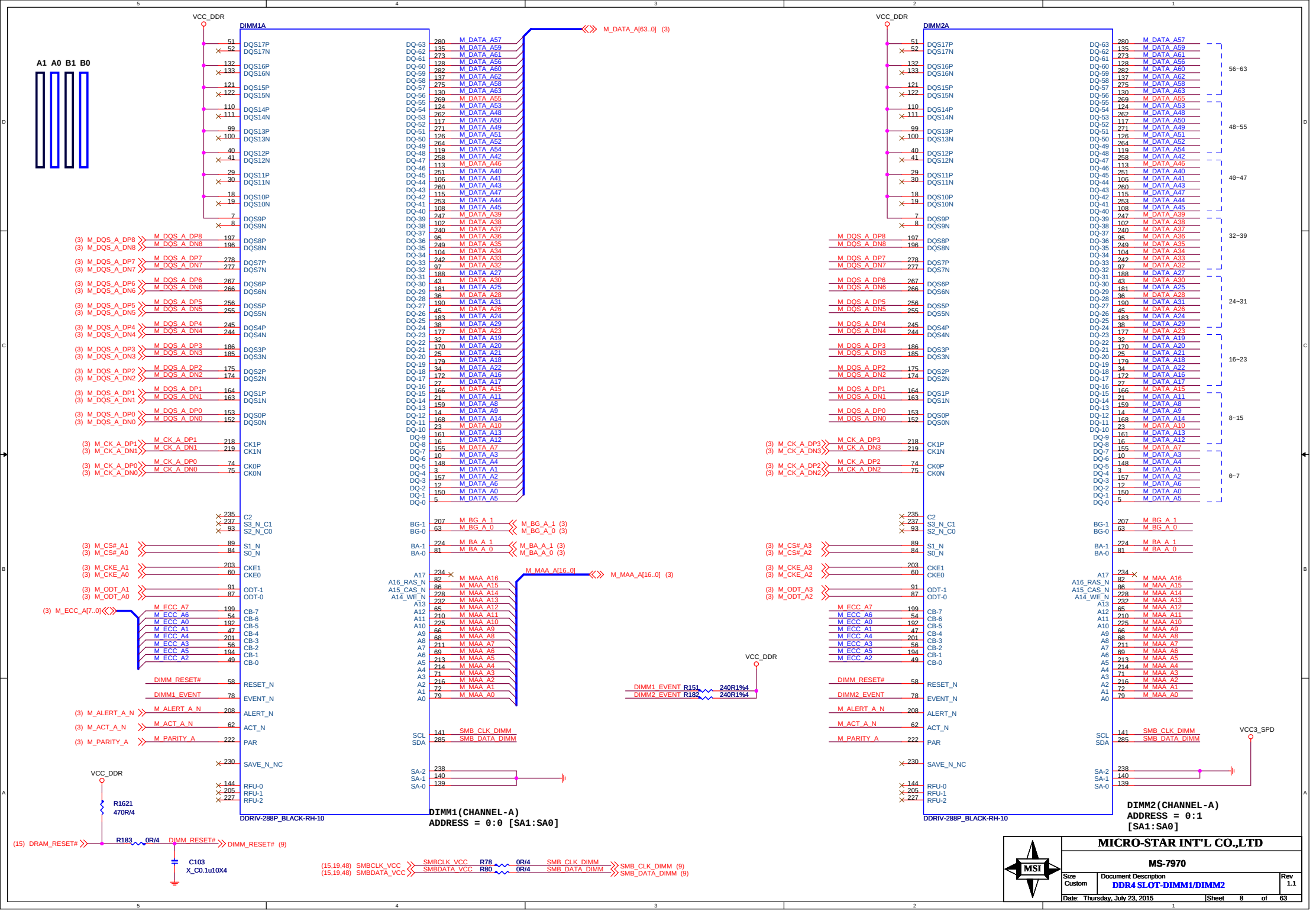
A1 A0 B1 B0
VCC_DDR
DIMM1A
DDRIV-288P_BLACK-RH-10
DIMM1(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]
DIMM2A
DDRIV-288P_BLACK-RH-10
DIMM2(CHANNEL-A)
ADDRESS = 0:1
[SA1:SA0]
M_DATA_A[63..0] (3)
M_MAA_A[16..0] (3)
R1621
470R/4
R183 0R/4 DIMM_RESET#
C103
X_C0.1u10X4
SMBCLK_VCC R78 0R/4 SMB_CLK_DIMM
SMBDATA_VCC R80 0R/4 SMB_DATA_DIMM
DIMM1_EVENT R151 240R1%4
DIMM2_EVENT R182 240R1%4
VCC3_SPD
56~63
48~55
40~47
32~39
24~31
16~23
8~15
0~7
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Size Custom
Document Description
DDR4 SLOT-DIMM1/DIMM2
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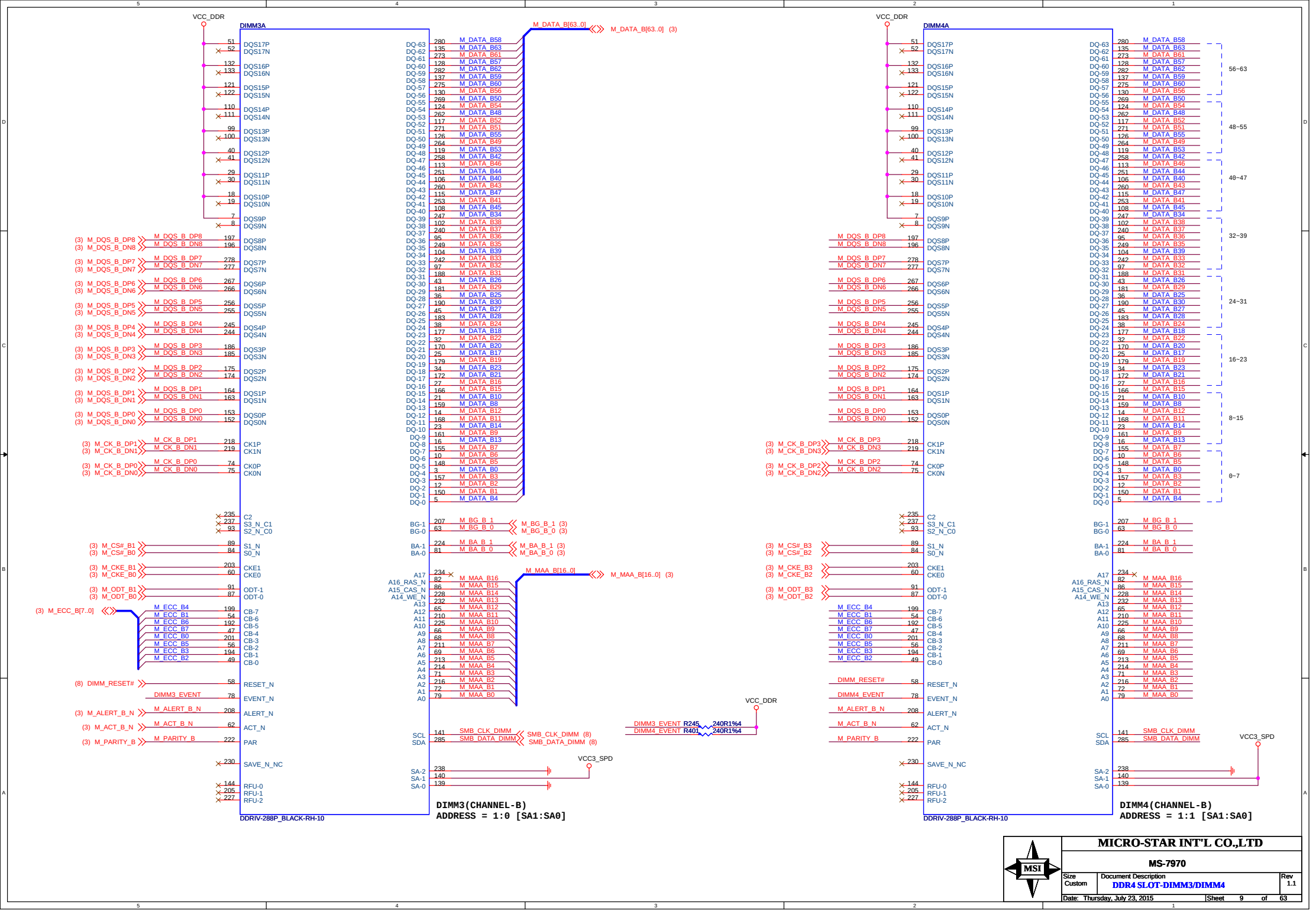

MICRO-STAR INT'L CO.,LTD	
MS-7970	
Size: Custom	Document Description: DDR4 SLOT-DIMM3/DIMM4
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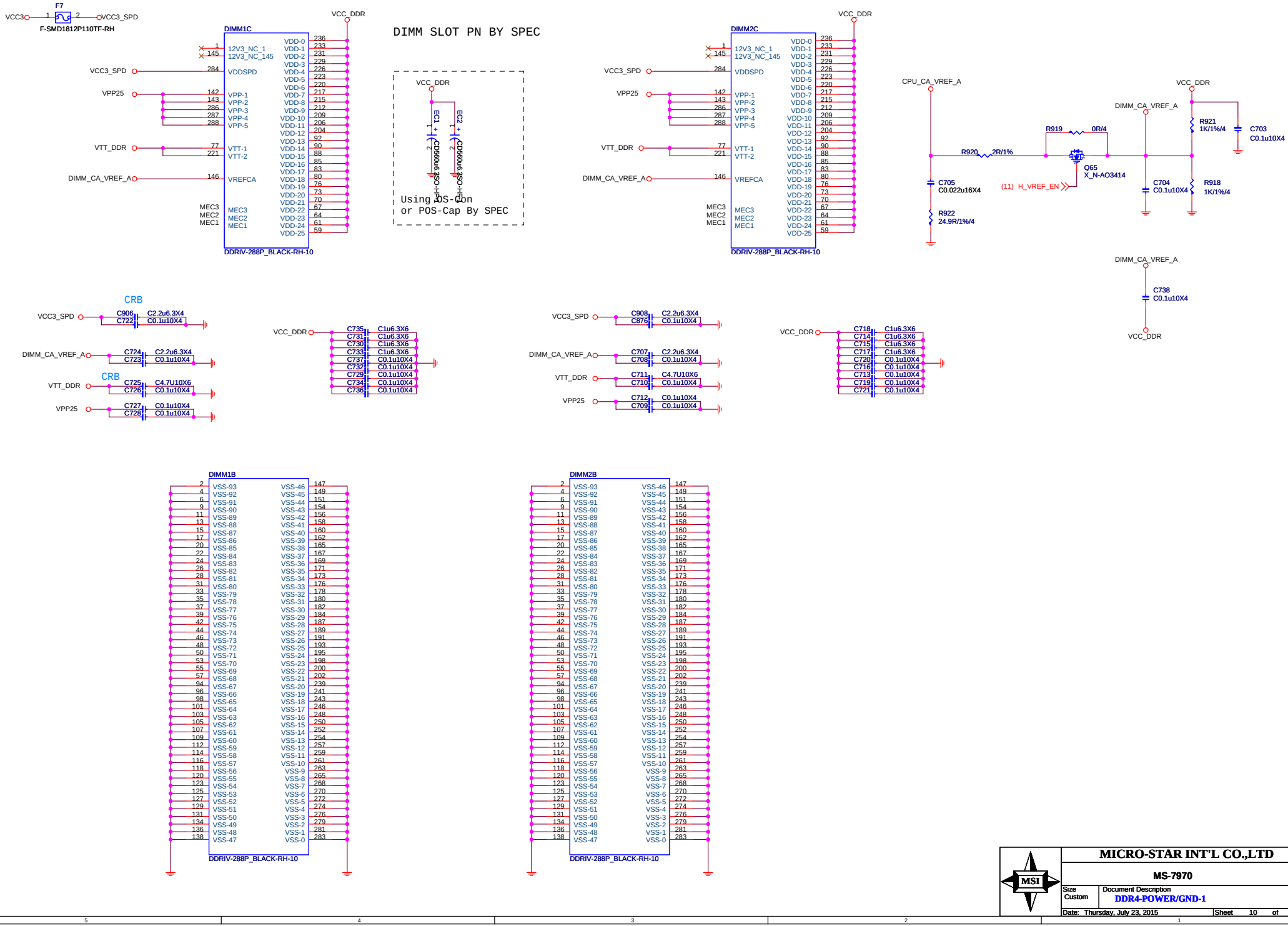

MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: DDR4-POWER/GND-1
Rev: 1.1	
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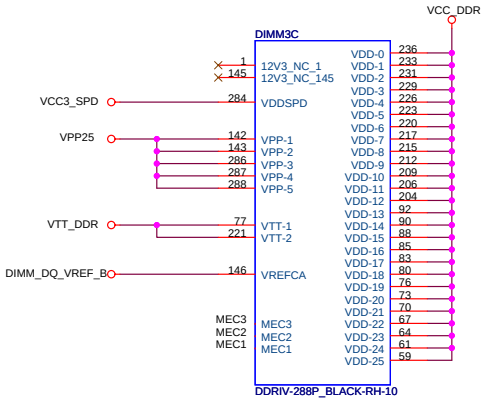

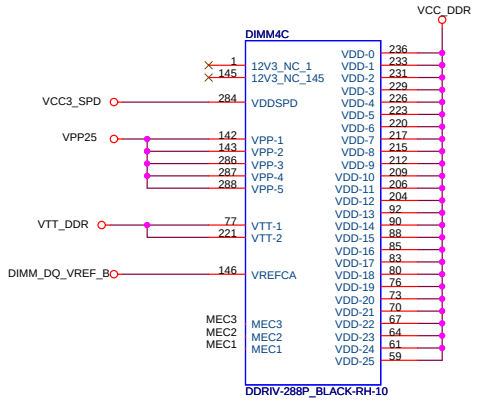

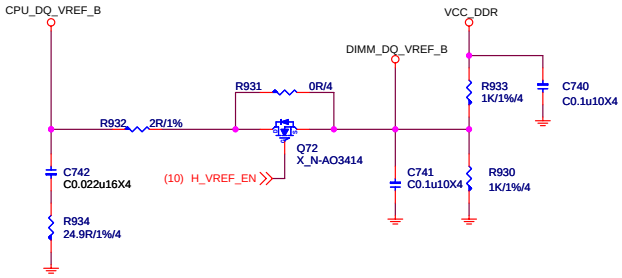

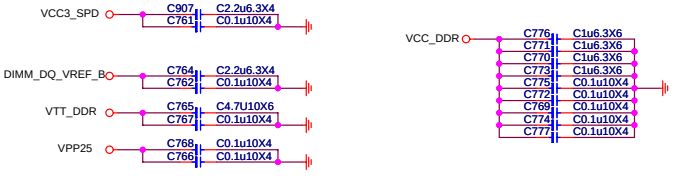

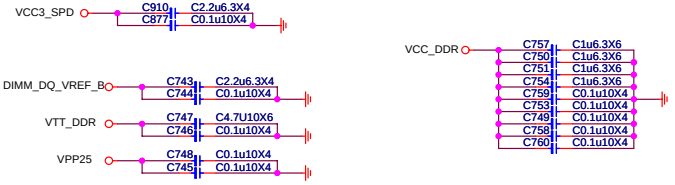

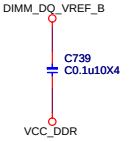

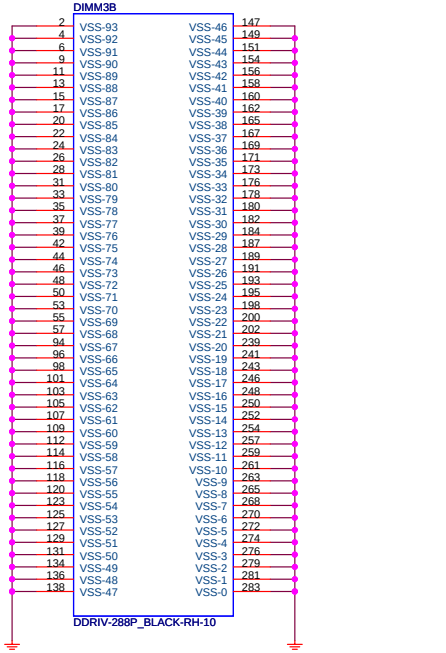

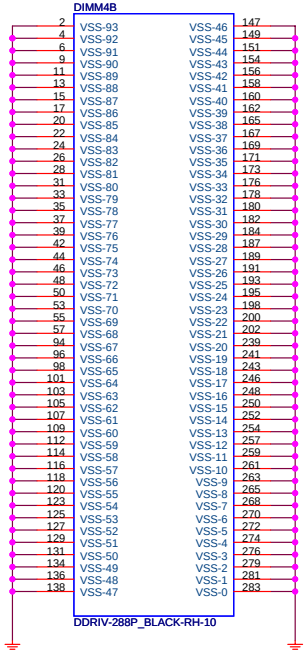

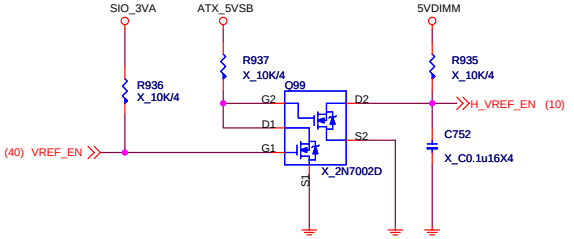

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Size	Document Description	Rev
Custom	DDR4-POWER/GND-2	1.1

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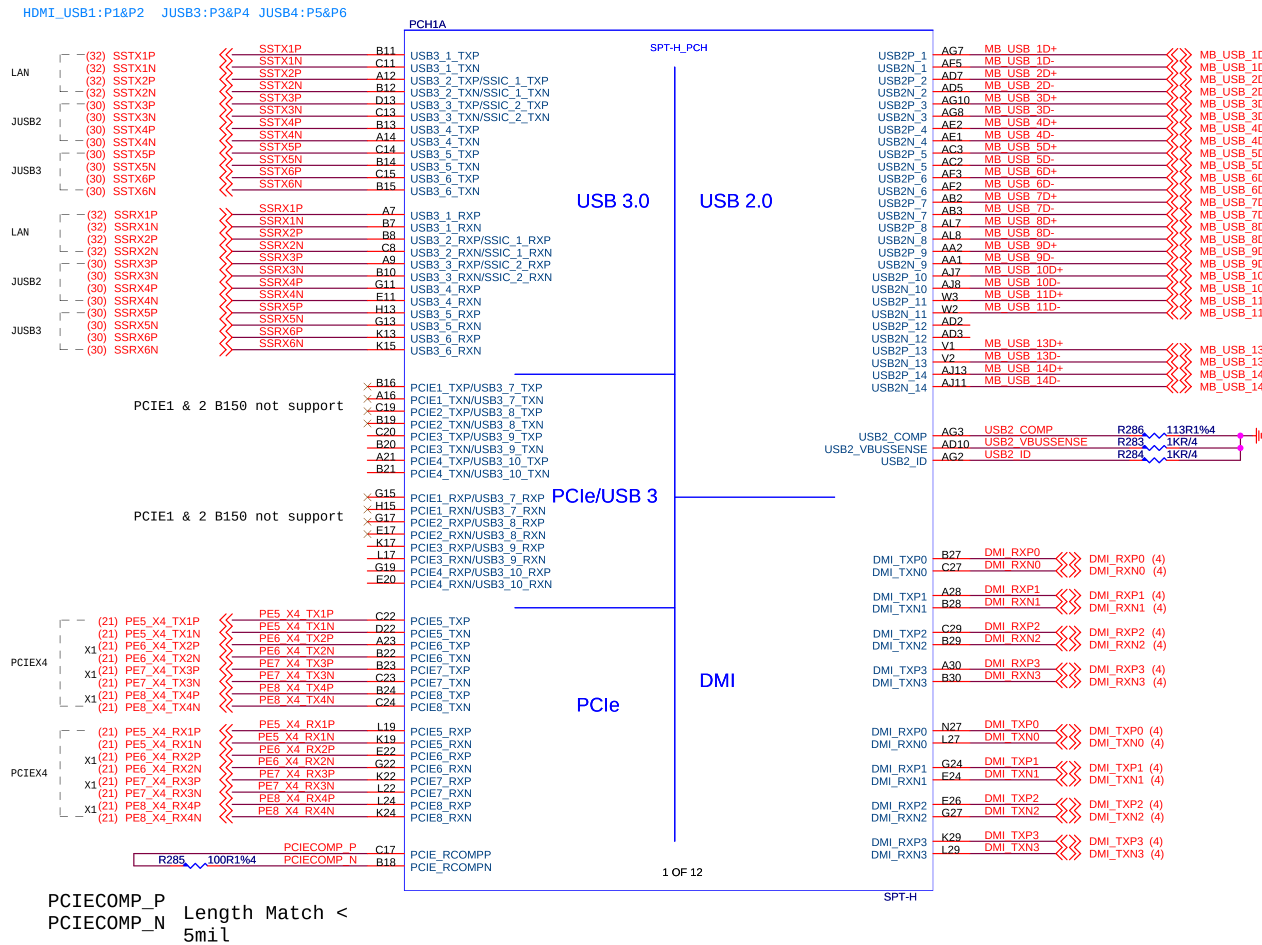
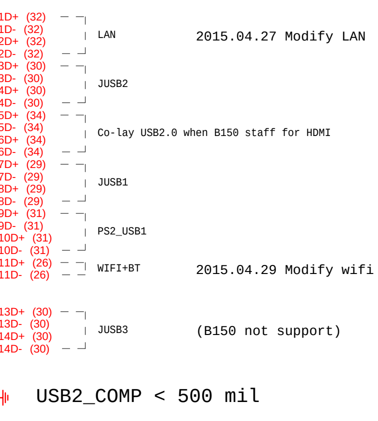
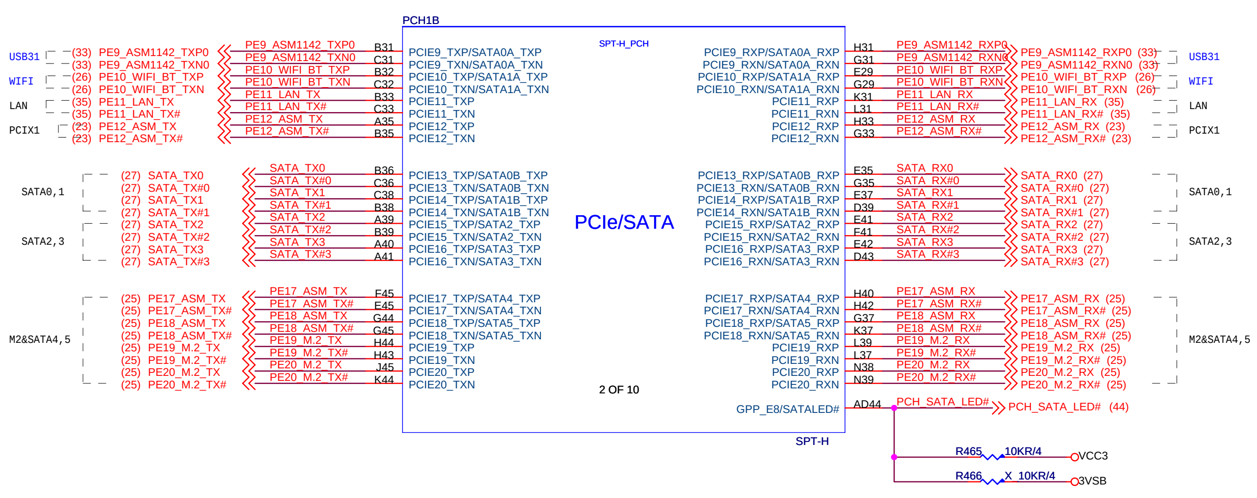




Sku	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	[illegible]	[illegible]	[illegible]	USB3	N/A	N/A	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
B150	[illegible]	[illegible]	[illegible]	USB3	USB3	USB3	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
H170	[illegible]	[illegible]	[illegible]	USB3	USB3	USB3	USB3	USB3	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
Z170	[illegible]	[illegible]	[illegible]	USB3	USB3	USB3	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe

Sku	15	16	17	18	19	20	21	22	23	24	25	26	RST for PCIe Ports
H110	PCIe/ LAN	PCIe	N/A	LAN Only	SATA*/ LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A	0
B150	PCIe/LAN SATA*	PCIe/ SATA*	PCIe	PCIe/ LAN	SATA* /LAN	SATA*	SATA	SATA	SATA	SATA	N/A	N/A	0
H170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	SATA	SATA	PCIe	PCIe	2
Z170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	3



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	PCH-USB/PCIE/DMI/SATA	1.1

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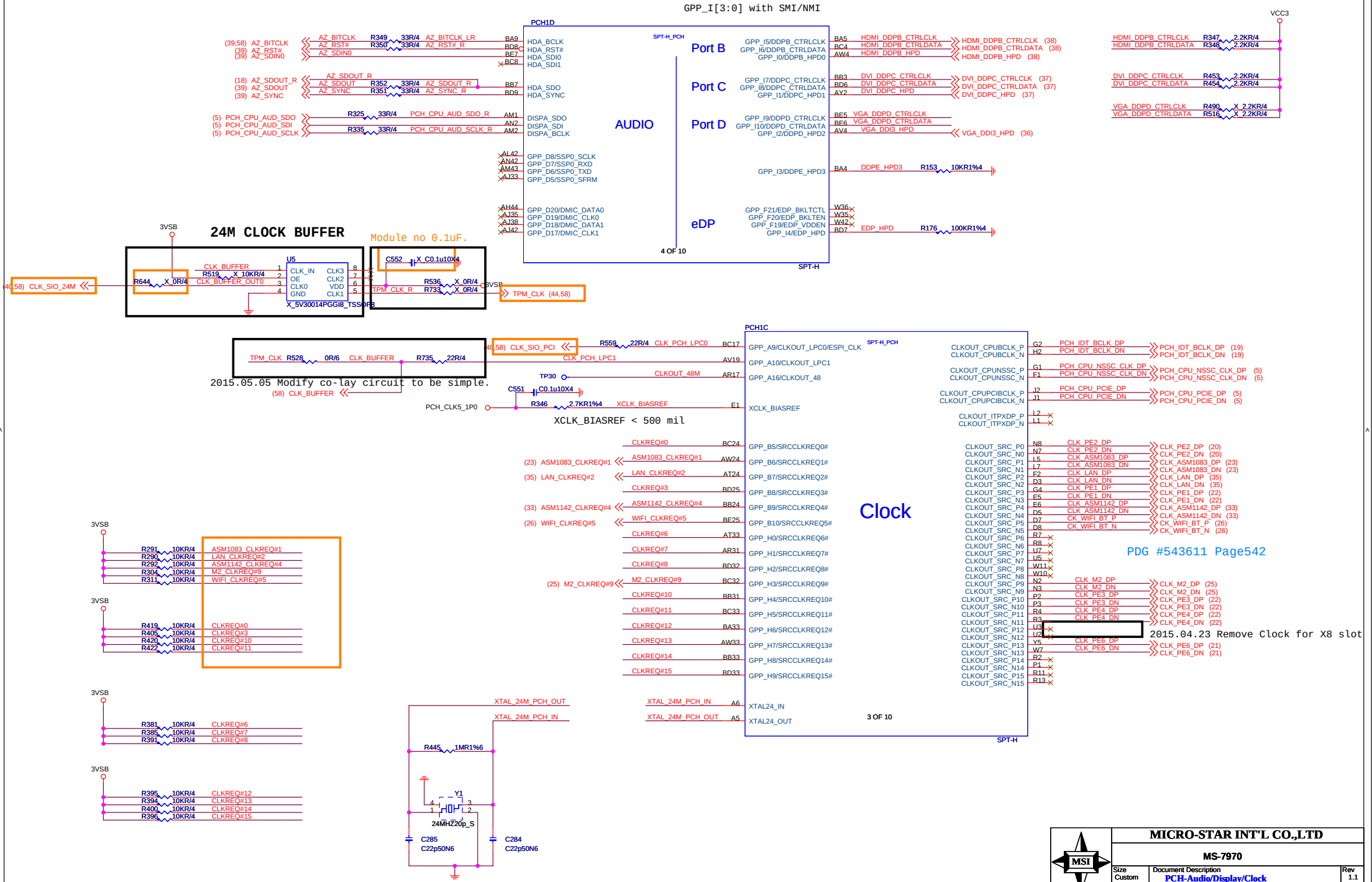
GPP_I[3:0] with SMI/NMI
PCH1D
SPT-H_PCH
AUDIO
Port B
Port C
Port D
eDP
4 OF 10
SPT-H
HDA_BCLK
HDA_RST#
HDA_SDI0
HDA_SDI1
HDA_SDO
HDA_SYNC
DISPA_SDO
DISPA_SDI
DISPA_BCLK
GPP_D8/SSP0_SCLK
GPP_D7/SSP0_RXD
GPP_D6/SSP0_TXD
GPP_D5/SSP0_SFRM
GPP_D20/DMIC_DATA0
GPP_D19/DMIC_CLK0
GPP_D18/DMIC_DATA1
GPP_D17/DMIC_CLK1
GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I0/DDPB_HPD0
GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
GPP_I1/DDPC_HPD1
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
GPP_I2/DDPD_HPD2
GPP_I3/DDPE_HPD3
GPP_F21/EDP_BKLTCTL
GPP_F20/EDP_BKLTEN
GPP_F19/EDP_VDDEN
GPP_I4/EDP_HPD
VCC3
24M CLOCK BUFFER
Module no 0.1uF.
X_5V30014PGGI8_TSSOP8
TPM_CLK (44,58)
2015.05.05 Modify co-lay circuit to be simple.
XCLK_BIASREF < 500 mil
PCH1C
SPT-H_PCH
Clock
3 OF 10
SPT-H
PDG #543611 Page542
2015.04.23 Remove Clock for X8 slot
XTAL24_IN
XTAL24_OUT
24MHZ20p_S
MICRO-STAR INT'L CO.,LTD
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PCH-Audio/Display/Clock
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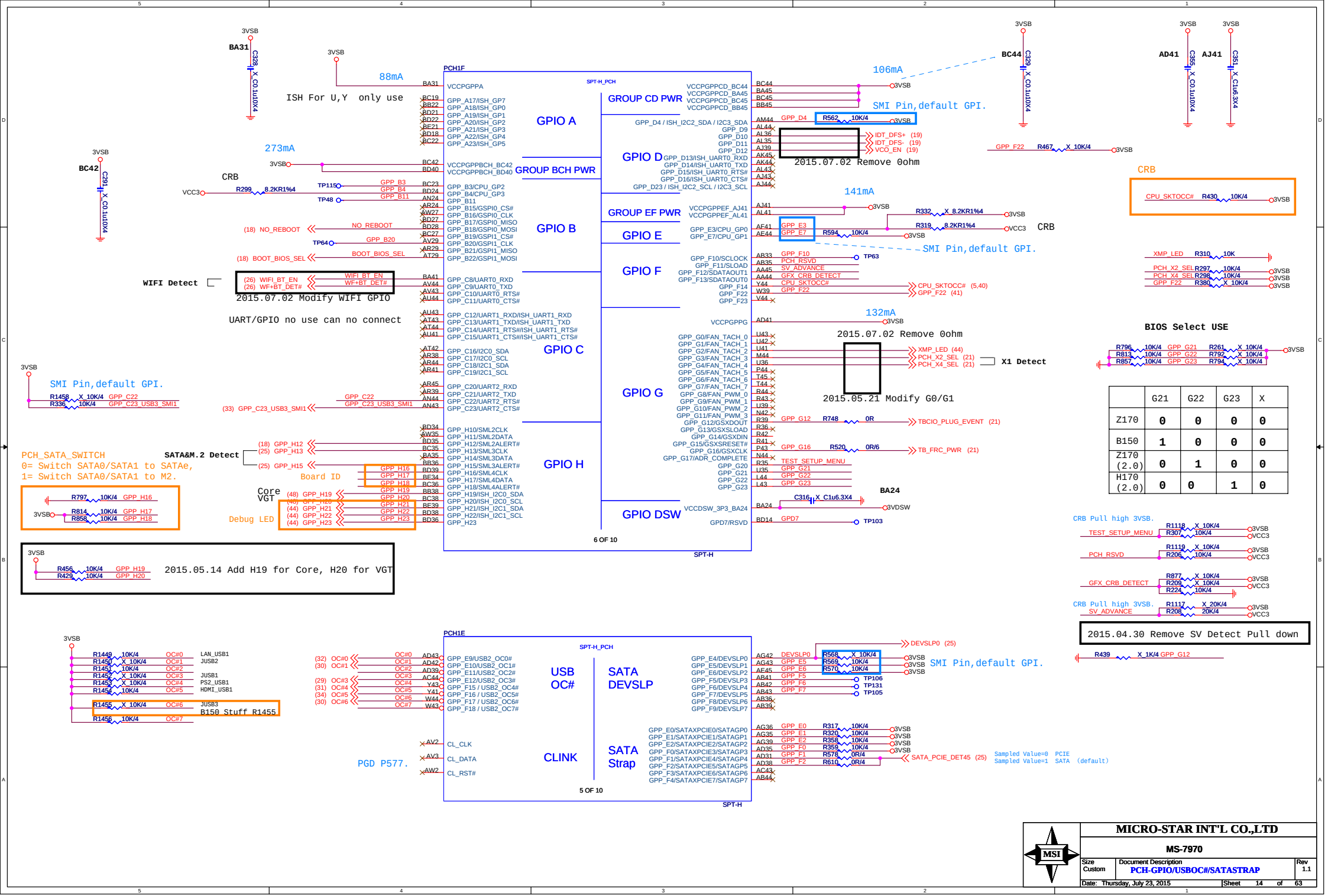

	G21	G22	G23	X
Z170	0	0	0	0
B150	1	0	0	0
Z170 (2.0)	0	1	0	0
H170 (2.0)	0	0	1	0

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Size: Custom | Document Description: PCH-GPIO/USBOC#/SATASTRAP | Rev: 1.1

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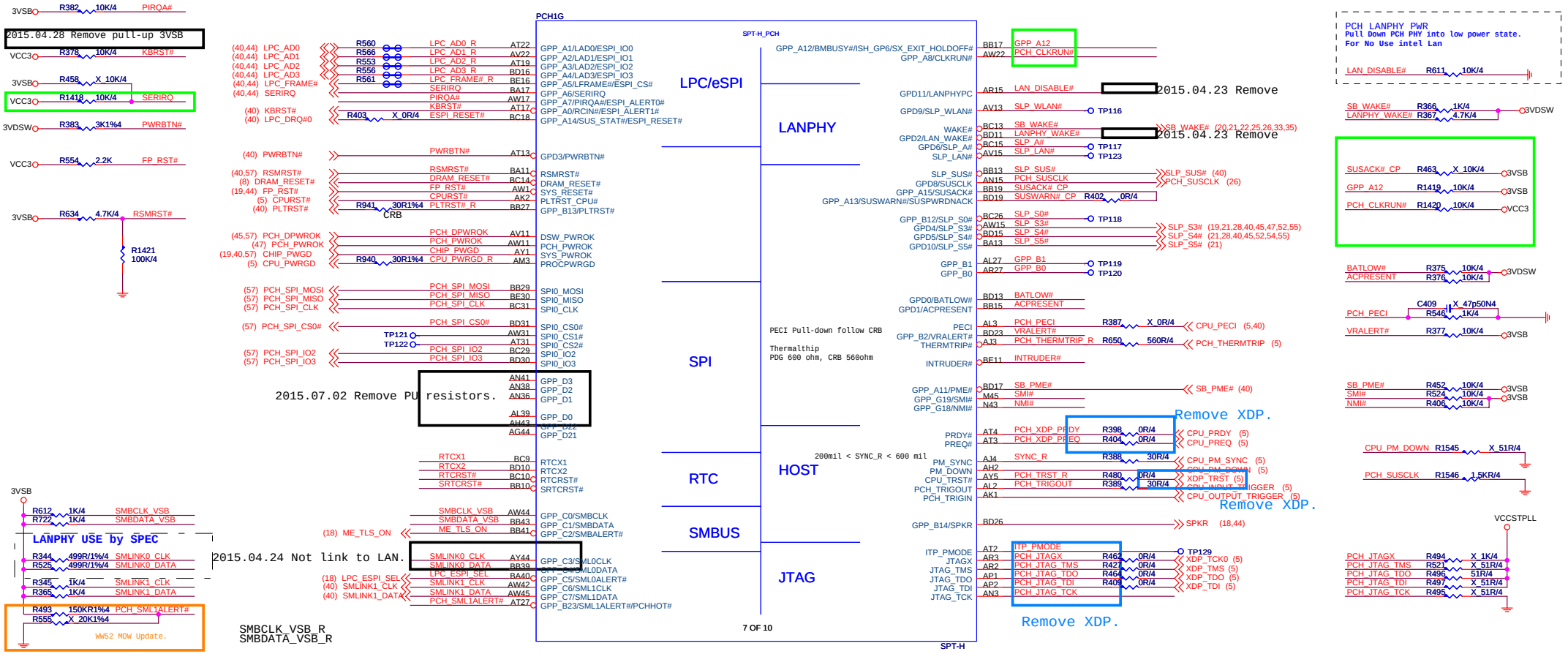
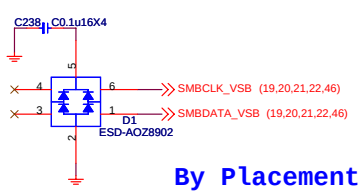


SMBUS ESD

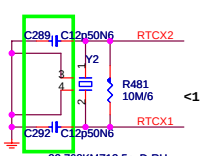


By Placement

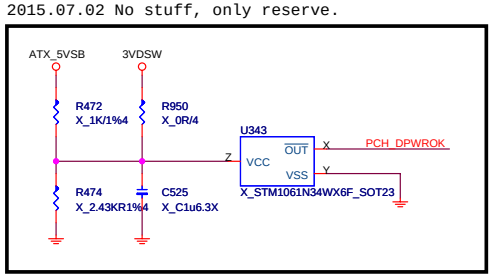
RTC Block

Footprint:OSCC_MS_TEST

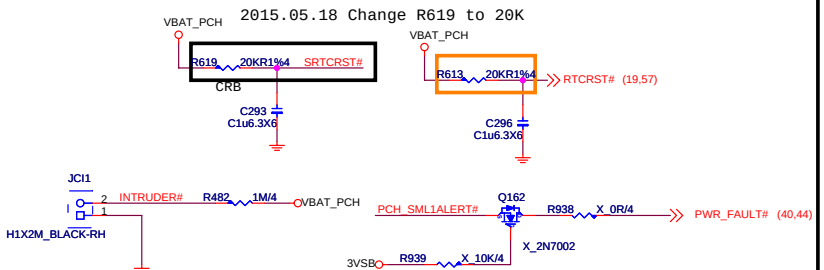
Close to PCH



2015.07.02 No stuff, only reserve.



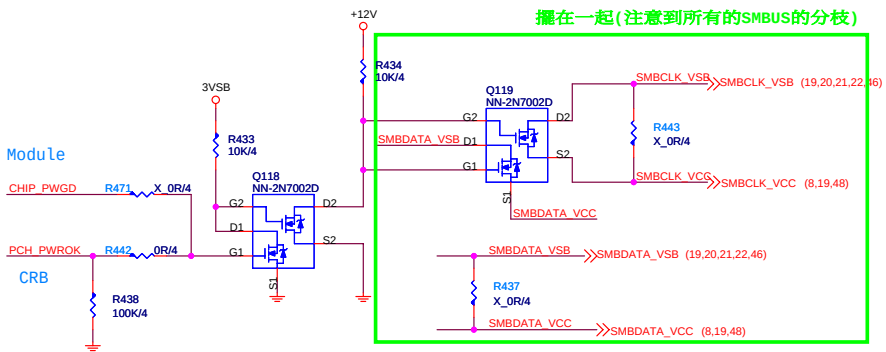
2015.05.18 Change R619 to 20K



SMBUS隔離線路(PCH接出來是PULL HIGH 3VSB)
需要再S3/S5底下動作的接SMBCLK_VSB/SMBDATA_VSB
不需要的接SMBCLK_VCC/SMBDATA_VCC

基本上PCIE的SLOT要接3VSB的CPU的PWM IC/DDR要接VCC3的其他的請注意要怎麼接

2015.07.02 Use dual-MOS



擺在一起(注意到所有的SMBUS的分枝)

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: PCH-LPC/SPI/SMBUS/MISC	Rev: 1.1
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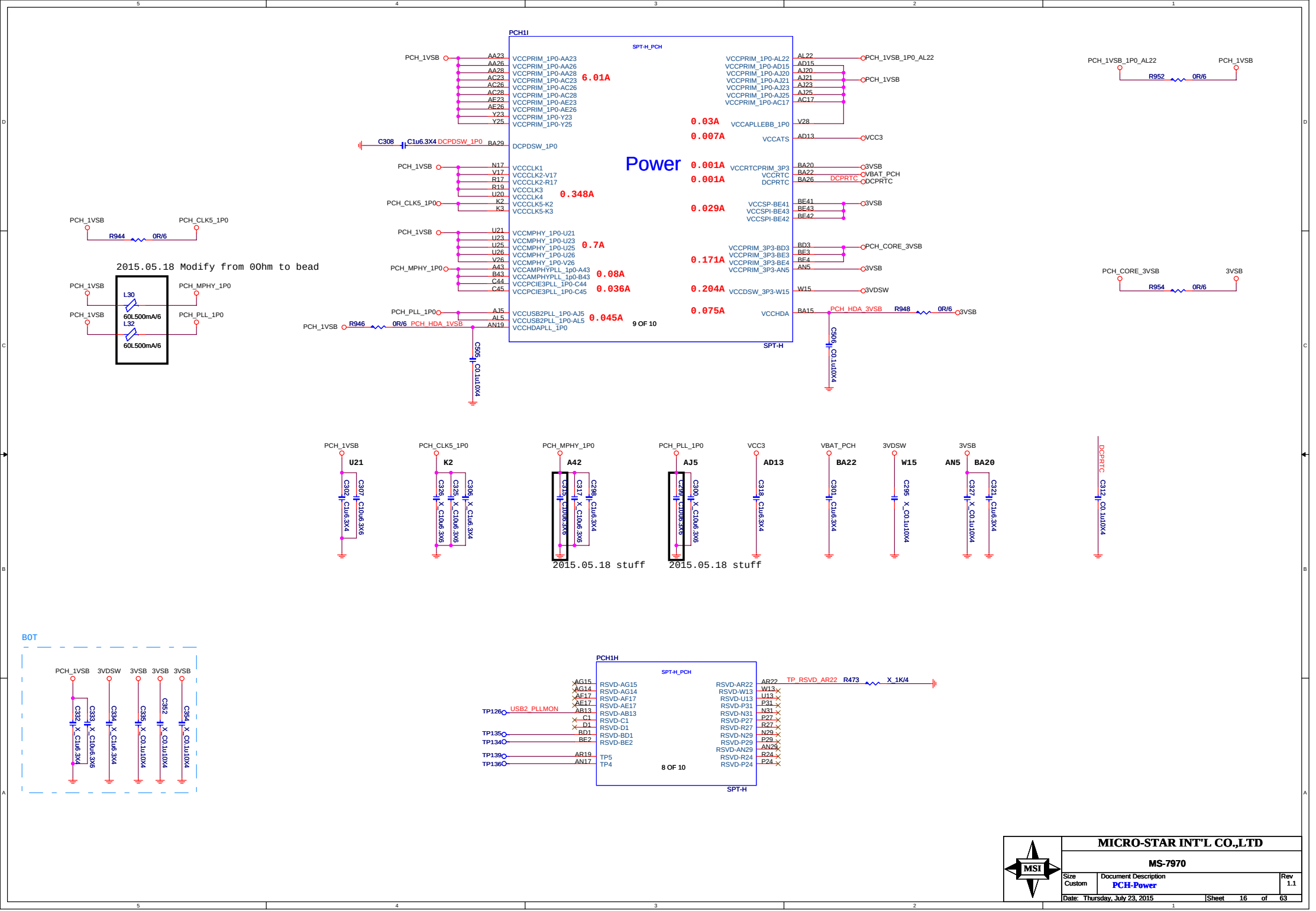
PCH1I
SPT-H_PCH
Power
6.01A
0.348A
0.7A
0.08A
0.036A
0.045A
0.03A
0.007A
0.001A
0.001A
0.029A
0.171A
0.204A
0.075A
9 OF 10
SPT-H
PCH_1VSB
PCH_CLK5_1P0
PCH_MPHY_1P0
PCH_PLL_1P0
PCH_1VSB_1P0_AL22
PCH_CORE_3VSB
3VSB
VBAT_PCH
3VDSW
DCPRTC
R944 0R/6
R952 0R/6
R954 0R/6
R946 0R/6 PCH_HDA_1VSB
R948 0R/6
C308 C1u6.3X4 DCPDSW_1P0
C505 C0.1u10X4
C506 C0.1u10X4
2015.05.18 Modify from 0Ohm to bead
L30 60L500mA/6
L32 60L500mA/6
2015.05.18 stuff
2015.05.18 stuff
BOT
PCH1H
SPT-H_PCH
8 OF 10
SPT-H
TP_RSVD_AR22 R473 X_1K/4
USB2_PLLMON
MICRO-STAR INT'L CO.,LTD
MS-7970
PCH-Power
Size Custom
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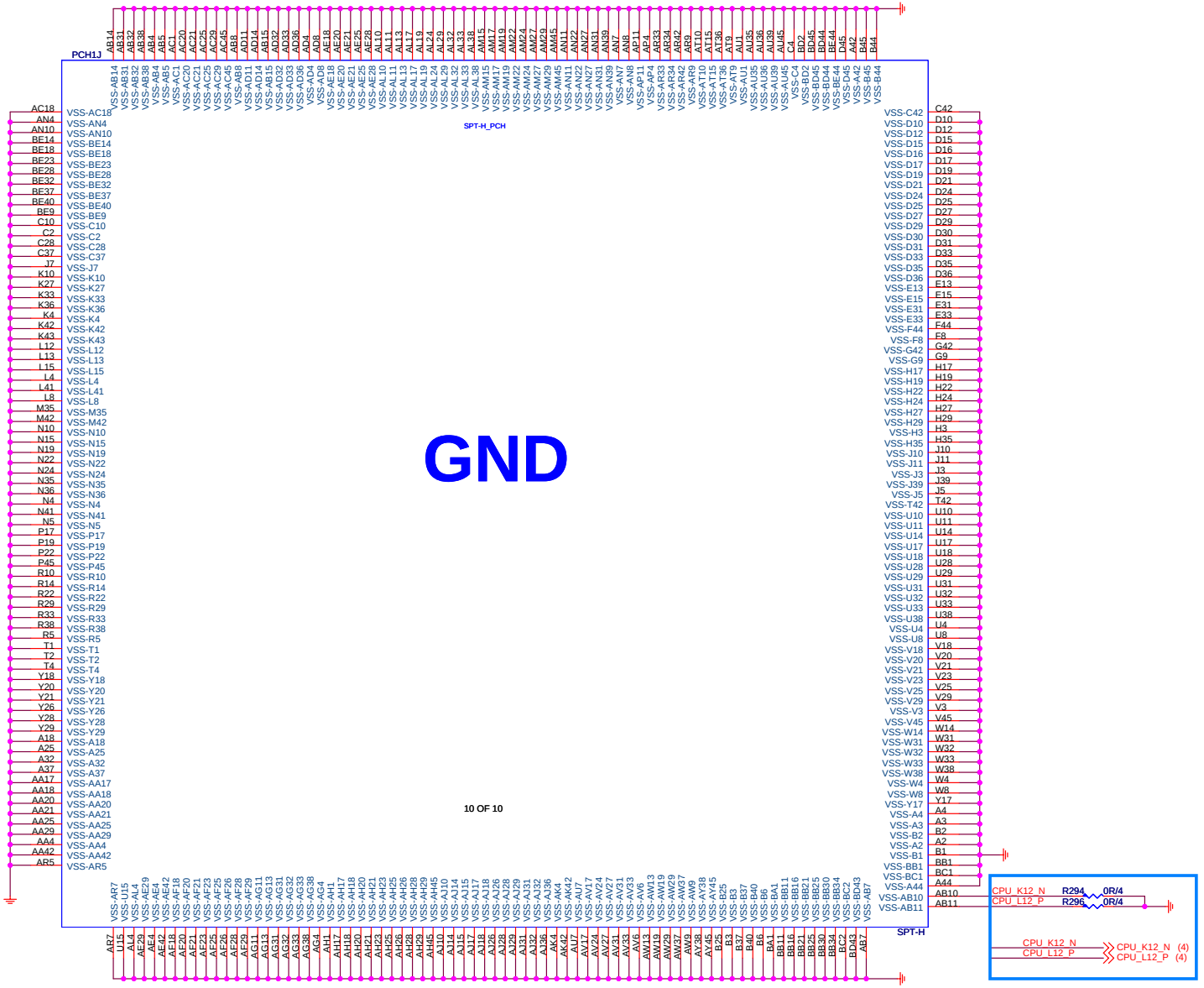

MICRO-STAR INT'L CO.,LTD	
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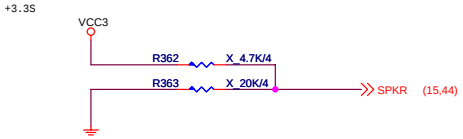
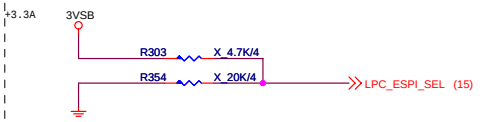
TOP Swap



Internal pull-down is disabled after PLTRST#

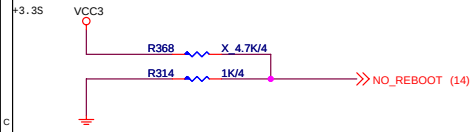
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

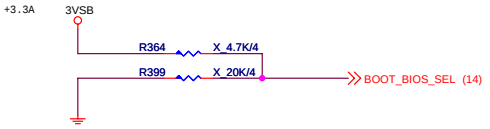
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

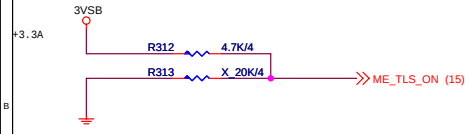
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

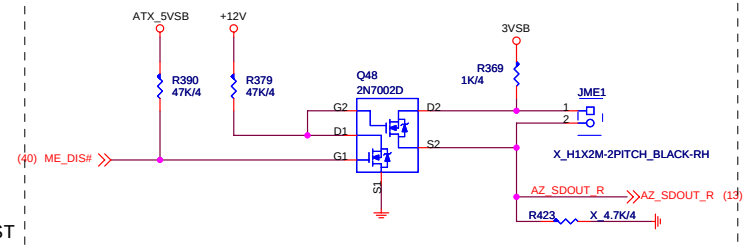
AMT and SBA with confidentiality



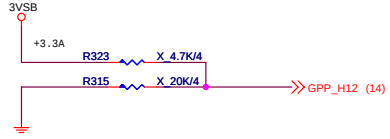
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down is disabled after RSMRST

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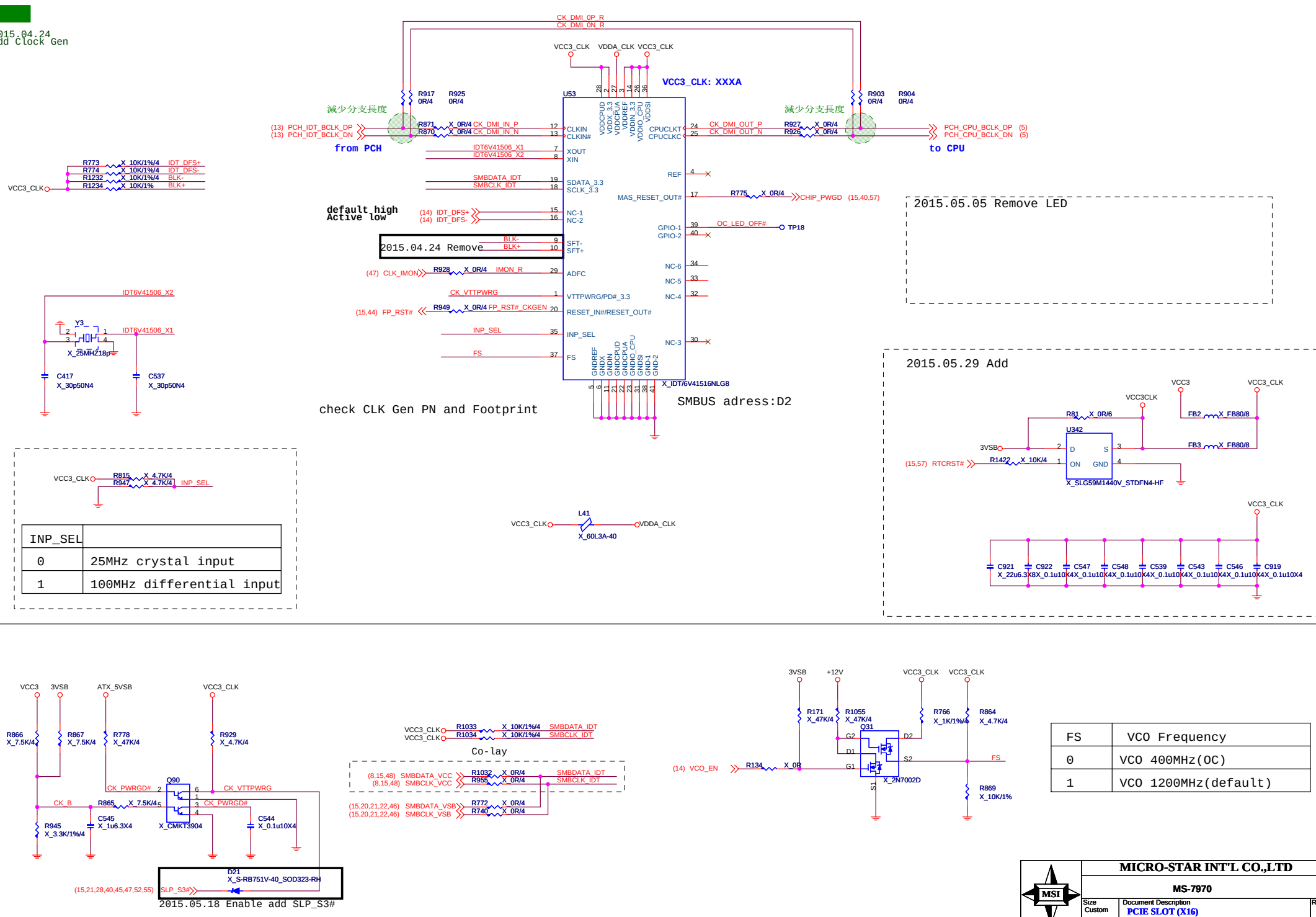
2015.04.24
Add Clock Gen



INP_SEL	
0	25MHz crystal input
1	100MHz differential input

FS	VCO Frequency
0	VCO 400MHz(OC)
1	VCO 1200MHz(default)

MICRO-STAR INT'L CO.,LTD

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Custom	PCIE SLOT (X16)	1.1

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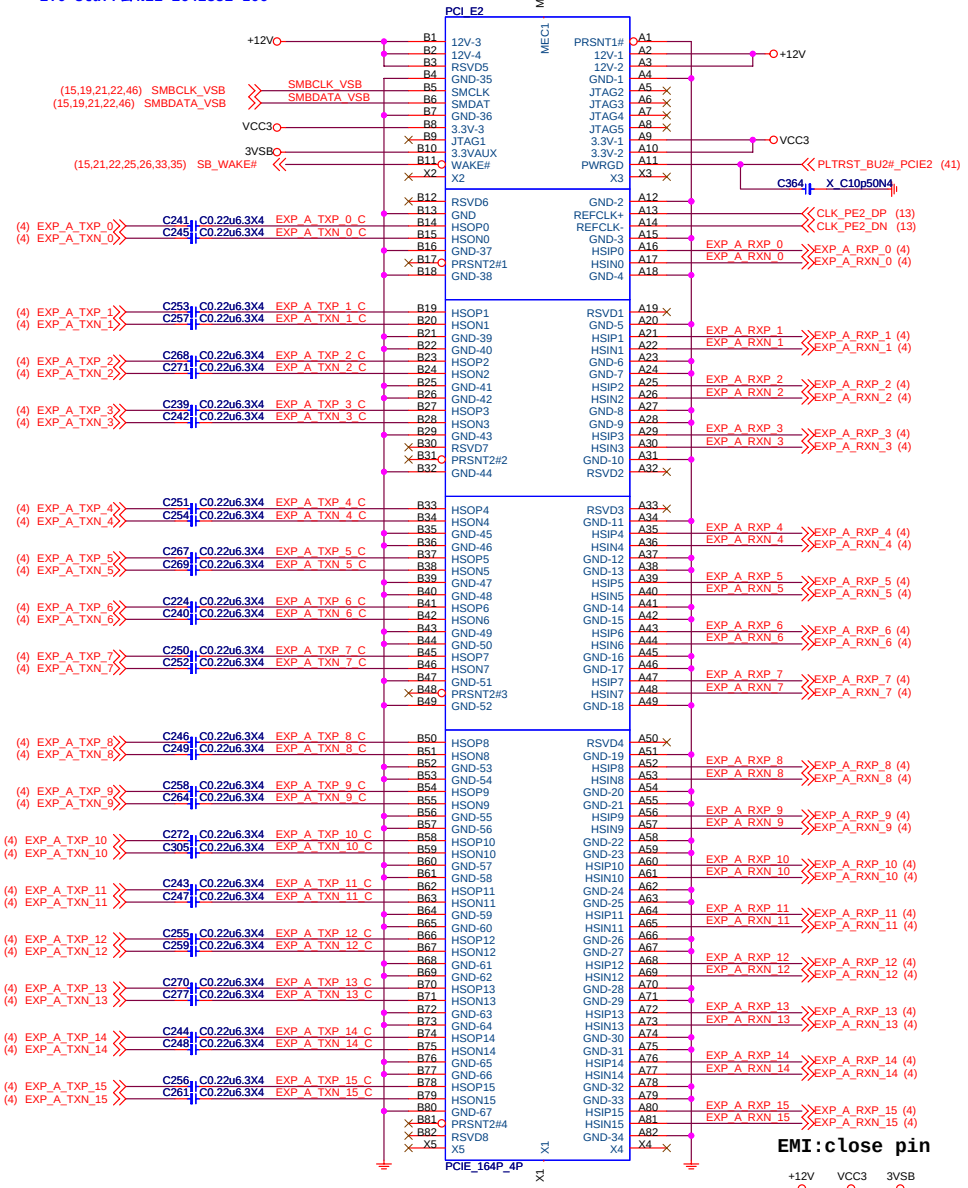
PCI_Express X16 Slot

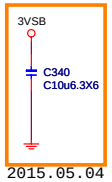
support max speed GEN3

Black

footprint ON1-7968002
1.0 stuff N11-1641221-L06
2.0 stuff N11-1641331-L06



Close to Slot



2015.05.04 Add for improve 5VDUAL Drop issue.

2015.04.23 Remove switch

2015.04.23 Remove

SEL	MODE_1	MODE_0
8X/8X	1	1
16X	1	0
8X/8X	0	1
16X	0	0

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	PCIE SLOT (X16)	1.1

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2015.04.28 Remove X8 slot and Add switch for X1 slot

PCI_Express X4 Slot

support max speed GEN3

Black

Truth Table

Function \ SEL	L	H
Function	IN+ to outa+	IN+ to outb+

Close to Slot

2015.05.04 Add for improve 5VDUAL Drop issue.

2015.05.22 Modify X1 detect circuit

GPP_G3	LOW(I)	HIGH(I)	LOW(I)
GPP_G4	LOW(I)	HIGH(O)	HIGH(I)
	X4/X0/X0/X0	X1/X1/X1/X1	X2/X0/X1/X1

EMI:close pin

JTBT

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Size: Custom	Document Description: PCIE SLOT (X4)/TBT — Rev: 1.1
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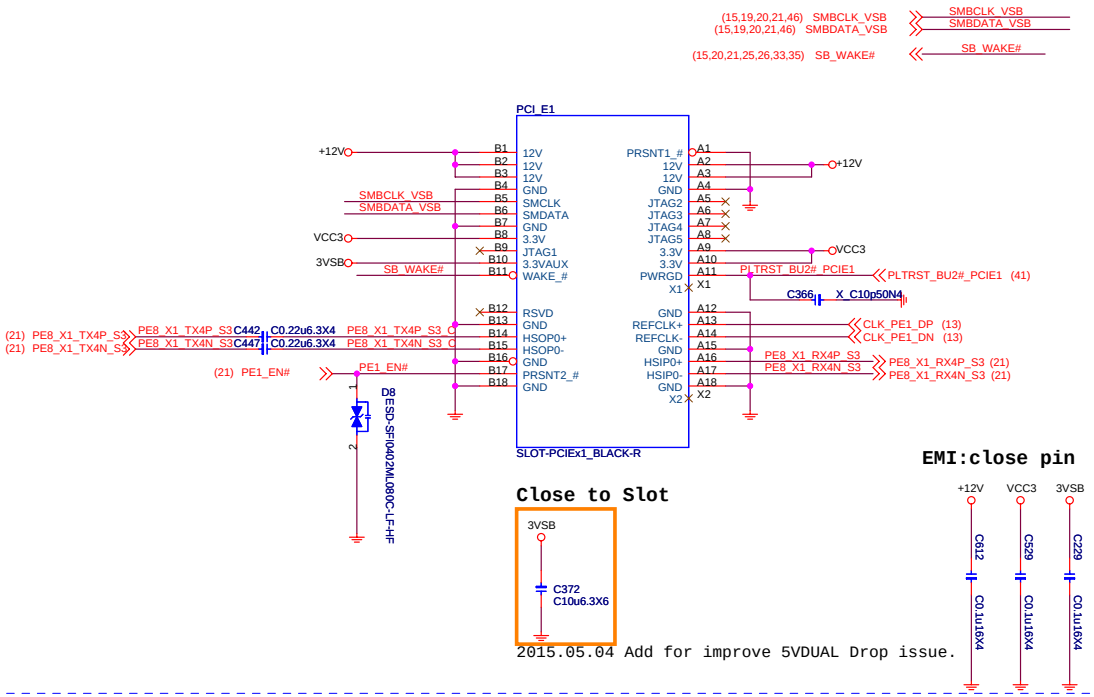
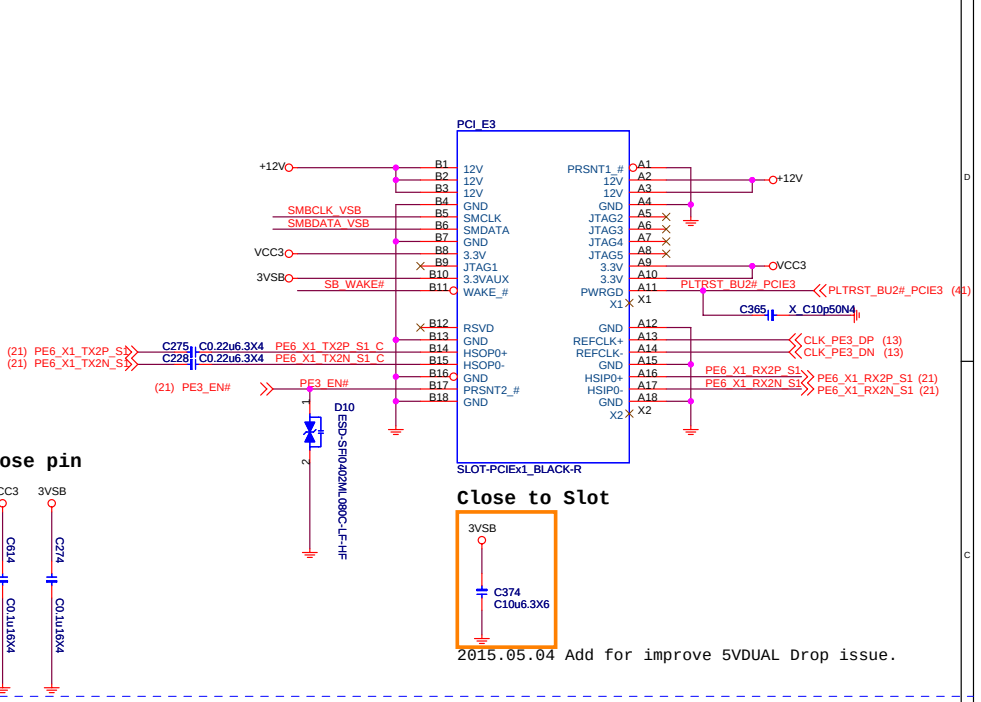
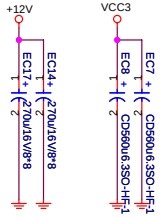
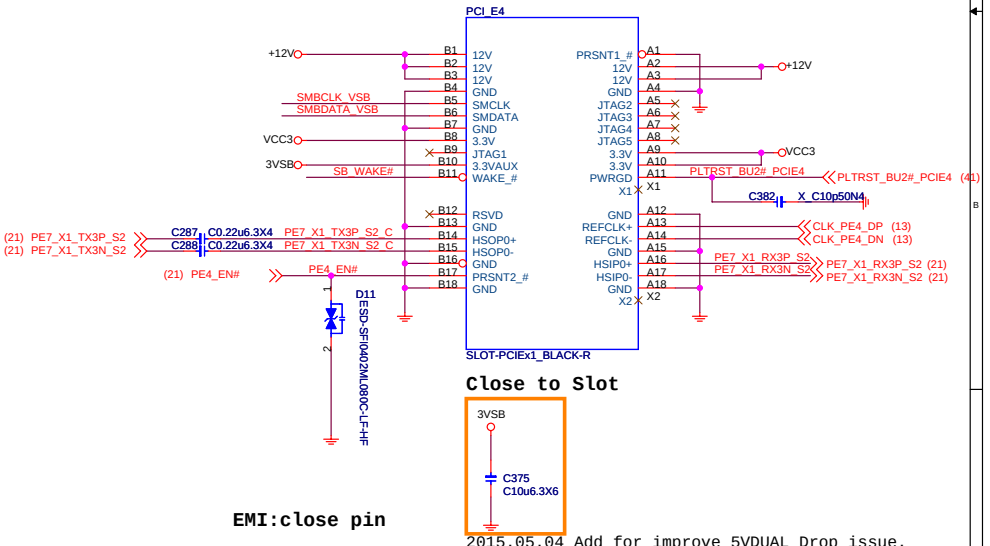




PCIE(X1) *3 PCIE(X4)*1 PCIE(X16)*1

3.3Vaux:0.375*5=1.5A(wake)
0.02*4=0.1A(no wake)
VCC3:3*5=15A
+12V:0.5*3+2.1+5.5=9.1A





MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7970	
Size: Custom	Document Description: PCIE SLOT (X1)	Rev: 1.1
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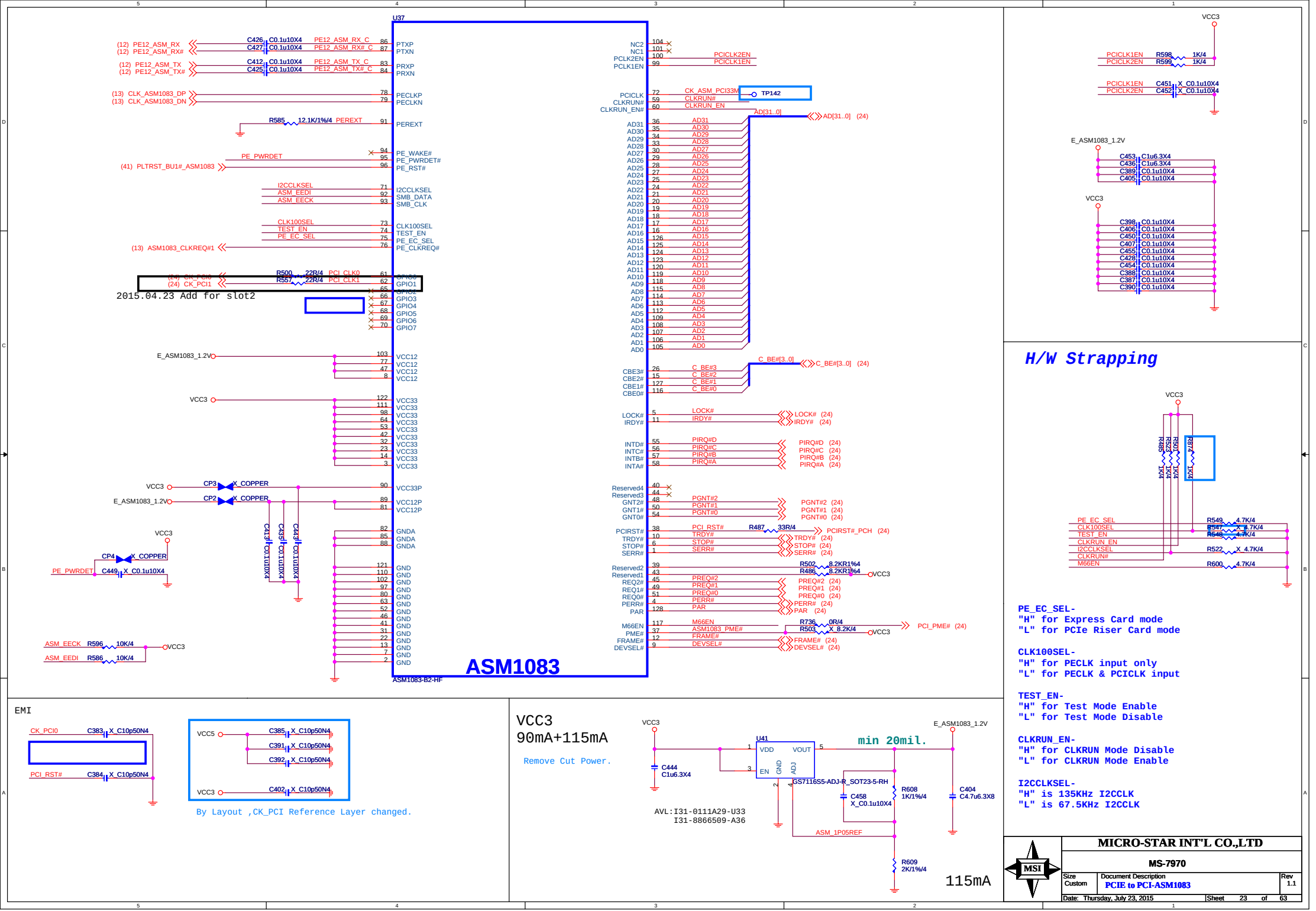
U37
ASM1083
ASM1083-B2-HF
2015.04.23 Add for slot2
E_ASM1083_1.2V
VCC3
VCC33P
VCC12P
GNDA
GND
PTXP
PTXN
PRXP
PRXN
PECLKP
PECLKN
PEREXT
PE_WAKE#
PE_PWRDET#
PE_RST#
I2CCLKSEL
SMB_DATA
SMB_CLK
CLK100SEL
TEST_EN
PE_EC_SEL
PE_CLKREQ#
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
PCICLK2EN
PCICLK1EN
PCICLK
CLKRUN#
CLKRUN_EN#
TP142
AD[31..0]
C_BE#[3..0]
LOCK#
IRDY#
INTD#
INTC#
INTB#
INTA#
PCIRST#
TRDY#
STOP#
SERR#
PREQ#2
PREQ#1
PREQ#0
PERR#
PAR
M66EN
PME#
FRAME#
DEVSEL#
PCI_PME#
EMI
CK_PCI0
PCI_RST#
VCC5
By Layout ,CK_PCI Reference Layer changed.
VCC3
90mA+115mA
Remove Cut Power.
U41
GS7116S5-ADJ-R_SOT23-5-RH
min 20mil.
AVL:I31-0111A29-U33
I31-8866509-A36
115mA
H/W Strapping
PE_EC_SEL-
"H" for Express Card mode
"L" for PCIe Riser Card mode
CLK100SEL-
"H" for PECLK input only
"L" for PECLK & PCICLK input
TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable
CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable
I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK
MICRO-STAR INT'L CO.,LTD
MS-7970
PCIE to PCI-ASM1083
Size Custom
Rev 1.1
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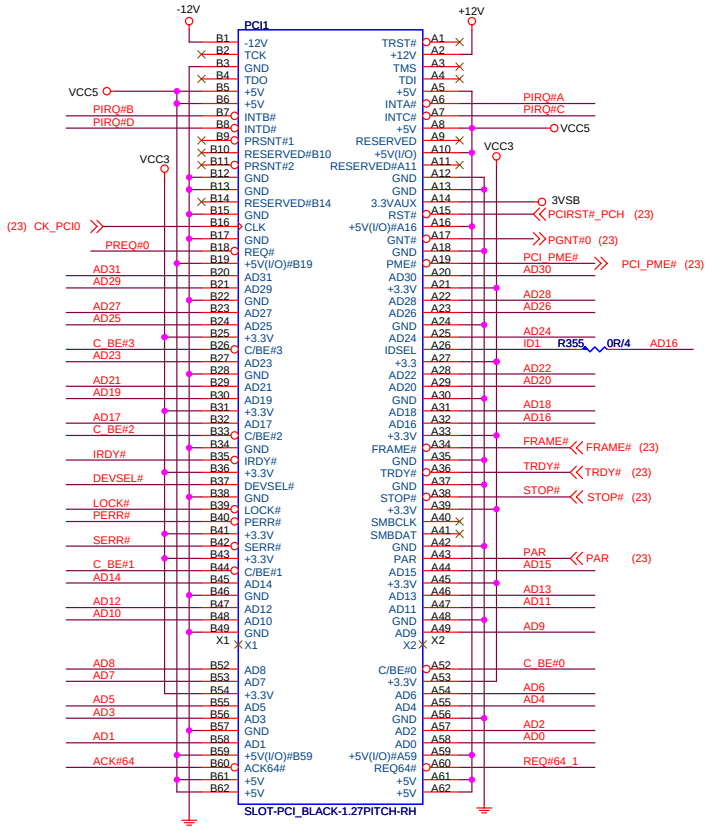
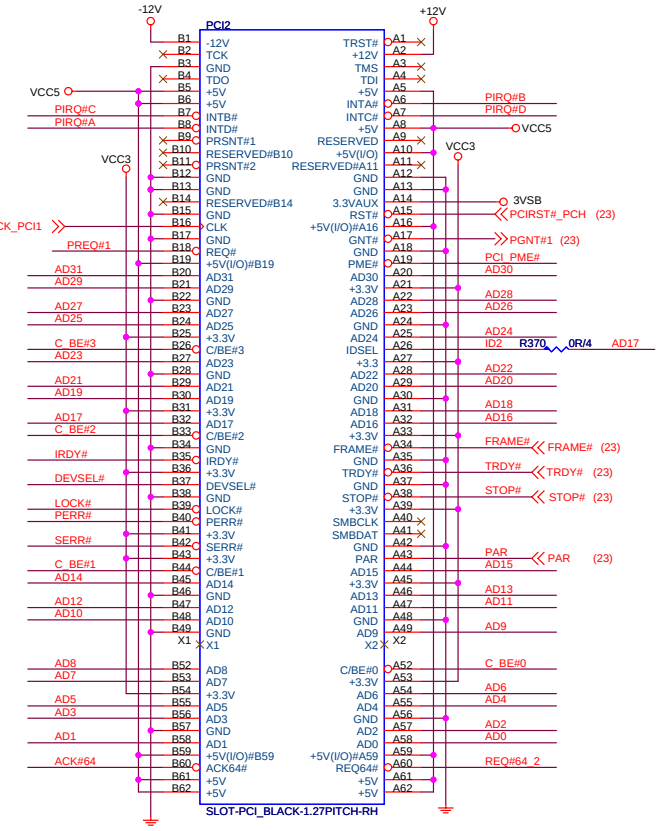


IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

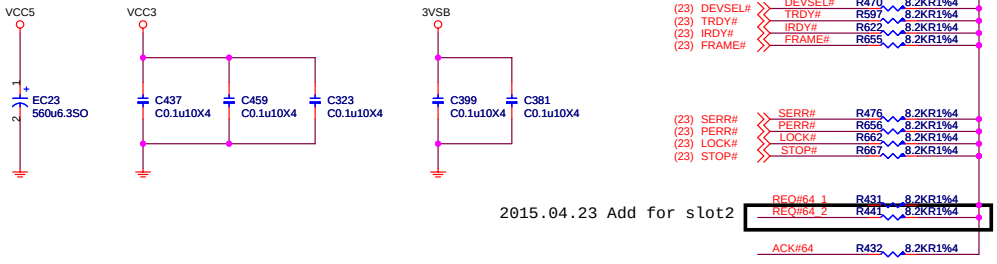


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B
2015.04.23 Add for slot2

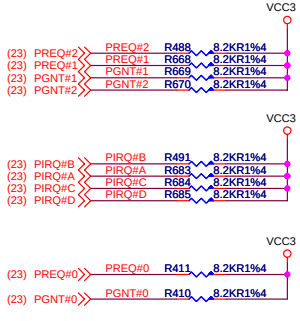
AD[31..0] AD[31..0] (23)

C_BE#[3..0] C_BE#[3..0] (23)

PCI PULL-UP / DOWN RESISTORS



2015.04.23 Add for slot2



PCI slot (X3)	
+3.3Vaux (wake)	- 1125mA
+3.3Vaux (no wake)	- 60mA
+3.3V	- 7.6A
+5V	- 15A
+12V	- 1.5A

MICRO-STAR INT'L CO.,LTD

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Custom	PCI SLOT	1.1

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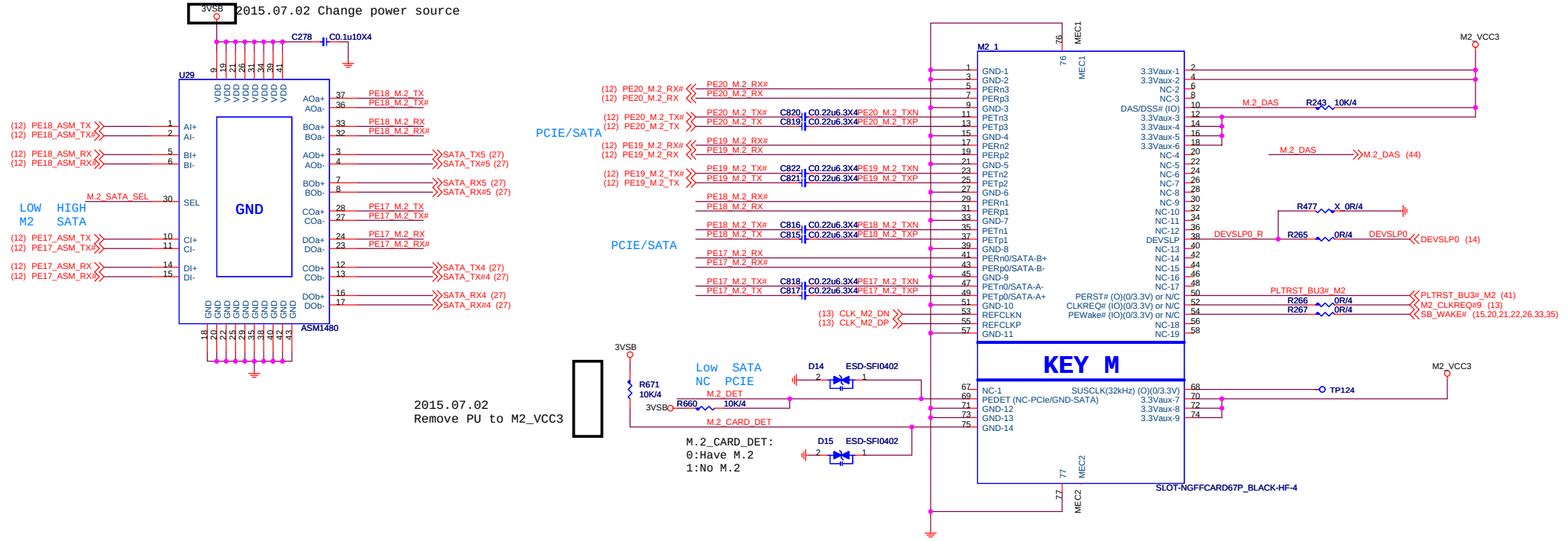
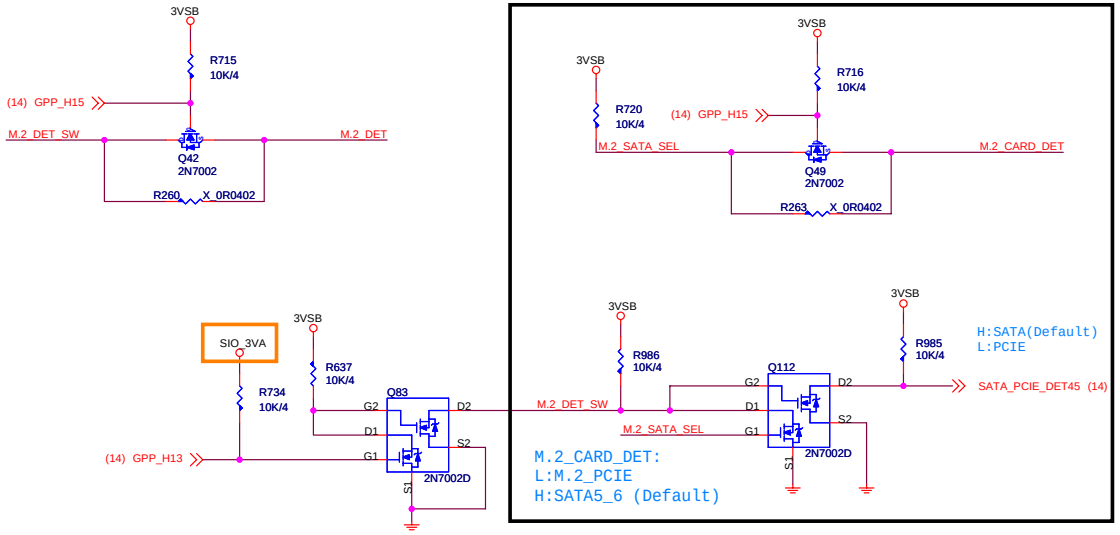
2015.07.02 Change power source



2015.07.08 ADD



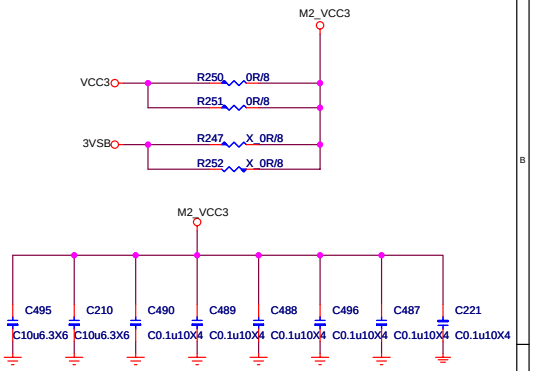
BIOS_MODE

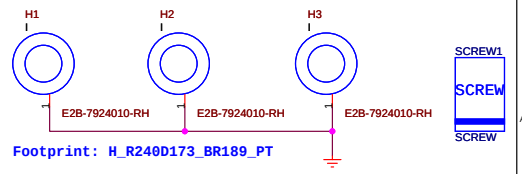
M2_2_GPP5	M2_2_GPP7	Mode
0	0	M2-SATA
1	0	M2-PCIE
GPI	1	AUTO

	SATA CARD	PCIE CARD	NA	NO CARD
M.2_DET	0	1	0	1
M.2_CARD_DET	0	0	1	1
SATA4/5GP 1 SATA MODE 0 PCIE MODE	1	0	1	1

SATA4GP/SATA5GP
for chipset that main power,if pull up to VSB maybe will leakage power
If sampled value = 1, select SATA; if sampled value = 0, select PCIe

2.5A





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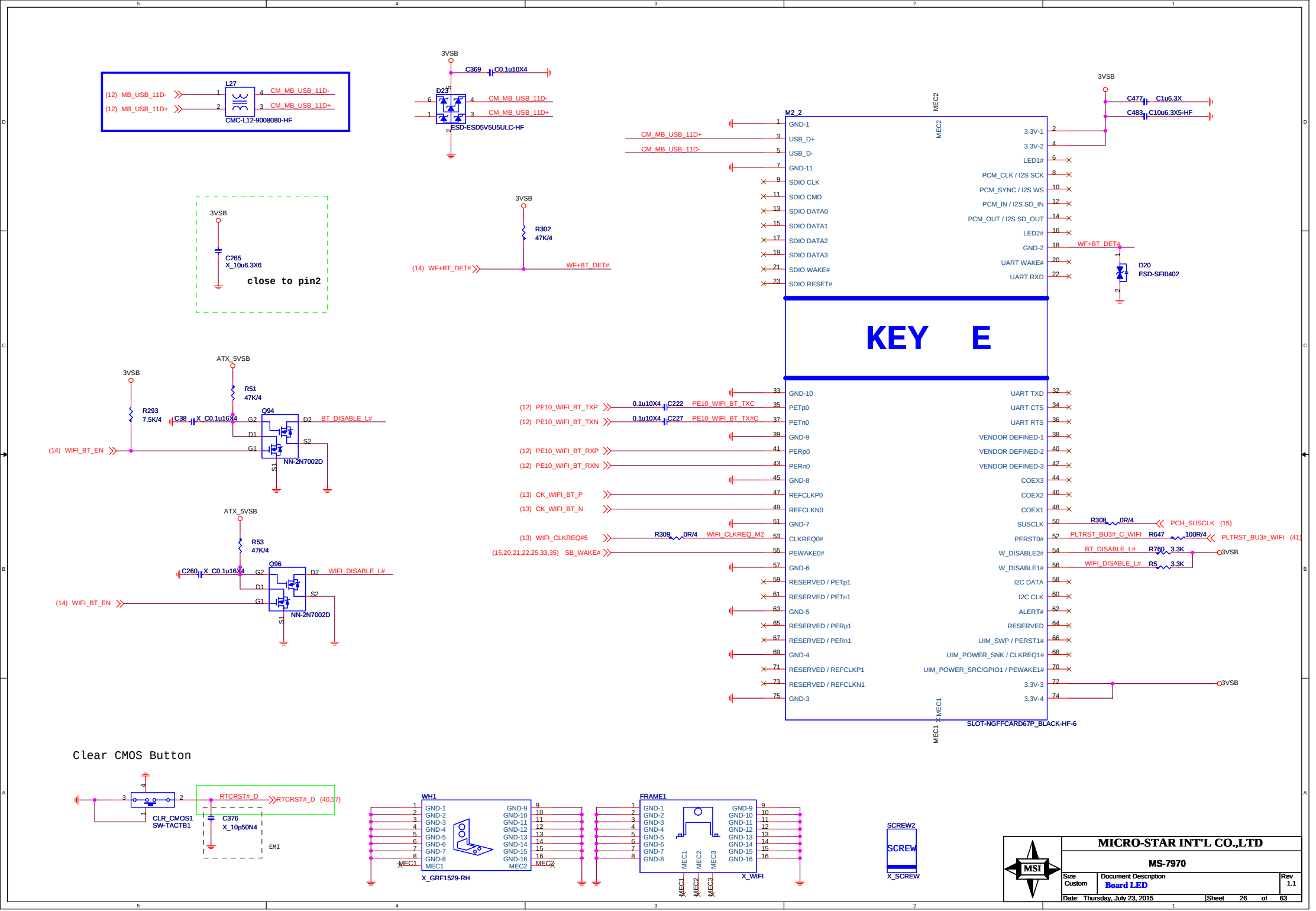
L27
(12) MB_USB_11D-
(12) MB_USB_11D+
CM_MB_USB_11D-
CM_MB_USB_11D+
CMC-L12-9008080-HF
3VSB
C369
C0.1u10X4
D23
ESD-ESD5V5U5ULC-HF
C265
X_10u6.3X6
close to pin2
R302
47K/4
(14) WF+BT_DET#
WF+BT_DET#
M2_2
MEC2
GND-1
USB_D+
USB_D-
GND-11
SDIO CLK
SDIO CMD
SDIO DATA0
SDIO DATA1
SDIO DATA2
SDIO DATA3
SDIO WAKE#
SDIO RESET#
3.3V-1
3.3V-2
LED1#
PCM_CLK / I2S SCK
PCM_SYNC / I2S WS
PCM_IN / I2S SD_IN
PCM_OUT / I2S SD_OUT
LED2#
GND-2
UART WAKE#
UART RXD
C477
C1u6.3X
C483
C10u6.3X5-HF
D20
ESD-SFI0402
KEY E
ATX_5VSB
R51
47K/4
R293
7.5K/4
C38
X_C0.1u16X4
Q94
BT_DISABLE_L#
(14) WIFI_BT_EN
NN-2N7002D
R53
47K/4
C260
Q96
WIFI_DISABLE_L#
GND-10
PETp0
PETn0
GND-9
PERp0
PERn0
GND-8
REFCLKP0
REFCLKN0
GND-7
CLKREQ0#
PEWAKE0#
GND-6
RESERVED / PETp1
RESERVED / PETn1
GND-5
RESERVED / PERp1
RESERVED / PERn1
GND-4
RESERVED / REFCLKP1
RESERVED / REFCLKN1
GND-3
(12) PE10_WIFI_BT_TXP
(12) PE10_WIFI_BT_TXN
(12) PE10_WIFI_BT_RXP
(12) PE10_WIFI_BT_RXN
(13) CK_WIFI_BT_P
(13) CK_WIFI_BT_N
(13) WIFI_CLKREQ#5
(15,20,21,22,25,33,35) SB_WAKE#
0.1u10X4
C222
PE10_WIFI_BT_TXC
C227
PE10_WIFI_BT_TX#C
R309
0R/4
WIFI_CLKREQ_M2
UART TXD
UART CTS
UART RTS
VENDOR DEFINED-1
VENDOR DEFINED-2
VENDOR DEFINED-3
COEX3
COEX2
COEX1
SUSCLK
PERST0#
W_DISABLE2#
W_DISABLE1#
I2C DATA
I2C CLK
ALERT#
RESERVED
UIM_SWP / PERST1#
UIM_POWER_SNK / CLKREQ1#
UIM_POWER_SRC/GPIO1 / PEWAKE1#
3.3V-3
3.3V-4
R308
0R/4
PCH_SUSCLK (15)
PLTRST_BU3# C_WIFI
R647
100R/4
PLTRST_BU3#_WIFI (41)
BT_DISABLE_L#
R760
3.3K
WIFI_DISABLE_L#
R5
3.3K
SLOT-NGFFCARD67P_BLACK-HF-6
MEC1
Clear CMOS Button
RTCRST# D
RTCRST#_D (40,57)
CLR_CMOS1
SW-TACTB1
C376
X_10p50N4
EMI
WH1
X_GRF1529-RH
FRAME1
X_WIFI
SCREW2
SCREW
X_SCREW
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MS-7970
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Custom
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Board LED
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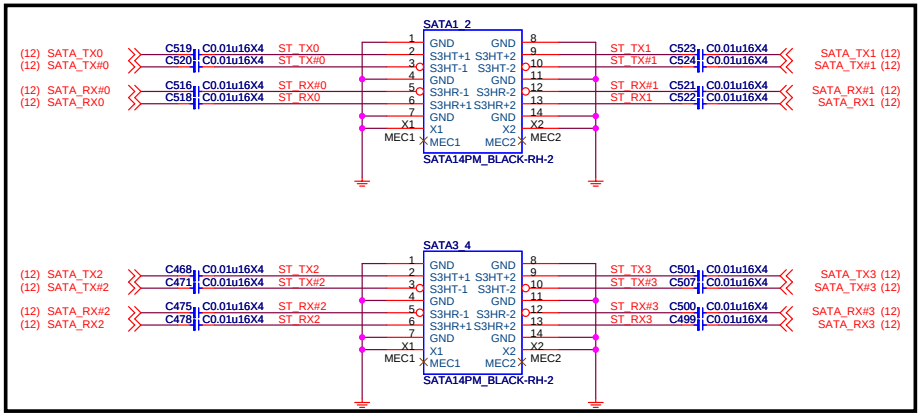
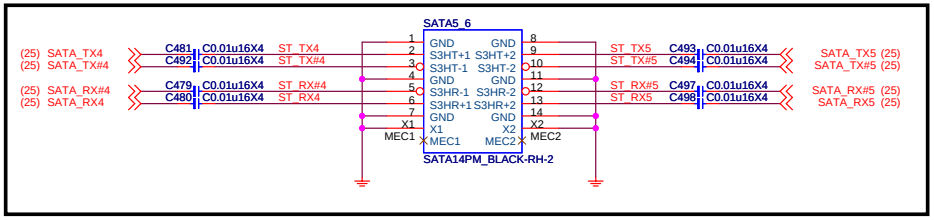
2015.05.12 Remove SE Re-Driver

2015.07.02 Remove SE connector

2015.07.02 Modify SPEC



2015.05.13 Change to 90 degree



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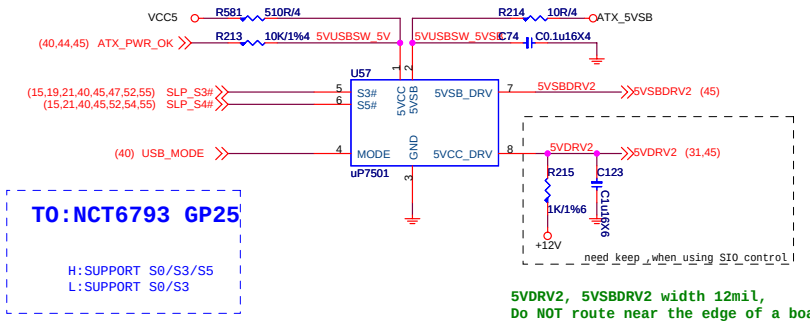
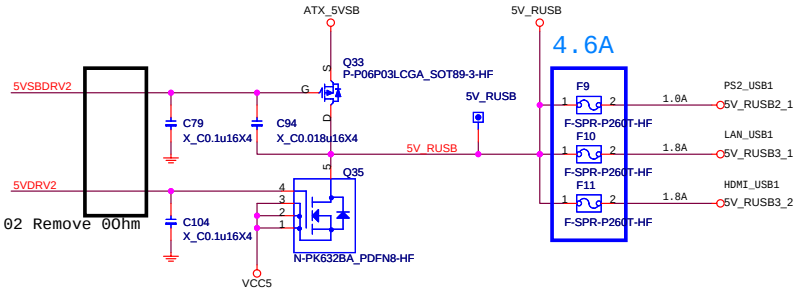
2015.04.27 Remove USB power MP1495



5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.

2015.07.02 Remove 0Ohm



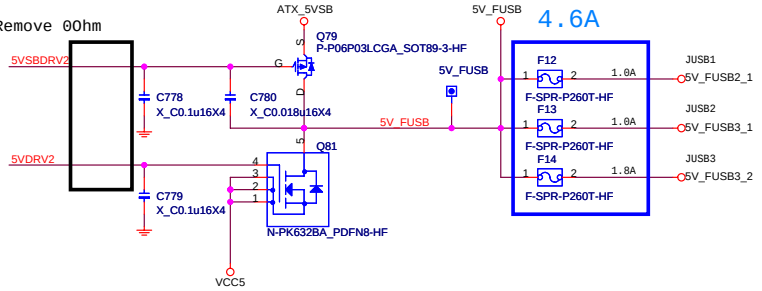
P-MOS
D03-06P0319-N03

N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

D08-2000300-P16 (Itrip=3.5A; 0.003ohm)
D08-0300700-P16 (Itrip=2.6A; 0.015ohm)

need confirm C780 value

2015.07.02 Remove 0Ohm



Front USB2.0 Voltage Drop Fail.

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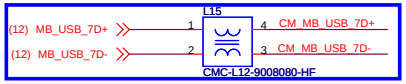
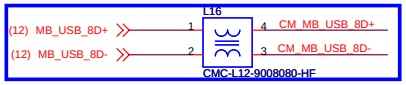
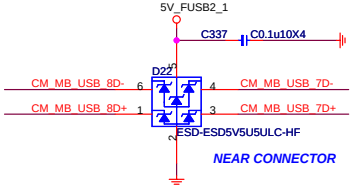
FRONT USB PORT 7,8

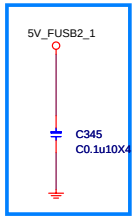


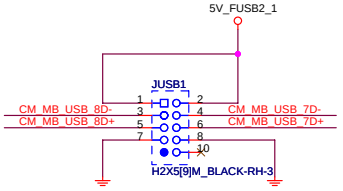


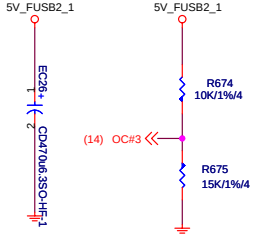


1.0A

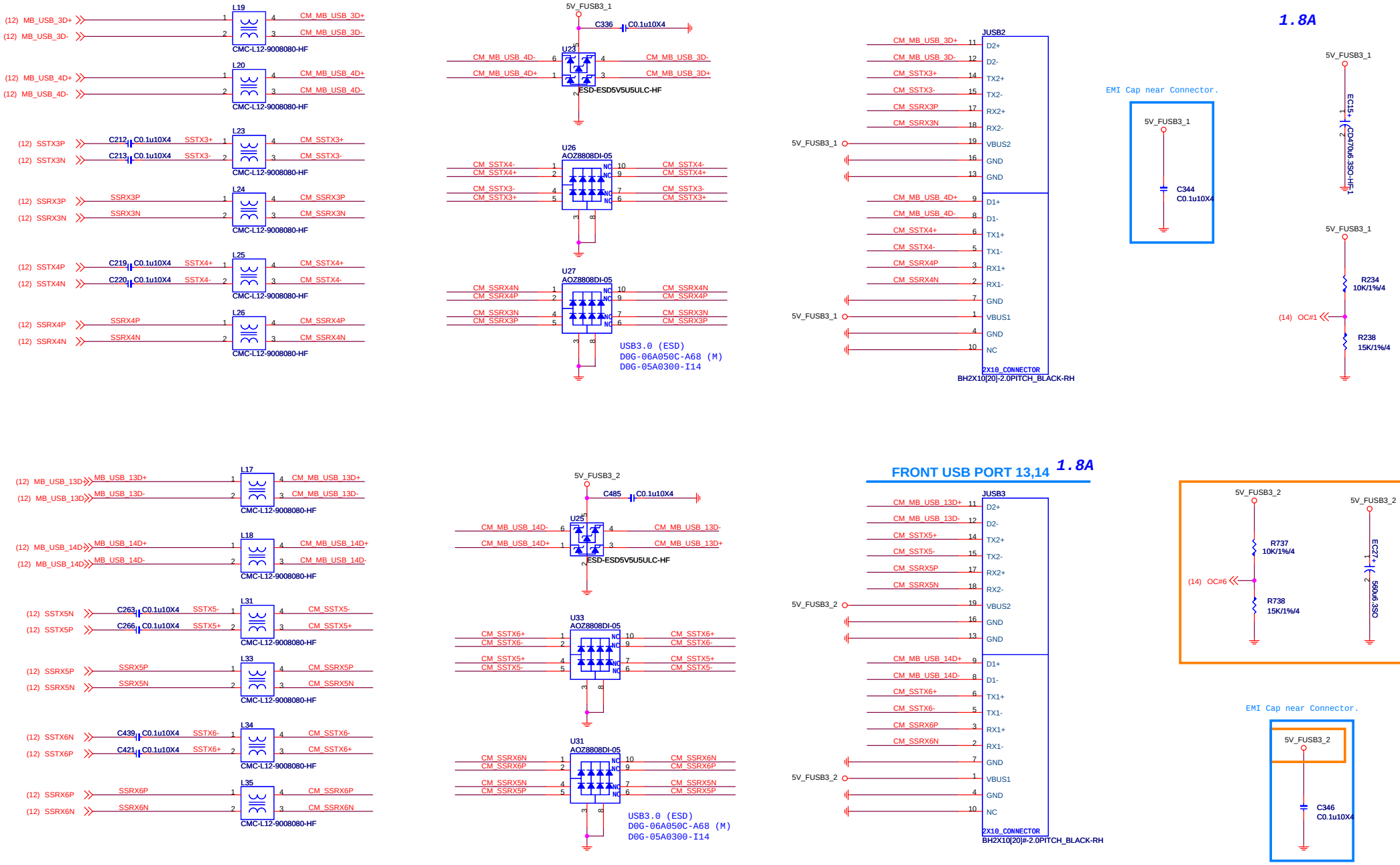
EMI Cap near Connector.







MICRO-STAR INT'L CO.,LTD		
MS-7970		
Size: Custom	Document Description: Front USB2.0	Rev: 1.1
Date: Thursday, July 23, 2015	Sheet 29 of 63	


L19
(12) MB_USB_3D+
(12) MB_USB_3D-
CM_MB_USB_3D+
CM_MB_USB_3D-
CMC-L12-9008080-HF
L20
(12) MB_USB_4D+
(12) MB_USB_4D-
CM_MB_USB_4D+
CM_MB_USB_4D-
CMC-L12-9008080-HF
L23
(12) SSTX3P
(12) SSTX3N
C212 C0.1u10X4
C213 C0.1u10X4
SSTX3+
SSTX3-
CM_SSTX3+
CM_SSTX3-
CMC-L12-9008080-HF
L24
(12) SSRX3P
(12) SSRX3N
SSRX3P
SSRX3N
CM_SSRX3P
CM_SSRX3N
CMC-L12-9008080-HF
L25
(12) SSTX4P
(12) SSTX4N
C219 C0.1u10X4
C220 C0.1u10X4
SSTX4+
SSTX4-
CM_SSTX4+
CM_SSTX4-
CMC-L12-9008080-HF
L26
(12) SSRX4P
(12) SSRX4N
SSRX4P
SSRX4N
CM_SSRX4P
CM_SSRX4N
CMC-L12-9008080-HF
5V_FUSB3_1
C336 C0.1u10X4
U23
CM_MB_USB_4D-
CM_MB_USB_4D+
CM_MB_USB_3D-
CM_MB_USB_3D+
ESD-ESD5V5U5ULC-HF
U26
AOZ8808DI-05
CM_SSTX4-
CM_SSTX4+
CM_SSTX3-
CM_SSTX3+
U27
AOZ8808DI-05
CM_SSRX4N
CM_SSRX4P
CM_SSRX3N
CM_SSRX3P
USB3.0 (ESD)
D0G-06A050C-A68 (M)
D0G-05A0300-I14
JUSB2
CM_MB_USB_3D+
CM_MB_USB_3D-
CM_SSTX3+
CM_SSTX3-
CM_SSRX3P
CM_SSRX3N
5V_FUSB3_1
CM_MB_USB_4D+
CM_MB_USB_4D-
CM_SSTX4+
CM_SSTX4-
CM_SSRX4P
CM_SSRX4N
5V_FUSB3_1
D2+
D2-
TX2+
TX2-
RX2+
RX2-
VBUS2
GND
GND
D1+
D1-
TX1+
TX1-
RX1+
RX1-
GND
VBUS1
GND
NC
2X10_CONNECTOR
BH2X10[20]-2.0PITCH_BLACK-RH
1.8A
EMI Cap near Connector.
5V_FUSB3_1
C344
C0.1u10X4
5V_FUSB3_1
EC15+
CD470u6.3SO-HF-L1
5V_FUSB3_1
R234
10K/1%/4
(14) OC#1
R238
15K/1%/4
L17
(12) MB_USB_13D+
(12) MB_USB_13D-
MB_USB_13D+
MB_USB_13D-
CM_MB_USB_13D+
CM_MB_USB_13D-
CMC-L12-9008080-HF
L18
(12) MB_USB_14D+
(12) MB_USB_14D-
MB_USB_14D+
MB_USB_14D-
CM_MB_USB_14D+
CM_MB_USB_14D-
CMC-L12-9008080-HF
L31
(12) SSTX5N
(12) SSTX5P
C263 C0.1u10X4
C266 C0.1u10X4
SSTX5-
SSTX5+
CM_SSTX5-
CM_SSTX5+
CMC-L12-9008080-HF
L33
(12) SSRX5P
(12) SSRX5N
SSRX5P
SSRX5N
CM_SSRX5P
CM_SSRX5N
CMC-L12-9008080-HF
L34
(12) SSTX6N
(12) SSTX6P
C439 C0.1u10X4
C421 C0.1u10X4
SSTX6-
SSTX6+
CM_SSTX6-
CM_SSTX6+
CMC-L12-9008080-HF
L35
(12) SSRX6P
(12) SSRX6N
SSRX6P
SSRX6N
CM_SSRX6P
CM_SSRX6N
CMC-L12-9008080-HF
5V_FUSB3_2
C485 C0.1u10X4
U25
CM_MB_USB_14D-
CM_MB_USB_14D+
CM_MB_USB_13D-
CM_MB_USB_13D+
ESD-ESD5V5U5ULC-HF
U33
AOZ8808DI-05
CM_SSTX6+
CM_SSTX6-
CM_SSTX5+
CM_SSTX5-
U31
AOZ8808DI-05
CM_SSRX6N
CM_SSRX6P
CM_SSRX5N
CM_SSRX5P
USB3.0 (ESD)
D0G-06A050C-A68 (M)
D0G-05A0300-I14
FRONT USB PORT 13,14
1.8A
JUSB3
CM_MB_USB_13D+
CM_MB_USB_13D-
CM_SSTX5+
CM_SSTX5-
CM_SSRX5P
CM_SSRX5N
5V_FUSB3_2
CM_MB_USB_14D+
CM_MB_USB_14D-
CM_SSTX6+
CM_SSTX6-
CM_SSRX6P
CM_SSRX6N
5V_FUSB3_2
D2+
D2-
TX2+
TX2-
RX2+
RX2-
VBUS2
GND
GND
D1+
D1-
TX1+
TX1-
RX1+
RX1-
GND
VBUS1
GND
NC
2X10_CONNECTOR
BH2X10[20]#-2.0PITCH_BLACK-RH
5V_FUSB3_2
R737
10K/1%/4
(14) OC#6
R738
15K/1%/4
5V_FUSB3_2
EC27+
560u6.3SO
EMI Cap near Connector.
5V_FUSB3_2
C346
C0.1u10X4
MICRO-STAR INT'L CO.,LTD
MS-7970
Size
Custom
Document Description
Front USB3.0
Rev
1.1
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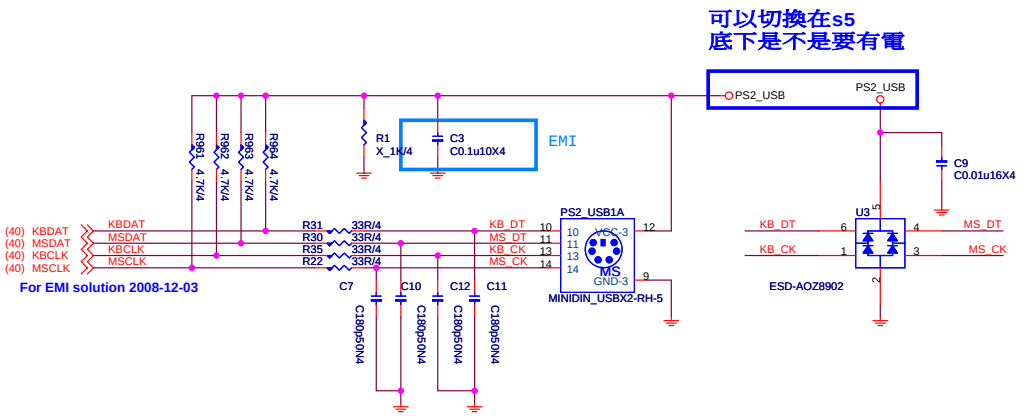
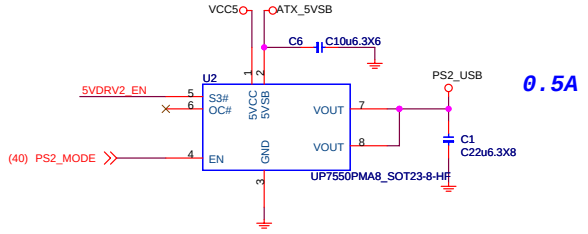
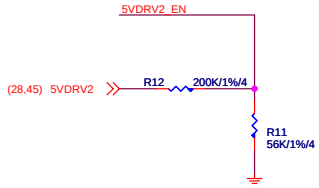
PS2 KEYBOARD & MOUSE CONNECTOR



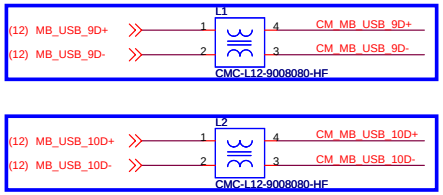
PS2 Power

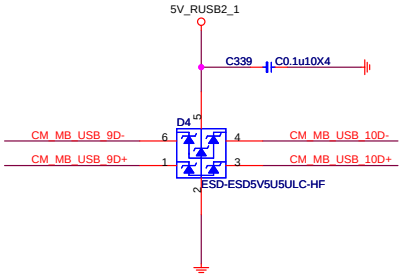


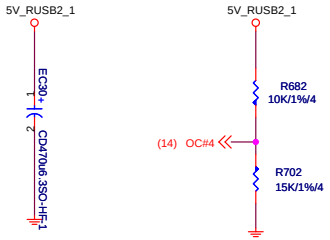
USB MODE



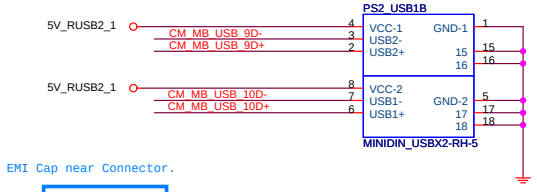
REAR USB PORT 2,3 (W/ PS2)



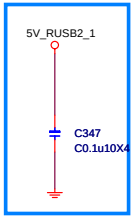




1.0A



EMI Cap near Connector.



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MS-7970		
Size: Custom	Document Description: Rear I/O PS2/USB2	Rev: 1.1
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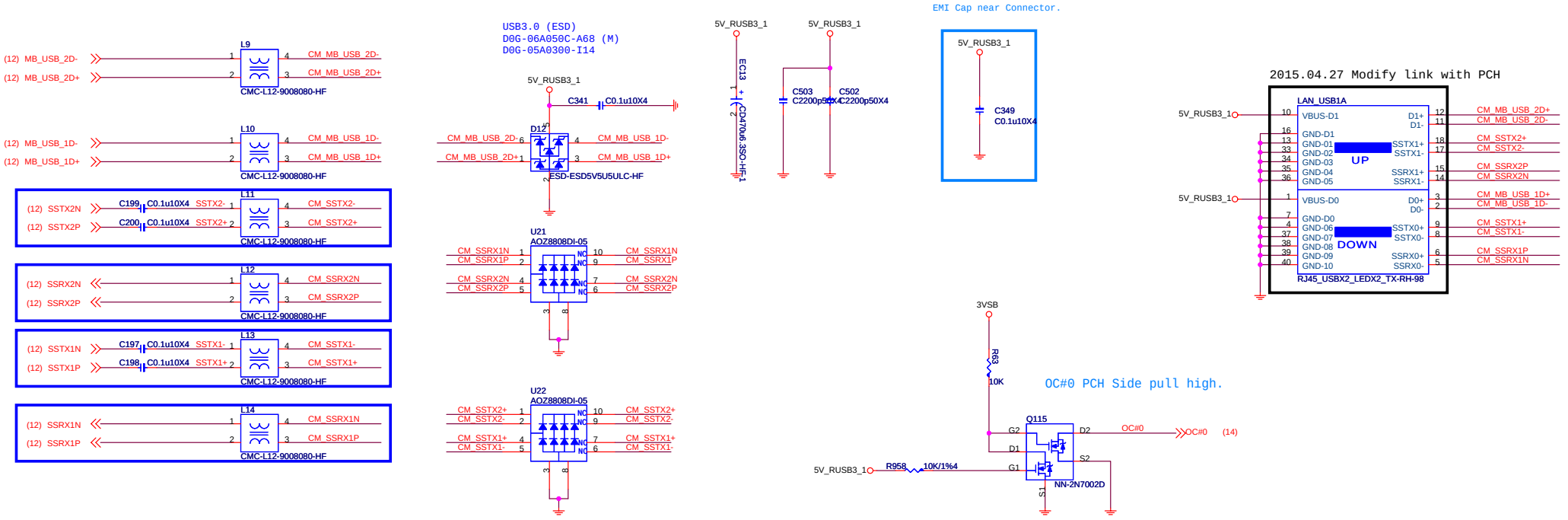

MICRO-STAR INT'L CO.,LTD		
MS-7970		
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Minimun gap should be greater of >15mil with other signal.

Chip to Connector ¯1.5 inch.
VIA Hole¯2

CLK Rule (Follow SB PDG)

PCIE Rule (Follow SB PDG)

USB HS (90Ohm-Diff)

USB SS (80Ohm-Diff)

USB HS (90Ohm-Diff)

USB SS (80Ohm-Diff)

PPON_X Internal Pull-up to VCC3

OCI_X Internal Pull-up to SUS

RX/TX Internal Pull-up

SMI connect to GPI which support smi function.
SB side need pull high 10K ohm to 3VSB.
(Intel 8X & 9X series use GPIO57)

2015.05.25 Remove co-lay power.

Remove Cut Power.

3VSB Total Current:246mA+635mA

X0/XI (95hm-Diff,Spacing 30mil)
UREXT,PEUREXT(W/S) : 10/7
OCIA,OCIB,PPONA,PPONB(W/S) : 5/8

ASM1042 1.05 VSB Power

635 mA

ASM1142 :RU32 change to 19.6K.(R11-3162T12-W08)

ASM1142 change to 2.2uF.

EEPROM

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Rev: 1.1	
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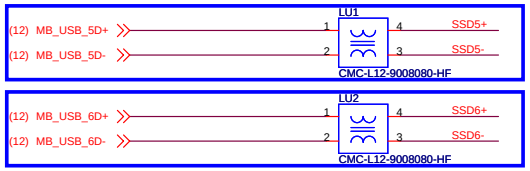
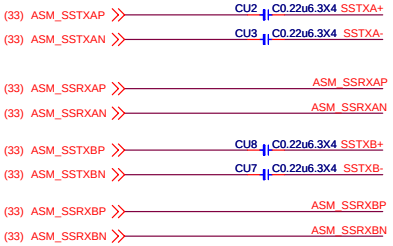
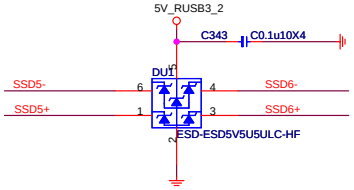
Rear USB3 CONN

Important~~
If USB3.0 signal conect to front pin header,
please must less than 1.5 inch,short trace
has better eye diagram with some bad fly cable by SI customer.



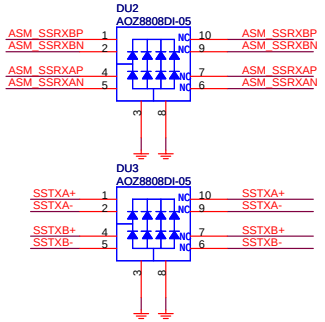


USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL

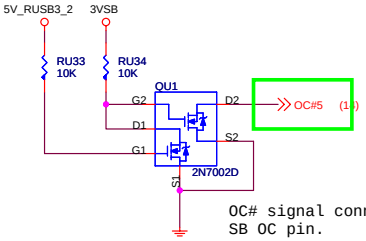


ESD Protection

NEAR CONNECTOR



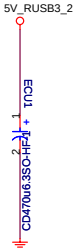
USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL



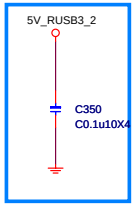
OC# signal connect to
SB OC pin.

min 80mil.

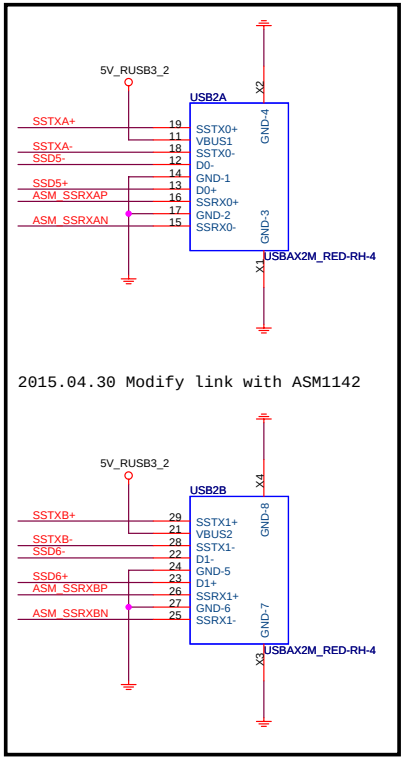
1.8 A



EMI Cap near Connector.



1.8A



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MS-7970		
Size: Custom	Document Description: Rear USB3.1 Connector	Rev: 1.1
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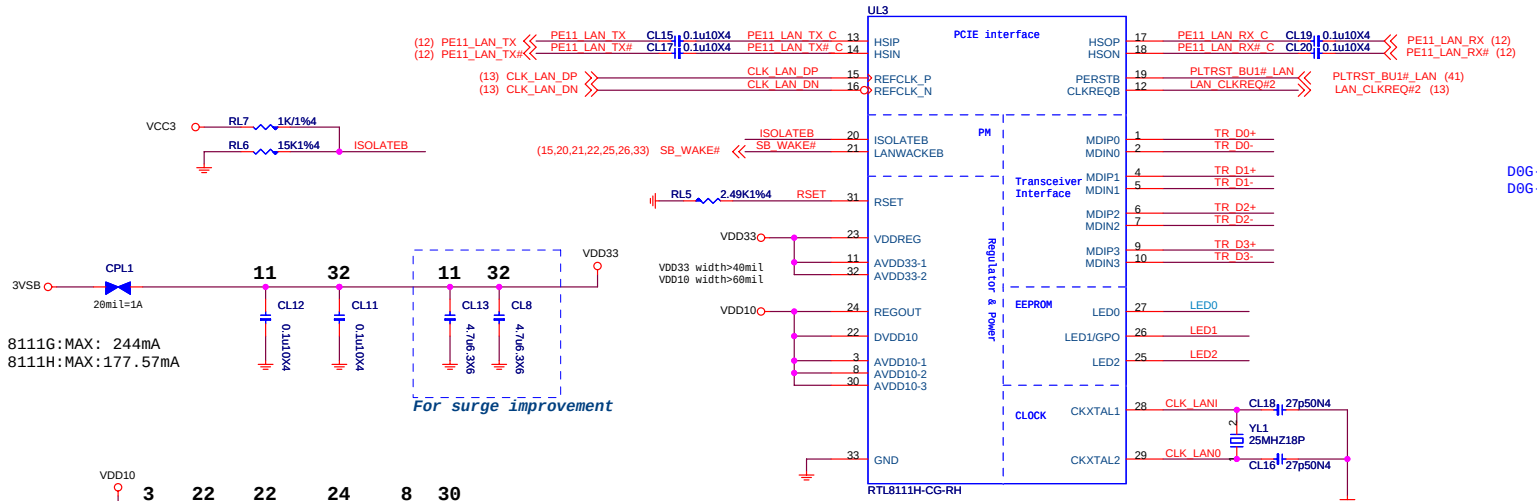
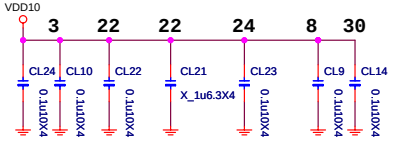
2015.04.23 Change from Intel LAN

RTL8111G/RTL8111H Giga LAN

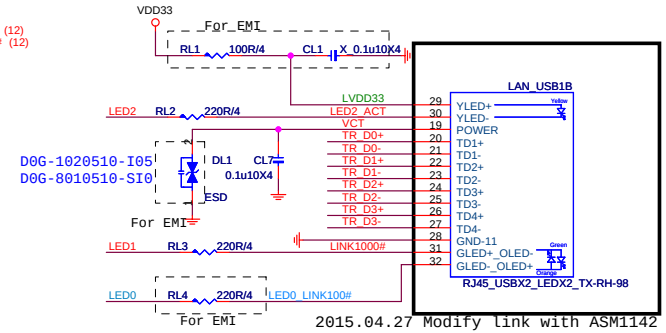
8111H:B06-08111CC-R09
8111G:B06-081116C-R09





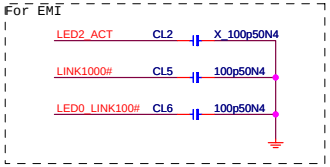
Pin33: 4 via from top layer to GND layer
and make the via at the center of IC.

LAN Connector



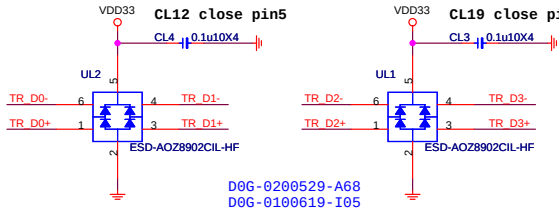
2015.04.27 Modify link with ASM1142

Update moduale 2015.05.25



ESD Protect

UL2&UL3 close to connector



D0G-0200529-A68
D0G-0100619-I05

8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

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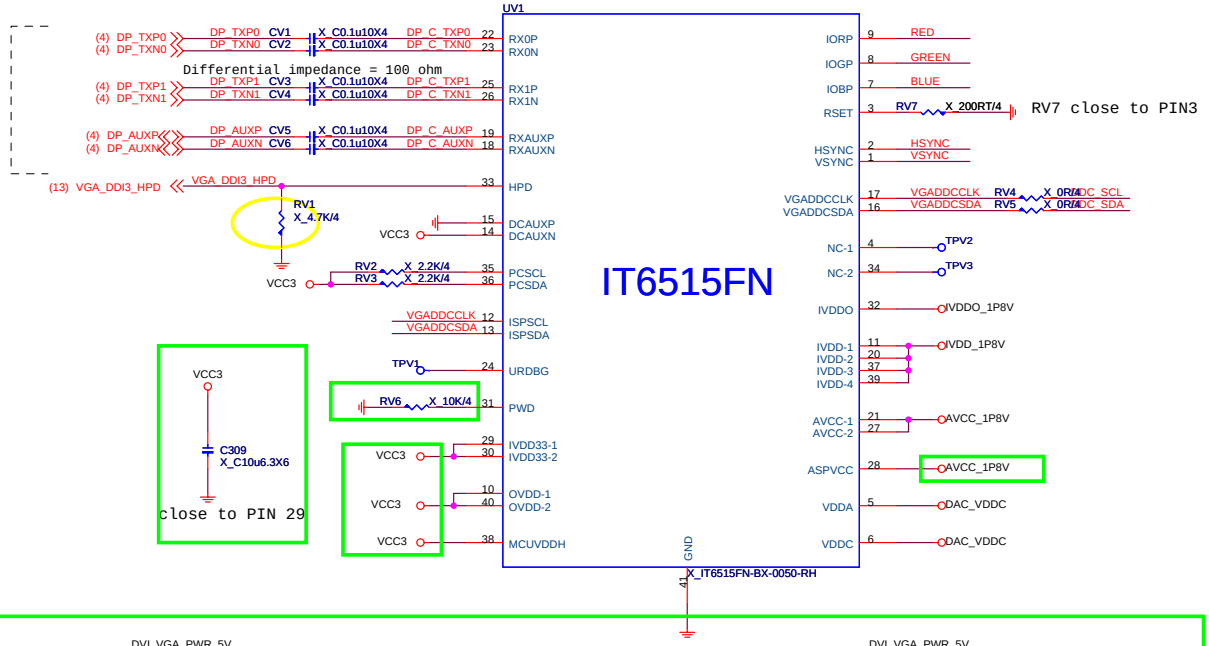
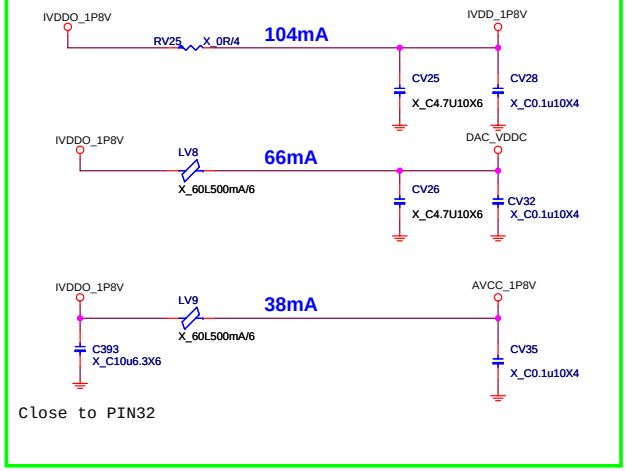
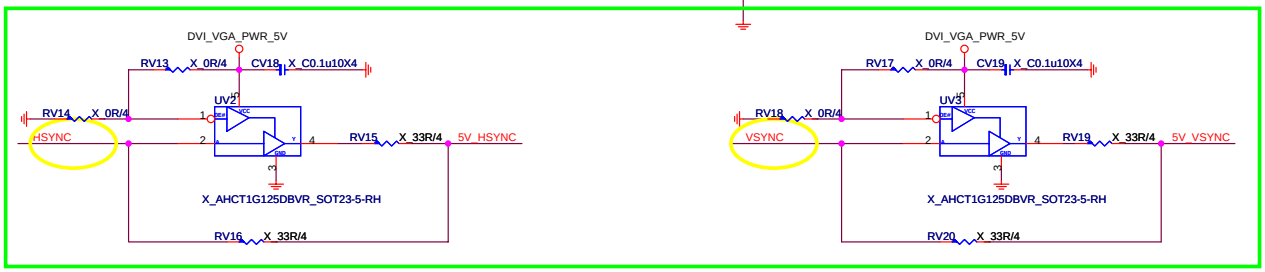
Note:

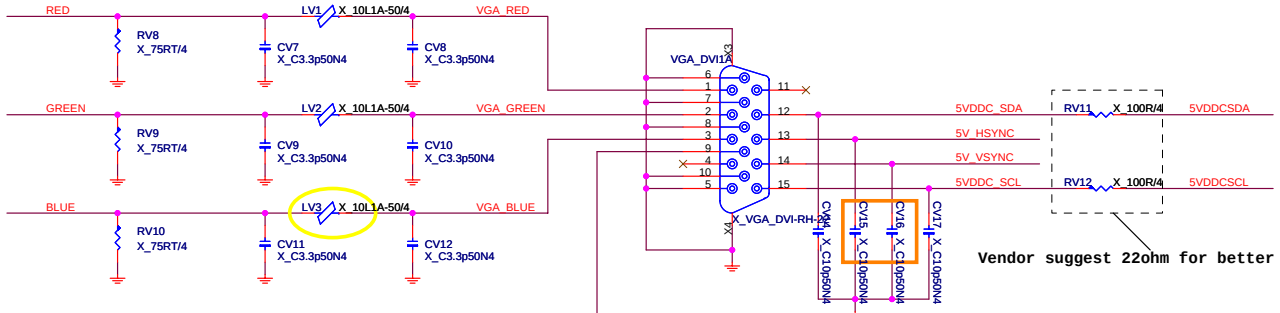
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

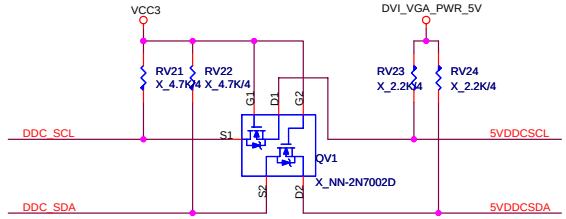


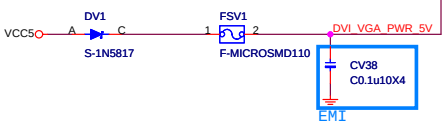
Remove

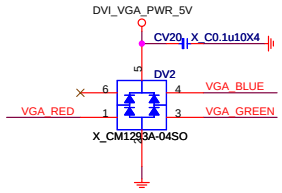


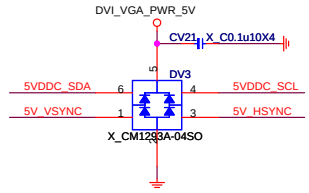












MICRO-STAR INT'L CO.,LTD		
MS-7970		
Size: Custom	Document Description: VGA Connector	Rev: 1.1
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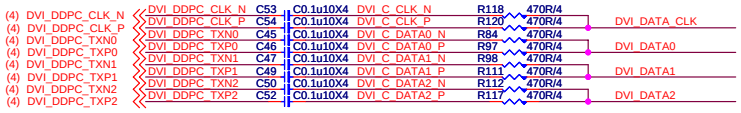
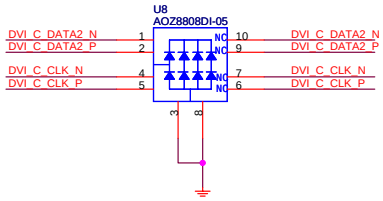
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

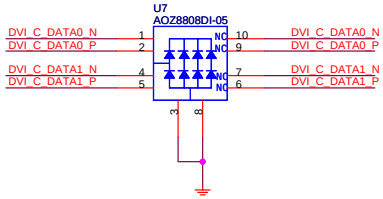
Check MSI PN
N58-39F0231-K06

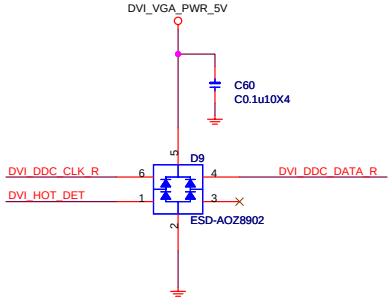


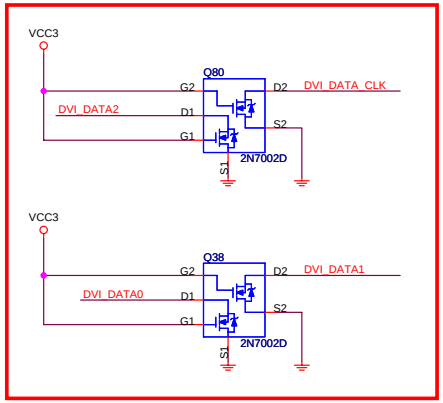
U26 AVL:D0G-05A050C-O05
D0G-06A050C-A68

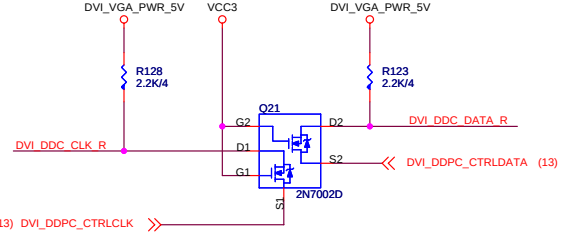


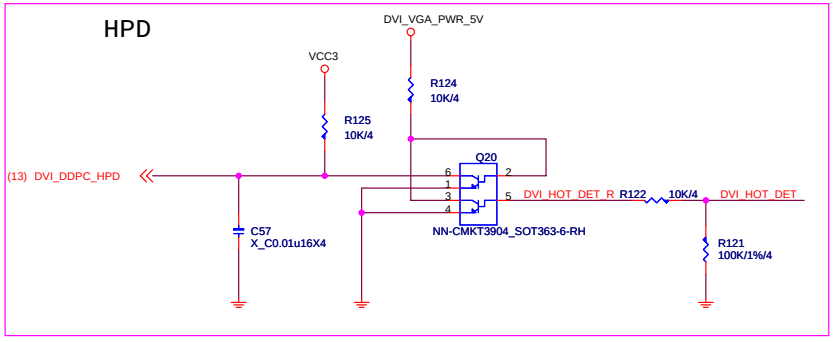
U27 AVL:D0G-05A050C-O05
D0G-06A050C-A68

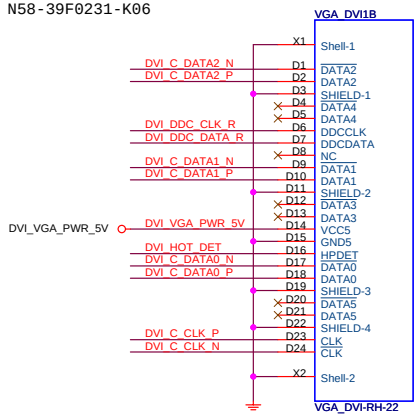


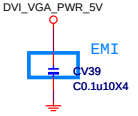


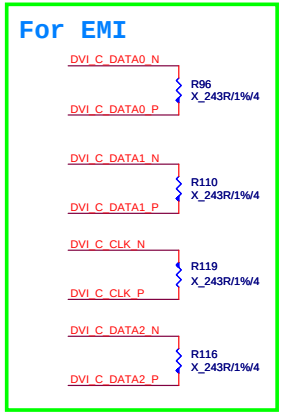


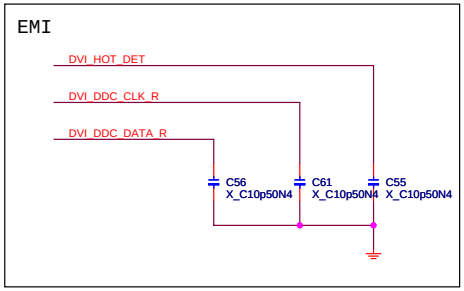












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HDMI level shifter

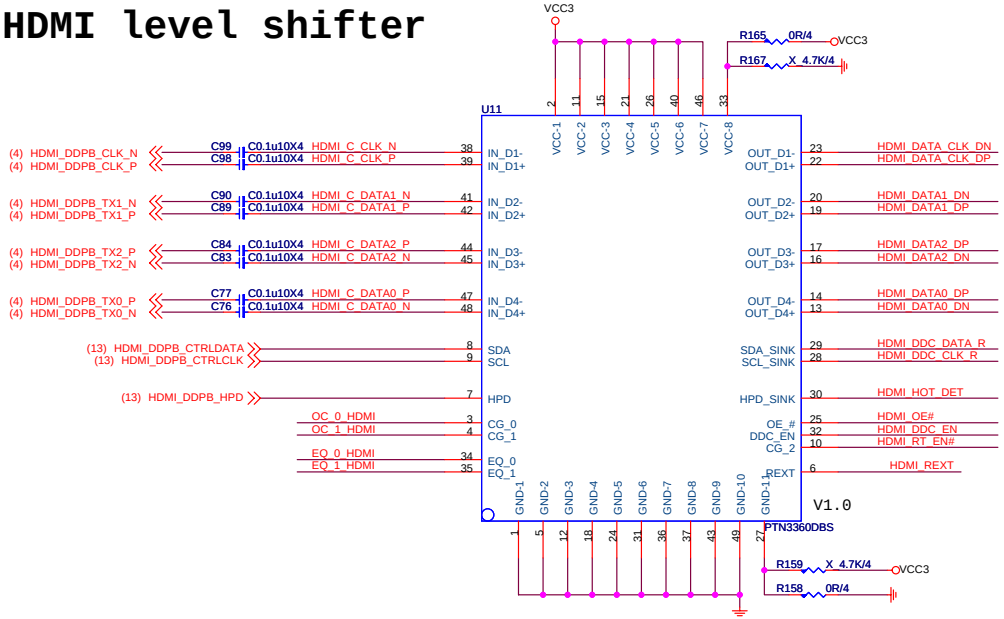
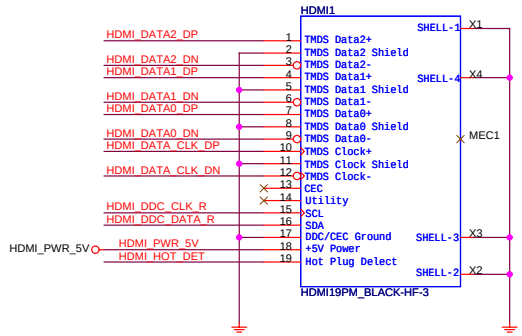
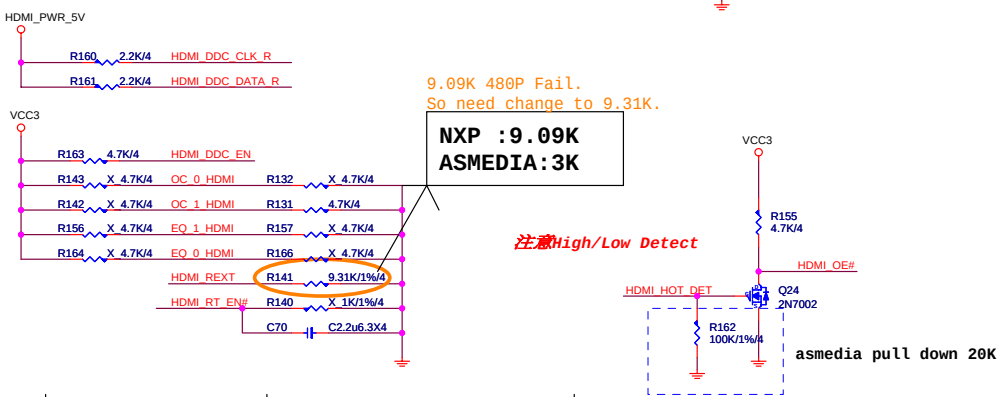
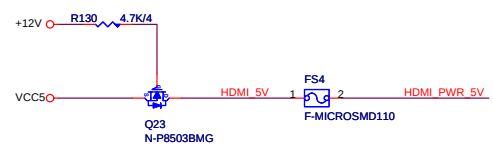


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA1#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	

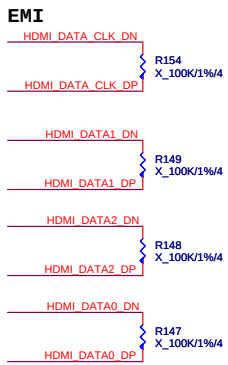




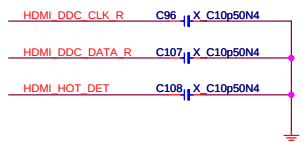


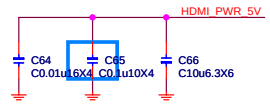
	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

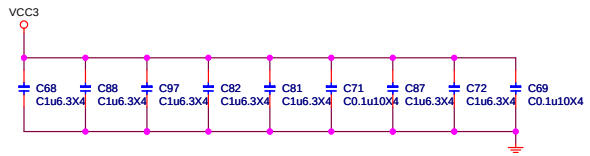
EMI



EMI cap.







[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

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Type B:
ALC892/~~887~~

2015.04.24 Modify from ALC1150 to ALC892

CA24 close to PIN25

CA25, CA32 close to PIN38

SMD CAP: Fail to test THD+N
EL/SOLID cap: Test THD+N will Pass

公版放 10uF

ALC892-CG-RH

CA26.CA28 close to Pin27

2.2k for better recording quality

for rear I/O 6port:
887VD/892:1k

for rear I/O 3port:
887VD/892:75R

0R for cost down

CA close to LA

DN010

Rear Line OUT De-POP circuit

(reserve de-pop circuit for Rear Line out & Front Headphone out)

All components are mounted by PM request

Digital

Analog

Varister --> cap for cost down

D0G-2950500-SI0
D0G-3010510-I05
Close to Jack

Close to Front panel
For HDA/AC97 front cable.

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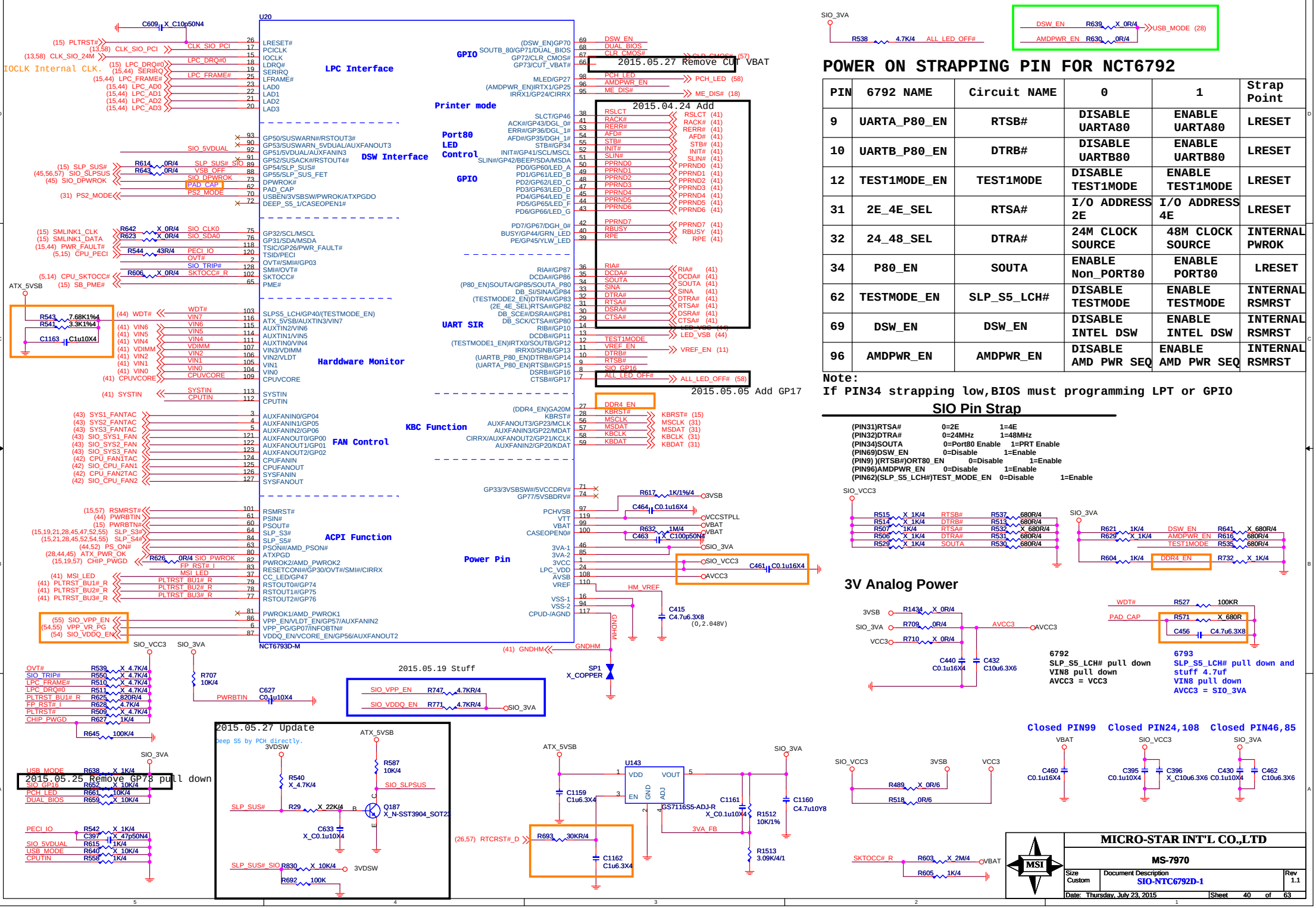

POWER ON STRAPPING PIN FOR NCT6792

PIN	6792 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	24_48_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
62	TESTMODE_EN	SLP_S5_LCH#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

SIO Pin Strap

(PIN31)RTSA# 0=2E 1=4E
(PIN32)DTRA# 0=24MHz 1=48MHz
(PIN34)SOUTA 0=Port80 Enable 1=PRT Enable
(PIN69)DSW_EN 0=Disable 1=Enable
(PIN9))(RTSB#)ORT80_EN 0=Disable 1=Enable
(PIN96)AMDPWR_EN 0=Disable 1=Enable
(PIN62)(SLP_S5_LCH#)TEST_MODE_EN 0=Disable 1=Enable

3V Analog Power

6792
SLP_S5_LCH# pull down
VIN8 pull down
AVCC3 = VCC3

6793
SLP_S5_LCH# pull down and stuff 4.7uf
VIN8 pull down
AVCC3 = SIO_3VA

Closed PIN99 Closed PIN24,108 Closed PIN46,85

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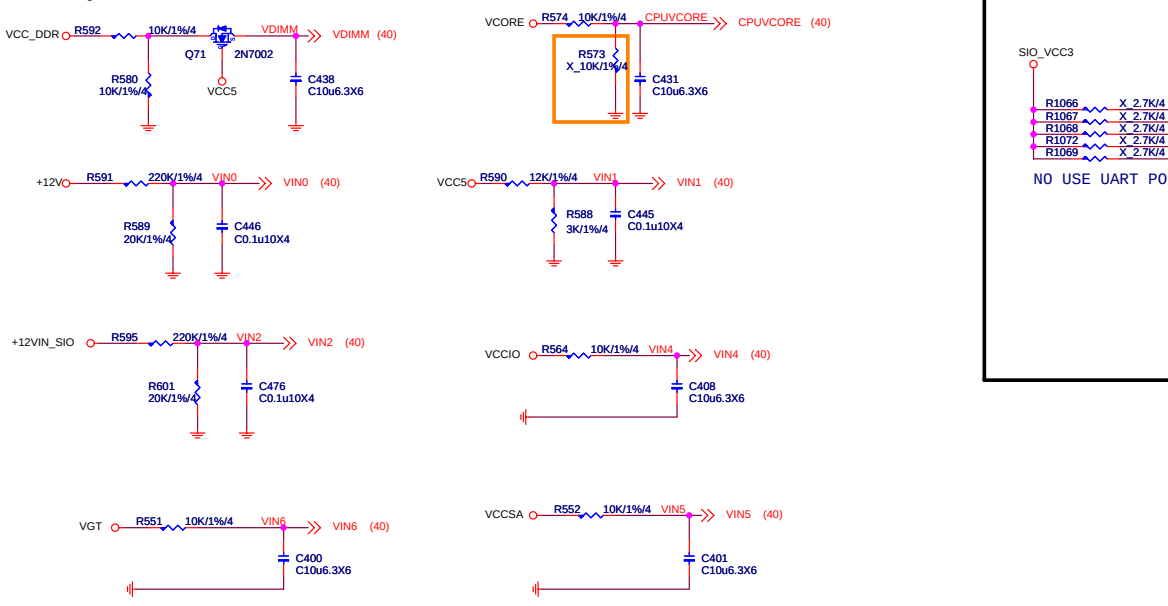
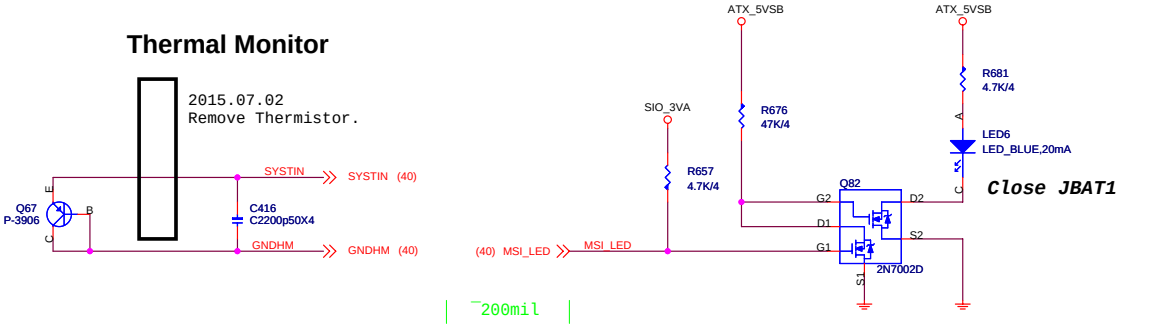
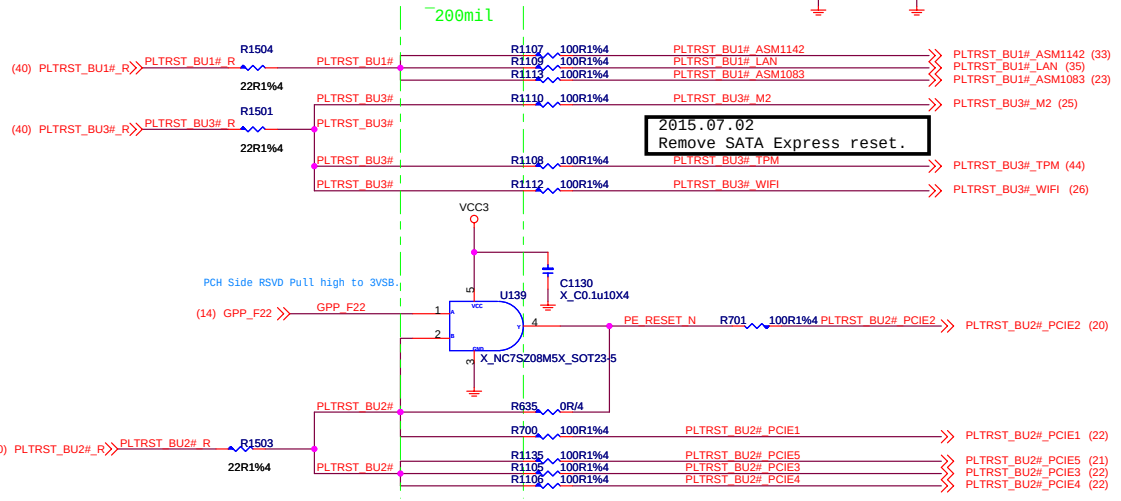
HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect



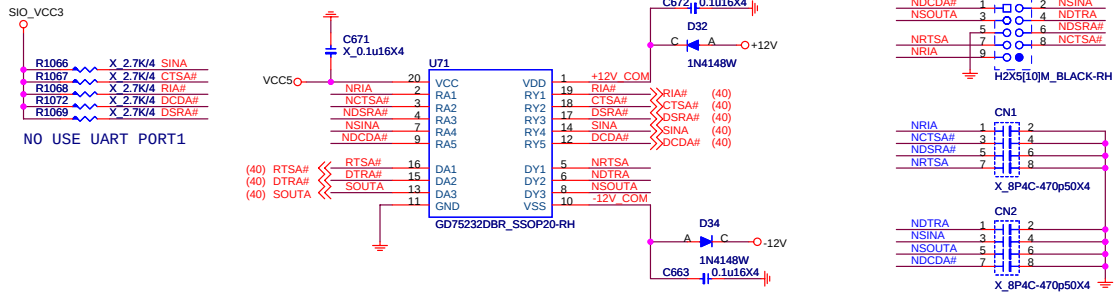
Thermal Monitor





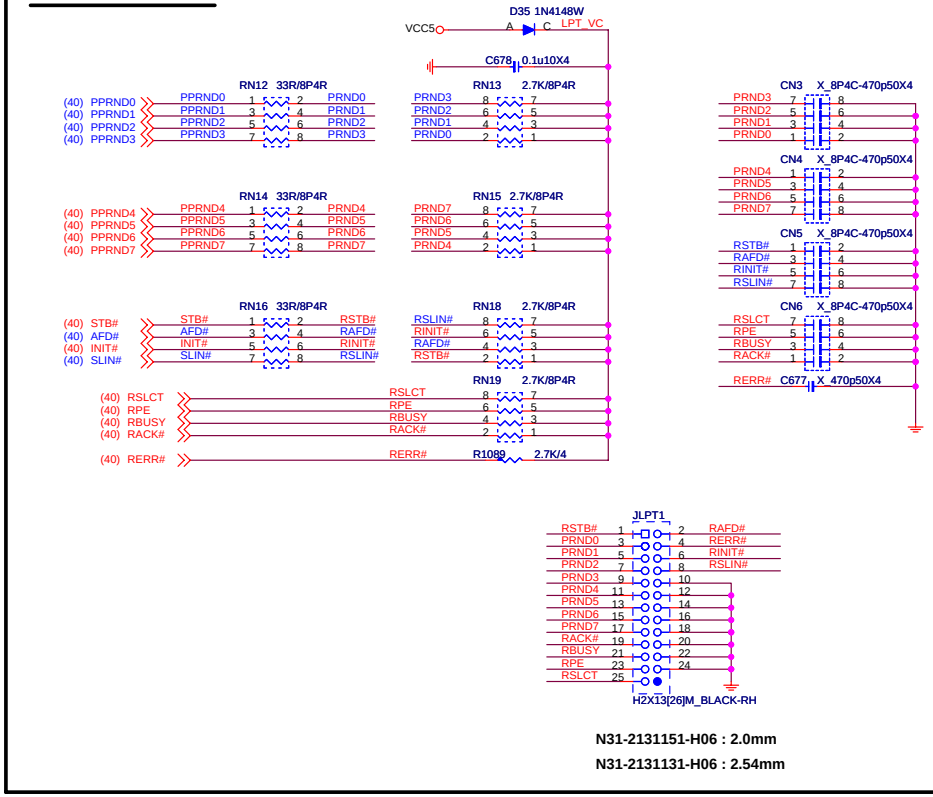
SERIAL PORT 1

2015.04.24 Add



PARALLAL PORT

2015.04.24 Add



N31-2131151-H06 : 2.0mm

N31-2131131-H06 : 2.54mm

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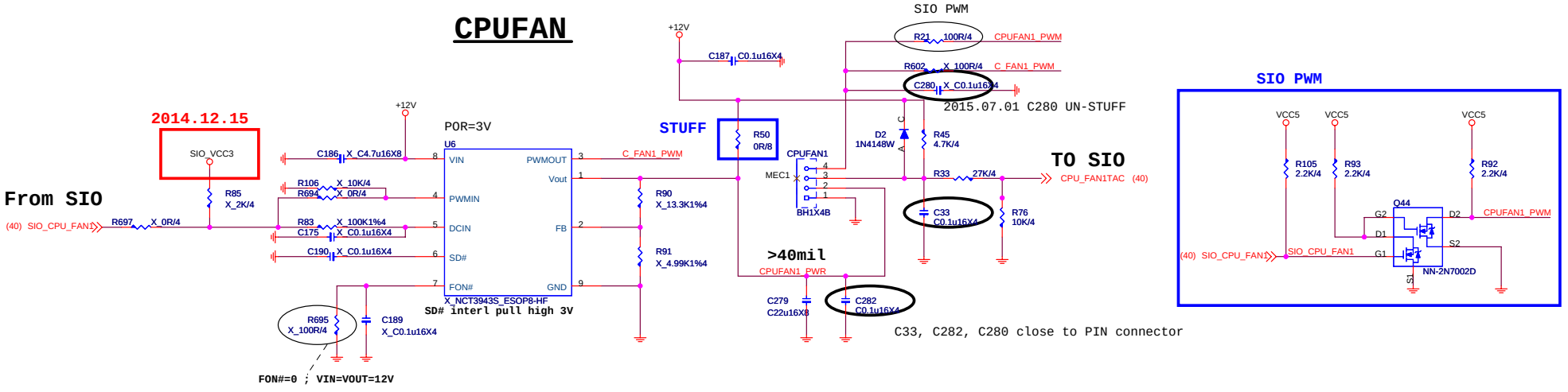
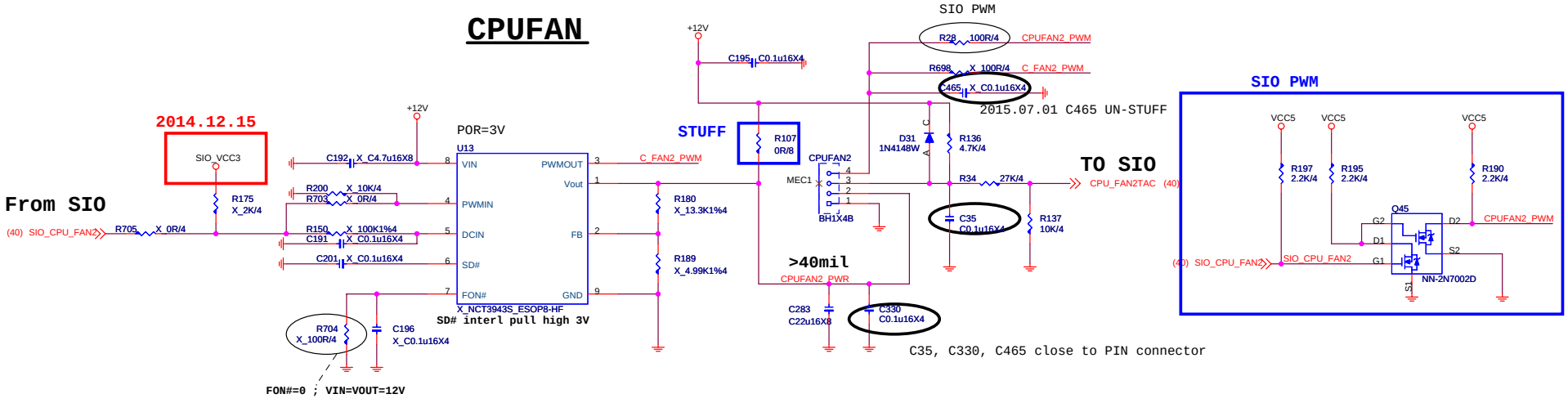
Type G : 4 PIN CPU FAN USE SIO PWM (Reserve NCT3943S & WITHOUT CUT POWER)



WITHOUT CUT POWER

BOM OPT	R602	R21	R105	R93	R92	Q44	R697	R85	R106	R694	R83	C175	R695	C186	U6	R90	R91	R50
SIO PWM	X	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	0

Type G : 4 PIN CPU FAN USE SIO PWM (Reserve NCT3943S & WITHOUT CUT POWER)



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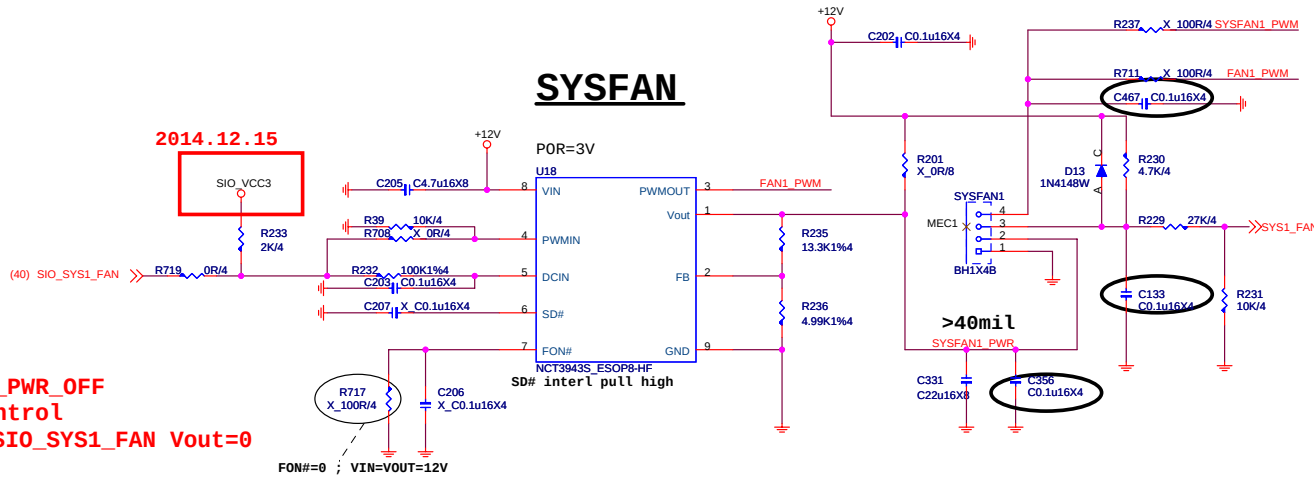
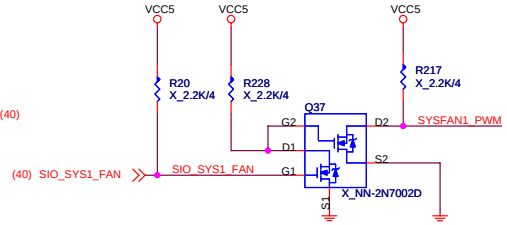
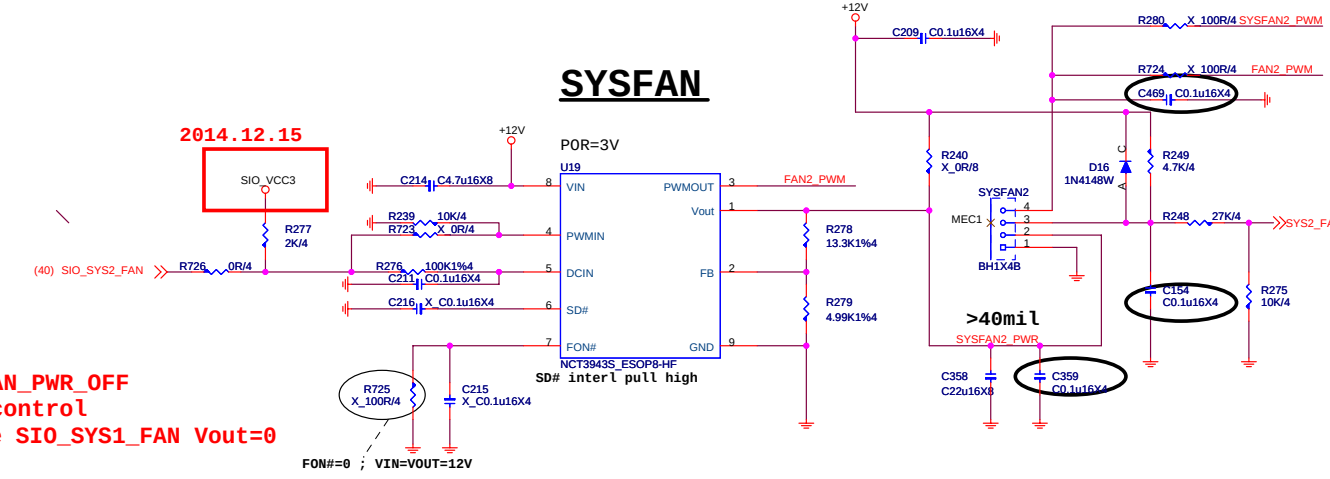
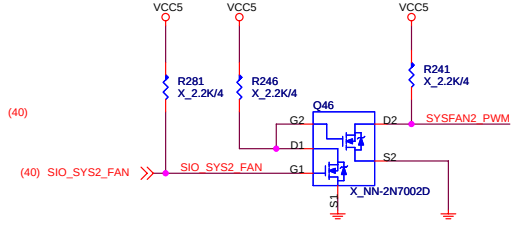
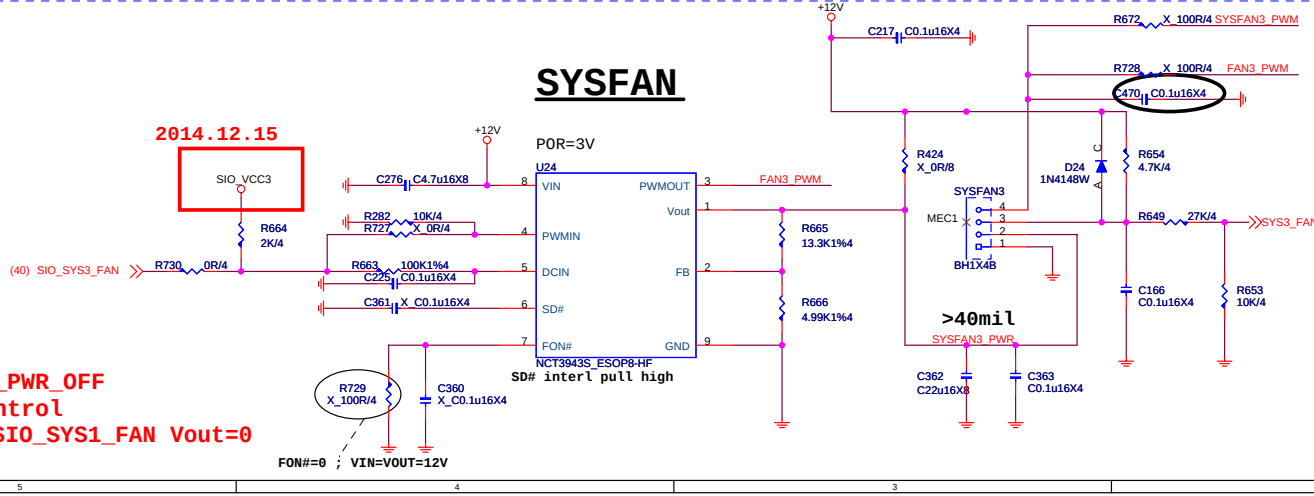
Type H : 4/3 PIN SYS FAN FROM NCT3943S(USE SIO CUT POWER)

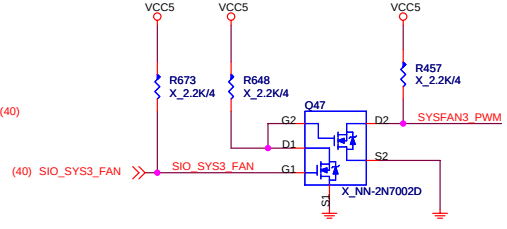












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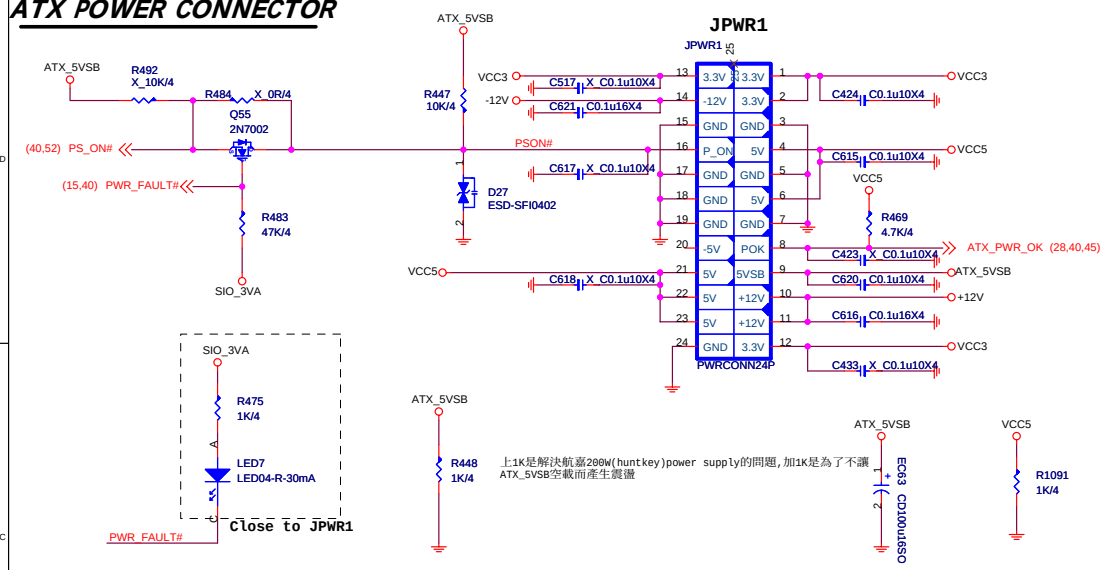
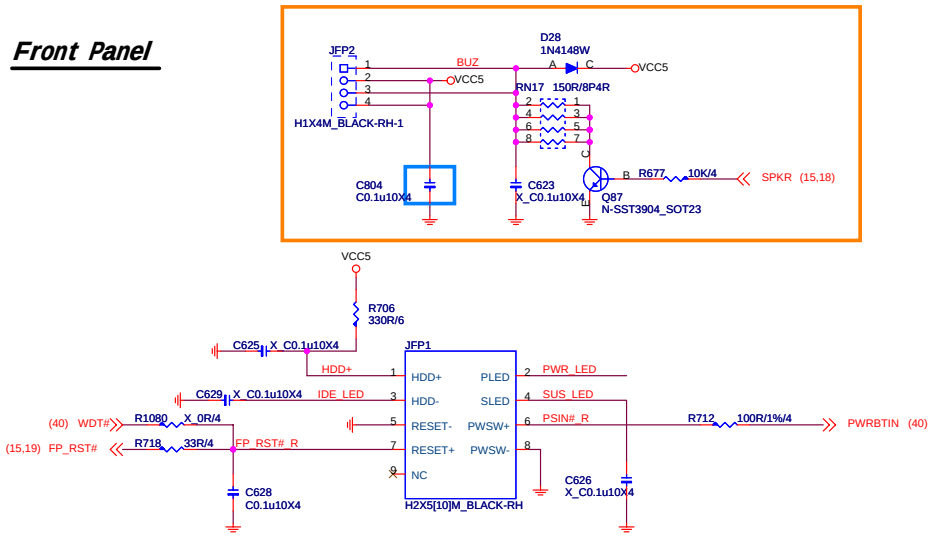
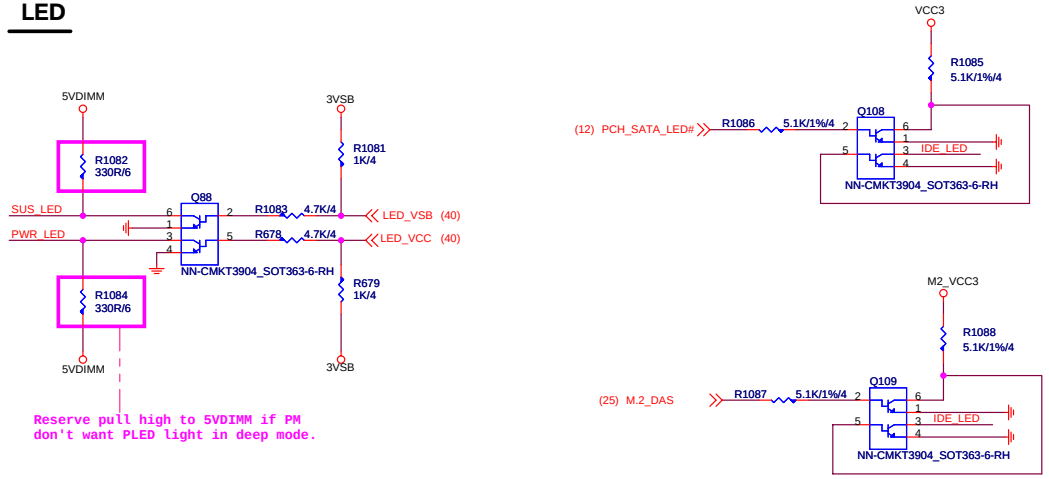
ATX POWER CONNECTOR



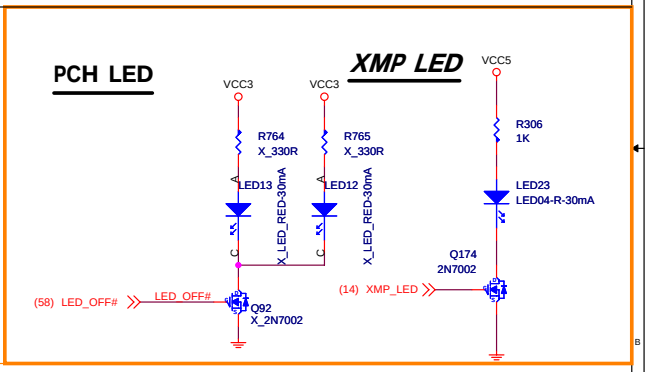
Front Panel



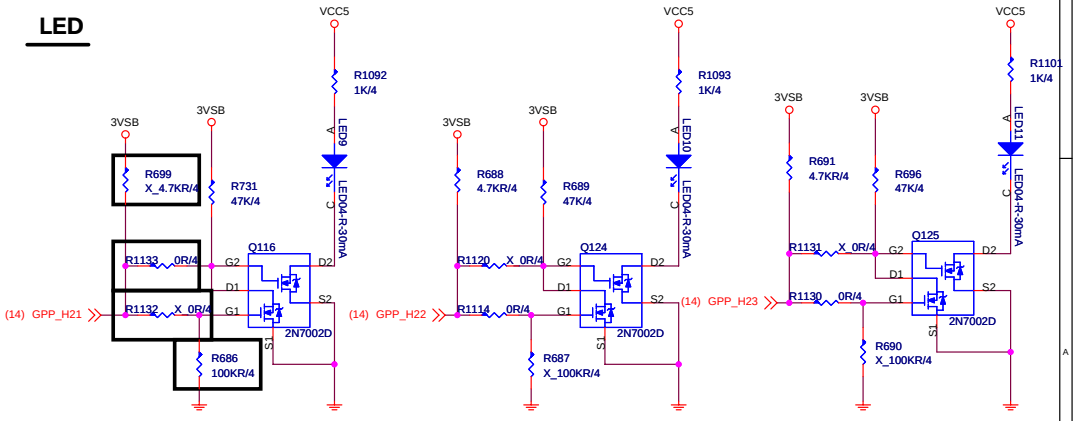
LED



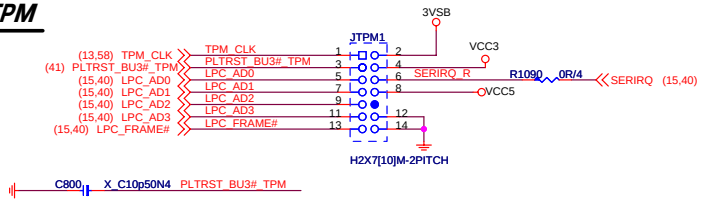
PCH LED / XMP LED



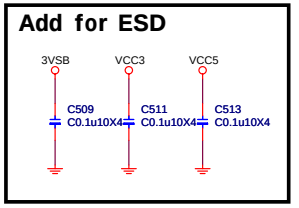
LED



TPM



Add for ESD



LED \ GPIO	GPP_H21	GPP_H22	GPP_H23
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

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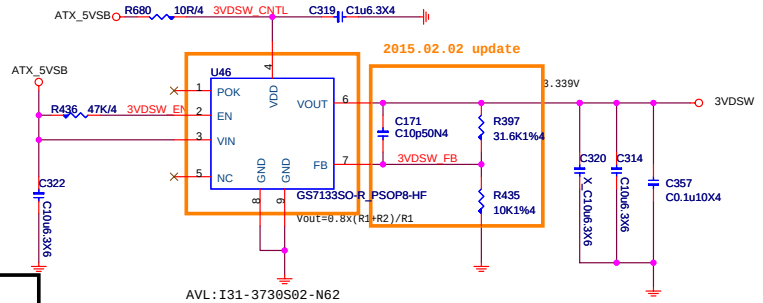
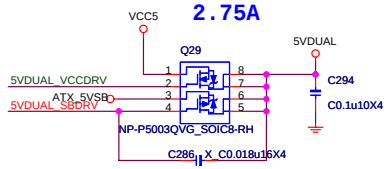
3VDSW



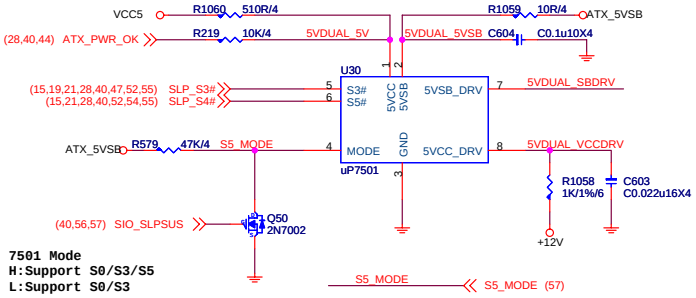
2015.05.25 Remove CUT VBAT

5VDUAL

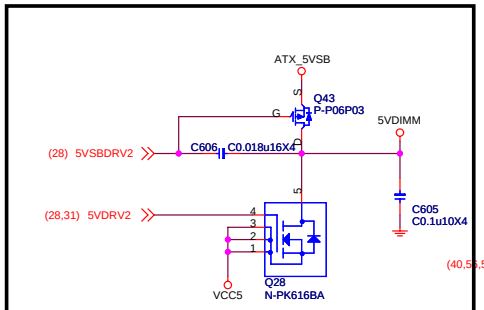
5VDUAL is power source of PCH_1VSB.



5VDIMM FOR 5VDUAL



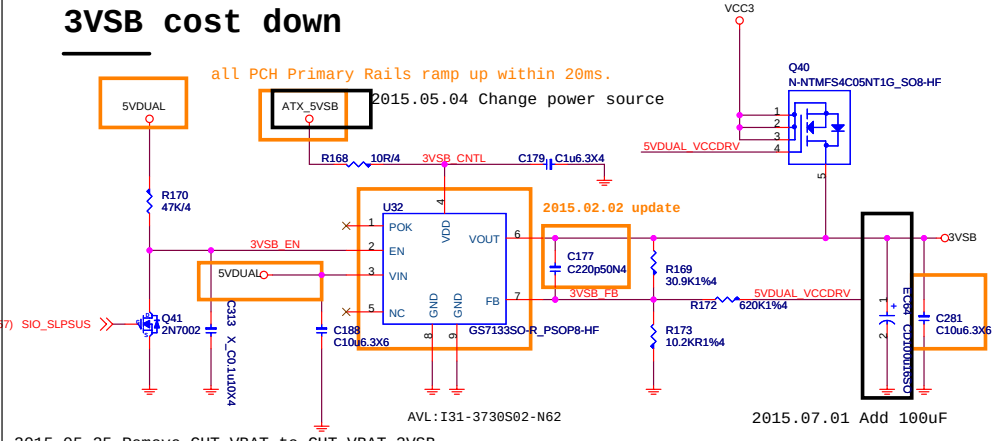
2015.05.19 Power source change with USB.



3VSB cost down

all PCH Primary Rails ramp up within 20ms.

2015.05.04 Change power source

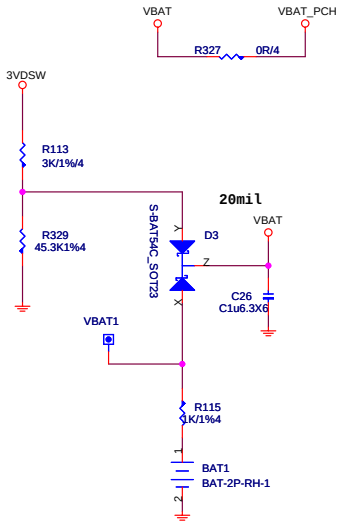


2015.05.25 Remove CUT VBAT to CUT_VBAT_3VSB

VFB=3.224V for S0->S3 3VSB voltage raise & ATX_5VSB drop.

CUT_VBAT

CRB



2015.05.25 Remove CUT VBAT to 3VDSW

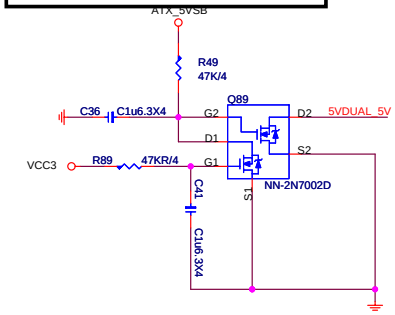
CUT 3VDSW

2015.05.25 Remove CUT VBAT to CUT_VBAT_3VSB

CUT 3VSB

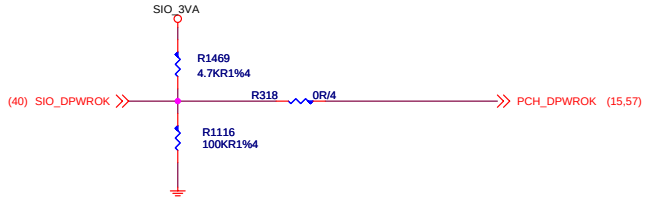
2015.05.25 Remove CUT VBAT to CUT_1VSB_EN

CUT PCH_1VSB



For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

patch power supply Vcc3 Vcc5 sequence



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Custom	ACPI UPI	1.1

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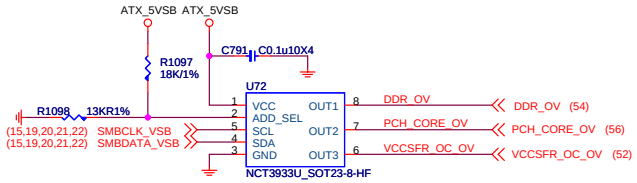
Remove Cut Power.

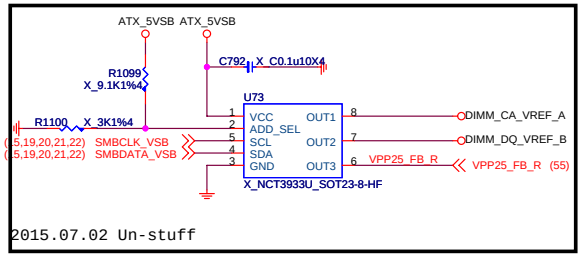
UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



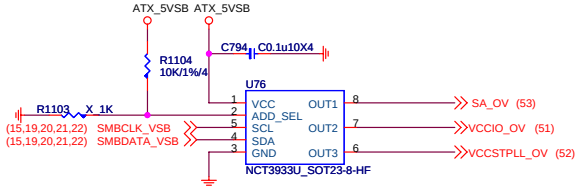
UPI VOLTAGE CONSOLE

0x28:RH=9.1K,RL=3K



UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN



ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

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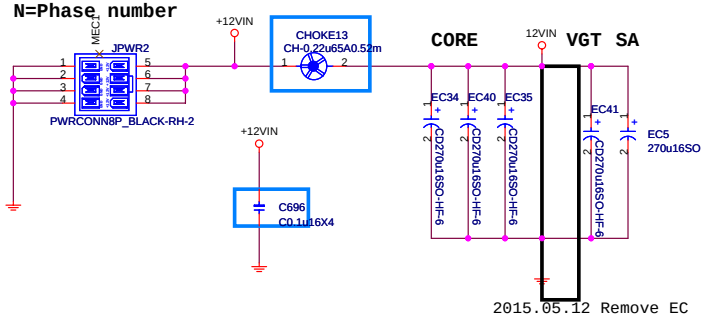
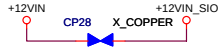
Irms = Iout * SQRT{D/N * (D)^2]}
D=Vout/Vin
N=Phase number



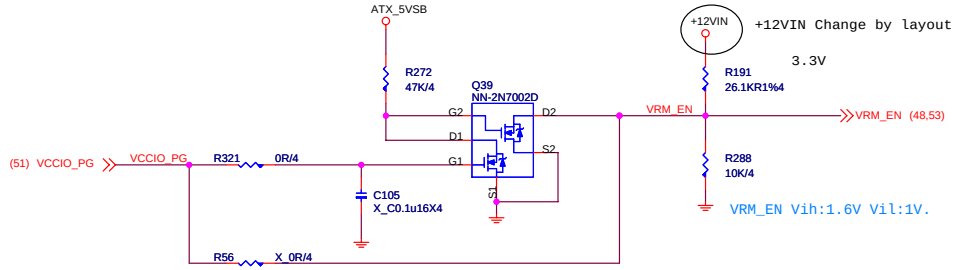
Iripple=23.097A
VCORE 12.47A
VGT 7.2977A
VCCSA 3.33A

2015.05.12 Remove EC

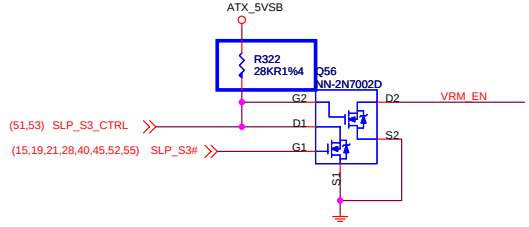


Close Power Connector

VRM_EN Control from VCCIO_PG

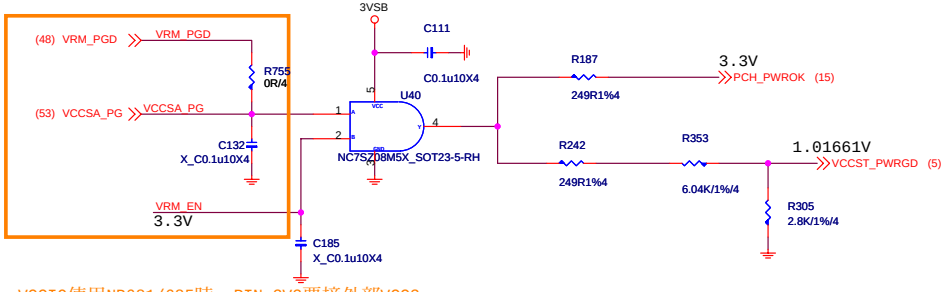


VRM_EN Vih:1.6V Vil:1V.

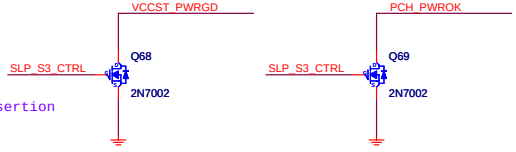


PCH_PWROK Control from VCCIO_PG&VCCSA
VCCST_PWRGD Control from VRM_PGD

VCCSA&Vcore use same PWM IC, pull up VCC3
VCCSA&Vcore use different PWM IC,pull up VCCSA
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.

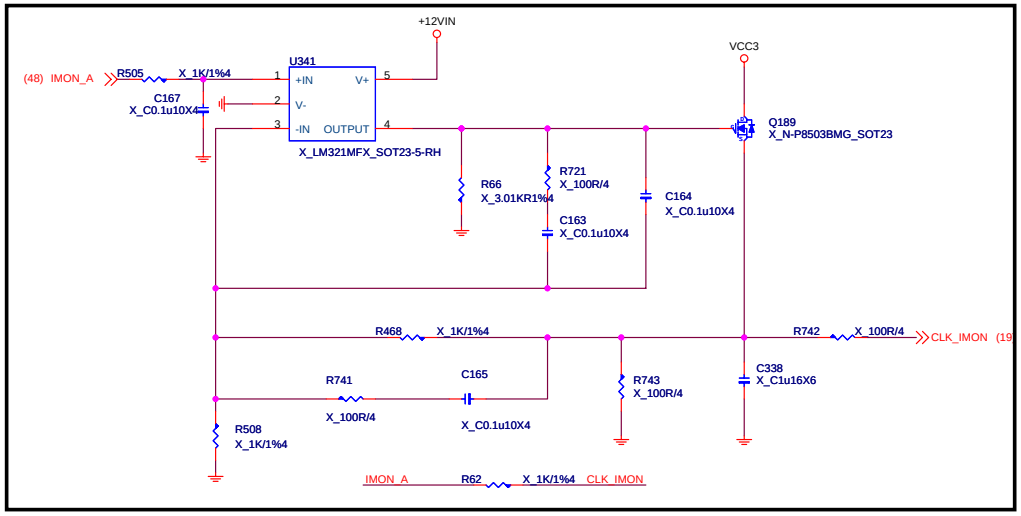


VCCIO使用NB681/685時, PIN 3V3要接外部VCC3,
VCCIO_PG上升時會彈一根到0.6V,
所以PCH_PWROK前端控制的VCCIO_PG改接VRM_EN.



For VCCST_PWRGD deassertion
max:1us

2015.05.22 Prevent use same IMON cause noise.



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Size: Custom	Document Description: +12VIN/VRM_EN&PGD
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The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).data & clk mismatch

Route the Alert signal between the Clock and the Data signals.
Constraint: 5/10/15

SVID Addr 00h : VCORE
SVID Addr 01h : VGT
SMBus Addr: XXh

TDP: 95W

VGT Total OCP: 90A

4+3 Application: VCORE+VGT

PWM1~PWM3	For VCORE 100A
PWM4~PWM5	For VGT 48A

close to VRM < 0.1"

close to VRM <0.1"

RC22 change 0603 to 0402

OCP 133A

OCP 90A

CLOSE Q2

CLOSE Q10

VCORE

VGT

RT6 CLOSE TO CHOKE5 or CHOKE6 PIN2

2015.05.14 Add for intersil to disable LL

2015.05.14 Add for intersil to disable LL

2015.07.07 Update

MICRO-STAR INT'L CO.,LTD

MS-7970

Size: Custom | Document Description: IMVP8 - PWM-ISL95858 VGT+VCORE | Rev: 1.1

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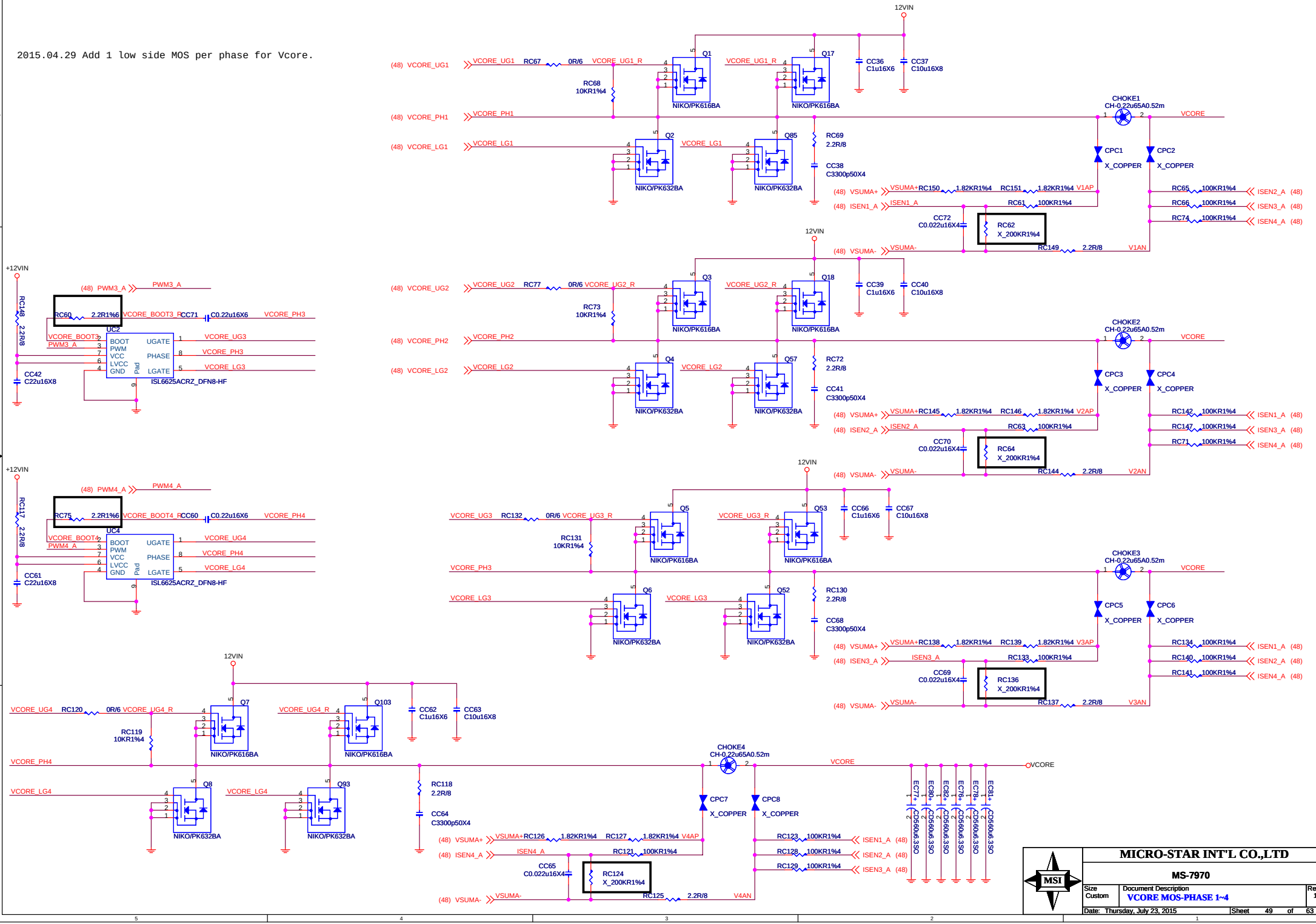
2015.04.29 Add 1 low side MOS per phase for Vcore.



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Size: Custom	Document Description: VCORE MOS-PHASE 1~4	Rev: 1.1
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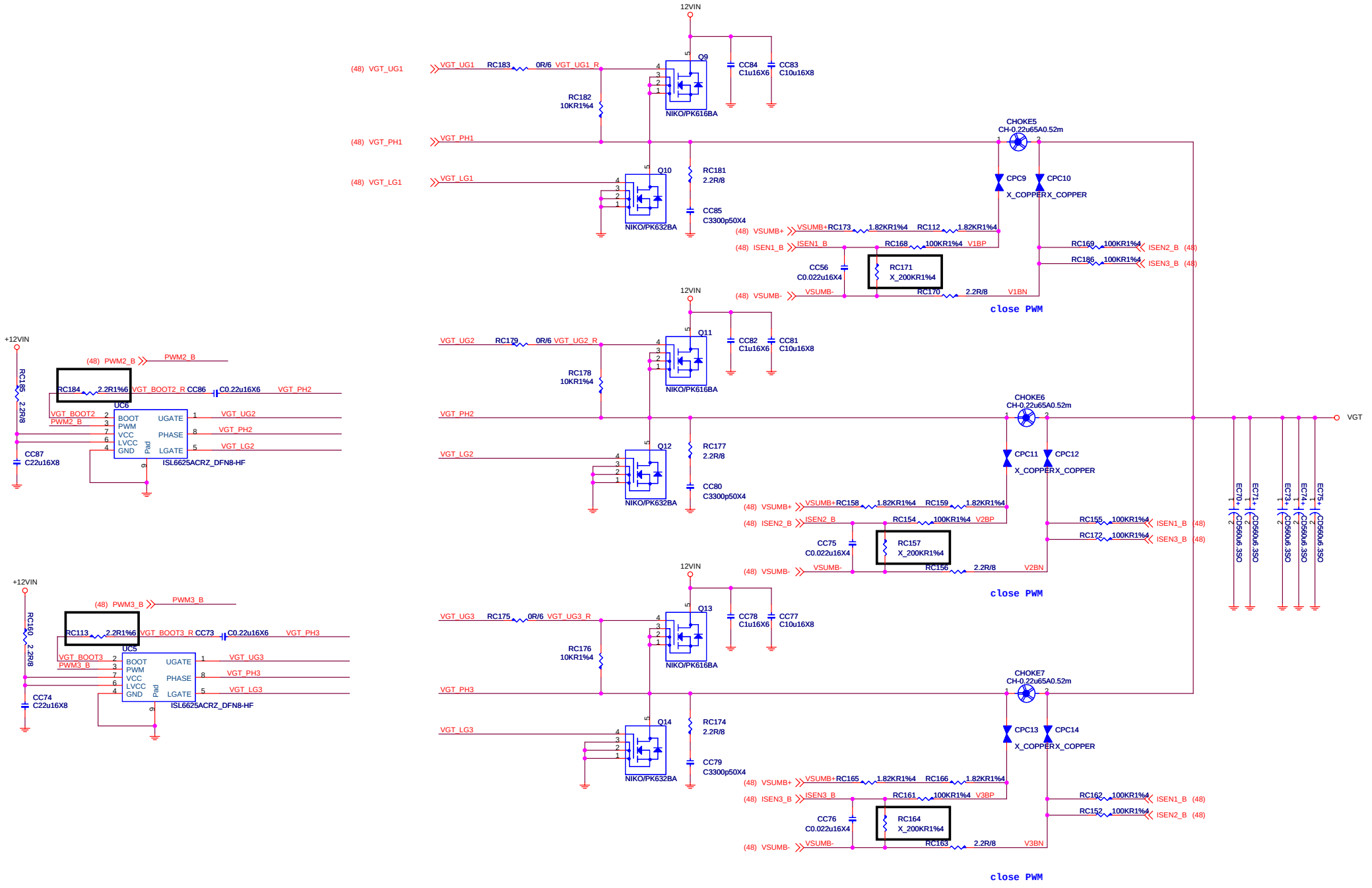
12VIN
(48) VGT_UG1
VGT_UG1
RC183
0R/6
VGT_UG1_R
Q9
CC84
C1u16X6
CC83
C10u16X8
RC182
10KR1%4
NIKO/PK616BA
(48) VGT_PH1
VGT_PH1
CHOKE5
CH-0.22u65A0.52m
(48) VGT_LG1
VGT_LG1
Q10
RC181
2.2R/8
CC85
C3300p50X4
NIKO/PK632BA
CPC9
CPC10
X_COPPER
X_COPPER
(48) VSUMB+
VSUMB+
RC173
1.82KR1%4
RC112
1.82KR1%4
(48) ISEN1_B
ISEN1_B
RC168
100KR1%4
V1BP
RC169
100KR1%4
ISEN2_B (48)
RC186
100KR1%4
ISEN3_B (48)
CC56
C0.022u16X4
RC171
X_200KR1%4
(48) VSUMB-
VSUMB-
RC170
2.2R/8
V1BN
close PWM
12VIN
VGT_UG2
RC179
0R/6
VGT_UG2_R
Q11
CC82
C1u16X6
CC81
C10u16X8
RC178
10KR1%4
NIKO/PK616BA
CHOKE6
CH-0.22u65A0.52m
VGT_PH2
VGT_LG2
Q12
RC177
2.2R/8
CC80
C3300p50X4
NIKO/PK632BA
CPC11
CPC12
X_COPPER
X_COPPER
(48) VSUMB+
VSUMB+
RC158
1.82KR1%4
RC159
1.82KR1%4
(48) ISEN2_B
ISEN2_B
RC154
100KR1%4
V2BP
RC155
100KR1%4
ISEN1_B (48)
RC172
100KR1%4
ISEN3_B (48)
CC75
C0.022u16X4
RC157
X_200KR1%4
(48) VSUMB-
VSUMB-
RC156
2.2R/8
V2BN
close PWM
VGT
EC70+
CD560u6.3SO
EC71+
CD560u6.3SO
EC73+
CD560u6.3SO
EC74+
CD560u6.3SO
EC75+
CD560u6.3SO
+12VIN
RC185
2.2R/8
(48) PWM2_B
PWM2_B
RC184
2.2R1%6
VGT_BOOT2_R
CC86
C0.22u16X6
VGT_PH2
UC6
VGT_BOOT2
PWM2_B
BOOT
PWM
VCC
LVCC
GND
Pad
UGATE
PHASE
LGATE
VGT_UG2
VGT_PH2
VGT_LG2
CC87
C22u16X8
ISL6625ACRZ_DFN8-HF
+12VIN
RC160
2.2R/8
(48) PWM3_B
PWM3_B
RC113
2.2R1%6
VGT_BOOT3_R
CC73
C0.22u16X6
VGT_PH3
UC5
VGT_BOOT3
PWM3_B
BOOT
PWM
VCC
LVCC
GND
Pad
UGATE
PHASE
LGATE
VGT_UG3
VGT_PH3
VGT_LG3
CC74
C22u16X8
ISL6625ACRZ_DFN8-HF
12VIN
VGT_UG3
RC175
0R/6
VGT_UG3_R
Q13
CC78
C1u16X6
CC77
C10u16X8
RC176
10KR1%4
NIKO/PK616BA
CHOKE7
CH-0.22u65A0.52m
VGT_PH3
VGT_LG3
Q14
RC174
2.2R/8
CC79
C3300p50X4
NIKO/PK632BA
CPC13
CPC14
X_COPPER
X_COPPER
(48) VSUMB+
VSUMB+
RC165
1.82KR1%4
RC166
1.82KR1%4
(48) ISEN3_B
ISEN3_B
RC161
100KR1%4
V3BP
RC162
100KR1%4
ISEN1_B (48)
RC152
100KR1%4
ISEN2_B (48)
CC76
C0.022u16X4
RC164
X_200KR1%4
(48) VSUMB-
VSUMB-
RC163
2.2R/8
V3BN
close PWM
MSI
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Size
Custom
Document Description
VGT MOS-PHASE 1~3
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VCCIO

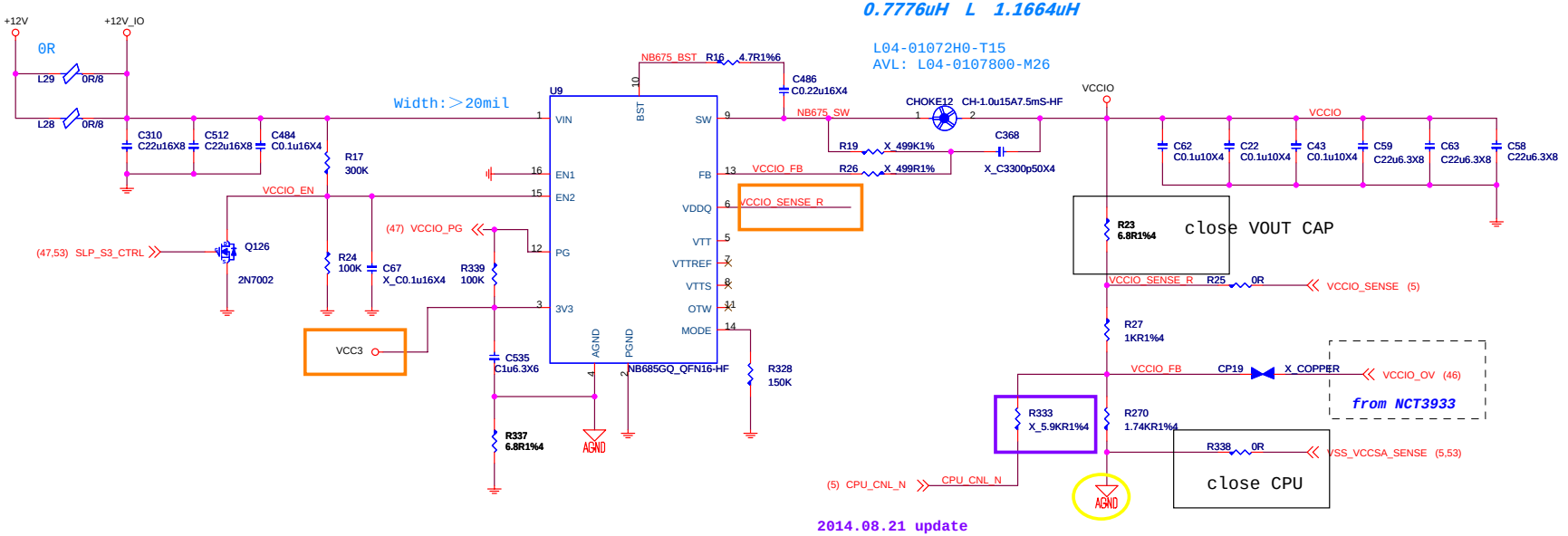
0.95V; 5.5A

(H110 VCCIO=VCCSA)

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

0.7776uH L 1.1664uH

L04-01072H0-T15
AVL: L04-0107800-M26

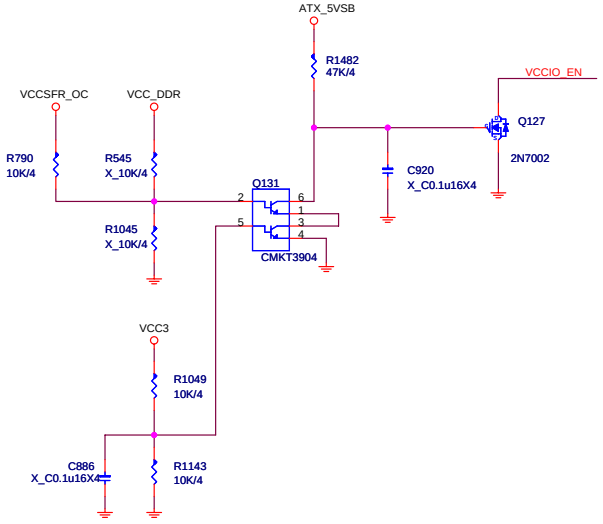


2014.08.21 update
RSVD for CRB

CPU_CNL_N come from CPU PROC_SELECT#

SLP_S3# assertion to VCCIO VR disabled <1uS.

SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off. <500ms



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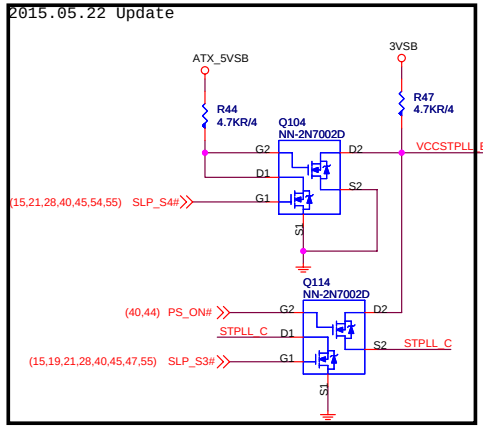
VCCSTPLL

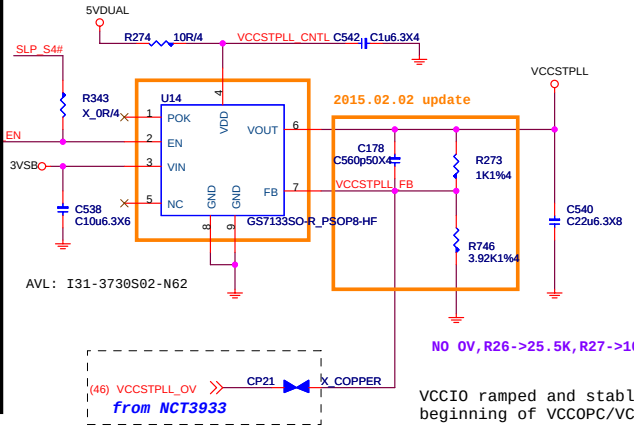
1.0V; 250mA

For Cost down VCCST&VCCPLL merge

for Gaming3/5, Classic, ECO and H110

2015.05.22 Update





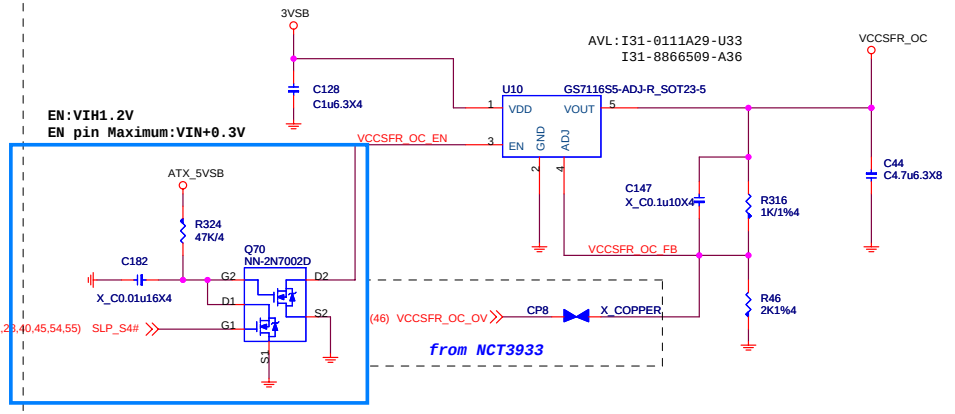
VCCIO ramped and stable before beginning of VCCOPC/VCCEOPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD

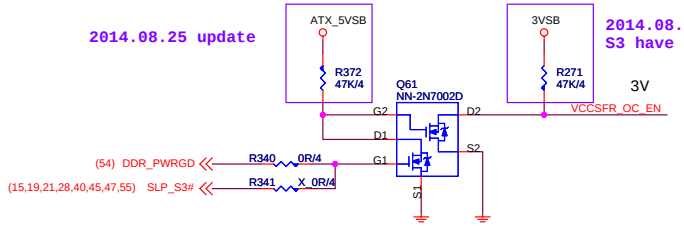
VCCPLL_OC

1.2V; 110mA

2014.08.21 update



2014.08.25 update



2014.08.25 update
S3 have power

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SA Power:1.05V,12.3A

OCP =12.3A*1.4=17.22A
Rocs(R15)=OCP*Rdson(Low side)3.4mohm]/10uA
=17.22*(3.4)mohm/10uA
=5.854Kohm

Rocs:5.76K,OCP:
D03-4C05N03-O05 : 16.94A
D03-632BA0C-N03 : 17.45A
use UBIQ MOS need Check

Rdson(low)10V
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

RT8125C R413->10R
up1540 R413->2.2R

+12VIN — R413 10R/8 — C34 C1u16X6

2015.07.14 update to 0603

VCC3 — R289 10K/4

EN:VIH2.4V
EN pin Maximum:6.5V

U4 RT8125CGQW_WDFN10-HF

7	EN	BOOT	1 SA_BOOT1
8	PGOOD	PHASE	3 SA_PH1
10	REFOUT	UGATE	2 SA_UG1
	LGATE/OCSET		4 SA_LG1
9	REFIN	FB	6 SA_FB
11	GND	VCC	5

VCCSA_EN
(47) VCCSA_PG — VCCSA_PG
SA_REFOUT
SA_REFIN

R440 0R/6 — C2 C0.1u16X4

VCCSA — R361 10R1%4 — R414 0R/4 — VCCSA_SENSE (5)

R416 1K/1%4 — C4 X_C0.1u10X4

FB:0.8V

RT8125C C5->1000pf;R415->768R
up1540 C5&R415 NC

C5 C1000p16X4 — R415 768R1%4

RT8125C C39->1000pF.
For up1540 :C39->5.36K, OCP 15.76A.
5K is min

C39 C1000p16X4

RT8125C R194->stuff;R179->NC
up1540 R194->NC;R179->stuff

R194 0R/4 — R179 X_0R/4 — (46) SA_OV

RT8125C R426->3.24K
up1540 R426->3.16K

R426 3.24KR1%4 — R428 0R/4 — VSS_VCCSA_SENSE (5,51)

R360 10R1%4

VCCSA_EN — R225 X_36KR/4 — C100 X_C33p50N4 — C85 X_C680p16X4

RT8125C C100&R225&C85 ->NC
up1540 C100->NC;R225->36K;C85->10nf

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 11.1* 0.8 * 0.282566
= 2.509A

2015.05.11 Update. To prevent VRM_EN level too low to make PWRGD not output.

ATX_5VSB — R356 47K/4 — Q110 NN-2N7002D — C193 C0.1u10X4 — (47,48) VRM_EN
+12VIN — R534 26.1KR1%4 — R526 10K/4 — VCCSA_EN 3.3V

EN:VIH2.4V
EN pin Maximum:6.5V

12VIN — C37 C1u16X6 — C40 C10u16X8

SA_UG1 — R418 0R/6 — SA_UG1_R — Q25 N-PK616BA_PDFN8-HF

R331 X_10K/4

Footprint:CHK_D2_10_5X7_2_H9_6

1.05V,11.1A

SA_PH1 — CHOKE14 CH-1.1u25A1.07m — VCCSA

R357 X_2.2R/8 — C101 X_C3300p50X4 — **snubber**

C8 C1u6.3X4 — C42 C22u6.3X8 — EC4 560u6.3SO — EC3 560u6.3SO

VCCSA_EN — Q74 2N7002 — (47,51) SLP_S3_CTRL

SA_LG1 — Q19 N-PK632BA_PDFN8-HF

R417 5.76KR1%4

OCPSET:min 5Kohm

OCP
=(R417*10uA)/DCR
=(5.76k*10uA)/3.3m
=17.4A

RT8125C R417->5.76K
up1540 R417->NC

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.5914uH (K = 30%)

SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.

SLP_S3# assertion to VR disabled
max:1us

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DDR4_1.2V 2.5A+9.5A+1.2A=13.2A

2.5A FOR CPU

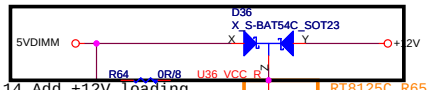
9.5A FOR 4DIMM

1.2A FOR DDR VTT

*OCP =13.2A*1.5=19.8A*
*Rocs(R95)=OCP*Rdson[(Low side)/2]/10uA*
=19.8A(4.6/2)mohm/10uA*
=4.95Kohm＜5K

Rocpset:5.1K
OCP=Rocset*Rdson[(Low side)/2]/10uA
=5.1K*(5/2)mohm/10uA
=22.173A
use UBIQ MOS need Check

Pull up change by layout



2015.07.14 Add +12V loading

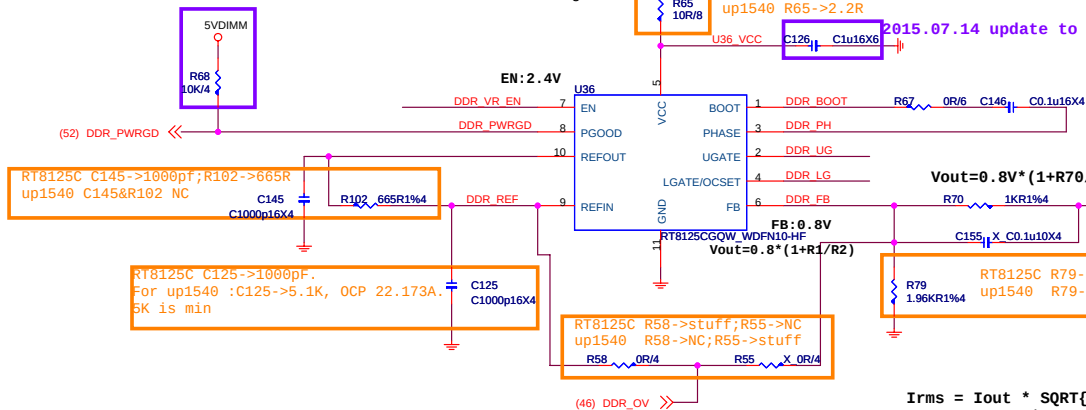
uP1504 & RT8125
VCC Input Range : 4.5V to 13.2V

R65 10R/8

RT8125C R65->10R
up1540 R65->2.2R

2015.07.14 update to 0603

U36_VCC C126 C1u16X6



RT8125C C145->1000pf;R102->665R
up1540 C145&R102 NC

C145 C1000p16X4
R102 665R1%4
DDR_REF

Vout=0.8V*(1+R70/R79)=0.8V*(1+1k/2.15k)=1.172V

R70 1KR1%4
VCC_DDR
C155 X_C0.1u10X4

R79 1.96KR1%4

RT8125C R79->1.96K
up1540 R79->2K

RT8125C C125->1000pF.
For up1540 :C125->5.1K, OCP 22.173A.
5K is min

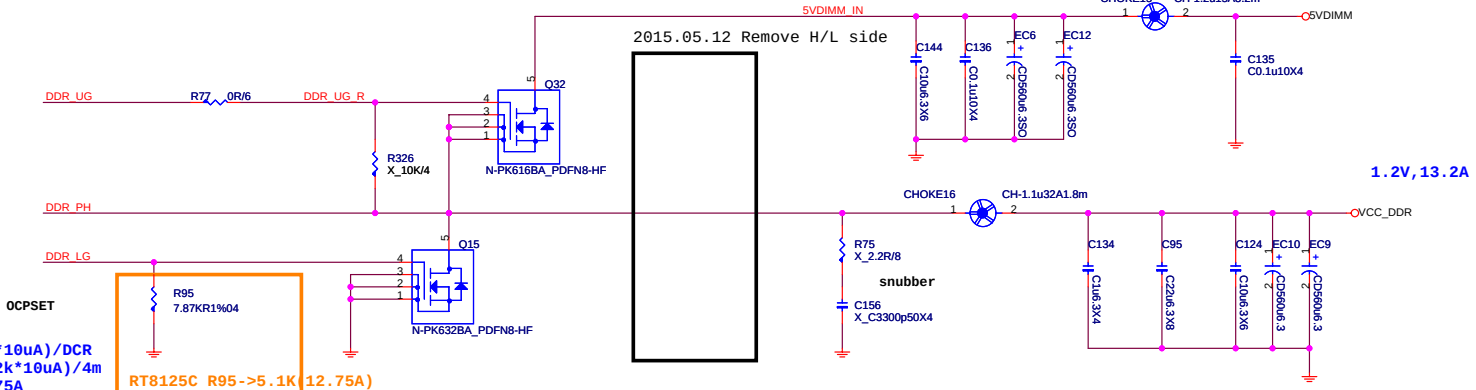
C125 C1000p16X4

RT8125C R58->stuff;R55->NC
up1540 R58->NC;R55->stuff

R58 0R/4
R55 X_0R/4
(46) DDR_OV

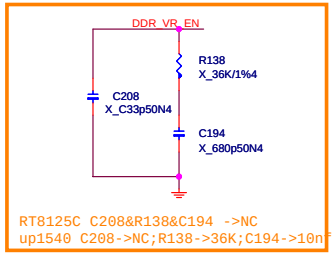
Irms = Iout * SQRT{(Vout/Vin) * [1 - (Vout/Vin)]}
= 13.2* 0.427
= 5.636A

(OS-CON CAP)



2015.05.12 Remove H/L side

1.2V,13.2A



RT8125C C208&R138&C194 ->NC
up1540 C208->NC;R138->36K;C194->10nF

OCPSET

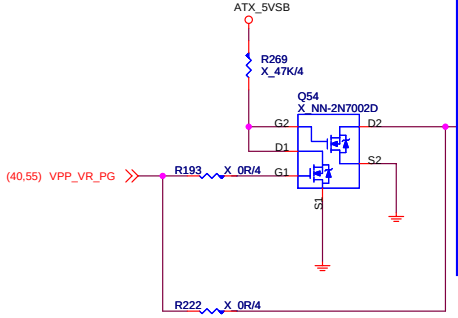
OCP
=(R95*10uA)/DCR
=(7.92k*10uA)/4m
=19.675A

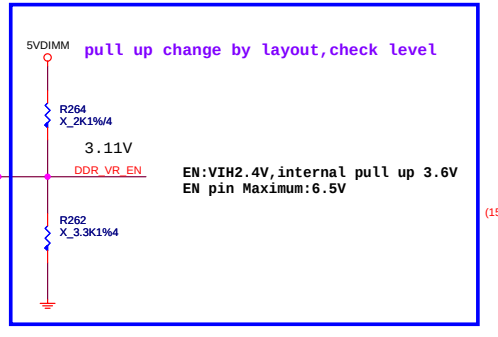
R95 7.87KR1%04

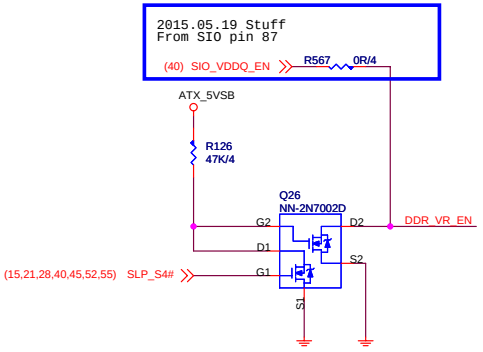
RT8125C R95->5.1K(12.75A)
up1540 R95->NC

Datasheet公式計算
Lmin = ((Vin - 1.2V)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.7677uH (K = 30%)

若帶入CAP ESR計算,0.2432uH＜L＜1.2897uH







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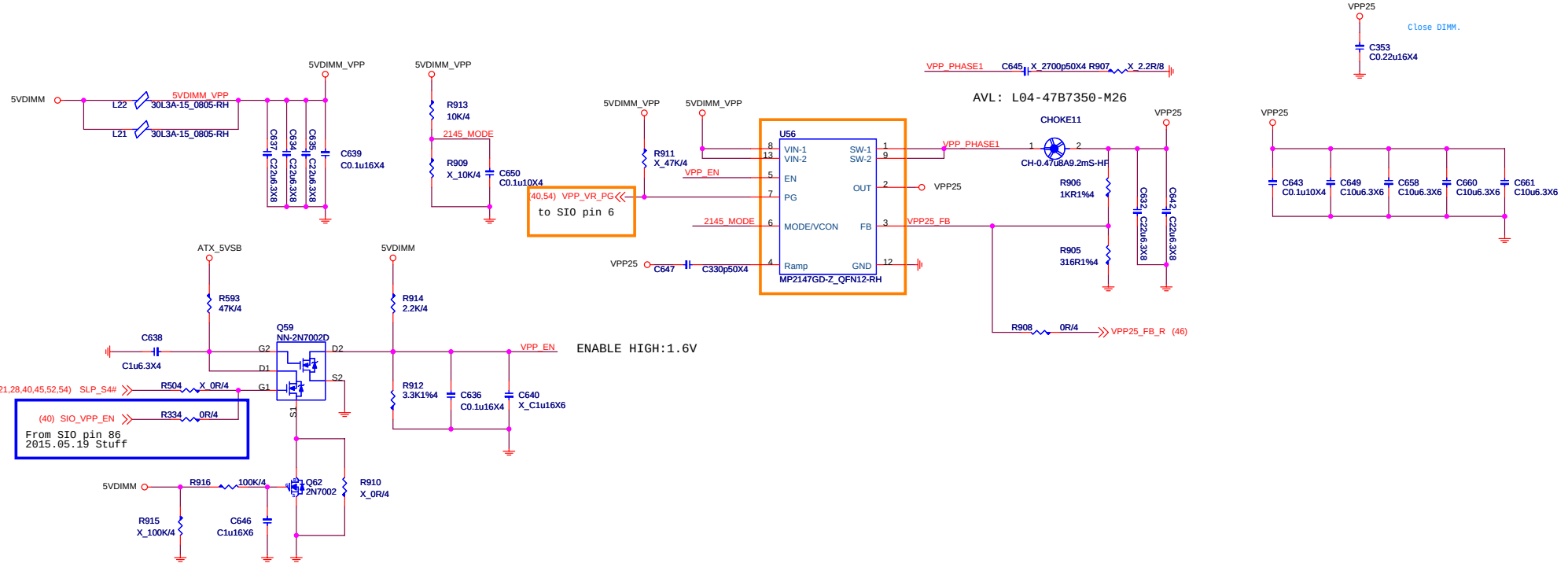
4DIMM :2.24A FOR DDR VPP2.5V

VPP25 Power

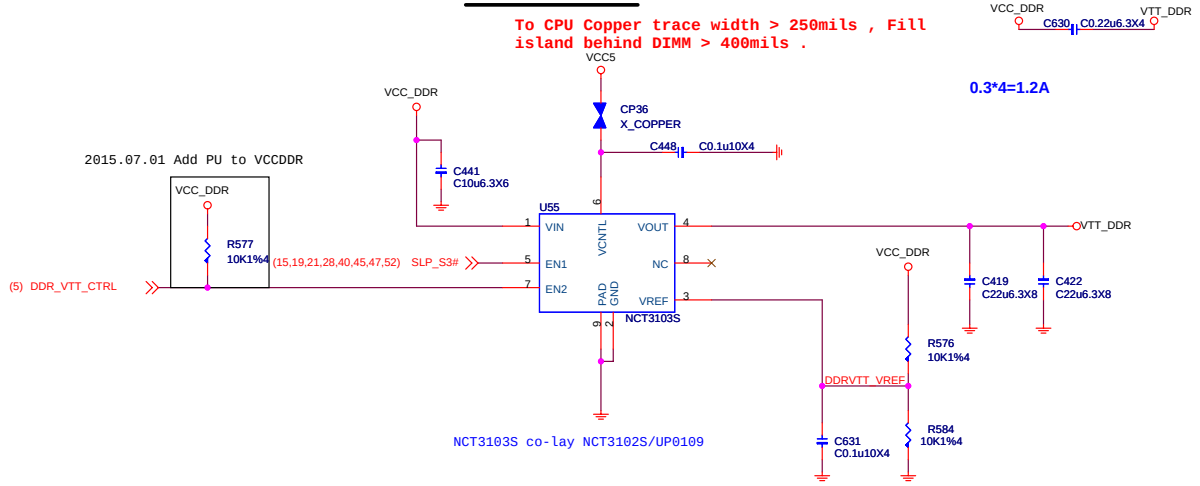
2.5V; 2.24A



To make sure VPP EN after 5VDIMM stable

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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PCH_1VSB

1.0V; 11A

OCP = 11.787A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 1.5 * 7.858 * 5mohm / 10uA
= 5.8935K

Rocs:9.9K,OCP:
D03-4C05N03-O05 : 11.8A
D03-632BA0C-N03 : 12.82A
use UBIQ MOS need Check

Rdson(low)4.5V
D03-4C05N03-O05 : 5 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm

2015.07.14 Add +12V loading

D37 X_S-BAT54C_SOT23 — 5VDUAL — +12V — R69 0R/8 U28_VCC_R

uP1504 & RT8125
VCC Input Range : 4.5V to 13.2V

R254 2.2R/8 — RT8125C R65->10R up1540 R65->2.2R

U28_VCC

C152 C1u16X6 — 2015.07.14:Change 1u/0603

2015.05.25 Remove CUT VBAT to CUT_1VSB_EN

PCH_1VSB_EN

2014.08.21 update

U28 RT8125CGQW_WDFN10-HF
EN, PGOOD, REFOUT, REFIN, VCC, GND, BOOT, PHASE, UGATE, LGATE/OCSET, FB

PCH_BOOT — R178 0R/6 — PCH_R_BOOT — C226 C0.1u16X4
PCH_PHASE
PCH_UGATE — R198 0R/6 — PCH_R_UGATE
PCH_LGATE
PCH_REFOUT
PCH_REFIN
PCH_CORE_FB_R

RT8125C C236->1000pf;R204->665R
up1540 C236&R204 NC
C236 X_C1000p16X4 — R204 X_1K1%4

RT8125C C180->1000pF.
For up1540 :C180->5.9K, OCP 12.82A.
Update 2015.05.06
C180 5.9KR1%0402

0CP
R177 X_5.9KR1%0402

RT8125C R177->5.9K
up1540 R177->NC

RT8125C R287->stuff;R188->NC
up1540 R287->NC;R188->stuff
R287 X_0R/4 — R188 0R/4

C233 X_C0.01u16X4 — PCH_TYPE3 — R255 X_0R/4

(46) PCH_CORE_OV

R253 1K1%4

R258 3.92K1%4

Vout = Vref * (1 + R821/R822)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V

R256 X_10K/4

Q22 N-NTMFS4C08NT1G
Q27 N-NTMFS4C05NT1G

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 10.664 * 0.4
= 4.2656A < 5000mA

L04-47B7730-T15 for OC, Gaming 10, 9, 7, 5
L04-12A7321-L65 for Gaming 3, SLI, ECO
L04-12A7721-T15 for cost down

5VDUAL_PCH_IN — CHOKE8 CH-1.2u15A3.2m-RH — 5VDUAL
too Big
C230 C0.1u16X4 — C235 C10u16X8 — EC19 CD560u6.3SO-HF-1 — C223 X_C0.1u16X4

MAX:10.664A

L04-01072H0-T15
AVL: L04-0107800-M26

CHOKE9 CH-1.0u15A7.5mS-HF
R257 X_2.2R/8 — C231 X_C3300p50X4
EC29 560u6.3SO — EC28 560u6.3SO — C183 C22u6.3X6 — C273 C10u6.3X6 — C232 C10u6.3X6 — C234 C1u6.3X4
PCH_1VSB

CP29 PCH_1VSB
PLACE UNDER THE PCH

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)

PCH_1VSB_EN — R192 36KR1%4 — C170 X_C33p50N4 — C142 C3300p50X4

RT8125C C170&R192&C142 ->NC
up1540 C170->NC;R192->36K;C142->3.3nf

0728: add
5VDUAL — R196 X_47K/4

PCH_1VSB_EN — C181 X_C0.1u10X4

0728: Change net name
ATX_5VSB — R184 10K/4 — OPC_1P8_EN# — Q36 2N7002
C173 X_C0.1u10X4

PCH_1VSB_EN — (40,45,57) SIO_SLPSUS — Q58 2N7002

3VSB — R10 1K1%4 — R13 2.21KR1%4 — Q34 N-SST3904_SOT23

0902 : Stuff R when NO PCH_1P8 & V_OPC_1P8

PCH_1P8

Remove circuit

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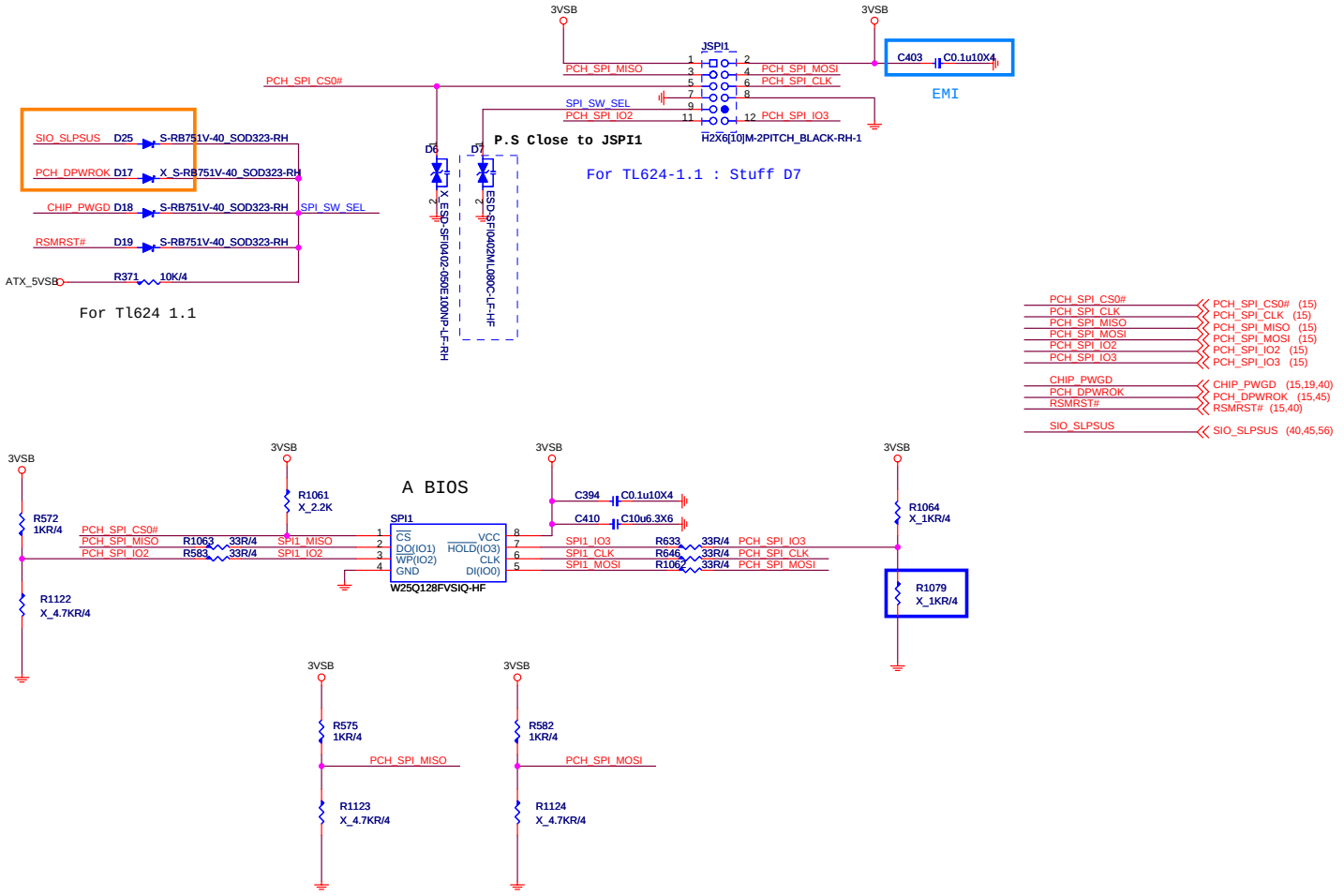
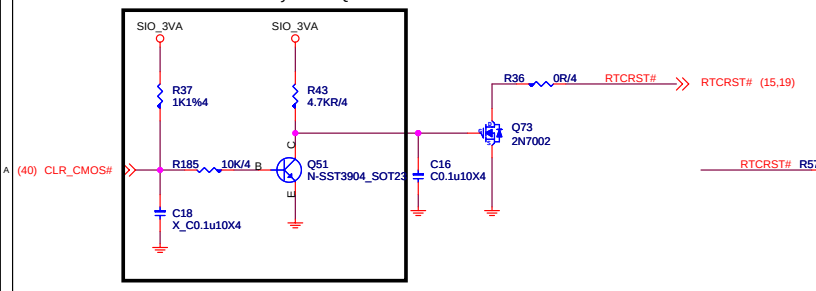
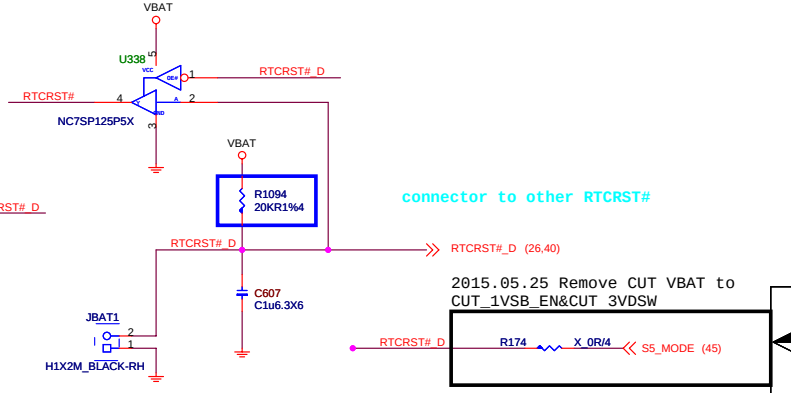


CLR_CMOS

2015.04.23 Modify R37 Q51 & Add R185





tri-state

INPUT		outout
PIN1	PIN2	pin4
L	H	H
L	L	L
H	X	Z

	R57	U338	R1094	C607
USE U338 Auto CLR_CMOS	X	0	0	0
NOT USE U338 Auto CLR_CMOS	0	X	X	X

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PCB

PCB

7970_1.0

P/N:PD0-0797010-G37

CPU Socket

CPU_H1

CPU 鍍座

CPU_H1

Battery

BAT1_X1

BAT-BCR2032P-RH

PCH

PCH_H170

PCH 料號

X_PCH_H170

D0:OB1-7968006

D1:OB1-7982001

PCH_B150

PCH 料號

X_PCH_B150

D0:OB1-7968004

D1:OB1-7981001

2015.04.28 Remove LAN/Audio cover

SBC Label

SBC_LA1

Label SBC

SBC LABEL

HDMI Label

HDMI_LA1

Label HDMI

HDMI LABEL

BIOS Label

AMI_LA1

AMI_BIOS LABLE

BIOS_LABLE

Marketing Label

Z170_LA1

Label Z97-Gaming3

MKT-LABEL

B150_LA3

Label Z97-Gaming3

X_MKT-LABEL

H170_LA2

Label Z97-Gaming3

X_MKT-LABEL

Z170-G43_LA1

Label Z97-Gaming3

X_MKT-LABEL

USB3.1 Label

USB31_LA1

Label HDMI

U3.1 LABEL

DIMM-R

DIMM 料號

X_DIMM-Red

PCIE-Rx16

SLOT 料號

X_PCIE-Redx16

PCIE-Rx4

SLOT 料號

X_PCIE-Redx4

Audio-C

Audio 料號

X_Audio-C

PS2-C

PS2 料號

X_PS2-C

USB-Black

USB2.0 料號

X_USB-Black

LAN-Blue1

LAN-CON 料號

X_LAN-Blue

USB-Blue1

USB3.1 料號

X_USB-Blue

PCH Heatsink

HS_PCH1

MEC2

MEC1

HS-0407410-RH

PCH-HS1

PCH HS

X_PCH-HS1

MOS1 Heatsink

HS_MOS1

HS-0503250-RH

MEC1 MEC2

MOS-HS1

MOS HS

X_MOS-HS1

1.1

2.0

MOS2 Heatsink

HS_MOS2

HS-0503260-RH

MEC1 MEC2

MOS-HS2

MOS HS

X_MOS-HS1

2015.05.11 Add EMI suggestion

(13,40) CLK_SIO_PCI — C377 X_10p50N4

(13) CLK_BUFFER — C378 X_10p50N4

(13,40) CLK_SIO_24M — C380 X_10p50N4

(13,44) TPM_CLK — C418 X_10p50N4

(13,39) AZ_BITCLK — C420 X_10p50N4

VCC5 — C482 X_10p50N4

VCC5 — C491 X_10p50N4

VCC5 — C514 X_10p50N4

VCC5 — C515 X_10p50N4

Mounting Holes

MH1 MH2 MH3 MH4 MH5 MH6 MH7 MH8 MH9

X_MH001

2015.05.11 Add

C466 C0.1u10X4

C510 C0.1u10X4

Test point

VCORE — VCORE

VGT — VGT

VCC_DDR — VCC_DDR

VCCSA — VCCSA

VCCIO — VCCIO

PCH_1VSB — PCH_1VSB

VCCSTPLL — VCCST

VCCSFR_OC — VCCSFR

VTT_DDR — VTT_DDR

VPP25 — VPP25

Simulation

SIM1 — X_PIN1*2

SIM2 — X_PIN1*2

Optical Fiducial Marks-120

FM1 FM2 FM3 FM4 FM5 FM6 FM7 FM8

X_FM

2015.04.28 Add

LED placed in the four corners of board.

2015.07.03 Add

2015.07.03 Add

VCC5

RA72 1K — LEDA8 LED04-R-30mA

RA71 1K — LEDA7 LED04-R-30mA

RA69 1K — LEDA6 LED04-R-30mA

RA68 1K — LEDA5 LED04-R-30mA

RA67 1K — LEDA1 LED04-R-30mA

RA70 1K — LEDA2 LED04-R-30mA

RA129 1K — LEDA3 LED04-R-30mA

RA130 1K — LEDA4 LED04-R-30mA

RA132 1K — LEDA9 LED04-R-30mA

RA131 1K — LEDA10 LED04-R-30mA

RA134 1K — LEDA11 LED04-R-30mA

RA133 1K — LEDA12 LED04-R-30mA

(40) ALL_LED_OFF# — R60 X_0R/4 — LED_OFF# — Q97 2N7002

(40) PCH_LED — R38 0R/4

(44) LED_OFF# — LED_OFF# — Q98 2N7002

LED_OFF# — Q100 2N7002

LED_OFF# — Q102 2N7002

LED_OFF# — Q111 2N7002

LED_OFF# — Q113 2N7002

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