
msi
Z77A-GD65
msi
GEN3
TOP QUALITY & STA
MILITAR
CLAS
III
1 Sec Overclocking
OC Genie II
Click BIOS II
MILITARY CLASS MAINBOARD
Z77A-GD65

MS-7751

ATX

Ver: 2.1

Intel -MahoBay plamform Z77

CPU:

IVY bridge LGA1155
*CPU DrMOS *8 Phase*
*GFX DrMOS *2 Phase*

System Chipset:

Panther Point

Onboard Chip:

SATA Controller: Asmedia ASM1061 6G
HD Audio Codec:ALC898 colay ALC892/887
LAN-INTEL 82579
SIO:Fintek F71889AD
Flash ROM: SPI 64 MB X2
1394: VT6315N
CLK Buffer: 9DB433

PWM:

VRD12 -UP1618 - 8Phase

Other:

SATA3.0 x2+SATA2.0 x4 (PCH)
SATA3.0 x2 (Marvell 88SE9128B1)
*USB2.0 *8*
*REAL USB3.0 *2*
*FRONT USB3.0 *2*
*FRONT 1394 *1*

Main Memory:

*DDRIII (800/1066/1333/1666MHz) * 4 (Dual Channel)*

ACPI:

UPI

Expansion Slots:

*PCI Express (X16) Slot * 3*
*PCI Express (X1) Slot * 4*

MICRO-STAR INT'L CO.,LTD

MS-7751

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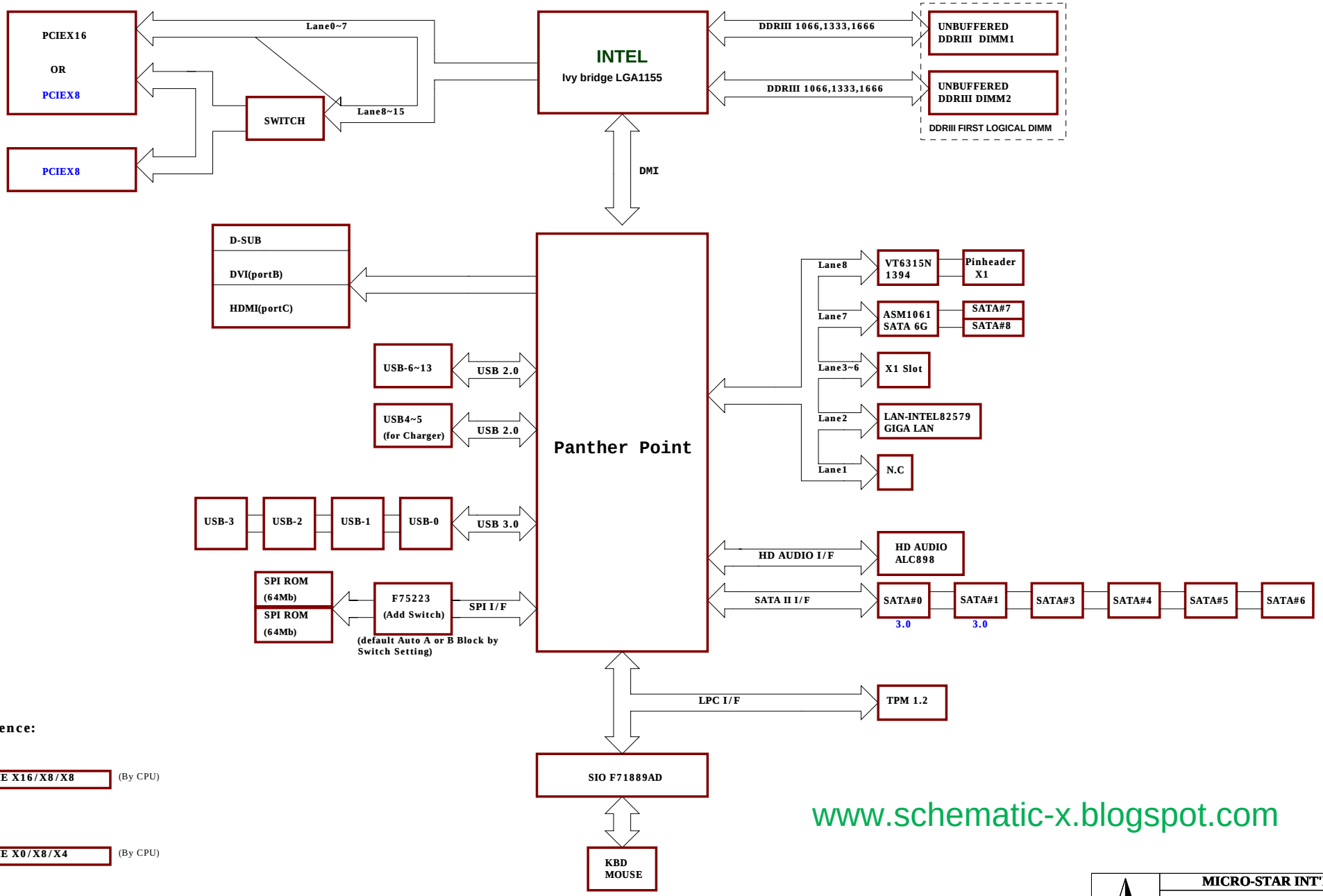
MS-7751_2.0 Block Diagram



Slot Sequence:

- PCIE X1
- PCIE X16/X8/X8 (By CPU)
- PCIE X1
- PCIE X1
- PCIE X0/X8/X4 (By CPU)
- PCIE X1
- PCIE X0/X0/X4 (By CPU)

MICRO-STAR INT'L CO.,LTD	
MS-7751	
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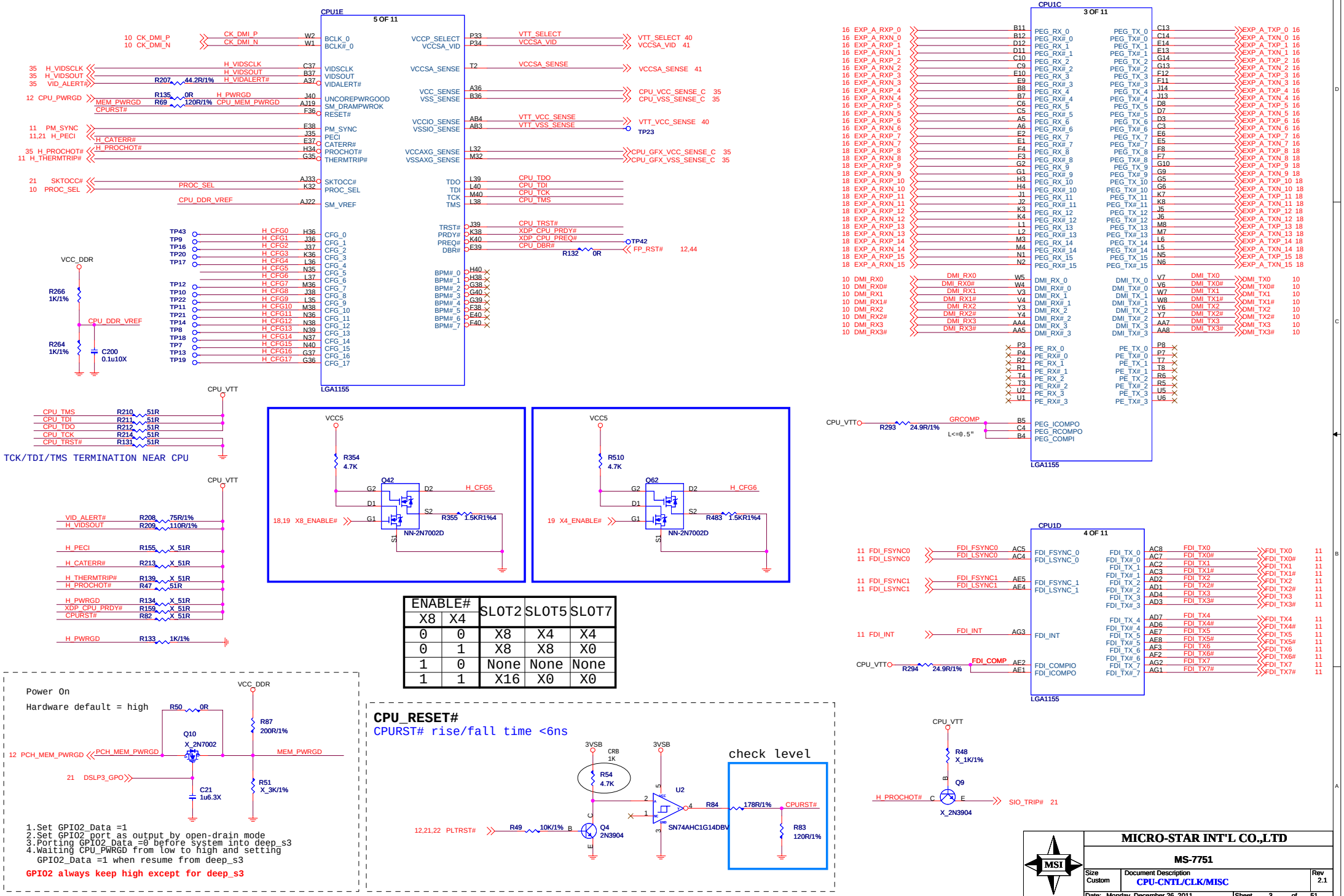
CPU1E
5 OF 11
LGA1155
CPU1C
3 OF 11
LGA1155
CPU1D
4 OF 11
LGA1155
TCK/TDI/TMS TERMINATION NEAR CPU
ENABLE#
X8 X4
SLOT2 SLOT5 SLOT7
0 0 X8 X4 X4
0 1 X8 X8 X0
1 0 None None None
1 1 X16 X0 X0
Power On
Hardware default = high
1.Set GPIO2_Data =1
2.Set GPIO2_port as output by open-drain mode
3.Porting GPIO2_Data =0 before system into deep_s3
4.Waiting CPU_PWRGD from low to high and setting
GPIO2_Data =1 when resume from deep_s3
GPIO2 always keep high except for deep_s3
CPU_RESET#
CPURST# rise/fall time <6ns
check level
MICRO-STAR INT'L CO.,LTD
MS-7751
CPU-CNTL/CLK/MISC
Size Custom
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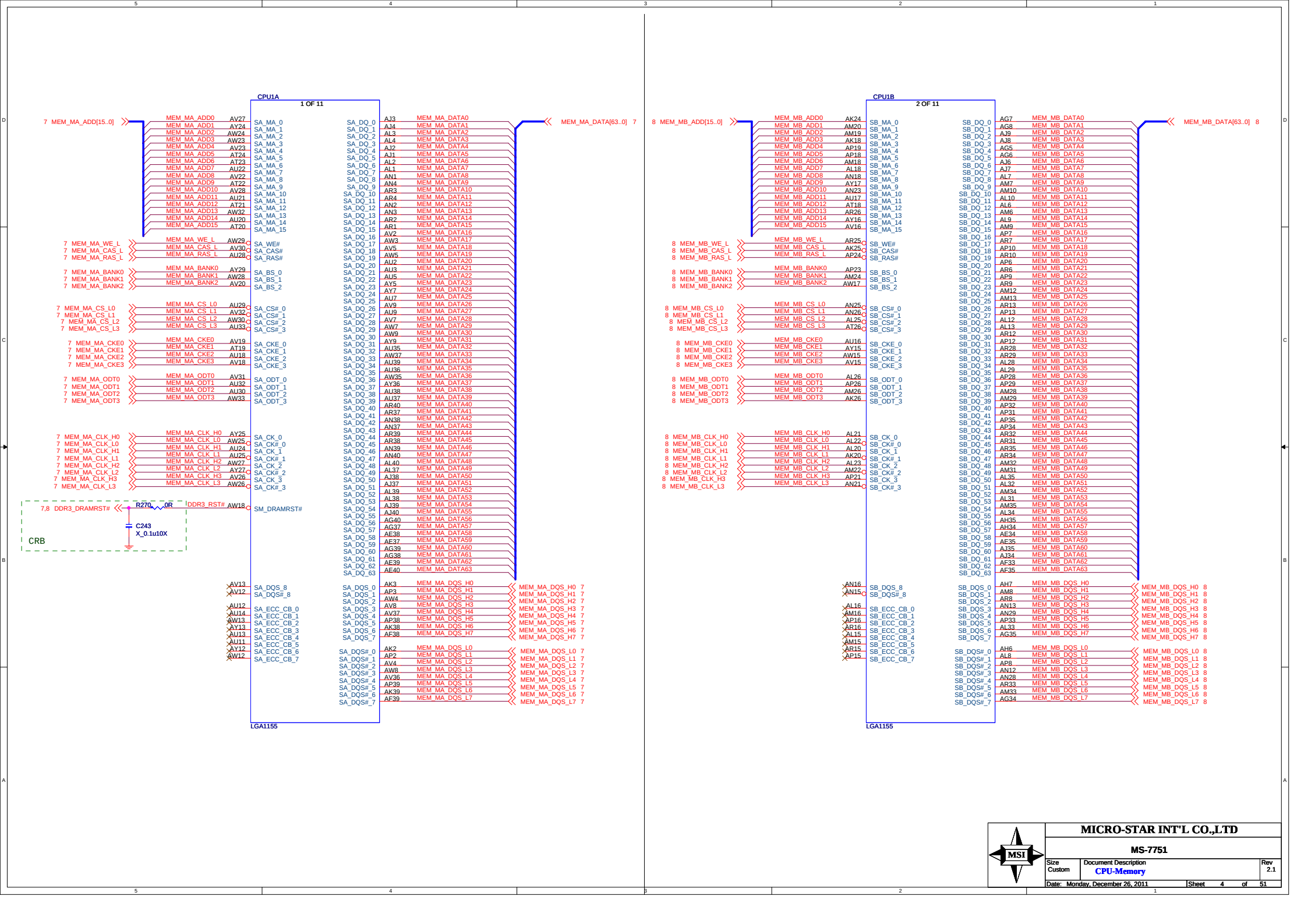
CPU1A
1 OF 11
LGA1155
CPU1B
2 OF 11
LGA1155
CRB
R270 0R
C243
X_0.1u10X
DDR3_RST#
SM_DRAMRST#
MEM_MA_DATA[63..0]
MEM_MB_DATA[63..0]
MICRO-STAR INT'L CO.,LTD
MS-7751
Size
Custom
Document Description
CPU-Memory
Rev
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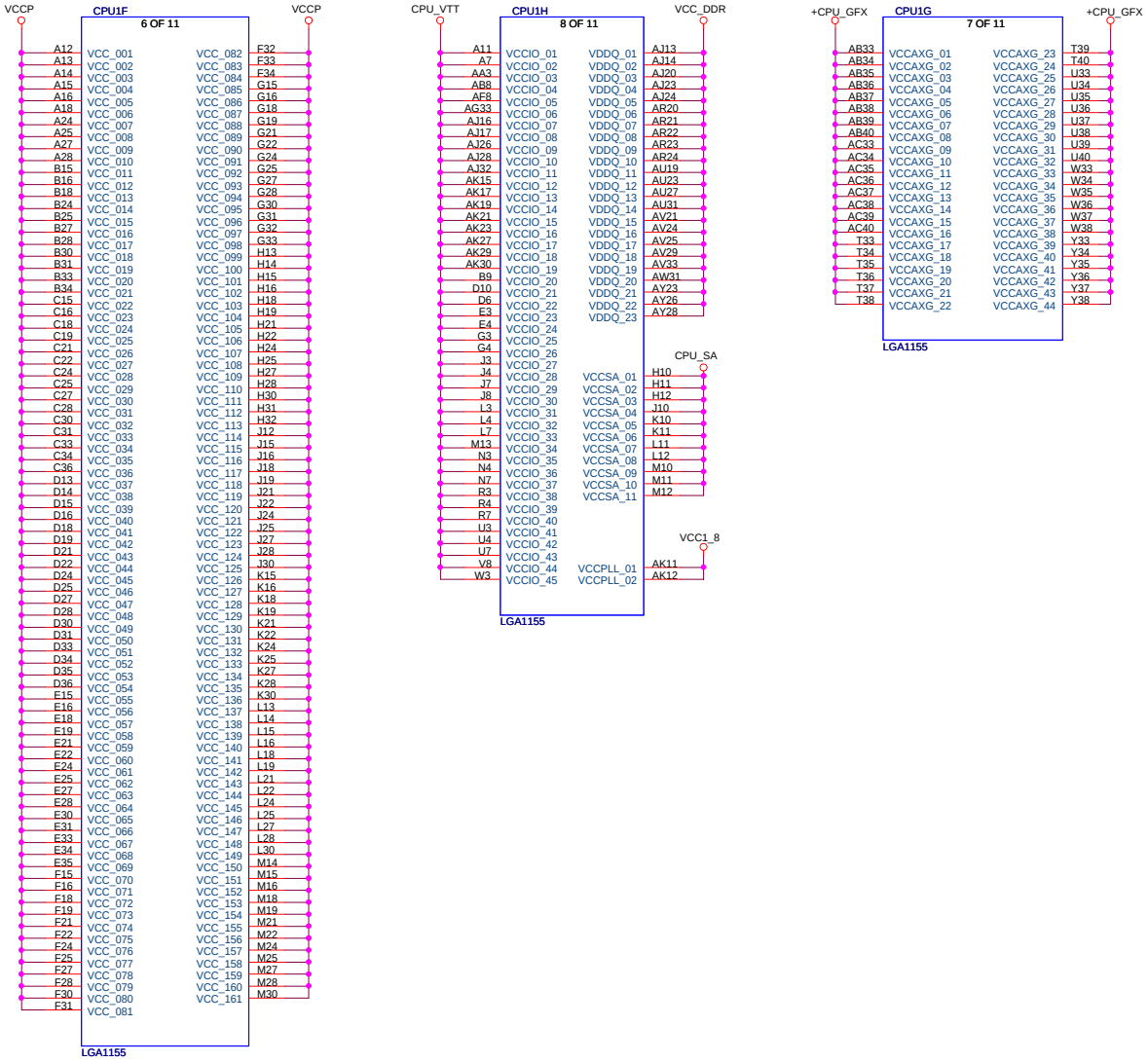
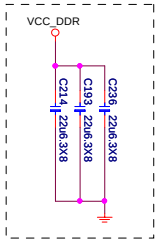


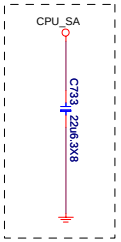
+1.5V_DDR3-Decoupling

CPU SOCKET CAVITY CAPS



+CPU_SA Decoupling

Backside

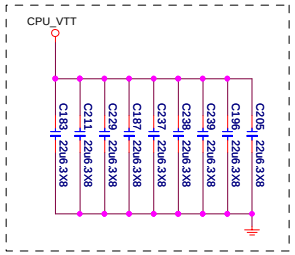


+VCC1_8 Decoupling

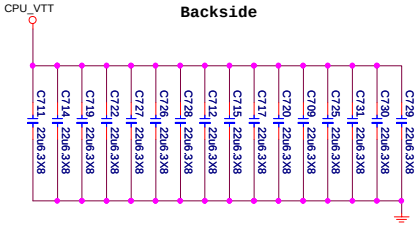
Backside

+CPU_VTT Decoupling

CPU SOCKET CAVITY CAPS

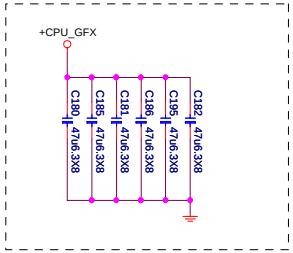


Backside

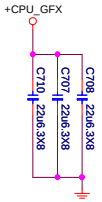


+CPU_GFX Decoupling

CPU SOCKET CAVITY CAPS

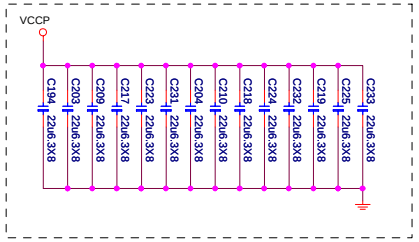


Backside

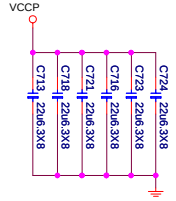


+CPU_VCCP-Decoupling

CPU SOCKET CAVITY CAPS



Backside



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7751	
Size: Custom	Document Description: CPU-Power	Rev: 2.1
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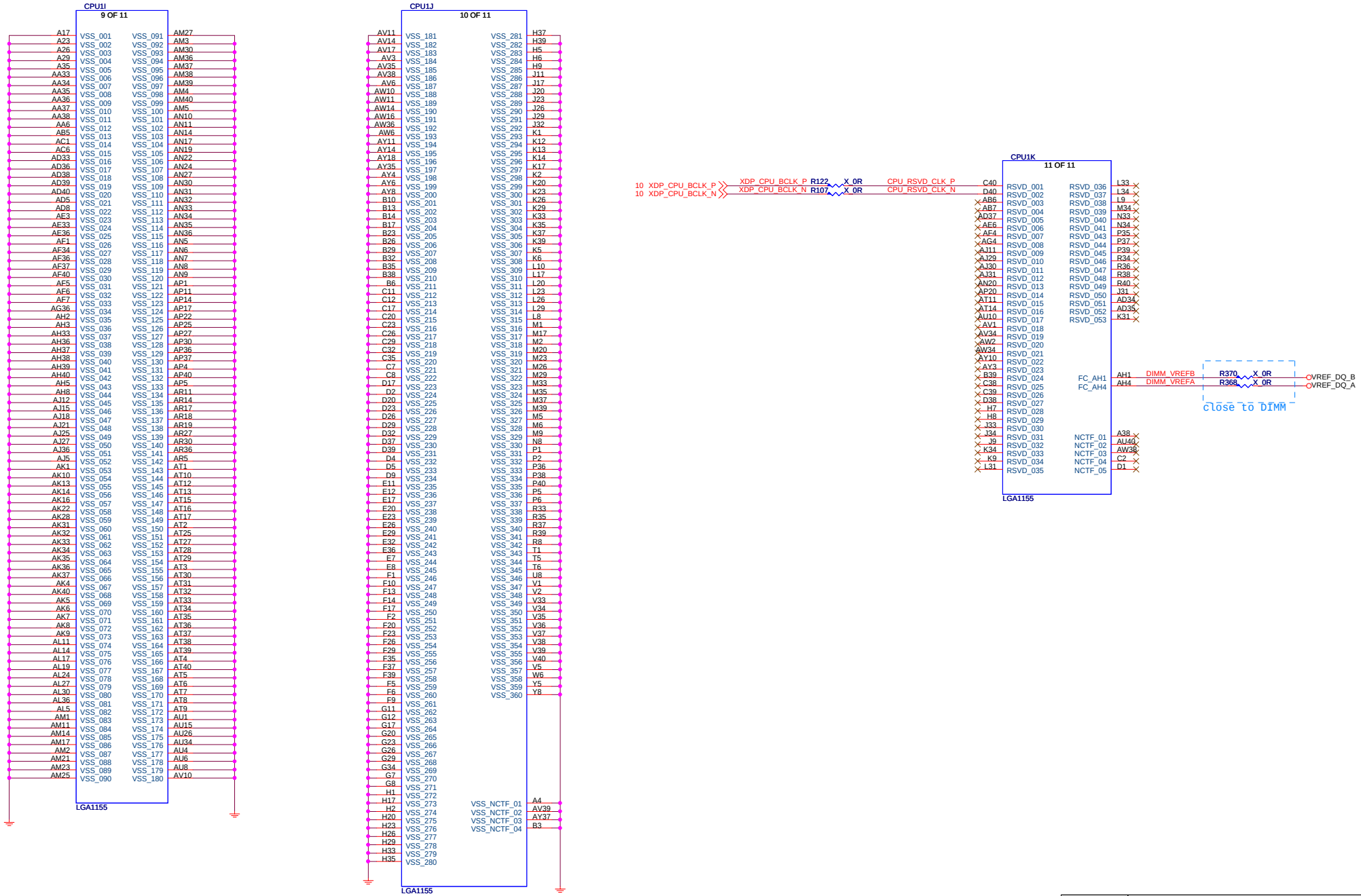
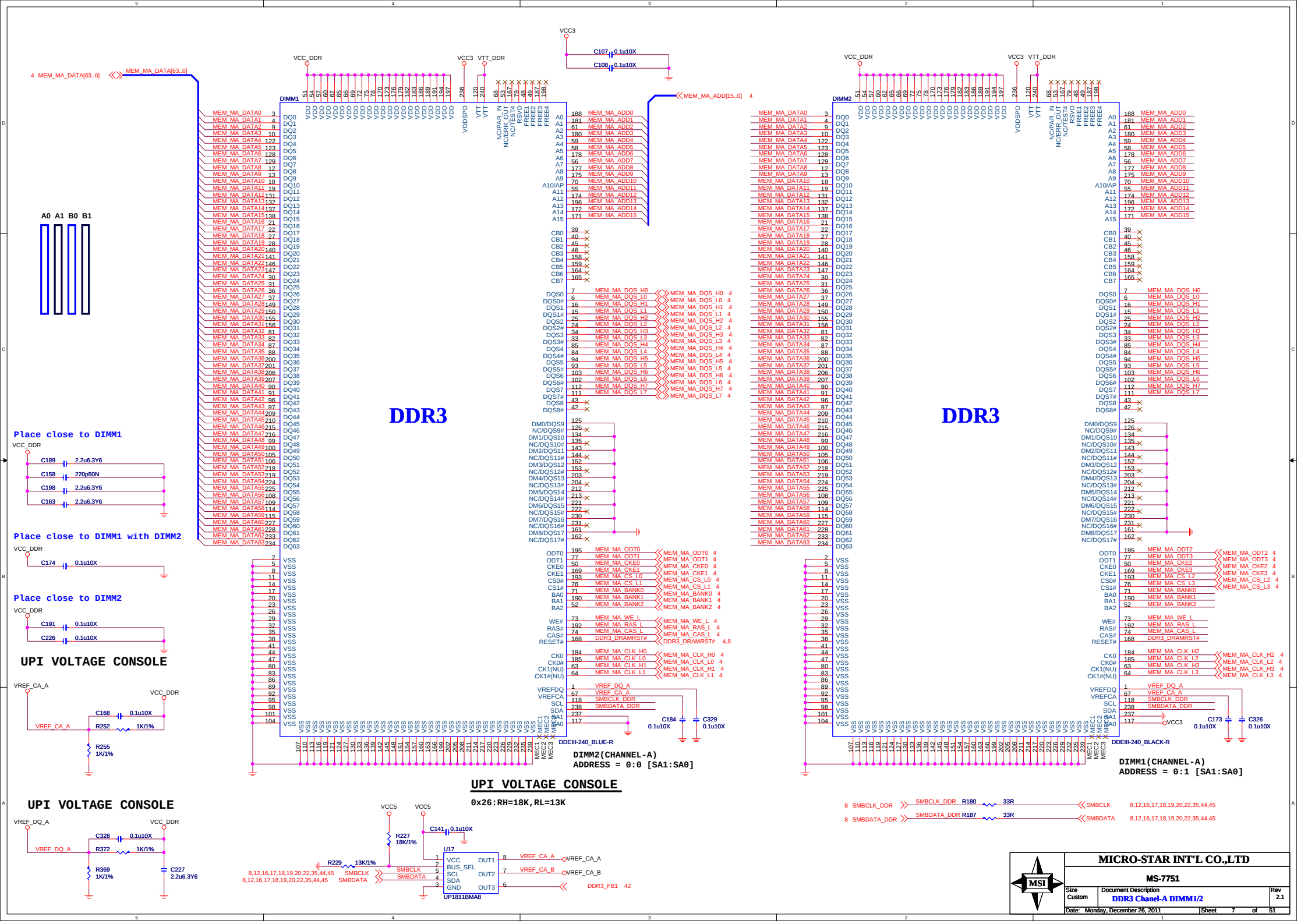


MICRO-STAR INT'L CO.,LTD	
MS-7751	
Size: Custom	Document Description: CPU-GND
Rev: 2.1	
Date: Monday, December 26, 2011	Sheet 6 of 51


DDR3
DIMM1
DIMM2
DDR3
DDEIII-240_BLUE-R
DDEIII-240_BLACK-R
DIMM2(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]
DIMM1(CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]
A0 A1 B0 B1
Place close to DIMM1
Place close to DIMM1 with DIMM2
Place close to DIMM2
UPI VOLTAGE CONSOLE
UPI VOLTAGE CONSOLE
UPI VOLTAGE CONSOLE
0x26:RH=18K,RL=13K
UP1811BMA8
MICRO-STAR INT'L CO.,LTD
MS-7751
DDR3 Chanel-A DIMM1/2
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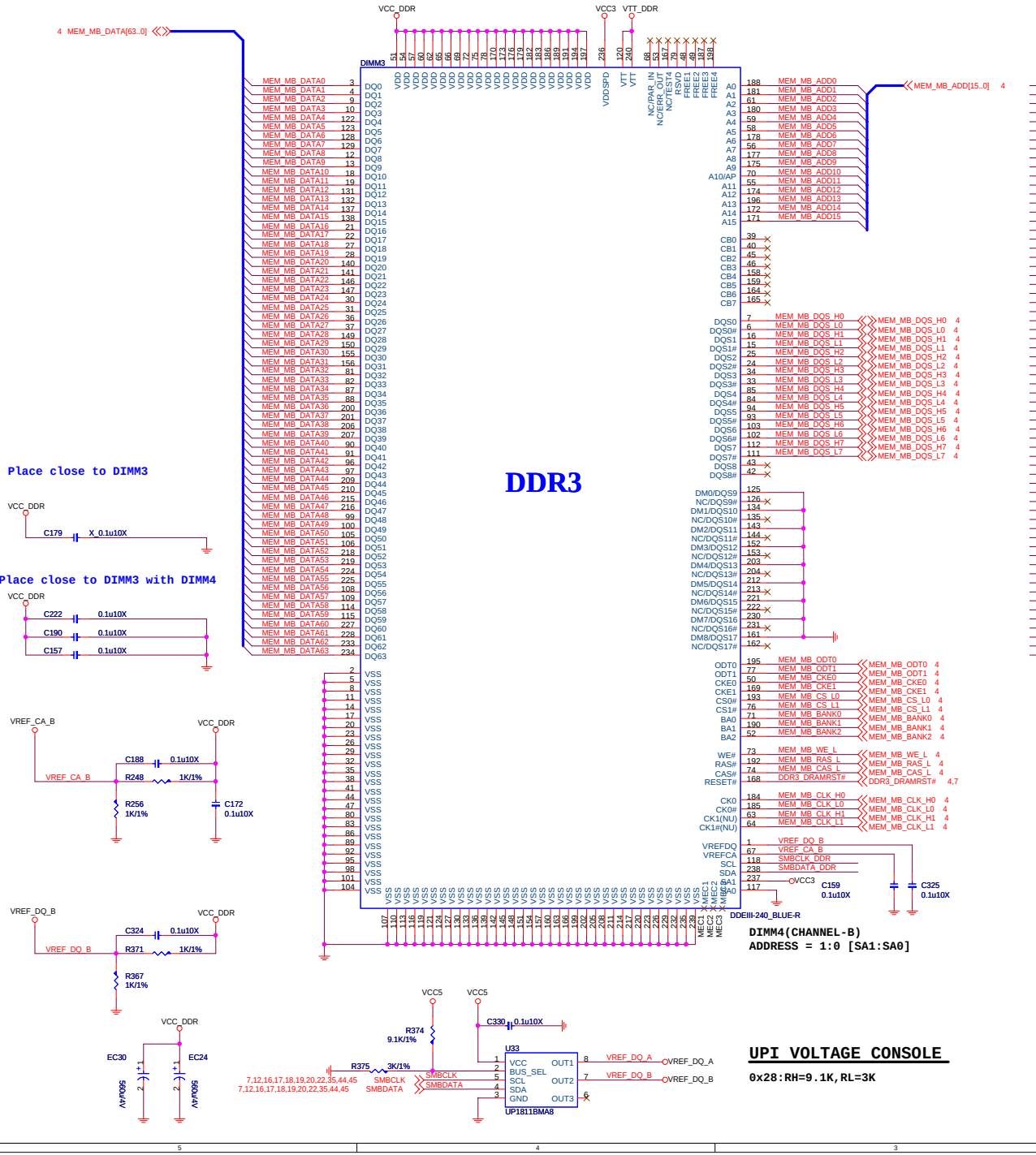
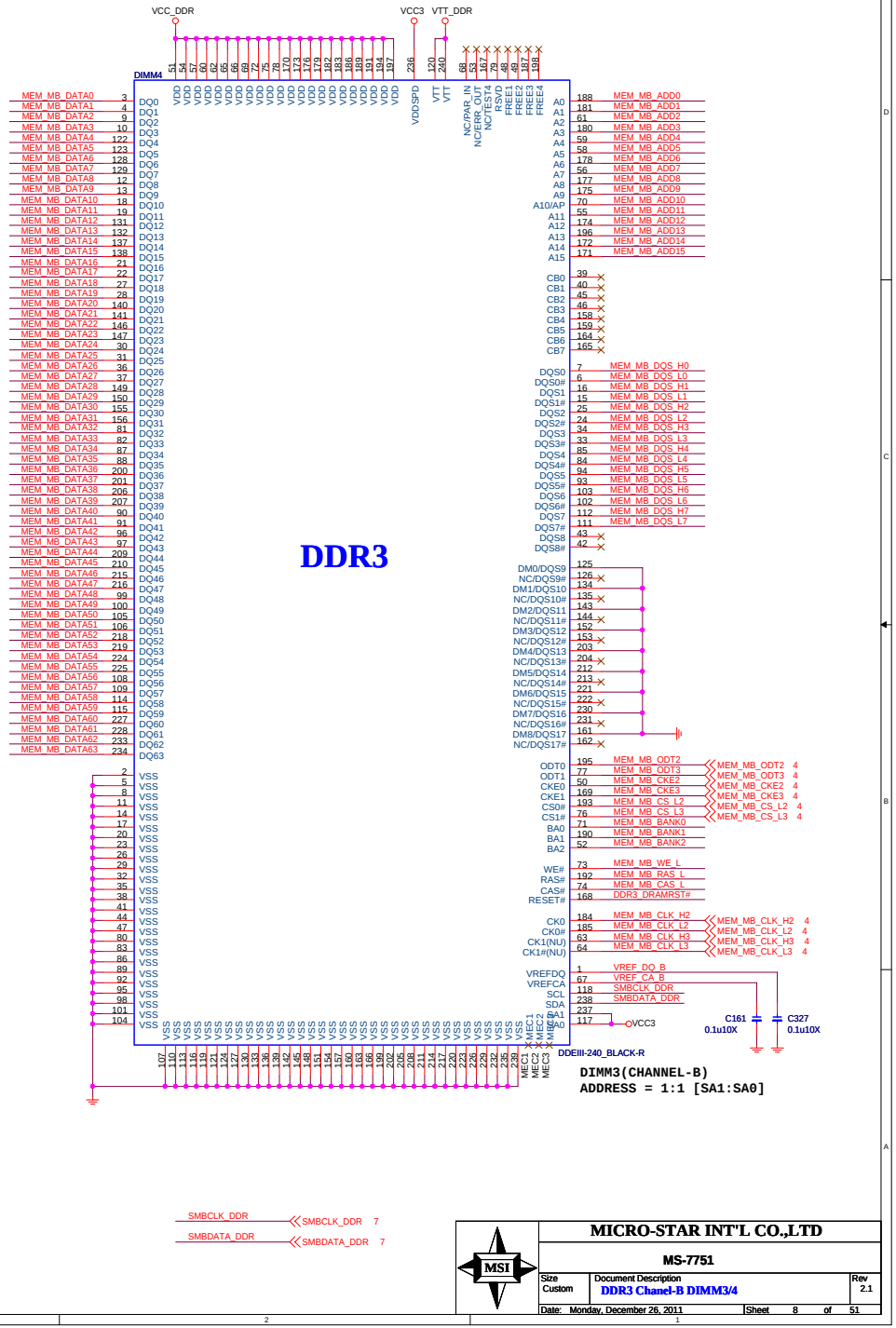
DDRIII DIMM_B0



DDRIII DIMM_B1



MICRO-STAR INT'L CO.,LTD		
MS-7751		
Size: Custom	Document Description: DDR3 Chanel-B DIMM3/4	Rev: 2.1
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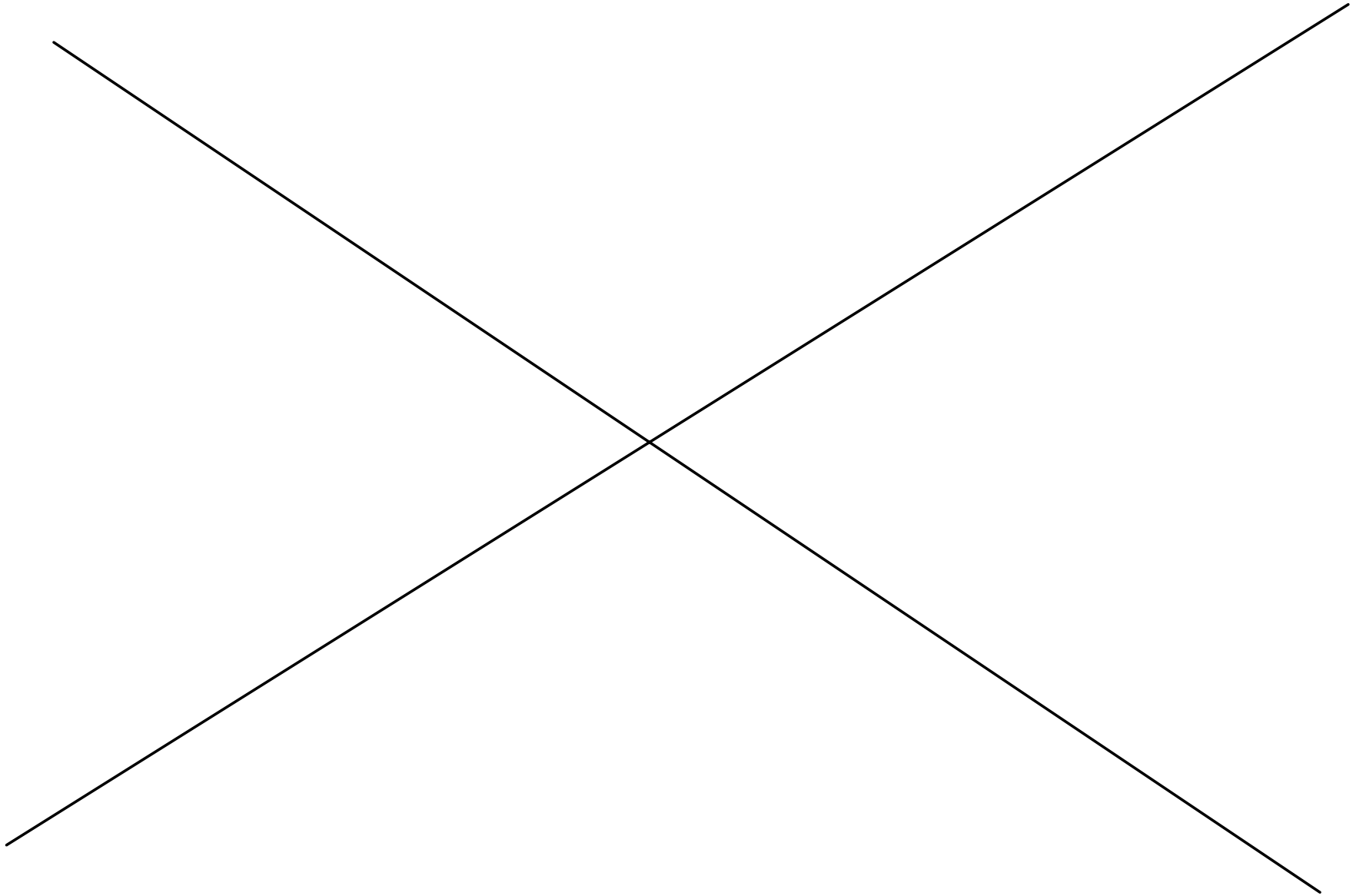

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7751	
Size: Custom	Document Description: CLK GEN4105	Rev: 2.1
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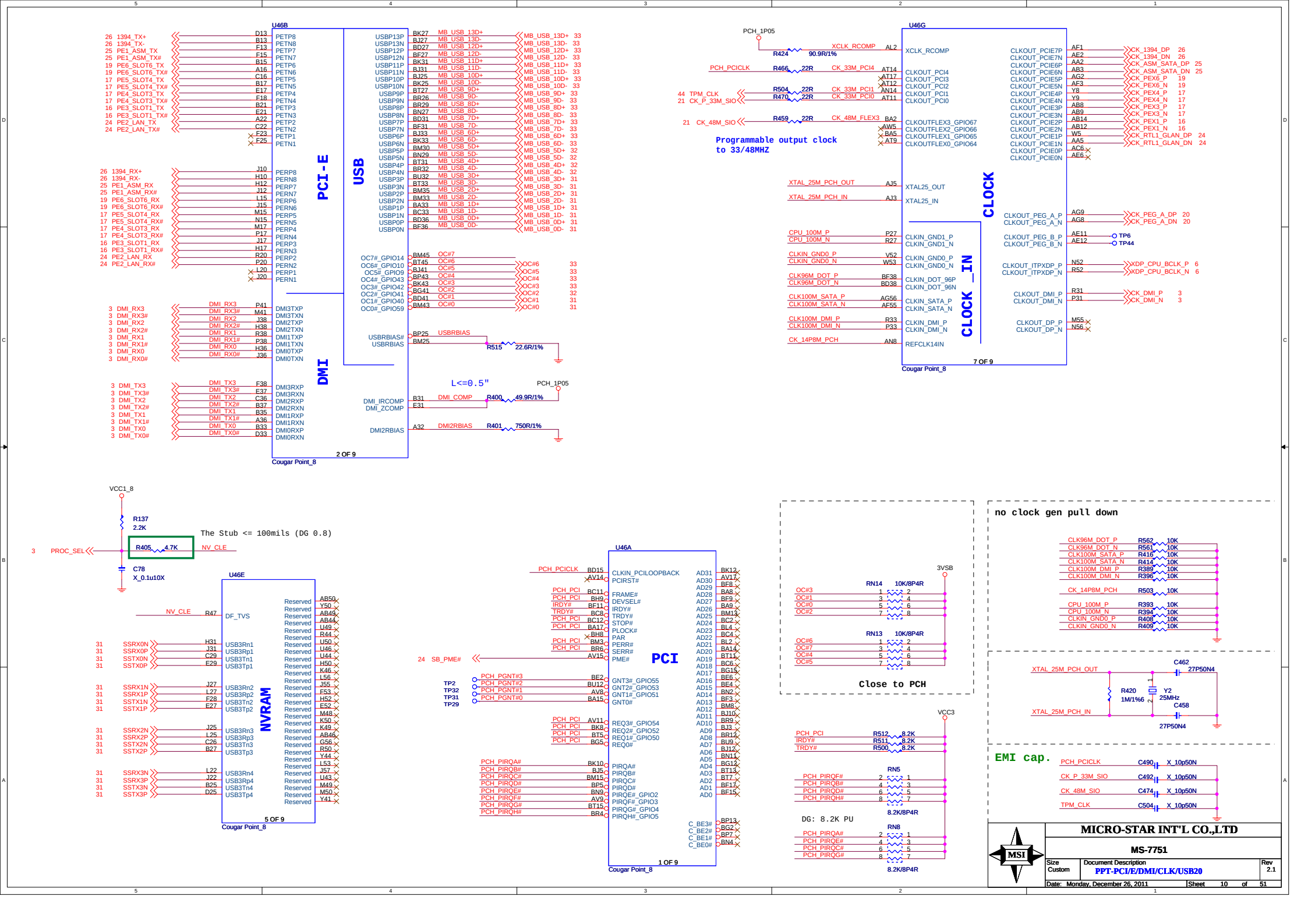
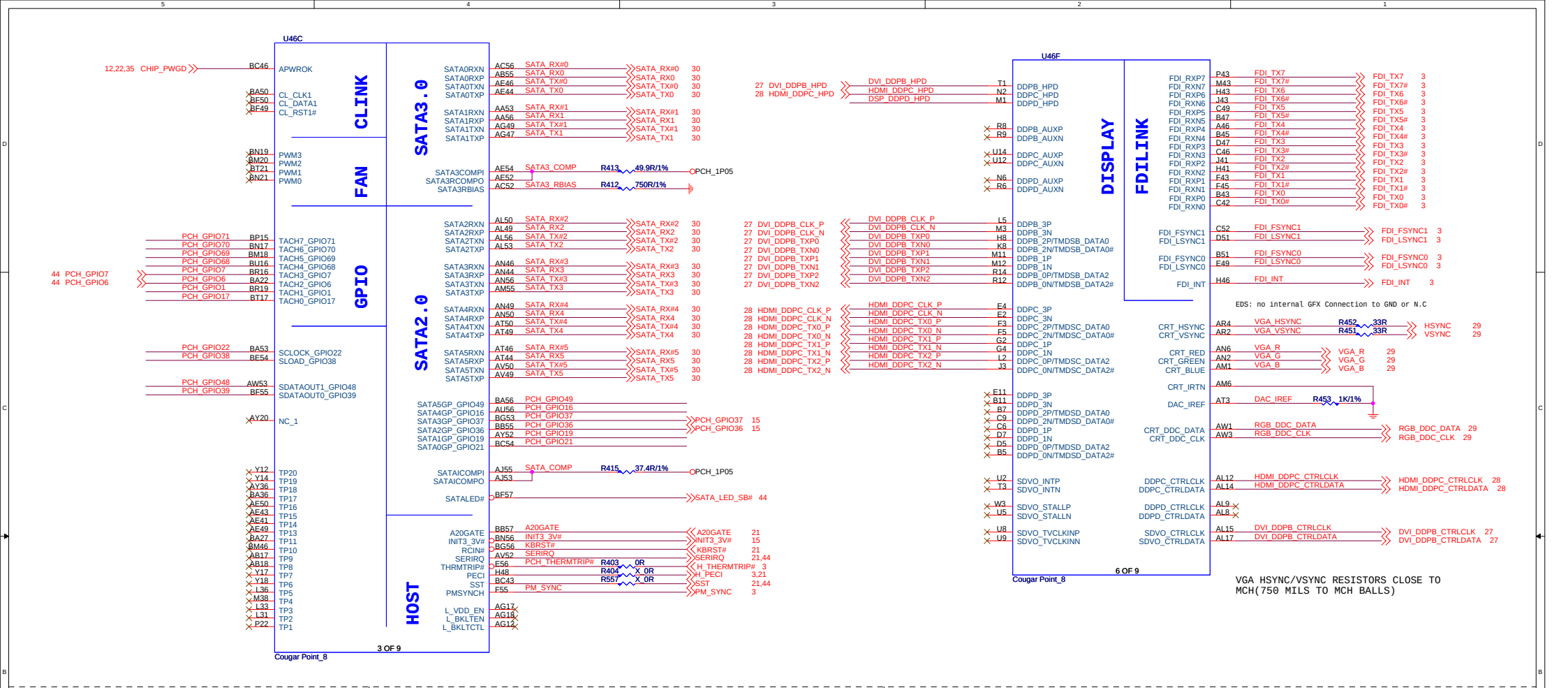

U46B
PCI-E
USB
DMI
2 OF 9
Cougar Point_8
U46G
CLOCK
CLOCK_IN
7 OF 9
Cougar Point_8
Programmable output clock
to 33/48MHZ
L<=0.5"
U46E
NVRAM
5 OF 9
Cougar Point_8
The Stub <= 100mils (DG 0.8)
U46A
PCI
1 OF 9
Cougar Point_8
Close to PCH
DG: 8.2K PU
no clock gen pull down
EMI cap.
MICRO-STAR INT'L CO.,LTD
MS-7751
PPT-PCI/E/DMI/CLK/USB20
Monday, December 26, 2011


U46C
CLINK
FAN
GPIO
SATA3.0
SATA2.0
HOST
CHIP_PWGD
APWROK
CL_CLK1
CL_DATA1
CL_RST1#
PWM3
PWM2
PWM1
PWM0
TACH7_GPIO71
TACH6_GPIO70
TACH5_GPIO69
TACH4_GPIO68
TACH3_GPIO7
TACH2_GPIO6
TACH1_GPIO1
TACH0_GPIO17
SCLOCK_GPIO22
SLOAD_GPIO38
SDATAOUT1_GPIO48
SDATAOUT0_GPIO39
NC_1
TP20
TP19
TP18
TP17
TP16
TP15
TP14
TP13
TP11
TP10
TP9
TP8
TP7
TP6
TP5
TP4
TP3
TP2
TP1
SATA_RX#0
SATA_RX0
SATA_TX#0
SATA_TX0
SATA_RX#1
SATA_RX1
SATA_TX#1
SATA_TX1
SATA3_COMP
SATA3_RBIAS
R413 49.9R/1%
R412 750R/1%
SATA_RX#2
SATA_RX2
SATA_TX#2
SATA_TX2
SATA_RX#3
SATA_RX3
SATA_TX#3
SATA_TX3
SATA_RX#4
SATA_RX4
SATA_TX#4
SATA_TX4
SATA_RX#5
SATA_RX5
SATA_TX#5
SATA_TX5
PCH_GPIO49
PCH_GPIO16
PCH_GPIO37
PCH_GPIO36
PCH_GPIO19
PCH_GPIO21
SATA_COMP
R415 37.4R/1%
SATALED#
SATA_LED_SB#
A20GATE
INIT3_3V#
KBRST#
RCIN#
SERIRQ
PCH_THERMTRIP#
R403 0R
R404 X_0R
R557 X_0R
PM_SYNC
L_VDD_EN
L_BKLTEN
L_BKLTCTL
3 OF 9
Cougar Point_8
U46F
DDPB_HPD
HDMI_DDPC_HPD
DSP_DDPD_HPD
DDPB_AUXP
DDPB_AUXN
DDPC_AUXP
DDPC_AUXN
DDPD_AUXP
DDPD_AUXN
DDPB_3P
DDPB_3N
DDPB_2P/TMDSB_DATA0
DDPB_2N/TMDSB_DATA0#
DDPB_1P
DDPB_1N
DDPB_0P/TMDSB_DATA2
DDPB_0N/TMDSB_DATA2#
DDPC_3P
DDPC_3N
DDPC_2P/TMDSC_DATA0
DDPC_2N/TMDSC_DATA0#
DDPC_1P
DDPC_1N
DDPC_0P/TMDSC_DATA2
DDPC_0N/TMDSC_DATA2#
DDPD_3P
DDPD_3N
DDPD_2P/TMDSD_DATA0
DDPD_2N/TMDSD_DATA0#
DDPD_1P
DDPD_1N
DDPD_0P/TMDSD_DATA2
DDPD_0N/TMDSD_DATA2#
SDVO_INTP
SDVO_INTN
SDVO_STALLP
SDVO_STALLN
SDVO_TVCLKINP
SDVO_TVCLKINN
DISPLAY
FDILINK
FDI_RXP7
FDI_RXN7
FDI_RXP6
FDI_RXN6
FDI_RXP5
FDI_RXN5
FDI_RXP4
FDI_RXN4
FDI_RXP3
FDI_RXN3
FDI_RXP2
FDI_RXN2
FDI_RXP1
FDI_RXN1
FDI_RXP0
FDI_RXN0
FDI_TX7
FDI_TX7#
FDI_TX6
FDI_TX6#
FDI_TX5
FDI_TX5#
FDI_TX4
FDI_TX4#
FDI_TX3
FDI_TX3#
FDI_TX2
FDI_TX2#
FDI_TX1
FDI_TX1#
FDI_TX0
FDI_TX0#
FDI_FSYNC1
FDI_LSYNC1
FDI_FSYNC0
FDI_LSYNC0
FDI_INT
EDS: no internal GFX Connection to GND or N.C
CRT_HSYNC
CRT_VSYNC
CRT_RED
CRT_GREEN
CRT_BLUE
CRT_IRTN
DAC_IREF
R452 33R
R451 33R
R453 1K/1%
CRT_DDC_DATA
CRT_DDC_CLK
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPD_CTRLCLK
DDPD_CTRLDATA
SDVO_CTRLCLK
SDVO_CTRLDATA
HSYNC
VSYNC
VGA_R
VGA_G
VGA_B
RGB_DDC_DATA
RGB_DDC_CLK
HDMI_DDPC_CTRLCLK
HDMI_DDPC_CTRLDATA
DVI_DDPB_CTRLCLK
DVI_DDPB_CTRLDATA
6 OF 9
Cougar Point_8
VGA HSYNC/VSYNC RESISTORS CLOSE TO MCH(750 MILS TO MCH BALLS)
Pull HIGH for PCH
VCC3
RN9
RN3
RN4
10K/8P4R
R541 10K
R517 10K
R539 X_10K
R518 X_10K
R439 10K
R428 10K
R422 10K
R437 10K
R473 10K
RTC and CLR_CMOS
VBAT
3VA
20mil
D16
SBAT54C
JBAT1
H1X2M_BLACK-RH
RTCRST#
R551
20K/1%
C524 1u16X6
C515 1u16X6
R495
1K/1%
BAT1
BAT-2P-RH-1
Close to PCH
CLR_CMOS1
SW-TACTB1
HDMI_DDPC_HPD R411 X_1K
DSP_DDPD_HPD R410 X_1K
DVI_DDPB_HPD R286 X_1K
PCH_THERMTRIP#
R402 X_51R
CPU_VTT
Enable VGA(CTRLCLK/DATA Pull High)
RN6 2.2K/8P4R
Close to PCH within 250 mils.
R434 150R/1%
R431 150R/1%
R425 150R/1%
MICRO-STAR INT'L CO.,LTD
MS-7751
Size Custom
Document Description PPT-SATA/HOST/GPIO/VGA/CCMOS
Rev 2.1
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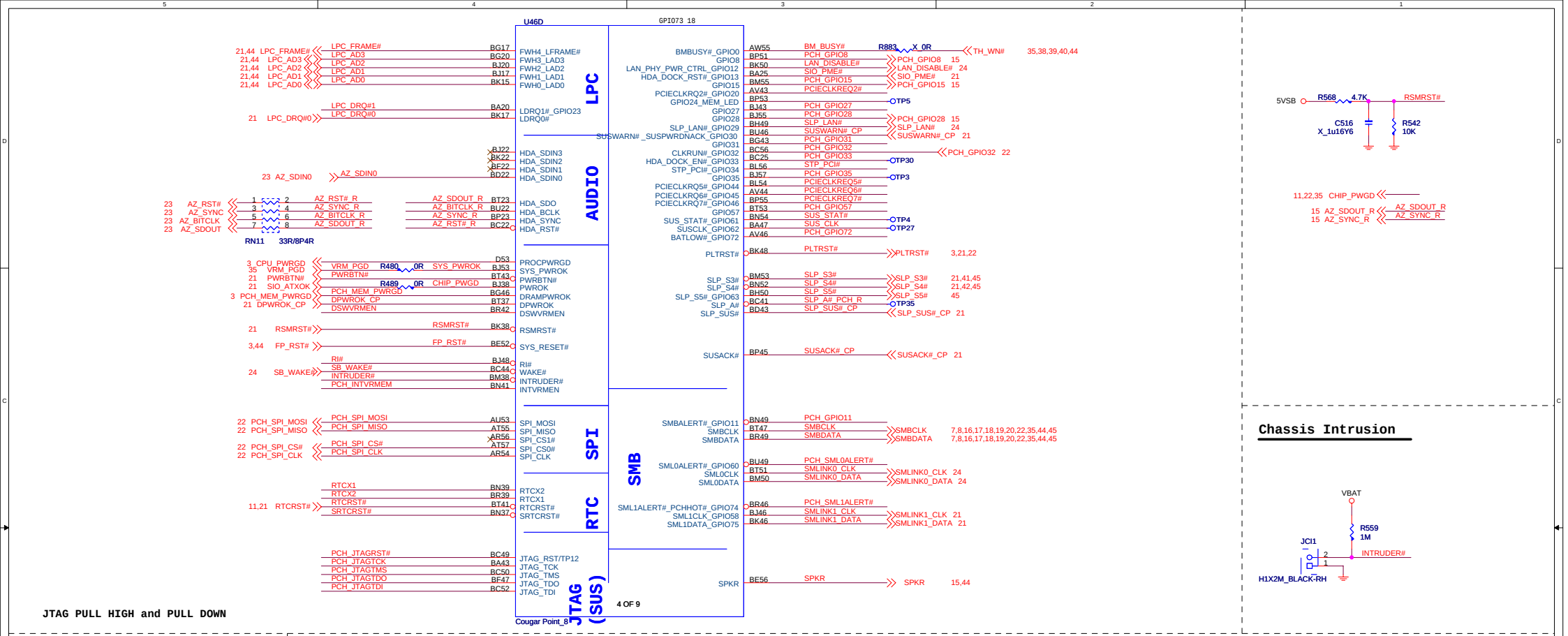
U46D
LPC
AUDIO
SPI
SMB
RTC
JTAG (SUS)
Cougar Point_8
4 OF 9
JTAG PULL HIGH and PULL DOWN
Chassis Intrusion
INTRUDER#
H1X2M_BLACK-RH
RTC Block
Close to PCH
32.768KHZ12.5P
Y3
EMI cap.
AZ_BITCLK
C527
X_10p50N
PCIECLKREQ can't find 0/1/3/4
MICRO-STAR INT'L CO.,LTD
MS-7751
PPT-SMB/LPC/AUDIO/RTC/SPI
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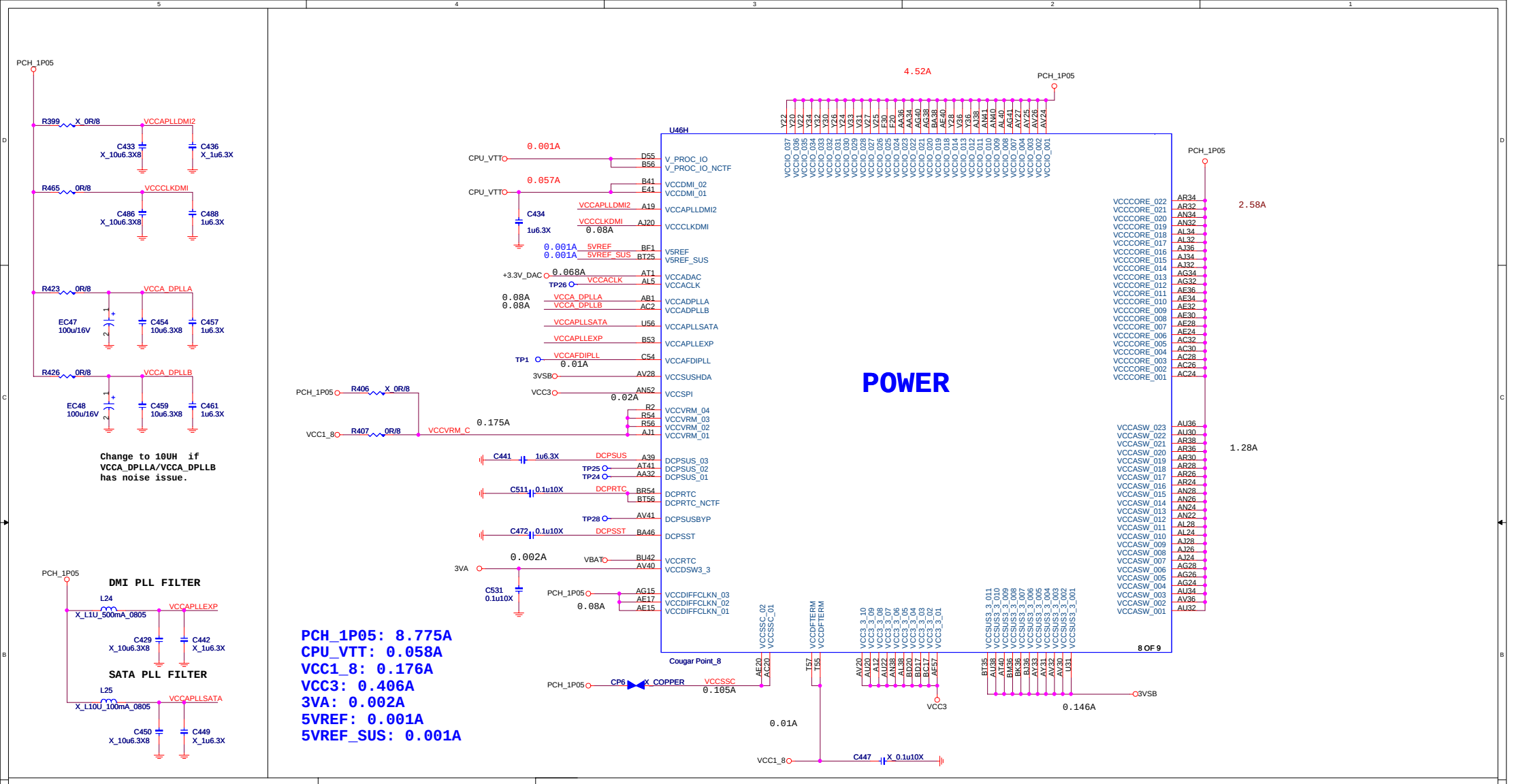
PCH_1P05
R399 X_0R/8
VCCAPLLDMI2
C433 X_10u6.3X8
C436 X_1u6.3X
R465 0R/8
VCCCLKDMI
C486 X_10u6.3X8
C488 1u6.3X
R423 0R/8
VCCA_DPLLA
EC47 100u/16V
C454 10u6.3X8
C457 1u6.3X
R426 0R/8
VCCA_DPLLB
EC48 100u/16V
C459 10u6.3X8
C461 1u6.3X
Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.
DMI PLL FILTER
L24
X_L1U_500mA_0805
VCCAPLLEXP
C429 X_10u6.3X8
C442 X_1u6.3X
SATA PLL FILTER
L25
X_L10U_100mA_0805
VCCAPLLSATA
C450 X_10u6.3X8
C449 X_1u6.3X
POWER
U46H
4.52A
0.001A
CPU_VTT
V_PROC_IO
V_PROC_IO_NCTF
0.057A
VCCDMI_02
VCCDMI_01
C434 1u6.3X
VCCAPLLDMI2
VCCCLKDMI
0.08A
0.001A 5VREF
0.001A 5VREF_SUS
V5REF
V5REF_SUS
+3.3V_DAC
0.068A
TP26
VCCACLK
VCCADAC
VCCACLK
0.08A
0.08A
VCCA_DPLLA
VCCA_DPLLB
VCCADPLLA
VCCADPLLB
VCCAPLLSATA
VCCAPLLEXP
TP1
VCCAFDIPLL
0.01A
VCCAFDIPLL
3VSB
VCCSUSHDA
VCC3
0.02A
VCCSPI
PCH_1P05
R406 X_0R/8
VCC1_8
R407 0R/8
VCCVRM_C
0.175A
VCCVRM_04
VCCVRM_03
VCCVRM_02
VCCVRM_01
C441 1u6.3X
DCPSUS
TP25
TP24
DCPSUS_03
DCPSUS_02
DCPSUS_01
C511 0.1u10X
DCPRTC
DCPRTC_NCTF
TP28
DCPSUSBYP
C472 0.1u10X
DCPSST
0.002A
VBAT
VCCRTC
VCCDSW3_3
3VA
C531 0.1u10X
PCH_1P05
0.08A
VCCDIFFCLKN_03
VCCDIFFCLKN_02
VCCDIFFCLKN_01
PCH_1P05: 8.775A
CPU_VTT: 0.058A
VCC1_8: 0.176A
VCC3: 0.406A
3VA: 0.002A
5VREF: 0.001A
5VREF_SUS: 0.001A
Cougar Point_8
8 OF 9
PCH_1P05
CP6 X_COPPER
VCCSSC
0.105A
0.01A
VCC1_8
C447 X_0.1u10X
VCC3
0.146A
3VSB
PCH_1P05
2.58A
1.28A
5VREF & 5VREF_SUS Sequencing Circuit
VCC3
Q55 2N3904
C489 1u6.3X
VCC5
R536 10R
5VREF
3VSB
Q57 2N3904
C519 0.1u10X
5VSB
R572 100R/1%
5VREF_SUS
CP3 X_COPPER
+3.3V_DAC
C469 0.1u10X
C493 10u6.3X8
C497 10u6.3X8
Near ball AF1
PCH decoupling cap
3VSB
PCH_1P05
VCC3
CPU_VTT
VBAT
MICRO-STAR INT'L CO.,LTD
MS-7751
Size Custom
Document Description PPT-POWER
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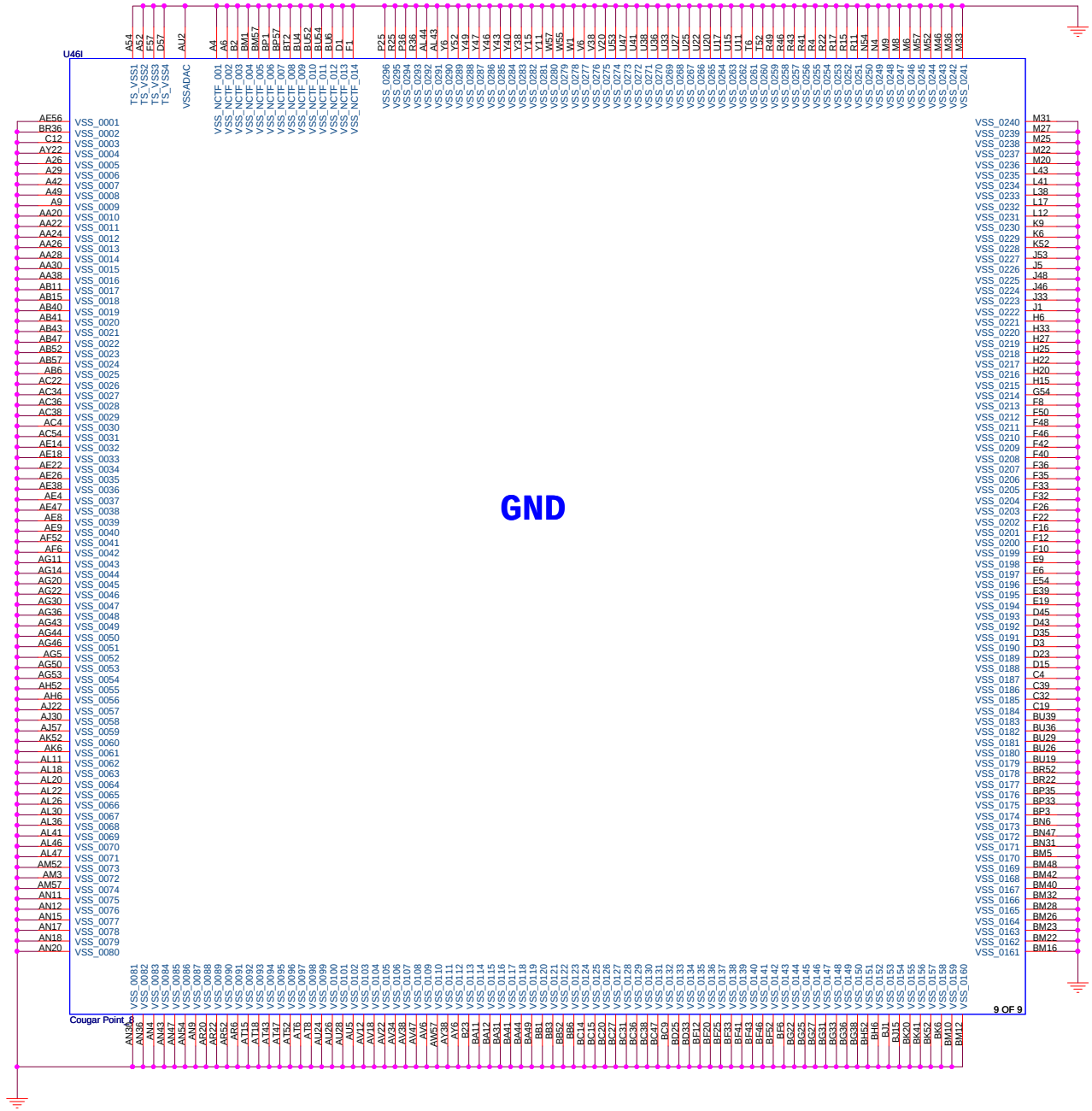
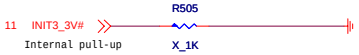


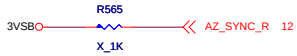
MICRO-STAR INT'L CO.,LTD	
MS-7751	
Size: Custom	Document Description: PPT-GND/NVRAM/USB30
Rev: 2.1	
Date: Monday, December 26, 2011	Sheet 14 of 51

PCH Straps

SPKR
0 : Default Mode:
1 : No Reboot Mode with TCO Disabled:



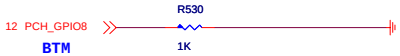
Do not pull low.



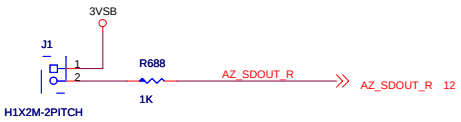
HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

Internal weak pull down. Do not pull up.

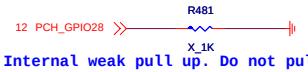
Enable TLS:GPIO15
Pull up with 1k Ohm to VccSus3.3.
Default (Disable TLS):
Leave NC. Internal pull down.



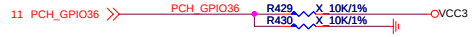
BTM
Leave floating. Do not pull low.
FCIM
Pull low with 1k Ohm to ground.
FCIM. Can be override by softstrap through ME.



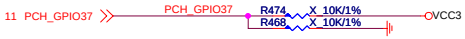
Default
Do not pull high.
Disable ME in Manufacturing Mode
Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.



Internal weak pull up. Do not pull low.
On die PLL voltage regulator

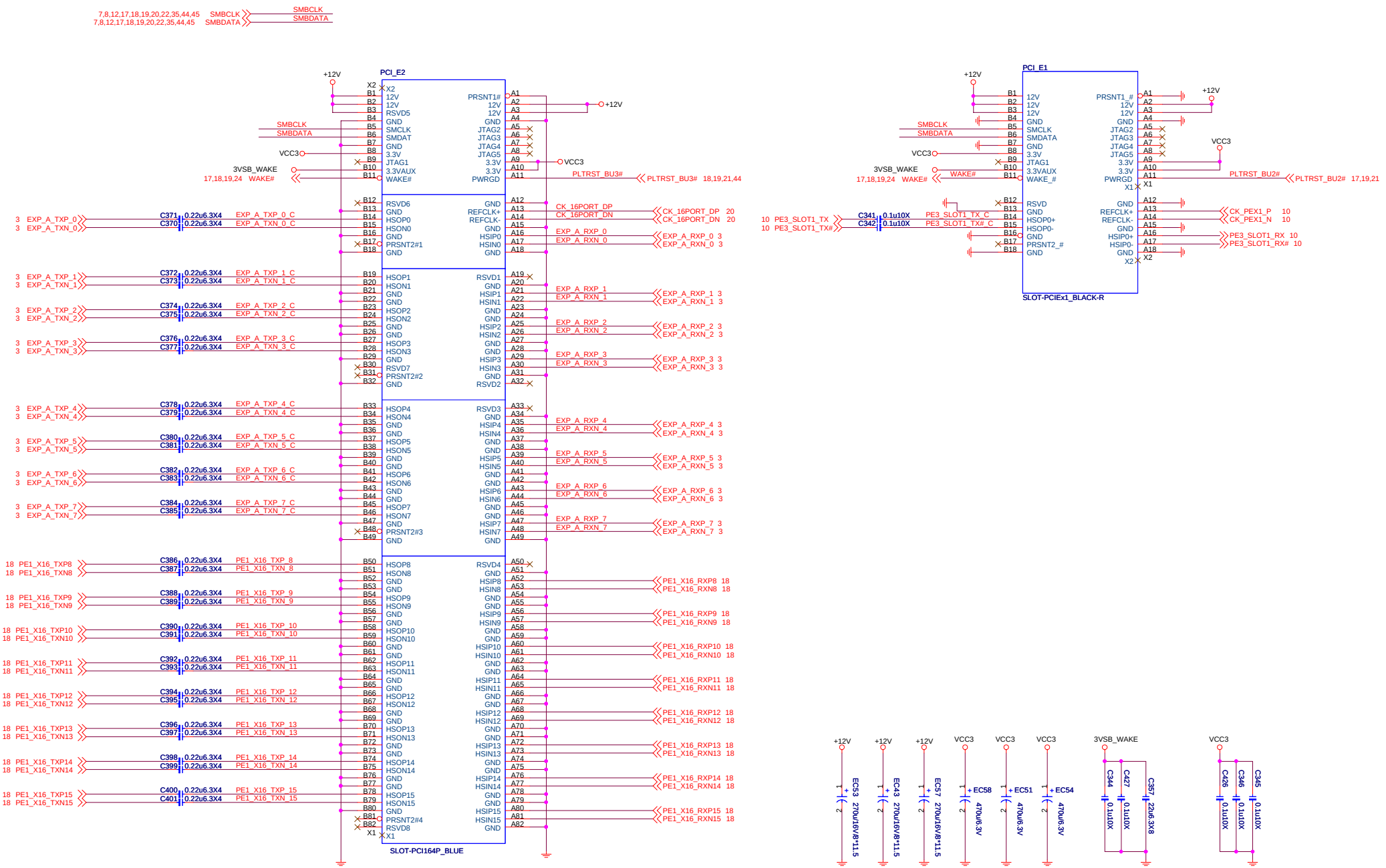


Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) – Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP – Use 8.2K-10K pull-down to ground.

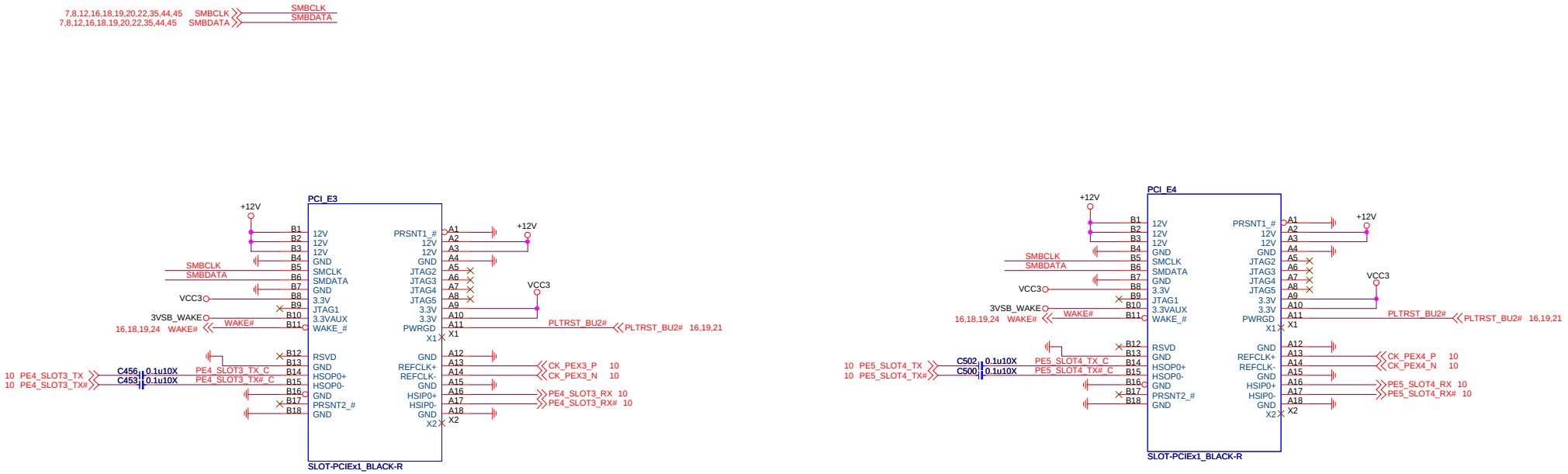


Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) – Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP – Use 8.2K-10K pull-down to ground.

MICRO-STAR INT'L CO.,LTD		
MS-7751		
Size: Custom	Document Description: PPT Strap	Rev: 2.1
Date: Monday, December 26, 2011	Sheet 15 of 51	



MICRO-STAR INT'L CO.,LTD		
MS-7751		
Size: Custom	Document Description: PCIE1(X1) & PCIE2(X16) Slots	Rev: 2.1
Date: Monday, December 26, 2011	Sheet 16 of 51	



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7751	
Size: Custom	Document Description: PCIE3(X1) & PCIE4(X1) Slots	Rev: 2.1
Date: Monday, December 26, 2011	Sheet 17 of 51	

PCI_Express X8 Slot
(Share with PCI_E x16 Slots)

7,8,12,16,17,19,20,22,35,44,45 SMBCLK
7,8,12,16,17,19,20,22,35,44,45 SMBDATA
SMBCLK
SMBDATA

Trace width > 200 mils

within 500mil

U34 U35 U36 U37 — PI3PCIE3415ZHE_TQFN42-RH

C348 C351 C352 C350 0.1u10X

C532 C533 C534 C535 C536 C537 C538 C539 C540 C541 C542 C543 C544 C545 C546 C547 C0.22u6.3X5

R584 4.7K

C349 C354 0.1u10X

PCI_E5 — SLOT-PCI164P_BLUE

MICRO-STAR INT'L CO.,LTD	
MS-7751	
Size: Custom	Document Description: PCIE5(X4)/Pericom switch
Rev: 2.1	
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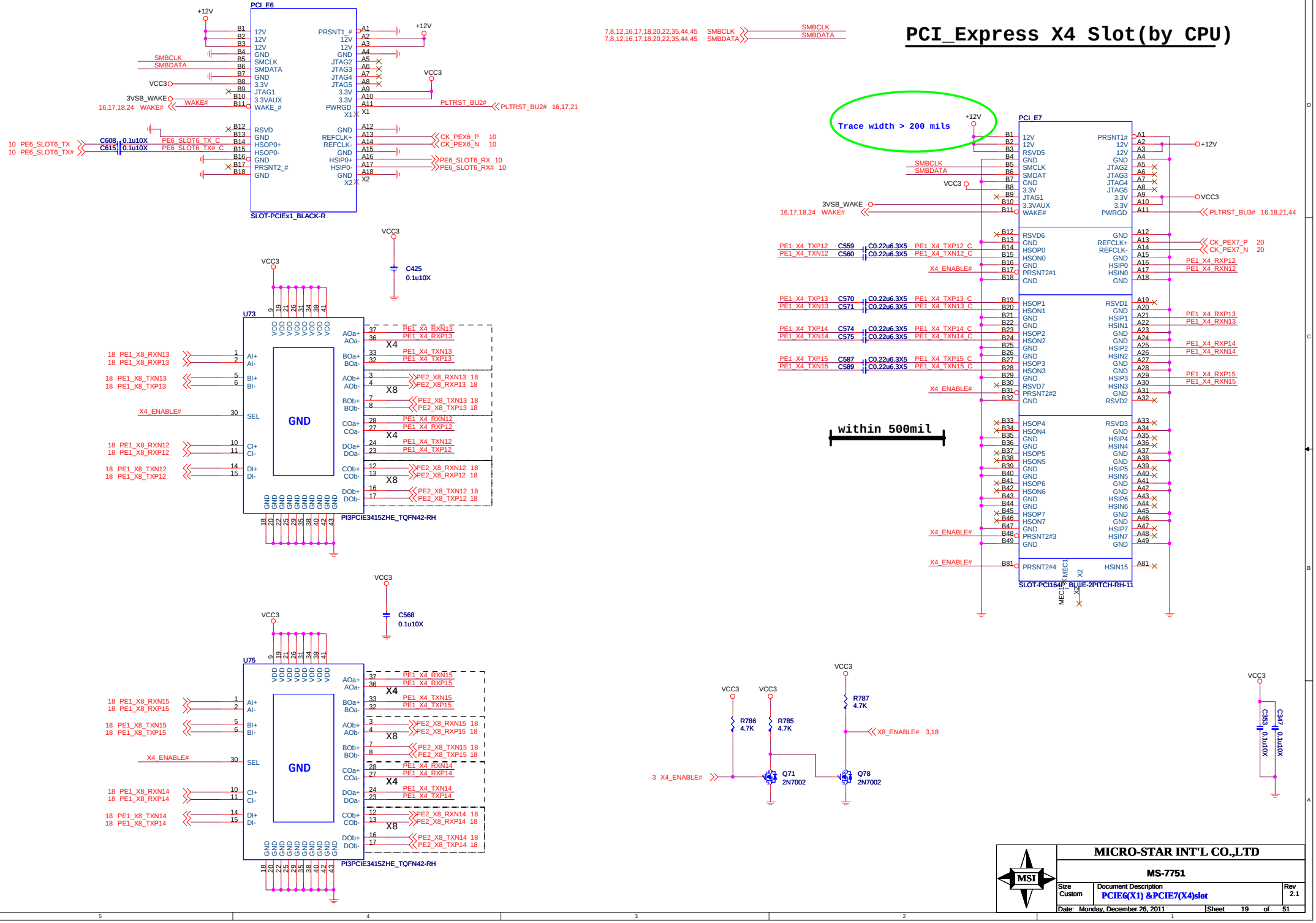
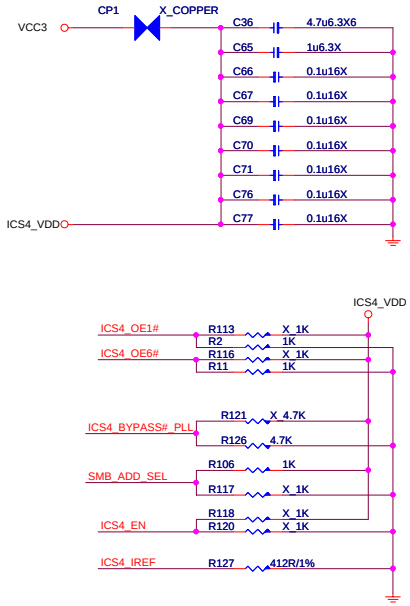
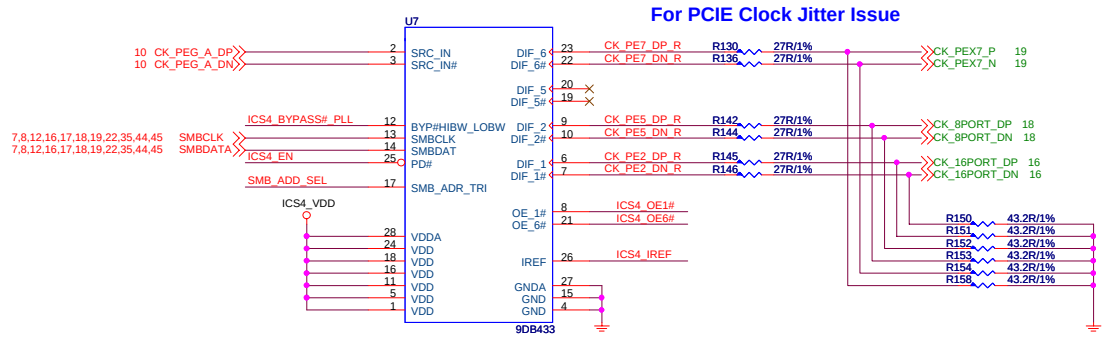
PCI_Express X4 Slot(by CPU)



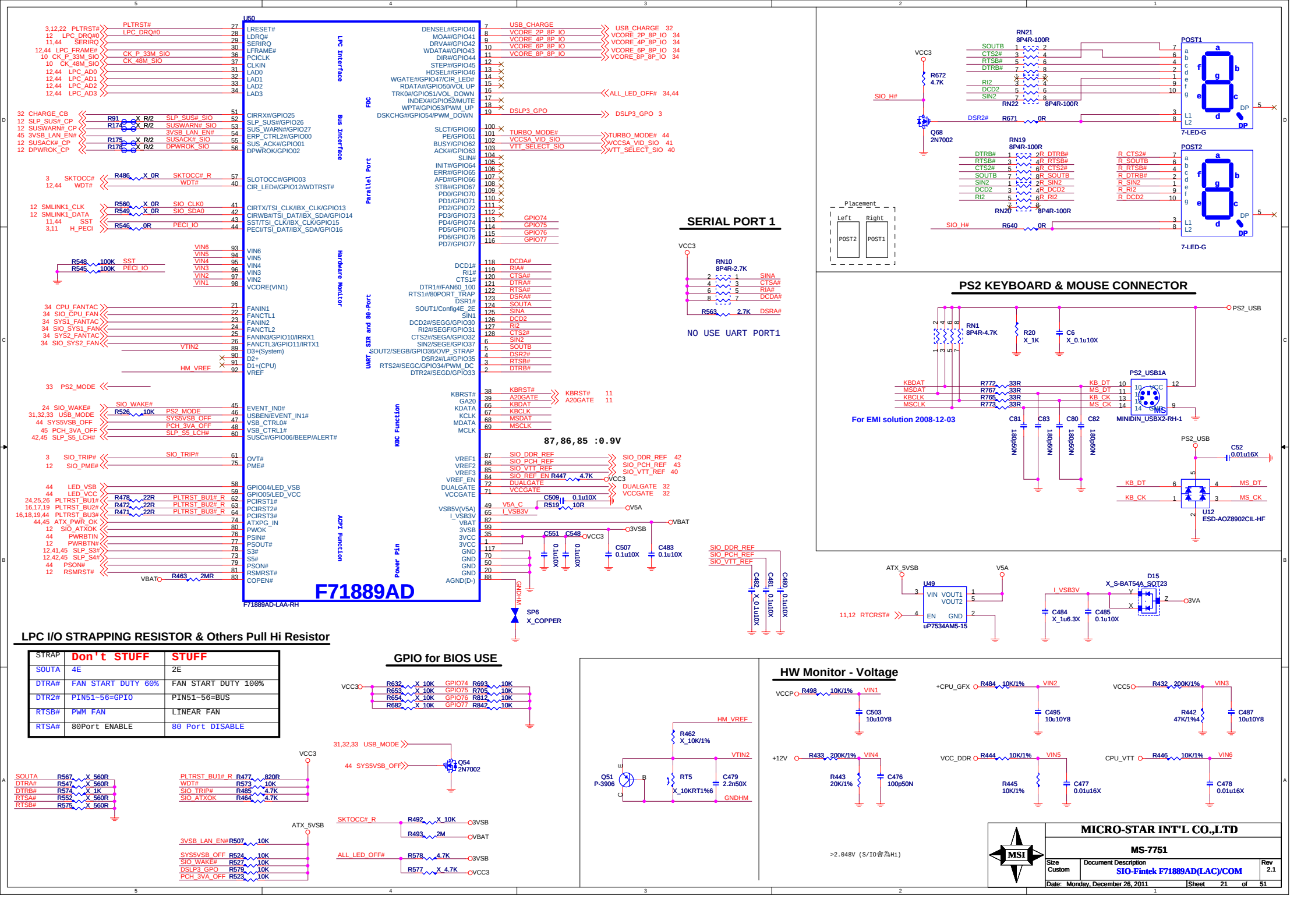
MICRO-STAR INT'L CO.,LTD	
MS-7751	
Size: Custom	Document Description: PCIE6(X1) &PCIE7(X4)slot
Rev: 2.1	
Date: Monday, December 26, 2011	Sheet 19 of 51





Address: D8/D9

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7751	
Size: Custom	Document Description: Clock Buffer 403D	Rev: 2.1
Date: Monday, December 26, 2011	Sheet 20 of 51	



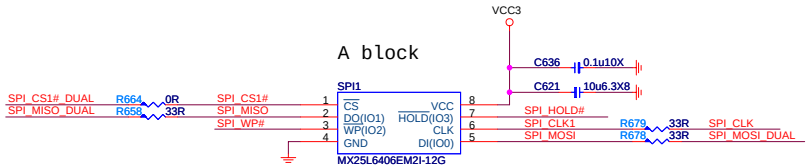
STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
DTR2#	PIN51~56=GPIO	PIN51~56=BUS
RTSB#	PWM FAN	LINEAR FAN
RTSA#	80Port ENABLE	80 Port DISABLE

SPI FLASH ROM

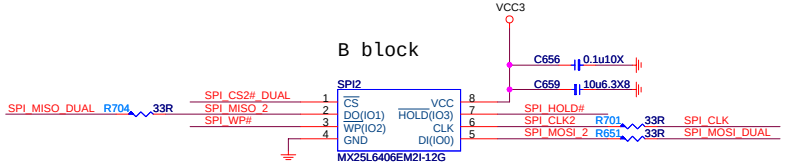
Place close to SB.

*SPI_CLK & SPI_MOSI must be length matched to within 500mils.
*SPI_CLK & SPI_CS0# must be length matched to within 500mils.

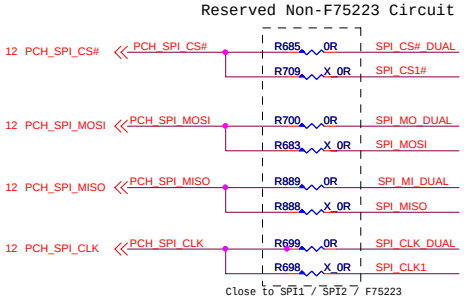
A block

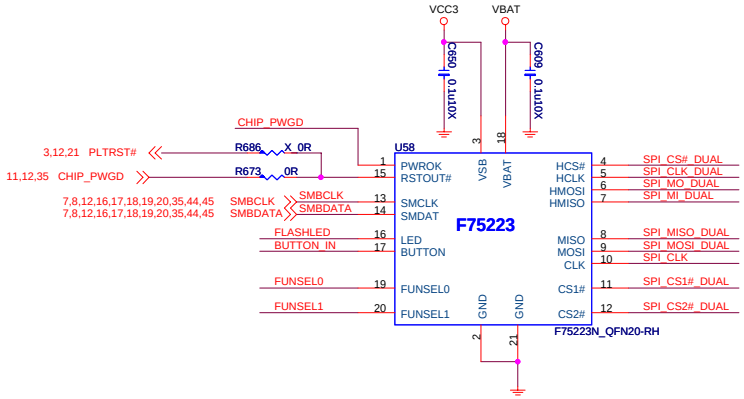


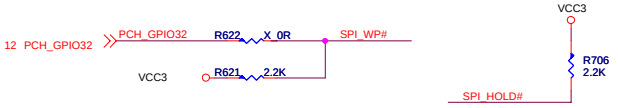
B block



Reserved Non-F75223 Circuit

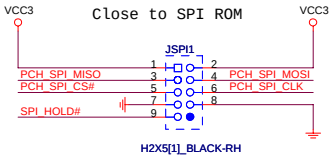






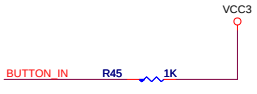
SPI DEBUG PROT

Close to SPI ROM



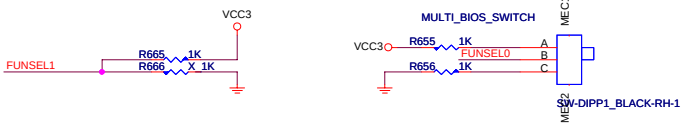
LED Status	Description
* Tri-state	Current block is A
Sink low	Current block is B
1 Hz pulse	Refreshing from A to B
10 Hz pulse	Refreshing from B to A

Part Number:N31-2051451-H06

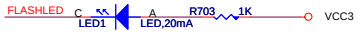


BUTTON_IN

SMBUS ADDRESS	
* Pull high 1K	0X96
Pull high 100K	0X58



FUNSEL[1:0]	Description
* 1 1	Auto Mode, using Block A flash as primary BIOS storage device. When an error occurs, it will automaticaly switch the flash from Block A to Block B.
1 0	Auto Mode, using Block B flash as primary BIOS storage device. When an error occurs, it will automaticaly switch the flash from Block B to Block A.
0 1	Manual select Block A flash. It won't switch to block B under any circumstance.
0 0	Manual select Block A flash. It won't switch to block B under any circumstance.



LED Status	Description
* Tri-state	Current block is A
Sink low	Current block is B
1 Hz pulse	Refreshing from A to B
10 Hz pulse	Refreshing from B to A

MICRO-STAR INT'L CO.,LTD

MS-7751

Size	Document Description	Rev
Custom	MULTI BIOS	2.1

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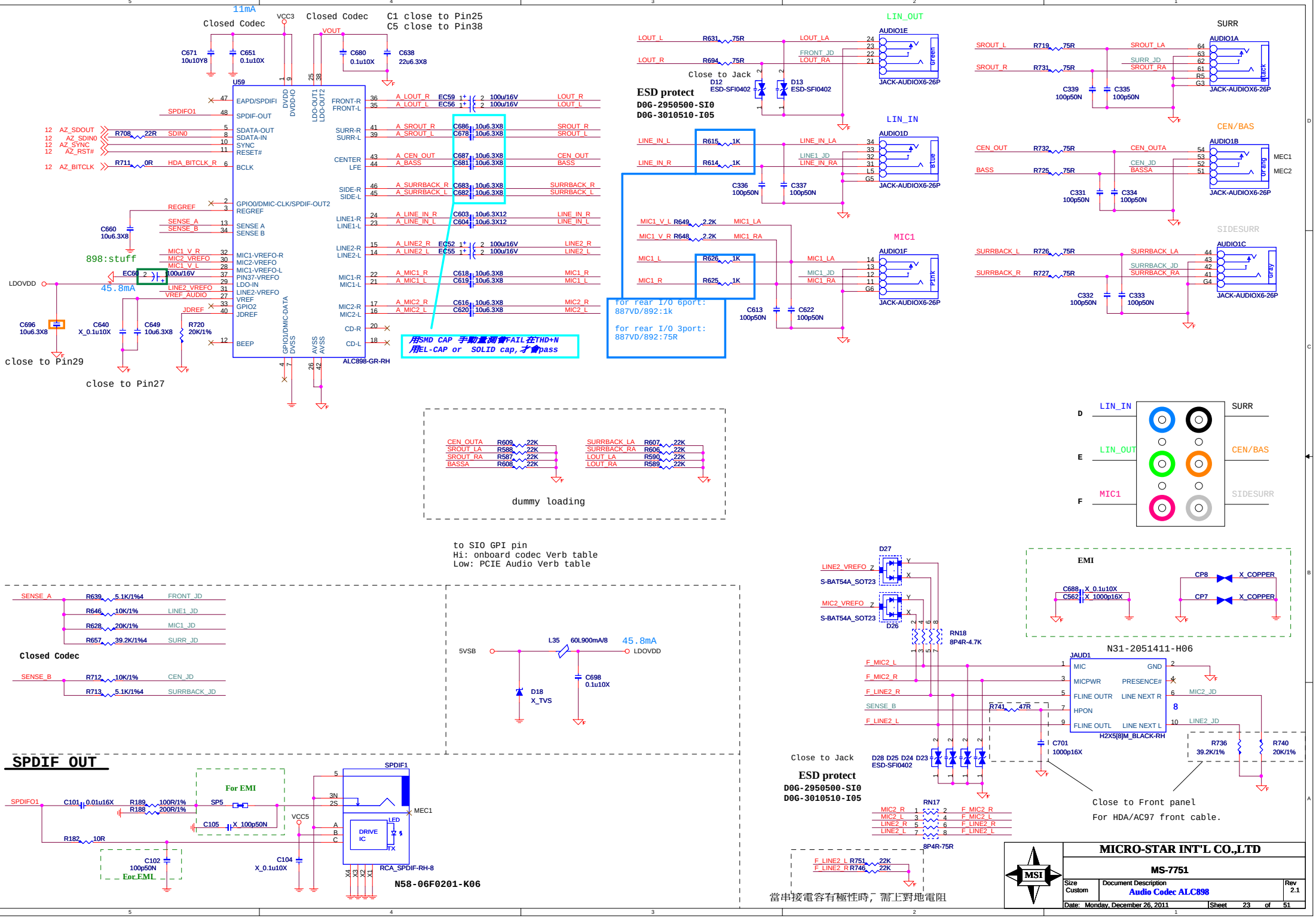
11mA
Closed Codec
VCC3
Closed Codec
C1 close to Pin25
C5 close to Pin38
VOUT
C671 10u10Y8
C651 0.1u10X
C680 0.1u10X
C638 22u6.3X8
U59
ALC898-GR-RH
EAPD/SPDIFI
SPDIF-OUT
SDATA-OUT
SDATA-IN
SYNC
RESET#
BCLK
GPIO0/DMIC-CLK/SPDIF-OUT2
REGREF
SENSE A
SENSE B
MIC1-VREFO-R
MIC2-VREFO
MIC1-VREFO-L
PIN37-VREFO
LDO-IN
LINE2-VREFO
VREF
GPIO2
JDREF
BEEP
FRONT-R
FRONT-L
SURR-R
SURR-L
CENTER
LFE
SIDE-R
SIDE-L
LINE1-R
LINE1-L
LINE2-R
LINE2-L
MIC1-R
MIC1-L
MIC2-R
MIC2-L
CD-R
CD-L
SPDIFO1
AZ_SDOUT
AZ_SDIN0
AZ_SYNC
AZ_RST#
AZ_BITCLK
R708 22R
R711 0R
HDA_BITCLK_R
SDIN0
REGREF
SENSE_A
SENSE_B
MIC1_V_R
MIC2_VREFO
MIC1_V_L
LINE2_VREFO
VREF_AUDIO
JDREF
C660 10u6.3X8
898:stuff
EC60 100u/16V
45.8mA
LDOVDD
C696 10u6.3X8
C640 X_0.1u10X
C649 10u6.3X8
R720 20K/1%
close to Pin29
close to Pin27
A_LOUT_R EC59 100u/16V LOUT_R
A_LOUT_L EC56 100u/16V LOUT_L
A_SROUT_R C686 10u6.3X8 SROUT_R
A_SROUT_L C678 10u6.3X8 SROUT_L
A_CEN_OUT C687 10u6.3X8 CEN_OUT
A_BASS C681 10u6.3X8 BASS
A_SURRBACK_R C683 10u6.3X8 SURRBACK_R
A_SURRBACK_L C682 10u6.3X8 SURRBACK_L
A_LINE_IN_R C603 10u6.3X12 LINE_IN_R
A_LINE_IN_L C604 10u6.3X12 LINE_IN_L
A_LINE2_R EC52 100u/16V LINE2_R
A_LINE2_L EC55 100u/16V LINE2_L
A_MIC1_R C618 10u6.3X8 MIC1_R
A_MIC1_L C619 10u6.3X8 MIC1_L
A_MIC2_R C616 10u6.3X8 MIC2_R
A_MIC2_L C620 10u6.3X8 MIC2_L
用SMD CAP 手動量測會FAIL在THD+N
用EL-CAP or SOLID cap,才會pass
LIN_OUT
LOUT_L R631 75R LOUT_LA
LOUT_R R694 75R LOUT_RA
FRONT_JD
Close to Jack
ESD protect
D0G-2950500-SI0
D0G-3010510-I05
D12 ESD-SFI0402
D13 ESD-SFI0402
AUDIO1E
JACK-AUDIOX6-26P
LIN_IN
LINE_IN_L R615 1K LINE_IN_LA
LINE_IN_R R614 1K LINE1_JD
C336 100p50N
C337 100p50N
AUDIO1D
MIC1
MIC1_V_L R649 2.2K MIC1_LA
MIC1_V_R R648 2.2K MIC1_RA
MIC1_L R626 1K MIC1_JD
MIC1_R R625 1K
C613 100p50N
C622 100p50N
AUDIO1F
for rear I/O 6port:
887VD/892:1k
for rear I/O 3port:
887VD/892:75R
SURR
SROUT_L R719 75R SROUT_LA
SROUT_R R731 75R SURR_JD SROUT_RA
C339 100p50N
C335 100p50N
AUDIO1A
CEN/BAS
CEN_OUT R732 75R CEN_OUTA
BASS R725 75R CEN_JD BASSA
C331 100p50N
C334 100p50N
AUDIO1B
MEC1
MEC2
SIDESURR
SURRBACK_L R726 75R SURRBACK_LA
SURRBACK_R R727 75R SURRBACK_JD SURRBACK_RA
C332 100p50N
C333 100p50N
AUDIO1C
CEN_OUTA R609 22K
SROUT_LA R588 22K
SROUT_RA R587 22K
BASSA R608 22K
SURRBACK_LA R607 22K
SURRBACK_RA R606 22K
LOUT_LA R590 22K
LOUT_RA R589 22K
dummy loading
D
E
F
LIN_IN
LIN_OUT
MIC1
SURR
CEN/BAS
SIDESURR
to SIO GPI pin
Hi: onboard codec Verb table
Low: PCIE Audio Verb table
SENSE_A R639 5.1K/1%4 FRONT_JD
R646 10K/1% LINE1_JD
R628 20K/1% MIC1_JD
R657 39.2K/1%4 SURR_JD
Closed Codec
SENSE_B R712 10K/1% CEN_JD
R713 5.1K/1%4 SURRBACK_JD
5VSB
L35 60L900mA/8
45.8mA
LDOVDD
D18 X_TVS
C698 0.1u10X
D27
LINE2_VREFO
S-BAT54A_SOT23
MIC2_VREFO
D26
RN18 8P4R-4.7K
EMI
C688 X_0.1u10X
C562 X_1000p16X
CP8 X_COPPER
CP7 X_COPPER
N31-2051411-H06
JAUD1
MIC
GND
MICPWR
PRESENCE#
FLINE OUTR
LINE NEXT R
HPON
FLINE OUTL
LINE NEXT L
H2X5[8]M_BLACK-RH
F_MIC2_L
F_MIC2_R
F_LINE2_R
SENSE_B
F_LINE2_L
R741 47R
MIC2_JD
LINE2_JD
C701 1000p16X
R736 39.2K/1%
R740 20K/1%
Close to Jack
ESD protect
D0G-2950500-SI0
D0G-3010510-I05
D28 D25 D24 D23
ESD-SFI0402
RN17
8P4R-75R
Close to Front panel
For HDA/AC97 front cable.
F_LINE2_L R751 22K
F_LINE2_R R746 22K
當串接電容有極性時，需上對地電阻
SPDIF OUT
SPDIFO1
C101 0.01u16X
R189 100R/1%
R188 200R/1%
For EMI
SP5
C105 X_100p50N
R182 10R
C102 100p50N
For EMI
VCC5
C104 X_0.1u10X
SPDIF1
MEC1
DRIVE IC
LED
RCA_SPDIF-RH-8
N58-06F0201-K06
MICRO-STAR INT'L CO.,LTD
MS-7751
Size Custom
Document Description
Audio Codec ALC898
Rev 2.1
Date: Monday, December 26, 2011
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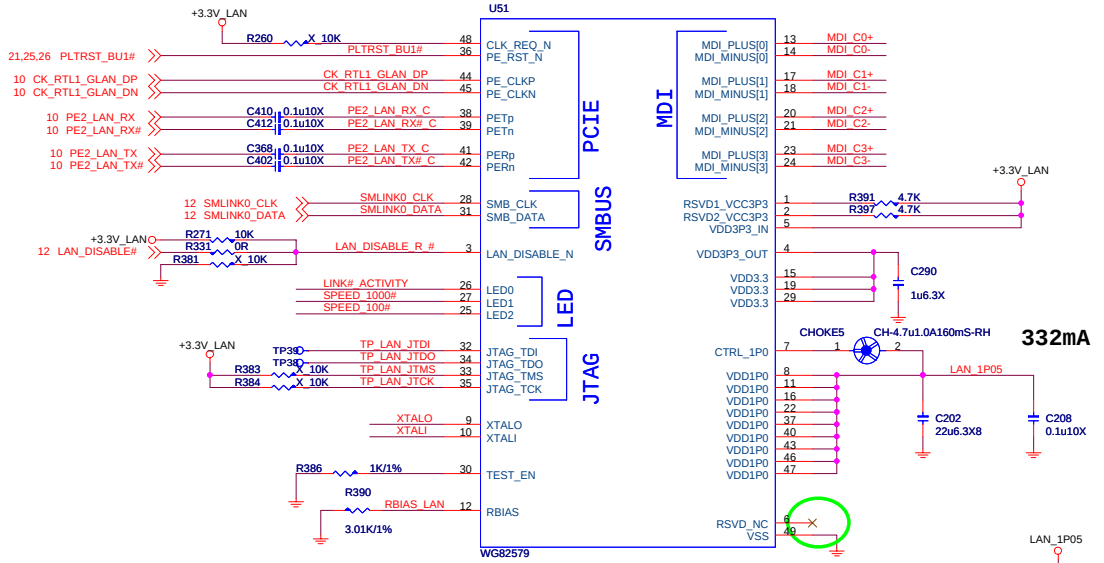
INTEL LAN 82579

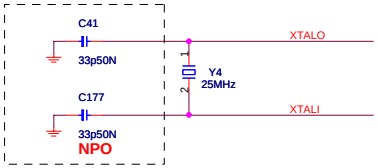
Vo = Vref (1+R2/R1) + Iadj x R2

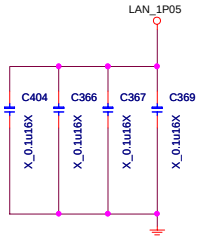
If CLK_REQ_N is connected to PCIECLKRQ[1:2]#,
the CLK_REQ_N pull-up resistor should be connected
to +V3.3s



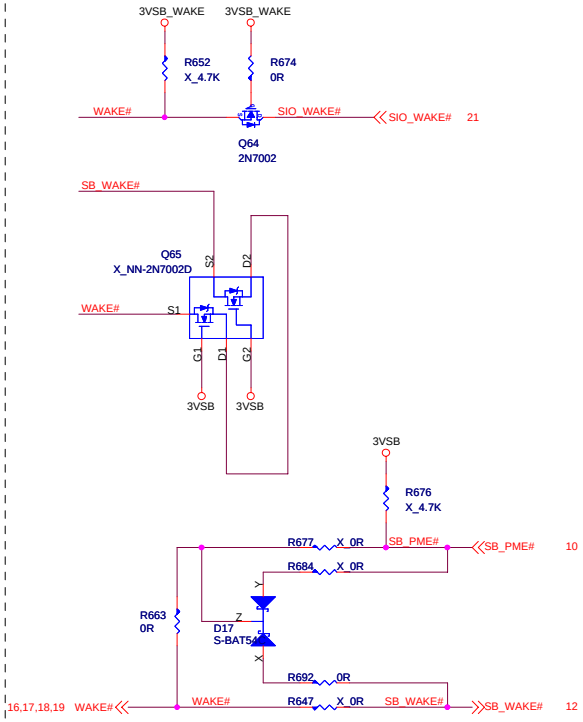
332mA

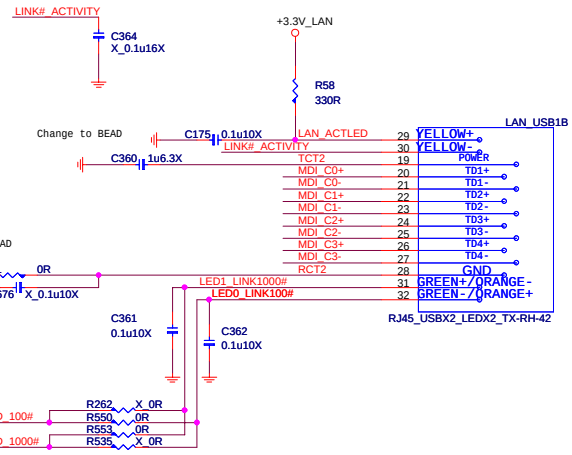
增加pPIN7 空間



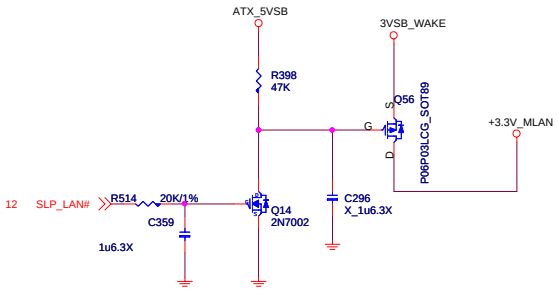


LAN/PCIE/PCI Wake Up CTRL Circuit

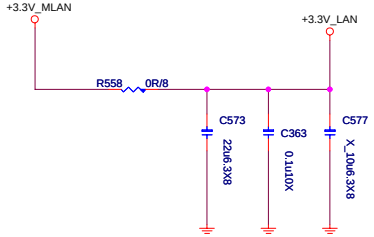




+3.3V_LAN



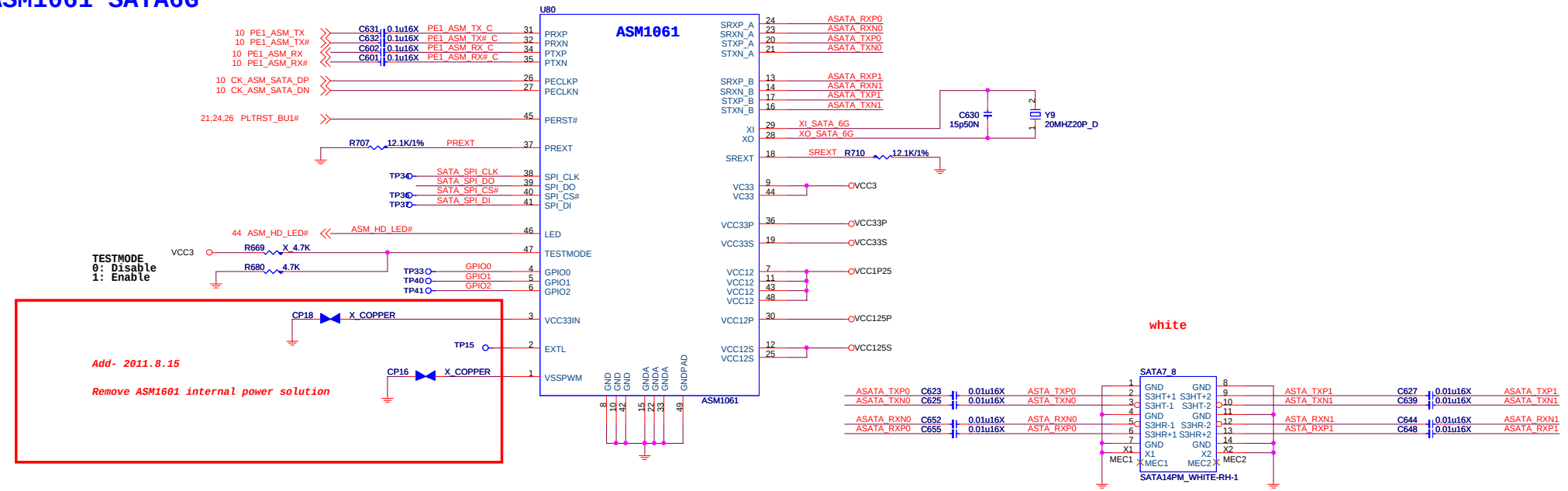
90mA

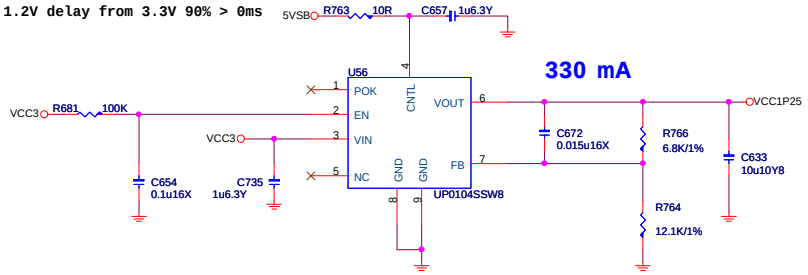


Note:These caps closed to PHY

MICRO-STAR INT'L CO.,LTD		
MS-7751		
Size: Custom	Document Description: LAN-RTL8111E	Rev: 2.1
Date: Monday, December 26, 2011	Sheet 24 of 51	

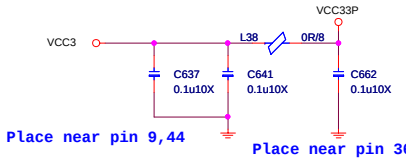
ASM1061 SATA6G

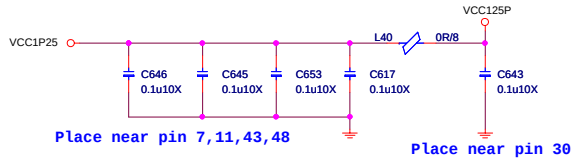


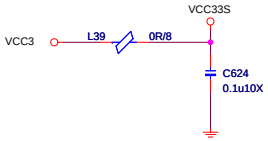


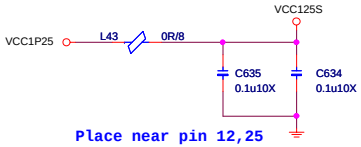
ASM1061 POWER Consumption

	3.3V	1.2V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47









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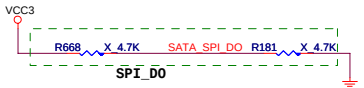

Add- 2011.3.18

SATA_SPI_DO don't need pull up (integrated pull-up)
or pull down for Asmedia recommendation.
Asmedia suggest that we use spinup by s/w mode for MB or PCI-E Card.

Add- 2011.8.15

If layout not enough space,you can take off EEPROM.

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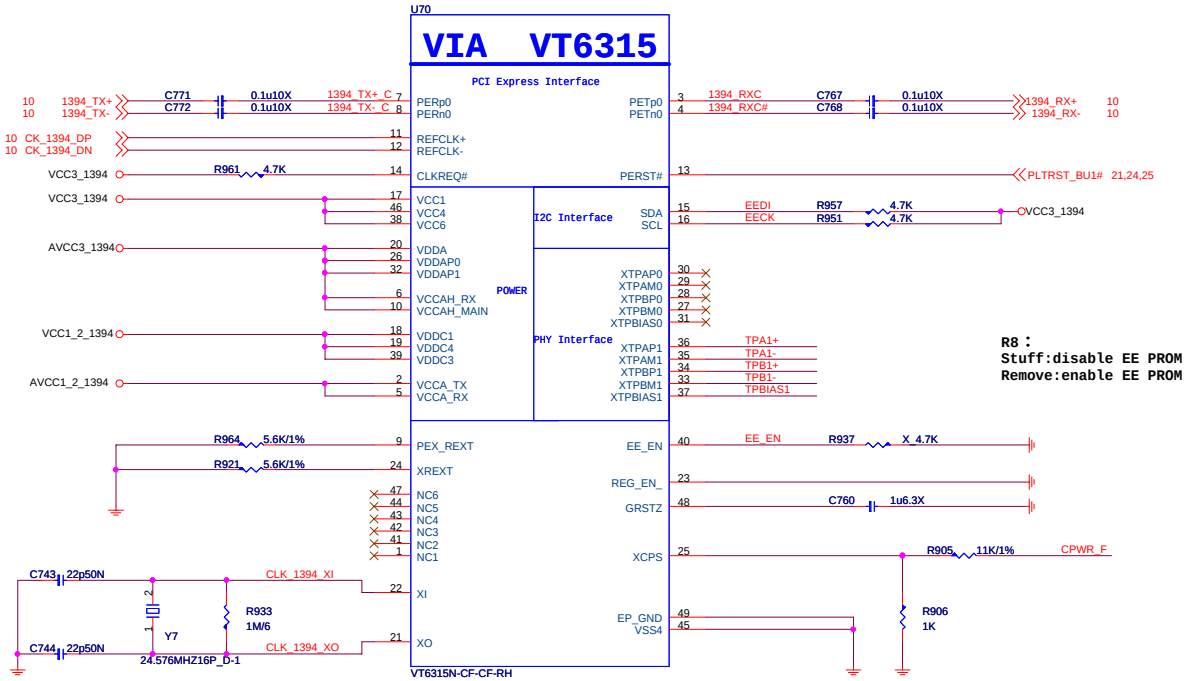
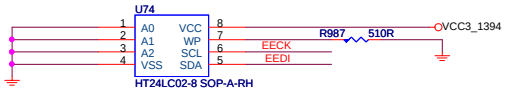
1394 CONTROLLER



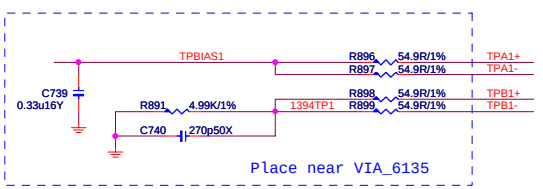
R8 :
Stuff:disable EE PROM
Remove:enable EE PROM

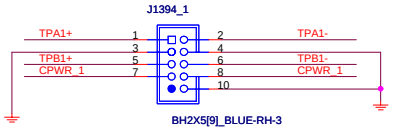
EE PROM



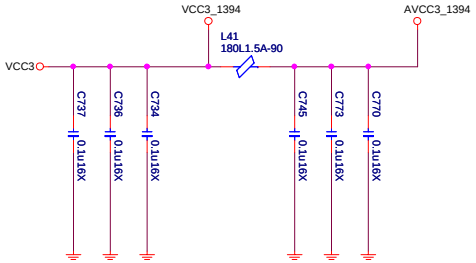
Rear 1394 port

Front 1394 pin header

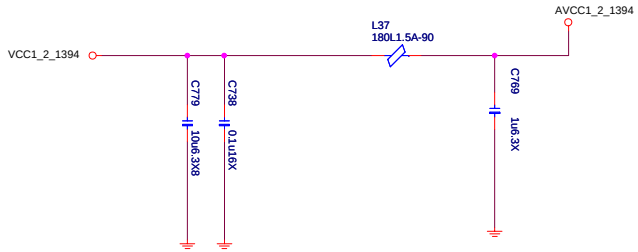


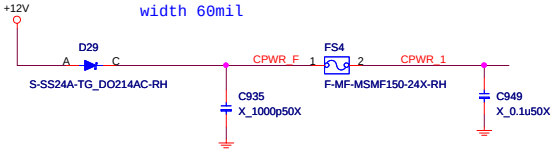


For Intel 1394 pinheader



close to chip of all Cap.





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	MS-7751	
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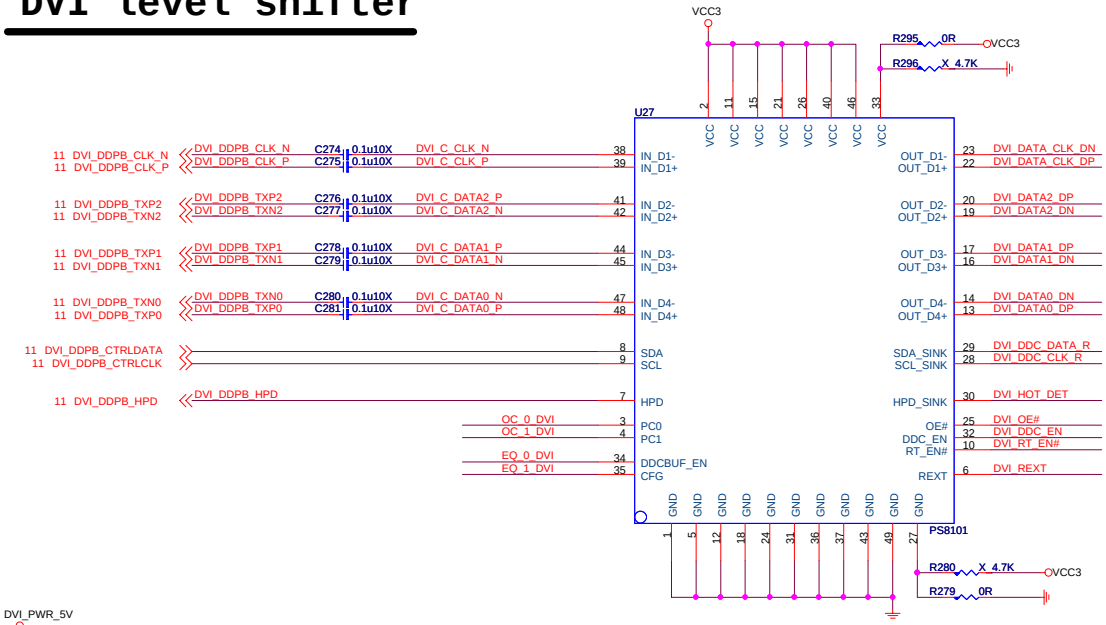
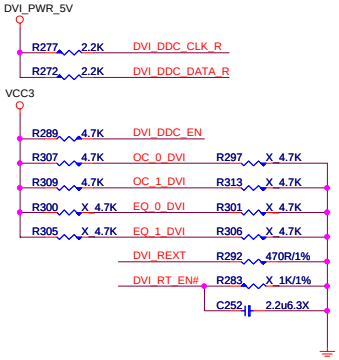
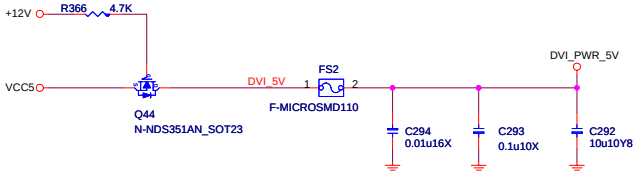
DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



PERICOM料號:B0B-411LS2C-P22.
PARADE料號:B0B-081010C-P97.



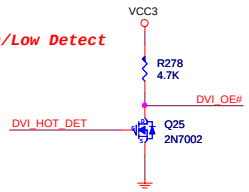


	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

注意High/Low Detect



EMI

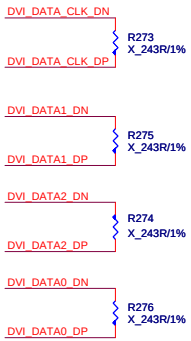
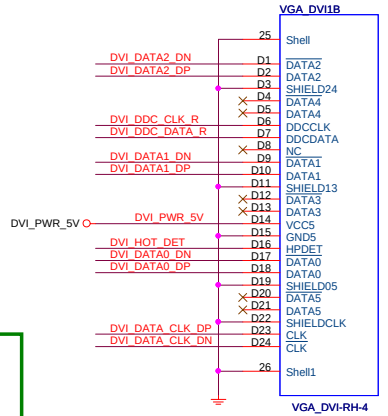
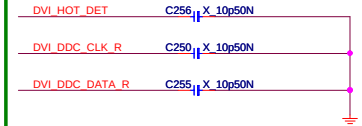
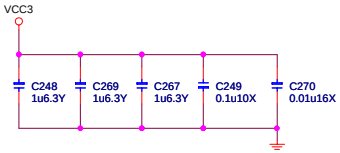


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings			
Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	



EMI cap.





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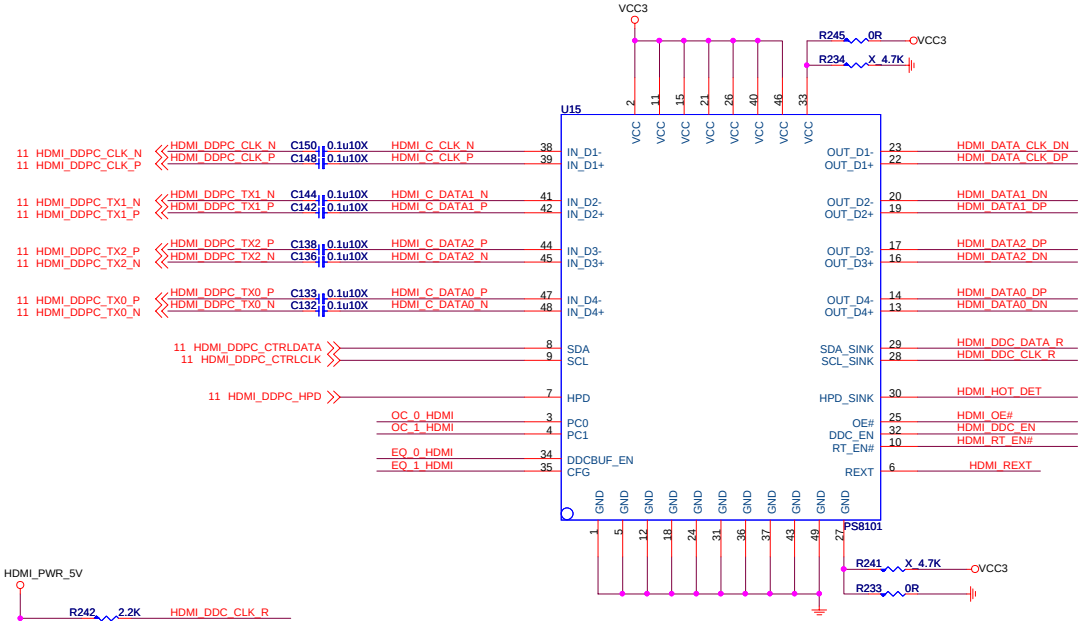
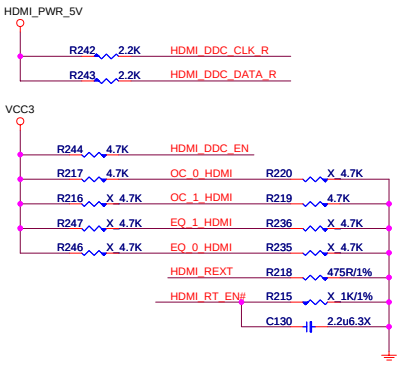
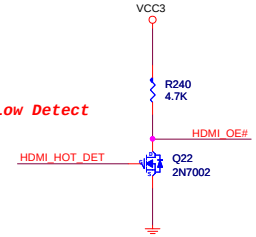
HDMI level shifter





注意High/Low Detect



	"0"	"1"	note
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DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

EMI

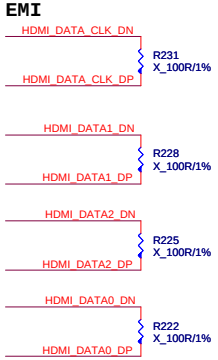

Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
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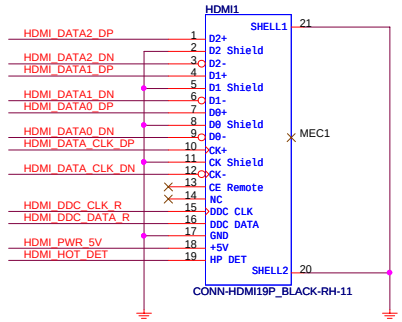
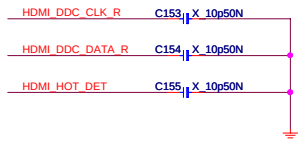
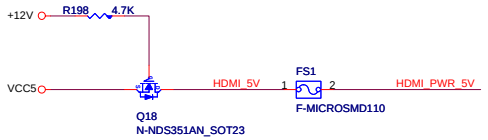
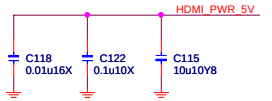
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	

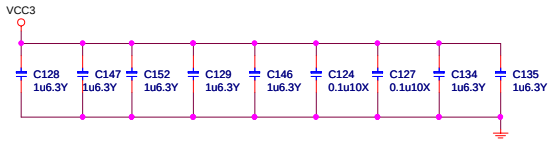


EMI cap.









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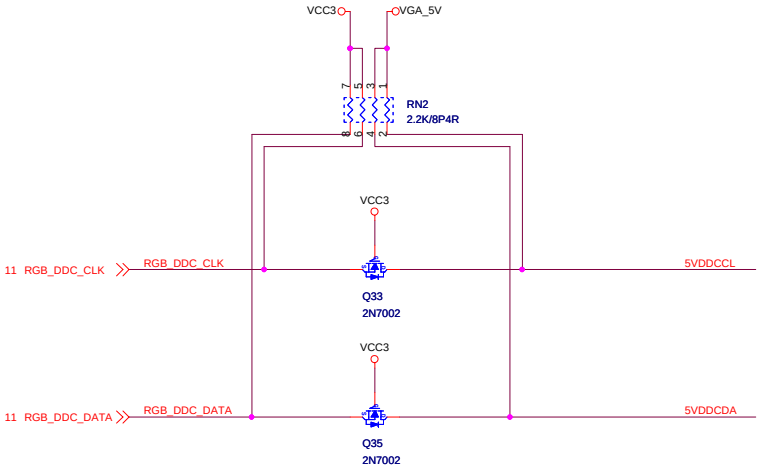
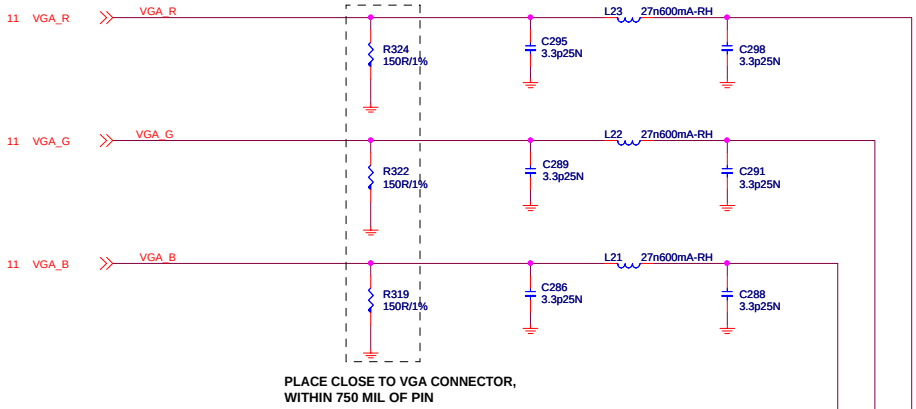
D-Sub

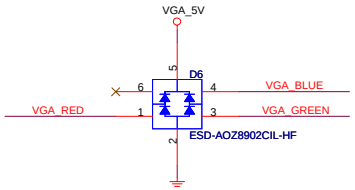
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

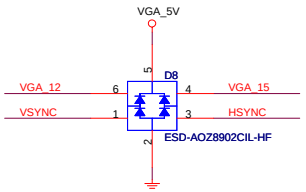
Level shift

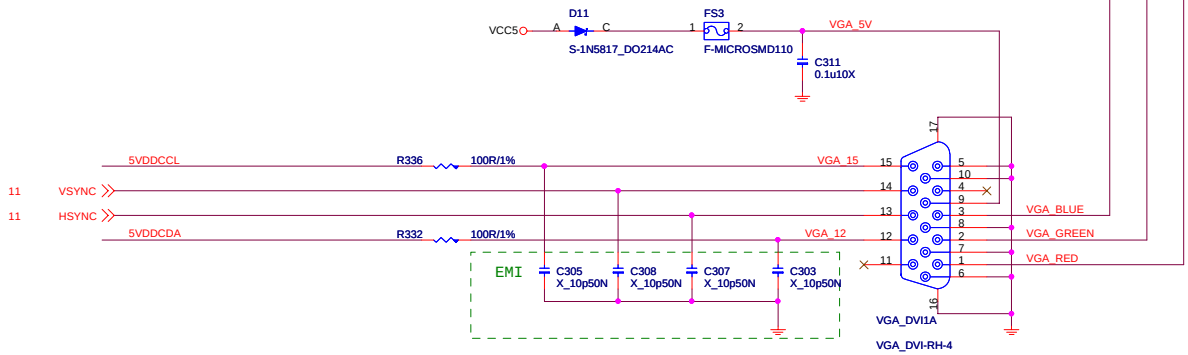




PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN







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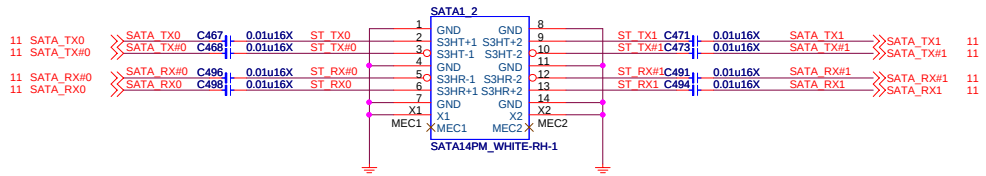
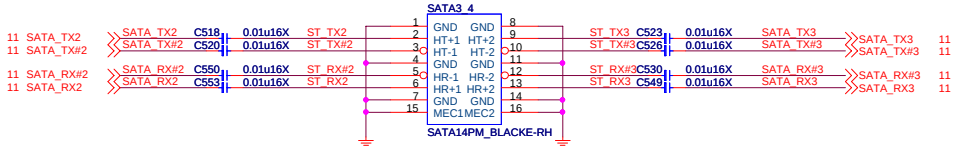
SATA1-2

3.0

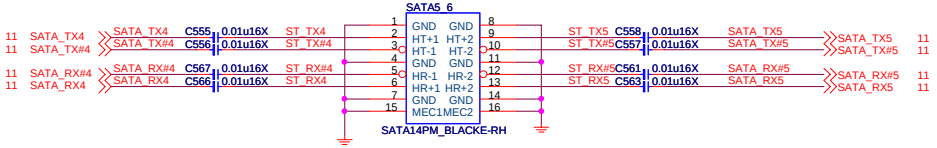
white



SATA3-4



SATA5-6



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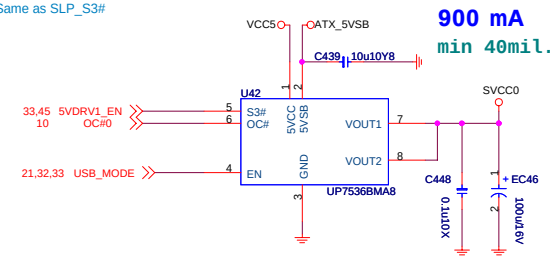
FRONT USB30 PORT 0,1

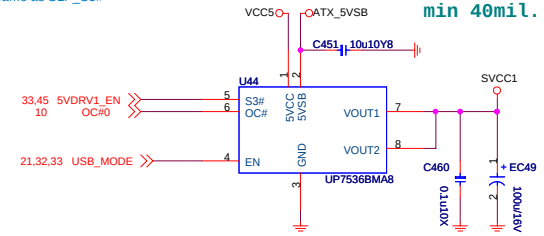
Same as SLP_S3#

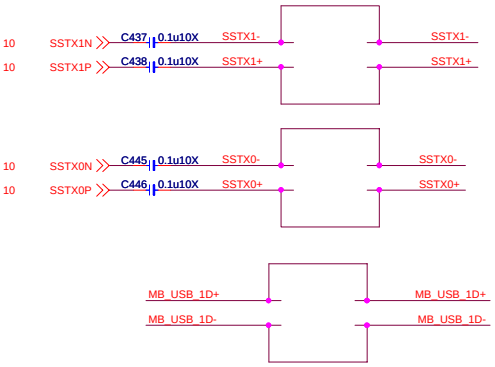
900 mA
min 40mil.

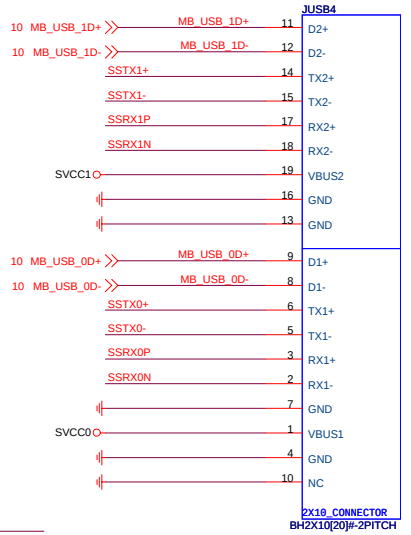


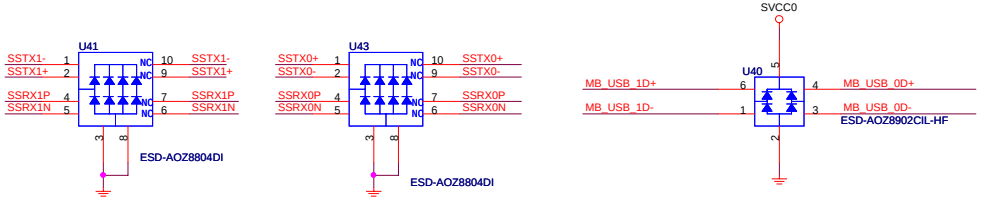
Same as SLP_S3#

900 mA
min 40mil.





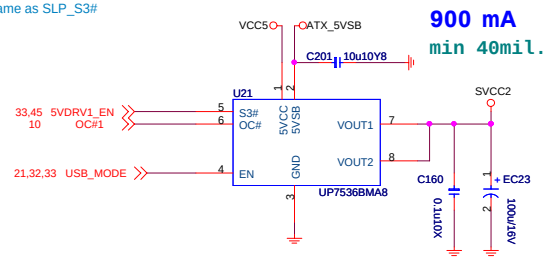




REAR USB30 PORT 2,3

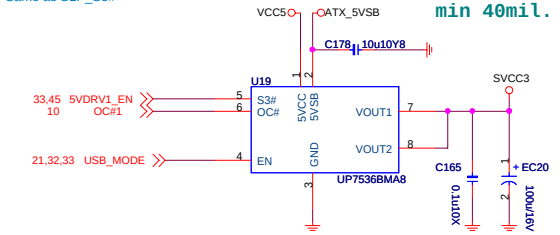
Same as SLP_S3#

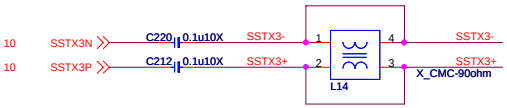
900 mA
min 40mil.

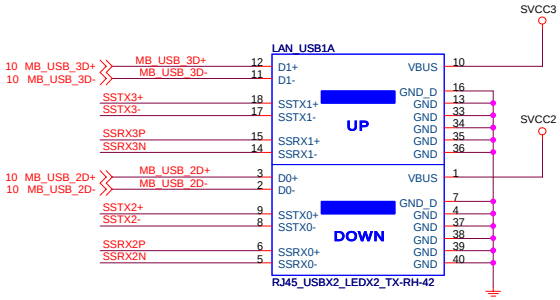


Same as SLP_S3#

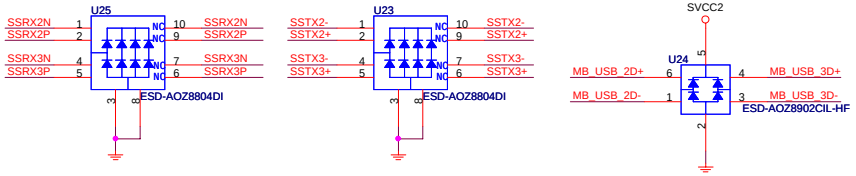
900 mA
min 40mil.







EMI



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MS-7751		
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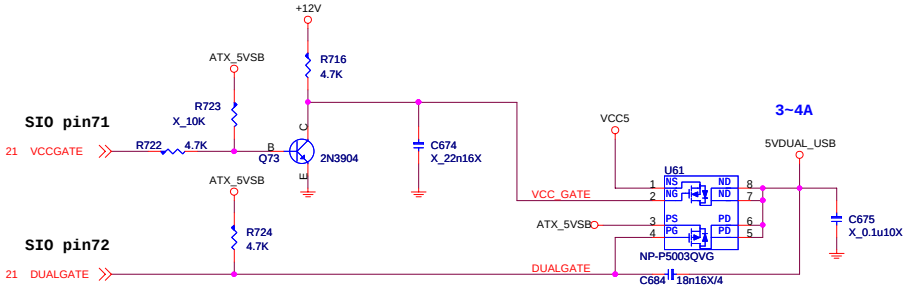
5VDUAL_USB



SIO GPIO40 Pin7 (I_VSB3V)

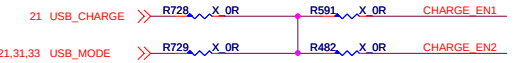
Pin power : I_3VSB or VBAT
Register power : I_3VSB or VBAT
Register reset : I_3VSB or VBAT

USB_CHARGE: (OD)
0: Don't support USB charge and resume.
1: Support USB charge and resume.

1st boot ,H/W default support USB charge.

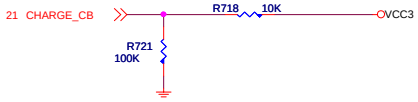
Update- 2010.7.15

SIO GPIO40



Pin power : I_3VSB
Register power : I_3VSB
Register reset : I_3VSB

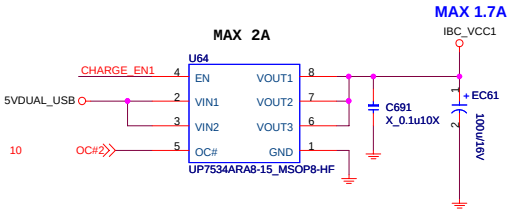
SIO GPIO25

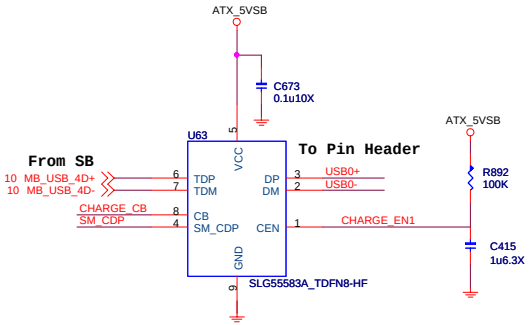


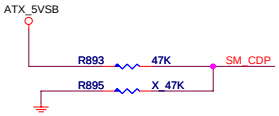
USB POWER PORT 0 For USB Charging

MAX 1.7A

MAX 2A



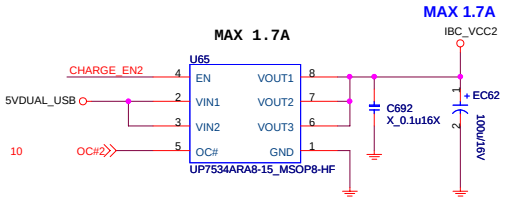


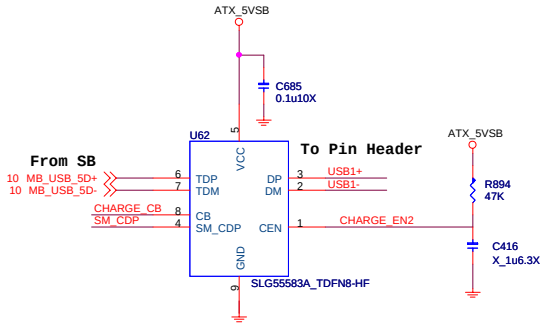


USB POWER PORT 1 For USB Charging

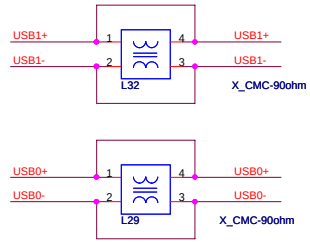
MAX 1.7A

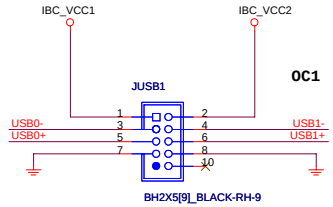
MAX 1.7A



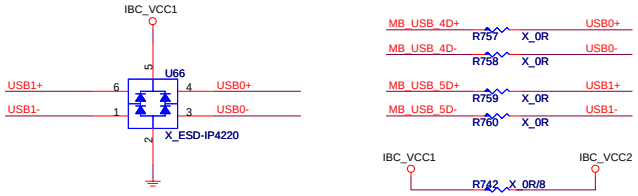


FRONT USB PORT 0,1





COLAY remove USB charger ic



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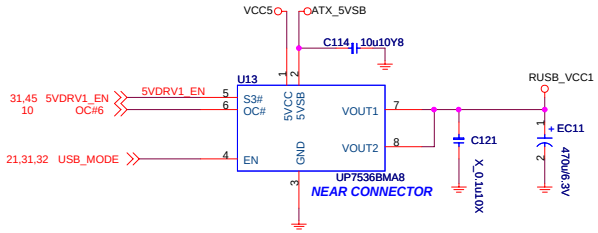
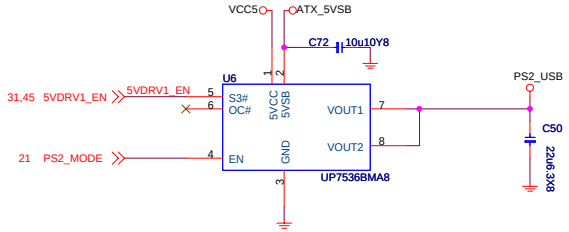
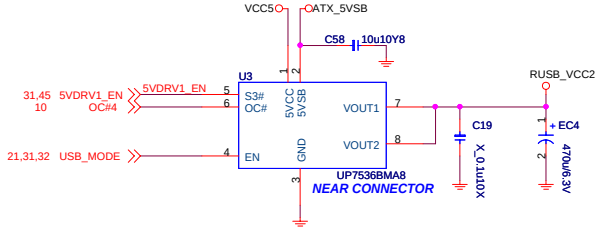
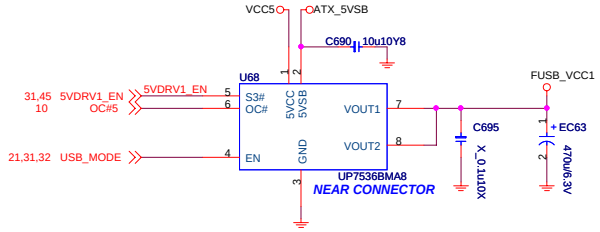
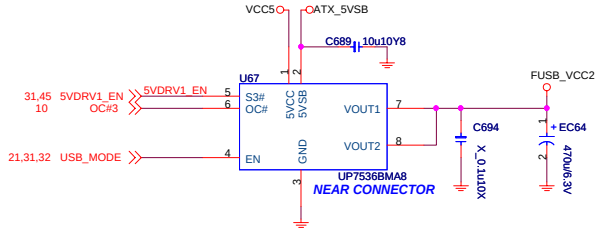
Rear USB Connector



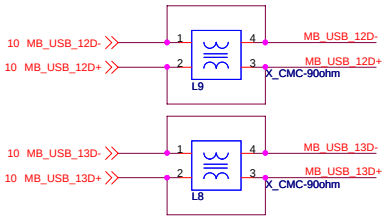


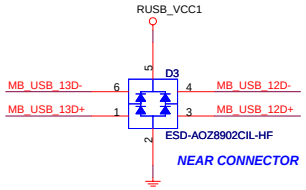


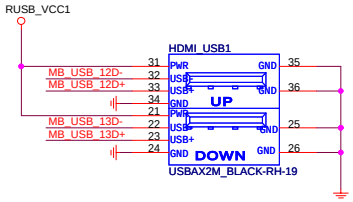




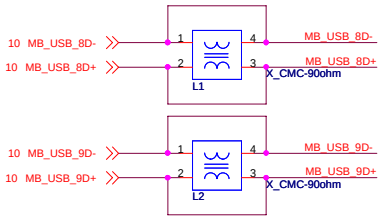
REAR USB PORT 8,9 (With PS2)

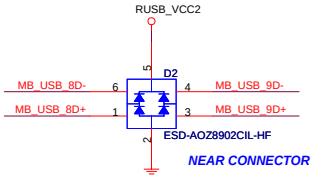


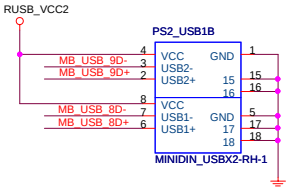




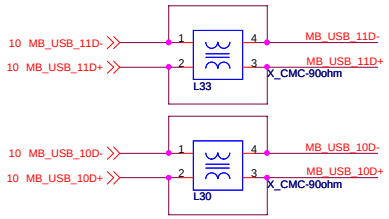
REAR USB PORT 8,9 (With PS2)

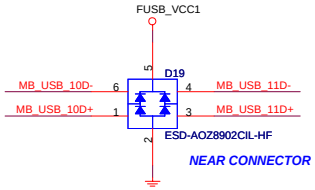


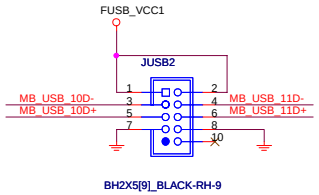




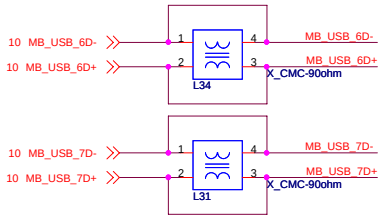
FRONT USB PORT 8,9

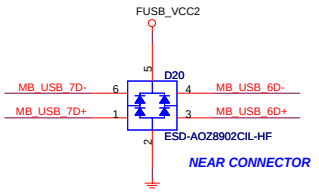


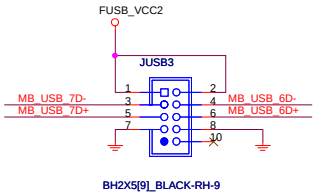




FRONT USB PORT 10.11







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MS-7751		
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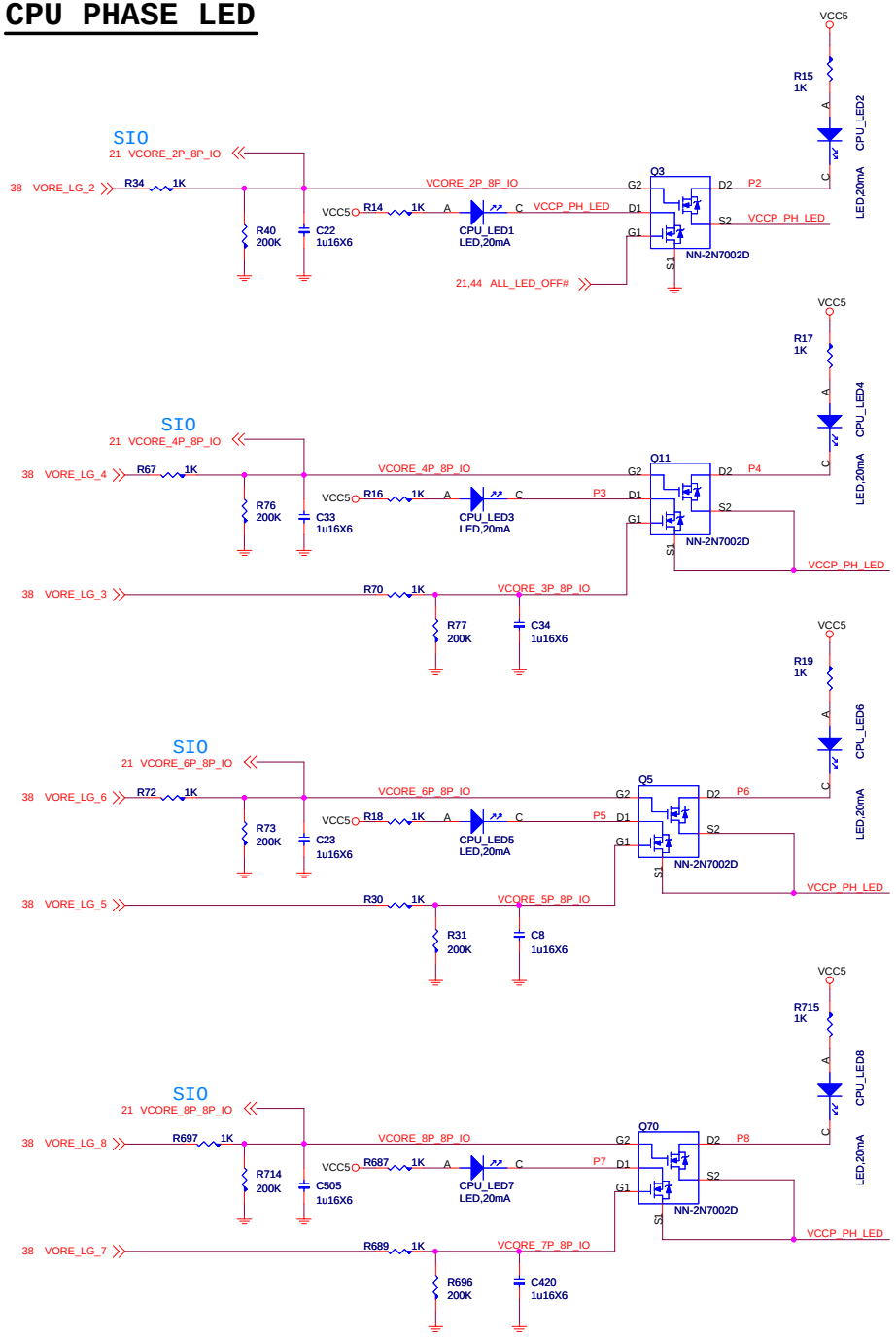
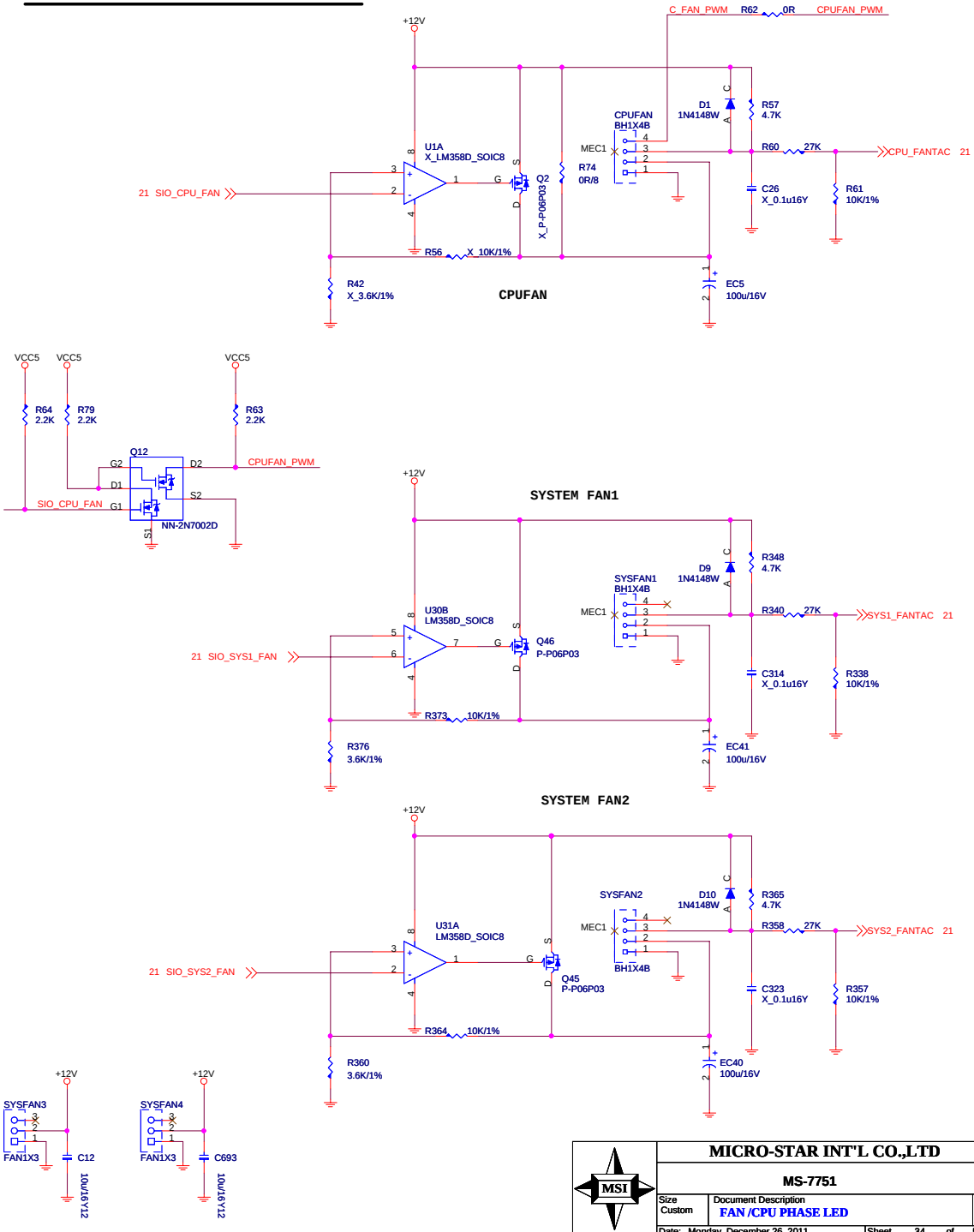
CPU PHASE LED



FAN-COUNTROL CIRCUIT



MICRO-STAR INT'L CO.,LTD		
MS-7751		
Size: Custom	Document Description: FAN /CPU PHASE LED	Rev: 2.1
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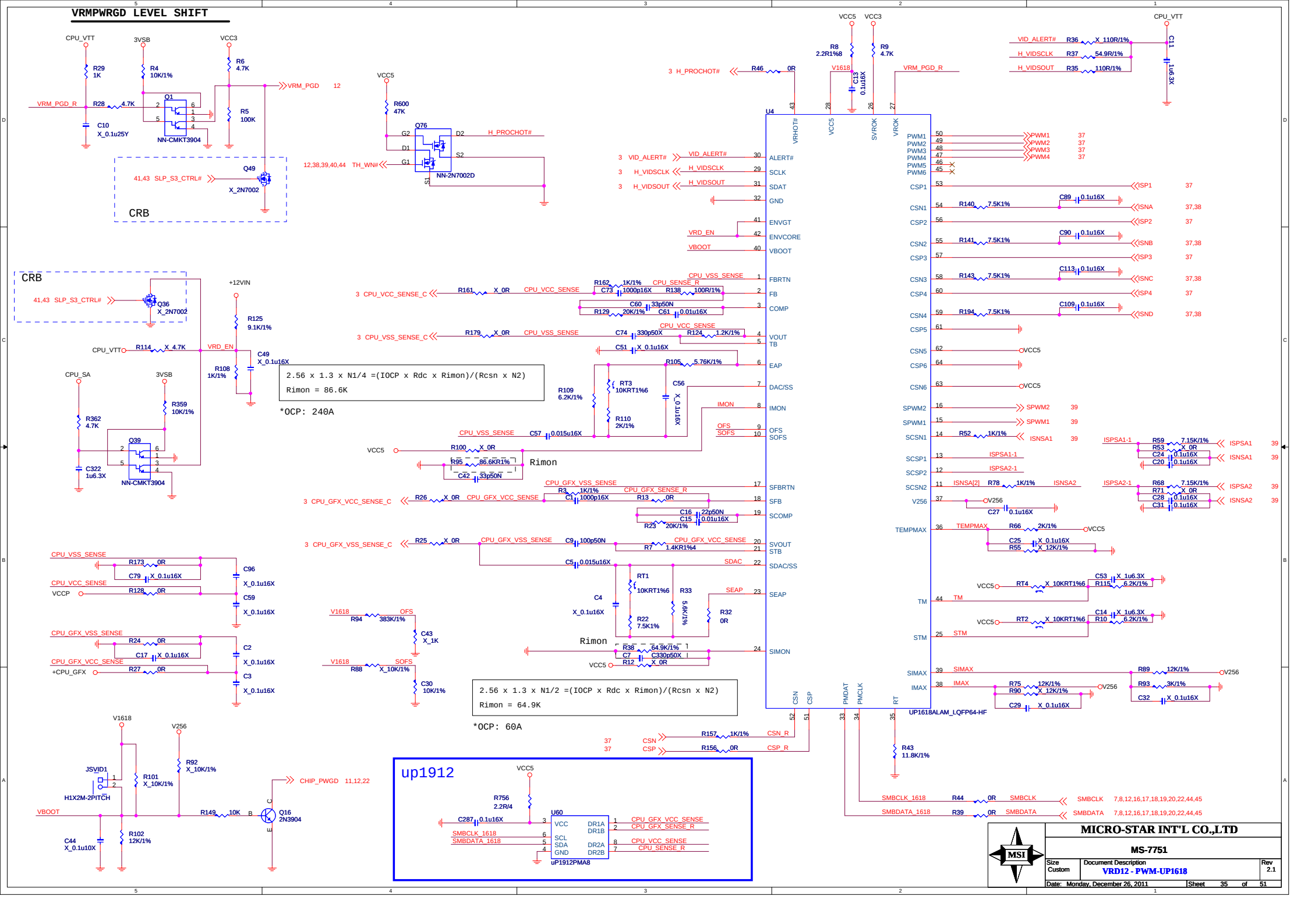
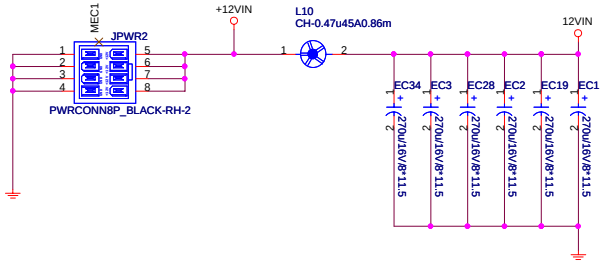
VRMPWRGD LEVEL SHIFT



POWER METER



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7751	
Size: Custom	Document Description: VRD12 - PWM-UP1618	Rev: 2.1
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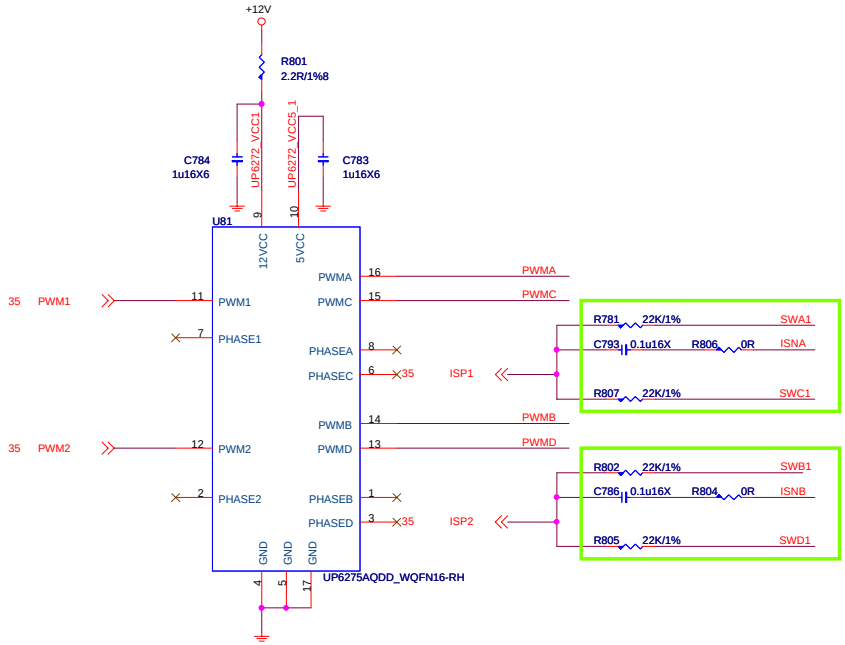

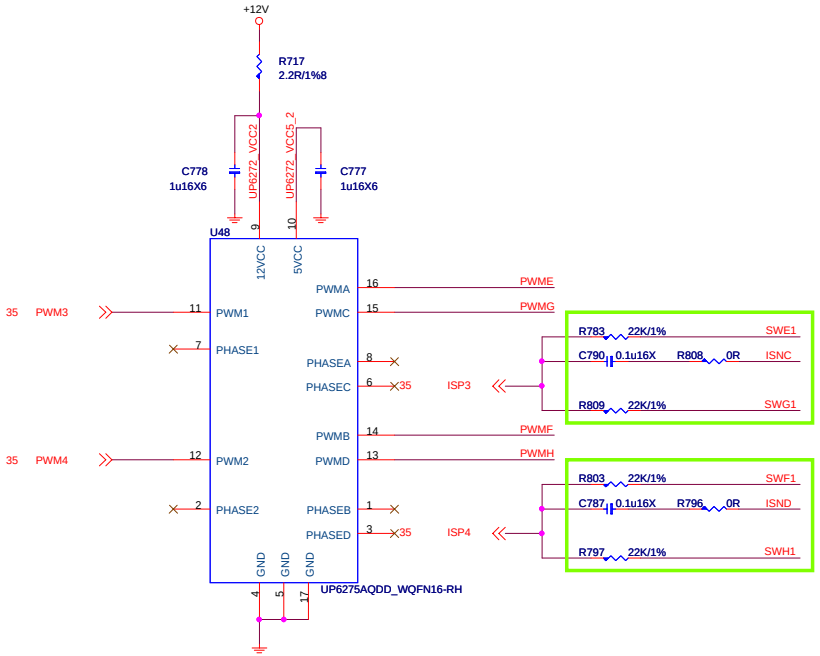

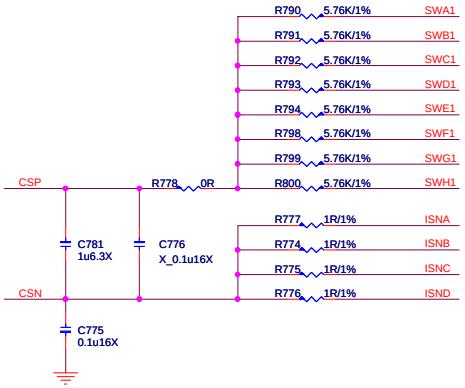

MICRO-STAR INT'L CO.,LTD		
MS-7751		
Size: Custom	Document Description: uP6275 - 4Phase to 8Phase	Rev: 2.1
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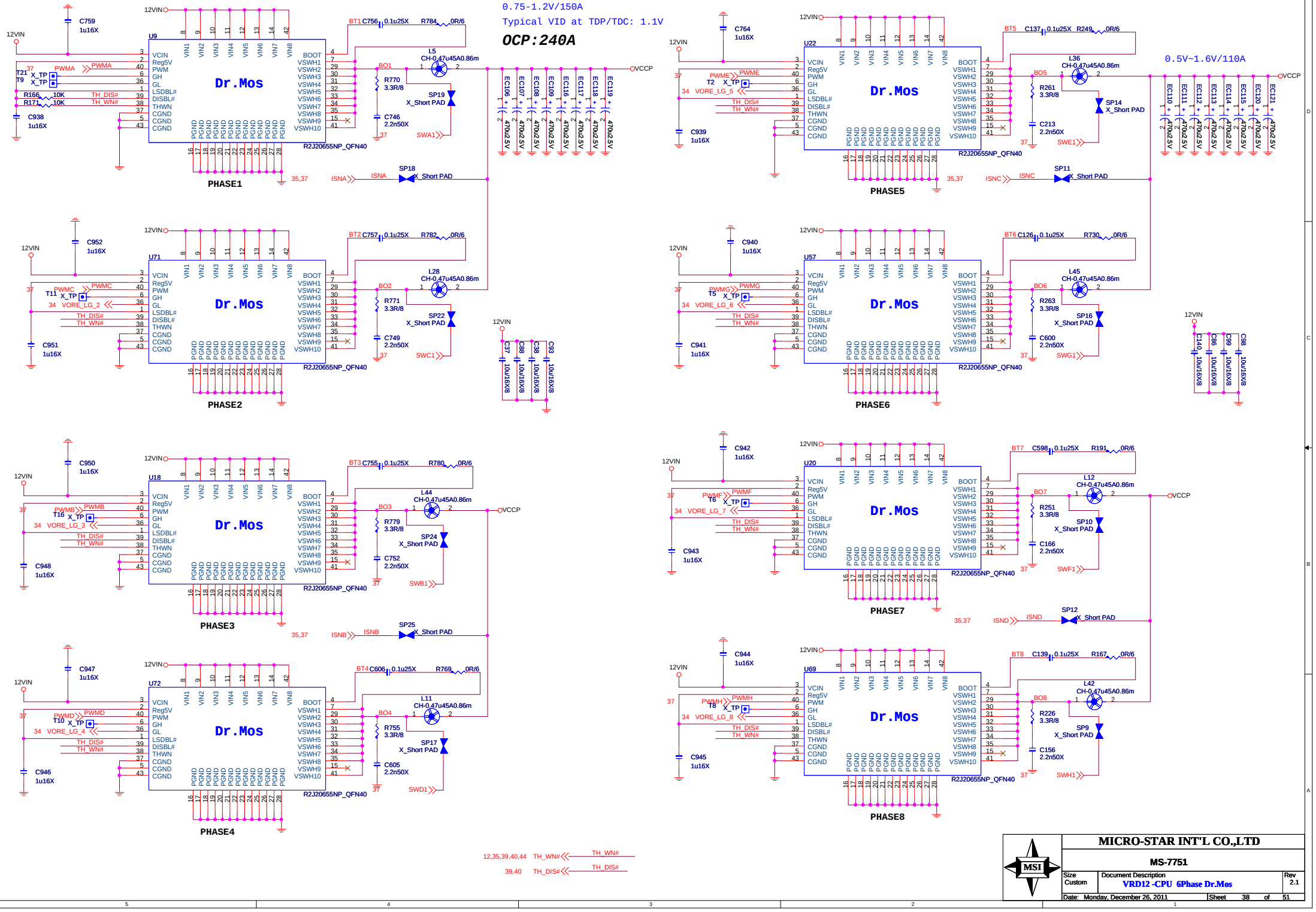
0.75-1.2V/150A
Typical VID at TDP/TDC: 1.1V
OCP:240A
0.5V~1.6V/110A
PHASE1
PHASE2
PHASE3
PHASE4
PHASE5
PHASE6
PHASE7
PHASE8
Dr.Mos
R2J20655NP_QFN40
MICRO-STAR INT'L CO.,LTD
MS-7751
VRD12 -CPU 6Phase Dr.Mos
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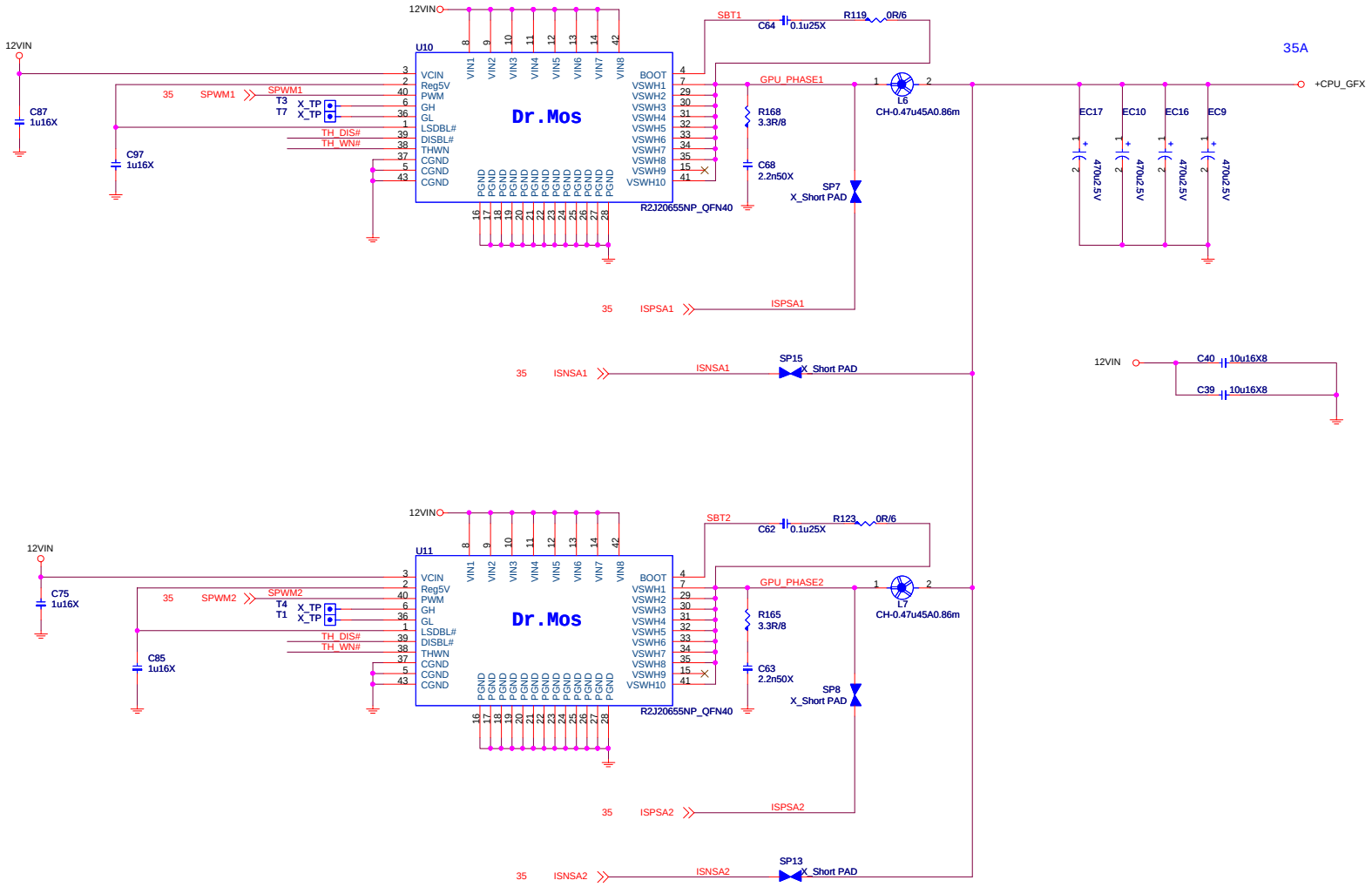
CPU_GFX:0.25-1.52

12,35,38,40,44 TH_WN#
38,40 TH_DIS#

35A FOR CPU

OCP:60A



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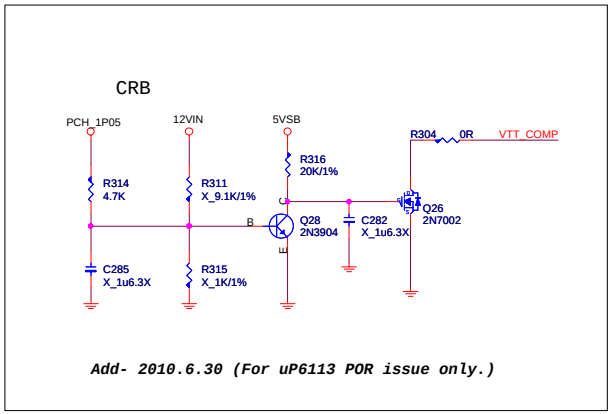
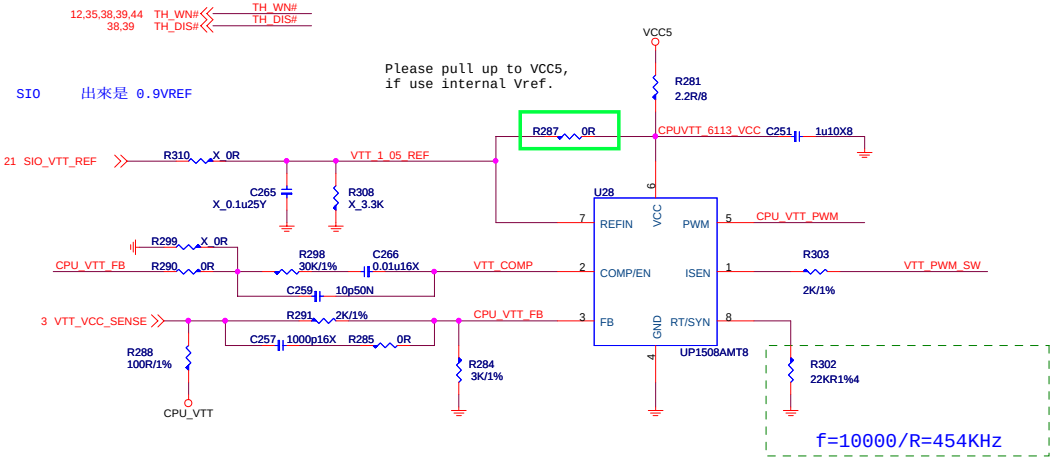
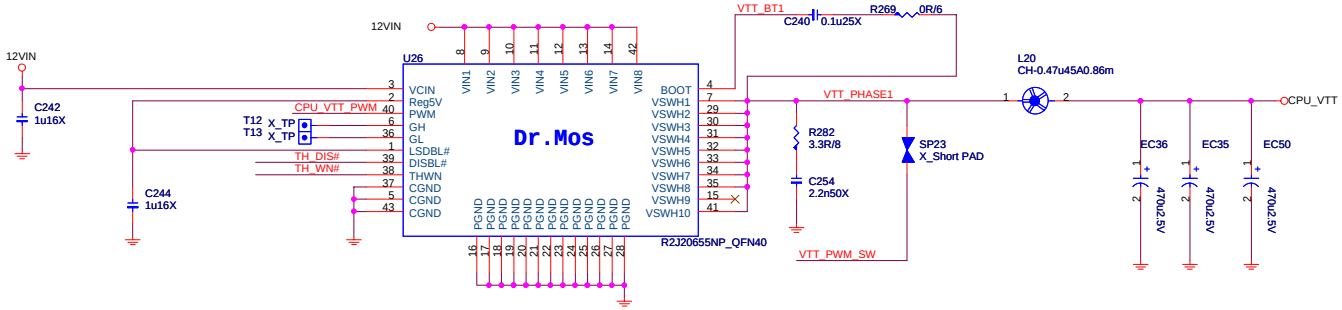
CPU_VTT:1.05/1.00

CPU VTT 8A

OCP:31.6A



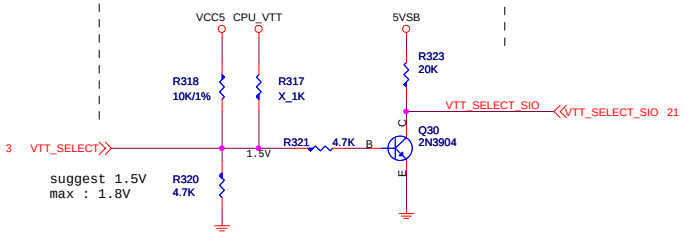


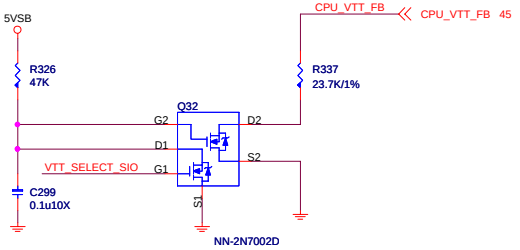


VTT_SELECT	
Ivy Bridge	1.0V
Sandy Bridge	1.05V

VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V





MICRO-STAR INT'L CO.,LTD	
MS-7751	
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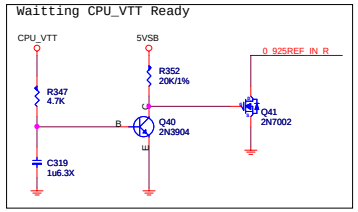
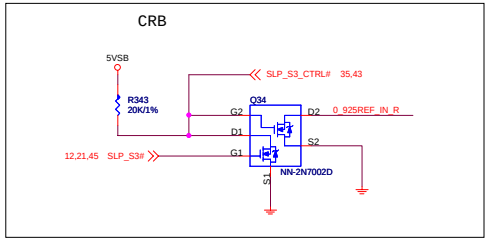
CPU_SA:0.925/0.85

SA Core =8.8A

OCP:19A

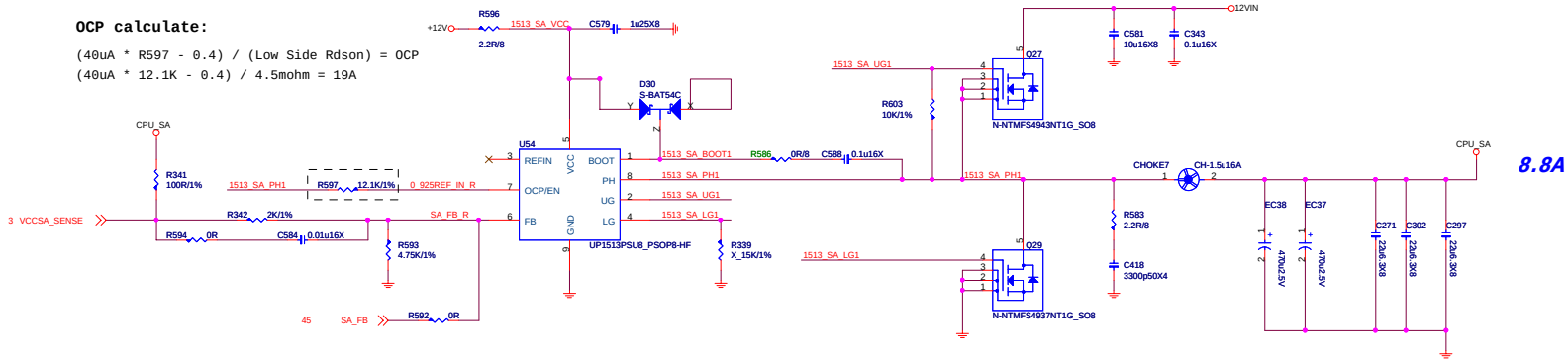
Iripple=2.12A
5*1=5A>2.12A





OCP calculate:

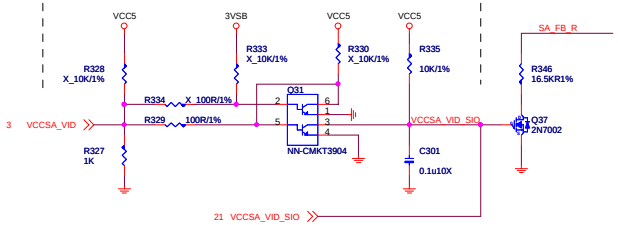
(40uA * R597 - 0.4) / (Low Side Rdson) = OCP
(40uA * 12.1K - 0.4) / 4.5mohm = 19A

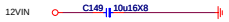


VCCSA_VID_SIO Table	
Ivy Bridge	0.85V/0.925V
Sandy Bridge	0.925V

VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.85V
High	0.925V





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MS-7751		
Size: Custom	Document Description: CPU_SA - uP6113 1-Phase	Rev: 2.1
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DDR Power:1.5V

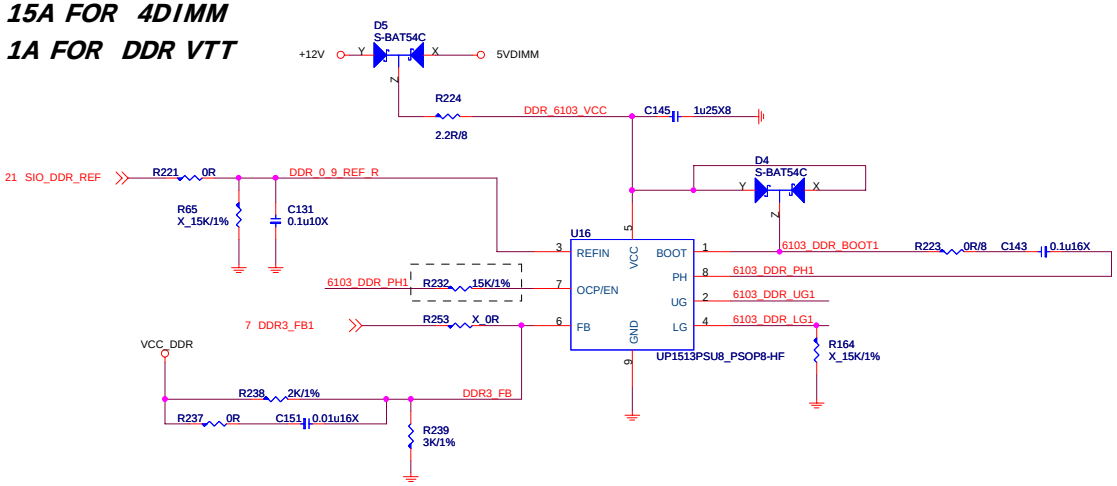
DDR3_1.5V 4.75A+15A+1A=20.75A

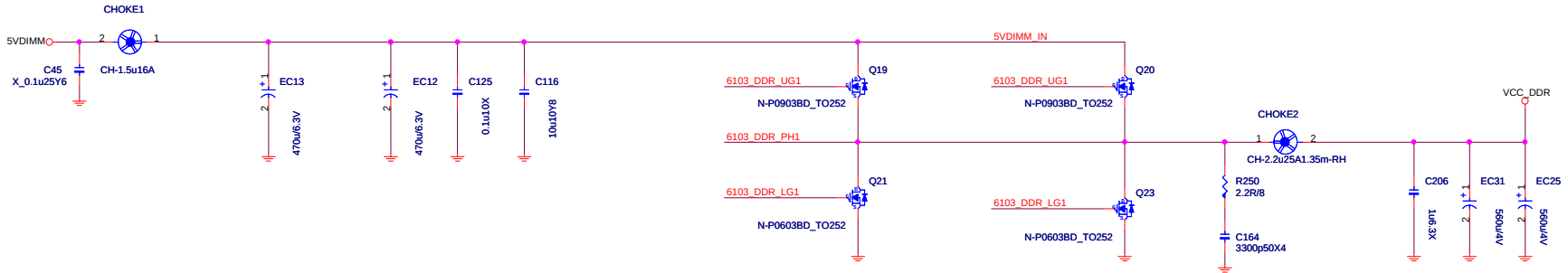
OCP:68.9A

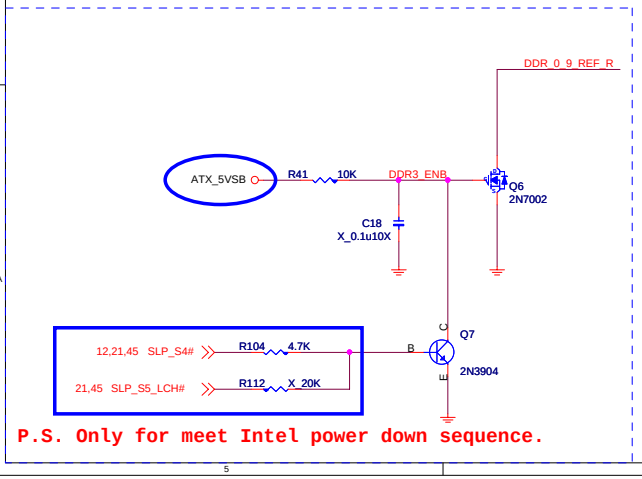
4.75A FOR CPU
15A FOR 4DIMM
1A FOR DDR VTT

OCP calculate:

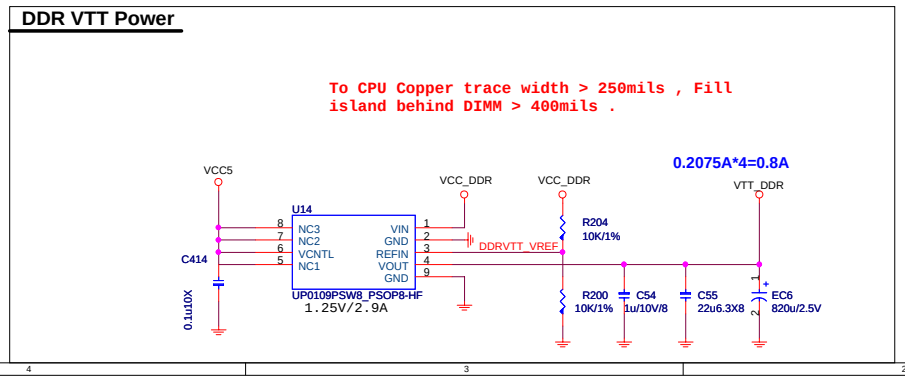
(40uA * R232 - 0.4) / (Low Side Rdson) = OCP
(40uA * 15K - 0.4) / (5.8mohm / 2) = 68.9A

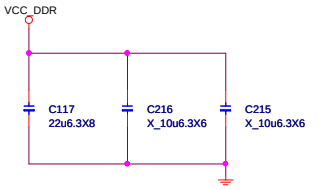






DDR VTT Power





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PCH Power:1.05V

PCH Core 6.2A+1.8A=8A

6.2A FOR PCH

1.8A FOR ME CORE

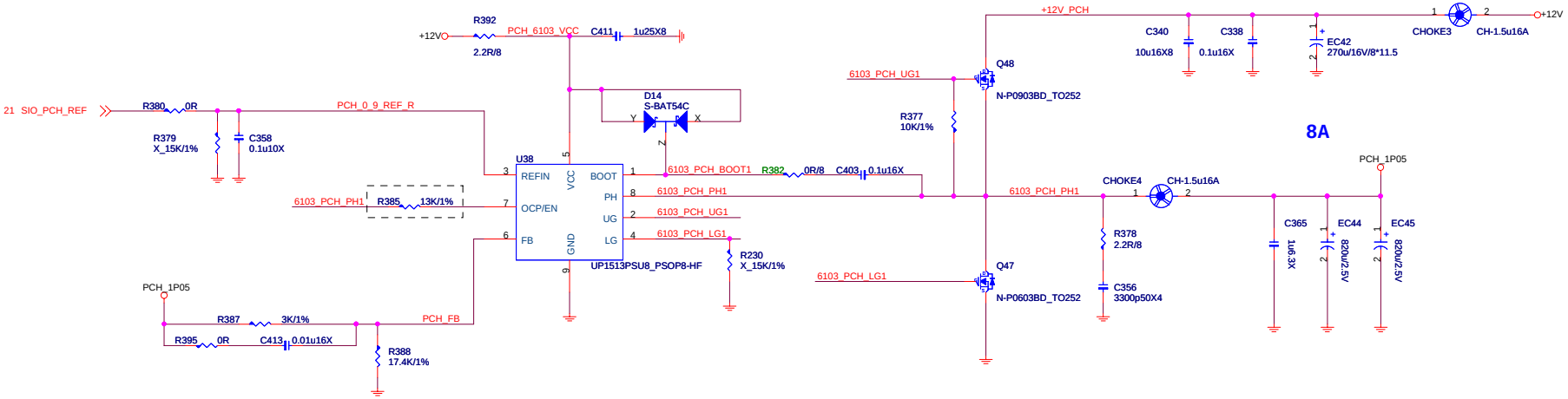
OCP:20.7A

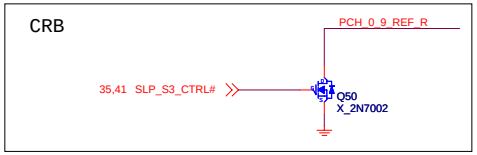
OCP calculate:

(40uA * R385 - 0.4) / (Low Side Rdson) = OCP

(40uA * 13K - 0.4) / 5.8mohm = 20.7A

Iripple=1.80A
5*1=5A>1.80A





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Size: Custom	Document Description: PCH Power - uP6103 1-Phase	Rev: 2.1
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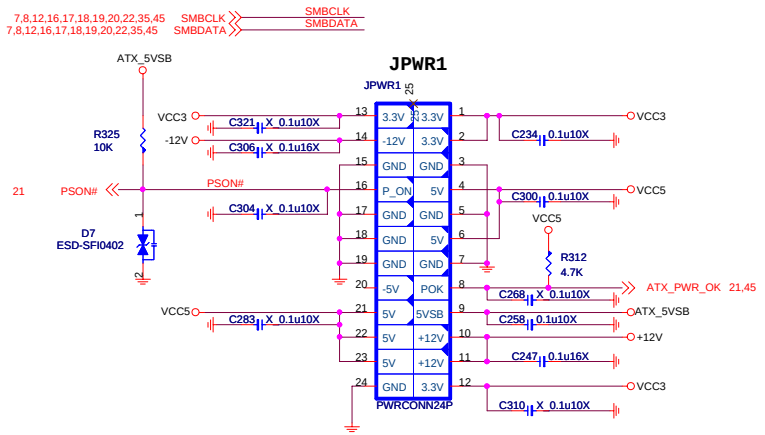
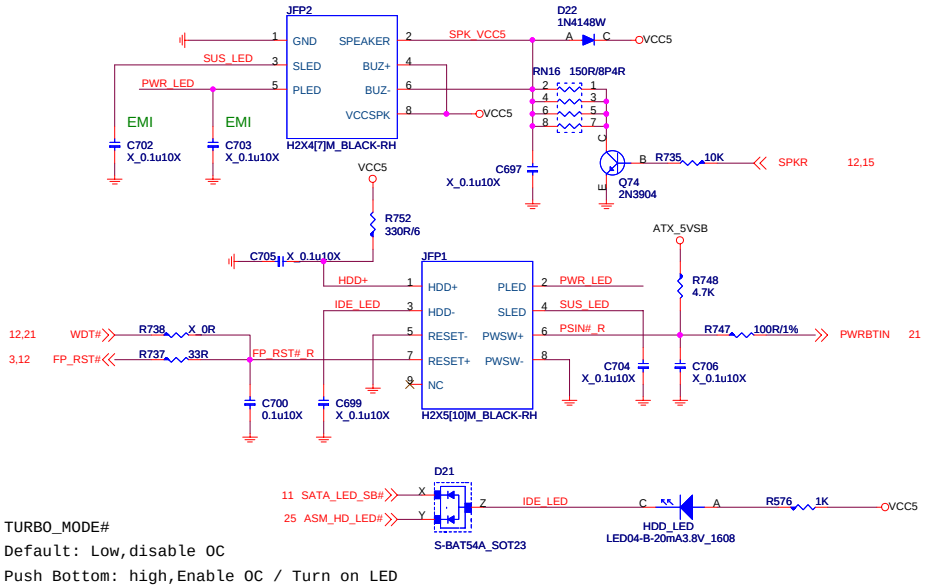
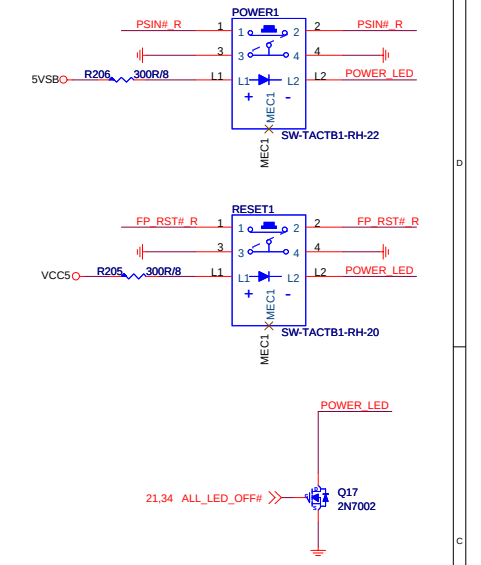
ATX POWER CONNECTOR



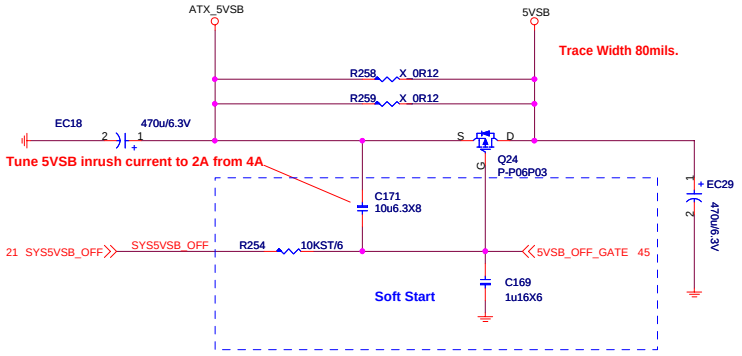
FRONT PANNEL



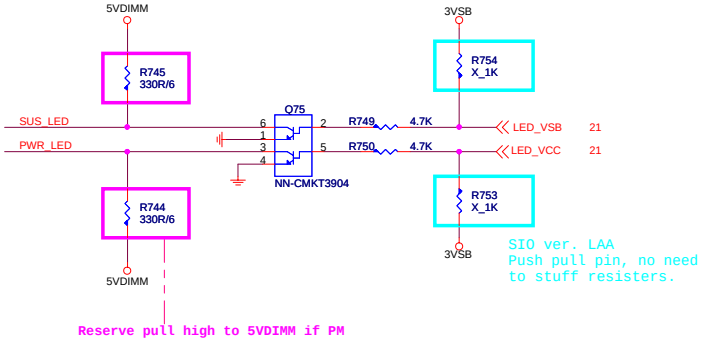
TURBO_MODE#
Default: Low,disable OC
Push Bottom: high,Enable OC / Turn on LED



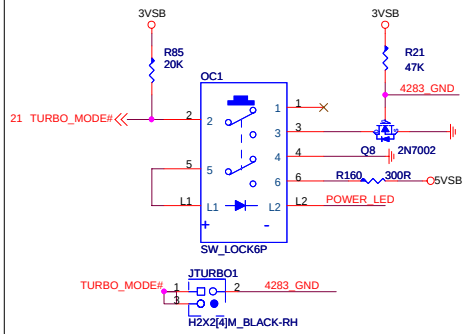
5VSB Power Switch



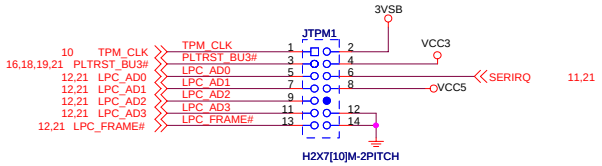
LED (for Fintek 71889)



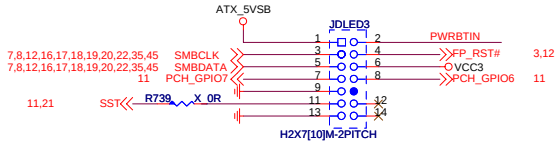
Turbo Button



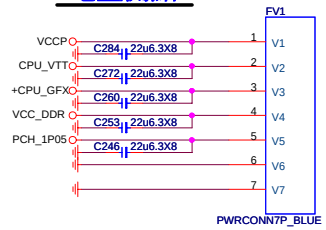
TPM



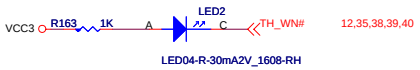
JDLED3



電壓測點



Warning LED



OCP SHUTDOWN

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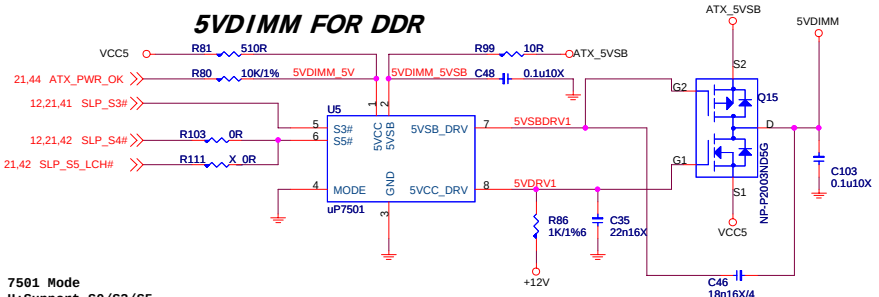
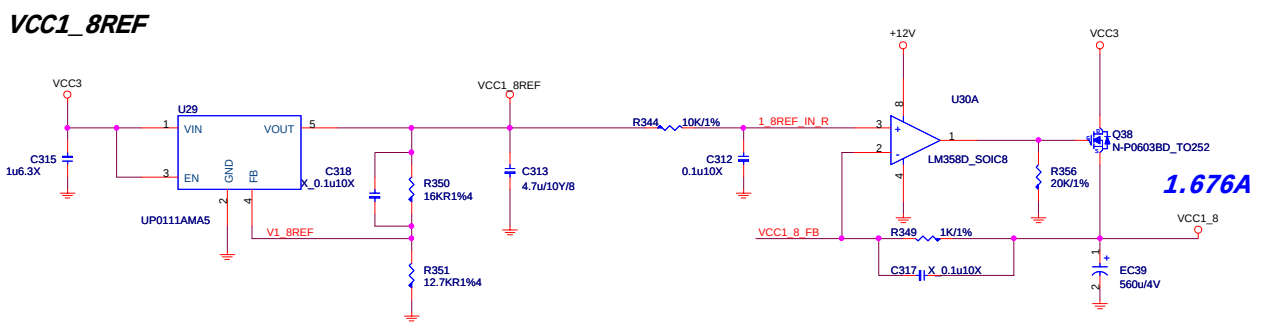
5VDIMM FOR DDR

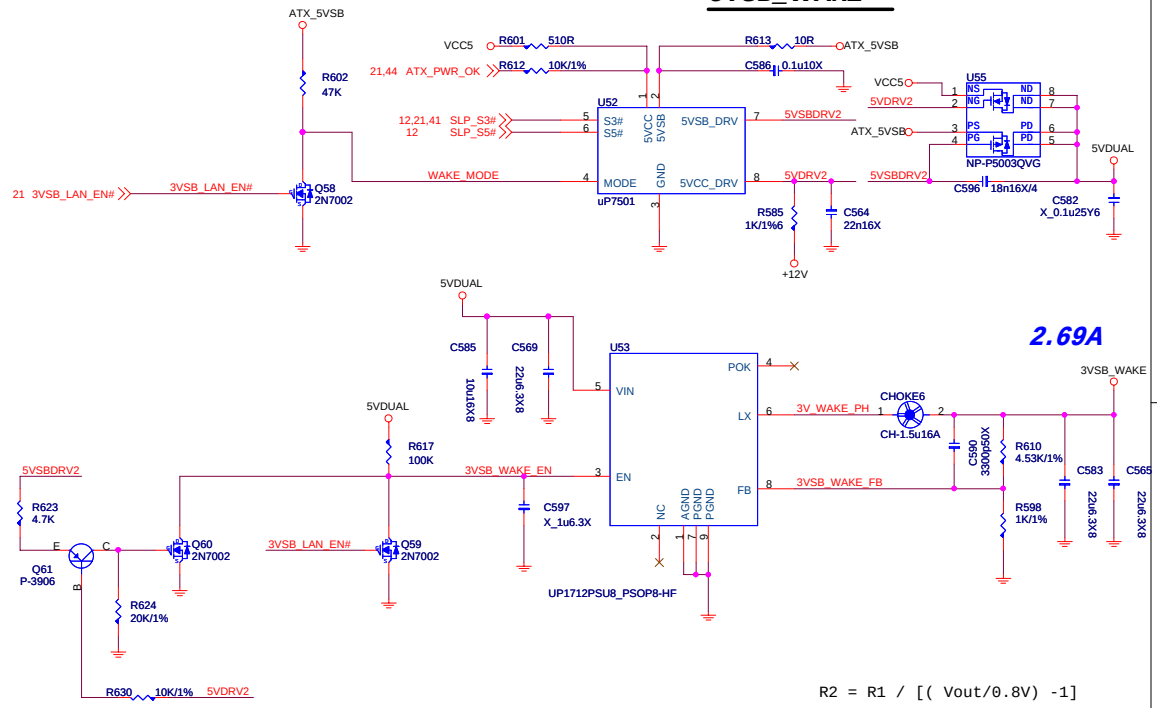


5VDRV1看VCC5起來6-10ms後起來,因為當初挑power

VCC1_8REF



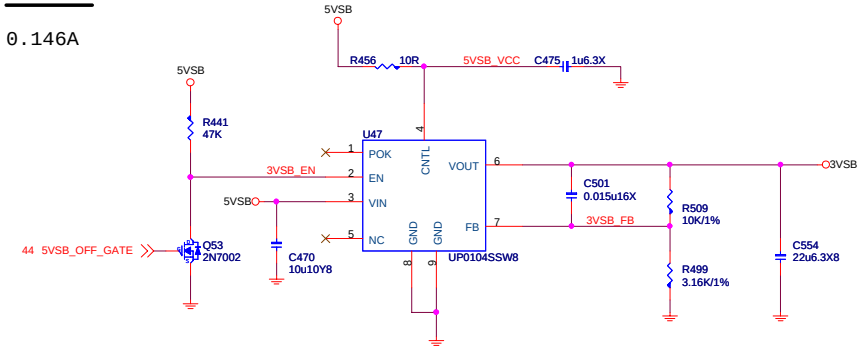
3VSB_WAKE



R2 = R1 / [(Vout/0.8V) -1]

3VSB

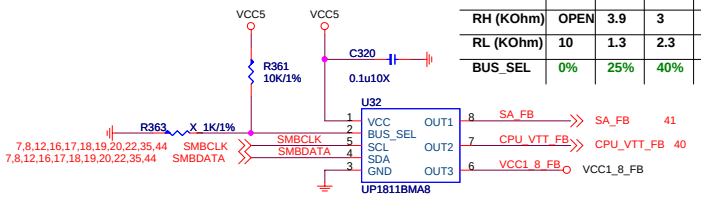
0.146A



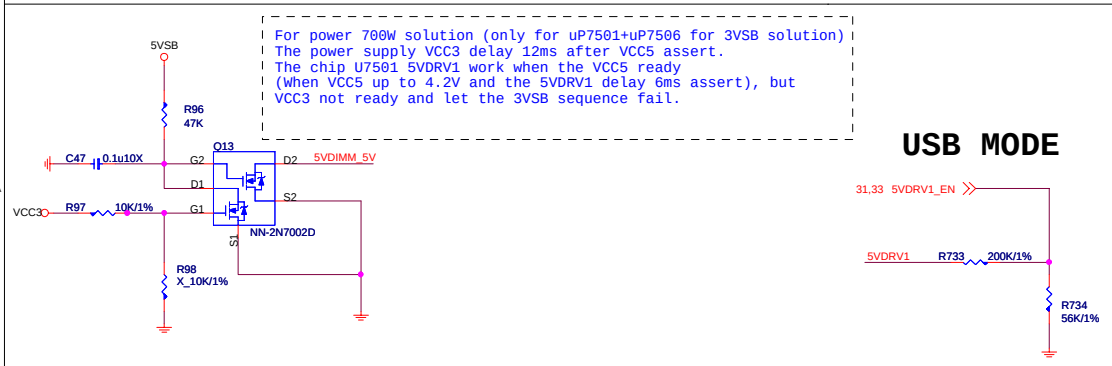
UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

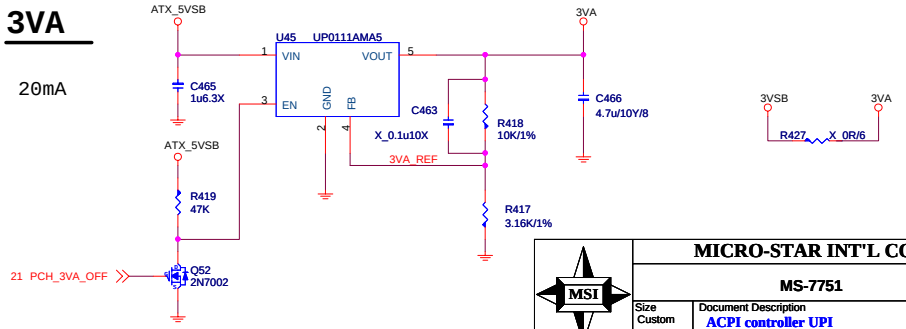


USB MODE



3VA

20mA



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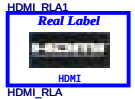
HDMI_RLA1



HDMI_RLA

HDMI Label Part Number

HDMI_LA1

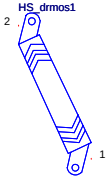
HDMI LABEL

HDMI Virtual Part Number

LA1

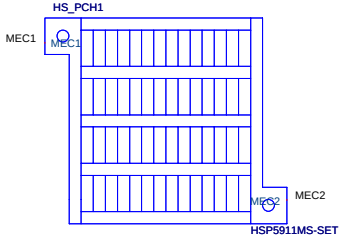
BIOS_LABLE

HS_drmos1



HS-502090-RH

HS_PCH1



HSP5911MS-SET

PCB1

7751_21

BAT1_X1

BAT-BCR2032P-RH

CPU_H1

CPU_H1

LABEL1

BUY

LABEL4

BUY

CPU_SA

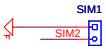
CPU_SA

Simulation

SIM2

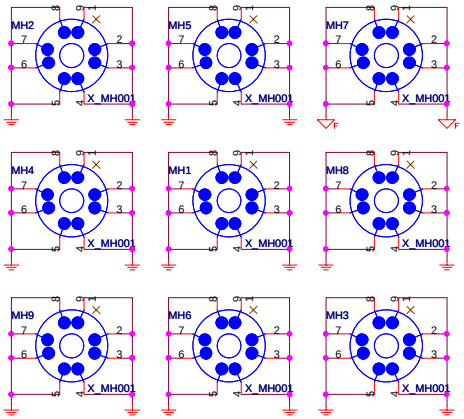
X_PIN1*2

SIM1

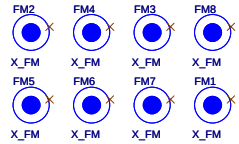


X_PIN1*2

Mounting Holes



Optical Fiducial Marks-120



OPT	Configure	BOM	Function
		601-7751-04S.001	Z77A-GD65 4*DDR3+3*PCI-Ex16,4*PCI-Ex1,+4*SATAII+4*SATAIII+1394+10*USB2.0+ 4*USB3.0+HD 8Ch Audio+HDMI+DVI+Gb LAN,Hi-C CAP,EuP,RoHS

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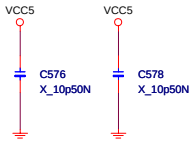
Close to EC11



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