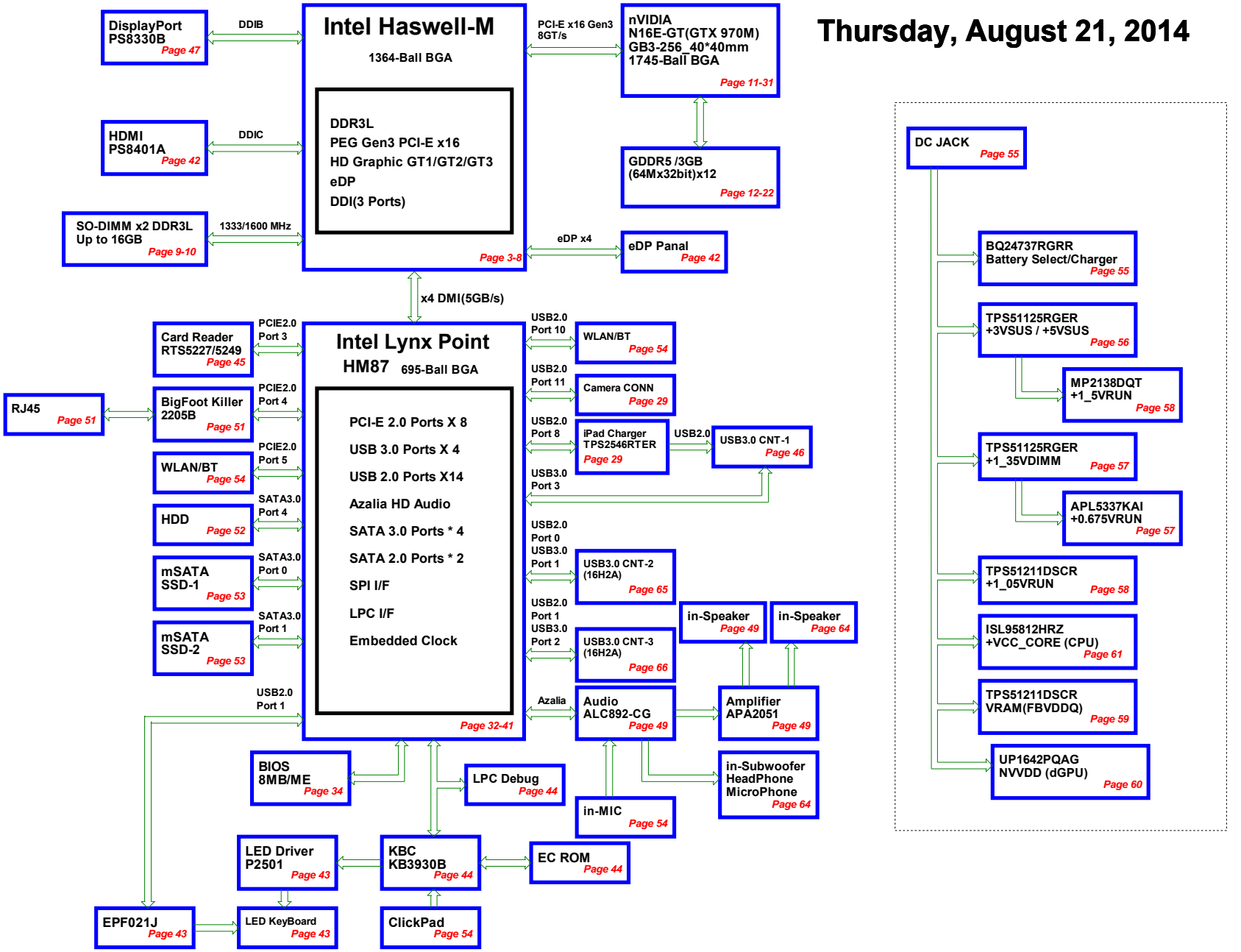
MS-16H5 Ver:1.2

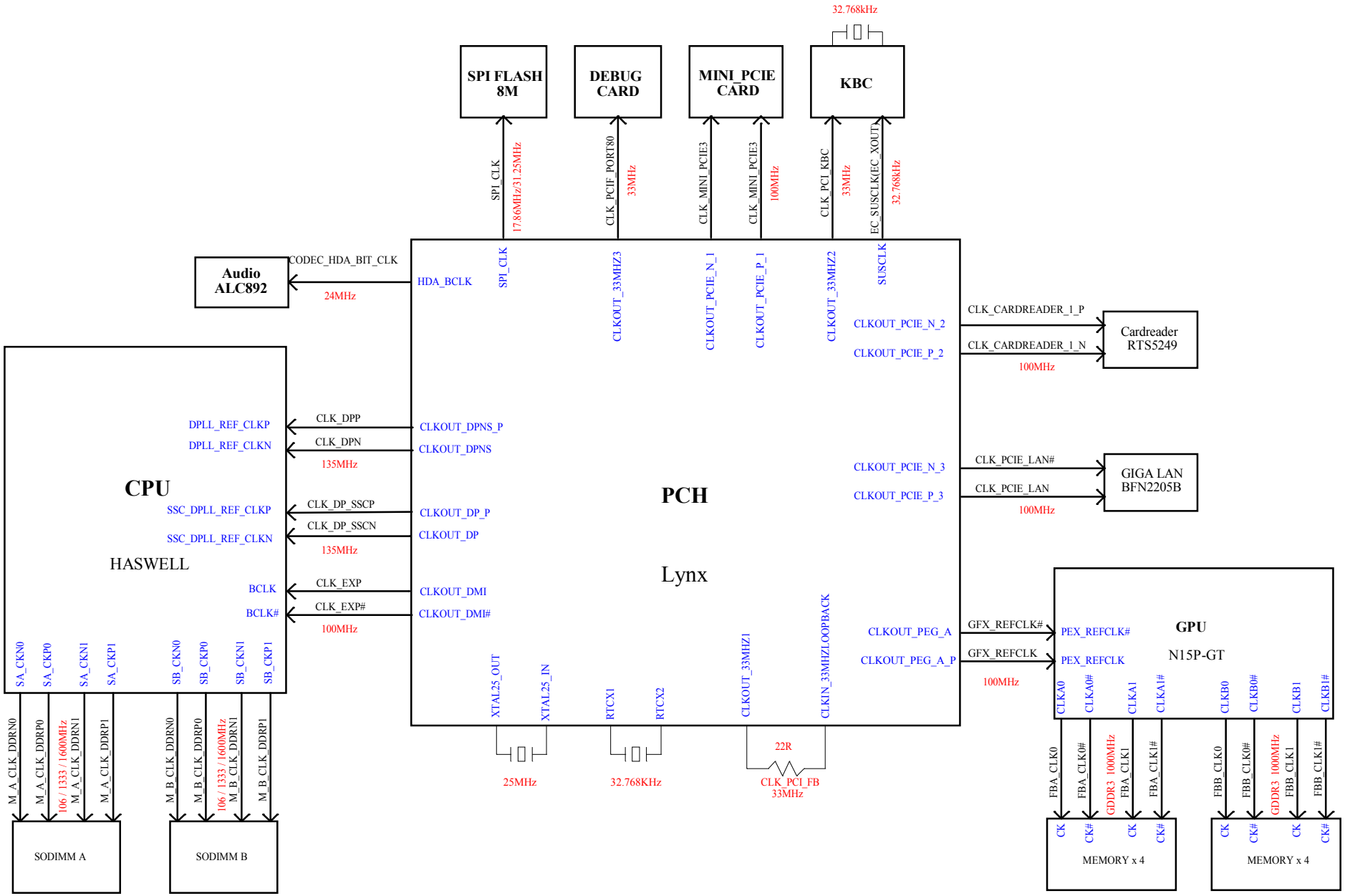
Shark Bay Mobile

Thursday, August 21, 2014



MICRO-STAR INT'L CO.,LTD.

Title: Block Diagram
Size: Document Number: MS-16H5
Rev: 1.2
Date: Sheet 1 of 72



MICRO-STAR INT'L CO.,LTD.

Title: CLock Delivery chart

Size | Document Number: MS-16H5 | Rev: 1.2

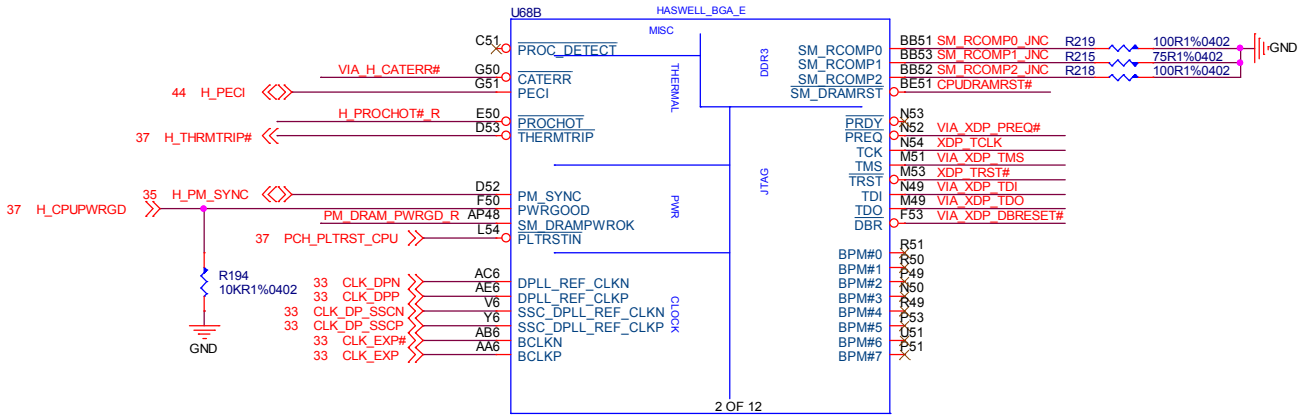
Date: Thursday, August 21, 2014 | Sheet 2 of 72

Haswell (DMI,PEG,FDI)

PEG_RCOMP
Width:12 mils
Spacing:15 mils
Length:400 mils

Haswell (CLK,MISC,JTAG)

SM_RCOMP_0/1/2 : 15/20/25/15/20/25
SM_RCOMP_0/1/2 Length max: 500mil

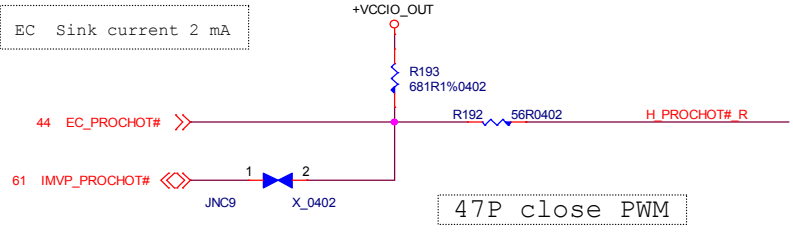


H_CPUPWRGD EC8 X_C15p50N0402 GND

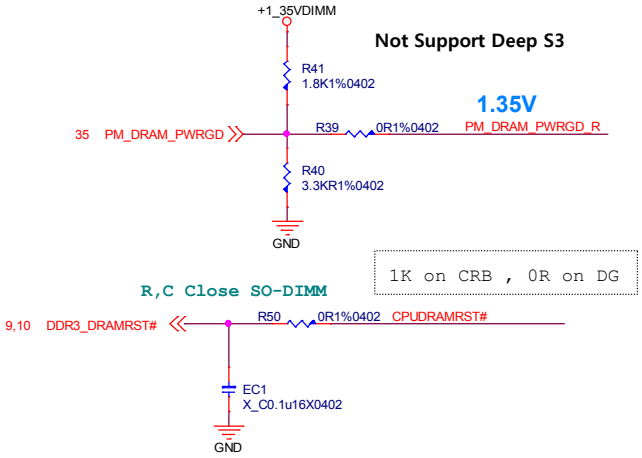
I7 4860

I7 4870

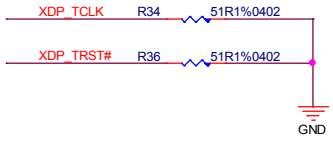
EC Sink current 2 mA



47P close PWM



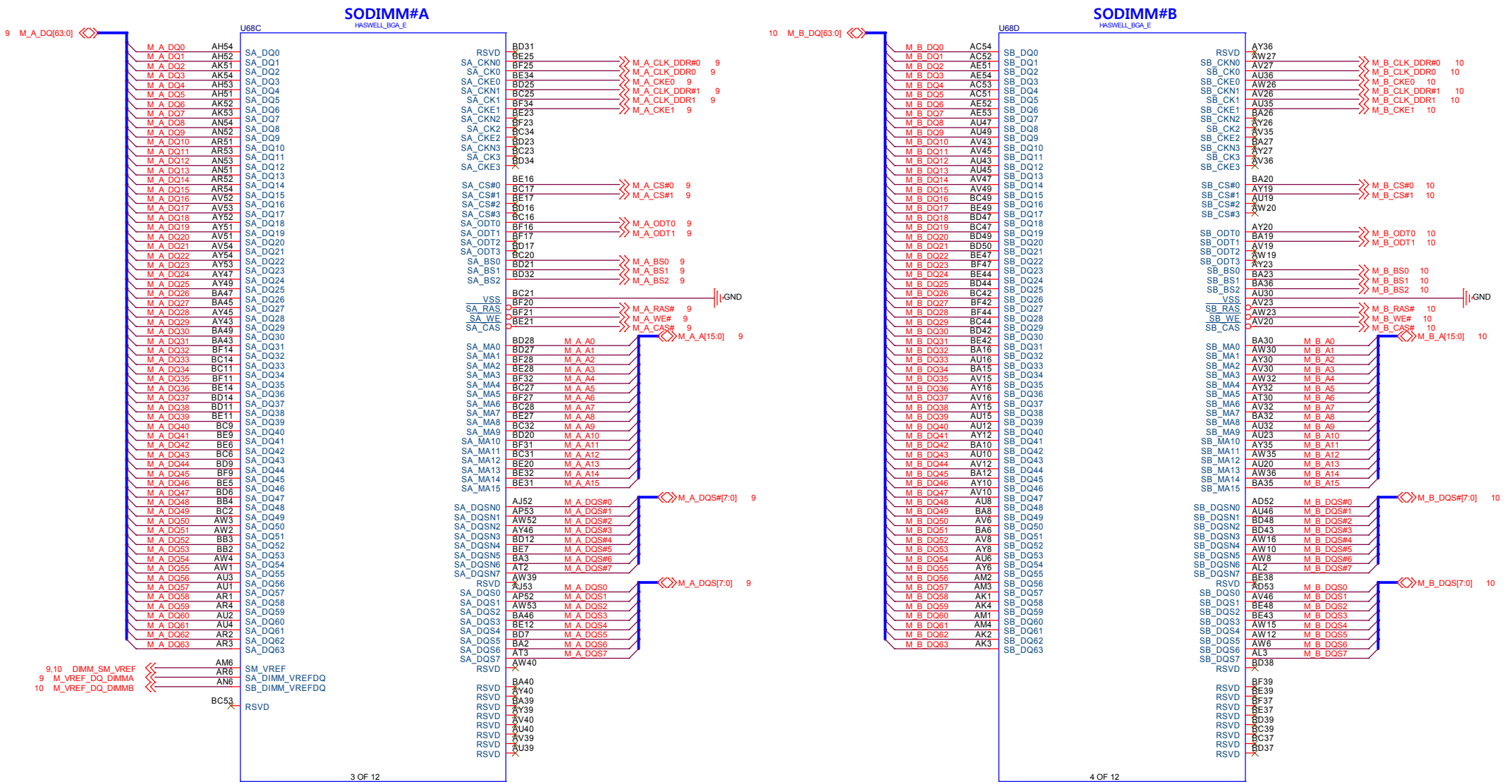
p.11 479493_479493_SharkBay_HSW_ext_rev2.0.pdf
Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals, PREQ# and PRDY# signals signals have adequate internal bias resistances to support the removal of the external pull up and pull down on the board when debug is no longer needed.



MICRO-STAR INT'L CO.,LTD.

Title	CPU-1 (Host Bus)	
Size	Document Number MS-16H5	Rev 1.2
Date: Thursday, August 21, 2014	Sheet 3 of 72	

Haswell (DDR3L)



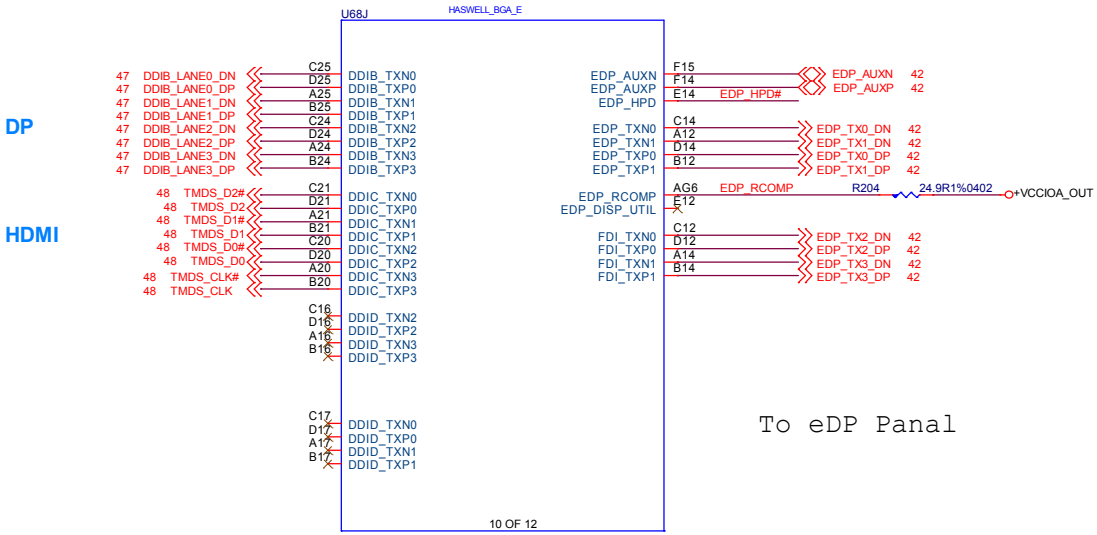
MICRO-STAR INT'L CO.,LTD.

Title: CPU-2 (DDR3L)

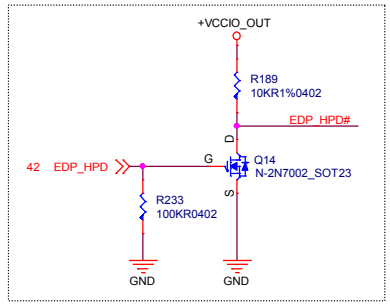
Size	Document Number	Rev
	MS-16H5	1.2

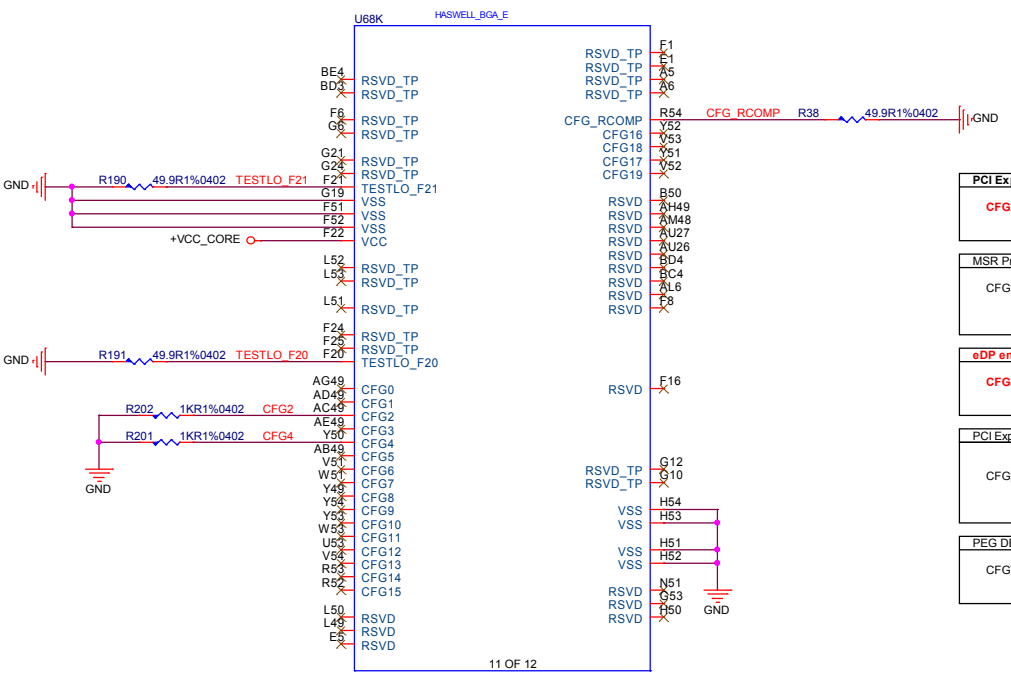
Date: Thursday, August 21, 2014 Sheet 4 of 72

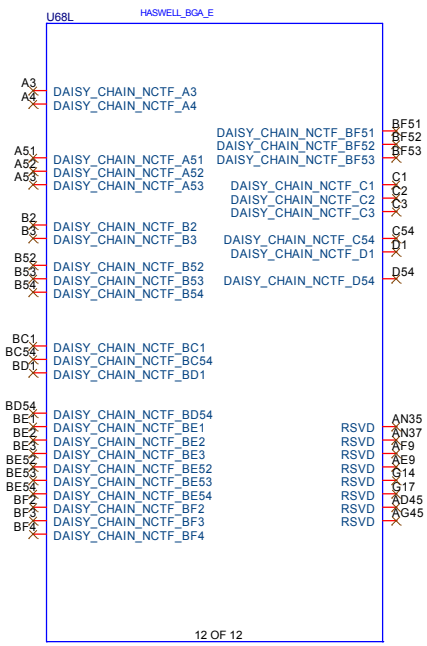
Display/Reserved



To eDP Panal







PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP enable	
CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

MICRO-STAR INT'L CO.,LTD.

Title: CPU-3 (Display/Reserved)

Size | Document Number: MS-16H5 | Rev: 1.2

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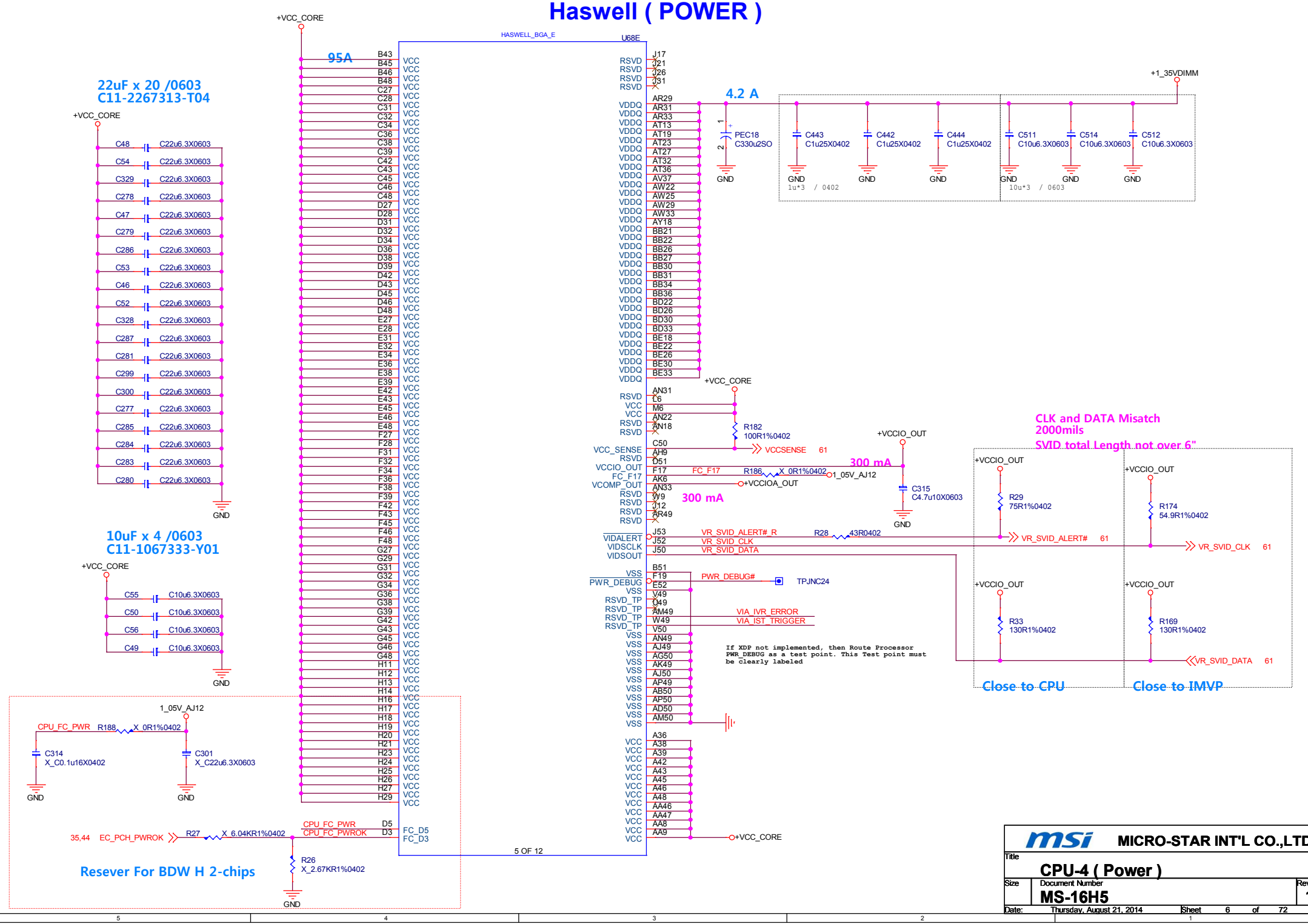
Haswell (POWER)



MICRO-STAR INT'L CO.,LTD.	
Title	CPU-4 (Power)
Size	Document Number: MS-16H5
Rev	1.2
Date:	Thursday, August 21, 2014
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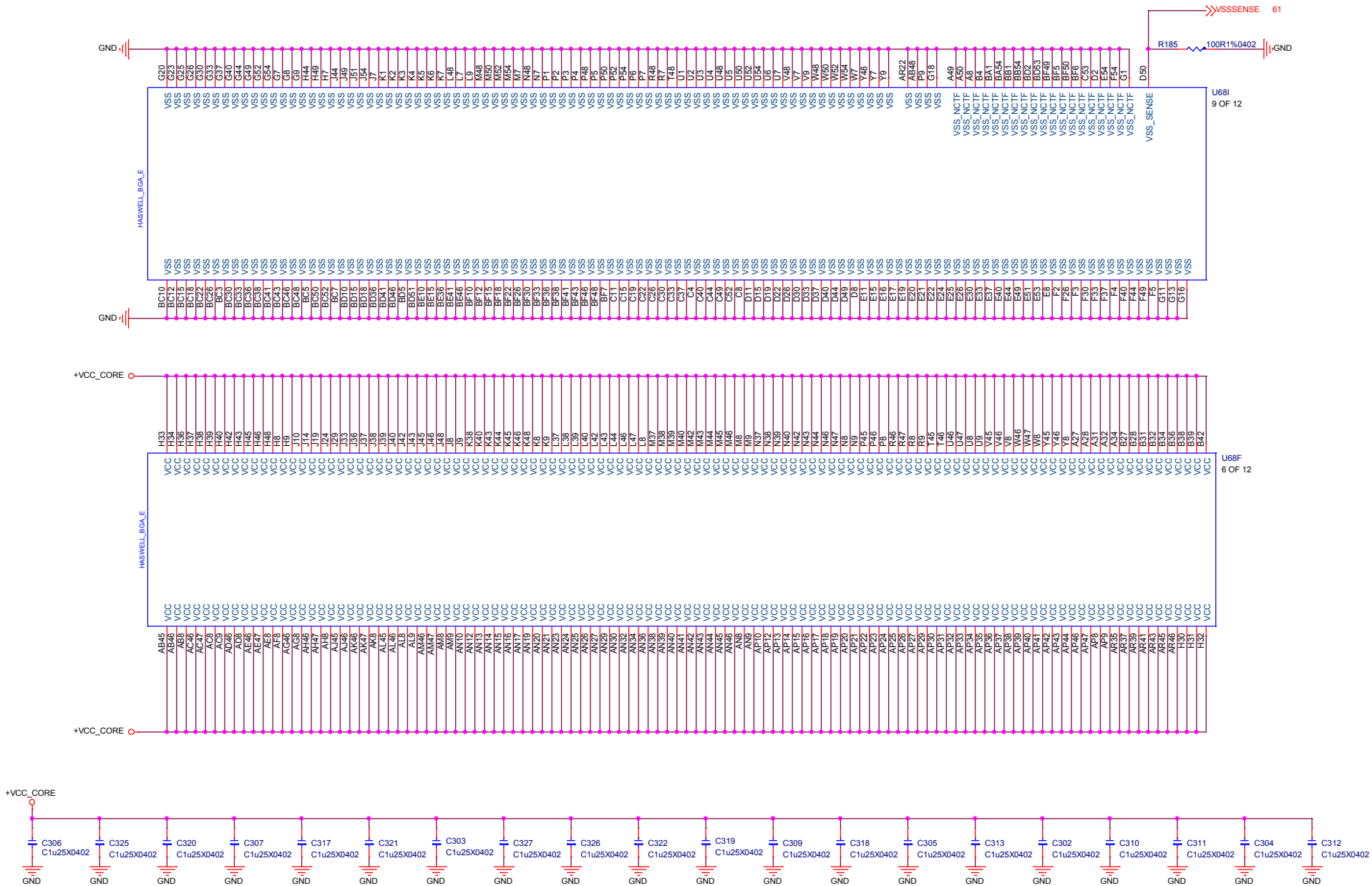
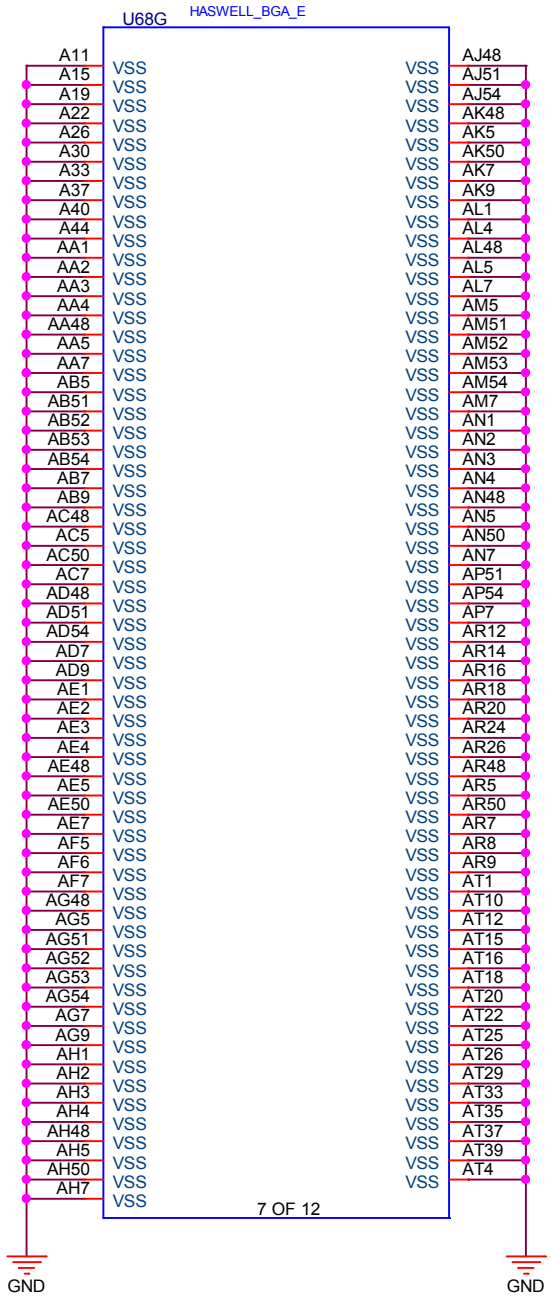
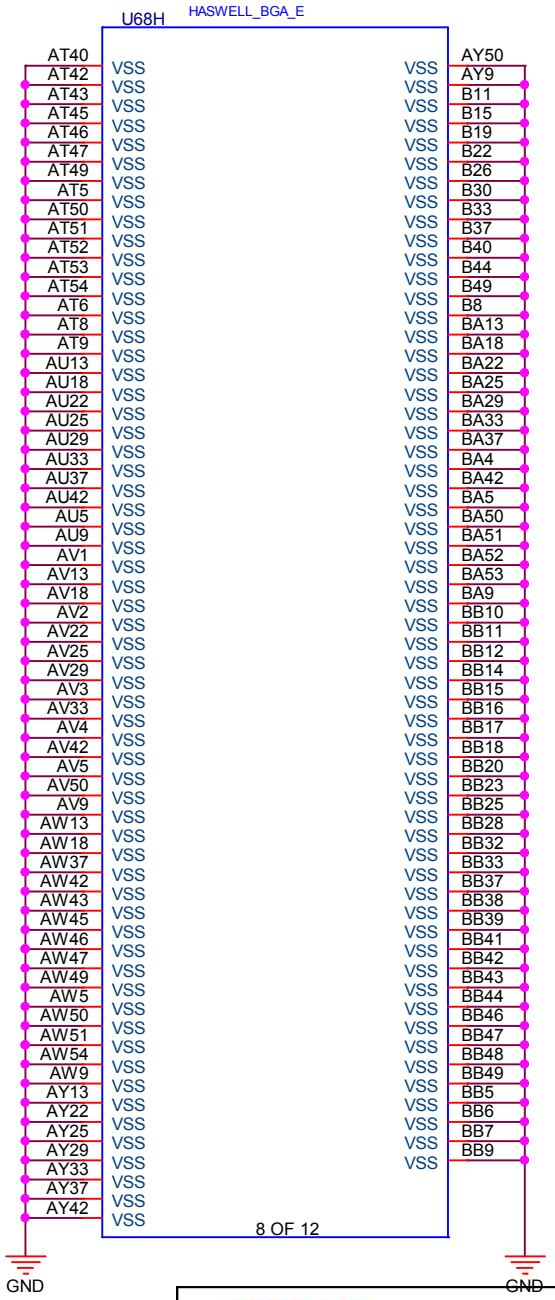
Haswell (Power & GND)



MICRO-STAR INT'L CO.,LTD.		
Title: CPU-6 (Power & GND)		
Size	Document Number: MS-16H5	Rev: 1.2
Date: Thursday, August 21, 2014	Sheet 7 of 72	

Haswell (GND)





MICRO-STAR INT'L CO.,LTD.

Title	CPU-5 (GND)	
Size	Document Number: MS-16H5	Rev: 1.2
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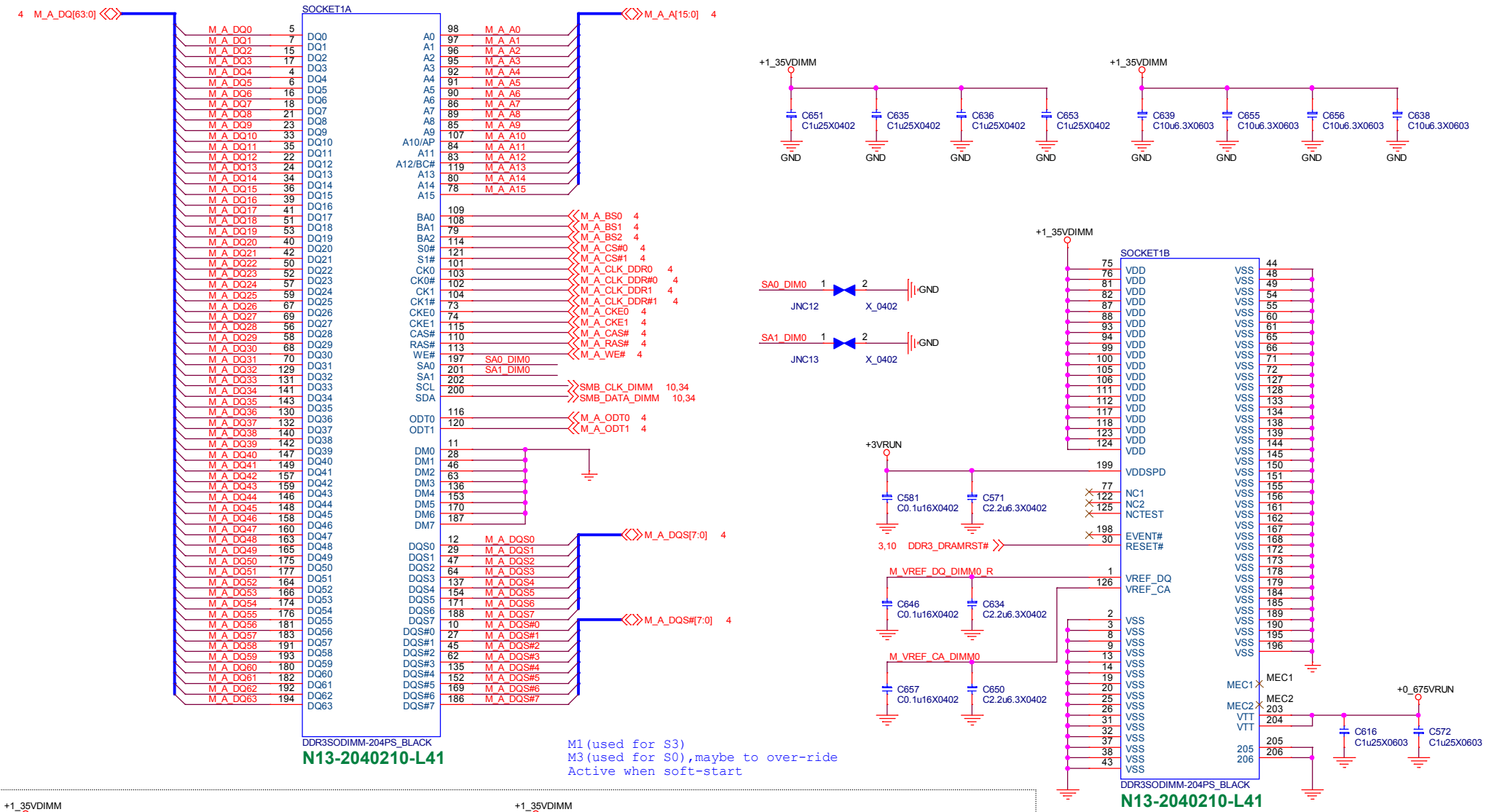
SODIMM#A



MICRO-STAR INT'L CO.,LTD.		
Title: DDR3L SODIMM 0		
Size	Document Number: MS-16H5	Rev: 1.2
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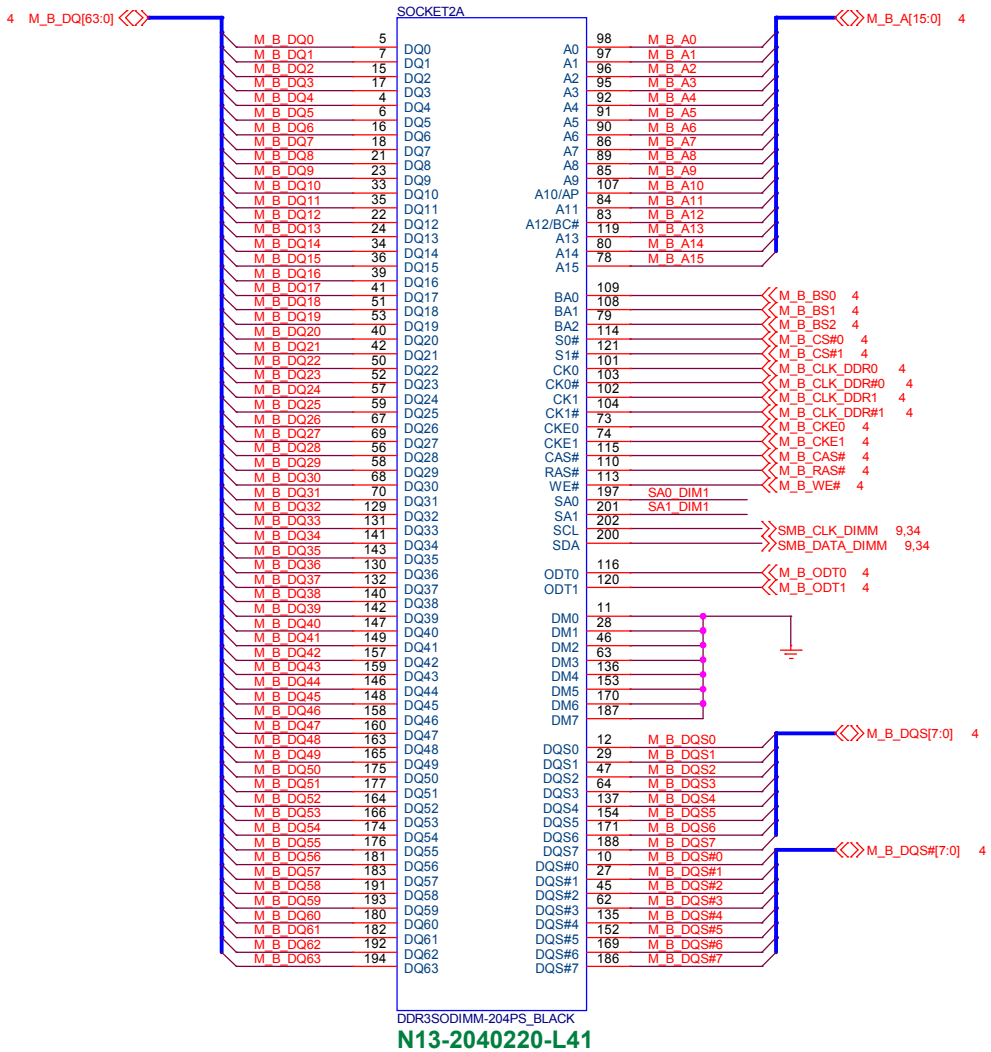
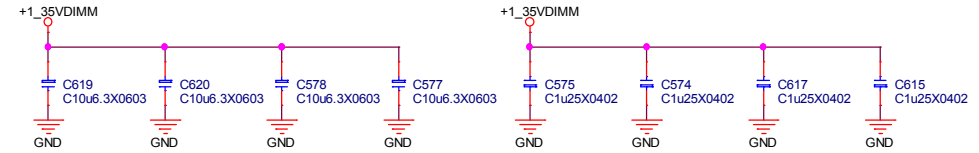
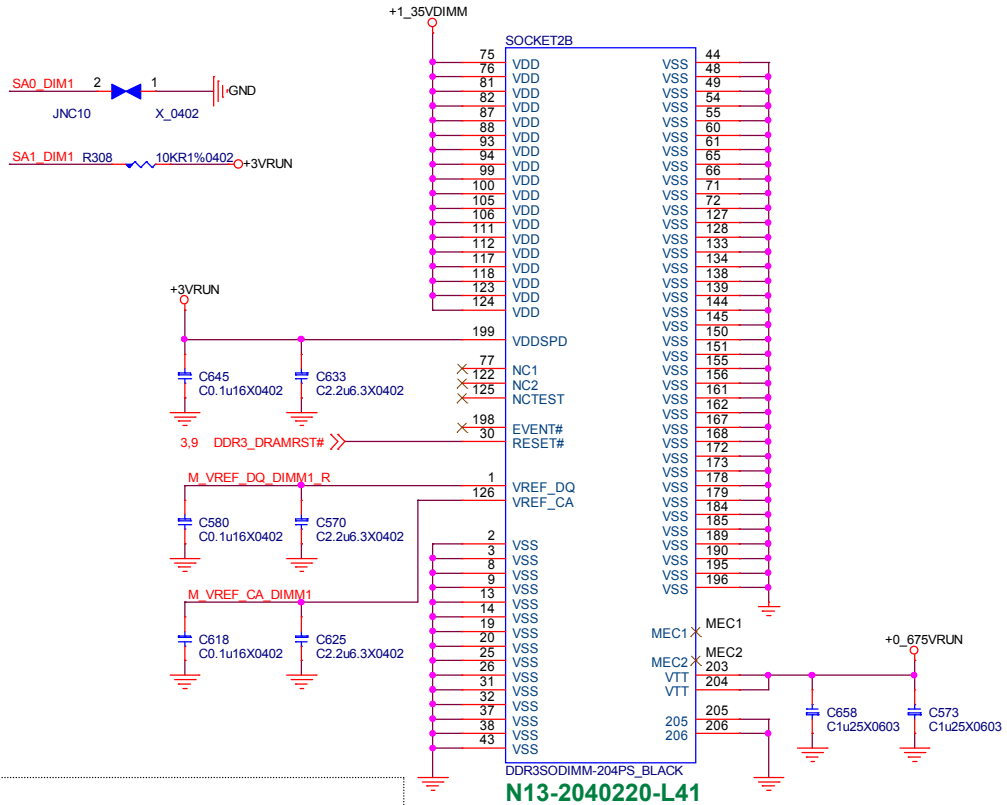
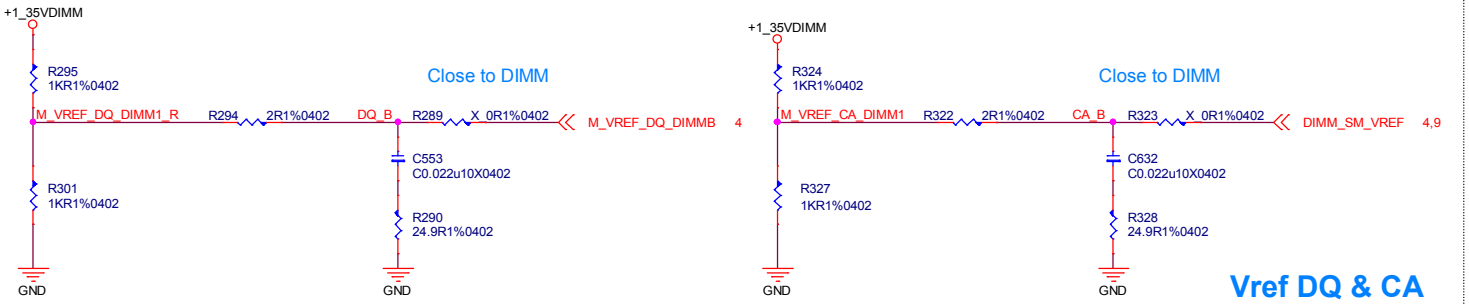
SODIMM#B









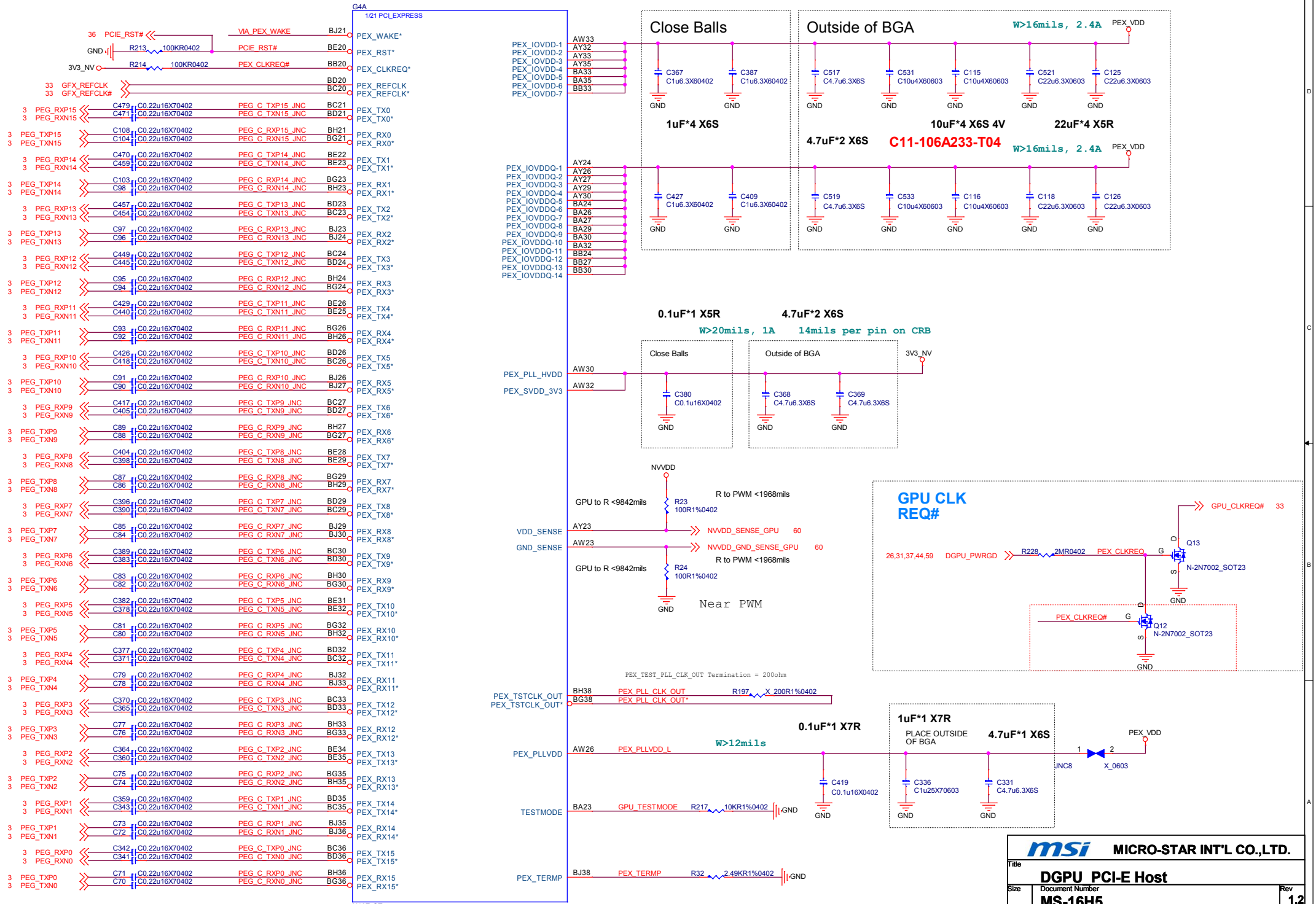
MICRO-STAR INT'L CO.,LTD.

Title: DDR3L SODIMM 1

Size | Document Number: MS-16H5 | Rev: 1.2

Date: Thursday, August 21, 2014 | Sheet 10 of 72

GPU PCI EXPRESS



MICRO-STAR INT'L CO.,LTD.	
Title	DGPU PCI-E Host
Size	Document Number: MS-16H5
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Date:	Thursday, August 21, 2014
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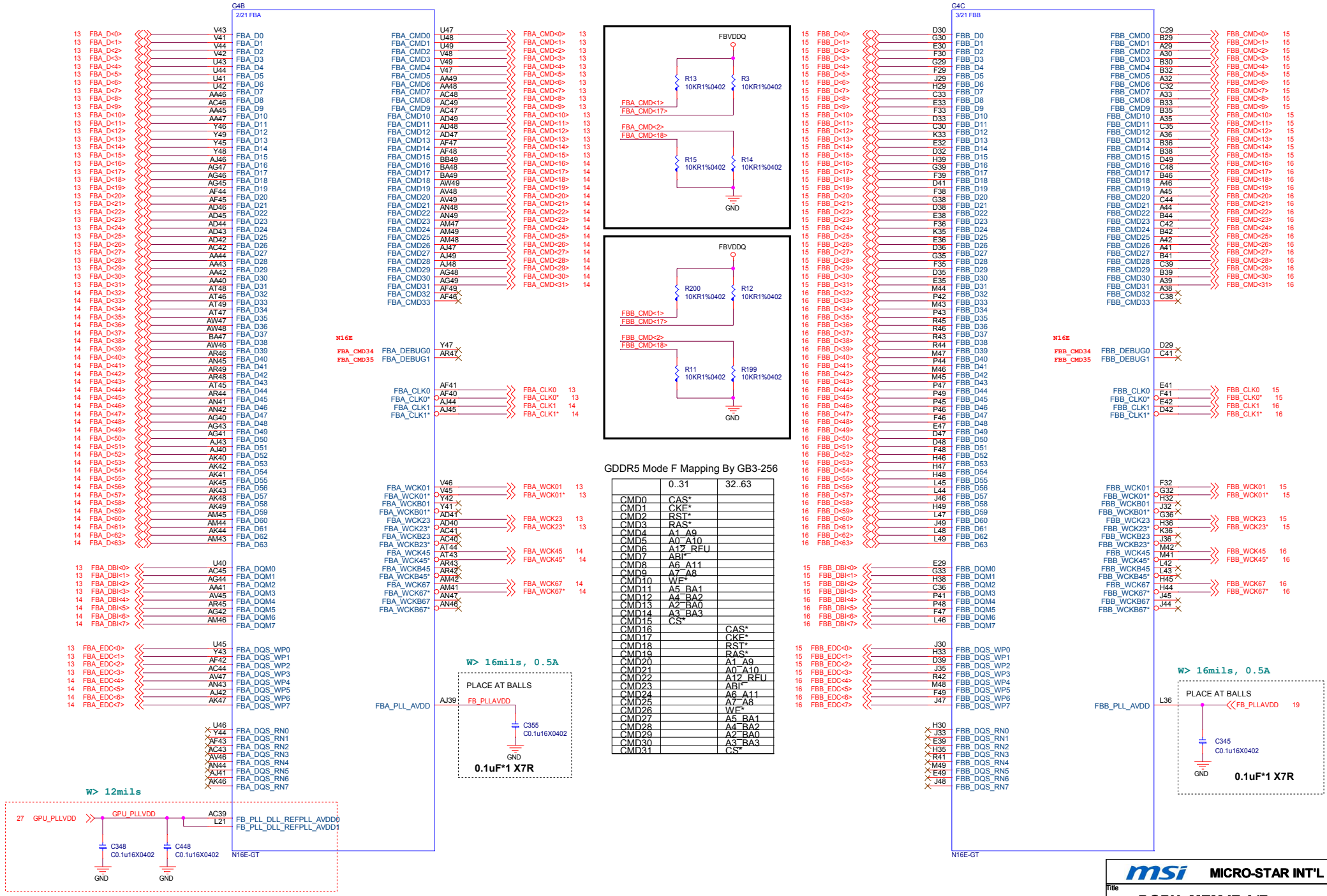
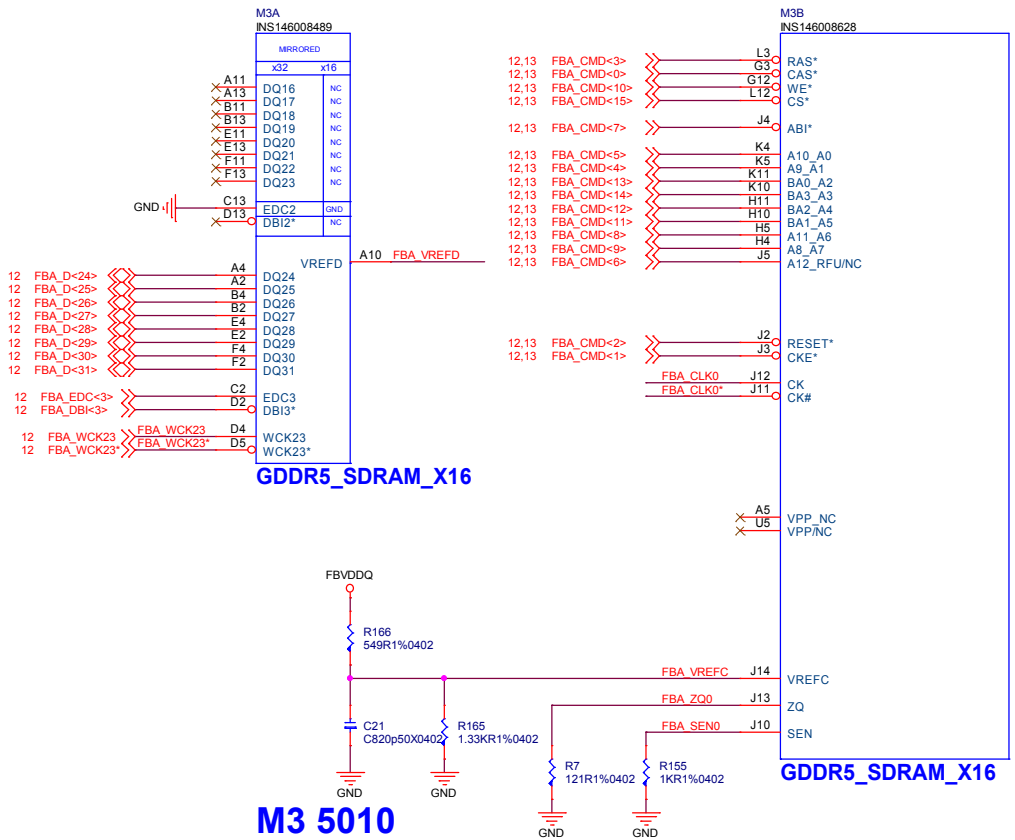
GPU Frame Buffer Partition A/B

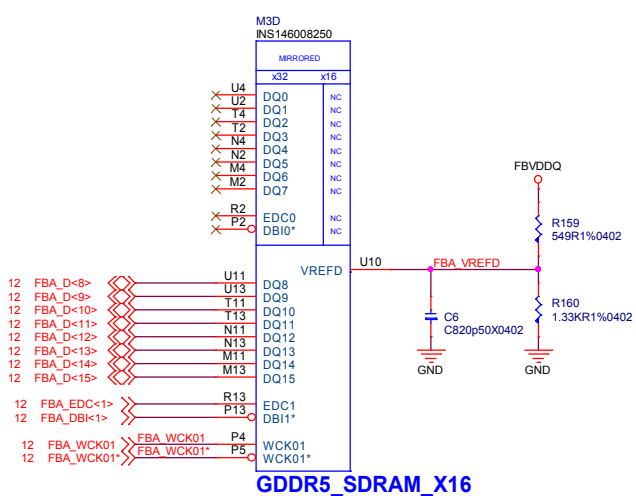


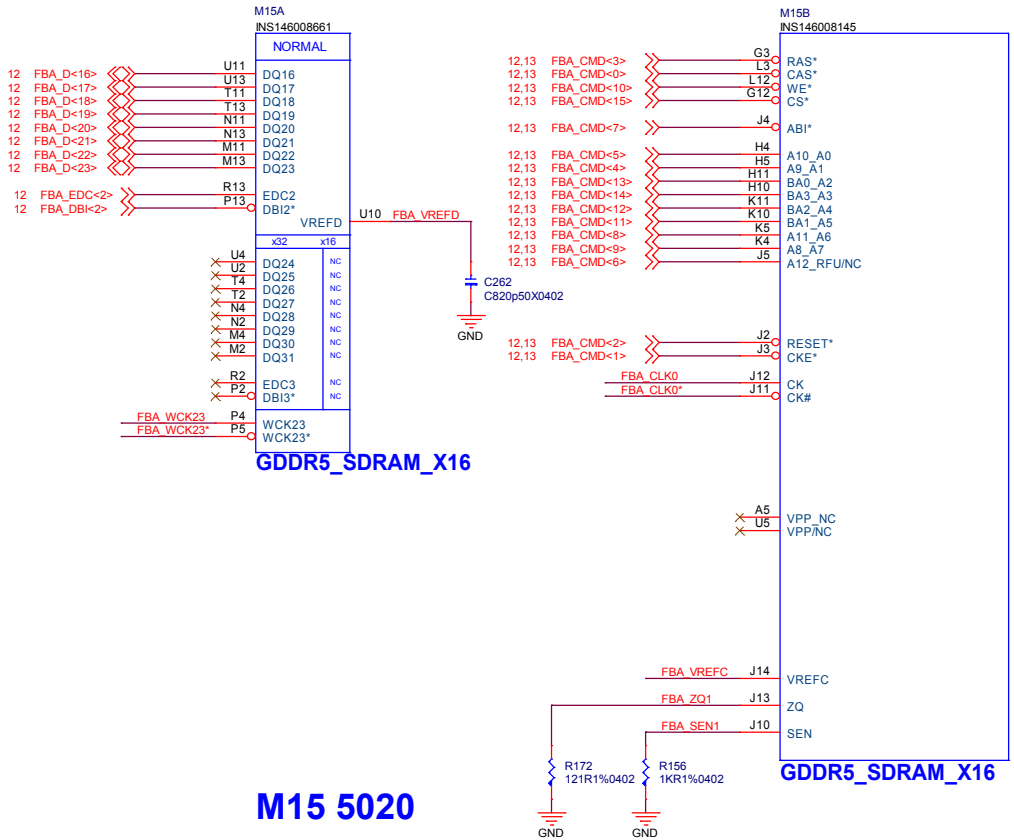
Title			
MICRO-STAR INT'L CO.,LTD.			
DGPU_MEM IF A/B			
Size	Document Number		Rev
	MS-16H5		1.2
Date:	Thursday, August 21, 2014	Sheet 12 of 72	

DGPU_GDDR5 FrameBuffer A0

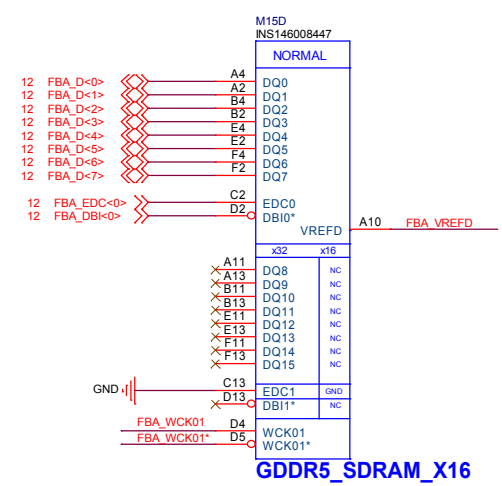


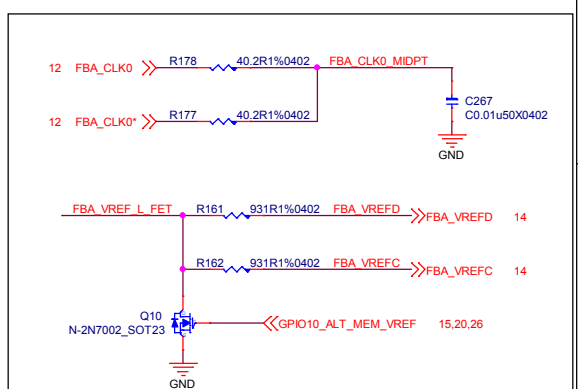
M3 5010





M15 5020





MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FrameBuffer A0	
Size	Document Number MS-16H5	Rev 1.2
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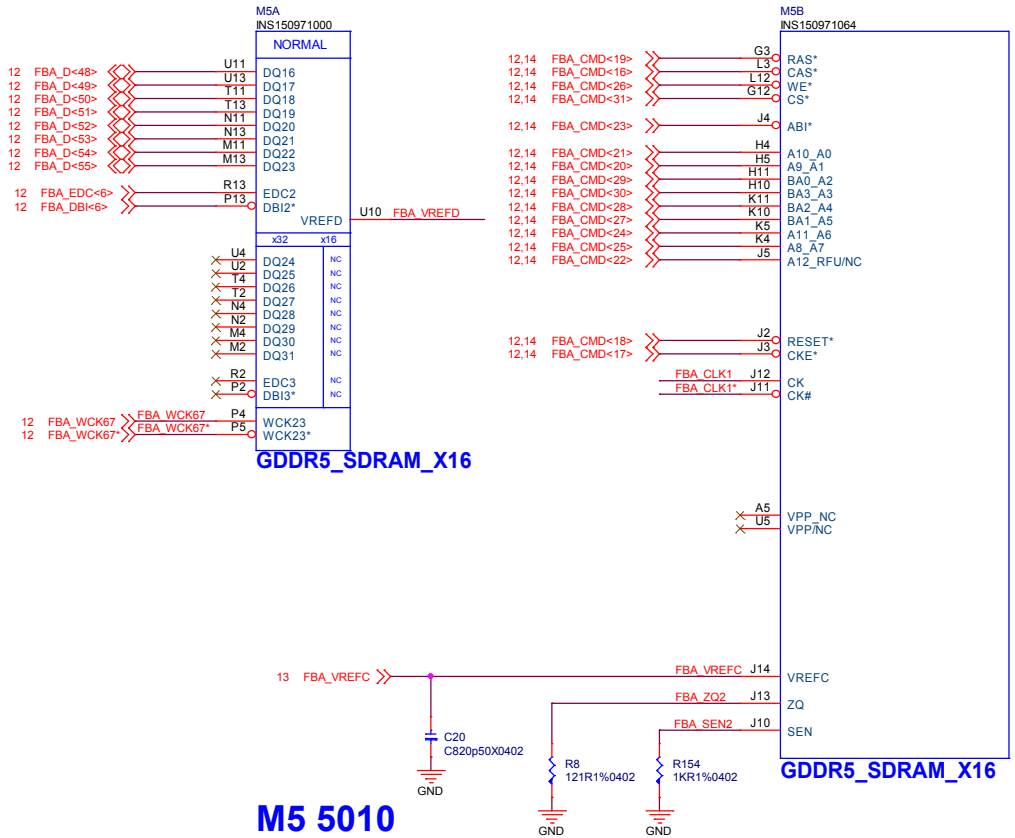
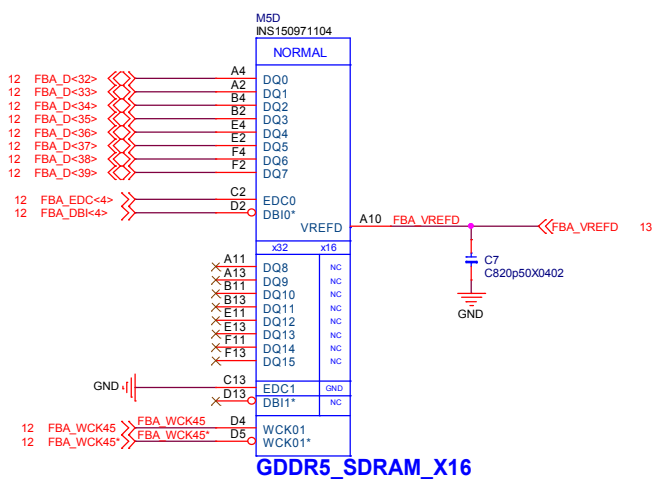
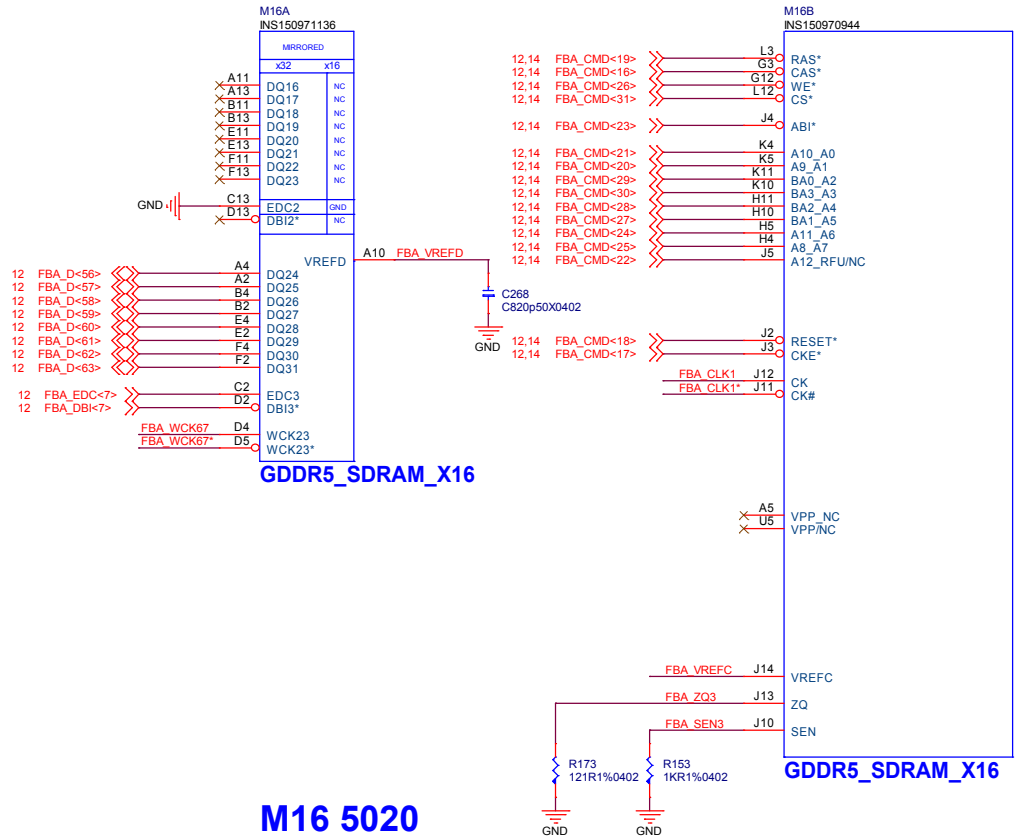
DGPU_GDDR5 FrameBuffer A1

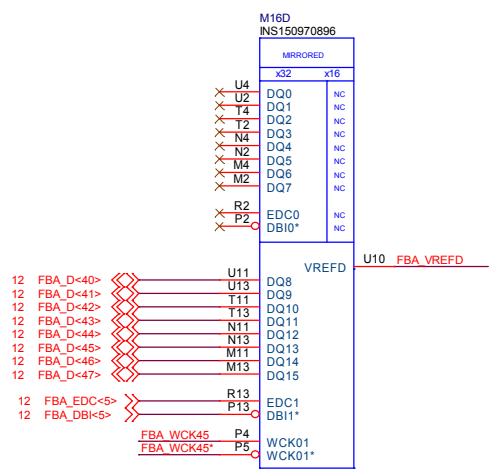


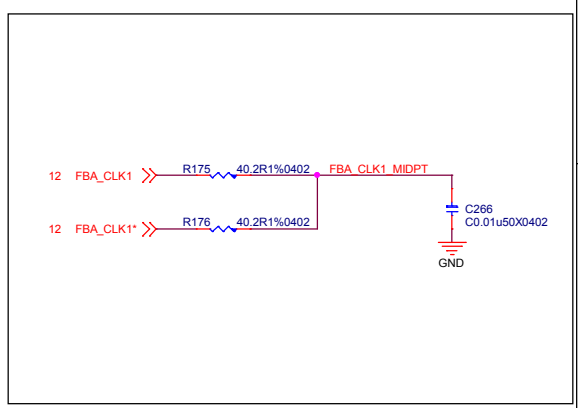
M5 5010





M16 5020





MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FrameBuffer A1	
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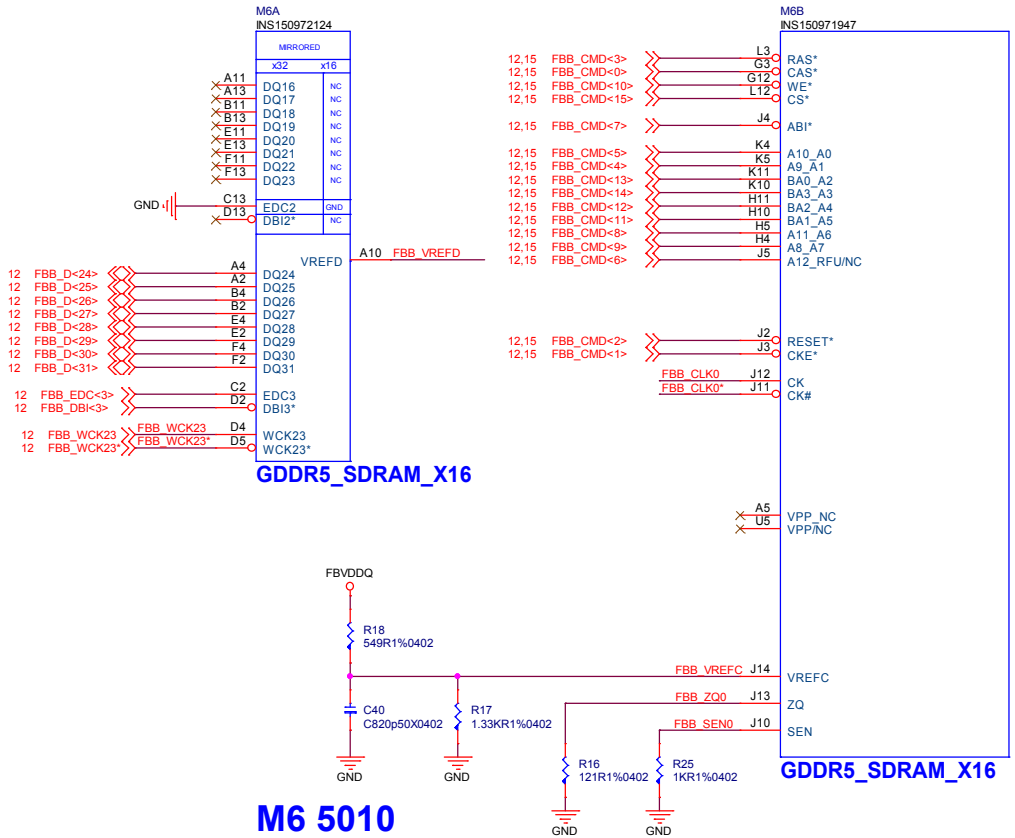
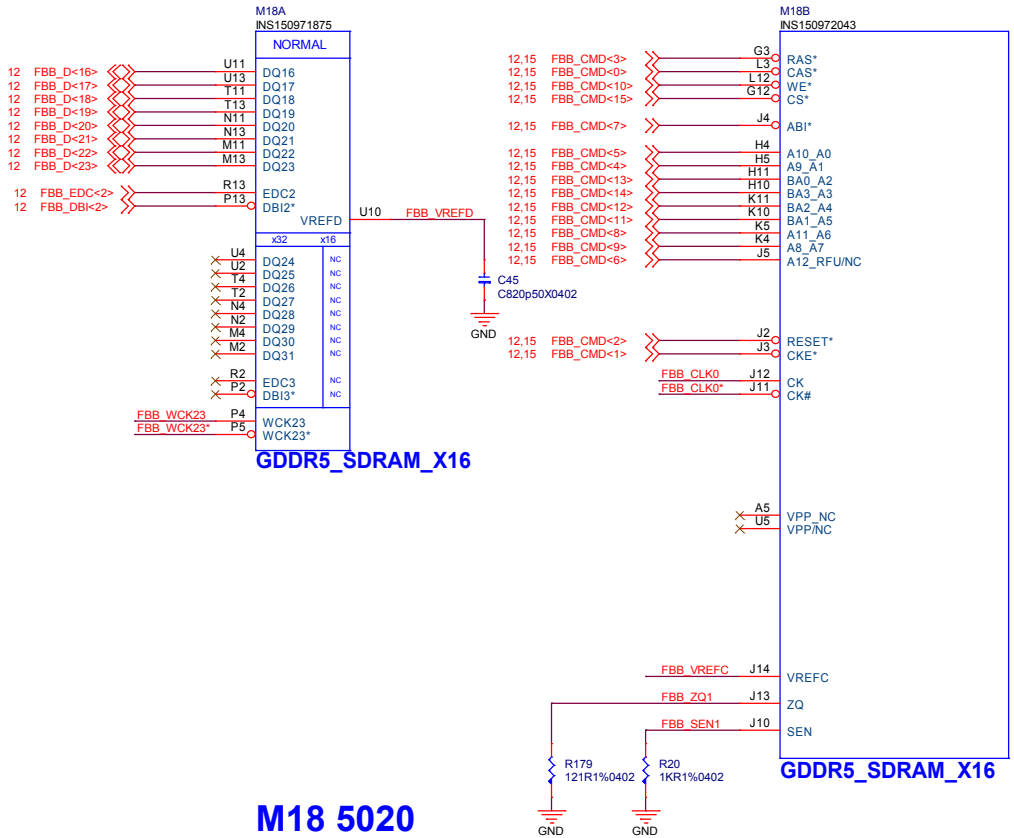
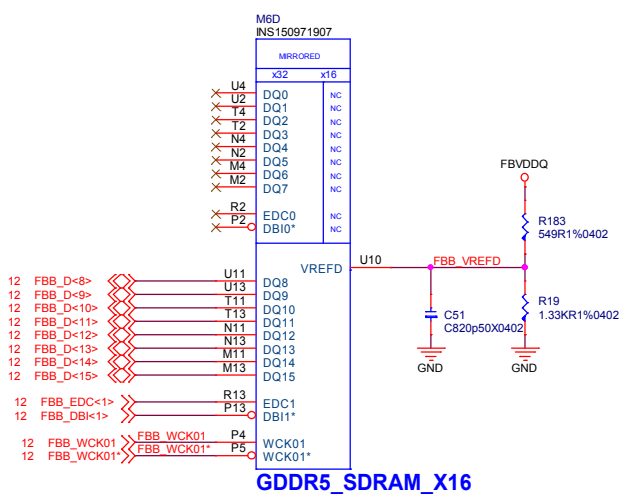
DGPU_GDDR5 FrameBuffer B0

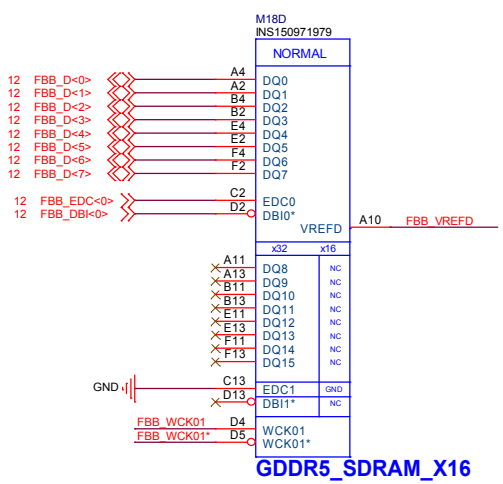


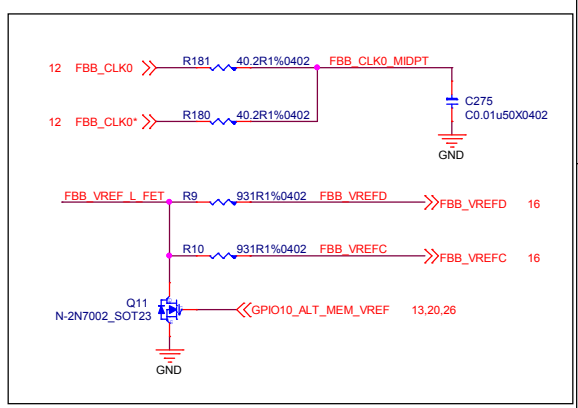


M6 5010

M18 5020







MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FrameBuffer B0	
Size	Document Number MS-16H5	Rev 1.2
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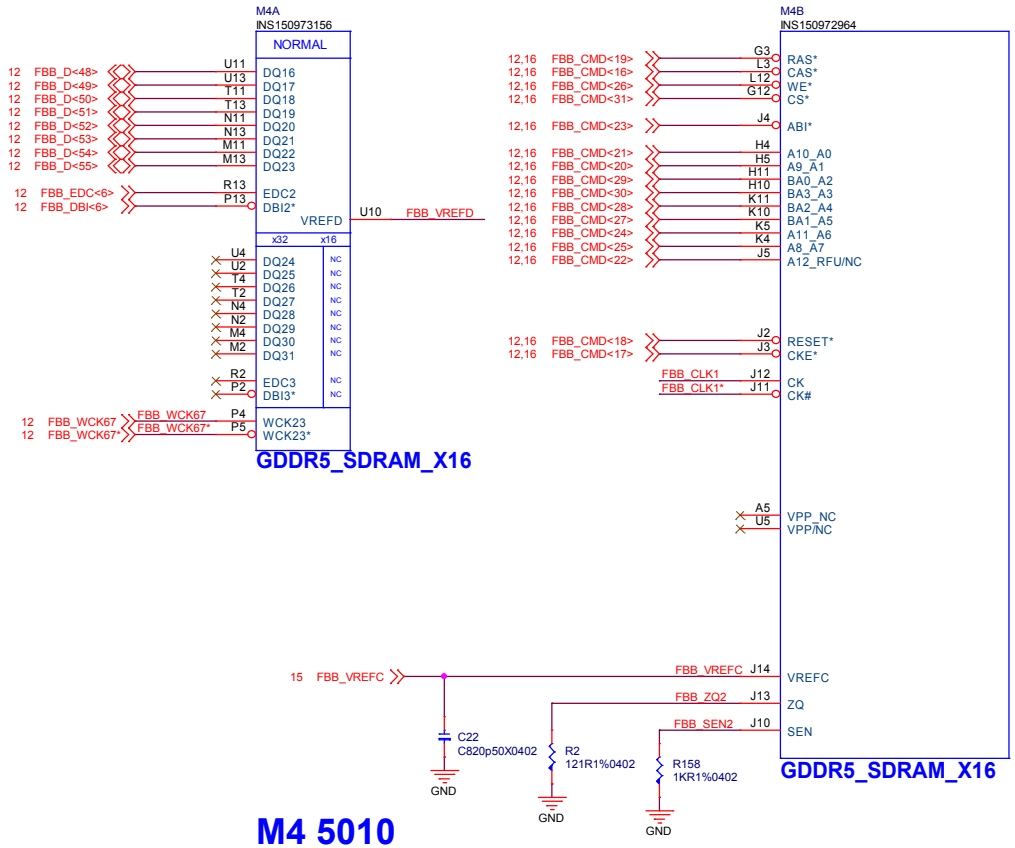
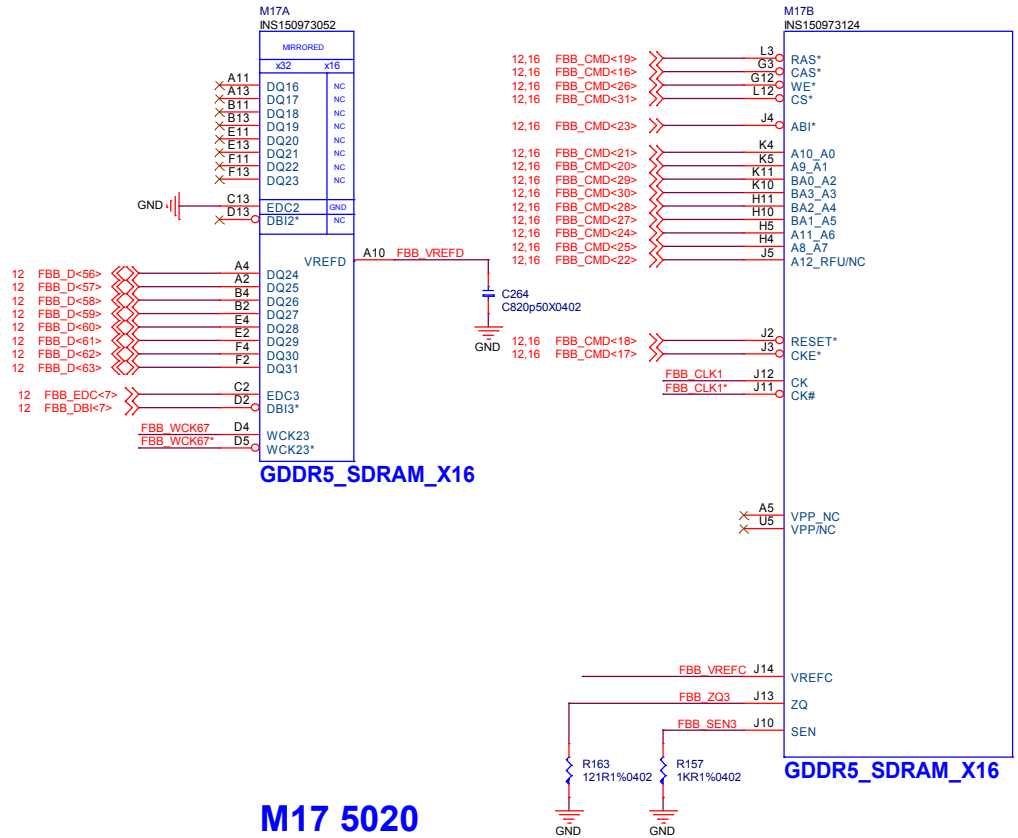
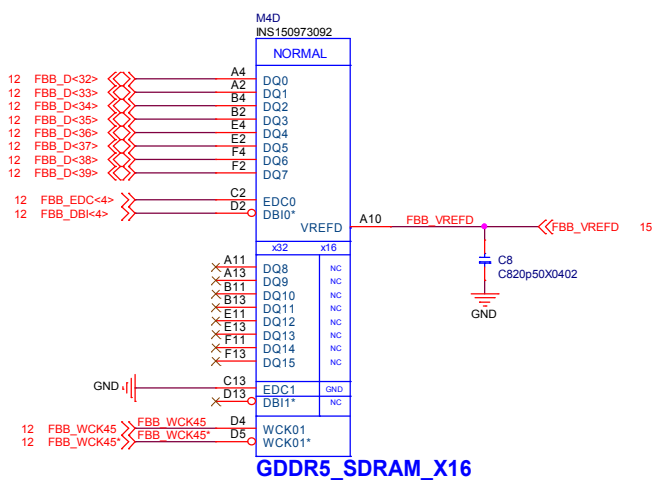
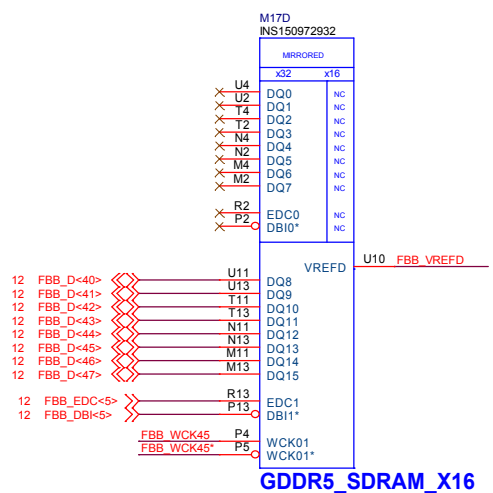
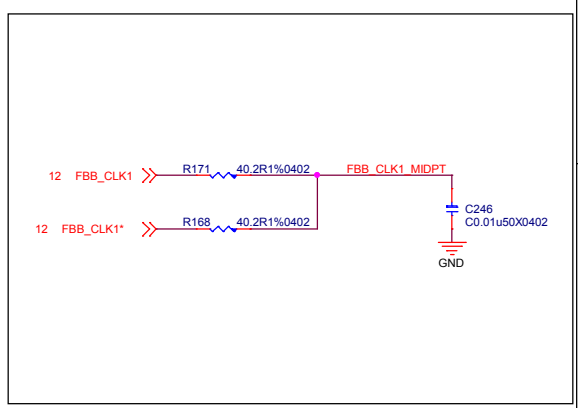
DGPU_GDDR5 FrameBuffer B1











MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FrameBuffer B1	
Size	Document Number: MS-16H5	Rev: 1.2
Date: Thursday, August 21, 2014	Sheet 16 of 72	

Frame Buffer Partition A Decoupling

FBVDDQ

SPARE

DECOUPLING AROUND FBA MEMORIES (DQ0-DQ31)

C255 C0.1u16X0402 · C240 C0.1u16X0402 · C16 C0.1u16X0402 · C30 C0.1u16X0402 · C27 C1u6.3X60402 · C254 C1u6.3X60402 · C242 C1u6.3X60402 · C15 C1u6.3X60402 · C26 C1u6.3X60402 · C32 C1u6.3X60402 · C260 C4.7u6.3X6S · C237 C4.7u6.3X6S · C35 C4.7u6.3X6S · C12 C4.7u6.3X6S · C233 C10u4X60603 · C9 C10u4X60603

GND

C11-106A233-T04

FBA_MF1 — R170 1KR1%0402 — J1

M15C INS150975090 — Normal — MF (add 1k to VSS) — GDDR5_SDRAM_X16

FBVDDQ — R4 1KR1%0402 — FBA_MF0 J1

M3C INS150975200 — Mirrored — MF (add 1k to VDD) — GDDR5_SDRAM_X16

FBA_MF2 — R6 1KR1%0402 — J1

M5C INS150974702 — Normal — MF (add 1k to VSS) — GDDR5_SDRAM_X16

FBVDDQ — R164 1KR1%0402 — FBA_MF3 J1

M16C INS150974972 — Mirrored — MF (add 1k to VDD) — GDDR5_SDRAM_X16

GND

FBVDDQ

SPARE

DECOUPLING AROUND FBA MEMORIES (DQ32-DQ63)

C23 C0.1u16X0402 · C243 C0.1u16X0402 · C31 C0.1u16X0402 · C14 C0.1u16X0402 · C252 C1u6.3X60402 · C256 C1u6.3X60402 · C241 C1u6.3X60402 · C29 C1u6.3X60402 · C253 C1u6.3X60402 · C17 C1u6.3X60402 · C235 C4.7u6.3X6S · C238 C4.7u6.3X6S · C11 C4.7u6.3X6S · C13 C4.7u6.3X6S · C234 C10u4X60603 · C10 C10u4X60603

GND

C11-106A233-T04

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FB-A_DECOUPLING

Size: — Document Number: MS-16H5 — Rev: 1.2

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Frame Buffer Partition B Decoupling

FBVDDQ

SPARE

DECOUPLING AROUND FBB MEMORIES (DQ0-DQ31)

C272 C0.1u16X0402 — C269 C0.1u16X0402 — C24 C0.1u16X0402 — C19 C0.1u16X0402 — C271 C1u6.3X60402 — C250 C1u6.3X60402 — C245 C1u6.3X60402 — C42 C1u6.3X60402 — C43 C1u6.3X60402 — C39 C1u6.3X60402 — C270 C4.7u6.3X6S — C261 C4.7u6.3X6S — C41 C4.7u6.3X6S — C36 C4.7u6.3X6S — C257 C10u4X60603 — C492 C10u4X60603

GND

C11-106A233-T04

FBB_MF1 — R30 1KR1%0402 — J1

M18C INS150977791 — Normal — MF (add 1k to VSS) — GDDR5_SDRAM_X16

FBVDDQ — R31 1KR1%0402 — FBB_MF0 J1

M6C INS150977435 — Mirrored — MF (add 1k to VDD) — GDDR5_SDRAM_X16

FBB_MF2 — R5 1KR1%0402 — J1

M4C INS150977949 — Normal — MF (add 1k to VSS) — GDDR5_SDRAM_X16

FBVDDQ — R167 1KR1%0402 — FBB_MF3 J1

M17C INS150977569 — Mirrored — MF (add 1k to VDD) — GDDR5_SDRAM_X16

FBVDDQ

SPARE

DECOUPLING AROUND FBB MEMORIES (DQ32-DQ63)

C236 C0.1u16X0402 — C251 C0.1u16X0402 — C62 C0.1u16X0402 — C332 C0.1u16X0402 — C347 C1u6.3X60402 — C249 C1u6.3X60402 — C244 C1u6.3X60402 — C18 C1u6.3X60402 — C239 C1u6.3X60402 — C28 C1u6.3X60402 — C263 C4.7u6.3X6S — C335 C4.7u6.3X6S — C37 C4.7u6.3X6S — C64 C4.7u6.3X6S — C288 C10u4X60603 — C258 C10u4X60603

GND

C11-106A233-T04

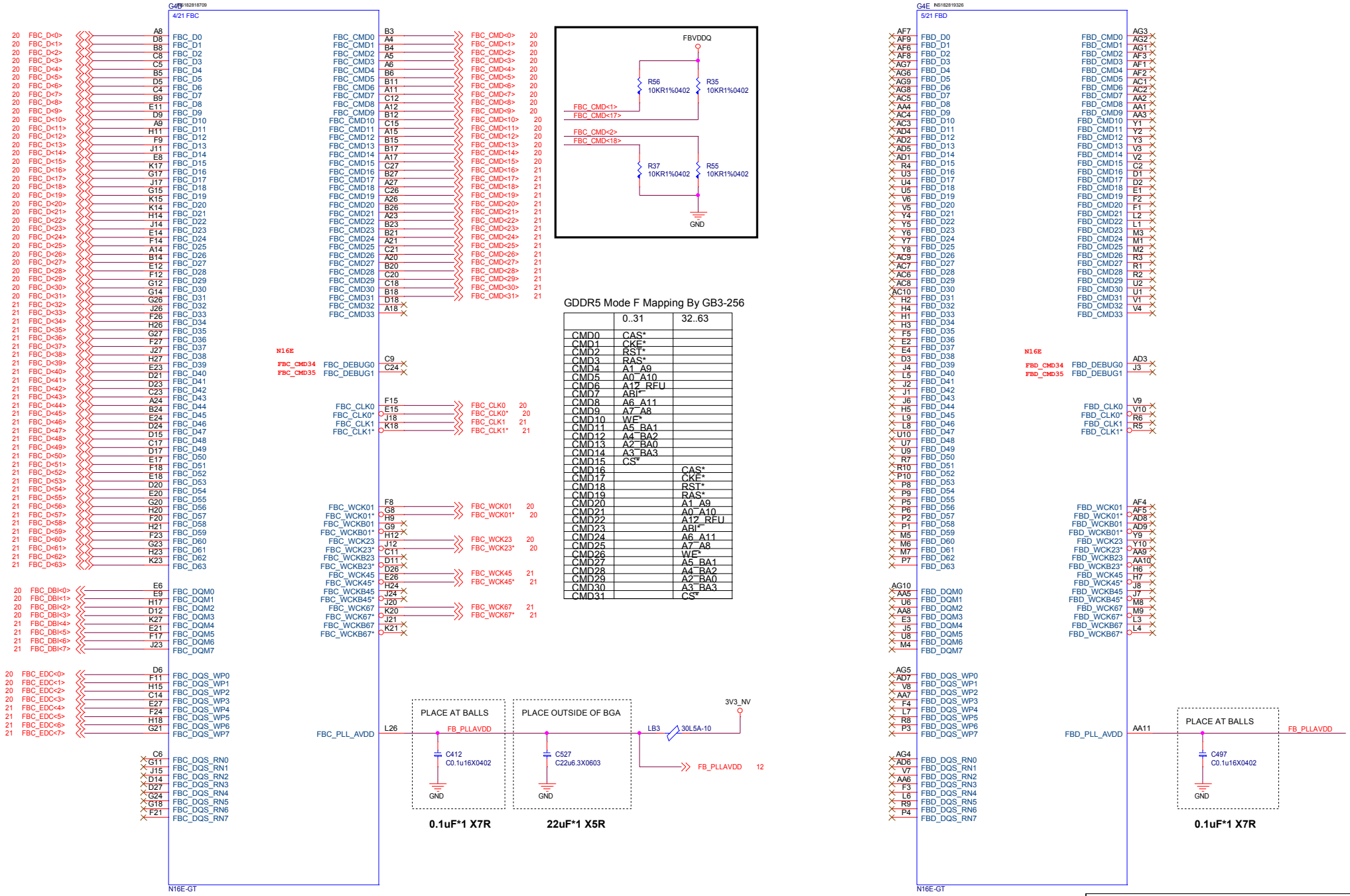
MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FB-B_DECOUPLING

Size: — Document Number: MS-16H5 — Rev: 1.2

Date: Thursday, August 21, 2014 — Sheet 18 of 72

GPU Frame Buffer Partition C/D



MICRO-STAR INT'L CO.,LTD.

Title: DGPU_MEM IF C/D

Size: | Document Number: MS-16H5 | Rev: 1.2

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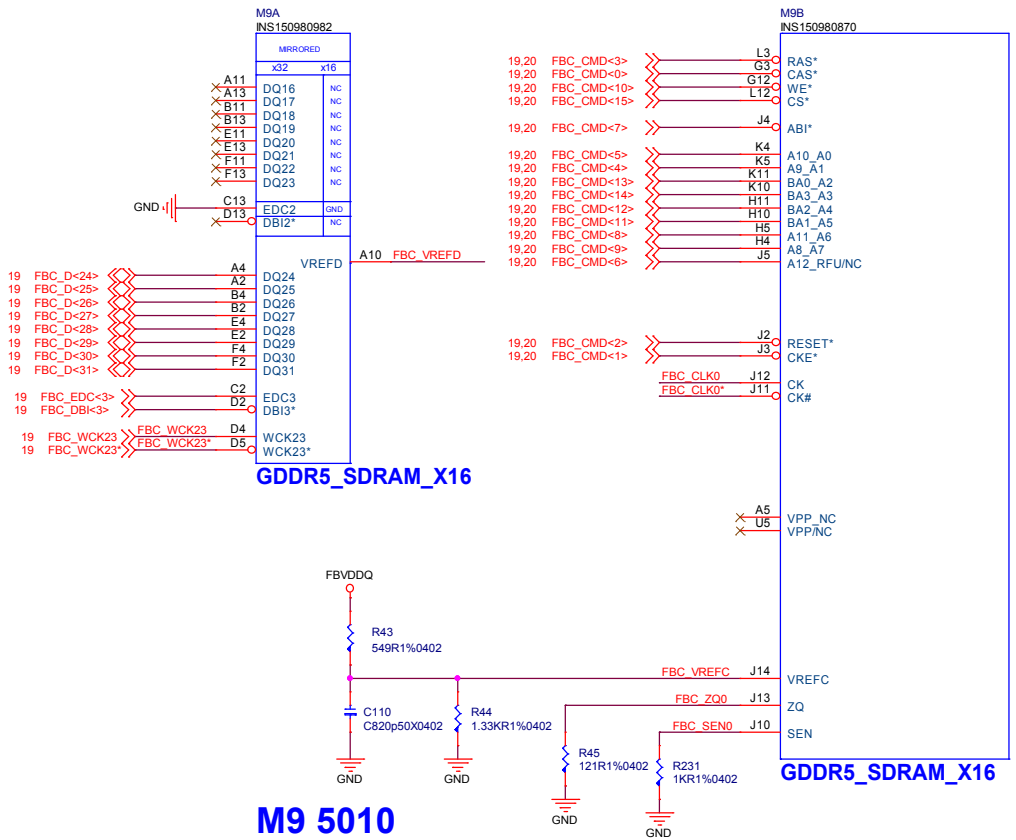
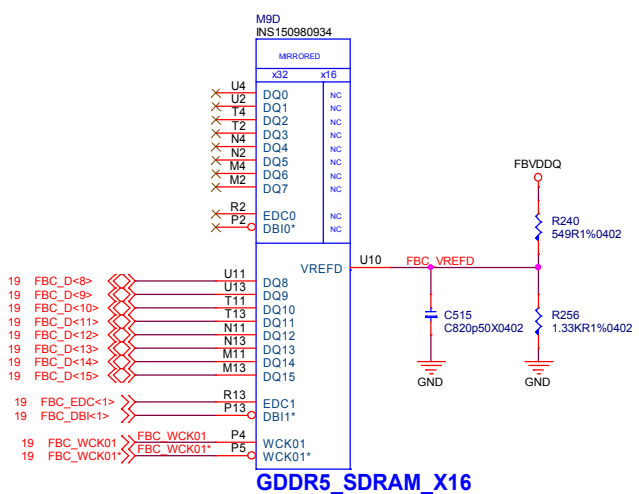
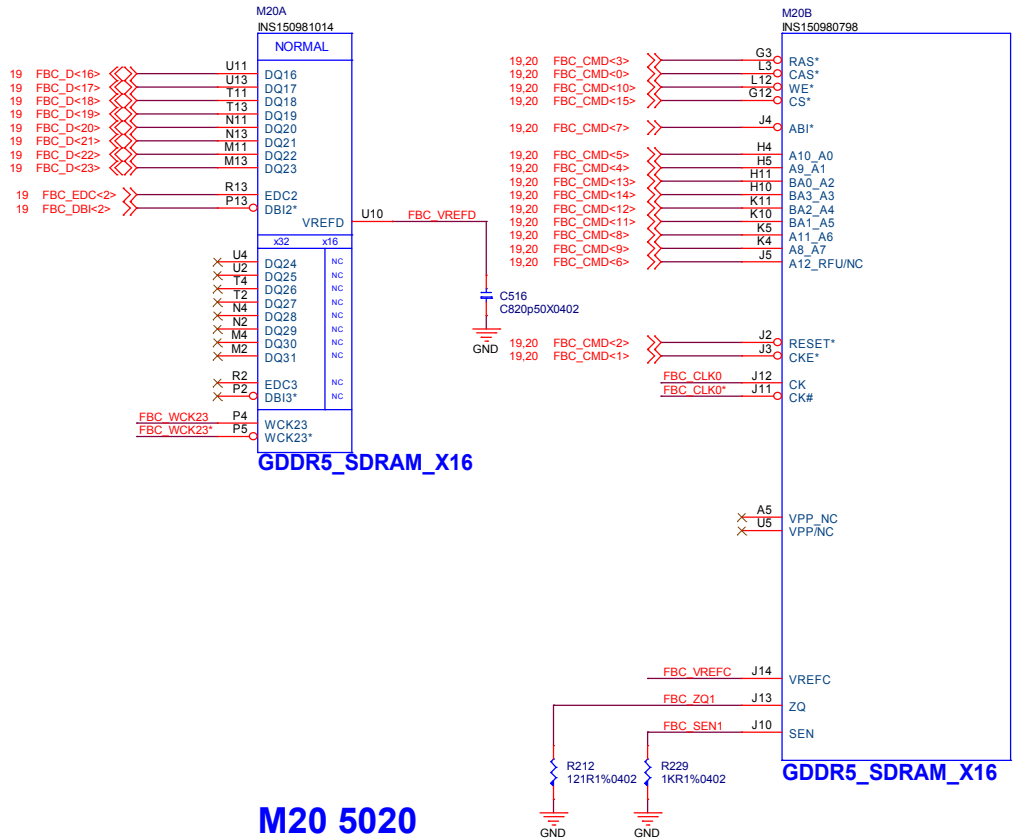
DGPU_GDDR5 FrameBuffer C0

(N16P-GX-B ALL unstuff)

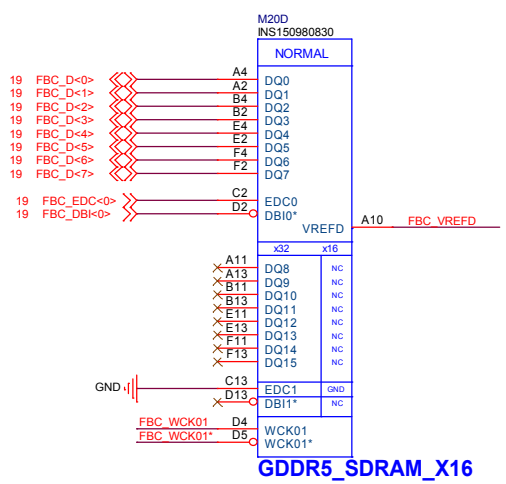


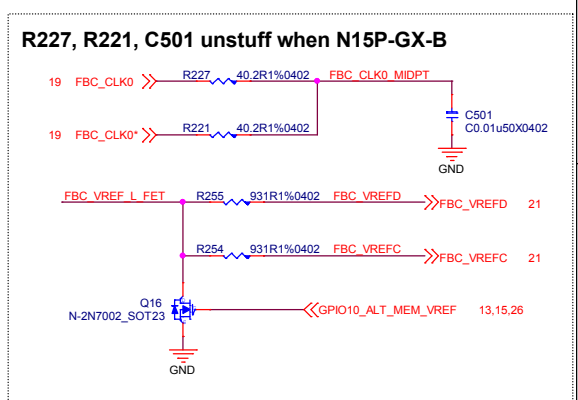
M9 5010





M20 5020

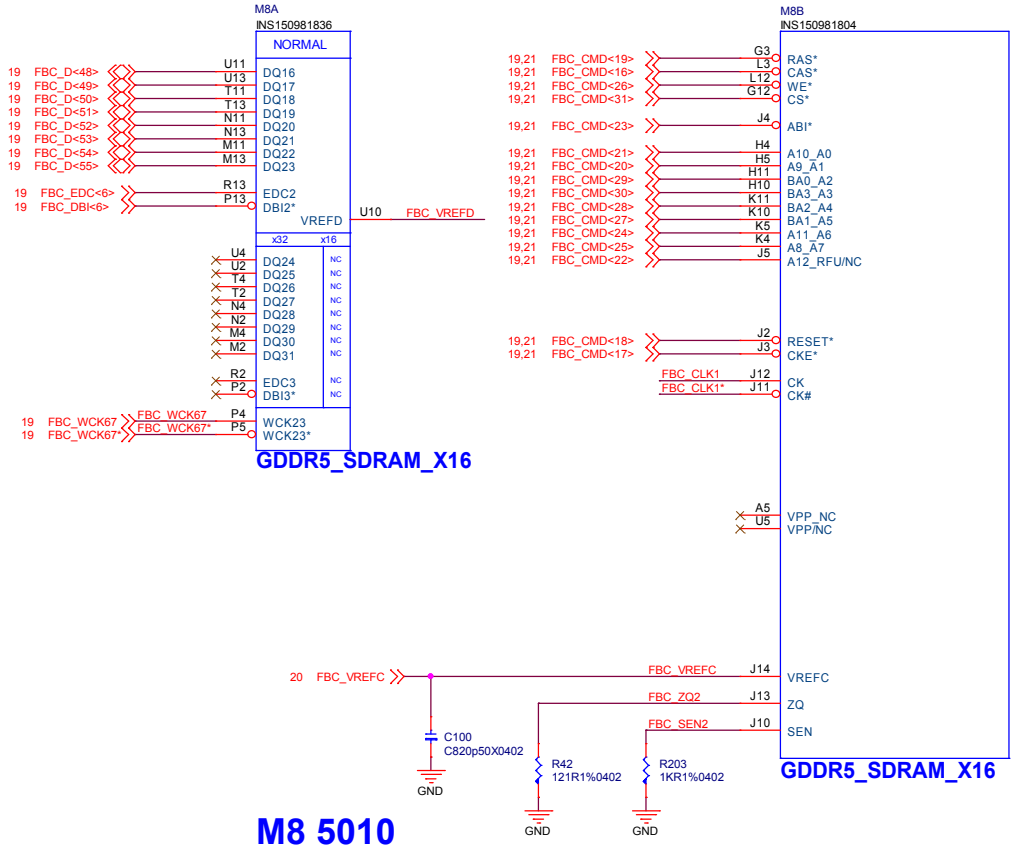


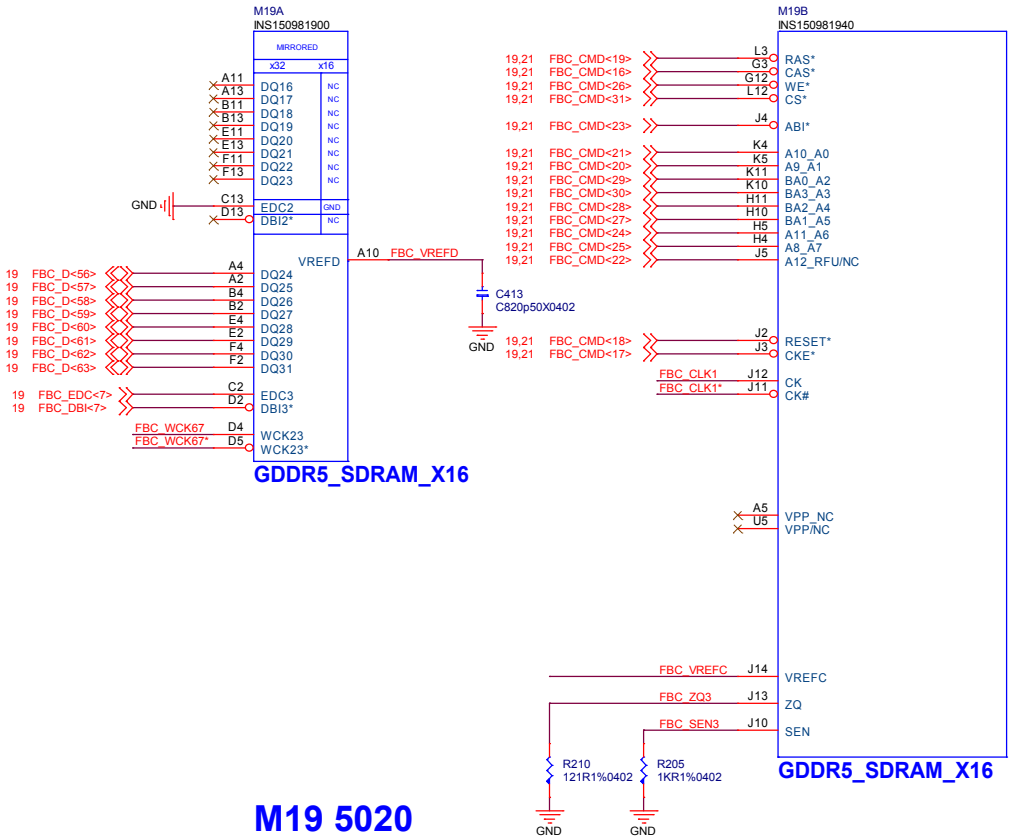


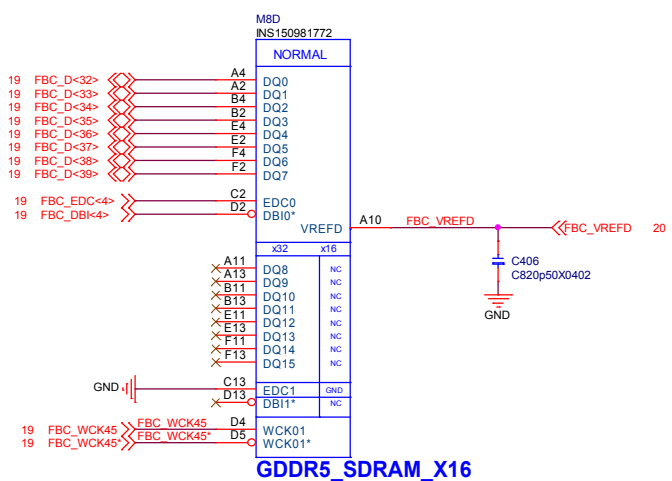
MICRO-STAR INT'L CO.,LTD.		
Title: DGPU_GDDR5 FrameBuffer C		
Size	Document Number: MS-16H5	Rev: 1.2
Date: Thursday, August 21, 2014	Sheet 20 of 72	

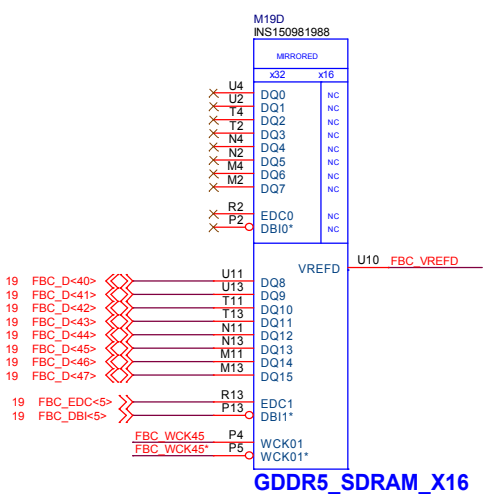
DGPU_GDDR5 FrameBuffer C1

(N16P-GX-B ALL unstuff)

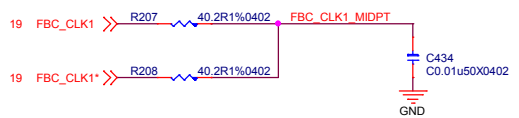








R227, R221, C501 unstuff when N15P-GX-B



MICRO-STAR INT'L CO.,LTD.			
Title: DGPU_GDDR5 FrameBuffer C			
Size	Document Number: MS-16H5		Rev: 1.2
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Frame Buffer Partition C Decoupling

(N16P-GX-B ALL unstuff)

FBVDDQ

SPARE

DECOUPLING AROUND FBC MEMORIES (DQ0-DQ31)

C333 C0.1u16X0402 — C337 C0.1u16X0402 — C99 C0.1u16X0402 — C102 C0.1u16X0402 — C338 C1u6.3X60402 — C461 C1u6.3X60402 — C462 C1u6.3X60402 — C68 C1u6.3X60402 — C69 C1u6.3X60402 — C61 C1u6.3X60402 — C530 C4.7u6.3X6S — C65 C4.7u6.3X6S — C67 C4.7u6.3X6S — C124 C4.7u6.3X6S — C334 C10u4X60603 — C66 C10u4X60603

GND

C11-106A233-T04

FBC_MF1 — R248 1KR1%0402 — J1

M20C INS150983487 — Normal — MF (add 1k to VSS)

R61 1KR1%0402 — FBC_MF0 — J1

M9C INS150983985 — Mirrored — MF (add 1k to VDD)

GDDR5_SDRAM_X16

FBC_MF2 — R196 1KR1%0402 — J1

M8C INS150983787 — Normal — MF (add 1k to VSS)

R195 1KR1%0402 — FBC_MF3 — J1

M19C INS150983645 — Mirrored — MF (add 1k to VDD)

GDDR5_SDRAM_X16

DECOUPLING AROUND FBC MEMORIES (DQ32-DQ63)

FBVDDQ

SPARE

C484 C0.1u16X0402 — C483 C0.1u16X0402 — C122 C0.1u16X0402 — C123 C0.1u16X0402 — C528 C1u6.3X60402 — C101 C1u6.3X60402 — C529 C1u6.3X60402 — C109 C1u6.3X60402 — C111 C1u6.3X60402 — C112 C1u6.3X60402 — C476 C4.7u6.3X6S — C475 C4.7u6.3X6S — C106 C4.7u6.3X6S — C107 C4.7u6.3X6S — C477 C10u4X60603 — C105 C10u4X60603

GND

C11-106A233-T04

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FB-C_DECOUPLING

Size: | Document Number: MS-16H5 | Rev: 1.2

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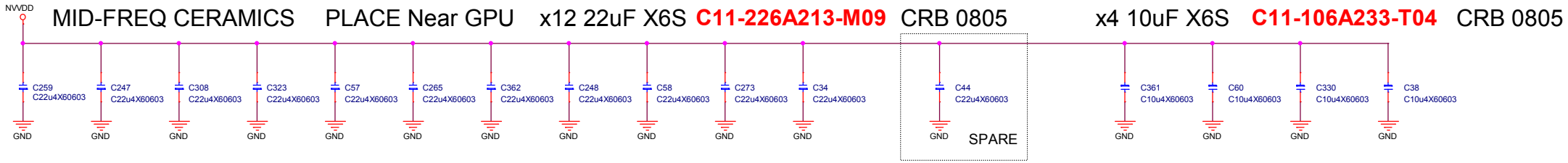
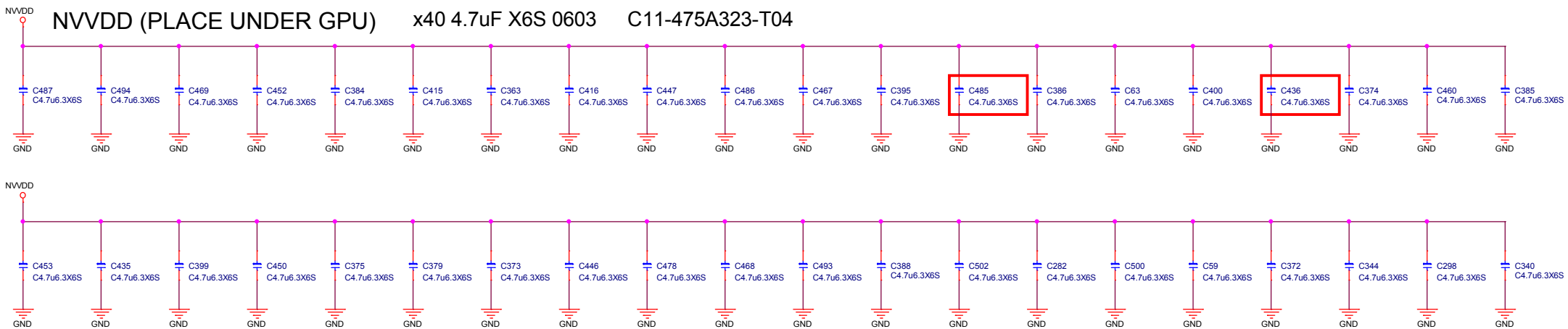
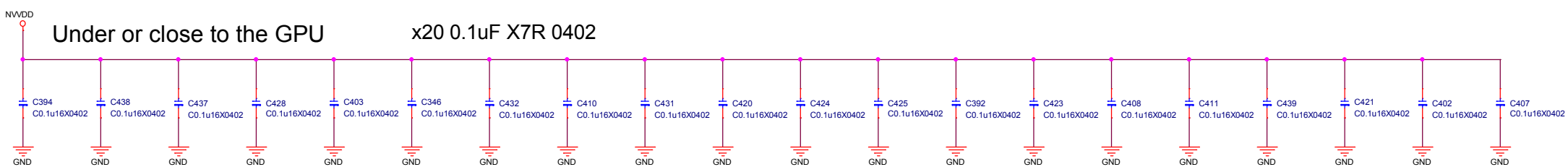
GPU DECOUPLING A







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Title	DGPU_GPU DECOUPLING A	
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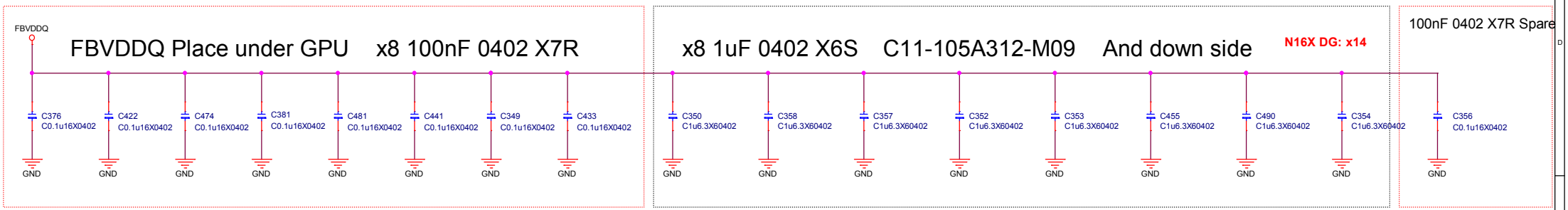
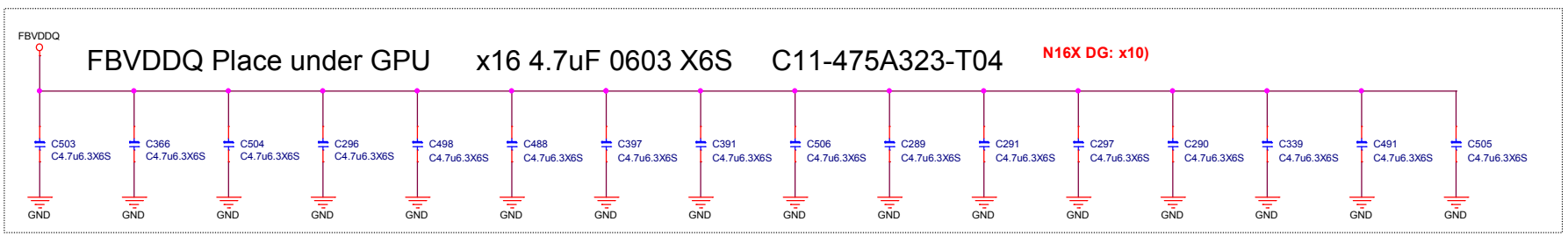
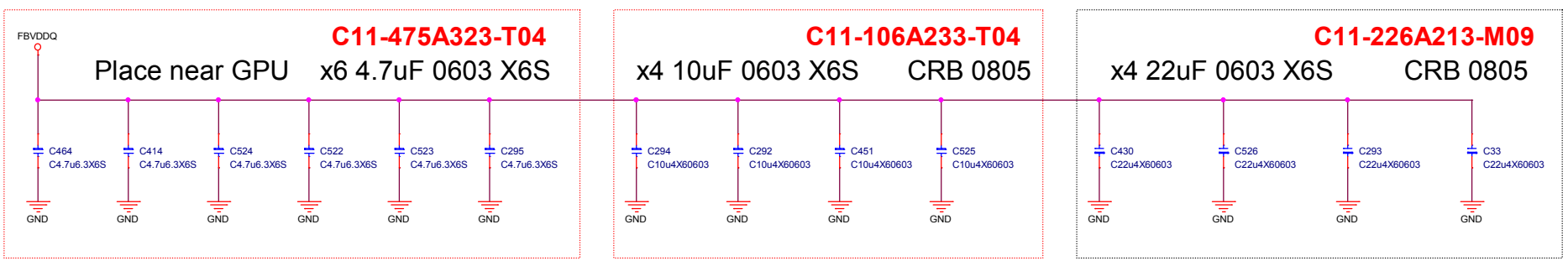
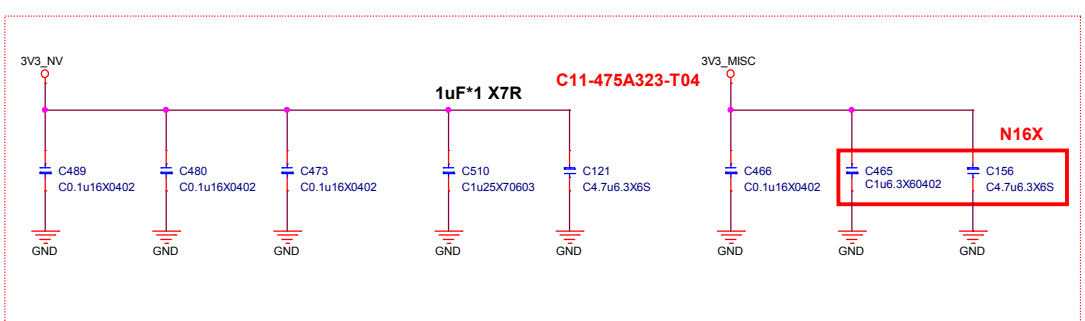
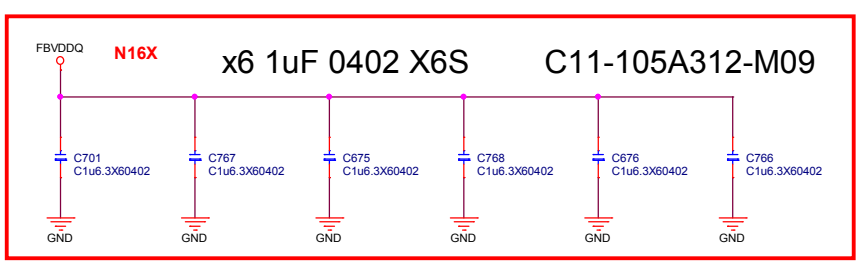
GPU DECOUPLING B











MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GPU DECOUPLING B	
Size	Document Number MS-16H5	Rev 1.2
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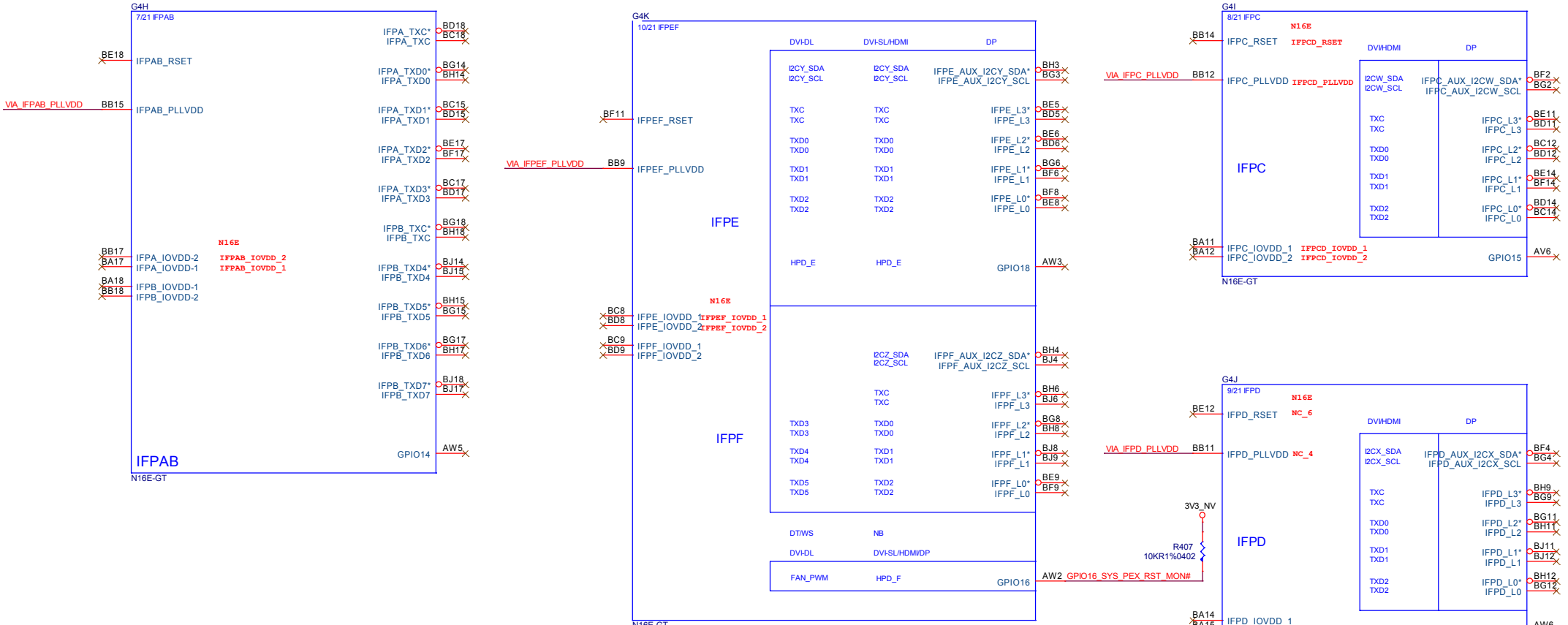
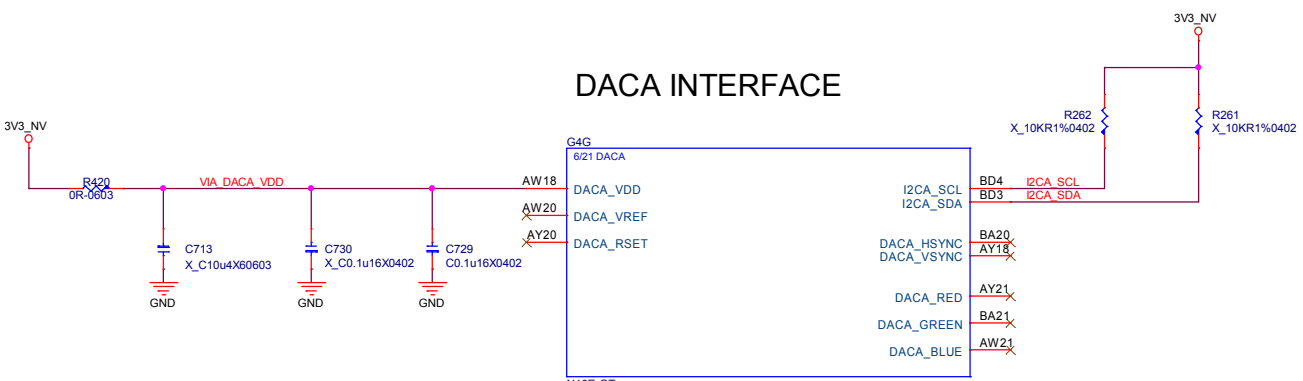
DACA,Display IF

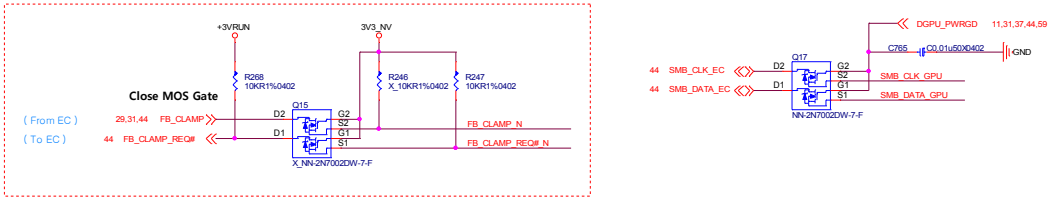


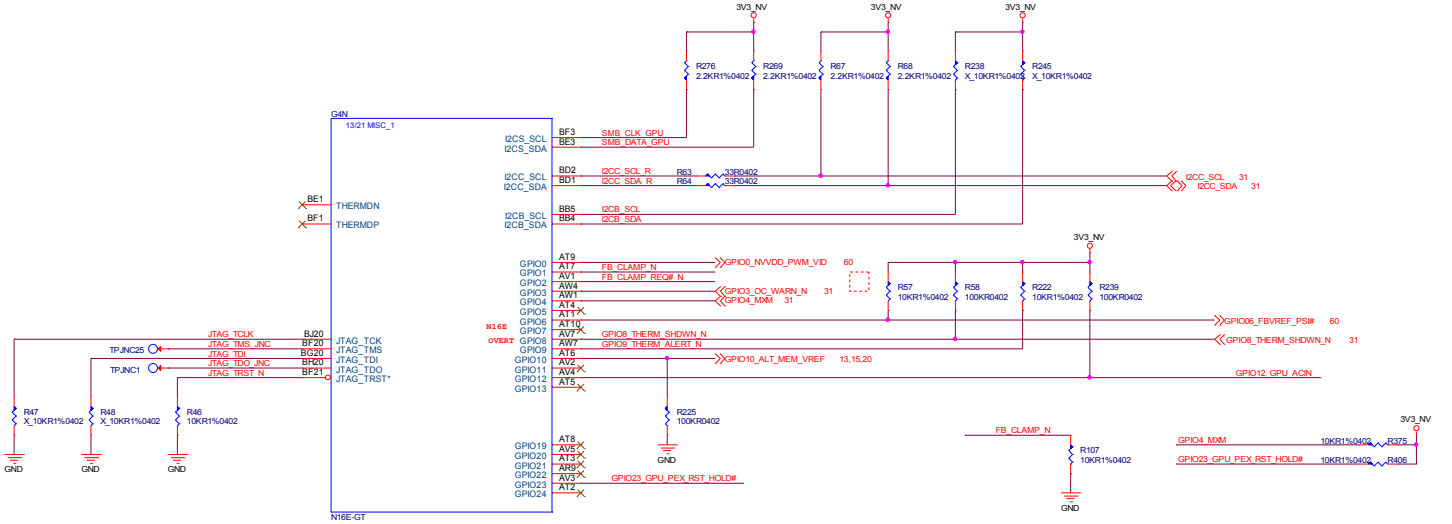
DACA INTERFACE



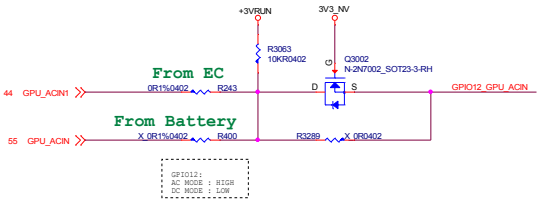
MICRO-STAR INT'L CO.,LTD.		
Title: DGPU_DACA,Display IF		
Size	Document Number: MS-16H5	Rev: 1.2
Date: Thursday, August 21, 2014	Sheet 25 of 72	

DGPU GPIO, I2C





Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWR_VID	O	GPU Core VDD PWM control signal	
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.0	10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10K pull-up to 3V3 _AON
GPIO3	OC_WARN	I	Over current throttling	10K pull-up to 3V3 _AON
GPIO4	3V3_MAIN_EN	O	GPU POWER Sequencing for GC6 2.0	10K pull-up to 3V3 _AON
GPIO5	RESERVED			
GPIO6	PSI	O	Phase shedding	
GPIO7	LCD_BL_PWM	O	Panel Backlight PWM Brighteness Control	100K pull-down
GPIO8	HPD_F	I	Hot Plug Detect for IFPDF	
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	10K pull-up to 3V3 _AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 3V3 _AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IFPAB	
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	
GPIO16	SYS_PEX_RST_MON#	I	System side PCI reset Monitor	10K pull-up to 3V3 _AON
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	
GPIO19	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO20	RESERVED			
GPIO21	SLI_RASTER_SYNC	I	SLI Raster Sync	100K pull-down
GPIO22	SLI_SWAP_DRY	I	SLI Swap Ready	1K pull-up to 3V3 _AON
GPIO23	GPU_PEX_RST_HOLD	O	GPU PCIE self-reset control	10K pull-up to 3V3 _AON
GPIO24	MEM_VDD_CTL	O	Memory VDD VID	
GPIO25	RESERVED			
GPIO26	RESERVED			
GPIO27	HPD_B	I	Hot Plug Detect for IFPB	
OVERT	OVERT(OVERT#)	I/O	Catastrophic Over Temperature	100K pull-up to 3V3 _AON



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Title: DGPU_GPIO,I2C

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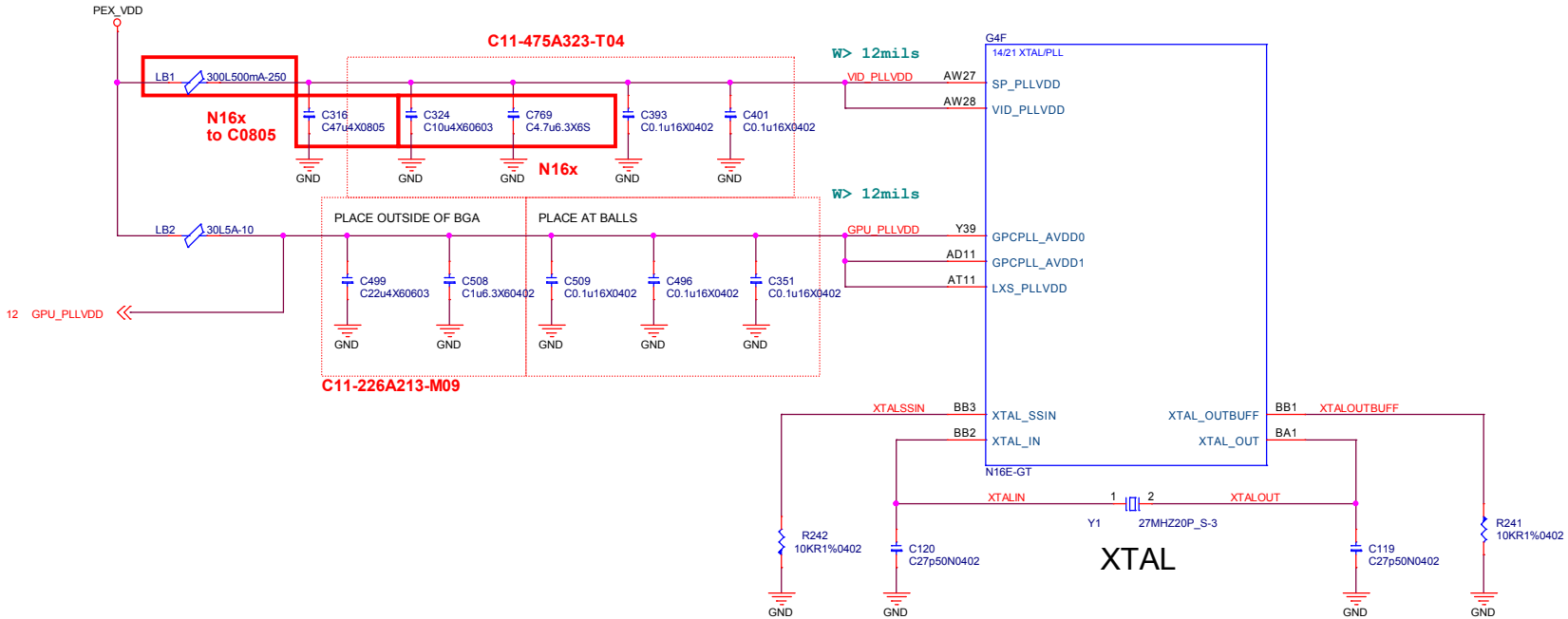
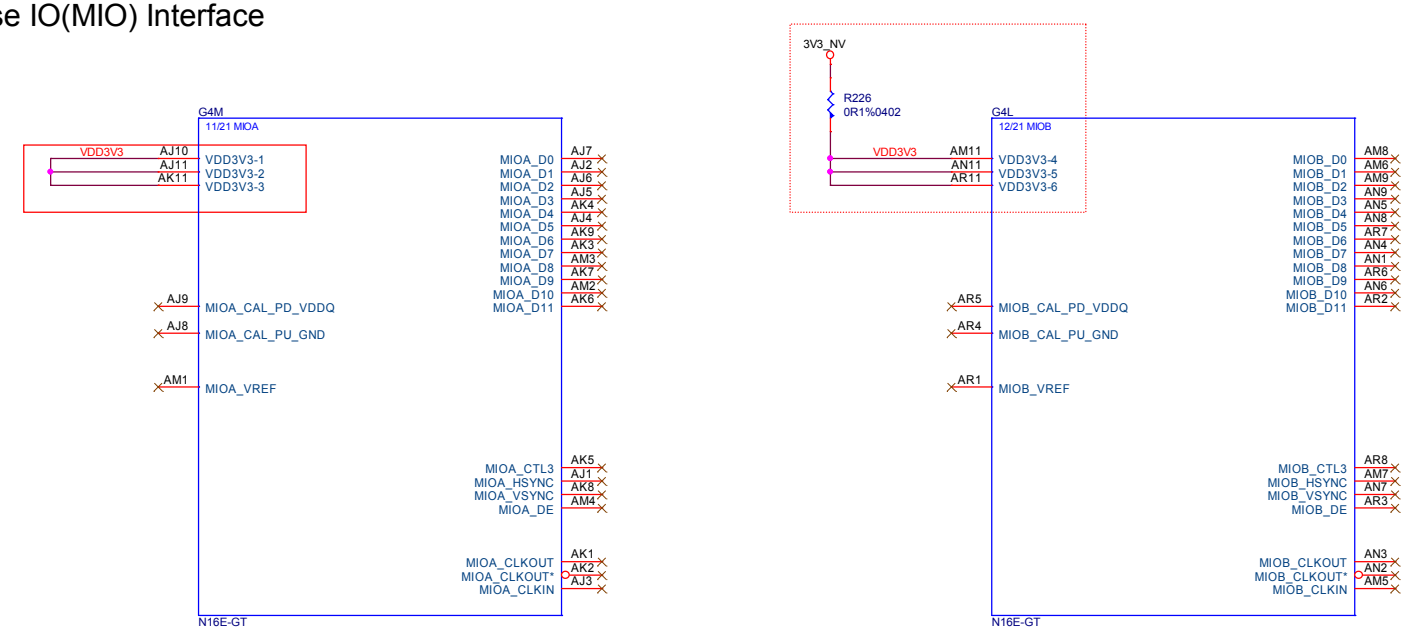
DGPU MIO & XTAL



Multi-use IO(MIO) Interface



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Title	DGPU MIO & XTAL	
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ROM, MULTI-LEVEL STRAPS

	GND	3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111
	PD	PU

ROM_SI10K **Hynix** V_TOP1 V_BOT1

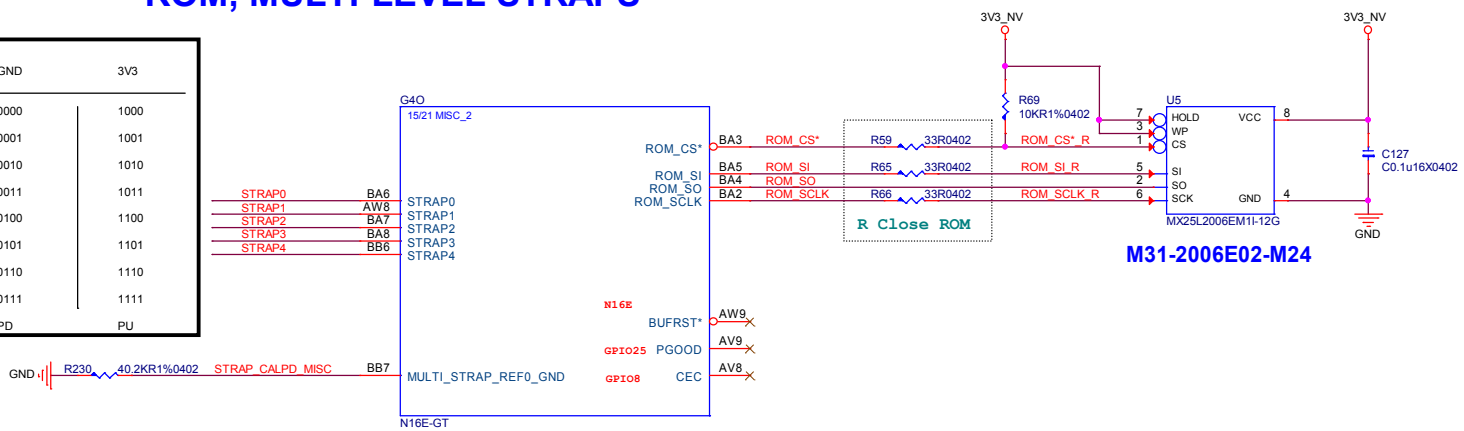
128Mx16bit **5010** **5020**

R11-0103T12-W08	M12-5GC2H05-H23	M12-5GC2H05-H23
X_10KR1%0402	X_H5GC2H24BFR-T2C	X_H5GC2H24BFR-T2C

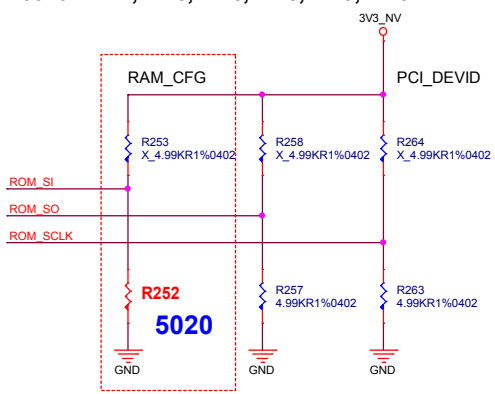
ROM_SI5K **Samsung** V_TOP2 V_BOT2

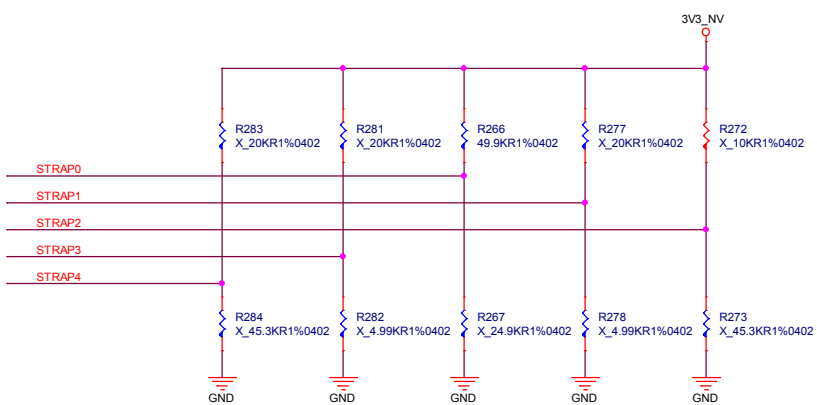
128Mx16bit **5010** **5020**

R11-4991T12-W08	M12-2032585-S02	M12-2032585-S02
X_5KR1%0402	X_K4G20325FD-FC03	X_K4G20325FD-FC03



GDDR5 Parts
5010 : M4 , M3 , M5 , M6 , M8 , M9
5020 : M17, M15, M16, M18, M19, M20





	N16E-GT ES		N16E-GT QS	
ROM_SI	35K PD	Hynix 128x16bit	10K PD	Hynix 128x16bit
	45K PD	Samsung 128x16bit	5K PD	Samsung 128x16bit
ROM_SO	5K PD			
ROM_SCLK	5K PD			
STRAP0	50K PU 3V3_AON			
STRAP1	Reserved			
STRAP2	Reserved			
STRAP3	Reserved			
STRAP4	Reserved			

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_ROM,HW Straps

Size | Document Number: MS-16H5 | Rev: 1.2

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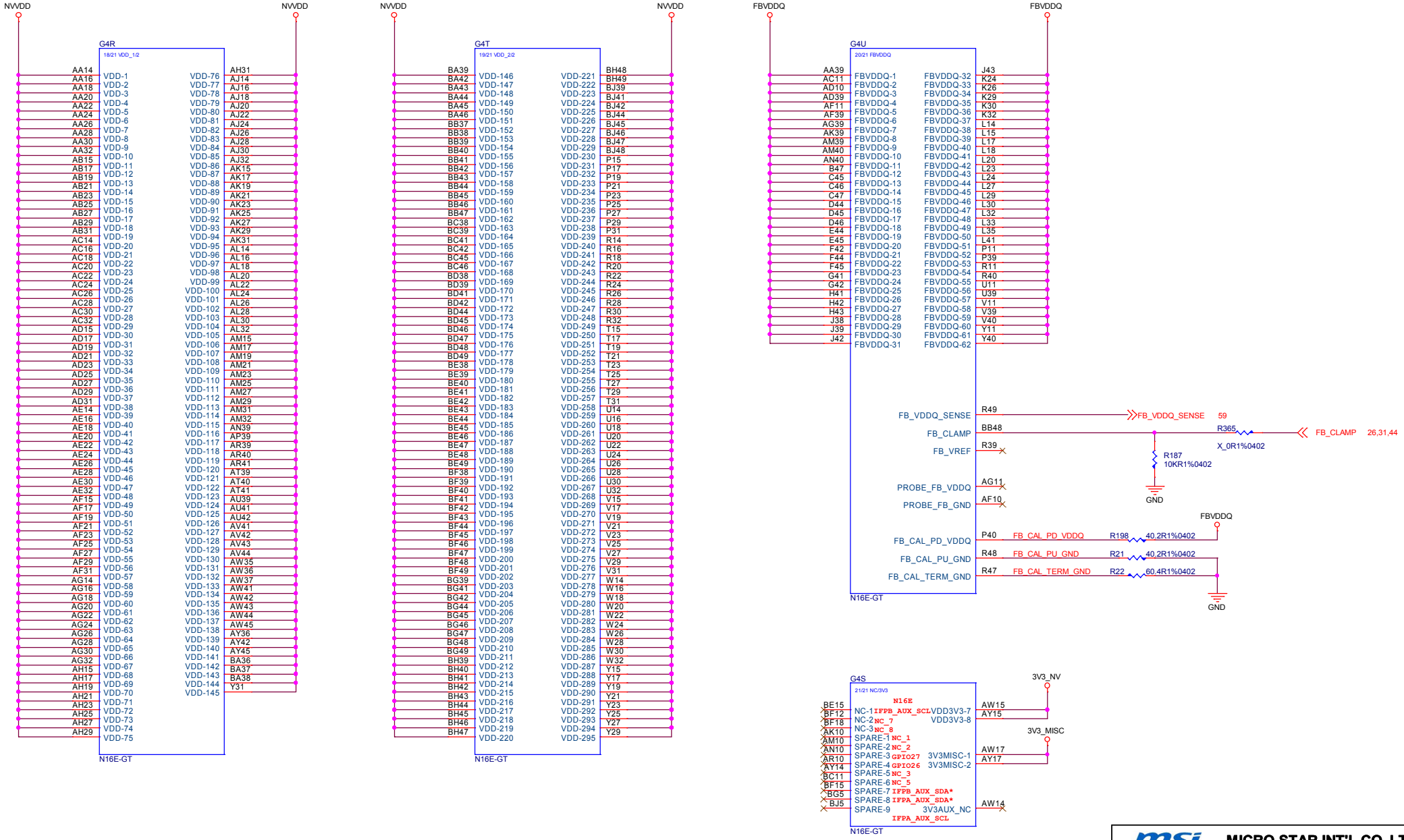
GPU NVVDD, FBVDDQ



Title	DGPU NVVDD, FBVDDQ
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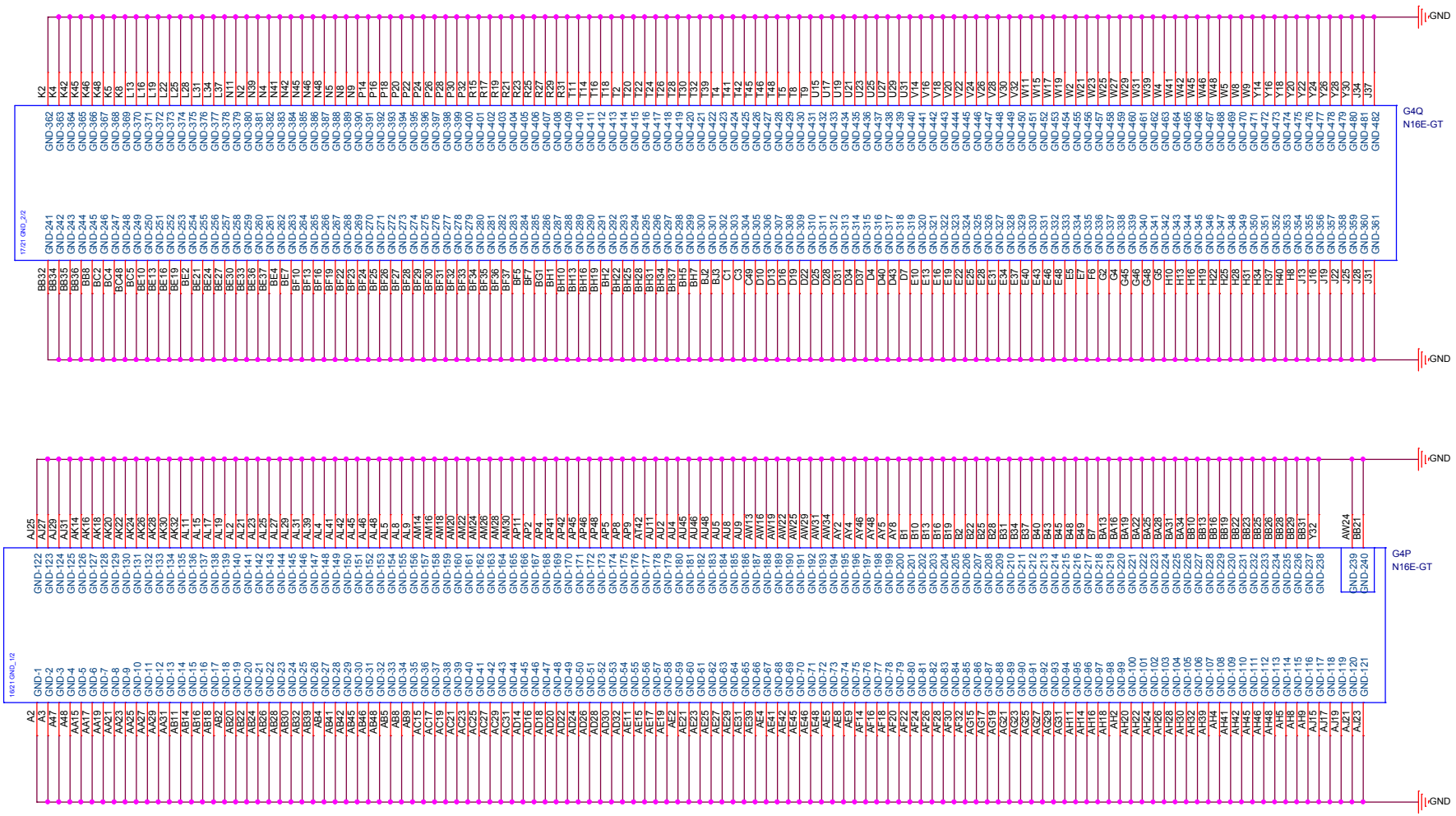
MICRO-STAR INT'L CO.,LTD.

DGPU GND



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	DGPU GND		
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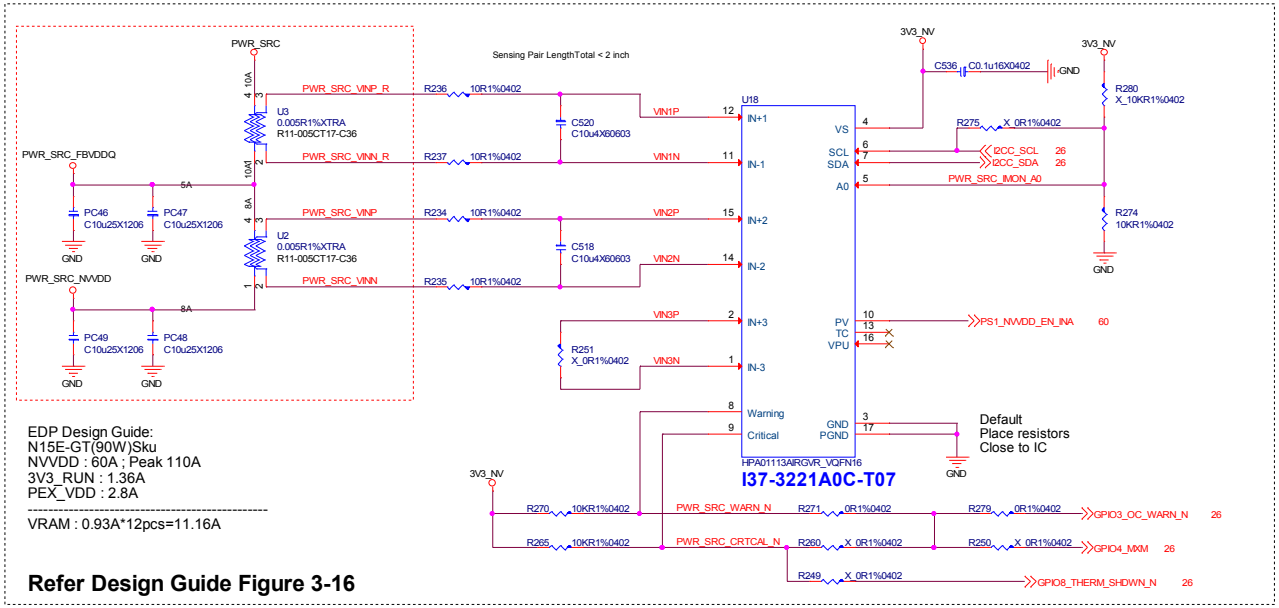
DGPU_Power Control

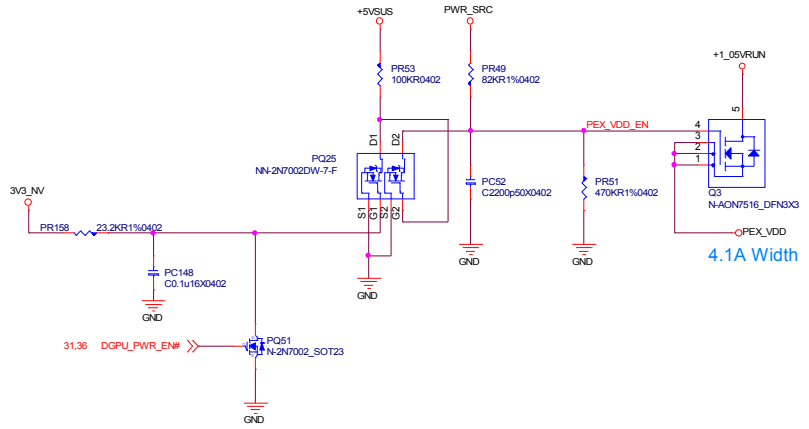


EDP Design Guide:
N15E-GT(90W)Sku
NVVDD : 60A ; Peak 110A
3V3_RUN : 1.36A
PEX_VDD : 2.8A

VRAM : 0.93A*12pcs=11.16A

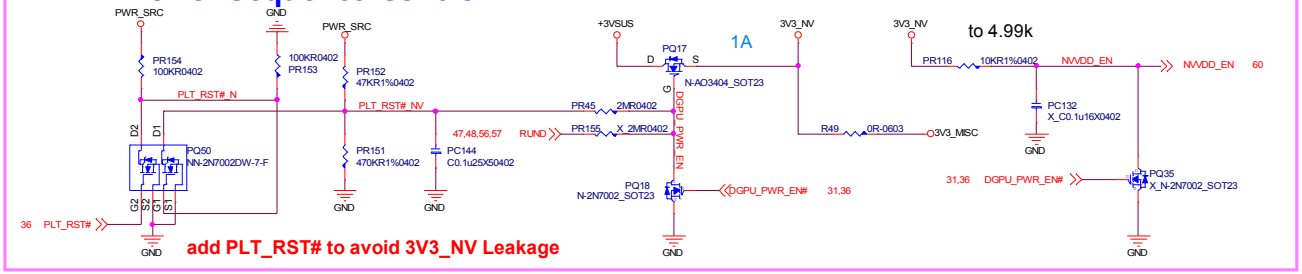
Refer Design Guide Figure 3-16

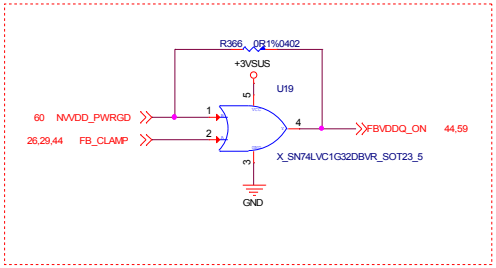
PEX_VDD



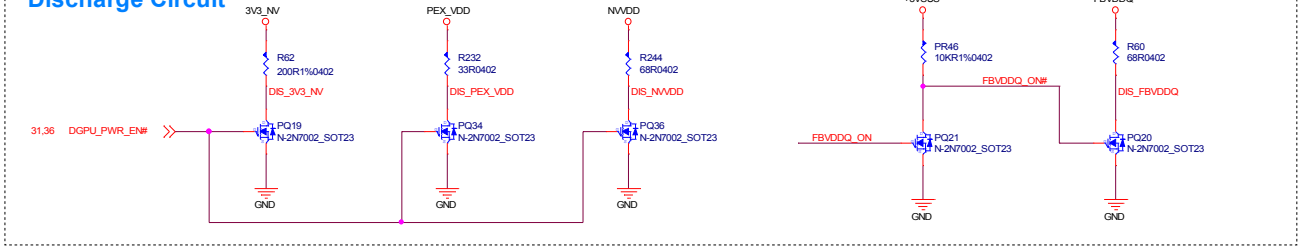
nVIDIA Power Sequence Control

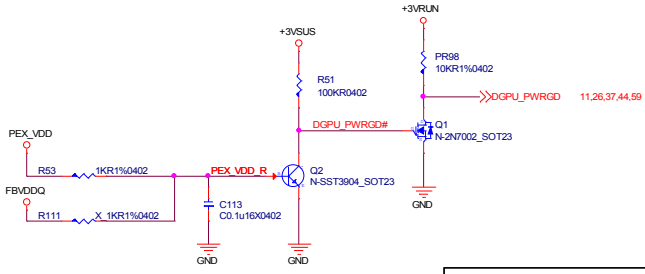
3V3_NV -> NVVDD, PEX_VDD -> FBVDDQ -> DGPUPWRGD





Discharge Circuit



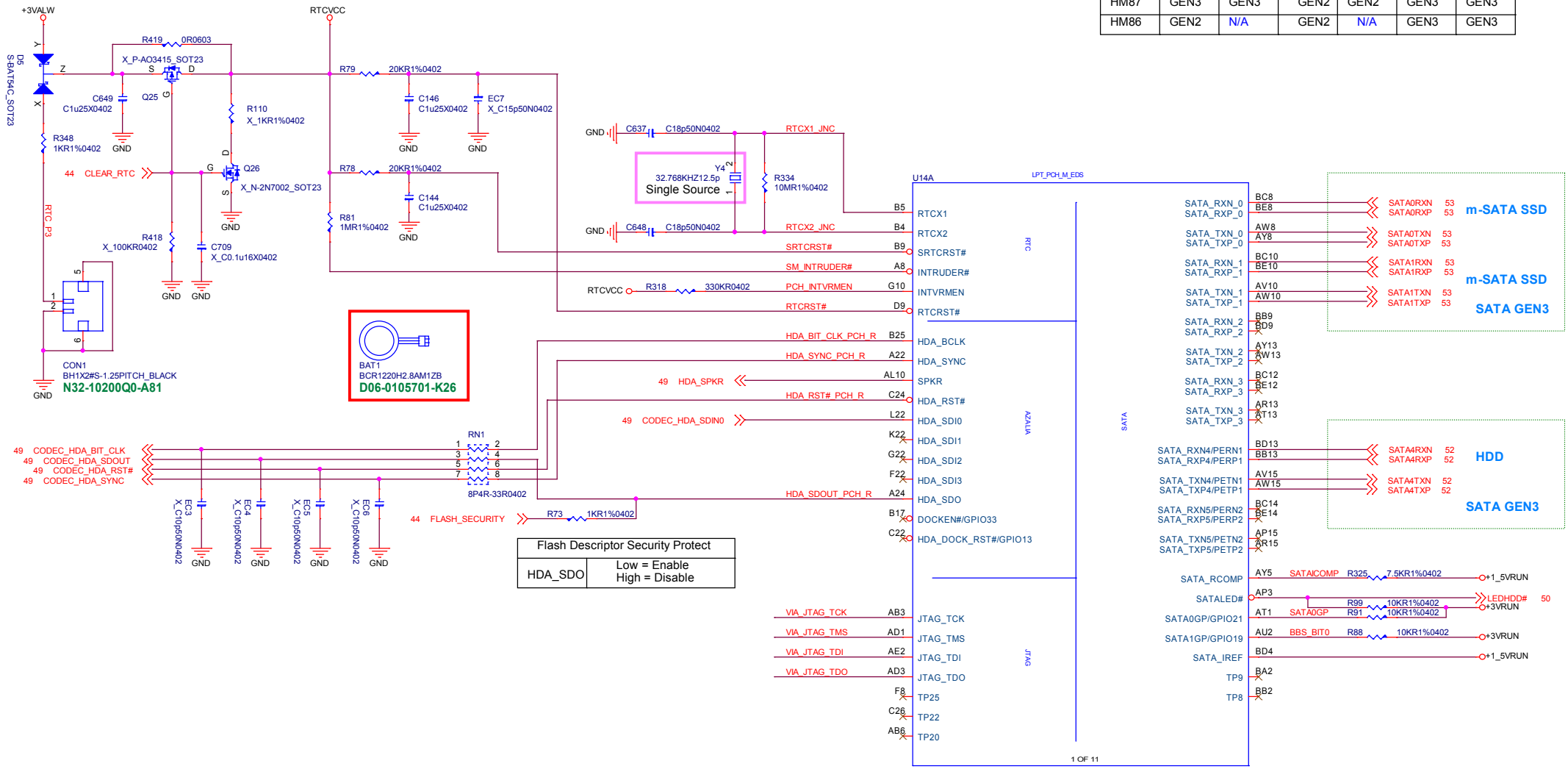


MICRO-STAR INT'L CO.,LTD.

Title	DGPU_Power Control	
Size	Document Number MS-16H5	Rev 1.2
Date: Thursday, August 21, 2014	Sheet 31 of 72	

Lynx Point (HDA/JTAG/SATA)

SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3



Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

SPK	The Signal has a weak internal pull-down Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)

MICRO-STAR INT'L CO.,LTD.

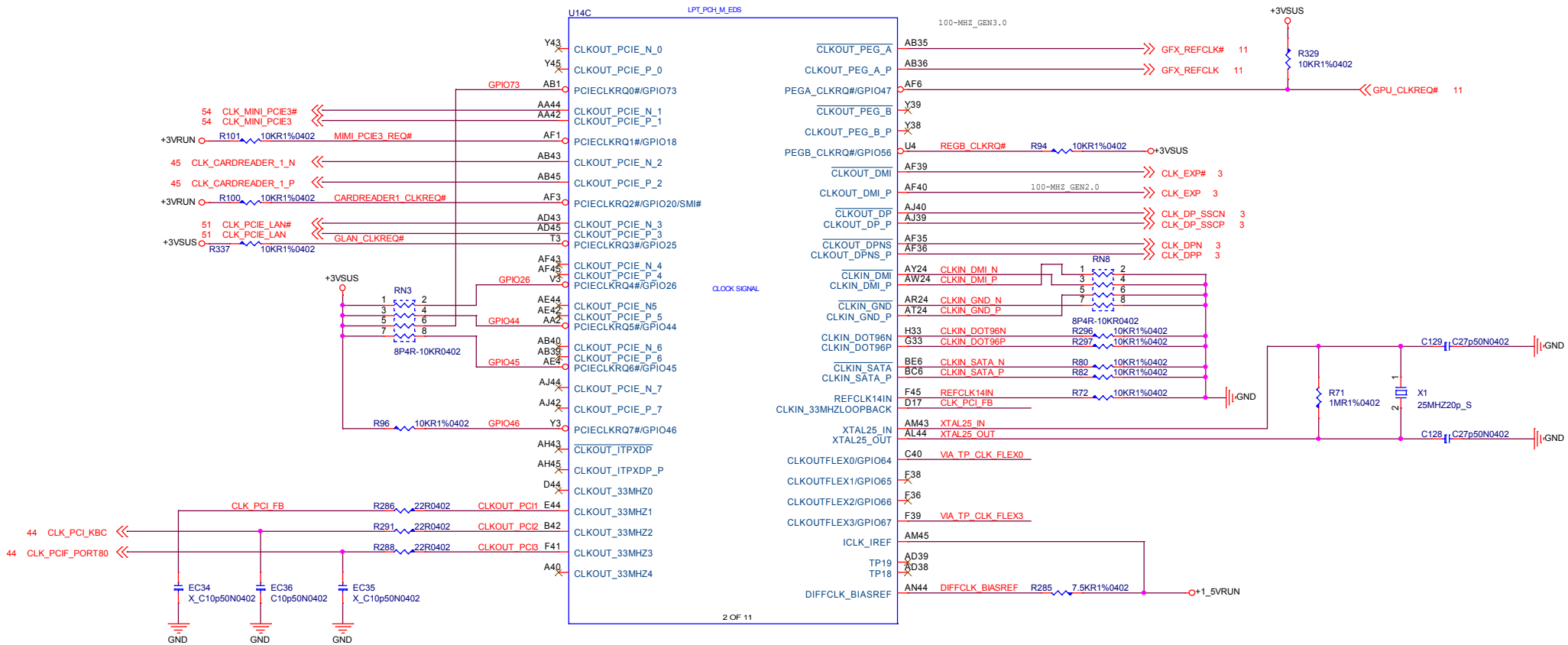
Title: PCH-1 (HDA/JTAG/SATA)

Size | Document Number: MS-16H5 | Rev: 1.2

Date: Thursday, August 21, 2014 | Sheet 32 of 72

Lynx Point (Clock)

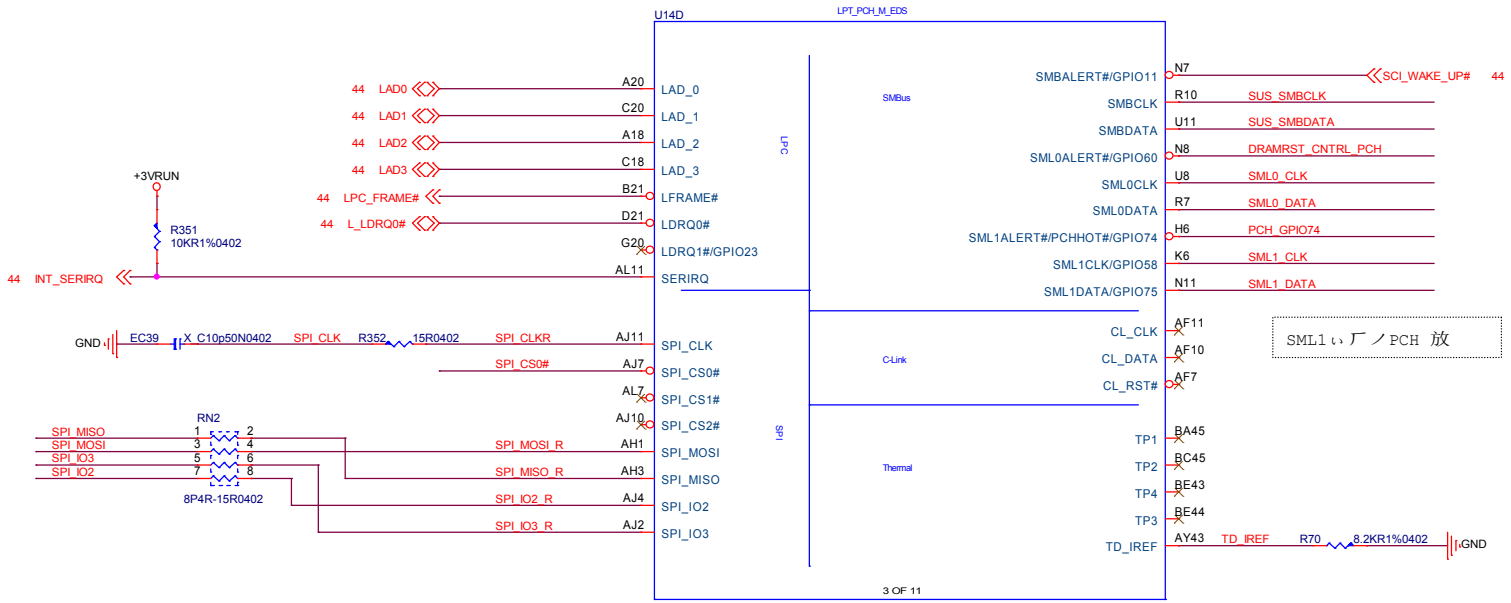
PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 k ±10% external pull-up resistor instead of No Connect.
Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.

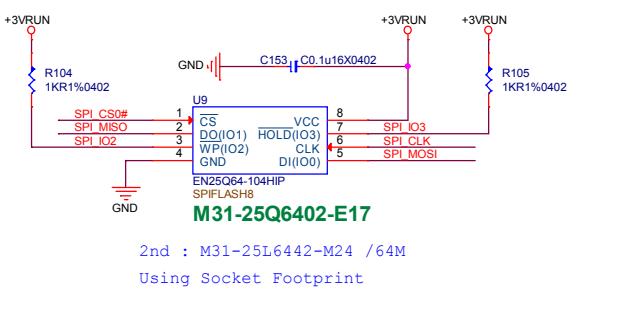


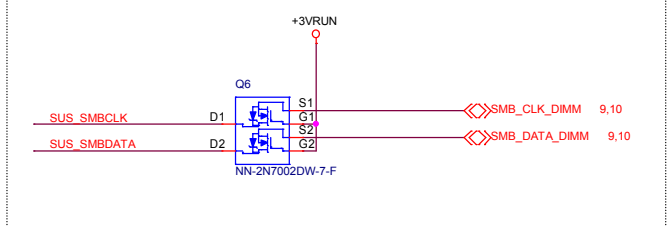
The CLKREQ# function can be disabled via intel management engine FW .Please refer to INTEL ME FW Bring up guide for configuring/disabling CLKREQ#

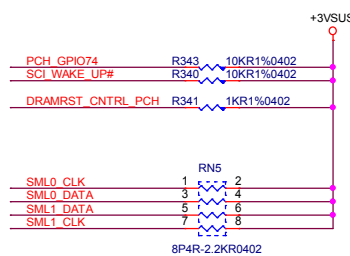
MICRO-STAR INT'L CO.,LTD.		
Title: PCH-2 (CLK)		
Size	Document Number: MS-16H5	Rev: 1.2
Date: Thursday, August 21, 2014	Sheet 33 of 72	

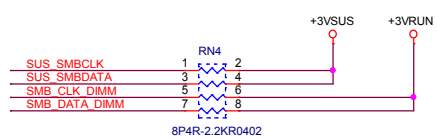
Lynx Point (LPC,SMBUS)







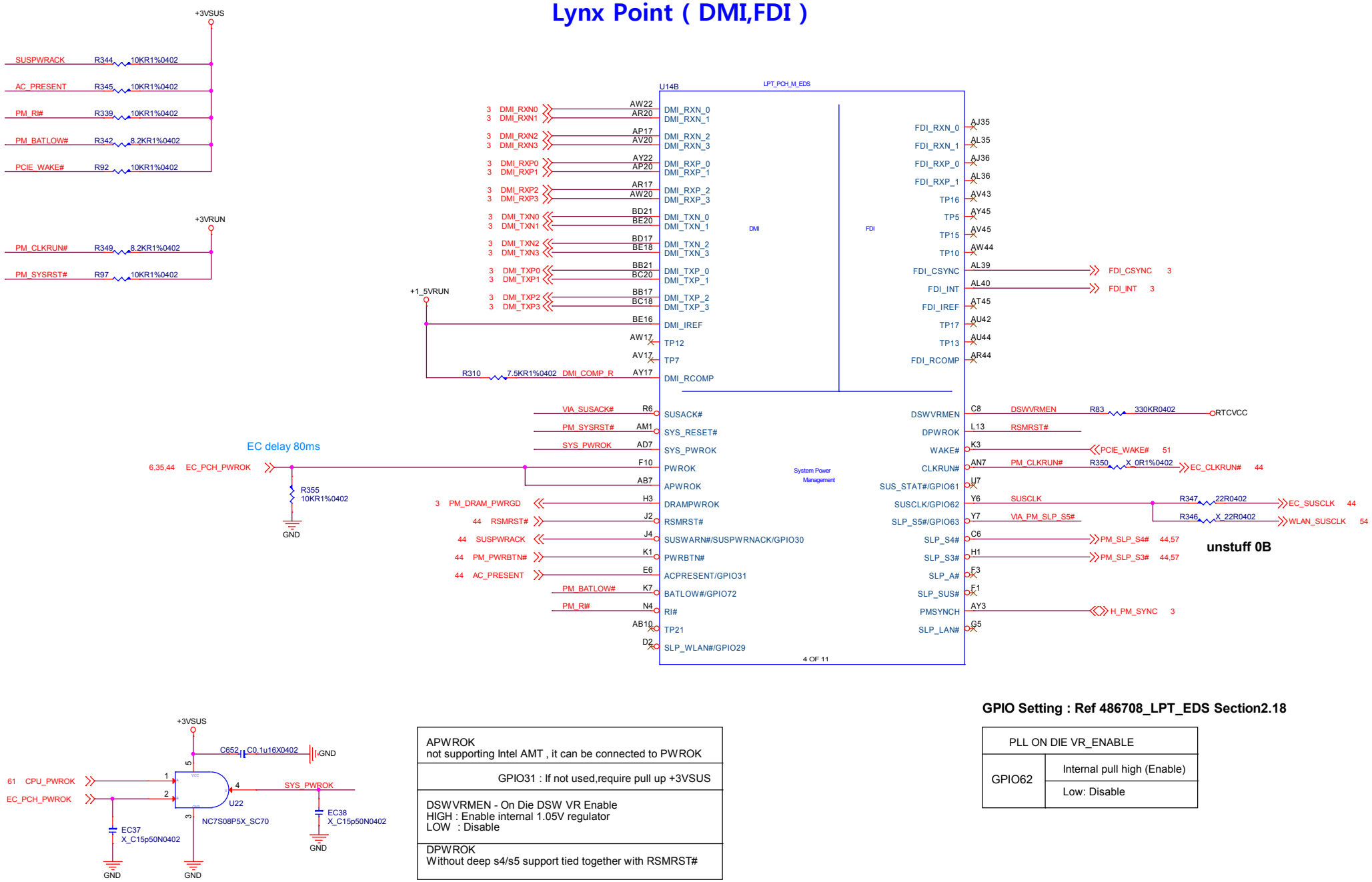




MICRO-STAR INT'L CO.,LTD.

Title	PCH-3 (LPC,SMBUS)	
Size	Document Number: MS-16H5	Rev: 1.2
Date: Thursday, August 21, 2014	Sheet 34 of 72	

Lynx Point (DMI,FDI)



APWROK not supporting Intel AMT , it can be connected to PWROK
GPIO31 : If not used,require pull up +3VSUS
DSWVRMEN - On Die DSW VR Enable HIGH : Enable internal 1.05V regulator LOW : Disable
DPWROK Without deep s4/s5 support tied together with RSMRST#

GPIO Setting : Ref 486708_LPT_EDS Section2.18

PLL ON DIE VR_ENABLE	
GPIO62	Internal pull high (Enable)
	Low: Disable

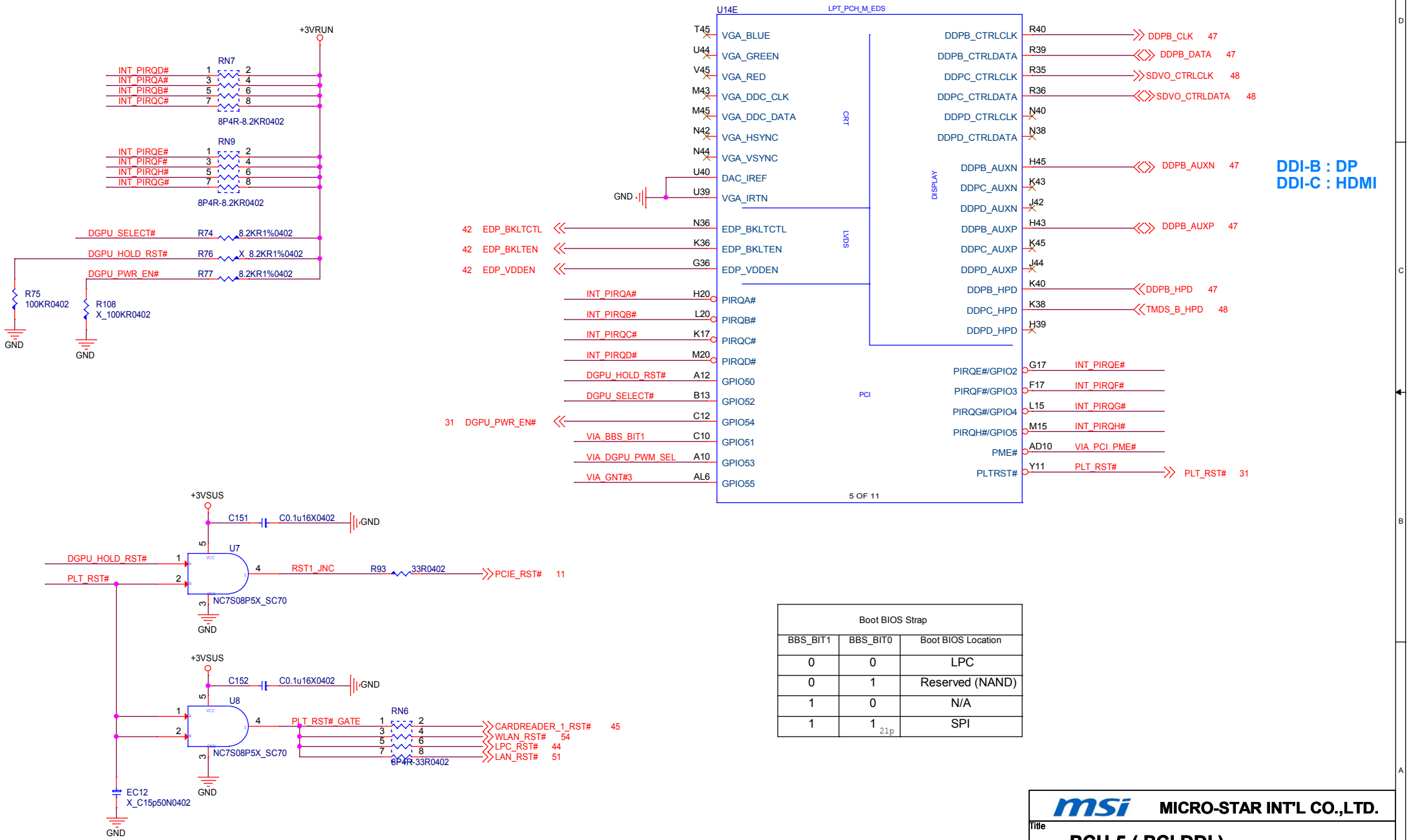
MICRO-STAR INT'L CO.,LTD.

Title: PCH-4 (DMI,FDI)

Size: | Document Number: MS-16H5 | Rev: 1.2

Date: Thursday, August 21, 2014 | Sheet 35 of 72

Lynx Point (PCI,DDI)



Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI

21p

MICRO-STAR INT'L CO.,LTD.

Title: PCH-5 (PCI,DDI)

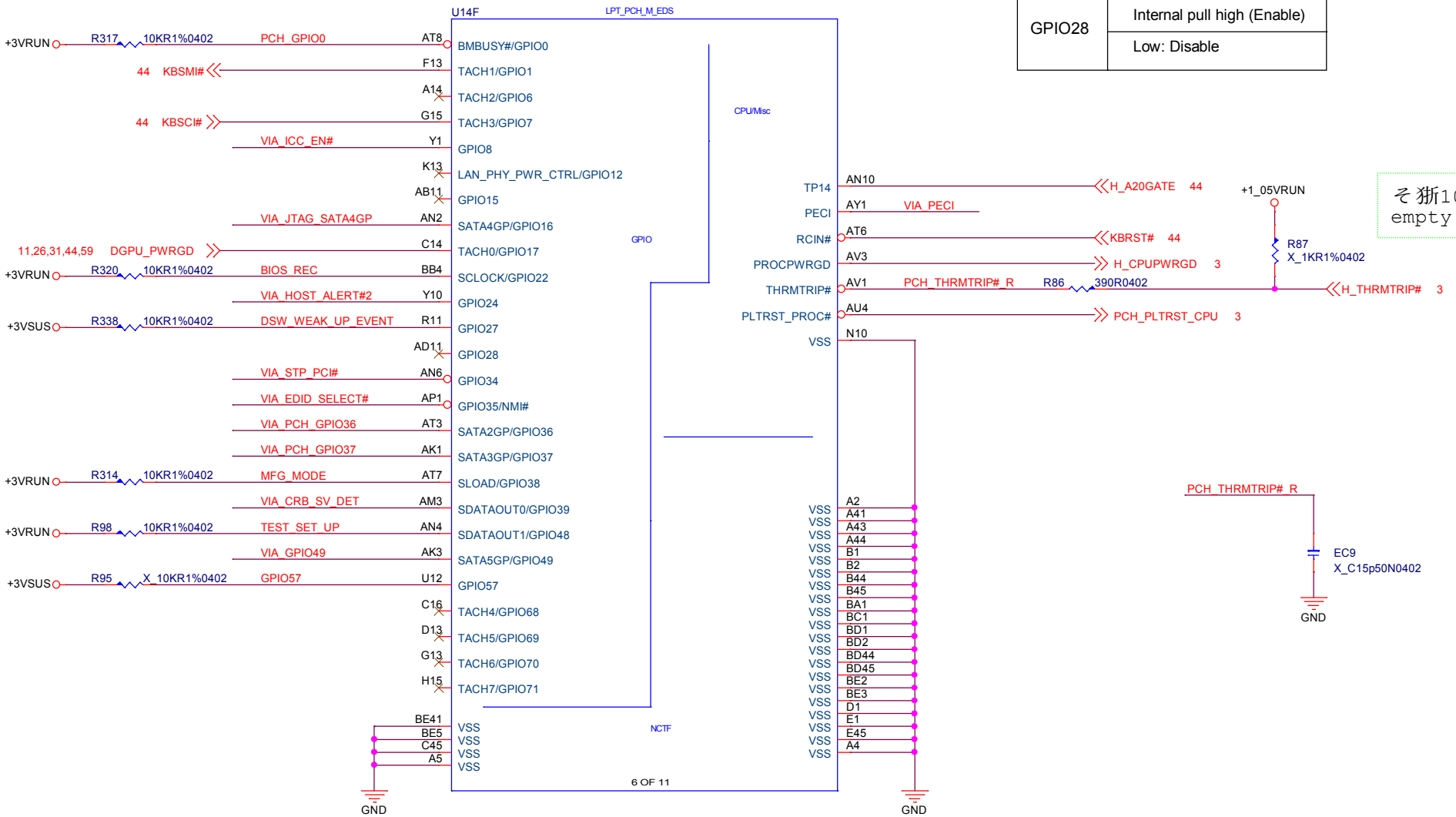
Size | Document Number: MS-16H5 | Rev: 1.2

Date: Thursday, August 21, 2014 | Sheet 36 of 72

Lynx Point (GPIO,MISC)

GPIO Setting : Ref 486708_LPT_EDS Section2.24

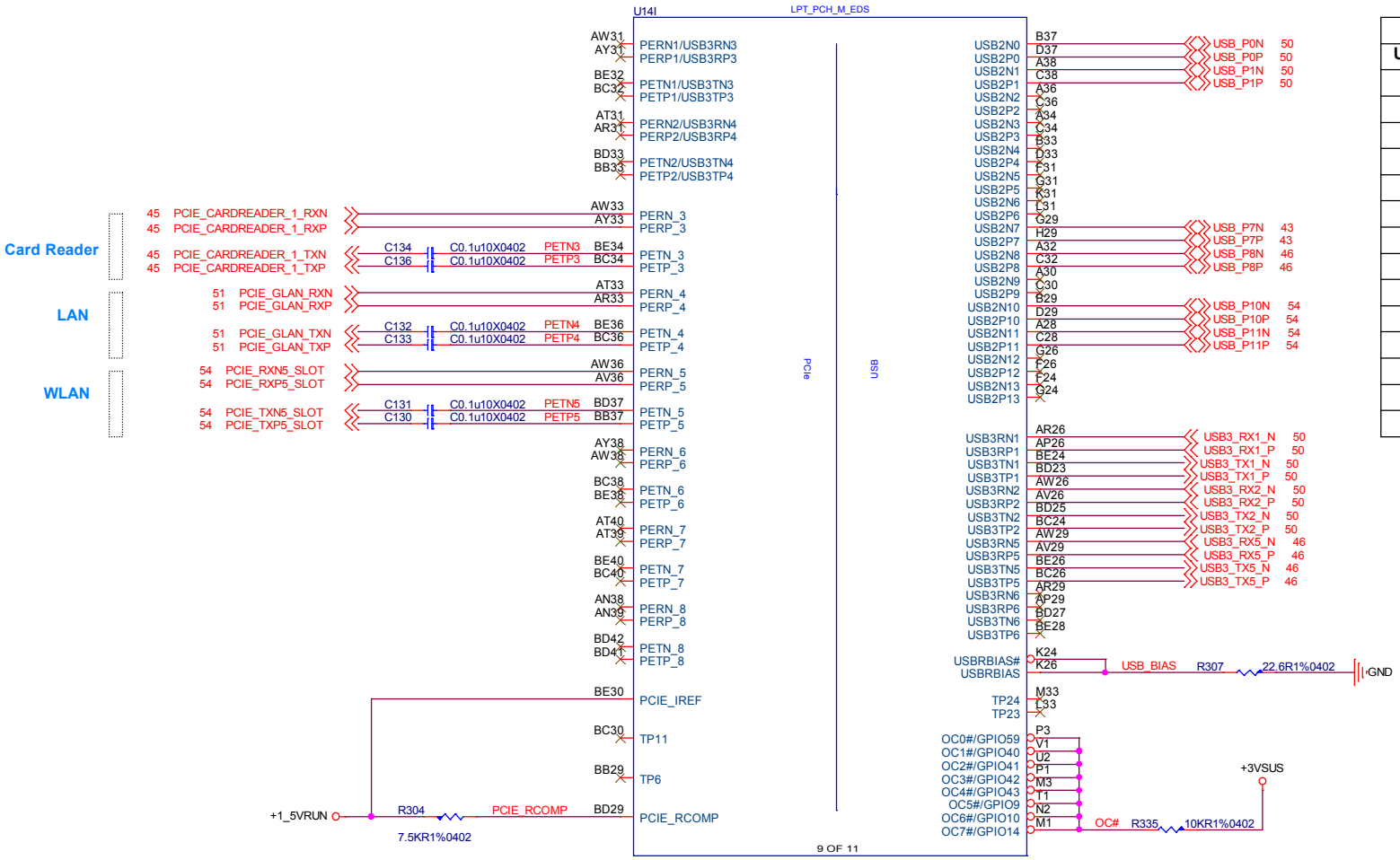
PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	PCH-6 (GPIO,MISC)	
Size	Document Number MS-16H5	Rev 1.2
Date: Thursday, August 21, 2014	Sheet 37 of 72	

Lynx Point (PCIE,USB)

Intel Lynx Point ECHI USB(2.0) debug transport 惠钡Port1 or Port9



USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	16H5A
1	2	USB 3.0 Port 2	16H5A
2			
3			NC
4			NC
5			NC
6			NC
7		EPF021	
8	3	USB 3.0 Port 5	16H51
9			NC
10		WLAN	
11		WebCam	
12			NC
13			NC

HM86 ⊿USB3.0 PORT 5,6

MICRO-STAR INT'L CO.,LTD.

Title: PCH-7 (PCIE,USB)

Size | Document Number: MS-16H5 | Rev: 1.2

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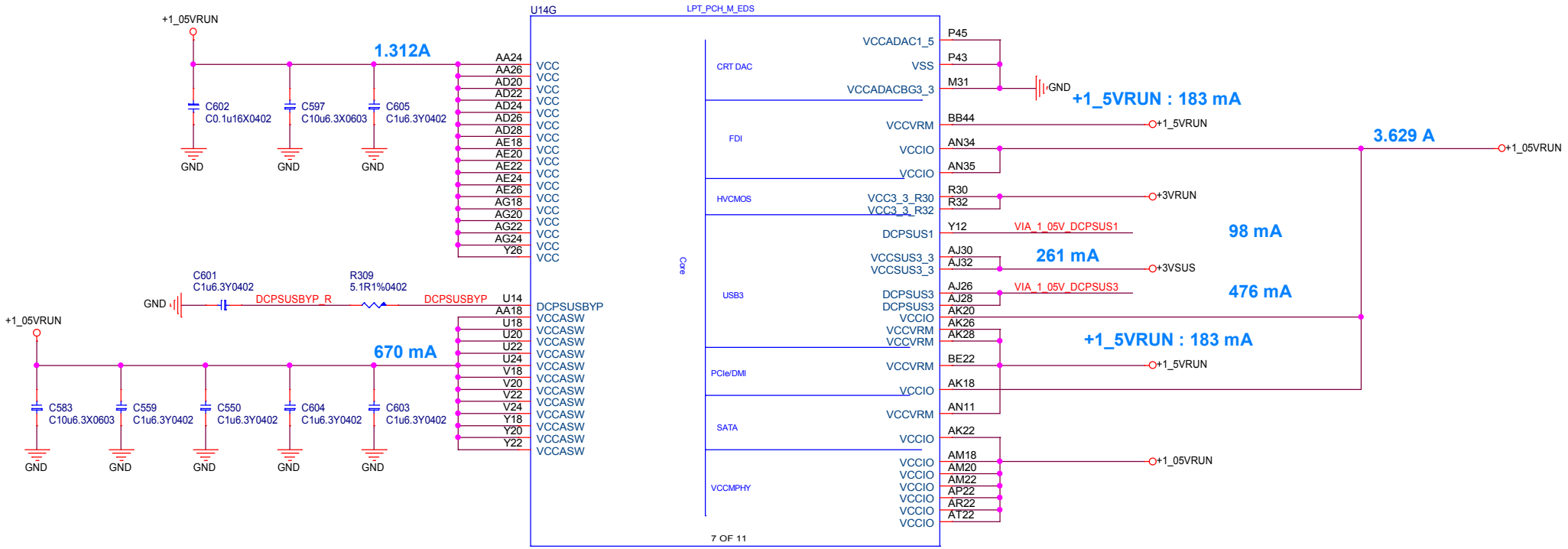
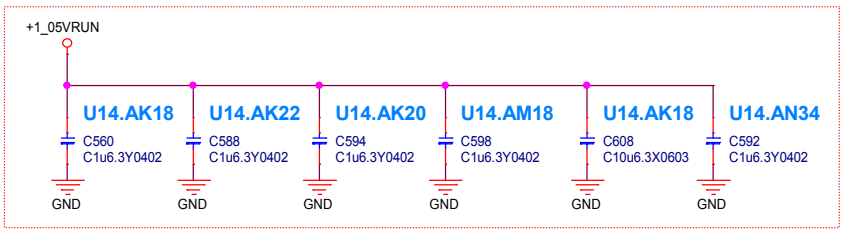
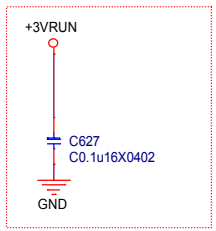
Lynx Point (Power)







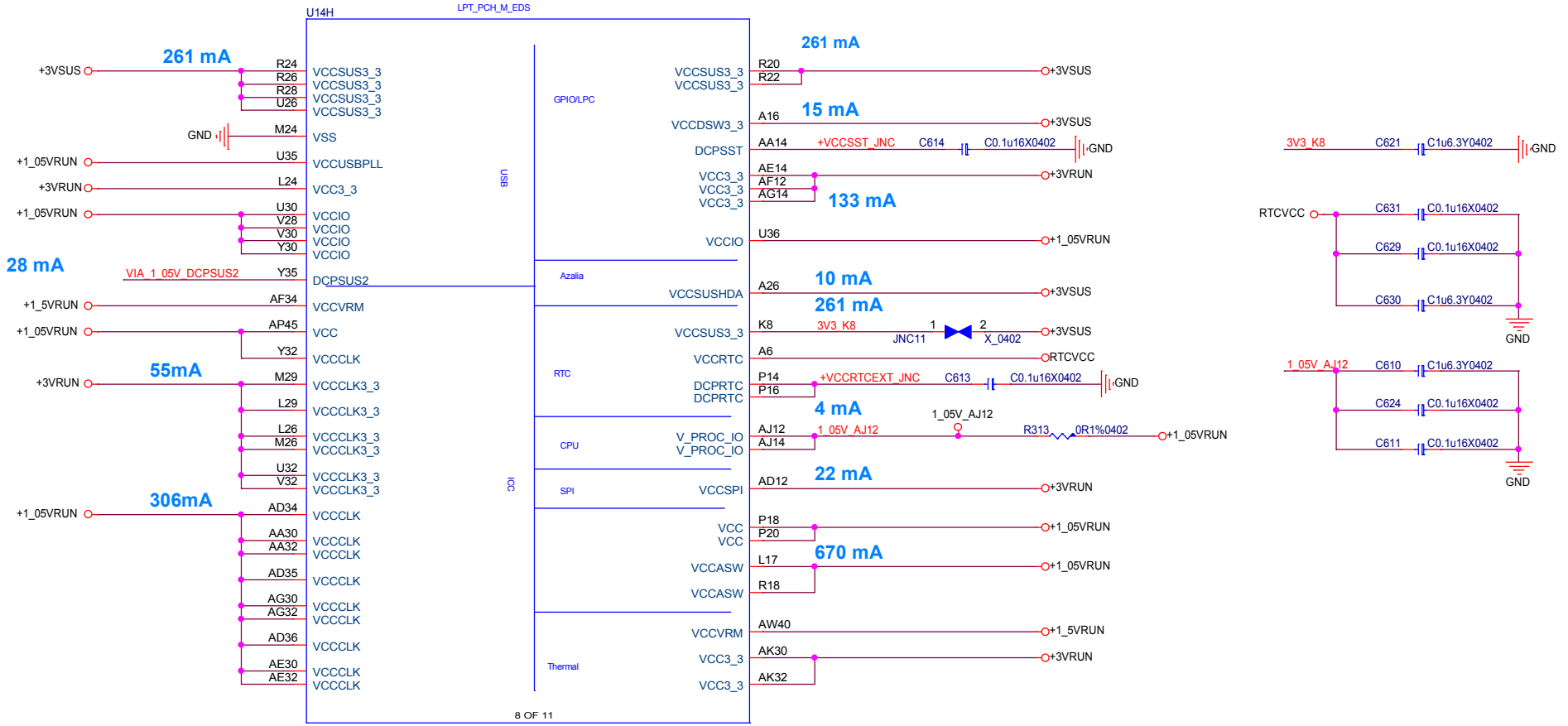
MICRO-STAR INT'L CO.,LTD.

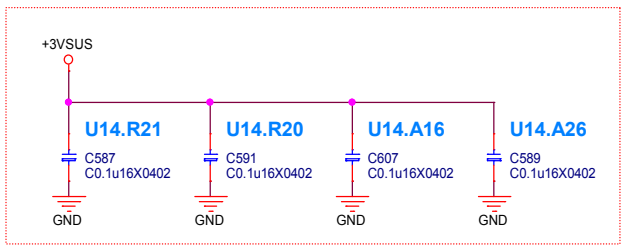
Title: PCH-8 (Power)

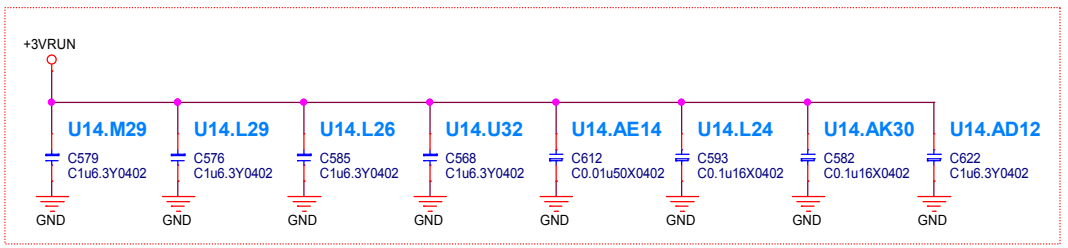
Size | Document Number: MS-16H5 | Rev: 1.2

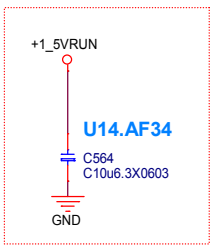
Date: Thursday, August 21, 2014 | Sheet 39 of 72

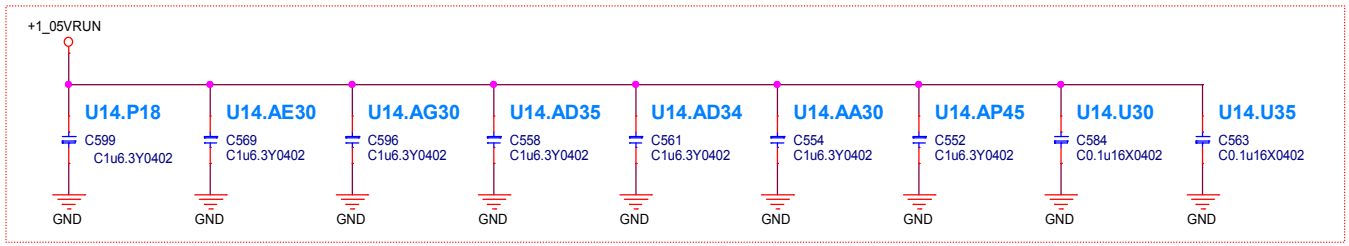
Lynx Point (Power)











MICRO-STAR INT'L CO.,LTD.

Title	PCH-8 (Power)	
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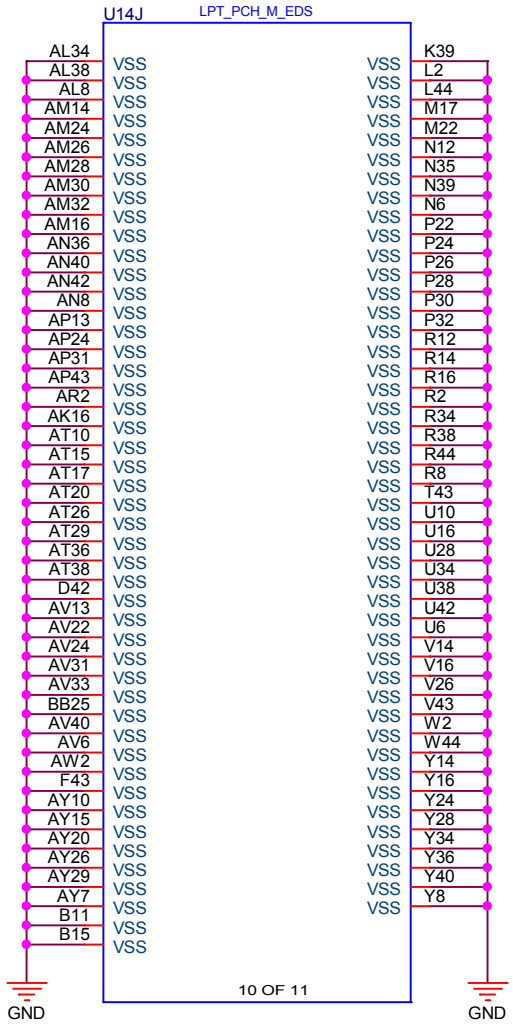
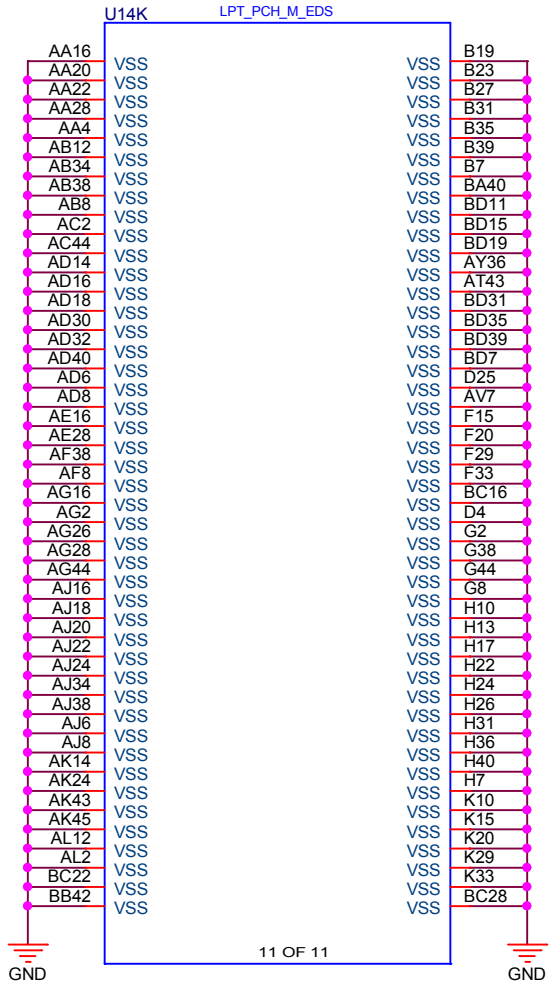
Lynx Point (GND)





MICRO-STAR INT'L CO.,LTD.		
Title: PCH-8 (GND)		
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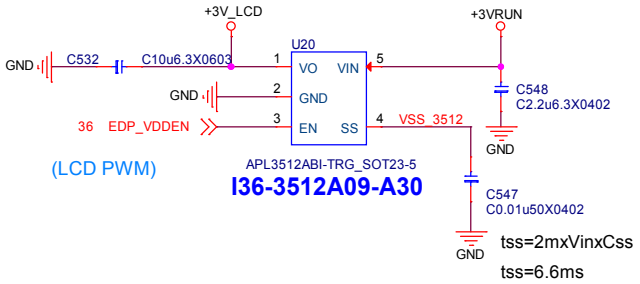
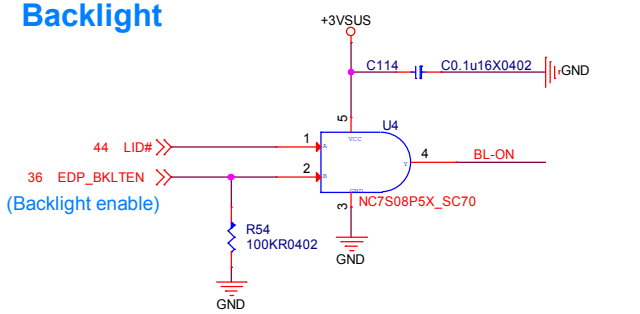
eDP Connector

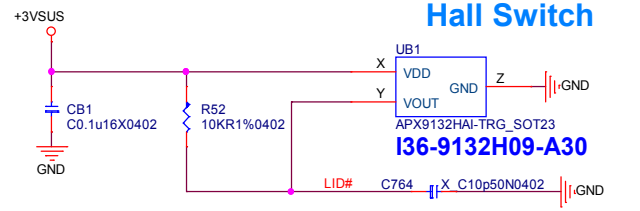
Pannel Device Logic Power



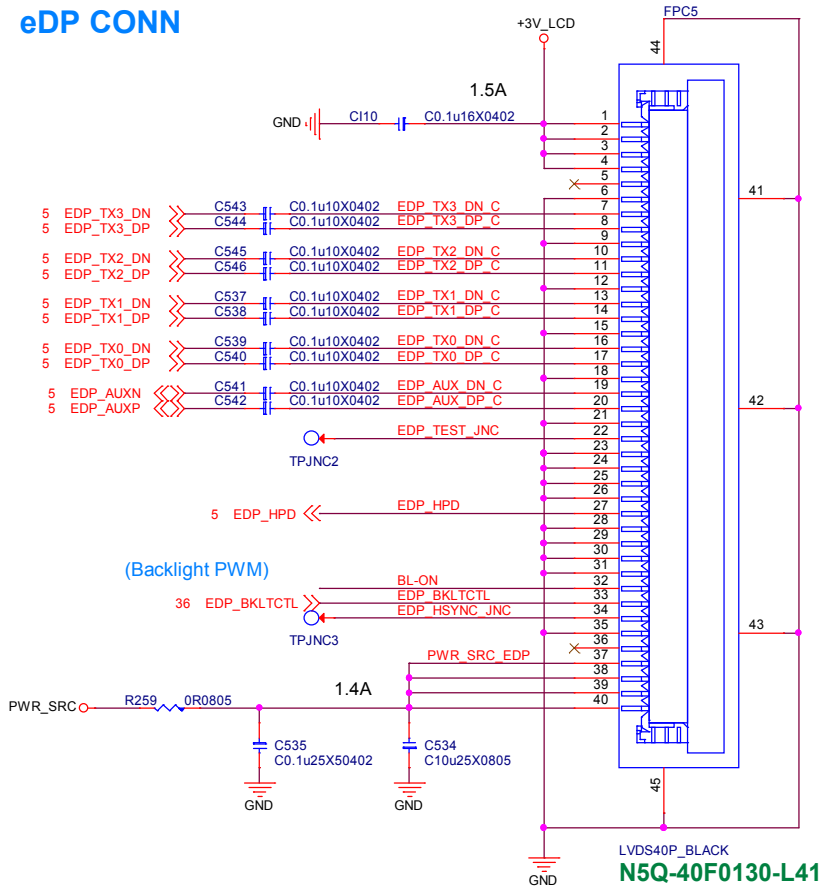
Backlight

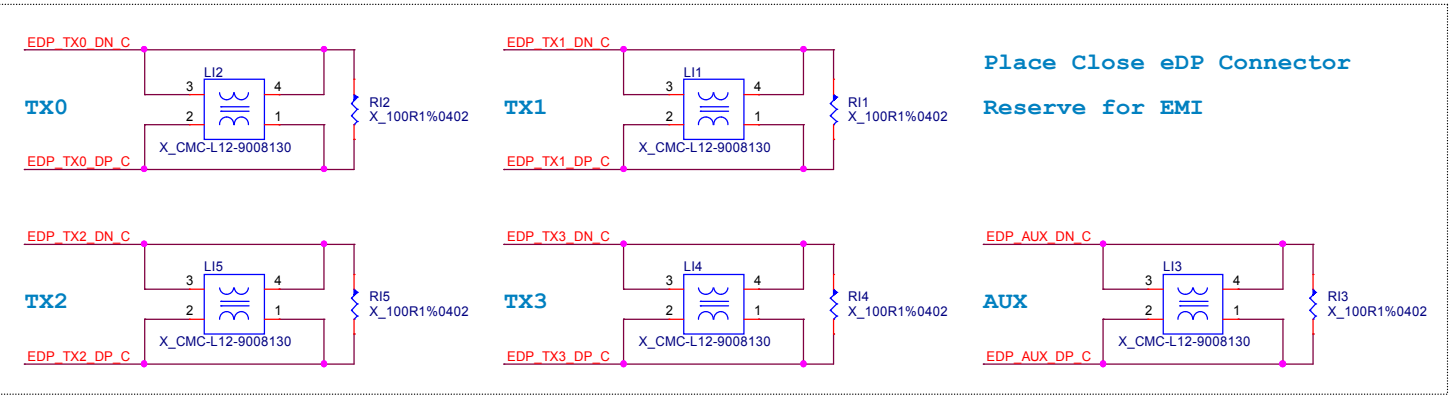


Hall Switch



eDP CONN





LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

MICRO-STAR INT'L CO.,LTD.

Title: eDP Connector

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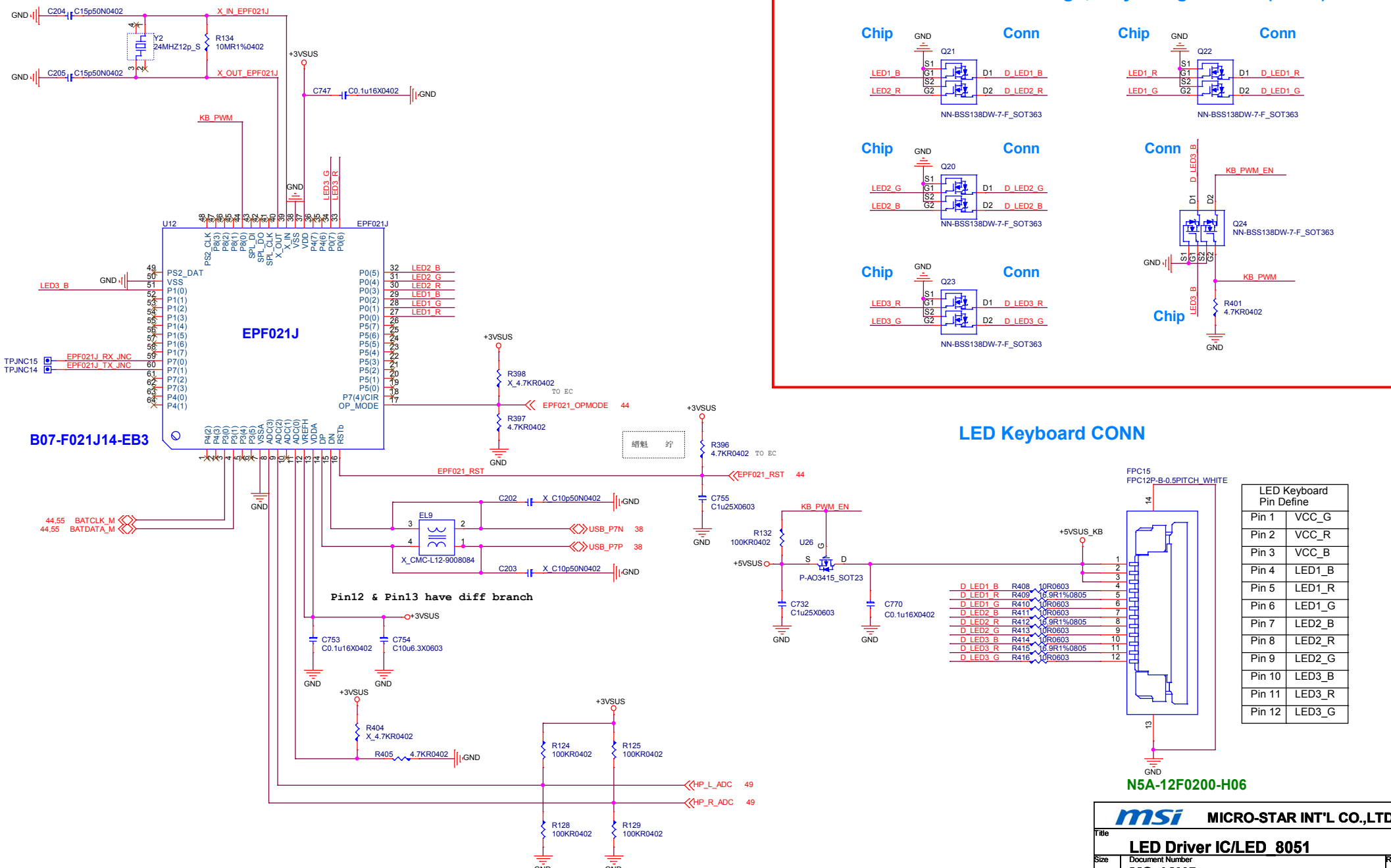
LED 8051 Controller



KBC(KB3930QFB1)

Hardware Reset

ED before RC

RC and R Close SW

SW-TACTB1-4PS5

N71-0100560-D02

SW Debug (LPC)

BH1X14#S-1PITCH

N32-1140130-H06

ROM

MX25L512EMI-10G

M31-2551222-M24

Keyboard conn

CON5 FPC26P-B-1PITCH_BLACK

N5A-26F0340-H06

PU/PD

MB_ID

ALLSYSPG

U1 — KB3930QFB1

LPC I/F

FAN&PWM

IKB

SPI FLASH

PS2 I/F

UART

ESB

CIR

SMBUS

AD/DA

SDI

LED

POWER/GROUND

Pin 105-108 8mA-16mA Sink

Pin 92 16mA-20mA Sink

Pin 39,91 16mA-20mA Sink

B02-0393024-E18

Title	KBC(KB3930QFB1)
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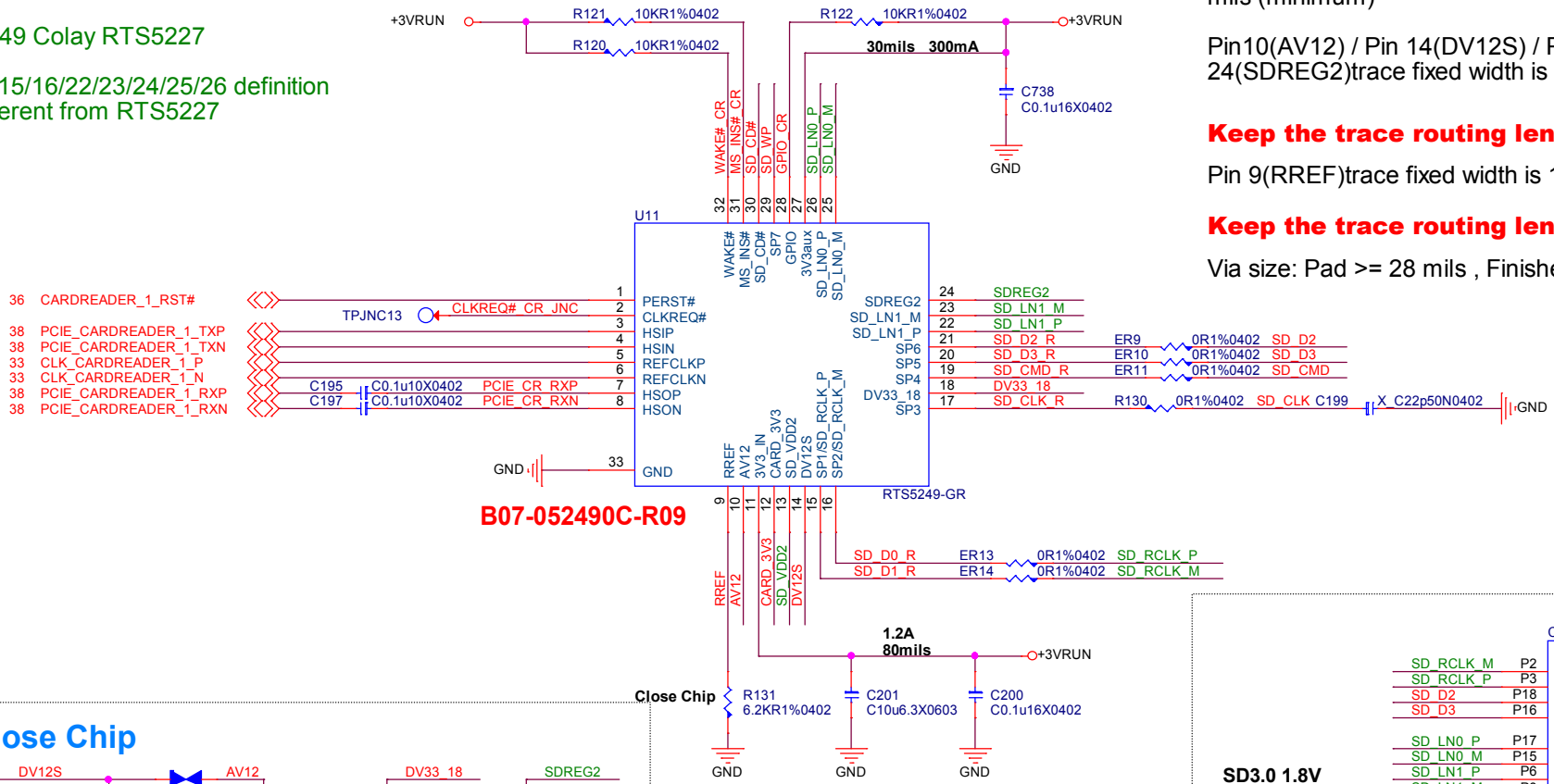
MICRO-STAR INT'L CO.,LTD.

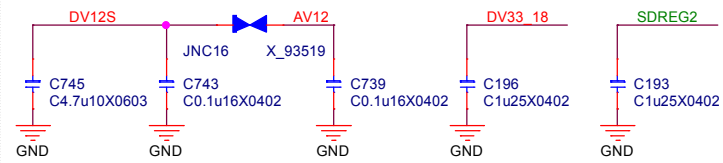
CardReader (RTS5249)

RTS5249 Colay RTS5227

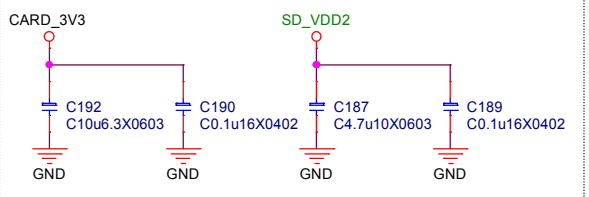
Pin 13/15/16/22/23/24/25/26 definition are different from RTS5227



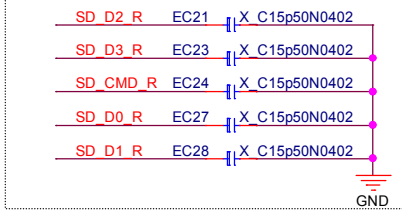
Close Chip



Close Connector



EMI



Power Trace

Pin11(3V3_IN) / Pin 12(CARD_3V3)trace fixed width is 40 mils (minimum)

Pin27(3V3aux) / Pin 13(SD_VDD2)trace fixed width is 30 mils (minimum)

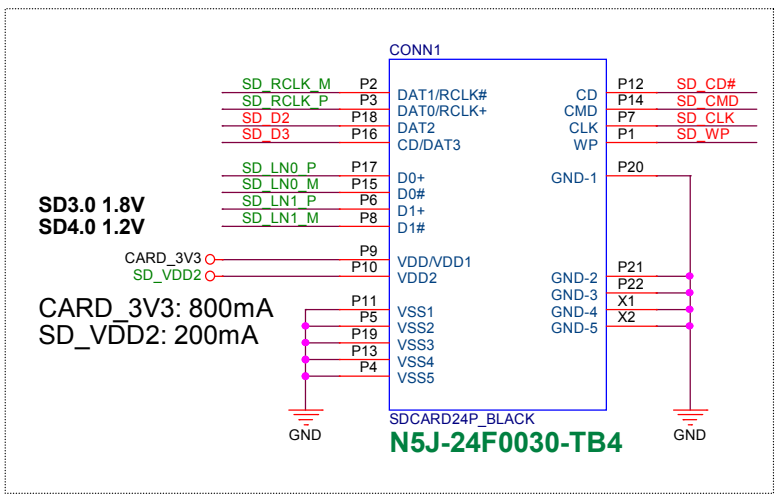
Pin10(AV12) / Pin 14(DV12S) / Pin 18(DV33_18) / Pin 24(SDREG2)trace fixed width is 20 mils (minimum)

Keep the trace routing lengths is limit to 200 mils

Pin 9(RREF)trace fixed width is 12 mils (minimum)

Keep the trace routing lengths is limit to 200 mils

Via size: Pad >= 28 mils , Finished hole >= 16 mils.



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	Card Reader		
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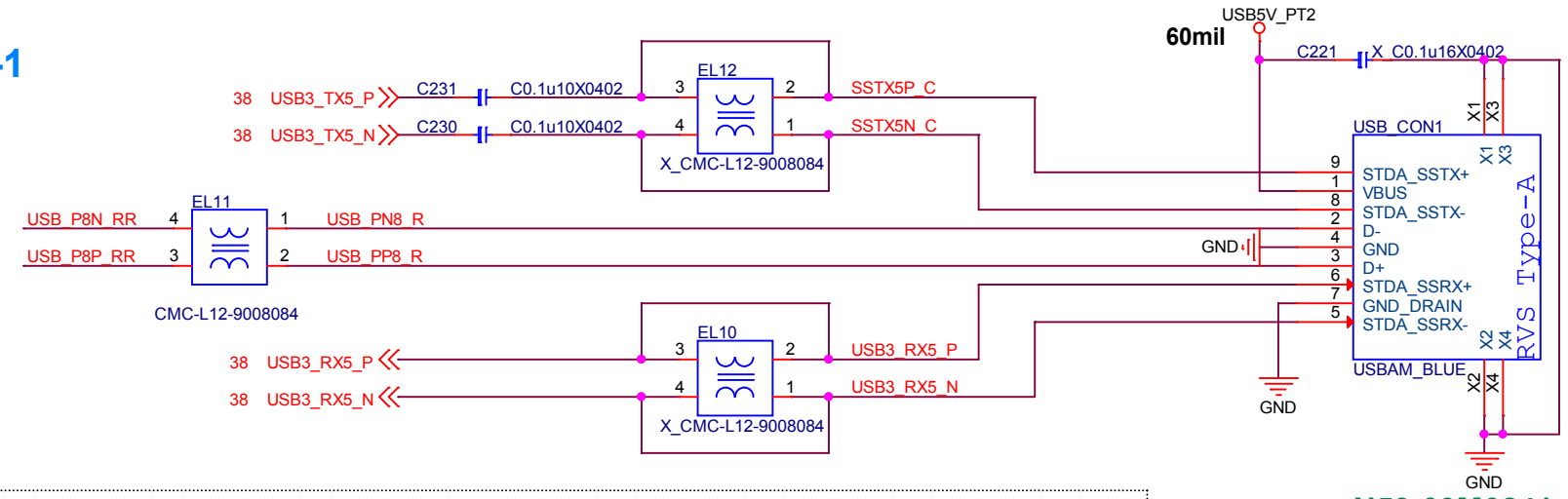
Date:	Thursday, August 21, 2014	Sheet 45 of 72	

USB 3.0 / iCharger

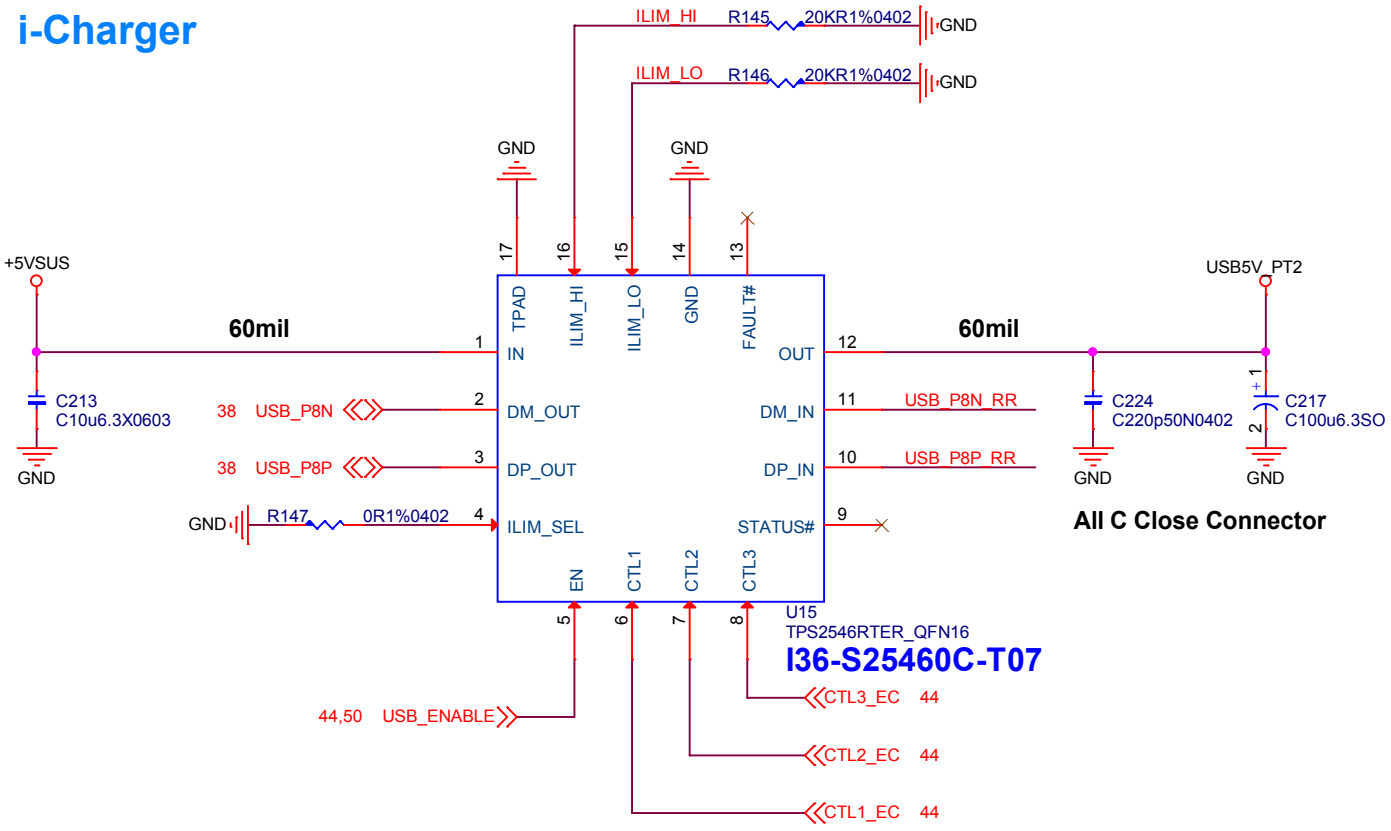
USB3.0 CNT-1

USB3.0 Port-6
USB2.0 Port-8

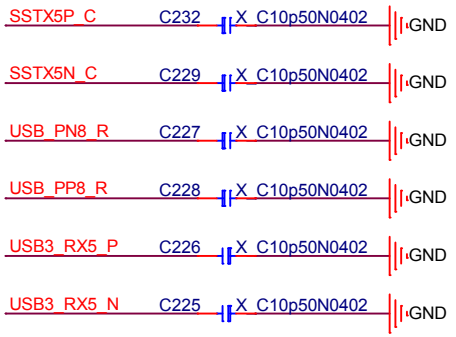


N53-09M0241-AF2

i-Charger

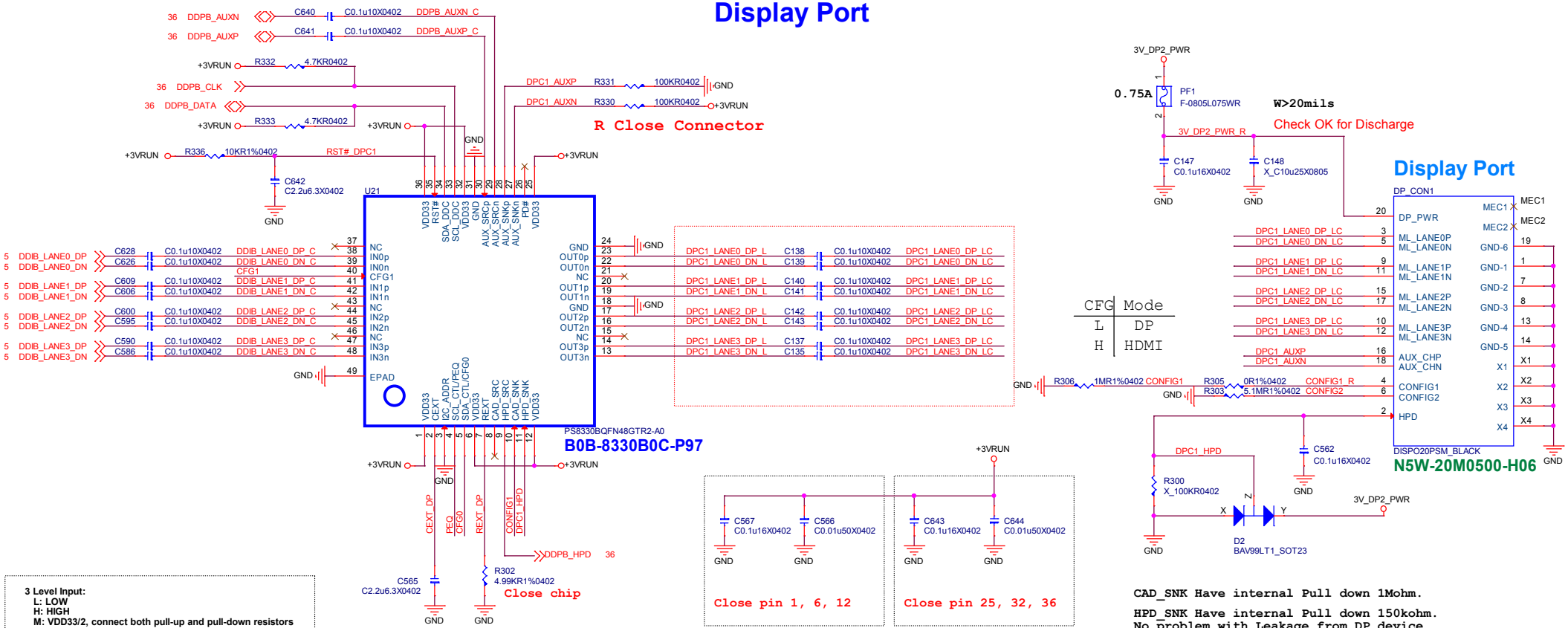


EMI



MICRO-STAR INT'L CO.,LTD.		
Title: USB 3.0 / iCharger		
Size	Document Number: MS-16H5	Rev: 1.2
Date: Thursday, August 21, 2014	Sheet 46 of 72	

Display Port

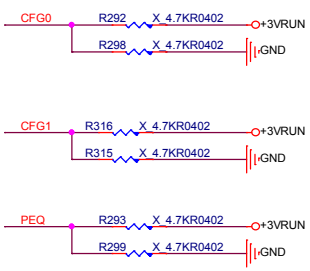


3 Level Input:
L: LOW
H: HIGH
M: VDD33/2, connect both pull-up and pull-down resistors

CAD_SNK Have internal Pull down 1Mohm.

HPD_SNK Have internal Pull down 150kohm. No problem with Leakage from DP device

The DP_PWR and RETURN pins of the box-to-box connectors must support the maximum current rating of 500mA.

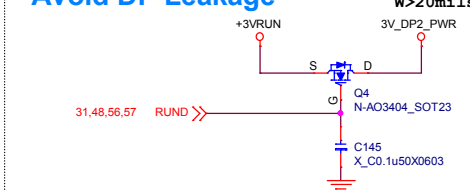



```
Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.
   L: default, automatic EQ enable & AUX interception enable
   H: automatic EQ disable & AUX interception enable
   M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing
```

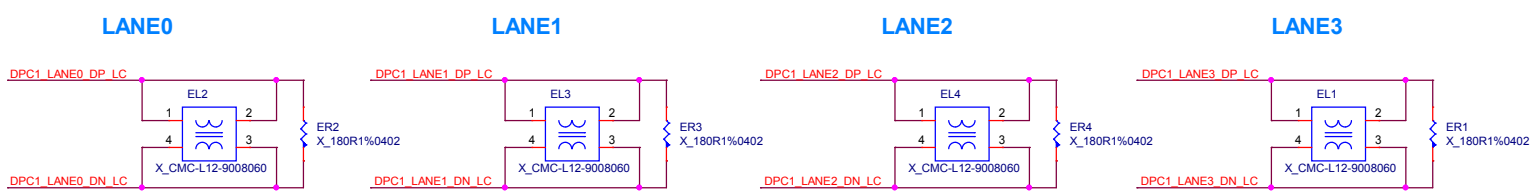
```
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K Ohm
   H: default, auto test disable & input offset cancellation enable
   L: auto test enable & input offset cancellation enable
   M: auto test disable & input offset cancellation disable
```

```
Programmable input equalization levels; Internal pull down at ~150k Ohm, 3.3V I/O.
   L: default, LEQ, compensate channel loss up to 12dB @ HBR2
   H: HEQ, compensate channel loss up to 15dB @ HBR2
   M: LLEQ, compensate channel loss up to 5dB @ HBR2
```

Avoid DP Leakage



EMI Close Connector



MICRO-STAR INT'L CO.,LTD.

Title	DP witch Repeater	
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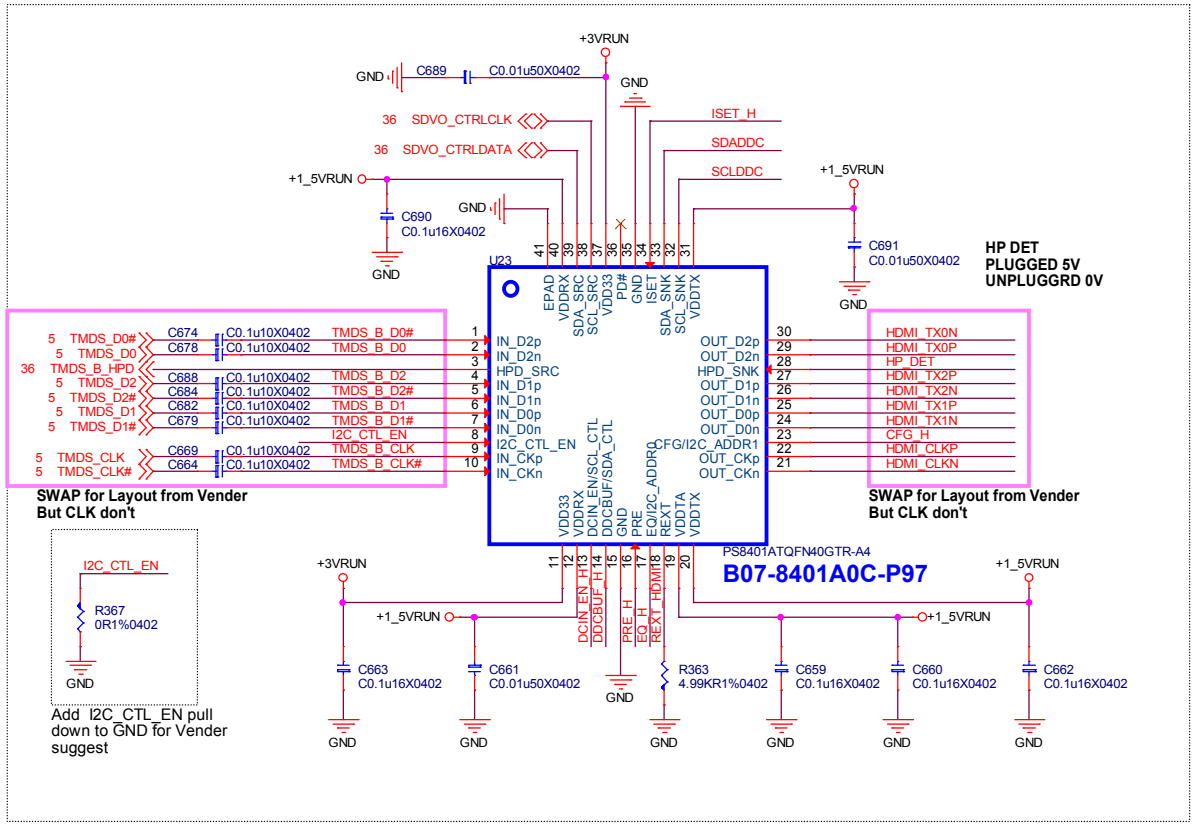
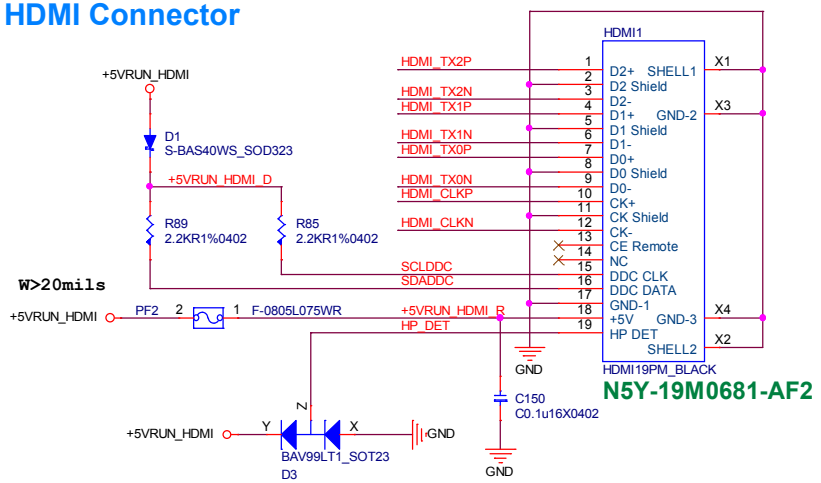
HDMI Repeater



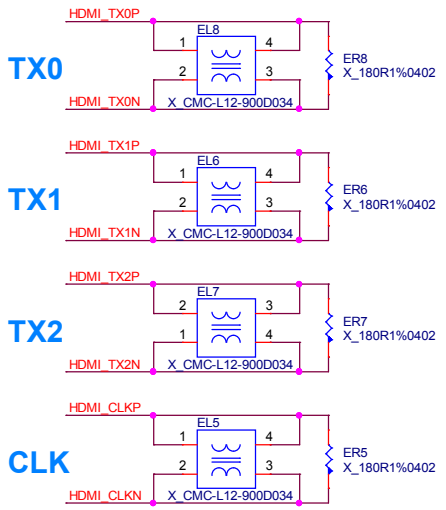
HDMI Connector

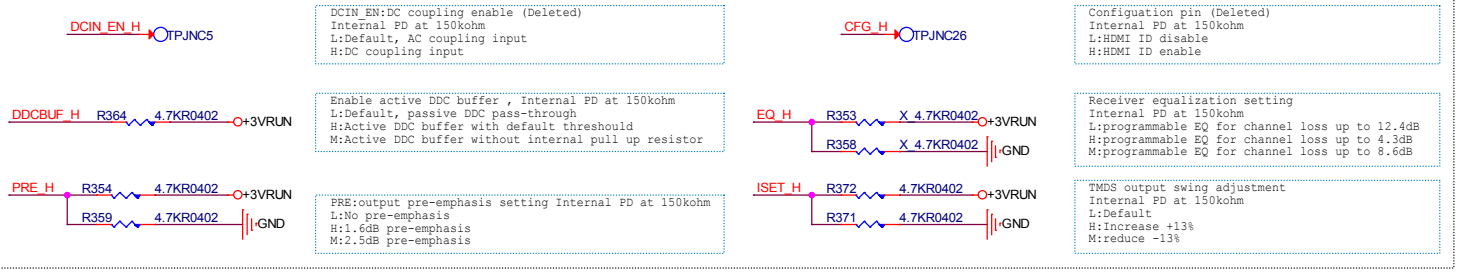


An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

HPD_SNK Internal PD 150kohm

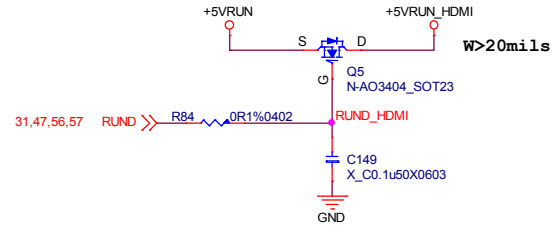
EMI Close Connector





ADDR1 (CFG)	ADDR0 (EQ)	I2C control bus address (Internal pull down at ~150k , 3.3V I/O)
0	0	0x4C / 4D (default)
0	1	0x5C / 5D
1	0	0xCC / CD
1	1	0xEC / ED

Avoid HDMI Leakage



MICRO-STAR INT'L CO.,LTD.

Title	HDMI Repeater	
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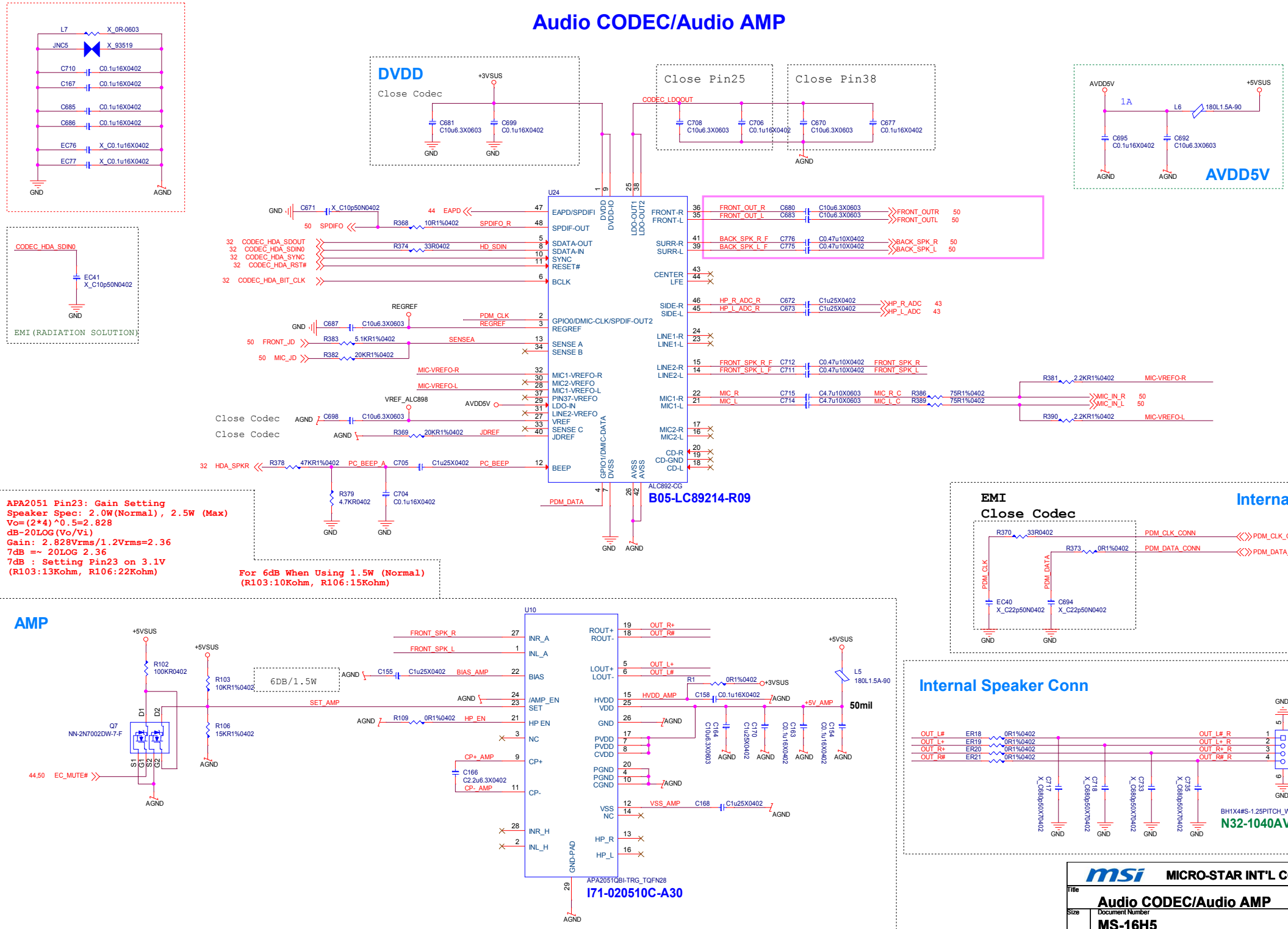
Audio CODEC/Audio AMP



msi	MICRO-STAR INT'L CO.,LTD.		
Title	Audio CODEC/Audio AMP		
Size	Document Number		Rev
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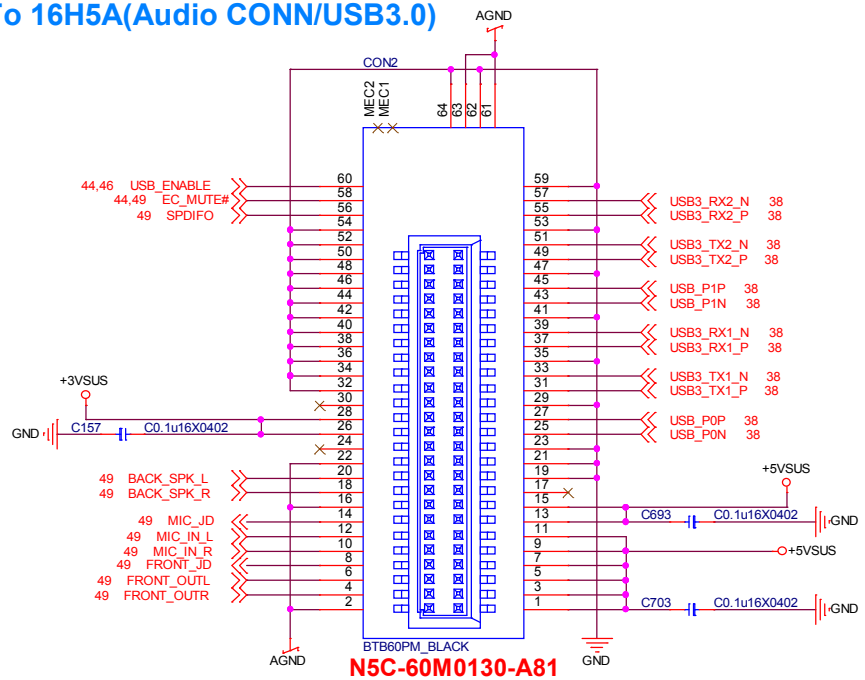
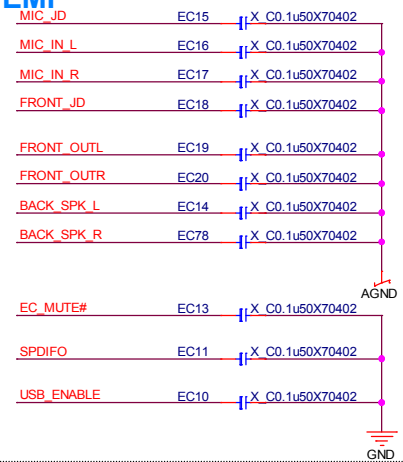
CPU FAN/BTB CONN

To 16H5A(Audio CONN/USB3.0)

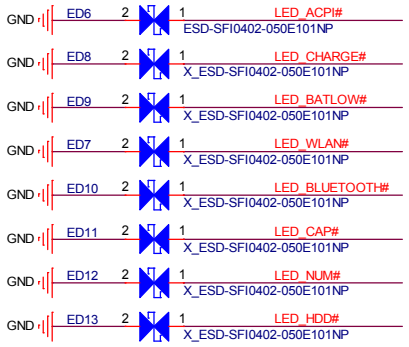


N5C-60M0130-A81

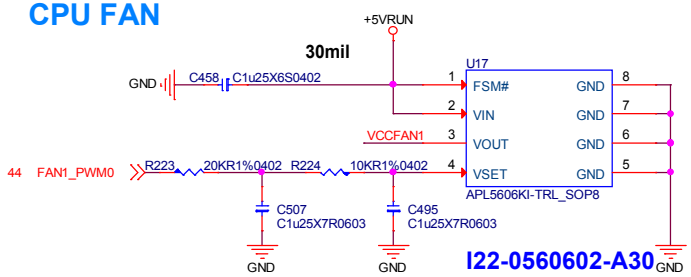
EMI



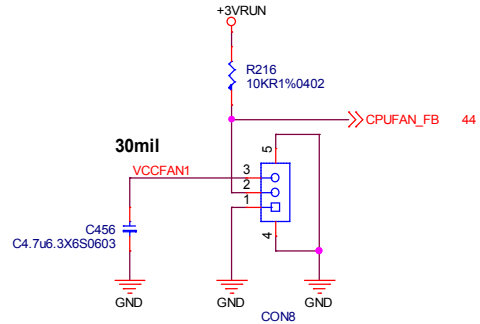
EMI



CPU FAN

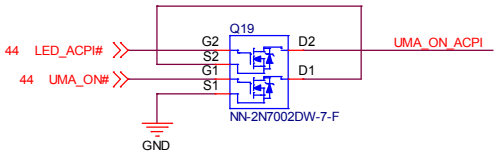


I22-0560602-A30

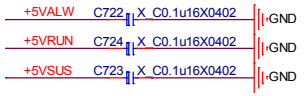


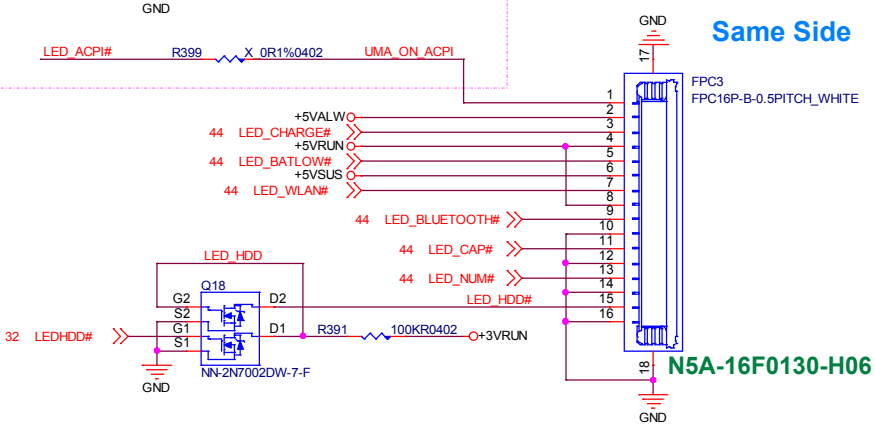
N32-1030AP0-H06

S3 Breath
S0 No active



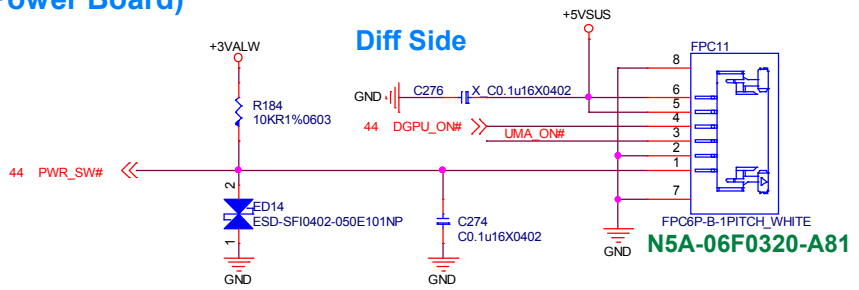
To 16H5B(LED Board)





N5A-16F0130-H06

To 16H5C (Power Board)



N5A-06F0320-A81

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Title	CPU FAN/BTB CONN	
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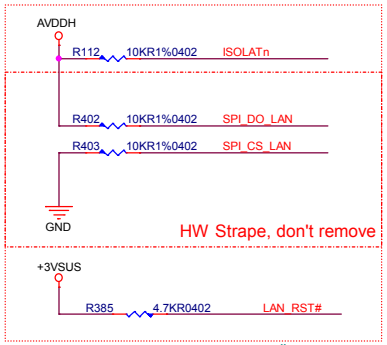
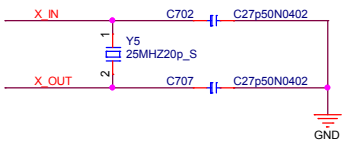
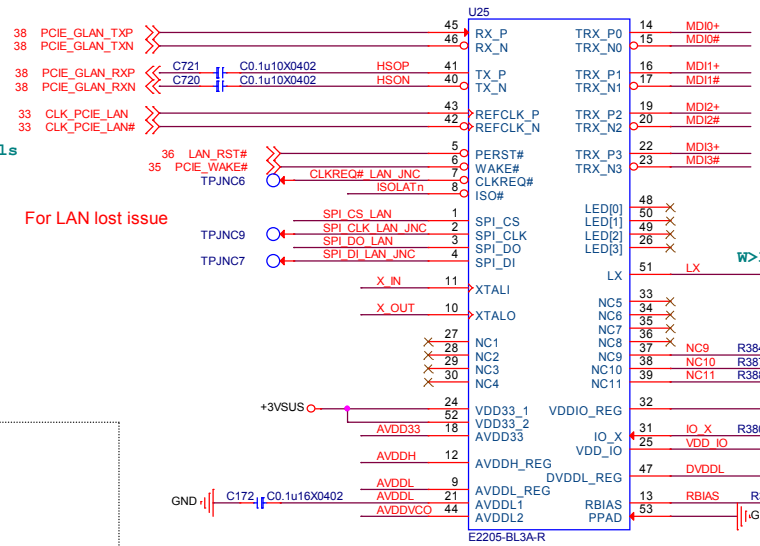
GIGA LAN(BigFoot BFN2205B)



RST# spacing 20mils

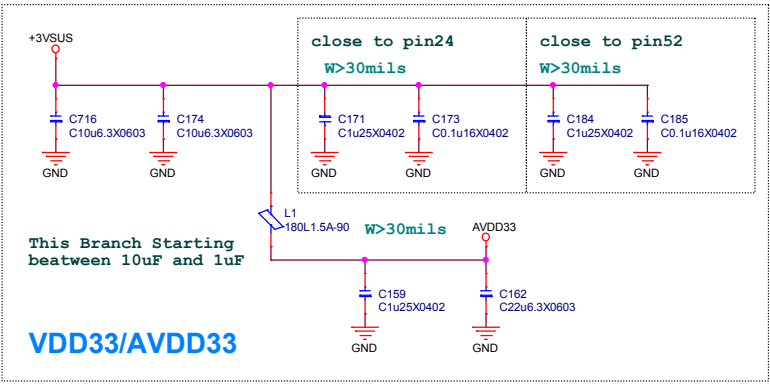


For LAN lost issue

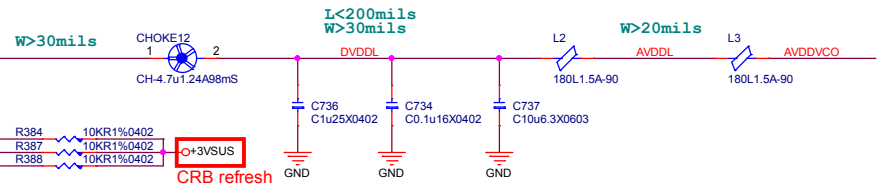


B06-E22050C-Q24

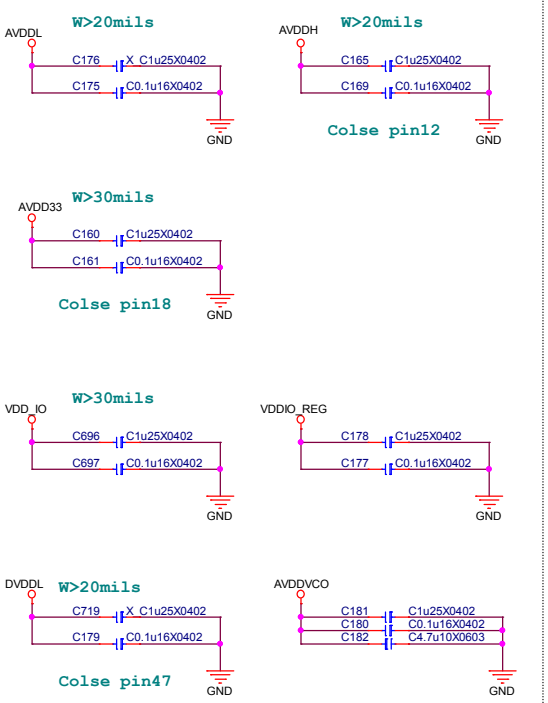
MAC 繙 CHIP
ず,TΩ计

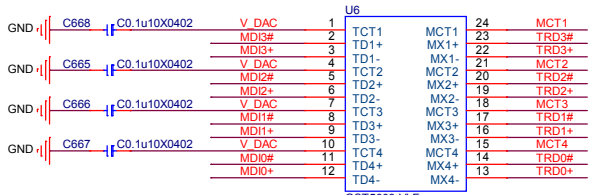


VDD33/AVDD33

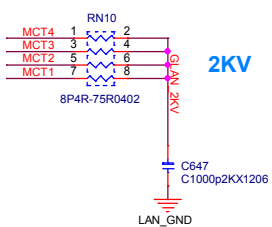


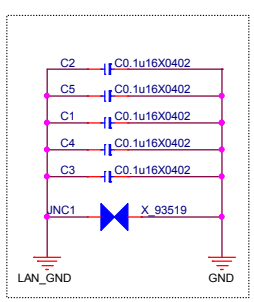
Power CAP

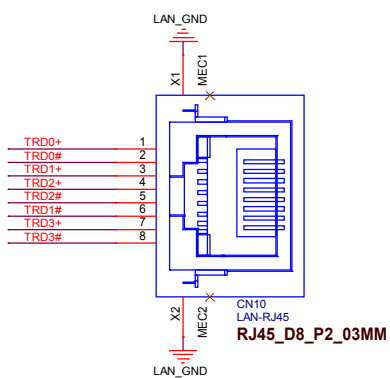




L05-0200150-B09



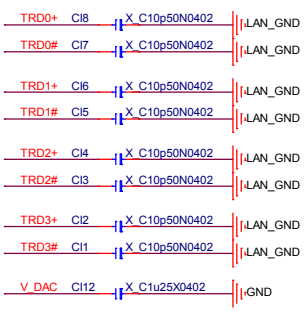




RJ45_D8_P2_03MM

N55-08F0691-AF2

EMI



MICRO-STAR INT'L CO.,LTD.		
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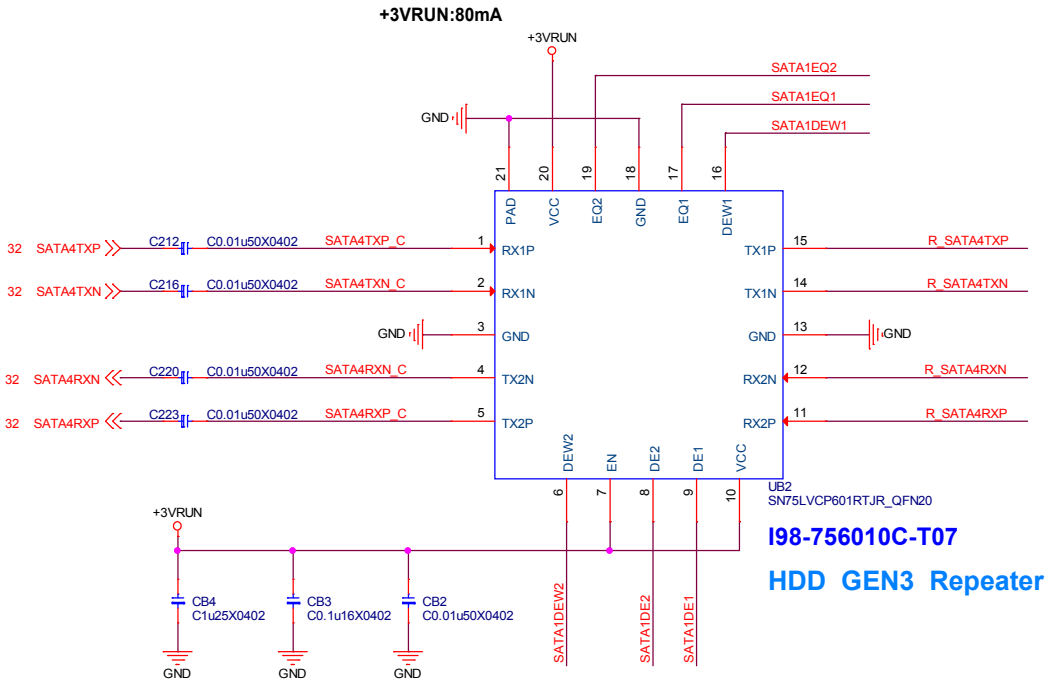
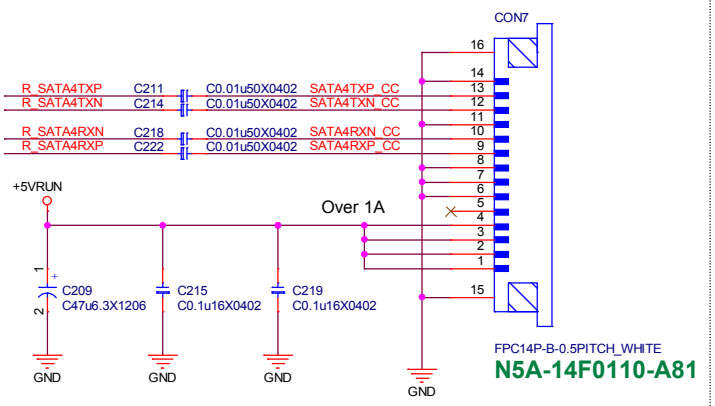
HDD (With Repeater)



I98-756010C-T07

HDD GEN3 Repeater

BTB Connecter



N5A-14F0110-A81

SATA1EQ1 R142 X_10KR1%0402 +3VRUN SATA1DE1 TPJNC19 SATA1DEW1 R140 0R1%0402 GND

SATA1EQ2 R141 X_10KR1%0402 +3VRUN SATA1DE2 TPJNC18 SATA1DEW2 R148 0R1%0402 GND

TI SN75LVCP601RTJR HW Setting

DE1/DE2	CH1/CH2De-Emphasis dB(at 6Gbps)	DQ1/DQ2	CH1/CH2De-Emphasis dB(at 6Gbps)
NC(default)	-4	NC(default)	0
0	0	0	7
1	-2	1	14

DEW1/DEW2	Device Function --> De Width for CH1/CH2
0	De-emphasis Pulse duration, short(recommended setting when linkoperates at SATA 1.5/3/6 Gbps)
1(default)	De-emphasis Pulse duration, long(recommended setting when linkoperates at SATA 1.5/3/6 Gbps)

MICRO-STAR INT'L CO.,LTD.

Title: HDD With Repeater

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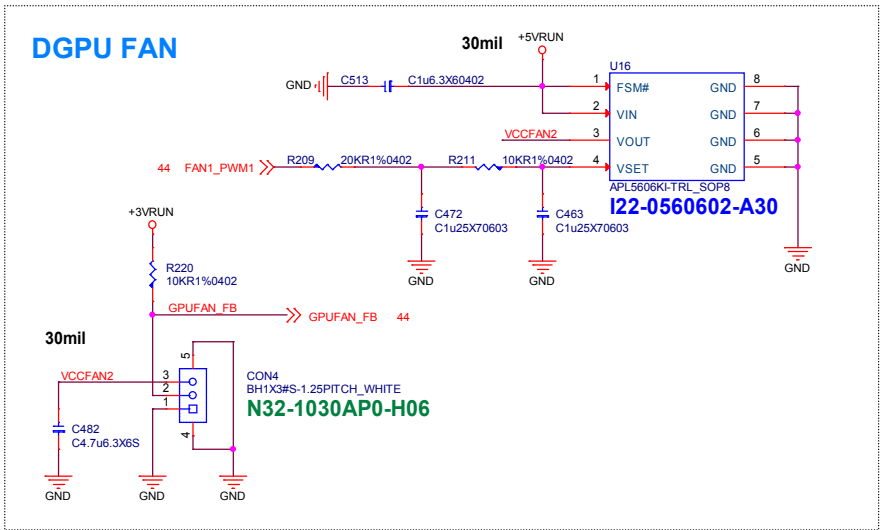
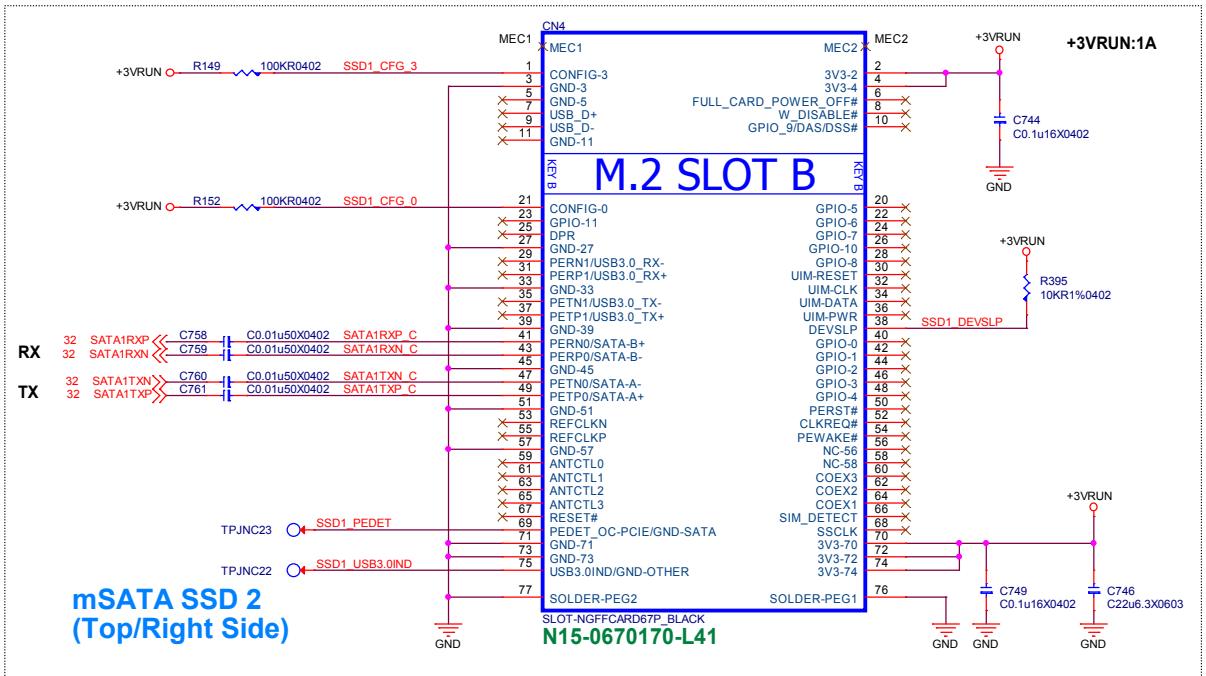
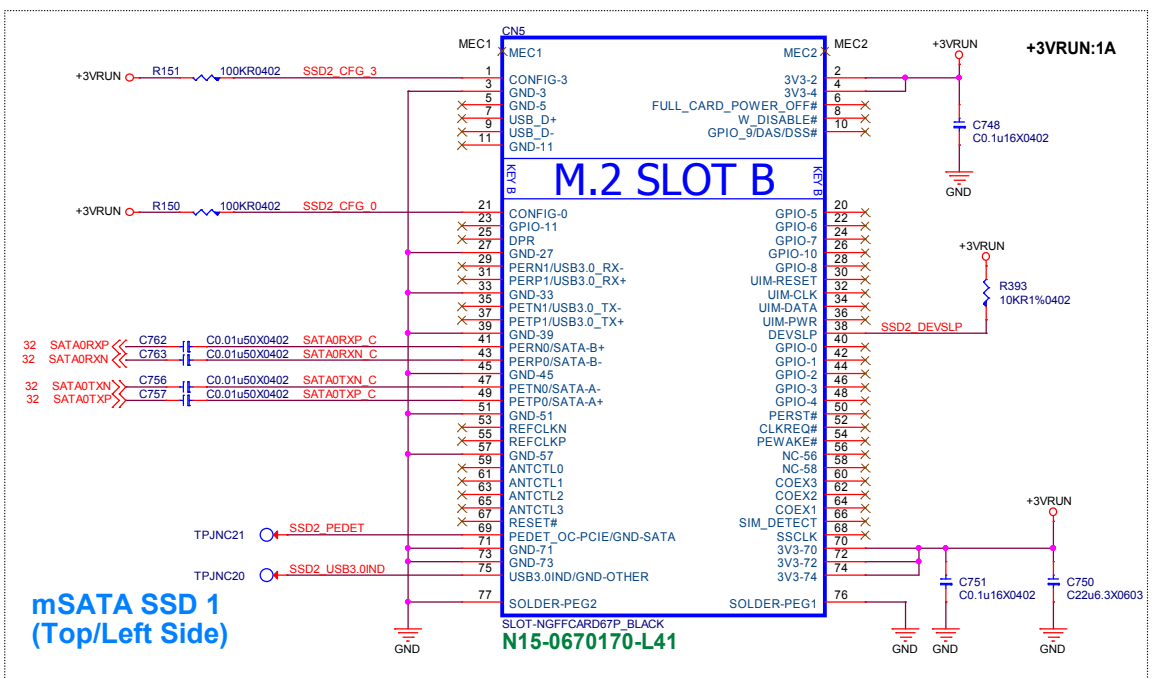
SSD/ DGPU FAN







40	NC	No Connect
41	SATA-B+/PERn0	Host receiver differential singal pair
42	NC	No Connect
43	SATA-B-/PERp0	Host receiver differential singal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A-/PETn0	Host Transmitter differential singal pair
48	NC	No Connect
49	SATA-A+/PETp0	Host Transmitter differential singal pair

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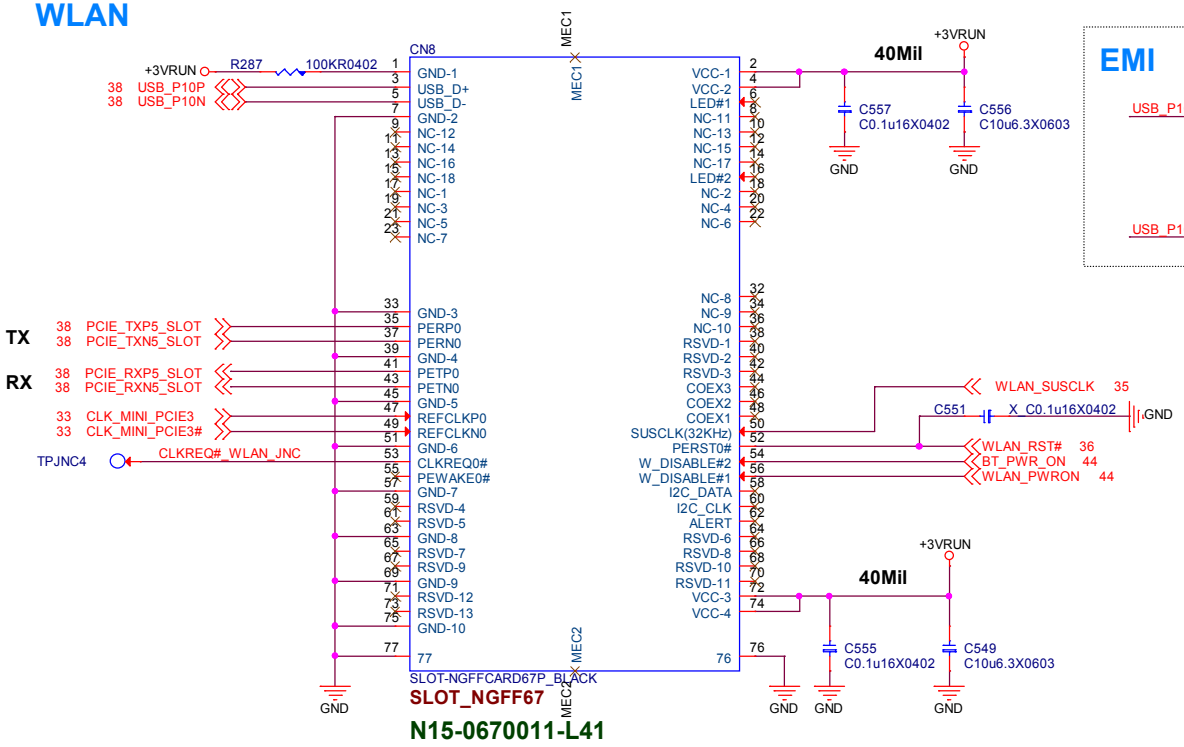
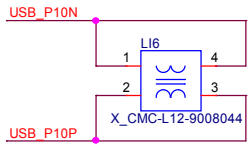
WLAN /Camera/ClickPad/FP

WLAN

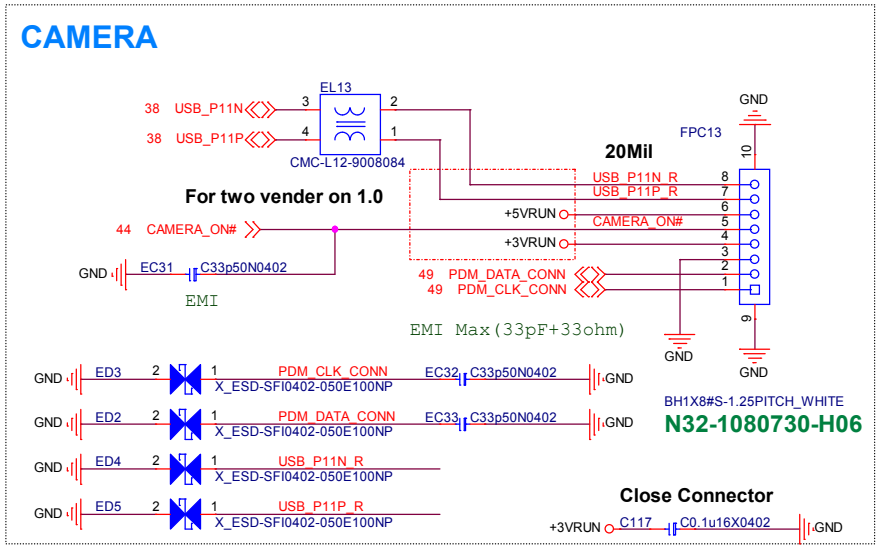


EMI

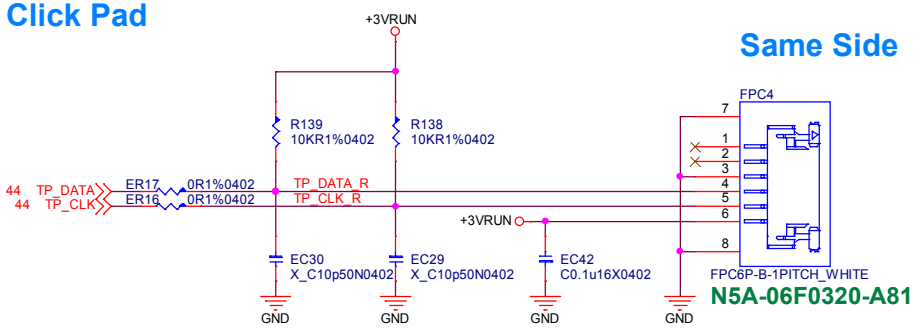


Pin 1	GND		
Pin 3	USB_D+	Pin 2	3.3V
Pin 5	USB_D-	Pin 4	3.3V
Pin 7	GND	Pin 6	LED1#
Pin 9	Module Key	Pin 8	Module Key
Pin 11	Module Key	Pin 10	Module Key
Pin 13	Module Key	Pin 12	Module Key
Pin 15	Module Key	Pin 14	Module Key
Pin 17	N/C	Pin 16	LED2#
Pin 19	N/C	Pin 18	GND
Pin 21	N/C	Pin 20	N/C
Pin 23	N/C	Pin 22	N/C
Pin 25	Module Key	Pin 24	Module Key
Pin 27	Module Key	Pin 26	Module Key
Pin 29	Module Key	Pin 28	Module Key
Pin 31	Module Key	Pin 30	Module Key
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN(W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	GND	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	GND	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V

CAMERA



Click Pad



Same Side

MICRO-STAR INT'L CO.,LTD.

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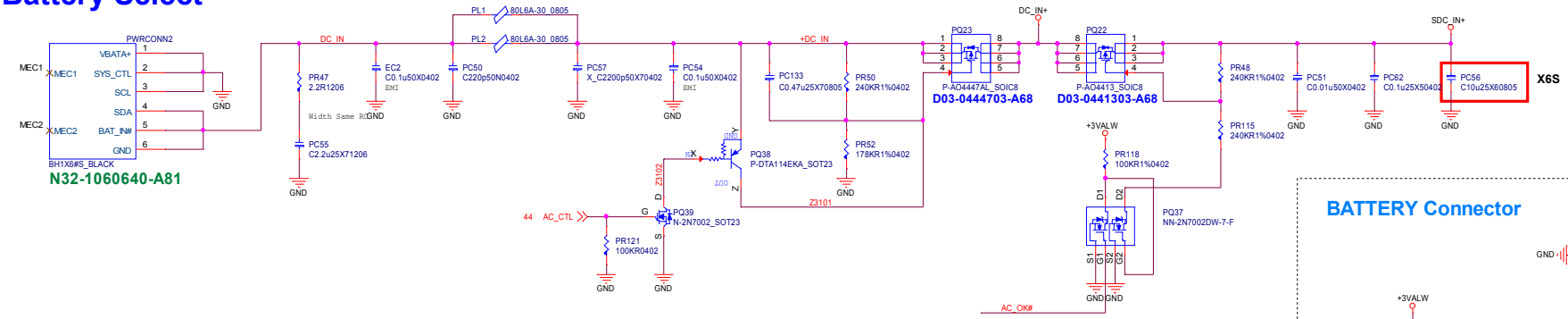
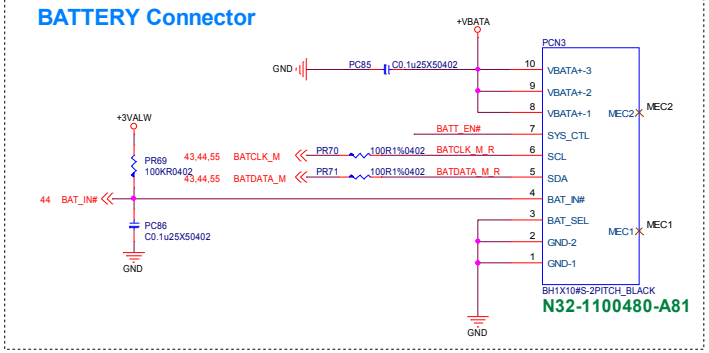
Battery Select/Charger

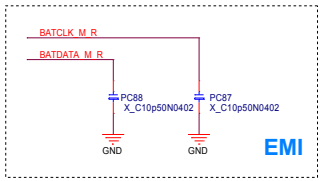
Battery Select



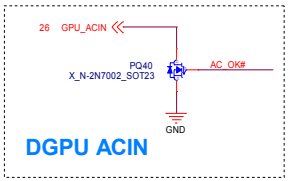
BATTERY Connector



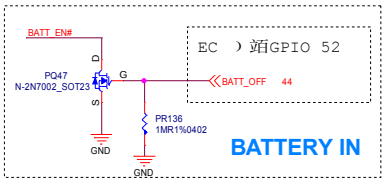
EMI



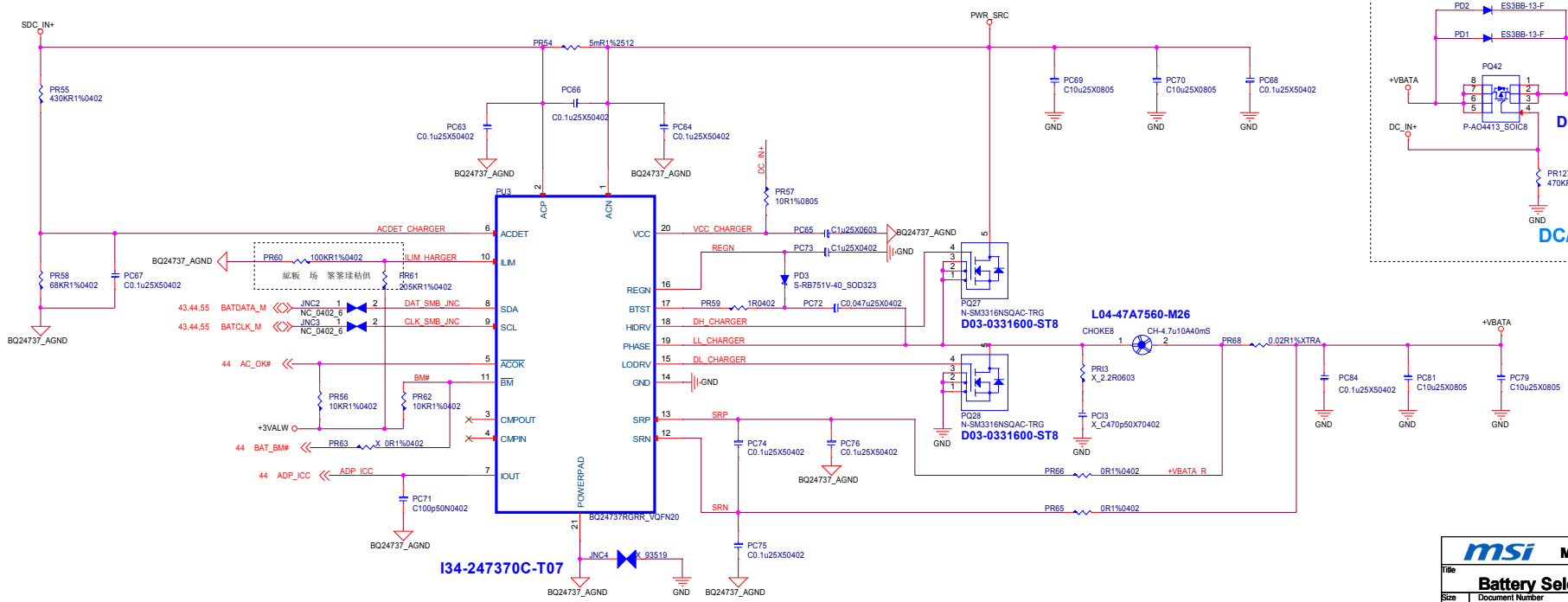
DGPU ACIN



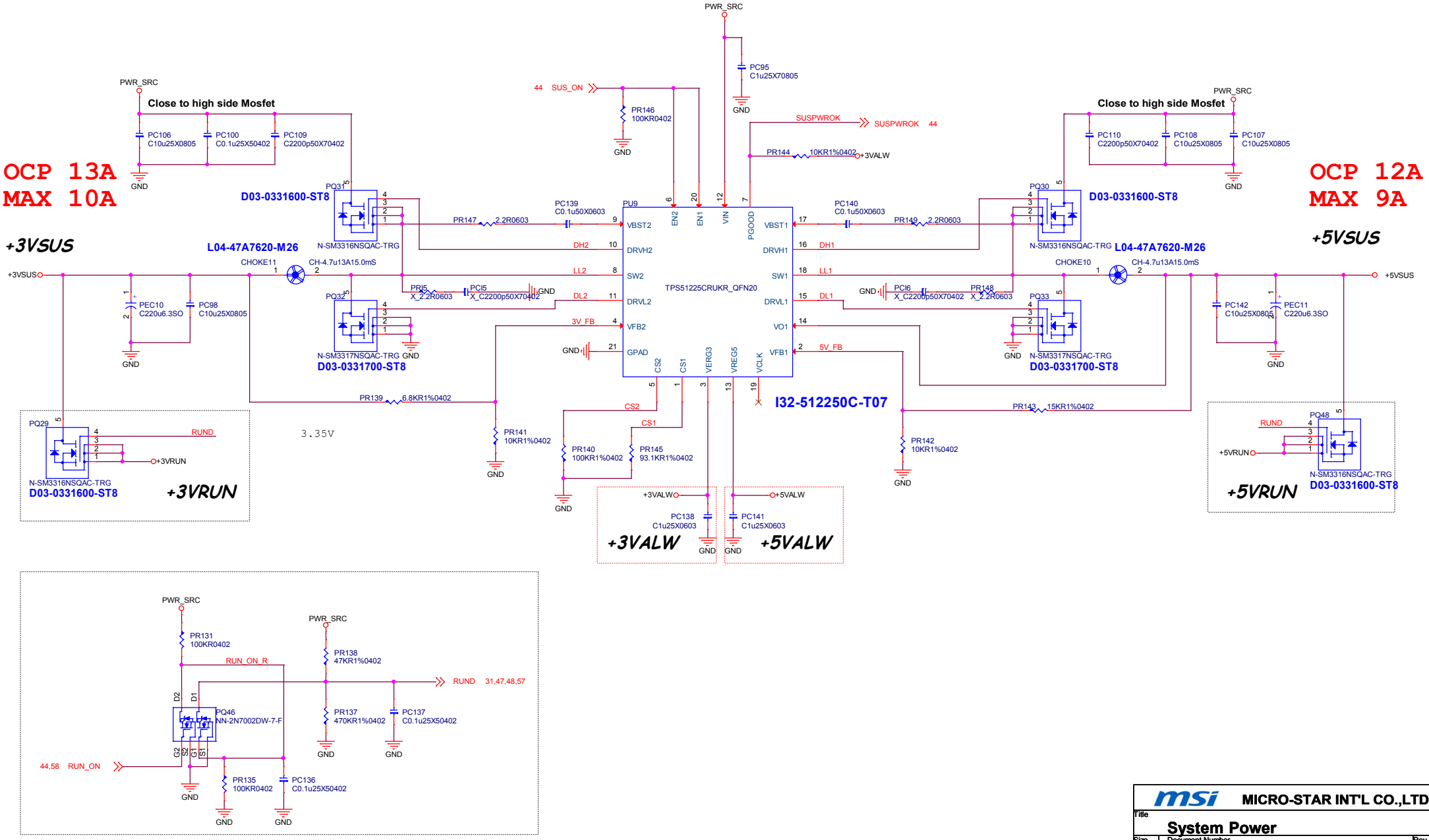
BATTERY IN



Battery Charger



System Power



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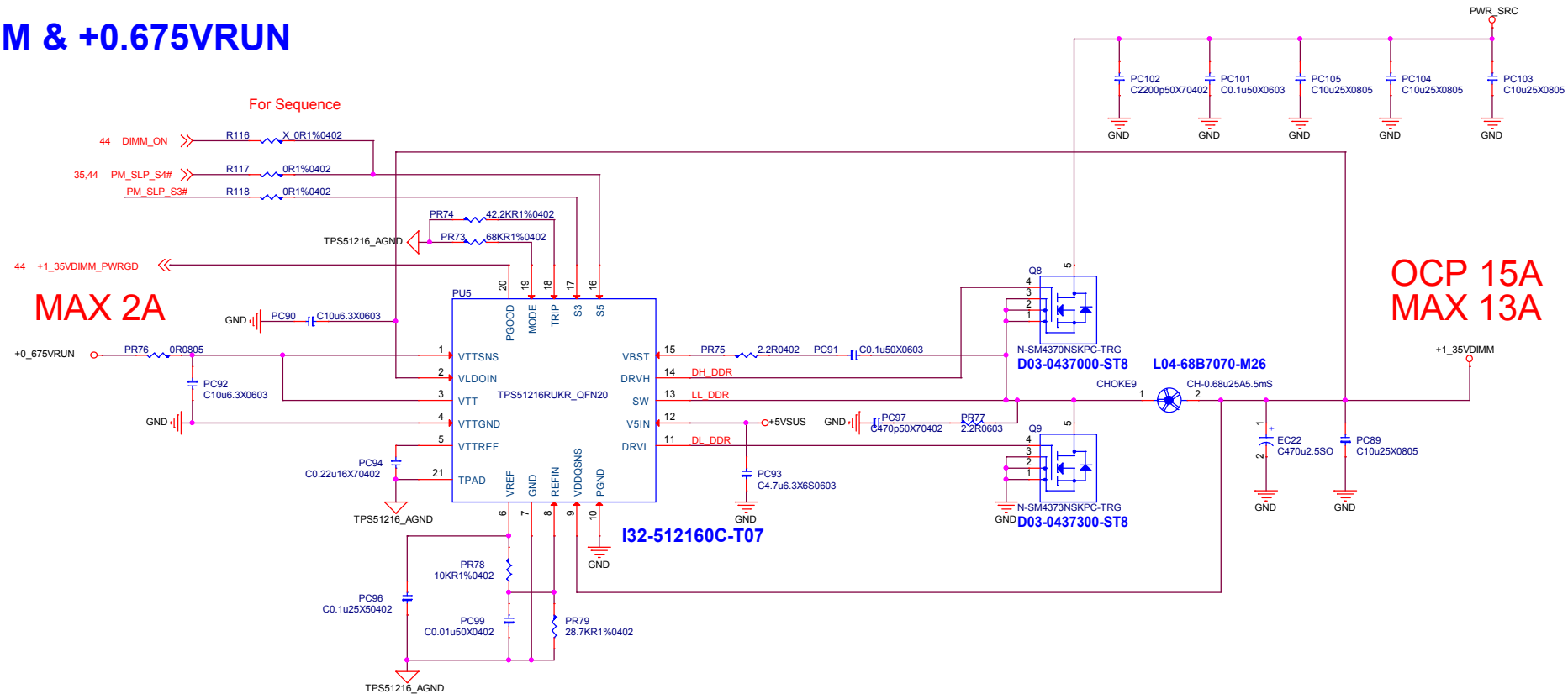
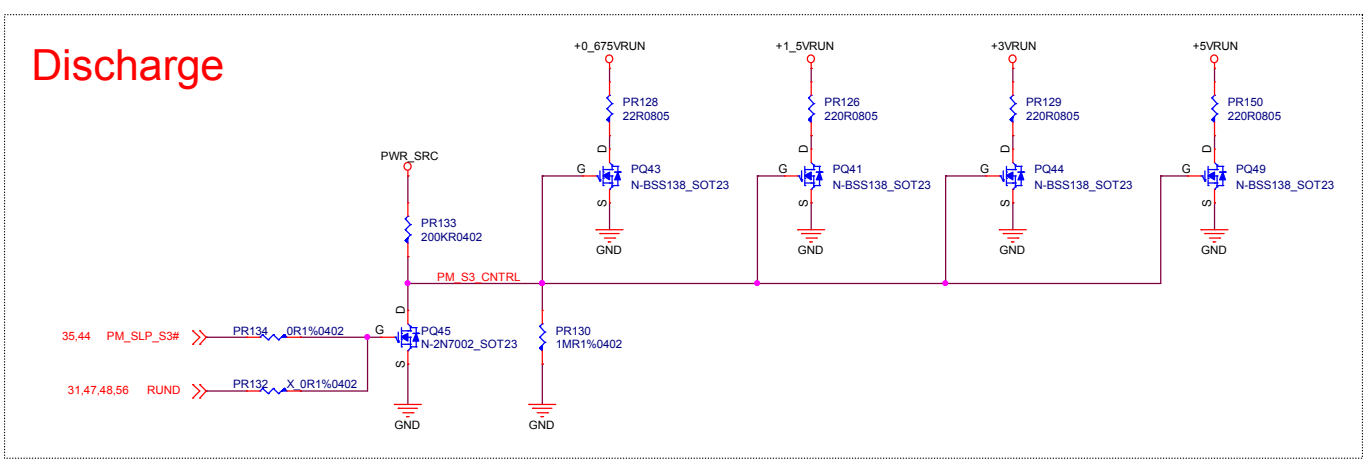
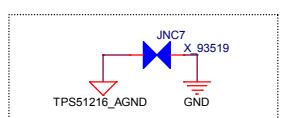
MICRO-STAR INT'L CO.,LTD.

+1.35VDIMM/+0.675VRUN

+1.35VDIMM & +0.675VRUN







MICRO-STAR INT'L CO.,LTD.		
Title: +1.35VDIMM/+0.675VRUN		
Size	Document Number: MS-16H5	Rev: 1.2
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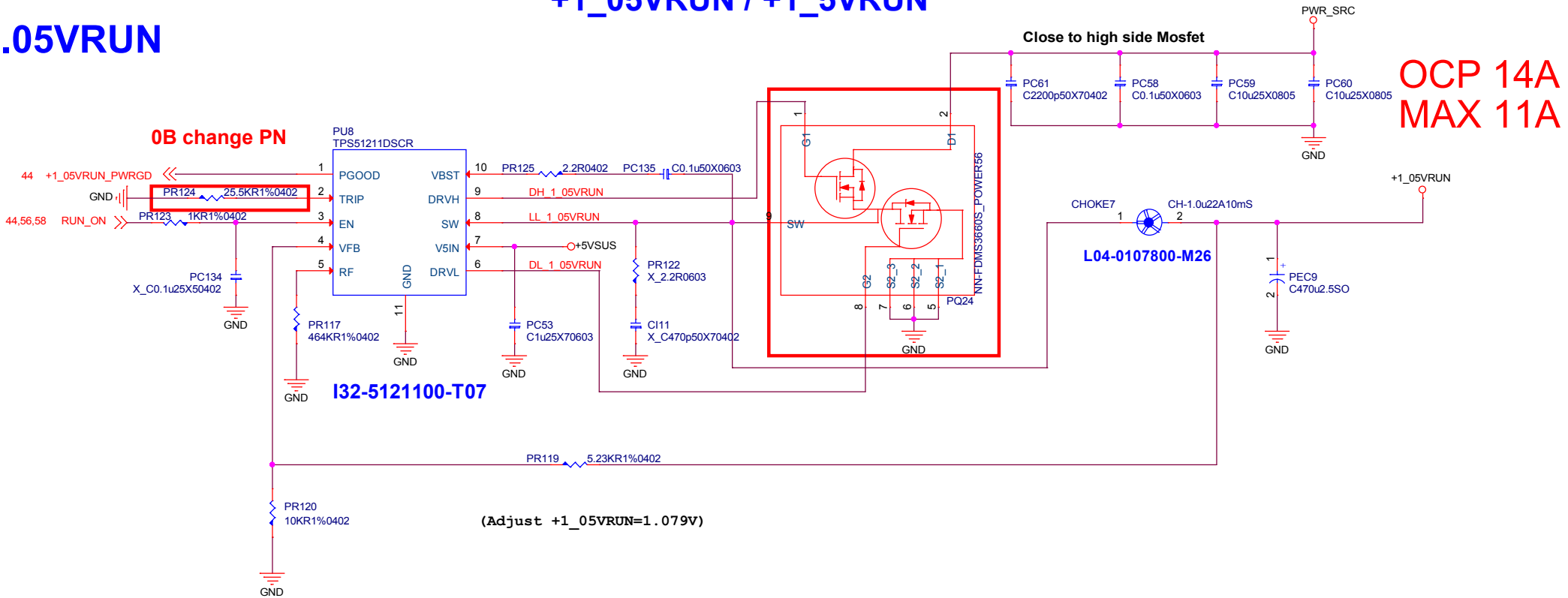
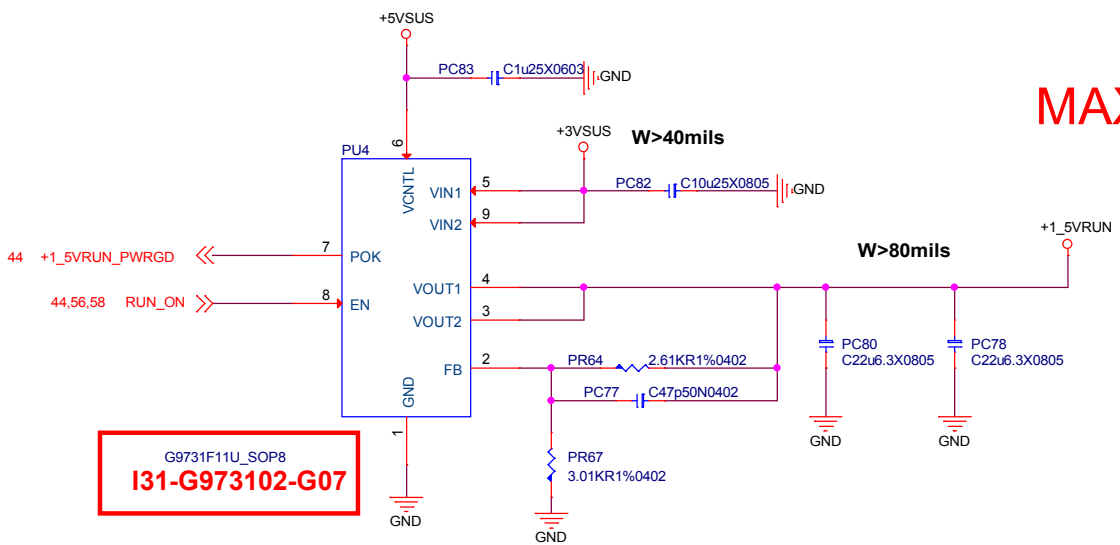
+1_05VRUN / +1_5VRUN

+1.05VRUN



+1.5VRUN



MICRO-STAR INT'L CO.,LTD.

Title	+1_05VRUN / +1_5VRUN	
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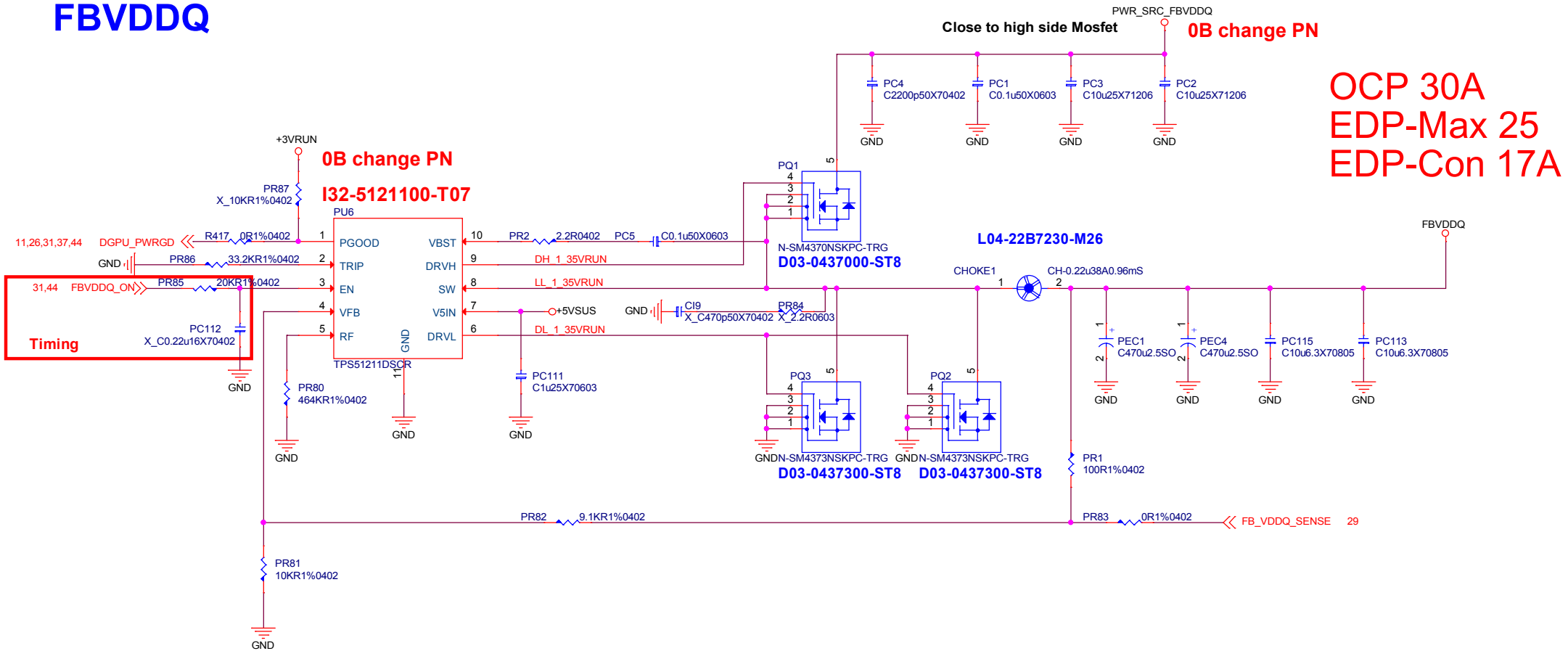
DGPU POWER FBVDDQ

FBVDDQ



MICRO-STAR INT'L CO.,LTD.		
Title: DGPU POWER FBVDDQ		
Size	Document Number: MS-16H5	Rev: 1.2
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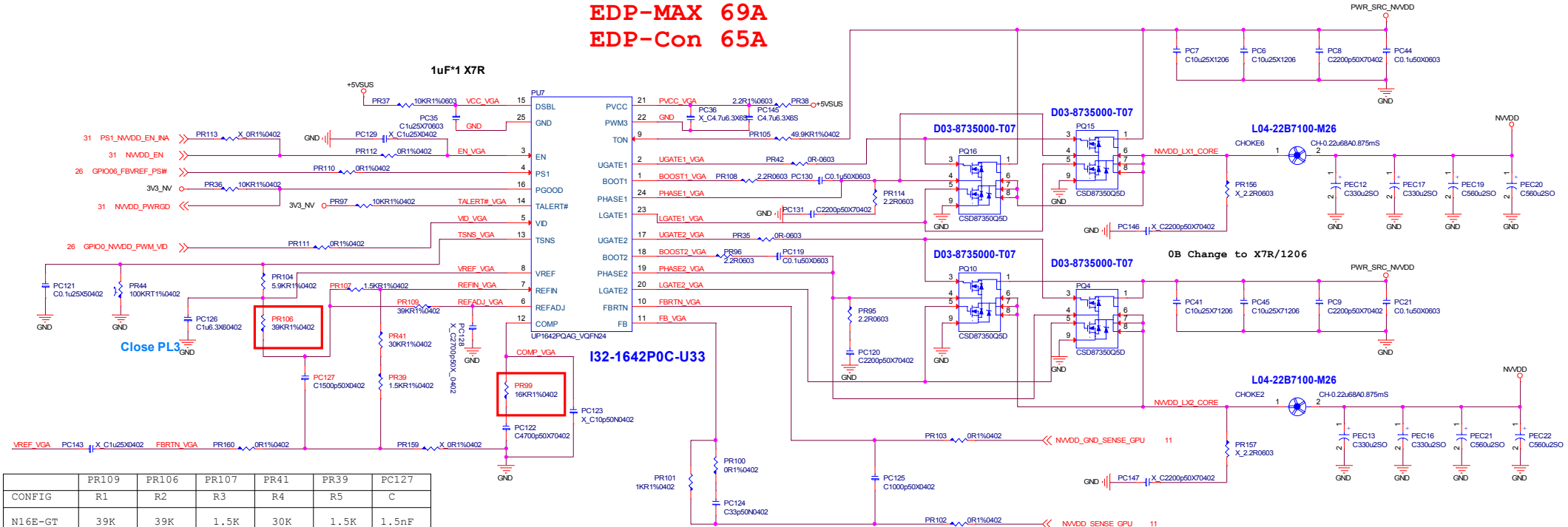
DGPU POWER NVVDD

DGPU POWER / UP1642PQAG

CONFIG B
VBoot:0.9V
Vmin:0.6V / Vmax:1.2V

EDP-Peak 130A
EDP-MAX 69A
EDP-Con 65A



	PR109	PR106	PR107	PR41	PR39	PC127
CONFIG	R1	R2	R3	R4	R5	C
N16E-GT	39K	39K	1.5K	30K	1.5K	1.5nF

Title	DGPU POWER NVVDD
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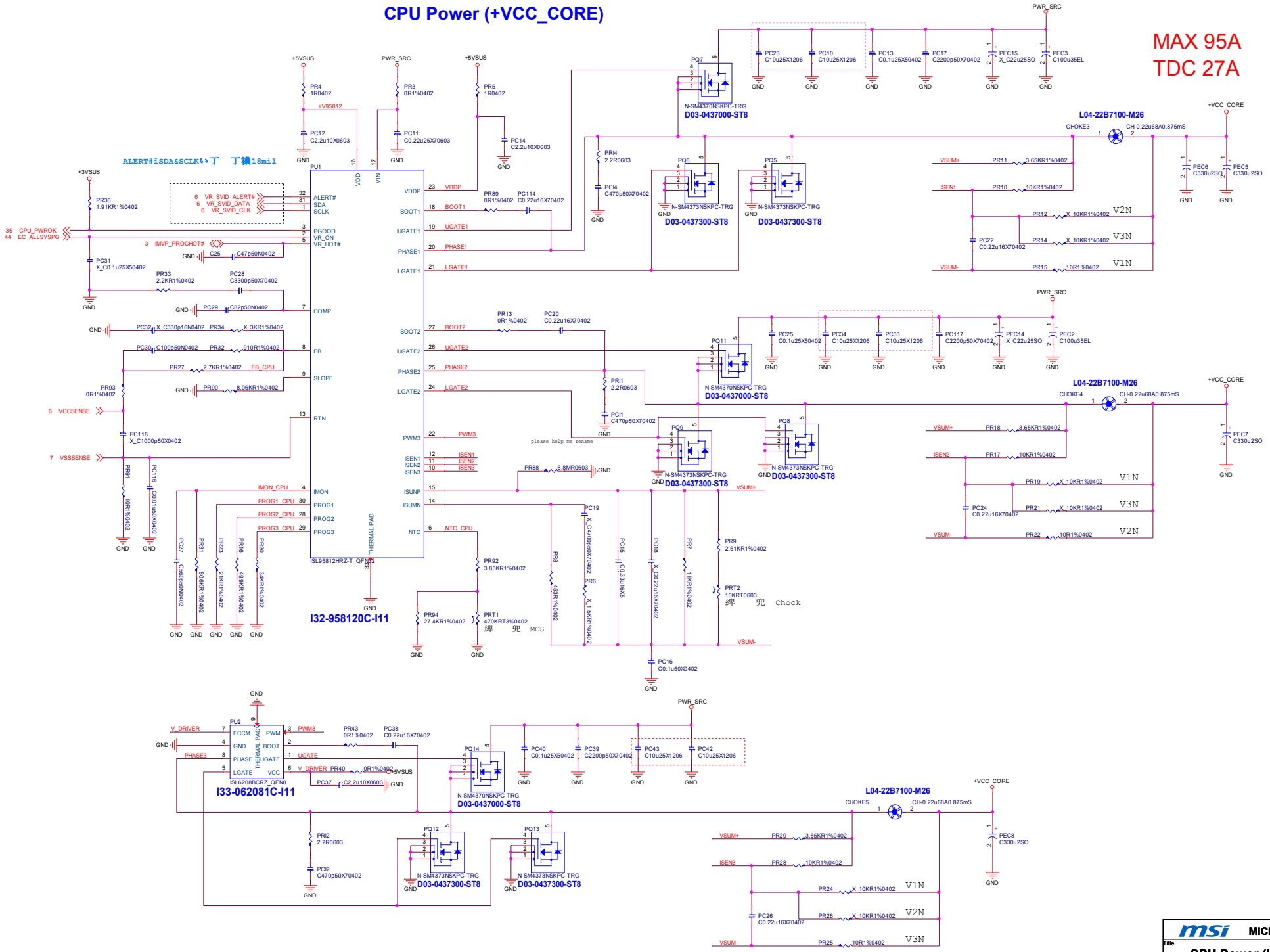
MICRO-STAR INT'L CO.,LTD.

CPU Power (+VCC_CORE)

MAX 95A
TDC 27A



msi	MICRO-STAR INT'L CO.,LTD.		
Title	CPU Power (ISL95812HRZ)		
Size	Document Number		Rev
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EMI/ Impedence

Impedence Connector No PN

40 ohm

J1 — 2 — L1_6.5mil_40_Ohm — 1 — GND2 — X_H1X2M_BLACK

J2 — 2 — L3_5mil_40_Ohm — 1 — GND2_GND4 — X_H1X2M_BLACK

J3 — 2 — L10_5mil_40_Ohm — 1 — GND9_GND11 — X_H1X2M_BLACK

45 ohm

J4 — 2 — L1_5.5mil_45_Ohm — 1 — GND2 — X_H1X2M_BLACK

J5 — 2 — L3_4mil_45_Ohm — 1 — GND2_GND4 — X_H1X2M_BLACK

J6 — 2 — L5_4mil_45_Ohm — 1 — GND4_GND6 — X_H1X2M_BLACK

J7 — 2 — L10_4mil_45_Ohm — 1 — GND9_GND11 — X_H1X2M_BLACK

J8 — 2 — L12_5.5mil_45_Ohm — 1 — GND11 — X_H1X2M_BLACK

50 ohm

J13 — 2 — L1_4mil_50_Ohm — 1 — GND2 — X_H1X2M_BLACK

J9 — 2 — L3_3mil_50_Ohm — 1 — GND2_GND4 — X_H1X2M_BLACK

J10 — 2 — L5_3mil_50_Ohm — 1 — GND4_GND6 — X_H1X2M_BLACK

J11 — 2 — L10_3mil_50_Ohm — 1 — GND9_GND11 — X_H1X2M_BLACK

J12 — 2 — L12_4mil_50_Ohm — 1 — GND11 — X_H1X2M_BLACK

80 ohm

J14	J15	J16	J17	J18
L1_DIFF_4.5/4/4.5_80ohm+	L3_DIFF_4.5/7/4.5_80ohm+	L5_DIFF_4.5/7/4.5_80ohm+	L10_DIFF_4.5/7/4.5_80ohm+	L12_DIFF_4.5/4/4.5_80ohm+
L1_DIFF_4.5/4/4.5_80ohm-	L3_DIFF_4.5/7/4.5_80ohm-	L5_DIFF_4.5/7/4.5_80ohm-	L10_DIFF_4.5/7/4.5_80ohm-	L12_DIFF_4.5/4/4.5_80ohm-
X_H1X4_BLACK	X_H1X4_BLACK	X_H1X4_BLACK	X_H1X4_BLACK	X_H1X4_BLACK
GND2	GND2_GND4	GND4_GND6	GND9_GND11	GND11

85 ohm

J19	J20	J21	J22	J23
L1_DIFF_4.5/4.5/4.5_85ohm+	L3_DIFF_4/6.5/4_85ohm+	L5_DIFF_4/6.5/4_85ohm+	L10_DIFF_4/6.5/4_85ohm+	L12_DIFF_4.5/4.5/4.5_85ohm+
L1_DIFF_4.5/4.5/4.5_85ohm-	L3_DIFF_4/6.5/4_85ohm-	L5_DIFF_4/6.5/4_85ohm-	L10_DIFF_4/6.5/4_85ohm-	L12_DIFF_4.5/4.5/4.5_85ohm-
X_H1X4_BLACK	X_H1X4_BLACK	X_H1X4_BLACK	X_H1X4_BLACK	X_H1X4_BLACK
GND2	GND2_GND4	GND4_GND6	GND9_GND11	GND11

88 ohm

J24	J25	J26	
L1_DIFF_4.5/6/4.5_88ohm+	L3_DIFF_3.5/4.5/3.5_88ohm+	L10_DIFF_3.5/4.5/3.5_88ohm+	
L1_DIFF_4.5/6/4.5_88ohm-	L3_DIFF_3.5/4.5/3.5_88ohm-	L10_DIFF_3.5/4.5/3.5_88ohm-	
X_H1X4_BLACK	X_H1X4_BLACK	X_H1X4_BLACK	
GND2	GND2_GND4	GND9_GND11	

90 ohm

J27	J28	J29	J30	J31
L1_DIFF_4/6/4_90ohm+	L3_DIFF_3.5/5.5/3.5_90ohm+	L5_DIFF_3.5/5.5/3.5_90ohm+	L10_DIFF_3.5/5.5/3.5_90ohm+	L12_DIFF_4/6/4_90ohm+
L1_DIFF_4/6/4_90ohm-	L3_DIFF_3.5/5.5/3.5_90ohm-	L5_DIFF_3.5/5.5/3.5_90ohm-	L10_DIFF_3.5/5.5/3.5_90ohm-	L12_DIFF_4/6/4_90ohm-
X_H1X4_BLACK	X_H1X4_BLACK	X_H1X4_BLACK	X_H1X4_BLACK	X_H1X4_BLACK
GND2	GND2_GND4	GND4_GND6	GND9_GND11	GND11

100 ohm

J32	J33	J34	J35	J36
L1_DIFF_3.5/7.5/3.5_100ohm+	L3_DIFF_3/10/3_100ohm+	L5_DIFF_3/10/3_100ohm+	L10_DIFF_3/10/3_100ohm+	L12_DIFF_3.5/7.5/3.5_100ohm+
L1_DIFF_3.5/7.5/3.5_100ohm-	L3_DIFF_3/10/3_100ohm-	L5_DIFF_3/10/3_100ohm-	L10_DIFF_3/10/3_100ohm-	L12_DIFF_3.5/7.5/3.5_100ohm-
X_H1X4_BLACK	X_H1X4_BLACK	X_H1X4_BLACK	X_H1X4_BLACK	X_H1X4_BLACK
GND2	GND2_GND4	GND4_GND6	GND9_GND11	GND11

CLAMP

CLAMP1	CLAMP2	CLAMP4	CLAMP5	CLAMP6	CLAMP7	CLAMP8	CLAMP9
GND	GND	GND	GND	GND	GND	GND	GND
E21-5801010-RH	E21-5801010-RH	E21-5801010-RH	E21-5801010-RH	E21-5801010-RH	E21-5801010-RH	E21-5801010-RH	E21-5801010-RH

EMI

RFI

PWR_SRC
- EC43 C0.1u25X50402
- EC44 C0.1u25X50402
- EC45 C0.1u25X50402
- EC46 C0.1u25X50402
- EC47 C0.1u25X50402
- EC48 X_C0.1u25X50402
- EC49 X_C0.1u25X50402

RFI

- EC50 C1000p50X0402
- EC51 C0.1u25X50402
- EC52 C0.1u25X50402
- EC53 C0.1u25X50402

GND

PWR_SRC_NVVDD
- EC54 X_C0.1u25X50402
- EC55 X_C0.1u25X50402
- EC56 X_C0.1u25X50402

GND

PWR_SRC_FBVDDQ
- EC57 C0.1u25X50402

GND

+VBATA
- EC58 C0.1u25X50402
- EC59 C0.1u25X50402

RFI

GND

+3VRUN
- EC60 X_C0.1u25X50402

GND

NVVDD
- EC73 X_C0.1u25X50402
- EC72 X_C0.1u25X50402
- EC74 X_C0.1u25X50402

GND

+1_35VDIMM
- EC69 X_C0.1u25X50402
- EC70 X_C0.1u25X50402
- EC71 X_C0.1u25X50402

GND

+1_05VRUN
- EC75 X_C0.1u25X50402

GND

+3VSUS
- EC66 C0.1u25X50402
- EC67 X_C0.1u25X50402

GND

+0_675VRUN
- EC68 X_C0.1u25X50402

GND

+5VSUS
- EC61 X_C0.1u25X50402
- EC62 X_C0.1u25X50402
- EC63 X_C0.1u25X50402
- EC64 X_C0.1u25X50402
- EC65 X_C0.1u25X50402

GND

MICRO-STAR INT'L CO.,LTD.

Title	EMI/ Impedence	
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CPU/GPU Holes

MCPU4 H_R200D150 — GND X_CPU_HOLE
MCPU2 H_R200D150 — GND X_CPU_HOLE
MCPU3 H_R200D150 — GND X_CPU_HOLE
MCPU1 H_R200D150 — GND X_CPU_HOLE

MGPU2 H_R276D169_PB — GND X_CPU_HOLE
MGPU4 H_R276D169_PB — GND X_CPU_HOLE
MGPU1 H_R276D169_PB — GND X_CPU_HOLE
MGPU3 H_R276D169_PB — GND X_CPU_HOLE

M2 X_H_R197D118_PT_V3 H_R197D118_PT_V3 — GND
M7 X_H_R197D118_PT_V3 H_R197D118_PT_V3 — GND

Fan Hole

MH1 H_R197D91 X_ME_ SCREW HOLE — GND

SSD Stand off

MH3 H_R220D146_PTB E2B-16H2020 — GND
MH2 H_R220D146_PTB E2B-16H2020 — GND

MH4 NPTH157 X_NPTH157

EMI

SPRING1 HS-MS-1721 — GND — E2M-7213211-CA7 — ATE_C006_106
SPRING2 HS-MS1058 — GND — E2M-2142011-CA7 — ATE_C006_106
SPRING3 HS-MS-1029 — GND — E23-1029060-CA7 — ATE_C006_106

MYLAR1 — E2P-6H22111-Y42 — MYLAR
MYLAR2 — E2P-6H24211-Y42 — MYLAR
MYLAR3 — E2P-6H22711-Y42 — MYLAR
MYLAR4 — E2P-6H23011-Y42 — MYLAR
MYLAR5 — E2P-6H23111-Y42 — MYLAR
MYLAR6 — E2P-6G13911-Y42 — MYLAR

RUBBER1 — E2Y-6H20712-Y40 — RUBBER
RUBBER2 — E2Y-6H21312-Y40 — RUBBER
RUBBER3 — E2Y-6H21312-Y40 — RUBBER

BRACKET1 — 307-6H20111-C22 — CPU_BRACKET
BRACKET2 — 307-6H20111-C22 — CPU_BRACKET
BRACKET3 — 307-6H20211-C22 — GPU_BRACKET

GASKET1 — E2Y-X005511-CA7 — X_GASKET

FM1 X_F_PAD_X
FM2 X_F_PAD_X
FM3 X_F_PAD_X
FM4 X_F_PAD_X
FM5 X_F_PAD_X
FM6 X_F_PAD_X
FM7 X_F_PAD_X
FM8 X_F_PAD_X

UME1 — HDMI Lable — HDMI ROYALTY — Y01-RHDMI03-000
UME2 — BIOS Lable — BIOS_LABEL — G51-LA01678-A09

For MP

PCB1 — PF0-16H5112-H73
PF0-16H5112-H73
Hannstar: PF0-16H5112-H73
TRIPOD: PF0-16H5112-T53

MICRO-STAR INT'L CO.,LTD.

Title	Screw/ME	
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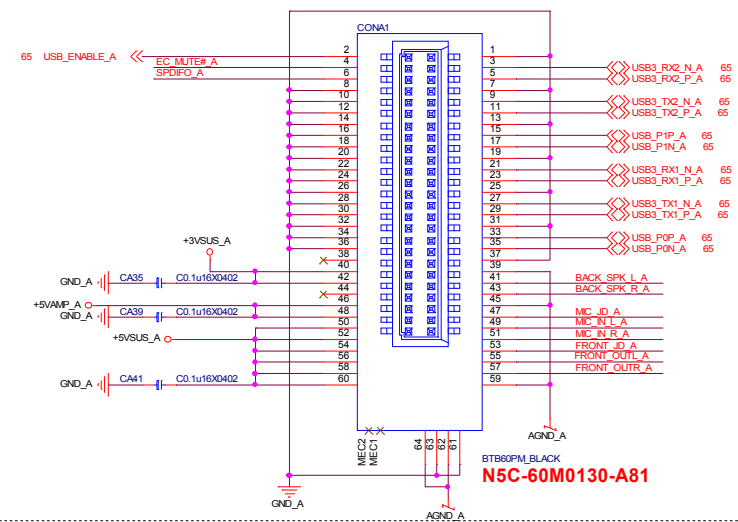
16H5-A Board (Audio CONN)

BTB Connector From MB

CONN Pin Current Capability : 0.5A/Pin



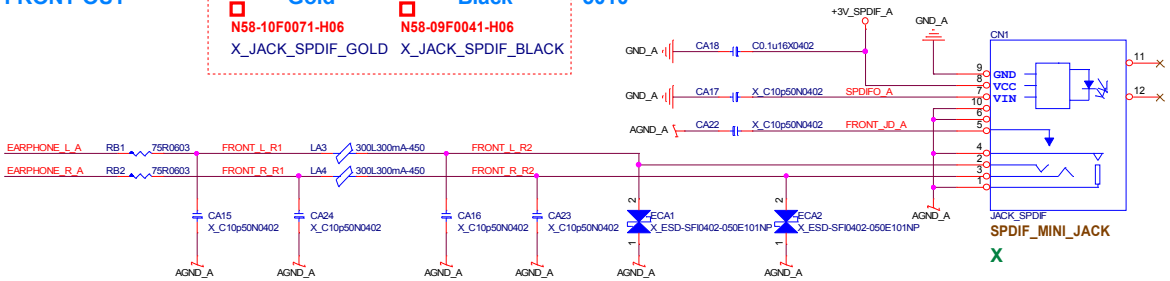
N5C-60M0130-A81

FRONT OUT

SPDIF1 Gold — N58-10F0071-H06 — X_JACK_SPDIF_GOLD

SPDIF2 Black — N58-09F0041-H06 — X_JACK_SPDIF_BLACK

5010



SPDIF_MINI_JACK

X

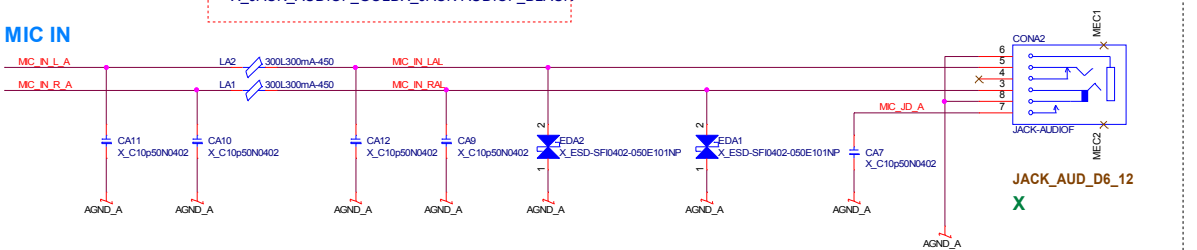
MIC IN

MIC1 Gold — N54-06F1191-H06

MIC2 Black — N54-06F0481-H06

X_JACK_AUDIOF_GOLDX_JACK-AUDIOF_BLACK

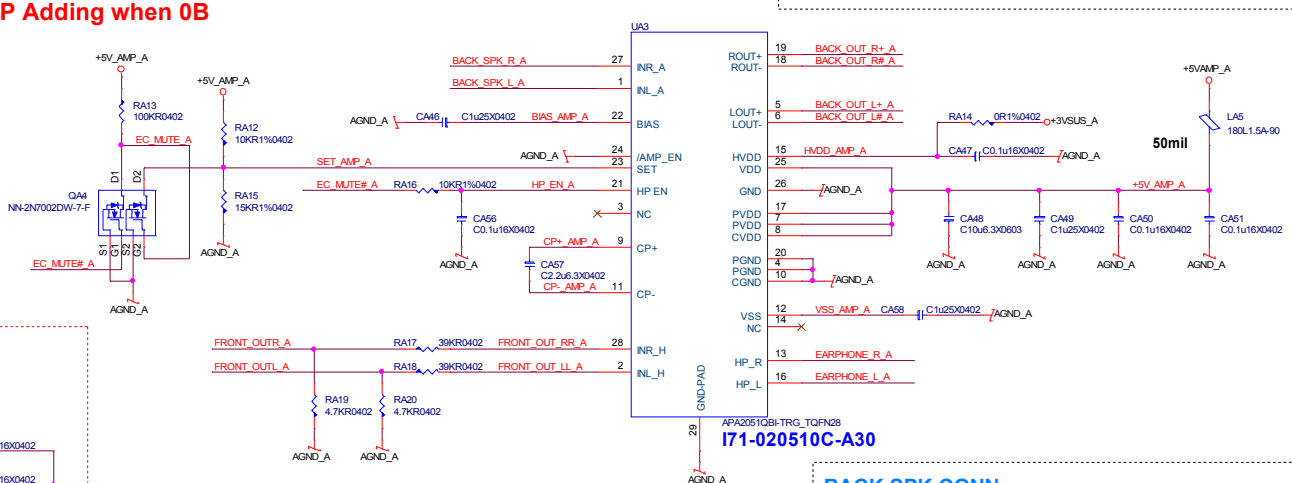
5010



JACK_AUD_D6_12

X

AMP Adding when 0B

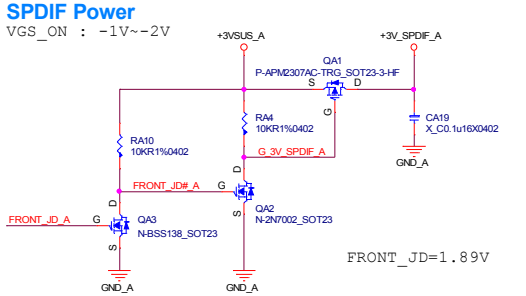


APA2051QBI-TRG_TQFN28

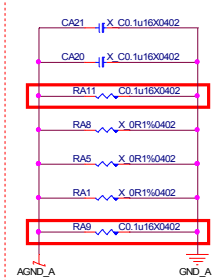
I71-020510C-A30

SPDIF Power

VGS_ON : -1V~-2V



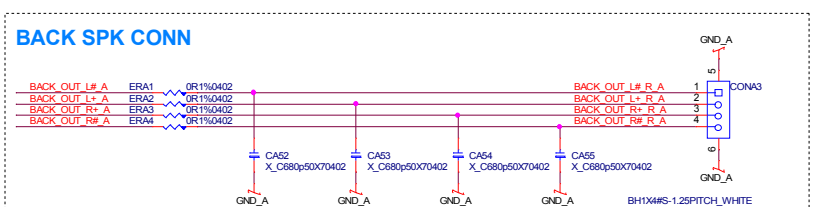
EMI



Change to Cap

Change to Cap

BACK SPK CONN



N32-1040AV0-H06

MICRO-STAR INT'L CO.,LTD.

Title: [A] Audio

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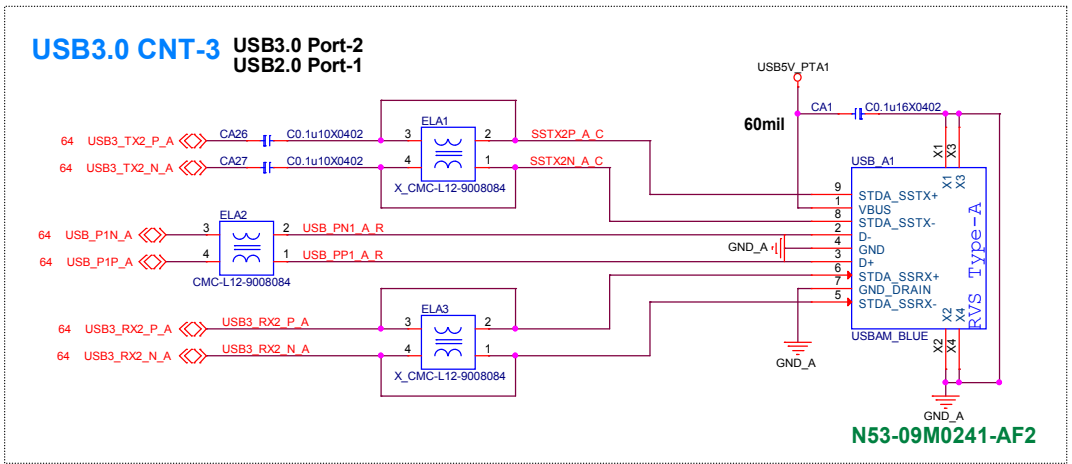
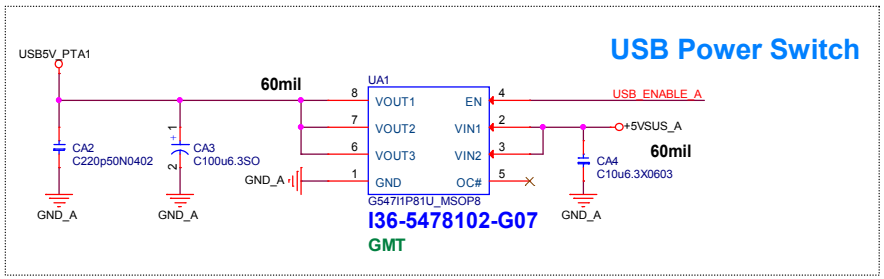
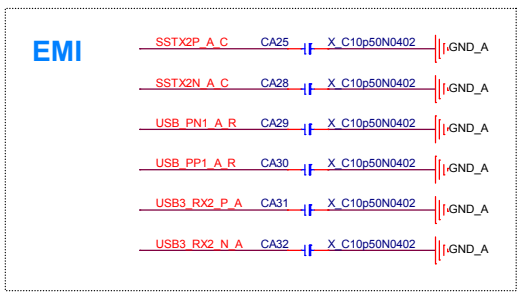
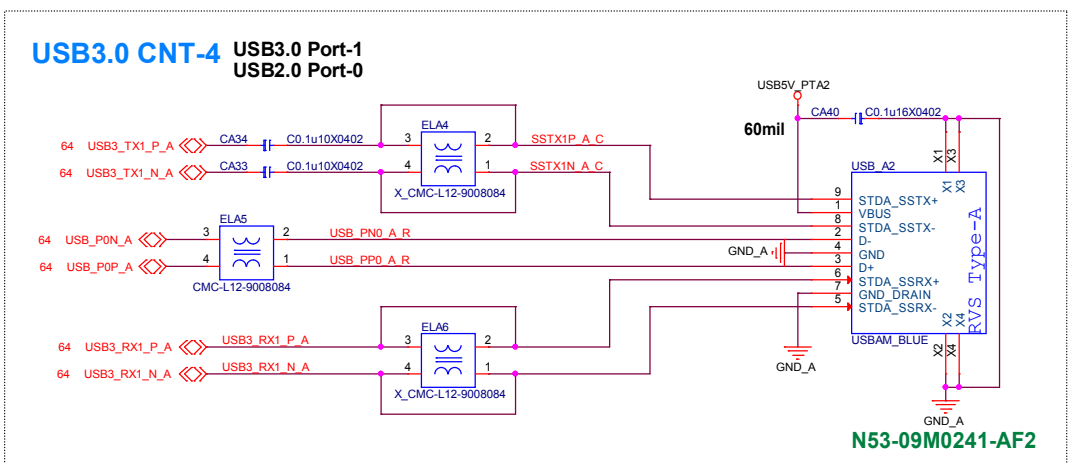
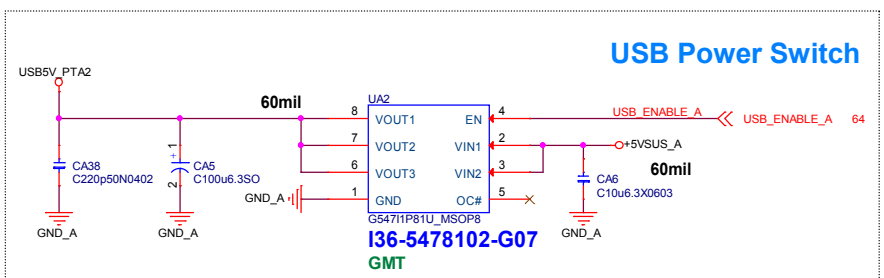
[A] USB3.0 CNT-2/-3

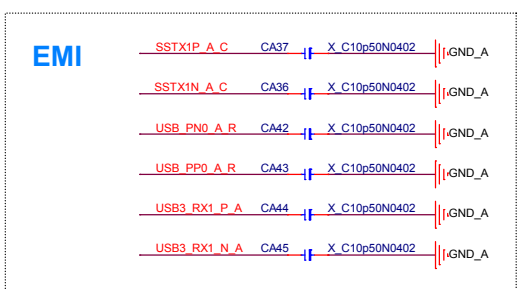


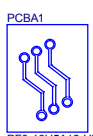












PF0-16H5A12-H73

Hannstar: PF0-16H5A12-H73
TRIPOD: PF0-16H5A12-T53

MYLARA1	MYLARA2
E2P-6H22812-G40	E2P-6H22311-G40
MYLAR	MYLAR

MICRO-STAR INT'L CO.,LTD.

Title	[A] USB3.0 CNT-3/-4	
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16H5-B Board (LED Board)

LED

BLUE (HDD)

+5VRUN_B → RB4 1KR1%0603 → HDD_LIGHT_A → DB2 LED04-B-20mA2.8V_1608 → LED_HDD# _B

D0C-04018F0-L05

GND_B → EDB3 2 → 1 X_ESD-DIODE

BLUE (BT)

RB6 1KR1%0603 → BT_LIGHT_A → DB5 LED04-B-20mA2.8V_1608 → LED_BLUETOOTH# _B

D0C-04018F0-L05

GND_B → EDB6 2 → 1 X_ESD-DIODE

BLUE (WLAN)

RB7 1KR1%0603 → WLAN_LIGHT_A → DB6 LED04-B-20mA2.8V_1608 → LED_WLAN# _B

D0C-04018F0-L05

GND_B → EDB7 2 → 1 X_ESD-DIODE

ORANGE (BATLOW)

+5VALW_B → RB8 220R0603 → BATL_LIGHT_A → DB7 LED04-O-30mA2.6V_1608 → LED_BATLOW# _B

D0C-040E200-L05

GND_B → EDB8 2 → 1 X_ESD-DIODE

BLUE (CHARGE)

RB10 1KR1%0603 → CHA_LIGHT_A → DB8 LED04-B-20mA2.8V_1608 → LED_CHARGE# _B

D0C-04018F0-L05

GND_B → EDB1 2 → 1 X_ESD-DIODE

BLUE (CAP)

+5VRUN_B → RB9 1KR1%0603 → CAP_LIGHT_A → DB4 LED04-B-20mA2.8V_1608 → LED_CAP# _B

D0C-04018F0-L05

GND_B → EDB5 2 → 1 X_ESD-DIODE

BLUE (NUM)

RB5 1KR1%0603 → NUM_LIGHT_A → DB3 LED04-B-20mA2.8V_1608 → LED_NUM# _B

D0C-04018F0-L05

GND_B → EDB4 2 → 1 X_ESD-DIODE

BLUE (ACPI)

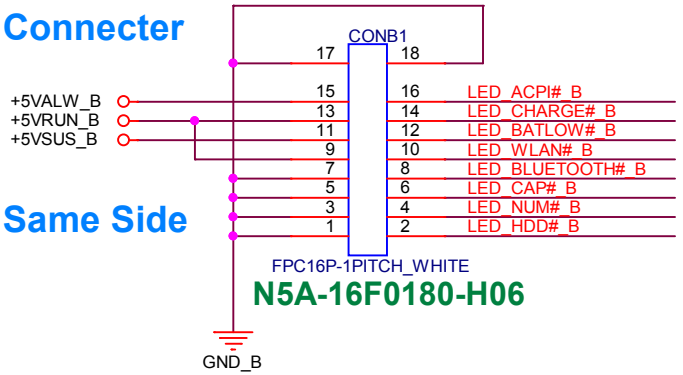
+5VSUS_B → RB3 1KR1%0603 → ACPI_LIGHT_A → DB1 LED04-B-20mA2.8V_1608 → LED_ACPI# _B

D0C-04018F0-L05

GND_B → EDB2 2 → 1 ESD-DIODE

Connecter

Same Side



MHB1 H_R197D91 X_ME_SCREW HOLE → GND_B

MHB2 H_R197D91 X_ME_SCREW HOLE → GND_B

PCBB1

PF0-16H5B12-H73

PF0-16H5B12-H73

Hannstar: PF0-16H5B12-H73
TRIPOD: PF0-16H5B12-T53

+5VALW_B	CB5	C0.1u16X0402	GND_B
+5VRUN_B	CB6	C0.1u16X0402	GND_B
+5VRUN_B	CB7	C0.1u16X0402	GND_B
+5VSUS_B	CB8	C0.1u16X0402	GND_B

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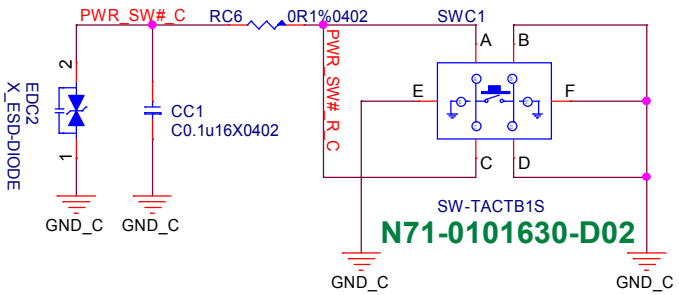
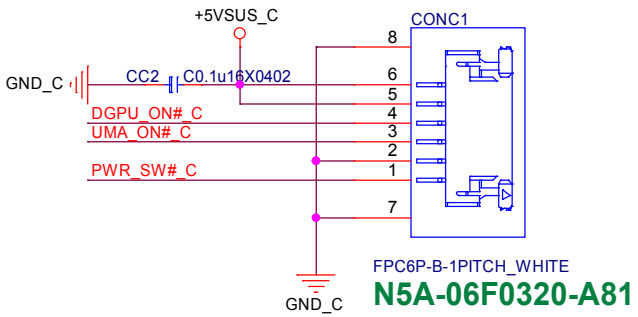
16H5-C Board (Power SW Board)

Power Switch

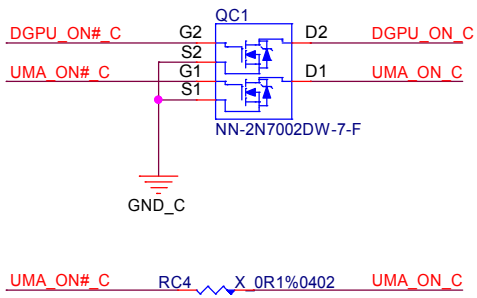


Diff Side Connecter

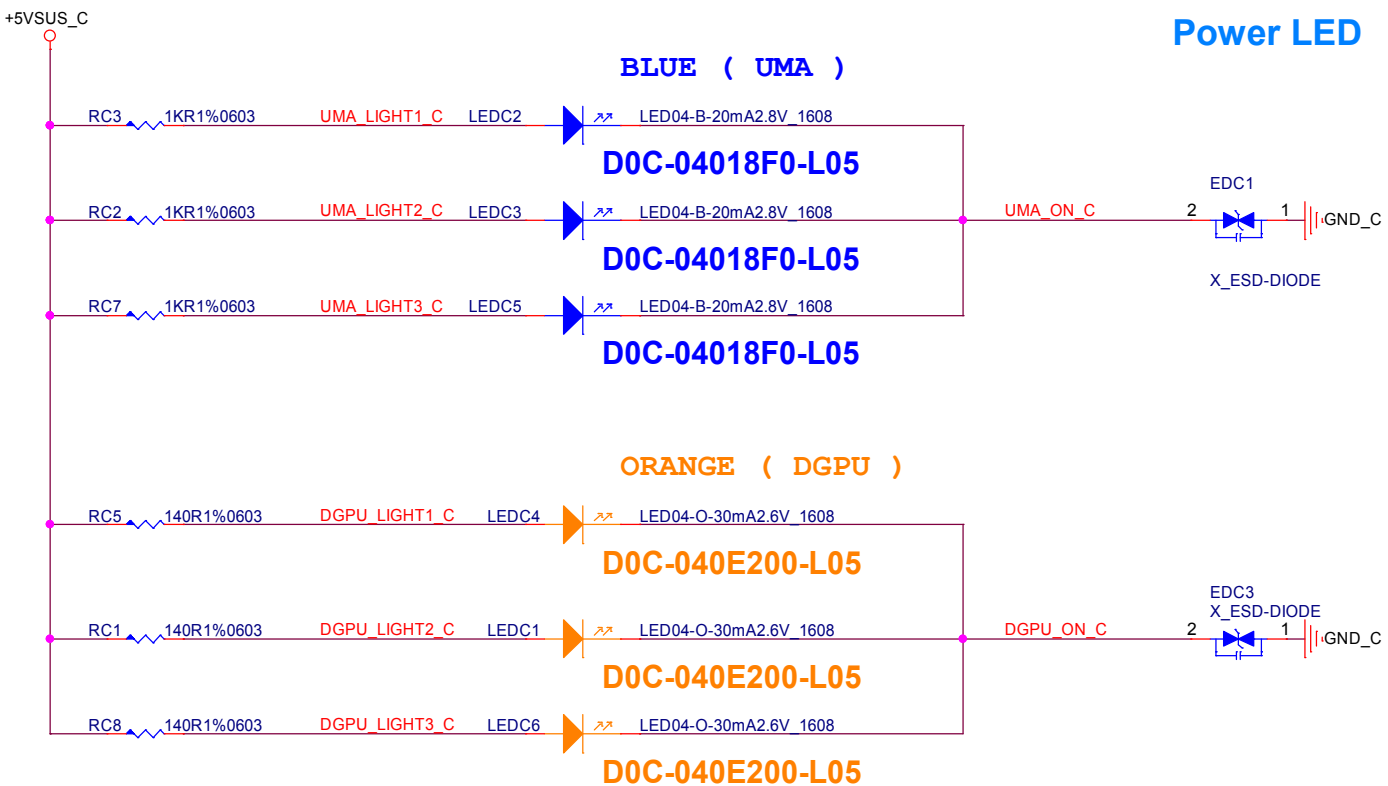


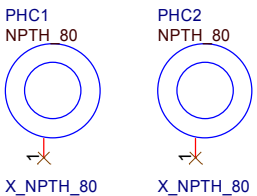
UMA/DGPU Logic

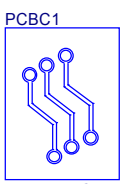
MOS Ton, Toff 20ns

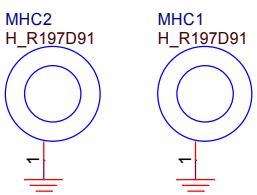


Power LED









PF0-16H5C12-H73

Hannstar: PF0-16H5C12-H73
TRIPOD: PF0-16H5C12-T53

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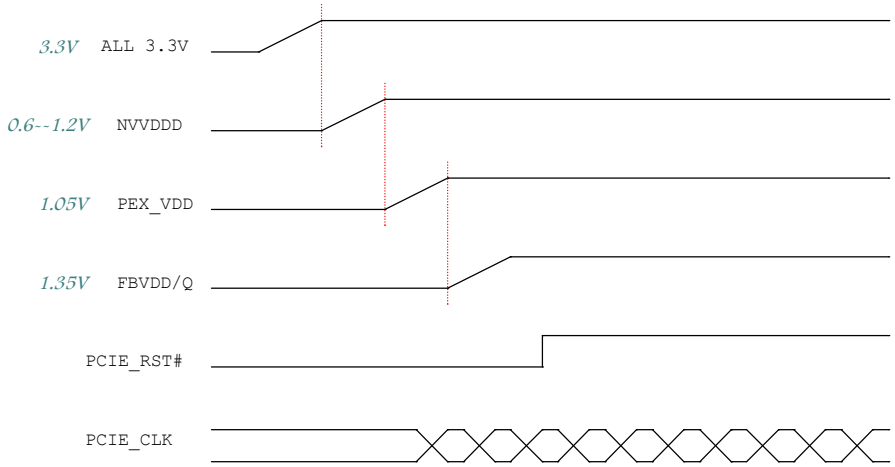
MS-16H5 DGPU POWER SEQUENCE

GPU POWER ON SEQUENCE



NOTES:

1. The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
2. The ramp up overshoot should not exceed the silicon reliability limit voltagr.
3. A VDD33 must ramp up to 90% before NVVDD and PEX_VDD in sequence can ramping up.
   NVVDD must ramp up to 90% before FBVDD/Q in sequence can ramping up.
3. No signal should be applied to the GPU before the power rails are fully ramped.
4. Refer to JEDEC Memory Specification for memory related power sequencing.

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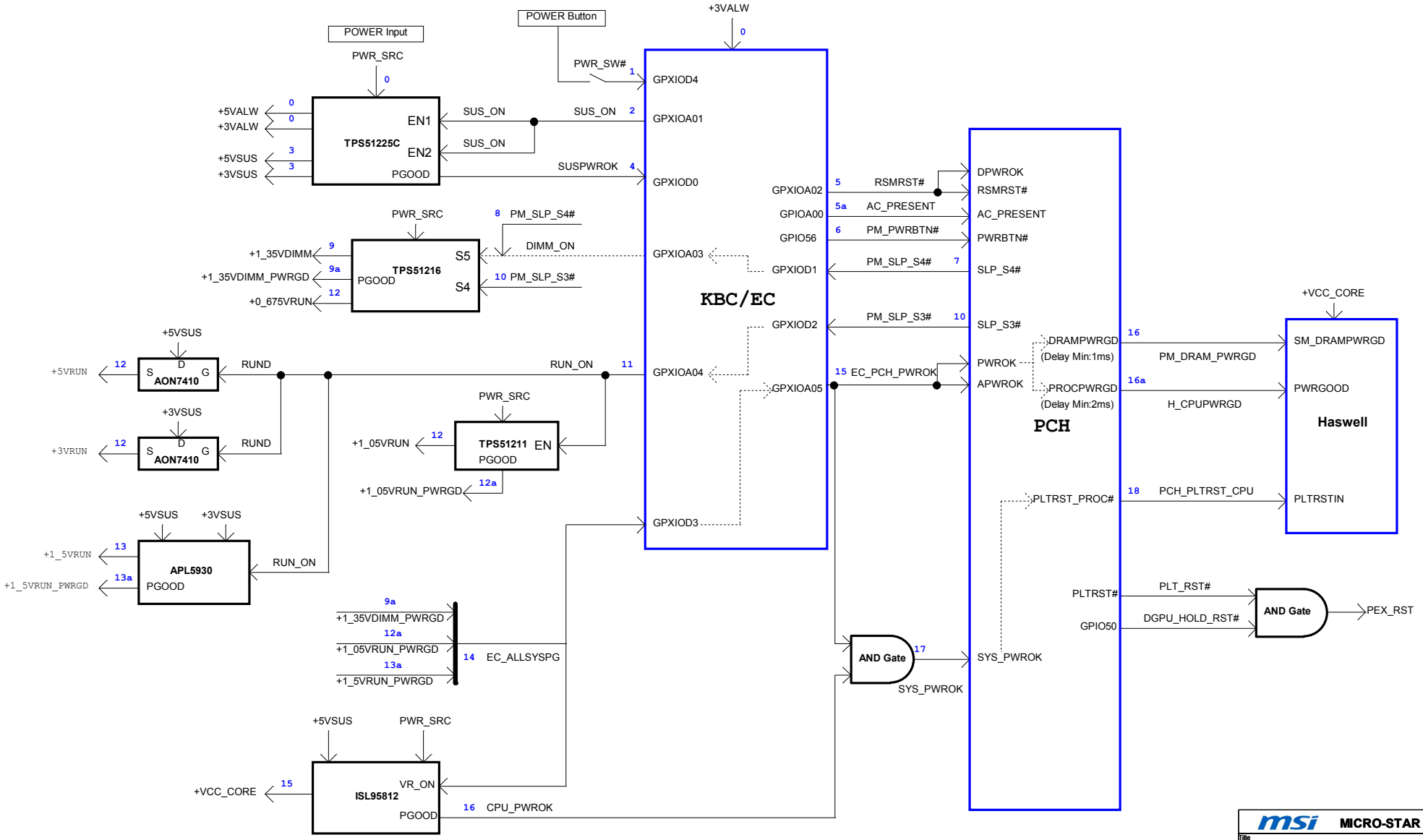
MS-16H5 Power on Block Diagram



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Title	Power on Block Diagram
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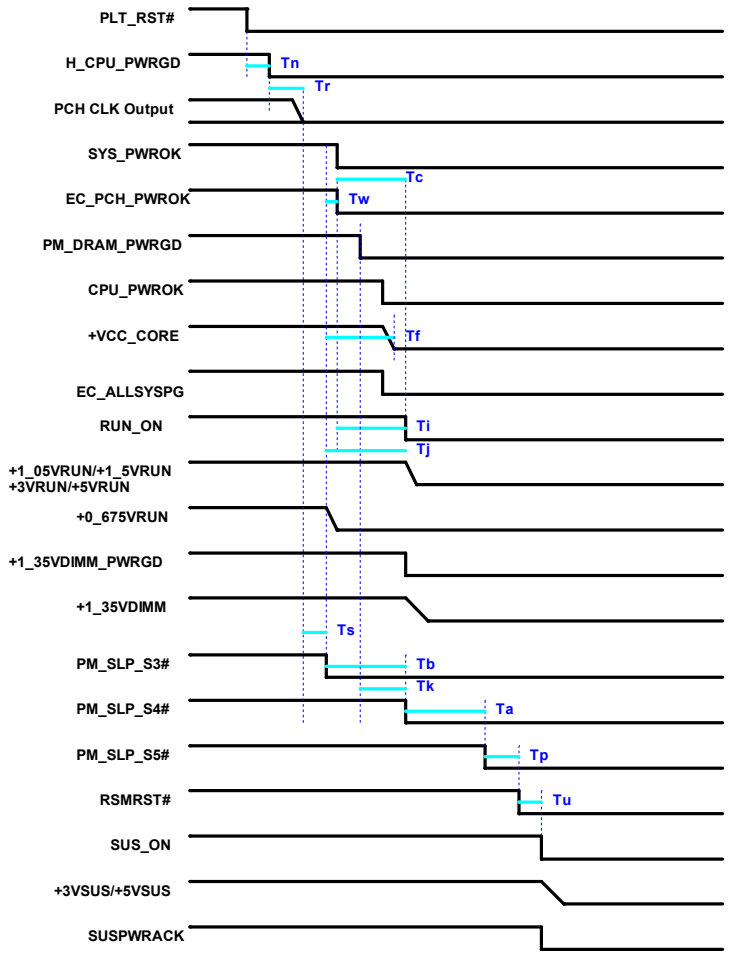
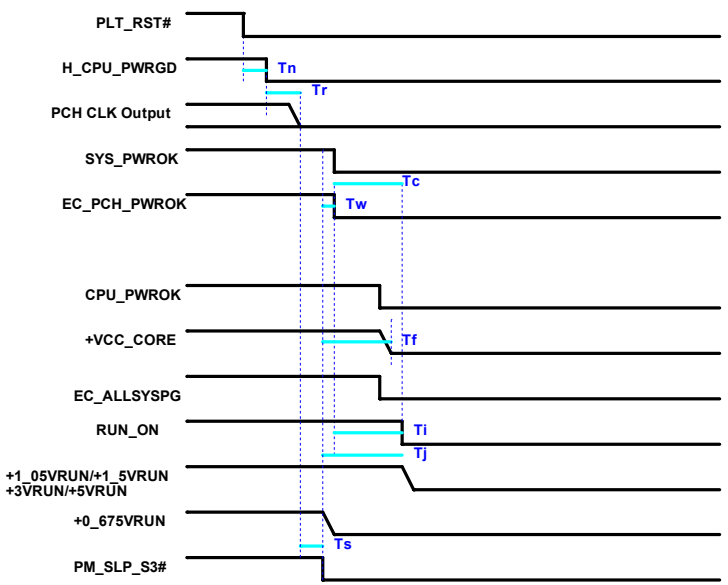
Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
Ta	30		us	SLP_S4# assertion to SLP_S5# assertion.
Tb	30		us	SLP_S3# assertion to SLP_S4# assertion.
Tc	40		ns	APWROK de-assertion to VCCASW/VCCSPI rails falling.
Tf		500	ms	SLP_S3# assertion to VCCIN(CPU) rail completely off.
Ti	40		ns	PWROK de-assertion to VCCCore (PCH) rail falling (-5% of nominal value).
Tj	5		us	SLP_S3# assertion to VCCCore (PCH) rails falling (-5% of nominal value).
Tk	-100		ns	DRAMPWROK de-assertion to SLP_S4# assertion
Tn	30		us	PLTRST# assertion to CPUPWRGOOD de-assertion.
Tp	500		us	Last SLP_Sx# or SLP_A# assertion to RSMRST# assertion
Tr	10		us	CPUPWRGOOD de-assertion to PCH clock outputs turning off.
Ts	1		us	PCH Clock outputs turning OFF to SLP_S3# assertion.
Tu	40		ns	RSMRST# assertion to VCCSUS rails falling (-5% of nominal value).
Tw	0		ms	SLP_S3# assertion to PWROK de-assertion.

S0 -> S3



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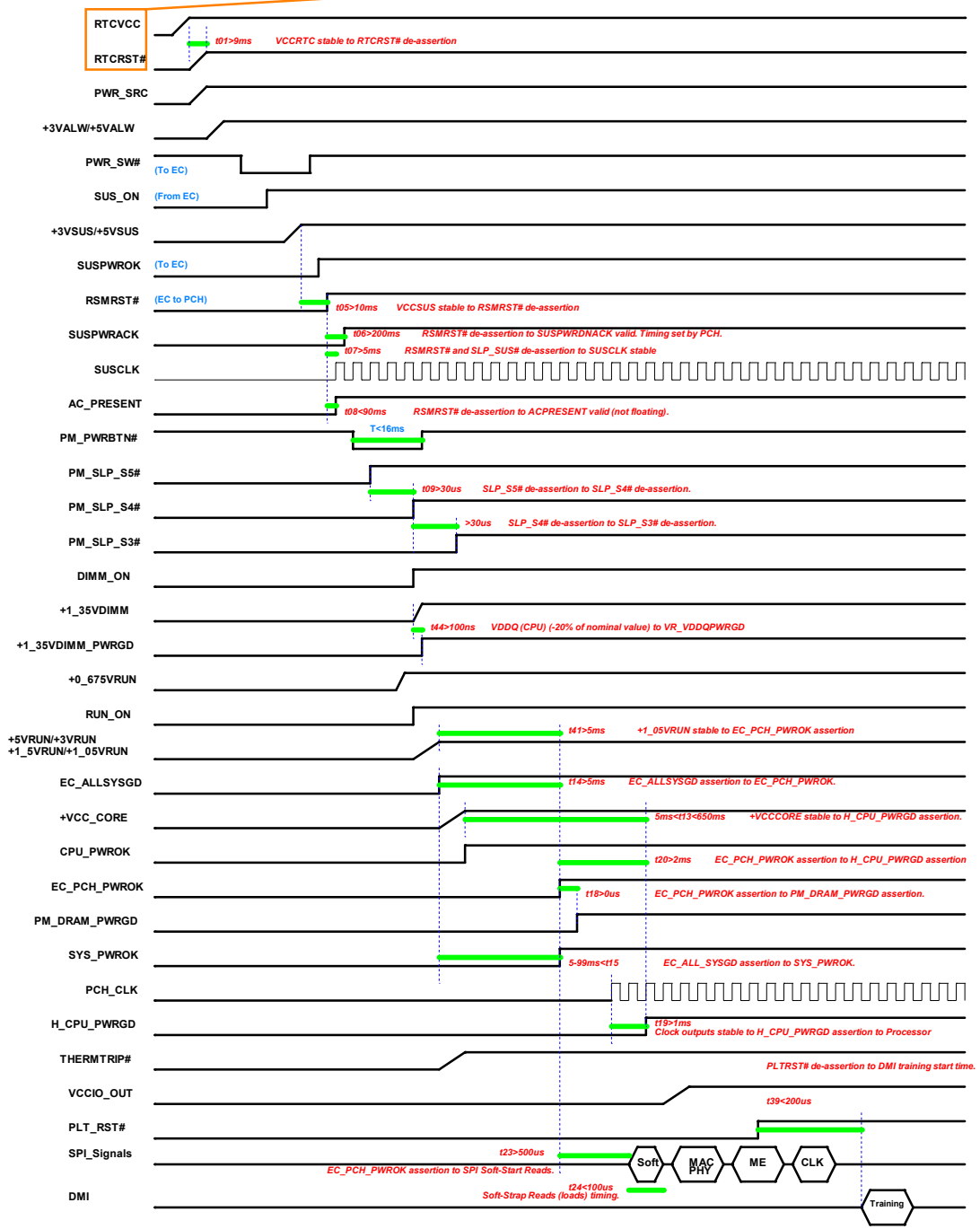
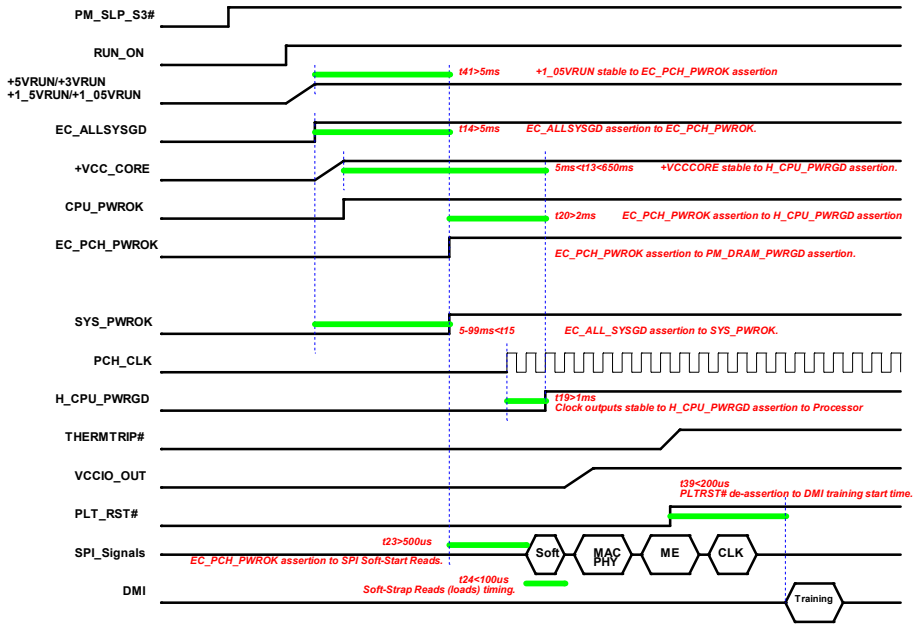
Power on Sequence

G3 -> S0



S3-> S0



msi	MICRO-STAR INT'L CO.,LTD.	
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History

1.1: 2014/7/3

01. P32 ADD R419 R418 R110
    ADD Q25 Q26
    ADD C709

02. P36 ADD R108 TO DGPU_PWR_EN#

03. P43 ADD R408 TO FPC15 PIN4
    ADD R409 TO FPC15 PIN5
    ADD R410 TO FPC15 PIN6
    ADD R411 TO FPC15 PIN7
    ADD R412 TO FPC15 PIN8
    ADD R413 TO FPC15 PIN9
    ADD R414 TO FPC15 PIN10
    ADD R415 TO FPC15 PIN11
    ADD R416 TO FPC15 PIN12

2014/7/8

01. P56 Remove JNC6

2014/7/10

01. P43 ADD C770 TO +5VSUS_KB

1.2: 2014/8/8

01. P25 ADD R420 TO G4 PIN AW18
    ADD C729 TO G4 PIN AW18
    DEL TPJNC28
    DEL TPJNC27
    DEL VIA_IFPAB_IOVDD
    DEL VIA_IFPEF_IOVDD
    DEL VIA_IFPC_IOVDD
    DEL VIA_IFPD_IOVDD

02. P31 ADD PR158 TO PQ25 PIN G1
    ADD PC148 TO PQ25 PIN G1
    ADD PQ51 TO PQ25 PIN G1
    ADD R111 TO PEX_VDD_R
    ADD PR98 TO DGPU_PWRGD
    PC52 Footprint N_R0603_NB TO Change F_C0402

03. P59 ADD R417 TO PU6 PIN1

2014/8/15

01. P25 ADD C713 TO G4 PIN AW18
    ADD C730 TO G4 PIN AW18

02. P47 Change D2 TO 3V_DP2_PWR

03. P60 ADD PR159 TO FBRTN_VGA

2014/8/15

01. P60 ADD PR160 TO FBRTN_VGA

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