V805-10
P682 DDR2
PCI-EXPRESSx16 DL-DVI VGA HDMI

07/30
01. Create V805-0A base on MS-V804-0A change to DDR2 Memory
02. DDR2 Memory schematic copy from MS-V202-0A
03. Reserve GPIO[5:6] NVVDD switch，NVVDD state = 0.9V(00)，1V(10)，1.0625V(11)
04. remove JTAG
05. remove HDCP ROM
06. remove FAN control，for 12V full speed
07. remove DAC EMI filter & ESD Diode & remove pi type left side cap
08. modify 5V circuit to TO-252 package
09. remove PWM NVVDD OCSET，Chage 10Kohm parallel low-side MOSFET VGS
10. remove R576 net IFP_PLLVDD change to 3V3
11. decrease caps
12. modify NVVDD & FBVDD PWM compensation value
13. MIOA_VDDQ net to GND，MIOA_CLKIN net to NC
14. del PEX_PLLVDD SUPPLY circuit
15. add NVVDD & FBVDD 12V input SMD choke overlap 0805 / 0 ohm
16. NVVDD & FBVDD 12V input DIP cap change to 3 pin
17. overlap NVVDD & FBVDD output choke

05/07

Page 01 1.Remove C690,C70 47uF
Page 10 1.Remove J1 D-Sub
Page 11 1.Remove R16,Q2
Page 12 1.Remove R1,Q1
Page 16 1.Change Crystal Footprint to 2-PIN SMD
2.Remove C71 47uF

05/08

Page 17 1.Remove Thermal Sensor Circuit
Page 18 1.Remove U2,C54,R31,R30,D16 INFOROM circuit
Page 19 1.Remove 3V3 to 1.8V circuit
2.Change 5V REGULATOR Circuit
Page 20 1.Change L8 Footprint to 1.6uH
2.Change Footprint to multi cap for EL 1500uF
Page 21 1.Change NVVDD to UP6161
2.Change L12 footprint to 1.2uH

05/10

Page 05 1. Remove Decoupling for EMI cap
Page 20 1. C84 change Footprint to multi cap

05/11

Page 21 1.Add C39 270uF
2.Add R922,R924 for APW7068 OCSET
Page 16 1.Add XTALIN R566 Risister
Add XTALOUT R573 Risister
Page 02 1.Change C51 to 0805 1UF and ADD C54 0805 1UF
Page 03 1.C642,C666,C633 change to .01UF
Page 05 1.Remove C516,C525,C549,C556,C541,C512
Remove C513,C546,C540,C528,C547,C507
Remove C544,C545,C520,C523,C532,C508
Remove C535,C526,C543,C553,C537,C88
Page 08 1.Remove C566,C567,C576,C578,C82,C564
Remove C619,C592,C586,C585,C622,C574
Remove C705,C706,C680,C729,C691,C683
Remove C742,C738,C731,C725,C743,C728
Page 20 1.Remove C86,C562,C563,C87

05/12

Page 17 1.Remove 4-PIN FAN Circuit
Page 12 1.Change Q509 to Q513,Q514 SOT23 footprint
Page 16 1.Change FAN Screw hole
Page 20 1.Add C102 820uF

05/14

Page 21 1.Remove D94 scottky diode

05/19

Page 11 1.Add EMI bridge
Page 12 2.Add EMI bridge

05/21

Page 03 1.Add RP24 termination risister
Page 06 2.Add RP23 termination risister

05/26

SWAP CMD
Page 03/06 RP5.1，RP5.2 FBC_CMD10，RP5.3，RP5.4 FBC_CMD22
RP4.1，RP4.2 FBC_CMD18，RP4.3，RP4.4 FBC_CMD7
RP24.1, RP24.2 FBA_CMD30, RP24.3, RP24.4 FBA_CMD7
RP20.1, RP20.2 FBA_CMD14, RP20.3, RP20.4 FBA_CMD18
RP14.1, RP14.2 FBA_CMD1, RP14.3, RP14.4 FBA_CMD20
RP12.3, RP12.4 FBA_CMD29

05/27

Page 05 1. Add Decoupling for EMI cap C80,C524,C517,C102

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10681-base-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0001	600-10681-0001-100	GT216-300 600/1500MHz 1024MB 64Mx16 BGA100 800MHz DDR3 DVI-I/VGA/HDMI
2	SKU0002	600-10681-0002-100.	GT216-300 600/1500MHz 1024MB 64Mx16 BGA100 1000MHz DDR3 DVI-I/VGA/HDMI
3	SKU0011	600-10681-0011-100	GT215-300 600/1500MHz 1024MB 64Mx16 BGA100 900MHz DDR3 DVI-I/VGA/HDMI
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P681-A01 OVERVIEW

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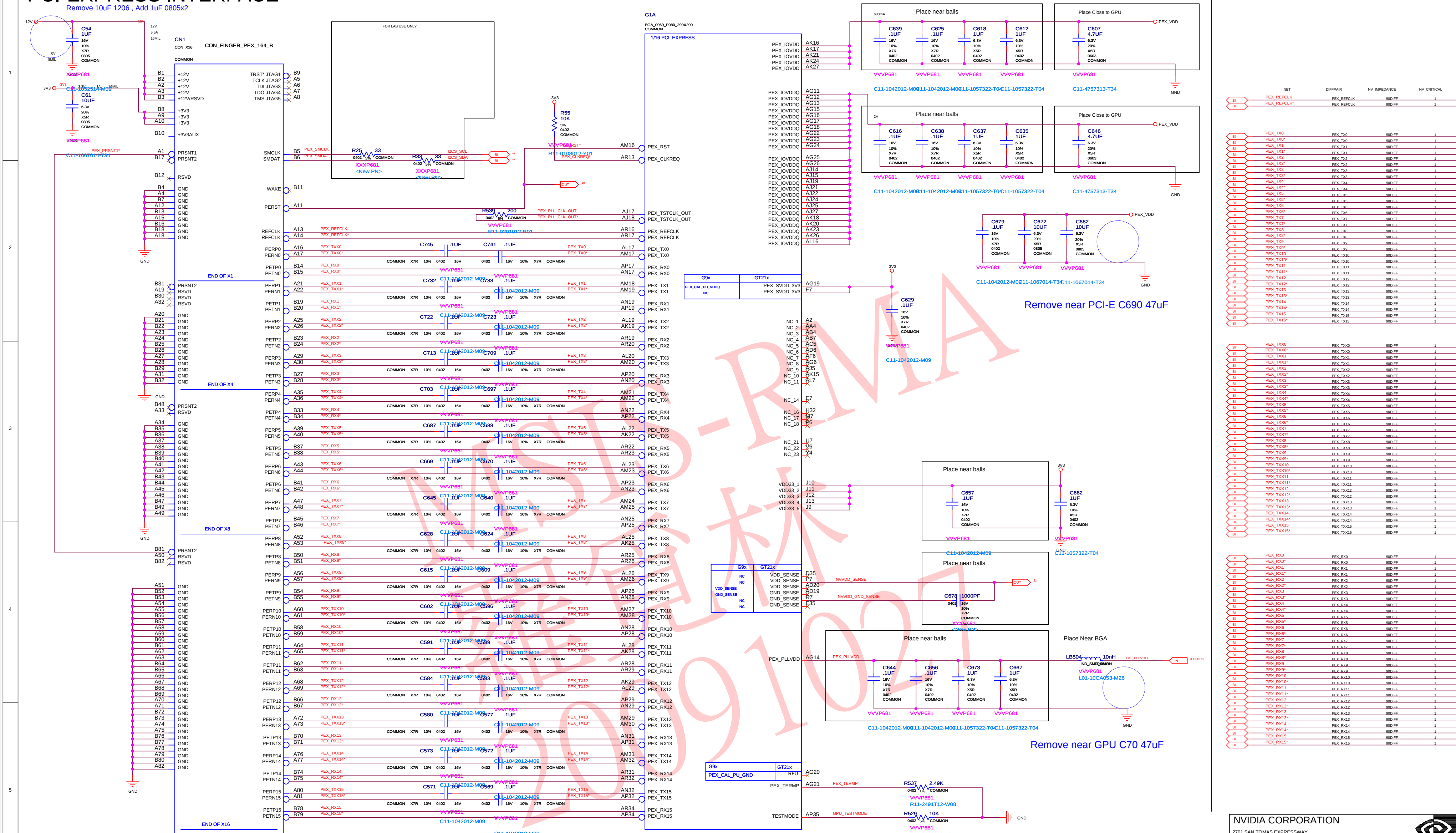
NV_PN	600-10681-base-100 A		
ID		PAGE	
NAME		DATE	05-FEB-2009

PCI-EXPRESS INTERFACE

Remove 10uF 1206 , Add 1uF 0805x2



ASSEMBLY
PAGE DETAIL PCI-EXPRESS INTERFACE

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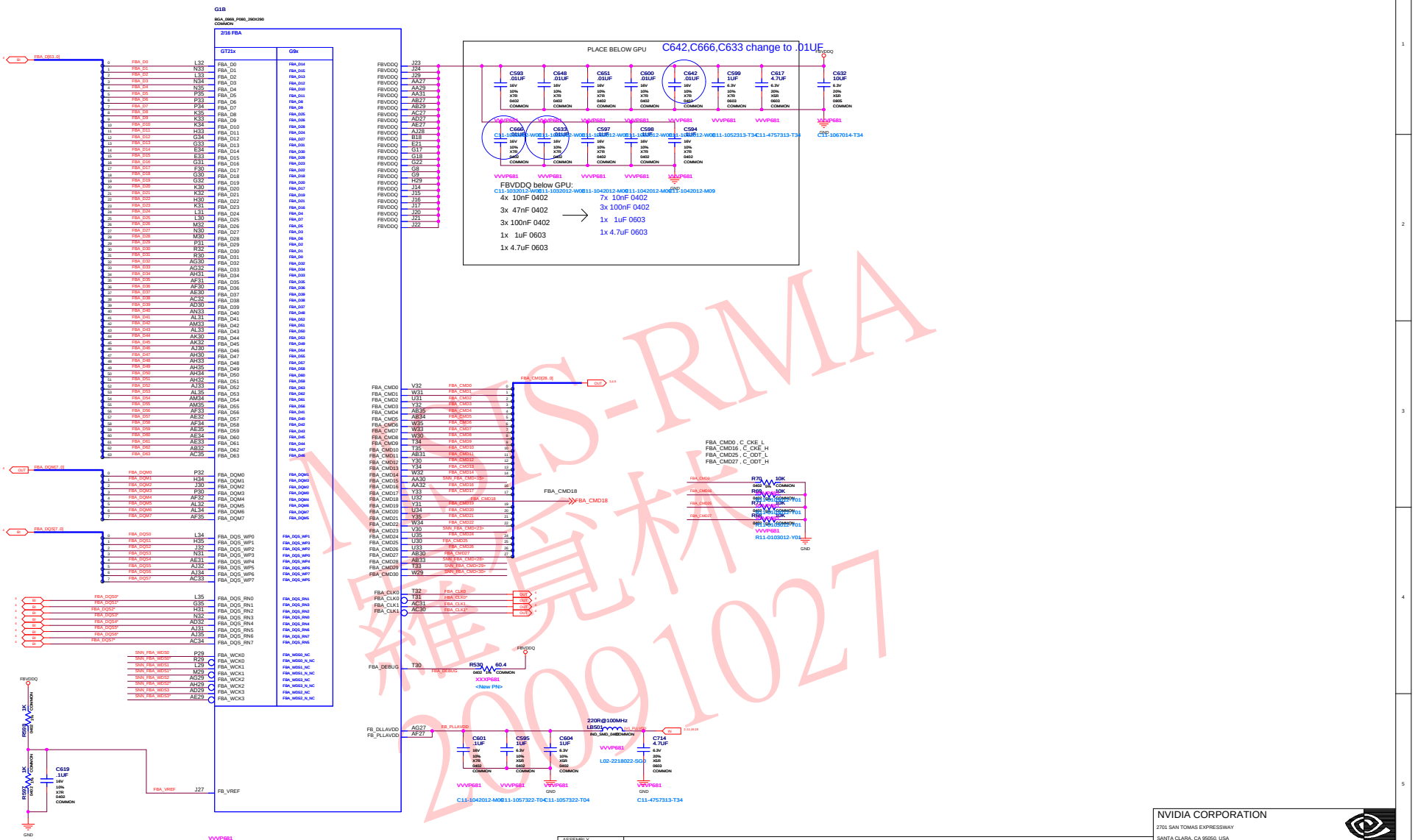
NV_PN 600-10681-base-100 A
ID
NAME
PAGE
DATE 05-FEB-2009

PARTITION A FRAME BUFFER INTERFACE



ASSEMBLY	
PAGE DETAIL	PARTITION A FRAME BUFFER INTERFACE

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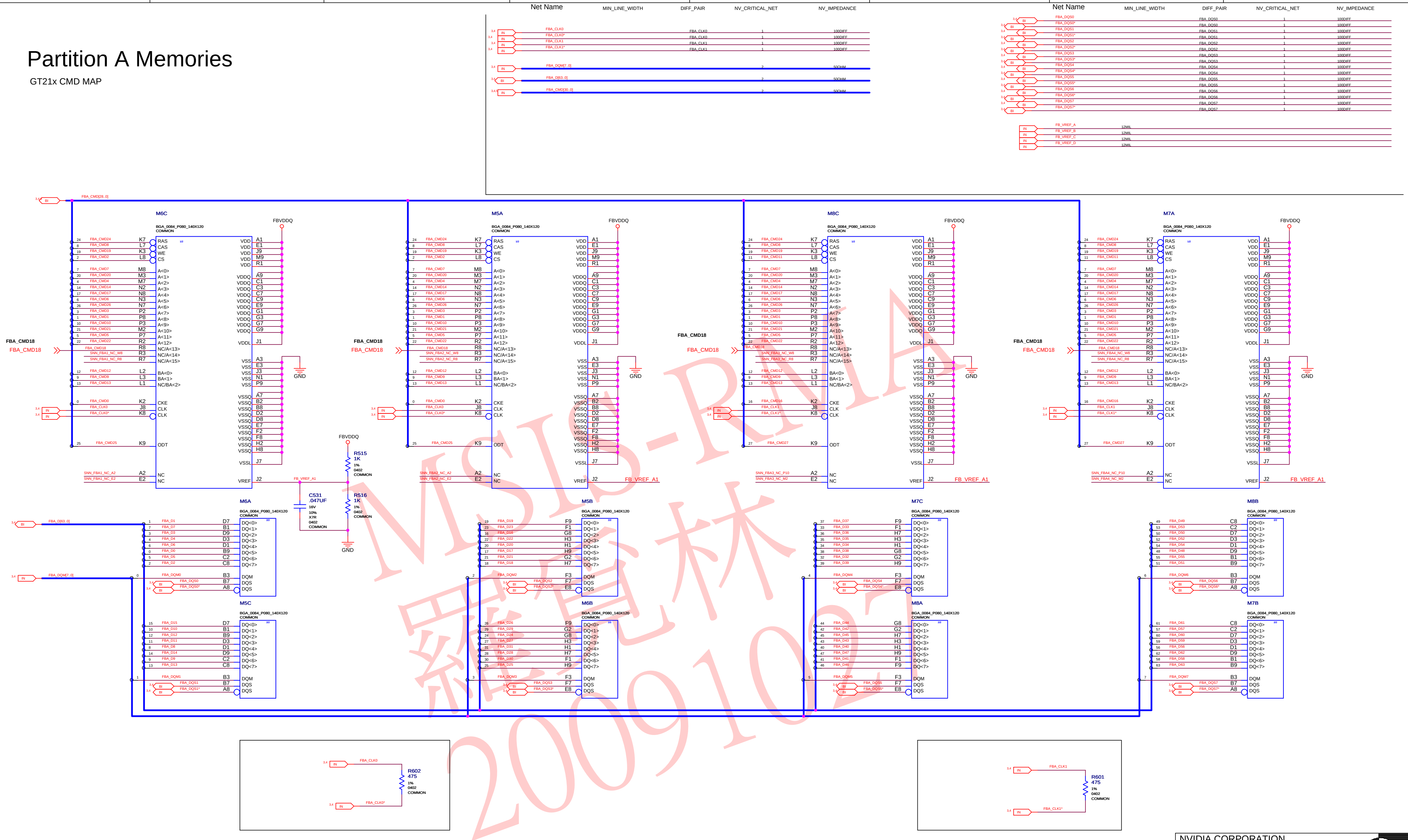
NV_PN	600-10681-base-100 A		
ID		PAGE	
NAME		DATE	05-FEB-2009

Partition A Memories

GT21x CMD MAP



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 16/32Mx32 GDDR3 MEMORIES, FBA COMMAND BUS PU'S, FBA CLK TERMS

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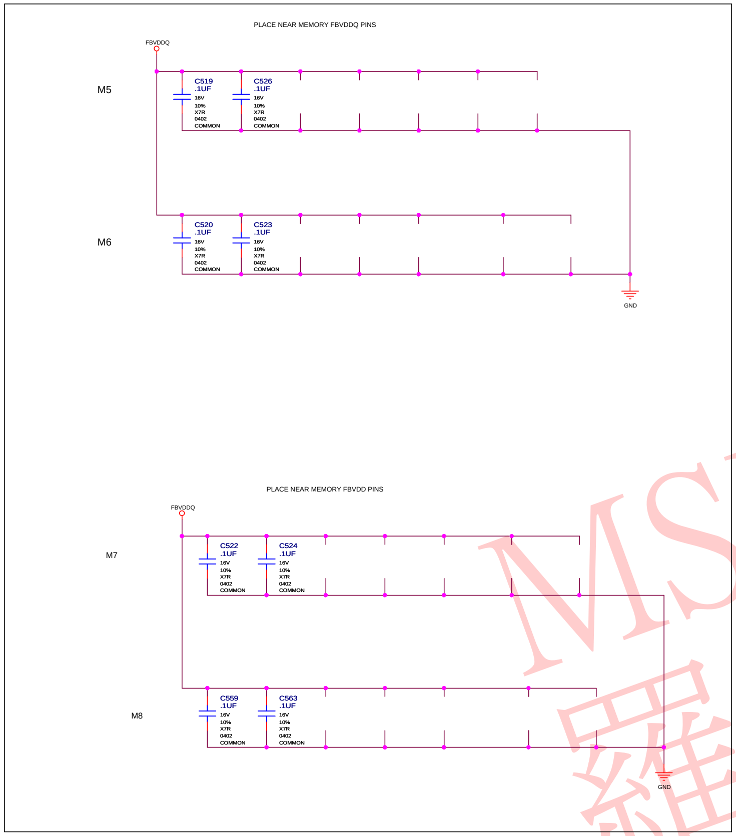
NV_PN	600-10682-base-100 A
ID	PAGE
NAME	DATE 15-MAY-2009

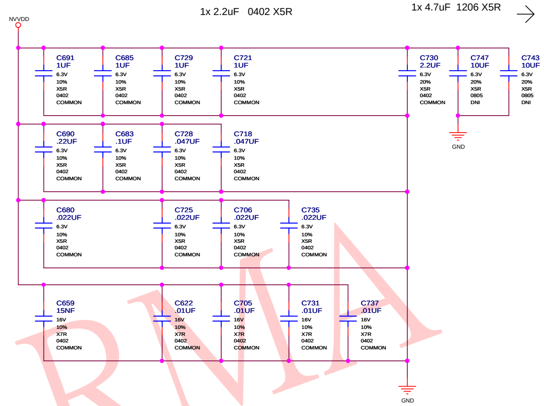
FBA DECOUPLING CAPS & NVVDD DECOUPLING CAPS

NVVDD under GPU:
4x 0.01uF 0402 X5R
1x 0.015uF 0402 X5R
5x 0.022pF 0402 X5R → 4 x 0.022pF 0402 X5R
2x 0.047uF 0402 X5R
1x 0.1uF 0402 X5R
1x 0.22uF 0402 X5R
4x 1.0uF 0402 X5R
1x 2.2uF 0402 X5R

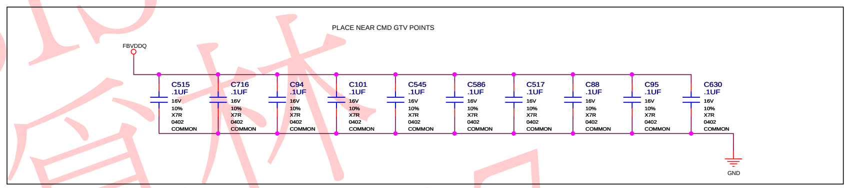
NVVDD near GPU:
3x 10uF 0805 X5R NO STUFF → 2 x 10uF 0805 X5R NO STUFF
1x 4.7uF 1206 X5R → 0 x 4.7uF 1206 X5R

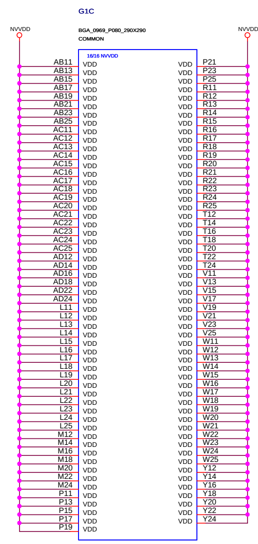
Decoupling for FBA





Return path coupling GND/FBVDDQ





VVVP681

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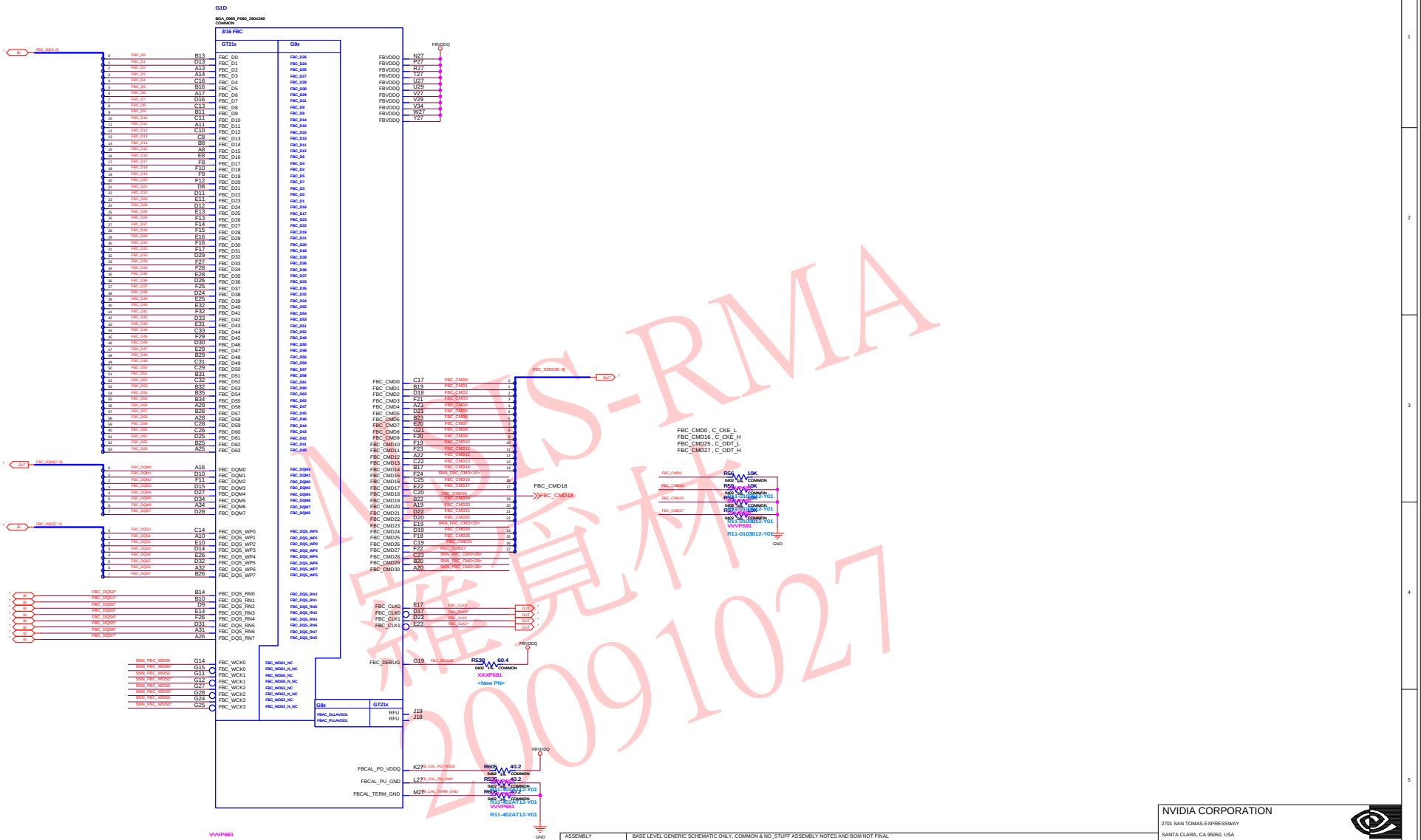
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA DECOUPLING CAPS & NVVDD DECOUPLING CAPS
NV_PN	600-10681-base-100 A
ID	PAGE
NAME	DATE 05-FEB-2009

PARTITION C FRAME BUFFER INTERFACE



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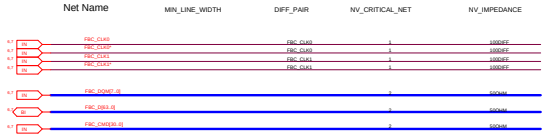
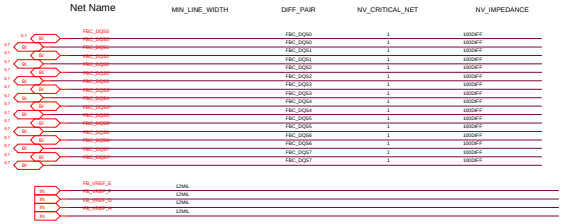
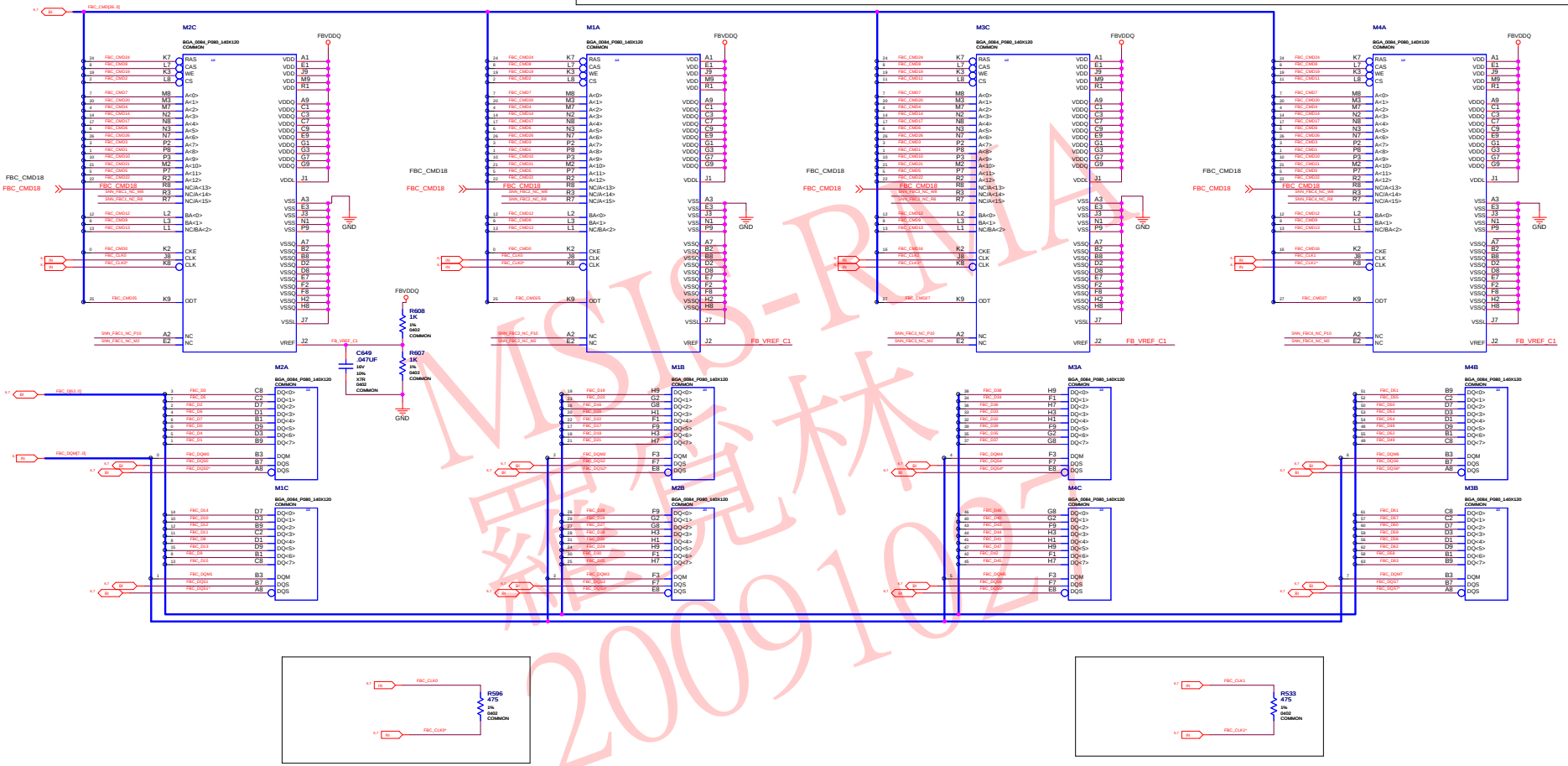
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PARTITION C FRAME BUFFER INTERFACE
NV_PN	600-10681-base-100 A
ID	
PAGE	
NAME	
DATE	05-FEB-2009

Partition C Memories

GT21x CMD MAP







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 16/32MX32 GDDR3 MEMORIES, FBC CMD BUS PU'S, FBC CLK TERMS

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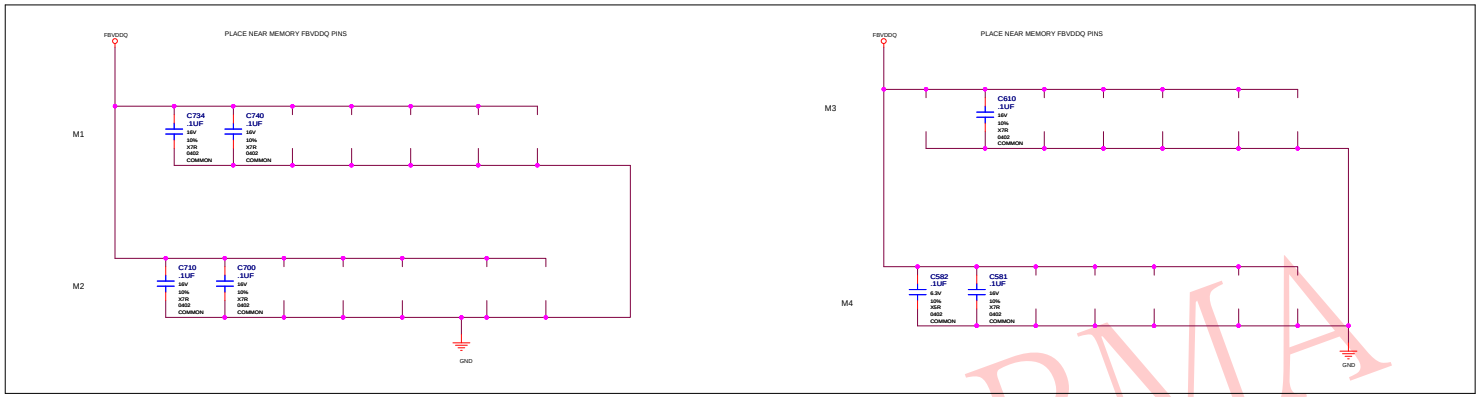
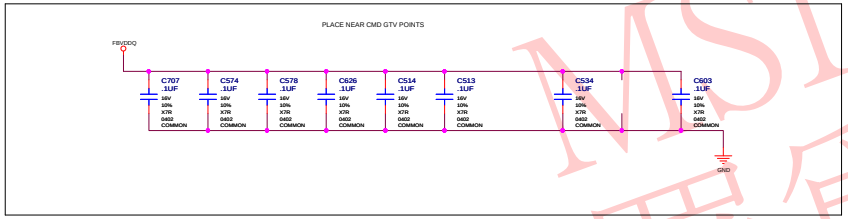
NV_PN	600-10682-base-100 A		
ID		PAGE	
NAME		DATE	15-MAY-2009

FBC DECOUPLING CAPS & NVVDD DECOUPLING CAPS

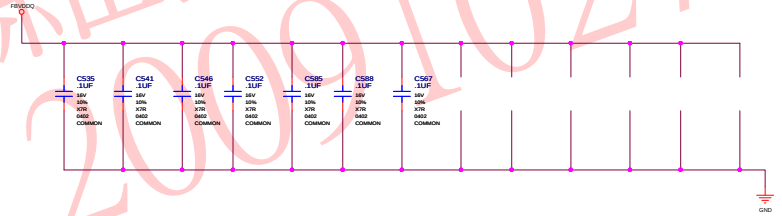
Decoupling for FBC

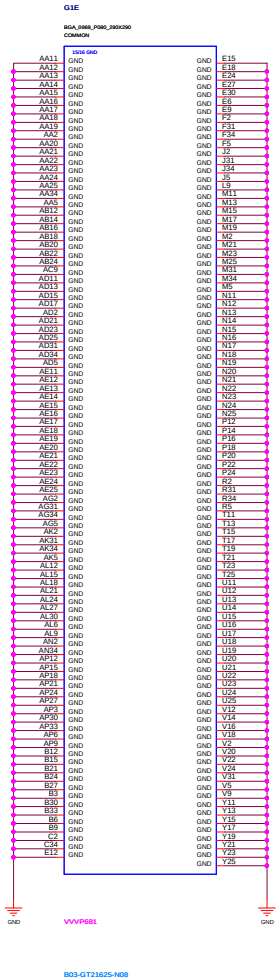


Return path coupling GND/FBVDDQ



Return path coupling GND/FBVDDQ for FBA/FBC





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC DECOUPLING CAPS

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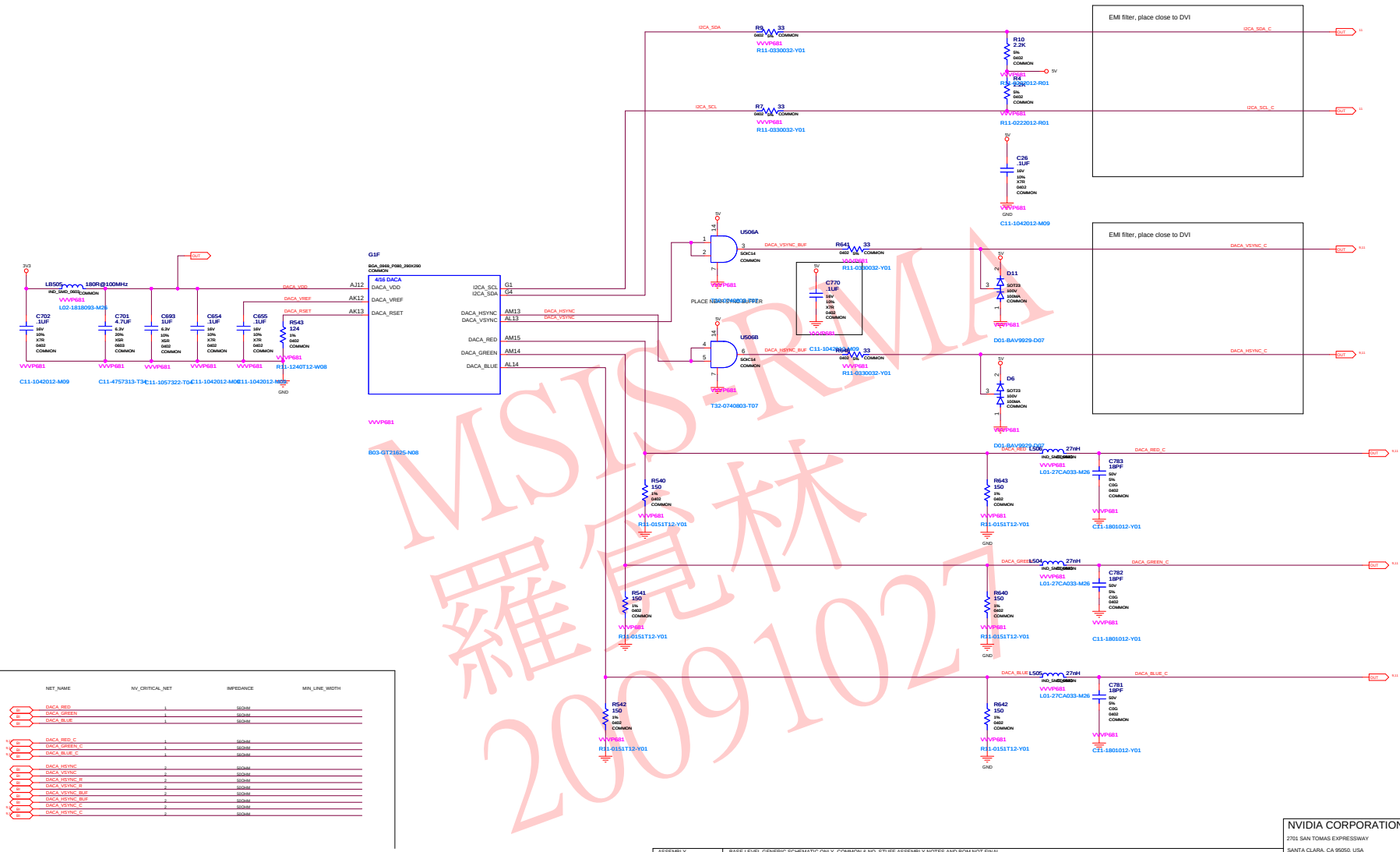
NV_PN	600-10681-base-100 A		
ID		PAGE	
NAME		DATE	05-FEB-2009

DACA (SOUTH DVI-I)



NET_NAME	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DACA_RED	1	50OHM	
DACA_GREEN	1	50OHM	
DACA_BLUE	1	50OHM	
DACA_RED_C	1	50OHM	
DACA_GREEN_C	1	50OHM	
DACA_BLUE_C	1	50OHM	
DACA_HSYNC	2	50OHM	
DACA_VSYNC	2	50OHM	
DACA_HSYNC_R	2	50OHM	
DACA_VSYNC_R	2	50OHM	
DACA_VSYNC_BUF	2	50OHM	
DACA_HSYNC_BUF	2	50OHM	
DACA_VSYNC_C	2	50OHM	
DACA_HSYNC_C	2	50OHM	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA (SOUTH DVI-I)

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NV_PN	600-10681-base-100 A		
ID		PAGE	
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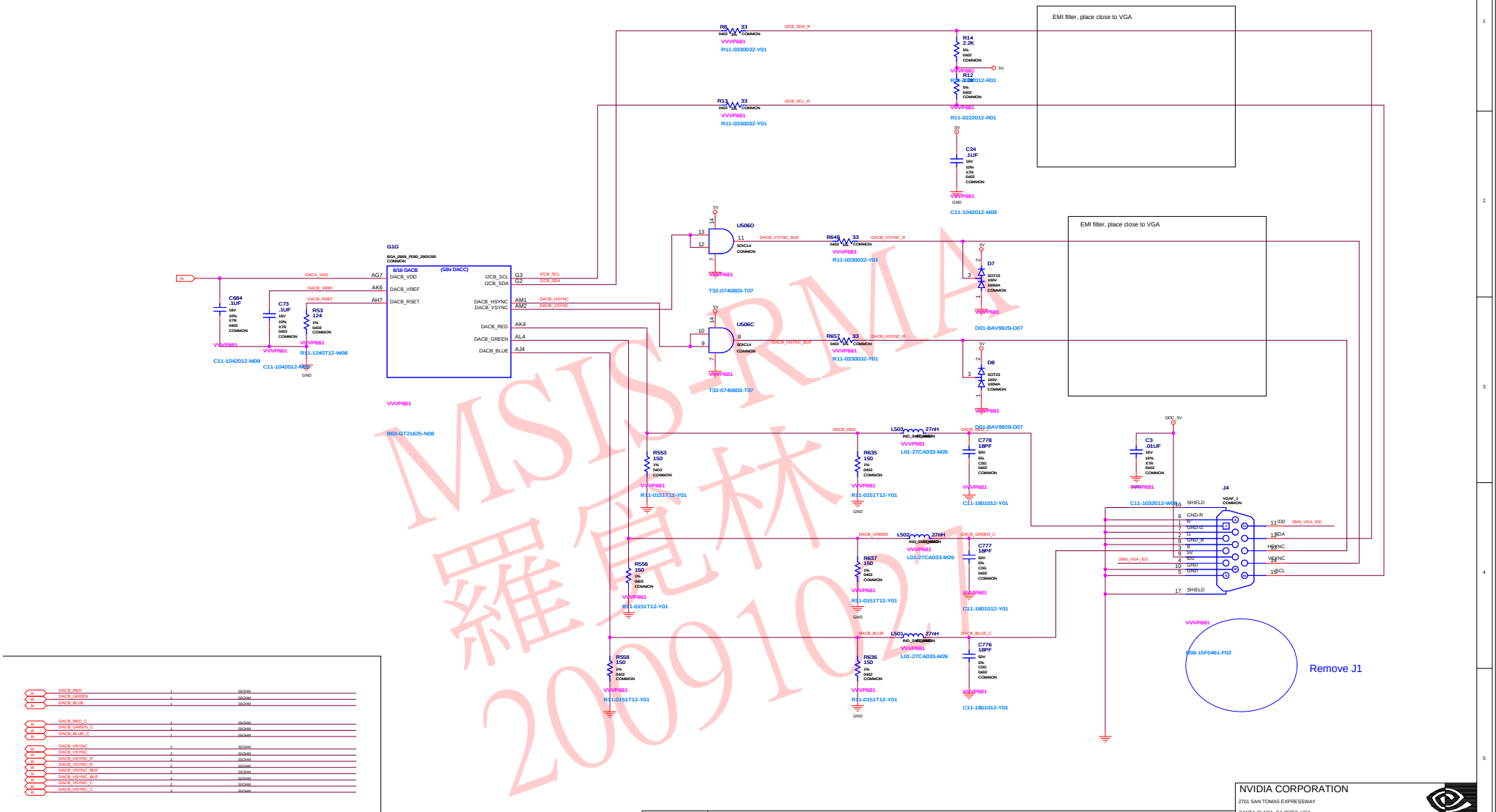
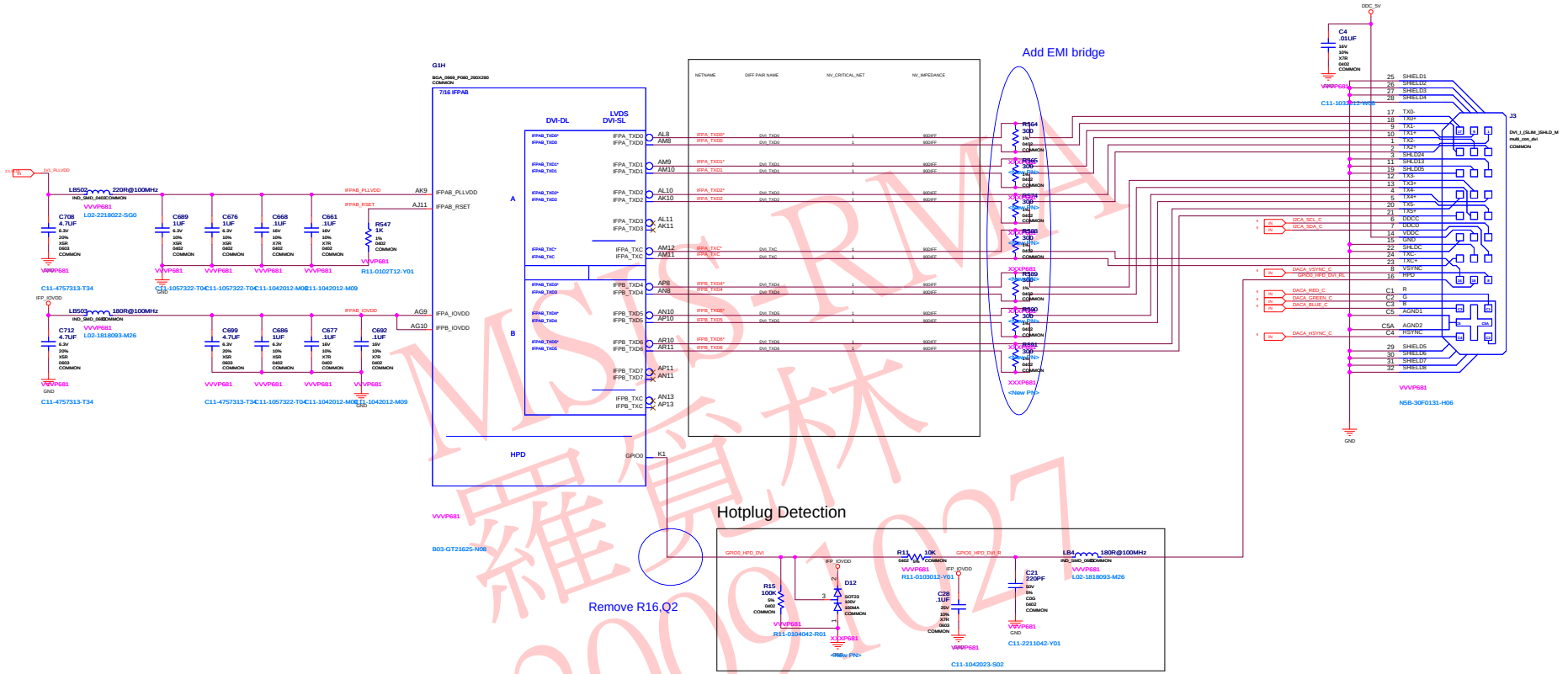
DACB (MID VGA)



IFP AB (SOUTH DVI-I)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP AB (SOUTH DVI-I)

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NV_PN	600-10681-base-100 A		
ID		PAGE	
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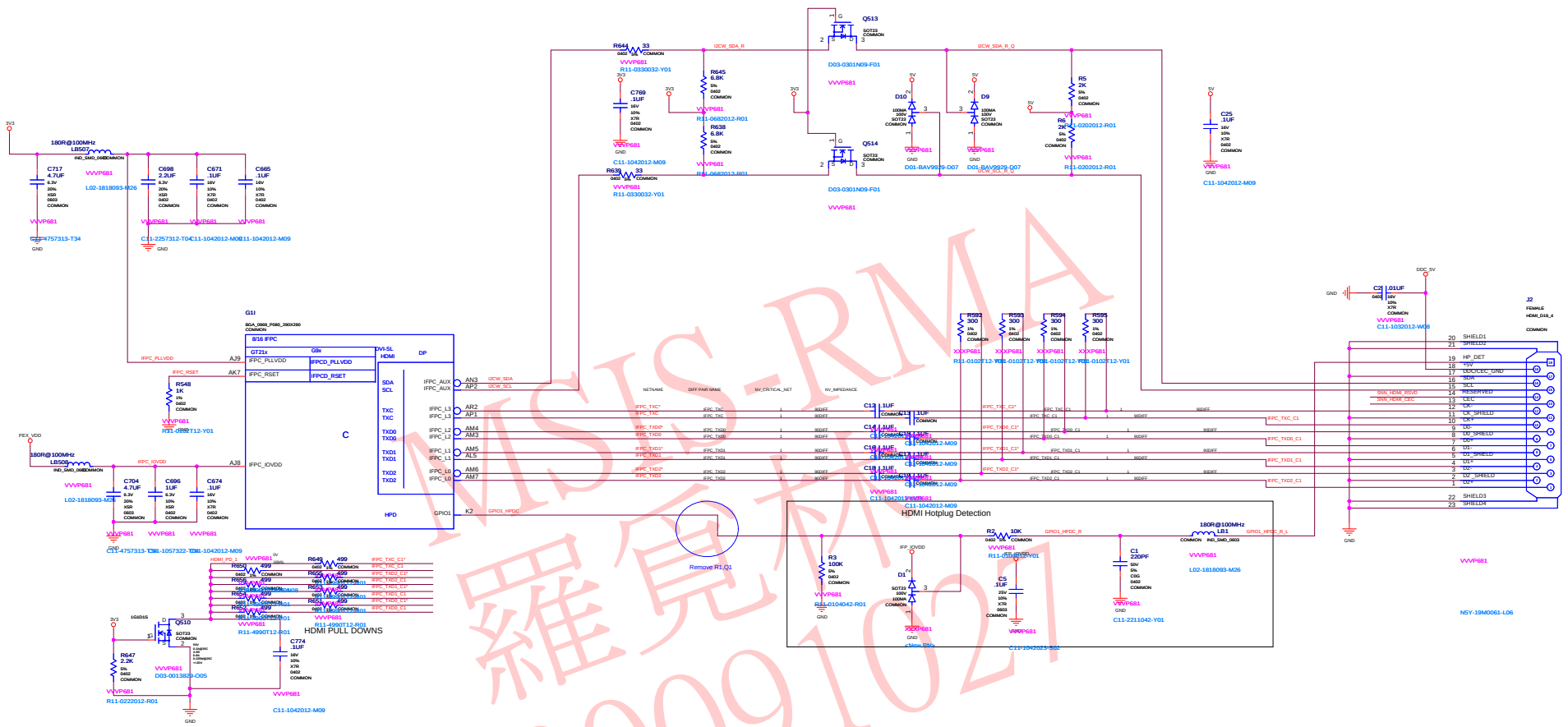
IFP C (NORTH HDMI)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP C (NORTH HDMI)

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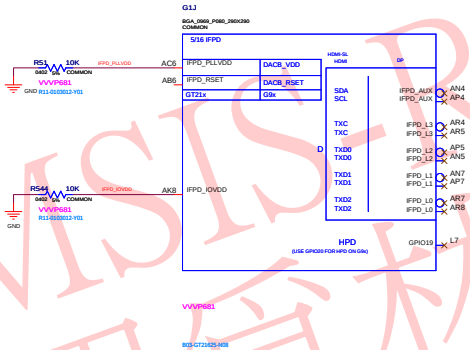
NV_PN	600-10681-base-100 A		
ID		PAGE	
NAME		DATE	05-FEB-2009

IFP D (UNUSED)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP D (UNUSED)

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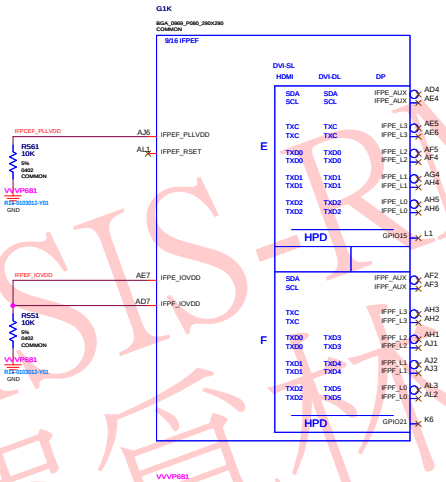
NV_PN	600-10681-base-100 A		
ID		PAGE	
NAME		DATE	05-FEB-2009

IFP EF (UNUSED)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP EF (UNUSED)

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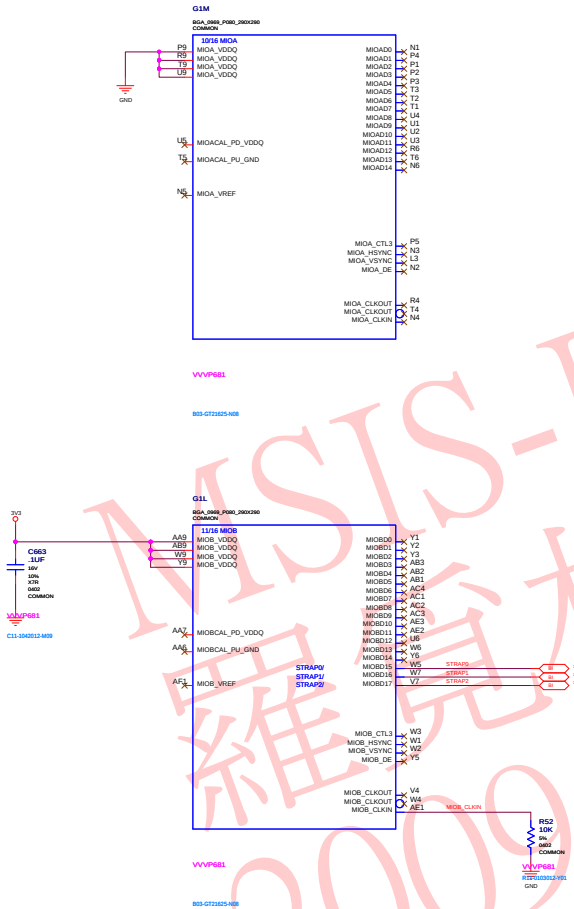
NV_PN	600-10681-base-100 A		
ID		PAGE	
NAME		DATE	05-FEB-2009

MIOA & MIOB



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIOA & MIOB

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NV_PN	600-10681-base-100 A		
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NAME		DATE	05-FEB-2009

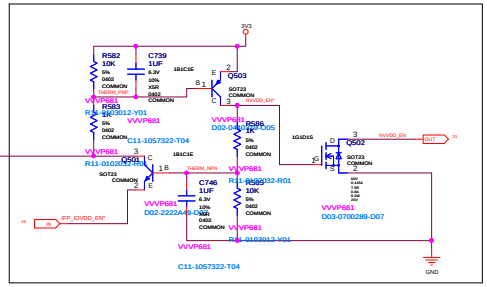
EXTERNAL THERMAL SENSOR, FAN CONTROL, GPIO, JTAG

THERMAL SENSOR

Remove U502,C730,R47,R566,C685 Thermal sensor circuit

I2C: 0x4CH

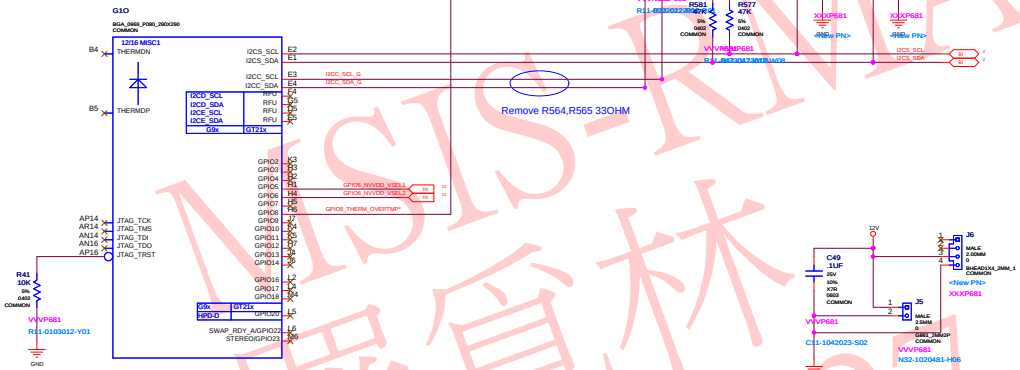
OVERTEMP LATCH

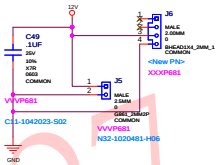


R46 1K

VVVP681

R11-0102032-R01





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	EXTERNAL THERMAL SENSOR, FAN CONTROL, GPIO, JTAG

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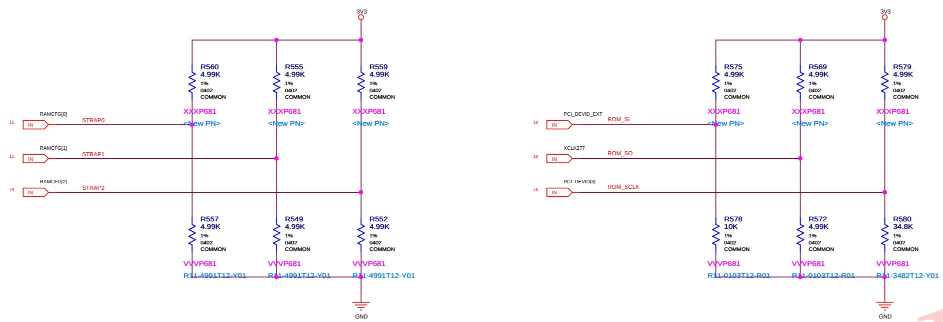
NV_PN	600-10681-base-100 A		
ID		PAGE	
NAME		DATE	05-FEB-2009

BIOS ROM, HDCP ROM, STRAPPING OPTIONS

STRAPPING OPTIONS



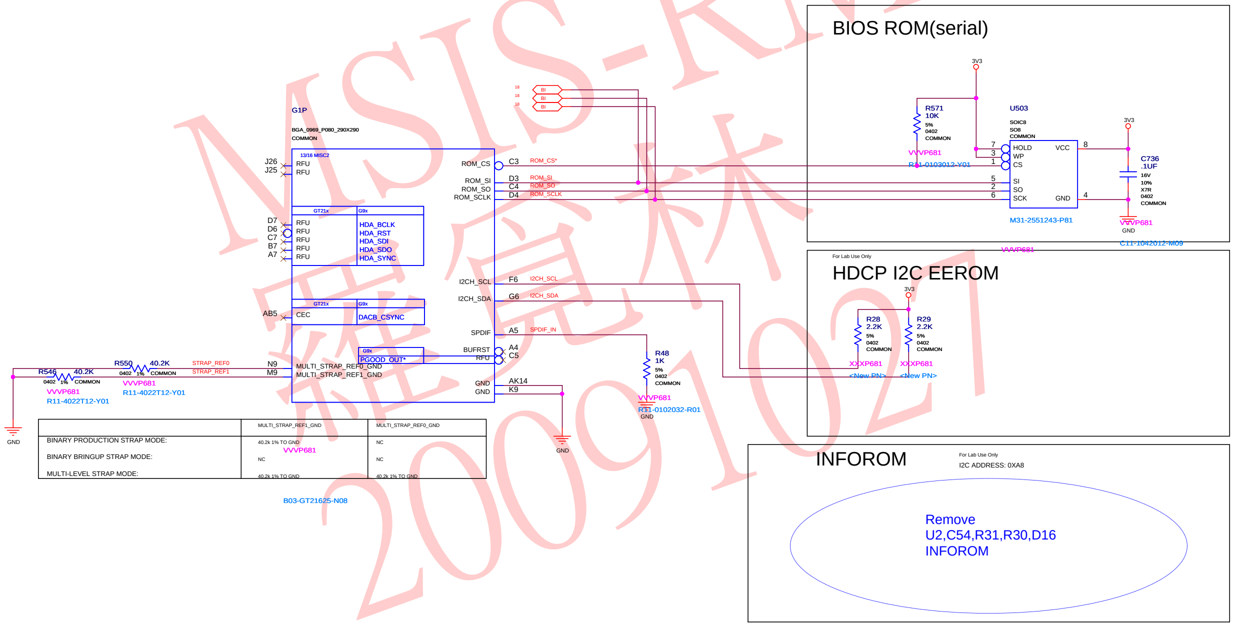
Strap0	USER[3:0]		EDID: 1111	45k PU
Strap1	3GIO_PADCFG[3:0]		DESKTOP: 0000	5k PD
Strap2	PCI_DEVID[3:0]		GT216-200: 0A21 0001	10k PD
ROM_SI	RAMCFG[3:0]	0001 128bit 64Mx16 DDR2 Samsung 0010 128bit 64Mx16 DDR2 Qimonda 0011 128bit 64Mx16 DDR2 Hynix 0101 128bit 32Mx16 DDR2 Samsung 0110 128bit 32Mx16 DDR2 Qimonda 0111 128bit 32Mx16 DDR2 Hynix	1001 64bit 64Mx16 DDR2 Samsung 1010 64bit 64Mx16 DDR2 Qimonda 1011 64bit 64Mx16 DDR2 Hynix 1101 64bit 32Mx16 DDR2 Samsung 1110 64bit 32Mx16 DDR2 Qimonda 1111 64bit 32Mx16 DDR2 Hynix	
ROM_SCLK	3: PCI_DEVID_EXT 2: SUB_VENDOR (1 = BIOS rom present) 1: SLOT_CLK_CFG (1 = common clk MCH/GPU) 0: PEX_PLL_EN_TERM (0 = disable pll term)		0110	35k PD
ROM_SO	3: XLK_417 (0 = POR 277MHz) 2: FB_0_BAR_SIZE (0 = POR 256MB) 1: SMB_ALT_ADDR (0=POR, 1= multiGPU) 0: VGA_DEVICE (0=3D device, 1=POR VGA device)		0001	5k PD

0 PD 5k		8 PU 5k
1 PD 10k		9 PU 10k
2 PD 15k		10 PU 15k
3 PD 20k		11 PU 20k
4 PD 25k		12 PU 25k
5 PD 30k		13 PU 30k
6 PD 35k		14 PU 35k
7 PD 45k		15 PU 45k

BIOS ROM(serial)

HDCP I2C EEROM

INFOROM



	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY PRODUCTION STRAP MODE:	40.2k 1% TO GND	NC
BINARY BRINGUP STRAP MODE:	NC	NC
MULTI-LEVEL STRAP MODE:	40.2k 1% TO GND	40.2k 1% TO GND

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BIOS ROM, HDCP ROM, STRAPPING OPTIONS

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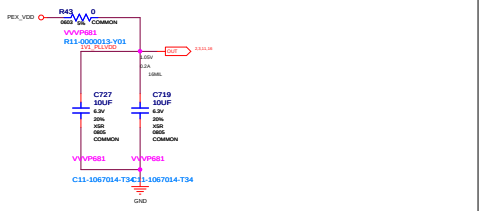
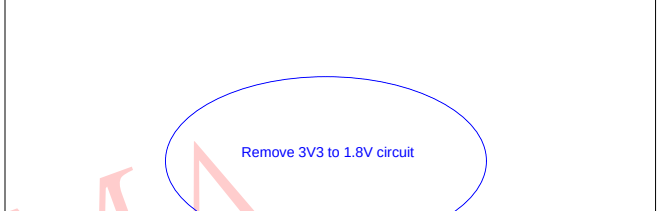
LINEAR POWER SUPPLIES

PEX_PLLVDD SUPPLY (OPTIAN)



VOUT = Vref * (1 + Rbot / Rtop)
1.053V = 0.8V * (1 + 1k / 3.16k)

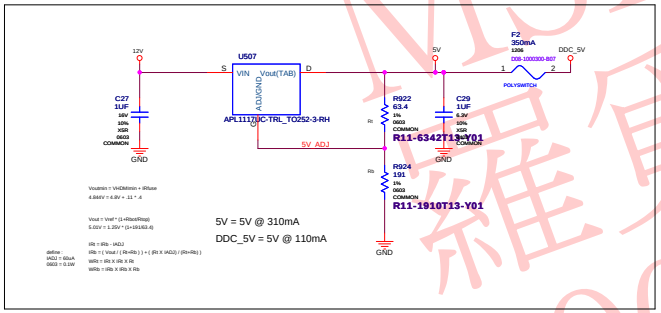
IFP_PLLVDD SUPPLY



VOUT = Vref * (1 + Rbot / Rtop)
1.793V = 0.8V * (1 + 1k / 0.808k)

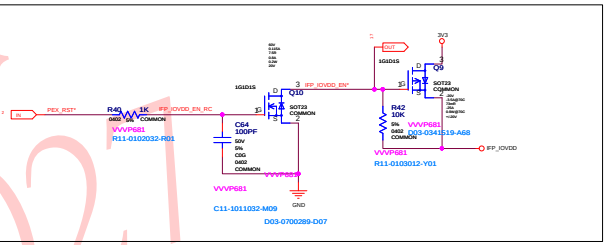
5V & DDC_5V REGULATOR

Change 5V REGULATOR Circuit



5V = 5V @ 310mA
DDC_5V = 5V @ 110mA

IFP_IOVDD BACKDRIVE PREVENTION



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LINEAR POWER SUPPLIES

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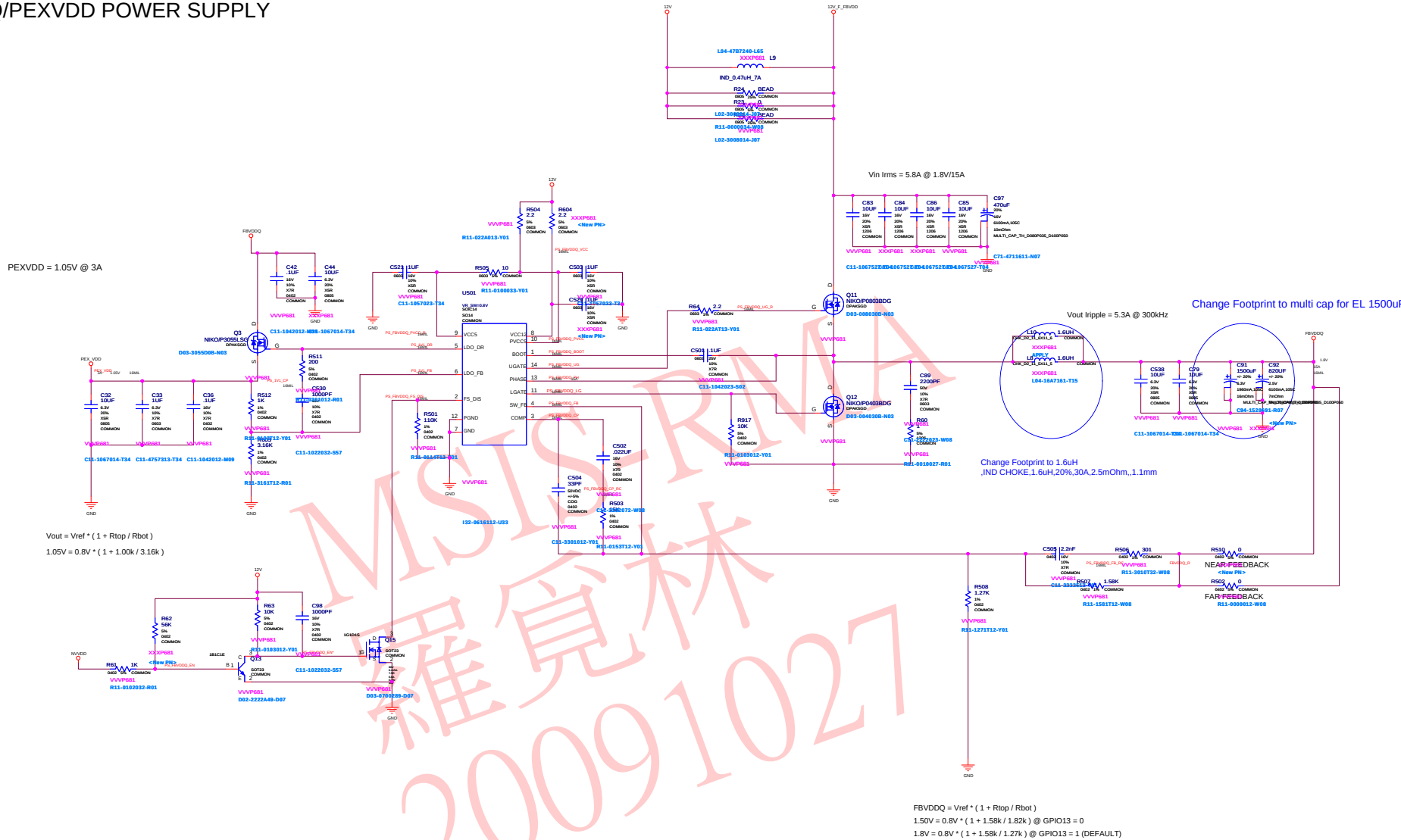
FBVDDQ/PEXVDD POWER SUPPLY



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBVDDQ/PEXVDD POWER SUPPLY

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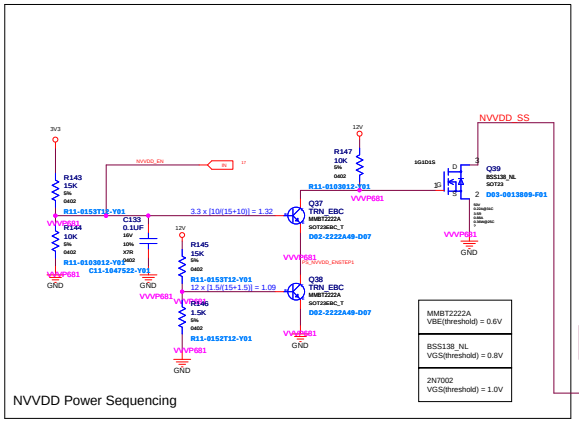
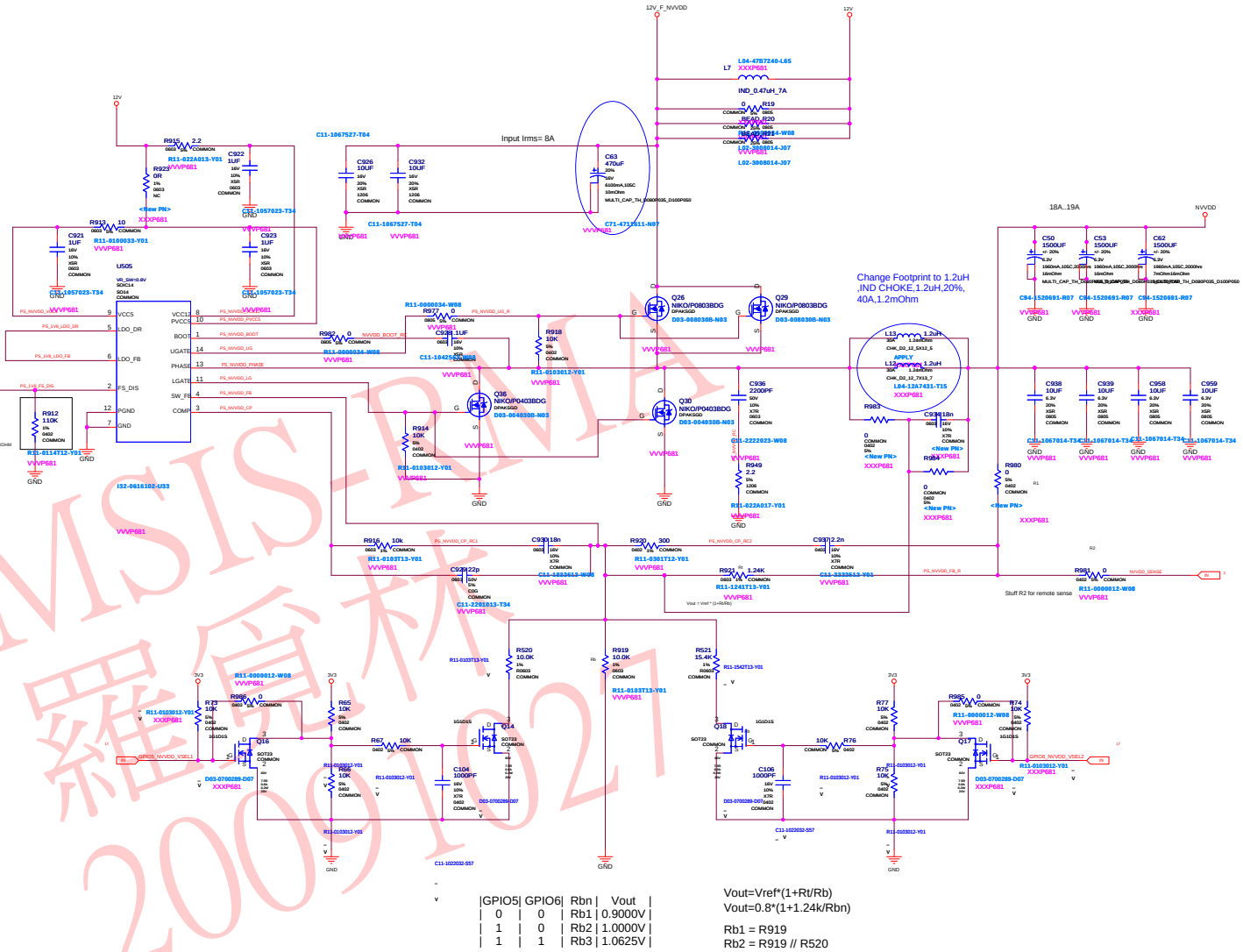
Power Supply III: NVVDD





GPIO5	GPIO6	Rbn	Vout
0	0	Rb1	0.9000V
1	0	Rb2	1.0000V
1	1	Rb3	1.0625V

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	NVVDD POWER SUPPLY

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XTAL, MECHANICALS, THERMALS