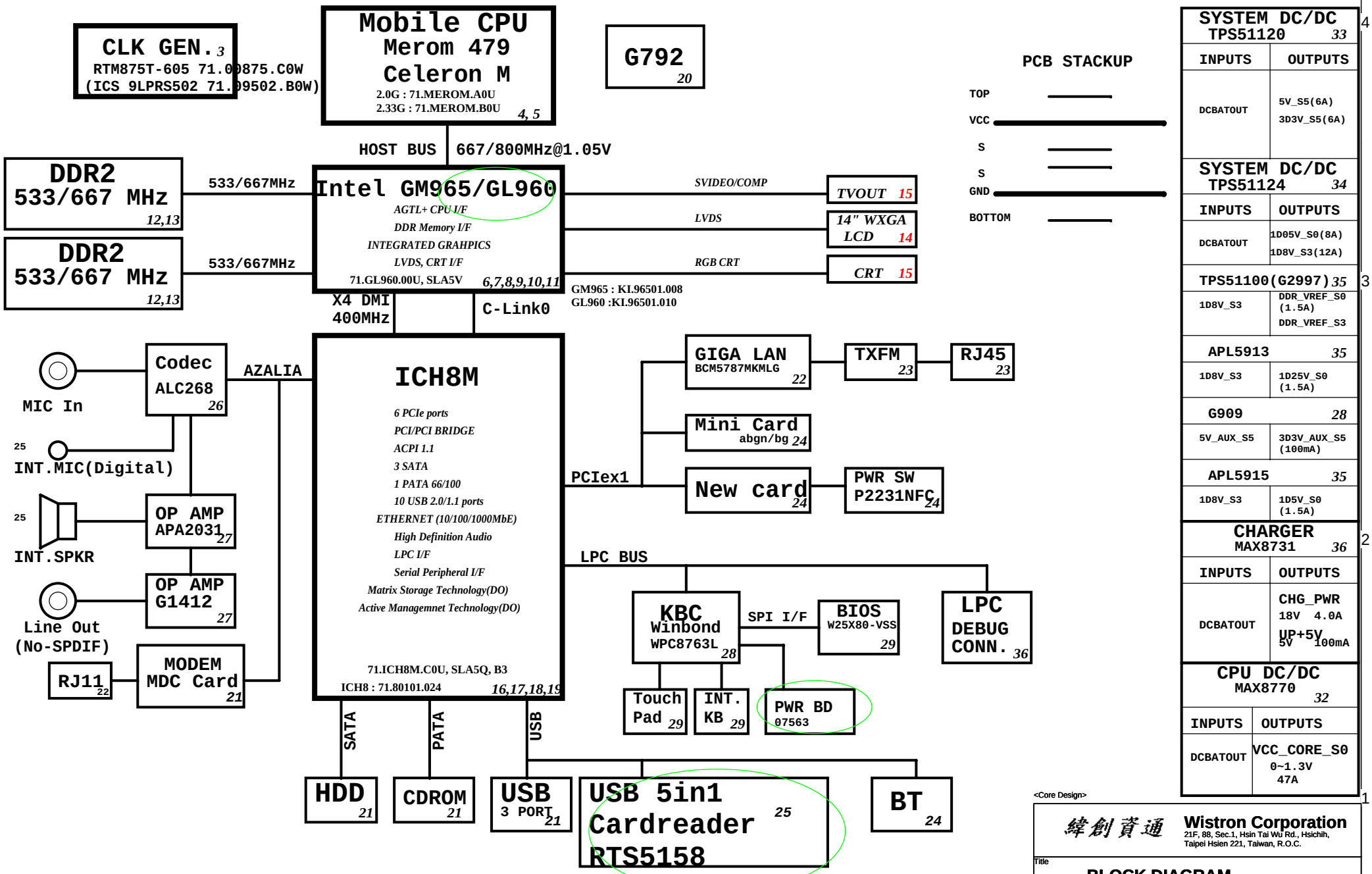
Calado Block Diagram

Project code: 91.4X401.001
PCB P/N : 07227
REVISION : -1



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51120 33

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC TPS51124 34

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(8A) 1D8V_S3(12A)

TPS51100(G2997) 35

1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL5913 35

1D8V_S3	1D25V_S0 (1.5A)

G909 28

5V_AUX_S5	3D3V_AUX_S5 (100mA)

APL5915 35

1D8V_S3	1D5V_S0 (1.5A)

CHARGER MAX8731 36

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC MAX8770 32

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

<Core Design>

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Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	Calado	-1

Date: Thursday, September 13, 2007 Sheet 1 of 39

ICH8M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K ?
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K ?
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode **1 = Low Power mode** (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

History

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

PCIE Routing

LANE1	LAN Marvell
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	NC
4	USB3
5	BT
6	Cardreader
7	MINICARD
8	CCD
9	NEW1

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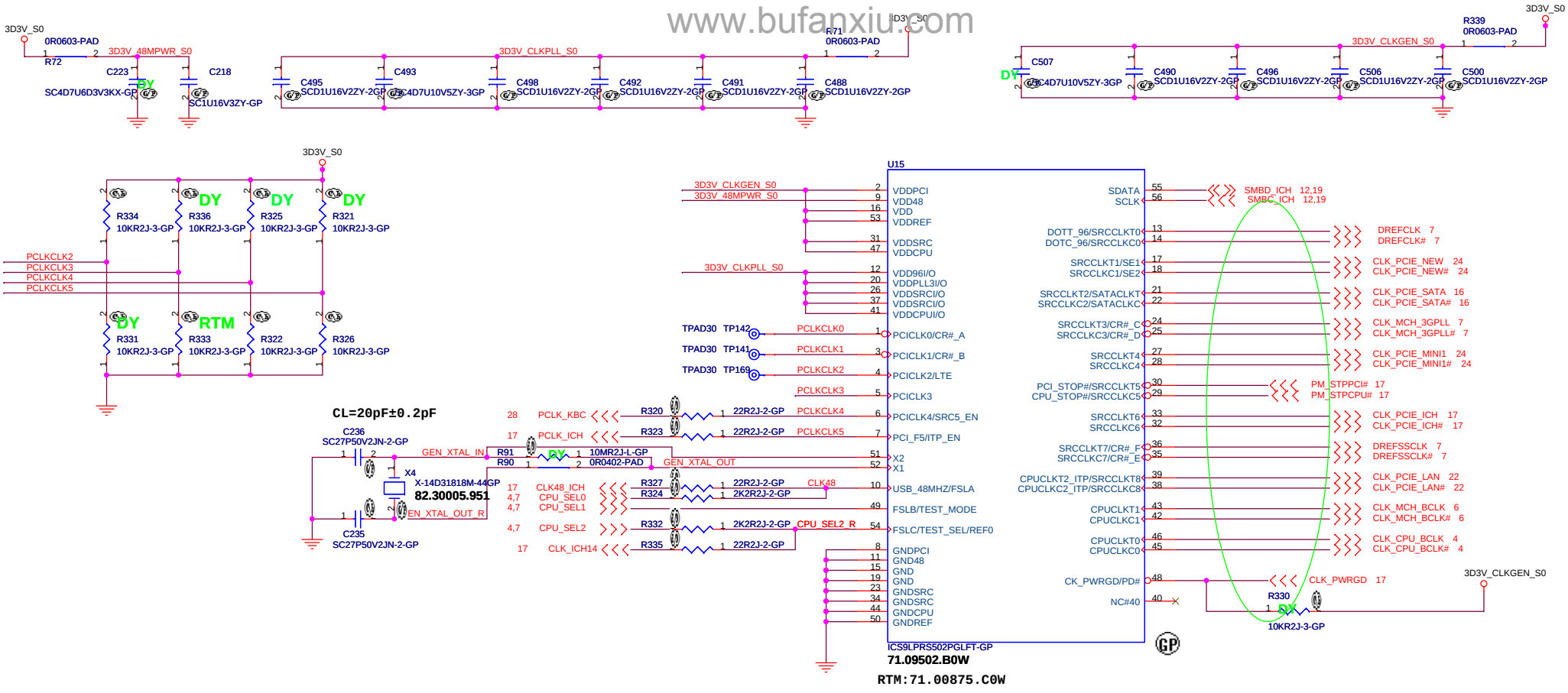
Title: Reference

Size: A3 | Document Number: Volvi2 | Rev: -1

Date: Monday, September 10, 2007 | Sheet 2 of 39



ICS9LPR502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

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Title: Clock Generator

Size	Document Number	Rev
	Calado	-1

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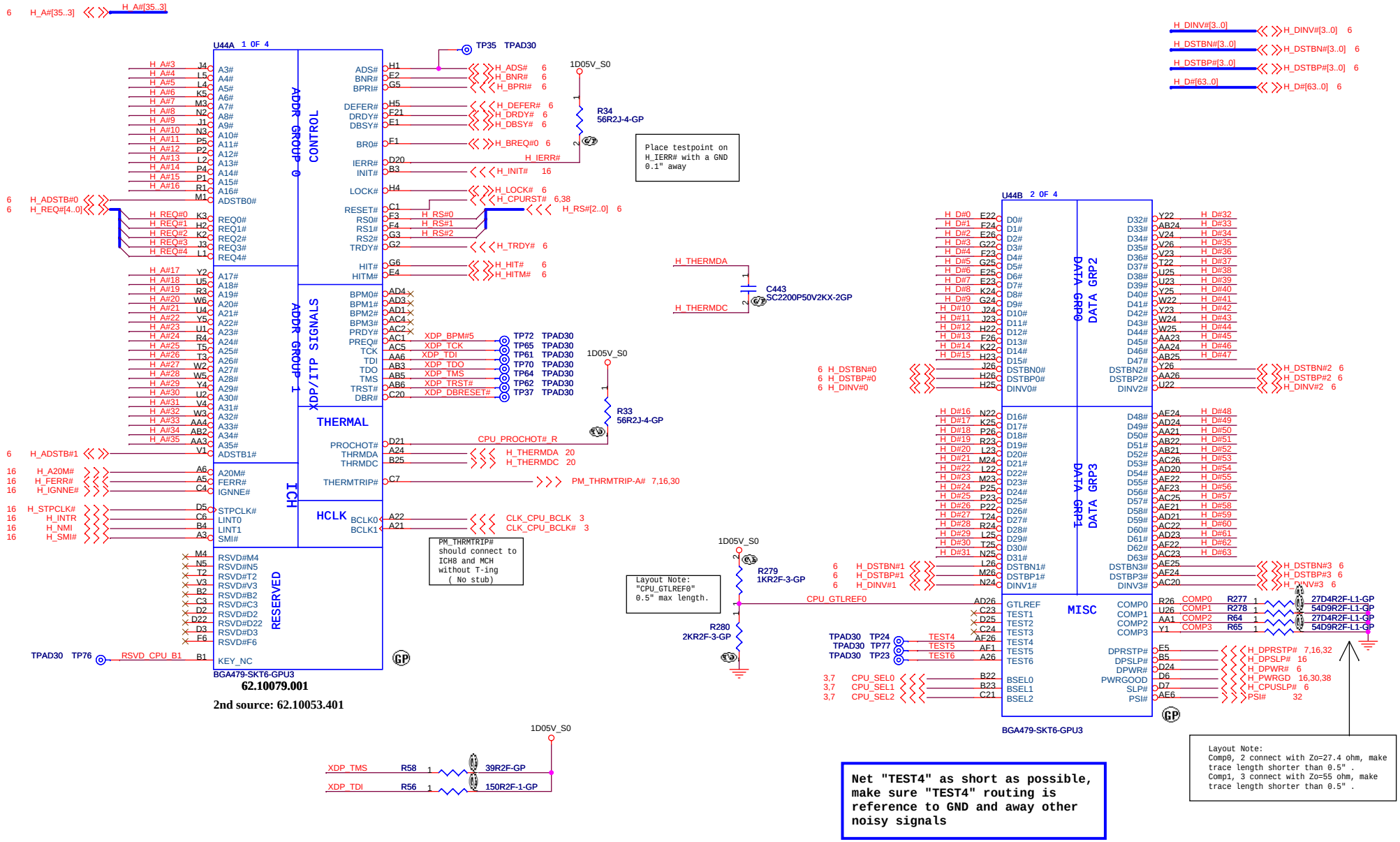

62.10079.001

2nd source: 62.10053.401

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Title: CPU (1 of 2)

Size | Document Number: Calado | Rev: -1

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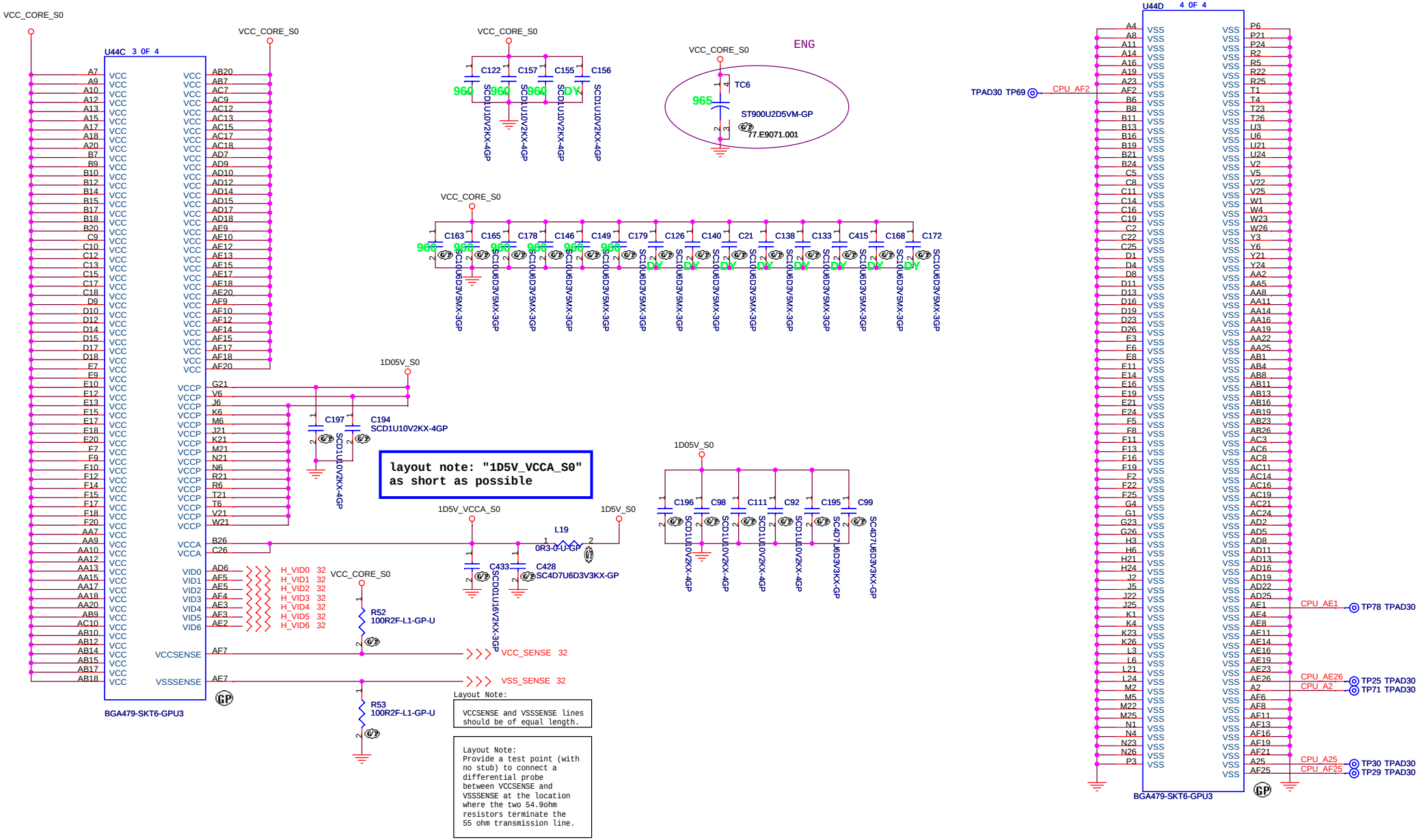

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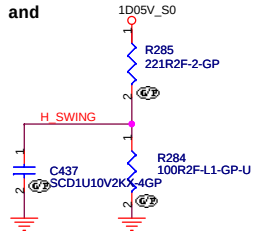
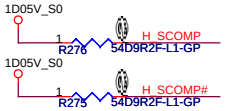
Title	**CPU (2 of 2)**	
Size	Document Number **Calado**	Rev -1
Date: Wednesday, September 12, 2007	Sheet 5 of 39	

H_SWING routing Trace width and Spacing use 10 / 20 mil

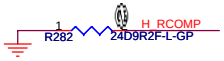
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)

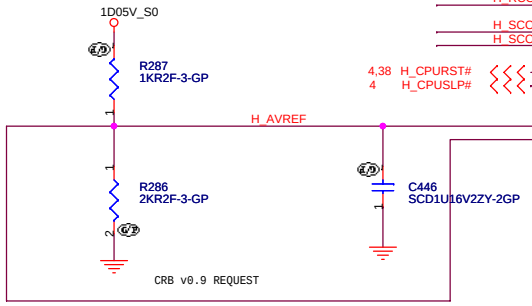


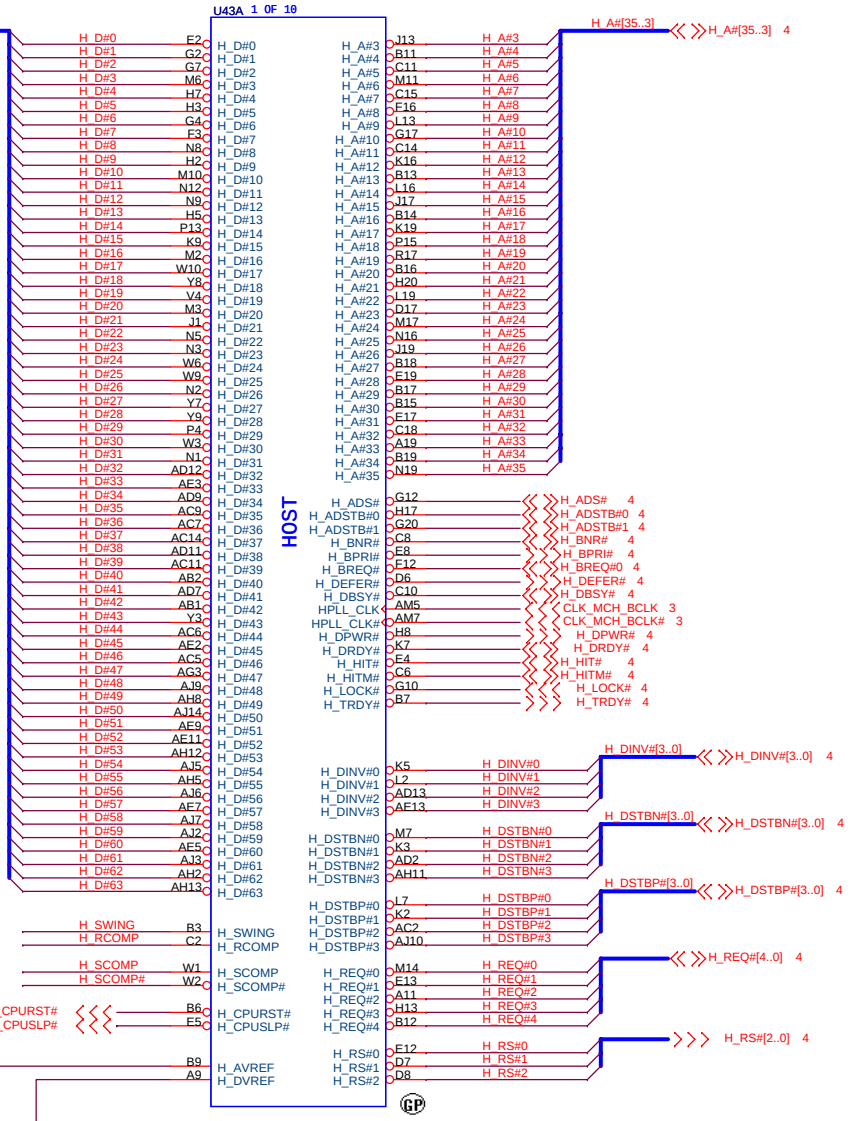
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

H_REF Decoupling Crestline close Crestline 100 mil





<Core Design>

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Title	**GMCH (1 of 6)**
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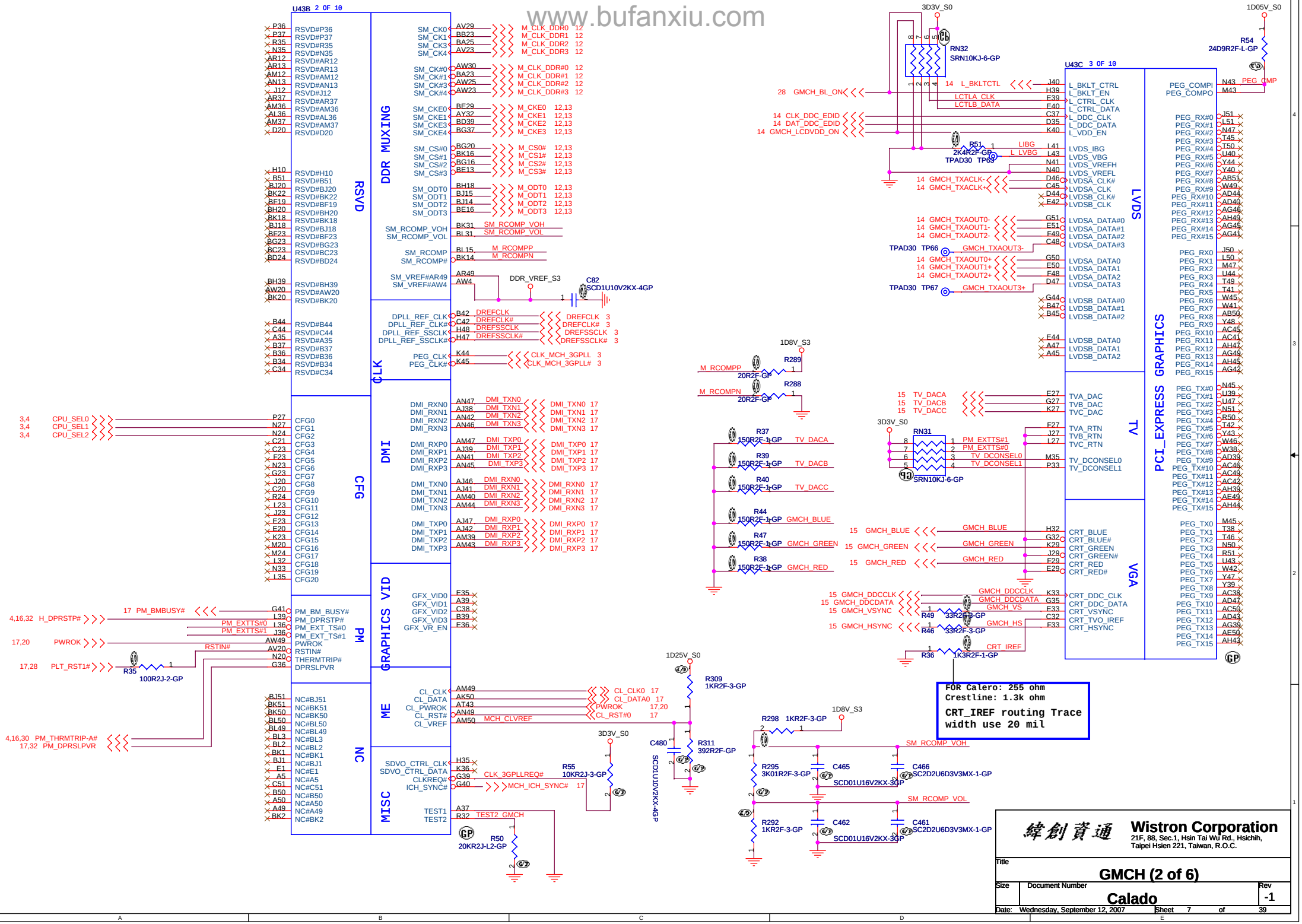

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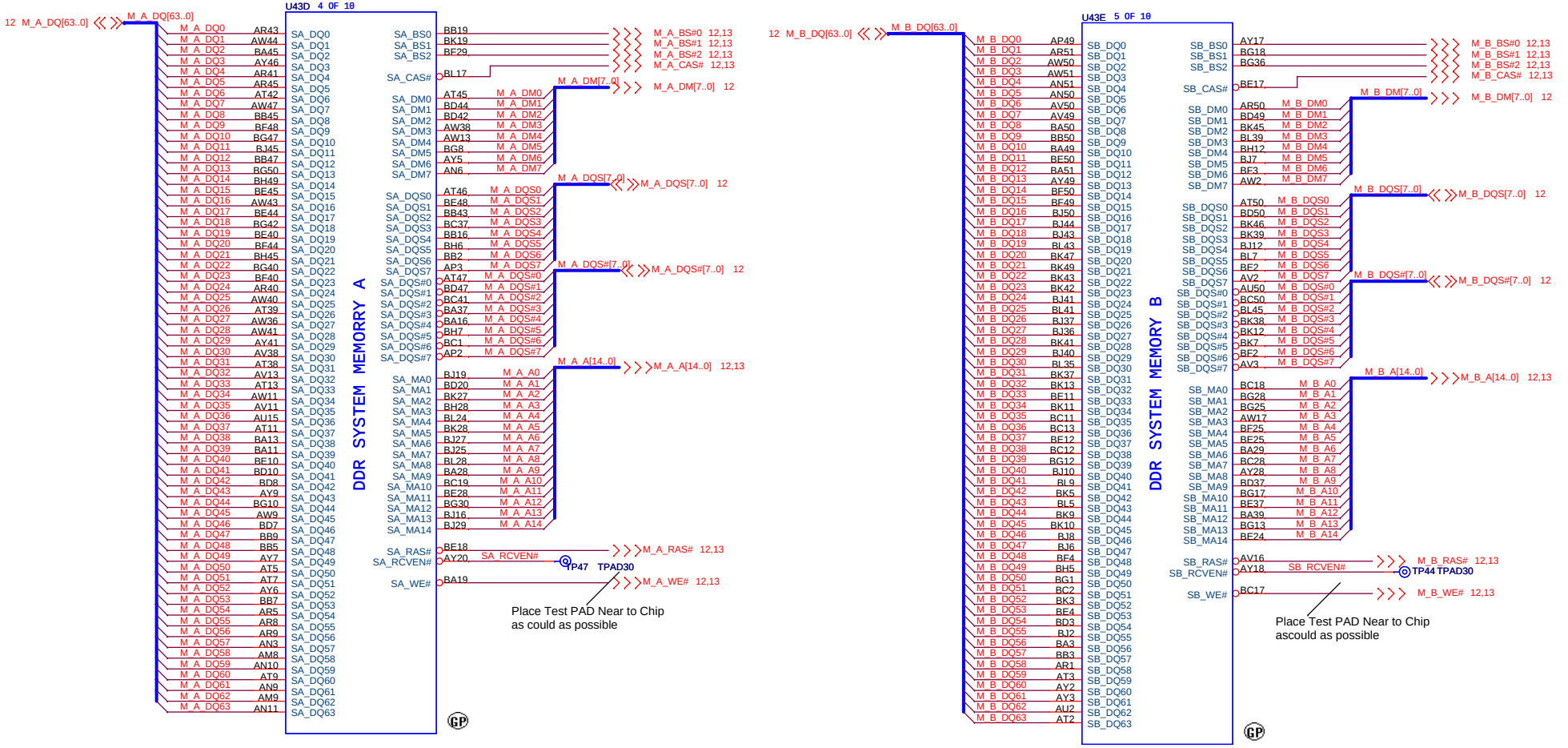
Title: GMCH (2 of 6)	
Size	Document Number: Calado — Rev: -1
Date: Wednesday, September 12, 2007	Sheet 7 of 39



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Title	**GMCH (3 of 6)**	
Size	Document Number: **Calado**	Rev: -1
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VCC_NCTF + VCC=1573mA

FOR VCC CORE

1573mA

1D05V_S0

U43F 6 OF 10

VCC CORE

Coupling CAP 370 mils from the Edge

R43 0R0402-PAD

POWER

1D8V_S3

3138mA

FOR VCC SM

Place CAP where LVDS and DDR2 taps

VCC SM

Place on the Edge

VCC GFX NCTF

VCC_AXG_NCTF + VCC_AXG=7700mA

VCC GFX

VCC SM LF

FOR VCC CORE AND VCC NCTF

308 mils from the Edge

Coupling CAP

U43G 7 OF 10

VCC NCTF

VSS NCTF

FOR VCC AXM NCTF AND VCC AXM

R42 0R0603-PAD

R48 0R6J-3-GP

VCC_AXM_S0

1D25V_S0

Place on the Edge

Coupling CAP

VCC_AXM_NCTF + VCC_AXM=540mA

VCC AXM

VSS AXM NCTF

VSS SCB

TP136TPAD30 TP135TPAD30 TP134TPAD30 TP20 TPAD30 TP74 TPAD30 TP75 TPAD30

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Title	GMCH (4 of 6)	
Size	Document Number: Calado	Rev: -1
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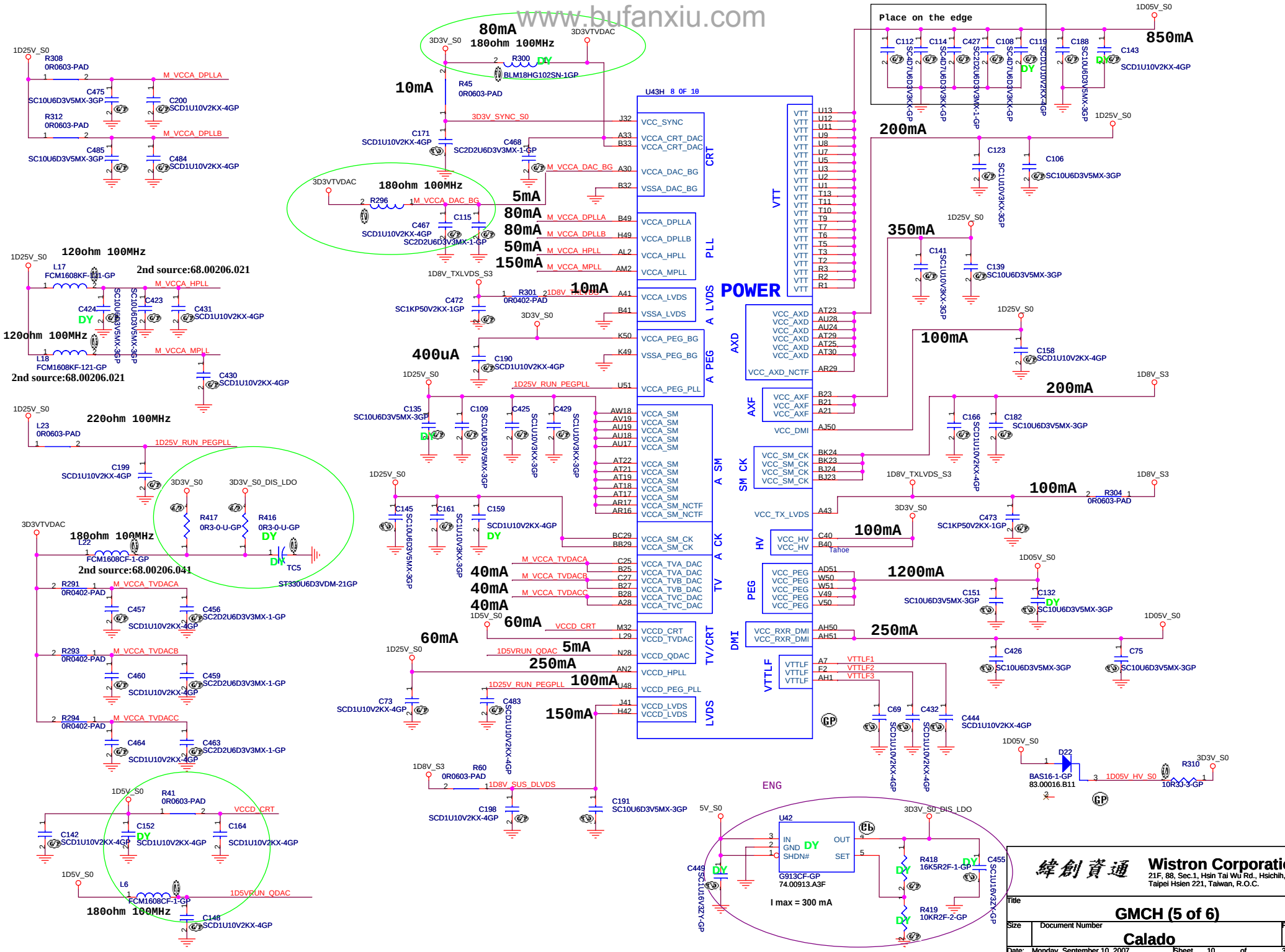

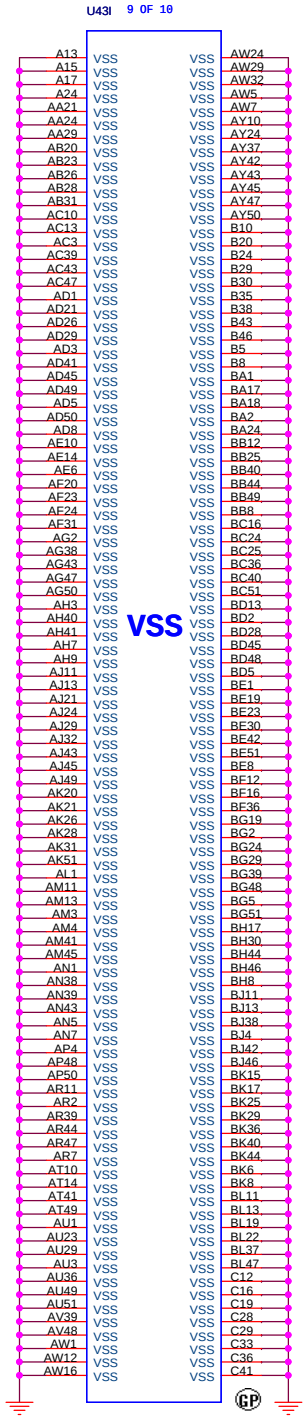

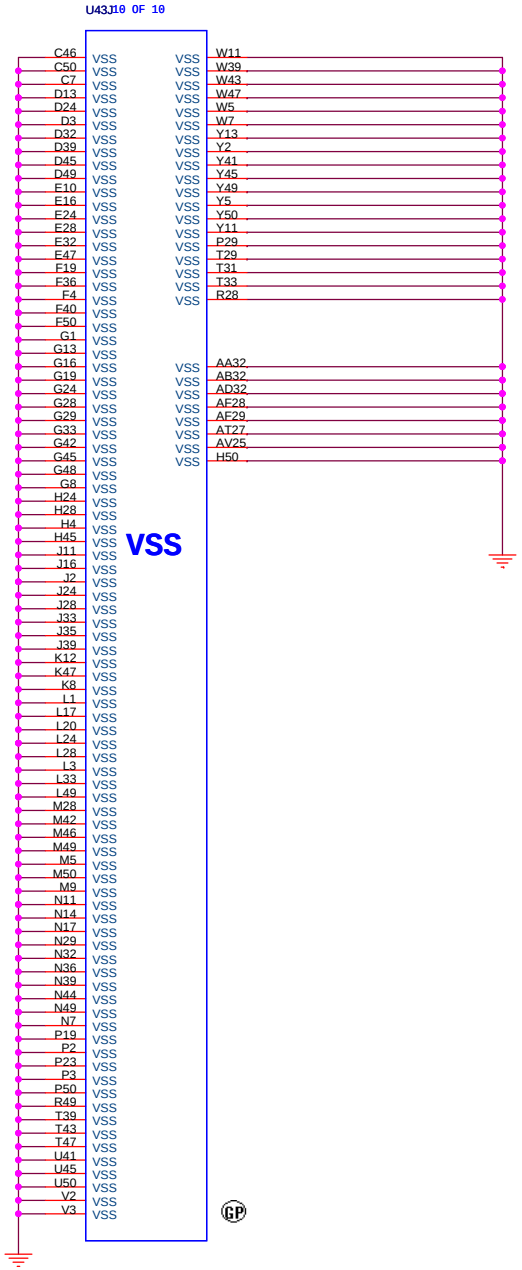

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Title	GMCH (6 of 6)	
Size	Document Number: Calado	Rev: -1
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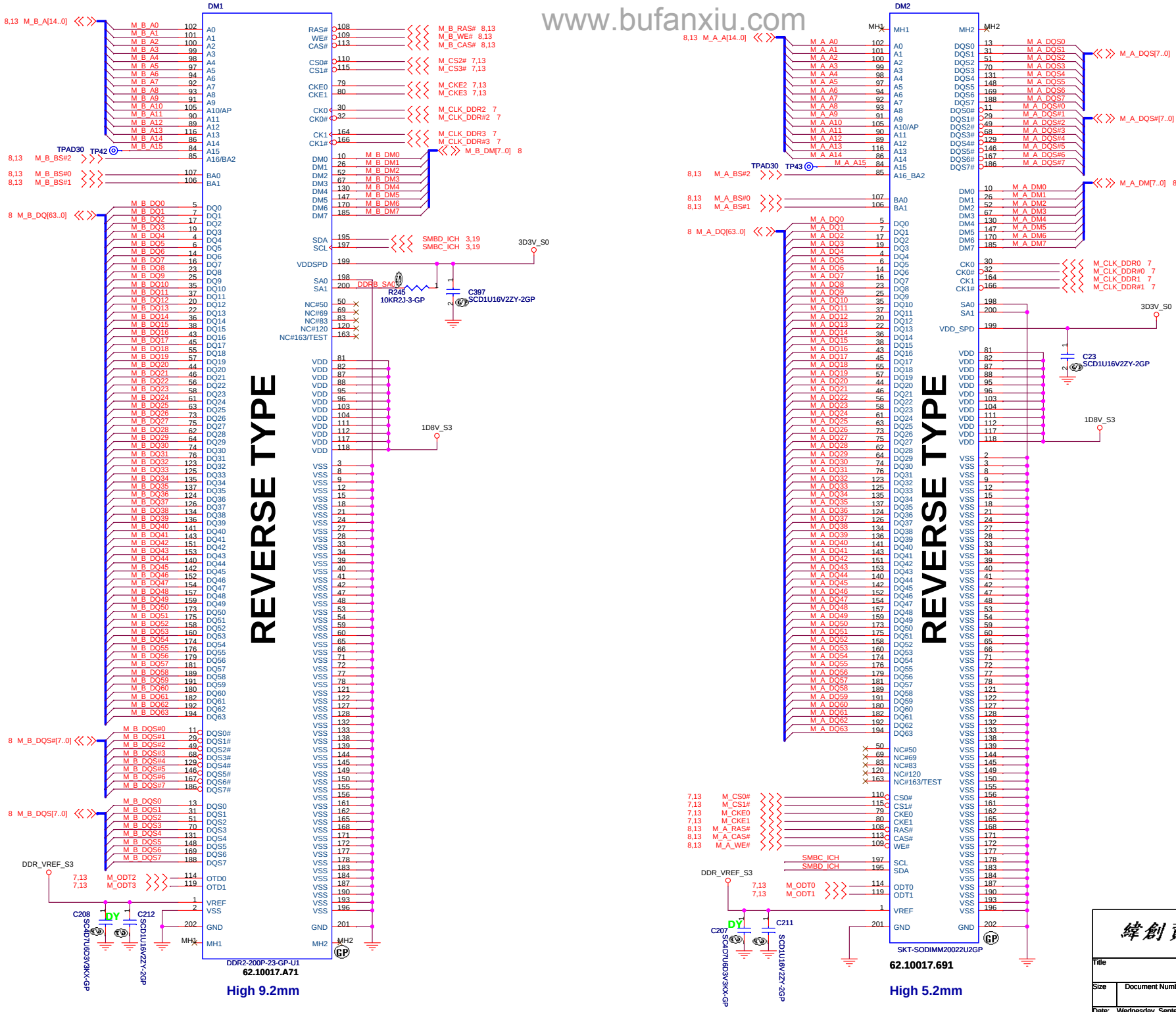

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Title	**DDR2 Socket**
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PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

RN14 SRN56J-5-GP
M_CKE0 7,12
M_CKE1 7,12
M_A_BS#2 8,12
M_A_A12

RN11 SRN56J-5-GP
M_B_A9
M_B_A5
M_B_A8

RN15 SRN56J-5-GP
M_CKE2 7,12
M_CKE3 7,12
M_B_BS#2 8,12
M_B_A12

RN7 SRN56J-5-GP
M_B_A3
M_B_A1
M_B_A10
M_B_WE# 8,12

RN3 SRN56J-5-GP
M_B_A13
M_ODT2 7,12
M_ODT3 7,12
M_B_RAS# 8,12

RN8 SRN56J-5-GP
M_B_BS#1 8,12
M_B_A2
M_B_A0
M_B_A4

RN12 SRN56J-5-GP
M_B_A14
M_B_A6
M_B_A7
M_B_A11

RN2 SRN56J-5-GP
M_B_BS#0 8,12
M_B_CAS# 8,12
M_CS3# 7,12
M_CS2# 7,12

RN4 SRN56J-5-GP
M_A_A13
M_ODT0 7,12
M_CS0# 7,12
M_A_RAS# 8,12

RN9 SRN56J-5-GP
M_A_BS#1 8,12
M_A_A2
M_A_A0
M_A_A4

RN5 SRN56J-5-GP
M_A_CAS# 8,12
M_CS1# 7,12
M_ODT1 7,12

RN10 SRN56J-5-GP
M_A_A9
M_A_A8
M_A_A5
M_A_A3

RN13 SRN56J-5-GP
M_A_A6
M_A_A7
M_A_A11
M_A_A14

RN6 SRN56J-5-GP
M_A_A1
M_A_A10
M_A_BS#0 8,12
M_A_WE# 8,12

M_A_A[14..0] → M_A_A[14..0] 8,12
M_B_A[14..0] → M_B_A[14..0] 8,12

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

C71 C86 C85 C103 C88 C78 C101 C121 C70 C100 C120 SCD1U16V2ZY-2GP DY
C127 C89 C105 C144 C129 C153 C96 C116 C134 C74 C130 SCD1U16V2ZY-2GP DY

Place these Caps near DM1

1D8V_S3

C84 C124 C102 C95 C107 SC2D2U6D3V3MX-1-GP
C77 C113 C118 C94 SCD1U16V2ZY-2GP DY

Place these Caps near DM2

1D8V_S3

C445 C454 C72 C450 C137 SC2D2U6D3V3MX-1-GP
C452 C80 C442 C447 SCD1U16V2ZY-2GP DY

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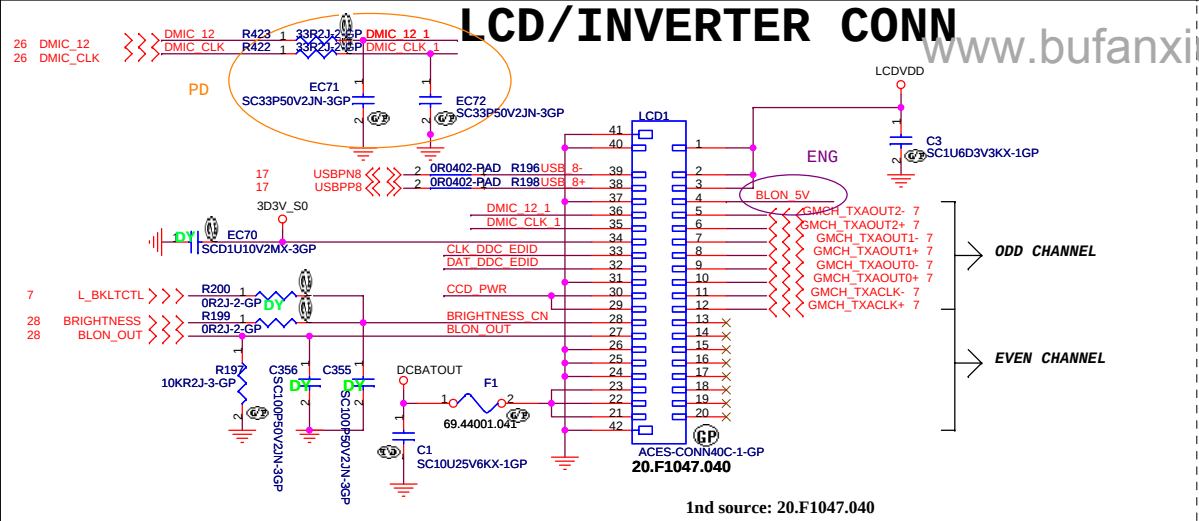
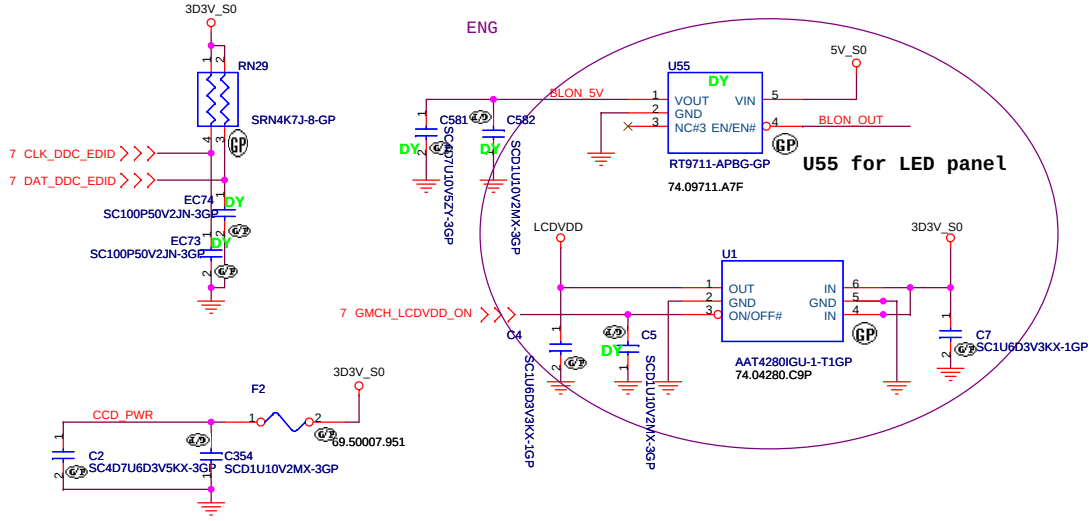
Title	DDR2 Termination Resistor	
Size	Document Number: Calado	Rev: -1
Date: Wednesday, September 12, 2007	Sheet 13 of 39	

LCD/INVERTER CONN



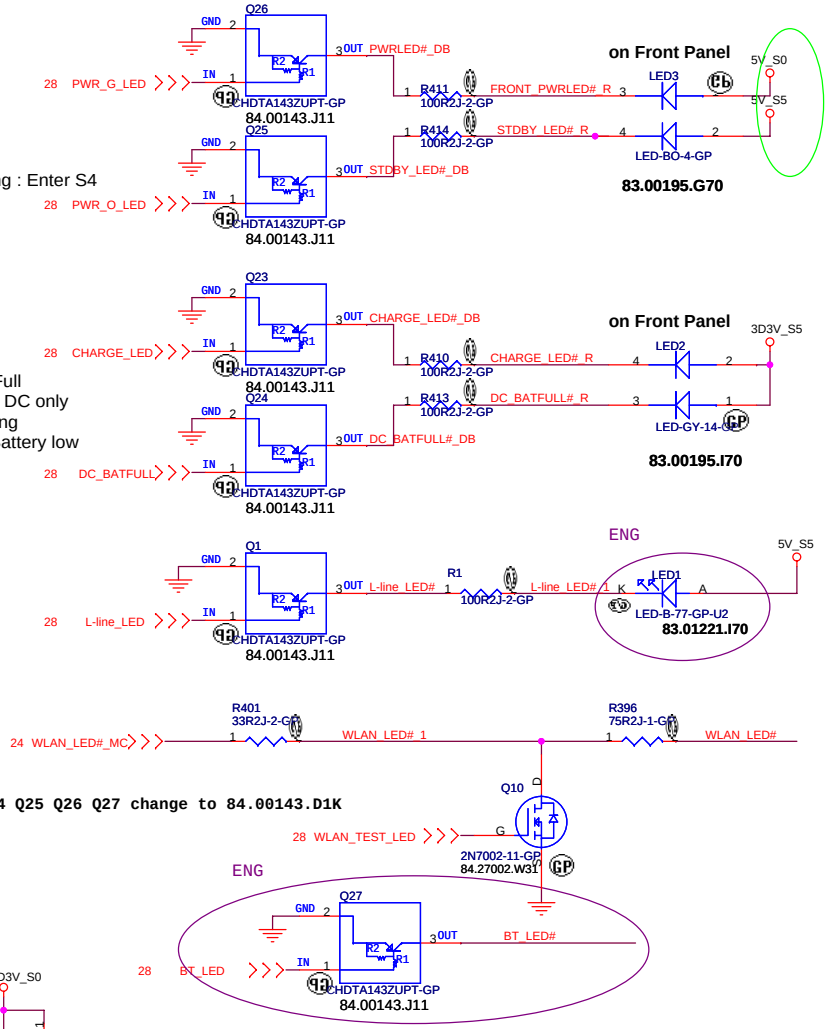
1nd source: 20.F1047.040



LED

Power:
BLUE : S0
Orange : S3
Orange Blinking : Enter S4

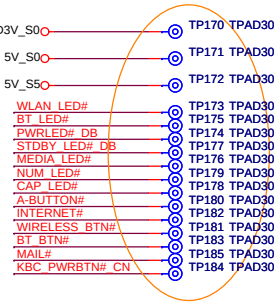
Charger:
Green: Battary Full
OFF : Battery or DC only
Orange : Charging
Orange Blink : Battery low

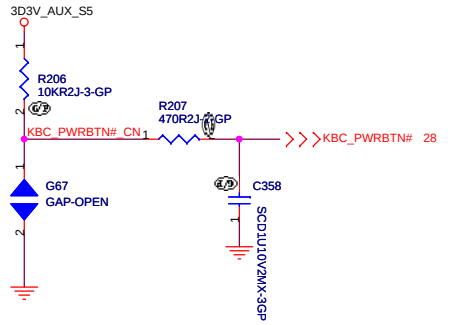


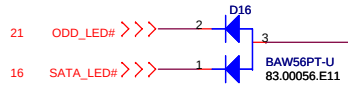
Q1 Q23 Q24 Q25 Q26 Q27 change to 84.00143.D1K

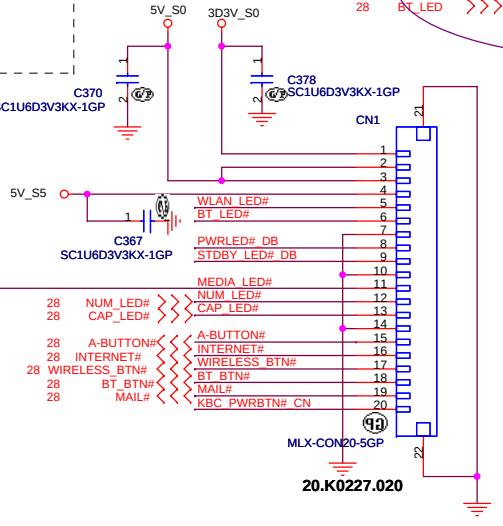
PWR BD

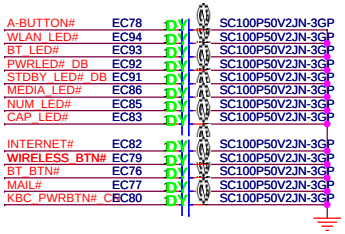
PD











<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN & LED & PWR BD

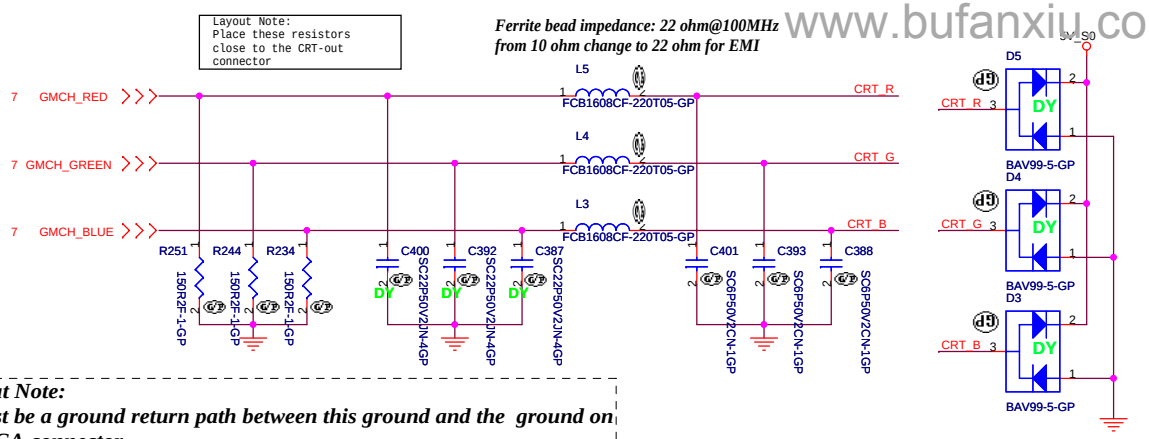
Size | Document Number: Calado | Rev: -1

Date: Wednesday, September 12, 2007 | Sheet 14 of 39

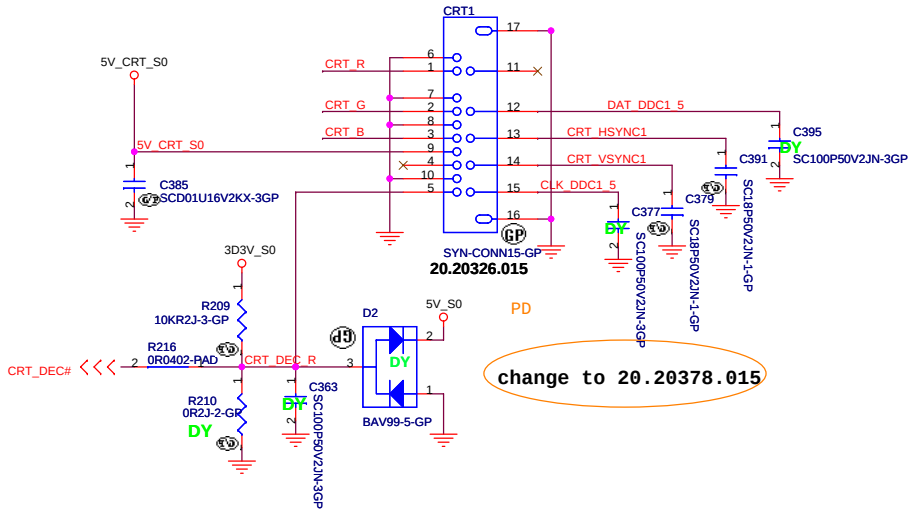
CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

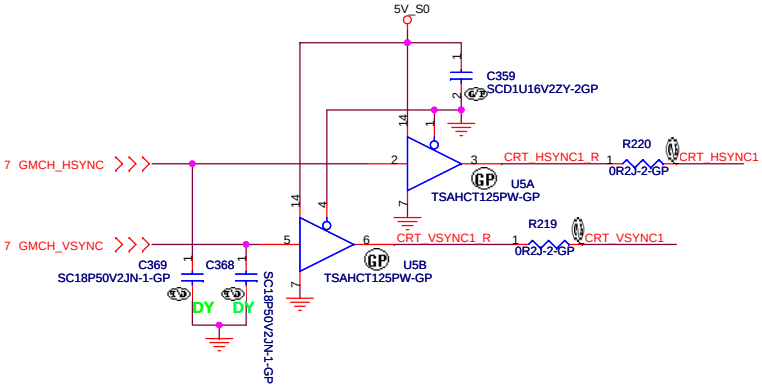
Ferrite bead impedance: 22 ohm@100MHz from 10 ohm change to 22 ohm for EMI



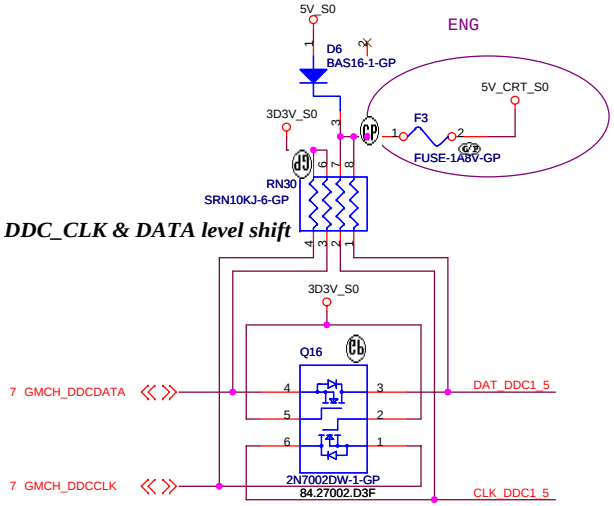
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



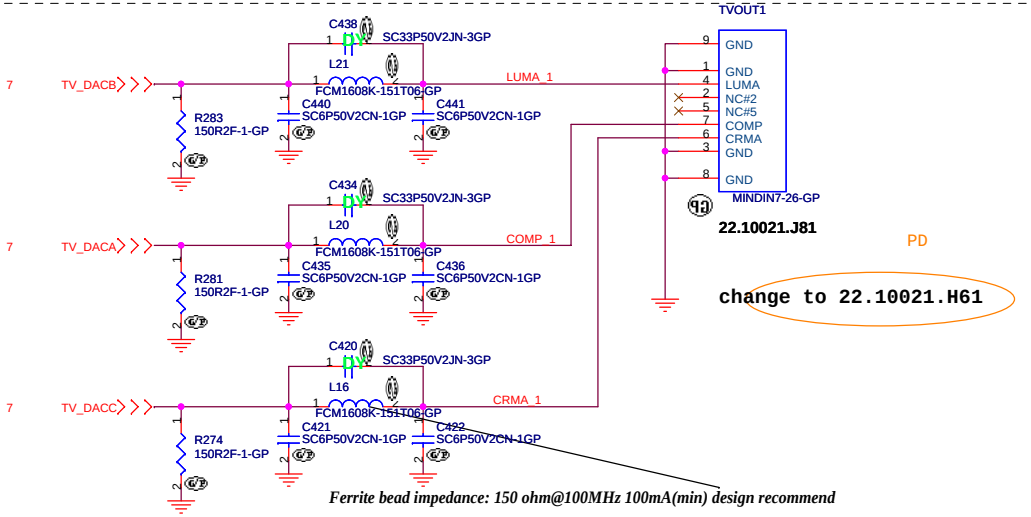
Hsync & Vsync level shift



DDC_CLK & DATA level shift

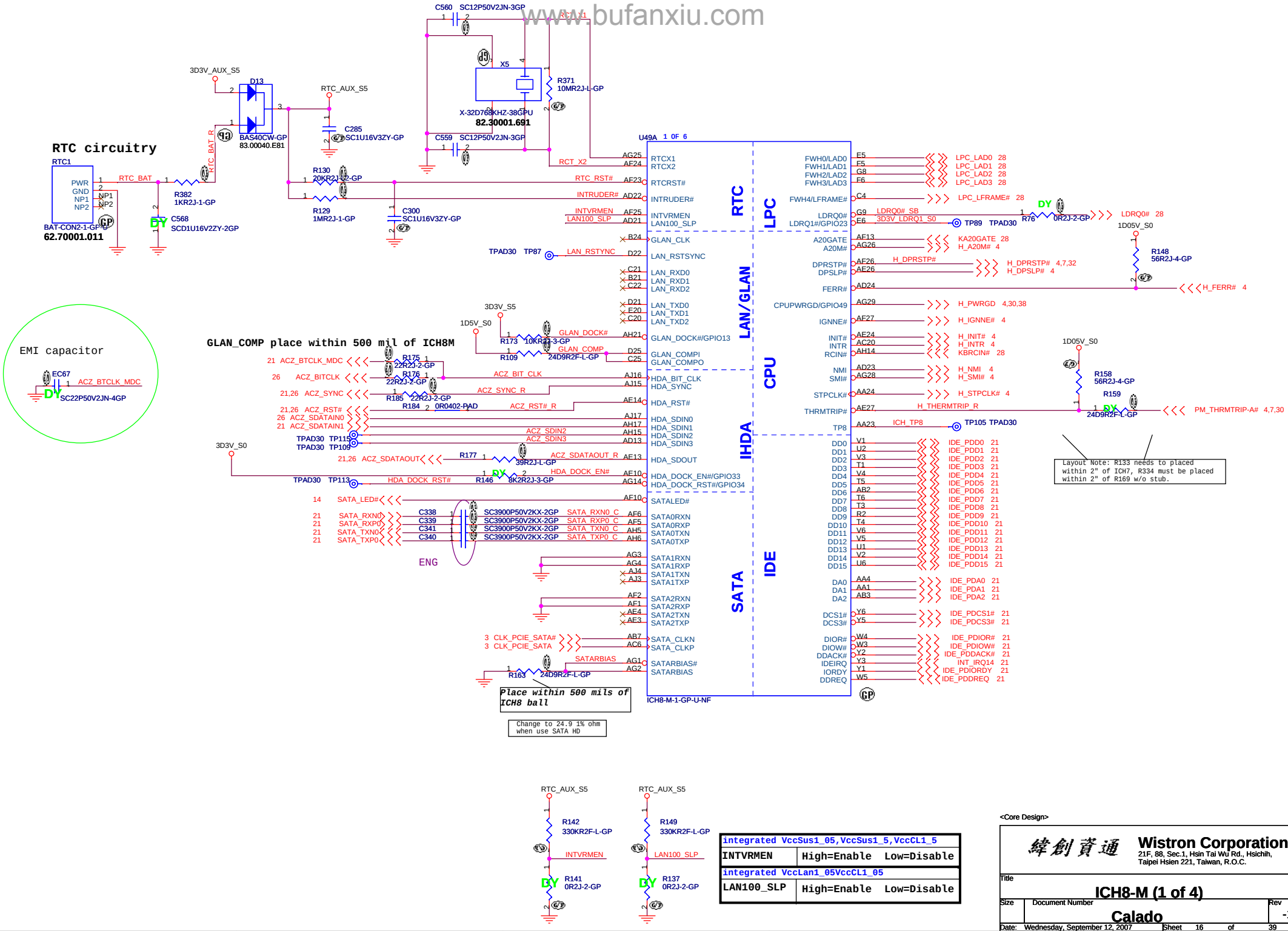


TV CONN



Ferrite bead impedance: 150 ohm@100MHz 100mA(min) design recommend

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CRT/TV Connector**	
Size	Document Number **Calado**	Rev -1
Date: Thursday, September 13, 2007	Sheet 15 of 39	



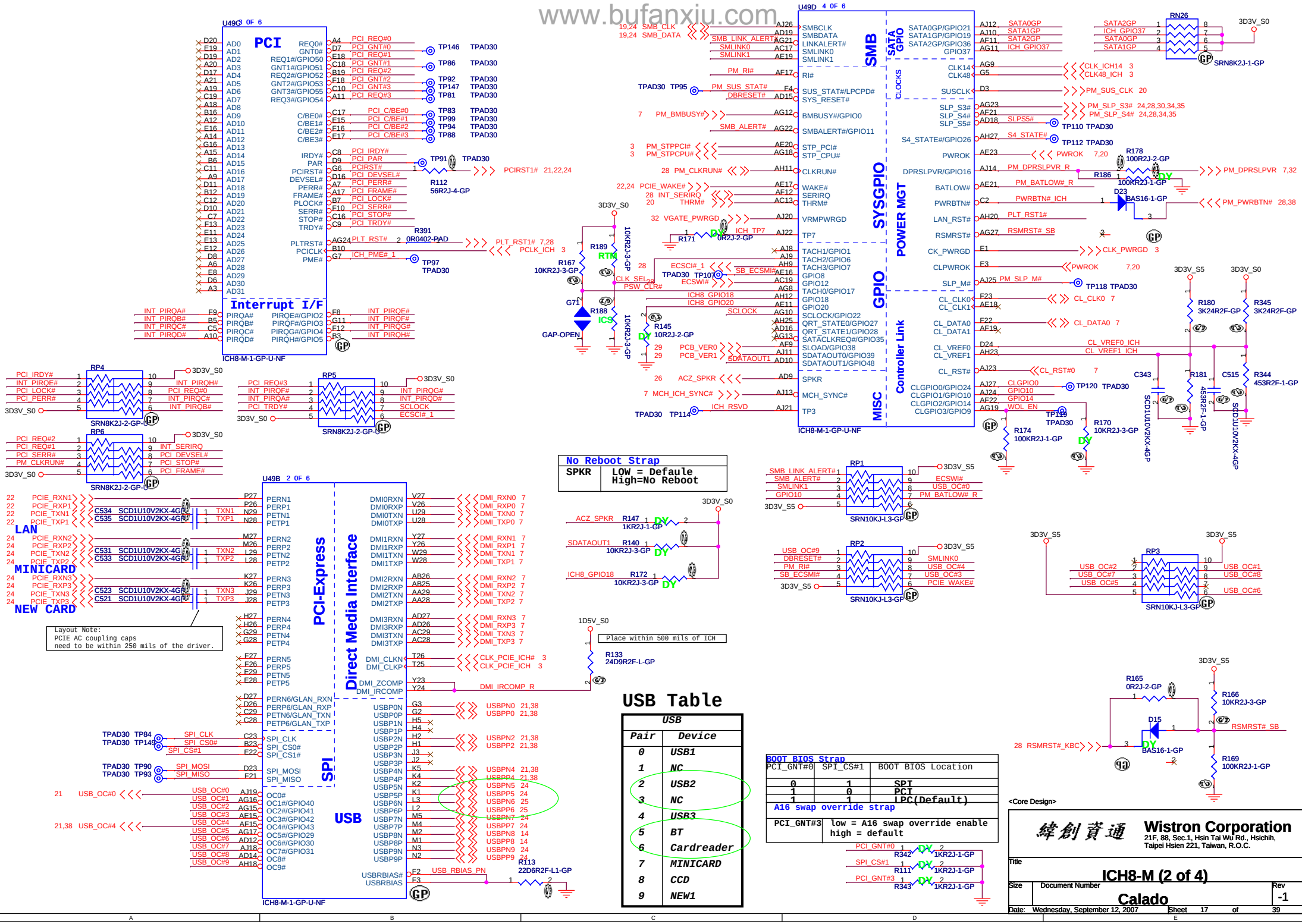
<Core Design>

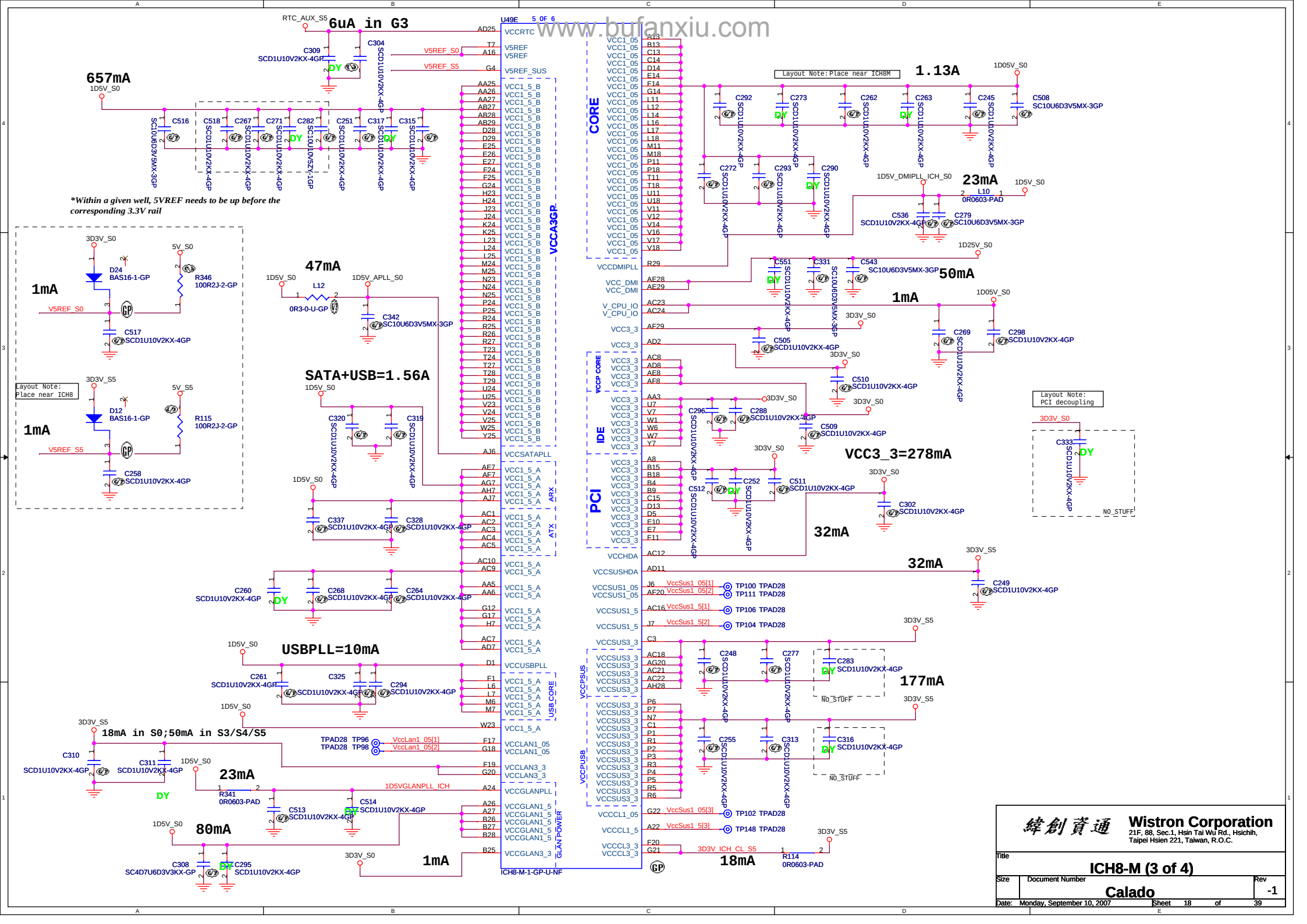
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

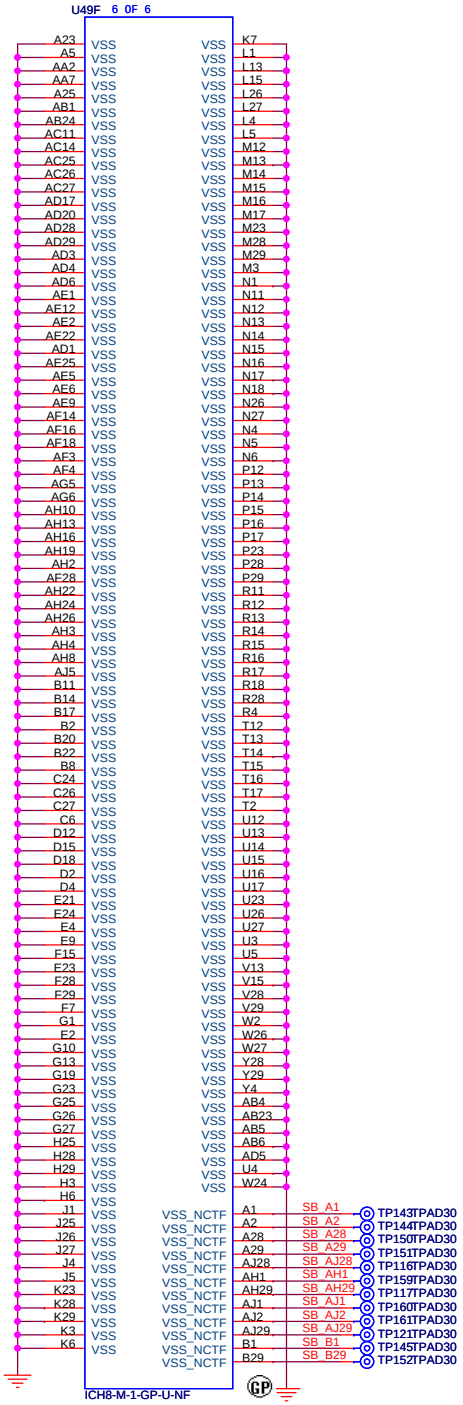
Title: ICH8-M (1 of 4)

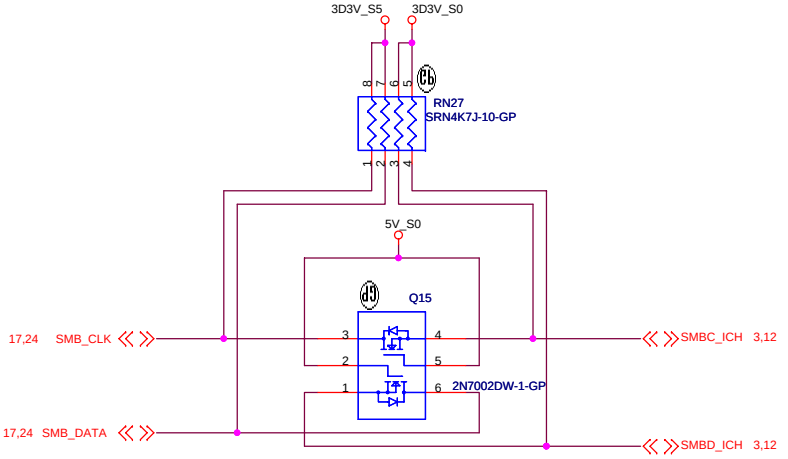
Size | Document Number: Calado | Rev: -1

Date: Wednesday, September 12, 2007 Sheet 16 of 39









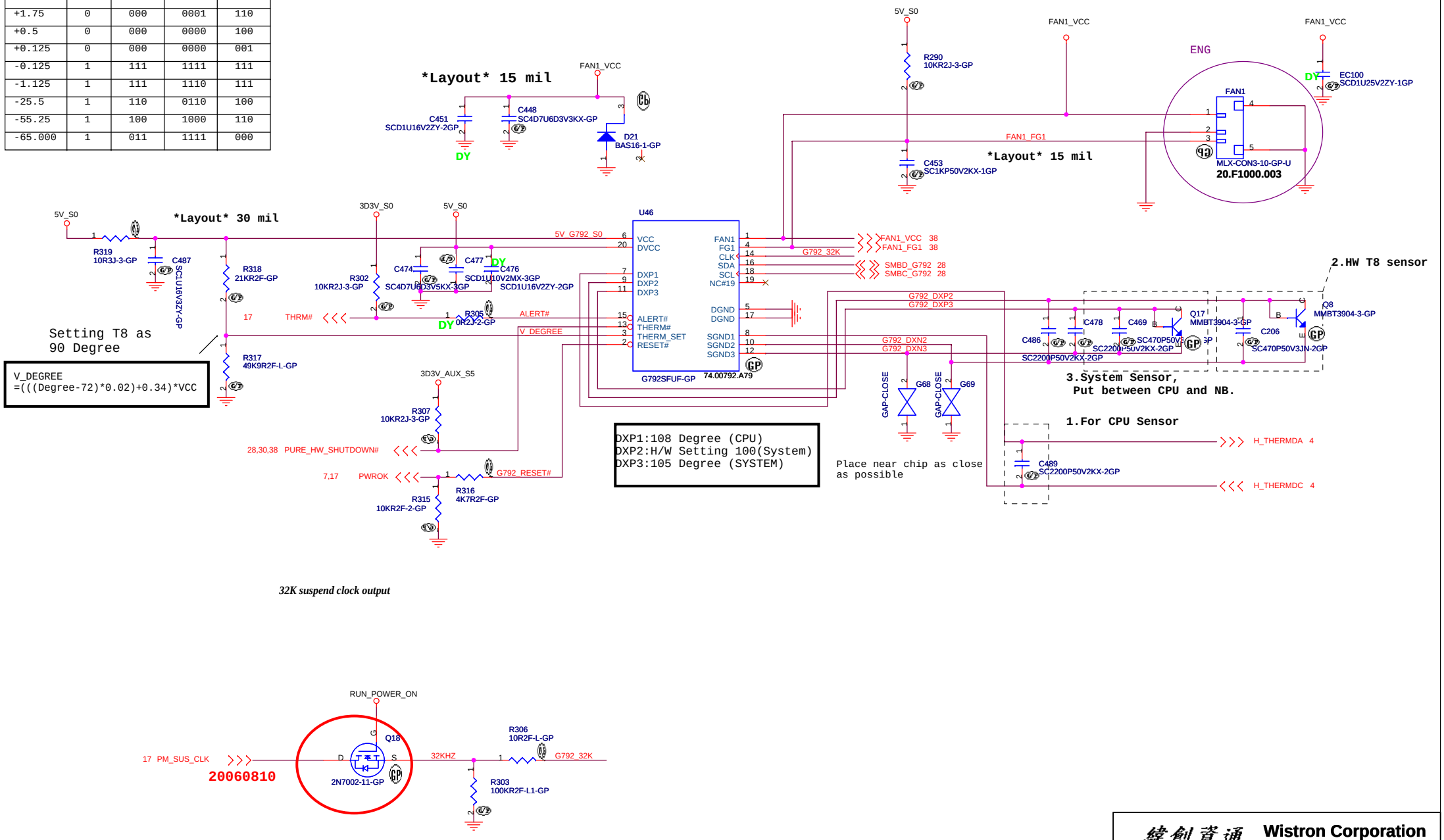
Q12 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ICH8-M (4 of 4)	
Size	Document Number: Calado	Rev: -1
Date: Wednesday, September 12, 2007	Sheet 19 of 39	

TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



32K suspend clock output

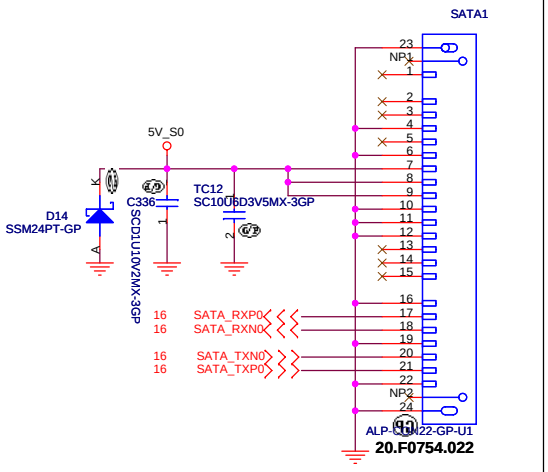
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal/Fan Controllor**

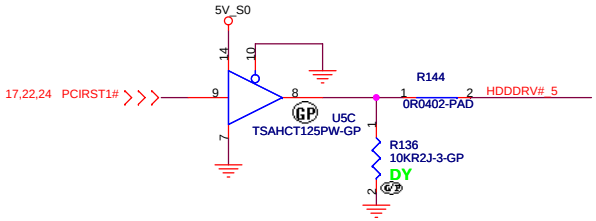
Size | Document Number: **Calado** | Rev: -1

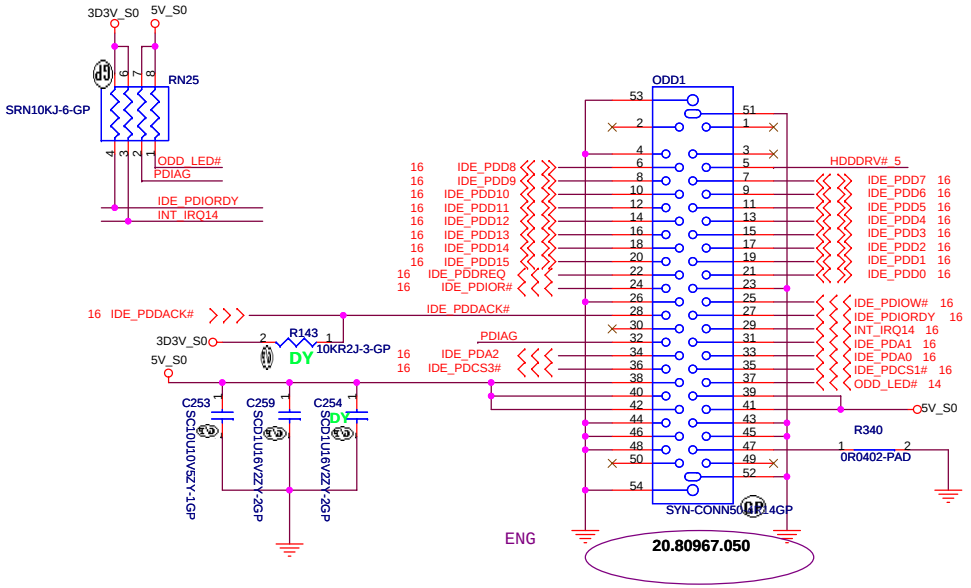
Date: Thursday, September 13, 2007 | Sheet 20 of 39

SATA HD Connector

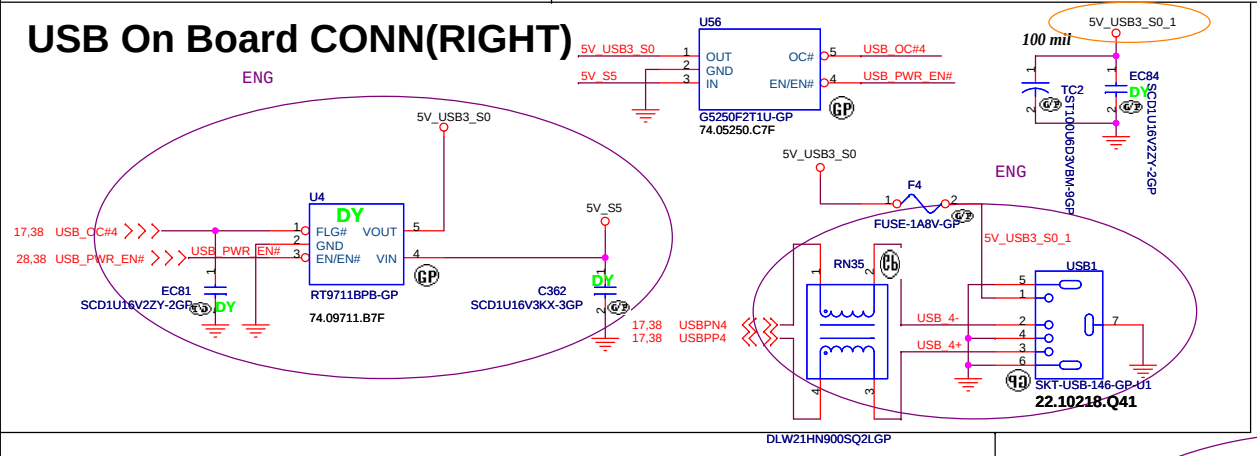


ODD Connector

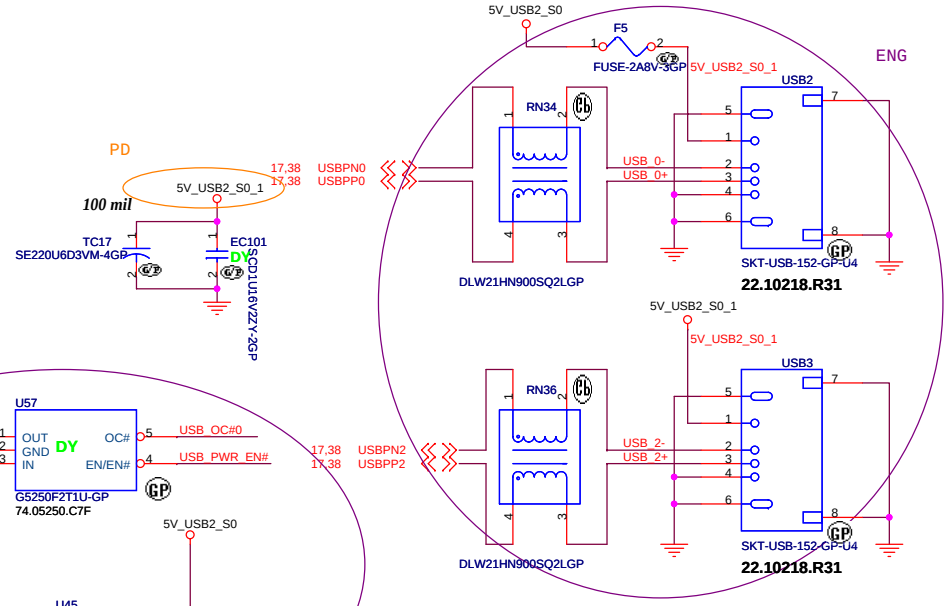




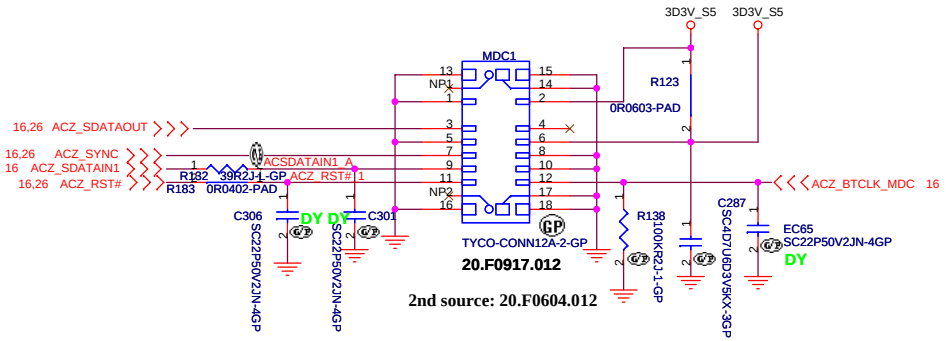
USB On Board CONN(RIGHT)

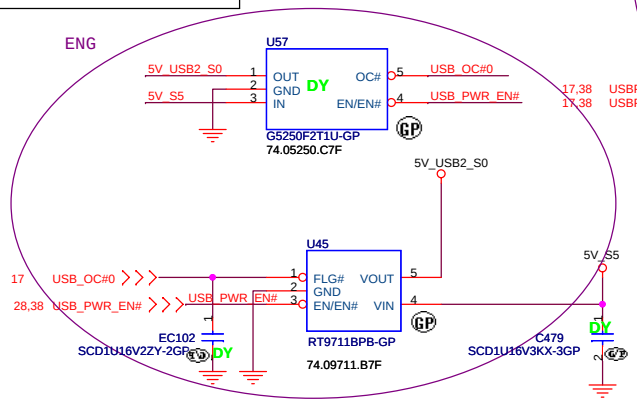


USB On Board CONN(LEFT)



MDC 1.5 CONN





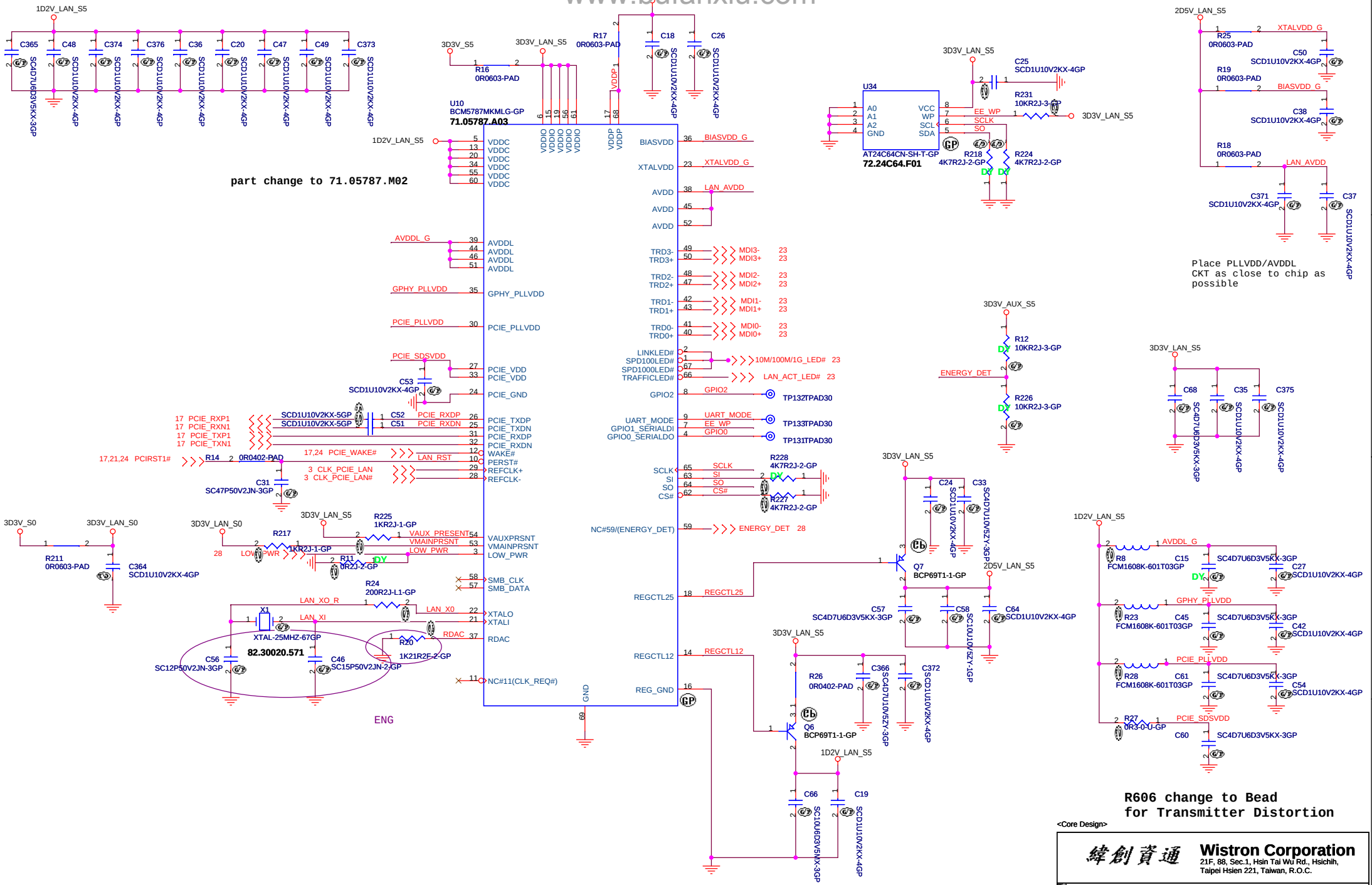
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD / CDROM / USB / MDC

Size | Document Number: Calado | Rev: -1

Date: Wednesday, September 12, 2007 | Sheet 21 of 39



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN BCM5787

Size: A3 | Document Number: Calado | Rev: -1

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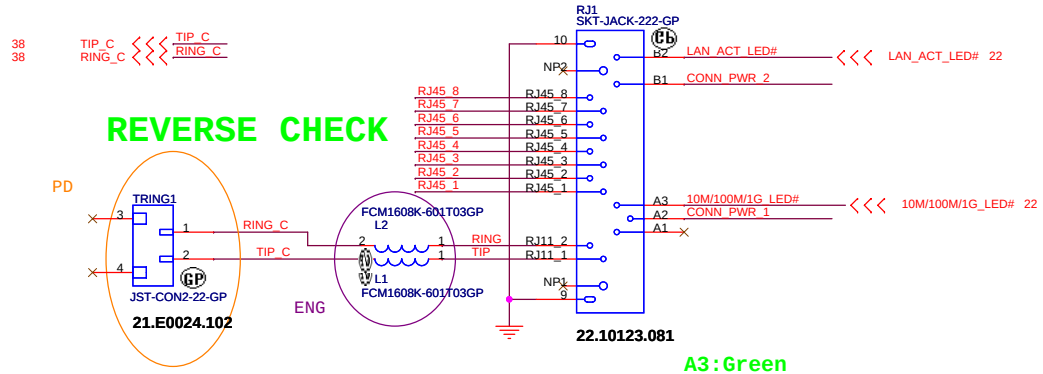
LAN Connector

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

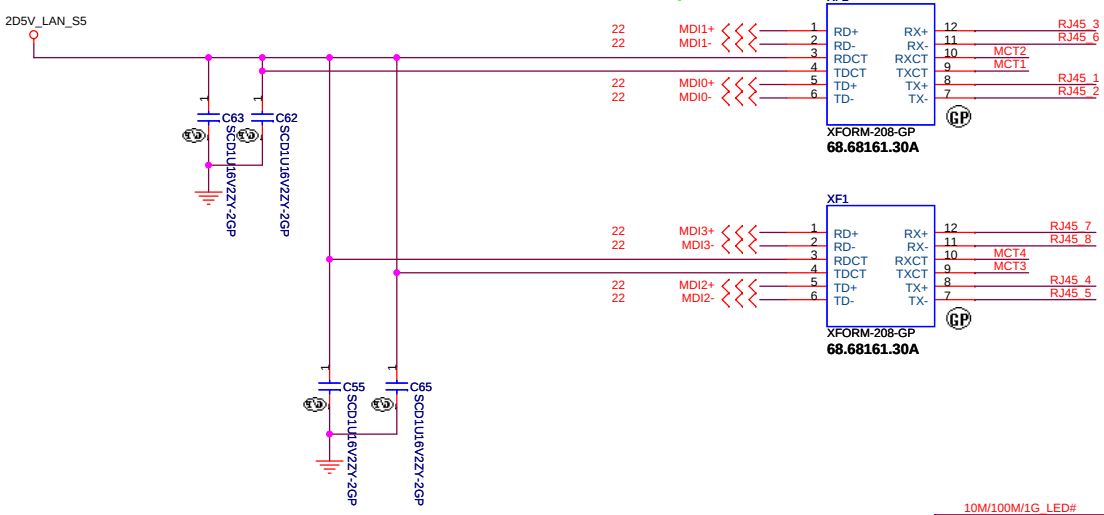


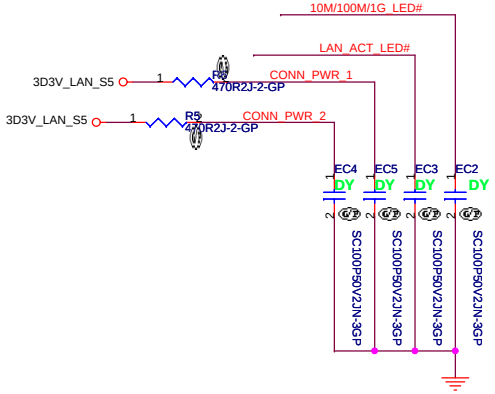
A3:Green
B2:YELLOW

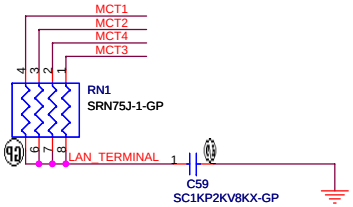
LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.

GIGA Lan Transformer







1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

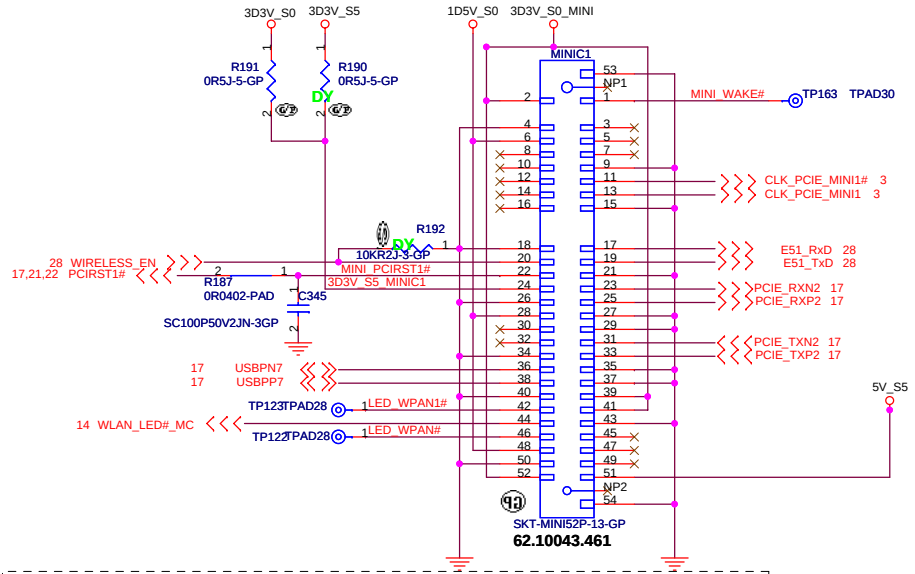
10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

<Core Design>

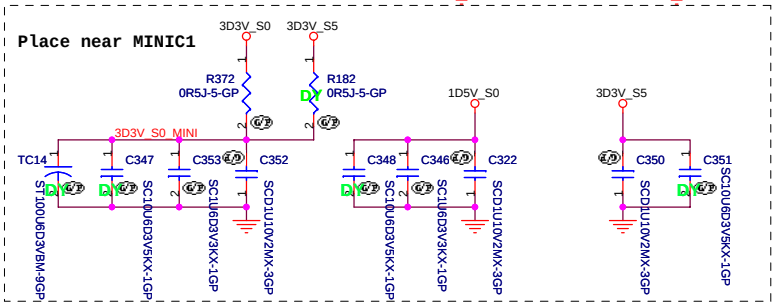
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector
Size: A3 | Document Number: Calado | Rev: -1
Date: Wednesday, September 12, 2007 | Sheet 23 of 39

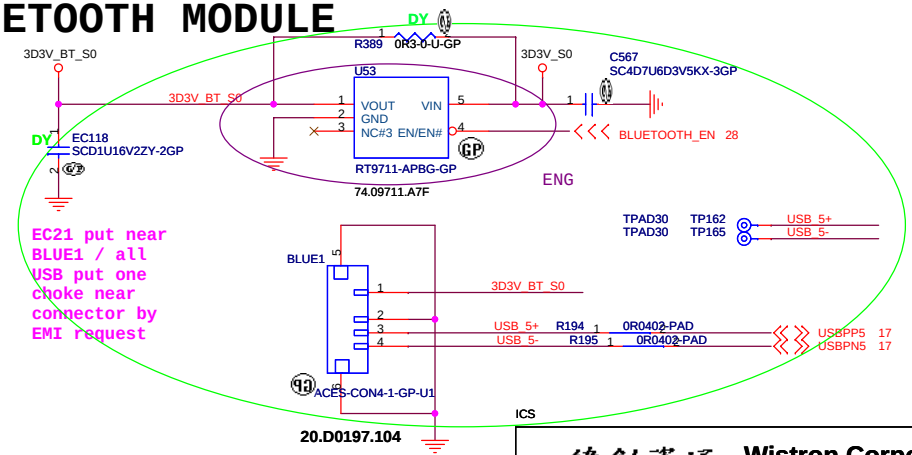
Mini Card Connector



Place near MINIC1



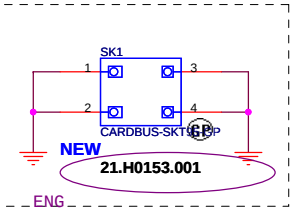
BLUETOOTH MODULE



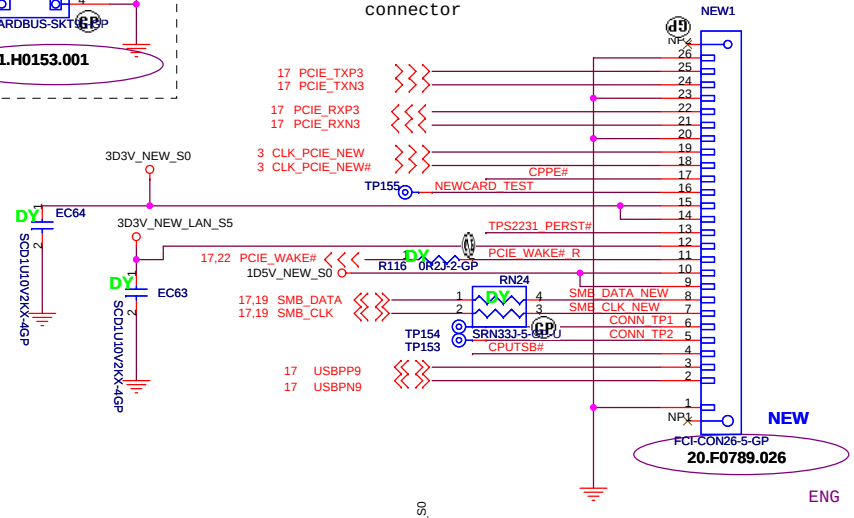
EC21 put near BLUE1 / all USB put one choke near connector by EMI request

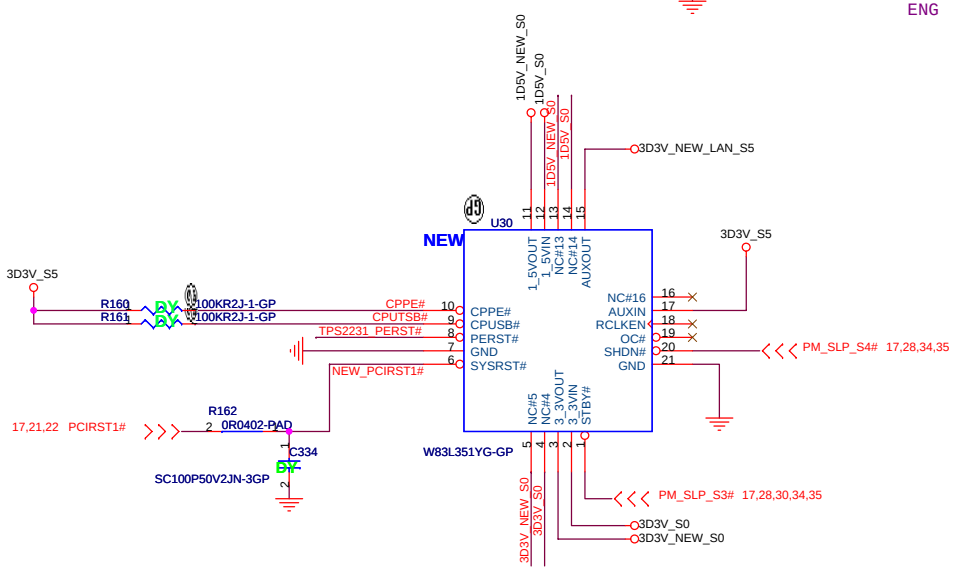
1st source:20.D0197.104
2nd source:20.F0984.004

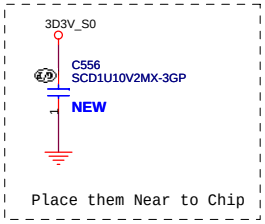
NEWCARD Connector

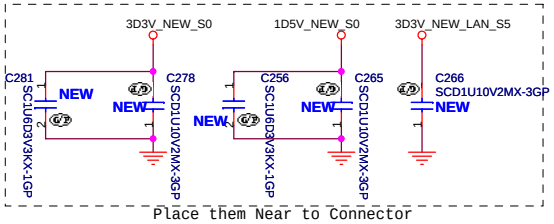


Reserve the symbol for bottom side connector



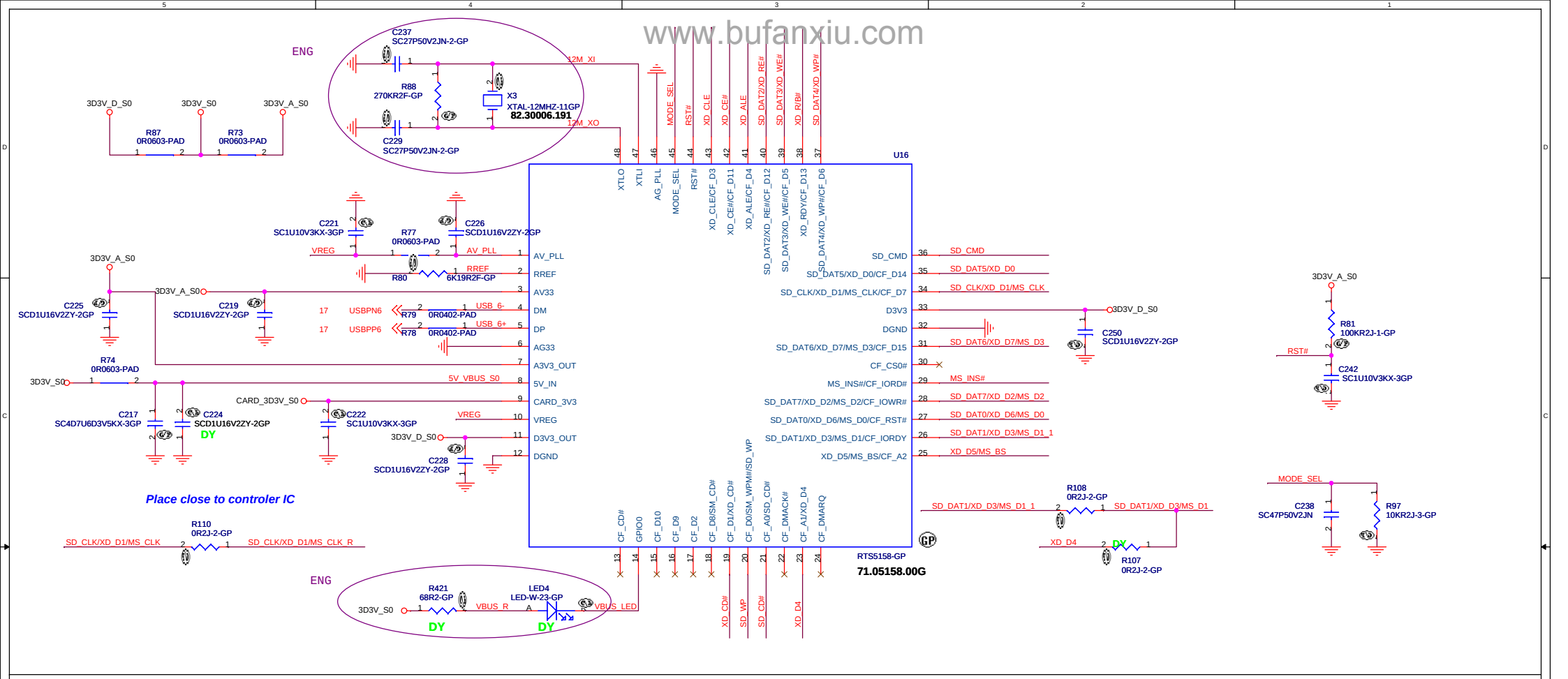




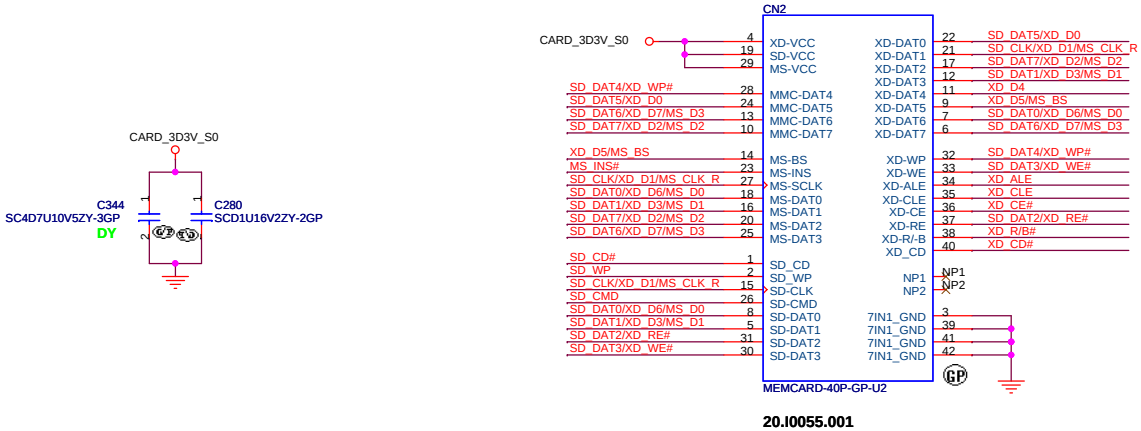


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD / NEW CARD/BT
Size: Document Number: Calado
Rev: -1
Date: Wednesday, September 12, 2007 Sheet 24 of 39



4 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)

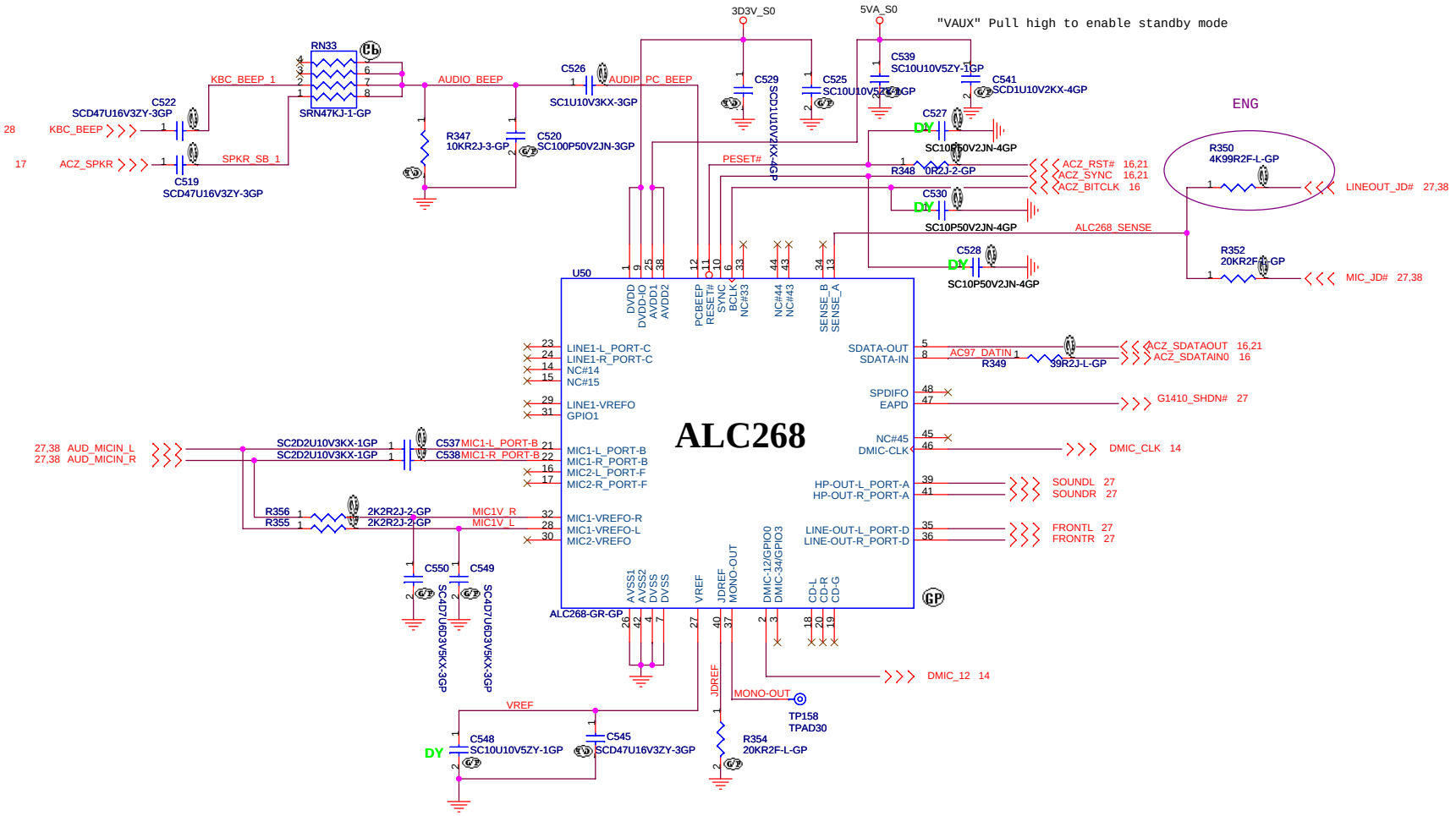


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Card Reader Controller - RTS5158

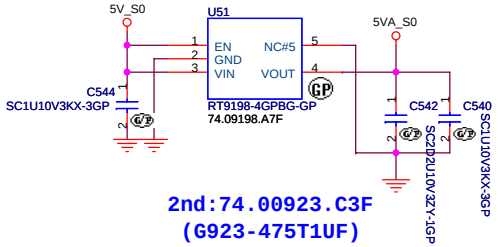
Size	Document Number	Rev
	Calado	-1

Date: Wednesday, September 12, 2007 Sheet 25 of 39



POWER GENERATE

Layout
20 mil



2nd:74.00923.C3F
(G923-475T1UF)

ICS

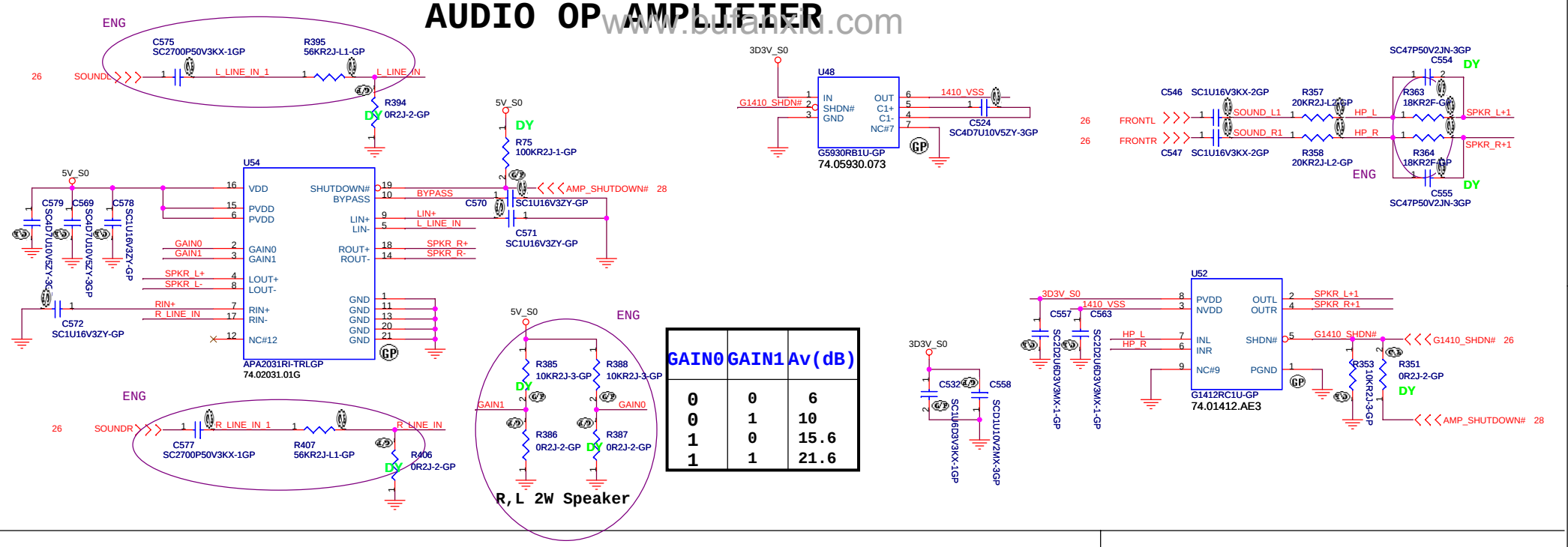
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AZALIA CODEC - ALC268**

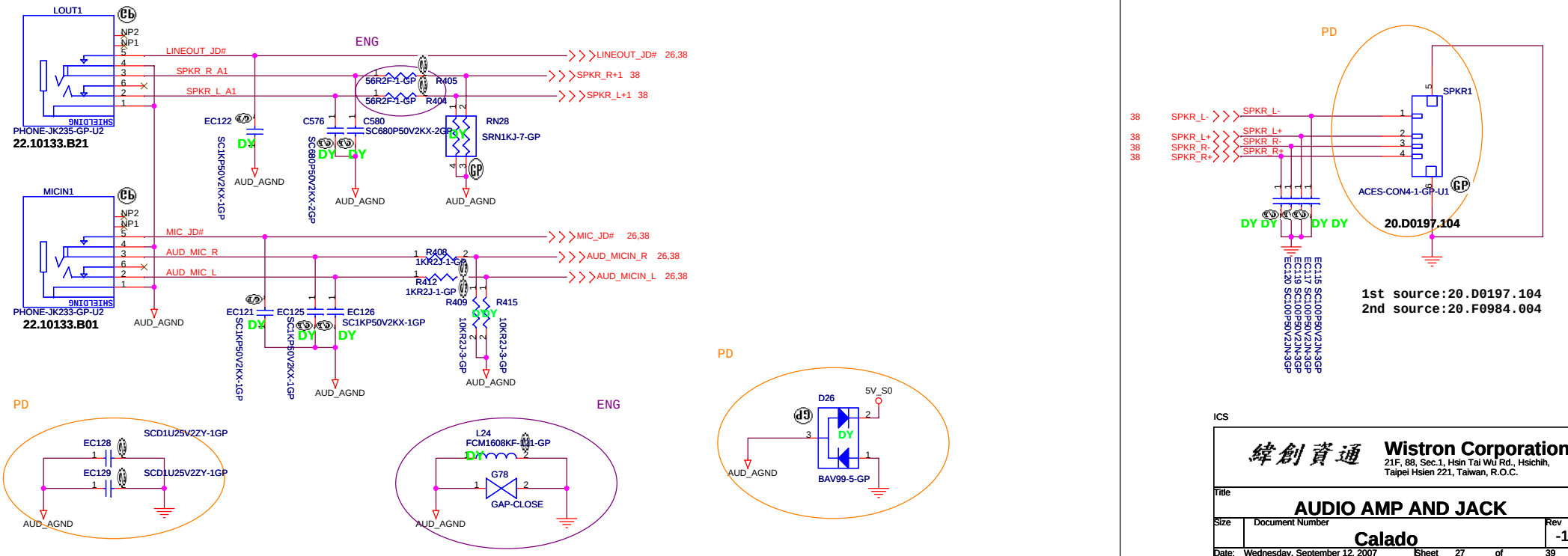
Size | Document Number: **Calado** | Rev: -1

Date: Wednesday, September 12, 2007 | Sheet 26 of 39

AUDIO OP AMPLIFIER



GAIN0	GAIN1	Av(dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6



Internal Speaker

1st source:20.D0197.104
2nd source:20.F0984.004

ICS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP AND JACK

Size | Document Number: Calado | Rev: -1

Date: Wednesday, September 12, 2007 | Sheet 27 of 39

FOR KBC DEBUG

C344,C645 colse to Pin VDD C319,C657 colse to Pin102

THERMAL----->

BATTERY----->

H	Big KB(17")
L	Small KB (Biwa)

ENG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

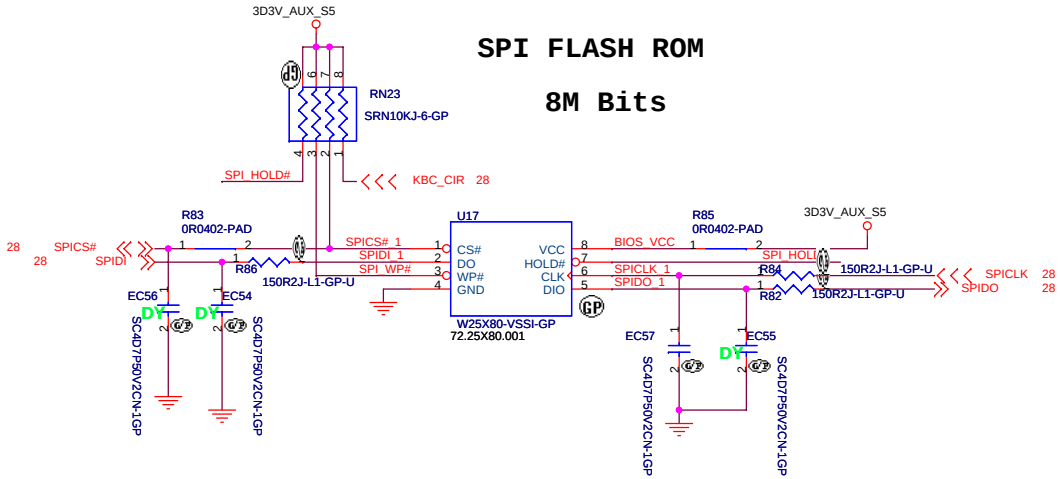
Title: KBC WPC8763L

Size: A3 | Document Number: Calado | Rev: -1

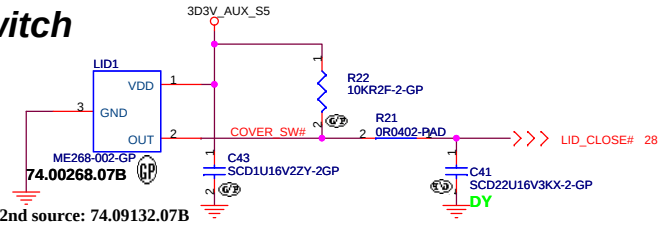
Date: Wednesday, September 12, 2007 | Sheet 28 of 39

SPI FLASH ROM

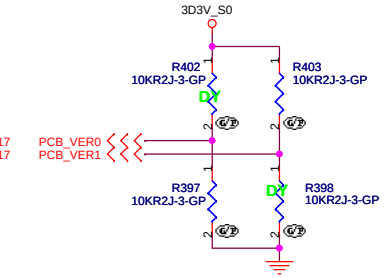
8M Bits



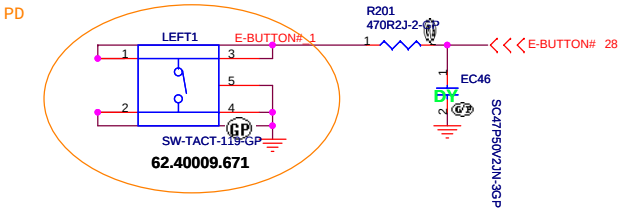
Hall Switch

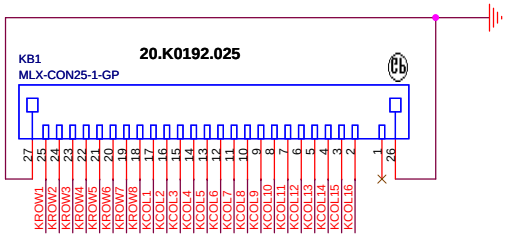


PlanarID
(1,0)
SA: 0,0
SB: 0,1
-1: 1,0
-2: 1,1

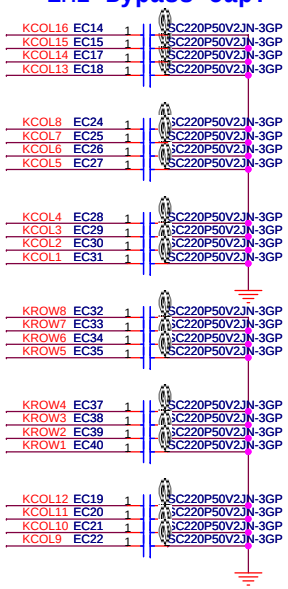


E-key

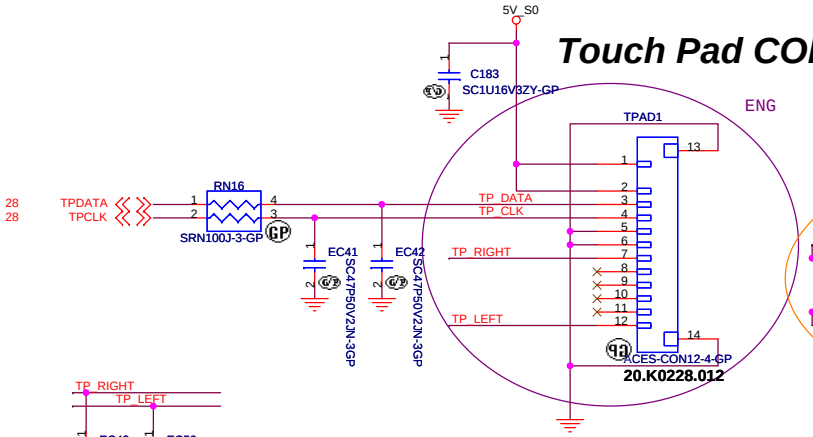




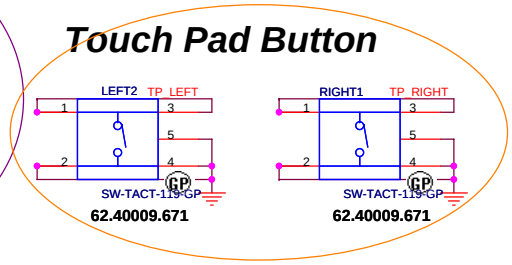
EMI Bypass cap.



Touch Pad CONN



Touch Pad Button



KROW[1..8] KROW[1..8] 28,38
KCOL[1..16] KCOL[1..16] 28,38

Internal KeyBoard CONN

1 25

CHECK KB SPEC. AND PIN DEFINE

ICS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: BUTTONs / KB / TOUCHPAD / BIOS

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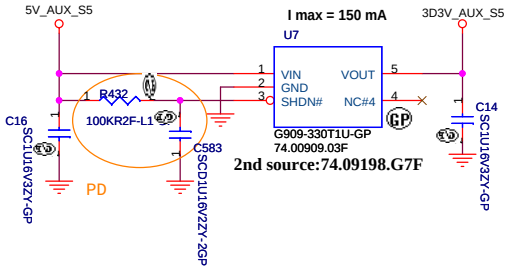
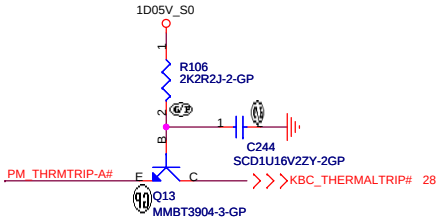
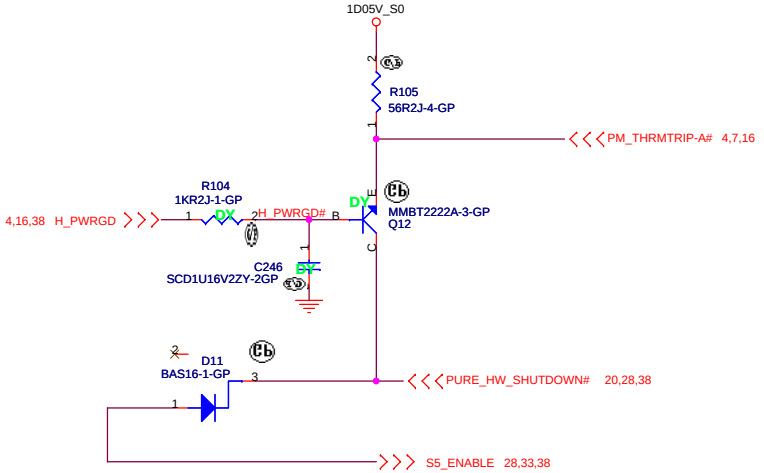
Date: Wednesday, September 12, 2007 Sheet 29 of 39

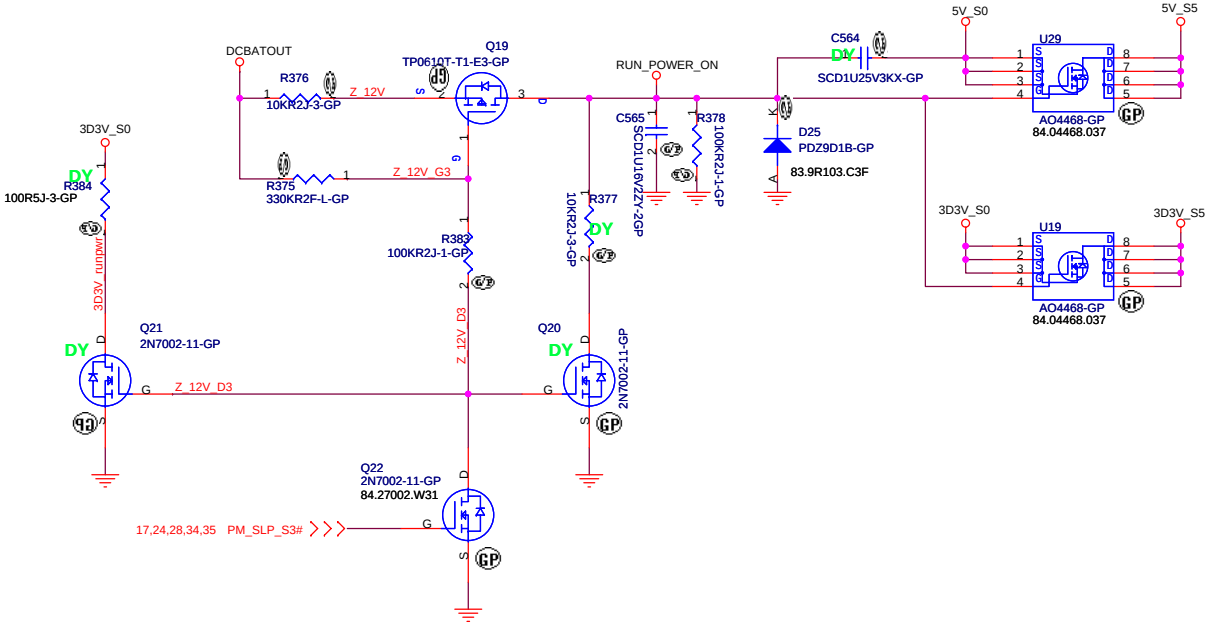
Aux Power 3D3V_AUX_S5







Run Power



ICS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN POWER and 3D3V_AUX_S5**

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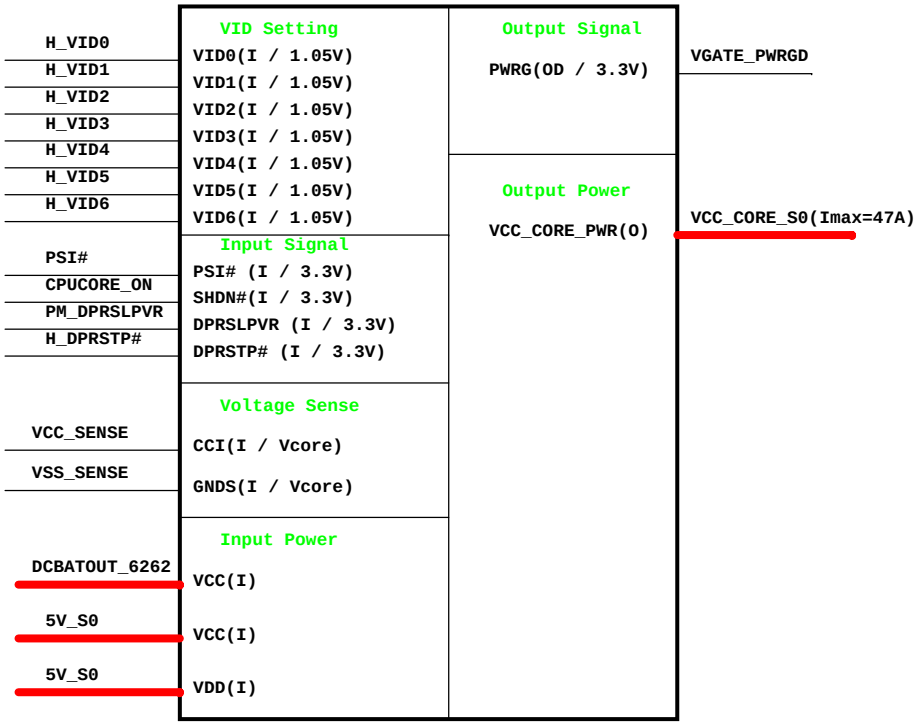
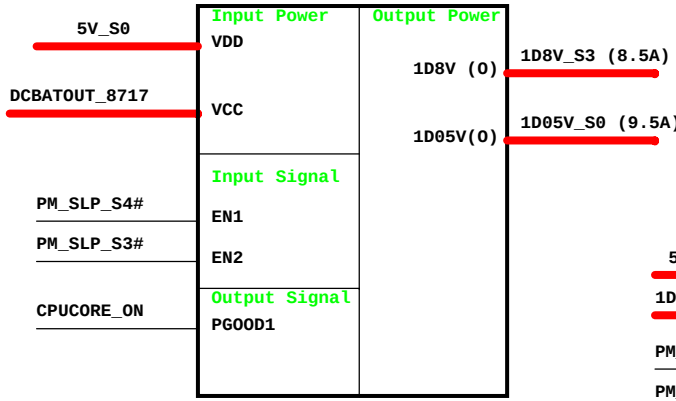
	Calado	-1

Date: Wednesday, September 12, 2007 Sheet 30 of 39

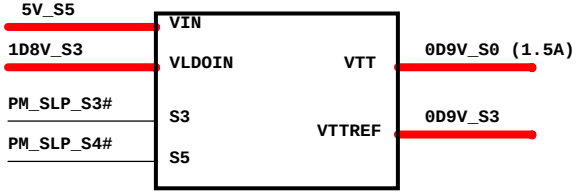
CPU_CORE
MAX8770



TPS51124
1D8V/1D05V

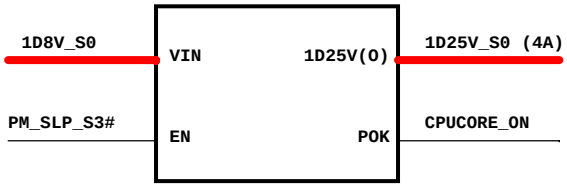


0D9V_S0



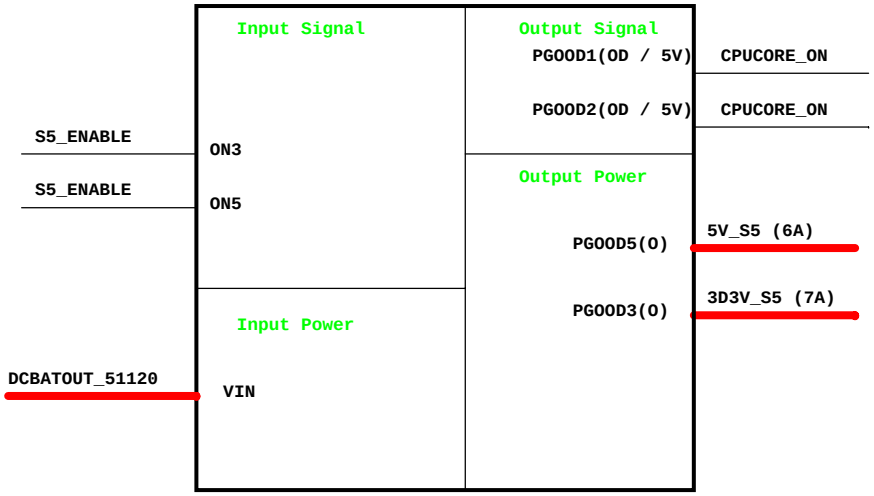
TPS51100

1D25V_S0

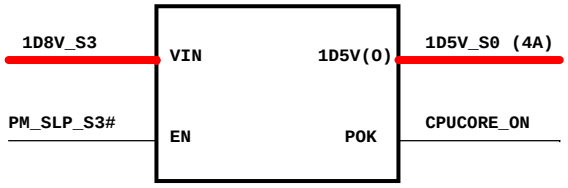


APL5913

TPS51120
5V/3D3V

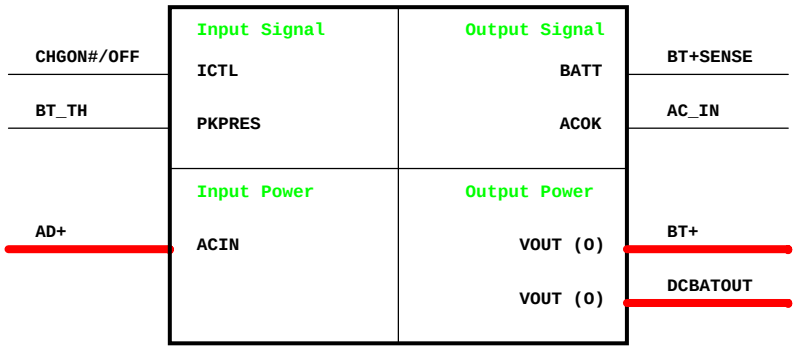


1D5V_S0



APL5915

Charger MAX8731



ICS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

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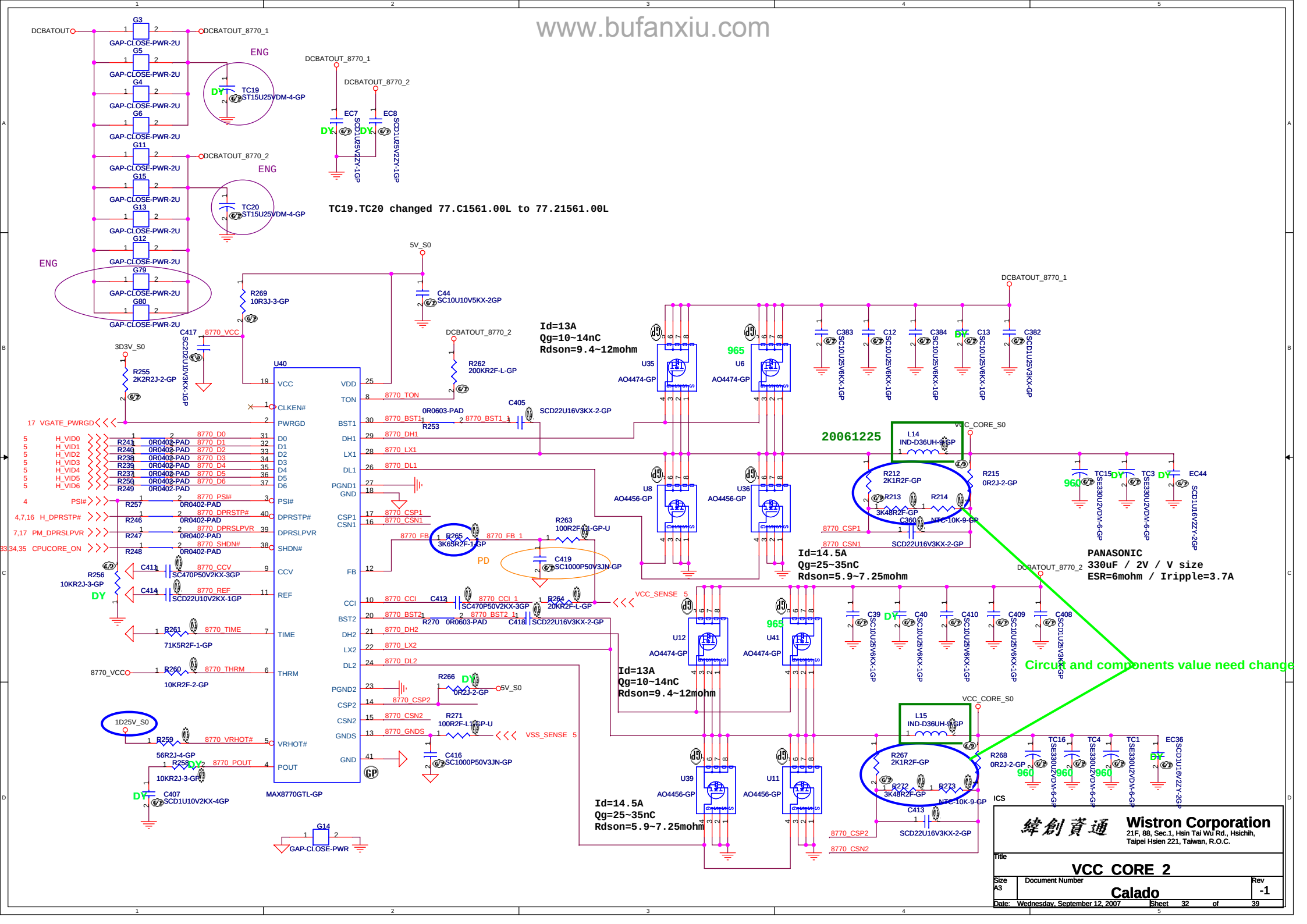

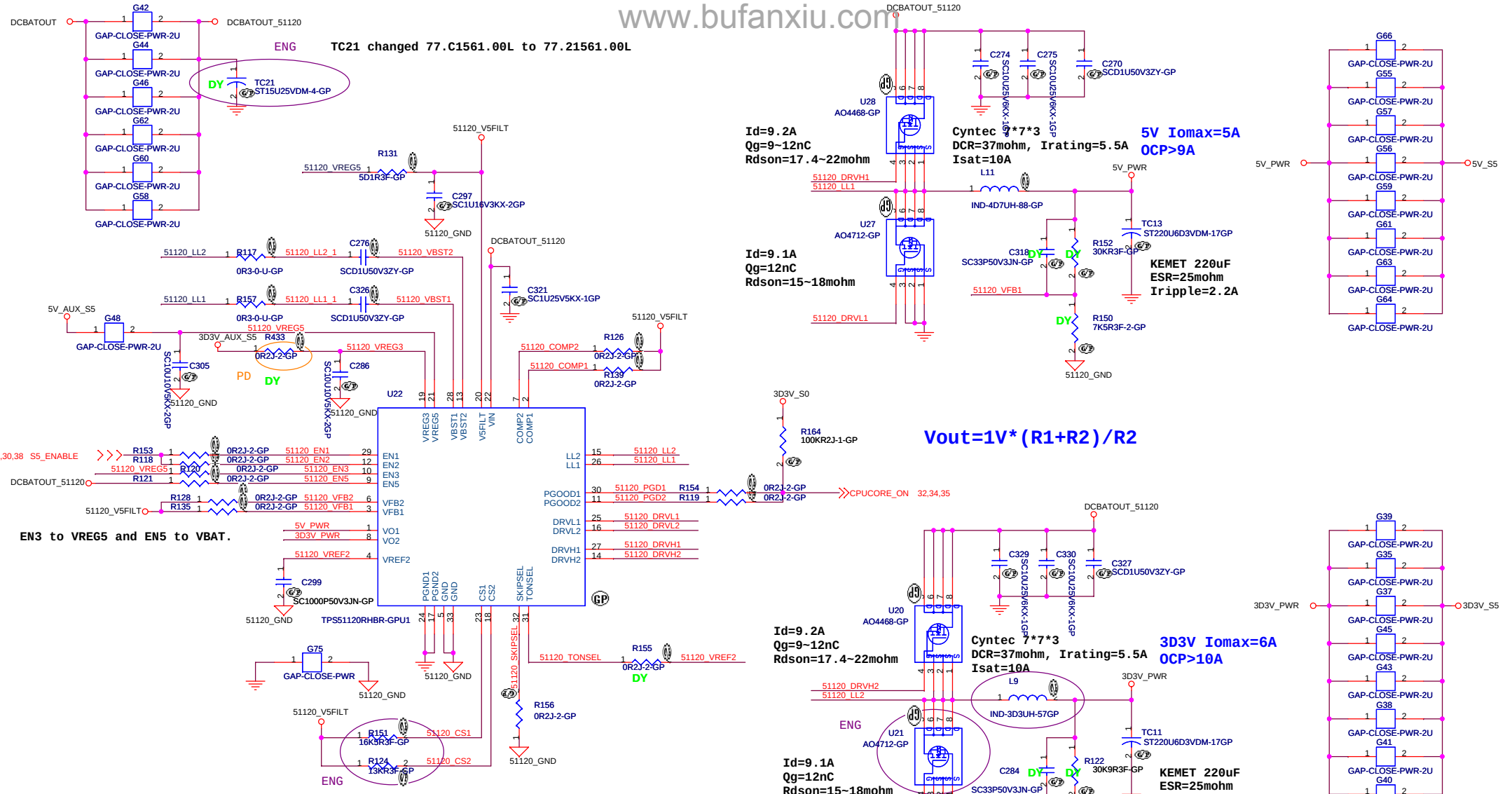

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swither ON**	Switcher ON
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Core Design>

緯創資通 **Wistron Corporation**
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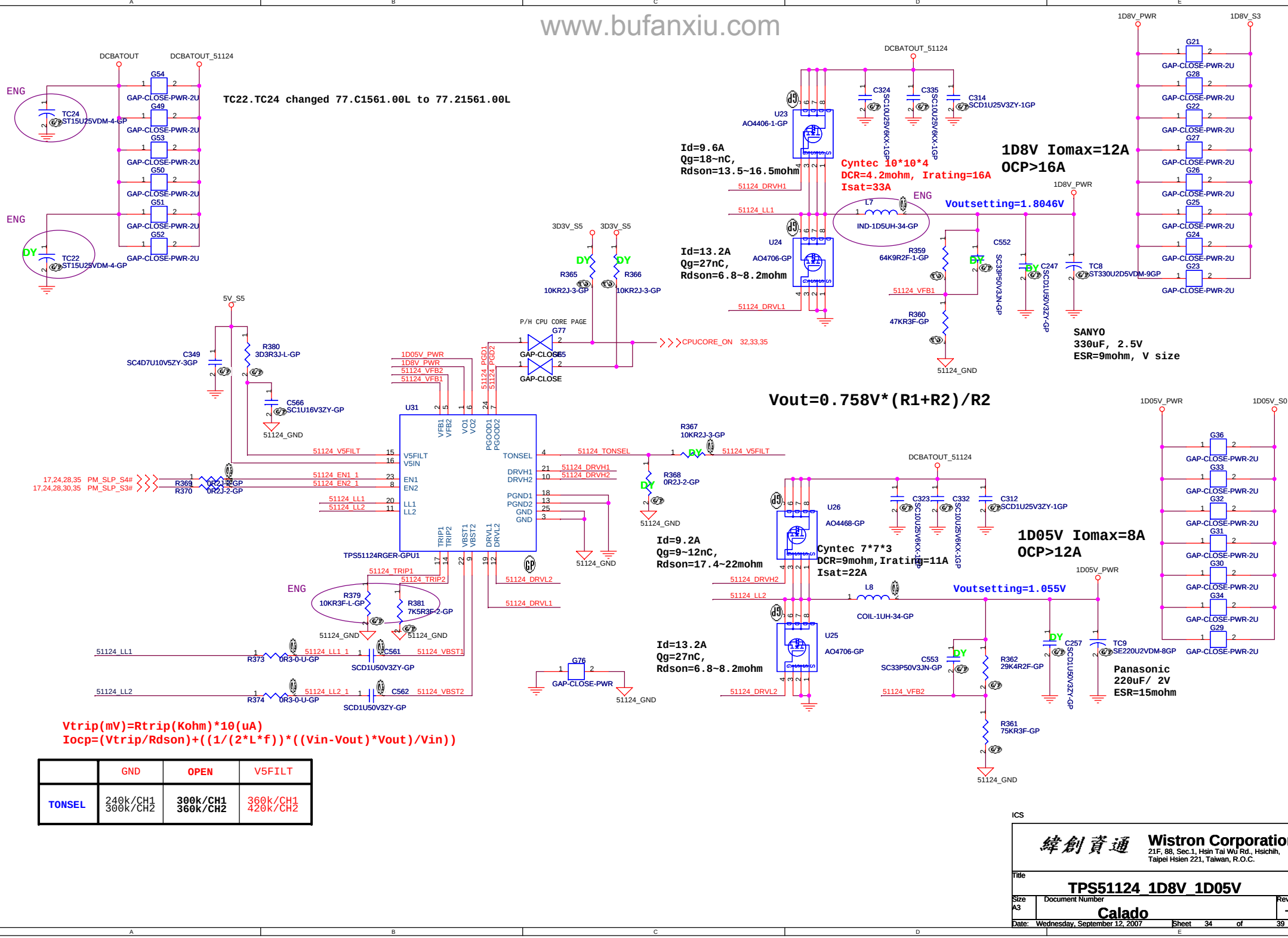
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51120_5V_3D3V**

Size: A3 | Document Number: **Calado** | Rev: -1

Date: Wednesday, September 12, 2007 | Sheet 33 of 39



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

ICS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D8V_1D05V

Size: A3 | Document Number: Calado | Rev: -1

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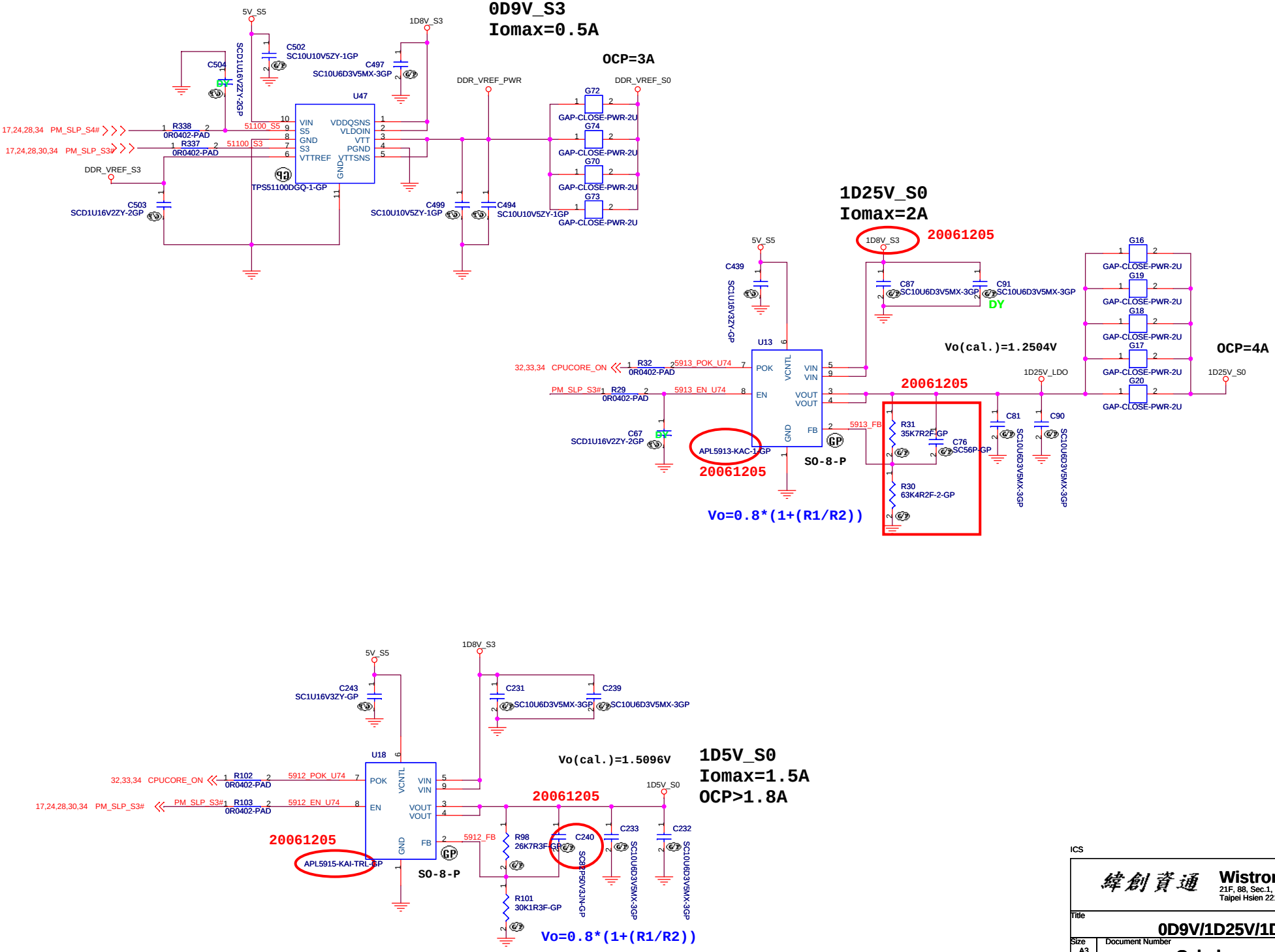

ICS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **0D9V/1D25V/1D5V**

Size	Document Number	Rev
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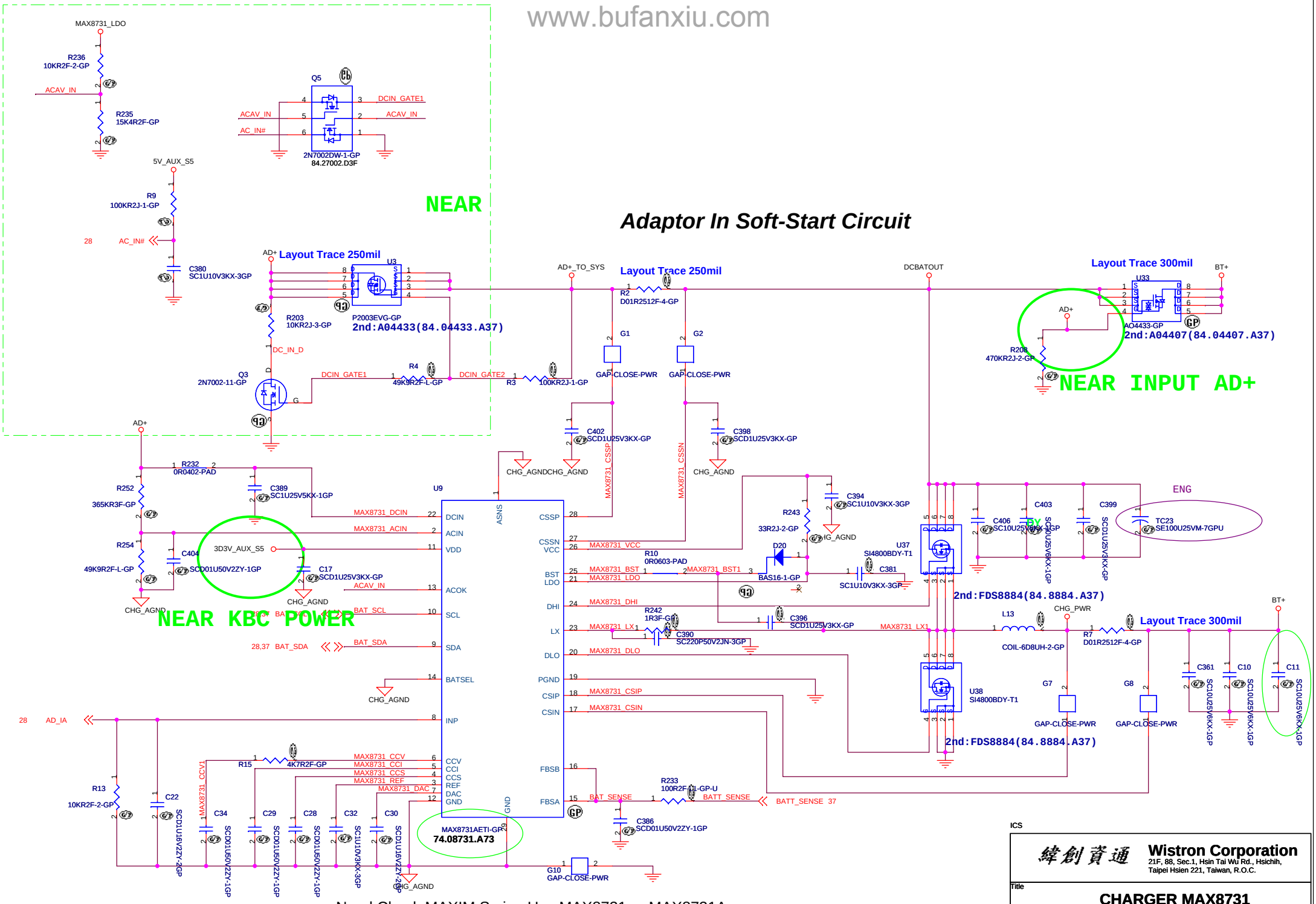
Date: Wednesday, September 12, 2007 Sheet 35 of 39

Adaptor In Soft-Start Circuit



Need Check MAXIM Sming Use MAX8731 or MAX8731A

ICS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER MAX8731**

Size	Document Number	Rev
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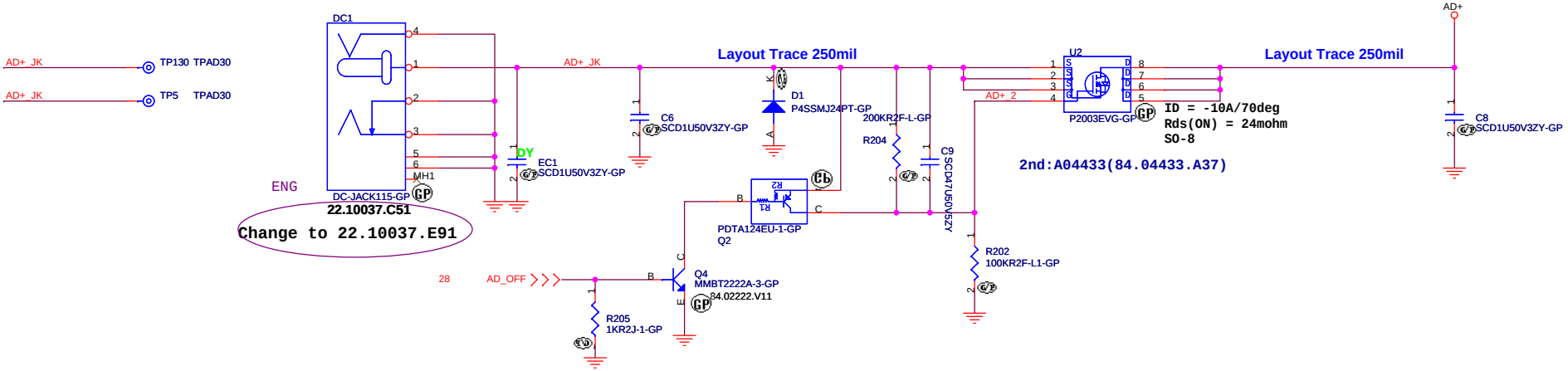
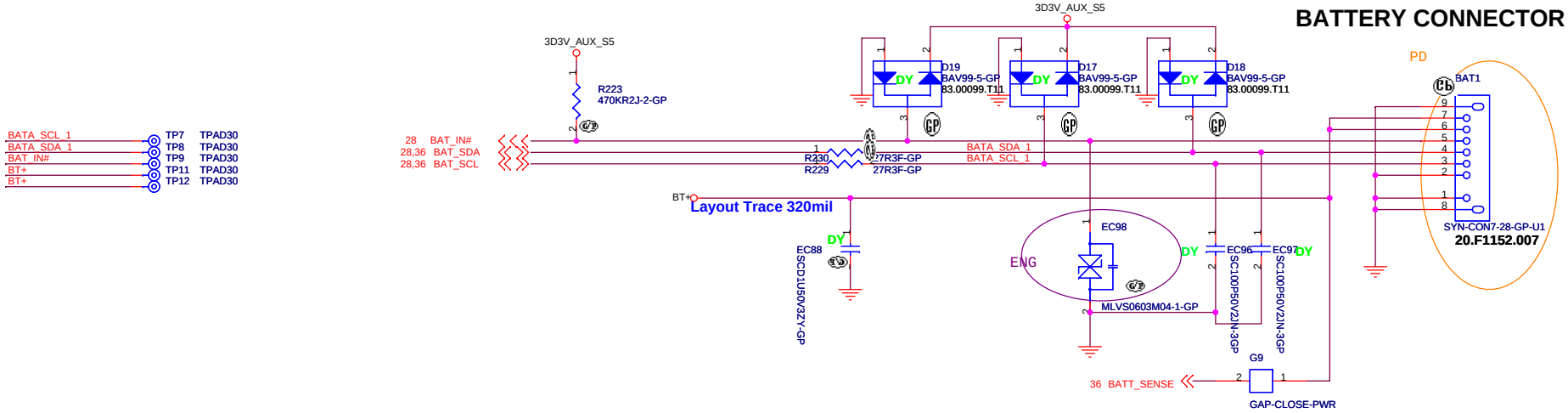
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



ICS

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

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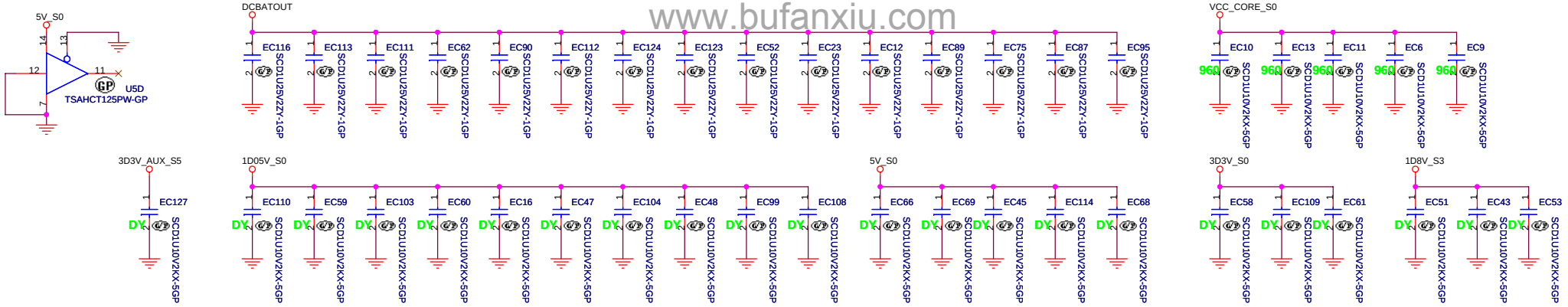

ENG

PD

FAN CONN

20	FAN1_VCC	FAN1_VCC	TP33	TPAD30
20	FAN1_FG1	FAN1_FG1	TP39	TPAD30
20,28,30	PURE_HW_SHUTDOWN#	PURE_HW_SHUTDOWN#	TP82	TPAD30

Audio Connector

26,27	LINEOUT_JD#	LINEOUT_JD#	TP156	TPAD30
27	SPKR_R+1	SPKR_R+1	TP166	TPAD30
27	SPKR_L+1	SPKR_L+1	TP164	TPAD30
26,27	MIC_JD#	MIC_JD#	TP157	TPAD30
26,27	AUD_MICIN_R	AUD_MICIN_R	TP167	TPAD30
26,27	AUD_MICIN_L	AUD_MICIN_L	TP168	TPAD30

Internal Speaker

27	SPKR_L-	SPKR_L-	TP124	TPAD30
27	SPKR_L+	SPKR_L+	TP126	TPAD30
27	SPKR_R-	SPKR_R-	TP127	TPAD30
27	SPKR_R+	SPKR_R+	TP128	TPAD30

Internal KeyBoard CONN

Test Point

28,29	KROW[1..8]	KROW[1..8]		
28,29	KCOL[1..16]	KCOL[1..16]		
		KCOL1	TP45	TPAD30
		KCOL2	TP41	TPAD30
		KCOL3	TP40	TPAD30
		KCOL4	TP38	TPAD30
		KCOL5	TP36	TPAD30
		KCOL6	TP34	TPAD30
		KCOL7	TP32	TPAD30
		KCOL8	TP31	TPAD30
		KCOL9	TP28	TPAD30
		KCOL10	TP26	TPAD30
		KCOL11	TP22	TPAD30
		KCOL12	TP21	TPAD30
		KCOL13	TP19	TPAD30
		KCOL14	TP18	TPAD30
		KCOL15	TP16	TPAD30
		KCOL16	TP17	TPAD30
		KROW1	TP56	TPAD30
		KROW2	TP55	TPAD30
		KROW3	TP52	TPAD30
		KROW4	TP51	TPAD30
		KROW5	TP50	TPAD30
		KROW6	TP49	TPAD30
		KROW7	TP48	TPAD30
		KROW8	TP46	TPAD30

TRING CONN

Test Point

23	TIP_C	TIP_C	TP2	TPAD30
23	RING_C	RING_C	TP3	TPAD30

Touch Pad CONN

Test Point near TPAD1

		5V_S0	TP10	TPAD30
29	TP_DATA	TP_DATA	TP54	TPAD30
29	TP_CLK	TP_CLK	TP53	TPAD30
29	TP_RIGHT	TP_RIGHT	TP57	TPAD30
29	TP_LEFT	TP_LEFT	TP58	TPAD30

USB ZIF CONN

Test Point

	5V_S5		TP79	TPAD30
	5V_S5		TP6	TPAD30
17,21	USBPN0	USBPN0	TP59	TPAD30
17,21	USBPP0	USBPP0	TP60	TPAD30
17,21	USBPN2	USBPN2	TP138	TPAD30
17,21	USBPP2	USBPP2	TP137	TPAD30
17,21	USBPN4	USBPN4	TP101	TPAD30
17,21	USBPP4	USBPP4	TP103	TPAD30
17,21	USB_OC#4	USB_OC#4	TP108	TPAD30
21,28	USB_PWR_EN#	USB_PWR_EN#	TP80	TPAD30

Check test point

	3D3V_S0		TP4	TPAD30
	3D3V_AUX_S5		TP13	TPAD30
	3D3V_S5		TP15	TPAD30
	5V_S5		TP125	TPAD30
17,28	PM_PWRBTN#		TP140	TPAD30
4,16,30	H_PWRGD		TP85	TPAD30
28,30,33	S5_ENABLE		TP139	TPAD30
4,6	H_CPURST#		TP27	TPAD30

CPU

H5 HOLE, H6 HOLE, H8 HOLE

34.42Y01.011

NB

H7 HOLE, H9 HOLE

34.42Y01.011

MDC

H10 HOLE, H11 HOLE

34.42Y01.011

MINI CARD

H1 HOLE, H2 HOLE

34.4G502.001

H3 HOLE, H4 HOLE, H12 HOLE, H13 HOLE, H14 HOLE, H15 HOLE, H16 HOLE, H17 HOLE, H18 HOLE, H19 HOLE, H20 HOLE, H21 HOLE, H22 HOLE, H23 HOLE

GND3 SPRING-23-GP (DY)

GND6 SPRING-6

GND7 SPRING-6

34.13B01.001

GND4 SPRING-16

GND5 SPRING-16

34.43E28.001

GND8 SPRING-9-GP

GND9 SPRING-9-GP

GND10 SPRING-9-GP

GND11 SPRING-9-GP

GND12 SPRING-9-GP

GND13 SPRING-9-GP

34.49U23.001

Test Point放在Dimm Door打開可量測處

ICS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

Size | Document Number: Calado | Rev: -1

Date: Thursday, September 13, 2007 | Sheet 38 of 39

SA to SB
1.TC6 change to 900U
2.modify U42(change to G913 300mA) add R417 for TV CRT ripple.
3.add Q27 for BT LED signal
4.change LED1 to 83.01221.I70(right angle)
5.add U55 BLON_5V for LED panel
6.change U1 to 74.04280.C9P for source request
7.add polyswitch F3 for safety.
8.C338 C339 C341 C340 change to 0402 size for SATA signal.
9.FAN1 change to 20.F1000.003 for ME.
10.USB1 swap pin3 pin4 signal.
11.USB2 USB3 change to 22.10218.R31 for ME.
12.add polyswitch F4 F5 for safety.
13.change U4 U45 to 74.09711.B7F ,U56 U57 74.05250.C7F for source request.
14.R20 change to 1.21K for IEEE.
15.C56 change to 12P for Oscillation report.
16.U53 change to 74.09711.A7F for source request.
17.NEW1 change to 20.F07890.026.SK1 change to 21.H0153.001 for ME
18.add R421 LED4 for CardReader test.
19.C237 C229 change to 27P for Oscillation report.
20.R350 change to 4.99K for jack detection.
21.R363 R364 change to 18K.R404 R405 change to 56 ohm for audio report.
22.add AUD_AGND.L24 for audio niose.
23.C575 C577 change to 2700p Cut frequency at 500HZ
24.add BT_LED to KBC GPIO50.
25.add TC19 TC20 TC21 TC22 TC23 TC24 for acoustic noise.
26.C419 change to 1000p for power team.
27.U21 change to 84.04712.037.L9 change to 68.3R310.20A for power team.
28.R151 change to 16.5K.R124 change to 13K for OCP.
29.L7 change to 68.1R510.10J for power team.
30.R379 change to 10K.R381 change to 7.5K for OCP.
31,BAT1 change to 20.80977.007 for ME.
32.EC98 add 69.80007.031 for EC damaged.
33.R402 change to 10K.R397 DY for planar ID.
34.ODD1 change to 20.80967.050 for ME.
35.add G79.G80 for power.
36.R385.R386.R388.R387 change for Gain.R395.R407 change to 56K.
37.add EC6.EC9.EC10.EC11.EC13 to 960 for EMI.
38.add EC41.EC42.EC49.EC50.EC127 for EMI.
39.add R423.R422 for EMI.
40.add RN34.RN35.RN36 for EMI.
41.remove Golden finger
42.swap Touchpad pin define.
43.change L1 L2 to 68.00084.371.
44.change DC1 to 22.10037.E91 for ME.
45.change TVOUT1 to 22.10021.F41 for ME.
SB to -1
1.add AFTE test point for power board Conn.
2.add R432.C583 change G47 to R433 for 3D3V_AUX_S5 power option
3.change to 0 ohm pad for R45.R41.R216.R391.R183.R184.R14.R162.
R78.R79.R74.R87.R73.R77.R390.R21.R194.R187
4.change SPKR1 to 20.D0197.104 for ME.
5.change TRING1 to 21.E0024.102 for ME.
6.remove D7.D8.D9 for EMI.
7.add EC116.EC113.EC111.EC62.EC90.EC112.EC124.EC123.EC52.EC23.EC12.EC89.EC75.EC87.EC95.
8.change R422.R423 to 33 ohm.add EC71.EC72 to 33P for EMI.
9.add EC128.EC129 for EMI.
10.change c419 to 78.10234.1BL for source OBSOLETED.
11.change LEFT1.LEFT2.RIGHT1 to 62.40009.671 for ME.
12.change TVOUT1 to 22.10021.H61 for ME.
13.change BAT1 to 20.F1152.007 for ME.
14.add D26 for EMI.
15.change TC17 to 79.22710.3AL for USB droop test fial.
16.change TC2.EC84 to 5V_USB3_S0_1,change TC17.EC101 to5V_USB2_S0_1 for UPT2 fail.
17.add GND6.GND7.GND8.GND9.GND10.GND11.GND12.GND13 fot EMI.
18.change CRT1 to 20.20378.015 for ME.
19.del GND1.GND2.

ICS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change List

Size | Document Number: Calado | Rev: -1

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