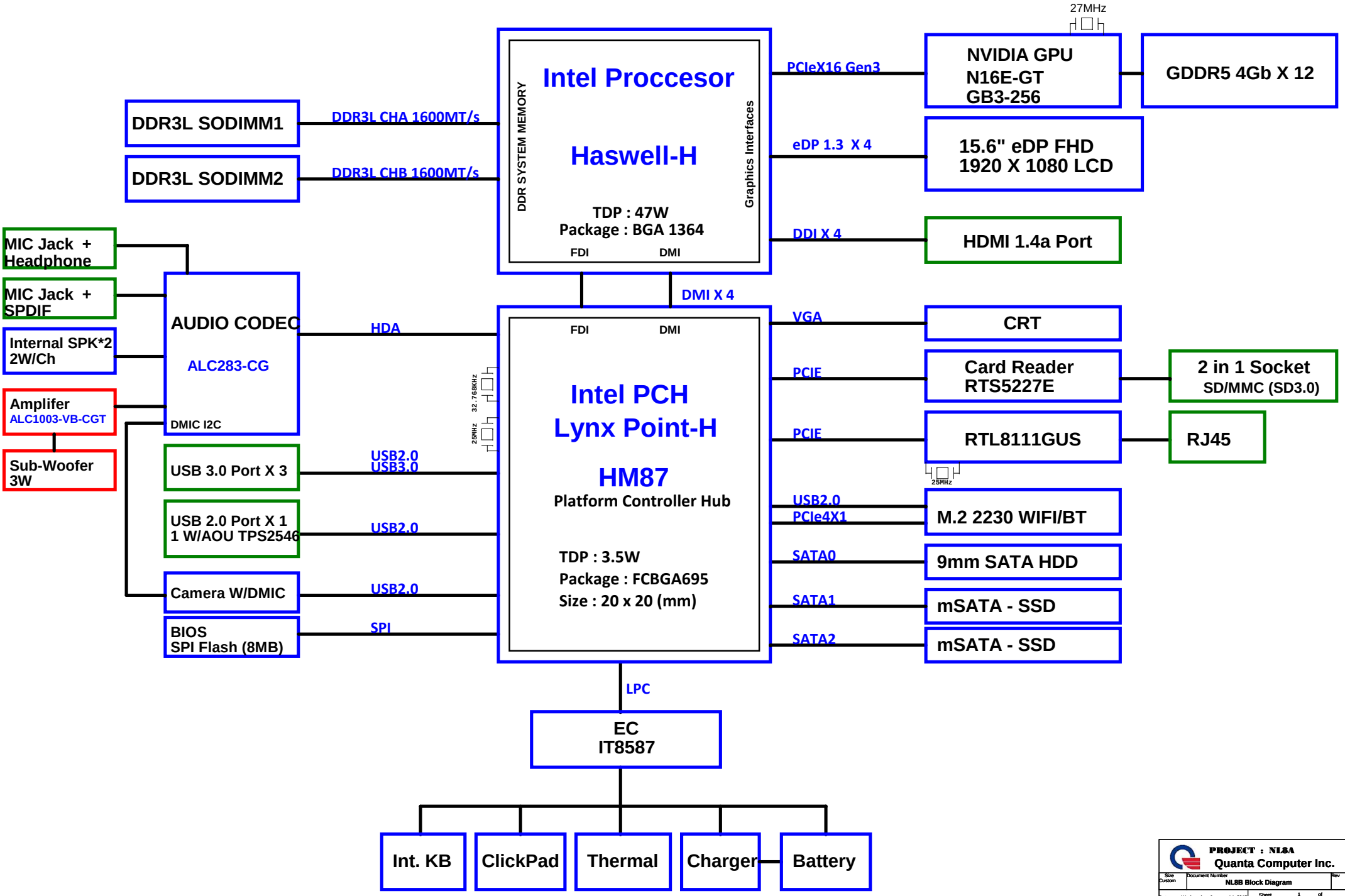
NL8B Block Diagram

01



PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NL8B Block Diagram	1A
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(4,5) VCCIOA_OUT
(4,5,37) VCCIO_OUT
(7,8,9,10,11,13,14,15,16,17,18,19,20,22,25,26,27,28,30,38,39,41,43,47) +3V
(5,10,11,35,40,41) +1.05V
(5,13,14,34,41) +1.35VSUS
(7,8,9,10,11,20,23,28,30,33,36,37,39,40,45,51) +3V_S5

Haswell Processor (DMI,PEG,FDI)

PEG_RCOMP
Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS

VCCIOA_OUT
R110 24.9/F_4
AH6 PEG_RCOMP

U34A HASWELL_BGA_E

DMI_RXN0 AB2
DMI_RXN1 AB3
DMI_RXN2 AC3
DMI_RXN3 AC1
DMI_RXP0 AB1
DMI_RXP1 AB4
DMI_RXP2 AC4
DMI_RXP3 AC2
DMI_TXN0 AF2
DMI_TXN1 AF4
DMI_TXN2 AG4
DMI_TXN3 AG2
DMI_TXP0 AF1
DMI_TXP1 AF3
DMI_TXP2 AG3
DMI_TXP3 AG1

(7) DMI_TXN0
(7) DMI_TXN1
(7) DMI_TXN2
(7) DMI_TXN3
(7) DMI_TXP0
(7) DMI_TXP1
(7) DMI_TXP2
(7) DMI_TXP3
(7) DMI_RXN0
(7) DMI_RXN1
(7) DMI_RXN2
(7) DMI_RXN3
(7) DMI_RXP0
(7) DMI_RXP1
(7) DMI_RXP2
(7) DMI_RXP3

(7) FDI_CSYNC — R75 *0_4_S — FDI_CSYNC_R — F11
(7) FDI_INT — F12
FDI_CSYNC
DISP_INT

FDI_CSYNC & FDI_INT
Trace length < 10000 Mils
Impendance = 50 ohm

PEG_RCOMP
PEG_RXN0 E10
PEG_RXN1 C10
PEG_RXN2 B10
PEG_RXN3 E9
PEG_RXN4 D9
PEG_RXN5 B9
PEG_RXN6 L5
PEG_RXN7 L2
PEG_RXN8 M4
PEG_RXN9 L4
PEG_RXN10 M2
PEG_RXN11 V5
PEG_RXN12 V4
PEG_RXN13 V1
PEG_RXN14 Y3
PEG_RXN15 Y2
PEG_RXP0 F10
PEG_RXP1 D10
PEG_RXP2 A10
PEG_RXP3 F9
PEG_RXP4 C9
PEG_RXP5 A9
PEG_RXP6 M5
PEG_RXP7 L1
PEG_RXP8 M3
PEG_RXP9 L3
PEG_RXP10 M1
PEG_RXP11 Y5
PEG_RXP12 V3
PEG_RXP13 V2
PEG_RXP14 Y4
PEG_RXP15 Y1

PEG_RX#15 (43)
PEG_RX#14 (43)
PEG_RX#13 (43)
PEG_RX#12 (43)
PEG_RX#11 (43)
PEG_RX#10 (43)
PEG_RX#9 (43)
PEG_RX#8 (43)
PEG_RX#7 (43)
PEG_RX#6 (43)
PEG_RX#5 (43)
PEG_RX#4 (43)
PEG_RX#3 (43)
PEG_RX#2 (43)
PEG_RX#1 (43)
PEG_RX#0 (43)
PEG_RX15 (43)
PEG_RX14 (43)
PEG_RX13 (43)
PEG_RX12 (43)
PEG_RX11 (43)
PEG_RX10 (43)
PEG_RX9 (43)
PEG_RX8 (43)
PEG_RX7 (43)
PEG_RX6 (43)
PEG_RX5 (43)
PEG_RX4 (43)
PEG_RX3 (43)
PEG_RX2 (43)
PEG_RX1 (43)
PEG_RX0 (43)

PEG_TXN0 B6 — C_PEG_TX#15 C554
PEG_TXN1 C5 — C_PEG_TX#14 C553
PEG_TXN2 E6 — C_PEG_TX#13 C565
PEG_TXN3 D4 — C_PEG_TX#12 C566
PEG_TXN4 G4 — C_PEG_TX#11 C569
PEG_TXN5 E3 — C_PEG_TX#10 C572
PEG_TXN6 J5 — C_PEG_TX#9 C573
PEG_TXN7 G3 — C_PEG_TX#8 C576
PEG_TXN8 J3 — C_PEG_TX#7 C581
PEG_TXN9 J2 — C_PEG_TX#6 C583
PEG_TXN10 T6 — C_PEG_TX#5 C584
PEG_TXN11 R6 — C_PEG_TX#4 C587
PEG_TXN12 R2 — C_PEG_TX#3 C589
PEG_TXN13 R4 — C_PEG_TX#2 C590
PEG_TXN14 T4 — C_PEG_TX#1 C593
PEG_TXN15 T1 — C_PEG_TX#0 C594
PEG_TXP0 C6 — C_PEG_TX15 C555
PEG_TXP1 B5 — C_PEG_TX14 C561
PEG_TXP2 D6 — C_PEG_TX13 C563
PEG_TXP3 E4 — C_PEG_TX12 C568
PEG_TXP4 G5 — C_PEG_TX11 C570
PEG_TXP5 E2 — C_PEG_TX10 C571
PEG_TXP6 J6 — C_PEG_TX9 C575
PEG_TXP7 G2 — C_PEG_TX8 C578
PEG_TXP8 J4 — C_PEG_TX7 C579
PEG_TXP9 J1 — C_PEG_TX6 C582
PEG_TXP10 R5 — C_PEG_TX5 C585
PEG_TXP11 R1 — C_PEG_TX4 C586
PEG_TXP12 R3 — C_PEG_TX3 C588
PEG_TXP13 T3 — C_PEG_TX2 C591
PEG_TXP14 T2 — C_PEG_TX1 C592
PEG_TXP15 — C_PEG_TX0 C595

0.22U/10V_4

PEG_TX#15 (43)
PEG_TX#14 (43)
PEG_TX#13 (43)
PEG_TX#12 (43)
PEG_TX#11 (43)
PEG_TX#10 (43)
PEG_TX#9 (43)
PEG_TX#8 (43)
PEG_TX#7 (43)
PEG_TX#6 (43)
PEG_TX#5 (43)
PEG_TX#4 (43)
PEG_TX#3 (43)
PEG_TX#2 (43)
PEG_TX#1 (43)
PEG_TX#0 (43)
PEG_TX15 (43)
PEG_TX14 (43)
PEG_TX13 (43)
PEG_TX12 (43)
PEG_TX11 (43)
PEG_TX10 (43)
PEG_TX9 (43)
PEG_TX8 (43)
PEG_TX7 (43)
PEG_TX6 (43)
PEG_TX5 (43)
PEG_TX4 (43)
PEG_TX3 (43)
PEG_TX2 (43)
PEG_TX1 (43)
PEG_TX0 (43)

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Haswell Processor (CLK,MISC,JTAG)

+1.05V
R421 *100/F_4

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

(10,27) H_PECI
(27,30,37) H_PROCHOT#
PM_THRMTRIP#
H_PROCHOT# R62 56/F_4 H_PROCHOT#_R
Close to CPU.

TP18 PROC_DETECT# C51
TP23 CATERR# G50
G51

U34B HASWELL_BGA_E
MISC
PROC_DETECT
CATERR
PECI
PROCHOT
THERMTRIP
THERMAL
PWR
JTAG
CLOCK
DDR3

PM_SYNC (50ohm)
Trace Length: 1~11.25 inches

(7) PM_SYNC — R60 *0_4_S — PM_SYNC_R — D52
(10) H_PWRGOOD — R53 *0_4_S — H_PWRGOOD_R — F50
PM_DRAM_PWRGD_R AP48
(10) CPU_PLTRST# — R424 *0_4_S — CPU_RST#_R — L54

PM_SYNC
PWRGOOD
SM_DRAMPWROK
PLTRSTIN
DPLL_REF_CLKN
DPLL_REF_CLKP
SSC_DPLL_REF_CLKN
SSC_DPLL_REF_CLKP
BCLKN
BCLKP

(9) CLK_DPLL_NSCLKN — R112 *0_4_S — CLK_DPLL_NSCLKN_R AC6
(9) CLK_DPLL_NSCLKP — R115 *0_4_S — CLK_DPLL_NSCLKP_R AE6
(9) CLK_DPLL_SSCLKN — R101 *0_4_S — CLK_DPLL_SSCLKN_R V6
(9) CLK_DPLL_SSCLKP — R106 *0_4_S — CLK_DPLL_SSCLKP_R Y6
(9) CLK_CPU_BCLKN — R103 *0_4_S — CLK_CPU_BCLKN_R AB6
(9) CLK_CPU_BCLKP — R99 *0_4_S — CLK_CPU_BCLKP_R AA6

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

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SM_RCOMP[0:2]
Trace length < 500 mils
Trace width = 12~15 mils
Trace spacing = 20 mils

SM_RCOMP0 BB51 — R138 100/F_4
SM_RCOMP1 BB53 — R136 75/F_4
SM_RCOMP2 BB52 — R137 100/F_4
SM_DRAMRST BE51 CPU_DRAMRST#

TCK,TMS
Trace Length < 9000mils

XDP_PRDY# N53 — TP31
XDP_PREQ# N52
XDP_TCLK N54
XDP_TMS M51
XDP_TRST# M53
XDP_TDI M49
XDP_TDO F53
XDP_DBRST# (7)

BPM#0 R51 XDP_BPM#0 — TP42
BPM#1 R50 XDP_BPM#1 — TP41
BPM#2 P49 XDP_BPM#2 — TP38
BPM#3 N50 XDP_BPM#3 — TP22
BPM#4 R49 XDP_BPM#4 — TP44
BPM#5 P53 XDP_BPM#5 — TP82
BPM#6 U51 XDP_BPM#6 — TP40
BPM#7 P51 XDP_BPM#7 — TP35

BPM#[0:7]
Trace Length 1~6 inches
Length match < 300 mils

SM_DRAMPWROK Processor Input.

To change the resistor values in the DRAMPWROK logic to reduce the leakage on VDDPWRGOOD

+3V_S5
PM_DRAM_PWRGD_C (50ohm)
Trace Length: < 1 inches
R168 100K_4
R169 100K_4
C258 0.1U/10V_4
U9
*74AHC1G09GW
+1.35VSUS
DG 498556 -> 1.8K
R160 1.8K/F_4
(34) DDR_VR_PWRGD
R167 *0_4_S
PM_DRAM_PWRGD_C
R150 *0_4_S
R162 *0_4_S
PM_DRAM_PWRGD_R
PM_DRAM_PWRGD (7)
C260 0.047U/10V_4
D4 *RB500V-40
R157 3.3K/F_4
C245 *0.047U/10V_4
DG 498556 -> 3.3K

PM_DRAM_PWRGD_R (50ohm)
Trace Length: 0.5~1 inches

PM_DRAM_PWRGD (50ohm)
Trace Length: 2~7 inches

PU/PD of CPU

VCCIO_OUT
H_PROCHOT# R54 62_4
H_PWRGOOD_R R66 10K_4
VCCIO_OUT
CLK_DPLL_SSCLKP_R R105 *10K_4
CLK_DPLL_SSCLKN_R R100 *10K_4

Reserved For buffer reset of PLTRSRIN#

+3V
+1.05V
(7,20,23,25,26,43) PLTRST#
U33
NC VCC
IN
GND OUT
*74LVC1G07GW
C580 *0.01U/10V_4
R422 *1K_4
R425 *43_4
CPU_PLTRST#_Q
CPU_RST#_R
R423 *20K_4

SM_DRAMRST# Topology

DDR3_DRAMRST#_R (50ohm)
Trace Length < 5 inches

+1.35VSUS
R451 *1K_4
CPU_DRAMRST#
R450 *0_4_S
DDR3_DRAMRST# (13,14)
R449 *4.99K/F_4

XDP PU/PD

XDP_TDO R84 51_4
XDP_TMS R86 *51_4
XDP_TDI R90 *51_4
XDP_PREQ# R88 *51_4
+1.05V
XDP_TCLK R428 51_4
XDP_TRST# R427 51_4

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Quanta Computer Inc.

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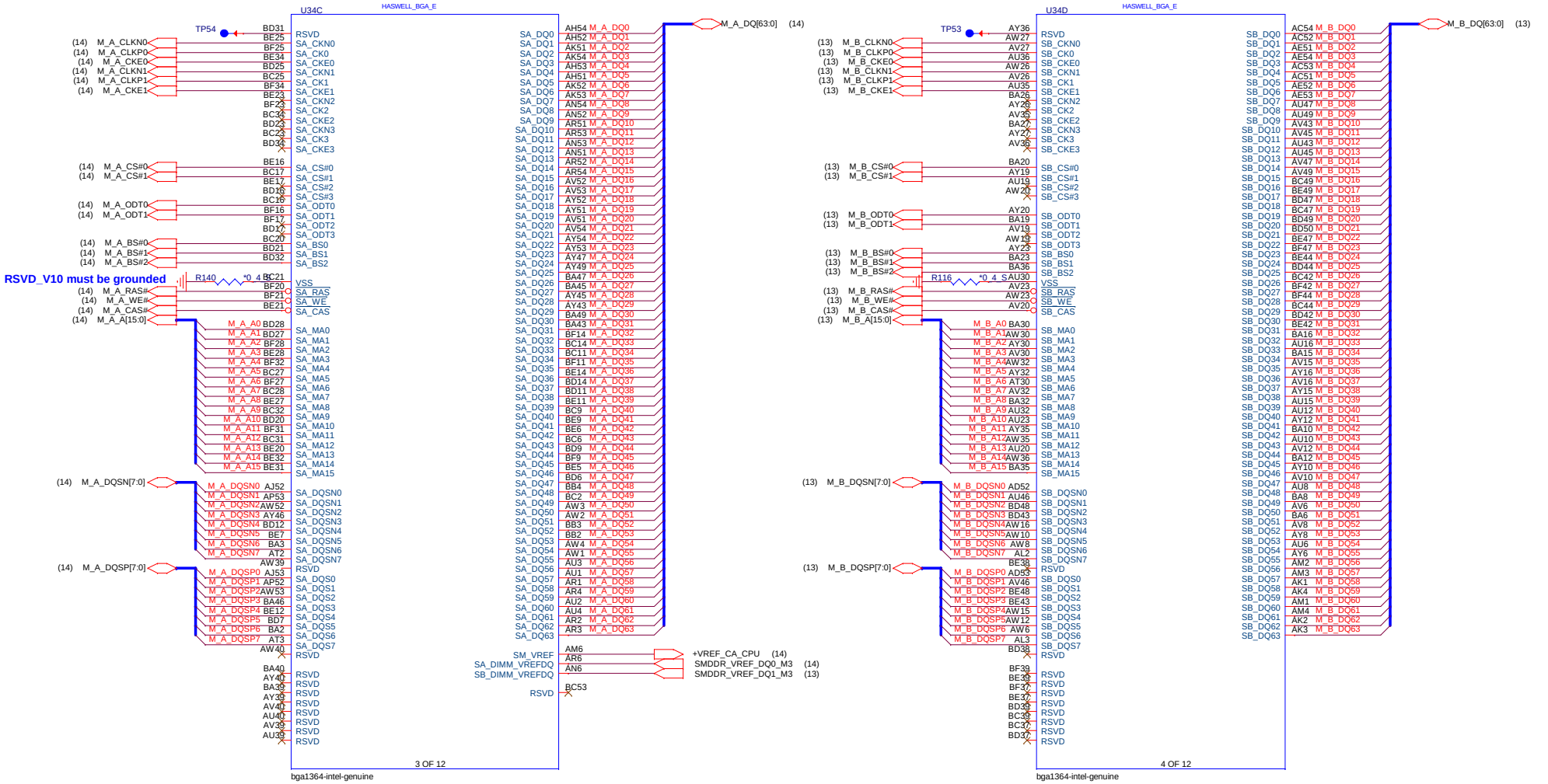
Haswell Processor (DDR3)



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Quanta Computer Inc.			
Size: Custom	Document Number: Haswell 2/5 (DDR3 I/F)		Rev: 3B
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Haswell Processor (DDI,eDP,FDI)

04

(2,5) VCCIOA_OUT
(2,5,37) VCCIO_OUT

U34J HASWELL_BGA_E

HDMI

(17) HDMI_TX2- C25 DDIB_TXN0
(17) HDMI_TX2+ D25 DDIB_TXP0
(17) HDMI_TX1- A25 DDIB_TXN1
(17) HDMI_TX1+ B25 DDIB_TXP1
(17) HDMI_TX0- C24 DDIB_TXN2
(17) HDMI_TX0+ D24 DDIB_TXP2
(17) HDMI_CLK- A24 DDIB_TXN3
(17) HDMI_CLK+ B24 DDIB_TXP3

C21 DDIC_TXN0
D21 DDIC_TXP0
A21 DDIC_TXN1
B21 DDIC_TXP1
C20 DDIC_TXN2
D20 DDIC_TXP2
A20 DDIC_TXN3
B20 DDIC_TXP3

C16 DDID_TXN2
D16 DDID_TXP2
A16 DDID_TXN3
B16 DDID_TXP3

C17 DDID_TXN0
D17 DDID_TXP0
A17 DDID_TXN1
B17 DDID_TXP1

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EDP_AUXN F15 EDP_AUXN (15)
EDP_AUXP F14 EDP_AUXP (15)
EDP_HPD E14 EDP_HPD_Q

EDP_TXN0 C14 EDP_TXN0 (15)
EDP_TXN1 A12 EDP_TXN1 (15)
EDP_TXP0 D14 EDP_TXP0 (15)
EDP_TXP1 B12 EDP_TXP1 (15)

EDP_RCOMP AG6 EDP_RCOMP R108 24.9/F_4 VCCIOA_OUT
EDP_DISP_UTIL E12

FDI_TXN0 C12 FDI_TXN0 (7)
FDI_TXP0 D12 FDI_TXP0 (7)
FDI_TXN1 A14 FDI_TXN1 (7)
FDI_TXP1 B14 FDI_TXP1 (7)

eDP_RCOMP
Trace length < 100 mils
Trace width = 20 mils
Trace spacing = 25 mils

VCCIO_OUT
R64 10K_4
EDP_HPD_Q
3
2
1
Q3 2N7002K
EDP_HPD (15)
R50 100K_4

PROJECT : NL8A
Quanta Computer Inc.

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Haswell Processor (POWER)

(2,13,14,34,41) +1.35VSUS
(6,37,41) +VCC_CORE
(2,4,37) VCCIO_OUT
(2,10,11,35,40,41) +1.05V
(2,4) VCCIOA_OUT

05

+1.35VSUS
4.2A

C145 22U/6.3V_6, C143 22U/6.3V_6, C141 *22U/6.3V_6, C140 *22U/6.3V_6, C138 *22U/6.3V_6, C147 *22U/6.3V_6
C137 *22U/6.3V_6, C144 *22U/6.3V_6, C142 *22U/6.3V_6, C139 *22U/6.3V_6, C146 *22U/6.3V_6
C215 10U/6.3V_6, C214 10U/6.3V_6, C223 *10U/6.3V_6, C221 *10U/6.3V_6, C216 *10U/6.3V_6
C218 *10U/6.3V_6, C217 *10U/6.3V_6, C226 *10U/6.3V_6, C220 *10U/6.3V_6, C219 *10U/6.3V_6

U34E HASWELL_BGA_E

J17	RSVD	
J21	RSVD	
J26	RSVD	
J31	RSVD	
AR29	VDDQ	
AR31	VDDQ	
AR33	VDDQ	
AT13	VDDQ	
AT19	VDDQ	
AT23	VDDQ	
AT27	VDDQ	
AT32	VDDQ	
AT36	VDDQ	
AV37	VDDQ	
AW22	VDDQ	
AW25	VDDQ	
AW29	VDDQ	
AW33	VDDQ	
AY18	VDDQ	
BB21	VDDQ	
BB22	VDDQ	
BB26	VDDQ	
BB27	VDDQ	
BB30	VDDQ	
BB31	VDDQ	
BB34	VDDQ	
BB36	VDDQ	
BD22	VDDQ	
BD26	VDDQ	
BD30	VDDQ	
BD33	VDDQ	
BE18	VDDQ	
BE22	VDDQ	
BE26	VDDQ	
BE30	VDDQ	
BE33	VDDQ	
AN31	RSVD	TP47
L6	VCC	+VCC_CORE
M6	VCC	
AN22	RSVD	TP50
AN18	RSVD	TP51
C50	VCC_SENSE	(37) VCC_SENSE
AH9	RSVD	
D51	VCCIO_OUT	300mA VCCIO_OUT
F17	FC_F17	300mA +1.05V VCCIOA_OUT
AK6	VCOMP_OUT	
AN33	RSVD	TP48
W9	RSVD	TP45
J12	RSVD	TP30
AR49	RSVD	TP52
J53	VIDALERT	H_CPU_SVIDART#
J52	VIDSCLK	H_CPU_SVIDCLK
J50	VIDSOUT	H_CPU_SVIDDAT
B51	VSS	
F19	PWR_DEBUG	TP10 PWR_DEBUG_R
E52	VSS	R65 *0_4_S
V49	RSVD_TP	TP43
U49	RSVD_TP	TP39
AM49	RSVD_TP	TP49
W49	RSVD_TP	TP46
V50	VSS	
AN49	VSS	
AJ49	VSS	
AC50	VSS	
AK49	VSS	
AJ50	VSS	
AP49	VSS	
AB50	VSS	
AP50	VSS	
AD50	VSS	
AM50	VSS	
A36	VCC	+VCC_CORE
A38	VCC	
A39	VCC	
A42	VCC	
A43	VCC	
A45	VCC	
A46	VCC	
A48	VCC	
AA46	VCC	
AA47	VCC	
AA8	VCC	
AA9	VCC	

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+VCC_CORE R68 100_4
(37) VCC_SENSE R56 *0_4_S VCC_SENSE_R
300mA VCCIO_OUT R47 *0_8_S +VCCIO_OUT_R
+1.05V
300mA VCCIOA_OUT R63 *0_8 +VCCIO_PCH_R
R113 *0_8_S +VCCIOA_OUT_R

B43	VCC	+VCC_CORE
B45	VCC	
B46	VCC	
B48	VCC	
C27	VCC	
C28	VCC	
C31	VCC	
C32	VCC	
C34	VCC	
C36	VCC	
C38	VCC	
C39	VCC	
C42	VCC	
C43	VCC	
C45	VCC	
C46	VCC	
C48	VCC	
D27	VCC	
D28	VCC	
D31	VCC	
D32	VCC	
D34	VCC	
D36	VCC	
D38	VCC	
D39	VCC	
D42	VCC	
D43	VCC	
D45	VCC	
D46	VCC	
D48	VCC	
E27	VCC	
E28	VCC	
E31	VCC	
E32	VCC	
E34	VCC	
E36	VCC	
E38	VCC	
E39	VCC	
E42	VCC	
E43	VCC	
E45	VCC	
E46	VCC	
E48	VCC	
F27	VCC	
F28	VCC	
F31	VCC	
F32	VCC	
F34	VCC	
F36	VCC	
F38	VCC	
F39	VCC	
F42	VCC	
F43	VCC	
F45	VCC	
F46	VCC	
F48	VCC	
G27	VCC	
G29	VCC	
G31	VCC	
G32	VCC	
G34	VCC	
G36	VCC	
G38	VCC	
G39	VCC	
G42	VCC	
G43	VCC	
G45	VCC	
G46	VCC	
G48	VCC	
H11	VCC	
H12	VCC	
H13	VCC	
H14	VCC	
H16	VCC	
H17	VCC	
H18	VCC	
H19	VCC	
H20	VCC	
H21	VCC	
H23	VCC	
H24	VCC	
H25	VCC	
H26	VCC	
H27	VCC	
H29	VCC	
D5	FC_D5	
D3	FC_D3	

VCC_CORE 85A

C80 22U/6.3V_6, C79 22U/6.3V_6, C78 22U/6.3V_6, C77 22U/6.3V_6, C89 22U/6.3V_6, C63 22U/6.3V_6
C558 22U/6.3V_6, C86 22U/6.3V_6, C82 22U/6.3V_6, C74 22U/6.3V_6, C68 22U/6.3V_6, C69 22U/6.3V_6
C52 22U/6.3V_6, C557 22U/6.3V_6, C90 22U/6.3V_6, C54 22U/6.3V_6, C67 22U/6.3V_6, C85 22U/6.3V_6
C53 22U/6.3V_6, C55 10U/6.3V_6, C81 10U/6.3V_6, C556 10U/6.3V_6, C559 10U/6.3V_6, C73 10U/6.3V_6
C66 10U/6.3V_6, C72 10U/6.3V_6, C71 10U/6.3V_6, C65 10U/6.3V_6, C64 10U/6.3V_6, C70 10U/6.3V_6

VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

+1.05V
R946 *0_6
C1084 0.1U/10V_4
R947 *6.04K/F_4
R948 *2.67K/F_4
EC_PWROK_R (7)

EC-D-23

U34F HASWELL_BGA_E

+VCC_CORE

AB45	VCC	
AB46	VCC	
AB8	VCC	
AC46	VCC	
AC47	VCC	
AC8	VCC	
AC9	VCC	
AD46	VCC	
AD8	VCC	
AE46	VCC	
AE47	VCC	
AE8	VCC	
AF8	VCC	
AG46	VCC	
AG8	VCC	
AH46	VCC	
AH47	VCC	
AH8	VCC	
AJ45	VCC	
AJ46	VCC	
AK46	VCC	
AK47	VCC	
AK8	VCC	
AL45	VCC	
AL46	VCC	
AL8	VCC	
AL9	VCC	
AM46	VCC	
AM47	VCC	
AM8	VCC	
AM9	VCC	
AN10	VCC	
AN12	VCC	
AN13	VCC	
AN14	VCC	
AN15	VCC	
AN16	VCC	
AN17	VCC	
AN19	VCC	
AN20	VCC	
AN21	VCC	
AN23	VCC	
AN24	VCC	
AN25	VCC	
AN26	VCC	
AN27	VCC	
AN29	VCC	
AN30	VCC	
AN32	VCC	
AN34	VCC	
AN36	VCC	
AN38	VCC	
AN39	VCC	
AN40	VCC	
AN41	VCC	
AN42	VCC	
AN43	VCC	
AN44	VCC	
AN45	VCC	
AN46	VCC	
AN8	VCC	
AN9	VCC	
AP10	VCC	
AP12	VCC	
AP13	VCC	
AP14	VCC	
AP15	VCC	
AP16	VCC	
AP17	VCC	
AP18	VCC	
AP19	VCC	
AP20	VCC	
AP21	VCC	
AP22	VCC	
AP23	VCC	
AP24	VCC	
AP25	VCC	
AP26	VCC	
AP27	VCC	
AP29	VCC	
AP30	VCC	
AP31	VCC	
AP32	VCC	
AP33	VCC	
AP34	VCC	
AP35	VCC	
AP36	VCC	
AP37	VCC	
AP38	VCC	
AP39	VCC	
AP40	VCC	
AP41	VCC	
AP42	VCC	
AP43	VCC	
AP44	VCC	
AP46	VCC	
AP47	VCC	
AP8	VCC	
AP9	VCC	
AR35	VCC	
AR37	VCC	
AR39	VCC	
AR41	VCC	
AR43	VCC	
AR45	VCC	
AR46	VCC	
H30	VCC	
H31	VCC	
H32	VCC	
H33	VCC	+VCC_CORE
H34	VCC	
H36	VCC	
H37	VCC	
H38	VCC	
H39	VCC	
H40	VCC	
H42	VCC	
H43	VCC	
H45	VCC	
H46	VCC	
H48	VCC	
H8	VCC	
H9	VCC	
J10	VCC	
J14	VCC	
J19	VCC	
J24	VCC	
J29	VCC	
J33	VCC	
J36	VCC	
J37	VCC	
J38	VCC	
J39	VCC	
J40	VCC	
J42	VCC	
J43	VCC	
J45	VCC	
J46	VCC	
J48	VCC	
J8	VCC	
J9	VCC	
K38	VCC	
K40	VCC	
K43	VCC	
K44	VCC	
K45	VCC	
K46	VCC	
K48	VCC	
K8	VCC	
K9	VCC	
L37	VCC	
L38	VCC	
L39	VCC	
L40	VCC	
L42	VCC	
L43	VCC	
L44	VCC	
L46	VCC	
L47	VCC	
L8	VCC	
M37	VCC	
M38	VCC	
M39	VCC	
M40	VCC	
M42	VCC	
M43	VCC	
M44	VCC	
M45	VCC	
M46	VCC	
M8	VCC	
M9	VCC	
N37	VCC	
N38	VCC	
N39	VCC	
N40	VCC	
N42	VCC	
N43	VCC	
N44	VCC	
N46	VCC	
N47	VCC	
N8	VCC	
N9	VCC	
P45	VCC	
P46	VCC	
P8	VCC	
R46	VCC	
R47	VCC	
R8	VCC	
R9	VCC	
T45	VCC	
T46	VCC	
U46	VCC	
U47	VCC	
U8	VCC	
U9	VCC	
V45	VCC	
V46	VCC	
V8	VCC	
W46	VCC	
W47	VCC	
W8	VCC	
Y45	VCC	
Y46	VCC	
Y8	VCC	
A27	VCC	
A28	VCC	
A31	VCC	
A32	VCC	
A34	VCC	
B27	VCC	
B28	VCC	
B31	VCC	
B32	VCC	
B34	VCC	
B36	VCC	
B38	VCC	
B39	VCC	
B42	VCC	

bga1364-intel-genuine
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SVID

Layout note: need routing together and ALERT need between CLK and DATA.

VCCIO_OUT
Place PU resistor close to CPU
R73 130/F_4
H_CPU_SVIDDAT R57 *0_4_S VR_SVIDDAT (37)
VCCIO_OUT
Place PU resistor close to CPU
R58 75/F_4
H_CPU_SVIDART# R74 43_4 VR_SVIDART# (37)
H_CPU_SVIDCLK R59 *0_4_S VR_SVIDCLK (37)

Power Test Propose

+1.05V
R61 150_4
PWR_DEBUG_R
R78 *10K_4

+1.05V
R48 *0_8
VCCIO_OUT
C48 *4.7U/6.3V_6

MOW WW12-->if PWR_DEBUG# is routed to the XDP the R741 value is 150 ohm

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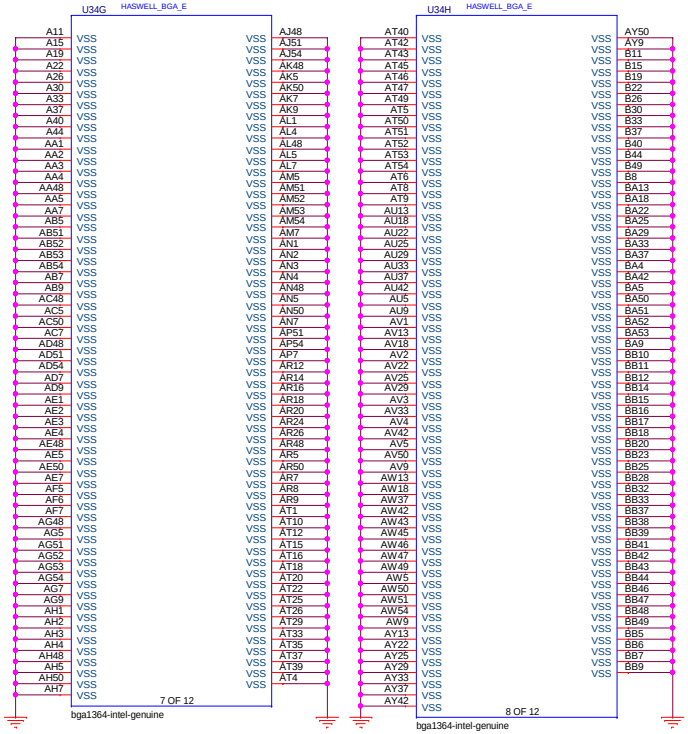
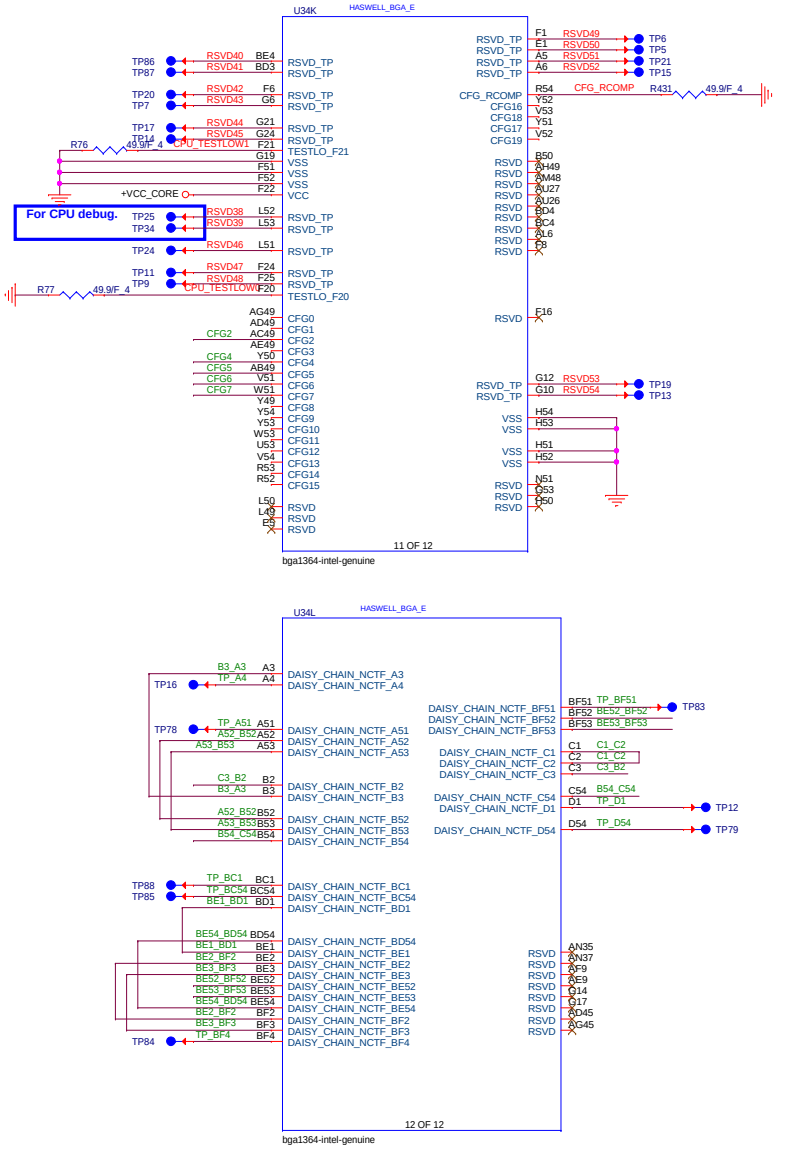
Haswell Processor (GND)



Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	CFG2 R102 1K_4
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	CFG4 R95 1K_4
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	CFG6 R91 *1K_4 CFG5 R96 *1K_4
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	CFG7 R93 *1K_4

Haswell Processor (CFG,RSVD)



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(8,9,11,17,18,23,36,41) +1.5V
(2,8,9,10,11,13,14,15,16,17,18,19,20,22,25,26,27,28,30,38,39,41,43,47) +3V
(2,8,9,10,11,20,23,28,30,33,36,37,39,40,45,51) +3V_S5

07

Lynx Point (DMI,FDI,PM)

U40B — LPT_PCH_M_EDS — REV = 5

DMI_RXN0 AW22 / DMI_RXN1 AR20
DMI_RXN2 AP17 / DMI_RXN3 AV20
DMI_RXP0 AY22 / DMI_RXP1 AP20
DMI_RXP2 AR17 / DMI_RXP3 AW20
DMI_TXN0 BD21 / DMI_TXN1 BE20
DMI_TXN2 BD17 / DMI_TXN3 BE18
DMI_TXP0 BB21 / DMI_TXP1 BC20
DMI_TXP2 BB17 / DMI_TXP3 BC18
DMI_IREF BE16 — R531 *0_4_S — +1.5V
AW17 TP12
AV17 TP7
DMI_RCOMP AY17 — R222 7.5K/F_4

FDI_RXN_0 AJ35 — FDI_TXN0 (4)
FDI_RXN_1 AL35 — FDI_TXN1 (4)
FDI_RXP_0 AJ36 — FDI_TXP0 (4)
FDI_RXP_1 AL36 — FDI_TXP1 (4)
TP16 AV43
TP5 AY45
TP15 AV45
TP10 AW44
FDI_CSYNC AL39 — FDI_CSYNC (2)
FDI_INT AL40 — FDI_INT (2)
FDI_IREF AT45 — R507 *0_4_S — +1.5V
TP17 AU42
TP13 AU44
FDI_RCOMP AR44 — R508 7.5K/F_4

(27) SUSACK#EC — for DS3 R626 *0_4_S — SUSACK#_R R6
(2) XDP_DBRST# — R304 *0_4_S — SYS_RESET# AM1
SYS_PWROK — R268 *0_4_S — SYS_PWROK_R AD7
(5) EC_PWROK_R — EC_PWROK_R F10
APWROK AB7
(2) PM_DRAM_PWRGD H3
(27) RSMRST# — R317 *0_4_S — PCH_RSMRST# J2
(27) SUSWARN#EC — for DS3 R624 *0_4_S — PCH_SUSPWRACK J4
(27) SIO_PWRBTN# — R583 *0_4_S — PCH_PWRBTN# K1
(27,45) AC_PRESENT — for DS3 R281 *0_4_S — PCH_ACPRESENT E6
PCH_BATLOW# K7
PCH_RI# N4
TP65 — AB10 TP21
(23) WLAN_AOAC_ON — WLAN_AOAC_ON D2

EC-D-23
EC-B-05

SUSACK# / SYS_RESET# / SYS_PWROK / PWROK / APWROK / DRAMPWROK / RSMRST# / SUSWARN#/SUSPWRNACK/GPIO30 (SUS) / PWRBTN# / ACPRESENT/GPIO31 (DSW) / BATLOW#/GPIO72 (SUS) / RI# / TP21 / SLP_WLAN#/GPIO29 (DSW)

System Power Management

DSWVRMEN C8 — DSWVREN (8) — (43) DGPU_HOLD_RST#
DPWROK L13 — DPWROK_R — (43,47) DGPU_PWROK
WAKE# K3 — PCIE_WAKE# — PCIE_WAKE# (20,23) — (38,40,51) GFXON
CLKRUN# AN7 — CLKRUN# — CLKRUN# (27) — (8) BBS_BIT1
(SUS) SUS_STAT#/GPIO61 U7 — SUS_STAT# — TP66
(SUS) SUSCLK/GPIO62 Y6 — SUSCLK (8)
(SUS) SLP_S5#/GPIO63 Y7 — TP64
SLP_S4# C6 — R600 *0_4_S — SLP_S4# (27)
SLP_S3# H1 — R584 *0_4_S — SIO_SLP_S3# (27)
SLP_A# F3
SLP_SUS# F1 — for DS3 R585 *0_4_S — SLP_SUS# (27)
PMSYNCH AY3 — PCH_SYNCH R569 *0_4_S — PM_SYNC (2)
SLP_LAN# G5

EC-A-14

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LPT_PCH_M_EDS/BGA

Lynx Point (CRT,PCI,DDI CNTL)

U40E — LPT_PCH_M_EV — REV = 5

(16) INT_CRT_BLU — R499 150/F_4 — VGA_BLUE T45
(16) INT_CRT_GRE — R498 150/F_4 — VGA_GREEN U44
(16) INT_CRT_RED — R497 150/F_4 — VGA_RED V45
(16) INT_DDCCLK — VGA_DDC_CLK M43
(16) INT_DDCDAT — VGA_DDC_DATA M45
(16) INT_CRT_HSYNC — R500 33_4 — PCH_HSYNC_R — VGA_HSYNC N42
(16) INT_CRT_VSYNC — R501 33_4 — PCH_VSYNC_R — VGA_VSYNC N44
DAC_IREF (50ohm)
Trace length < 500 MILS
Trace spacing = 30 MILS
R496 649/F_4 — DAC_IREF — DAC_IREF U40
VGA_IRTN U39

(15) LCD_PWM — EDP_BKLTCTL N36
(15) PANEL_BKEN — EDP_BKLTEN K36
(15) ENVDD — EDP_VDDEN G36

PCI_PIRQA# — PIRQA# H20
PCI_PIRQB# — PIRQB# L20
PCI_PIRQC# — PIRQC# K17
PCI_PIRQD# — PIRQD# M20

DGPU_HOLD_RST# — R860 *0_4_S — GPIO50 A12 (CORE)
DGPU_PWROK — R861 *0_4_S — GPIO52 B13 (CORE)
GFXON — GPIO54 C12 (CORE)
GPIO51 C10 (CORE)
TP94 — DGPU_PWM_SLT# — GPIO53 A10 (CORE)
(8) STP_A16OVR — GPIO55 AL6 (CORE)

DDPB_CTRLCLK R40 — HDMI_SCL (17)
DDPB_CTRLDATA R39 — HDMI_SDA (17)
DDPC_CTRLCLK R35
DDPC_CTRLDATA R36
DDPD_CTRLCLK N40 — TP89
DDPD_CTRLDATA N38 — TP59
DDPB_AUXN H45
DDPC_AUXN K43
DDPD_AUXN J42
DDPB_AUXP H43
DDPC_AUXP K45
DDPD_AUXP J44
DDPB_HPD K40 — INT_HDMI_HPD (17)
DDPC_HPD K38
DDPD_HPD H39

PIRQE#/GPIO2 G17 — GPIO2 (CORE)
PIRQF#/GPIO3 F17 — GPIO3 (CORE)
PIRQG#/GPIO4 L15 — EXTTS_SNI_DRV0_PCH (CORE)
PIRQH#/GPIO5 M15 — EXTTS_SNI_DRV1_PCH (CORE)
PME# AD10 — PCI_PME# — TP62
PLTRST# Y11 — PCI_PLTRST#

5 OF 11
LPT_PCH_M_EDS/BGA

When GPIO[5:2] are configured as output GPIOs, they behave in an open drain manner.

PLTRST# Buffer

+3V_S5 — C692 0.1U/10V_4
PCI_PLTRST# — U42 TC7SH08FU — PLTRST# (2,20,23,25,26,43)
R632 100K_4

GPIO50 DGPU_HOLD_RST#_R

R235 100K_4 — DGPU_HOLD_RST#
+3V — R236 *10K_4

PCH PM PU/PD

+3V: SYS_RESET# R617 1K_4 / CLKRUN# R256 8.2K_4
+3V_S5: WLAN_AOAC_ON R298 10K_4 / PCH_BATLOW# R273 8.2K_4 / PCIE_WAKE# R602 1K_4
EC-A-09
+3V_S5: PCH_RI# R582 10K_4 / SUSACK#_R R625 10K_4 / PCH_SUSPWRACK R603 10K_4 / PCH_ACPRESENT R274 8.2K_4 / SYS_PWROK R263 *100K_4 / PCH_RSMRST# R291 10K_4 / DELAY_VR_PWRGOOD R299 10K_4 / R344 *100K_4

SYSPWOK

+3V_S5 — C426 *0.1U/10V_4
(34) SYS_PWROK — SYS_PWROK — U18 TC7SH08FU — DELAY_VR_PWRGOOD — DELAY_VR_PWRGOOD (37)
EC_PWROK — EC_PWROK (18,27)
R336 *100K_4
R353 *0_4

PCH_PWROK_OK(CLG)

+3V_S5 — C427 0.1U/10V_4
EC_PWROK_R — U19 TC7SH08FU — HWPG (27,31,33,34,35,36)
DELAY_VR_PWRGOOD
EC-D-24
APWROK — R338 *0_4/S — EC_PWROK_R
DELAY_VR_PWRGOOD R362 *0_4
EC_PWROK R337 *0_4 — EC_PWROK_R

DSW Circuit

SUSACK#_R — R604 *0_4 — PCH_SUSPWRACK
R305 *0_4_S — PCH_RSMRST#
DPWROK_R — for DS3 R312 *0_4 — DPWROK (27)

PCI PU

EC-A-14
GFXON — R880 *100K_4
+3V
PCI_PIRQA# R207 8.2K_4
PCI_PIRQB# R203 8.2K_4
PCI_PIRQC# R209 8.2K_4
PCI_PIRQD# R197 8.2K_4
EXTTS_SNI_DRV0_PCH R536 8.2K_4
EXTTS_SNI_DRV1_PCH R548 8.2K_4
GPIO2 R863 8.2K_4
GPIO3 R862 8.2K_4
EC-A-07

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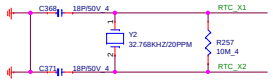
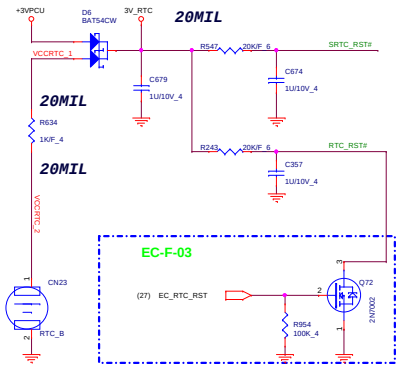
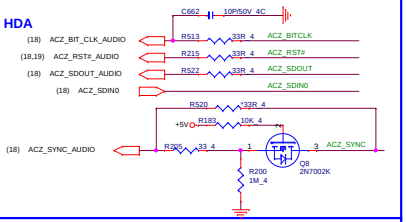
RTC Clock 32.768KHz (RTC)



RTC Circuitry (RTC)

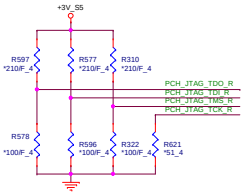


HDA

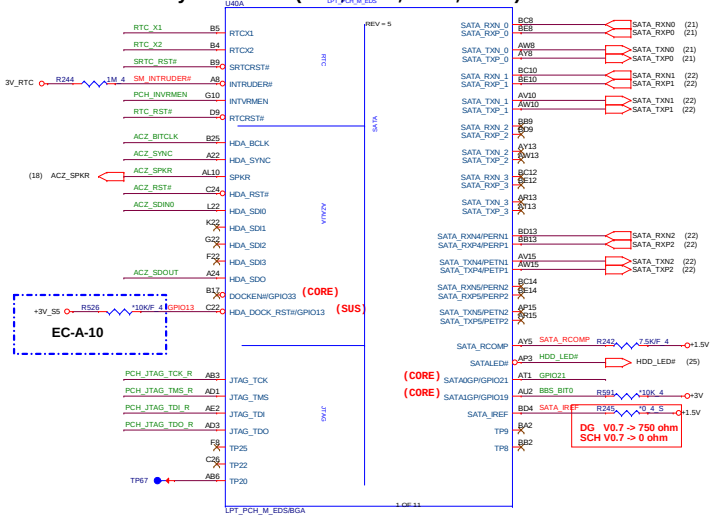


PCH JTAG

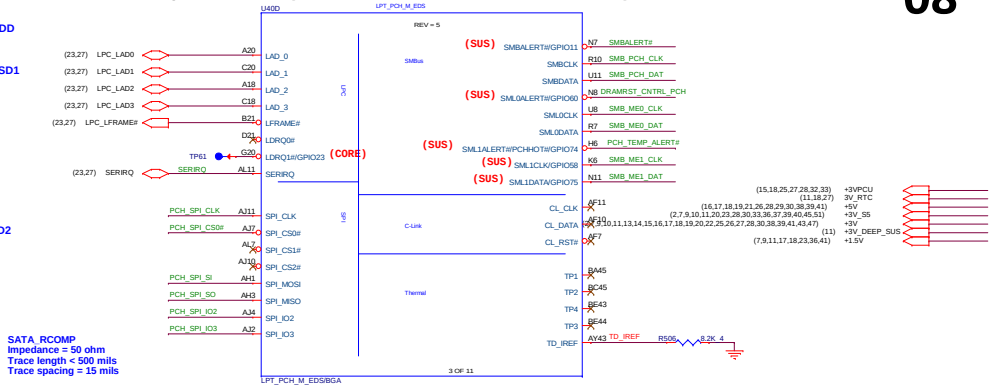
JTAG_TCK,JTAG_TMS
Trace Length < 9000mils



Lynx Point (RTC,IHDA,SATA,JTAG)



Lynx Point (LPC,SPI,SMBUS,C-LINK,THERMAL)

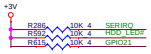


SATA_RCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils

PCH STRAPING

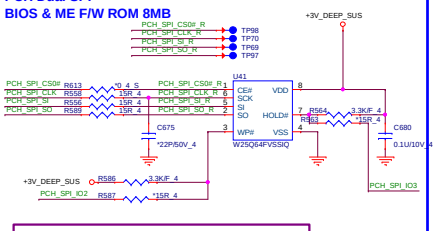
Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	ACZ_SPKR R288 *1K_4 +3V
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	(7) SUSCLK R293 *1K_4
GPIO55	Top-Block Swap Override	PWROK	0 = Top-Block Swap mode 1 = Default (Int PU)	(7) STP_A16OVR R248 *1K_4
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	PCH_INVRMEN R565 330K_4 3V_RTC
GPIO51	Boot BIOS Strap bit 1	PWROK	Bit1 Bit0 0 0 Reserved 0 1 SPI 1 0 LPC	(7) BBS_BIT1 R226 *1K_4 BBS_BIT0 R572 *1K_4
SATA1GP/GPIO19	Boot BIOS Strap bit 0	PWROK		
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	ACZ_SDOUT 1K_4 R523 R521 *1K_4 +VCC_HDA_IO ME_WR# (27)
GPIO36	RSVD	PWROK	Internal PD	(10) GPIO36 R573 *1K_4 +3V
SATA3GP/GPIO37	TLS Confidentiality	PWROK	0 = TLS no confidentiality (Int PD) 1 = TLS with confidentiality	(10) FDI_OVRVLTG R576 *1K_4 +3V
GPIO8	RSVD	RSMRST#	Internal PU	(10,23) BT_OFF# R321 *1K_4
GPIO28	PLL on die VR enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	(10) PLL_ODVR_EN R231 *1K_4
DSWVREN	On Die DSW VR Enable	Always	0 = Enable 1 = Disable Must be PU to VCCRTC	(7) DSWVREN R560 330K_4 R559 *330K_4 3V_RTC
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+VCC_HDA_IO R201 1K_4 ACZ_SYNC

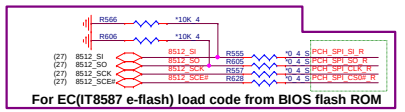
Pull High



PCH Dual SPI

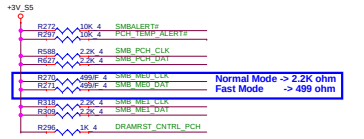
BIOS & ME F/W ROM 8MB



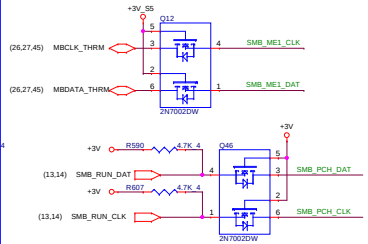


For EC(IT8587 e-flash) load code from BIOS flash ROM

SMBus



SMBus/Pull-up(CLG)



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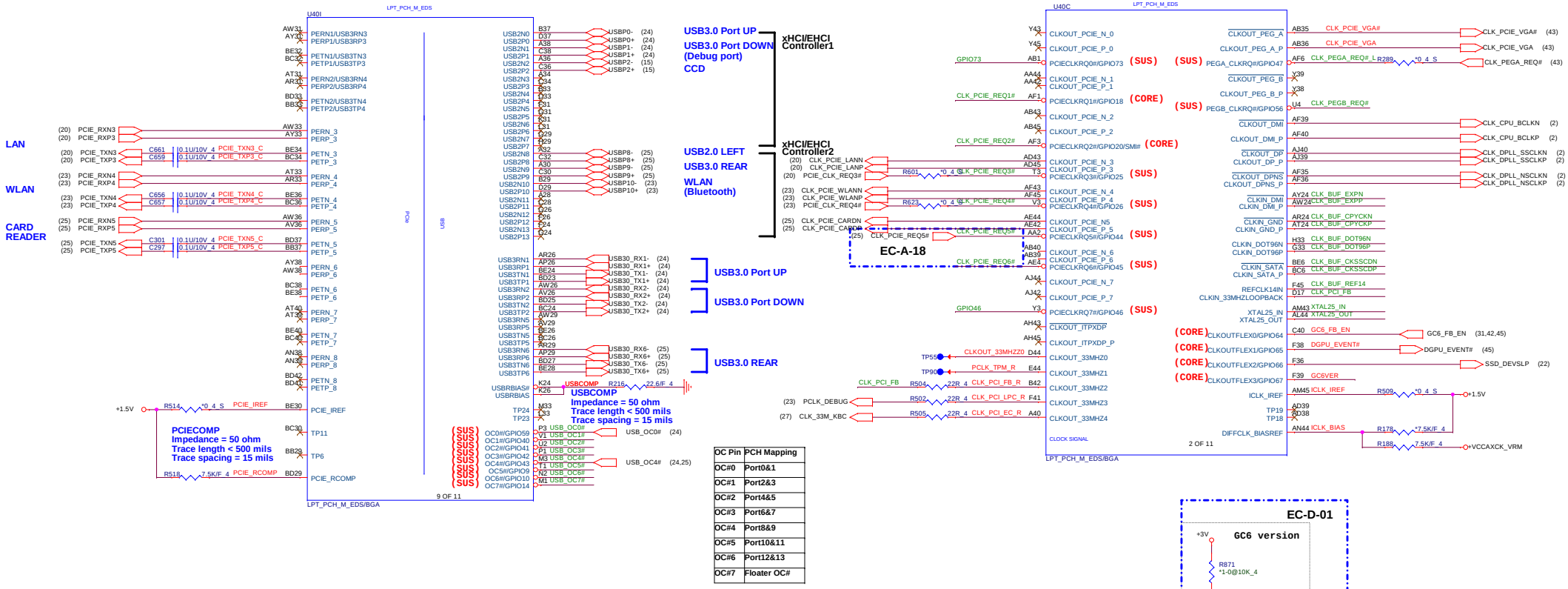
Lynx Point (PCIE,USB3.0,USB2.0)

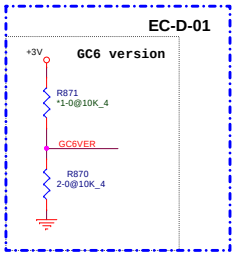
Lynx Point (CLOCK)

09

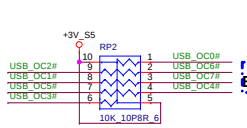
(2,7,8,10,11,13,14,15,16,17,18,19,20,22,25,26,27,28,30,38,39,41,43,47) +3V
(7,8,11,17,18,23,36,41) +1.5V
(2,7,8,10,11,20,23,28,30,33,36,37,39,40,45,51) +3V_S5



OC Pin	PCH Mapping
OC#0	Port0&1
OC#1	Port2&3
OC#2	Port4&5
OC#3	Port6&7
OC#4	Port8&9
OC#5	Port10&11
OC#6	Port12&13
OC#7	Floater OC#

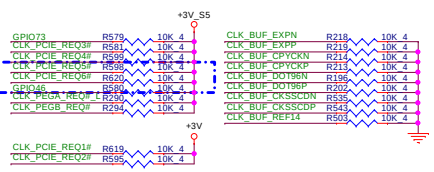


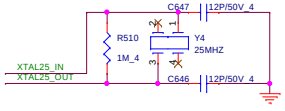
USB Overcurrent



EC-A-18

PCH Intenal Clock





PCH XDP Signal

Routed by 50 ohm

PROJECT : NL8A			
Quanta Computer Inc.			
Size: Custom	Document Number: LPT 3/6 (PCIE/USB/CLK)		Rev: 3B
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Lynx Point (GPIO,CPU/MISC,NCTF)

(2,7,8,9,11,13,14,15,16,17,18,19,20,22,25,26,27,28,30,38,39,41,43,47) +3V
(2,5,11,35,40,41) +1.05V
(2,7,8,9,11,20,23,28,30,33,36,37,39,40,45,51) +3V_S5

10

U40F — LPT_PCH_M_EDS

SGPIO	R230 100_4	GPIO0	AT8
(27) SIO_EXT_SMI#		SIO_EXT_SMI#	F13
		GPU_GX/GT	A14
(27) SIO_EXT_SCI#		SIO_EXT_SCI#	G15
(8,23) BT_OFF#		BT_OFF#	Y1
		GPIO12	K13
(23) WLAN_ON/OFF#		WLAN_ON/OFF#	AB11
		GPU_N15P/N15E	AN2
		GPIO17	C14
		BIOS_REC	BB4
(22) NGFF_SSD_PRESENT#	R307 *0_4_S	GPIO24	Y10
		GPIO27	R11
(8) PLL_ODVR_EN			AD11
(26) TEMP_ALERT#		TEMP_ALERT#	AN6
		GPIO35	AP1
(8) GPIO36		GPIO36	AT3
(8) FDI_OVRVLTG		FDI_OVRVLTG	AK1
		MFG_MODE	AT7
		BOARD_ID1	AM3
		BIOS_RESP	AN4
(15) CCD_EN		CCD_EN	AK3
		GPIO57	U12
(15) LCD_BK_OFF		LCD_BK_OFF	C16
		SV_DET	D13
		BOARD_ID2	G13
		BOARD_ID0	H15

BMBUSY#/GPIO0	(CORE)		
TACH1/GPIO1	(CORE)		
TACH2/GPIO6	(CORE)		
TACH3/GPIO7	(CORE)		
GPIO8	(SUS)		
LAN_PHY_PWR_CTRL/GPIO12	(SUS)		
GPIO15	(SUS)		
SATA4GP/GPIO16	(CORE)		
TACH0/GPIO17	(CORE)		
SCLOCK/GPIO22	(CORE)		
GPIO24	(SUS)		
GPIO27	(DSW)		
GPIO28	(SUS)		
GPIO34	(CORE)		
GPIO35/NMI#	(CORE)		
SATA2GP/GPIO36	(CORE)		
SATA3GP/GPIO37	(CORE)		
SLOAD/GPIO38	(CORE)		
SDATAOUT0/GPIO39	(CORE)		
SDATAOUT1/GPIO48	(CORE)		
SATA5GP/GPIO49	(CORE)		
GPIO57	(SUS)		
TACH4/GPIO68	(CORE)		
TACH5/GPIO69	(CORE)		
TACH6/GPIO70	(CORE)		
TACH7/GPIO71	(CORE)		
		TP14	AN10 EC_A20GATE
		PECI	AY1 PCH_PECI
		RCIN#	AT6 EC_RCIN#
		PROCPWRGD	AV3
		THRMTRIP#	AV1 PCH_THRMTRIP#
		PLTRST_PROC#	AU4
		VSS	N10
		VSS	A2
		VSS	A41
		VSS	A43
		VSS	A44
		VSS	B1
		VSS	B2
		VSS	B44
		VSS	B45
		VSS	BA1
		VSS	BC1
		VSS	BD1
		VSS	BD2
		VSS	BD44
		VSS	BD45
		VSS	BE2
		VSS	BE3
		VSS	D1
		VSS	E1
		VSS	E45
		VSS	A4
R549 *0_4_S TP_VSS_NCTF2		VSS	BE41
		VSS	BE5
		VSS	C45
		VSS	A5

CPU/Misc — GPIO — NCTF — 6 OF 11 — LPT_PCH_M_EDS/BGA

TP95 TP96

EC_A20GATE (27) · H_PECI (2,27) · EC_RCIN# (27) · H_PWRGOOD (2) · PM_THRMTRIP# (2) · CPU_PLTRST# (2)

BOARD ID SETTING

BOARD_ID0 R538 10K_4 +3V, R539 *10K_4
BOARD_ID1 R575 10K_4 +3V, R594 *10K_4
BOARD_ID2 R554 10K_4 +3V, R562 *10K_4

EC-D-01

GPIO35 R949 *10K_4

EC-E-01

BOARD_ID[3:0] Model Name

GPIO35	BOARD_ID0	BOARD_ID1	BOARD_ID2	NLx
1	0	0	0	SDV
1	0	0	1	SIV
1	0	1	0	SIT
1	0	1	1	SVT
1	1	0	0	SOVP
1	1	0	1	NL8B SDV
1	1	1	0	NL8B SIT
1	1	1	1	NL8B MV
0	0	0	0	NL9 SDV
0	0	0	1	NL9 MV
0	0	1	0	
0	0	1	1	

PCH GPIO PU/PD

+3V
SIO_EXT_SMI# R551 10K_4
SIO_EXT_SCI# R537 10K_4
TEMP_ALERT# R262 10K_4
GPIO35 R574 10K_4
LCD_BK_OFF R542 10K_4
+3V_S5
BT_OFF# R622 *10K_4
WLAN_ON/OFF# R306 10K_4
GPIO12 R561 10K_4
GPIO24 R269 10K_4
GPIO57 R308 10K_4
GPIO27 R295 10K_4

EC-B-02

CCD_EN R320 100K_4
GPIO17 R227 10K_4

PCH MISC PU/PD

+3V
EC_A20GATE R287 8.2K_4
EC_RCIN# R247 10K_4
+1.05V
PCH_THRMTRIP# R571 *1K_4

NL8 GPU N16P/N16E Select setting

GPIO16	N16P	N16E
Stuff	Ra (Hi)	Rb (Lo)

+3V — R648 Rb 10K_4 GPU_N15P/N15E — R593 Ra *10K_4

NL8 GPU GX/GT Select setting

	GX	GT
Stuff	Ra (Hi)	Rb (Lo)

+3V — R228 Rb 10K_4 GPU_GX/GT — R232 Ra *10K_4

BIOS RECOVERY

0 = Enable
1 = Disable

BIOS_REC R261 10K_4 +3V, R255 *0_4

Swap GPIO

0 = SGPIO
1 = Default

SGPIO R241 1K_4 +3V, R233 *0_4

MFG TEST

MFG_MODE R285 10K_4 +3V, R284 *0_4

SV Detect

0 = SV Detect
1 = Default

SV_DET R541 10K_4 +3V, R540 *0_4

BIOS_RESP

0 = BIOS RESP
1 = Default

BIOS_RESP R616 10K_4 +3V, R319 *0_4

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	LPT 4/6 (GPIO/MISC)	3B
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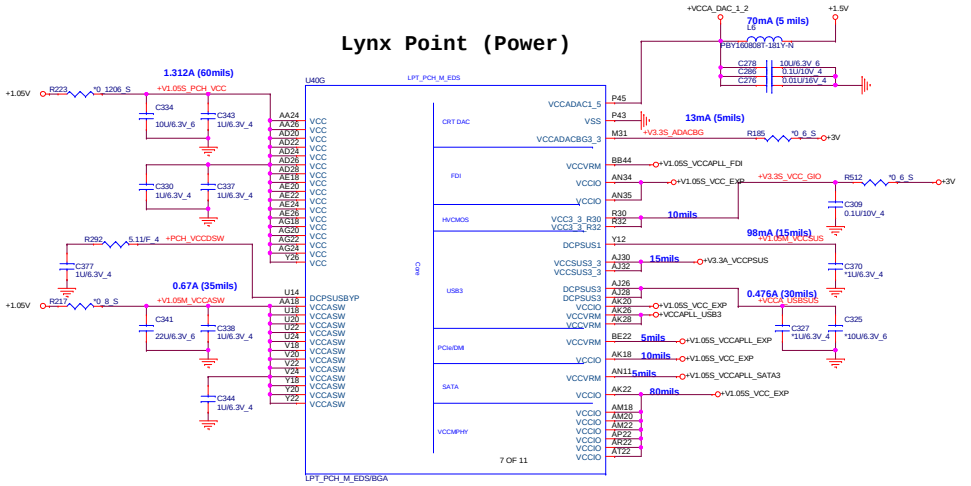
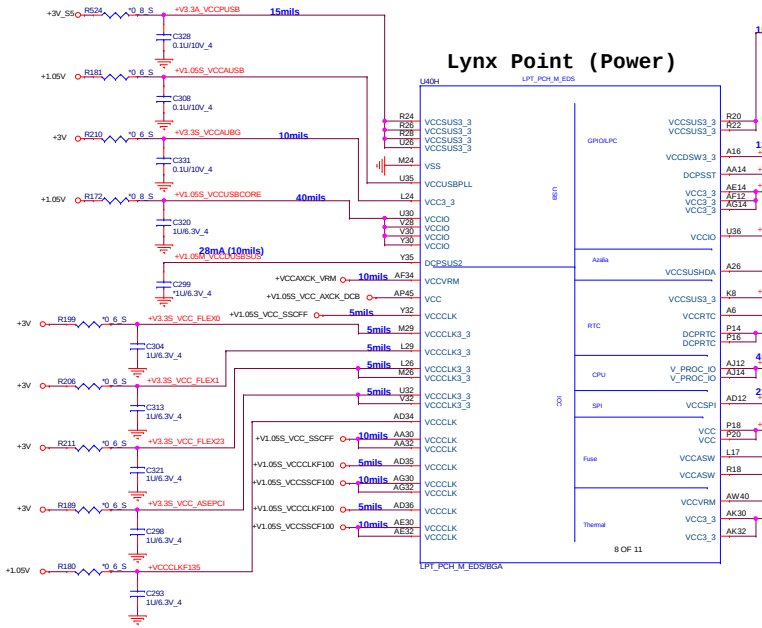
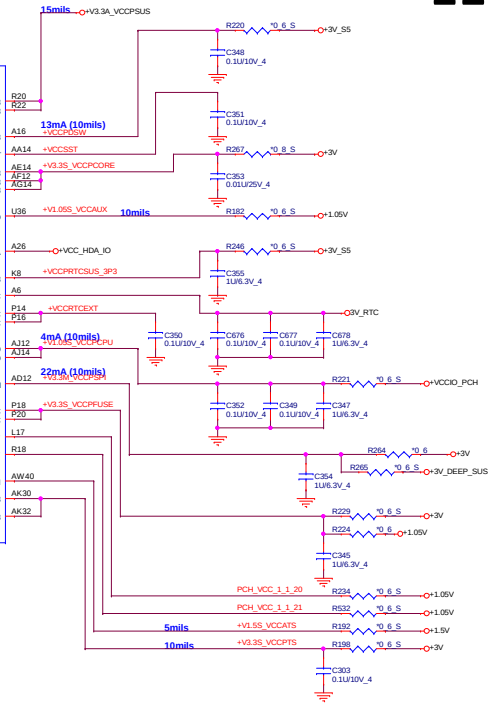
Lynx Point (Power)



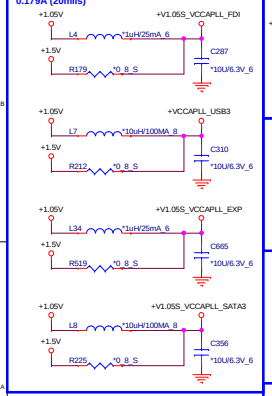




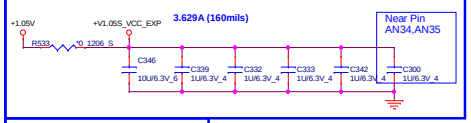
PCH VRM Power

1.05V OPTION IS PROVIDED FOR VALIDATION PURPOSES

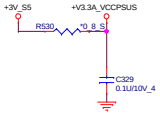
0.179A (20mils)



PCH VCCIO Power

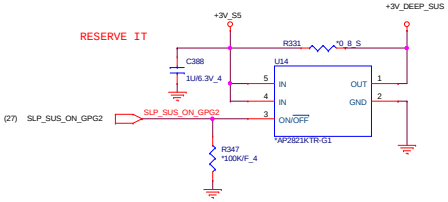


PCH band gap Power

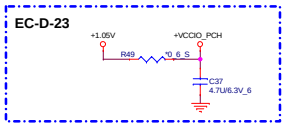


PCH DS3 PWR

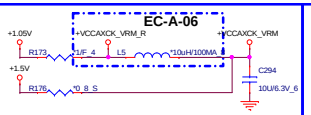
RESERVE IT

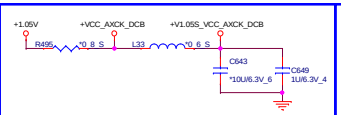


EC-D-23



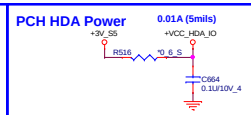
EC-A-06

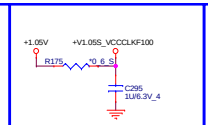


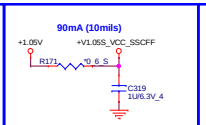


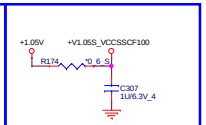
PCH HDA Power

0.01A (5mils)









(8,18,27) 3V_RTC
(2,5,10,35,40,41) +1.05V
(7,8,9,17,18,23,36,41) +1.5V
(2,7,8,9,10,13,14,15,16,17,18,19,20,22,25,26,27,28,30,38,39,41,43,47) +3V
(2,7,8,9,10,20,23,28,30,33,36,37,39,40,45,51) +3V_S5
(8) +3V_DEEP_SUS

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Quanta Computer Inc.

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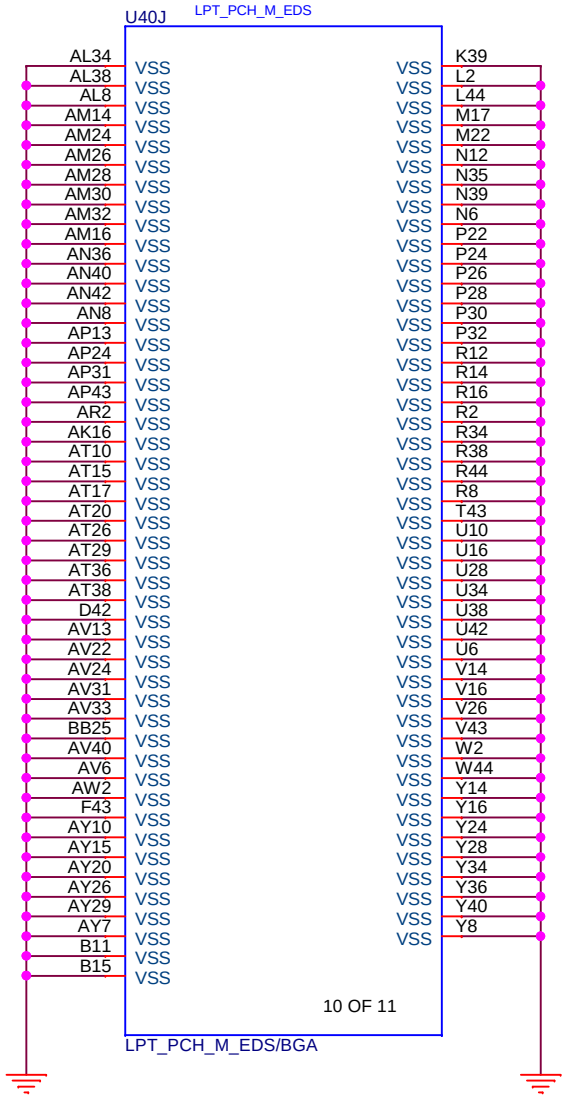
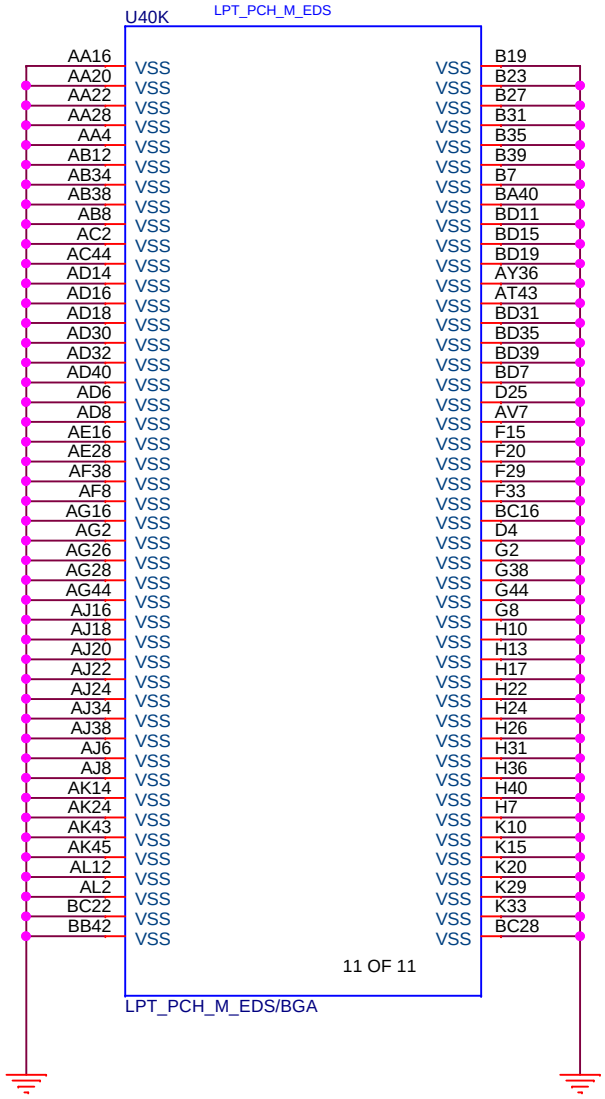
Lynx Point (GND)



Lynx Point (GND)



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PROJECT : NL8A

Quanta Computer Inc.

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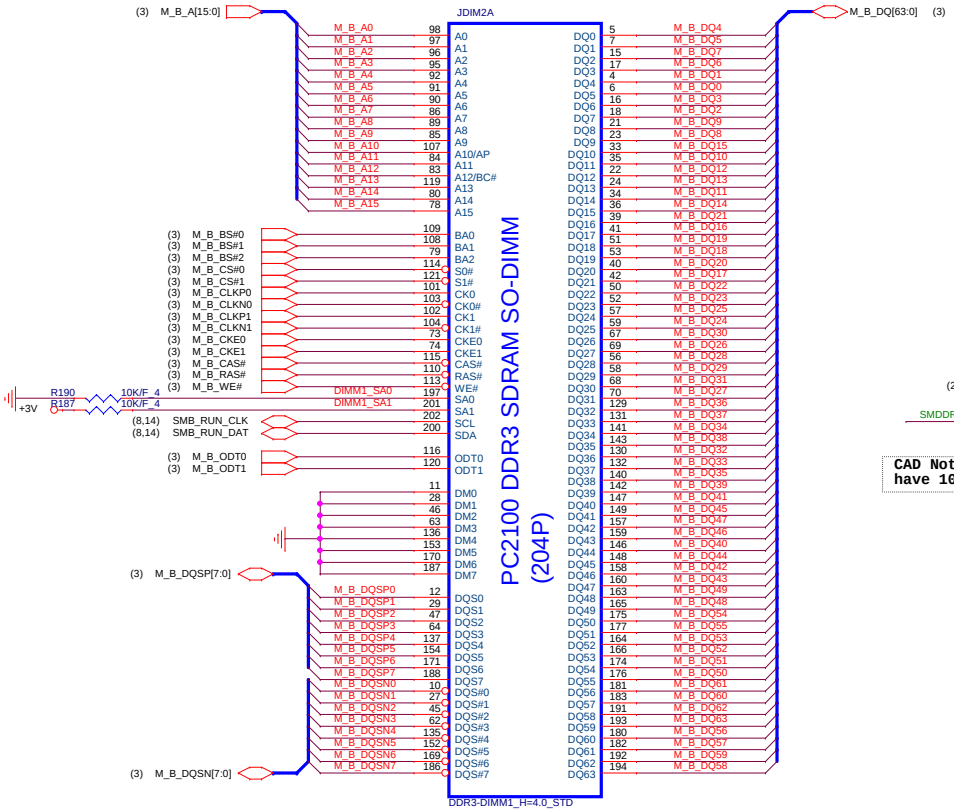
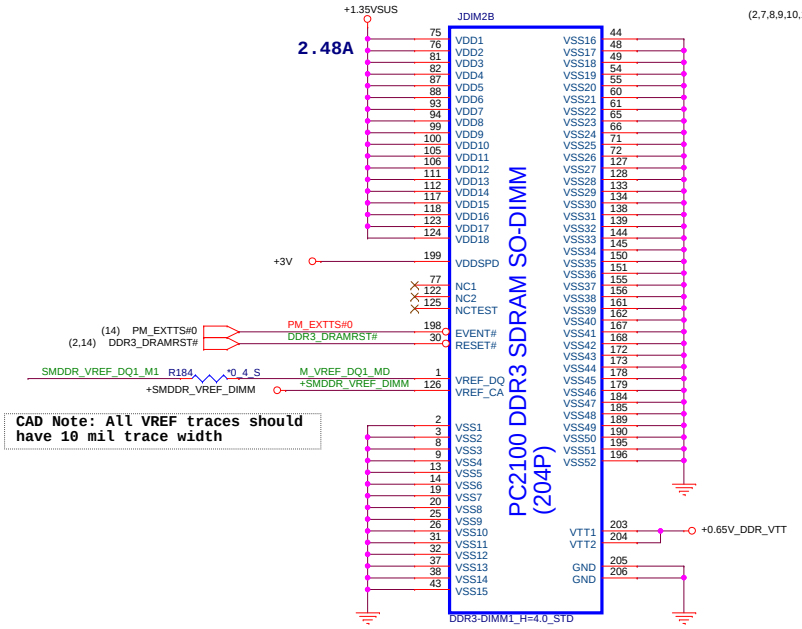
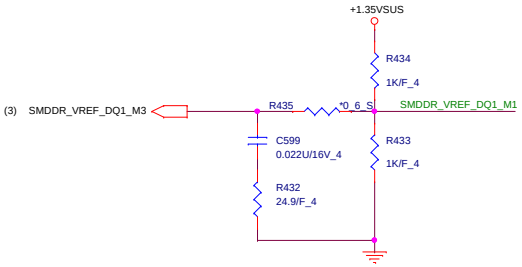
DDR_STD(DDR)

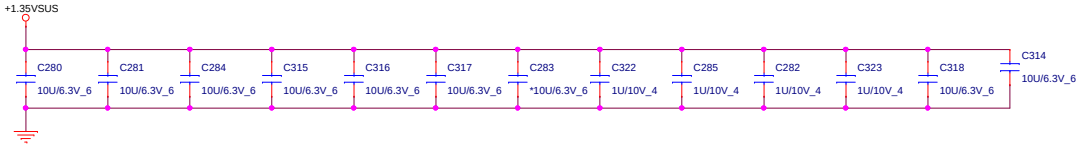


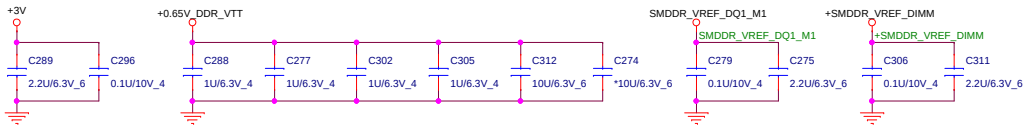


CAD Note: All VREF traces should have 10 mil trace width



Place these Caps near SO-Dimm1





PROJECT : NL8A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3L DIMM1-STD (4.0H)	3B
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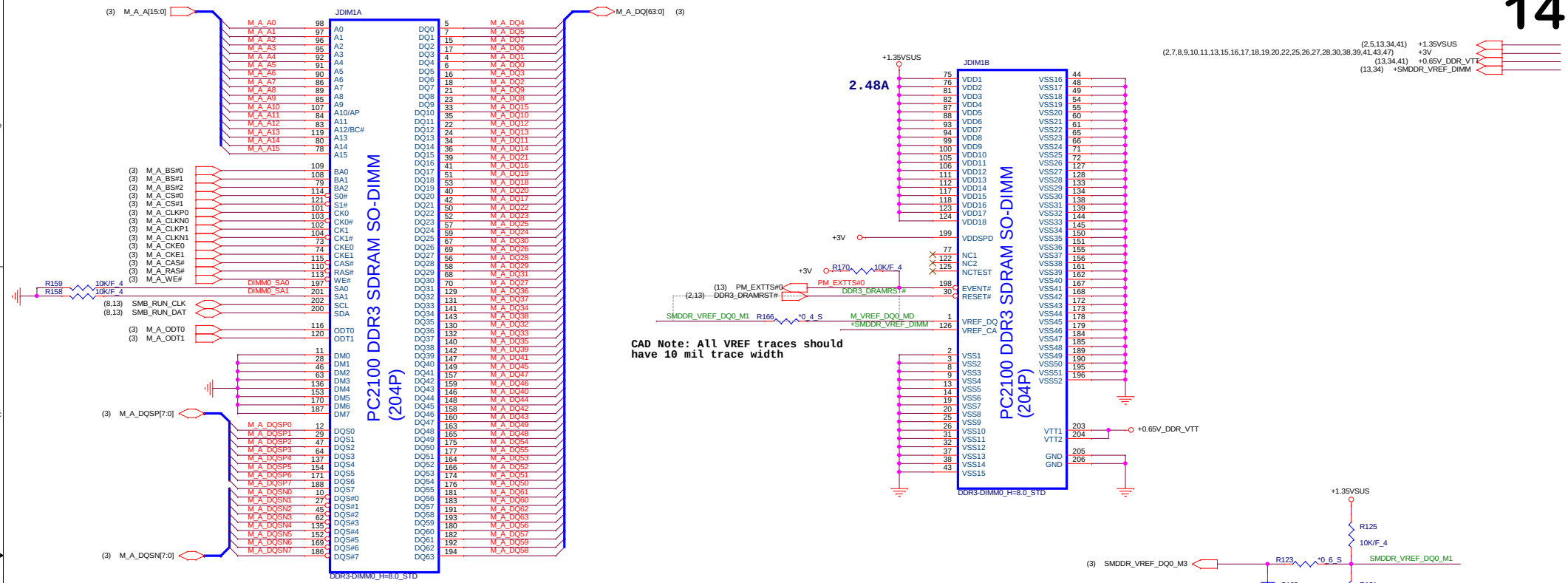
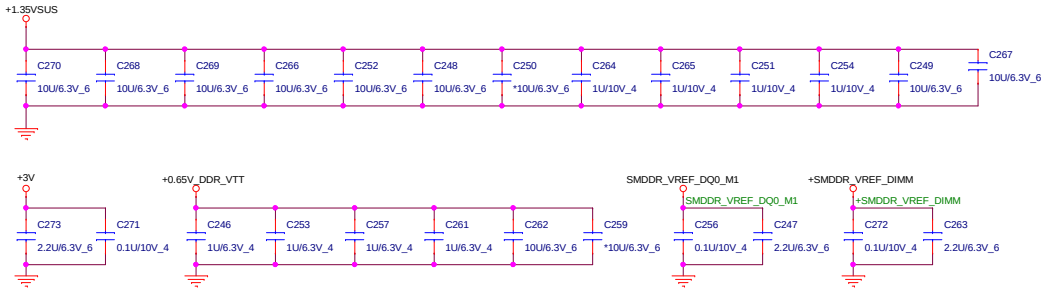
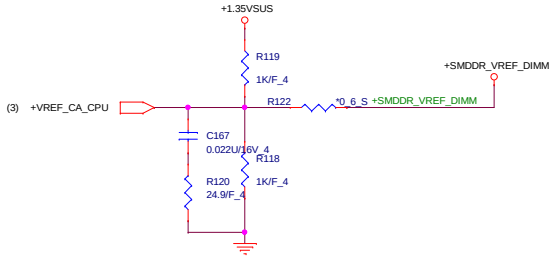
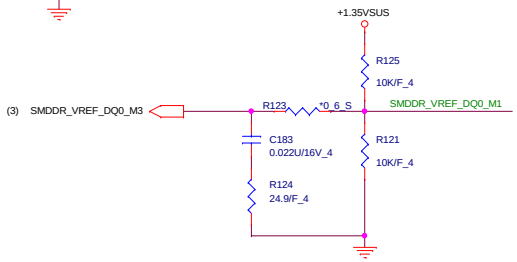
DDR_STD(DDR)



Place these Caps near SO-Dimm0







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Quanta Computer Inc.		
Size: Custom	Document Number: DDR3L DIMM0-STD (8.0H)	Rev: 3B
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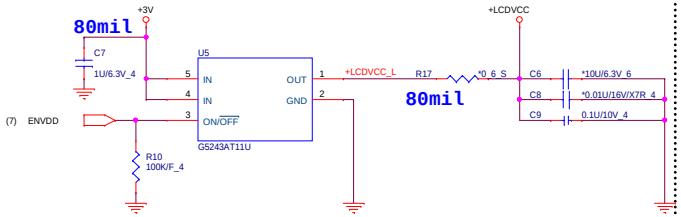
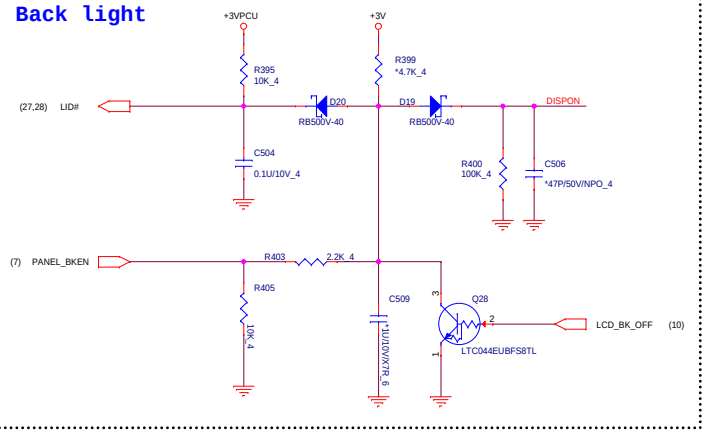
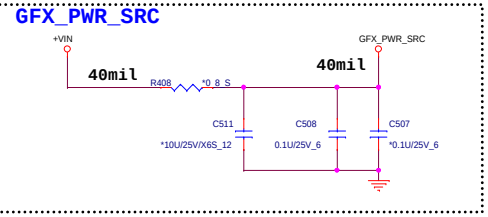
LCDVCC

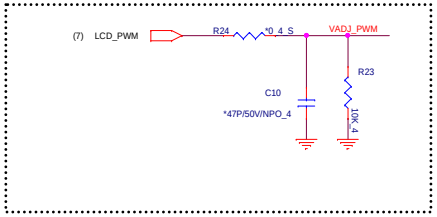


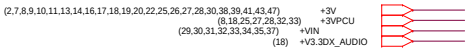
Back light



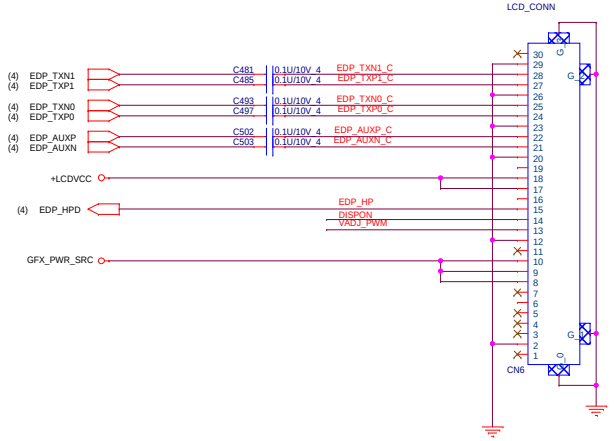
GFX_PWR_SRC



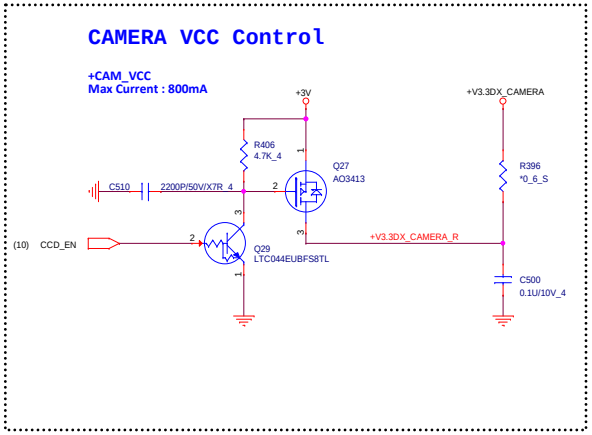




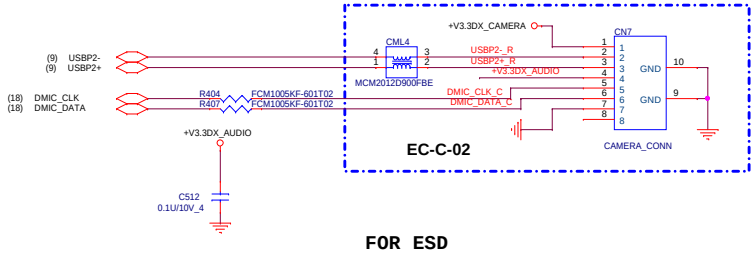
30Pin eDP CN



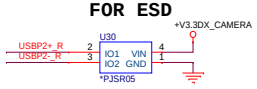
CAMERA VCC Control



CAMERA/DMIC CONN



FOR ESD



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	eDP LCD/CAMERA	3B
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(8,17,18,19,21,26,28,29,30,38,39,41) +5V
(2,7,8,9,10,11,13,14,15,17,18,19,20,22,25,26,27,28,30,38,39,41,43,47) +3V

Layout Note:
Setting R,G,B trace impedance to 50 ohm.

(7) INT_CRT_RED
(7) INT_CRT_GRE
(7) INT_CRT_BLU
(7) INT_CRT_VSYNC
(7) INT_CRT_HSYNC
(7) INT_DDCCLK
(7) INT_DDCDAT

+5V
CRT_VCC
D1 RB500V-40
C1 0.1U/10V_4
F2 FUSE1A8V_POLY
CRT_VCC_R
C2 0.1U/10V_4

L27 BLM15BA470SN1D_4
L28 BLM15BA470SN1D_4
L29 BLM15BA470SN1D_4
CRT_R1
CRT_G1
CRT_B1

R384 150/F_4
R385 150/F_4
R386 150/F_4
C469 5.6P/50V/COG_4
C470 5.6P/50V/COG_4
C471 5.6P/50V/COG_4
C464 5.6P/50V/COG_4
C463 5.6P/50V/COG_4
C462 5.6P/50V/COG_4

TP77 TP1

CN3
CRT CONN

U2 74AHCT1G125GW
U3 74AHCT1G125GW
C3 0.1U/10V_4

Place close to U8,U9 < 200 mil
VGAVSYNC_R
VGAHSYNC_R
R9 *0_4_S
R382 *0_4_S
CRTVSYNC1
CRTHSYNC1
C480 *10P/50V_4
C4 *10P/50V_4

Place close to CRT CONN < 200 mil
L26 HCB1608KF-121T20
L30 HCB1608KF-121T20
CRTVSYNC
CRTHSYNC
C467 10P/50V_4
C460 10P/50V_4

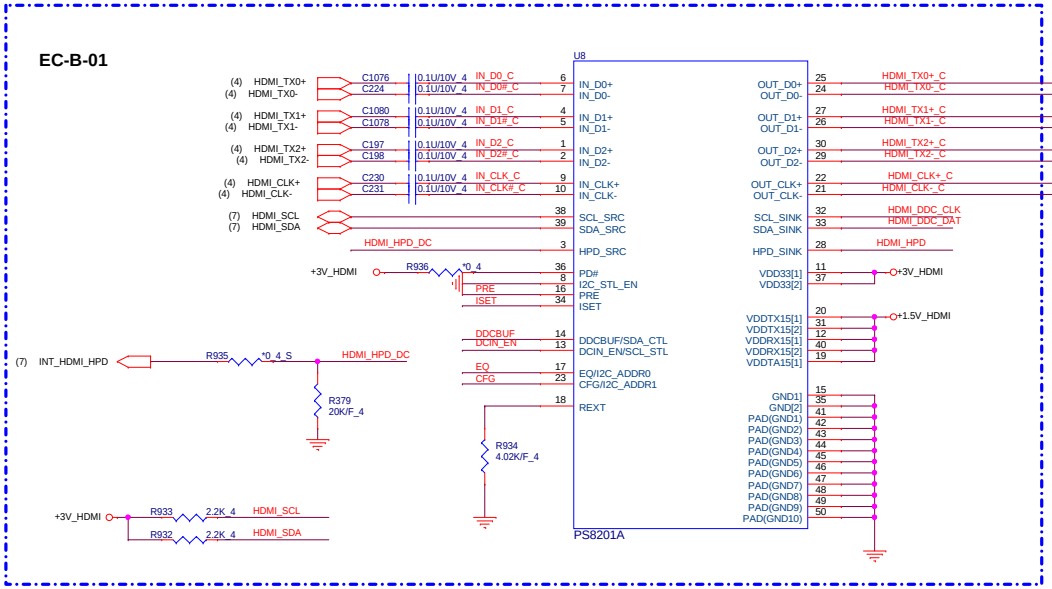
+3V
R383 2.2K_4
R389 2.2K_4
R377 4.7K_4
R378 4.7K_4
Q23A 2N7002KDW
Q23B 2N7002KDW
DDCCLK
DDCDAT
C465 *10P/50V_4
C466 *10P/50V_4

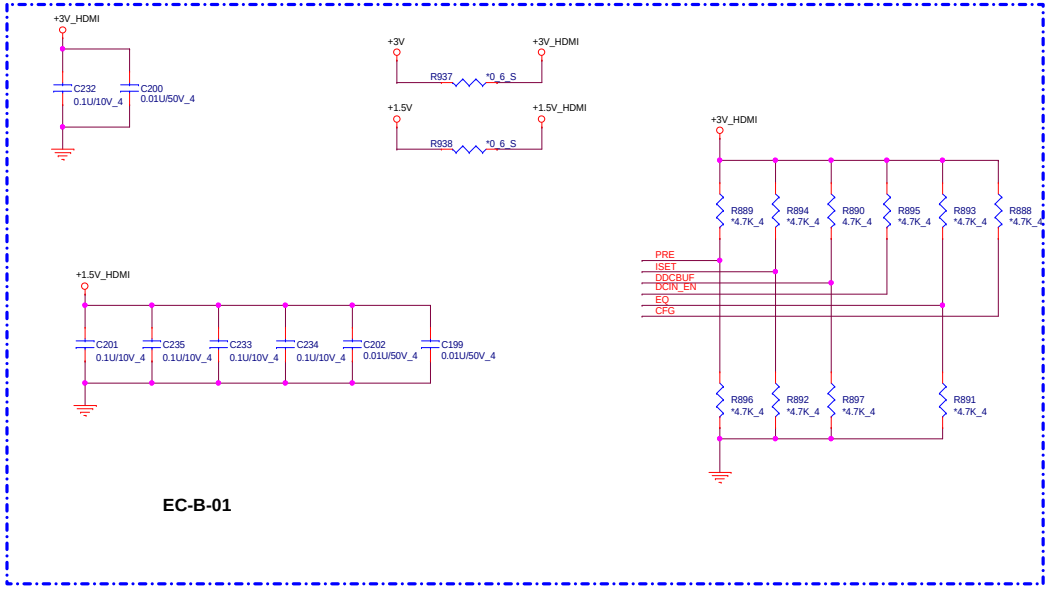
For ESD
U23 *IP4220CZ6
U22 *IP4220CZ6
CRT_R1
CRT_G1
CRT_B1
DDCDAT
DDCCLK
CRTVSYNC
CRTHSYNC
TP1
CRT_VCC

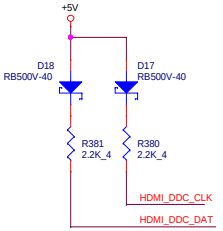
PROJECT : NL8A
Quanta Computer Inc.

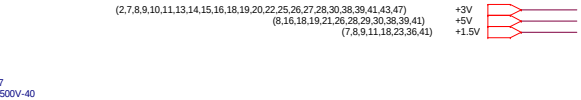
Size	Document Number	Rev
Custom	CRT CONN	3B
Date: Wednesday, January 14, 2015	Sheet 16 of 58	

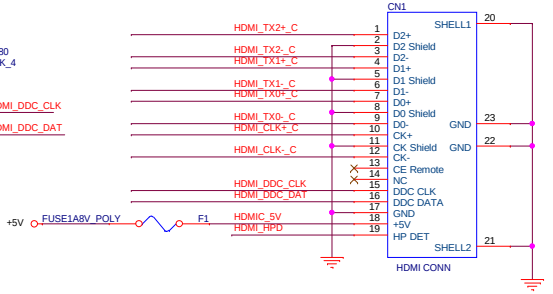
EC-B-01



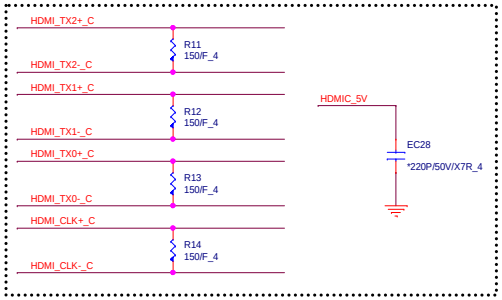


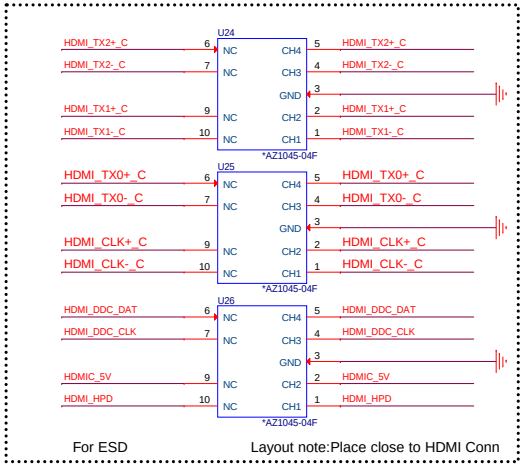






EMI reserve for HDMI





For ESD

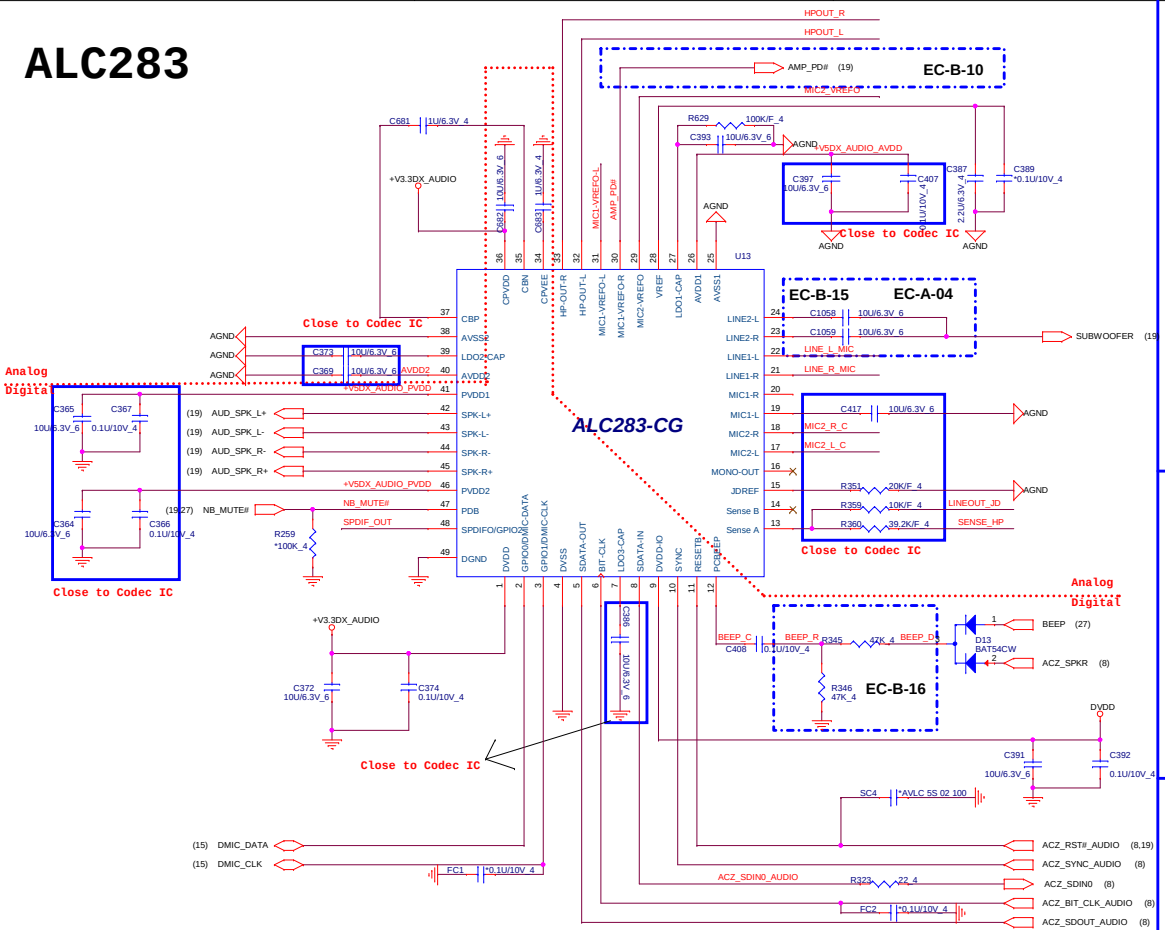
Layout note:Place close to HDMI Conn

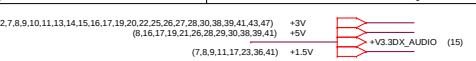
PROJECT : NL8A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI CONN	3B
Date: Wednesday, January 14, 2015	Sheet 17 of 58	

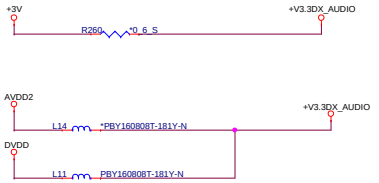
ALC283

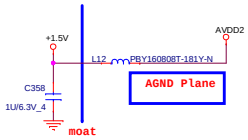




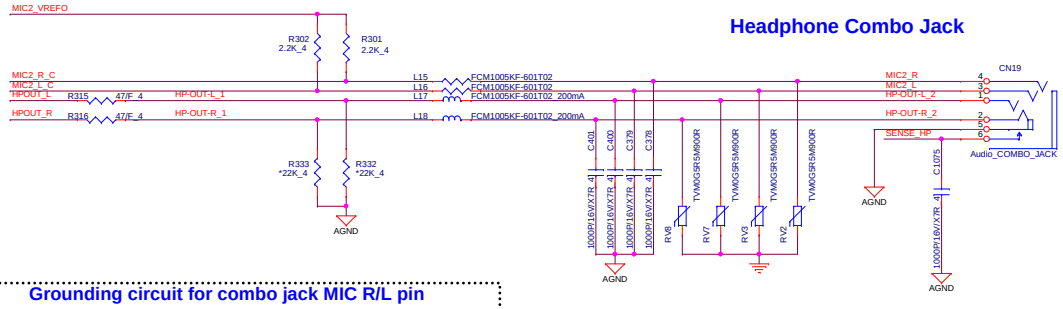
CODEC 5V POWER

+3.3V_AUDIO_CODEC
Max Current : 419mA

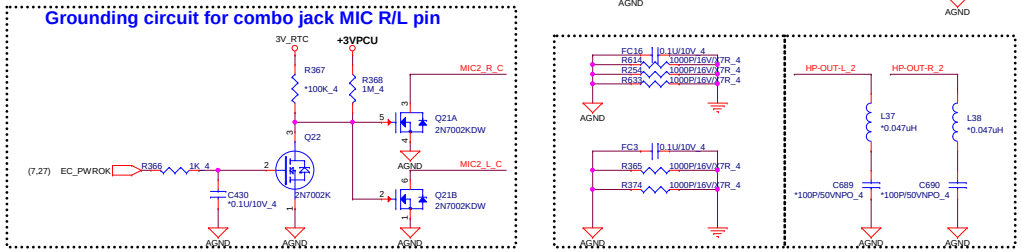




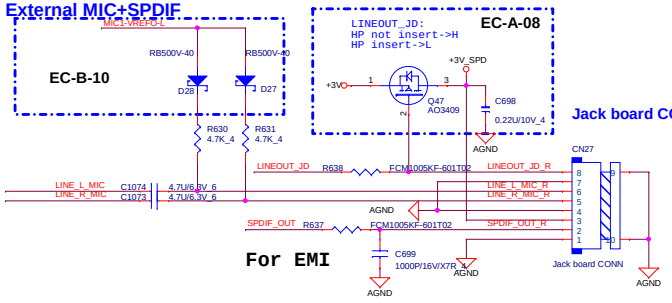
Headphone Combo Jack

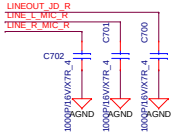


Grounding circuit for combo jack MIC R/L pin



External MIC+SPDIF





PROJECT : NL8A		
Quanta Computer Inc.		
Size: Custom	Document Number: Audio(ALC283-CG)	Rev: 3B
Date: Wednesday, January 14, 2015	Sheet 18 of 58	

Reserve for Input attenuation
To have optimization output power

Placement C4609
and then C4611

Close to IC

need to Close to connector
Reserve for EMI Depression

need to very
Close to IC

GND PAD 6 VIA (2x3)
inner 12mil, outer 20mil

EC-B-13

EC-A-05

EC-B-10

EC-B-10

EC-C-04

Output Gain Table

R364	R363	R373	R372	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

PROJECT : NL8A			
Quanta Computer Inc.			
Size: Custom	Document Number: Amplifer(ALC1003)		Rev: 3B
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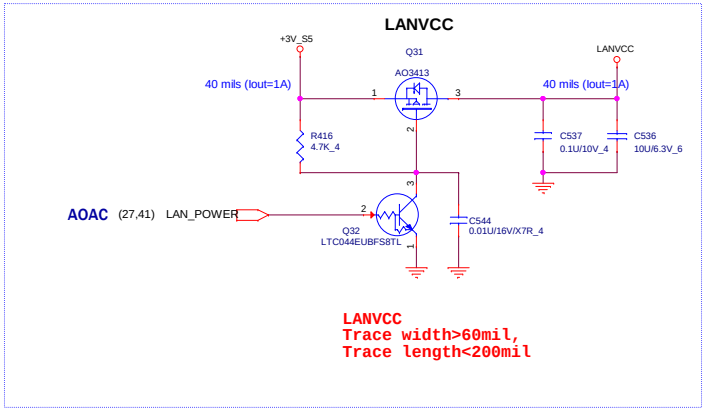
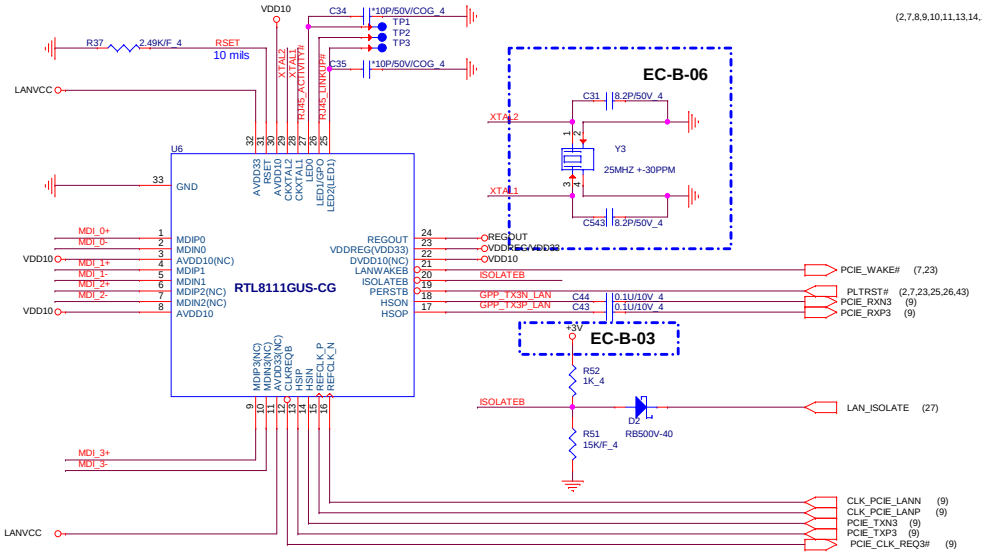
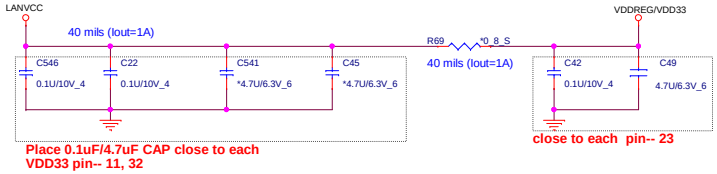
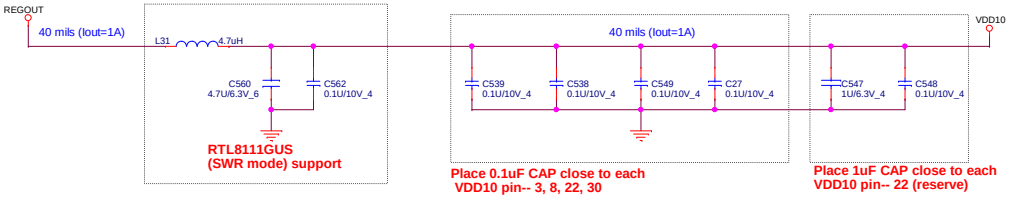


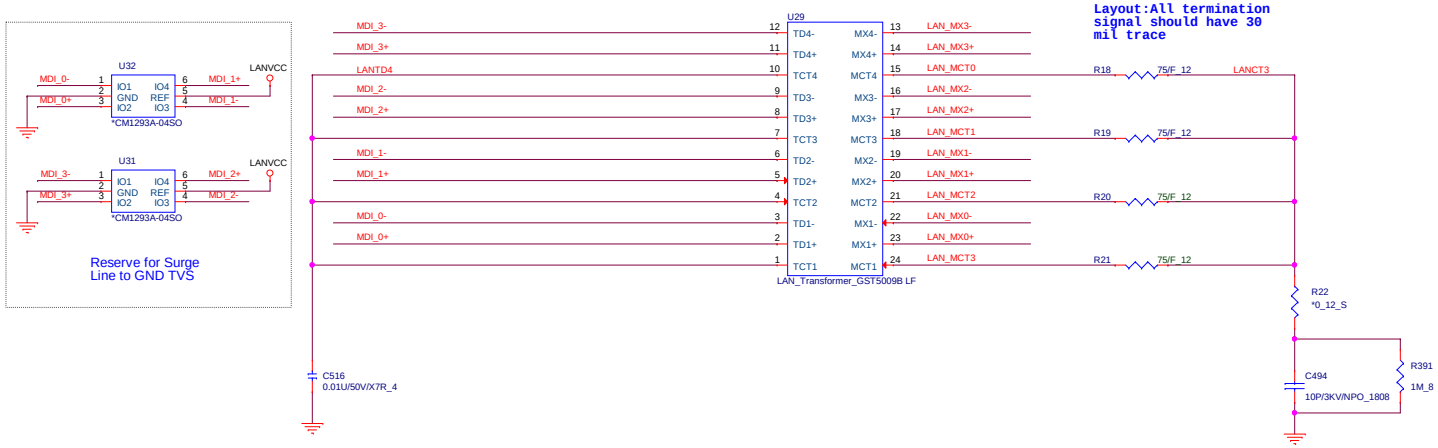


(41) LANVCC
(2,7,8,9,10,11,23,28,30,33,36,37,39,40,45,51) +3V_S5
(2,7,8,9,10,11,13,14,15,16,17,18,19,22,25,26,27,28,30,38,39,41,43,47) +3V

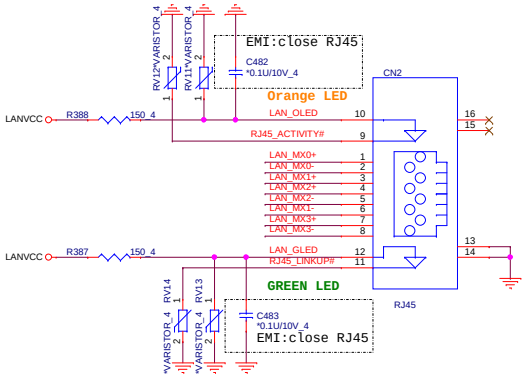




Tramsformer



RJ45 Connector

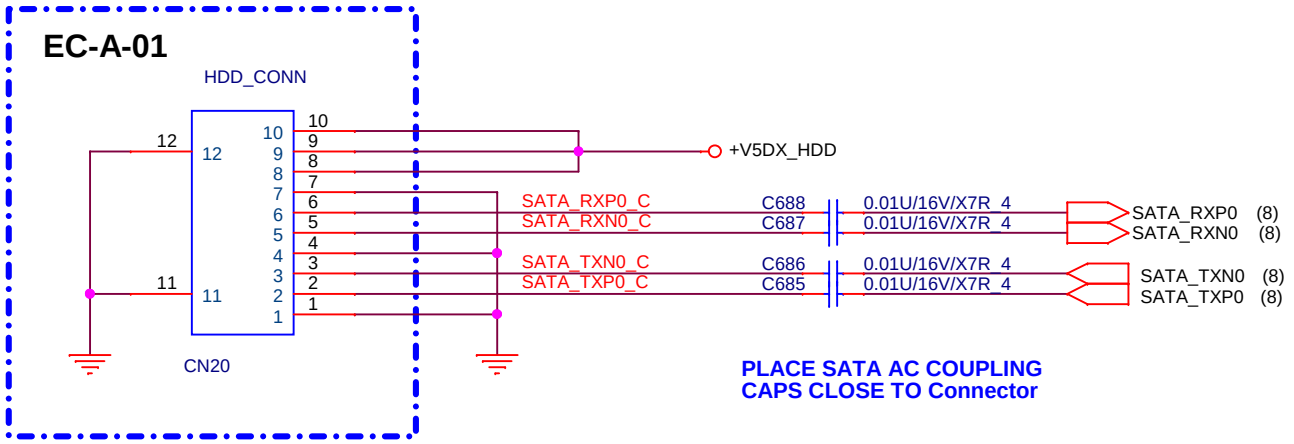


PROJECT : NL8A			
Quanta Computer Inc.			
Size: Custom	Document Number: LAN(RTL8111GUS-CG)		Rev: 3B
Date: Wednesday, January 14, 2015	Sheet 20 of 58		

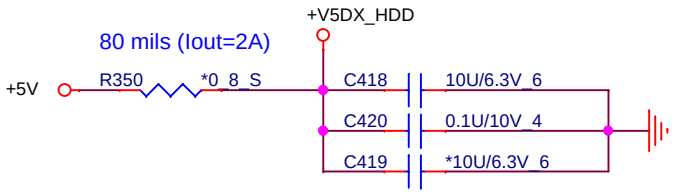
HDD

21

(8,16,17,18,19,26,28,29,30,38,39,41) +5V



DC Current rating: 2 A (MAX)



PROJECT : NL8A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD	3B
Date: Wednesday, January 14, 2015	Sheet 21 of 58	

(2,7,8,9,10,11,13,14,15,16,17,18,19,20,25,26,27,28,30,38,39,41,43,47) +3V

Mini-PCIe SSD connector

120 mils (Iout=3A)

+3V

+3.3V_SSD

R398 *0_8_S

C505 1U/6.3V_4

120 mils (Iout=3A)

+3.3V_ NGFF_WWAN
Max Current : 2750mA

CN8

1	WAKE#	3.3V_1	2
3	RESERVED_1	GND0	4
5	RESERVED_2	1.5V_1	6
7	CLKREQ#	UIM_PWR	8
9	GND1	UIM_DATA	10
11	REFCLK-	UIM_CLK	12
13	REFCLK+	UIM_RESET	14
15	GND2	UIM_VPP	16
17	UIM_C8	GND3	18
19	UIM_C4	W_DISABLE#	20
21	GND4	PERST#	22
23	PERp0	3.3VAUX1	24
25	PERn0	GND5	26
27	GND6	1.5V_2	28
29	GND7	SMB_CLK	30
31	PETn0	SMB_DATA	32
33	PETp0	GND8	34
35	GND9	USB_D-	36
37	RESERVED_3	USB_D+	38
39	RESERVED_4	GND10	40
41	RESERVED_5	LED_WWAN#	42
43	RESERVED_6	LED_WLAN#	44
45	RESERVED_7	LED_WPAN#	46
47	RESERVED_8	1.5V_3	48
49	RESERVED_9	GND11	50
51	RESERVED_10	3.3V_2	52

Mini-PCIe

(8) SATA_RXP1 — 0.01U/16V/X7R_4 — C513 — SATA_RXP1_C
(8) SATA_RXN1 — 0.01U/16V/X7R_4 — C515 — SATA_RXN1_C
(8) SATA_TXN1 — 0.01U/16V/X7R_4 — C529 — SATA_TXN1_C
(8) SATA_TXP1 — 0.01U/16V/X7R_4 — C530 — SATA_TXP1_C

T3
T4

(10) NGFF_SSD_PRESENT# — R186 *0_4_S — NGFF_SSD_PRESENT#_R

+3.3V_SSD

C534 0.1U/10V_4
C514 0.047U/10V_4
C496 0.1U/10V_4
C545 0.047U/10V_4
C495 4.7U/6.3V_6

Place caps close to connector.

10K_4 R415
*0_4_S R417 SSD_DEVSLP

EC-B-11

Mini-PCIe SSD connector

120 mils (Iout=3A)

+3V

C375 1U/6.3V_4

120 mils (Iout=3A)

+3.3V_ NGFF_WWAN
Max Current : 2750mA

CN18

1	WAKE#	3.3V_1	2
3	RESERVED_1	GND0	4
5	RESERVED_2	1.5V_1	6
7	CLKREQ#	UIM_PWR	8
9	GND1	UIM_DATA	10
11	REFCLK-	UIM_CLK	12
13	REFCLK+	UIM_RESET	14
15	GND2	UIM_VPP	16
17	UIM_C8	GND3	18
19	UIM_C4	W_DISABLE#	20
21	GND4	PERST#	22
23	PERp0	3.3VAUX1	24
25	PERn0	GND5	26
27	GND6	1.5V_2	28
29	GND7	SMB_CLK	30
31	PETn0	SMB_DATA	32
33	PETp0	GND8	34
35	GND9	USB_D-	36
37	RESERVED_3	USB_D+	38
39	RESERVED_4	GND10	40
41	RESERVED_5	LED_WWAN#	42
43	RESERVED_6	LED_WLAN#	44
45	RESERVED_7	LED_WPAN#	46
47	RESERVED_8	1.5V_3	48
49	RESERVED_9	GND11	50
51	RESERVED_10	3.3V_2	52

Mini-PCIe

(8) SATA_RXP2 — 0.01U/16V/X7R_4 — C340 — SATA_RXP2_C
(8) SATA_RXN2 — 0.01U/16V/X7R_4 — C335 — SATA_RXN2_C
(8) SATA_TXN2 — 0.01U/16V/X7R_4 — C326 — SATA_TXN2_C
(8) SATA_TXP2 — 0.01U/16V/X7R_4 — C324 — SATA_TXP2_C

T6
T5

NGFF_SSD_PRESENT#_R

+3V

C663 0.1U/10V_4
C292 0.047U/10V_4
C291 0.1U/10V_4
C336 0.047U/10V_4
C290 4.7U/6.3V_6

Place caps close to connector.

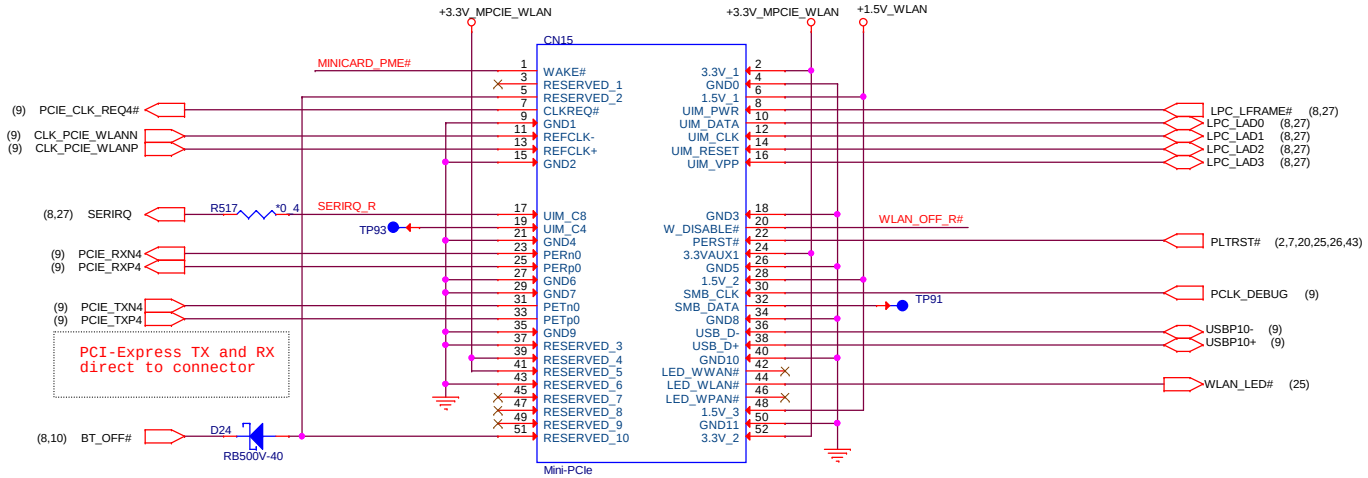
*0_4_S R191 SSD_DEVSLP — SSD_DEVSLP (9)

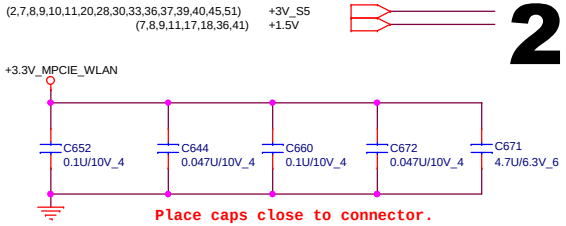
EC-B-11

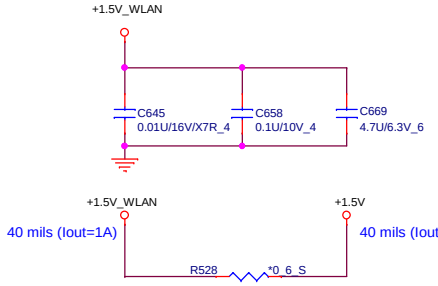
PROJECT : NL8A
Quanta Computer Inc.

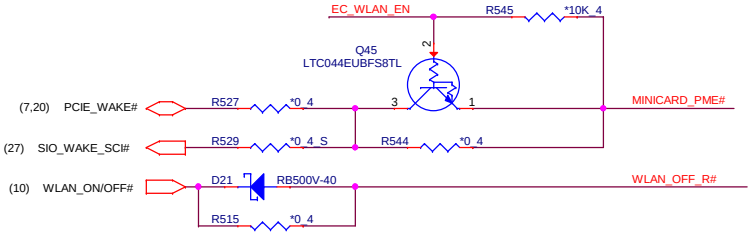
Size	Document Number	Rev
Custom	SSD mSATA X2	3B
Date: Wednesday, January 14, 2015	Sheet 22 of 58	

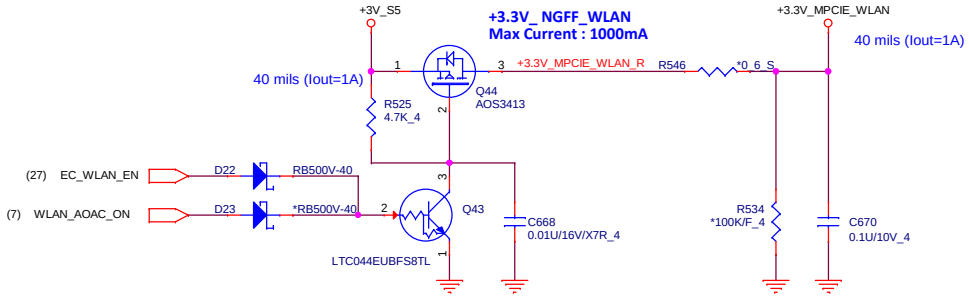
Mini PCIE Wifi/BT connector







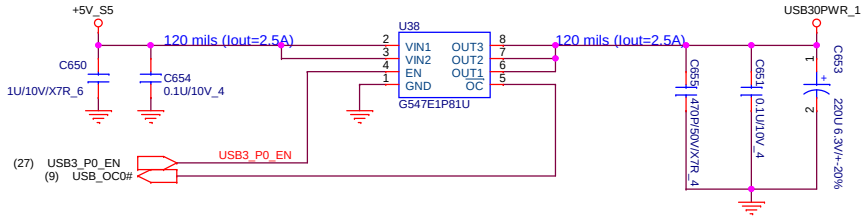


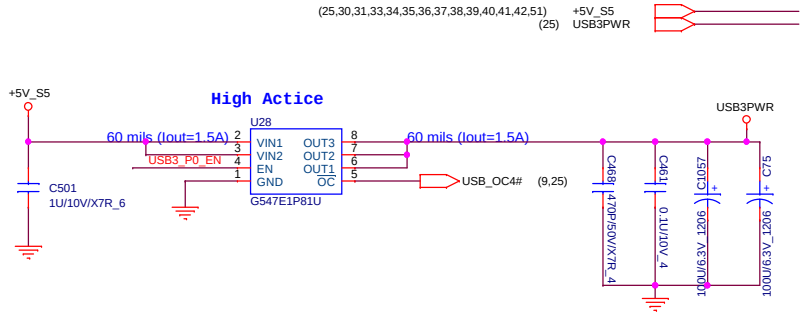


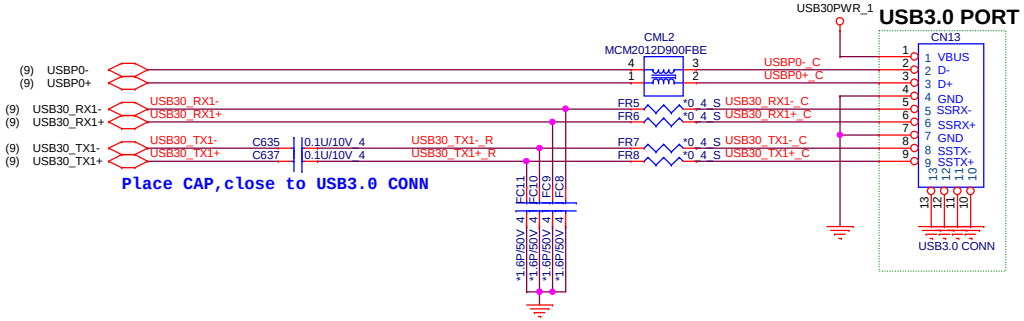
PROJECT : NL8A

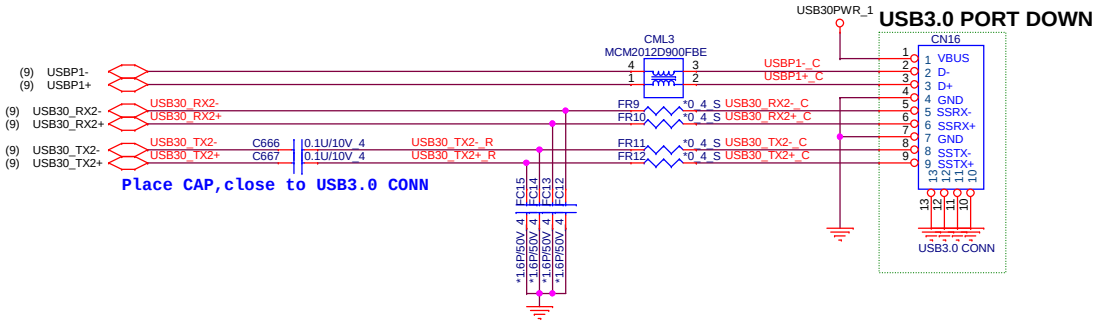
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Wifi/BT MiniPCIE	3B
Date: Wednesday, January 14, 2015	Sheet 23 of 58	

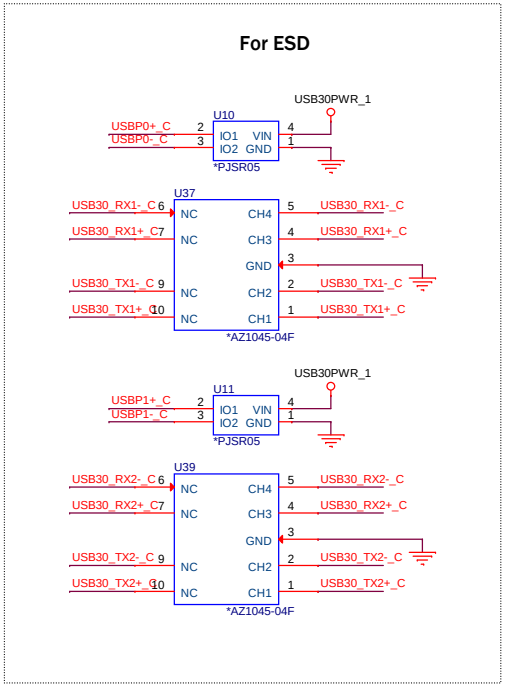




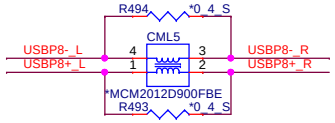


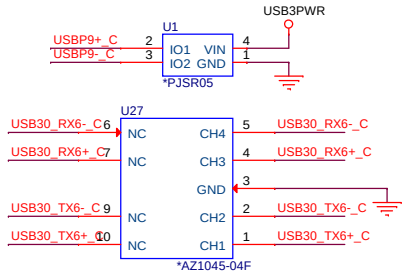


EC-A-17

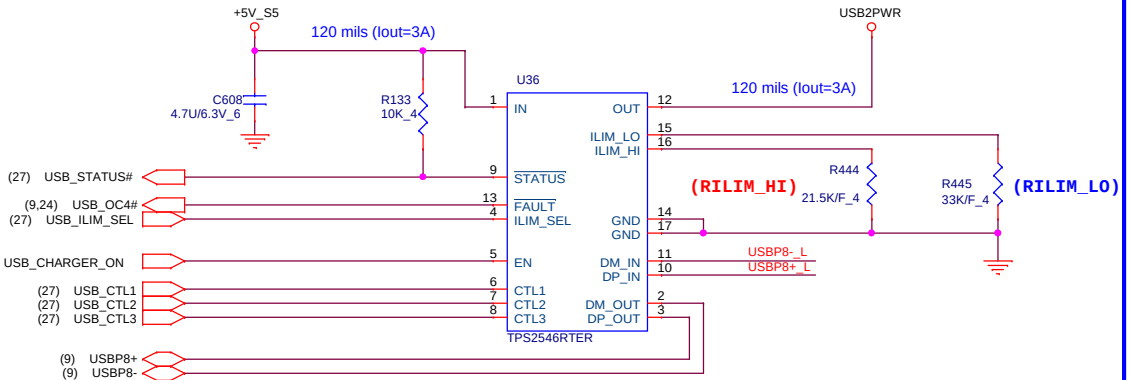


PROJECT : NL8A		
Quanta Computer Inc.		
Size: Custom	Document Number: USB3.0 X3	Rev: 3B
Date: Wednesday, January 14, 2015	Sheet 24 of 58	





USB Charger 2.0 Port

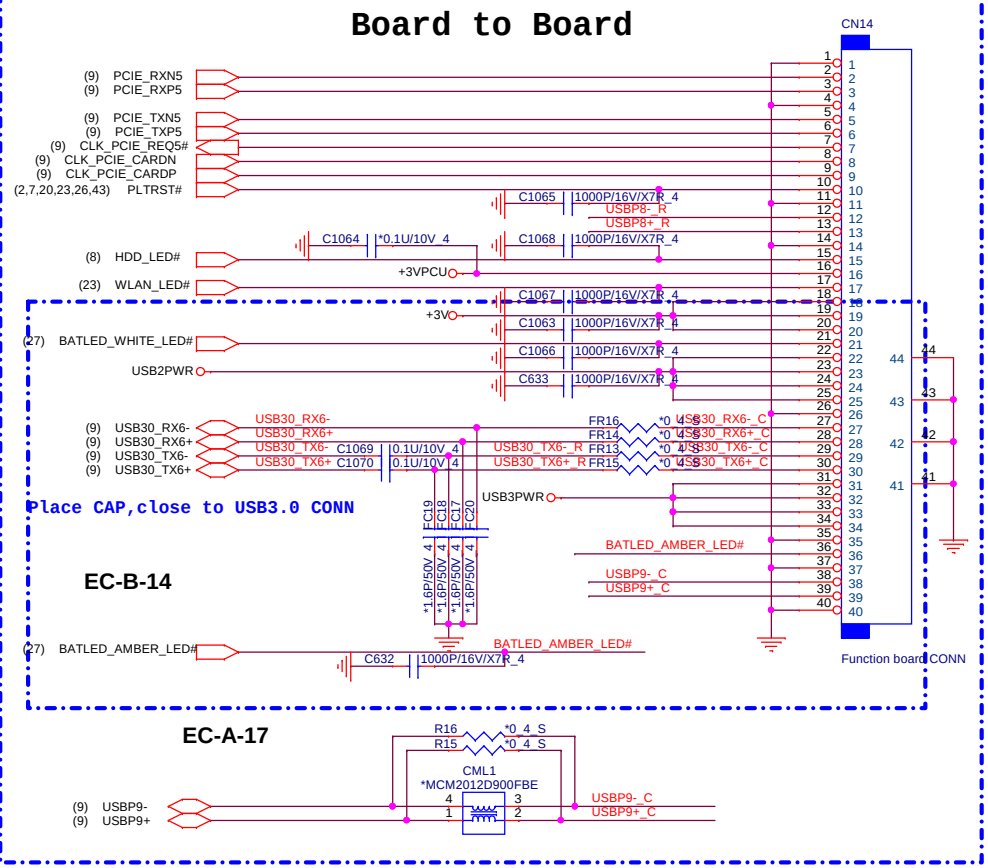


RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$I_{OS\_typ}(mA) = \frac{50{,}500}{(R_{ILIM\_XX}(k\Omega) + 0.1)}$$

(24) USB3PWR
(24,30,31,33,34,35,36,37,38,39,40,41,42,51) +5V_S5
(2,7,8,9,10,11,13,14,15,16,17,18,19,20,22,26,27,28,30,38,39,41,43,47) +3V

Board to Board



EC-A-17

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Quanta Computer Inc.

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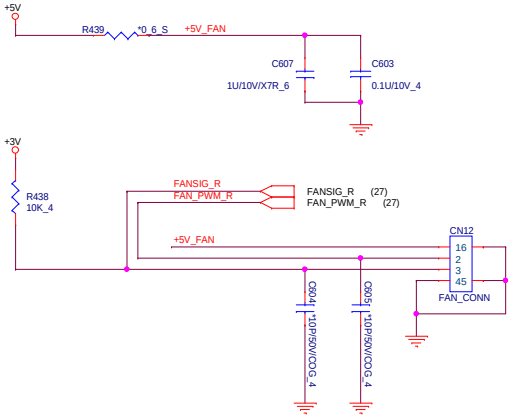
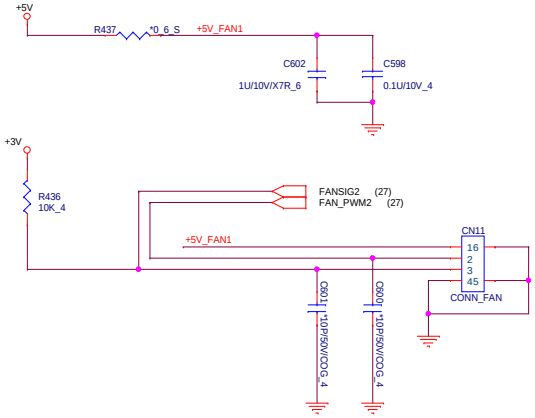
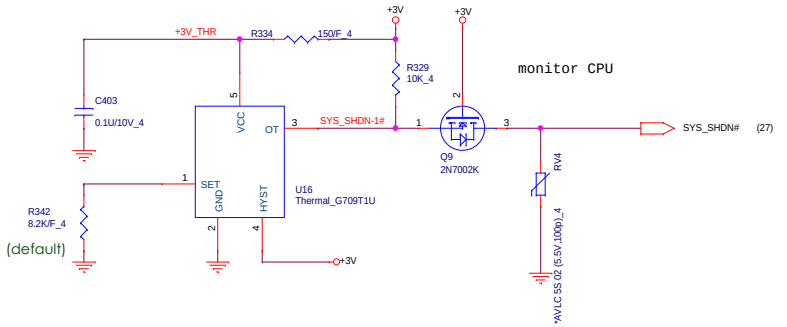
FAN CONTROL

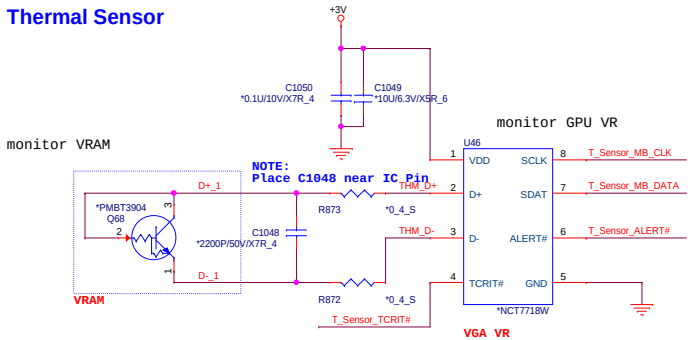




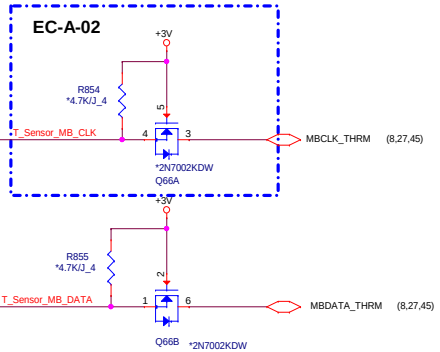
Thermal Sensor

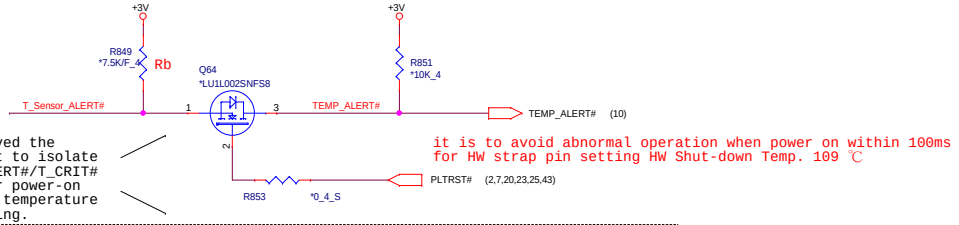


Thermal Sensor



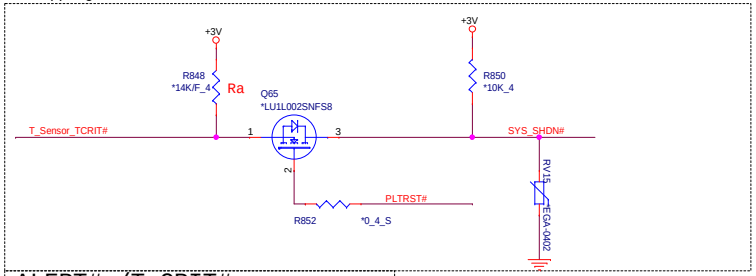
ADDRESS: 98





*Reserved the circuit to isolate the ALERT#/T_CRIT# pin for power-on T_CRIT temperature strapping.

it is to avoid abnormal operation when power on within 100ms for HW strap pin setting HW Shut-down Temp. 109 ℃



ALERT# /T_CRIT# Pull-up Resistor

Rb \ Ra	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

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(8,11,18) 3V_RTC
(2,7,8,9,10,11,13,14,15,16,17,18,19,20,22,25,26,28,30,38,39,41,43,47) +3V
(8,15,18,25,28,32,33) +3VPCU

RTC_VCC
3V_RTC
R258 *0_4_S
R275 *0_4

Layout Note:
net "+3.3V_ALW2" and "RTC_VCC"
minimum trace width 12mils.

Layout Note:
Place all capacitors close to IT8512.

IT8512_VSTBY
C363 0.1U/10V_4
C362 0.1U/10V_4
C359 0.1U/10V_4
C380 0.1U/10V_4
C459 0.1U/10V_4
C422 0.1U/10V_4

+3VPCU
L20 10_6
IT8512_AVCC
C409 100P/50V/NPO_4
C411 1000P/16V/X7R_4
C410 1U/6.3V_4
L19 BLM15AG121SN1D

For EMI, Close EC. pin74

IT8512_VSTBY
L10 BLM15AG121SN1D
+3VPCU
C360 0.1U/10V_4
(For PLL Power)

+3V
R282 *0_4_S
+3.3V_RUN_EC
C376 0.1U/10V_4

RTC_VCC

CLK_33M_KBC
C384 *15P/50V/NPO_4

EMI suggestion:
Add a 15p bypass
CAP on CLK_PCI_8512

EC-F-01

IT8587

U15
IT8587E/FX

LPC
(8,23) LPC_LAD0
(8,23) LPC_LAD1
(8,23) LPC_LAD2
(8,23) LPC_LAD3
(15,28) LID#
(9) CLK_33M_KBC
(8,23) LPC_LFRAME#
(34,35,36,39) MAINON
(10) EC_A20GATE
(8,23) SERIRQ
(10) SIO_EXT_SMI#
(10) SIO_EXT_SCI#
(40) EC_RCIN#
(28,45) FB_CLAMP_TGL_REQ#
CLK_33M_KBC
WRST_8512#
D11 RB500V-40
D15 RB500V-40
D9 RB500V-40
LAD0/GPM0(X)
LAD1/GPM1(X)
LAD2/GPM2(X)
LAD3/GPM3(X)
LCRST#/WUI4/GPD2(Up)
LPCCLK/GPM4(X)
LFRAME#/GPM5(X)
LPCPD#/WUI6/GPE6(Dn)
GA20/GPB5(X)
SERIRQ/GPM6(X)
ECSMI#/GPD4(Up)
ECSCI#/GPD3(Up)
WRST#
KBRST#/GPB6(X)
PWUREQ#/BBO/SMCLK2ALT/GPC7(Up)/SMCLK2ALT

GPIO
EGCLK/WUI27/GPE3(Dn)
EGCS#/WUI26/GPE2(Dn)
EGAD/WUI25/GPE1(Dn)
L80HLAT/BAO/WUI24/GPE0(Dn)
L80LLAT/WUI7/GPE7(Up)
WUI42/GPH6/ID6(Dn)
WUI41/GPH5/ID5(Dn)
WUI40/GPH4/ID4(Dn)
WUI39/GPH3/ID3(Dn)
WUI16/GPH0/ID0(Dn)
CLKRUN#/WUI16/GPH0/ID0(Dn)

SM BUS
SMCLK0/GPB3(X)
SMDAT0/GPB4(X)
SMCLK1/GPC1(X)
SMDAT1/GPC2(X)
PECI/SMCLK2/WUI22/GPF6(Up)
SMDAT2/WUI23/GPF7(Up)

PS/2
PS2CLK0/TMB0/CEC/GPF0(Up)
PS2DAT0/TMB1/GPF1(Up)
PS2CLK2/WUI20/GPF4(Up)
PS2DAT2/WUI21/GPF5(Up)

CLKRUN#_R
R278 *0_4_S
CLKRUN# (7)

MBCLK (32)
MBDATA (32)
MBCLK_THRM (8,26,45)
MBDATA_THRM (8,26,45)
H_PECI (2,10)
NB_MUTE# (18,19)
R238 43_4
R311 10K_4
R303 10K_4
+3V

LAN_ISOLATE (20)
USB_ILIM_SEL (25)
TPCLK (28)
TPDATA (28)

CIR
S5_ON
(20,41) LAN_POWER
CRX0/GPC0(Dn)
CTX0/TMA0/GPB2(Dn)

RB500V-40
D12
(7) SIO_PWRBTN#
(34,41) SUSON
(7) RSMRST#
(32) BATSHIP
(28) USER3_BTN#
(23) EC_WLAN_EN
(25) BATLED_AMBER_LED#
(25) BATLED_WHITE_LED#
SIO_PWRBTN#_R
SYS_PWROK_EC

UART port
DAC4/DCD0#/GPJ4(X)
DSR0#/GPC6(X)
GINT/CTS0#/GPD5(Up)
PS2DAT1/RTS0#/GPF3(Up)
DAC5/RIG0#/GPJ5(X)
PS2CLK1/DTR0#/GPF2(Up)
TXD/SOUT0/GPB1(Up)
RXD/SIN0/GPB0(Up)

SUB_MUTE#
(19) SUB_MUTE#
(37) VCORE_IMON_EC
(28) USER2_BTN#
(25) USB_CHARGER_ON
(7,45) AC_PRESENT
(7) SUSWARN#EC
(7) SLP_S4#
(24) USB3_P0_EN
ADC5/DCD1#/WUI29/GPI5(X)
ADC6/DSR1#/WUI30/GPI6(X)
ADC7/CTS1#/WUI31/GPI7(X)
RTS1#/WUI5/GPE5(Dn)
PWM7/RIG1#/GPA7(Up)
DTR1#/SBUSY/GPG1/ID7(Dn)
CTX1/WUI18/SQUT1/GPH2/SMDAT3/ID2(Dn)
CRX1/WUI17/SIN1/SMCLK3/GPH1/ID1(Dn)

EXTERNAL SERIAL FLASH
FSCK/GPG7
FSCE#/GPC3
FMOSI/GPG4
FMISO/GPG5

SPI ENABLE
KSO16/SMOSI/GPC3(Dn)
KSO17/SMISO/GPC5(Dn)
PWM6/SSCK/GPA6(Up)
SSCE0#/GPG2(X)
SSCE1#/GPG0(X)
(8) 8512_SCK
(8) 8512_SCE#
(8) 8512_SI
(8) 8512_SO
(28) LED_ON/OFF_BTN#
(28) USER1_BTN#
BOARD_ID
TP68
GPG2
RB500V-40
D7
(8) ME_WR#

KBMX
KSO0/PD0
KSO1/PD1
KSO2/PD2
KSO3/PD3
KSO4/PD4
KSO5/PD5
KSO6/PD6
KSO7/PD7
KSO8/ACK#
KSO9/BUSY
KSO10/PE
KSO11/ERR#
KSO12/SLCT
KSO13
KSO14
KSO15
MY0
MY1
MY2
MY3
MY4
MY5
MY6
MY7
MY8
MY9
MY10
MY11
MY12
MY13
MY14
MY15
(28) MY[0..15]
MX0
MX1
MX2
MX3
MX4
MX5
MX6
MX7
(28) MX[0..7]

CLOCK
CK32KE/GPJ7
CK32K/GPJ6
R250 *0_4
C381 *1U/6.3V/X5R_4
C382 0.1U/10V_4

PWM
PWM0/GPA0(Up)
PWM1/GPA1(Up)
PWM2/GPA2(Up)
PWM3/GPA3(Up)
PWM4/GPA4(Up)
PWM5/GPA5(Up)
TACH0A/GPD6(Dn)
TACH1A/TMA1/GPD7(Dn)
TMRI0/WUI2/GPC4(Dn)
TMRI1/WUI3/GPC6(Dn)
HWPG
C361 *0.1U/10V_4

WAKE UP
PWRSW/GPE4(Up)
RI1#/WUI0/GPD0(Up)
RI2#/WUI1/GPD1(Up)
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7(Dn)

A/D D/A
ADC0/GPI0(X)
ADC1/GPI1(X)
ADC2/GPI2(X)
ADC3/GPI3(X)
ADC4/WUI28/GPI4(X)
TACH2/GPJ0(X)
GPJ1(X)
DAC2/TACH0B/GPJ2(X)
DAC3/TACH1B/GPJ3(X)

VGA_OVT# → VGA_OVT# (45)
SIO_WAKE_SCI# → SIO_WAKE_SCI# (23)
S5_ON_5V → S5_ON_5V (38)
EC_PWROK → TP_WHITE# (28), EC_PWROK (9,16)

EC-F-02

USB_CTL3 (25)
USB_CTL2 (25)
USB_CTL1 (25)
USB_STATUS# (25)

EC-E-02

PWR_WHITE# (28)
BREATHE_LED# (28)
FAN_PWM_R (26)
KB_LIGHT (28)
FAN_PWM2 (26)
BEEP (18)

FANSIG_R (26)
TP_RED# (28)
ADIN# (30)
HWPG (7,31,33,34,35,36)

EC-F-02

NBSWON# (28)
SIO_SLP_S3# (7)
ACIN (32)

FB_CLAMP
R866 *0_4
FB_CLAMP (31,42,46,51)

USER5_BTN# (28)

EC-F-01

R369 *0_4_S
GPU_SELECT_EC
USER_LED_ON/OFF
USER4_BTN# (28)

EC-F-03

SLP_SUS# (7)
DPWROK (7)
FANSIG2 (26)

EC_SLP_S4#
R250 *0_4
VRON (37,41)
SUSACK#EC (7)

For ESD

MBCLK
MBDATA
CLK_33M_KBC
SC3 *6.8P/50V_4
SC1 *6.8P/50V_4
SC2 *6.8P/50V_4

+3VPCU
SLP_SUS_ON_GPG2 R278 10K_4
MBCLK_THRM R253 4.7K_4
MBDATA_THRM R252 4.7K_4
MBCLK R240 4.7K_4
MBDATA R239 4.7K_4
SIO_WAKE_SCI# R326 *10K_4
TEMP_MBAT R370 *100K_4

+3V
HWPG R251 10K_4
VGA_OVT# R313 10K_4

EC_PWROK R356 100K_4
S5_ON_5V R327 100K_4

EC-F-03
GC6 version

+3VPCU
R868 *DIS@10K_4
GPU_SELECT_EC
R867 *UMA@10K_4

H_PROCHOT# (2,30,37)
H_PROCHOT_EC
R328 100K_4
Q10 2N7002K

+3V
R361 4.7K_4
Q16 AO3413
C428 0.1U/10V_4
C421 2200P/50V/X7R_4
USER_LED_ON/OFF
Q19 LTC044EUBFS8TL
USER_LED_ON/OFF_R (28)

For EC E-flash(embedded flash) auto load code

+3VPCU
C385 *0.1U/10V_4
C383 *0.1U/10V_4
R280 *10K_4
SLP_SUS_ON_GPG2
ACIN
U12 *TC7SH08FU
S5_ON
DSW_LOAD_CODE
D8 RB500V-40
D10 RB500V-40
S5_ON_C (33)
R300 *100K/F_4
R237 100K/F_4
R249 100K/F_4
R277 *0_4_S
GPG2
R279 *0_4_S
SLP_SUS_ON_GPG2
SLP_SUS_ON_GPG2 (11)

Note:
IT8587 with 128K-byte e-flash
Auto load code condition:
1. Let PCH SPI interface in High-Z state.
2. RSMRST# pull low
(PCH SPI pins are tri-stated prior to RSMRST# de-assertion)
3. EC pin 100(GPG2) pull high(force EC load code)
4. Supply power to SPI flash ROM,PCH(VCCSPI,+1.05V_SUS) and EC

POWER SWITCH

POWER SWITCH For Bring Up Test
placement in BOT side

SW1
*Power-BUTTON
EC-C-01
NBSWON#
+3VPCU
R608 10K_4
C684 0.1U/10V_4

EC Board ID

+3VPCU
R357 DIS@10K_4
BOARD_ID
R358 *UMA@10K_4

Thermal reset function

+3V
+3VPCU
TP72
R355 4.7K_4
R325 100K_4
WRST_8512#
EC_PWROK
D14 RB500V-40
Q15 METR3904-G
C390 1U/6.3V_4
(26) SYS_SHDN#

EC reset function, press power button 8 sec

+3VPCU
R335 *10_6
RST_IC_VCC
C394 *0.1U/10V_4
WRST_8512#
R354 *4.7K_4
R324 *10K_4
Q14 *MMBT3904-7-F
D16 *RB500V-40
EC_PWROK
EC_8S_RST#
NBSWON#
U17
MRDLY VCC
GND RESET#
CD MR#
*G677L308A31U
C402 *0.1U/10V_4
C413 *0.1U/10V_4

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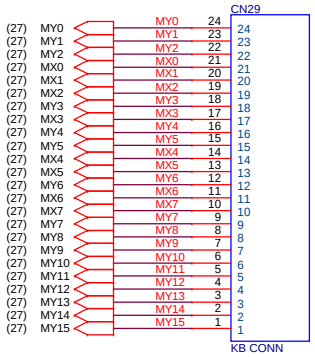
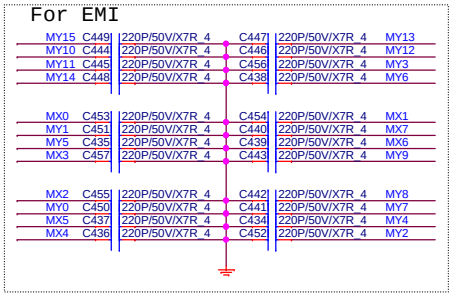
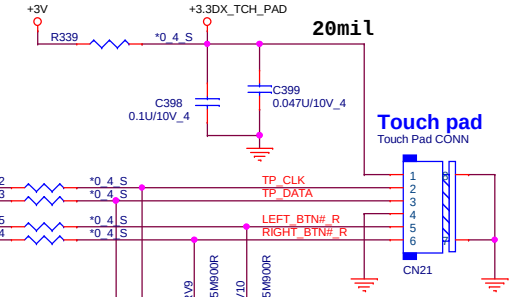
KEYBOARD



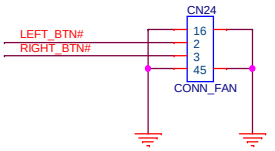


(8,16,17,18,19,21,26,29,30,38,39,41) +5V
(2,7,8,9,10,11,13,14,15,16,17,18,19,20,22,25,26,27,30,38,39,41,43,47) +3V
(8,15,18,25,27,32,33) +3VPCU
(2,7,8,9,10,11,20,23,30,33,36,37,39,40,45,51) +3V_S5

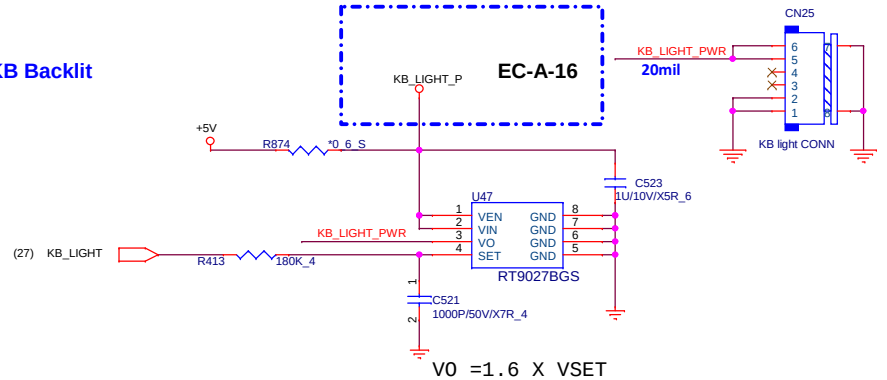
+3V_TP
Max Current : 50mA



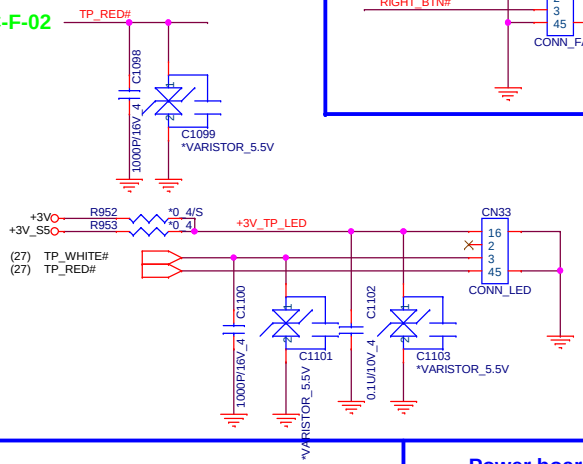
Touch button connector



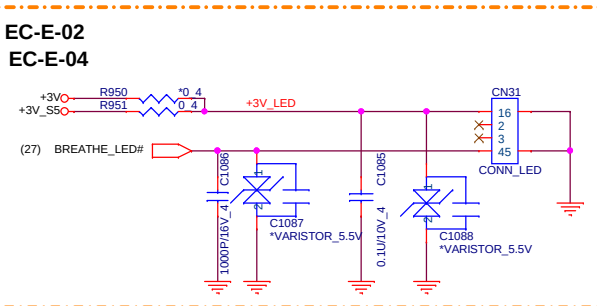
KB Backlit



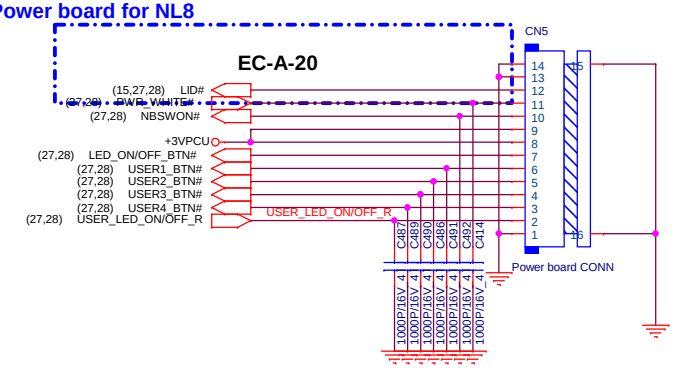
EC-F-02



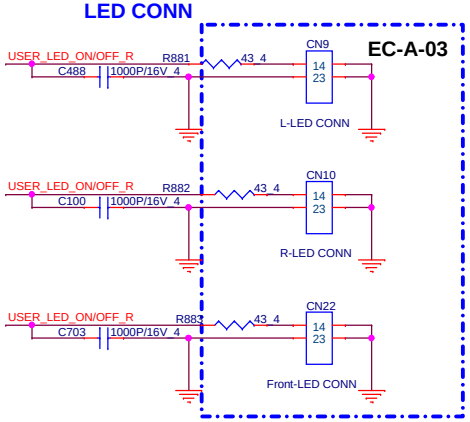
EC-E-02
EC-E-04



Power board for NL8



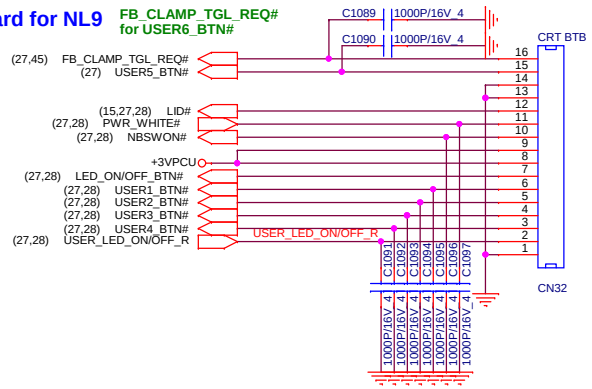
LED CONN



Power board for NL9

EC-F-01

FB_CLAMP_TGL_REQ# for USER6_BTN#



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Quanta Computer Inc.

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(8,16,17,18,19,21,26,28,30,38,39,41) +5V
(15,30,31,32,33,34,35,37) +VIN

CPU BRACKET

INTEL-CPU-BKT3

H3
*INTEL-CPU-BKT3

H37
*h-c83d83n

H23
*HG-TC236BC315D110P2

H17
*HG-TC236BC315D110P2

H6
*hg-ts2bc236d110p2

H7
*spad-nl8-2np

H8
*hg-ts3bc315d110p2

H9
*spad-nl8-2np

H10
*hg-ts1bc236d110p2

H11
*spad-c315np

H20
*HG-C315D110P2

H22
*H-TC236IC150BC315D110P2

H15
*O-NL8-4

H14
*h-c83d83n

H25
*spad-nl8-1np

H24
*h-o102x83d102x83n

H16
*HG-C315D110P2

H18
H-TC197IC87BC47D47P2

H19
H-TC197IC87BC47D47P2

H21
H-TC197IC87BC47D47P2

H13
H-TC197IC87BC47D47P2

H12
*h-ts1bc83d83pt

H28
SPAD-re118x157np

H29
*SPAD-NL8-3-NP

H5
*h-tc315ic150bc150d150pt

H4
*h-tc315ic150bc150d150pt

H1
*h-tc315ic150bc150d150pt

H30
*SPAD-NL8-4-NP

H26
*spad-re196x340np

H27
*spad-re276x340np

H31
*spad-c315np

H32
*spad-c236np

H33
*spad-c236np

H35
*spad-c236np

H36
*spad-c236np

EMI

+5V

EC16	*0.1U/10V_4
EC10	*0.1U/10V_4
EC8	*0.1U/10V_4
EC6	*0.1U/10V_4
EC2	*0.1U/10V_4
EC3	*0.1U/10V_4
EC5	*0.1U/10V_4
EC1	*0.1U/10V_4
EC25	*0.1U/10V_4

+VAD

EC31	0.1U/10V_4
EC32	0.1U/10V_4
EC33	0.1U/10V_4
EC35	0.1U/10V_4
EC34	0.1U/10V_4

+VIN

EC4	0.1U/10V_4
EC7	0.1U/10V_4
EC11	0.1U/10V_4
EC26	0.1U/10V_4
EC24	0.1U/10V_4
EC27	0.1U/10V_4
EC23	0.1U/10V_4
EC17	0.1U/10V_4
EC9	0.1U/10V_4

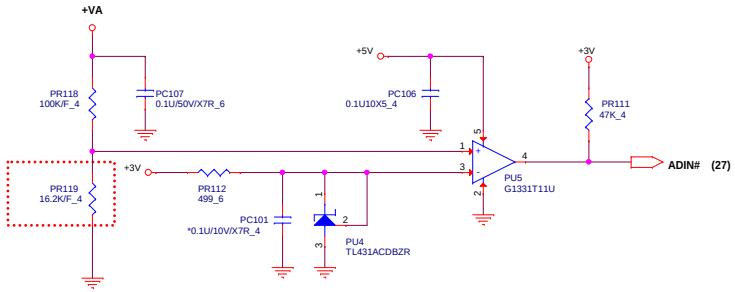
ESD

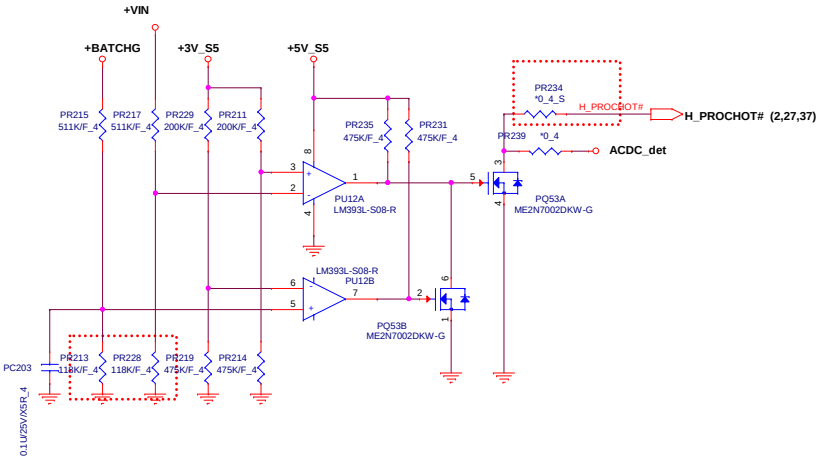
R879	*0_4_S
R876	*0_4_S
R877	*0_4_S
R878	*0_4_S

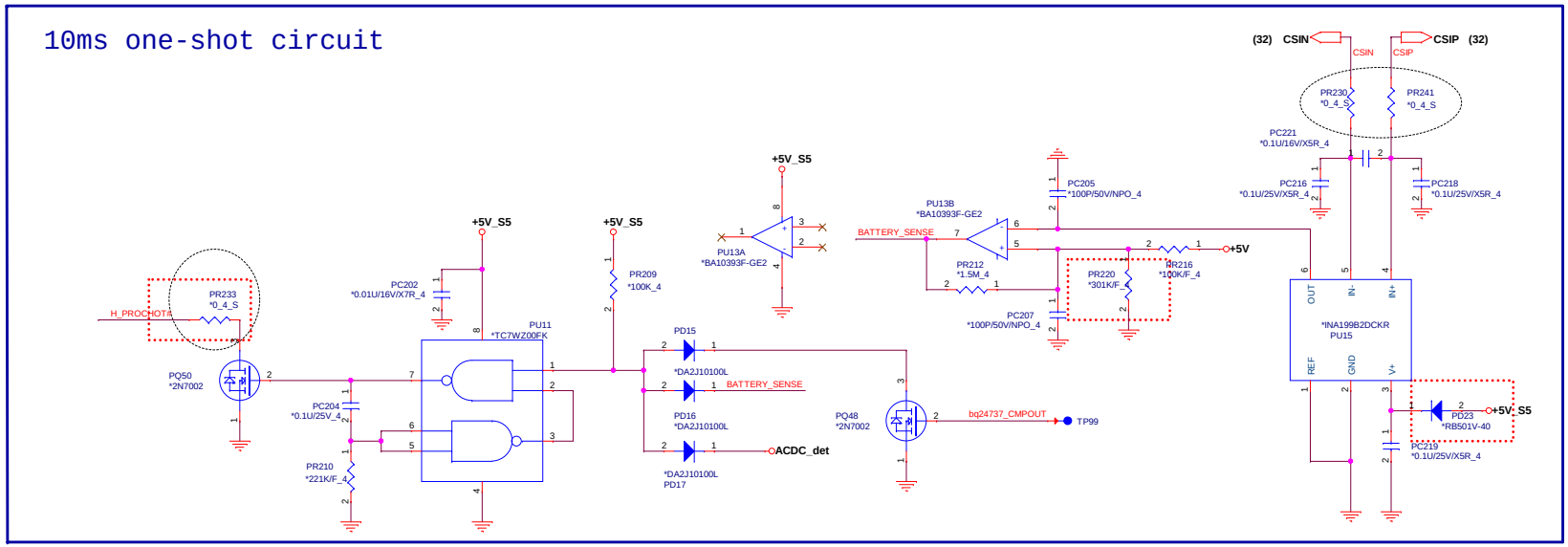
AGND

PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HOLE	3B
Date: Wednesday, January 14, 2015	Sheet 29 of 58	

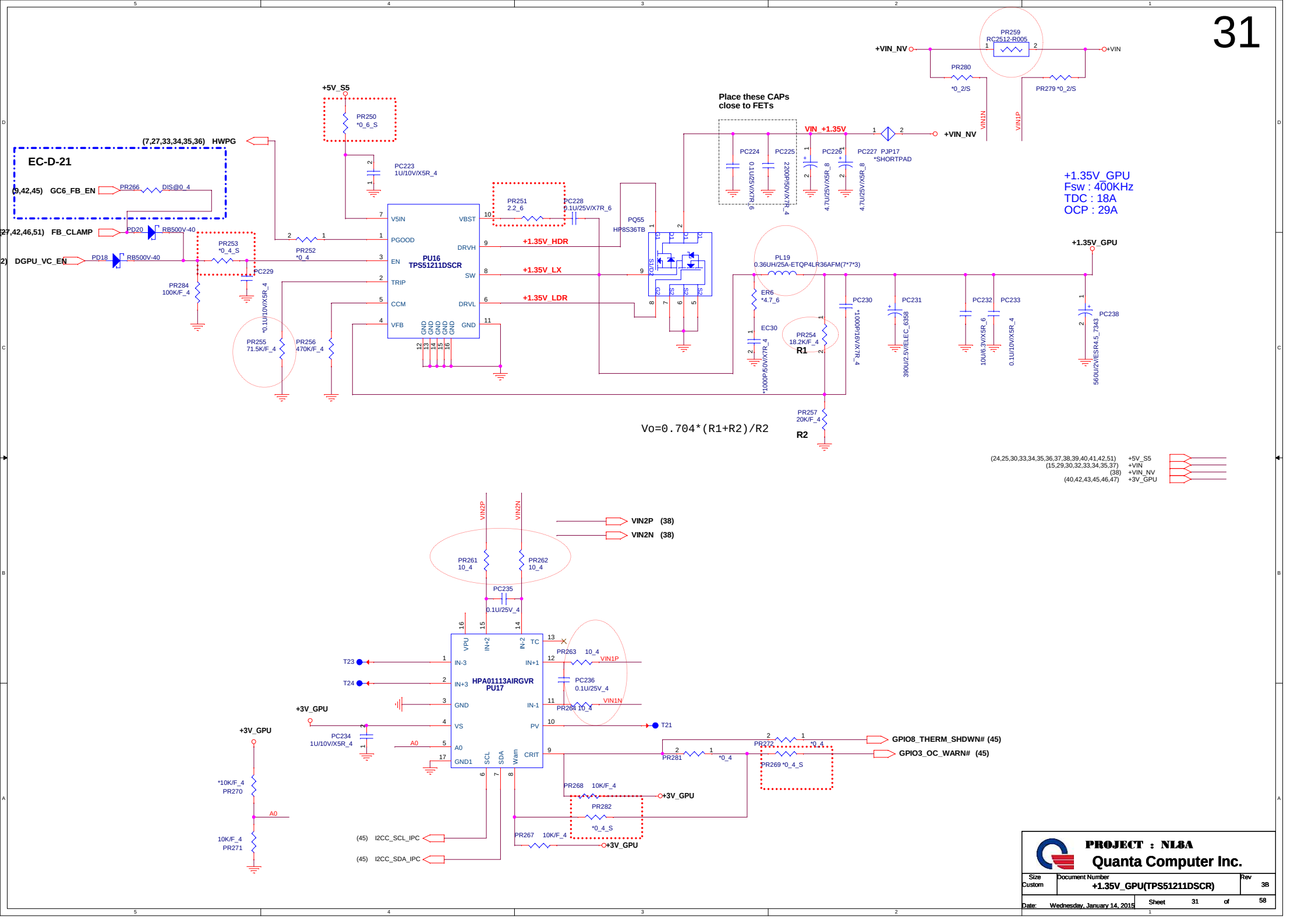




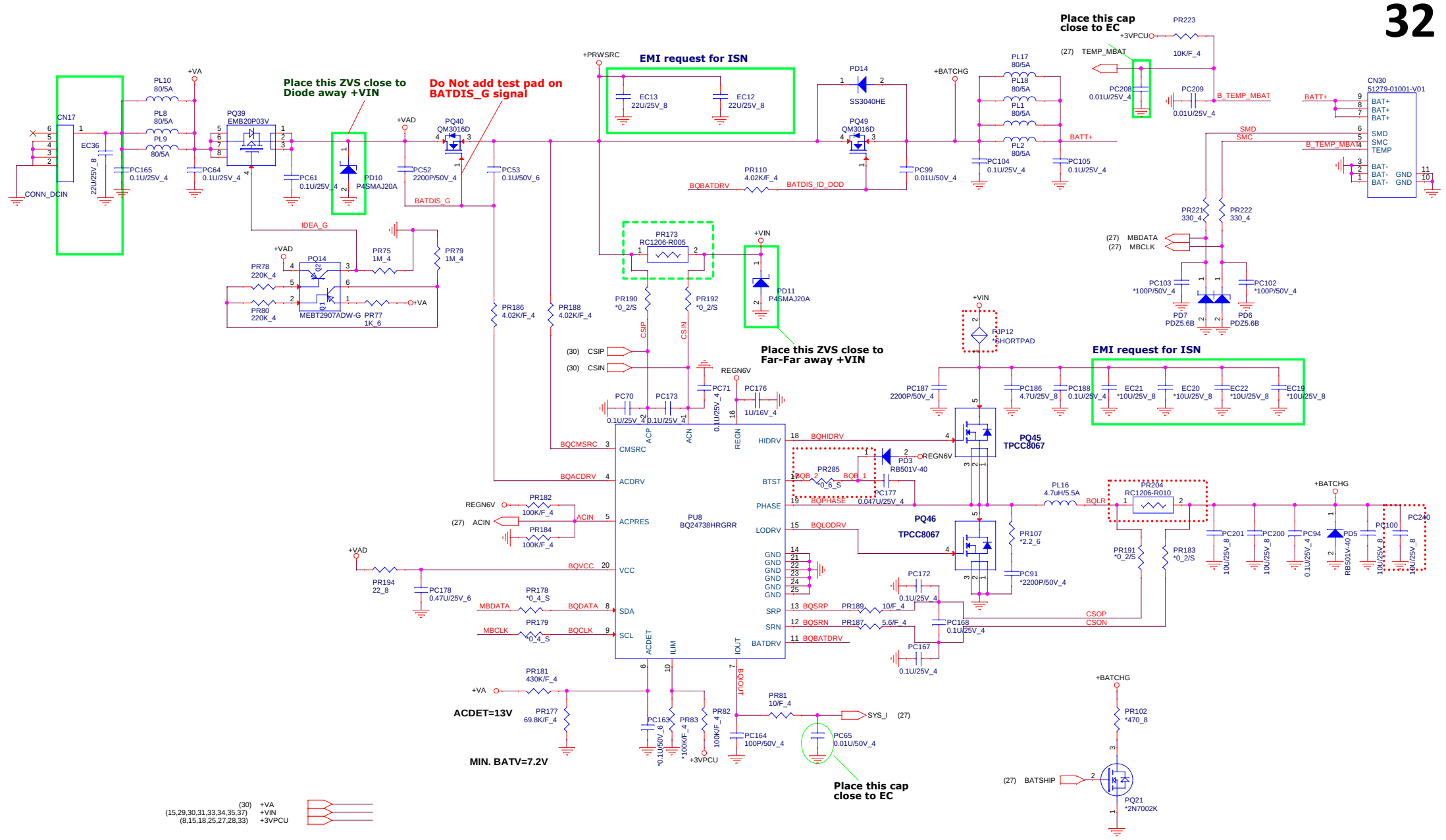


PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10ms	3B
Date: Wednesday, January 14, 2015	Sheet 30 of 58	



Quanta Computer Inc.	PROJECT : NL8A	
Size: Custom	Document Number: +1.35V_GPU(TPS51211DSCR)	Rev: 3B
Date: Wednesday, January 14, 2015	Sheet 31 of 58	



PROJECT : NL8A			
Quanta Computer Inc.			
Size: Custom	Document Number: Charger (BQ24738H)		Rev: 3B
Date: Wednesday, January 14, 2015	Sheet 32 of 58		

(15,29,30,31,32,34,35,37) +VIN
(24,25,30,31,34,35,36,37,38,39,40,41,42,51) +5V_S5
(39,40) +15V_ALW
(8,15,18,25,27,28,32) +3VPCU
(2,7,8,9,10,11,20,23,28,30,36,37,39,40,45,51) +3V_S5

5 Volt
Fsw : 400KHz
Peak : 11.3A
OCP : 15A

3.3 Volt
Fsw : 475KHz
Peak : 5.2A
OCP: 8A

Place these CAPs close to FETs

Place these CAPs close to FETs

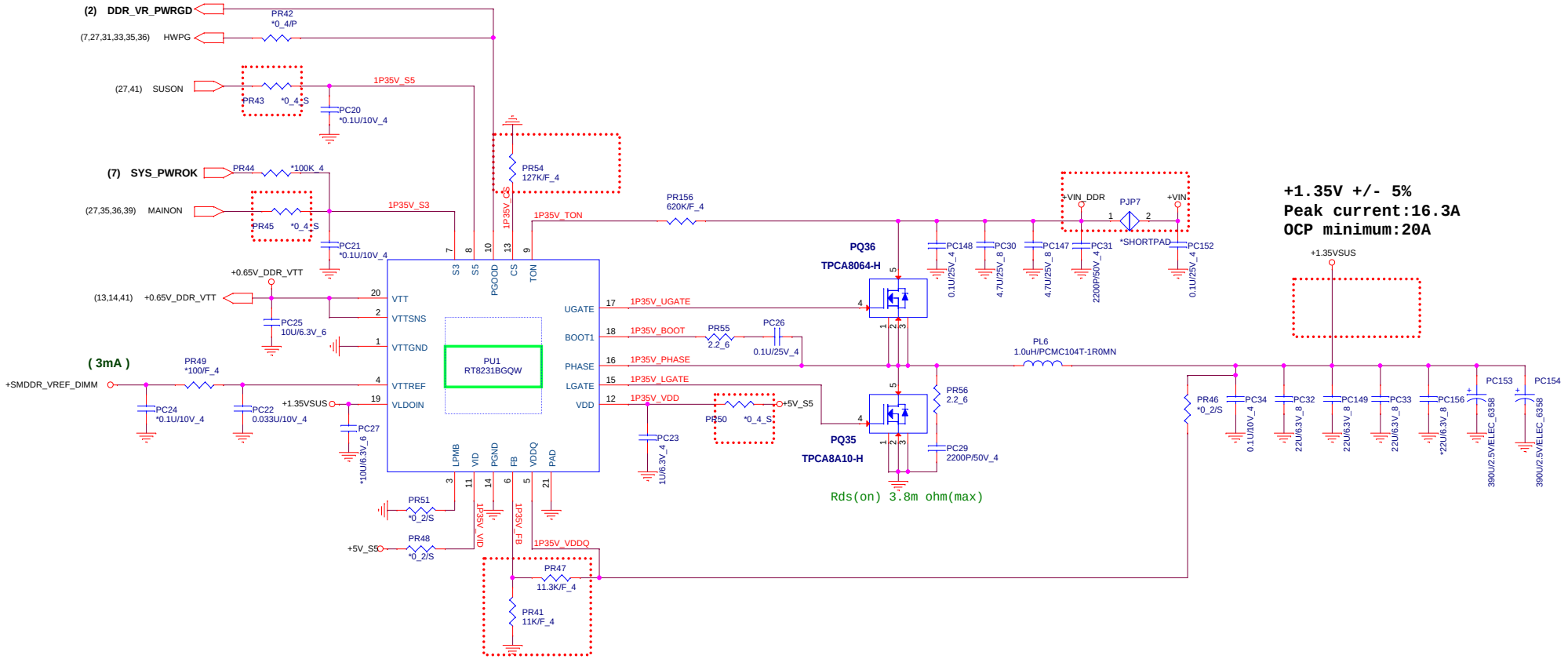
+VIN
+3VPCU
+5VPCU
+5V_S5
+3V_S5
+15V_ALW
PJP2 *SHORTPAD
PJP1 *SHORTPAD
PJP14 *SHORTPAD
PJP10 *SHORTPAD
PC100 4.7U/25V/X5R_8
PC89 4.7U/25V/X5R_8
PC92 *0.1U/25V/X5R_4
PC191 2200p/50V/X7R_4
PC87 *0.1U/25V/X5R_4
PC189 2200p/50V/X7R_4
PC69 4.7U/25V/X5R_8
PC170 4.7U/25V/X5R_8
PR200 10_8
PR99 *0_4_S
PC82
PC80 0.1U/25V/X7R_6
PC83 4.7U/6.3V/X5R_6
4.7U/10V/X5R_6
PR108 *0_4_S
PR93 *0_4_S
S5_ON_R
S5_ON_C (27)
(27) S5_ON_5V
PQ23 TPCC8067
PQ17 TPCC8067
PQ22 TPCC8065
PQ19 TPCC8065
PC93 0.1U/25V/X7R_6
PR109 2.2/F_6
PR89 2.2/F_6
PC76 0.1U/25V/X7R_6
PU3 TPS5128SBRUKR
EN1
EN2
VIN
VREG5
VREG3
DRVH1
DRVH2
VBST1
VBST2
SW1
SW2
DRVL1
DRVL2
VO1
VFB1
VFB2
PDDG
VCLK
CS1
CS2
GPAD
5V_DH
5V_BST
5V_LX
5V_DL
3.3V_DH
3.3V_BST
3.3V_LX
3.3V_DL
TPS51275_VO1
TPS51275_VFB1
TPS51275_VFB2
PL15 ETQP3W1R5WFN-1.5
PL13 NIMS0603N-2R2M
ER2 4.7_6
EC18 1000P/50V/X7R_4
ER5 4.7_6
EC29 1000P/50V/X7R_4
PC88 0.1U/10V/X5R_4
PC86 *4.7U/10V/X5R_6
PC239 150U/6.3V/ESR38_3528
PC189 330U/6.3V_6X5.8
PC174 330U/6.3V_6X5.8
PC74 4.7U/6.3V/X5R_6
PC75 0.1U/10V/X5R_4
PR101 30K/F_4
PR105 19.6K/F_4
PR106 22.1K/F_4
PR90 13K/F_4
PR97 13K/F_4
PR95 20K/F_4
PR87 *100K/F_4
PR92 *0_4_S
RV1 *AVC-SS 02 (5.9V-100)_4
HWPG (7,27,31,34,35,36)
3VS5_P
PC195 0.1U/25V/X5R_4
PR207 *0_S
VCLK
PD4 BAT54SW-L
PD13 BAT54SW-L
PC192 0.1U/25V/X5R_4
PC98 0.1U/25V/X5R_4
PR208 22_8
+15V_ALWP
PC97 0.1U/25V/X5R_4
PR196 *39K/F_4
S5_ON_R

PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3V/5V (TPS51285BRUKR)	3B

Date: Wednesday, January 14, 2015 Sheet 33 of 58

(2,5,13,14,41) +1.35VSUS
(24,25,30,31,33,35,36,37,38,39,40,41,42,51) +5V_S5
(15,29,30,31,32,33,35,37) +VIN

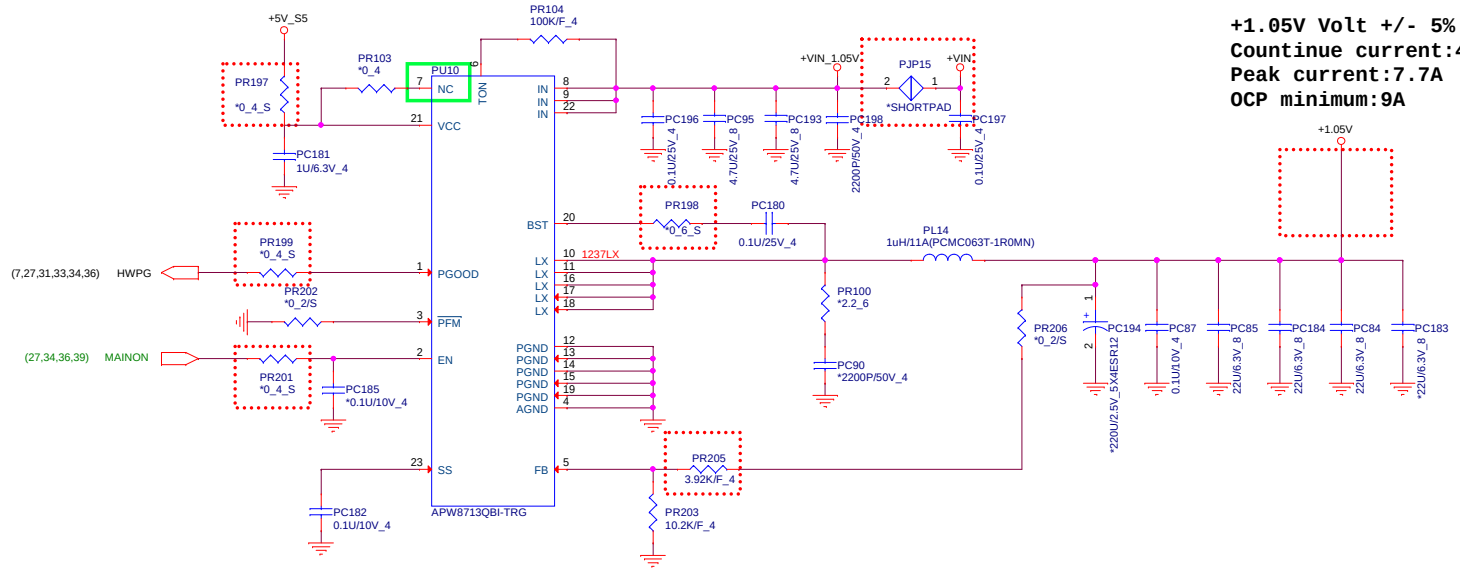


+1.35V +/- 5%
Peak current:16.3A
OCP minimum:20A

Size: Custom	Document Number: DDR3 (RT8231B)	Rev: 3B
Date: Wednesday, January 14, 2015	Sheet 34 of 58	

PROJECT : NL8A
Quanta Computer Inc.

(24,25,30,31,33,34,36,37,38,39,40,41,42,51) +5V_S5
(15,29,30,31,32,33,34,37) +VIN
(2,5,10,11,40,41) +1.05V



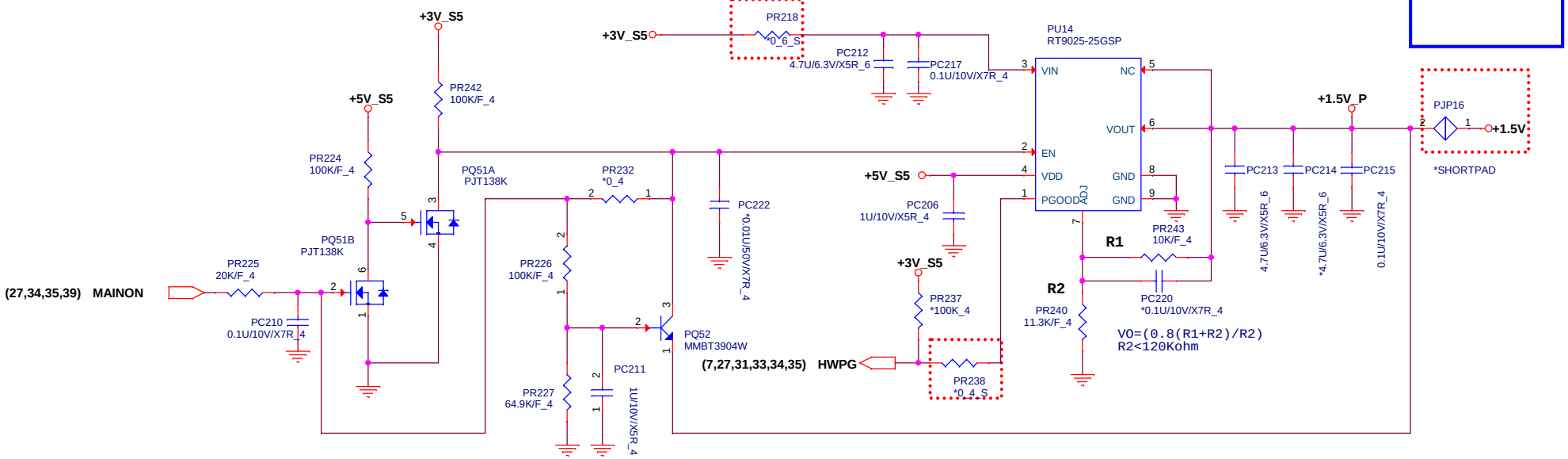
+1.05V Volt +/- 5%
Countinue current:4A
Peak current:7.7A
OCP minimum:9A

PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.05V (APW8713)	3B
Date: Wednesday, January 14, 2015	Sheet 35 of 58	

(24,25,30,31,33,34,35,37,38,39,40,41,42,51) +5V_S5
(2,7,8,9,10,11,20,23,28,30,33,37,39,40,45,51) +3V_S5
(7,8,9,11,17,18,23,41) +1.5V

+1.5V
Peak :20mA



PROJECT : NL8A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.5V (RT9025)	3B
Date: Wednesday, January 14, 2015	Sheet 36 of 58	

CPU Core : Loadline = -1.5mV/A
TDC = 33A ICCMAX=85A

OCP=120A

CPU Core : Loadline = -1.5mV/A
TDC = A ICCMAX=55A

OCP=66A

(2,4,5) VCCIO_OUT
(2,7,8,9,10,11,20,23,28,30,33,36,39,40,45,51) +3V_S5
(24,25,30,31,33,34,35,36,38,39,40,41,42,51) +5V_S5
(15,29,30,31,32,33,34,35) +VIN
(5,6,41) +VCC_CORE

3.24K for SharkBay
16.9K for CresentBay

PU6 ISL95812HRZ-T

(Near by MOS side)
(Near by Choke side)
(Near by IC side)
* PR135 PLACE NEAR PL8

C3A

PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCORE(ISL95812) 47W	3B
Date: Wednesday, January 14, 2015	Sheet 37 of 58	

(24,25,30,31,33,34,35,36,37,39,40,41,42,51) +5V_S5
(2,7,8,9,10,11,13,14,15,16,17,18,19,20,22,25,26,27,28,30,39,41,43,47) +3V
(31) +VIN_NV
(42,46,47) +VGACORE

VIN2P (31)
VIN2N (31)

PU2
RT8813AGQW

PR163 1_6 +5V_S5 8813PVCC 21 PVCC
PC49 0.22U/6.3V_4
PR70 1_6 +VIN_VGACORE
PR68 499K/F_4 8813TON 9 TON
PC51 0.22U/25V_6
PR157 10K/F_4 +3V
(31,42) DGPU_VC_EN 16 PGOOD
EC-D-21
(40,47) 3V_MAIN_PWGD
(7,40,51) GFXON
PR245 0_4/P
PR246 *0_4
PR76 10K/F_4
PD2 RB501V-40
PC58 0.22U/6.3V_4 3 EN
(45) DGPU_PSI PR168 *0_4/S 8813PSI 4 PSI
(45) DGPU_PWM_VID PR169 *0_4/S 8813VID 5 VID
8813VREF
8813VREF 8 VREF
PC54 0.1U/10V_4
PR73 39K/F_4
PR72 39K/F_4
PC60 1500P/50V_4
8813REFADJ 6 REFADJ
PR74 1.5K/F_4
PR172 1.5K/F_4
PR171 30K/F_4
PR170 *5.1K/F_4
8813REFIN 7 REFIN
PC55 *0.01U/16V_4
PR174 *0_4/P
TP92
PR175 *10K/F_4
PQ15 *2N7002K

PR71 1_6 2 UGATE1 8813UGATE1 8813UGATE1_1
PC56 0.22U/25V_6 1 BOOT1 8813BOOT1
24 PHASE1 8813PHASE1
PQ42 TPCA8064-H
PC62 10U/25V_8X
PC161 10U/25V_8X
PC63 0.1U/25V_4
PC162 2200P/50V_4
+VIN_VGACORE
PR249 RC2512-R005
PR278 *0_2/S
PR277 *0_2/S
PC146 100U/25V_105CE_f
PC145 100U/25V_105CE_f
PC28 0.1U/25V_4
+VIN_NV
PL12 0.22uH/50A
+VGACORE
PC160 560U/2V/ESR4.5_7343
PC159 560U/2V/ESR4.5_7343
VIN2N
VIN2P

POP Ri, Cb and NC Rh for 2phase
PQ41 TPCA8056-H
PR69 2.2_6
PC57 2200P/50V_4
PR67 16.9K/F_4
23 8813LGAT1 LGATE1
15 8813ISEN1 VCC/ISEN1
PR166 10K/F_4

+VGA_CORE
N15P-GX
Countinue current: 49A
Peak current: 76A
OCP minimum 90A

+VGA_CORE
N15E-GT
Countinue current: 76A
Peak current: 135A
OCP minimum 150A

17 8813UGATE2 UGATE2 8813UGATE2_1
PR59 1_6
PC151 10U/25V_8X
PC38 10U/25V_8X
PC37 0.1U/25V_4
PC150 2200P/50V_4
+VIN_VGACORE
PQ37 TPCA8064-H
PC44 0.22U/25V_6
18 8813BOOT2 BOOT2
19 8813PHASE2 PHASE2
PL7 0.22uH/50A
+VGACORE
PC59 0.1U/10V_4
PC155 560U/2V/ESR4.5_7343
PQ38 TPCA8056-H
PR58 2.2_6
PC43 2200P/50V_4
20 8813LGAT2 LGATE2

POP Ra and NC Rb for 2phase
Ra
Rb
PR158 *30K/F_4
+5V
PR161 10K/F_4
14 8813ISEN2 TALERT/ISEN2

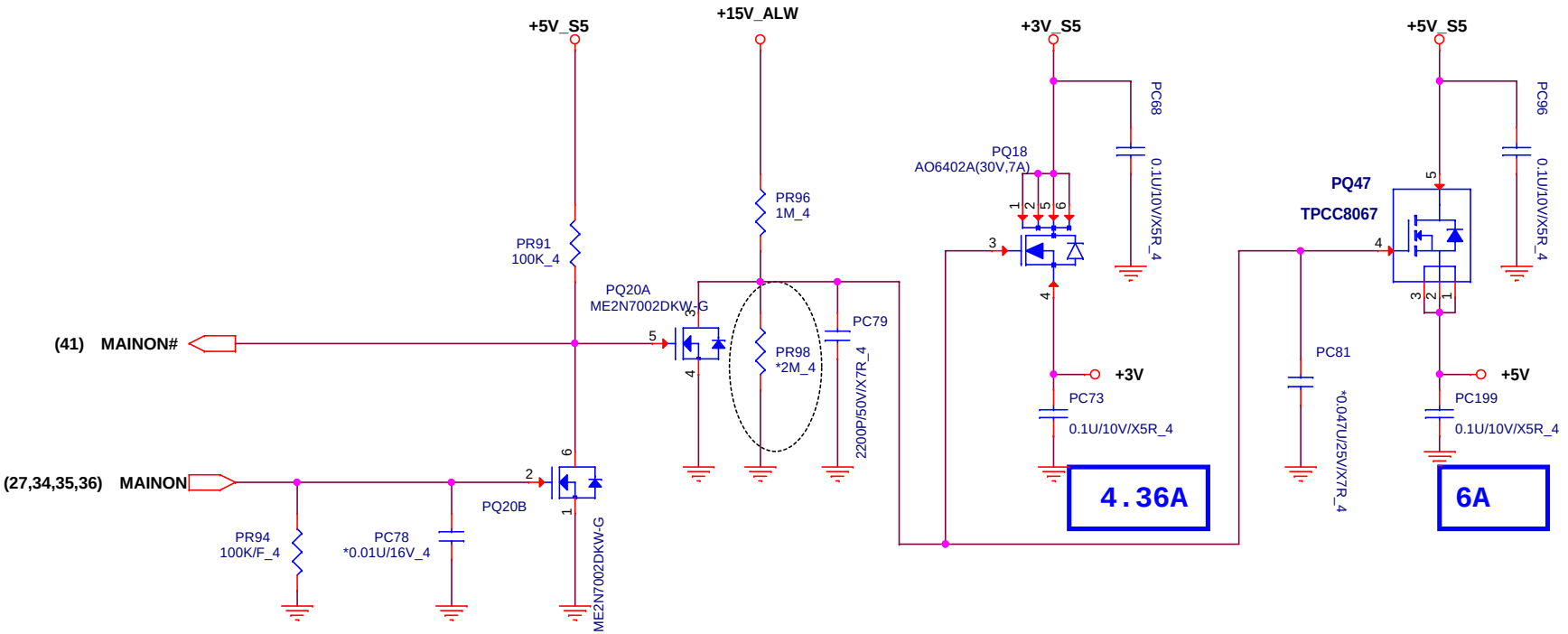
11 8813VOUT1 VSNS
PC46 56P/50V_4
PC157 *100P/50V_4
PR162 *0_4_S
PR164 *0_4_S
PR160 100/F_4
+VGACORE
VGPU_CORE_SENSE (43)
VSS_GPU_SENSE (43)
PR165 100/F_4
10 8813RGN RGND
PC50 56P/50V_4
12 8813SS SS
PC45 56P/50V_4

3Phase application
PU9
RT9610BZQW
22 8813PWM3 GND/PWM3
PR193 *0_4_S
9610PWM3 5 PWM
Rc
PR167 *0_4
25 GND
+5V
PR185 *0_4_S
9610EN 1 EN
PR88 10_8
+5V_S5
9610VCC 8 VCC
PC171 1U/6.3V_4
GND
GND
PR180 1_6
9610UGATE3 3 UGATE
9610UGTE3_1
+5V_S5
PD12 RB501V-40
PC166 0.22U/25V_6
4 9610BOOT3 BOOT
2 9610PHASE3 PHASE
7 9610LGATE3 LGATE
PQ44 TPCA8064-H
PQ43 TPCA8056-H
PR86 *2.2_6
PC66 *2200P/50V_4
PC179 10U/25V_8X
PC77 10U/25V_8X
PC175 0.1U/25V_4
PC72 2200P/50V_4
+VIN_VGACORE
PL11 0.22uH/50A
+VGACORE
PC158 330u_2.5V_7343

Rg
NC Rg for 2phase
PR159 10K/F_4
13 TSNS/ISEN3

POP Rc for 2phase

(24,25,30,31,33,34,35,36,37,38,40,41,42,51) +5V_S5
(33,40) +15V_ALW
(2,7,8,9,10,11,20,23,28,30,33,36,37,40,45,51) +3V_S5
(2,7,8,9,10,11,13,14,15,16,17,18,19,20,22,25,26,27,28,30,38,41,43,47) +3V
(8,16,17,18,19,21,26,28,29,30,38,41) +5V



PROJECT : NL8A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Load switch	3B
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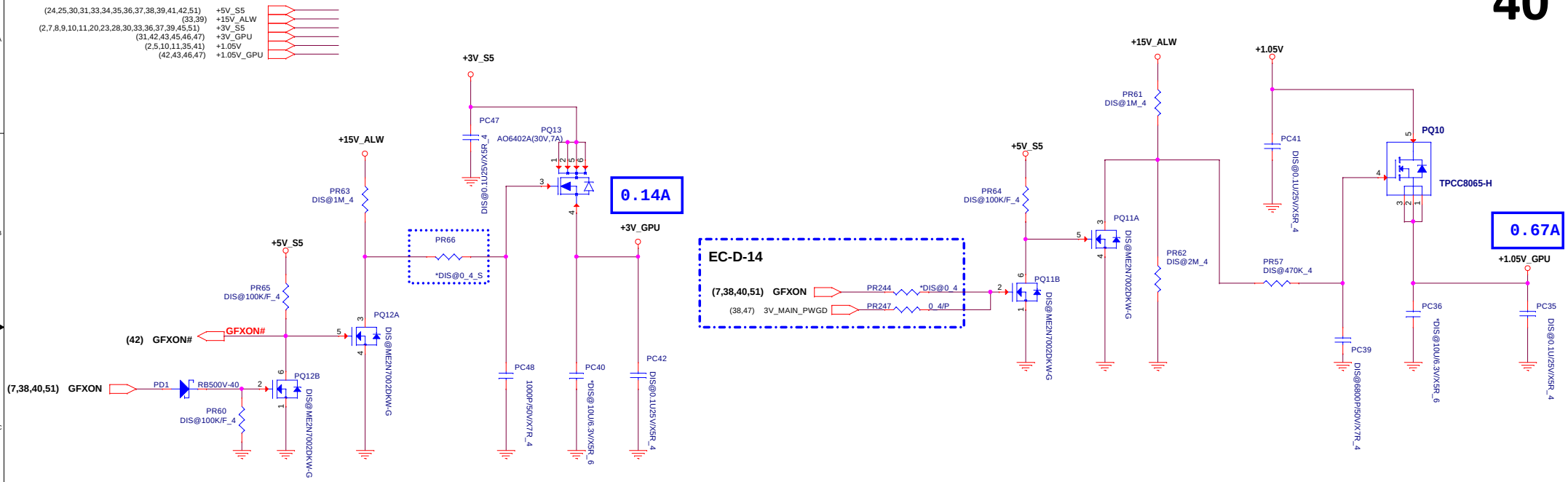

PROJECT : NL8A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DIS Load switch	3B
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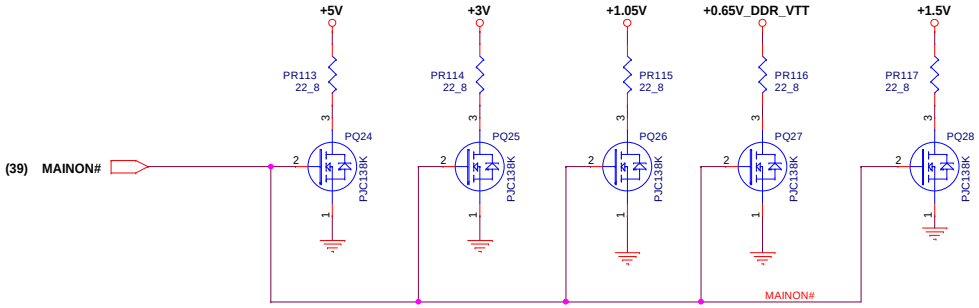
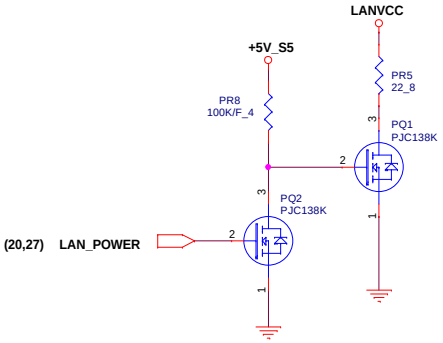
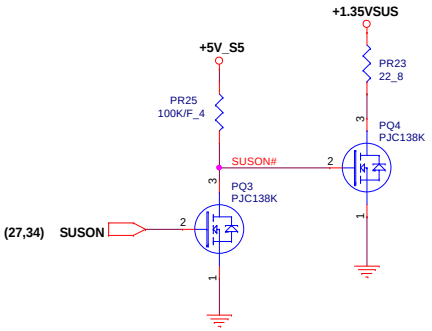
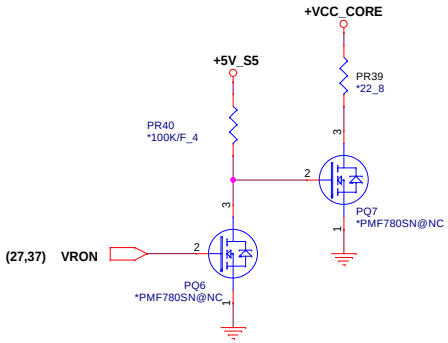
DISCHARGE

(8,16,17,18,19,21,26,28,29,30,38,39) +5V
(2,7,8,9,10,11,13,14,15,16,17,18,19,20,22,25,26,27,28,30,38,39,43,47) +3V
(2,5,10,11,35,40) +1.05V
(13,14,34) +0.65V_DDR_VTT
(7,8,9,11,17,18,23,36) +1.5V
(2,5,13,14,34) +1.35VSUS
(24,25,30,31,33,34,35,36,37,38,39,40,42,51) +5V_S5
(5,6,37) +VCC_CORE
(20) LANVCC









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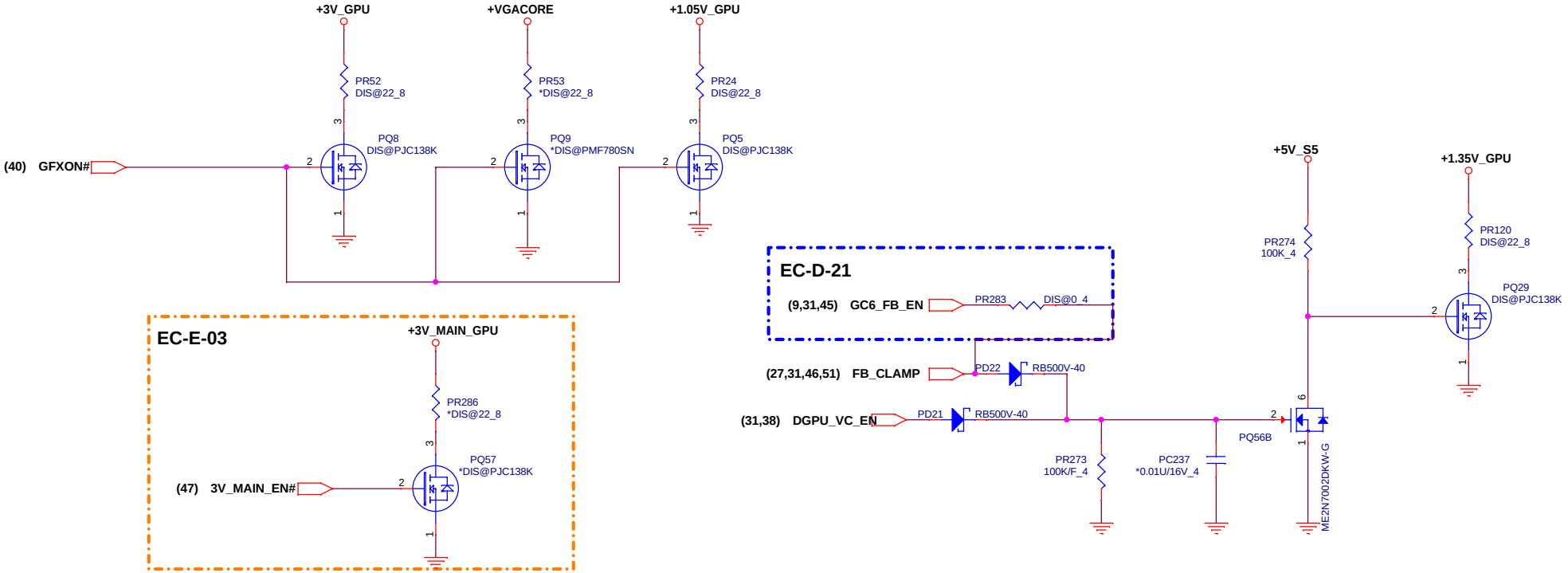
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge	3B
Date: Wednesday, January 14, 2015	Sheet 41 of 58	

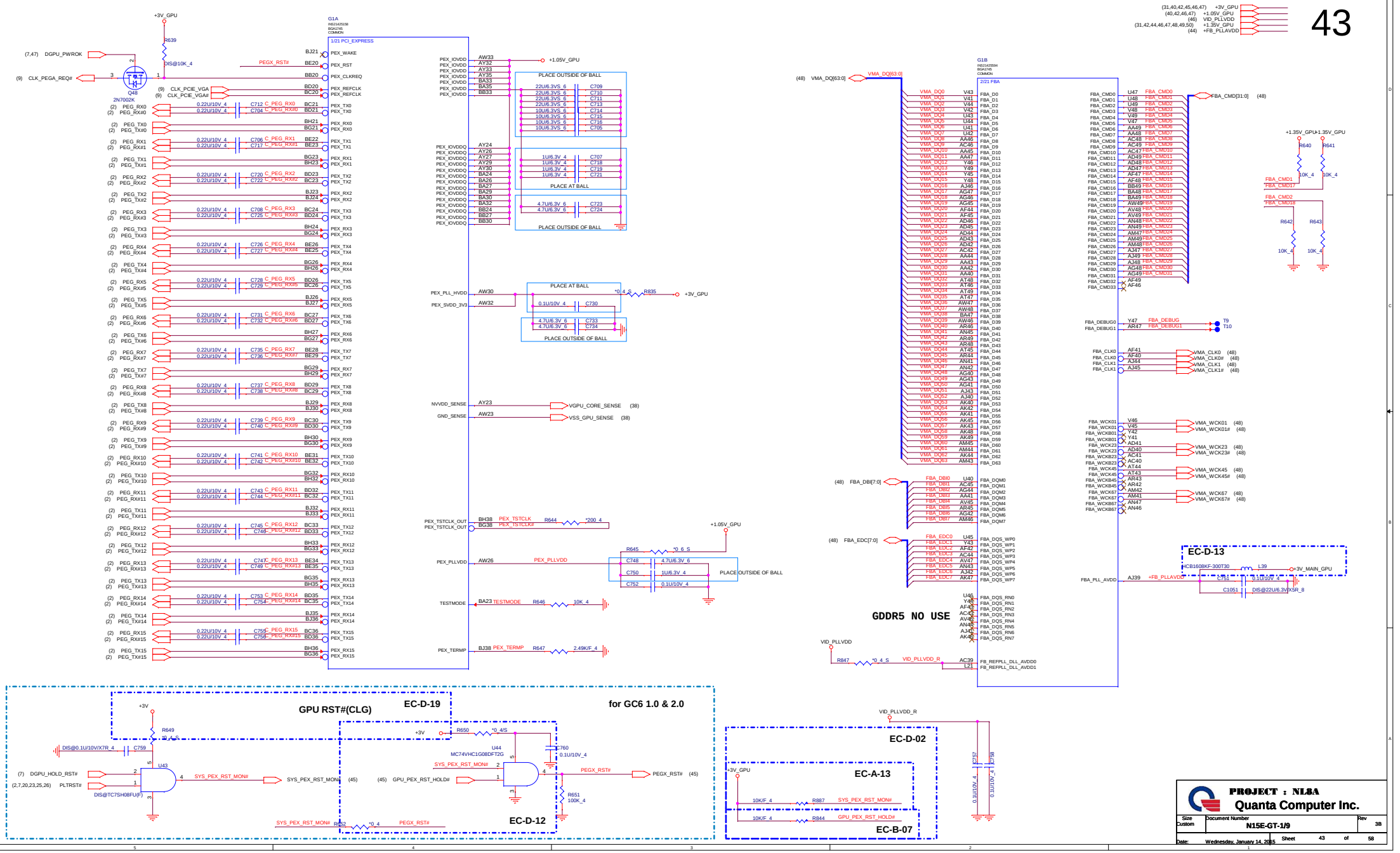
Discrete only

(31,40,43,45,46,47) +3V_GPU
(38,46,47) +VGACORE
(40,43,46,47) +1.05V_GPU
(31,43,44,46,47,48,49,50) +1.35V_GPU
(43,45,46,47) +3V_MAIN_GPU



PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discrete Discharge	3B
Date: Wednesday, January 14, 2015	Sheet 42 of 58	


G1A
1/21 PCI_EXPRESS
PEX_WAKE
PEX_RST
PEX_CLKREQ
PEX_REFCLK
PEX_REFCLK
PEX_TX0
PEX_TX0
PEX_RX0
PEX_RX0
PEX_TX1
PEX_TX1
PEX_RX1
PEX_RX1
PEX_TX2
PEX_TX2
PEX_RX2
PEX_RX2
PEX_TX3
PEX_TX3
PEX_RX3
PEX_RX3
PEX_TX4
PEX_TX4
PEX_RX4
PEX_RX4
PEX_TX5
PEX_TX5
PEX_RX5
PEX_RX5
PEX_TX6
PEX_TX6
PEX_RX6
PEX_RX6
PEX_TX7
PEX_TX7
PEX_RX7
PEX_RX7
PEX_TX8
PEX_TX8
PEX_RX8
PEX_RX8
PEX_TX9
PEX_TX9
PEX_RX9
PEX_RX9
PEX_TX10
PEX_TX10
PEX_RX10
PEX_RX10
PEX_TX11
PEX_TX11
PEX_RX11
PEX_RX11
PEX_TX12
PEX_TX12
PEX_RX12
PEX_RX12
PEX_TX13
PEX_TX13
PEX_RX13
PEX_RX13
PEX_TX14
PEX_TX14
PEX_RX14
PEX_RX14
PEX_TX15
PEX_TX15
PEX_RX15
PEX_RX15
+3V_GPU
R639
DIS@10K_4
Q48
2N7002K
PEGX_RST#
CLK_PEGA_REQ#
CLK_PCIE_VGA
CLK_PCIE_VGA#
DGPU_PWROK
C712 C_PEG_RX0
C704 C_PEG_RX0#
C706 C_PEG_RX1
C717 C_PEG_RX1#
C720 C_PEG_RX2
C722 C_PEG_RX2#
C708 C_PEG_RX3
C725 C_PEG_RX3#
C726 C_PEG_RX4
C727 C_PEG_RX4#
C728 C_PEG_RX5
C729 C_PEG_RX5#
C731 C_PEG_RX6
C732 C_PEG_RX6#
C735 C_PEG_RX7
C736 C_PEG_RX7#
C737 C_PEG_RX8
C738 C_PEG_RX8#
C739 C_PEG_RX9
C740 C_PEG_RX9#
C741 C_PEG_RX10
C742 C_PEG_RX10#
C743 C_PEG_RX11
C744 C_PEG_RX11#
C745 C_PEG_RX12
C746 C_PEG_RX12#
C747 C_PEG_RX13
C749 C_PEG_RX13#
C753 C_PEG_RX14
C754 C_PEG_RX14#
C755 C_PEG_RX15
C758 C_PEG_RX15#
0.22U/10V_4
PEX_IOVDD
PEX_IOVDDQ
AW33
AW32
AY33
AY35
BA33
BA35
BB33
AY24
AY26
AY27
AY29
AY30
BA24
BA26
BA27
BA29
BA30
BA32
BB24
BB27
BB30
+1.05V_GPU
PLACE OUTSIDE OF BALL
PLACE AT BALL
22U/6.3VS_6
C709
C710
C711
C713
C714
C715
C716
C705
1U/6.3V_4
C707
C718
C719
C721
4.7U/6.3V_6
C723
C724
PEX_PLL_HVDD
PEX_SVDD_3V3
AW30
AW32
*0_4_S
R835
0.1U/10V_4
C730
C733
C734
NVDD_SENSE
GND_SENSE
AY23
AW23
VGPU_CORE_SENSE
VSS_GPU_SENSE
(38)
PEX_TSTCLK_OUT
BH38
BG38
PEX_TSTCLK
PEX_TSTCLK#
R644
*200_4
PEX_PLLVDD
AW26
R645
*0_6_S
C748
C750
C752
TESTMODE
BA23
R646
10K_4
PEX_TERMP
BJ38
R647
2.49K/F_4
G1B
2/21 FBA
VMA_DQ[63:0]
FBA_D0
FBA_D1
FBA_D2
FBA_D3
FBA_D4
FBA_D5
FBA_D6
FBA_D7
FBA_D8
FBA_D9
FBA_D10
FBA_D11
FBA_D12
FBA_D13
FBA_D14
FBA_D15
FBA_D16
FBA_D17
FBA_D18
FBA_D19
FBA_D20
FBA_D21
FBA_D22
FBA_D23
FBA_D24
FBA_D25
FBA_D26
FBA_D27
FBA_D28
FBA_D29
FBA_D30
FBA_D31
FBA_D32
FBA_D33
FBA_D34
FBA_D35
FBA_D36
FBA_D37
FBA_D38
FBA_D39
FBA_D40
FBA_D41
FBA_D42
FBA_D43
FBA_D44
FBA_D45
FBA_D46
FBA_D47
FBA_D48
FBA_D49
FBA_D50
FBA_D51
FBA_D52
FBA_D53
FBA_D54
FBA_D55
FBA_D56
FBA_D57
FBA_D58
FBA_D59
FBA_D60
FBA_D61
FBA_D62
FBA_D63
FBA_DBI[7:0]
FBA_DQM0
FBA_DQM1
FBA_DQM2
FBA_DQM3
FBA_DQM4
FBA_DQM5
FBA_DQM6
FBA_DQM7
FBA_EDC[7:0]
FBA_DQS_WP0
FBA_DQS_WP1
FBA_DQS_WP2
FBA_DQS_WP3
FBA_DQS_WP4
FBA_DQS_WP5
FBA_DQS_WP6
FBA_DQS_WP7
FBA_DQS_RN0
FBA_DQS_RN1
FBA_DQS_RN2
FBA_DQS_RN3
FBA_DQS_RN4
FBA_DQS_RN5
FBA_DQS_RN6
FBA_DQS_RN7
GDDR5 NO USE
VID_PLLVDD
R847
*0_4_S
VID_PLLVDD_R
FB_REFPLL_DLL_AVDD0
FB_REFPLL_DLL_AVDD1
FBA_CMD[31:0]
FBA_CMD0
FBA_CMD1
FBA_CMD2
FBA_CMD3
FBA_CMD4
FBA_CMD5
FBA_CMD6
FBA_CMD7
FBA_CMD8
FBA_CMD9
FBA_CMD10
FBA_CMD11
FBA_CMD12
FBA_CMD13
FBA_CMD14
FBA_CMD15
FBA_CMD16
FBA_CMD17
FBA_CMD18
FBA_CMD19
FBA_CMD20
FBA_CMD21
FBA_CMD22
FBA_CMD23
FBA_CMD24
FBA_CMD25
FBA_CMD26
FBA_CMD27
FBA_CMD28
FBA_CMD29
FBA_CMD30
FBA_CMD31
FBA_DEBUG
FBA_DEBUG0
FBA_DEBUG1
T9
T10
FBA_CLK0
FBA_CLK0#
FBA_CLK1
FBA_CLK1#
VMA_CLK0
VMA_CLK0#
VMA_CLK1
VMA_CLK1#
FBA_WCK01
FBA_WCK01#
FBA_WCKB01
FBA_WCK23
FBA_WCK23#
FBA_WCKB23
FBA_WCK45
FBA_WCK45#
FBA_WCKB45
FBA_WCK67
FBA_WCK67#
FBA_WCKB67
VMA_WCK01
VMA_WCK01#
VMA_WCK23
VMA_WCK23#
VMA_WCK45
VMA_WCK45#
VMA_WCK67
VMA_WCK67#
+1.35V_GPU
R640
R641
R642
R643
10K_4
FBA_PLL_AVDD
+FB_PLLAVDD
AJ39
L39
HCB1608KF-300T30
+3V_MAIN_GPU
C751
C1051
DIS@22U/6.3V_X5R_8
EC-D-13
(31,40,42,45,46,47) +3V_GPU
(40,42,46,47) +1.05V_GPU
(46) VID_PLLVDD
(31,42,44,46,47,48,49,50) +1.35V_GPU
(44) +FB_PLLAVDD
GPU RST#(CLG)
EC-D-19
for GC6 1.0 & 2.0
R649
DIS@0.1U/10V/X7R_4
C759
U43
DIS@TC7SH08FU(F)
DGPU_HOLD_RST#
PLTRST#
SYS_PEX_RST_MON#
SYS_PEX_RST_MON
GPU_PEX_RST_HOLD#
R650
*0_4/S
U44
MC74VHC1G08DFT2G
C760
0.1U/10V_4
PEGX_RST#
R651
100K_4
R652
EC-D-12
EC-D-02
EC-A-13
EC-B-07
10K/F_4
R887
R844
C757
C758
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(31,42,43,46,47,48,49,50) +1.35V_GPU
(43) +FB_PLLAVDD

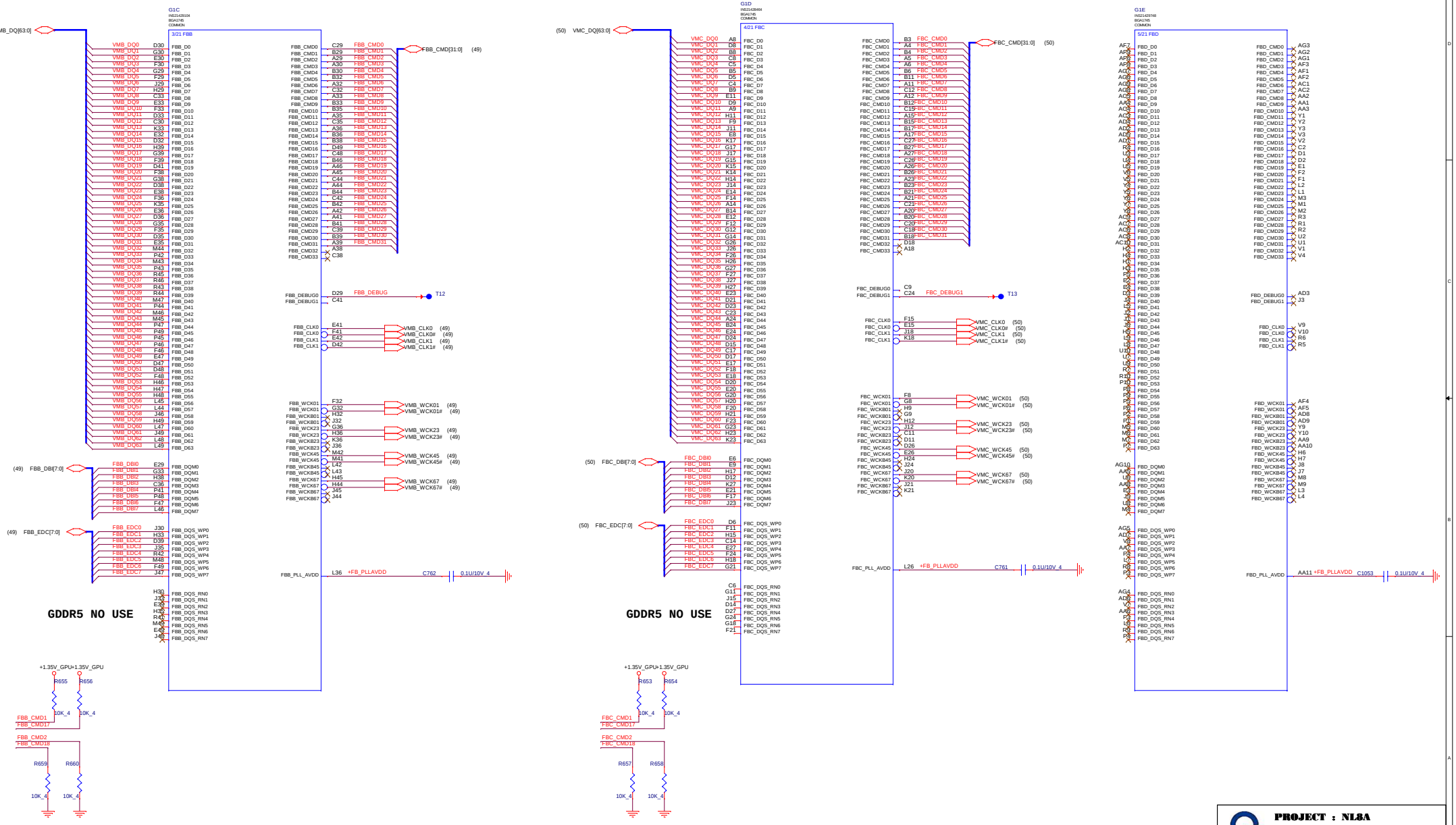

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Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 15-3 and Table15-4 contain mapping tables for the Multi-Level Strapping Modes.

N15E-GX/GT GDDR5 MEMORY RVL

N15E-GX recommends the following GDDR5 memories for use in conjunction with notebook designs using N15E-GX/GT GPU.

Note: For N15E-GX/-GT, the maximum allowable memory case temperature is 115 °C, as these are our highest end flagship GPUs.

Table 12. N15E-GX/GT GDDR5 Recommended Memories

Memory Type	FBVDDI/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Clk Grade(MHz)	Memory Data Code (Minimum)	Status
GDDR5	1.35V/ 1.35V	128Mx16	Hynix	H5GQ2H24AFR-R0C	A-die	0x6	2500	N/A	Production candidate
			Samsung	K4G20325FD-FC03	D-die	0x7	2500	N/A	Production candidate
			Hynix	H5GC4H24MFR-T2C	M-die	0x1	2500	N/A	Production candidate
		256Mx16	Micron	EDW8032B4PB-60-F	A-die	0x3	2500	N/A	Production candidate
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production candidate

256M x16	H5GC4H24MFR-T2C	AKG5PWUTW06
256M x16	K4G41325FC-HC03	AKG5PGDT500

Default: GDDRS Hynix 2G VRAM (for NL8)

Memory Size	Vendor	P/N	Mfr. P/N	ROM_SI	
128M x 16	Hynix (1.35V)	AKG5MWUTW23	H5GC2H24BFR-T2C	0001 (0x1)	10K PD
256M x 16	Hynix (1.35V)	AKG5MWUTW06	H5GC4H24MFR-T2C	0010 (0x2)	15K PD
128M x 16	Samsung (1.35V)	AKG5MWDTS02	K4G20325FD-FC03	0000 (0x0)	4.99K PD
256M x 16	Samsung (1.35V)	AKG5PGDTS00	K4G41325FC-HC03	0011 (0x3)	20K PD
128M x 16	Micron (1.35V)	AKG5MWBTL03	EDW2032BBBG-6A-F-R		30.1K PD

Table 1. N15E-GX / -GT GC6 Pin Assignment

GPIO/ Power Rail	GC6 1.0 Control Signal	GC6 2.0 Control Signal [1]
GPIO1	FB_CLAMP_MOH	GC6_FB_EH
GPIO2	FBCLAMP_TGL_REQ#	GPU_EVEHT#
GPIO4	Reserve	3V3_MAIH_EH
GPIO23	Reserve	GPU_PEX_RST_HOLD#
CEC	HC	SYS_PEX_RST_MOH#
PEX_PLL_HVDD	VDD33	3V3_AOH
PEX_SVDD_3V3	VDD33	3V3_AOH
3V3MISC	VDD33	3V3_AOH

Note:

1. All GPIO, I2CA/B/C/S, DAC_H/V_SYHC, PCIe Reset, CLKREQ#, XTAL, and JTAG signals, when pulled-up, should be connected to the 3V3_AOH power rail for GC6 2.0.

Table 12-2. GB3-256 GPIO Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO1	FB_CLAMP_MOH	I	FB clamp monitor	
GPIO2	FB_CLAMP_TGL_REQ	O	Active low FB clamp toggle request	10K pull-up to system 3.3V
GPIO3	OC_WARH	I	Over current interrupt for IPC	10K pull-up
GPIO4	Reserved			
GPIO5	Reserved			
GPIO6	PSI	O	Phase Shedding	PSI: 10k pull-up to enable two phase.
GPIO7	LCD_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO8	OVERT	O	Active Low Thermal Catastrophic Over Temperature	10K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	10K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up
GPIO13	LCD_BLEH	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_AB	I	Hot Plug Detect for IFPAB	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	
GPIO16	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or IFPB	
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	

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(31,40,42,43,45,47) +3V_GPU
(40,42,43,47) +1.05V_GPU
(43,46) VID_PLLVDD
(42,43,45,47) +3V_MAIN_GPU

G1P
INS21439001
BGA1745
COMMON
16/21 GND_1/2

G1Q
INS21437008
BGA1745
COMMON
17/21 GND_2/2

G1R
INS21437986
BGA1745
COMMON
18/21 VDD_1/2

G1T
INS21438888
BGA1745
COMMON
19/21 VDD_2/2

G1U
INS21439518
BGA1745
COMMON
20/21 FBVDDQ

+VGACORE
+1.35V_GPU

FBVDDQ_SENSE R49 FBVDDQ_SENSE TP103
FB_CLAMP BB48 FB_CLAMP_GPU
FB_VREF R39 FB_VREF_PROBE TP104
PROBE_FBVDDQ AG11 GPU_FBVDDQ_PROBE TP105
PROBE_FB_GND AF10 GPU_FBVDDQ_PROBE_GND TP106
FB_CAL_PD_VDDQ P40 FB_CAL_PD_VDDQ R697 40.2/F_4 O+1.35V_GPU
FB_CAL_PU_GND R48 FB_CAL_PU_GND R698 40.2/F_4
FB_CALTERM_GND R47 FB_CAL_TERM_GND R699 60.4/F_4
PLACE CLOSE TO GPU BALLS

(27,31,42,51) FB_CLAMP *0_4 R700 FB_CLAMP_GPU R701 10K_4

G1S
INS21439643
BGA1745
COMMON
21/21 NC/3V3

+3V_MAIN_GPU
+3V_GPU
R706 *0_4_S
EC-D-10

+1.05V_GPU
L40 PBY160808T-181Y-N
EC-D-25
C764 DS@0.1U/6.3V/X6R_6
C765 DS@0.1U/6.3V/X6R_6
C763 DS@0.1U/10V/X7R_4
C766 DS@0.1U/10V/X7R_4
L41 HCB1608KF-300T30
C767 22U/6.3VS_6
C768 1U/6.3V_4
C769 0.1U/10V_4
C770 0.1U/10V_4
C771 0.1U/10V_4
(43,46) VID_PLLVDD
PLACE CLOSE TO GPU
PLACE CLOSE TO BALLS

G1F
INS21439822
BGA1745
COMMON
14/21 XTAL/PLL

AW27 SP_PLLVDD
AW28 VID_PLLVDD
Y39 GPCPLL_AVDD0
AD11 GPCPLL_AVDD1
AT11 LXS_PLLVDD
BB3 XTALSSIN
BB2 XTALIN
BB1 XTALOUTBUFF
BA1 VGA_XTALOUT

+3V_GPU +3V_GPU
R704 10K_4
R705 10K_4
XTALSSIN
XTALOUTBUFF
R707 10K_4
R708 10K_4

VGA_XTALIN
VGA_XTALOUT
Y5
27MHZ +-10PPM
C772 10P/50V_4
C773 10P/50V_4

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EC-B-04

+3V_GPU
R709 4.7K_4
DGPU_PWROK (7,43)
+3V
10K/F_4 R710
Q53
R711 *100K/F_4
DGPU_PGOK-1
LTC044EUBFS8TL
+1.05V_GPU R712 10K/F_4 DGPU_POK4 Q54 METR3904-G
C780 0.1U/10V/X7R_4
C775 2200P/50V/X7R_4
+1.35V_GPU R713 10K/F_4 DGPU_POK2 Q55 METR3904-G
C790 *1000P/16V/X7R_4

+VGACORE

Near GPU

C1052 22U/6.3V_6
C1022 22U/6.3V_6
C1023 22U/6.3V_6
C1024 22U/6.3V_6
C1025 22U/6.3V_6
C1026 22U/6.3V_6
C1027 22U/6.3V_6
C1028 22U/6.3V_6
C1029 22U/6.3V_6
C1030 22U/6.3V_6
C1031 22U/6.3V_6

C774 10u/6.3V_6
C777 10u/6.3V_6
C779 10u/6.3V_6
C782 10u/6.3V_6

Under GPU

C776 4.7U/6.3V/X5R_6
C778 4.7U/6.3V/X5R_6
C781 4.7U/6.3V/X5R_6
C783 4.7U/6.3V/X5R_6
C784 4.7U/6.3V/X5R_6
C785 4.7U/6.3V/X5R_6
C786 4.7U/6.3V/X5R_6
C787 4.7U/6.3V/X5R_6
C788 4.7U/6.3V/X5R_6
C789 4.7U/6.3V/X5R_6

C791 4.7U/6.3V/X5R_6
C792 4.7U/6.3V/X5R_6
C793 4.7U/6.3V/X5R_6
C794 4.7U/6.3V/X5R_6
C795 4.7U/6.3V/X5R_6
C796 4.7U/6.3V/X5R_6
C797 4.7U/6.3V/X5R_6
C798 4.7U/6.3V/X5R_6
C799 4.7U/6.3V/X5R_6
C800 4.7U/6.3V/X5R_6

C801 4.7U/6.3V/X5R_6
C805 4.7U/6.3V/X5R_6
C809 4.7U/6.3V/X5R_6
C813 4.7U/6.3V/X5R_6
C817 4.7U/6.3V/X5R_6
C821 4.7U/6.3V/X5R_6
C825 4.7U/6.3V/X5R_6
C829 4.7U/6.3V/X5R_6
C833 4.7U/6.3V/X5R_6
C836 4.7U/6.3V/X5R_6

C802 0.1u/10V_4
C806 0.1u/10V_4
C810 0.1u/10V_4
C814 0.1u/10V_4
C818 0.1u/10V_4
C822 0.1u/10V_4
C826 0.1u/10V_4
C830 0.1u/10V_4
C834 0.1u/10V_4
C837 0.1u/10V_4

C841 4.7U/6.3V/X5R_6
C844 4.7U/6.3V/X5R_6
C847 4.7U/6.3V/X5R_6
C850 4.7U/6.3V/X5R_6
C853 4.7U/6.3V/X5R_6
C856 4.7U/6.3V/X5R_6
C859 4.7U/6.3V/X5R_6
C862 4.7U/6.3V/X5R_6
C865 4.7U/6.3V/X5R_6
C868 4.7U/6.3V/X5R_6

C842 0.1u/10V_4
C845 0.1u/10V_4
C848 0.1u/10V_4
C851 0.1u/10V_4
C854 0.1u/10V_4
C857 0.1u/10V_4
C860 0.1u/10V_4
C863 0.1u/10V_4
C866 0.1u/10V_4
C869 0.1u/10V_4

+1.35V_GPU

Near GPU

C1042 10u/6.3V_6
C1041 10u/6.3V_6
C803 10u/6.3V_6
C807 10u/6.3V_6
C811 10u/6.3V_6
C815 10u/6.3V_6
C819 DIS@22U/6.3V/X5R_8
C823 DIS@22U/6.3V/X5R_8
C827 DIS@22U/6.3V/X5R_8
C831 DIS@22U/6.3V/X5R_8
C1043 DIS@22U/6.3V/X5R_8
C1044 DIS@22U/6.3V/X5R_8

Under GPU

C804 0.1u/10V_4
C808 0.1u/10V_4
C812 0.1u/10V_4
C816 0.1u/10V_4
C820 0.1u/10V_4
C824 0.1u/10V_4
C828 0.1u/10V_4
C832 0.1u/10V_4
C835 1u/6.3V_4
C838 1u/6.3V_4
C839 1u/6.3V_4
C840 1u/6.3V_4
C843 1u/6.3V_4
C846 1u/6.3V_4
C849 1u/6.3V_4
C852 1u/6.3V_4
C1034 1u/6.3V_4
C1036 1u/6.3V_4
C1037 1u/6.3V_4
C1035 1u/6.3V_4
C1039 1u/6.3V_4
C1040 1u/6.3V_4
C884 4.7U/6.3V/X5R_6
C885 4.7U/6.3V/X5R_6
C886 4.7U/6.3V/X5R_6
C887 4.7U/6.3V/X5R_6
C888 4.7U/6.3V/X5R_6
C889 4.7U/6.3V/X5R_6
C890 4.7U/6.3V/X5R_6
C891 4.7U/6.3V/X5R_6
C892 4.7U/6.3V/X5R_6
C893 4.7U/6.3V/X5R_6

+3V_MAIN_GPU
C1047 1u/6.3V_4
C1046 4.7U/6.3V/X5R_6
C1045 0.1u/10V_4

+3V_GPU
C870 1u/6.3V_4
C872 4.7U/6.3V/X5R_6
C874 0.1u/10V_4

(2,7,8,9,10,11,13,14,15,16,17,18,19,20,22,25,26,27,28,30,38,39,41,43) +3V
(42,43,45,46) +3V_MAIN_GPU
(31,40,42,43,45,46) +3V_GPU
(38,42,46) +VGACORE
(31,42,43,44,46,48,49,50) +1.35V_GPU
(40,42,43,46) +1.05V_GPU

3V MAIN POWER for GC6 2.0

EC-D-07
EC-D-11
EC-E-03
(42) 3V_MAIN_EN#
(45) 3V_MAIN_EN
+3V_GPU
R453 10K_4
R480 10K_4
R454 *0_4/S
Q38 2N7002K
C621 0.022U/25V_4
C620 0.022U/25V_4
Q37 AO3413
R838 *0_4
+3V_MAIN_GPU

for GC6 2.0

+3V_GPU
+3V
R489 4.7K_4
R492 4.7K_4
3V_MAIN_PWGD
3V_MAIN_PWGD (38,40)
R490 100K/F_4
+3V_MAIN_GPU R491 4.7K_4
C641 1000p/50V_4
Q41 MMBT3904-7-F
C638 1000P/16V/X7R_4
Q42 DTC144EU

+1.05V_GFX and GPU core power EN

for meet Power down sequence for +3V_GFX

+VGACORE D25 RB500V-40
+1.35V_GPU D26 *RB500V-40
+3V_GPU

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CHANNEL A: 2G/4G GDDR5

(43) VMA_DQ[63..0]
(43) FBA_CMD[31:0]
(43) FBA_DBI[7..0]
(43) FBA_EDC[7..0]

(31,42,43,44,46,47,49,50) +1.35V_GPU

Channel 0 <0-31>
MF=0 Non-mirrored

QD16~23

QD0~7

VRAM1

Channel 0 <0-31>
MF=1 Mirrored

QD8~15

QD24~31

VRAM2

Channel 1 <32-63>
MF=0 Non-mirrored

QD48~55

QD32~39

VRAM3

Channel 1 <32-63>
MF=1 Mirrored

QD40~47

QD56~63

VRAM4

VREFD_VMA1 0.4MM=16mils
VREFC_VMA1 0.4MM=16mils
VREFD_VMA2 0.4MM=16mils
VREFC_VMA2 0.4MM=16mils

VREF_VMA1_MOS
VREF_VMA2_MOS
2N7002K
GPIO10_VREF

Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CMD0	CAS*	CMD16	CAS*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0		
CMD35	DEBUG1		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

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CHANNEL B: 2G/4G GDDR5

(44) VMB_DQ[63..0] → VMB_DQ[63..0]
(44) FBB_CMD[31..0] → FBB_CMD[31..0]
(44) FBB_DBI[7..0] → FBB_DBI[7..0]
(44) FBB_EDC[7..0] → FBB_EDC[7..0]

(31,42,43,44,46,47,48,50) +1.35V_GPU

Channel 0 <0-31>
MF=0 Non-mirrored

QD16~23

QD0~7

Channel 0 <32-63>
MF=1 Mirrored

QD8~15

QD24~31

Channel 1 <0-31>
MF=0 Non-mirrored

QD48~55

QD32~39

Channel 1 <32-63>
MF=1 Mirrored

QD40~47

QD56~63

VRAM5 / VRAM6 / VRAM7 / VRAM8 — GDDR5

VREFD_VMA1 0.4MM=16mils
VREFC_VMA1 0.4MM=16mils
VREFD_VMA2 0.4MM=16mils
VREFC_VMA2 0.4MM=16mils

Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CMD0	CAS*	CMD16	CAS*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0[1]		
CMD35	DEBUG1[1]		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

Channel 0 <0-31> MF=0 Non-mirrored

Channel 0 <32-63> MF=1 Mirrored

Channel 1 <0-31> MF=0 Non-mirrored

Channel 1 <32-63> MF=1 Mirrored

QD16~23

QD8~15

QD48~55

QD40~47

QD0~7

QD24~31

QD32~39

QD56~63

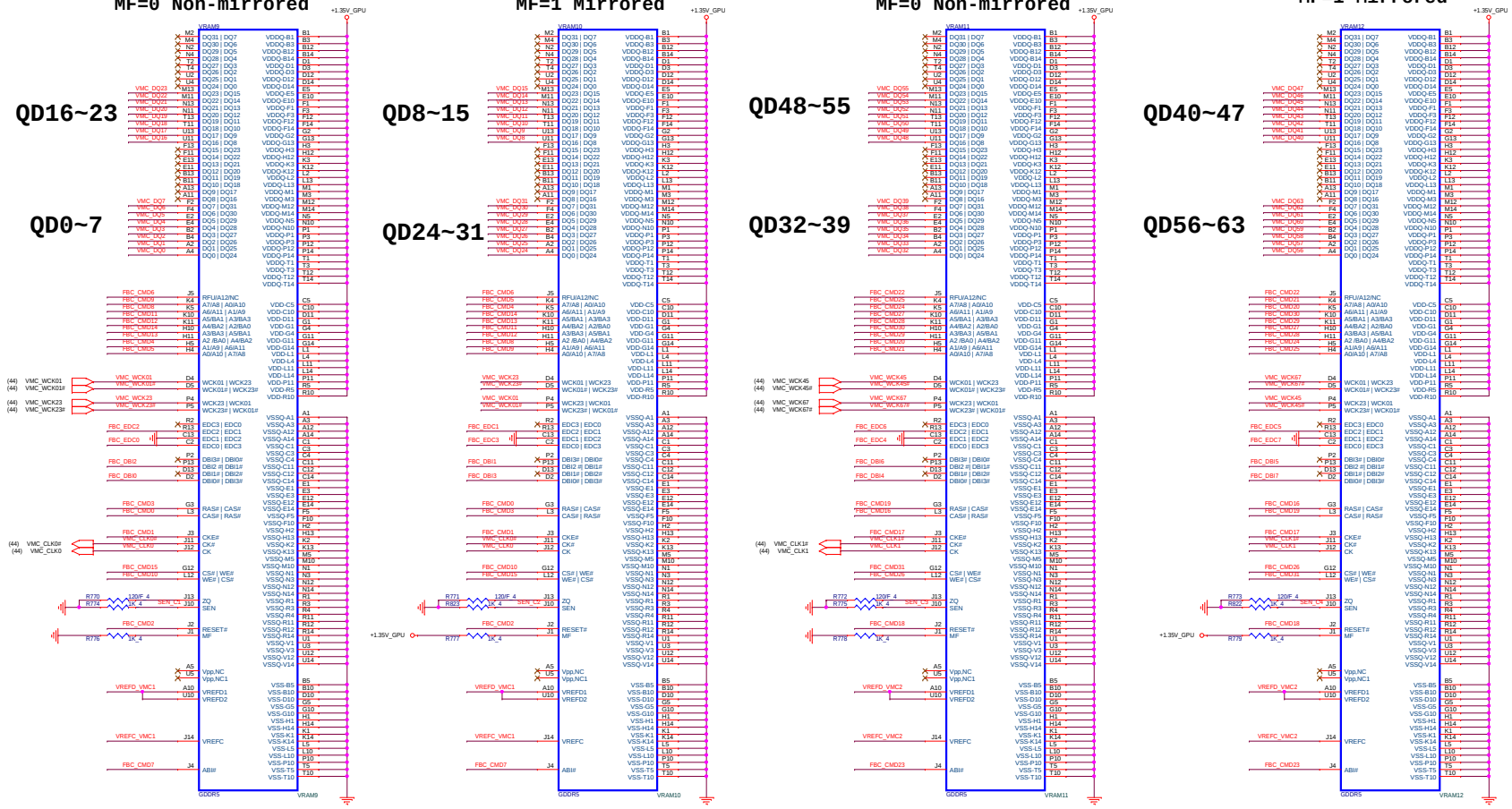

Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CMD0	CA5*	CMD16	CA5*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0[1]		
CMD35	DEBUG1[1]		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

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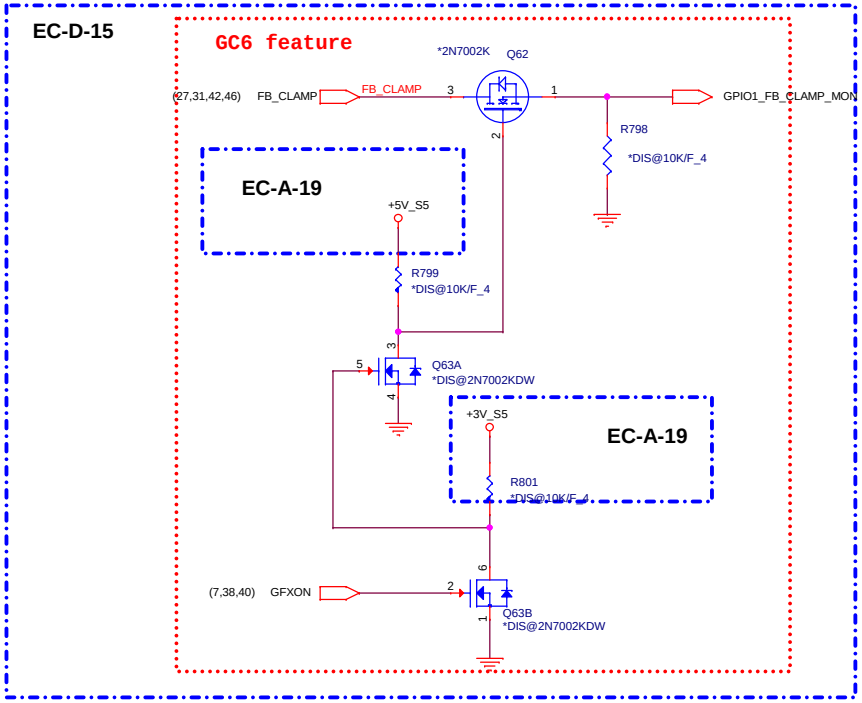

Power rail	State in GC6
3V3_AON	On
3V3_MAIN	Off
PEX_1.05V	Off
NVVDD	Off
FBVDD/Q	On

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SDV~SIV

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-A-01	21	02/19	CN20	HDD pin define change.
EC-A-02	26	02/19	Q67	change to Q66A(delete Q67).
EC-A-03	28	02/19	R881,R882,R883	add for current limit
EC-A-04	18,19	02/19	C1058,C1059,C458,R884,C1060	co-lay line and mono-out for subwoofer
EC-A-05	19	02/20	U21	change to AND GATE
EC-A-06	11	02/20	L5	depop
EC-A-07	7	02/20	R862,R863,R536,R548	R862,R863,R536,R548 change to 8.2K
EC-A-08	18	02/20	Q47	Q47 chnage to BAM34090009 for SPDIF LED always tune on issue
EC-A-09	7	02/20	R602	R602 change to 1K to follow CRB
EC-A-10	8	02/20	R526	POP
EC-A-11	48	02/21	R885	reserve 10K for GC6_FB_EN
EC-A-12	48	02/21	R886	reserve R886 for GC6 2.0 GPU_EVENT need pull up to 3V3_AON
EC-A-13	46	02/21	R887	reserve R887 for GC6 2.0 SYS_PEX_RST_MON# need pull up to 3V3_AON
EC-A-14	7,27	02/24	R880	change R880 to 100K pull low and GFXON change from EC to PCH(for GC6 2.0)
EC-A-15	48	02/26	R888,R889	reserve to follow DG but CRB pull low
EC-A-16	28	02/27	R874	change net form KB_LIGHT to KB_LIGHT_P due to same net name as EC control
EC-A-17	24,25	02/27		change U3B(real side) form MB to FB
EC-A-18	9	02/27	R598	add CLKREQ# for card reader and R598 change to pull up
EC-A-19	54	02/27		change power rail
EC-A-20	28	03/04		move LID function to PWR/B

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SIV~SIT

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-B-01	17	04/01		change HDMI solution to support 4K*2K
EC-B-02	10	04/01	R320	add R320 to avoid GPIO float.
EC-B-03	20	04/01	R52	change to +3V for lan wake issue
EC-B-04	50	04/01	R713,R712,C790,C780,R710,C775	change DGPU PWR OK power sequence
EC-B-05	7	04/02	R281	ACPI for GPU(improve perf. under DC mode)
EC-B-06	20	04/03	C31,C543	C31,C543 change to 8.2p for X'tral report
EC-B-07	46	04/03	R844	GPIO23 for GC6 1.0 just only reserve
EC-B-08	47	04/07		delete T11/T14 due to located on no probe area
EC-B-09	48	04/07		change SYS_PEX_RST_MON# from CEC to GPIO16
EC-B-10	18,19	04/07	D27,D28,D29,D30,D31,R939	for SUBWOOFER pop noise issue
EC-B-11	22	04/08		SSD_DEVSLP chnage to pin44
EC-B-12	28	04/09		change CN5.9 to 3VPCU(user define key)
EC-B-13	19	04/11	C1081,C1082	add C1081 for subwoofer RC filter & reserve C1082 for pi filter
EC-B-14	25	04/11	CN14	change CN14 pin define
EC-B-15	18	04/11	C1058,C1059	change to 10u
EC-B-16	18	04/17	R345,R346	change to 47K for PC beep sound

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SIT~SVT

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-C-01	27	05/19	SW1	remove form SVT stage
EC-C-02	15	05/19		CCD pin define change
EC-C-03	22	05/19	CN8,CN18	pin43 change to NA
EC-C-04	19	05/22	R943,R944	reserve for POP noise
EC-C-05	48	05/28	R669,R670	remove for MIO interface no support

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SIT~SVT

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-D-01	09,10	9/16	R870,R871;R538,R539,R575,R594,R554,R562	GC6 2.0;board ID;
EC-D-02	43	9/15	R887	reserve for GPIO pull up +3V_GPU(GC6 2.0)
EC-D-03	45	9/15	DACA_VDD, R945	reserve for N16E add +3V_MAIN_GPU pin(thermal detect)
EC-D-04	45	9/15	R824, R825 (short)	+3V-GPU change to +3V_MAIN_GPU (GC6 2.0)
EC-D-05	45	9/15	GFx_SCL, GFx_SDA	+3V_MAIN_GPU change to +3V_GPU (GC6 2.0)
EC-D-06	45	9/15	R840, R841, R885	reserve to GC6 2.0
EC-D-07	45, 47	9/15	R833, R480	reserve to GC6 2.0; pull up +3V_GPU
EC-D-08	43, 45	9/15	R834, R844	reserve to GC6 2.0; pull up +3V_GPU
EC-D-09	45	9/15	R869	+3V_MAIN_GPU change to +3V_GPU (GC6 2.0)
EC-D-10	46	9/15	VDD33, 3V3MISC	+3V-GPU change to +3V_MAIN_GPU; +3V_MAIN_GPU change to +3V_GPU (GC6 2.0)
EC-D-11	47	9/15,9/17	C621	+3V_GPU change to +3V; change back +3V_GPU
EC-D-12	43, 45	9/15	R650,R652,U44,C760,R687,R875,Q71,R691,Q51	reserve to GC6 2.0
EC-D-13	43	9/15	L39	+3V-GPU change to +3V_MAIN_GPU (GC6 2.0)
EC-D-14	40	9/15	PR244, PR247	GFXON change to 3V_MAIN_PWGD (GC6 2.0)
EC-D-15	51	9/15	R798, R799, R801, Q62, Q63	GC6 feature remove
EC-D-16	45	9/15	R676	change to 49.9K
EC-D-17	45	9/15	R864,Q69,R886, R865,R831,R832	reserve to FB_CLAMP_TGL_REQ#_R(GC6 2.0)
EC-D-18	45	9/16	R667,R668,R868,R869	multi-level mode strapping

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SIT~SVT

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-D-19	43	9/17	U43,U44	+3V_GPU change to +3V(Nelson)
EC-D-20	45	9/17	Q52 pin5	+3V_GPU change to +3V_MAIN_GPU(Nelson)
EC-D-20	38	9/17	PR245,PR246	GFXON change to +3V_MAIN_PWGD
EC-D-21	31, 42	9/17	PR266,PR283	GC6_FB_EN derive 1.35_GPU
EC-D-22	27, 46	9/17	R866, R700	FB_CLAMP discable
EC-D-23	5,7,11	9/18	R946, R947, R948, C1084	Haswell & Broadwell Compatibility Considerations
EC-D-24	7	9/18	R338	Haswell & Broadwell Compatibility Considerations
EC-D-25	46	10/06	C764, C765	VID_PLLVDD power rail filtering combined form Albert

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SIT~MV

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-E-01	10	11/12	R949	Add GPIO35 for board ID
EC-E-02	27,28	11/12	CN31,R950,R951	Add Breathe LED function
EC-E-03	42,47	11/12	PQ57,PR286	Add +3V_MAIN_GPU discharger circuite
	29	11/18	H34	GND pad remove for new 4 pin connector
EC-E-04	28	11/19	C1085,C1086,C1087,C1088	Add Breathe LED function EMI ESD part

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SIT~MV

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-F-01	27,28	12/09	CN32,C1089~C1097,U15	add power button conn for NL9
EC-F-02	27,28	12/09	CN33,R952,R953,C1098~C1103,U15	add touch PAD WHITE/RED LED for NL9
EC-F-03	8,27	01/13	Q72, R954; R867 no stuff	add EC RTC RST for system can't power on untill remove RTC issue

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