Compal LA-G131P

CFL-H MB Schematic Document

Rev: 1.0

2018.06.08

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Title: Cover Sheet		
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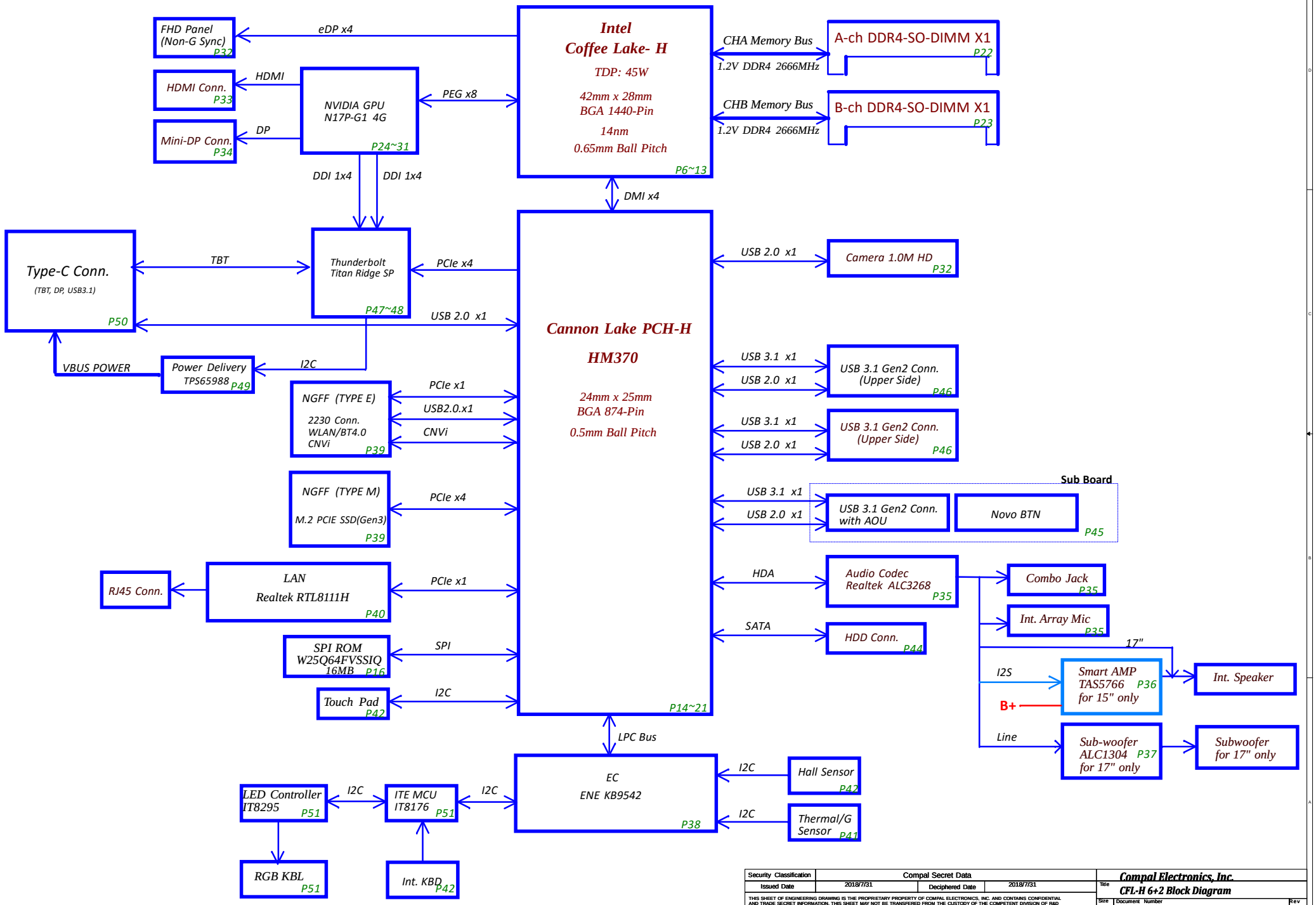
Coffee Lake H Block Diagram



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Title	CFL-H 6+2 Block Diagram		
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Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID /PCB Revision	Rb	V_{AD_BID} min	V_{AD_BID} TYP	V_{AD_BID} Max	EC AD3
0 --> 0.1	0		0 V	0.300 V	0x00 - 0x13
1 --> 0.2	12K +/- 1%	0.347 V	0.354 V	0.36 V	0x14 - 0x1E
2 --> 0.3	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3 --> 0.4	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4 --> 0.5	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5 --> 0.6	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6 --> 0.7	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7 --> 0.8	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8 --> 0.9	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9 --> 1.0	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10 --> 1.1	130K +/- 1%	1.849 V	1.865 V	1.881V	0x88 - 0x96
11 --> 1.2	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12 --> 1.3	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13 --> 1.4	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14 --> 1.5	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15 --> 1.6	330K +/- 1%	2.521 V	2.533V	2.544 V	0xC0 - 0xC9
16 --> 1.7	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17 --> 1.8	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18 --> 1.9	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19 --> 2.0	NC	3.000 V	3.000 V		0xF1 - 0xFF

HSIO Port Table(CPU)

HSIO Port	Device	PCIE CLK&CLKREQ	HPD
PEG	DGPU (DIS)	CLK4 & & CLKREQ#4	
DDI1	NA		NA
DDI2	NA		NA
DDI3	NA		NA
eDP	Embedded Display		EDP_HPD

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCH SMBUS Address Table

PCH_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
PCH_SMBCLK PCH_SMBDATA	+3V_PCH_PRIM	JDIMM1	0X50	0XA0	0XA1
		JDIMM3	0X52	0XA4	0XA3
PCH_SML0CLK PCH_SML0DATA	+3VS	NA			
PCH_SML1CLK PCH_SML1DATA	+3VS	EC	TBC	TBC	TBC

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBUS Port1 EC_SMB_CK1 EC_SMB_DA1	+3VLP_EC	BAT	0x16	TBC	TBC
		CHGR	0x09	0x12	0x13
		TBT	Reserved	TBC	TBC
SMBUS Port2 EC_SMB_CK2 EC_SMB_DA2	+3VS	Current Mon 1	0x41	0x82	0x83
		Current Mon 2	0x40	0x80	0x81
		PCH	TBC		
		GPU	0x9E/0x9F	TBC	TBC
		Smart Amp	0x4C	0x98	0x99
		THERMAL	0x4D	0x9A	0x9B
		USB3.1 re-driver	0x29	0x52	0x53
SMBUS Port4 EC_SMB_CK4 EC_SMB_DA4	+3VS	G-sensor	0x1F	0x3E	0X3F
		Anti-ghost	TBC		

I2C Address Table

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
I2C_0_SCL I2C_0_SDA	+3VS				
		EC KB9542	TBC	TBC	TBC
I2C_1_SCL I2C_1_SDA	+3VS	Touch Pad	0x15	TBC	TBC

BOM Structure Table (1/2)

Function	Stuff	Note
Unit SKU	UMA@	
	DIS@	
Project SKU	Y730@	
Project SKU	15@	
	17@	
CFL-H SKU	CPU1@	i5-8300H-R1
	CPU2@	i7-8750H-R1
	CPU3@	i5-8300H
	CPU4@	i7-8750H
	CPU5@	i5-8300H-R3
	CPU6@	i7-8750H-R3
DGPU SKU	N17@	
	N18@	
PCH SKU HM370	PCH1@	SR40B-R1
	PCH2@	QNYF
	PCH3@	SR40B-R3
N17x SKU	GPU1@	1050Ti-R1
	GPU2@	1050Ti-R3
VRAM 4G	M4G@	X7678038L01
	H4G@	X7678038L02
	S4G@	X7678038L03
EC	9542@	
	9022@	
eSPI I/F	ESPI@	
	LPC@	
Debug	CMC@	
	DCI@	
Panel SKU	GSYNC@	
	NOGSYNC@	
Intel TBT TR	TBT@	
Intel CNVi	CNVI@	
LAN Mode	8111H_SW@	
	8111H_LDO@	
G Sensor	GSEN@	
ME Connector	ME@	
EMI Components	EMI@	@EMI@
ESD Components	ESD@	@ESD@
RF Components	RF@	@RF@

HSIO Port Table(PCH) HM370

HSIO Port	Capable	USB3.0	PCIE	SATA	Device	PCIE CLK&CLKREQ	NOTE
0	USB3.1_1(OTG)	1			USB3.1 PORT 1		Left Back
1	USB3.1_2	2			USB3.1 PORT 2		Right Back
2	USB3.1_3	3			USB3.1 PORT 3		Right Fornt
3	USB3.1_4	4					
4	USB3.1_5	5					
5	USB3.1_6	6					
6	USB3.1_7	7					
7	USB3.1_8	8					
8							
9							
10							
11							
12							
13							
14	PCIE_9 / GbE		9				
15	PCIE_10		10				
16	PCIE_11 / SATA_0A		11	0	HDD		
17	PCIE_12 / GbE / SATA_1A		12	1			
18	PCIE_13 / GbE / SATA_0B		13	0	LAN	CLK2 & & CLKREQ#2	
19	PCIE_14 / SATA_1B		14	1	WLAN+BT NGFF	CLK3 & & CLKREQ#3	
20	PCIE_15 / SATA_2		15	2			
21	PCIE_16 / SATA_3		16	3			
22	PCIE_17 / SATA_4		17	4			
23	PCIE_18 / SATA_5		18	5	NGFF SSD	CLK1 & & CLKREQ#1	Support SATA function on SATA#4
24	PCIE_19		19				
25	PCIE_20		20				
26	PCIE_21		21				
27	PCIE_22		22				
28	PCIE_23		23		Thunderbolt Intel Titan Ridge SP	CLK0 & & CLKREQ#0	
29	PCIE_24		24				

USB2.0 Port Table

USB2	Function
1	USB3.1 PORT 1
2	USB3.1 PORT 2
3	USB3.1 PORT 3
4	Anti-ghost IT8176
5	TBT TYPE-C
6	LED Controller IT8295
7	Camera
8	XBOX
9	Tobii
10	
11	
12	
13	
14	WLAN+BT NGFF

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	DS3
VIN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF
+VCC_SA	System Agent voltage Supply	ON	OFF	OFF	OFF	OFF
+VCC_GT/+VCC_GTX	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+VCC_EOPIO/+VCC_EDRAM	Processor EOPIO/EDRAM supply	ON	OFF	OFF	OFF	OFF
+1.05VALW	System +1.0V power rail	ON	ON	ON	ON*	OFF
+0.95VS_VCCIO	+1.0VS IO power rail	ON	ON	OFF	OFF	OFF
+1.05V_VCCMPHY	+1.0V power for PCH MODPHY rails	ON/OFF	ON/OFF	ON/OFF	ON/OFF	OFF
+0.95VS_DGPU	+0.95VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	ON	OFF	ON
+1.5VS_MEM_GFX	+1.5VS power rail for GPU/VRAM	ON	OFF	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*	OFF
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+2.5V	DDR4 +2.5Vpp power rail	ON	ON	ON	OFF	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VALW	+3VALW power for PCH suspend rails	ON	ON	ON	ON*	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON	ON
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

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Title: Notes List

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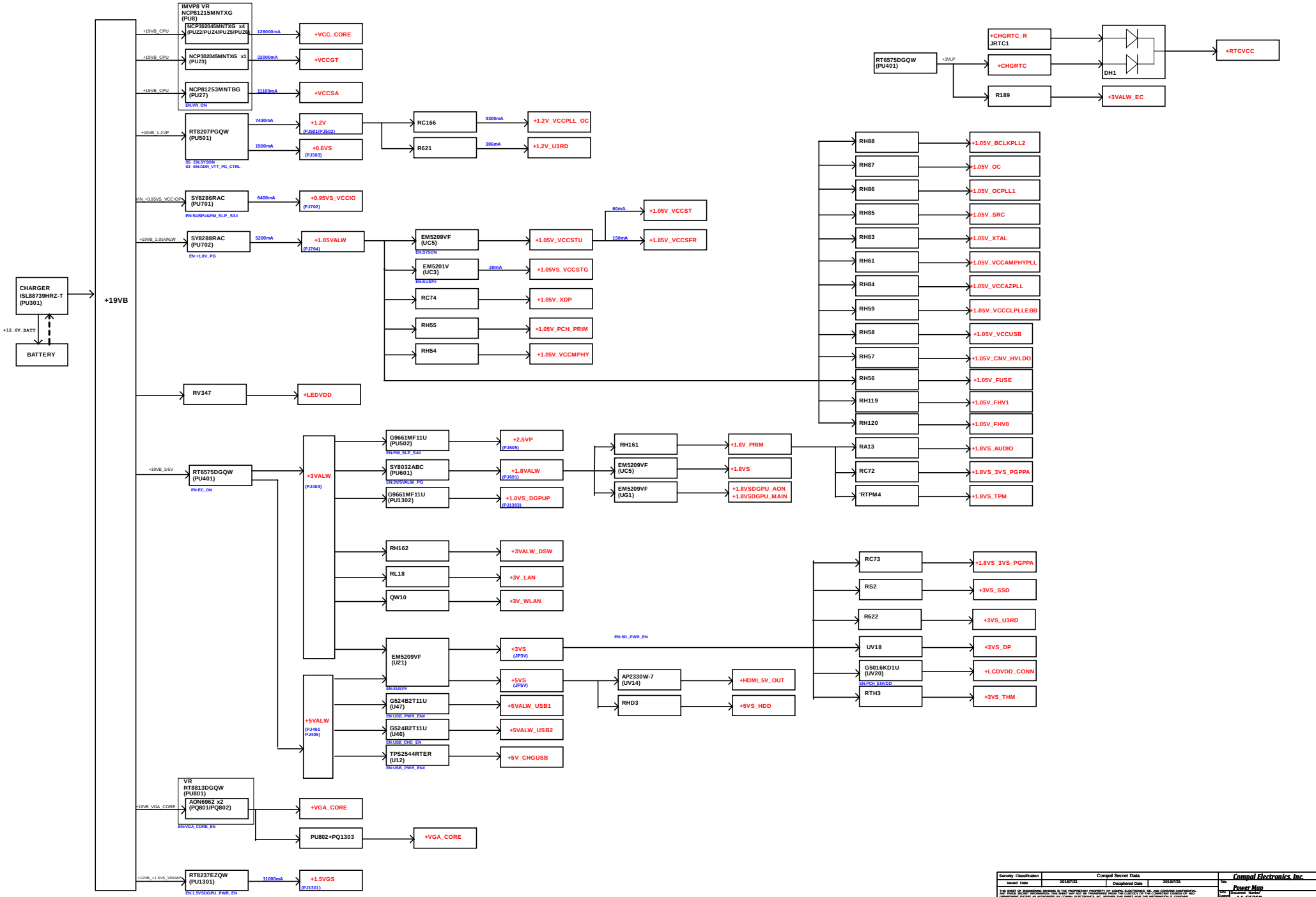

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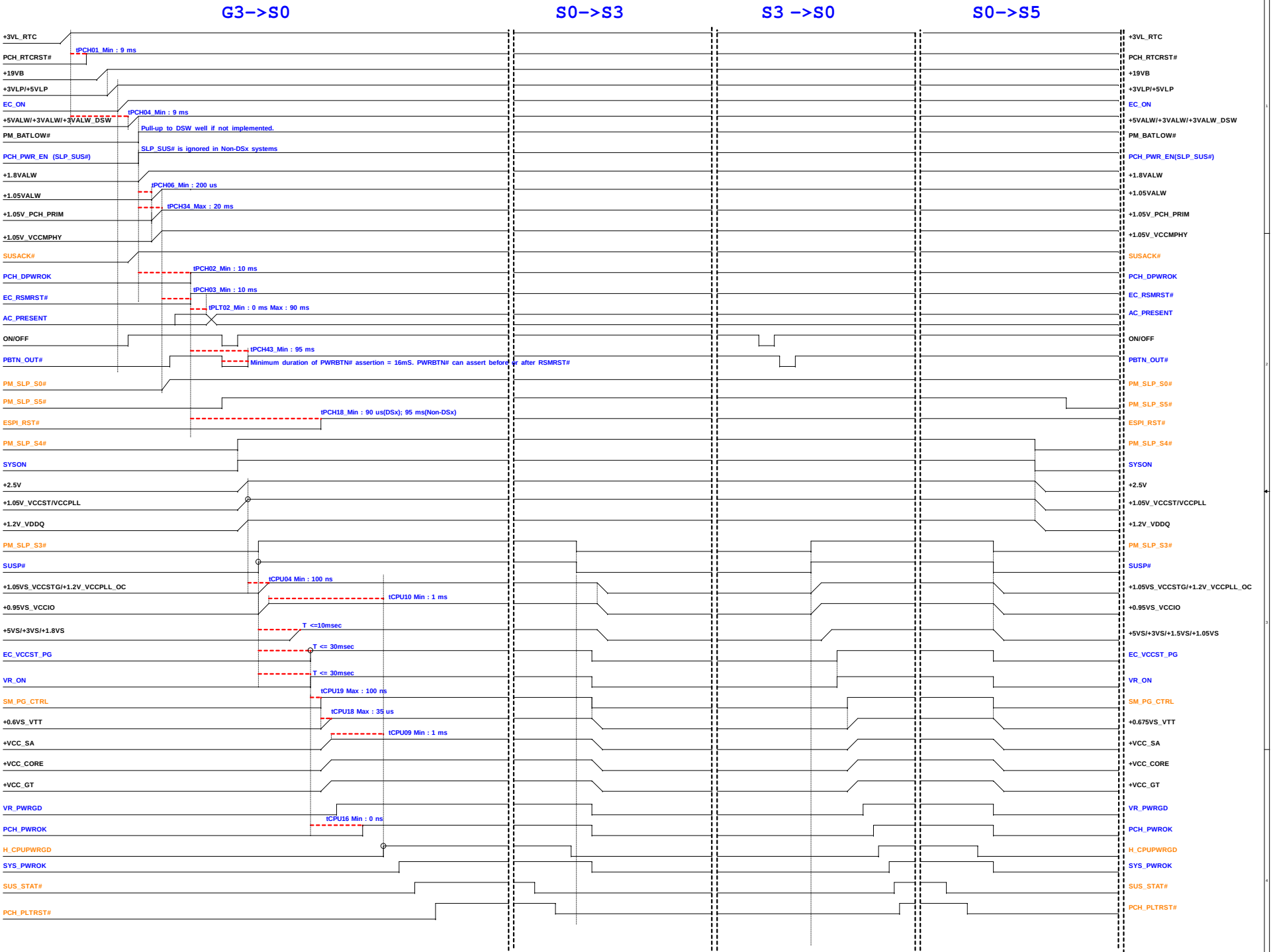
[DDX03 PWR Sequence_CFL-H 6+2_DDR4]



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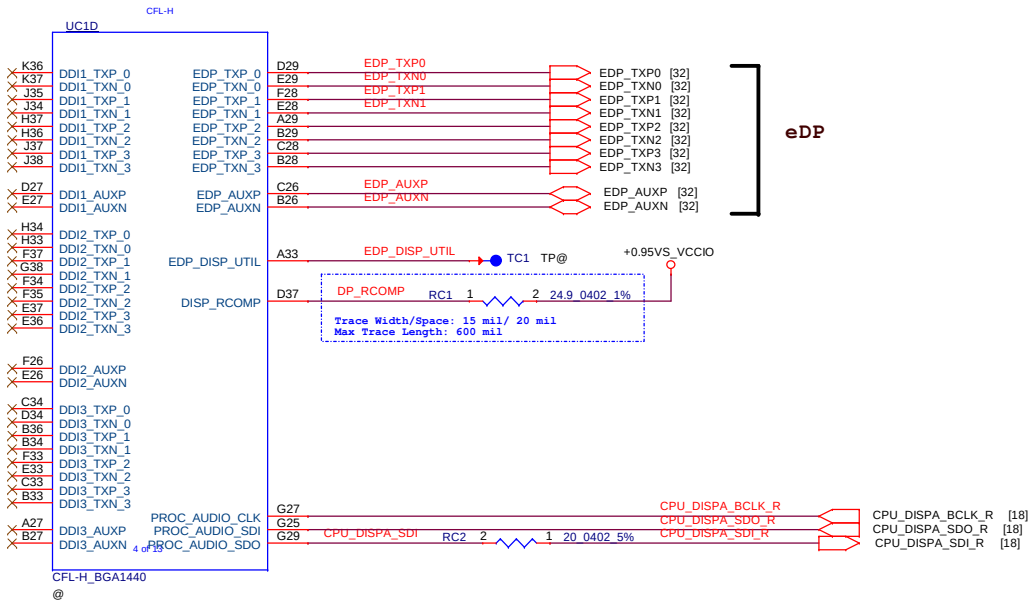

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Title: CFL-H(1/8)DDI/eDP

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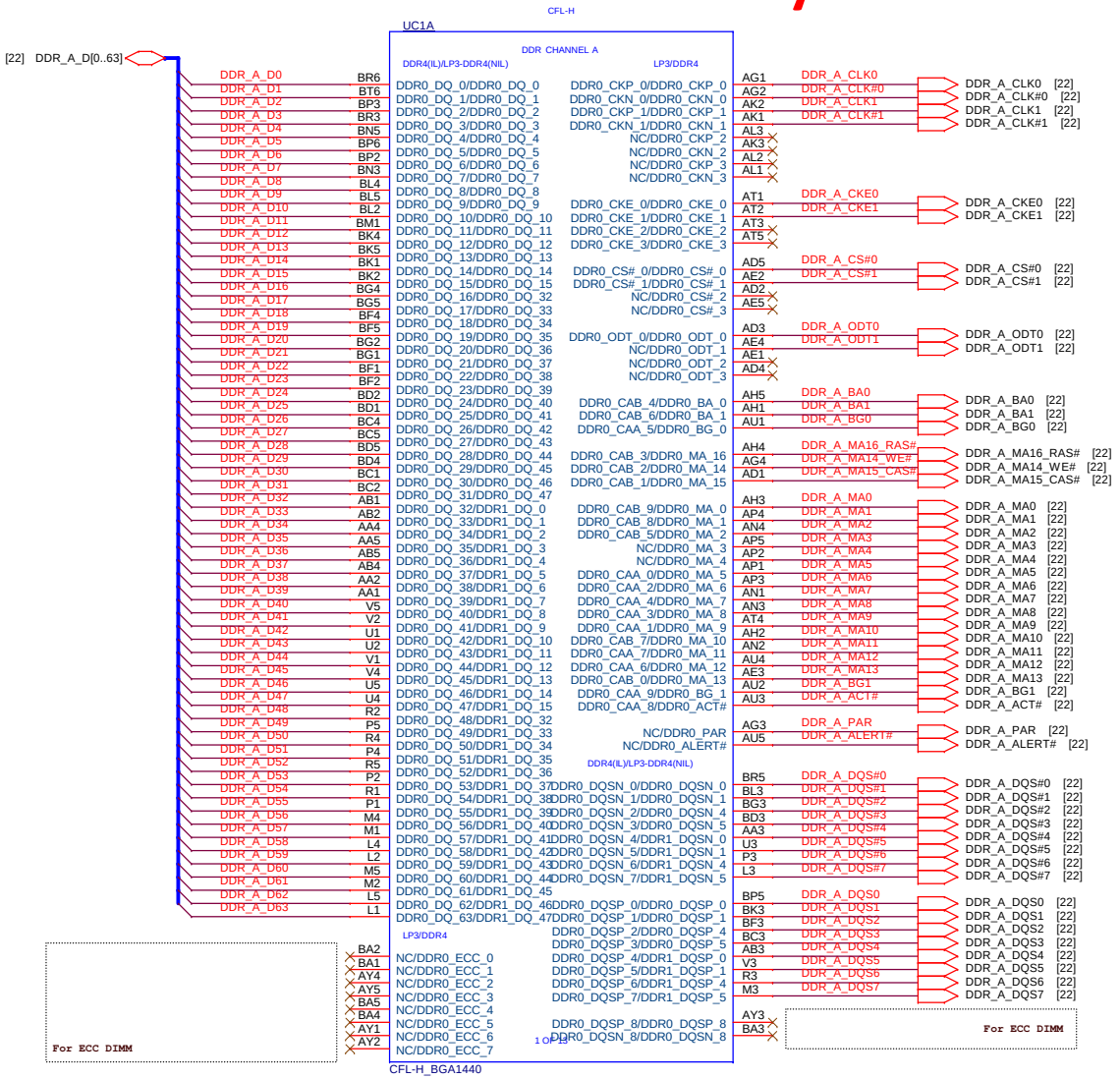
CHANNEL-A

Interleaved Memory



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Title: CFL-H(2/8)DIMMA

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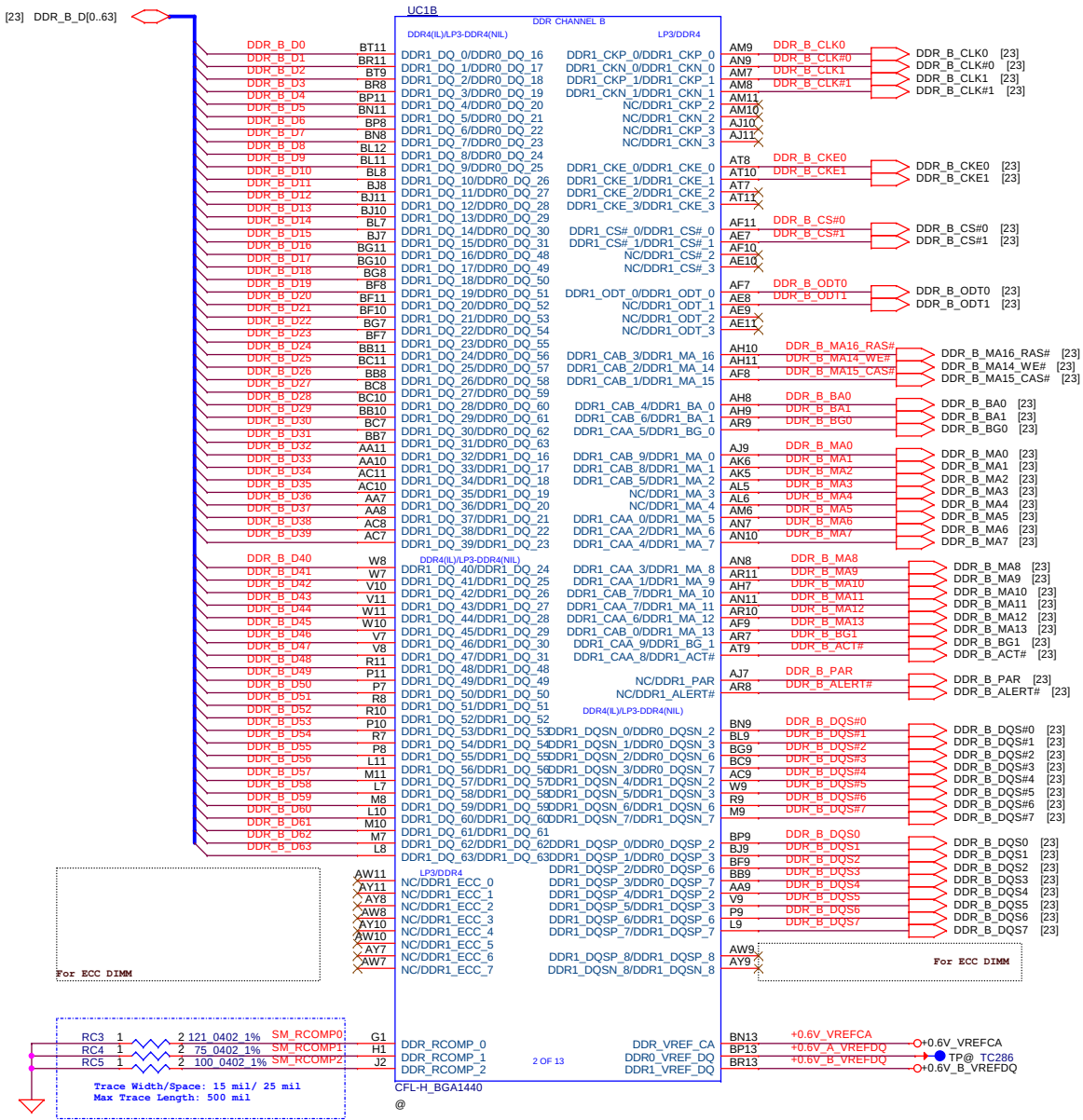
CHANNEL-B

Interleaved Memory



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Title	CFL-H(3/8)DIMMB		
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PEG&DMI

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Title: PEG/DMI

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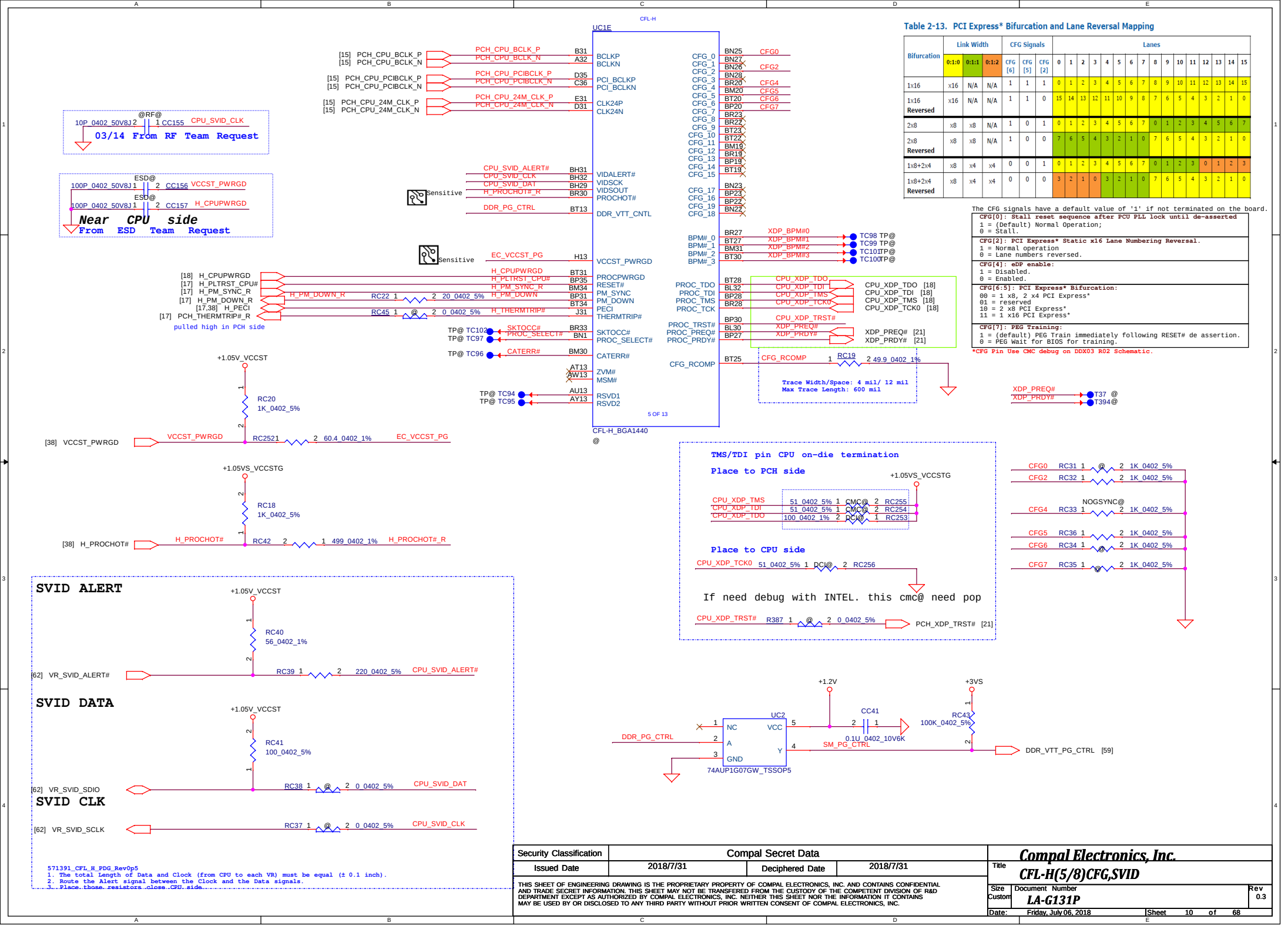

Table 2-13. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			CFG Signals			Lanes													
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 Reversed	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 Reversed	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 Reversed	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

The CFG signals have a default value of '1' if not terminated on the board.

CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted
1 = (Default) Normal Operation;
0 = Stall.

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
0 = Lane numbers reversed.

CFG[4]: eDP enable:
1 = Disabled.
0 = Enabled.

CFG[6:5]: PCI Express* Bifurcation:
00 = 1 x8, 2 x4 PCI Express*
01 = reserved
10 = 2 x8 PCI Express*
11 = 1 x16 PCI Express*

CFG[7]: PEG Training:
1 = (default) PEG Train immediately following RESET# de assertion.
0 = PEG Wait for BIOS for training.

*CFG Pin Use CMC debug on DDX03 R02 Schematic.

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Title	CFL-H(5/8)CFG,SVID		
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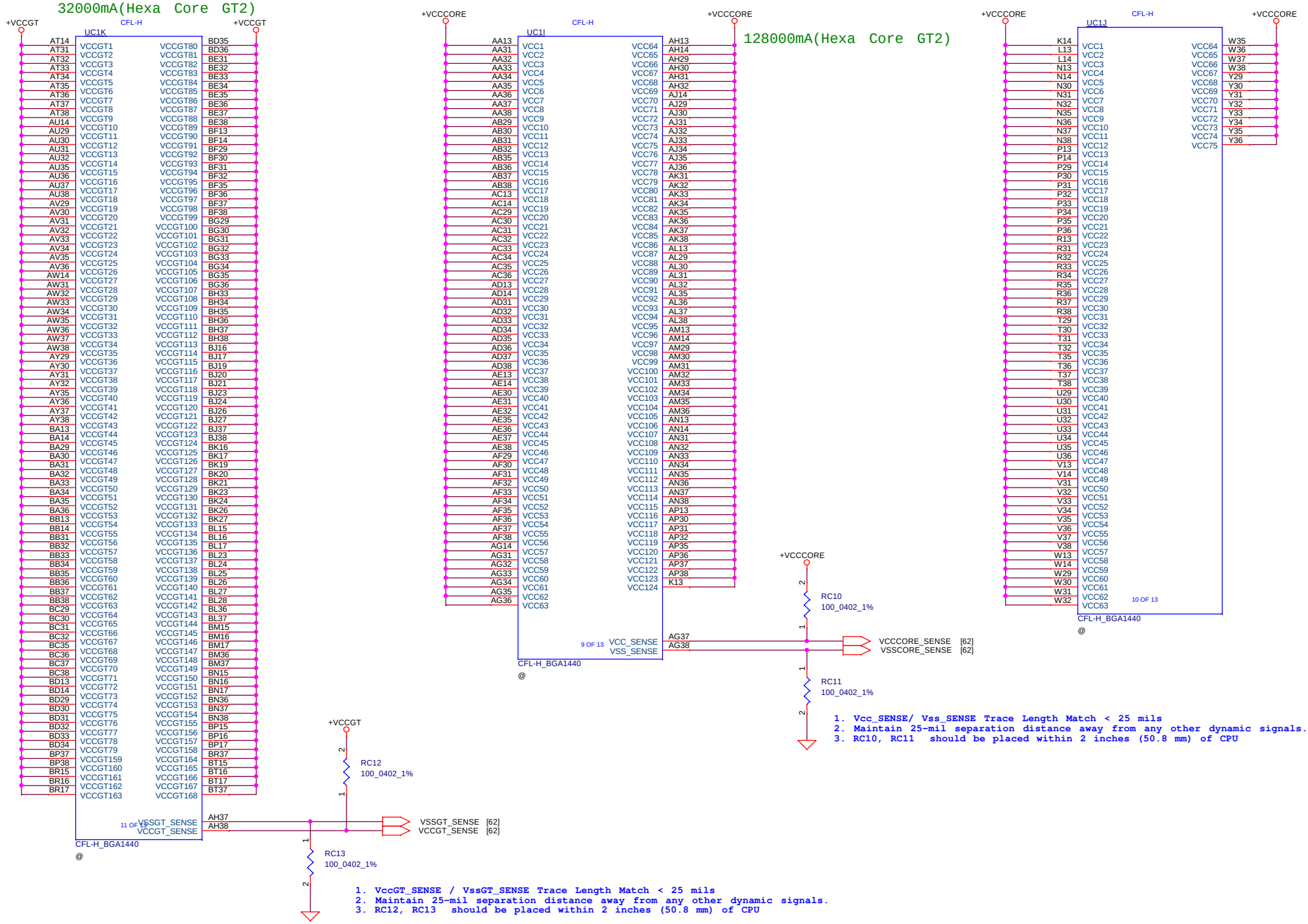

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Title: CFL-H(6/8)VCC CORE/GT

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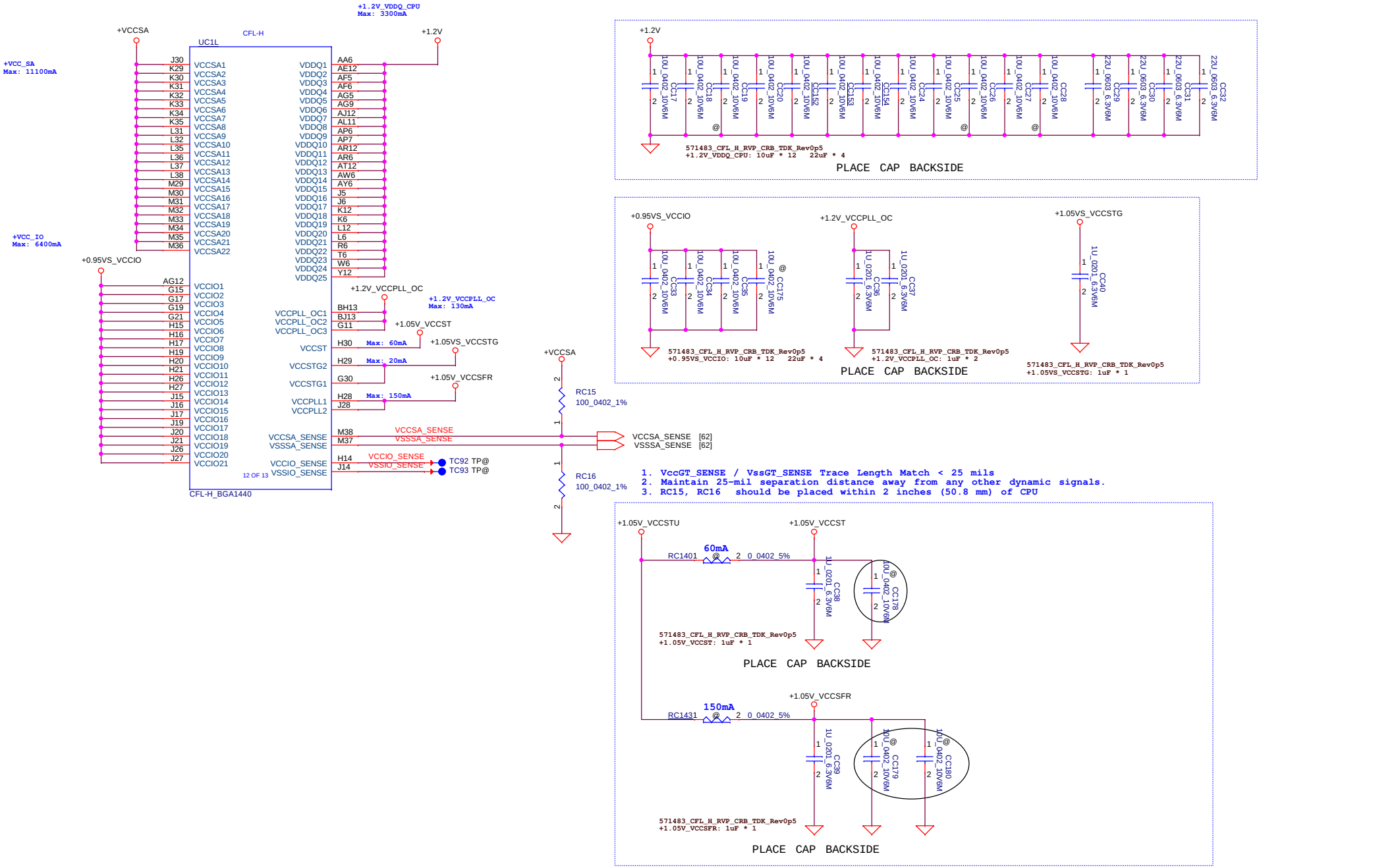

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Title: CFL-H(7/8)VCCSA/VCCIO/VDDQ

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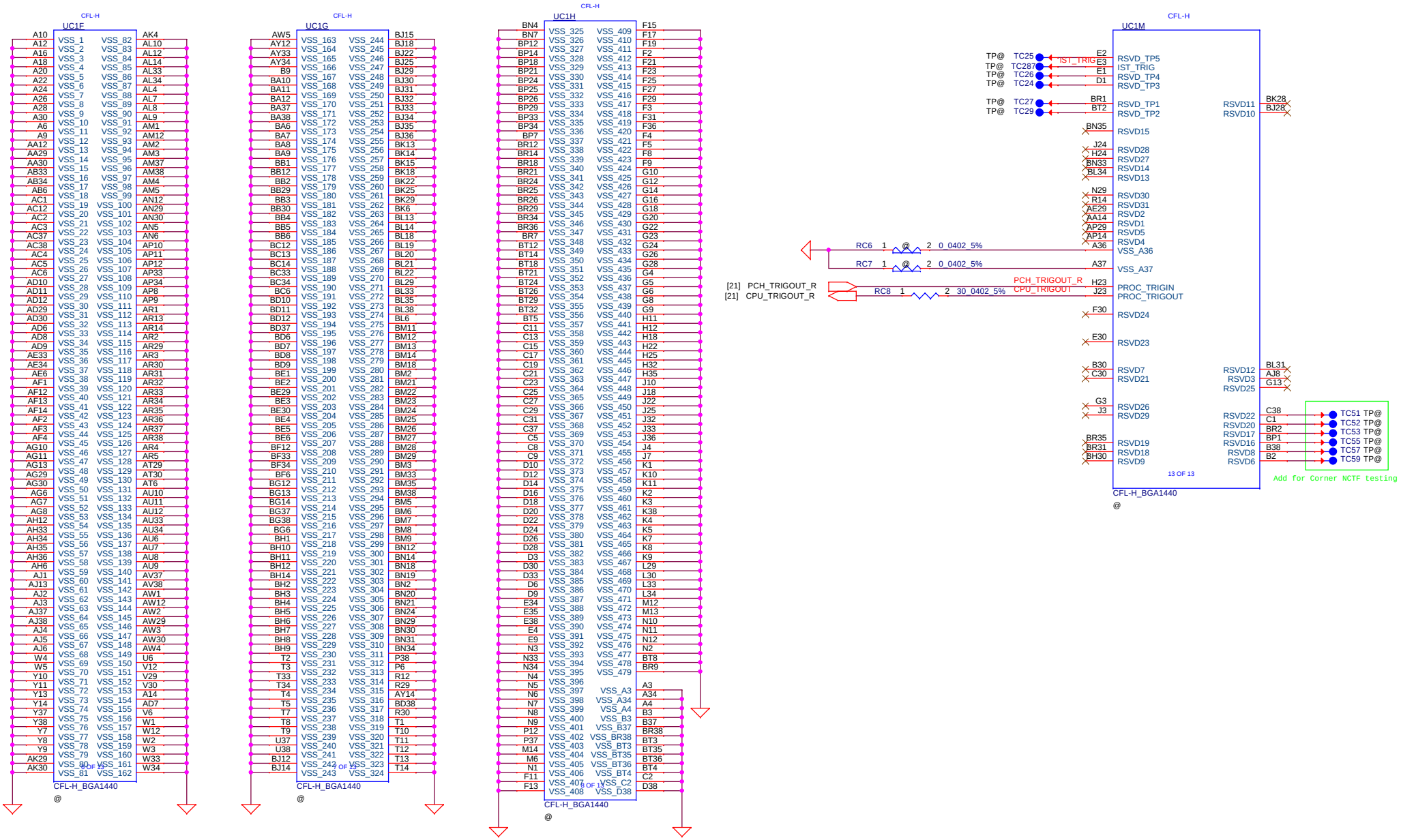

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Title: CFL-H(8/8)GND/RSVD

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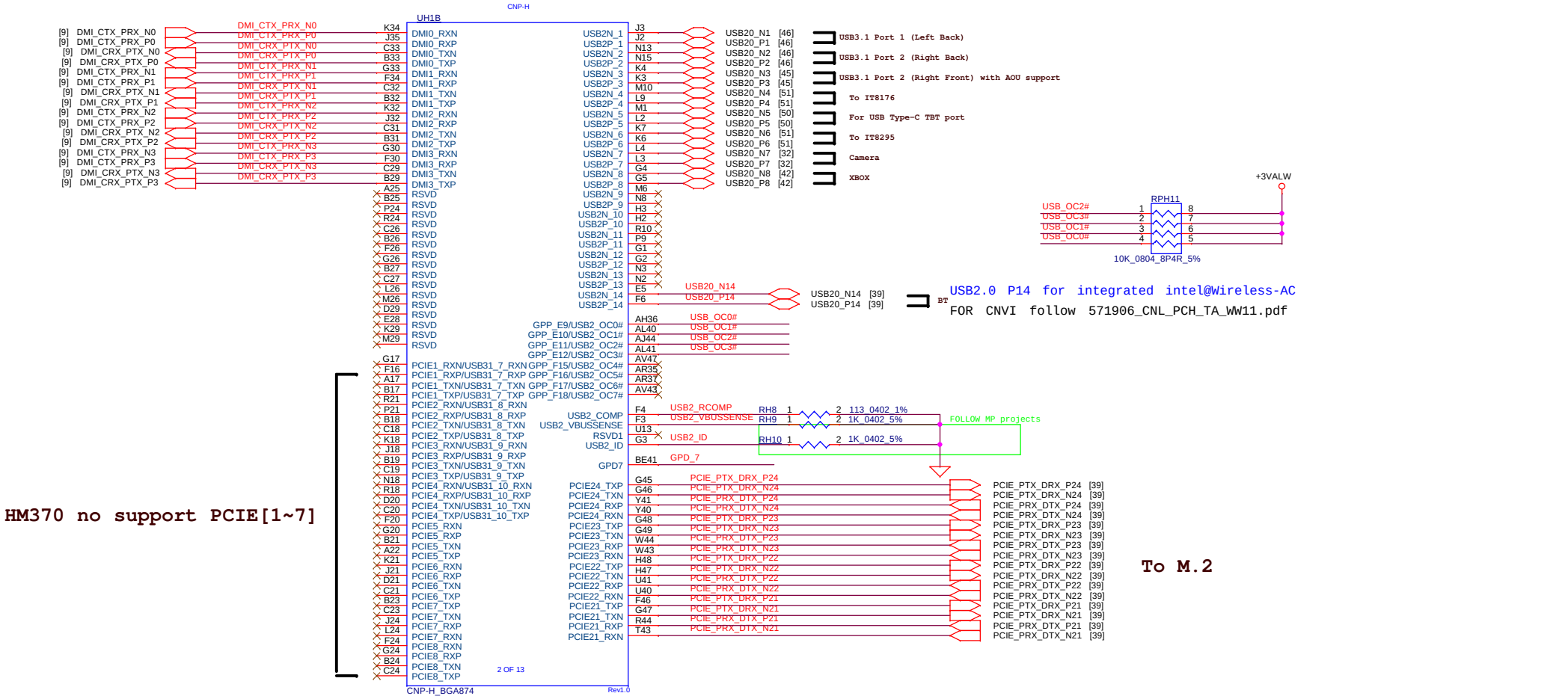
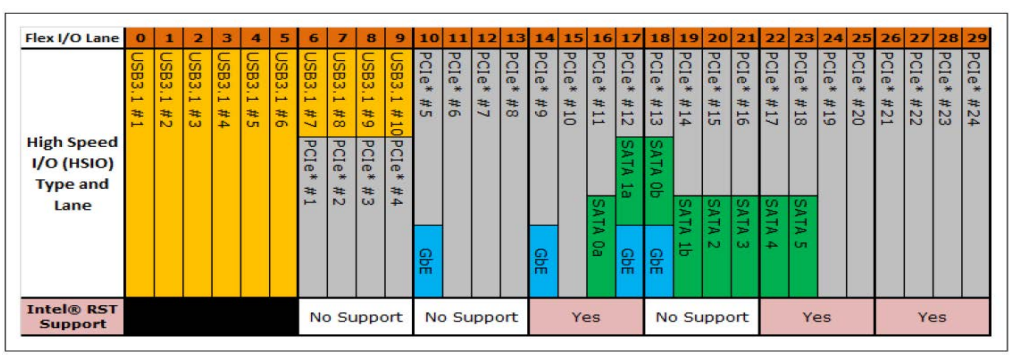
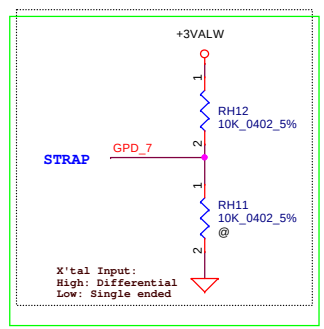




The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
– A maximum of 16 PCIe* Ports (or devices) can be enabled
• When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 – GbE (0 or 1)
– PCIe* Lanes 1–4 (PCIe* Controller #1), 5–8 (PCIe* Controller #2), 9–12 (PCIe* Controller #3), 13–16 (PCIe* Controller #4), 17–20 (PCIe* Controller #5), and 21–24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
– A maximum of 6 SATA Ports (or devices) can be enabled
– SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
– SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
– A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
– A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (IntelR Rapid Storage Technology) PCIe* storage devices
– x2 and x4 PCIe* NVMe SSD
– x2 IntelR Optane? Memory Device
– See the " PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers,configurations , and lanes that can be used for IntelR Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the IntelR Flash Image Tool (FIT) tool.



check its function

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Title: PCH(1/8)DMI/PCIE/USB2

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PCH-H XTAL_IN/OUT POR is 24MHz for 571697_CNL_MOW_WW16_2017.pdf

XTAL_24M_PCH_OUT
XTAL_24M_PCH_IN
RH17 1 EMI@ 2 33_0402_5% XTAL_24M_PCH_OUT_R
RH18 1 EMI@ 2 33_0402_5% XTAL_24M_PCH_IN_R

RH16 1 2 1M_0402_5%
24MHZ_18PF_XRCGB24M000F2P51R0
YH1 SJ10000UJ00 NC NC
27P_0402_50V8J CH4
27P_0402_50V8J CH5

PCH_RTCX1
PCH_RTCX2
RH19 1 2 10M_0402_5%
YH2
32.768KHZ_9PF_X1A000141000200
8P_0402_50V8D CH6
8P_0402_50V8D CH7
Trace Space: 15 mil
Max Trace Length: 1000 mil

+3VS
RPH3
TBT_CLKREQ0#
SSD_CLKREQ1#
LAN_CLKREQ2#
WLAN_CLKREQ3#
10K_0804_8P4R_5%
RH189 DIS@ 2 1 10K_0402_5% GPU_CLKREQ4#

For DDX03 R02

+1.8V_PRIM **XTAL Frequency Select**

RH26 1 2 4.7K_0402_5% CNV_BRI_PTX_DRX **STRAP**

This signal has a weak internal pull-down 20K.
0 = 38.4/19.2MHz XTAL frequency selected.
1 = 24MHz XTAL frequency selected. (DDX03)
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

+1.8V_PRIM **VCCPSPI Select**

RH93 1 @ 2 4.7K_0402_5% GPP_J9 **STRAP**

The signal has a weak internal pull-down 20K
0 = VCCPSPI is connected to 3.3V rail
1 = VCCPSPI is connected to 1.8V rail
Note: If VCCPSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

+1.8V_PRIM **M.2 CNV Mode Select**

RH167 2 1 10K_0402_5% CNV_RGI_PTX_DRX **STRAP**
RH168 2 @ 1 10K_0402_5%

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
Pulled down by CRF CNVi RGI_DT pin

RH20 1 2 60.4_0402_1% XCLK_BIASREF
XCLK_BIASREF
Trace Width/Space: 15mil /15 mil
Max Trace Length: 1000 mil

PCH_RTCX1
PCH_RTCX2

[47] TBT_CLKREQ0#
[39] SSD_CLKREQ1#
[40] LAN_CLKREQ2#
[39] WLAN_CLKREQ3#
[24] GPU_CLKREQ4#

CNP-H

UH1G

	GPP_A16/CLKOUT_48	BE33	TH74 TP@
[10] PCH_CPU_24M_CLK_P	CLKOUT_CPUNSSC_P	D7	
[10] PCH_CPU_24M_CLK_N	CLKOUT_CPUNSSC#	C6	
[10] PCH_CPU_BCLK_P	CLKOUT_CPUBCLK_P	B8	
[10] PCH_CPU_BCLK_N	CLKOUT_CPUBCLK#	C8	
XTAL_24M_PCH_OUT_R	XTAL_OUT	U9	
XTAL_24M_PCH_IN_R	XTAL_IN	U10	
XCLK_BIASREF	XCLK_BIASREF	T3	
PCH_RTCX1	RTCX1	BA49	
PCH_RTCX2	RTCX2	BA48	
[47] TBT_CLKREQ0#	GPP_B5/SRCCLKREQ0#	BF31	
[39] SSD_CLKREQ1#	GPP_B6/SRCCLKREQ1#	BE31	
[40] LAN_CLKREQ2#	GPP_B7/SRCCLKREQ2#	AR32	
[39] WLAN_CLKREQ3#	GPP_B8/SRCCLKREQ3#	BB30	
[24] GPU_CLKREQ4#	GPP_B9/SRCCLKREQ4#	BA30	
	GPP_B10/SRCCLKREQ5#	AN29	
	GPP_H0/SRCCLKREQ6#	AE47	
	GPP_H1/SRCCLKREQ7#	AC48	
	GPP_H2/SRCCLKREQ8#	AE41	
	GPP_H3/SRCCLKREQ9#	AF48	
	GPP_H4/SRCCLKREQ10#	AC41	
	GPP_H5/SRCCLKREQ11#	AC39	
	GPP_H6/SRCCLKREQ12#	AE39	
	GPP_H7/SRCCLKREQ13#	AB48	
	GPP_H8/SRCCLKREQ14#	AC44	
	GPP_H9/SRCCLKREQ15#	AC43	
	CLKOUT_PCIE_N15	V2	
	CLKOUT_PCIE_P15	V3	
	CLKOUT_PCIE_N14	T2	
	CLKOUT_PCIE_P14	T1	
	CLKOUT_PCIE_N13	AA1	
	CLKOUT_PCIE_P13	Y2	
	CLKOUT_PCIE_N12	AC7	
	CLKOUT_PCIE_P12	AC6	
	CLKOUT_ITPXDP#	Y3	TP@ TH73
	CLKOUT_ITPXDP_P	Y4	TP@ TH72
PCH_CPU_PCIBCLK_N	CLKOUT_CPUPCIBCLK#	B6	PCH_CPU_PCIBCLK_N [10]
PCH_CPU_PCIBCLK_P	CLKOUT_CPUPCIBCLK_P	A6	PCH_CPU_PCIBCLK_P [10]
	CLKOUT_PCIE_N0	AJ6	CLK_PCIE_N0 [47] Thunderbolt
	CLKOUT_PCIE_P0	AJ7	CLK_PCIE_P0 [47]
	CLKOUT_PCIE_N1	AH9	CLK_PCIE_N1 [39] NGFF SSD
	CLKOUT_PCIE_P1	AH10	CLK_PCIE_P1 [39]
	CLKOUT_PCIE_N2	AE14	CLK_PCIE_N2 [40] LAN
	CLKOUT_PCIE_P2	AE15	CLK_PCIE_P2 [40]
	CLKOUT_PCIE_N3	AE6	CLK_PCIE_N3 [39] WLAN
	CLKOUT_PCIE_P3	AE7	CLK_PCIE_P3 [39]
	CLKOUT_PCIE_N4	AC2	CLK_PEG_N4 [24] GPU
	CLKOUT_PCIE_P4	AC3	CLK_PEG_P4 [24]
	CLKOUT_PCIE_N5	AB2	
	CLKOUT_PCIE_P5	AB3	
	CLKOUT_PCIE_N6	W4	
	CLKOUT_PCIE_P6	W3	
	CLKOUT_PCIE_N7	W7	
	CLKOUT_PCIE_P7	W6	
	CLKOUT_PCIE_N8	AC14	
	CLKOUT_PCIE_P8	AC15	
	CLKOUT_PCIE_N9	U2	
	CLKOUT_PCIE_P9	U3	
	CLKOUT_PCIE_N10	AC9	
	CLKOUT_PCIE_P10	AC11	
	CLKOUT_PCIE_N11	AE9	
	CLKOUT_PCIE_P11	AE11	
	CLKIN_XTAL	R6	REFCLK_CNV [39] 1V@38.4MHZ

7 OF 13

CNP-H_BGA874 Rev1.0

@

RH173 1 2 10K_0402_5%

CNP-H

UH1M

	GPP_G0/SD_CMD	AW13	
	GPP_G1/SD_DATA0	BE9	
	GPP_G2/SD_DATA1	BF8	
	GPP_G3/SD_DATA2	BF9	
	GPP_G4/SD_DATA3	BG8	
	GPP_G5/SD_CD#	BE8	
	GPP_G6/SD_CLK	BD8	
	GPP_G7/SD_WP	AV13	
	GPP_I11/M2_SKT2_CFG0	AP3	
	GPP_I12/M2_SKT2_CFG1	AP2	
	GPP_I13/M2_SKT2_CFG2	AN4	
	GPP_I14/M2_SKT2_CFG3	AM7	
	GPP_J0/CNV_PA_BLANKING	AV6	
	GPP_J1/CPU_C10_GATE#	AY3	
	GPP_J11/A4WP_PRESENT	AR13	
	GPP_J10	AV7	
	GPP_J_2	AW3	
	GPP_J_3	AT10	
[39] CNV_BRI_PTX_DRX	GPP_J4/CNV_BRI_DT/UART0B_RTS#	AV4	CNV_BRI_PTX_DRX
[39] CNV_BRI_PRX_DTX	GPP_J5/CNV_BRI_RSP/UART0B_RXD	AY2	CNV_BRI_PRX_DTX
[39] CNV_RGI_PTX_DRX	GPP_J6/CNV_RGI_DT/UART0B_TXD	BA4	CNV_RGI_PTX_DRX
[39] CNV_RGI_PRX_DTX	GPP_J7/CNV_RGI_RSP/UART0B_CTS#	AV3	CNV_RGI_PRX_DTX
	GPP_J8/CNV_MFUART2_RXD	AW2	
GPP_J9	GPP_J9/CNV_MFUART2_TXD	AU9	
	CNV_WR_CLKN	BD4	CLK_CNV_PRX_DTX_N CLK_CNV_PRX_DTX_N [39]
	CNV_WR_CLKP	BE3	CLK_CNV_PRX_DTX_P CLK_CNV_PRX_DTX_P [39]
	CNV_WR_D0N	BB3	CNV_PRX_DTX_N0 CNV_PRX_DTX_N0 [39]
	CNV_WR_D0P	BB4	CNV_PRX_DTX_P0 CNV_PRX_DTX_P0 [39]
	CNV_WR_D1N	BA3	CNV_PRX_DTX_N1 CNV_PRX_DTX_N1 [39]
	CNV_WR_D1P	BA2	CNV_PRX_DTX_P1 CNV_PRX_DTX_P1 [39]
	CNV_WT_CLKN	BC5	CLK_CNV_PTX_DRX_N CLK_CNV_PTX_DRX_N [39]
	CNV_WT_CLKP	BB6	CLK_CNV_PTX_DRX_P CLK_CNV_PTX_DRX_P [39]
	CNV_WT_D0N	BE6	CNV_PTX_DRX_N0 CNV_PTX_DRX_N0 [39]
	CNV_WT_D0P	BD7	CNV_PTX_DRX_P0 CNV_PTX_DRX_P0 [39]
	CNV_WT_D1N	BG6	CNV_PTX_DRX_N1 CNV_PTX_DRX_N1 [39]
	CNV_WT_D1P	BF6	CNV_PTX_DRX_P1 CNV_PTX_DRX_P1 [39]
	CNV_WT_RCOMP	BA1	CNV_WT_RCOMP RH25 1 2 150_0402_1%
	PCIE_RCOMPN	B12	PCIE_RCOMPN RH21 1 2 100_0402_1%
	PCIE_RCOMPP	A13	PCIE_RCOMPP
	SD_1P8_RCOMP	BE5	SD_RCOMP_1P8 RH22 1 2 200_0402_1%
	SD_3P3_RCOMP	BE4	SD_RCOMP_3P3 RH23 1 2 200_0402_1%
	GPPJ_RCOMP_1P81	BD1	
	GPPJ_RCOMP_1P82	BE1	GPPJ_RCOMP_1P8 RH24 1 2 200_0402_1%
	GPPJ_RCOMP_1P83	BE2	
	RSVD2	Y35	
	RSVD3	Y36	
	RSVD1	BC1	
	TP	AL35	TP@ TH101

3.3V
1.8V

13 OF 13

CNP-H_BGA874 Rev1.0

@

#571483_CFL_H_RVP_CRB_TDK_Rev0p5
Recommend external test point

+1.8V_PRIM

RH1811 2 20K_0402_1% CNV_BRI_PRX_DTX
RH1821 2 20K_0402_1% CNV_RGI_PRX_DTX

571391_CFL_H_PDG_Rev0p71
To avoid floating input at the I/O pin BRI_RSP and RGI_RSP it is recommended to add a weak pull up resistor to the SoC pin with a recommended value of 20K ohm.

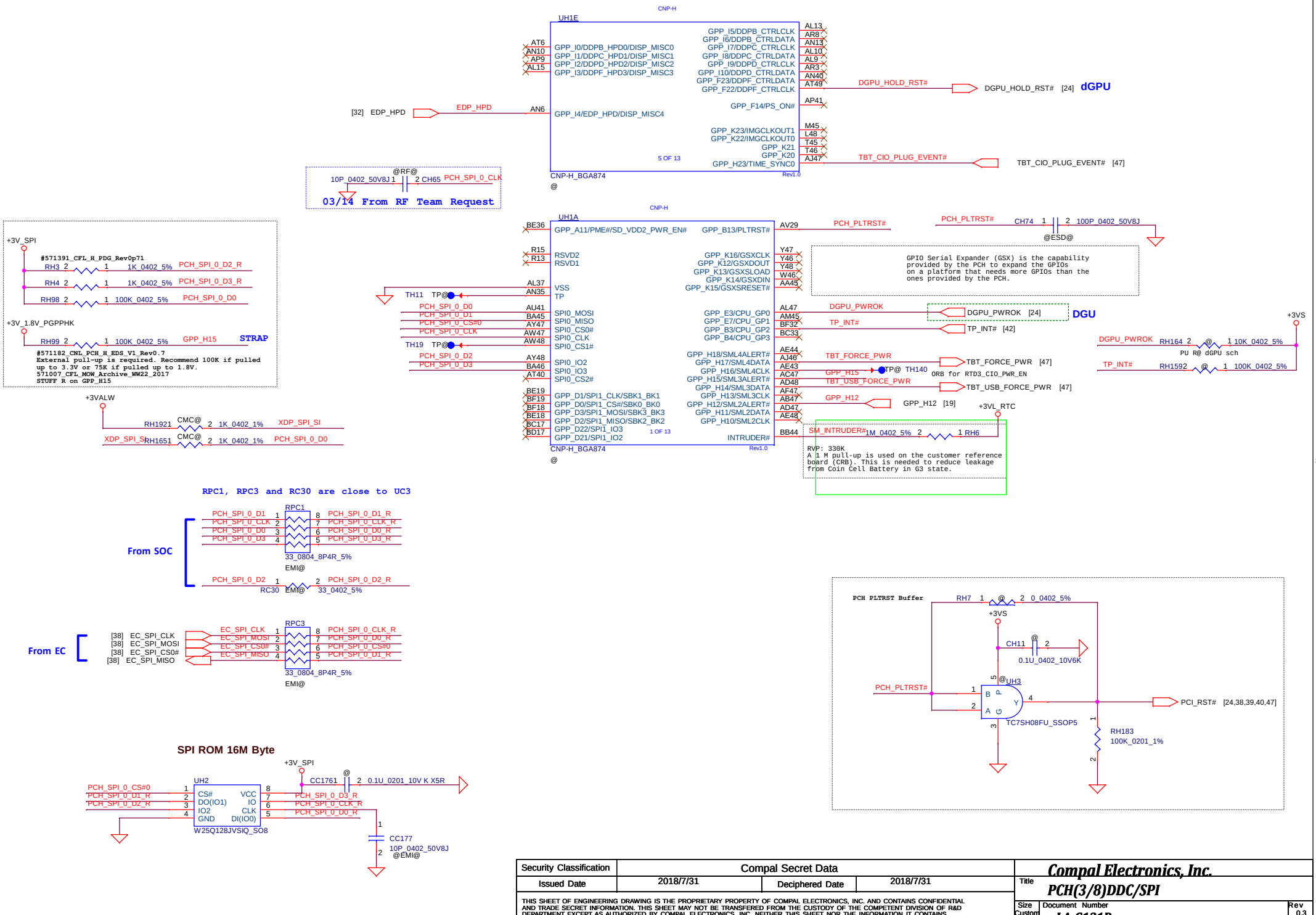
Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: PCH(2/8)CLK/CNVI/SD

Size	Document Number	Rev
Custom	LA-G131P	0.3

Date: Friday, July 06, 2018 Sheet 15 of 68



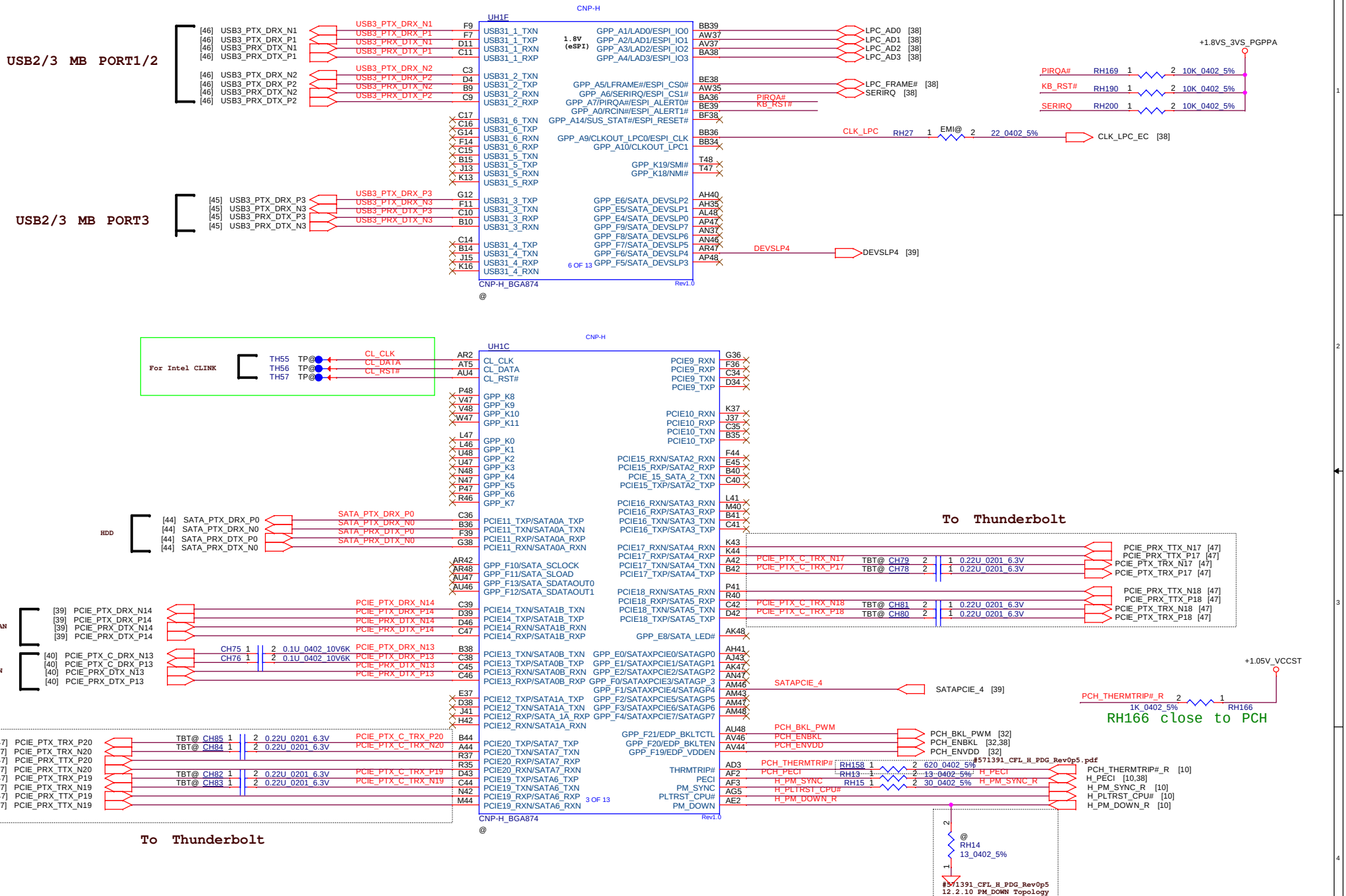
Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: PCH(3/8)DDC/SPI

Size: Custom | Document Number: LA-G131P | Rev: 0.3

Date: Friday, July 06, 2018 | Sheet 16 of 68



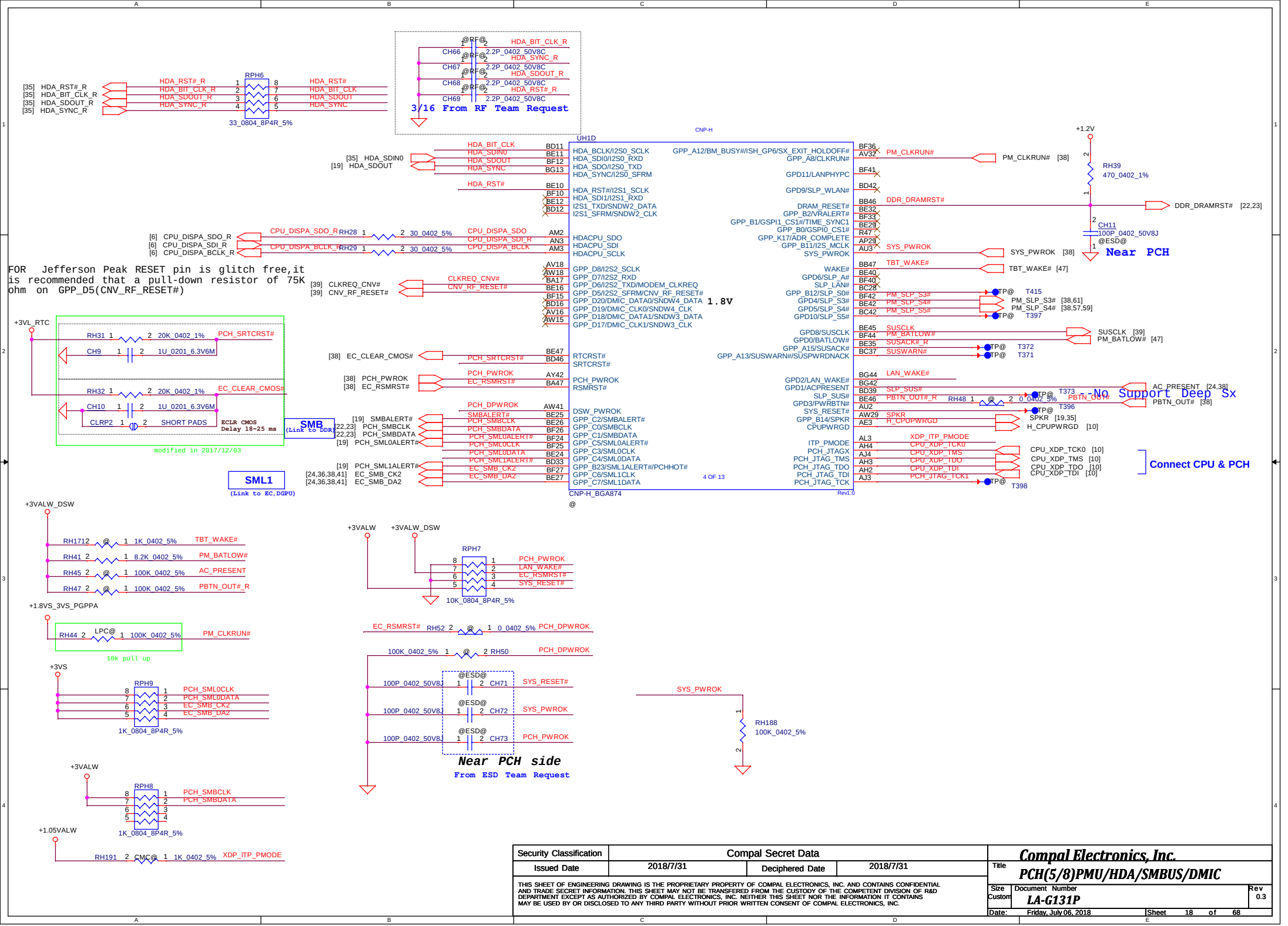
Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: PCIE/SATA/USB3/eSPI

Size	Document Number	Rev
Custom	LA-G131P	0.3

Date: Friday, July 06, 2018 Sheet 17 of 68



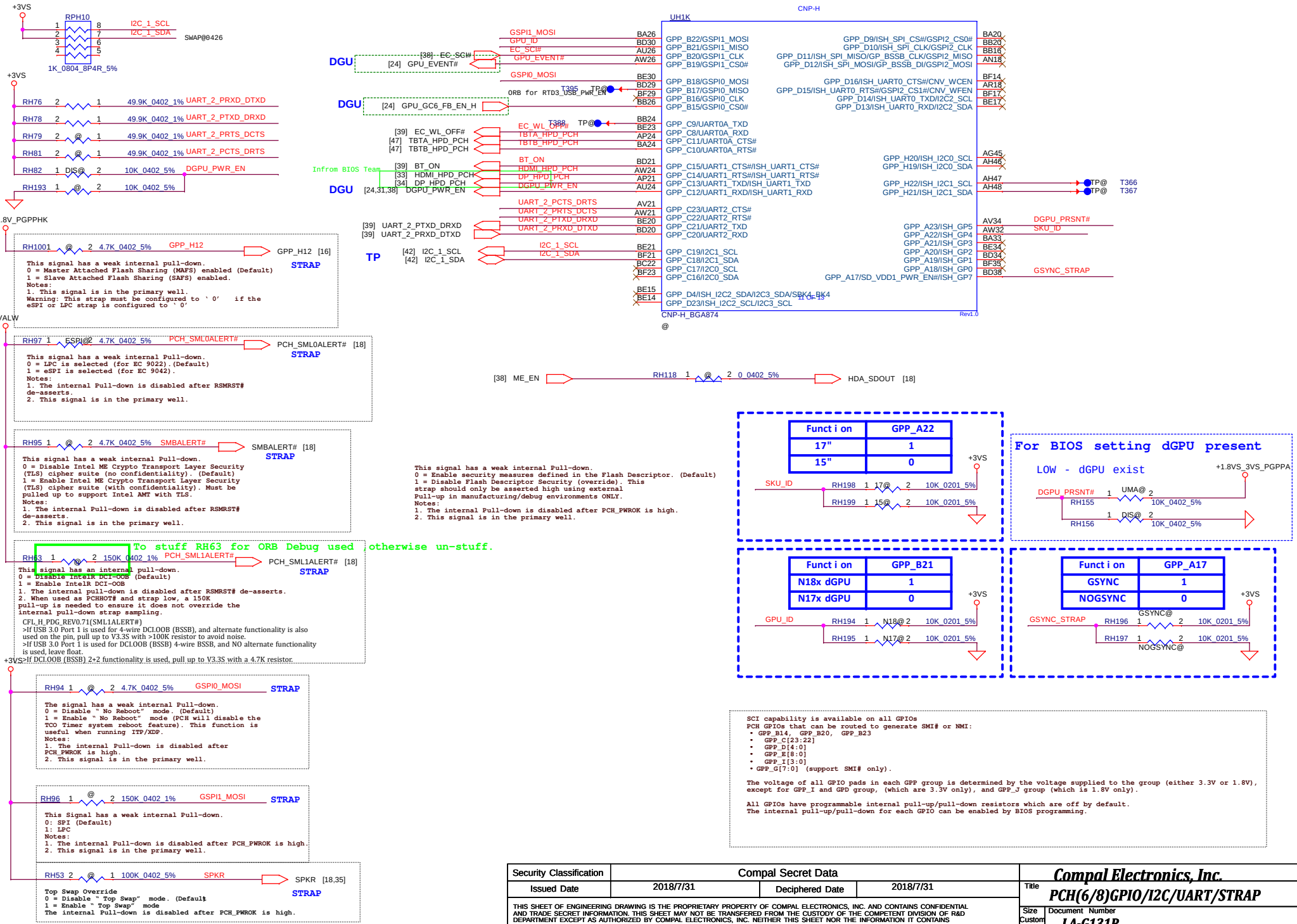
Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: PCH(5/8)PMU/HDA/SMBUS/DMIC

Size	Document Number	Rev
Custom	LA-G131P	0.3

Date: Friday, July 06, 2018 Sheet 18 of 68



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: PCH(6/8)GPIO/I2C/UART/STRAP

Size	Document Number	Rev
Custom	LA-G131P	0.3

Date: Friday, July 06, 2018 Sheet 19 of 68

GPIO Group	Voltage
GPPA	LPC: 3.3V eSPI: 1.8V ★
GPPB GPPC	3.3V
GPPD	1.8V for SOC_DMIC ★ 3.3V for IR_DMIC
GPPE GPPF	3.3V
GPPG	3.3V
GPPH GPPK	3.3V
GPPI	3.3V Only
GPPJ	1.8V Only
GPD	3.3V Only

PLACE 3-5MM FROM PACKAGE EDGE

HSIO for DMIU/USB3.1/PCIE=4162mA

W=20mils

RH174 for 571391_CFL_H_PDG_Rev0p71.pdf

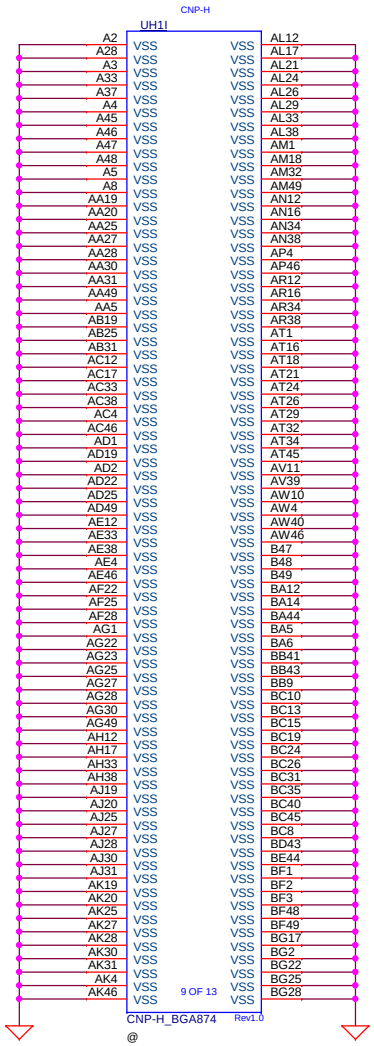
Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

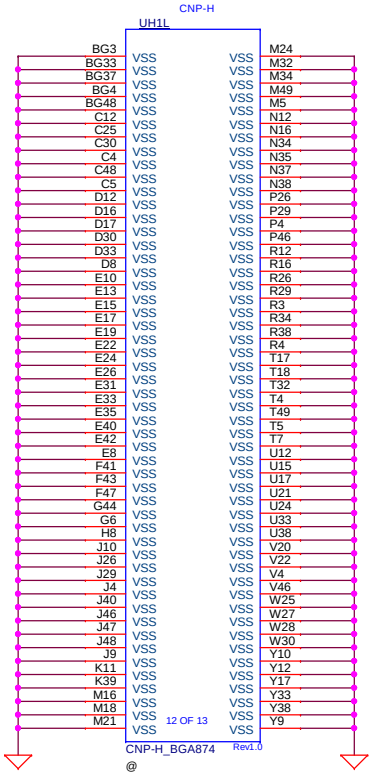
Compal Electronics, Inc.

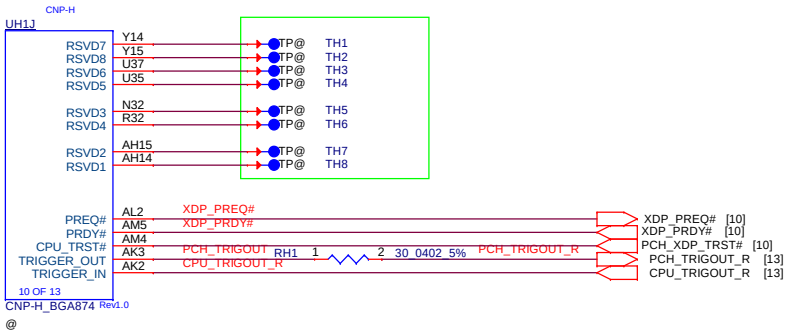
Title: PCH(7/8)Power

Size: Custom | Document Number: LA-G131P | Rev: 0.3

Date: Friday, July 06, 2018 | Sheet 20 of 68







Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

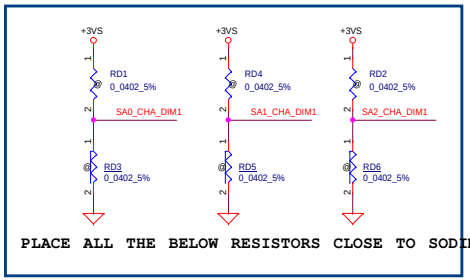
Compal Electronics, Inc.			
Title: PCH(8/8)GND/RSVD			
Size: Custom	Document Number: LA-G131P		Rev: 0.3
Date: Friday, July 06, 2018	Sheet 21 of 68		

CHANNEL-A

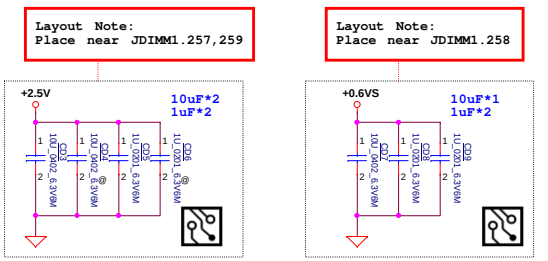
BOT REVERSE TYPE (4 mm)

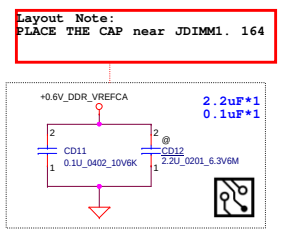
Interleaved Memory

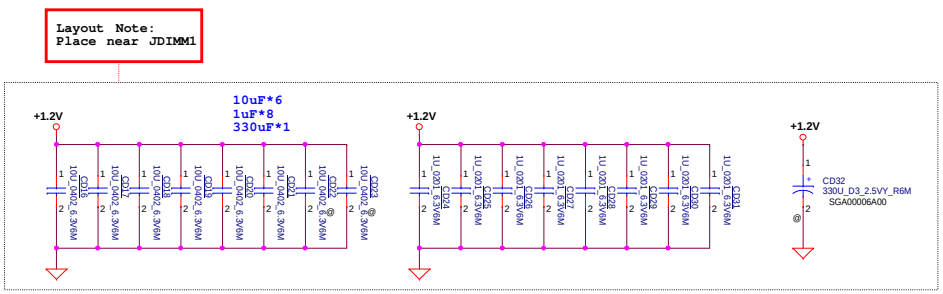
TOP: JDIMM1 CONN Non-ECC DIMM

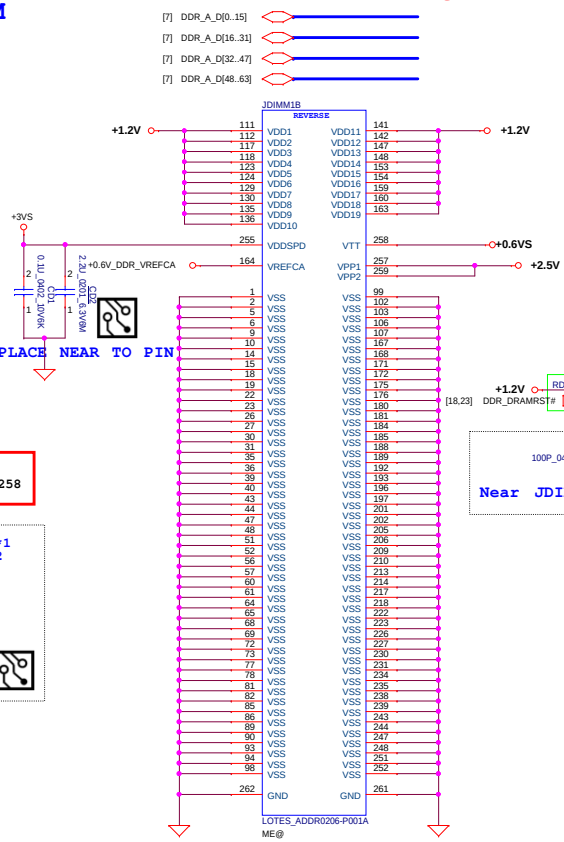


SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

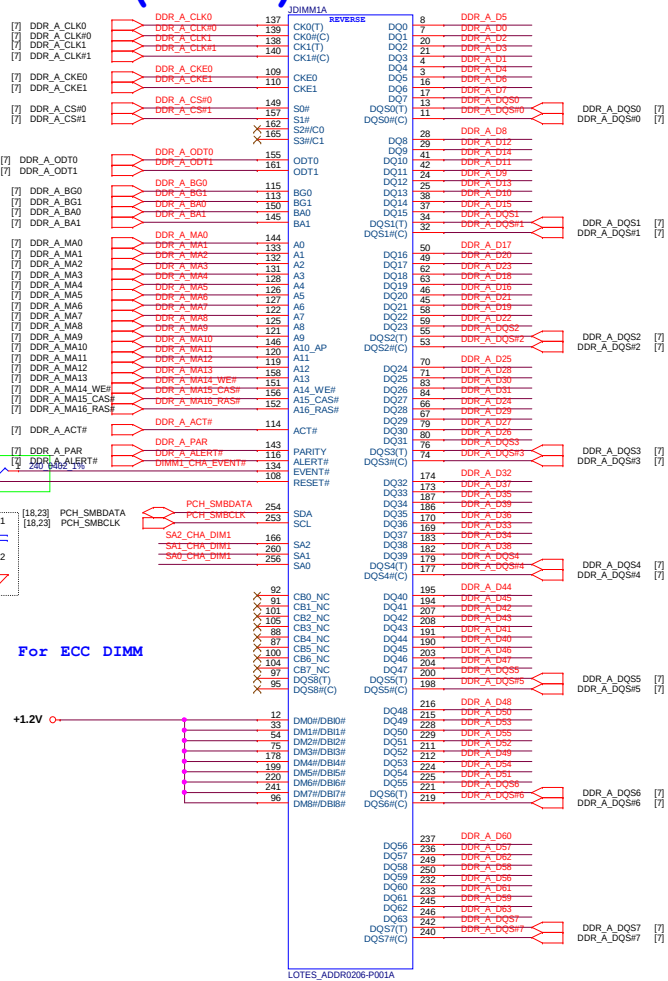


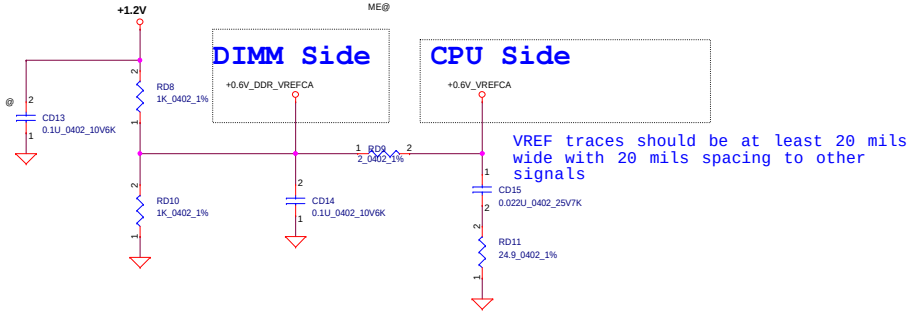






Part Number:SP07001FYH0
Part Value:S SOCKET FOX_AS0A826-H4RB-7H 260P DDR4



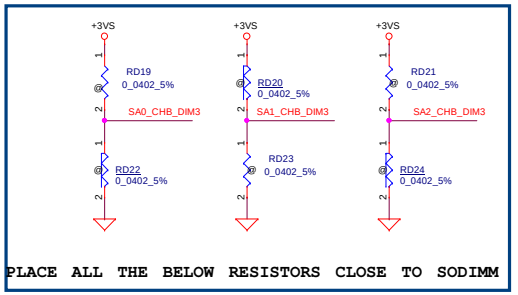


Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.	
Title	DDRIV_CHA: DIMM0
Size	Document Number: LA-G131P
Rev	0.3
Date:	Friday, July 06, 2018
Sheet	22 of 68

CHANNEL-B

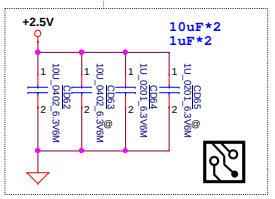
TOP: JDIMM3 CONN Non-ECC DIMM



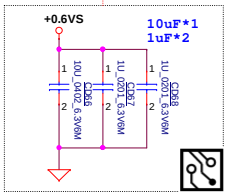
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

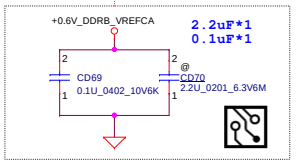
Layout Note:
Place near JDIMM3.257,259



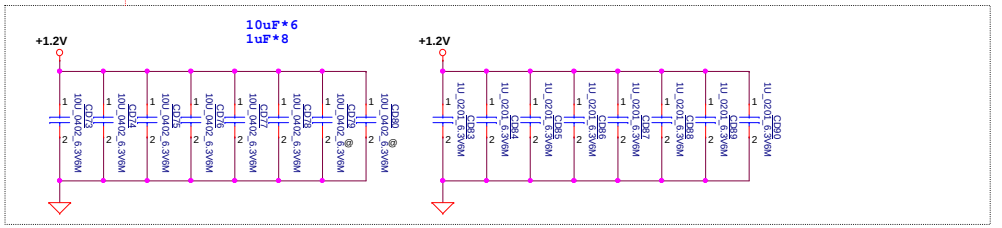
Layout Note:
Place near JDIMM3.258



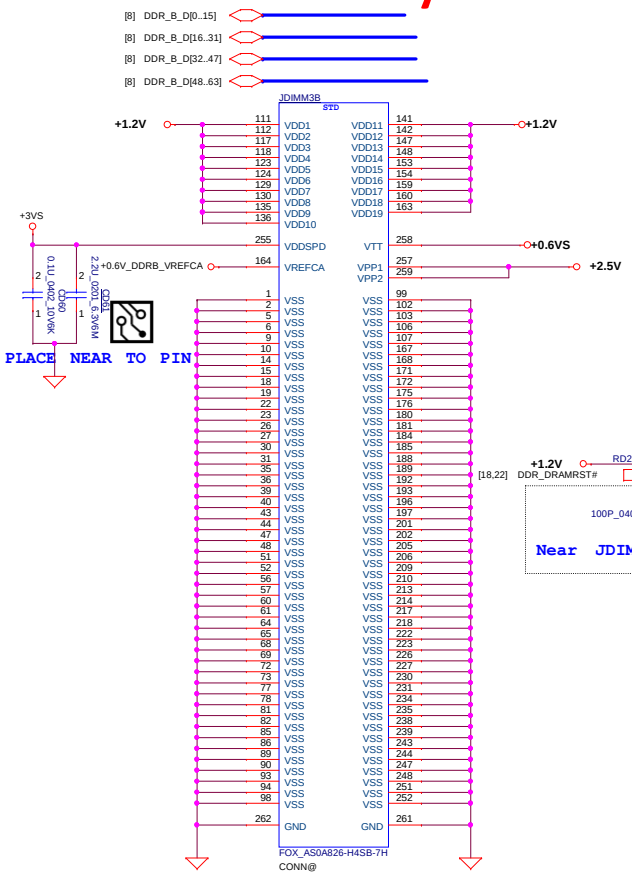
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM3



Layout Note:
Place near JDIMM3

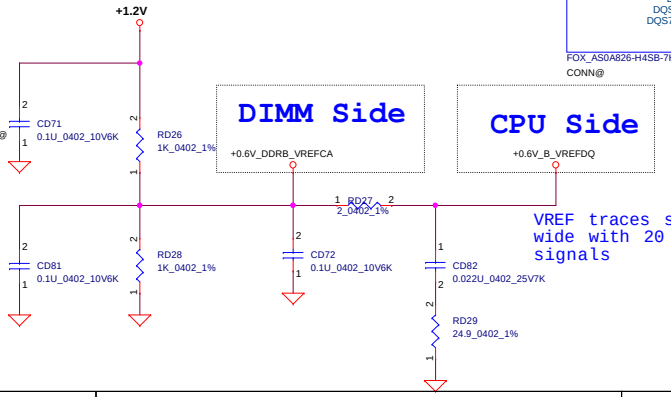


Interleaved Memory



Part Number:SP07001CEA0
Part Value:S SOCKET FOX_AS0A826-H4SB-7H 260P DDR4

BOT STD (4 mm)



VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: DDRIV_CHB: DIMM0

Size	Document Number	Rev
	LA-G131P	0.3

Date: Friday, July 06, 2018 | Sheet 23 of 68

GPIO	I/O	N17
GPIO0	O	NVVDD_PWM_VID
GPIO1	O	GC6_FB_EN
GPIO2	I	GPU_EVENT#/ WAKE*
GPIO3	O	NVVDD_SRAM_PWM
GPIO4	O	1V8_MAIN_EN
GPIO5	I	FRM_CLK
GPIO6	O	NVVDD_PSI
GPIO7	O	LCD_BL_PWM
GPIO8	O	MEM_VDD_CTL
GPIO9	I/O	THERM_ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	LCD_VDD
GPIO12	I	PWR_LEVEL
GPIO13	O	LCD_BLEN
GPIO14	I	HPD_IFPA
GPIO15	I	HPD_IFPB
GPIO16	O	SYS_PEX_RST_MON#
GPIO17	I	HPD_IFPD
GPIO18	I	HPD_IFPE
GPIO19	O	3D Vision
GPIO20		GC5_MODE
GPIO21	I/O	UNUSED
GPIO22	I/O	UNUSED
GPIO23	O	GPU_PEX_RST_HOLD#
GPIO24	I	HPD_IPFF
GPIO25		UNUSED
GPIO26		UNUSED
GPIO27	I	HPD_IPFC

GC6 2.1 function

GPU clock down to 1/4

Thermal shutdown protection

Double check the PG Pull up Resistor at power side.

Double check the PG Pull up Resistor at power side.

Crystals must have a max ESR of 80 ohm

VGS=0.95V

Enable: Vh:2.1V Vl:1V

Enable: Vh:1.5V Vl:0.7V

Delay 1.33ms

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

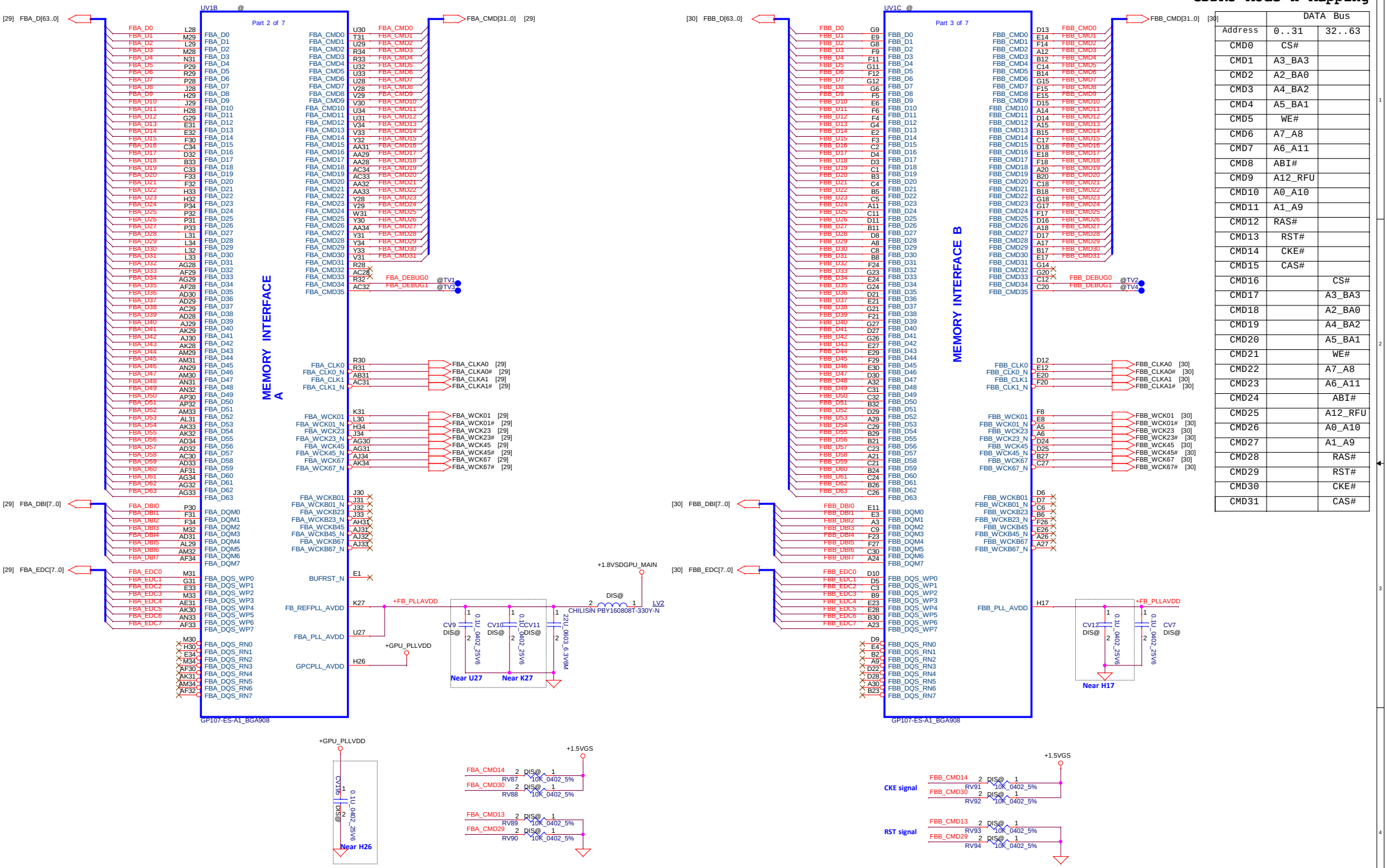
Title: N17P PEG 1/7

Size: C | Document Number: LA-G131P | Rev: 0.3

Date: Friday, July 06, 2018 | Sheet 24 of 68

GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#



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Title: **N17P VRAM 2/7**

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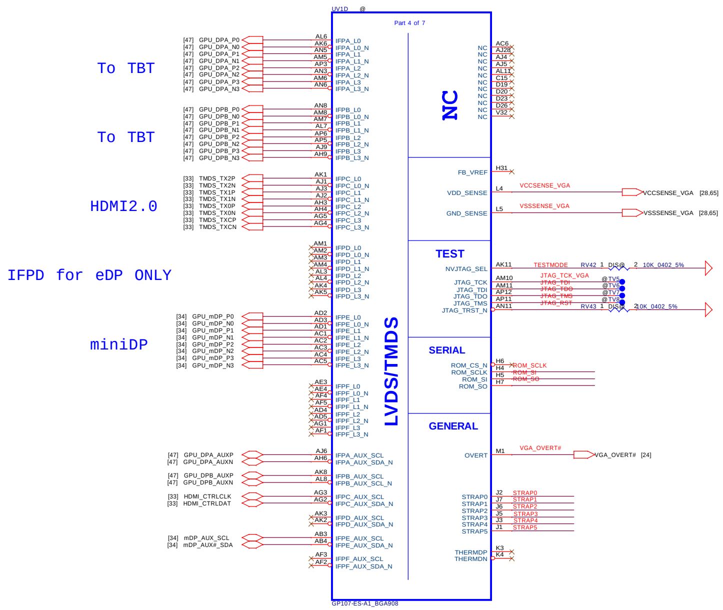

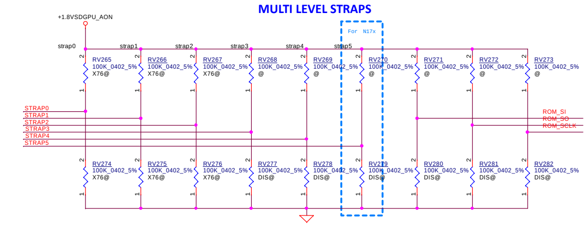

GDDR5 RAM_CFG															
GPU SKU	GPU	Memory Type	FBVDD/ FBVDDQ	Memory Density	Memroy configura tion	Vendor	Manufacturer Part Number	Die Revision	Memory Speed CK Grad	Memory D/C Minimum	Strap	Strap2	Strap1	Strap0	Status
	N17P-G0/G1	GDDR5	1.35V and 1.5V	8Gb	256Mx32	Samsung	K4G80325FB-HC28	B-die	7 Gbps	N/A	0x0	L	L	L	Prodution Candidate
						Micron	MT51J256M32HF-70:A	A-die	7 Gbps	N/A	0x1	L	L	H	Prodution Candidate
						Hynix	H5GC8H24MJR-R0C	M-die	7 Gbps	N/A	0x2	L	H	L	Post-Prodution Candidate
				4Gb	128Mx32	Samsung	K4G41325FE-HC28	E-die	7 Gbps	N/A	0x7	H	H	H	Prodution Candidate
						Hynix	H5GC4H24AJR-R0C	A-die	7 Gbps	N/A	0x6	H	H	L	Prodution Candidate
			1.35V and 1.55V			Micron	EDW4032BABG-70-F	A-die	7 Gbps	N/A	0x8	L	L	M	Post-Prodution Candidate

- **SMB_ALT_ADDR Enable**: This strap function allows an alternate SMBus address to be configured, so that graphics circuits with multiple GPUs can have separate SMBus connections for each GPU. In dual GPU configurations, use of the alternate address on one GPU (by setting this function to '1') avoids conflicts between the two GPUs on an SMBUS port. The "SMB_ALT_ADDR disabled" setting ('0') is correct for single-GPU graphics circuits. (see Section 13.3.2.1 for the SMBus address.)
- **DEVID_SEL**: NVIDIA defines an original and a re-brand Device ID on a per-GPU basis. This Device ID Select strap function allows selection between the original PCIe Device ID defined for the GPU (via a function setting of '0'), and the alternate "re-brand" Device ID defined for the GPU (via a function setting of '1').
- **PCIE_CFG**: This function sets electrical characteristics of PCIe lanes, in particular signal amplitude (swing). A setting of '0' selects normal (full) signal swing. N17x graphics circuits should strap for this setting. (A setting of '1' designates reduced signal amplitude, available if special concerns require. Consult NVIDIA for guidance.)
- **VGA_DEVICE**: This strap function is used to report the graphics circuit either as a 3D device (class code 302, designated by a setting of '0' for this strap) or as a VGA device (class code 300, designated by a setting of '1') to the host system. The 3D Device (class code 302, strap='0') setting is correct for most MS-Hybrid notebook GeForce graphics circuits.

6.3 UNCONNECTED SIGNALS (NC)

The Video BIOS (VBIOS) may be integrated into the System BIOS (SBIOS), therefore the VBIOS ROM interface may be left unused. If the VBIOS ROM interface is not used, then the ROM_CS, ROM_SCLK, ROM_SI, and ROM_SO pins need not be connected to a ROM device. (Note that the ROM_SCLK, ROM_SI, and ROM_SO pins also fill ternary strap functions; see Chapter "GPU Straps" for specifics on how they should be connected.)

Table 5.5 SORx_EXPOSED Strap Enablement for Dover Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

Table 10.3 GB4C-128 Standard Configurations

Link	Standard Display Configurations	
Link A	DisplayPort, DVI (Single Link)	DVI (Dual Link)
Link B	DisplayPort, DVI (Single Link)	
Link C	DisplayPort, HDMI, DVI (Single Link)	
Link D	eDP only (does not support drive of an external display)	
Link E	DisplayPort, HDMI, DVI (Single Link)	DVI (Dual Link)
Link F	DisplayPort, HDMI, DVI (Single Link)	
Note: Maximum of four independent simultaneously served display heads supported. **Note:** eDP is supported on IFPD only		

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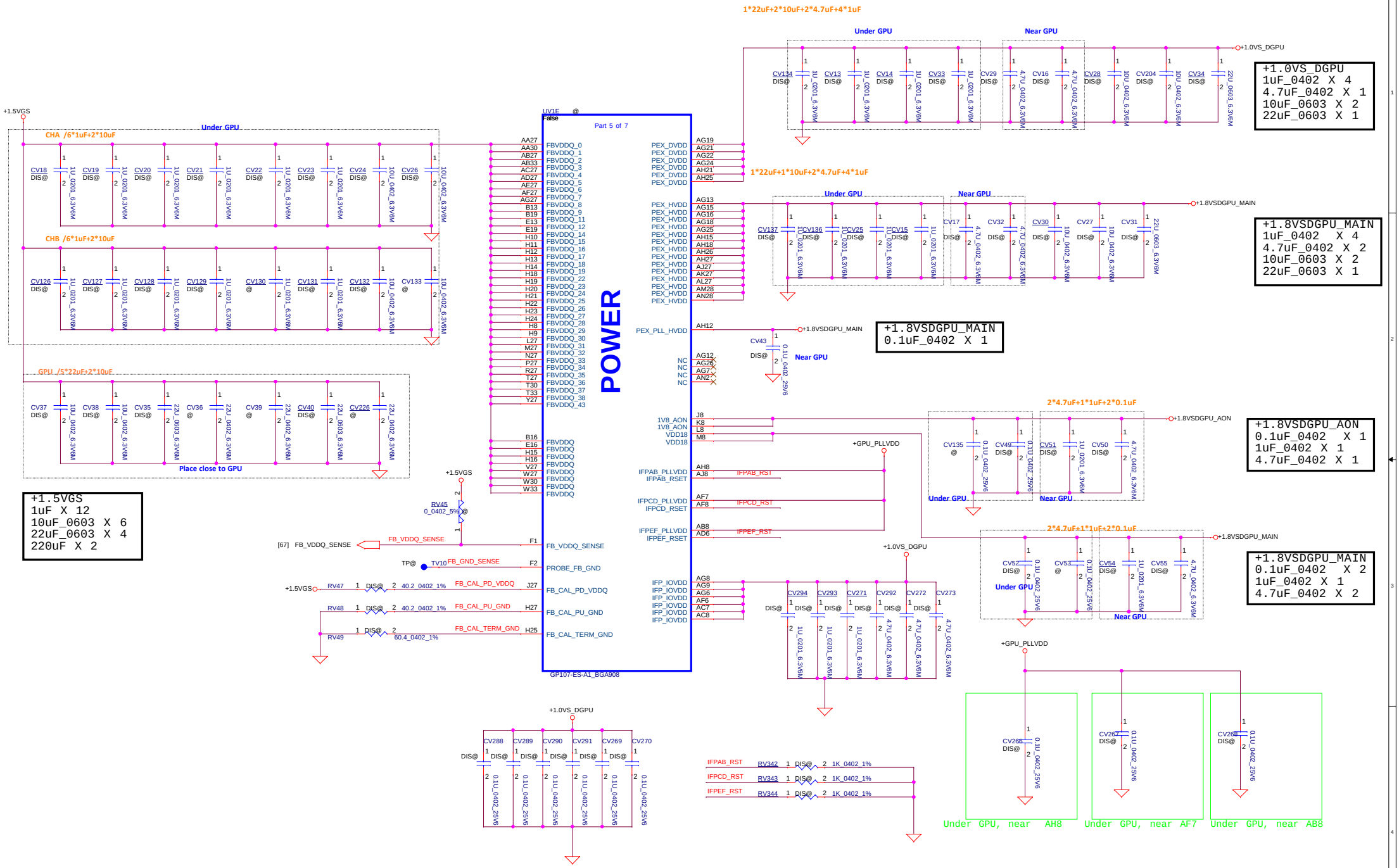
				Size: D; Document Number: LA-G131P; Rev: 0.3
				Date: Friday, July 06, 2018; Sheet 26 of 68



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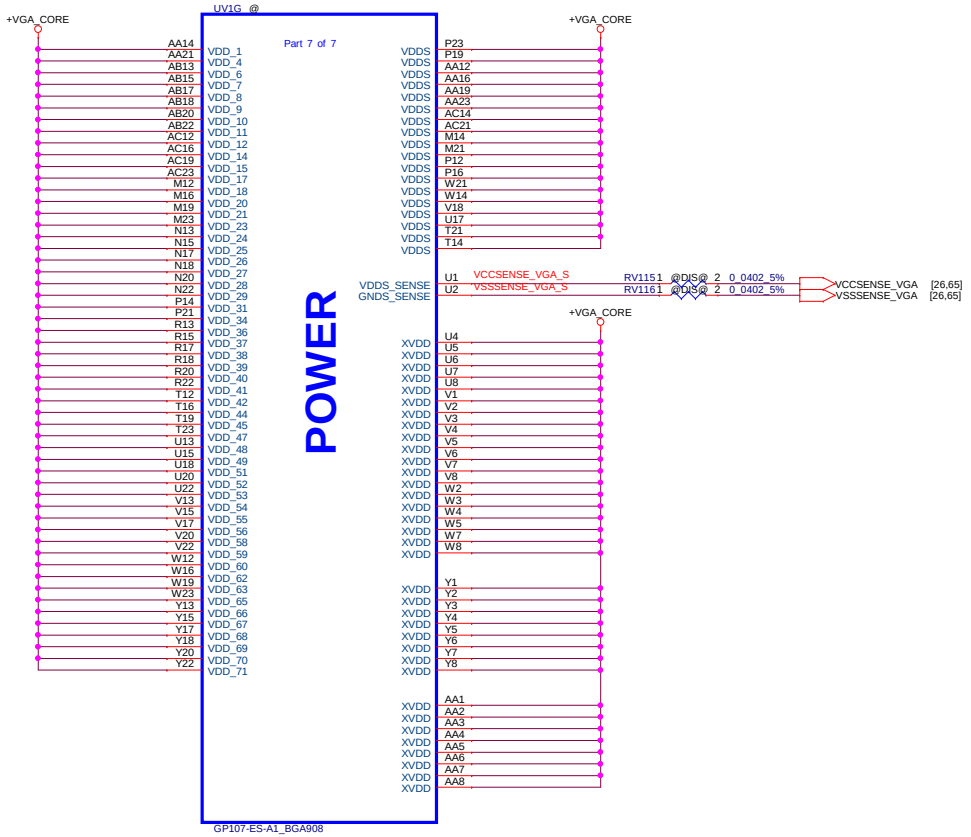
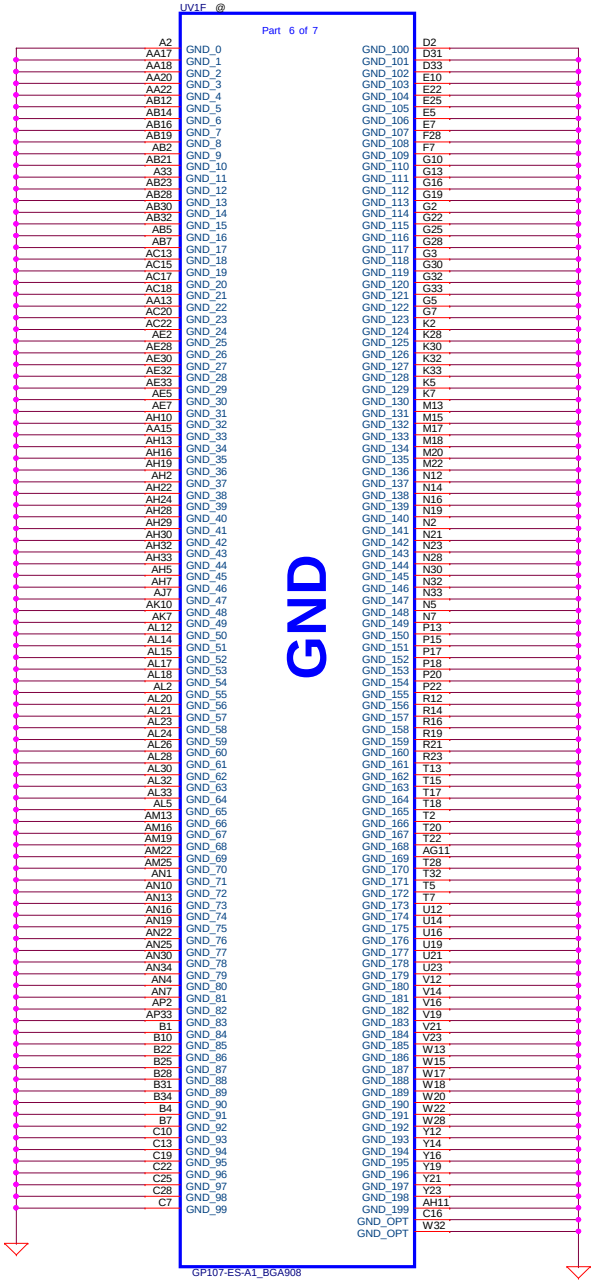
N17P VDDS
1uF*5/4.7uF*5 (under GPU)
330uF*1/22uF*3/10uF*2/4.7uF*2

VDD and VDDS merge design





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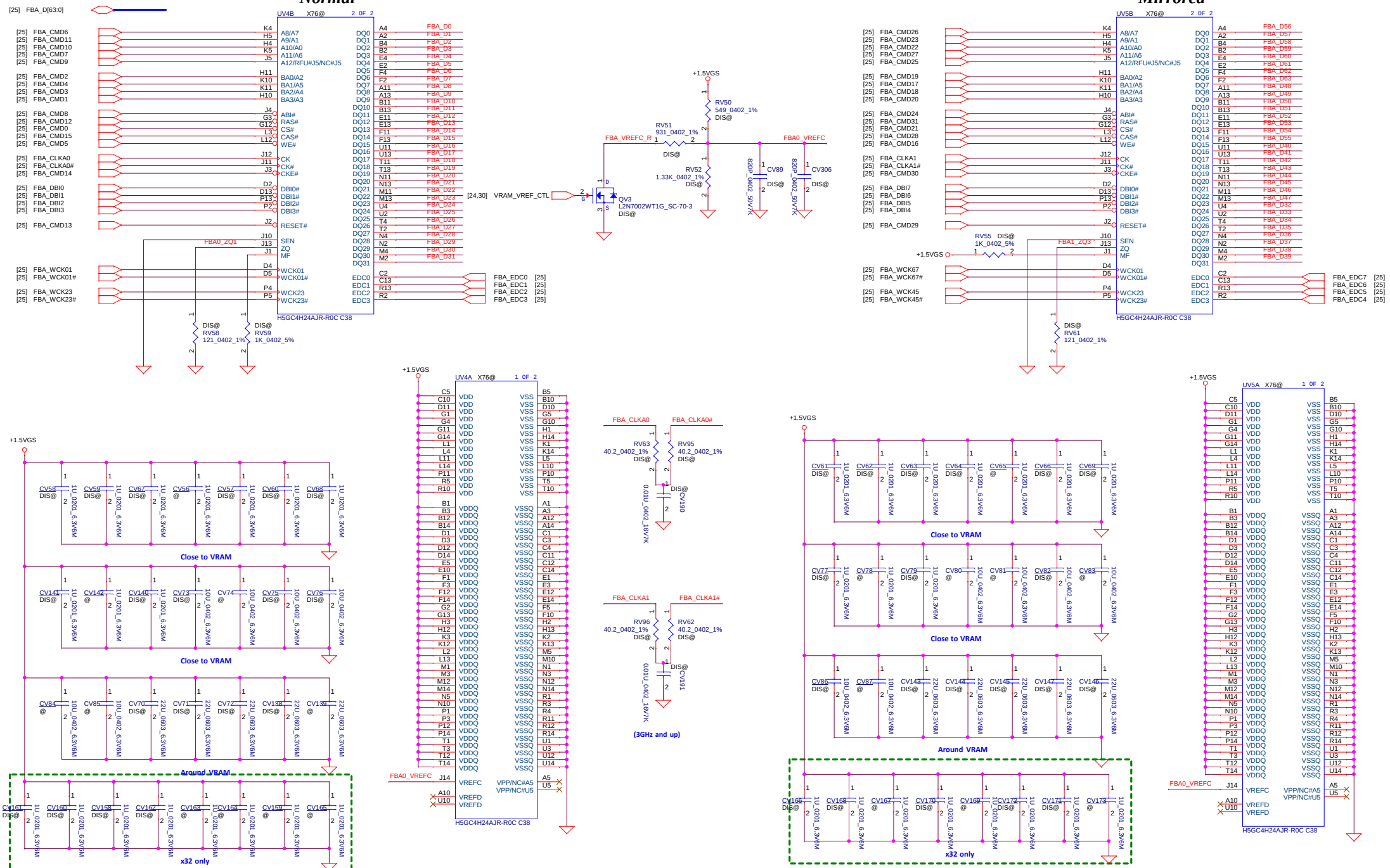

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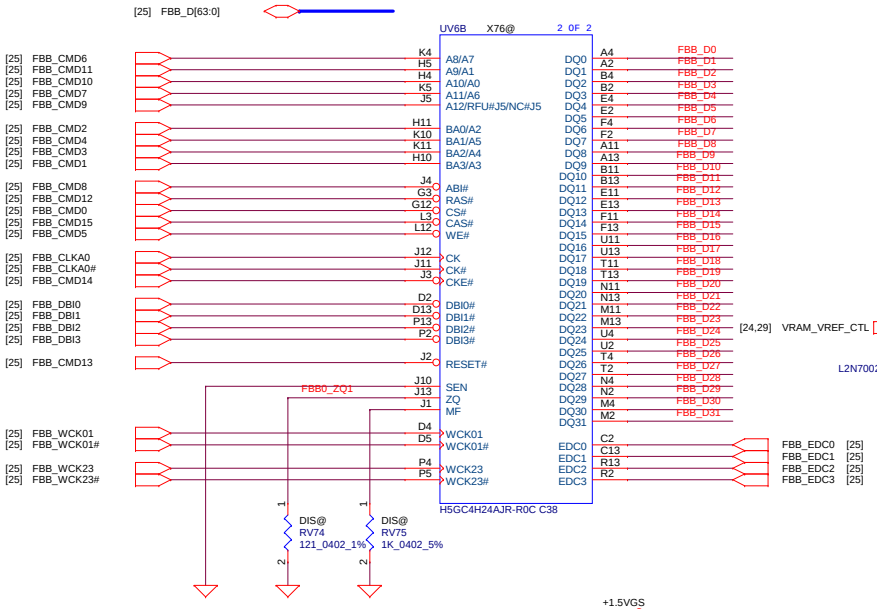

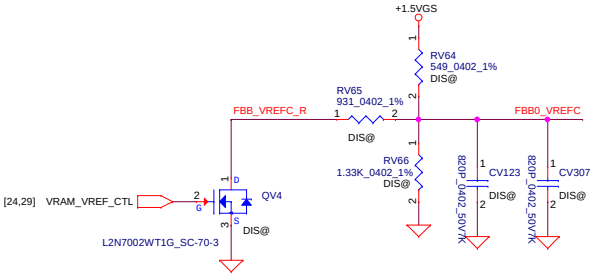

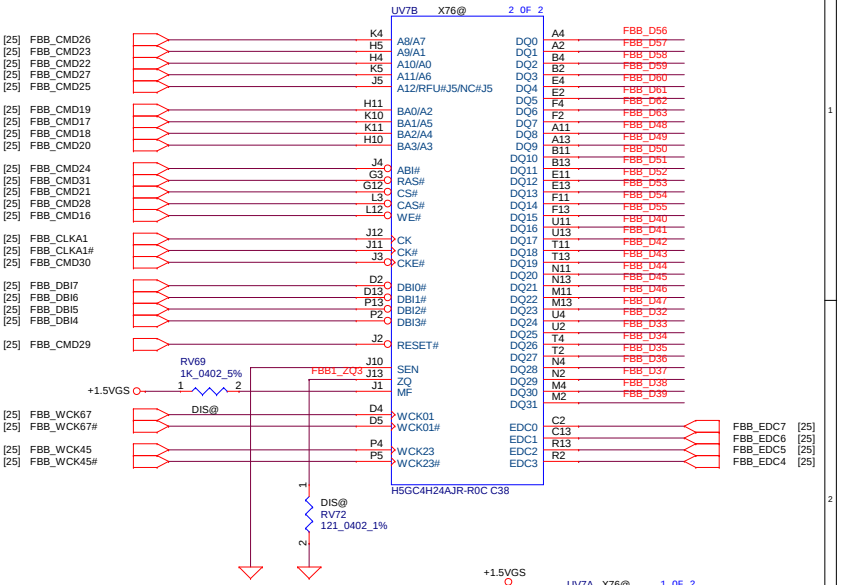

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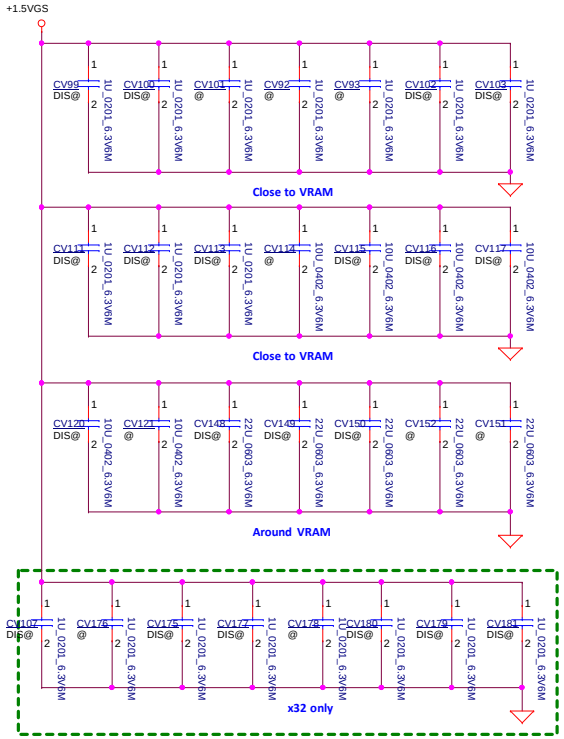

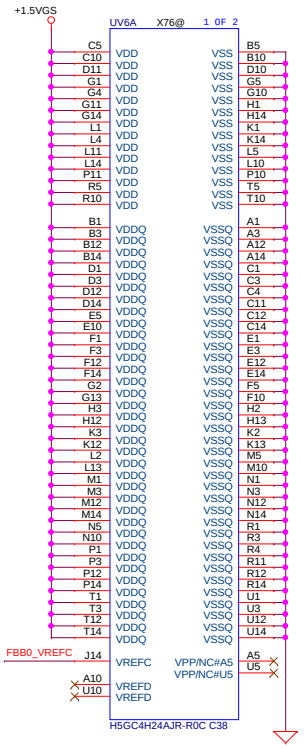

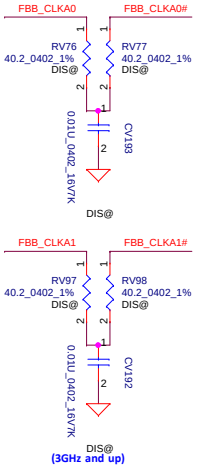

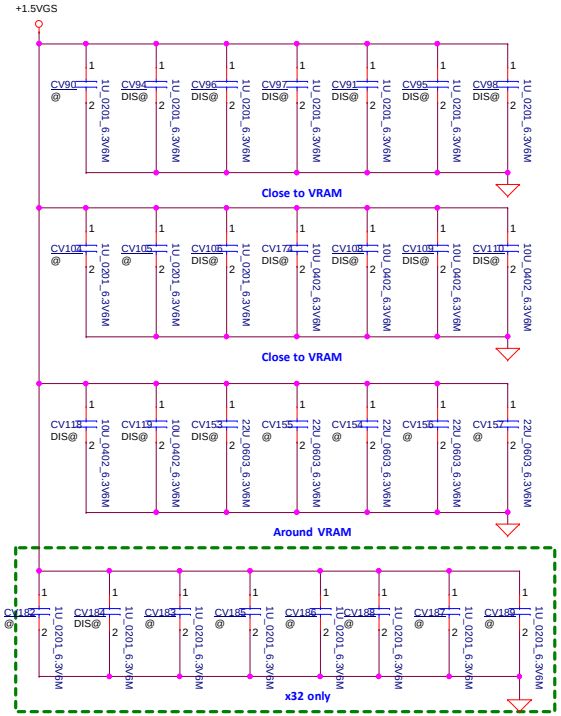

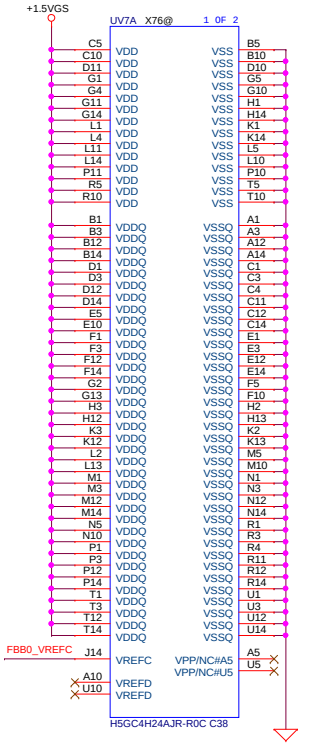

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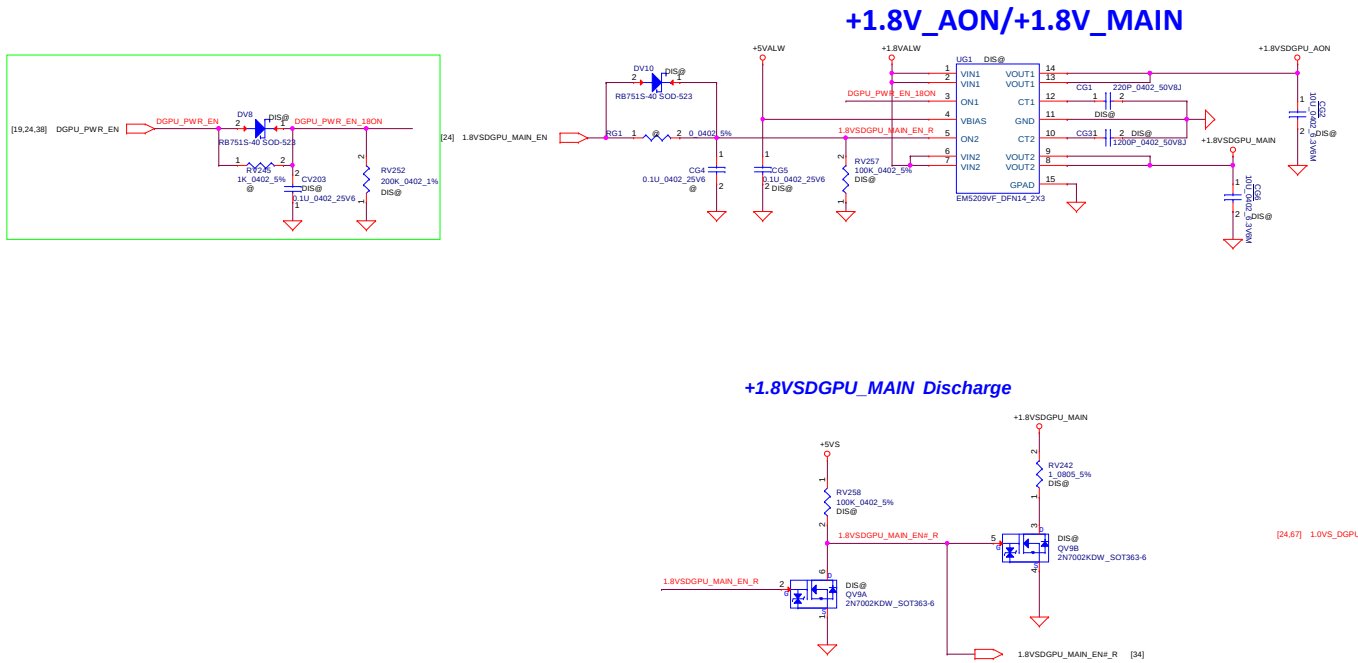

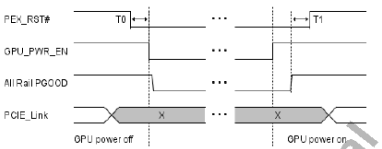

Figure 8.7 Optimus Entry/Exit Timing Diagram

Table 8.1 Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

7.3.2.1 Power-Up Sequence

The following power-up sequence is required:

1V8_AON → 1V8_MAIN → NVVDD → NVVDDS/ PEX_DVDD → FBVDD(Q)

- All GPU power rails must ramp up after 1V8_AON.
- FBVDD(Q) should ramp up after NVVDDS and PEX_DVDD.

All other 1.8V power rails can ramp up with 1V8_MAIN including PEX_HVDD and all PLLVDD rails; all other 1V power rails can ramp up with PEX_DVDD.

7.3.2.2 Power-Down Sequence

The following power-down sequence is required:

- NVVDDS/PEX_DVDD must ramp down before NVVDD, all other power rails can ramp down together with NVVDD;
- For GDDR5x, VPP must be equal to or higher than FBVDD/Q at all times, use gate logic and discharge circuit as needed.
- All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1.8V_AON and 1.8V_MAIN power down.
- The previous power rail must ramp down to 10% before the next power rail can start ramping down

Power Sequencing Requirement

GC6 2.1 requires the following power sequences. At GPU power up, first, the 1V8_MAIN power rails ramp up, followed by NVVDD_L,NVVDD_S then PEX_VDD and all other 1.0V power rails. And finally FBVDD/Q should power on. The following representation describes the required power sequencing for the GC6 2.1 system:

- Cold boot: Check Chapter :Power
- GC6 2.1 Exit: 1V8_MAIN > NVVDD_L>NVVDD_S > PEX_VDD or 1V8_MAIN > NVVDD_L > NVVDD_S & PEX_VDD

8.2.3 GC6 2.1 Entry/Exit Timing

The following timing diagram in Figure 8.15 and Table 8.2 describes the GC6 2.1 entry and exit sequence and timing requirements.

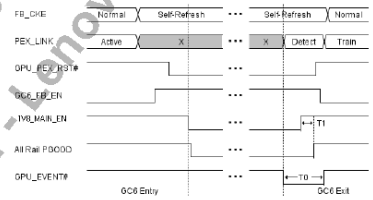

Figure 8.15 GC6 2.1 Entry/Exit Sequence Timing Diagram

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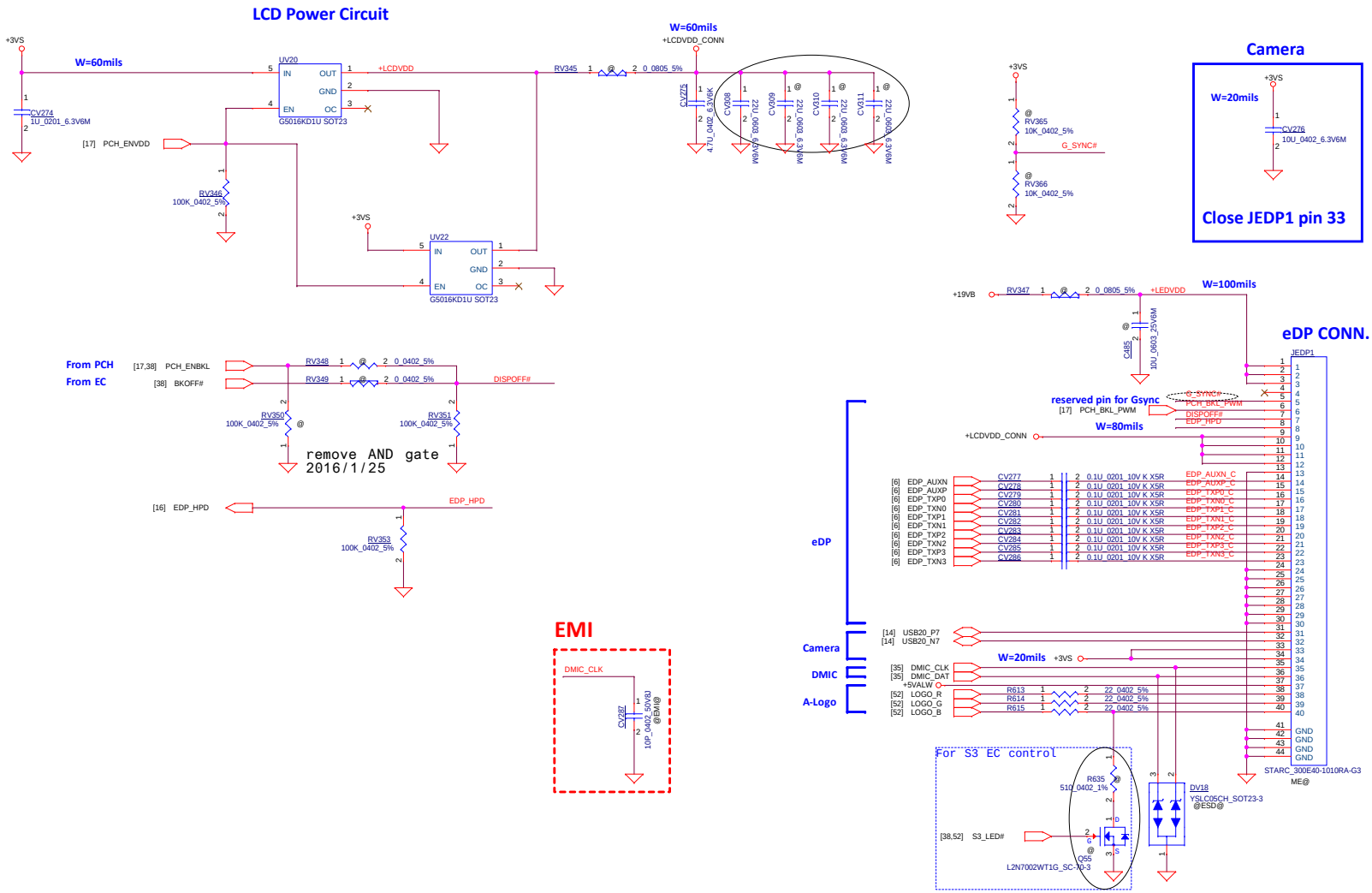

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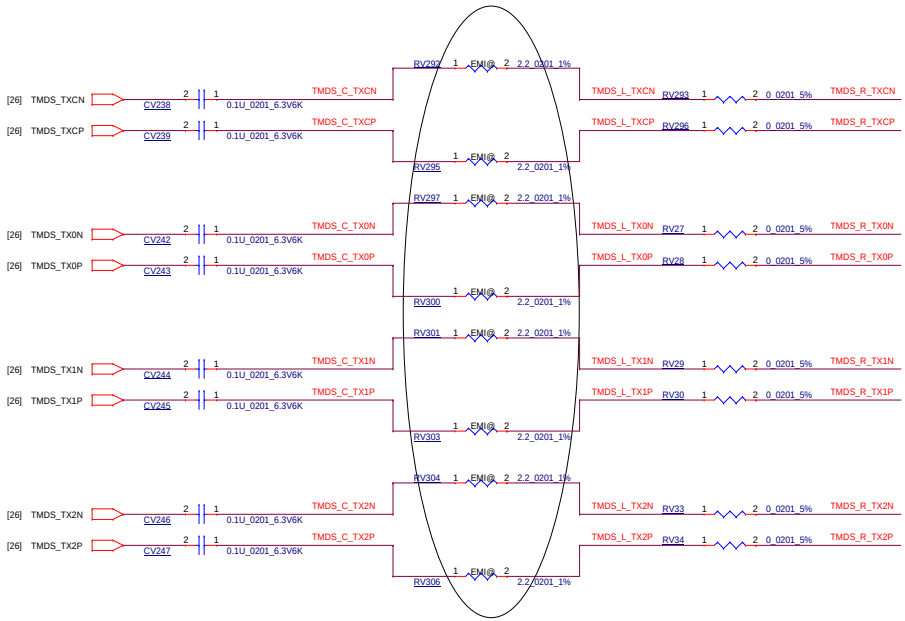
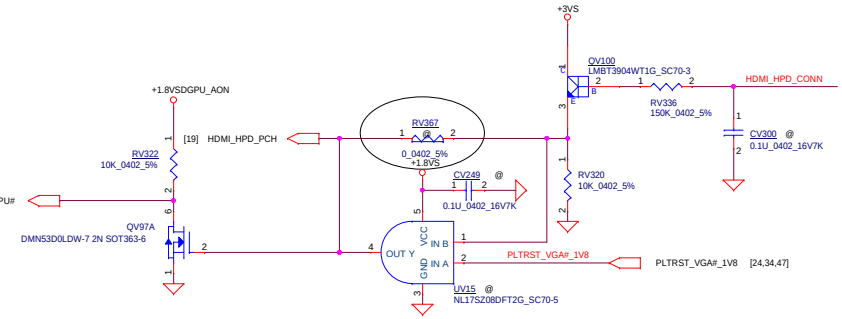
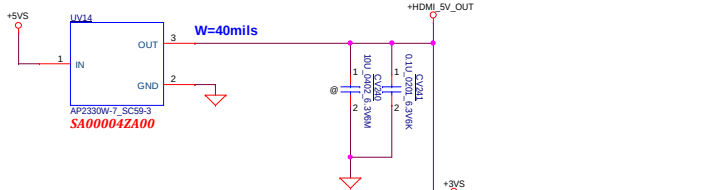
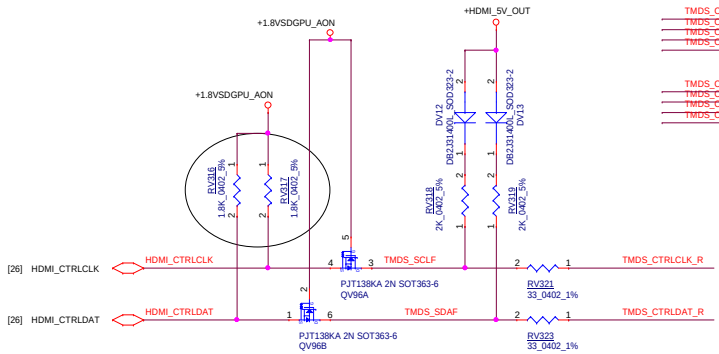
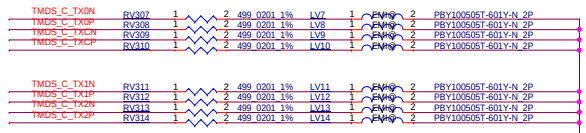


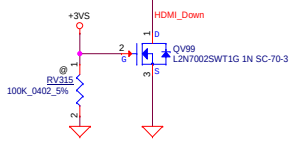


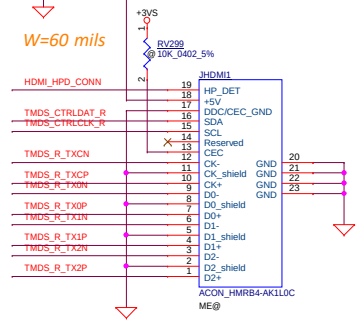




To GPU







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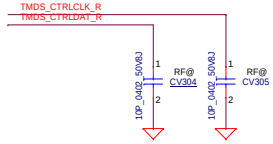

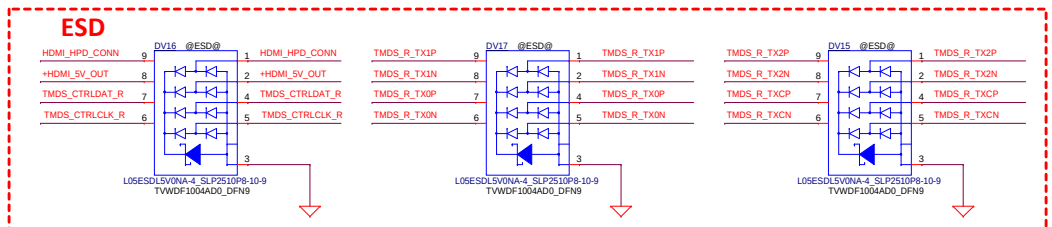

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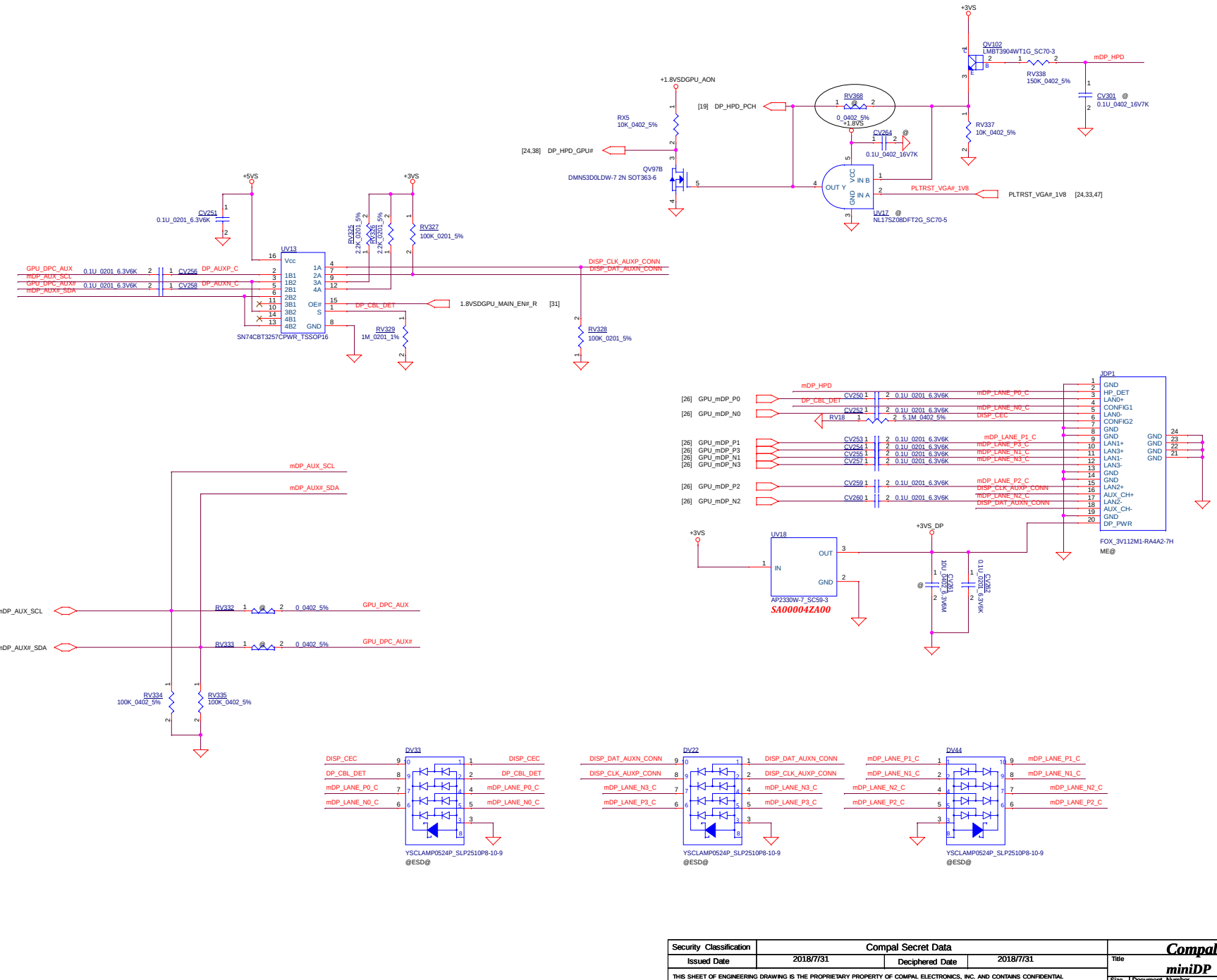

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Title: **miniDP**

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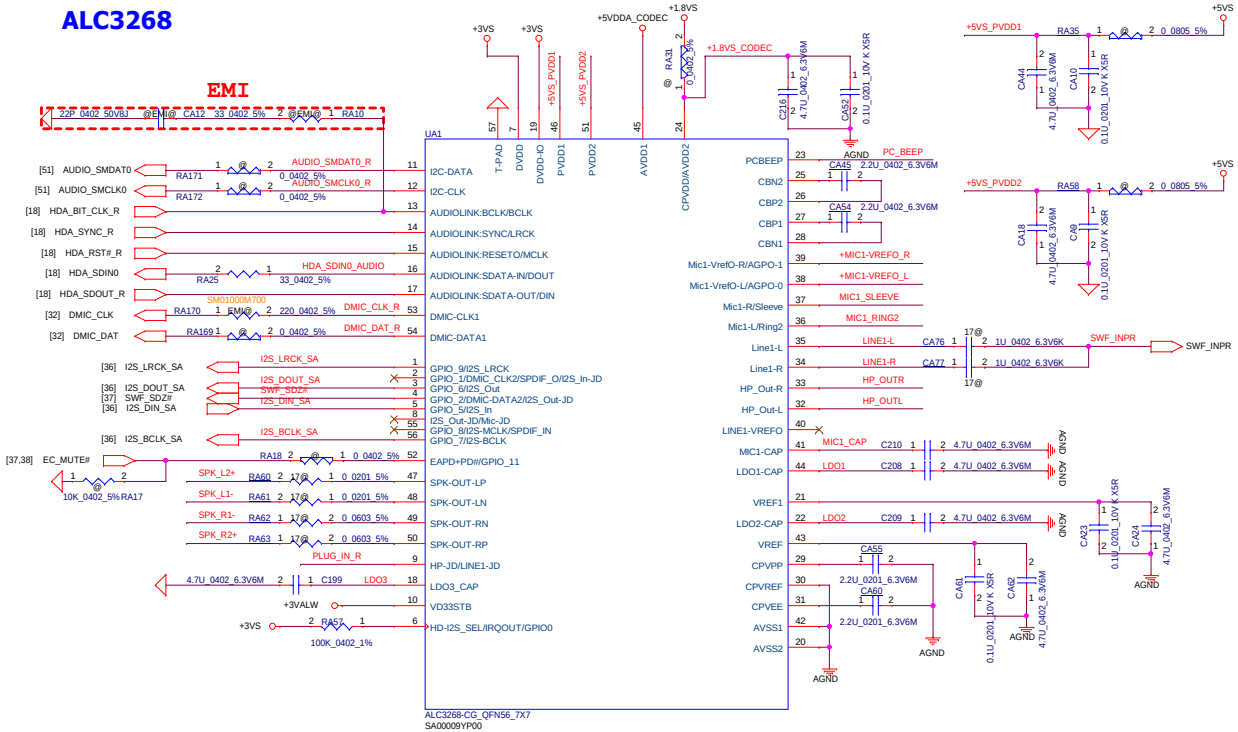

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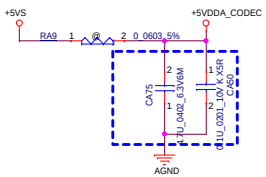

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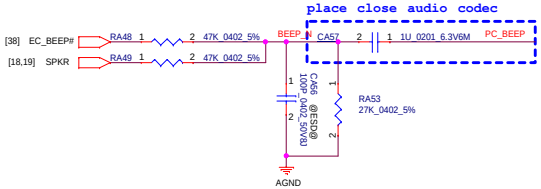

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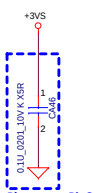
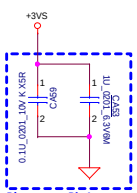
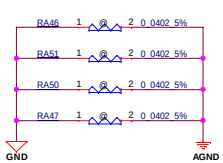


+3VS for +3VDD_CODEC



EMI



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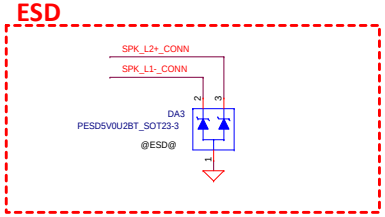
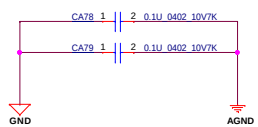
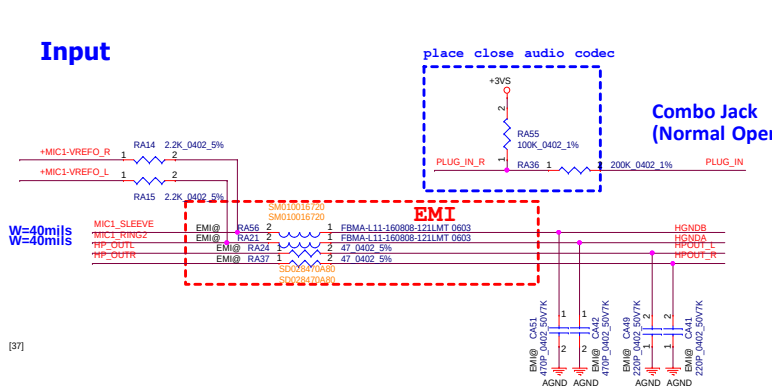
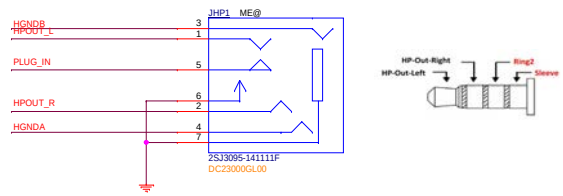
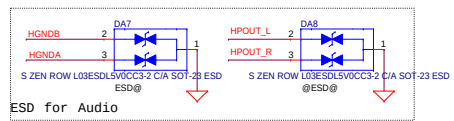


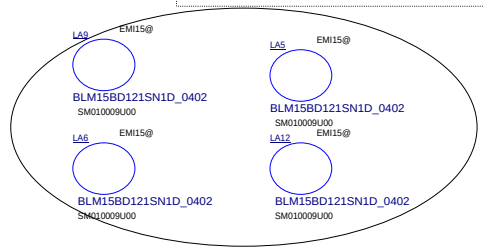


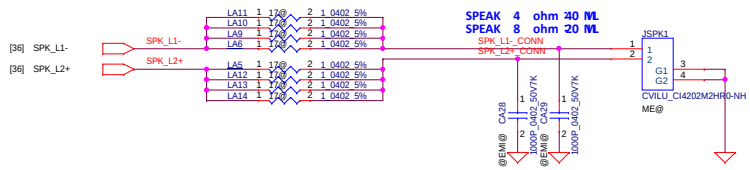
Input

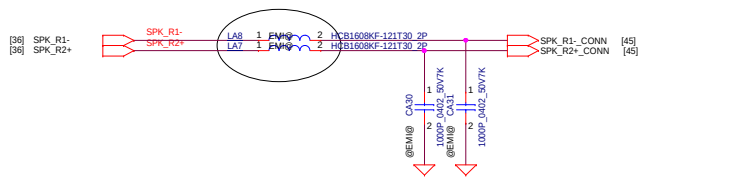












Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

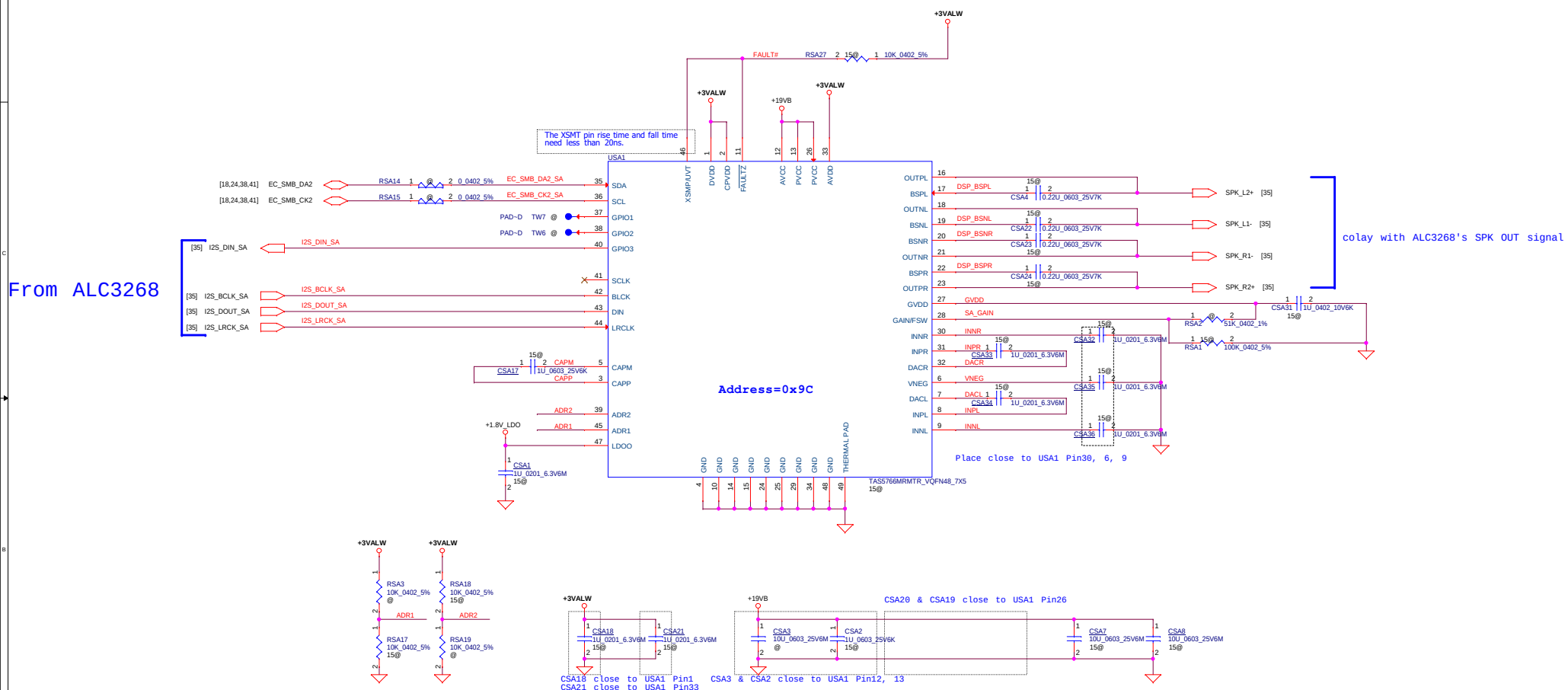
Compal Electronics, Inc.

Title: HD Audio Codec_ALC3268

Size	Document Number	Rev
C	LA-G131P	0.3

Date: Friday, July 06, 2018 | Sheet 35 of 68

TAS5766 Smart Amp for 15" only



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

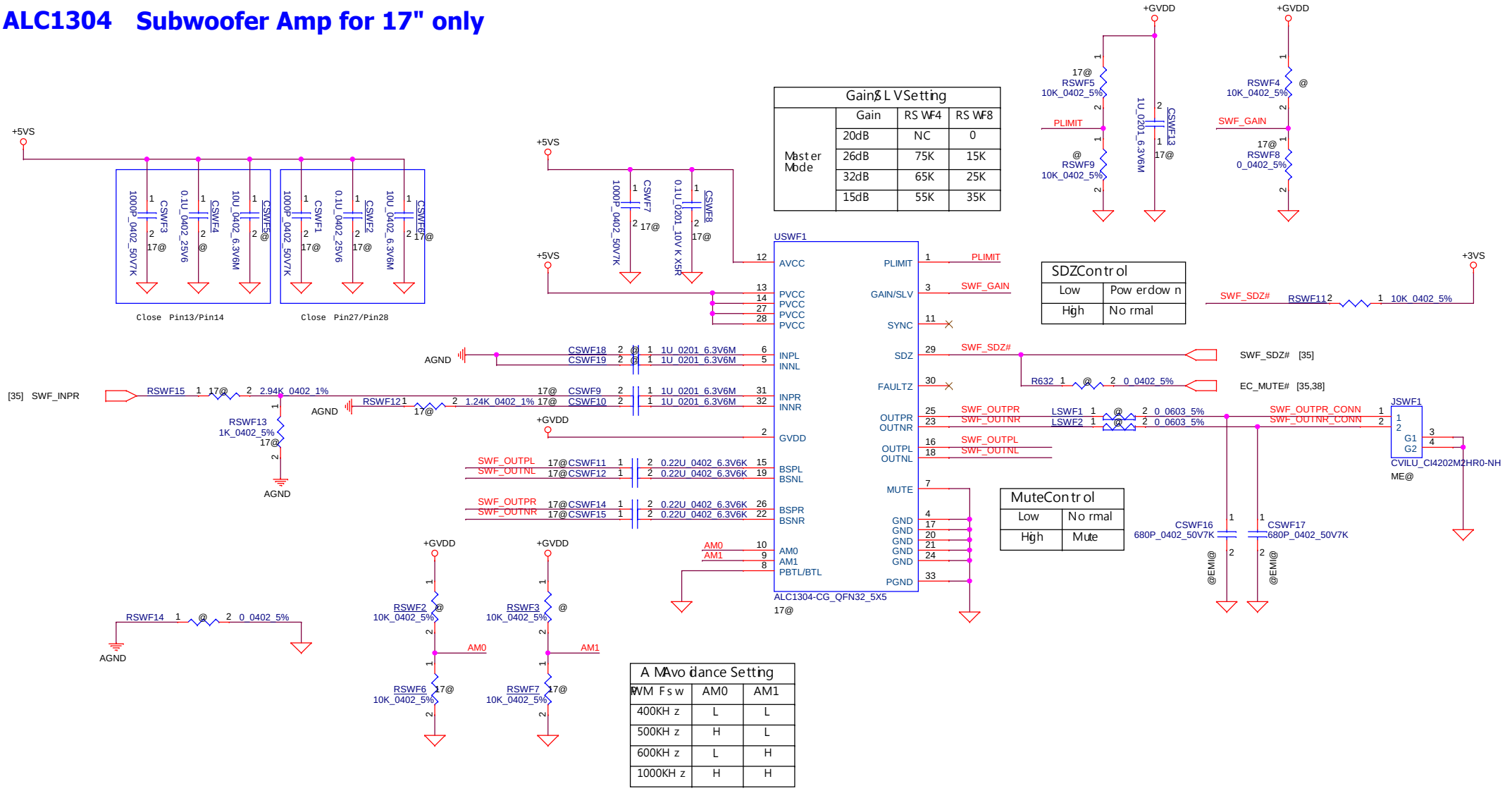
Compal Electronics, Inc.

Title: Smart Amp TAS5766

Size	Document Number	Rev
	LA-G131P	0.3

Date: Friday, July 06, 2018 Sheet 36 of 68

ALC1304 Subwoofer Amp for 17" only



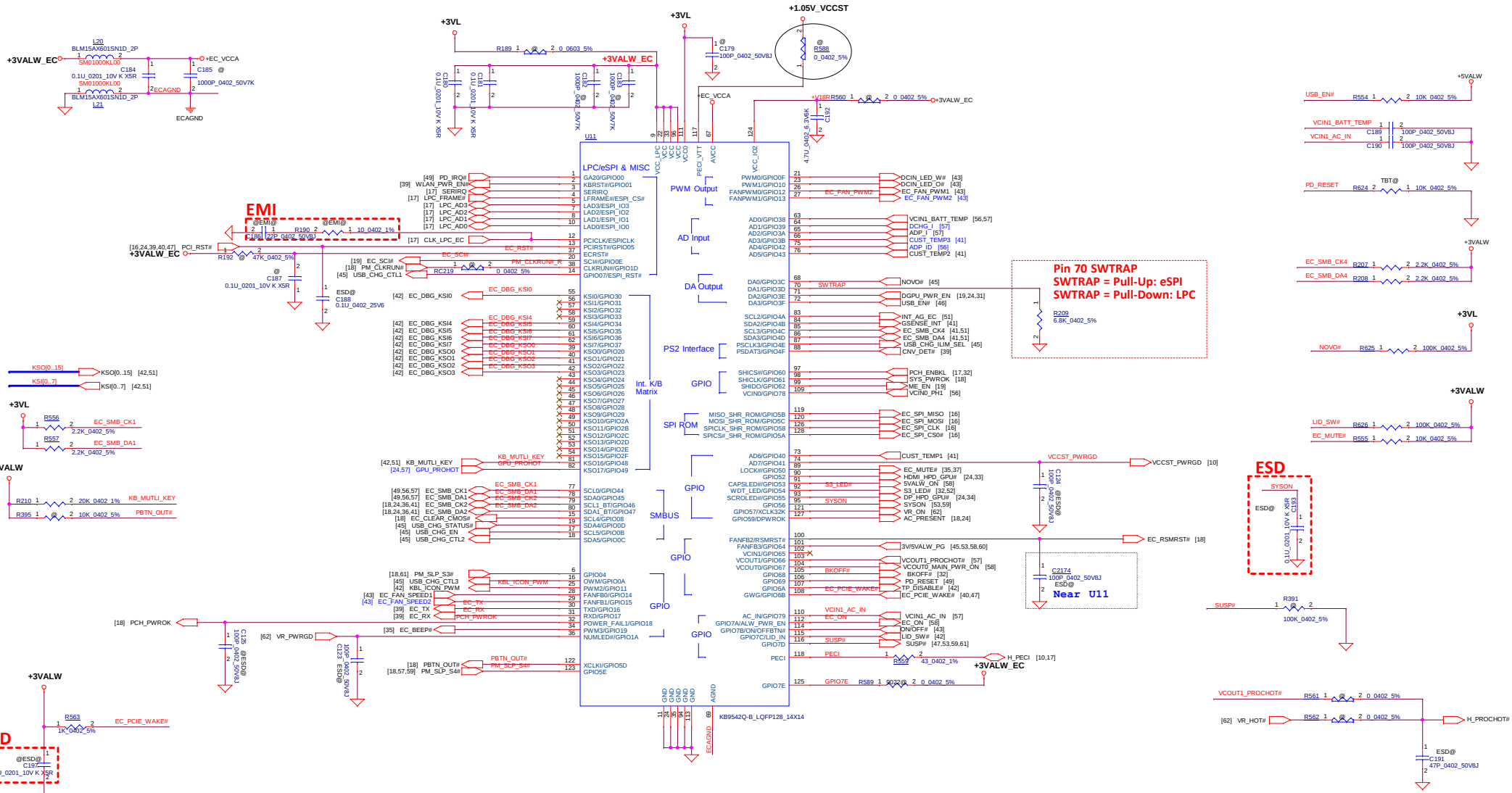
Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: **Subwoofer ALC1304**

Size	Document Number	Rev
	LA-G131P	0.3

Date: Friday, July 06, 2018 Sheet 37 of 68

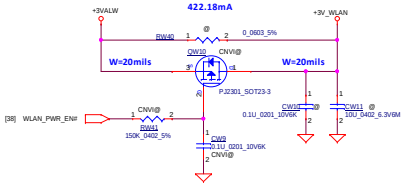


Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

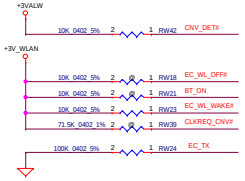
Compal Electronics, Inc.			
Title	EC KB9542Q		
Size	Document Number		Rev
Custom	LA-G131P		0.3
Date:	Friday, July 06, 2018	Sheet	38 of 68

NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]

For Power consumption Measurement

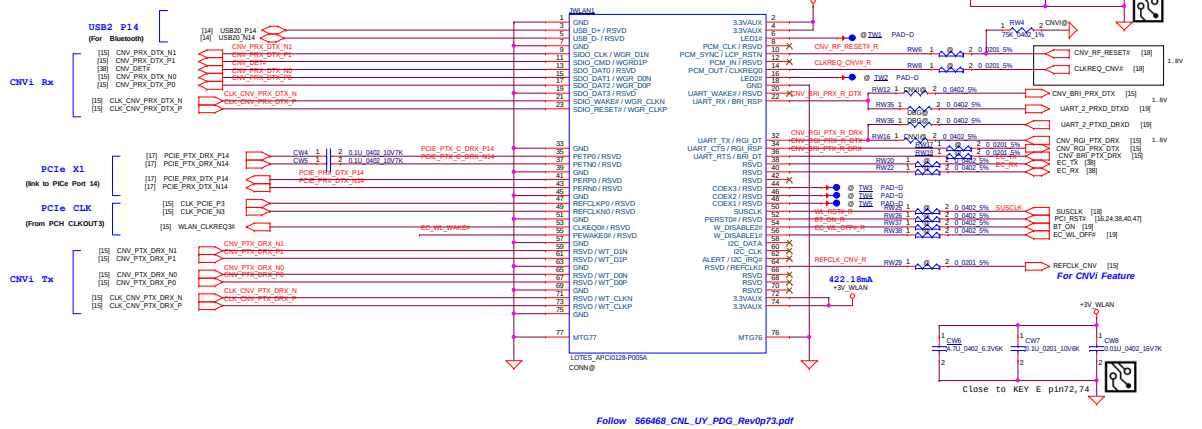


The connectivity module power supply pin shall be connected directly to thr rail DSW.
From 567240_Intel_Wireless_AC_9560_Jefferson_Peak_EPS_Rev1.1



Jefferson Peak:1360mA@peak current
Thunder_Peak_2:1100mA@peak current

KEY E



Follow 566468_CNL_UY_PDG_Rev0p73.pdf

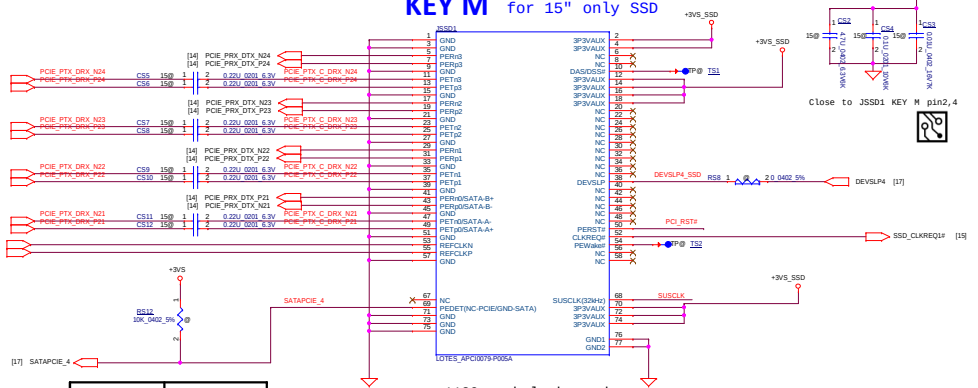
NGFF SSD1 (KEY M)

For Power consumption Measurement

PCIE X4
(link to PICE Port 17~20)

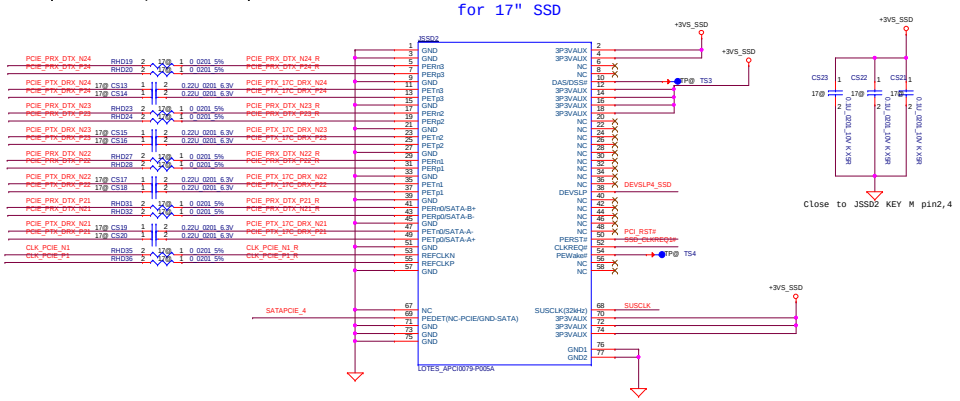
PCIE CLK
(From PCH CLKOUT1)

KEY M for 15" only SSD



PEDET	Module Type
0	SATA
1	PCIE

for 17" SSD



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.			
Title	WLAN(KEY E)/SSD(KEY M)		
Size	Document Number		Rev
	LA-G131P		0.3
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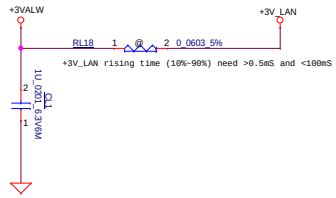
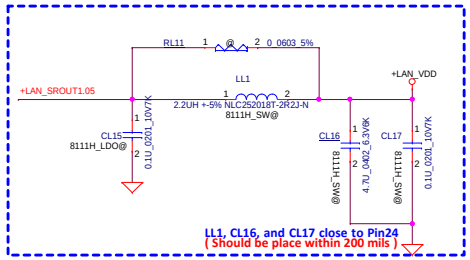
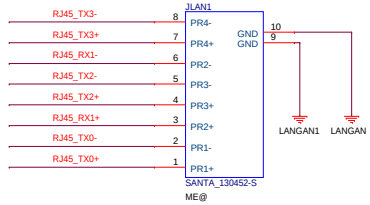
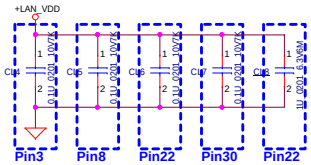
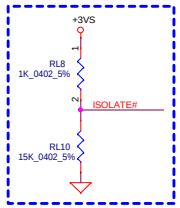
RJ-45 CONN.

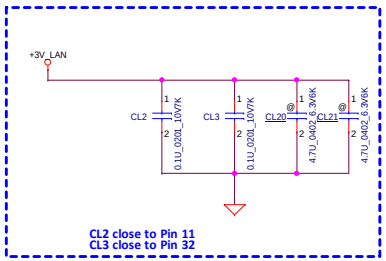


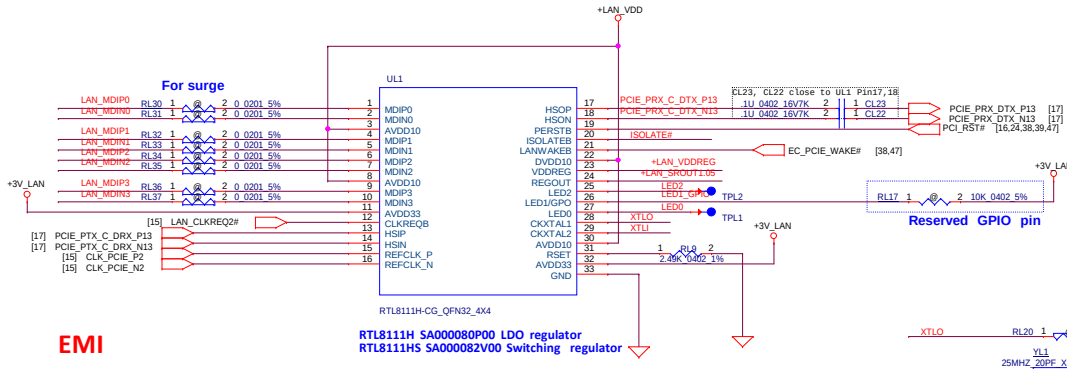


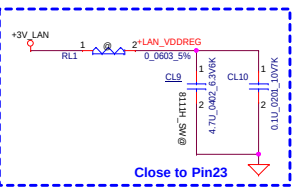


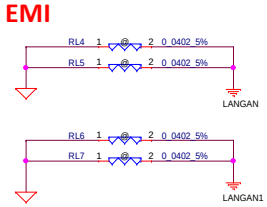


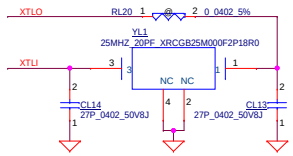


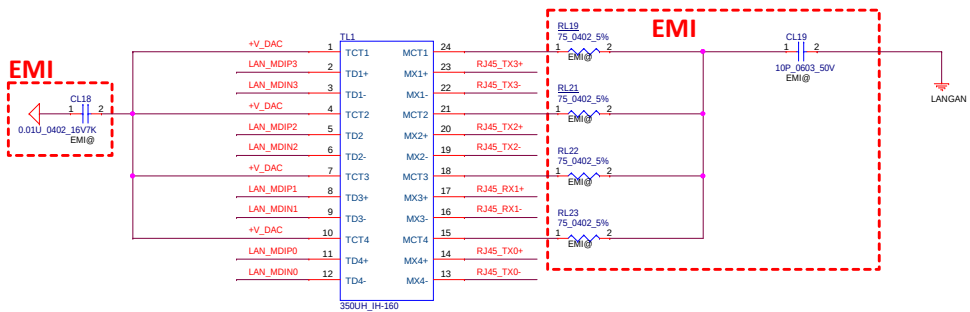


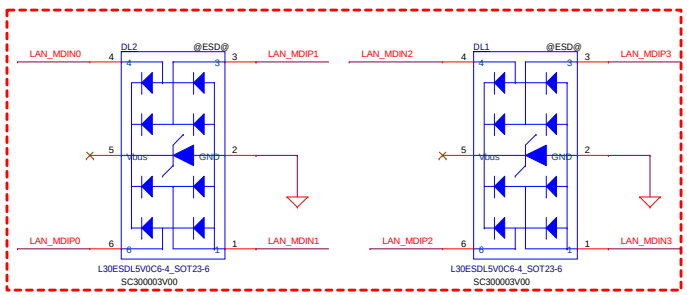












Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: LAN_RTL8111H/RTL8107E

Size	Document Number	Rev
C	LA-G131P	0.3

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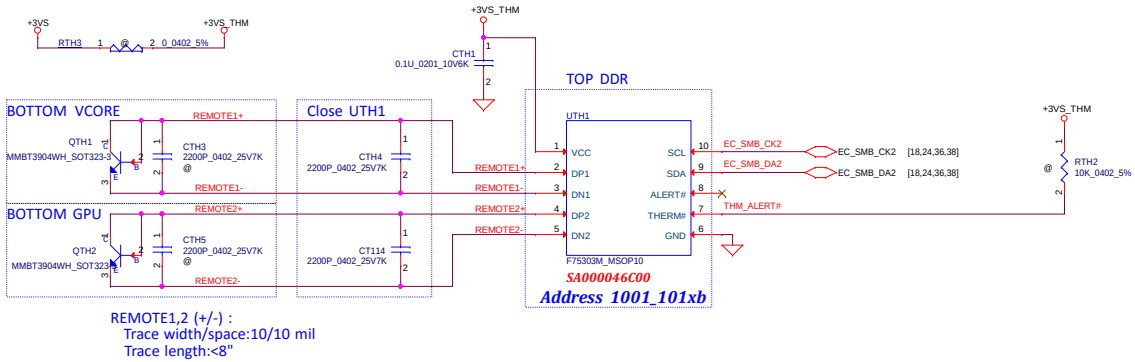
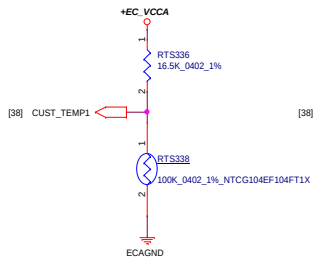
THERMAL SENSOR

For Smart Performance

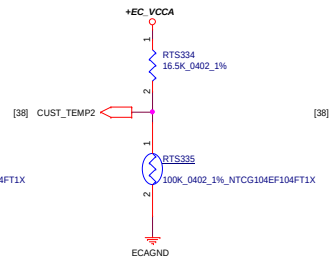


REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

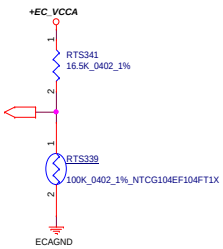
GPU Fan



CPU Fan



SSD



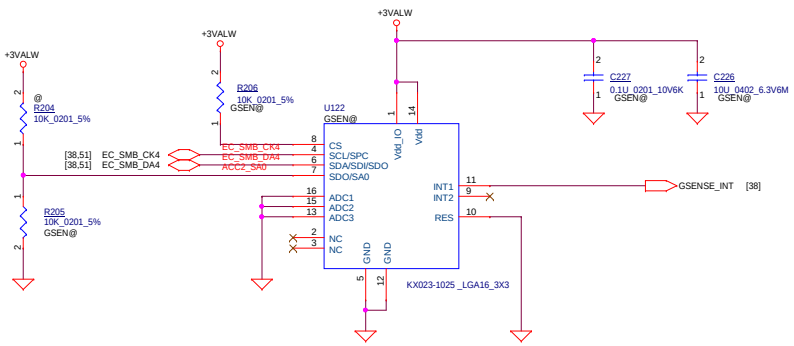
Intelligent Cooling G-Sensor

TABLE

ACC2_SA0	Address Selection
H	32h (W) & 33h (R)
L	30h (W) & 31h (R)

TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode



KX023-1025 Address: 0x1Eh

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: G-/THM Sensor

Size: C | Document Number: LA-G131P | Rev: 0.3

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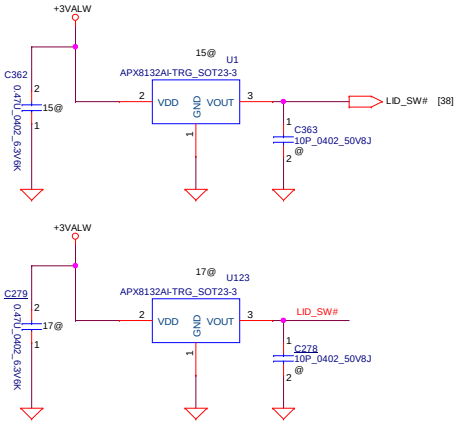
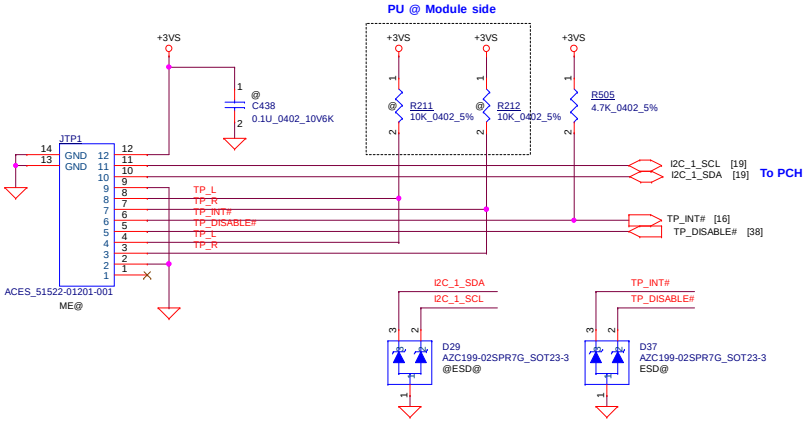
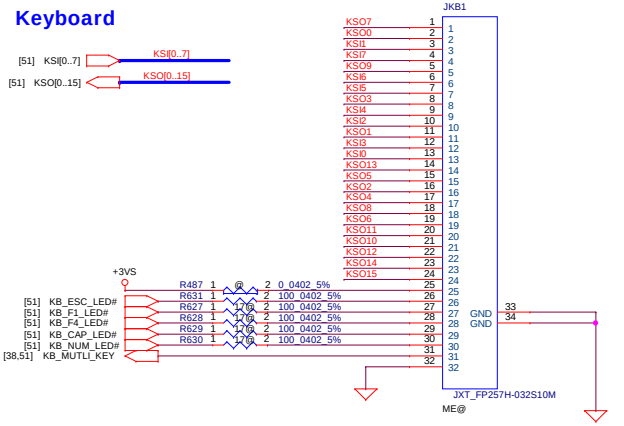
Lid Switch

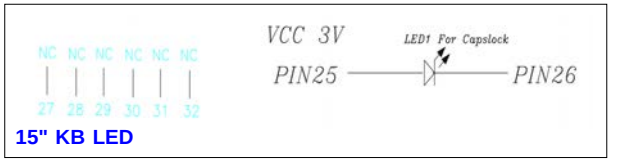


Touch Pad

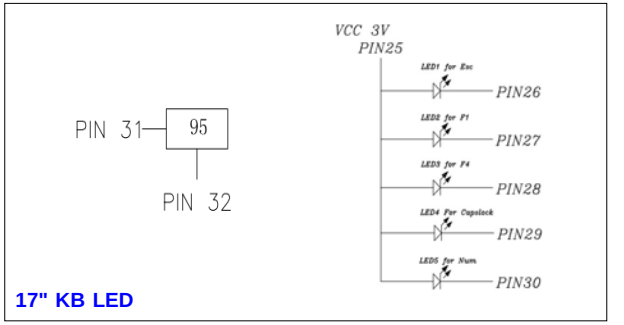


Keyboard





15" KB LED



17" KB LED

Bom Structure

VRAM 4G

ZZZ M4G@	ZZZ H4G@	ZZZ S4G@
VRAM	VRAM	VRAM
MT51J256M32HF-70:A	H5GC8H24MJR-R0C	K4G80325FB-HC28
X7678038L01	X7678038L02	X7678038L03

Nvidia GPU SKU

UV1 GPU1@	UV1 GPU2@
1050Ti-R1	1050Ti-R3
N17P-G1-A1	N17P-G1-A1
SA0000A0600	SA0000A0680

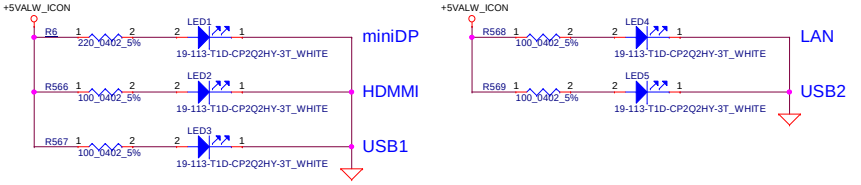
Coffee Lake-H CPU SKU

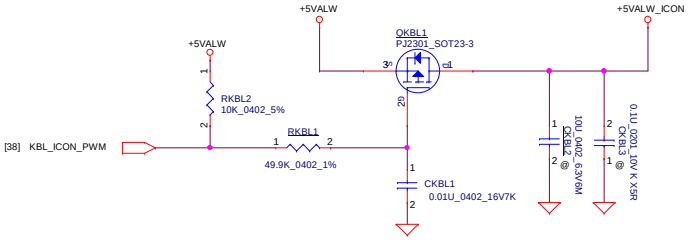
UC1 CPU1@	UC1 CPU3@	UC1 CPU5@
MP-R1	QS	MP-R3
CFL-H_i5-8300H	CFL-H_i5-8300H	CFL-H_i5-8300H
SA0000BPJ20	SA0000BPJ10	SA0000BPJ60
UC1 CPU2@	UC1 CPU4@	UC1 CPU6@
MP-R1	QS	MP-R3
CFL-H_i7-8750H	CFL-H_i7-8750H	CFL-H_i7-8750H
SA0000BPZ20	SA0000BPZ10	SA0000BPZ60

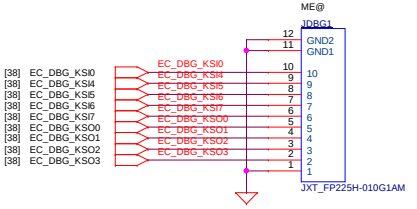
Cannn Lake PCH HM370

UH1 PCH1@	UH1 PCH2@	UH1 PCH3@
MP-R1	QS	MP-R3
HM370 SR40B	HM370 QNYF	HM370 SR40B
SA0000BVP00	SA0000BPF10	SA0000BVP30

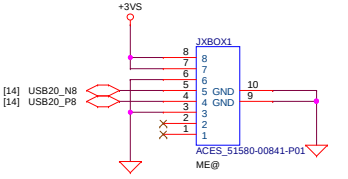
Icon LED







XBOX Module connector



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: KB/TP/LID/XBOX/BOM S.

Size	Document Number	Rev
	LA-G131P	0.3

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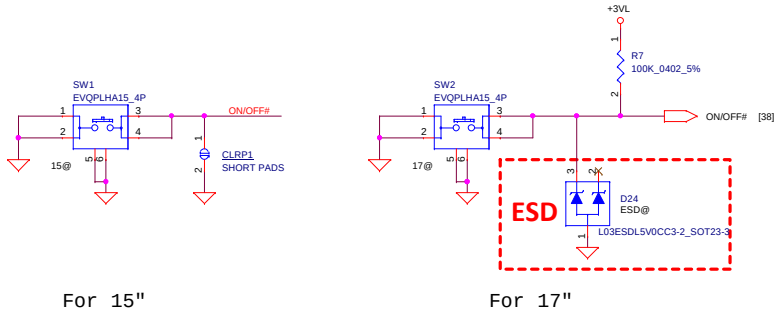
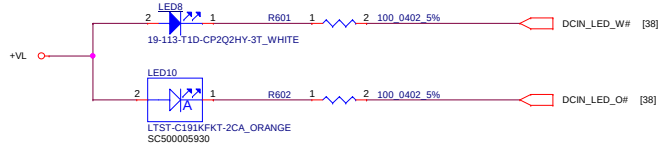
Power BTN

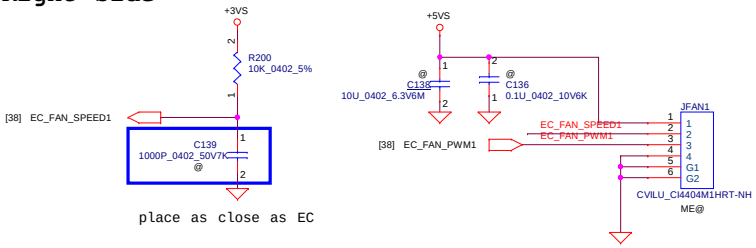


DCIN LED



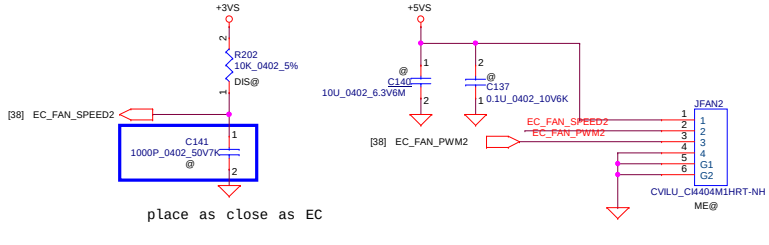
CPU Fan Control Circuit

Right Side



GPU Fan Control Circuit

Left Side



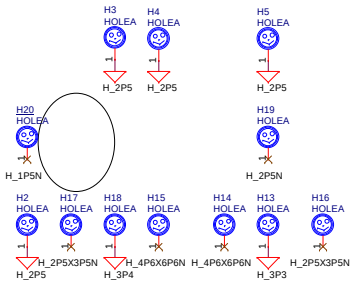
PCB

ZZZ

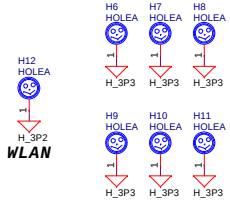
LA-G131P

DAZ2BX00100

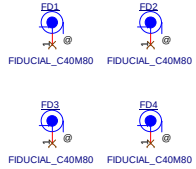
Screw Hole



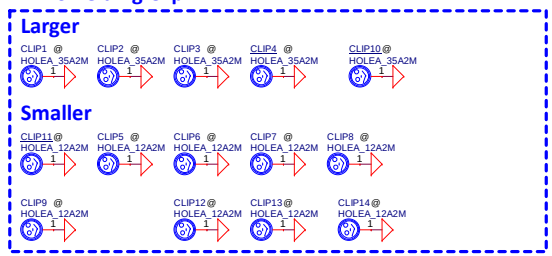
CPU/GPU Thermal Standoff



Fiducial Mark



DDR Shielding Clip



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

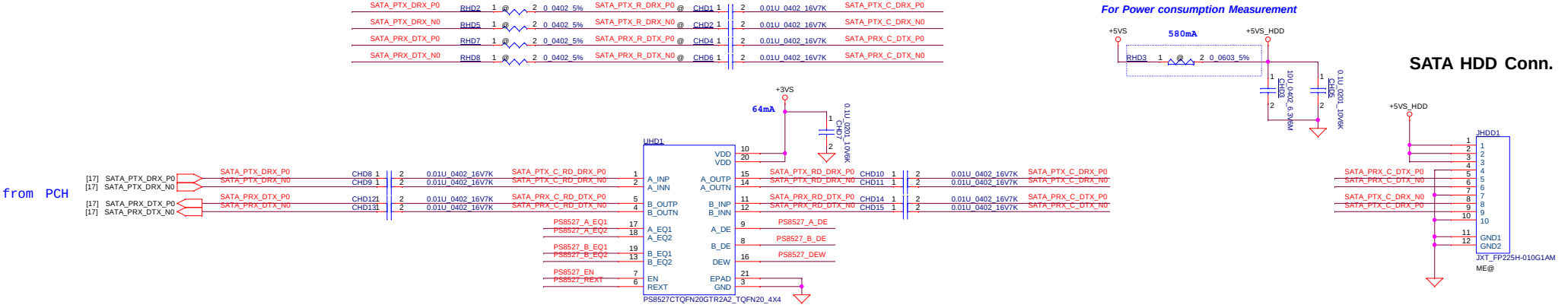
Compal Electronics, Inc.

Title: FAN/LED/PBTN/PCB PN/SCREWS

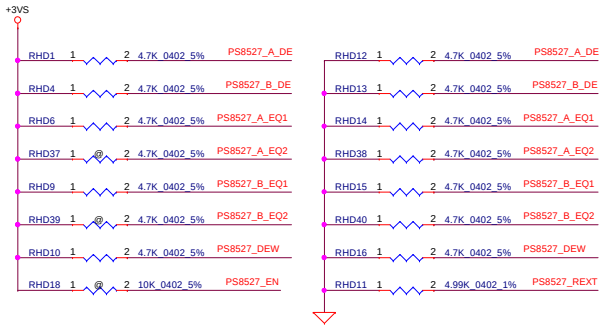
Size | Document Number: LA-G131P | Rev: 0.3

Date: Friday, July 06, 2018 | Sheet 43 of 68

SATA HDD



PN:SA00007JU10



Equalizer control and program for channel A.

Internally tied to VDD/2 (M status).

A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Equalizer control and program for channel B.

Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Programmable output de-emphasis level setting for channel A.

Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.

Internally tied to VDD/2(M status).

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

De-emphasis width setting for channel A& B .

Internally tied to VDD/2(M status).

DEW	DE pulse duration optimized for
M	SATA 6Gbp/s(default)
L	SATA 6Gbp/s
H	SATA 3Gbp/s

Compal Electronics, Inc.

Title: HDD Connector

Size: | Document Number: LA-G131P | Rev: 0.3

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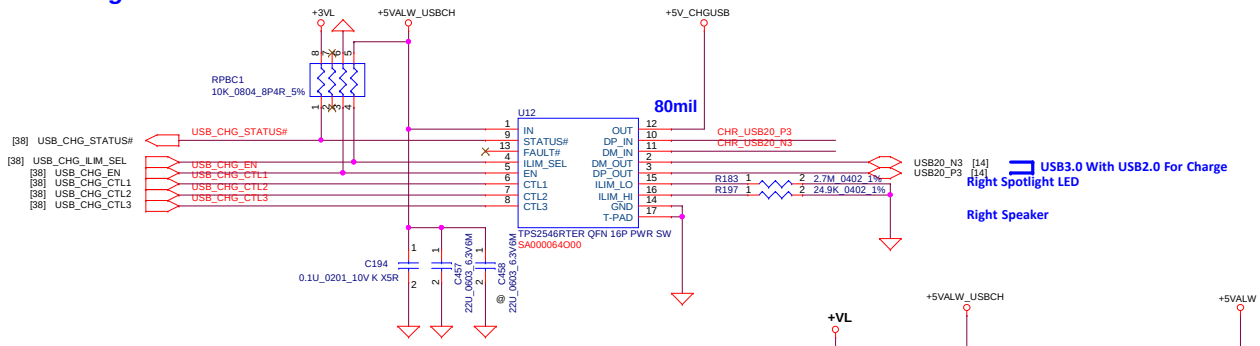
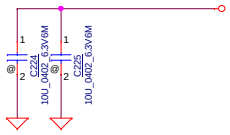
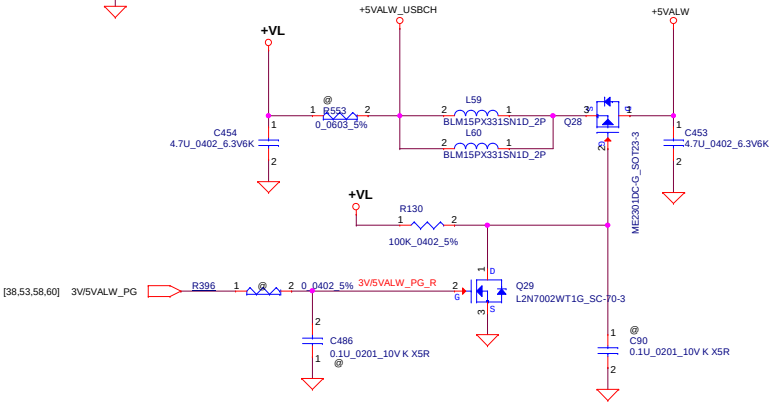
USB Charger from YOGA730 15

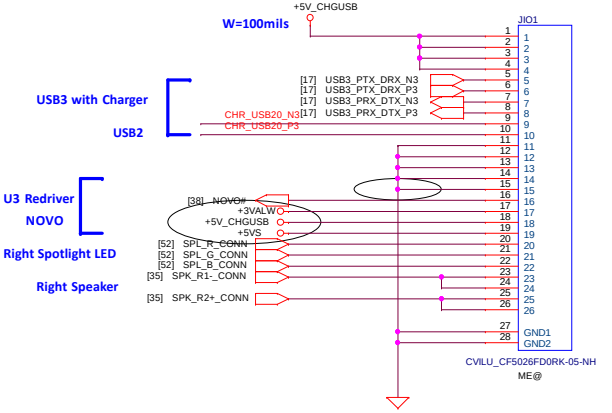


Down USB charger Iout ripple
must under 20mA on DC S5





IO CONN



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: **USB3_Port 3 CONN.**

Size	Document Number	Rev
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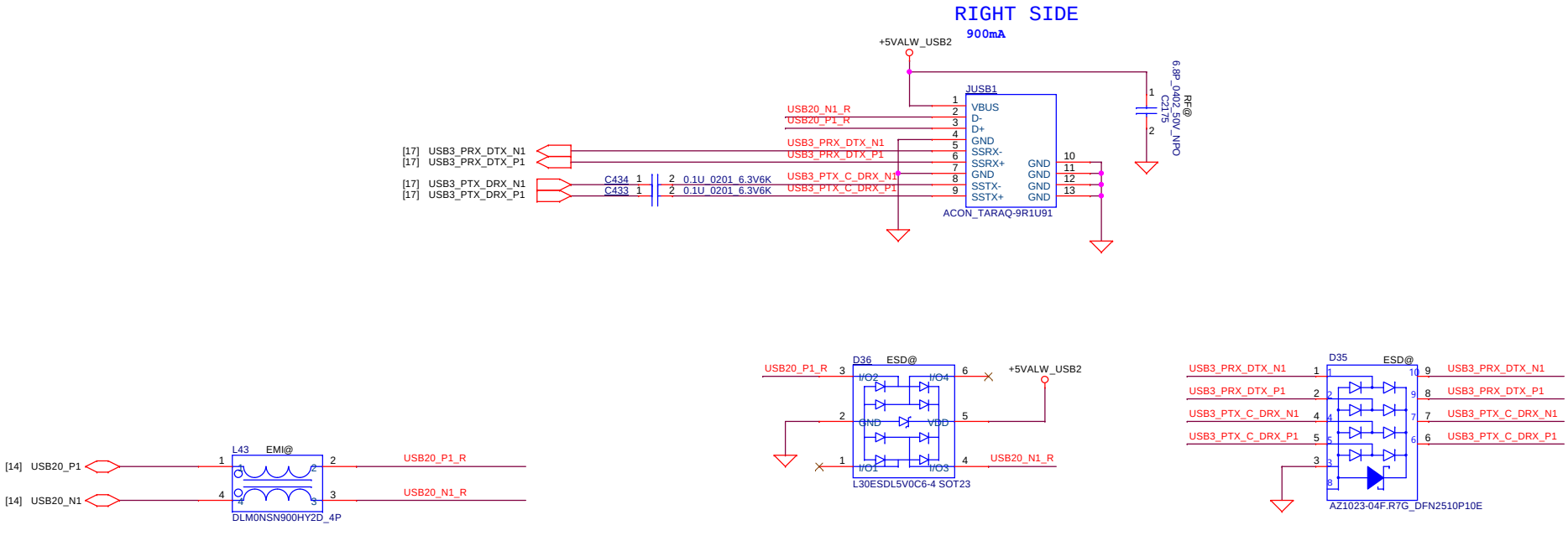
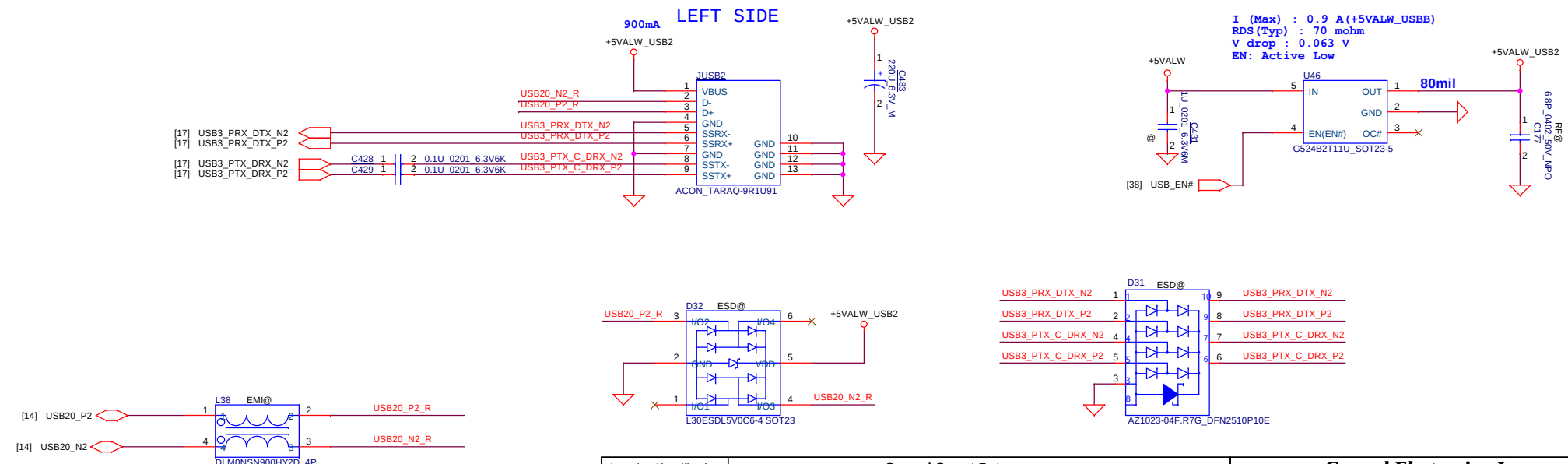
MB_USB3.1 Conn. (Port 1)



MB_USB3.1 Conn. (Port 2)



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: **USB3 Port1/2 Conn.**

Size	Document Number	Rev
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Titan Ridge SP - High Speed (CIO, USB and PCIe) Parts

Polarity Reversal is allowed on CIO/USB/DP domains.
Need to be configured on NVM.

In case of unused high speed interface,
please leave pins open. No need for termination.

TR DP Configuration:
CIO x2 ports may be used
PCIe x4 lanes may be used
DPSNK x8 lanes may be used
USB 3.1 may be used (for debug only)
DPSRC may be used

From PCH PCIe TX

To SoC PCIe RX

From GPU DDI

Follow TR_DP_TI_PD_HOST_REF_DESIGN_R0V95
PE isn't POR -
Please don't use

Place as close as possible to pins

USB2 Rbias Place as close as possible to pins

PCIE RBIAS
Place as close as possible to pins

TBT_GPIO_8
'0' - Unsecure mode
'1' - Secure mode

DG_FORCE_PWR:
'0' - Regular Mode, Force Power is disabled (Default)
'1' - Force Power Mode is enabled

DG_USB_FORCE_PWR:
Might be use for seperatly force USB domain - connect to EC/PCH
'0' - by default

DG_FORCE_PWR:
Connect to EC/PCH for FW update
'0' - by default
'1' - for debug only

DG_CIO_PLUG_EVENT# should be conncted to PCH SCI GPIO

JTAG

SPI ROM

25M XTAL

Must use Metal shielded crystal for better noise immunity.
(Recommended: FL2500123Z by Pericom)

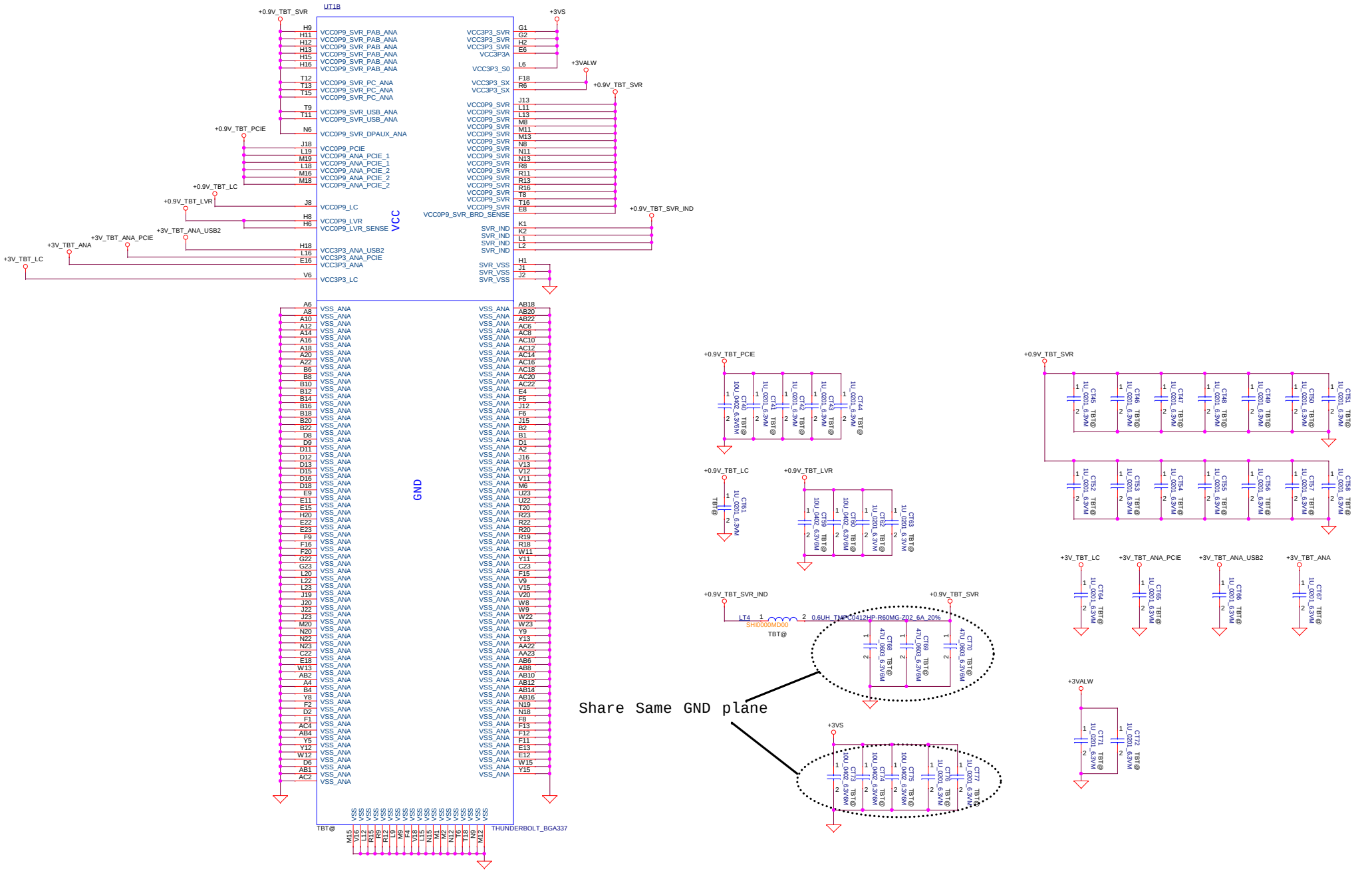
Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: Thunderbolt Titanrid (1/2)

Size: Custom | Document Number: LA-G131P | Rev: 0.3

Date: Friday, July 06, 2018 | Sheet 47 of 68



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Title	Compal Electronics, Inc.		
	Thunderbolt Titanrid (2/2)		
Size	Document Number		Rev
Custom	LA-G131P		0.3
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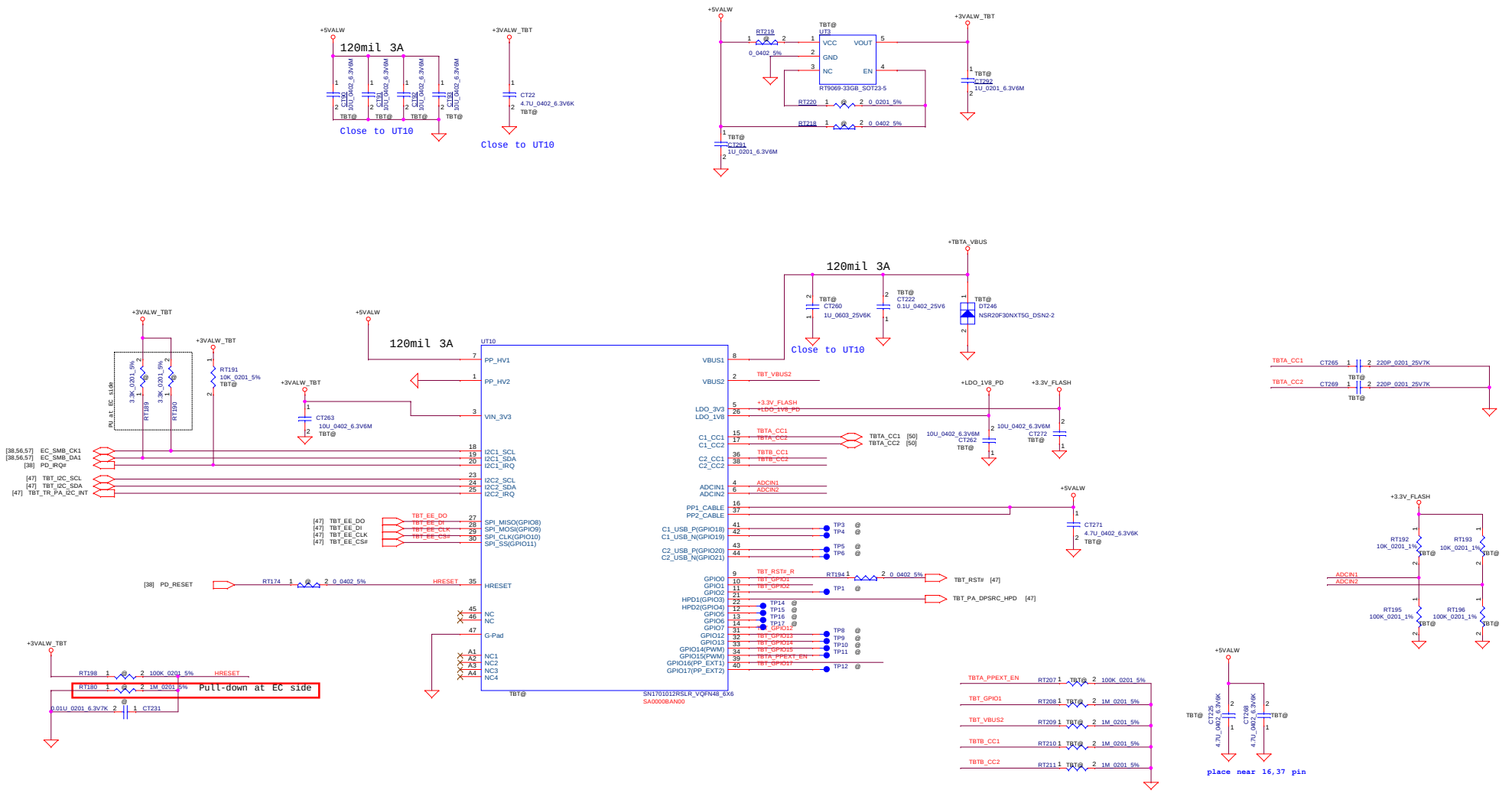

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: CC_TPS65988

Size	Document Number	Rev
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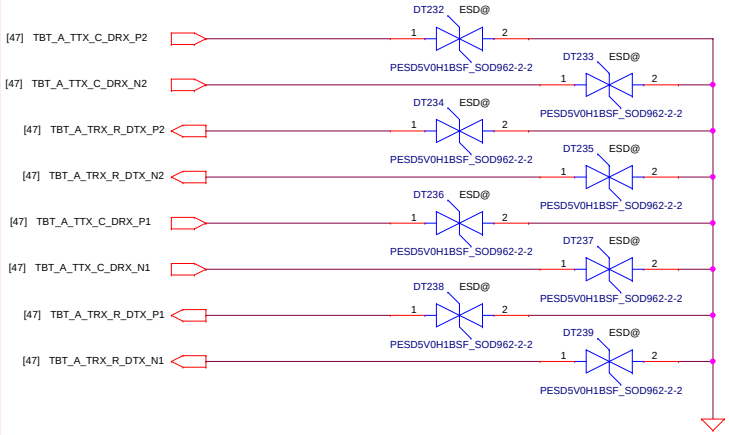
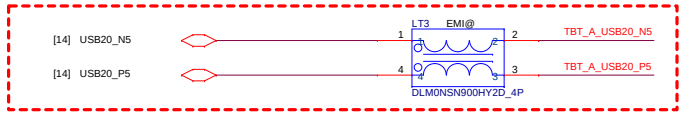
Main source:SC40000AT00
Foorprint: ESD8011MUT5G_X3DFN2-2(SC40000AR00 Footprint)

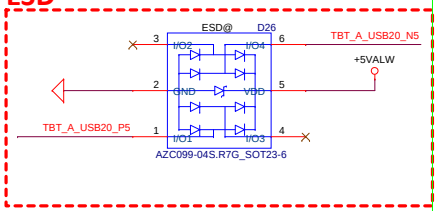




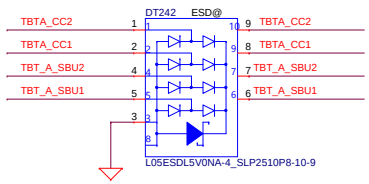
EMI

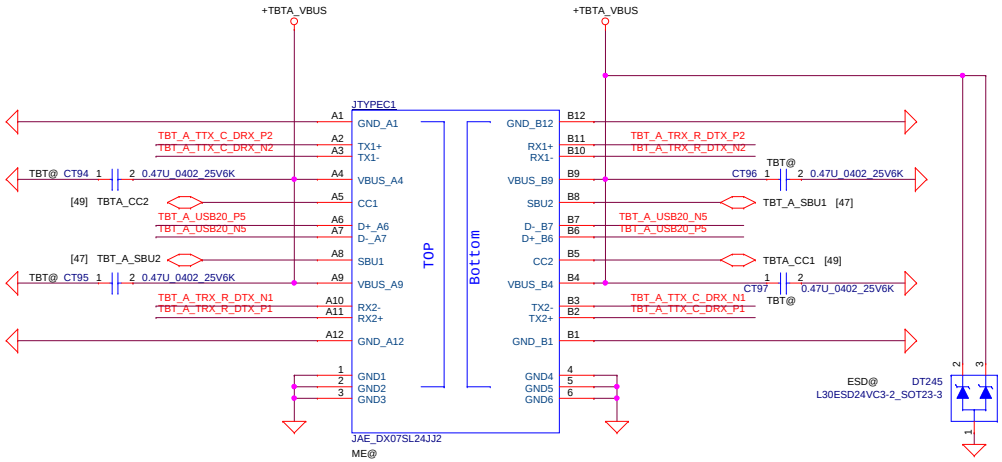
different from USB3.0 port's ESD

ESD



ESD Diode for CC1 CC2





Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: USB3.1 TypeC Conn

Size	Document Number	Rev
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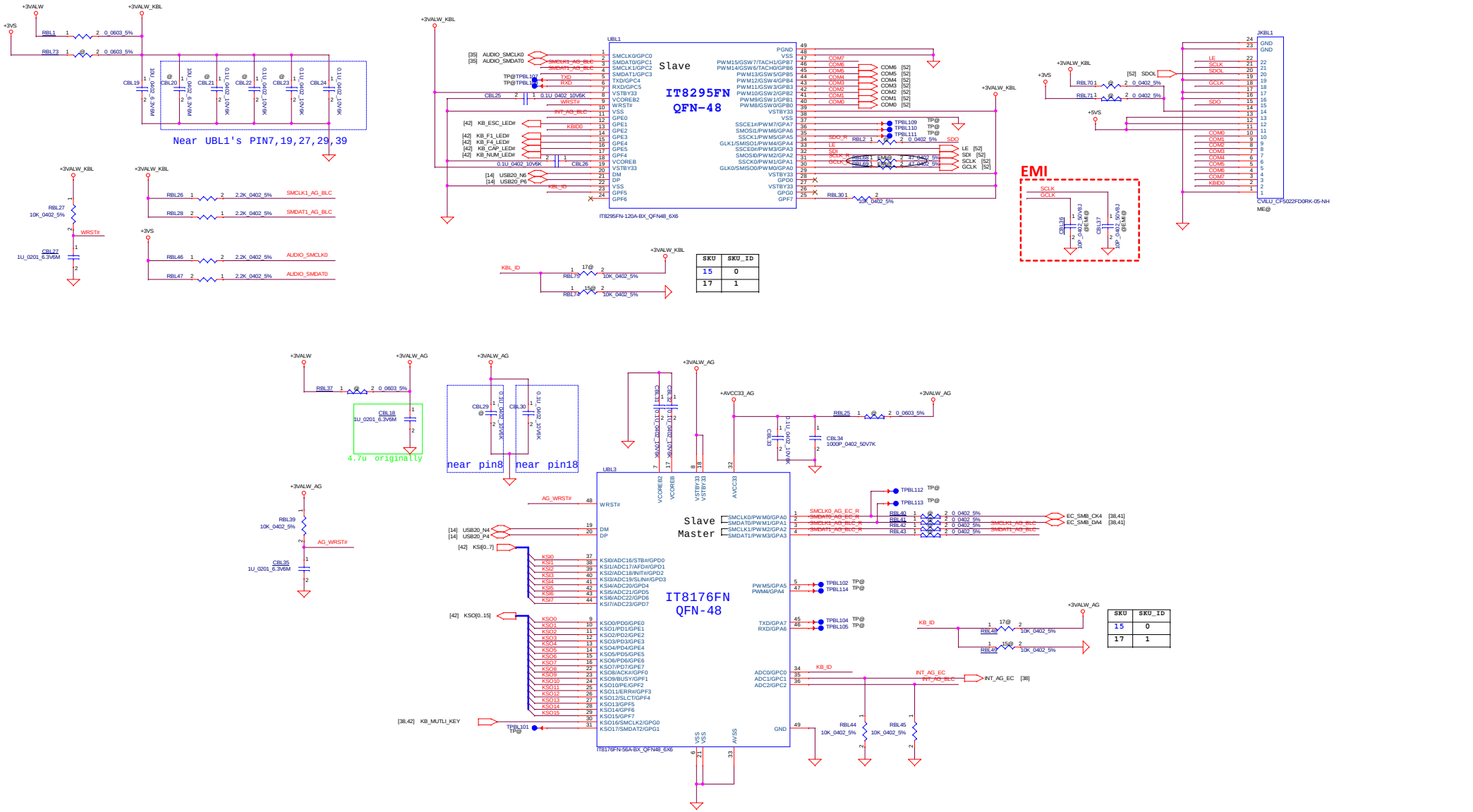

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: KB LED IT8176

Size: Custom | Document Number: LA-G131P | Rev: 0.3

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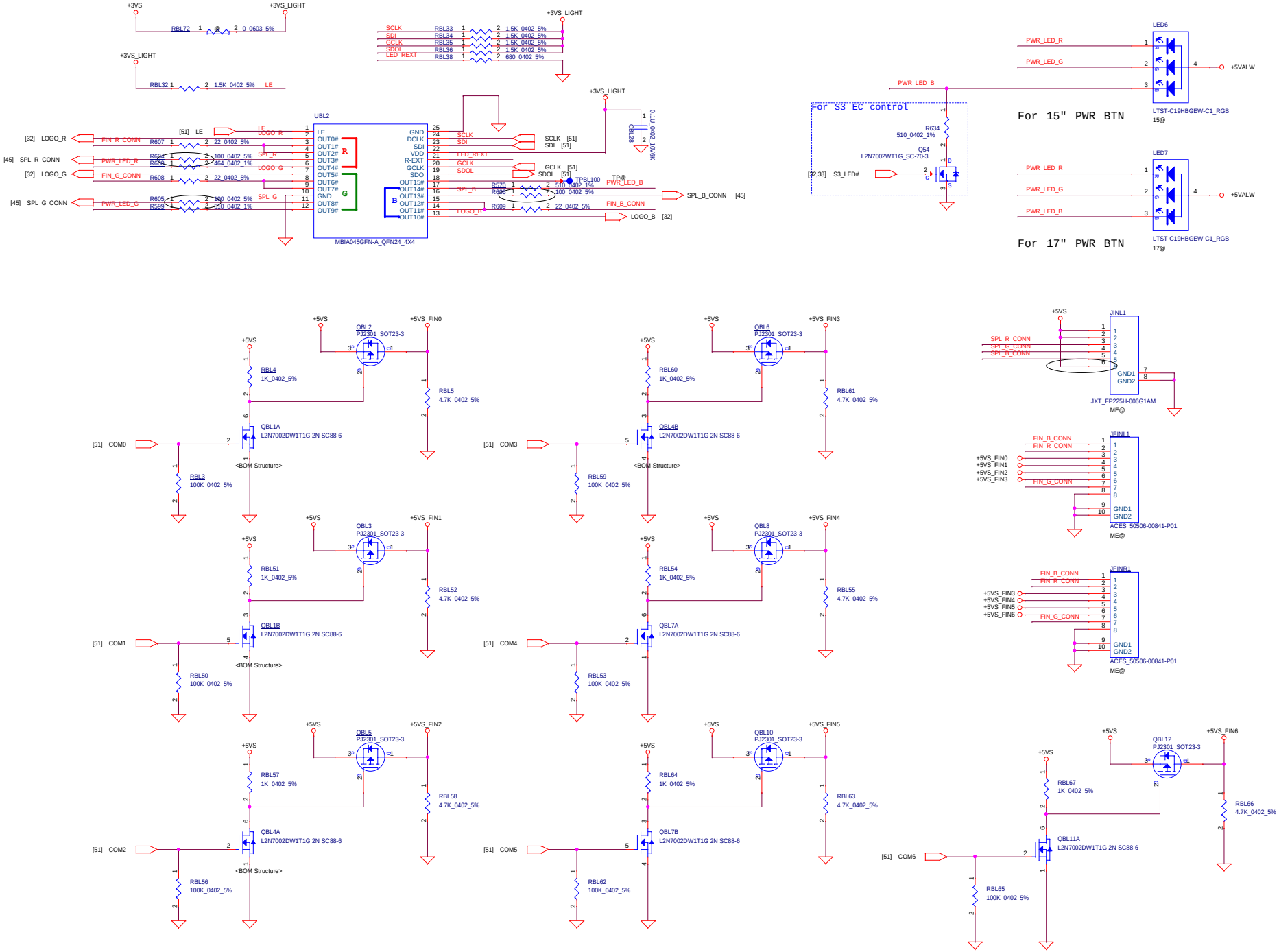

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: **FIN LED**

Size	Document Number	Rev
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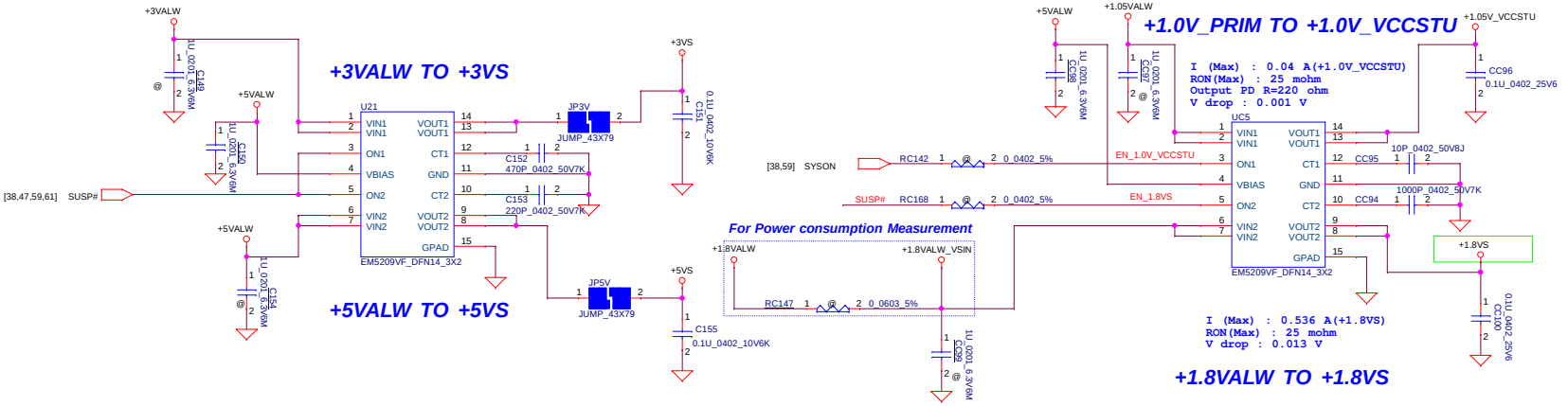
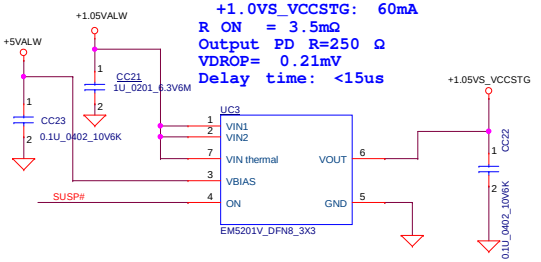
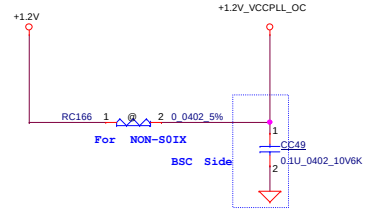
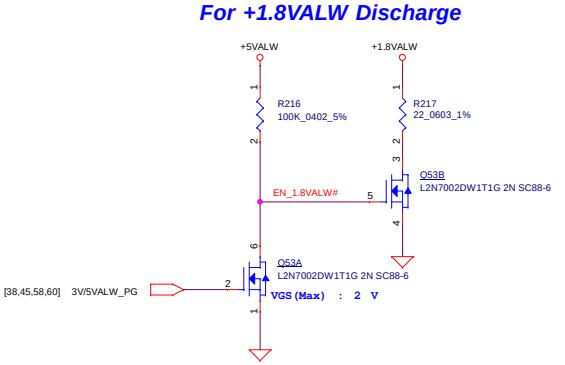


+1.05VALW TO +1.05VS_VCCSTG





+ 1.2V_VCCSFR_OC Load switch timing meet intel spec<= 240μ s



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.			
Title	DC INTERFACE		
Size	Document Number		Rev
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For Smart Performance (0608 remove)

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.		
Title: Smart performance		
Size: Custom	Document Number: LA-G131P	Rev: 0.3
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Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: **Backup**

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Fuse rating=(Normal operating current)/(0.75*percent of rating by temperature)
BATT(95c):8A/(0.75*0.8)=13.3A

CONN@
JBAT201
SUYIN_125022HB012M200ZL
SP071412230

VMB2
PF201
15A_32V_0501015.WR
SP040006F00
VMB
EMI@ PL201
5A_Z80_0805_2P
EMI@ PL202
5A_Z80_0805_2P
+12.6V_BATT+
EC_SMCA
EC_SMDA
PR201
100_0402_1%
PR202
100_0402_1%
PC201 EMI@
1000P_0402_50V7K
PC202 EMI@
0.01U_0402_25V7K
EC_SMB_CK1 [38,49,57]
EC_SMB_DA1 [38,49,57]
PR203
200K_0402_1%
+3VL
PR204
10K_0402_5%
VCIN1_BATT_TEMP [38,57]

PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

+EC_VCCA
PR205
16.5K_0402_1%
[38] VCIN0_PH1
PH201
100K_0402_1%_B25/50 4250K
ECAGND

CONN@
JDCIN1
DRAPH_PJSS0056-PB21H
APDIN
PF202
12A_24VDC_429007.WRML
SP040006C00
APDIN1
EMI@ PL203
5A_Z80_0805_2P
EMI@ PL204
5A_Z80_0805_2P
+19V_VIN
EMI@ PC203
1000P_0402_50V7K
EMI@ PC204
100P_0402_50V8J
EMI@ PC205
100P_0402_50V8J
EMI@ PC206
1000P_0402_50V7K
@PR206
0_0402_5%

Fuse rating=(Normal operating current)/(0.75*percent of rating by temperature)
AC(75c):6.75/(0.75*0.85)=10.6A

65W ID:287 ohm->0.913V
90W ID:549 ohm->1.394V
135W ID:1k ohm->1.885V

+3VALW
PR207
750_0402_1%
PC207
0.1U_0402_16V7K
PC208
680P_0402_50V7K
ADP_ID [38]
A/D

PR209
45.3K_0603_1%
+CHGRTC
1.5K_0603_5%
PR208
+3VL
PD201
S SCH DIO BAS40CW SOT-323
+RTCVCC
+CHGRTC_R
PR210
1K_0603_5%
JRTC1 CONN@
ACES_50271-0020N-001

RTC Battery
GC02001DR00
BATT CR2032 3V 210MAH MB 5 W/C 30MM

Compal Electronics, Inc.

Title: PWR- BATTERY CONN/OTP

Size: Custom | Document Number: DLPY5 / Y7 | Rev: 0.3

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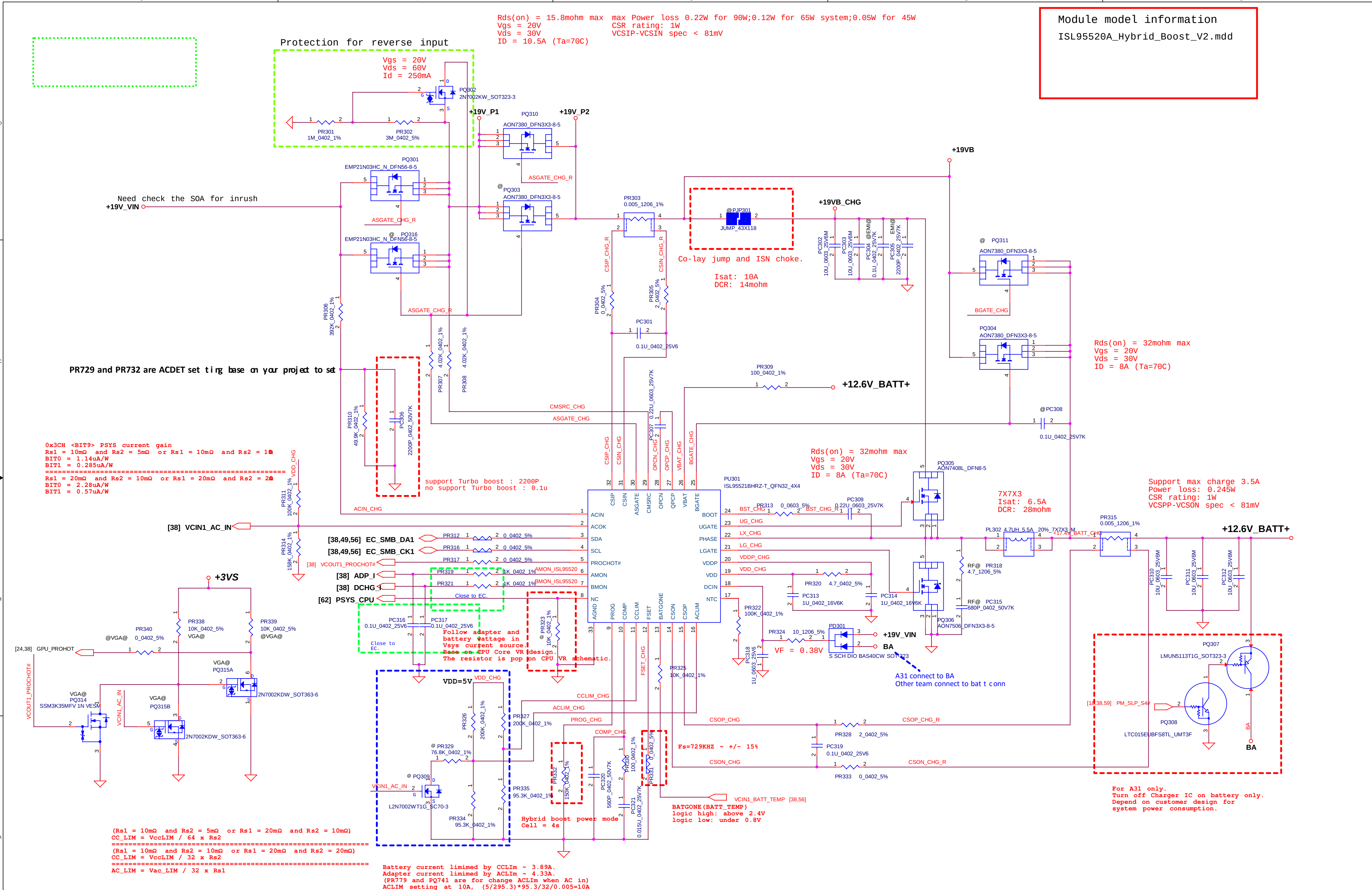


Module model information
ISL95520A_Hybrid_Boost_V2.mdd
Rds(on) = 15.8mohm max
Vgs = 20V
Vds = 30V
ID = 10.5A (Ta=70C)
max Power loss 0.22W for 90W;0.12W for 65W system;0.05W for 45W
CSR rating: 1W
VCSIP-VCSIN spec < 81mV
Protection for reverse input
Vgs = 20V
Vds = 60V
Id = 250mA
PQ302
2N7002KW_SOT323-3
PR301
1M_0402_1%
PR302
3M_0402_5%
+19V_P1
+19V_P2
PQ310
AON7380_DFN3X3-8-5
PQ301
EMP21N03HC_N_DFN56-8-5
ASGATE_CHG_R
Need check the SOA for inrush
+19V_VIN
PQ303
AON7380_DFN3X3-8-5
PQ316
EMP21N03HC_N_DFN56-8-5
PR303
0.005_1206_1%
@PJP301
JUMP_43X118
Co-lay jump and ISN choke.
Isat: 10A
DCR: 14mohm
+19VB
+19VB_CHG
PC302
10U_0603_25V6M
PC303
10U_0603_25V6M
PC304
0.1U_0402_25V7K
PC305
2200P_0402_25V7K
PQ311
AON7380_DFN3X3-8-5
BGATE_CHG
PQ304
AON7380_DFN3X3-8-5
Rds(on) = 32mohm max
Vgs = 20V
Vds = 30V
ID = 8A (Ta=70C)
PR306
392K_0402_1%
PR304
0_0402_5%
PR305
2_0402_5%
PC301
0.1U_0402_25V6
PR729 and PR732 are ACDET setting base on your project to set
PR307
4.02K_0402_1%
PR308
4.02K_0402_1%
PR309
100_0402_1%
+12.6V_BATT+
@PC308
0.1U_0402_25V7K
PR310
49.9K_0402_1%
PC306
2200P_0402_50V7K
CMSRC_CHG
ASGATE_CHG
PC307
0.22U_0603_25V7K
support Turbo boost : 2200P
no support Turbo boost : 0.1u
0x3CH <BIT9> PSYS current gain
Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 10mΩ and Rs2 = 10mΩ
BIT0 = 1.14uA/W
BIT1 = 0.285uA/W
Rs1 = 20mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ
BIT0 = 2.28uA/W
BIT1 = 0.57uA/W
Rds(on) = 32mohm max
Vgs = 20V
Vds = 30V
ID = 8A (Ta=70C)
PQ305
AON7408L_DFN8-5
PU301
ISL95521BHRZ-T_QFN32_4X4
7X7X3
Isat: 6.5A
DCR: 28mohm
Support max charge 3.5A
Power loss: 0.245W
CSR rating: 1W
VCSPP-VCSON spec < 81mV
PR311
100K_0402_1%
ACIN_CHG
[38] VCIN1_AC_IN
PR314
158K_0402_1%
[38,49,56] EC_SMB_DA1
[38,49,56] EC_SMB_CK1
[38] VCOUT1_PROCHOT#
[38] ADP_I
[38] DCHG_I
[62] PSYS_CPU
PR312
0_0402_5%
PR316
0_0402_5%
PR317
0_0402_5%
PR319
1K_0402_1%
PR321
1K_0402_1%
AMON_ISL95520
BMON_ISL95520
Close to EC
ACIN
ACOK
SDA
SCL
PROCHOT#
AMON
BMON
NC
BOOT
UGATE
PHASE
LGATE
VDDP
VDD
DCIN
NTC
PR313
0_0603_5%
BST_CHG
BST_CHG_R
PC309
0.22U_0603_25V7K
UG_CHG
LX_CHG
LG_CHG
VDDP_CHG
VDD_CHG
PL302
4.7UH_5.5A_20%_7X7X3_M
PR315
0.005_1206_1%
+12.6V_BATT+
PR320
4.7_0402_5%
PC313
1U_0402_16V6K
PC314
1U_0402_16V6K
RF@ PR318
4.7_1206_5%
RF@ PC315
680P_0402_50V7K
PQ306
AON7506_DFN3X3-8-5
PC310
10U_0603_25V6M
PC311
10U_0603_25V6M
PC312
10U_0603_25V6M
PR322
100K_0402_1%
PR324
10_1206_5%
PD301
S SCH DIO BAS40CW SOT-323
+19V_VIN
BA
VF = 0.38V
PC318
1U_0603_25V6
A31 connect to BA
Other team connect to batt conn
+3VS
PR338
10K_0402_5%
PR339
10K_0402_5%
PR340
0_0402_5%
[24,38] GPU_PROHOT
VGA@ PQ315A
2N7002KDW_SOT363-6
VGA@ PQ314
SSM3K35MFV 1N VESM
VGA@ PQ315B
2N7002KDW_SOT363-6
VCOUT1_PROCHOT#
VCIN1_AC_IN
PC316
0.1U_0402_25V6
PC317
0.1U_0402_25V6
Close to EC
Follow adapter and battery wattage in Vsys current source. Base on CPU Core VR design. The resistor is pop on CPU VR schematic.
PR323
10K_0402_1%
VDD=5V
VDD_CHG
PR326
200K_0402_1%
PR327
200K_0402_1%
CCLIM_CHG
ACLIM_CHG
PROG_CHG
COMP_CHG
@PR329
76.8K_0402_1%
@PQ309
L2N7002WT1G_SC70-3
VCIN1_AC_IN
PR335
95.3K_0402_1%
PR334
95.3K_0402_1%
PR332
150K_0402_1%
PC320
560P_0402_50V7K
PR330
100_0402_1%
PC321
0.015U_0402_25V7K
PR331
0_0402_5%
Hybrid boost power mode
Cell = 4s
PR325
10K_0402_1%
FSET_CHG
CSOP_CHG
CSOP_CHG_R
PR328
2_0402_5%
PC319
0.1U_0402_25V6
CSON_CHG
CSON_CHG_R
PR333
0_0402_5%
Fs=729KHZ ~ +/- 15%
VCIN1_BATT_TEMP [38,56]
BATGONE(BATT_TEMP)
logic high: above 2.4V
logic low: under 0.8V
PQ307
LMUN5113T1G_SOT323-3
[18,38,59] PM_SLP_S4#
PQ308
LTC015EUBFS8TL_UMT3F
BA
For A31 only.
Turn off Charger IC on battery only.
Depend on customer design for system power consumption.
(Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 20mΩ and Rs2 = 10mΩ)
CC_LIM = VccLIM / 64 x Rs2
(Rs1 = 10mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ)
CC_LIM = VccLIM / 32 x Rs2
AC_LIM = Vac_LIM / 32 x Rs1
Battery current limimed by CCLIm ~ 3.89A.
Adapter current limimed by ACLIm ~ 4.33A.
(PR739 and PQ741 are for change ACLIm when AC in)
ACLIM setting at 10A, (5/295.3)*95.3/32/0.005=10A

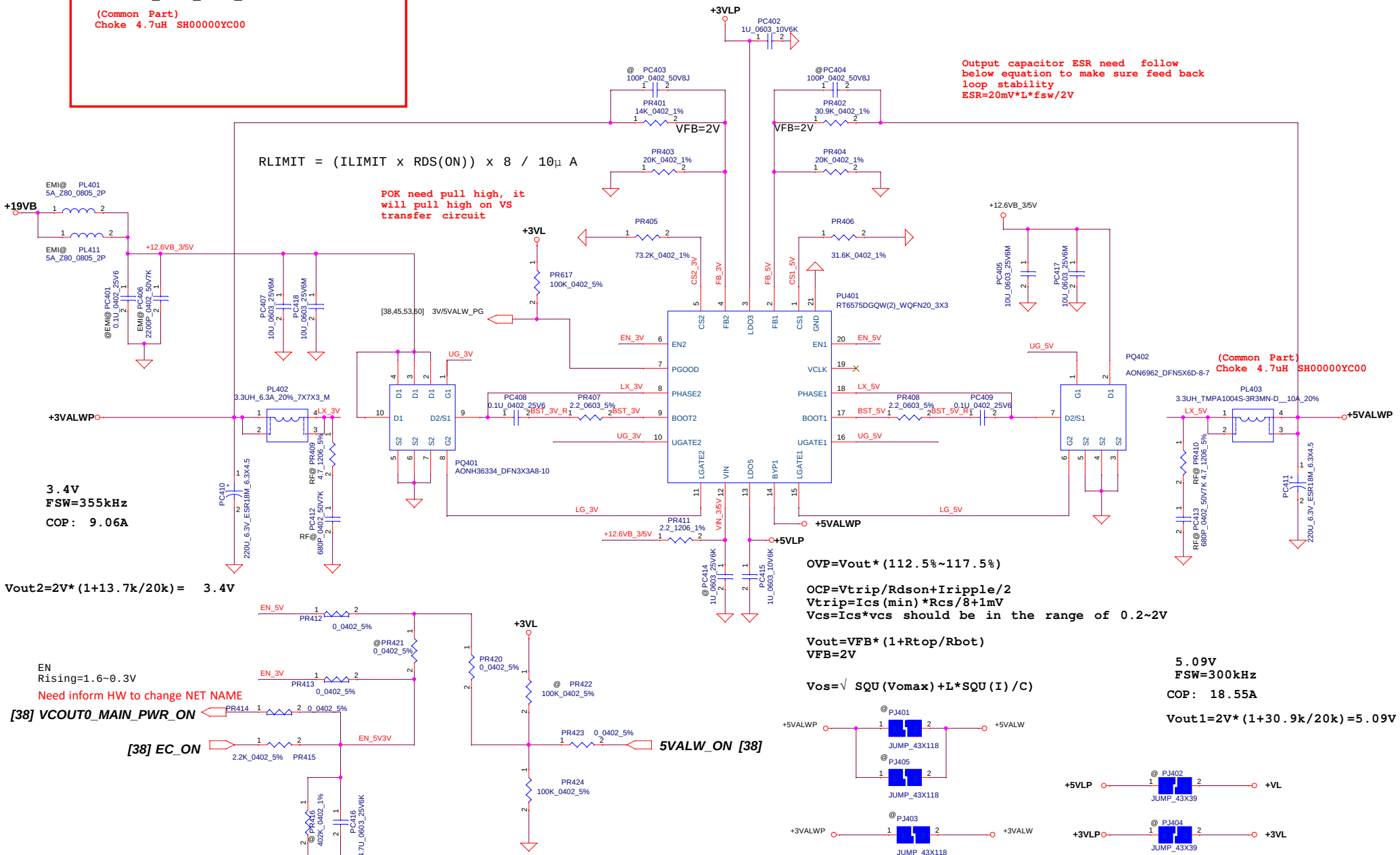
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2018/7/31	Deciphered Date	2018/7/31	Title: PWR_CHARGER

Size | Document Number | Rev 0.3

Module model information

RT6575D_DMOS_single_V2.mdd
RT6575D_DMOS_dual_V2.mdd

(Common Part)
Choke 4.7uH SH00000YC00



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size	Document Number	Rev
Custom		0.3

Date: Friday, July 06, 2018 Sheet 58 of 69

Module model information

RT8207P_single_V3.mdd For Single layer
RT8207P_dual_V3.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question, you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Vout=0.75V(1+6.04k/10k) =1.205V
OCP= 13.45 A

Vout=0.8V* (1+Rup/Rdown)

Down size

Down size

Down size

Down size

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

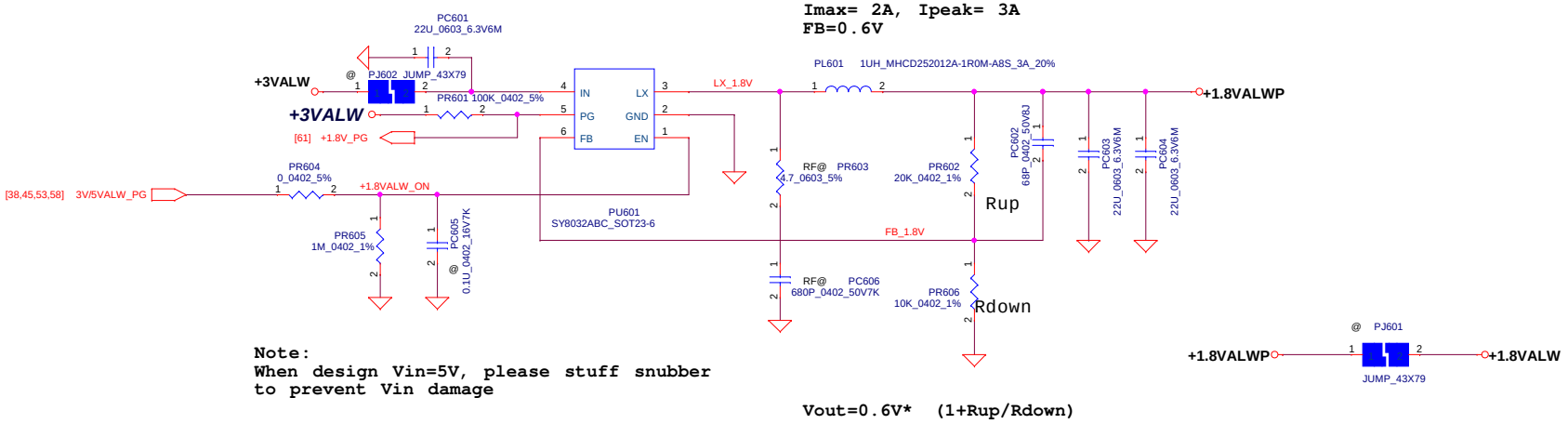
Title: RT8207P

Size: Custom | Document Number | Rev 0.3

Date: Friday, July 06, 2018 | Sheet 59 of 69

Module model information

SY8032_V2.mdd



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

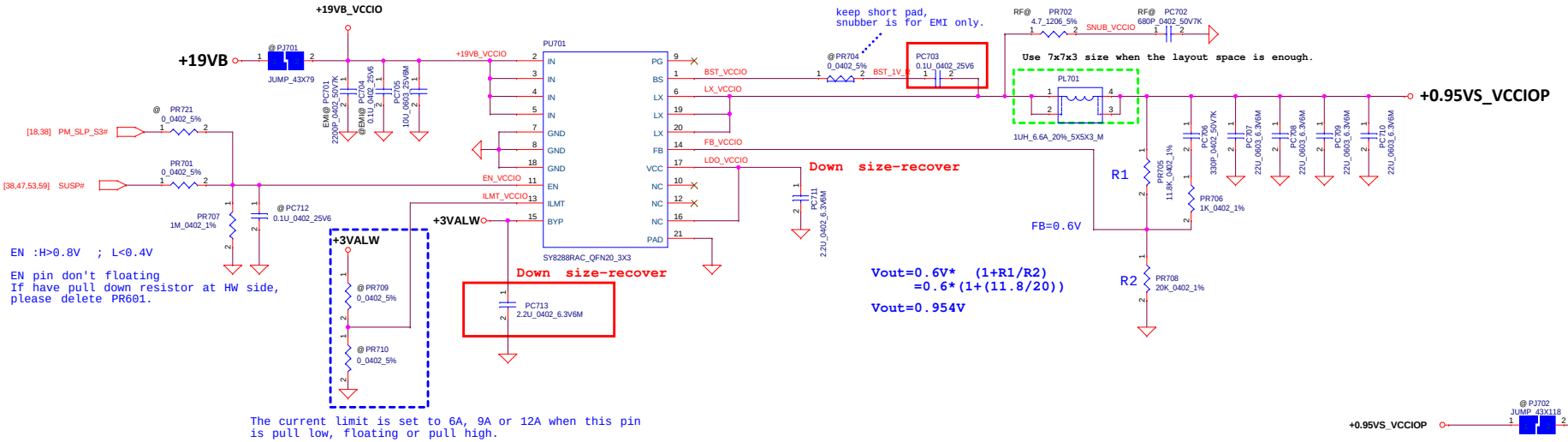
Title: APL5930

Size: Custom | Document Number | Rev: 0.3

Date: Friday, July 06, 2018 | Sheet 60 of 69

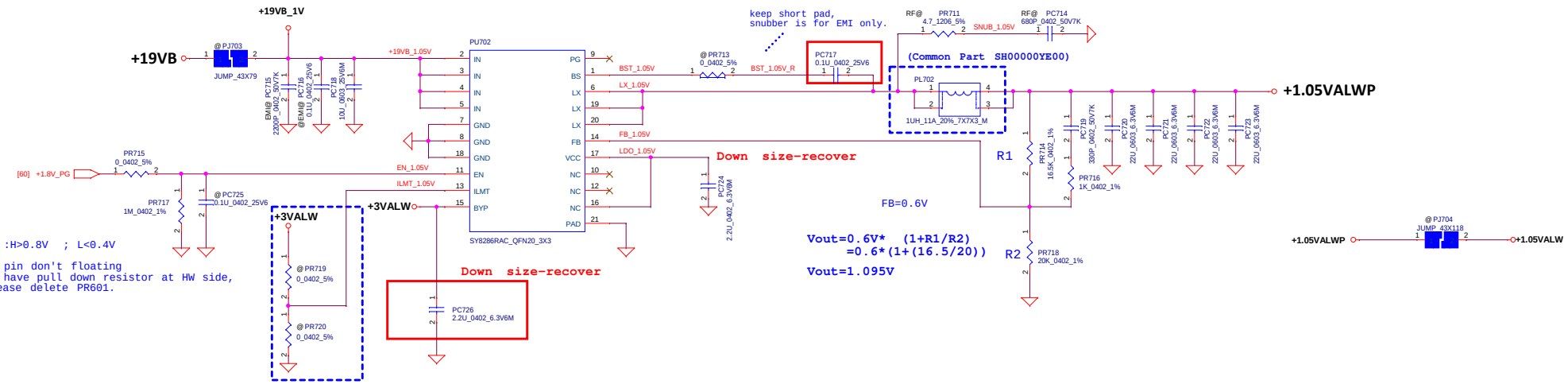
Module model information

SY8286_V2_single.mdd
SY8286_V2_dual.mdd



Module model information

SY8288_V2_single.mdd
SY8288_V2_dual.mdd



Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: SY8286

Size	Document Number	Rev
C		0.3

Date: Friday, July 06, 2018 Sheet 61 of 69

Module model information

NCP81205_H42_V6A.mdd for IC portion

NCP81205_H42_V6B.mdd for SW portion

SKL H42(45W)		
TDC@VCORE	56A	
IccMax@VCORE	68A	
OCP@VCORE	75A	
TDC@VGT	39A	
IccMax@VGT	54A	
OCP@VGT	61A	
TDC@VCCSA	10A	
IccMax@VCCSA	11A	
OCP@VCCSA	16.5A	
Fsw	600KHz	
DCR	0.9mohm +/-7%	

VCCSA:

H42: IccMAX@SA= 11A RIccMAX@SA= 34.8K ---> PR109

RIccMAX@SA= IccMAX*2V/10uA/64A

H42: IOUTSP@SA= 11A RIOUTSP@SA=19.6K ---> PR102

RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR/(RPHSP+Rth+RCSSP))

H42: OCP@SA= 16.5A RLIMSP@SA=8.45K ---> PR101

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR/(RPHSP+Rth+RCSSP))

Load line@SA= 9.1m

RDRPSP@SA=1.4K ---> PR95

RDRPSP= Load line*(RPHSP+Rth+RCSSP)/(gm * DCR) /(Rth+RCSSP)

CFL-H62 (45W)
IA: Max current=128A, loadline=1.8mohm,
GT: 0~1.52V, Max current=32A, loadline=2.7mohm
SA: 0~1.52V, Max current=11A, loadline=10.3mohm

OCP
IA: 154A
GT: 38.4A
SA: 16.5A
OVP
DAC+370mV

VCCCORE:

H42 OCP@Vcore= 75A RLIM@VCORE=13.7K ---> PR129

RLIM= IoutLIMIT * Load line/10

H42 IccMAX@Vcore= 68A RIccMAX2ph= 52.3K ---> PR154

RIccMAX2ph= (IccMAX2Ph*2V)/ (10uA*256A)

H42 Iout@Vcore= 68A RIOUT@Vcore=22.6K ---> PR120

RIOUT= 2* RLIM /(10 *IOUTICCMAX * Load line)

H42 Load line@VCORE= 1.8m RPH@Vcore=113K ---> PR135,PR137,PR140

Load line= (RCS2+(RCS1*Rth/(RCS1+Rth)))*IOUTTOTAL * DCR/RPH

VCCGT:

H42 OCP@GT= 61A RLIM@GT=16.2K ---> PR130

RLIM= IoutLIMIT * Load line/10

H42 IccMAX@GT= 54A RIccMAX2ph= 42.2K ---> PR150

RIccMAX2Ph= (IccMAX2Ph*2V)/ (10uA*256A)

H42 Iout@GT= 54A RIOUT@GT=24.9K ---> PR126

RIOUT= 2* RLIM /(10 *IOUTICCMAX * Load line)

H42 Load line@GT= 2.65m RPH@GT=75K ---> PR139,PR141,PR144

Load line= (RCS2+(RCS1*Rth/(RCS1+Rth)))*IOUTTOTAL * DCR/RPH

ENABLE
Upper Threshold > 0.8V
Lower Threshold < 0.3V

472mV/120uA=3.933K ohm
Active Point110 degreeC = 4.206K ohm

472mV/120uA=3.933K
Active Point110 degreeC = 4.206K ohm

NCP81205 Operating Frequency Rosc=97.6K
I/A, GT and SA are 600KHz

VBOOT: Debug setting
PR156 change from 24.9K to 169K.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/7/31	Deciphered Date 2018/7/31	Title NCP81205 H42

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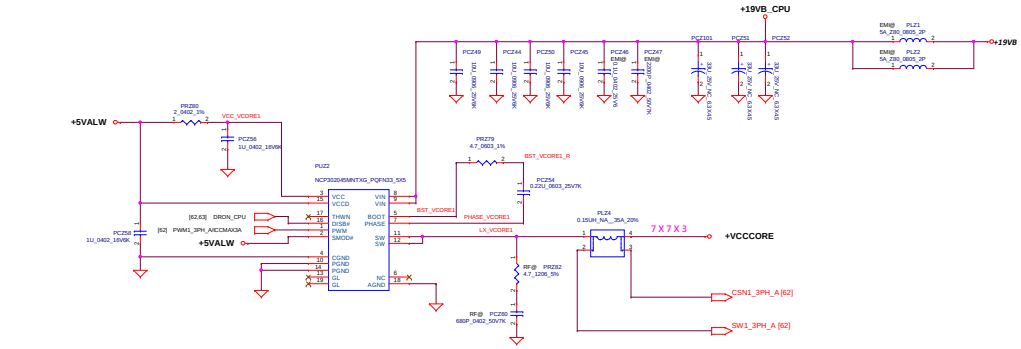
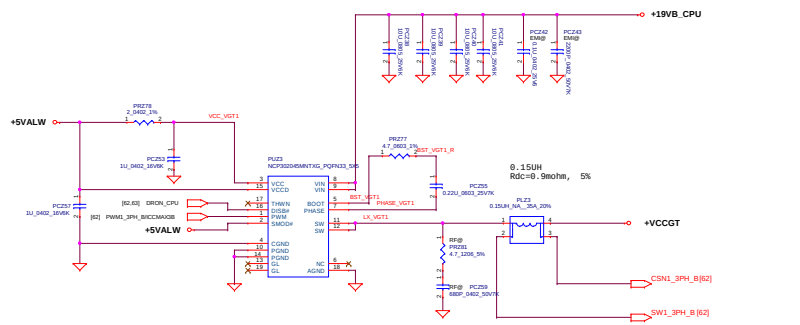
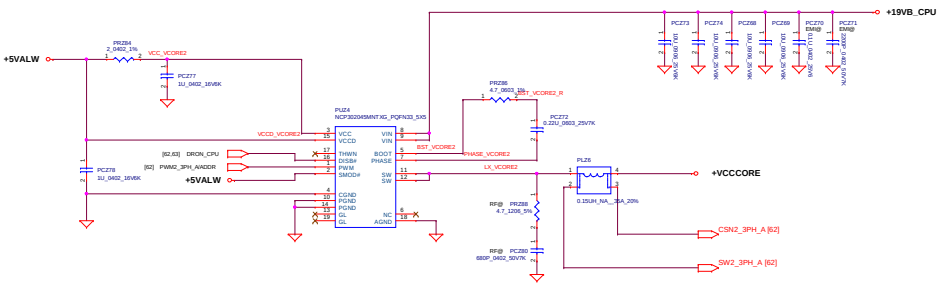
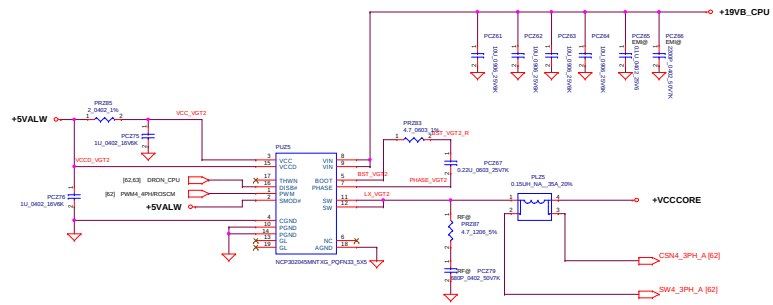
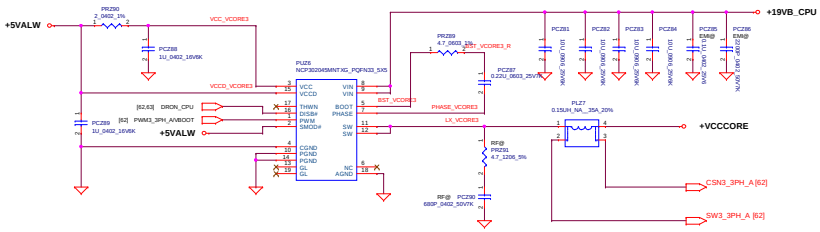










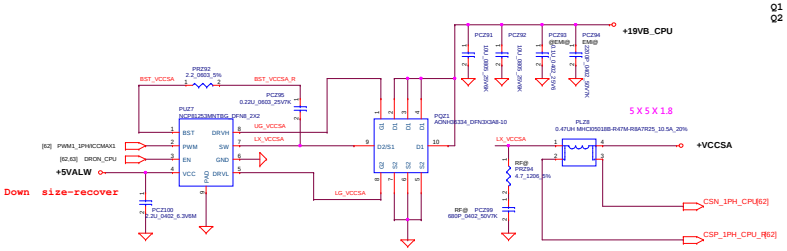
VCC_CORE(3 phase)
TDC 56A(Dual-MOS)
Peak Current 67A
OCP current > 60A
Load line -1.6mV/A (SKL H-44e)
FSW=600kHz
DCR 0.9mohm +/-5%

	TYP	MAX
Q1 Rds(on)	:6.8mohm ,	8.6mohm
Q2 Rds(on)	:2.0mohm ,	2.5mohm

VCCGT(2phase)
TDC 80A(Dual-MOS)
Peak Current 109A
OCP current > 109A
Load line -1.4mV/A (SKL H-44e)

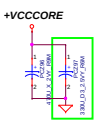
FSW=600kHz
DCR 0.9mohm +/-5%

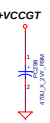
	TYP	MAX
Q1 Rds(on)	:6.8mohm ,	8.6mohm
Q2 Rds(on)	:2.0mohm ,	2.5mohm



VCCSA
Load line -9.1mV/A
FSW=600kHz
DCR = 6.2 mohm +/- 5%

	TYP	MAX
Q1 Rds(on)	:12.4mohm ,	15.8mohm
Q2 Rds(on)	:9.1mohm ,	11.6mohm





Must review KBL SA rating.

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Issued Date	2018/7/31	Deciphered Date 2018/7/31	Title: NCP81205_PowerStage

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VCC_CORE Place on CPU Back Side @ V09
22U_0603 *23 pcs+ 1U_0201*30 pcs

SIT
22U_0603 *11 pcs+ 1U_0201*30 pcs

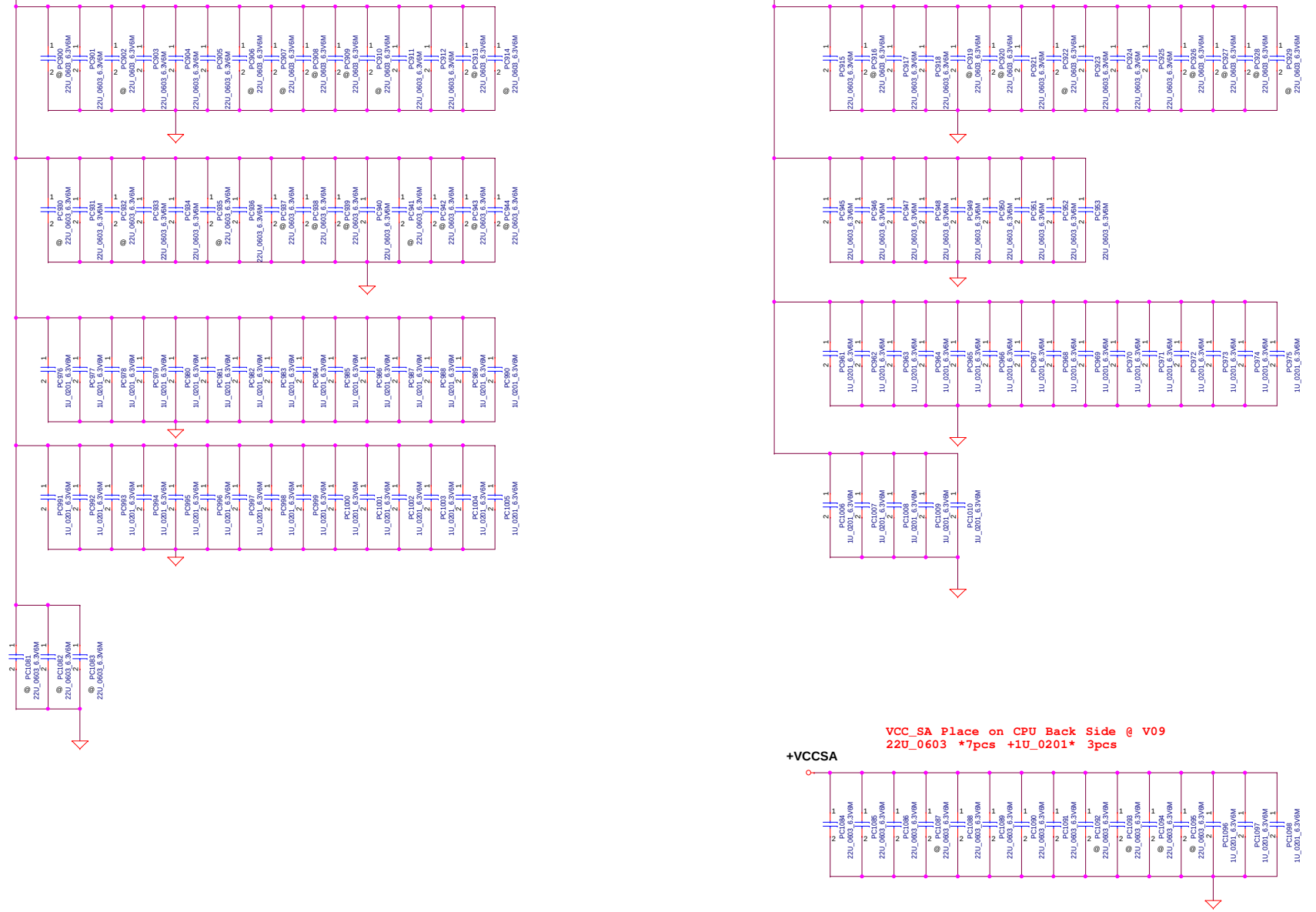
VCC_GT Place on CPU Back Side @ V09
22U_0603 * 16 pcs +1U_0201* 20pcs

+VCCCORE

+VCCGT

VCC_SA Place on CPU Back Side @ V09
22U_0603 *7pcs +1U_0201* 3pcs

+VCCSA



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/7/31	Deciphered Date 2018/7/31	Title: PWR-PROCESSOR DECOUPLING

Size	Document Number	Rev
C		0.3

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Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

Module model information:
RT8813D_V2A for IC module
RT8813D_V2B for SW module

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

R1, R2, R3, R4, R5, C are based on VGA type to set.

+VGA_CORE
EDP-Continuous 46+13=59A
EDP-Peak 106+18=124A
OCP > 100A
Please base on GPU spec to calculate.

PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

Switching frequency setting:
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)=352Khz

Current Limit threshold setting
Rocset= (Ivalley * Rds(on) +40mv) / Iocset

OCP=Current limit + Iripple/2
=[((15.8k*10uA-40mV)/2.5mohm)+(7.8A/2)]*3phase
=153A

Relative Over Voltage Protection Threshold : 145% ~150%
Absolute Over Voltage Protection Threshold : 1.9 V~ 2.1V

PWM VID Pull high on HW side

High: >1.6V
Low: <0.8V

Please base on GPU spec to modify output cap.

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Issued Date	2018/7/31	Deciphered Date	2018/7/31

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Title: VGA_CORE

Size	Document Number	Rev
Custom	VGA_CORE	0.3

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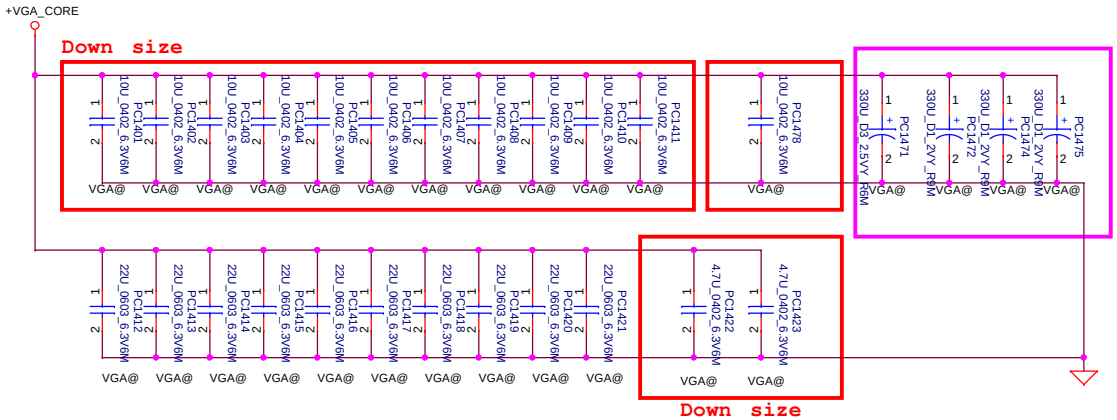
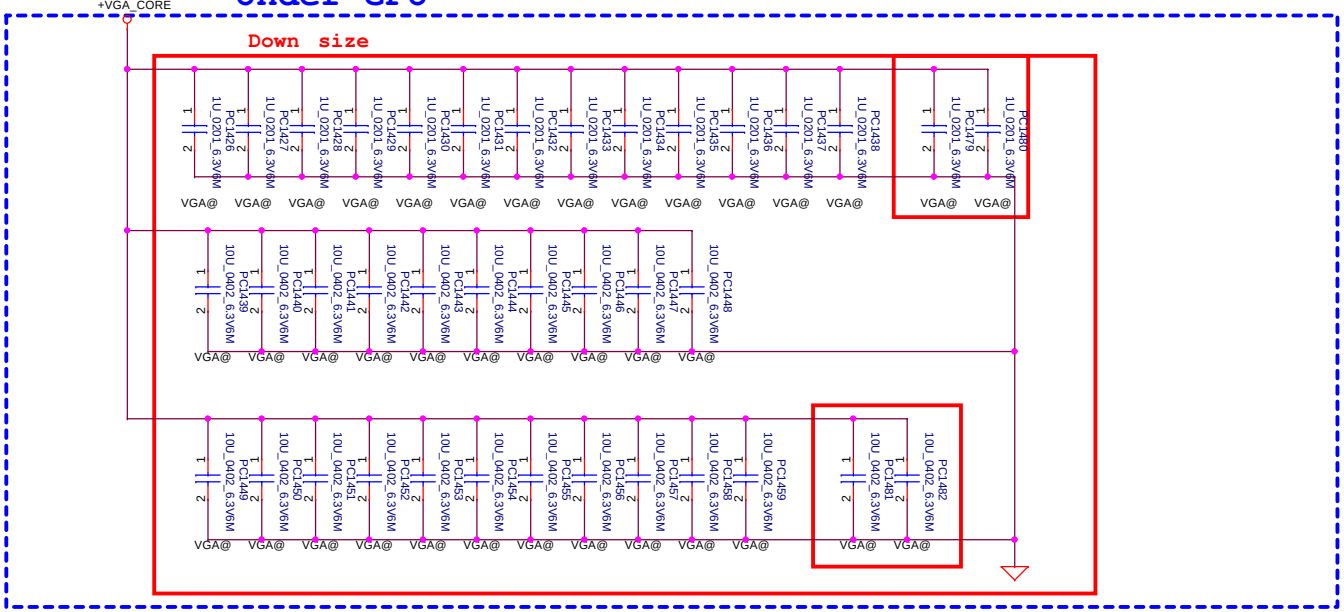
Must confirm the thermal for Input/output cap rating.

+NVVDD
330uF X 4
22uF_0603 X 10
10uF_0603 X11+1
4.7uF_0603 X 2

Near GPU



Under GPU



+NVVDD

10uF_0603 X21+2
1uF_0402 X 13+2

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: VGA DECOUPLING

Size | Document Number: VGA_CORE | Rev: 0.3

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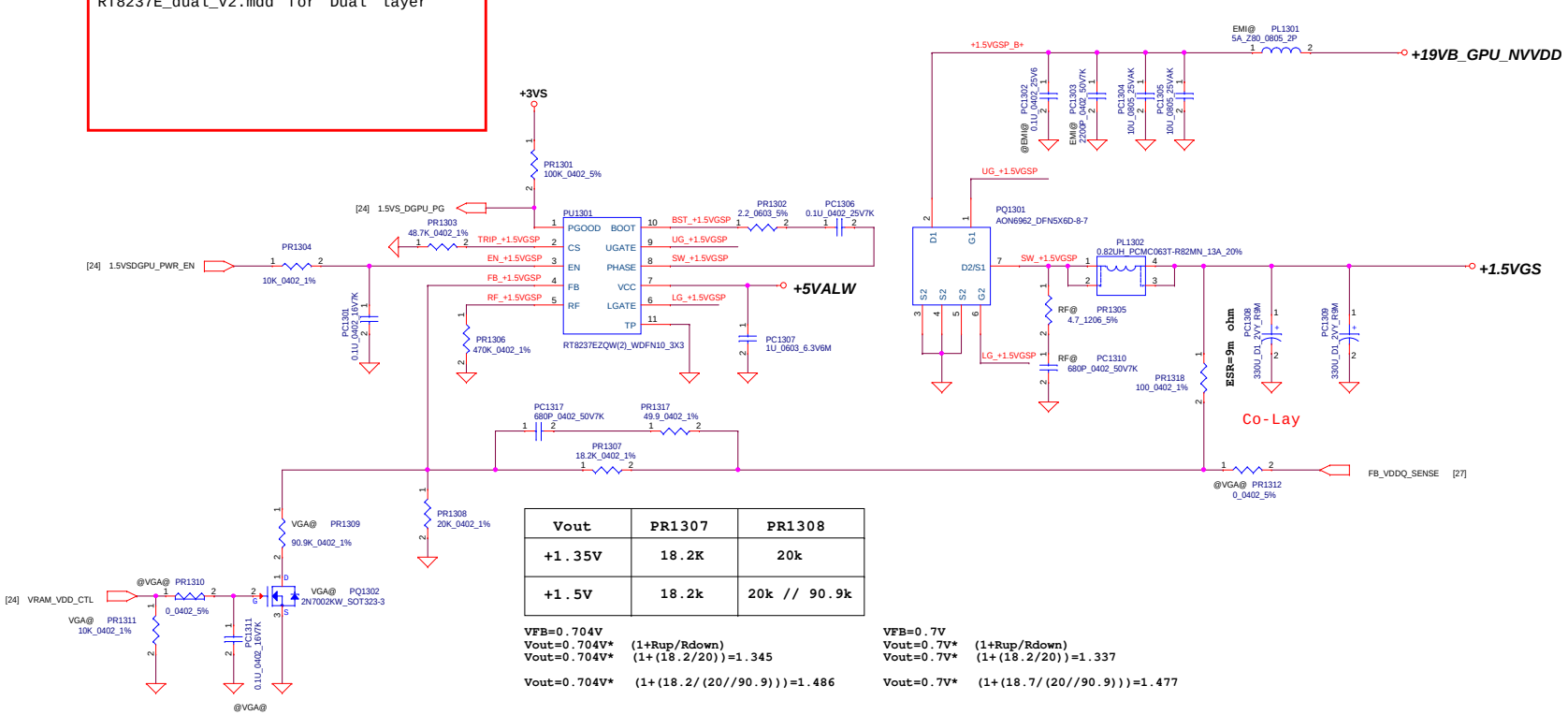
Module model information

RT8237E_single_V2.mdd for Single layer
RT8237E_dual_V2.mdd for Dual layer



Vout	PR1307	PR1308
+1.35V	18.2K	20k
+1.5V	18.2k	20k // 90.9k

VFB=0.704V
Vout=0.704V* (1+Rup/Rdown)
Vout=0.704V* (1+(18.2/20))=1.345

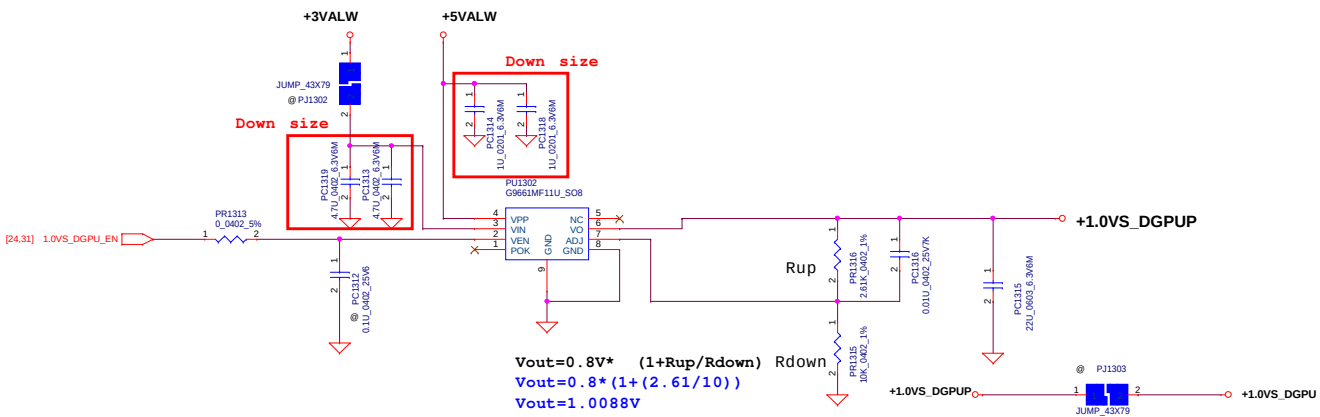
Vout=0.704V* (1+(18.2/(20//90.9)))=1.486

VFB=0.7V
Vout=0.7V* (1+Rup/Rdown)
Vout=0.7V* (1+(18.2/20))=1.337

Vout=0.7V* (1+(18.7/(20//90.9)))=1.477

Switching Frequency: 290kHz

Rlimt=48.7K
Iocp=27.27A (max)
OVP: 120%~130%



Vout=0.8V* (1+Rup/Rdown)
Vout=0.8*(1+(2.61/10))
Vout=1.0088V

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/7/31

Compal Electronics, Inc.

Title: VRAM

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Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	FAE Suggest Boost CAP change to 0402 size	59	PC703 & PC717 from 0.1U 0201 10V6K change to 0.1U 0402 25V6	1/22	SDV
2	EMI Suggest, Unmount Snubber	63	Unmount PR803 PR819 PR830 PC807 PC818 PC826	1/31	SDV
3	RF Suggest, Mount Snubber		Mount PC315 PR318 PC412 PR409 PC413 PR410 PC606 PR603, PC714 PR711 PC702 PR702 PCZ59 PRZ81 PCZ80 PRZ88 PCZ60 PRZ82 PCZ99, PRZ94 PCZ79 PRZ87 PCZ90 PRZ91 PC807 PR803 PR819 PC818 PC826 PR830 PC1310 PR1305	1/31	SDV
4	Power design VR_HOT# pull high at HW side	60	Unmount PR123	1/31	SDV
5	MLCC Downsize		PC302 PC303 PC310 PC311 PC312 PC407 PC405 PC503 PC504 PC705 PC718 from 10U 0805 25V6K change to 10U 0603 25V6 M PCZ59 PCZ60 PCZ79 PCZ80 PCZ90 PCZ99 PC412 PC413 (RF @) PC208, PC315 PC702 PC714 (RF @) PC807 PC818 PC826 (@ EMI@) from 0805 change to 0603 (SE074681K80) PC416 from 0805 change to 4.7U 0603 25V6K (SE000013880) PC505 & PC1306 from 0.1U 0603 25V7K change to 0.1U 0402 25V7K (SE00000W210)	02/02	SDV
6	Common P/N for other part, for 2nd	56	PD301 from SCS00008E00 change to SCS00001200 PQ302, PQ1302 from SB00000ST00 change to SB000009Q80	02/02	SDV
7	ME interfeence	65	PC1471 from SGA00009S00 (D1) change to SGA00006A00 (D3) PL502 Change to SH00001D000 (H=2mm)	02/07	SDV
8	Power design Reserved PROCHOT 0ohm for test	56	PR317 from R-SHORT change to 0ohm	02/08	SDV
9	Part Count Reduce		PR90 PR94 PR107 PR111 PR114 PR117 PR165 PR166 PR331, PRZ93, PR110, PR103 from 0ohm change to R-SHORT Remove PRZ93	02/08	SDV SDV
10	Reserved, for Current rating	56	Add PQ310, PQ311 AON7380_DFN3X3-8-5	02/09	SDV
11	CPU VTT interposer test adjust	61	PRZ79, PRZ77, PRZ86, PRZ83, PRZ89 from 39_0603_1% change to 47_0603_1% PR102 from 27.4K_0402_1% change to 25.5K PC111 from 0015U_0402_25V7K change to 001U PC113 from 150P_0402_50V8J change to 47P PR95 from 143K_0402_1% change to 133K PR120 from 24.3K_0402_1% change to 25.5K PR135 PR137 PR140 PR145 from 113K_0603_1% change to 118K PR139 from 75K_0603_1% change to 84.5K	02/09	SDV
12	Power design, for GPU PROCHOT	56	Add PR338, PQ314, PQ315, PR340	02/22	SDV
13	HW sequence	66	PR1313 from 10k change to 0ohm, Unmount PC1312 PR1304 from 0ohm change to 10k, Mount PC1301	02/22	SDV
14	Source (Bead) change tone w common part		PLZ1 PLZ2 PL201 PL202 PL401 PL411 PL501 PL801 PL802 PL1301 PL203 PL204 From SM01000P200 change to SM01000U600, SUPPRE_5A Z80 20 M0805	02/26	SDV
15	Thermal test M/B temperature over 85, MLCC form X5R change to X6S	64	PC803 PC804 PC812 PC813 PC823 PC824 PC1304 PC1305 From 10U 25V KX5R 0805 H125 change to SE000010S00, 10U 25V KX6S 0805 H125	02/26	SDV
16	GPU PGD add 3300PF, To avoid signal glitch	64	Add PC830	02/26	SDV
17	Change to Common source	62	PRZ77 PRZ79 PRZ83 PRZ86 PRZ89 change to SD000006T80	03/06	SDV
18	MLCC Downsize		PC520 PC1314 PC1426 PC1438 from 1U 63V KX5R 0402 change to 1U 63V MX5R 0201 .& add PC525 PC1318 PC1479 PC1480 PC713 PC726 PC711 PC724 PCZ100 from 2.2U 63V M X5R 0402 change to 2.2U 63V M X5R 0201 & add PCZ102 PC727 PC728. PC521 PC1313 PC1422 PC1423 from 4.7U 63V KX5R 0603 change to 4.7U 63V M X5R 0402 .Add PC526 PC1319. PC506 PC507 PC1401 PC1411 PC1439 PC1459 from 10U 63V M X5R 0603 change to 10U 63V M X5R 0402 Add PC1478 PC1481 PC1482	03/19	SIT
19	Power design	56	PQ306 From AON7752 change to AON7506	04/16	SIT
20	CPU VTT interposer test adjust	61	Mount PC125 PC128 & change to 82P_0402_50V8J PC130 from 01U_0402_25V6 change to 022U_0402_25V6K Unmount PC930 PC902 PC910 PC914 PC1083 PC935 PC906 PC907 PC941 PC1081 PC1082 PC932 PC922 PC929	04/16	SIT
21	Power design	57	Add PC417 & PC418, 10U 0603 PCZ101 PCZ51 & PCZ52 change to 47U 25V M 63X5.4	04/19	SIT
22	HW Suggest	57	Add PR420 PR421 PR422 PR424	04/25	SIT
23	Power design	56	Unmount PR340	04/27	SIT
24	HW Suggest	56	Add +12V_PGnet at PU501 pin10. PR829 change to 10K	05/14	SVT
25	MLCC Downsize		PCZ11, PC724 PCZ100 PC713 & PC726 change to 2.2U 63V MX5R 0402 (SE000008880)	05/22	SVT
26	ME	63	PCZ101 PCZ51 & PCZ52 change to 33U_25V_NC_63X4.5	06/06	SVT
27	HW Suggest	61	PR714 change to 16.5K, PR401 change to 14K		
28	HW Suggest	63	Remove PRZ97 PRZ98 PRC99 PR851 & PR852		
29	170 Wadapter design	57	Add PQ316 (EMP21N03)		
30	Acoustic noise issue	64	PCZ96 PCZ98 change to SGA00003N00 (470U 2V Y XL E=RSM)		
31	HW Suggest	58	Mount PR424		

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Compal Electronics, Inc.

Title: **PIR (PWR)**

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Custom		0.3

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Reduce SATA stub	44	Add 0 ohm to avoid stub in SATA driver	2018/01/23	
2	Follow the HSIO for HM370		M.2 SSD change the HSIO port to 21,22,23,24 TBT change the HSIO port to 17,18,19,20	2018/01/23	
3	Optimize the USB3 signal	45	remove U3 redriver from MB, and move to Sub board	2018/01/31	
4	Optimize the USB3 signal	45	change io pin define	2018/01/31	
5	ME requirement	35	change the Audio jack symbol	2018/02/02	
6	Increase the speaker power	36	change the smart AMP to use B+	2018/02/07	
7	Follow Intel design	39	Add CNVi power control	2018/02/07	
8	Optimize the USB3 signal	39	Move the 17" lid switch to MB	2018/01/31	

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Title: PIR (EE)

Size: Custom | Document Number | Rev: 0.3

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