Compal Confidential

N3V3 Intel Gemini Lake Schematic

COMPAL CONFIDENTIAL

MODEL NAME : EDI55
PCB NO : DA60021O010
BOM P/N : 431ADZ31L01

2018/11/08

Rev 1.0(A00)

@ : Un-pop Component
EC@ : EC
EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
ESPI@:ESPI
LPC@:LPC
PCB@:PCB
Lan@: lan component
lan@EMI@:EMI for lan pop component
1000@:Giga
CNVI@: CNVI interface
XDP@ : XDP Component
CONN@ : Connector Component
TP_WAKE@/NTP_WAKE@ : TouchPad wake
KBBL@ : KB Backlight
MMC@ : eMMC / NMMC@: without eMMC
FFS@ : Free Fall Sensor
45@:HDMI logo
N3@/V3@:N3000/V3000

SR3RZ_R3@/SR3S0_R3@/SR3S1_R3 : Pentium/Celeron QC/Celeron DC
S32G_R3@/S64G_R3@/H32G_R3@/H64G_R3@ : eMMC Type

DAZ R1

ZZZ
PCB
Part Number = DAZ2ED00100
PCB EDI55 LA-G094P LS-F112P/F114P 02
PCB_DAZ_R1@

DAZ R3

ZZZ
PCB
Part Number = DAZ2ED00101
PCB EDI55 LA-G094P LS-F112P 02 GOLD A31!
PCB_DAZ_R3@

PCB R1

ZZZ
PCB
Part Number = DA60021O010
PCB 2ED LA-G094P REV1 M/B 3
PCB_R1@

PCB R3

ZZZ
PCB
Part Number = DA60021O011
PCB 2ED LA-G094P REV1 M/B GOLD 3 A31 !
PCB_R3@

CPU R1

UC1 SR3RZ_R1@
FH8068003067406 SR3RZ
Part Number = SA0000BEH2L
S IC FH8068003067406 SR3RZ B0 1.1G FCBGA

UC1 SR3S0_R1@
FH8068003067408 SR3S0
Part Number = SA0000BDQ1L
S IC FH8068003067408 SR3S0 B0 1.1G FCBGA

UC1 SR3S1_R1@
FH8068003067417 SR3S1
Part Number = SA0000BEJ0L
S IC FH8068003067417 SR3S1 B0 1.1G

CPU R3

UC1 SR3RZ_R3@
FH8068003067406 SR3RZ
Part Number = SA0000BEH3L
S IC FH8068003067406 SR3RZ B0 1.1G A31!

UC1 SR3S0_R3@
FH8068003067408 SR3S0
Part Number = SA0000BDQ2L
S IC FH8068003067408 SR3S0 B0 1.1G A31!

UC1 SR3S1_R3@
FH8068003067417 SR3S1
Part Number = SA0000BEJ1L
S IC FH8068003067417 SR3S1 B0 1.1G A31!

Layout Dell logo

Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2016/12/31

Compal Electronics, Inc.			
Title: Cover Sheet			
Size: Custom	Document Number: LA-G094PR10		Rev: 1.0
Date: Thursday, November 08, 2018	Sheet: 1	of: 39	

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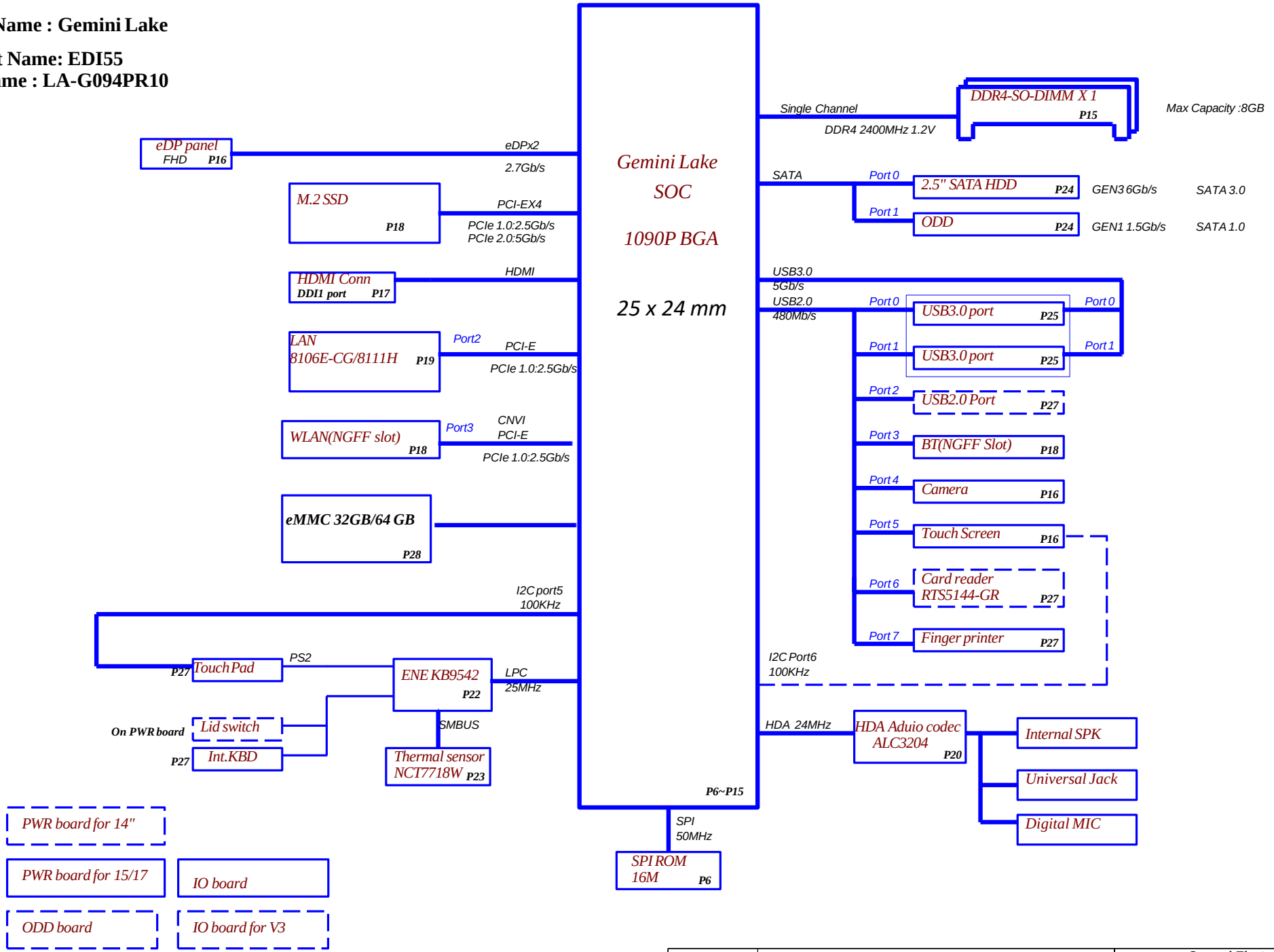
Model Name : Gemini Lake

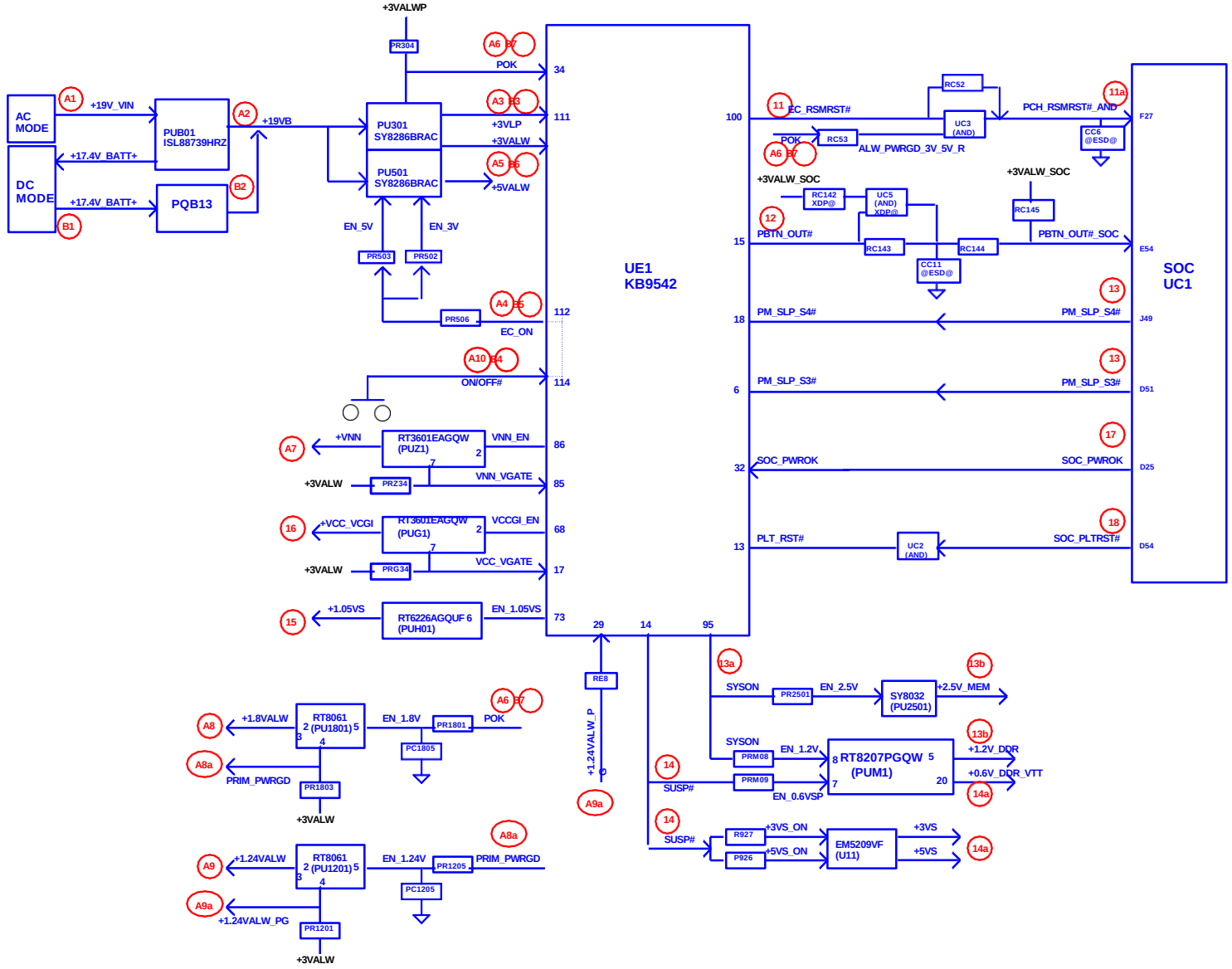
Project Name: EDI55
File Name : LA-G094PR10



Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2018/07/10

Compal Electronics, Inc.	
Title	Block Diagrams
Size / Document Number	LA-G094PR10
Rev	1.0
Date:	Thursday, November 08, 2018
Sheet	2 of 39

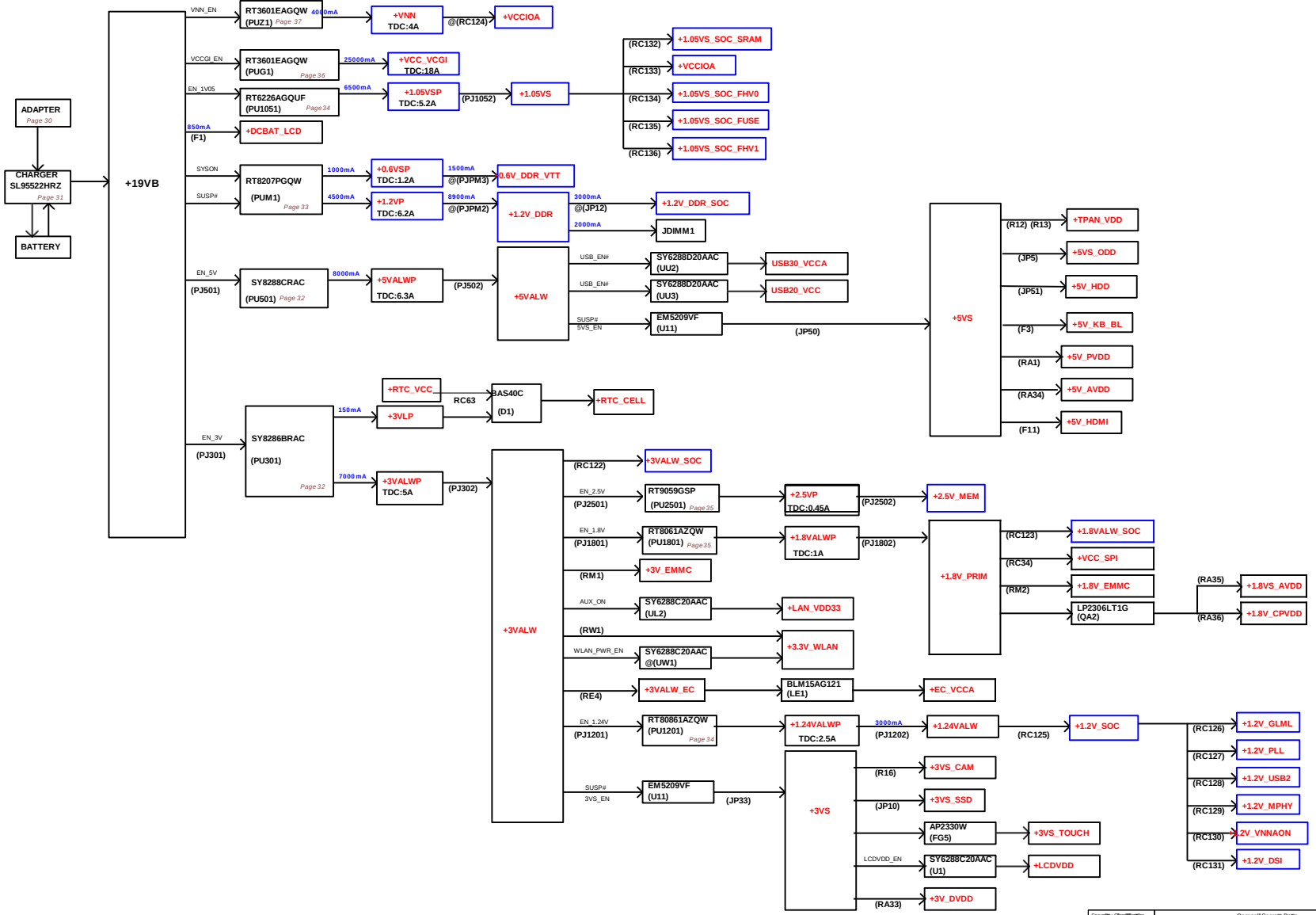
MODEL NAME: *Power Sequence Block Diagram*
PCB NAME:
REVISION: *0.2*
DATE: *2018/01/29*



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/11/10	Deciphered Date	2018/01/25
Title: P05-Power Sequence Block Diagram			
Size: Custom	Document Number: LA-G094PR10		Rev: 1.0
Date: Thursday, November 08, 2018		Sheet 5 of 39	

MODEL NAME: *Power Rail Block Diagram*
PCB NAME:
REVISION:
DATE: *2018/01/22*

Eletro-X



Security Classification	Compall Secretti Datta		Compal Electronics, Inc.
Issued Date	2014/11/30	Deciphered Date	2018/01/05	Title: P04-Power Rail
Size: Document Number:			Rev: 1.0
Date: Thursday, November 08, 2018			Sheet 1 of 39

Voltage Rails

Voltage	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.24VALW	+1.2 v Always power rail(SOC L2 , I/O Logic and PLLs)	ON	ON	ON
+1.8V_PRIM	+1.8v Always power rail(SOC all GPIOs)	ON	ON	ON
+3VALW	+3.3v Always power rail(SOC GPIO , I/O Logic ,USB2 PHY)	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.2V	+1.2V power rail for DDR4	ON	ON	ON
+VCC_VCGI	CPU , GFX and ISP logic voltage for SOC	ON	ON	OFF
+VNN	non-Core Logic voltage for SOC	ON	OFF	OFF
+0.6V_DDR_VTT	+0.6V power rail for DDR4 Terminator	ON	OFF	OFF
+1.05VS	+1.05v system power rail(SDRAM and I/O Logic)	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

BOM Option Table

BTO Item	BOM Structure
Unpop	@/@RF@
Connector	CONN@
XDP (Debug Port)	XDP@
EMI requirement	EMI@
EMI requirement unpop	@EMI@
ESD requirement	ESD@
ESD requirement unpop	@ESD@
Board ID	EC@
N3000/V3000	N3@/V3@
CNVI	CNVI@
Free fall sensor	FFS@
lan 10/100	100@
lan giga	1000@
lan compoent	Lan@
lan EMI compoent	Lan@EMI@
ESPI for EC	ESPI@
LPC for EC	LPC@
TP_WAKE	TP_WAKE/NTP_WAKE
eMMC	MMC@

Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF

BOARD ID Table

Board ID	
0	GLK EVT
1	GLK DVT1
2	GLK DVT2
3	GLK pilot
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

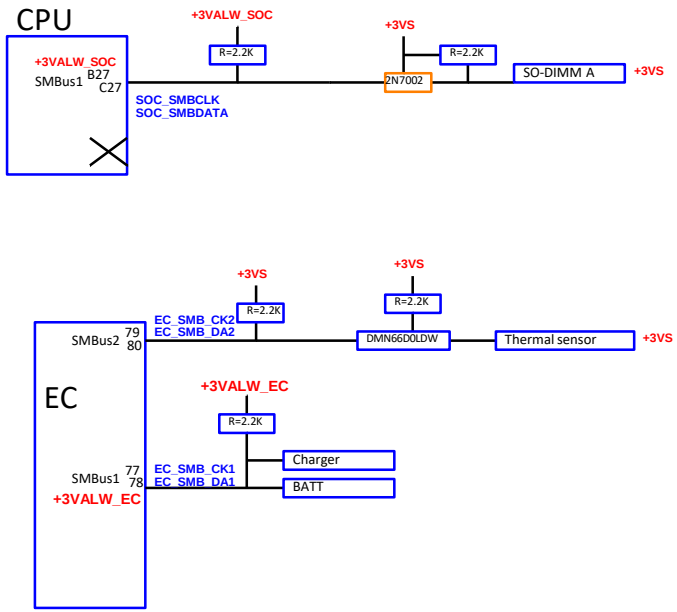
EC SM Bus2 address

Device	Address

SOC SM Bus address

Device	Address
ChannelA JDIMM1	0xA0(1010 0000).

<SMBus Routing>



HSIO Port Table

GLK BASE I/O SKU			N3V3
USB XHCI Port 0			USB3.0 Port 0
USB XHCI Port 1			USB3.0 Port 1
PCIe-0	X 2	X 4	SSD
PCIe-1			SSD
PCIe-2	X 2		SSD
PCIe-3 / USB XHCI Port 4			SSD
PCIe-4 / USB XHCI Port 3	X 2		WLAN
PCIe-5 / USB XHCI Port 2			LAN
SATA 0	X 2		HDD
SATA 1 / USB XHCI Port 5			ODD
USB Port 0			USB3.0 Port 0
USB Port 1			USB3.0 Port 1
USB Port 2			USB2.0 IO/B
USB Port 3			BT
USB Port 4			Camera
USB Port 5			Touch Screen
USB Port 6			Card Reader
USB Port 7			Fingerprint
VIDEO	eDP		LCD
	DDI0		
	DDI1		HDMI

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Title: Notes List

Document Number: LA-G094PR10 | Rev: 1.0

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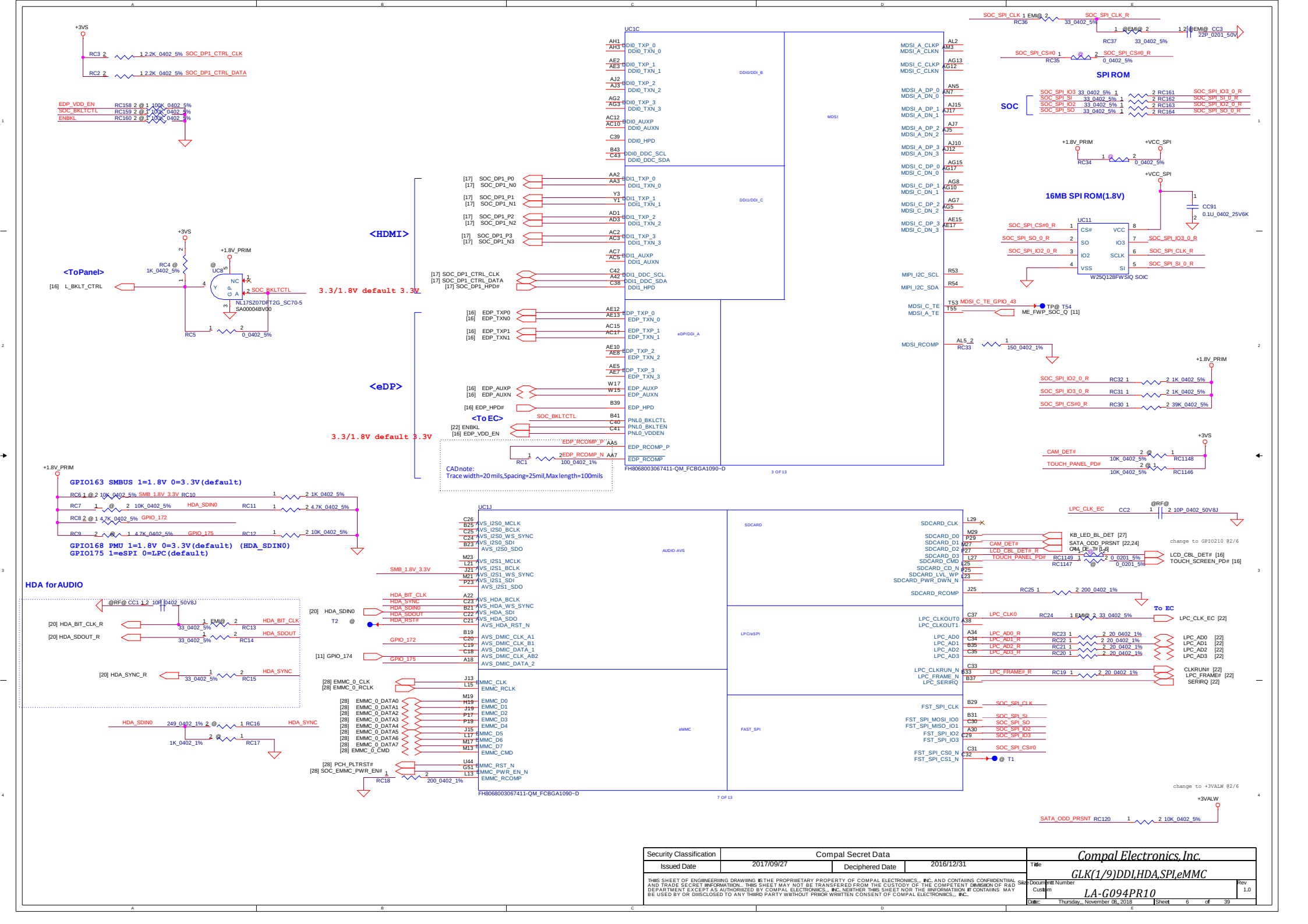
Date: Thursday, November08, 2018 | Sheet 8 of 39



Security Classification	Compal Secret Data		
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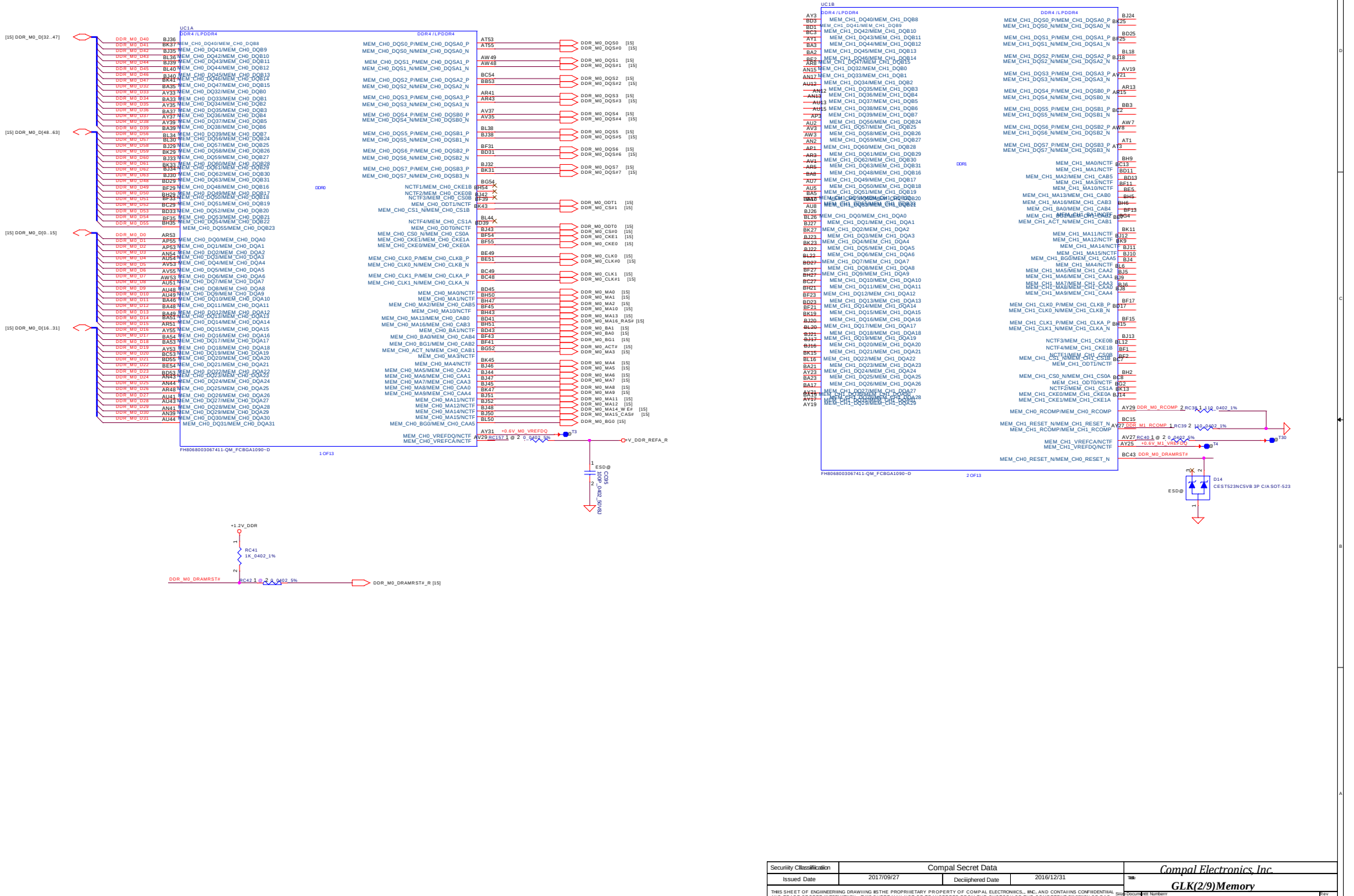
Title: GLK(1/9)DDI,HDA,SPI,eMMC

Size: Custom | Document Number: LA-G094PR10 | Rev: 1.0

Date: Thursday, November 08, 2018 | Sheet 6 of 39



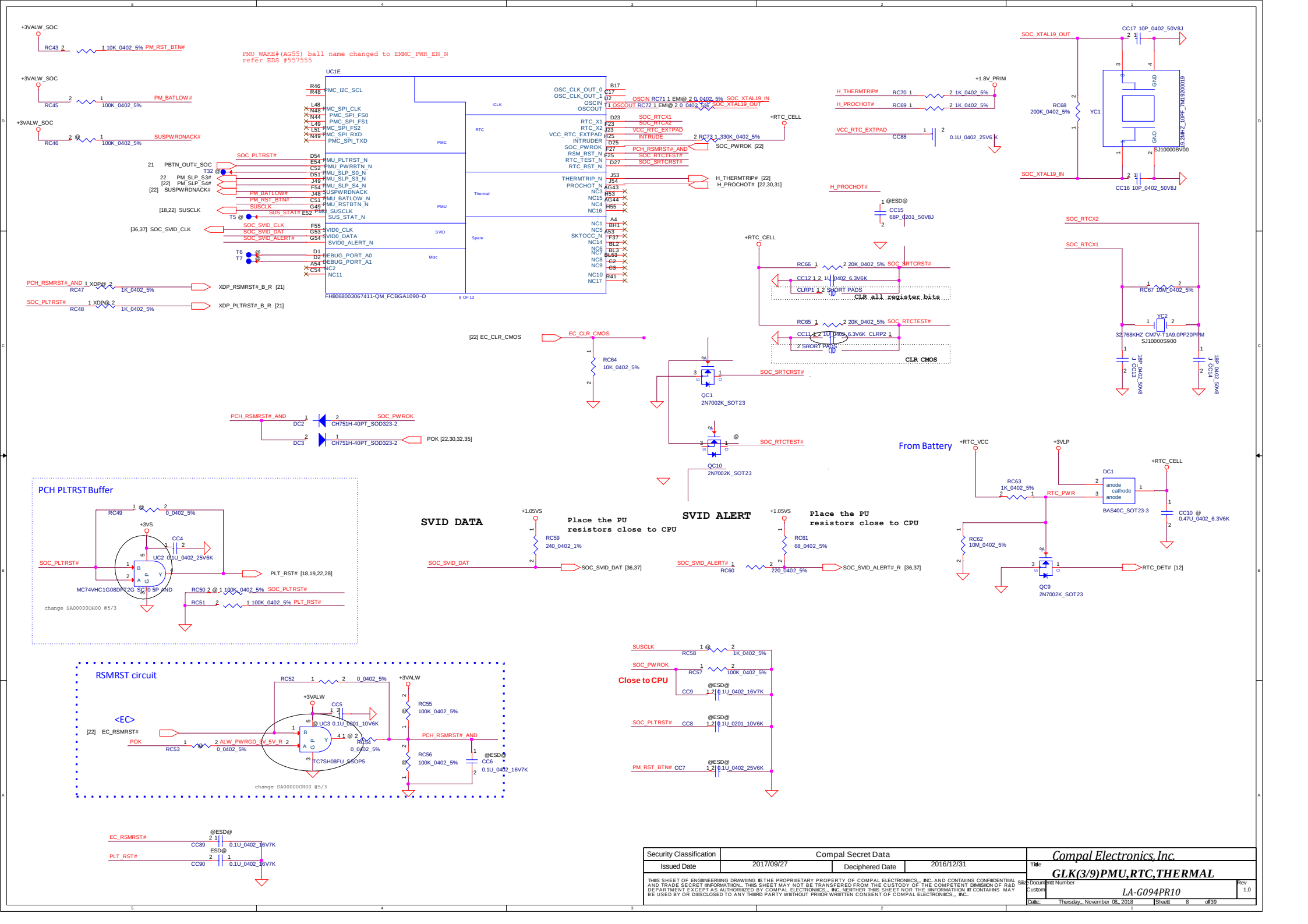
Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **GLK(2/9)Memory**

Size	Document Number	Rev
Custom	LA-G094PR10	1.0

Date: Thursday, November 08, 2018 Sheet 7 of 39



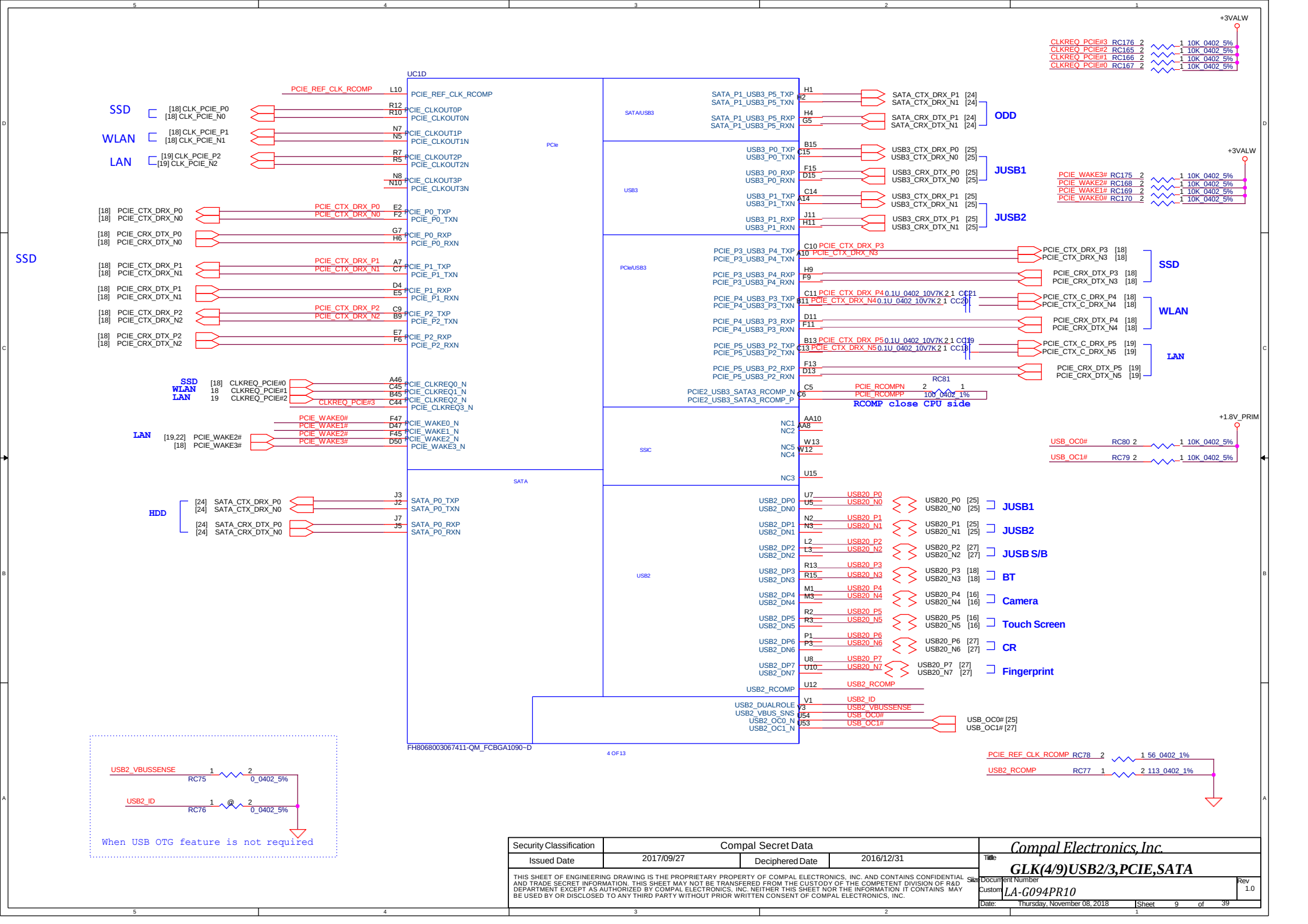
Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: GLK(3/9)PMU,RTC,THERMAL

Size	Document Number	Rev
Custom	LA-G094PR10	1.0

Date: Thursday, November 08, 2018 Sheet 8 of 39



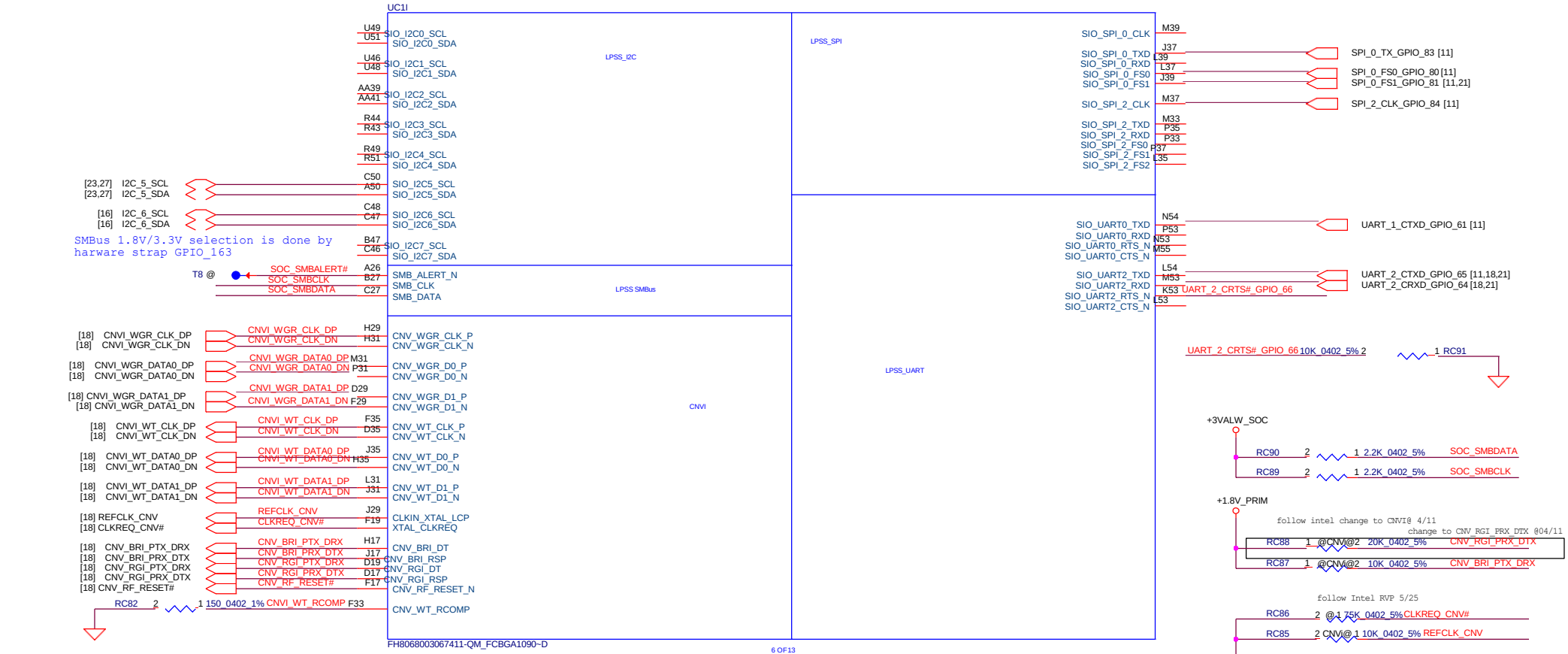
Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2016/12/31

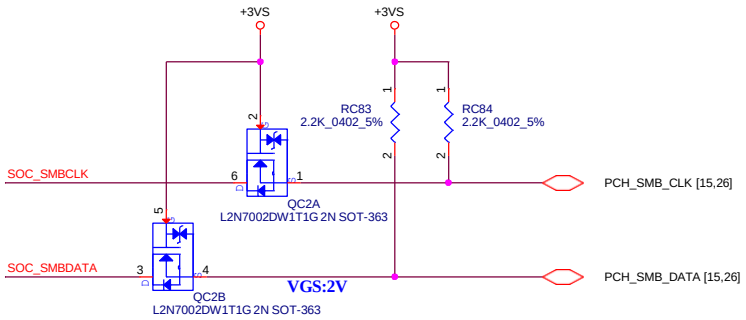
Compal Electronics, Inc.

Title: GLK(4/9)USB2/3,PCIE,SATA

Size: Custom | Document Number: LA-G094PR10 | Rev: 1.0

Date: Thursday, November 08, 2018 | Sheet 9 of 39





Notice:
SIO_EXT_SCI#, (20K PD)
SIO_EXT_SMI#, (20K PD)
SIO_EXT_WAKE# (20K PU)
is Opendrain

Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2016/12/31

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Title: GLK(5/9)I2C,SMB,CNVi

Size: Custom | Document Number: LA-G094PR10 | Rev: 1.0

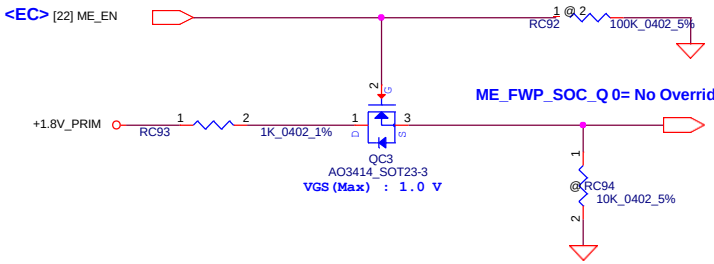
Date: Thursday, November 08, 2018 | Sheet 10 of 39

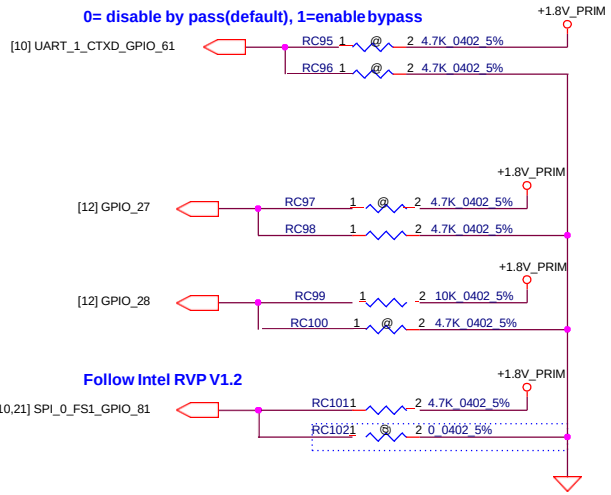
GPIO_86	SIO_SPI_2_FS1	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_87	SIO_SPI_2_FS2	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_89	SIO_SPI_2_TXD	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_159	AVS_I2S0_SDI	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_163	AVS_I2S1_WS_SY NC	SMBus 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_164	AVS_I2S1_SDI	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_168	AVS_HDA_SDI	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_172	AVS_M_CLK_B1	SMBus No Re-Boot	20K PD	1 = Enable 0 = Disable (default) **Note:** Platforms should strap this LOW. Functionality is handled by the PMC.
GPIO_174	AVS_M_CLK_AB2	VDD2 1.24V vs. 1.20V select	20K PD	1=VDD2 is 1.24V; 0=VDD2 is 1.20V (default)

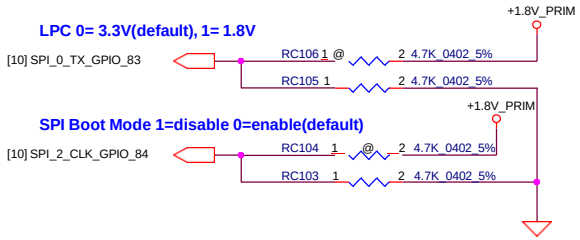
GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_27	GPIO_27	Allow eMMC as a boot source	20K PU	1=enable (default); 0=disable; If platform is using SPI as the boot device, then provide a pull-down for this strap to disable eMMC
GPIO_28	GPIO_28	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable **Note:** If platform is using eMMC as boot device, then provide a pull down for this strap to disable SPI.
GPIO_42	MDSI_A_TE	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override **Note:** This strap enables the platform to override security features in the SPI.
GPIO_43	MDSI_C_TE	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_44	USB2_OC0_N	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_45	USB2_OC1_N	Top swap override	20K PD	1 = Enable 0 = Disable (default) **Note:** Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_61	SIO_UART0_TXD	Enable TXE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) **Note:** This strap tells TXE 3.0 to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of TXE3.0 before the first patch point this strap enabled the platform tell TXE 3.0 to bypass the ROM causing the issue and go to the patch space instead.
GPIO_62	SIO_UART0_RTS_N	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

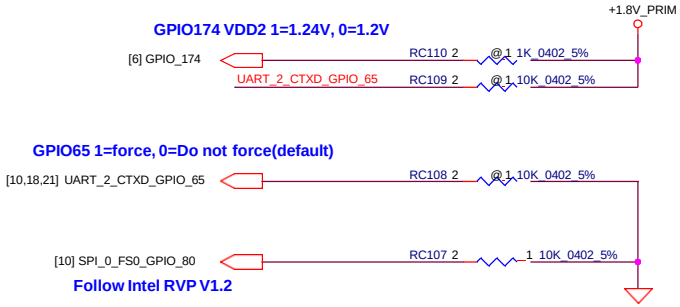
GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_65	SIO_UART2_TXD	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) ***Notes:*** 1. DnX: Download and Execute 2. This strap is a recovery strap for corrupted FW image. This strap will force TXE3.0 to execute a "Download and Execute" (DnX) flow, where it would download a new firmware image from a recovery host, over USB, and overwrite the image in the storage media.TXE can do it for BIOS part of FW, but if TXE FW itself is corrupted we need this strap.
GPIO_66	SIO_UART2_RTS_N	LPC boot BIOS strap	20K PD	1=boot from LPC; 0=do not boot from LPC (default) **Note:** The board should strap this low and do not use otherwise
GPIO_79	SIO_SPI_0_CLK	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_80	SIO_SPI_0_FS0	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_81	SIO_SPI_0_FS1	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_83	SIO_SPI_0_TXD	LPC 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_84	SIO_SPI_2_CLK	Allow SPI as a boot source	20K PU	1=disable 0=enable (default)
GPIO_85	SIO_SPI_2_FS0	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_86	SIO_SPI_2_FS1	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_175	AVS_M_DATA_2	eSPI vs. LPC	20K PD	1=eSPI mode; 0=LPC mode (default) Note: The default for A0 will be eSPI due to a bug on LPC.
GPIO_177	SMB_CLK	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_191	CNV_BRI_DT	eSPI Flash Sharing Mode	20K PD	eSPI Flash Sharing Mode: 1=slave attached flash sharing (SAFS); 0=master attached flash sharing (MAFS; default) Note: If eSPI mode is disabled (eSPI/LPC hard strap(GPIO_175) is set to select LPC) then the eSPI slave attached flash sharing strap must also be set to 0.
GPIO_192	CNV_BRI_RSP	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_193	CNV_RGI_DT	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_194	CNV_RGI_RSP	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_195	CNV_RF_RESET_N	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_196	XTAL_CLKREQ	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.









Security Classification	Compal Secret Data		
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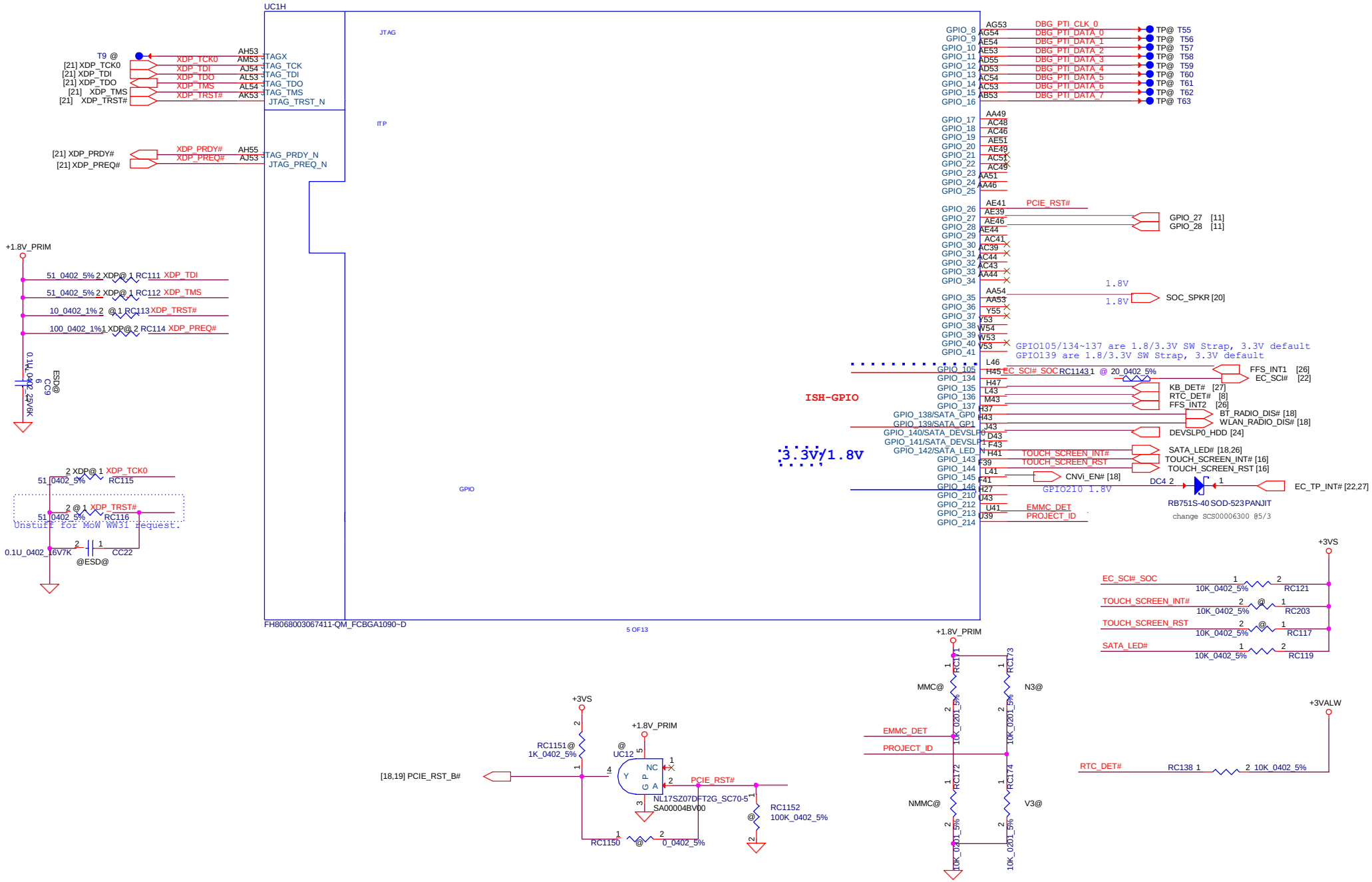
Compal Electronics, Inc.

Title: GLK(6/9)GPIO strap

Size: Custom | Document Number: LA-G094PR10 | Rev: 1.0

Date: Thursday, November 08, 2018 | Sheet 11 of 39



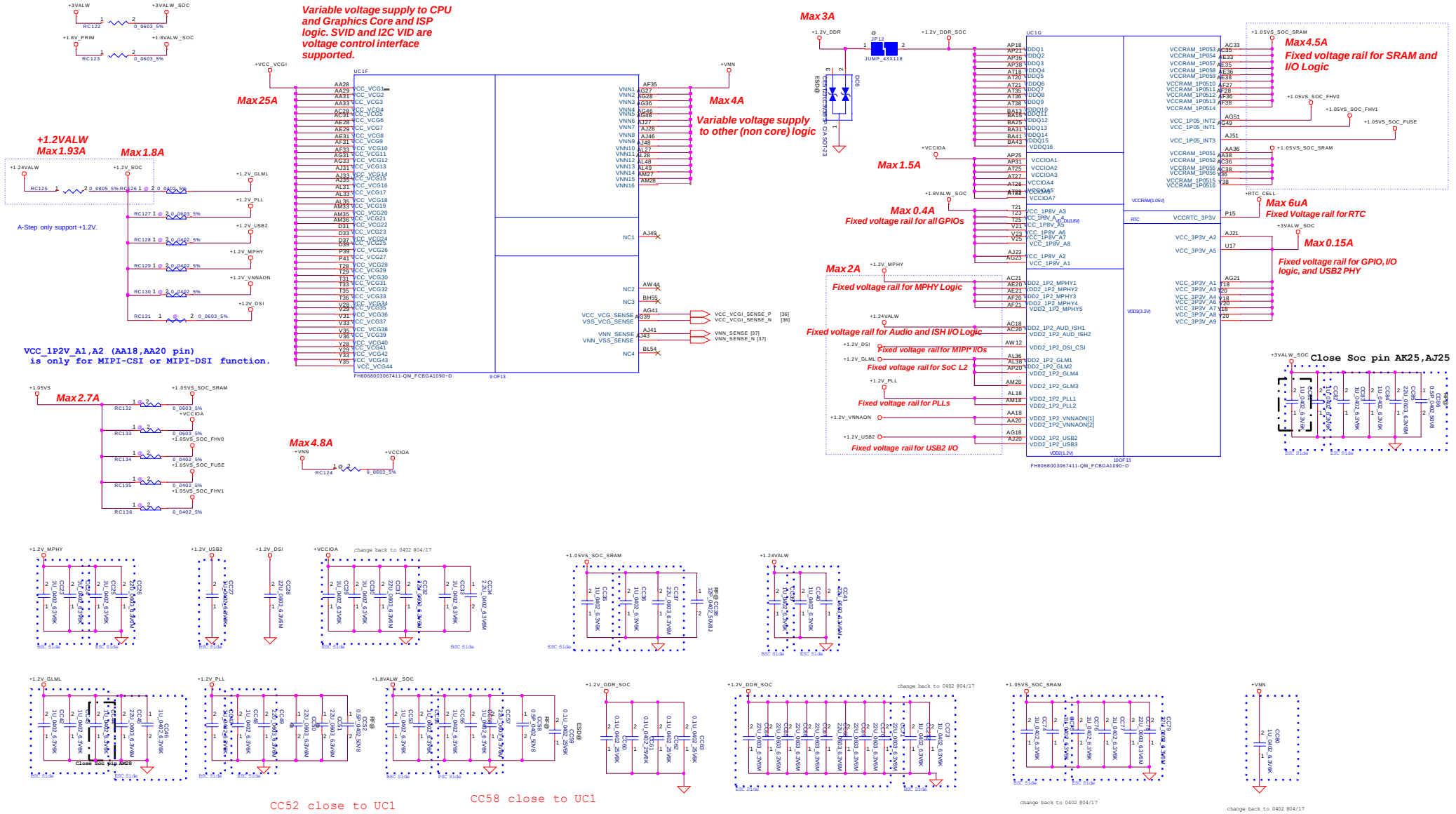
Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: GML(7/9)GPIO,JTAG

Size	Document Number	Rev
Custom	LA-G094PR10	1.0

Date: Thursday, November 08, 2018 Sheet 12 of 39



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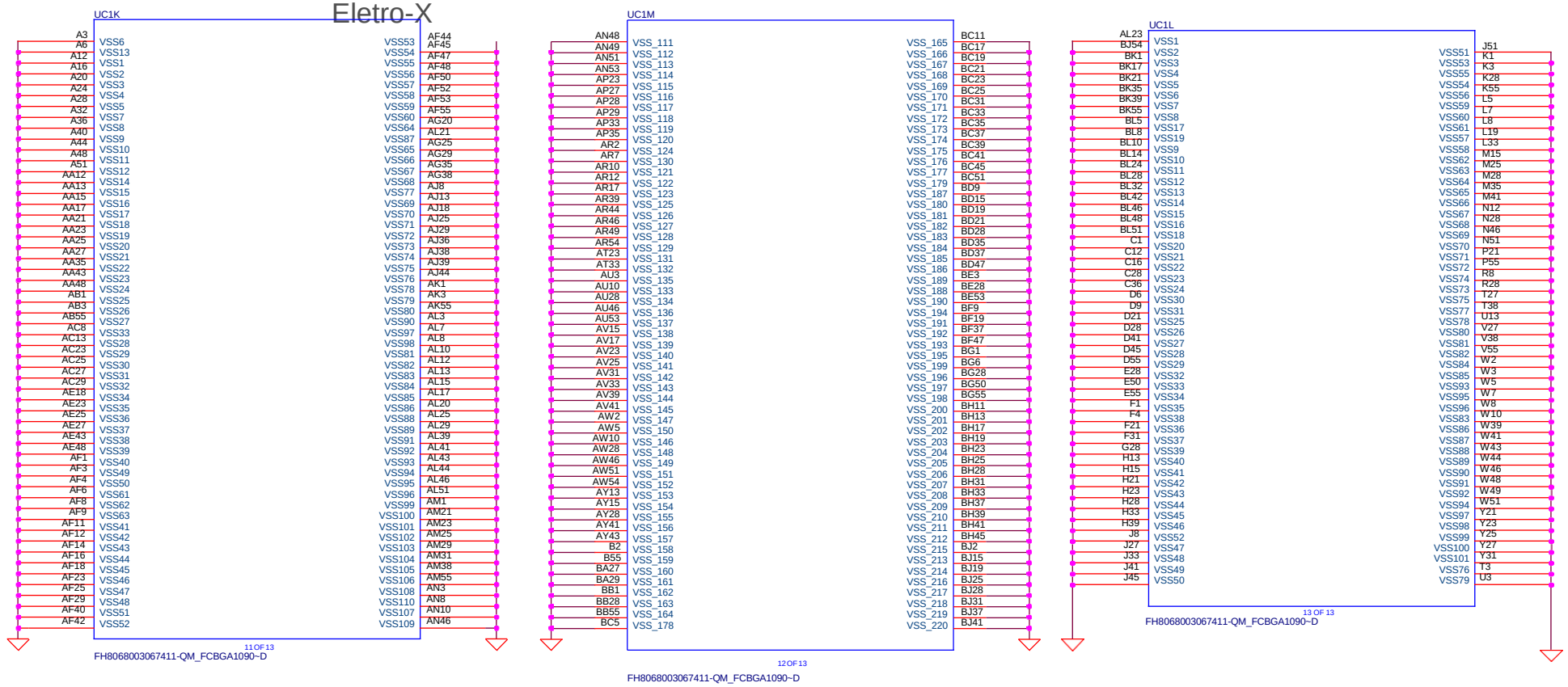
Issued Date	2017/09/27	Deciphered Date	2016/12/31
			GLK(8/9)Power
			LA-G094PR10 Rev 1.0
			Date: Thursday, November 08, 2018 Sheet 13 of 39



Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **GLK(9/9)GND**

Size: Custom | Document Number: LA-G094PR10 | Rev: 1.0

Date: Thursday, November 08, 2018 | Sheet 14 of 39

Main Func = DDR

Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.258

Layout Note:
Place near JDIMM1.255

Layout Note:
Place near JDIMM1

[7] DDR_M0_D[0..63]
[7] DDR_M0_MA[0..13]
[7] DDR_M0_DQS#[0..7]
[7] DDR_M0_DQS[0..7]

+2.5V_MEM
+0.6V_DDR_VTT
+3VS
+1.2V_DDR

JDIMM1 CONN@

LOTES_ADDR0206-P001A02~D
DEREN_40-42271-26001RHF
SP07001CV0L

All VREF traces should have 10 mil trace width

add by esd require 1/17

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: DDR4 DIMMA RVS

Size: Document Number: LA-G094PR10 Rev: 1.0

Date: Thursday, November 08, 2018 Sheet 15 of 39

Main Func = LCD

INVERTER POWER

JEDP1_CONN@
ACES_51540-04001-P01
SP010029F00

+DCBAT_LCD
CAM_DET# R1 R131 2 CAM_DET# 0_0402_5%
CAM_DET# [6]
Trace width = 60mil
+LCDVDD_LCD
RF@ 82P_0402_50V8J

LCD_TST_C
DMIC_PANEL_EN_R
EDP_HPD
LCD_CBL_DET# [6]
EDP_AUXP_C
EDP_AUXN_C
EDP_TXN0_C
EDP_TXP0_C
EDP_TXN1_C
EDP_TXP1_C
TOUCH_SCREEN_INT# [12]
TOUCH_SCREEN_RST [12]
+MIC_VCC
LCD_BRIGHTNESS
BLON_OUT_C
+3VS_CAM
DMIC_DATA_EDP [20]
DMIC_CLK_EDP [20]
USB20_N4_R
USB20_P4_R
USB20_N5_R
USB20_P5_R
TS_EN
+TPAN_VDD

C2_C3_C42 0.1U_0402_16V7K
0.1U_0402_16V7K
2.2U_0603_6.3V6M

+LCDVDD_LCD +LCDVDD
R3 0_0603_5%

EE note: Never change R3 to short pad after MP

+19VB
F1 1.5A_24V_SMD1812P150TF-24
R301 0_0603_5%
850mA
+DCBAT_LCD
C4 0.1U_0603_25V7K
C5 1000P_0402_50V7K

+3VS
R5 10K_0402_5%
DBC_PANEL_EN_R
R6 0_0402_5%
DBC_EN [22]

DMIC_DATA_EDP
DMIC_CLK_EDP
ESD@ D12 CES7523NC5VB 3P C/A SOT-523
D12 place close to JEDP1

I2C Touch Screen (Reserved)

Close to JEDP1

[10] I2C_6_SDA R84 0_0201_5% USB20_N5_R
[10] I2C_6_SCL R85 0_0201_5% USB20_P5_R
+3VS
R86 4.7K_0402_5% I2C_6_SDA
R87 4.7K_0402_5% I2C_6_SCL

+3VS +1.8V_PRIM
@ RT31 100K_0402_5%
RT28 100K_0402_5%
[6] EDP_HPD#
<CPU 1.8V level>
Q5027 MESS138W-G_SOT323-3
CT14 220P_0402_50V7K
RT29 100K_0402_5%
EDP_HPD

R52171 2 100K_0402_5% BKLT_CTRL
R52181 2 100K_0402_5% BLON_OUT_C
BLON_OUT_C 100_0402_5%1 2 R302 BKLT_CTRL
LCD_BRIGHTNESS 100_0402_5%1 2 R303 LCD_TEST
LCD_TST_C 100_0402_5%1 2 R304
BKOFF# [22]
R9 1 @ 2 0_0402_5%
D3 BAT54C-7-F_SOT23-3
eDP_BKLT_CTRL
LCD_TEST
LCD_TEST [22]
EC (BIST MODE)

[6] EDP_TXN0
[6] EDP_TXP0
C6 C7 0.1U_0402_16V7K EDP_TXN0_C EDP_TXP0_C
[6] EDP_TXN1
[6] EDP_TXP1
C8 C9 0.1U_0402_16V7K EDP_TXN1_C EDP_TXP1_C
[6] EDP_AUXN
[6] EDP_AUXP
C10 C11 0.1U_0402_16V7K EDP_AUXN_C EDP_AUXP_C
Brightness
[6] L_BKLT_CTRL
R8 1 @ 2 0_0402_5% eDP_BKLT_CTRL

+3VS
R100 @ 10K_0402_5% LCD_CBL_DET#

+3VS
C17 1U_0201_6.3V_M
U1 SY6288C20AAC_SOT23-5
IN OUT GND EN OC
40mil
+LCDVDD
R57 10K_0402_5%
+3VS

[6] EDP_VDD_EN
[22] EC_ENVDD
EC (BIST MODE)
D4 BAT54C-7-F_SOT23-3
R10 100K_0402_5%
LCDVDD_EN
High Active

Main Func = CAM

EE note: Never change R16 to short pad after MP

+3VS
F5 1A_65V_T0603FF-1000TM
+3VS_CAM
C14 3.3P_0402_50V8J
C15 4.7U_0402_6.3V6M
+3VS_CAM
C48 @ 68P_0201_50V8J

+MIC_VCC
R83 2 @ 1 0_0402_5%
+3VS_CAM
C39 @ 1U_0201_6.3V6M

del npm 84/13
R17 1 @EMI@ 2 0_0402_5%
USB20_P4_R
L3_EMI@ MCM1012B900F06BP_4P
USB20_P4 [9]
USB20_N4_R
USB20_N4 [9]
D11 ESD@ AZC199-02SPR7G_SOT23-3
R18 1 @EMI@ 2 0_0402_5%

D11 place close to JEDP1

Main Func = TS

[22,26] LID_SW#
D5 RB551V-30_SOD323-2
Touch Panel
TS_EN
R19 1 33_0402_5%
TOUCH_SCREEN_PD# [6]
C16 @ 10P_0402_50V8J

USB20_P5_R
R20 1 EMI@ 2 0_0402_5%
USB20_P5 [9]
L4_@EMI@ MCM1012B900F06BP_4P
del npm 84/13
USB20_N5_R
R21 1 EMI@ 2 0_0402_5%
USB20_N5 [9]

USB20_N5_R
USB20_P5_R
DA6 @ESD@ AZC199-02SPR7G_SOT23-3

+TS_VDD_IN
+TPAN_VDD
R13 1 2 0_0603_5%
+5VS R5222 1 2 0_0603_5%
+3VS R5221 @ 1 2 0_0603_5%
@ C983 1U_0201_6.3V6M
+3VS R5220 @ 1 2 0_0402_5%
3.3V_TS_EN
@ U14 SY6288C20AAC_SOT23-5
IN OUT GND EN OC
+TPAN_VDD_OUT
R74 0_0603_5%
20 mils
+TPAN_VDD
C35 1U_0201_6.3V6M
@ R72 100K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

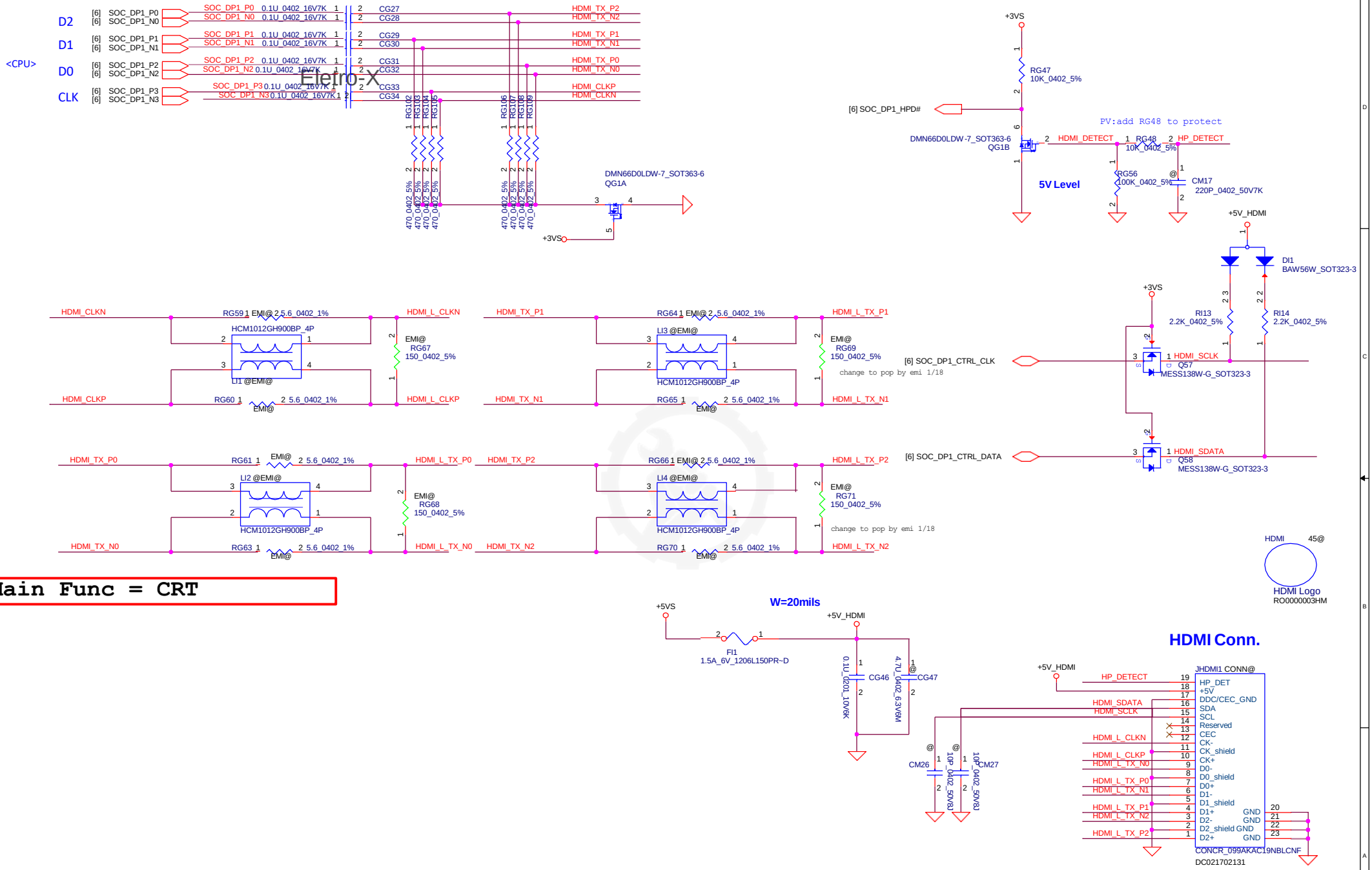
Title: LCD/Cam/MIC/T.Panel

Document Number: LA-G094PR10

Rev: 1.0

Date: Thursday, November 08, 2018

Sheet 16 of 39



Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2018/07/10

Compal Electronics, Inc.

Title: **HDMI Conn/Level shift**

Size	Document Number	Rev
	LA-G094PR10	1.0

Date: Thursday, November 08, 2018 Sheet 17 of 39

Reserved for NGFF Debug Card

E Key CONN

CNVi Rx
PCIe X1
(link to PICe Port 14)
CNVi Tx
JWLAN1
CONN@
LOTES_APCI0136-P001A
+3.3V_WLAN
+1.8V_PRIM
follow Intel RVP 5/25
change to CNVI@ @ 4/11
0201 change to 0402 @4/13

M Key CONN

NGFF Key M

JSSD1 CONN@
Key M
LCN_DAN05-67306-0103
SP070019G00
+3VS_SSD
change to Test point @04/17

High Active

SY6288C20AAC_SOT23-5
QW1
L2N7002WT1G_SC-70-3

JP10
Always Short

JUMP_43X79

Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2018/07/10

Compal Electronics, Inc.

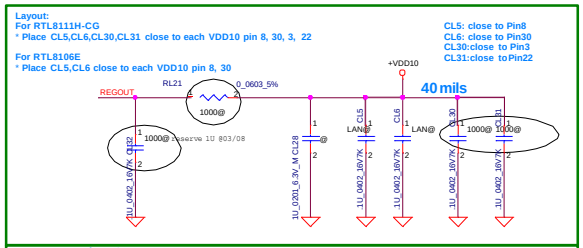
Title: WLAN-BT/SSD Conn

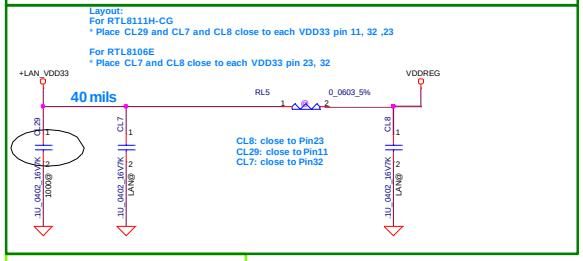
Size: Document Number: LA-G094PR10 Rev: 1.0

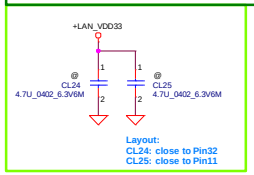
Date: Thursday, November 08, 2018 Sheet: 18 of 39

Main Func = LAN

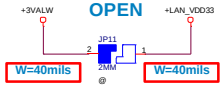
LAN Chip (10/100/1000M)

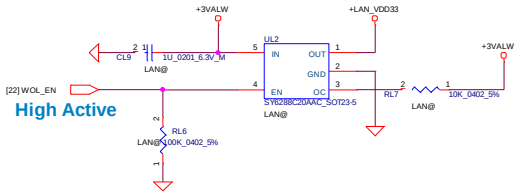






+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.

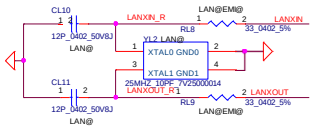


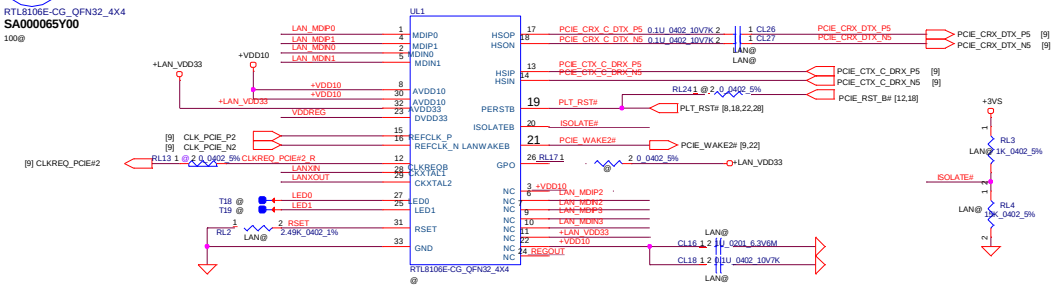


UL1 1000@
RTL8111H-CG_QFN 32P E-LAN CTRL
SA000080P00

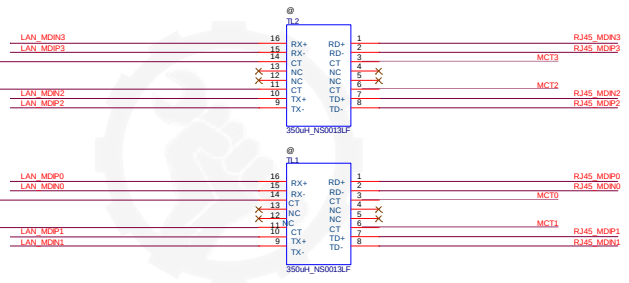
UL1
RTL8106E-CG_QFN32_4X4
SA000065Y00
100@

RTL8106E-CG
SA000065Y00
LDO mode
10/100M

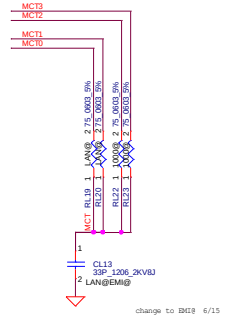




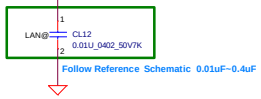
LAN TransFormer (10/100/1000M)



Layout note:
30 mil spacing between MDI differential pairs.



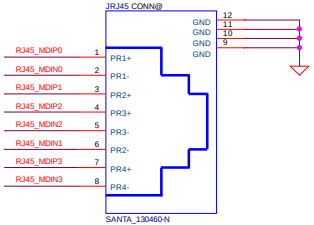
Layout note:
30 mil spacing between MDI differential pairs.



TL1
MHPC_NS681611H
SP050009800
100@

TL1
MHPC_NS681611H
SP050009800
1000@

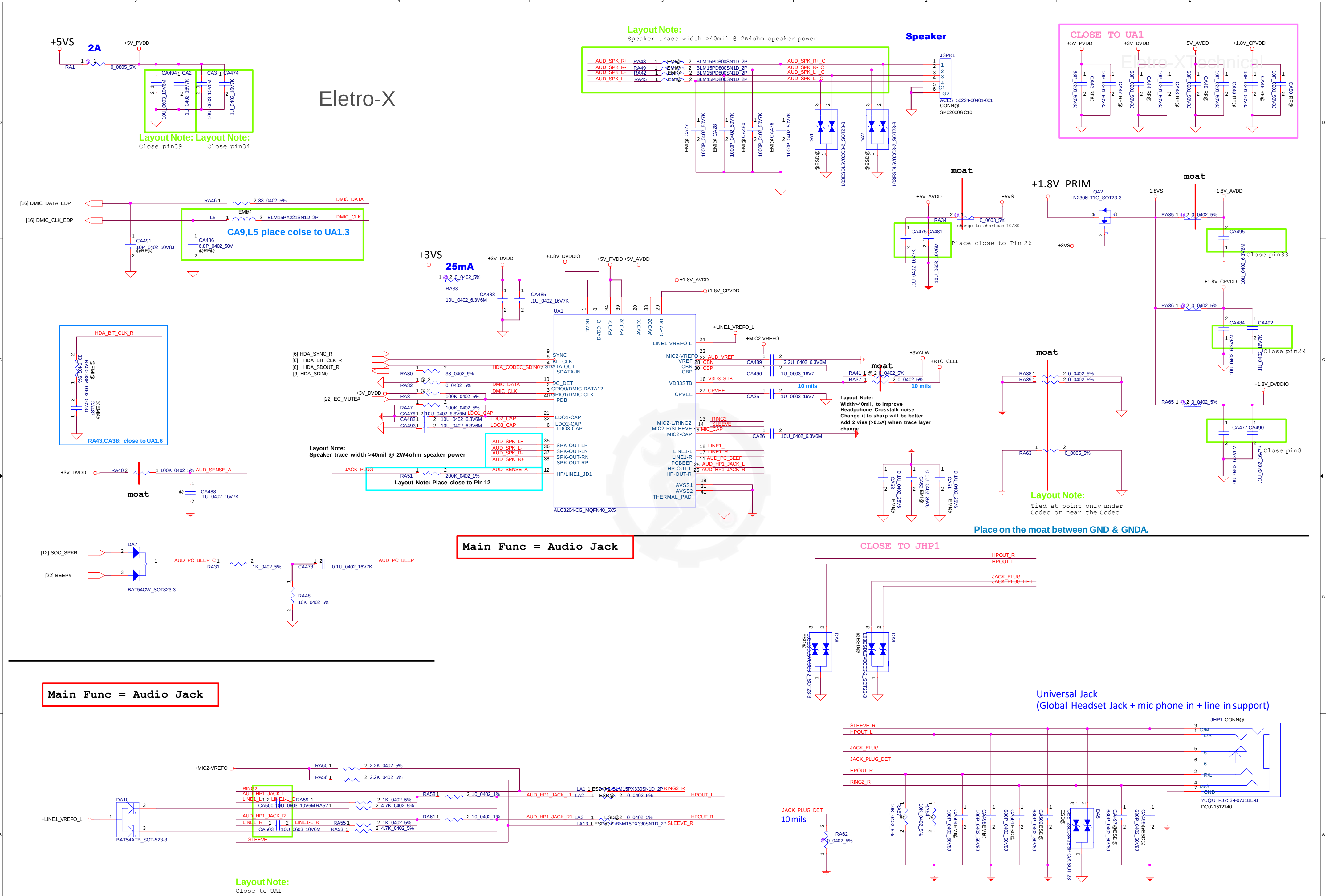
TL2
MHPC_NS681611H
SP050009800
1000@



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title	LAN(RTL8106E-CG)		
Size	Document Number		Rev
	LA-G094PR10		1.0
Date: Thursday, November 08, 2018		Sheet 19 of 39	



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Issued Date	2017/09/27	Deciphered Date 2018/07/10	Audio Codec-ALC3204/HP/MIC

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Date: Thursday, November 08, 2018 — Sheet 20 of 39

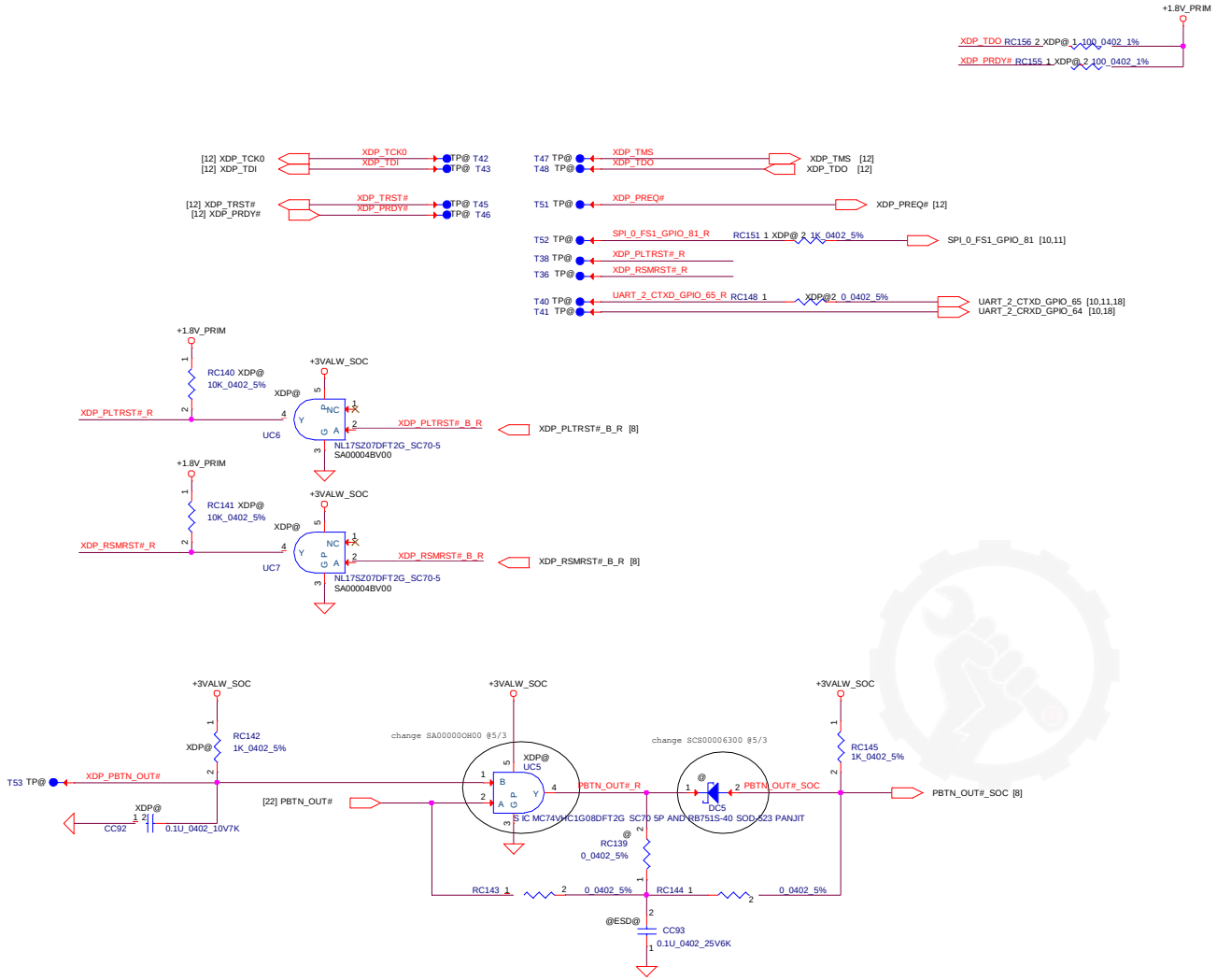

Table 167. MIPI-60 Connector Pinout

Pin	MIPI-60 Signal Name	Target Signal Name	I/O	Pin	MIPI-60 Signal Name	Target Signal Name	I/O
1	VREF_DEBUG	V1P8	NA	2	TMS/TMSC	JTAG_TMS	O
3	TCK	JTAG_TCK	O	4	TDO/EXTA	JTAG_TDO	I
5	TDI/EXTB	JTAG_TDI	O	6	nRESET	PMU_RSTBTN_N. Refer to Figure 171	O
7	RTCK/EXTC	PMU_PLTRST_N	I	8	TRST_PD	10kOhm Pull-Down to GND	NA
9	nTRST/EXTD	JTAG_TRST_N	O	10	EXTE/TRIGIN	JTAG_PREQ_N	O
11	EXTF/TRIGOUT	JTAG_PRDY_N	I	12	VREF_TRACE	V1P8	NA
13	TRC_CLK0	GPIO_0	I	14	TRC_CLK1	GPIO_18[1]	I
15	Target Presence Detect	Strapping resistor of SIO_SPI_2_TXD/ GPIO_123 Refer to Figure 220	NA	16	GND	GND	NA
17	TRC_DATA0[0]	GND	NA	18	TRC_DATA1[0]/ TRC_DATA0[20]	GPIO_19[1]	I
19	TRC_DATA0[1]	GPIO_1	I/O	20	TRC_DATA1[1]/ TRC_DATA0[21]	GPIO_20[1]	I
21	TRC_DATA0[2]	GPIO_2	I/O	22	TRC_DATA1[2]/ TRC_DATA0[22]	GPIO_21[1]	I
23	TRC_DATA0[3]	GPIO_3	I/O	24	TRC_DATA1[3]/ TRC_DATA0[23]	GPIO_22[1]	I
25	TRC_DATA0[4]	GPIO_4	I/O	26	TRC_DATA1[4]/ TRC_DATA0[24]	GPIO_23[1]	I
27	TRC_DATA0[5]	GPIO_5	I/O	28	TRC_DATA1[5]/ TRC_DATA0[25]	GPIO_24[1]	I
29	TRC_DATA0[6]	GPIO_6	I/O	30	TRC_DATA1[6]/ TRC_DATA0[26]	GPIO_25[1]	I
31	TRC_DATA0[7]	GPIO_7	I/O	32	TRC_DATA1[7]/ TRC_DATA0[27]	GPIO_26[1]	I
33	TRC_DATA0[8]	GPIO_8	I/O	34	TRC_DATA1[8]/ TRC_DATA0[28]	Connect to Pin 6 (RESET_BTN_N)	O
35	TRC_DATA0[9]	GPIO_10	I/O	36	TRC_DATA1[9]/ TRC_DATA0[29]	Strapping resistor of GP_SSP_0_FS1/ GPIO_106 (BOOT_HALT_N Strap) Refer to Figure 220	O
37	TRC_DATA3[0]/ TRC_DATA0[10]	GPIO_11	I/O	38	TRC_DATA2[0]/ TRC_DATA1[10]/ TRC_DATA0[30]	Connect to Pin 7 (PMU_PLTRST_N)	I
39	TRC_DATA3[1]/ TRC_DATA0[11]	GPIO_12	I/O	40	TRC_DATA2[1]/ TRC_DATA1[11]/ TRC_DATA0[31]	POWER_BTN_N	O
41	TRC_DATA3[2]/ TRC_DATA0[12]	GPIO_13	I/O	42	TRC_DATA2[2]/ TRC_DATA1[12]/ TRC_DATA0[32]	RSMRST_N	I
43	TRC_DATA3[3]/ TRC_DATA0[13]	GPIO_14	I/O	44	TRC_DATA2[3]/ TRC_DATA1[13]/ TRC_DATA0[33]	GPIO_28[1]	I
45	TRC_DATA3[4]/ TRC_DATA0[14]	GPIO_15	I/O	46	TRC_DATA2[4]/ TRC_DATA1[14]/ TRC_DATA0[34]	GPIO_29[1]	I
47	TRC_DATA3[5]/ TRC_DATA0[15]	GPIO_16	I/O	48	TRC_DATA2[5]/ TRC_DATA1[15]/ TRC_DATA0[35]	I2C_SCL	I/O
49	TRC_DATA3[6]/ TRC_DATA0[16]	GPIO_17	I/O	50	TRC_DATA2[6]/ TRC_DATA1[16]/ TRC_DATA0[36]	I2C_SDA	I/O
51	TRC_DATA3[7]/ TRC_DATA0[17]	No Connect	NA	52	TRC_DATA2[7]/ TRC_DATA1[17]/ TRC_DATA0[37]	GPIO_30[1]	I
53	TRC_DATA3[8]/ TRC_DATA0[18]	No Connect	NA	54	TRC_DATA2[08]/ TRC_DATA1[18]/ TRC_DATA0[38]	UART1_TXD/GPIO_43	I
55	TRC_DATA3[9]/ TRC_DATA0[19]	No Connect	NA	56	TRC_DATA2[9]/ TRC_DATA1[19]/ TRC_DATA0[39]	UART1_RXD/GPIO_42	O
57	GND	GND	NA	58	GND	GND	NA
59	TRC_CLK3	GPIO_9	I	60	TRC_CLK2	GPIO_27[1]	I

Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2016/12/31

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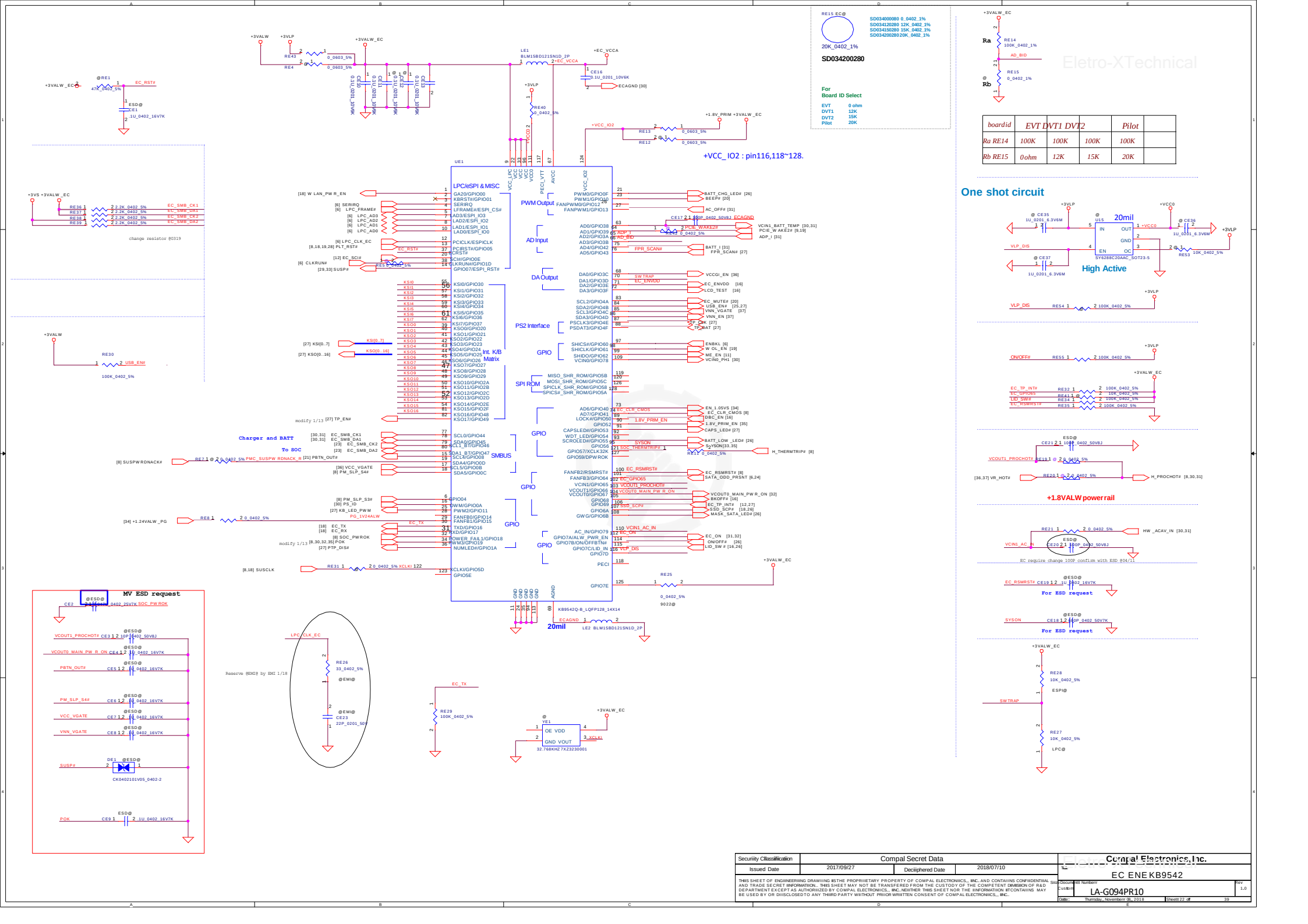
Compal Electronics Inc.

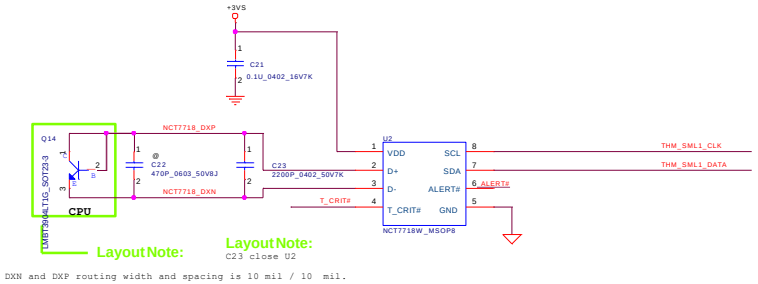
Title: ***XDP debug port***

Size	Document Number	Rev
Custom	LA-G094PR10	1.0

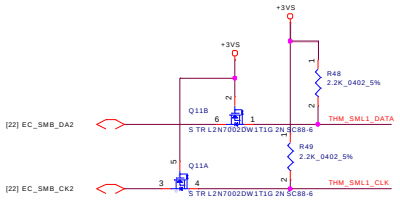
Date: Thursday, November 08, 2018 Sheet 21 of 39

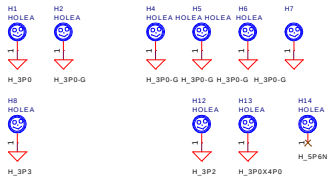

RE15 EC@
20K_0402_1%
SD034000080 0_0402_1%
SD034120280 12K_0402_1%
SD034150280 15K_0402_1%
SD034200280 20K_0402_1%
SD034200280
For
Board ID Select
EVT 0 ohm
DVT1 12K
DVT2 15K
Pilot 20K
+3VALW_EC
Ra
RE14
100K_0402_1%
AD_BID
Rb
RE15
0_0402_1%
Eletro-XTechnical
boardid
EVT DVT1 DVT2
Pilot
Ra RE14
100K
100K
100K
100K
Rb RE15
0ohm
12K
15K
20K
One shot circuit
+3VLP
+VCC0
@ CE35
1U_0201_6.3V6M
@ U15
20mil
IN
OUT
GND
EN
OC
SY6288C20AAC_SOT23-5
@ CE36
1U_0201_6.3V6M
@ CE37
1U_0201_6.3V6M
VLP_DIS
RES3
10K_0402_5%
High Active
RES4
100K_0402_5%
ON/OFF#
RES5
100K_0402_5%
EC_TP_INT#
EC_GPIO65
LID_SW#
EC_RSMRST#
RE32
RE33
RE34
RE35
10K_0402_5%
ESD@
CE21 1000P_0402_50V8J
VCOUT1_PROCHOT#
RE19 0_0402_5%
RE20 0_0402_5%
[36,37] VR_HOT#
H_PROCHOT# [8,30,31]
+1.8VALW powerrail
RE21 0_0402_5%
HW _ACAV_IN [30,31]
VCIN1_AC_IN
CE20 1000P_0402_50V8J
EC require change 100P confirm with ESD 804/11
EC_RSMRST#
CE19 1U_0402_16V7K
For ESD request
SYSON
CE18 1000P_0402_50V7K
For ESD request
SWTRAP
RE28
10K_0402_5%
ESPI@
RE27
10K_0402_5%
LPC@
+VCC_ IO2 : pin116,118~128.
UE1
LPC/eSPI & MISC
PWM Output
AD Input
DA Output
PS2 Interface
GPIO
Int. K/B Matrix
SPI ROM
SMBUS
Charger and BATT
To SOC
MV ESD request
LPC_CLK_EC
Reserve @EMI@ by EMI 1/18
RE26
33_0402_5%
@EMI@
CE23
22P_0201_50V
EC_TX
RE29
100K_0402_5%
YE1
OE VDD
GND VOUT
32.768KHZ 7X23230001
KB9542Q-B_LQFP128_14X14
20mil
LE2 BLM15BD121SN1D_2P
ECAGND
RE25
0_0402_5%
9022@
Compal Secret Data
2017/09/27
2018/07/10
Compal Electronics, Inc.
EC ENE KB9542
LA-G094PR10
1.0
Thursday, November 08, 2018
39

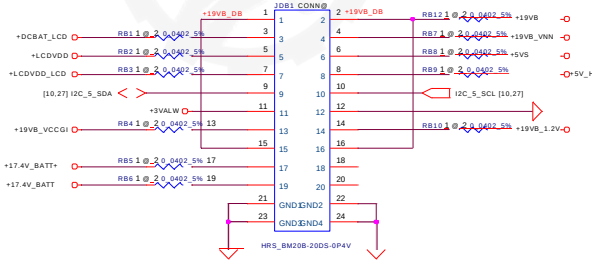
Main Func = Thermal



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125







RB1 Close to R301
RB2 Close to R3
RB3 Close to R3
RB4 Close to PJPG1
RB5 Close to PJP3
RB6 Close to PJP3

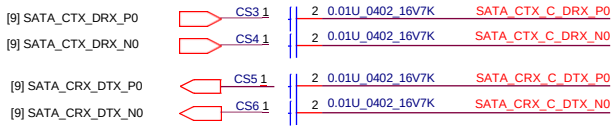
RB12 Close to PJPH02
RB7 Close to PJPZ1
RB8 Close to RS32
RB9 Close to RS32
RB10 Close to PJPM01

2	4	6	8	10	12	14	16	18	20
P1+	P1-	P2+	P2-	CLK	GND	P7-	P7+	P8-	P8+
P4+	P4-	P3+	P3-	DATA	3.3V	P6-	P6+	P5-	P5+
1	3	5	7	9	11	13	15	17	19

Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2018/07/10

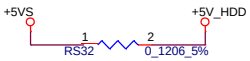
Compal Electronics, Inc.			
Title: Thermal/Screw hole			
Size:	Document Number: LA-G094PR10		Rev: 1.0
Date: Thursday, November 08, 2018		Sheet 23 of 39	

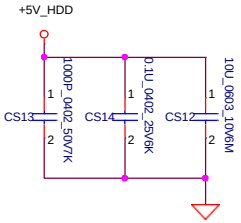
Main Func = HDD

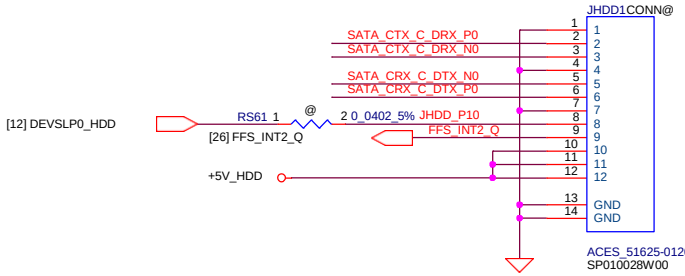


+5V_HDD Source

60 mils



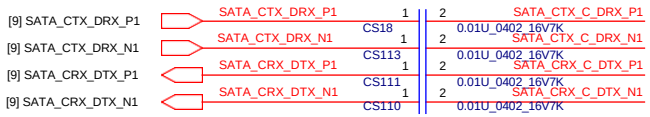




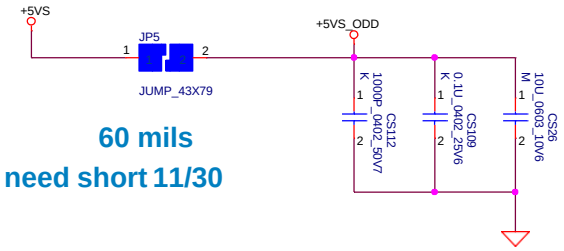
Main Func = ODD

SOC TX

SOC RX



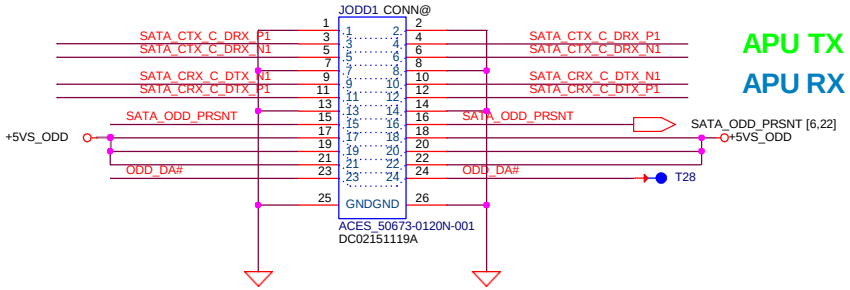
ODD Power Control



60 mils

need short 11/30

SATA ODD Connector (FFC Type)



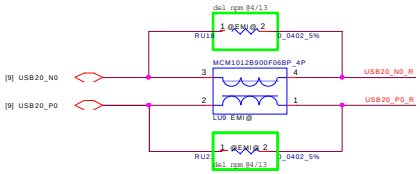
APU TX

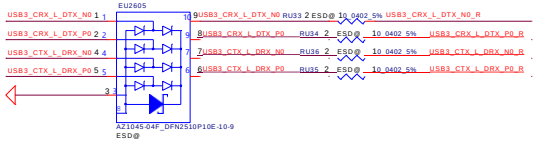
APU RX

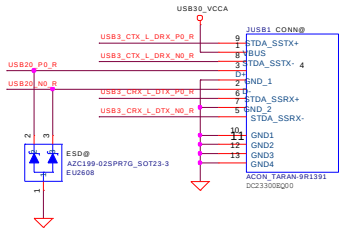
Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2018/07/10

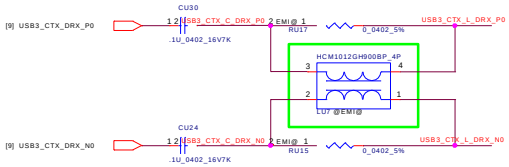
Compal Electronics, Inc.	
Title	HDD/ODD Conn
Size: Custom	Document Number: LA-G094PR10
Rev	1.0
Date: Thursday, November 08, 2018	Sheet 24 of 39

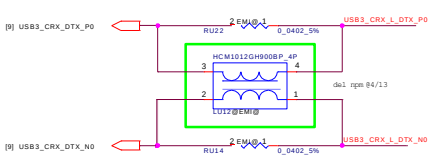
Main Func = USB3.0 Port1



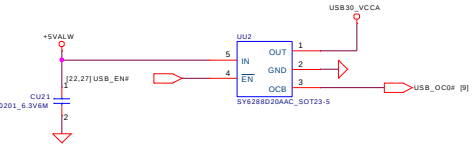


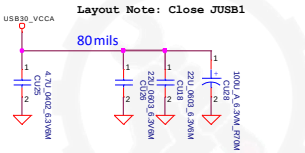


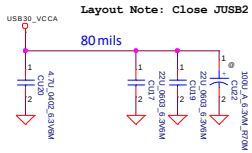




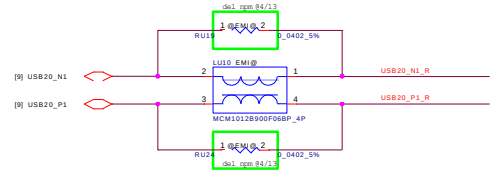
Maximum Output Current 2A

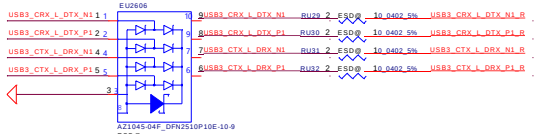


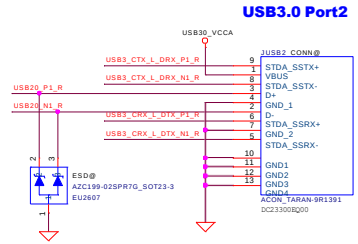


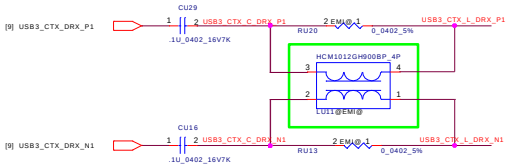


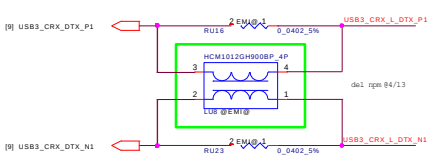
Main Func = USB3.0 Port2











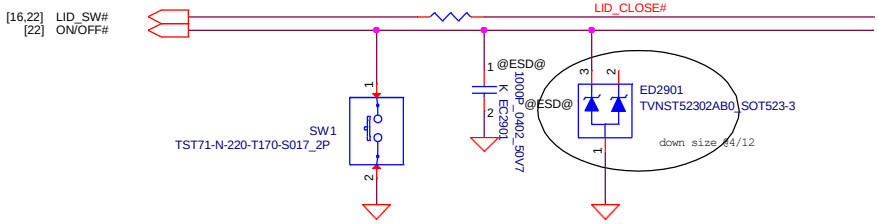
Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2018/07/10

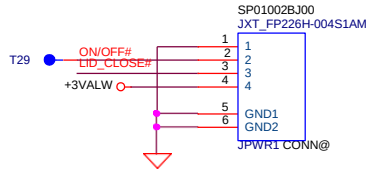
Compal Electronics, Inc.

USB 3.0 Conn

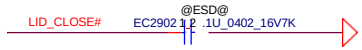
Size	Document Number	Rev
Custom	LA-G094PR10	1.0

Date: Thursday, November 08, 2018 Sheet 25 of 39





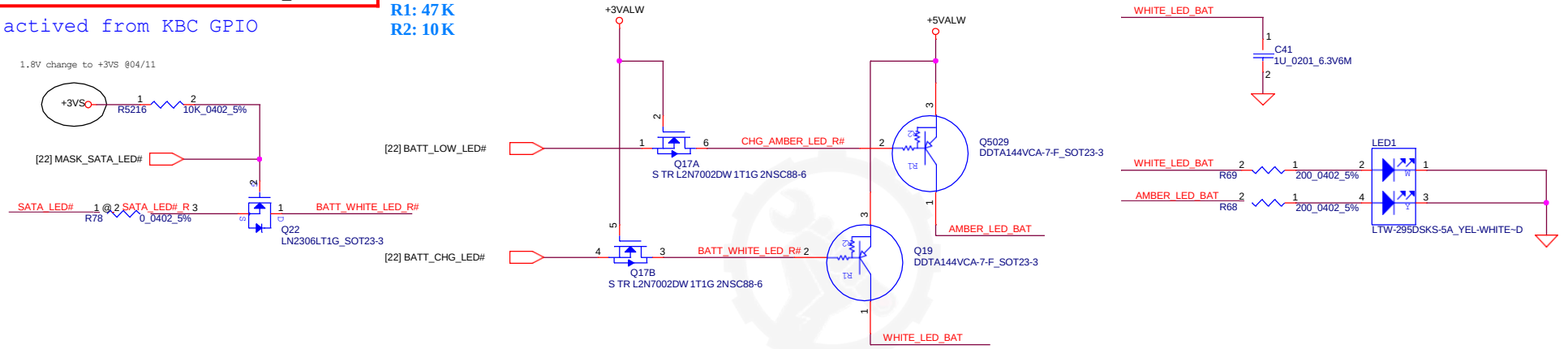
For EMI Reserved



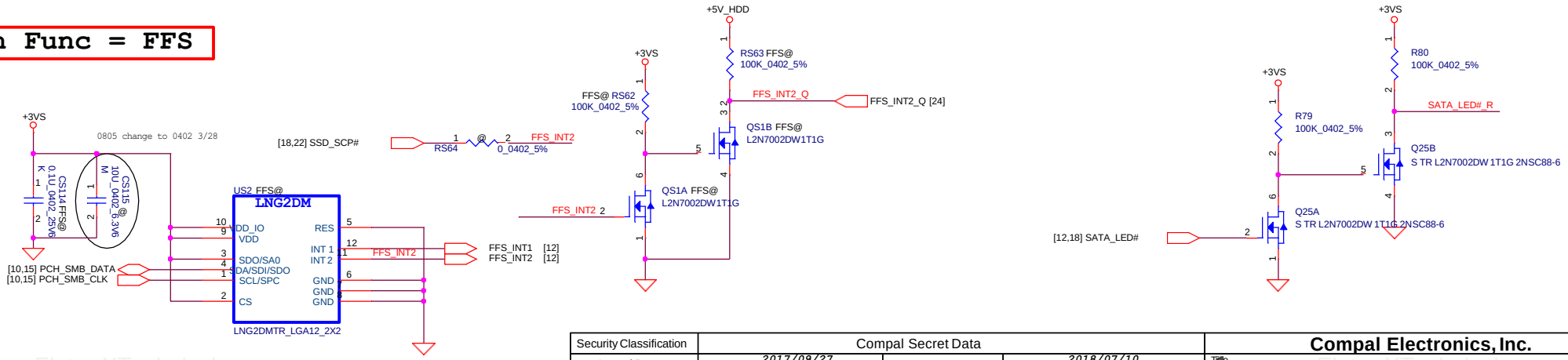
Main Func = Battery LED

Low actived from KBC GPIO

BJT
R1: 47 K
R2: 10 K



Main Func = FFS



Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2018/07/10

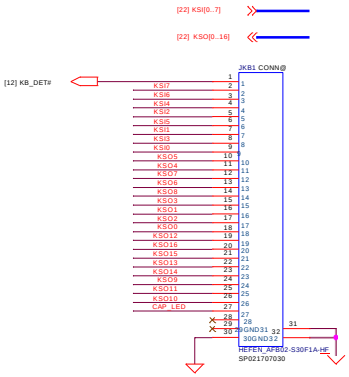
Compal Electronics, Inc.

Title: PWRBTN_LID Conn/LED/FFS

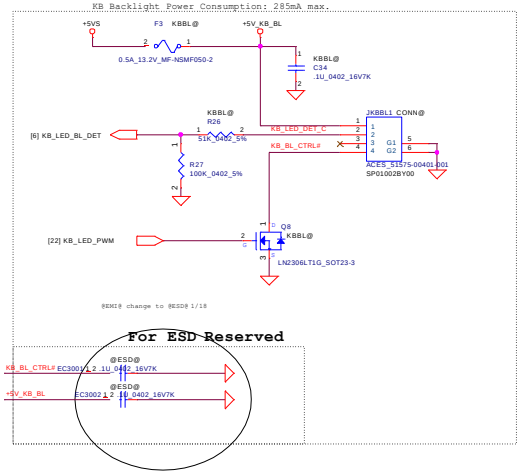
Size: Custom | Document Number: LA-G094PR10 | Rev: 1.0

Date: Thursday, November 08, 2018 | Sheet 26 of 39

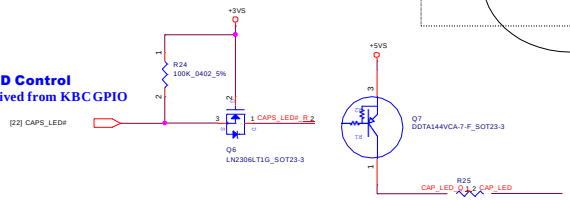
Main Func = KB



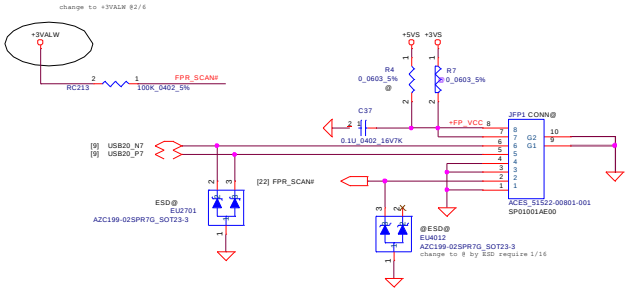
Keyboard Backlight (Reserved)



CAP LED Control
LOW actived from KBC GPIO

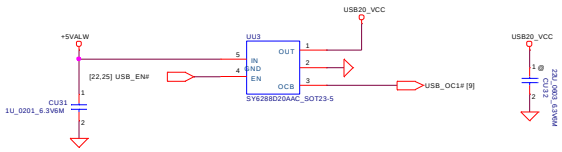


Main Func = FP

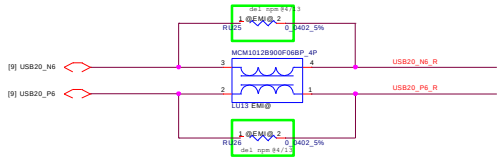


Main Func = USB2.0 + Card Reader on IO/B

SY6288D Support 2A

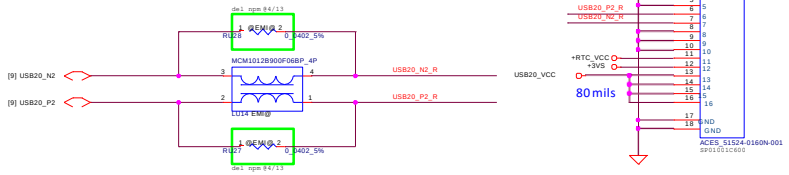


CardReader

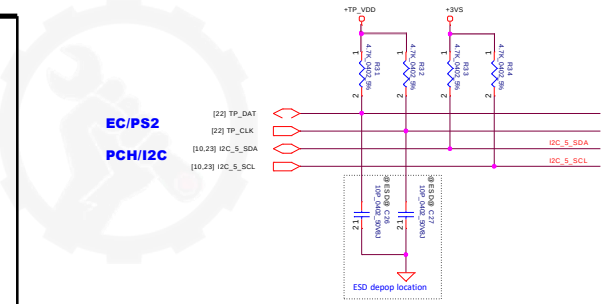


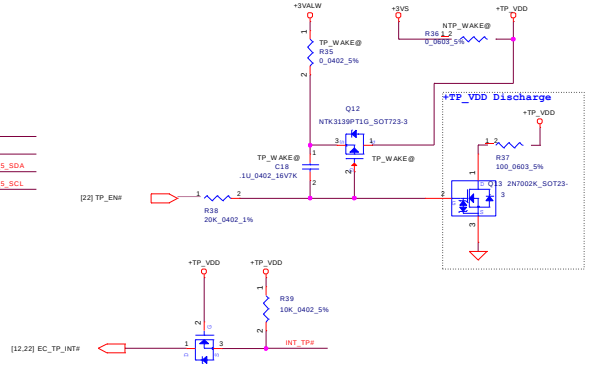
I/O Board Connector

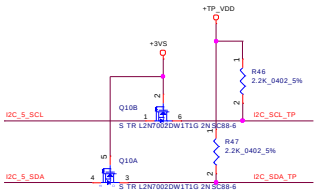
CardReader

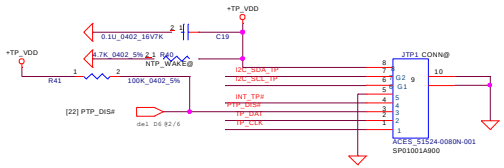


Main Func = TPAD



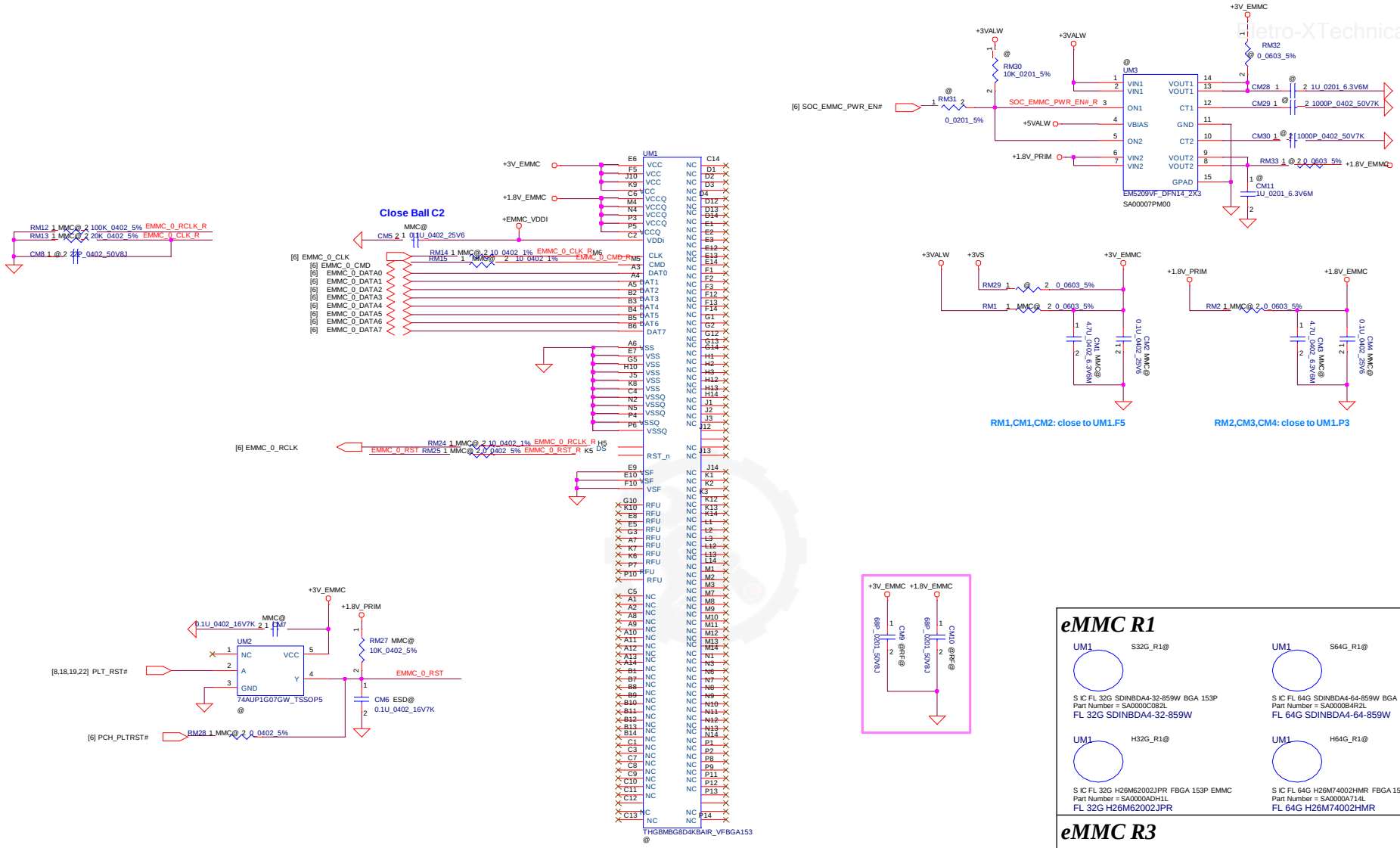






Security Classification	Compall Secret Data		Compal Electronics, Inc.
Issued Date	2017/07/ 9 7	Deciphered Date	2016/07/10
			Title: KB/KBBL/TP/FP/IO Conn
			Document Number: LA-G094PR10 Rev: 1.0
			Date: Thursday, November 08, 2018 Sheet 27 of 39

Main Func = eMMC



eMMC R1

UM1 S32G_R1@

S IC FL 32G SDINBDA4-32-859W BGA 153P
Part Number = SA0000C082L
FL 32G SDINBDA4-32-859W

UM1 S64G_R1@

S IC FL 64G SDINBDA4-64-859W BGA 153P EMMC
Part Number = SA0000B4R2L
FL 64G SDINBDA4-64-859W

UM1 H32G_R1@

S IC FL 32G H26M62002JPR FBGA 153P EMMC
Part Number = SA0000ADH1L
FL 32G H26M62002JPR

UM1 H64G_R1@

S IC FL 64G H26M74002HMR FBGA 153P
Part Number = SA0000A714L
FL 64G H26M74002HMR

eMMC R3

UM1 S32G_R3@

S IC FL 32G SDINBDA4-32-859W BGA 153P A31 !
Part Number = SA0000C083L
FL 32G SDINBDA4-32-859W

UM1 S64G_R3@

S IC FL 64G SDINBDA4-64-859W BGA 153P EMMC A31 !
Part Number = SA0000B4R3L
FL 64G SDINBDA4-64-859W

UM1 H32G_R3@

S IC FL 32G H26M62002JPR FBGA 153P A31!
Part Number = SA0000ADH2L
FL 32G H26M62002JPR

UM1 H64G_R3@

S IC FL 64G H26M74002HMR FBGA 153P A31 !
Part Number = SA0000A715L
FL 64G H26M74002HMR

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics Inc.

Title: RSV for eMMC

Size: Document Number: LA-G094PR10 Rev: 1.0

Date: Thursday, November 08, 2018 Sheet 28 of 39

VIH=1.2~5.5V
3.3V@82k/0.1uF=3.042ms
3.3V@47k/0.1uF=1.893ms

VIH=1.2~5.5V
3.3V@100k/0.1uF=3.538ms
3.3V@120k/0.1uF=4.272ms

[22,33] SUSP#

SUSP#

R926
100K_0402_5%

C979 1 2
0.1U_0402_10V7K

change to 0402 @5/3

R927
100K_0402_5%

C980 1 2
0.1U_0402_10V7K

change to 0402 @5/3

Vin : 0.8V - Vbias
V_ONH min : 1.2V
V_ONL max : 0.6V
RDS(max) : 29 mohm

+5VS/+3VS swap @02/12

+5VALW TO +5VS

+3VALW TO +3VS

+5VALW
+3VALW

5VS_ON
3VS_ON

U11
EM5209VF_SON14_2X3

VIN1
VIN1
ON1
VBIAS
ON2
VIN2
VIN2
VOUT1
VOUT1
CT1
GND
CT2
VOUT2
VOUT2
GPAD

+5VS_OUT
+3VS_OUT

C967
12 2 1 470P_0402_50V7K

C976
10 2 1 470P_0402_50V7K

C981
0.1U_0201_10V6K

C982
0.1U_0201_10V6K

@ JP50
JUMP_43X118

@ JP33
JUMP_43X118

+5VS
+3VS

C231
10U_0402_6.3V6

C225
1U_0201_6.3V_

C233
10U_0402_6.3V6

C232
1U_0201_6.3V_

C230
10U_0402_6.3V6

C234
10U_0402_6.3V6

Security Classification	Compal Secret Data		
Issued Date	2017/09/27	Deciphered Date	2018/07/10

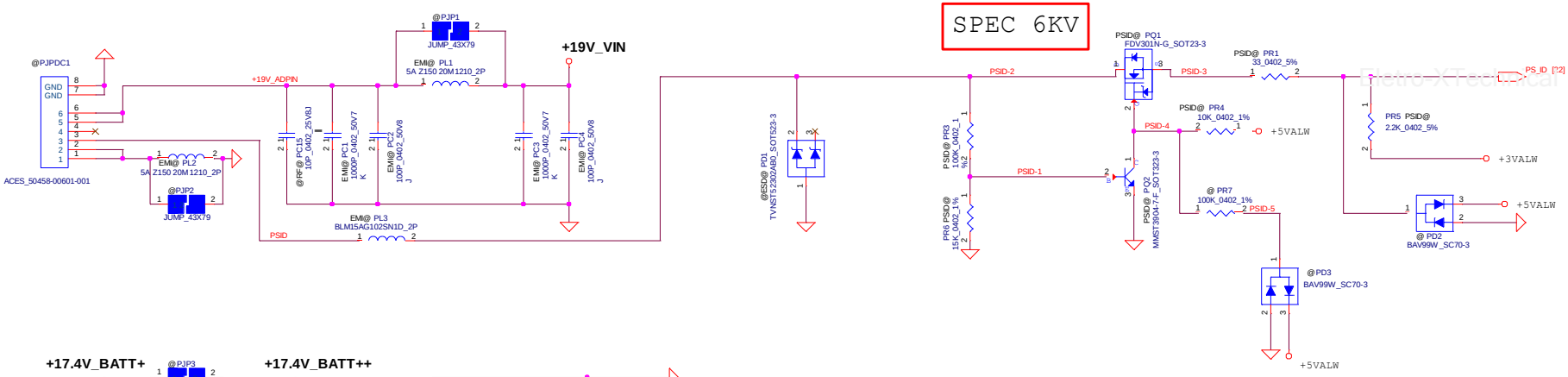
Compal Electronics, Inc.

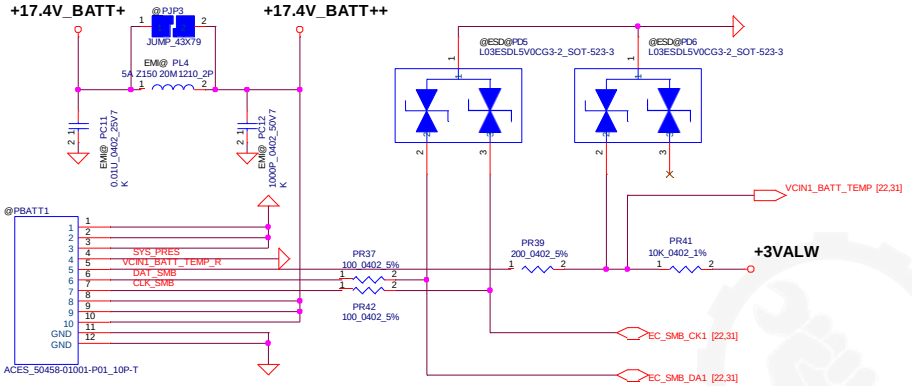
Title: DC Interface

Size: Custom | Document Number: LA-G094PR10 | Rev: 1.0

Date: Thursday, November 08, 2018 | Sheet 29 of 39

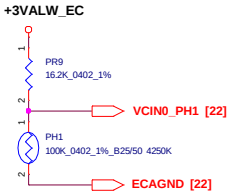
SPEC 6KV

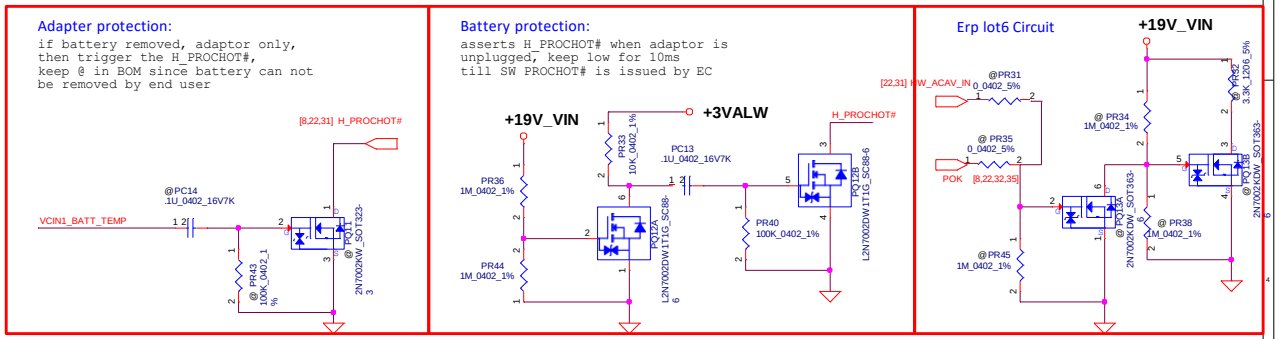




Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Batt+
PIN9 Batt+
PIN10 Batt+
SP021412220
ACES_50458-01001-P01_10P-T





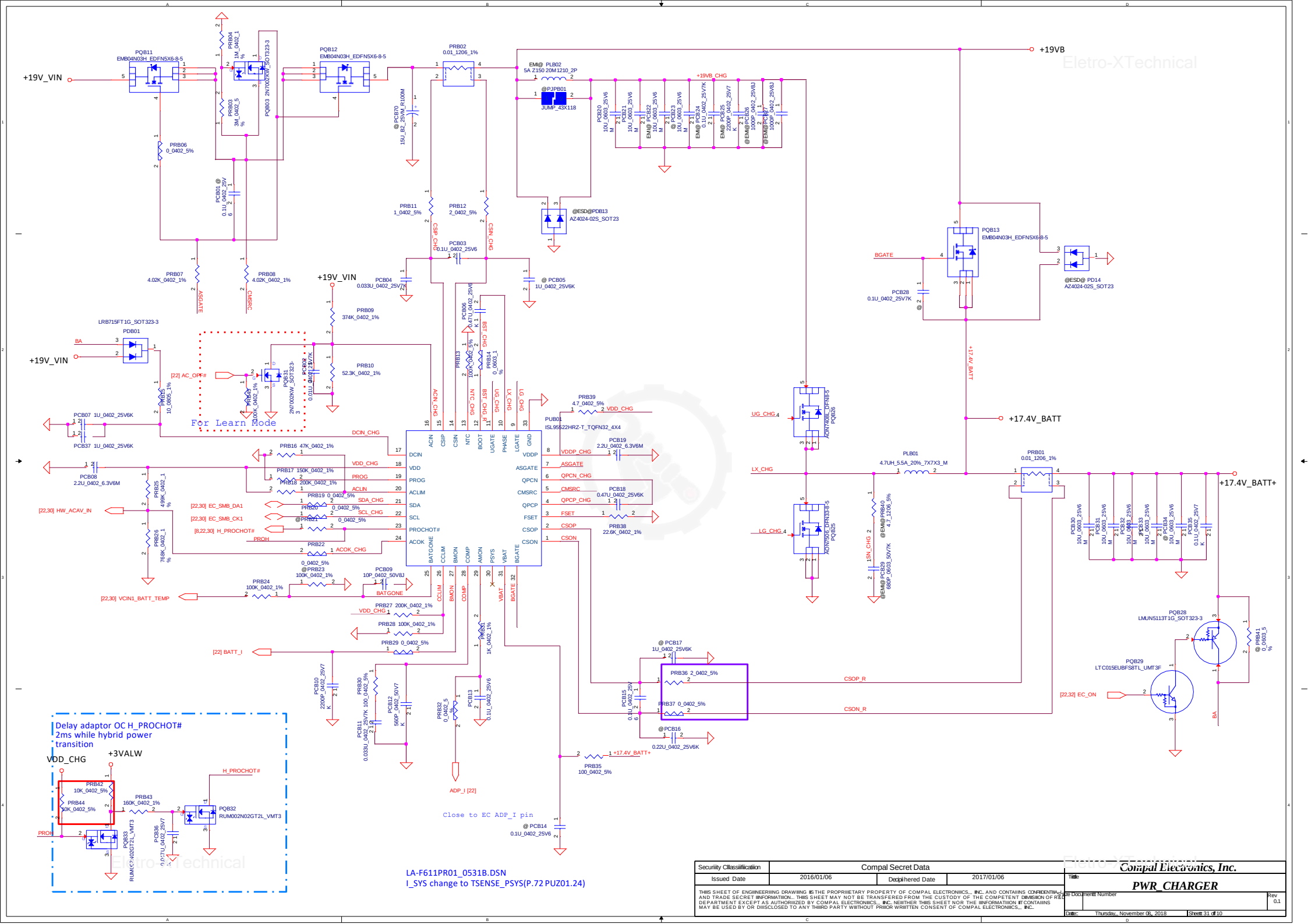
Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.

Title: PWR_DCIN/BATT CONN/OTP

Size: Document Number: Rev: X00

Date: Thursday, November 08, 2018 Sheet 30 of 10



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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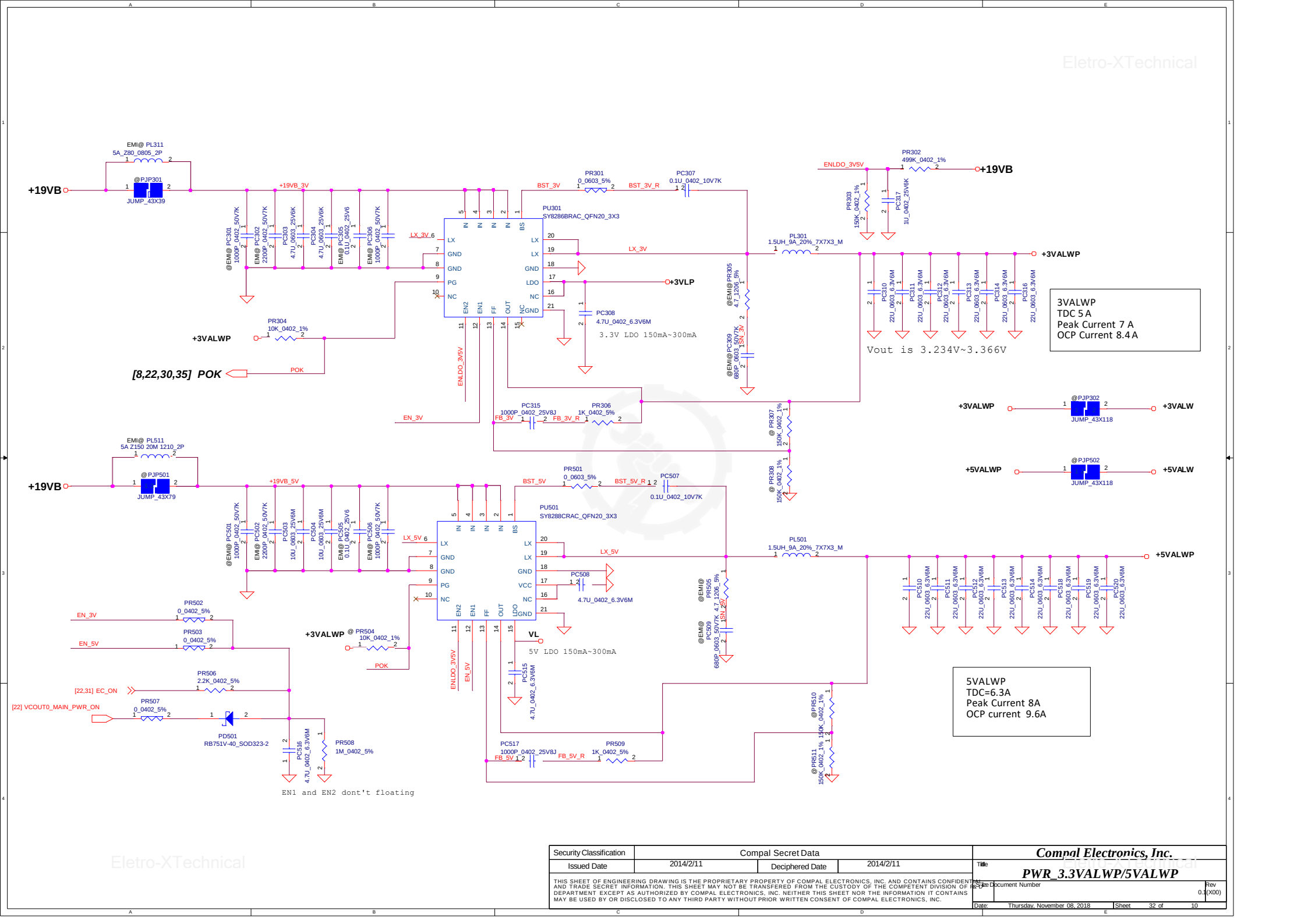
Compal Electronics, Inc.

Title: PWR_CHARGER

Size: Document Number: Rev 0.1

Date: Thursday, November 08, 2018 Sheet 31 of 110



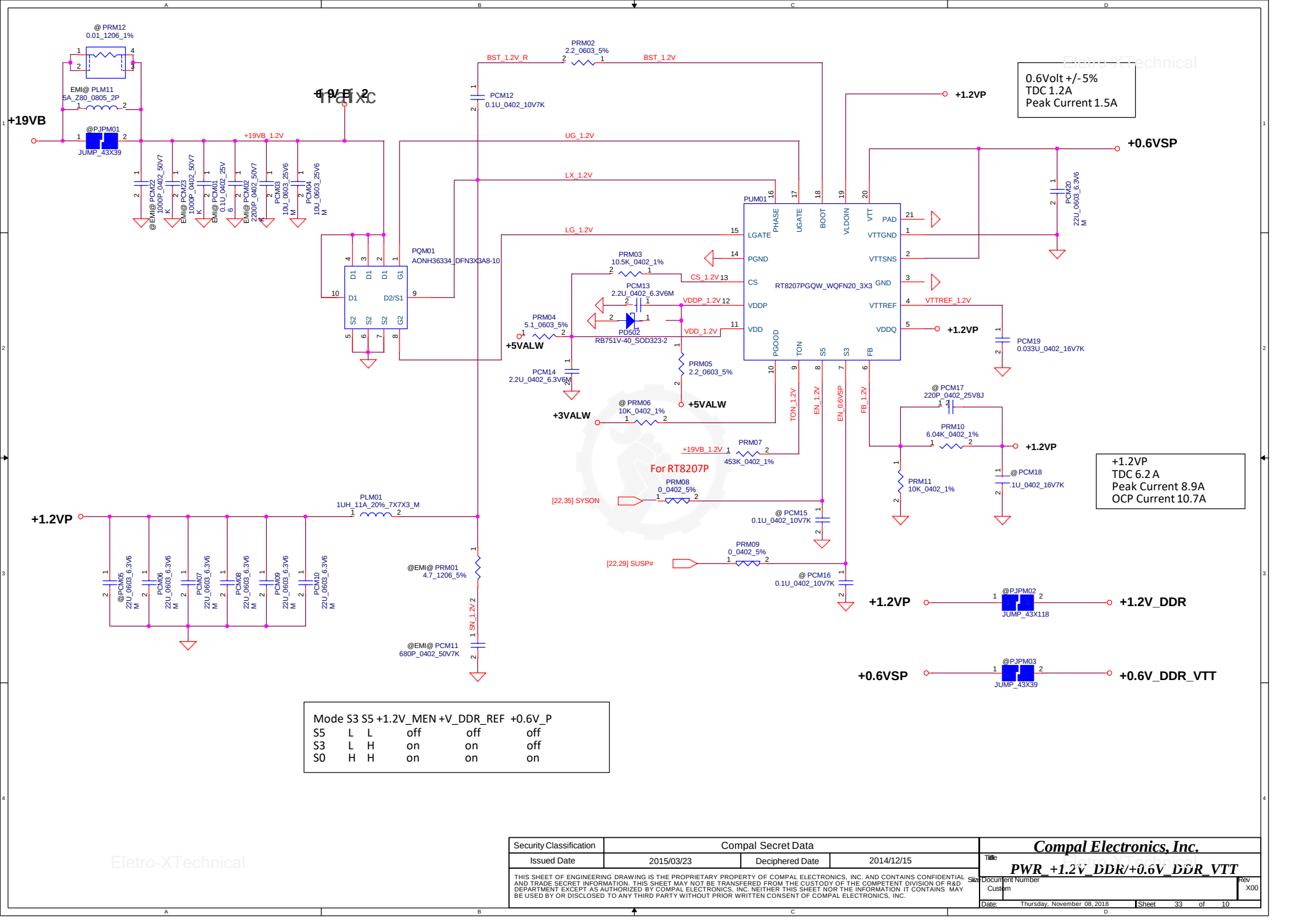
Security Classification	Compal Secret Data		
Issued Date	2014/2/11	Deciphered Date	2014/2/11

Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

Size: Document Number: Rev 0.1(X00)

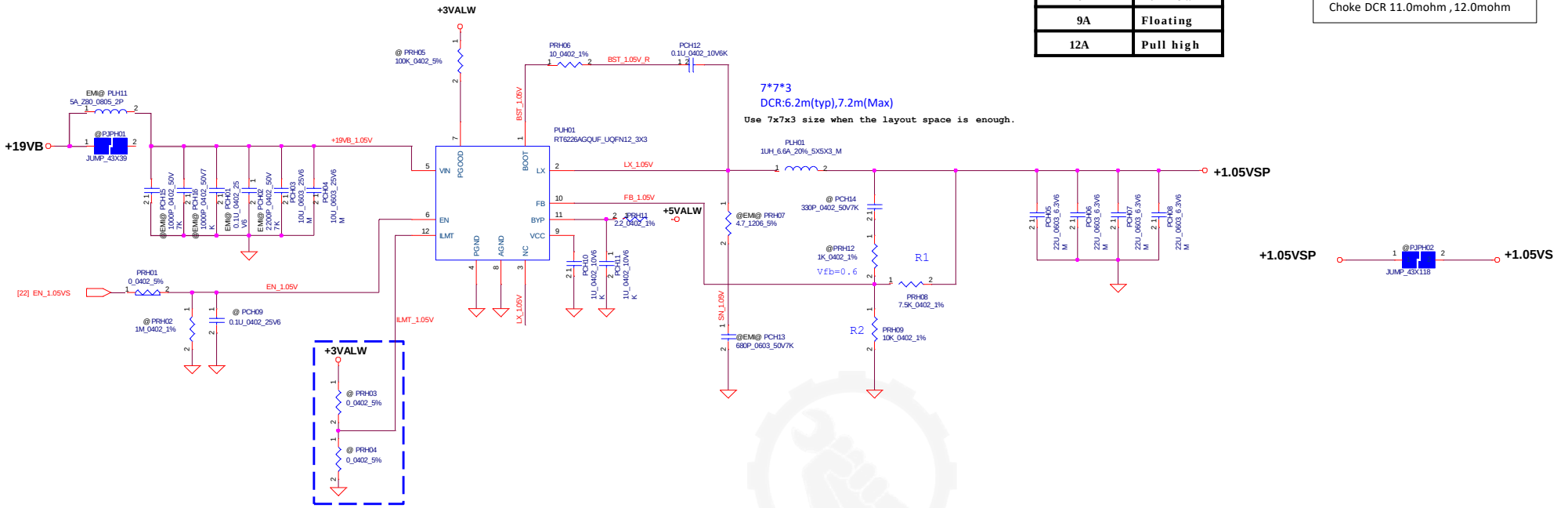
Date: Thursday, November 08, 2018 Sheet 32 of 10

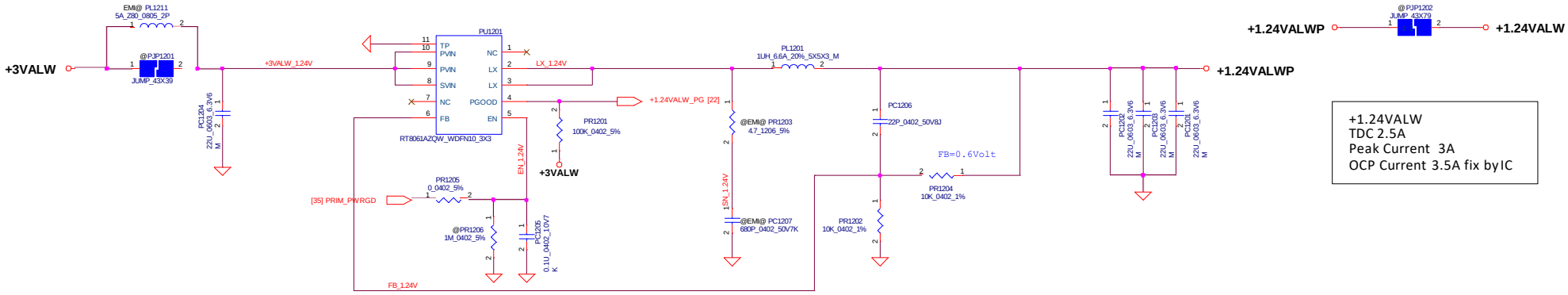

+19VB
+19VB_1.2V
+1.2VP
+0.6VSP
+5VALW
+3VALW
+1.2V_DDR
+0.6V_DDR_VTT
PUM01
RT8207PGQW_WQFN20_3X3
PQM01
AONH36334_DFN3X3A8-10
PLM01
1UH_11A_20%_7X7X3_M
PD502
RB751V-40_SOD323-2
JUMP_43X39
JUMP_43X118
For RT8207P
0.6Volt +/-5%
TDC 1.2A
Peak Current 1.5A
+1.2VP
TDC 6.2 A
Peak Current 8.9A
OCP Current 10.7A
Mode S3 S5 +1.2V_MEN +V_DDR_REF +0.6V_P
S5 L L off off off
S3 L H on on off
S0 H H on on on
Compal Secret Data
Compal Electronics, Inc.
PWR_+1.2V_DDR/+0.6V_DDR_VTT
Issued Date 2015/03/23
Deciphered Date 2014/12/15
Thursday, November 08, 2018
Sheet 33 of 10

The current limit is set to 6A, 9A or 12A when this pin
is pull low, floating or pull high

OCP setting	ILMT(pin3)
6A	Pull low
9A	Floating
12A	Pull high

+1.05VSP
TDC 5.2 A
Peak Current 6.5 A
OCP Current 9 A Fix by IC
TYP MAX
Choke DCR 11.0mohm , 12.0mohm





+1.24VALW
TDC 2.5A
Peak Current 3A
OCP Current 3.5A fix by IC

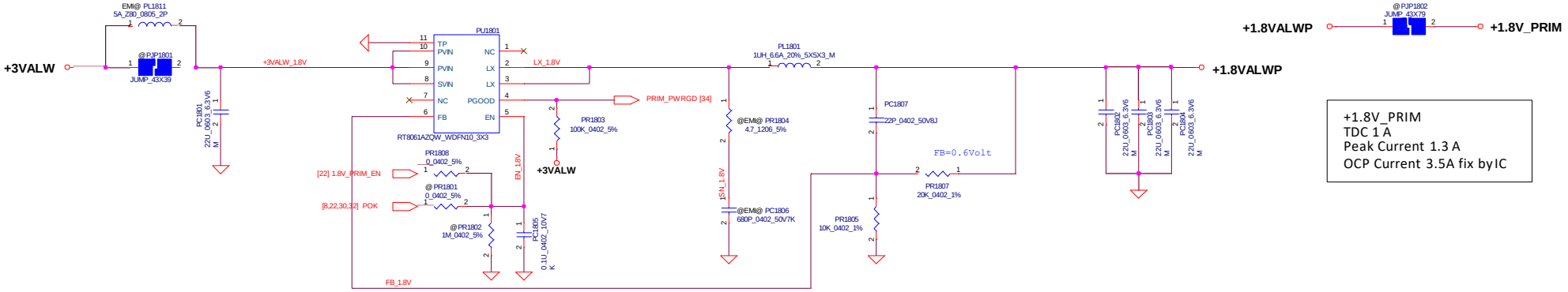
Securiity Cllassiifiicatiion	Compal Secret Data		
Issued Date	2015/03/23	Deciiiphered Date	2014/12/15

Compal Electronics, Inc.

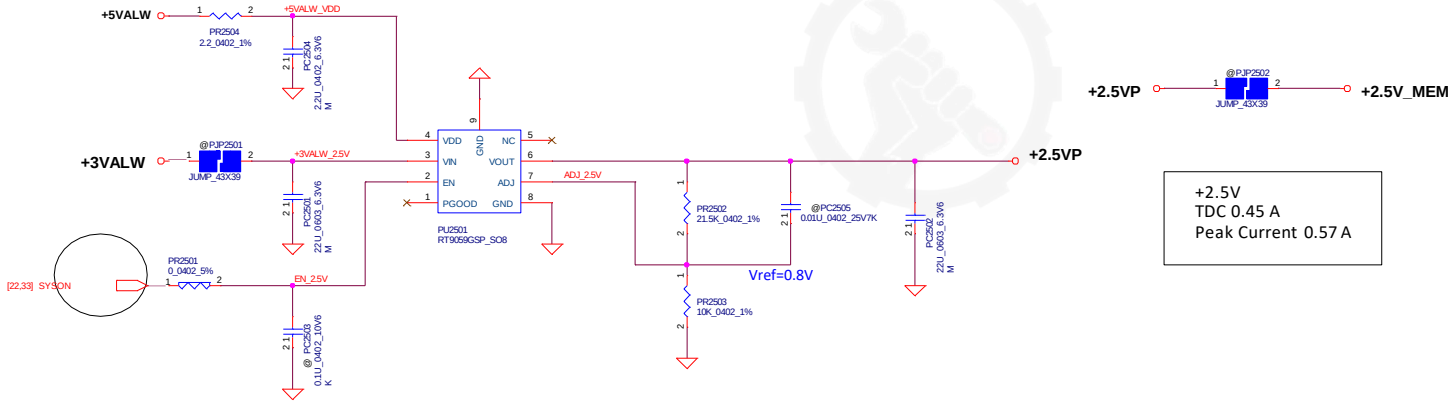
Title: PWR_+1.05VS/+1.24VALW

Size	Document Number	Rev
C		X00

Date: Thursday,, November 08,, 2018 Sheet 34 of 10



+1.8V_PRIM
TDC 1 A
Peak Current 1.3 A
OCP Current 3.5A fix by IC



+2.5V
TDC 0.45 A
Peak Current 0.57 A

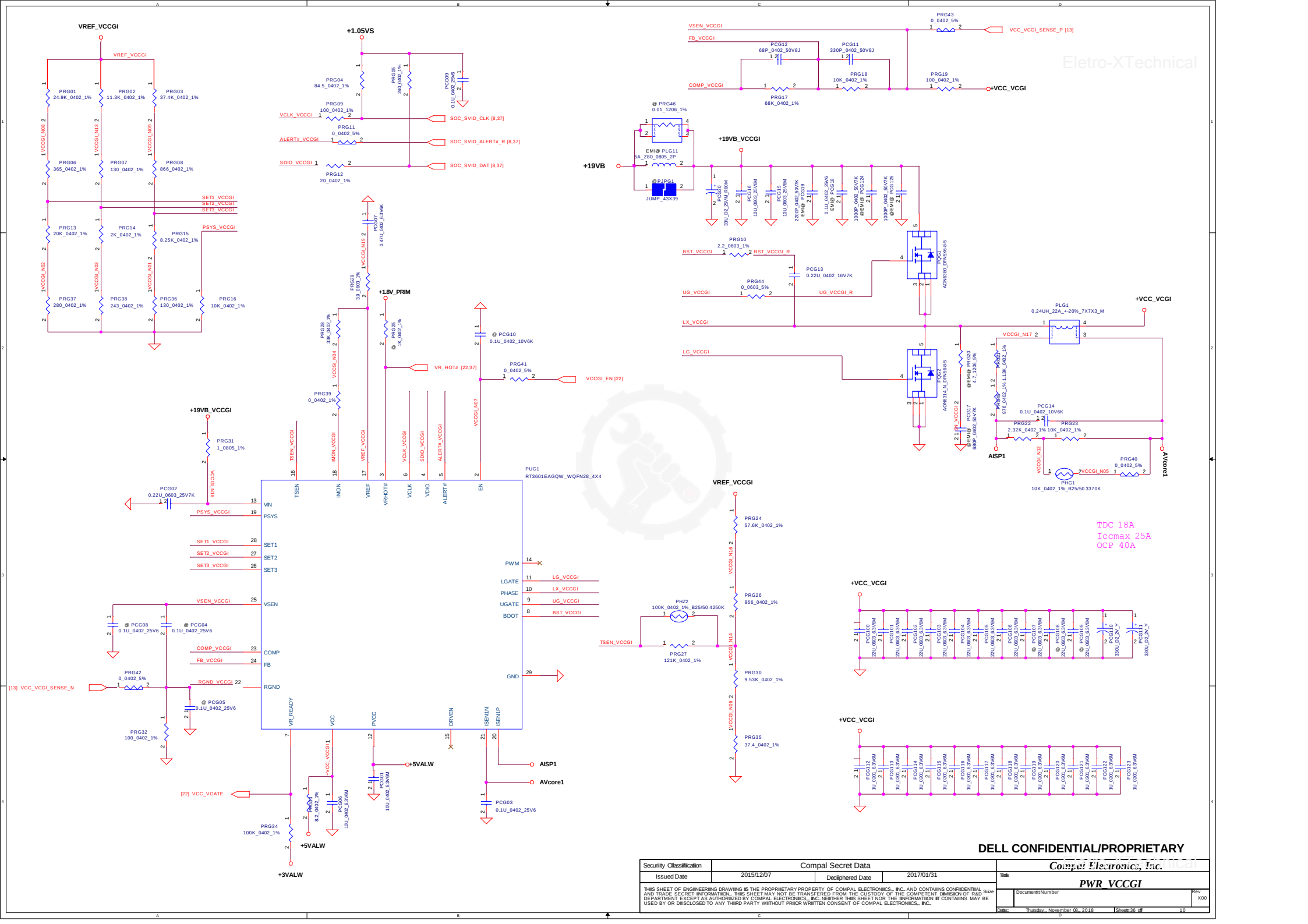
Securiity Cllassiification	Compal Secret Data		
Issued Date	2015/03/23	Deciiphered Date	2014/12/15

Compal Electronics, Inc.

Title: PWR_+1.8V_PRIM and +2.5V

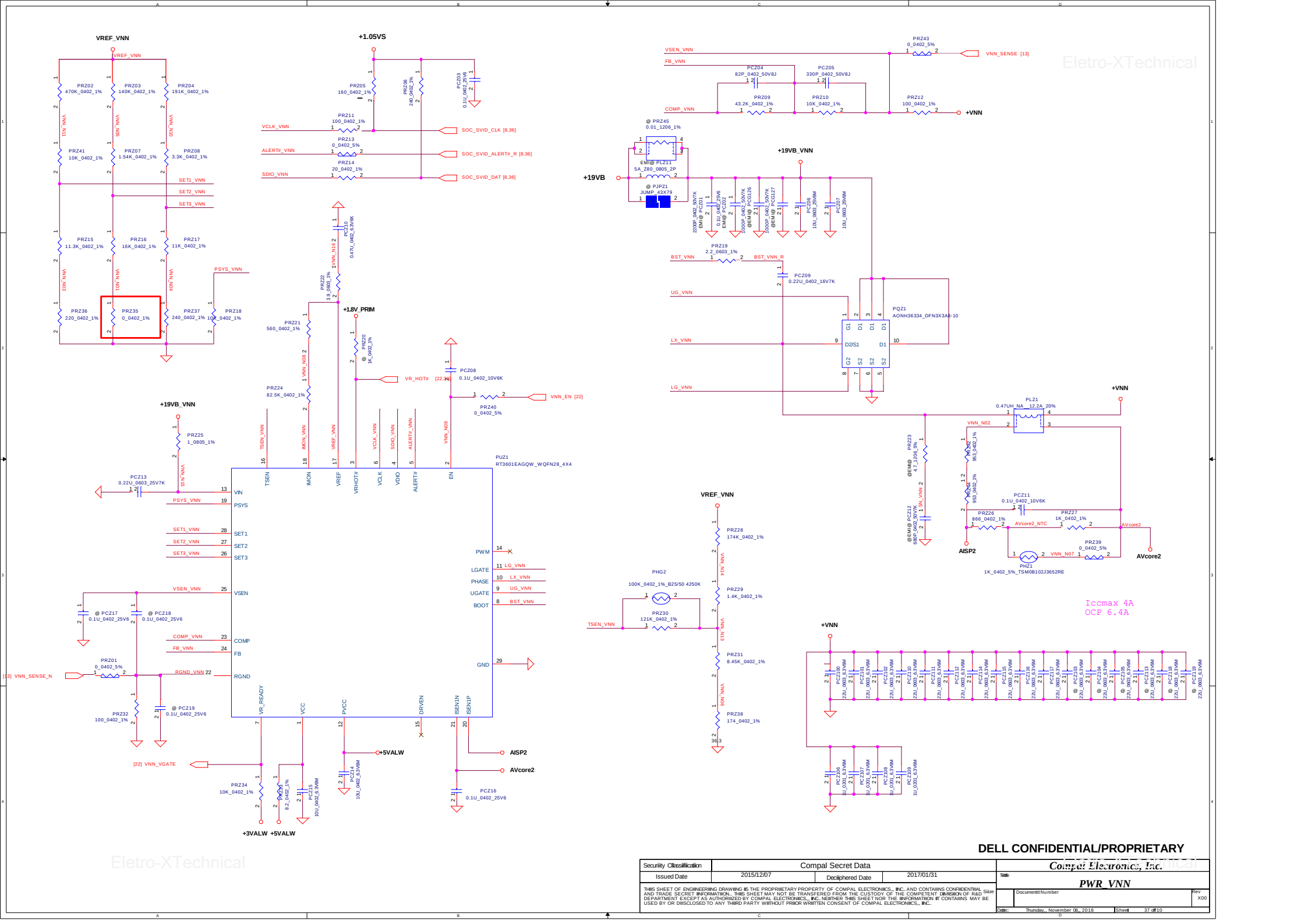
Size: Document Number: C | Rev: X00

Date: Thursday,, November 08,, 2018 | Sheet 35 of 10



Security Classification	Compal Secret Data		
Issued Date	2015/12/07	Declphered Date	2017/01/31

Title	PWR_VCCGI		
Document Number		Rev	X00
Date: Thursday, November 08, 2018		Sheet 36 of	10


VREF_VNN
+1.05VS
+19VB_VNN
+19VB
+1.8V_PRIM
+VNN
VREF_VNN
PRZ202 470K_0402_1%
PRZ203 140K_0402_1%
PRZ204 191K_0402_1%
PRZ41 10K_0402_1%
PRZ207 1.54K_0402_1%
PRZ208 3.3K_0402_1%
SET1_VNN
SET2_VNN
SET3_VNN
PRZ215 11.3K_0402_1%
PRZ216 16K_0402_1%
PRZ217 11K_0402_1%
PSYS_VNN
PRZ236 220_0402_1%
PRZ235 0_0402_1%
PRZ237 240_0402_1%
PRZ218 10K_0402_1%
PRZ205 160_0402_1%
PRZ206 240_0402_1%
PCZ203 0.1U_0402_25V6
VCLK_VNN
ALERT#_VNN
SDIO_VNN
PRZ211 100_0402_1%
PRZ213 0_0402_5%
PRZ214 20_0402_1%
SOC_SVID_CLK [8,36]
SOC_SVID_ALERT#_R [8,36]
SOC_SVID_DAT [8,36]
PCZ210 0.47U_0402_6.3V6K
PRZ22 3.9_0603_1%
PRZ221 560_0402_1%
PRZ224 82.5K_0402_1%
PRZ220 1K_0402_1%
PCZ208 0.1U_0402_10V6K
PRZ40 0_0402_5%
VR_HOT# [22,40]
VNN_EN [22]
PRZ225 1_0805_1%
PCZ13 0.22U_0603_25V7K
PUZ1 RT3601EAGQW_WQFN28_4X4
TSEN
IMON
VREF
VRHOT#
VCLK
VDIO
ALERT#
EN
VIN
PSYS
SET1
SET2
SET3
VSEN
COMP
FB
RGND
PWM
LGATE
PHASE
UGATE
BOOT
GND
VR_READY
VCC
PVCC
DRVEN
ISEN1N
ISEN1P
PCZ217 @ 0.1U_0402_25V6
PCZ218 @ 0.1U_0402_25V6
PRZ201 0_0402_5%
[33] VNN_SENSE_N
PRZ232 100_0402_1%
PCZ219 @ 0.1U_0402_25V6
[22] VNN_VGATE
PRZ234 10K_0402_1%
PRZ233 8.2_0402_1%
PCZ215 @ 10U_0402_6.3V6M
PCZ214 10U_0402_6.3V6M
+5VALW
AISP2
AVcore2
PCZ216 0.1U_0402_25V6
+3VALW +5VALW
VSEN_VNN
FB_VNN
COMP_VNN
PCZ204 82P_0402_50V8J
PCZ205 330P_0402_50V8J
PRZ09 43.2K_0402_1%
PRZ10 10K_0402_1%
PRZ12 100_0402_1%
PRZ43 0_0402_5%
VNN_SENSE [13]
@ PRZ45 0.01_1206_1%
EMI@ PLZ11 5A_Z80_0805_2P
@ PJPZ1 JUMP_43X79
PCZ201 @ 220P_0402_50V7K
PCZ202 @ 0.01U_0402_25V6
PCZ212 @ 100P_0402_50V7K
PCZ213 @ 100P_0402_50V7K
PCZ206 10U_0603_25V6M
PCZ207 10U_0603_25V6M
BST_VNN
BST_VNN_R
PRZ19 2.2_0603_1%
PCZ209 0.22U_0402_16V7K
UG_VNN
LX_VNN
LG_VNN
PQZ1 AONH36334_DFN3X3A8-10
PLZ1 0.47UH_NA__12.2A_20%
PRZ23 4.7_1206_5%
PCZ211 0.1U_0402_10V6K
PRZ226 866_0402_1%
PRZ227 1K_0402_1%
AVcore2_NTC
PRZ39 0_0402_5%
PHZ1 1K_0402_5%_TSM0B102J3652RE
AISP2
AVcore2
PHG2 100K_0402_1%_B25/50 4250K
PRZ230 121K_0402_1%
PRZ228 174K_0402_1%
PRZ229 1.4K_0402_1%
PRZ231 8.45K_0402_1%
PRZ238 174_0402_1%
Iccmax 4A
OCP 6.4A
PCZ100 22U_0603_6.3V6M
PCZ101 22U_0603_6.3V6M
PCZ102 22U_0603_6.3V6M
PCZ110 22U_0603_6.3V6M
PCZ111 22U_0603_6.3V6M
PCZ112 22U_0603_6.3V6M
PCZ114 22U_0603_6.3V6M
PCZ115 22U_0603_6.3V6M
PCZ116 22U_0603_6.3V6M
PCZ117 22U_0603_6.3V6M
PCZ103 22U_0603_6.3V6M
PCZ104 22U_0603_6.3V6M
PCZ105 22U_0603_6.3V6M
PCZ113 22U_0603_6.3V6M
PCZ118 22U_0603_6.3V6M
PCZ119 22U_0603_6.3V6M
PCZ106 3U_0201_6.3V6M
PCZ107 3U_0201_6.3V6M
PCZ108 3U_0201_6.3V6M
PCZ109 3U_0201_6.3V6M
DELL CONFIDENTIAL/PROPRIETARY
Compal Secret Data
2015/12/07
2017/01/31
Compal Electronics, Inc.
PWR_VNN
Thursday, November 08, 2018
37 of 10
X00

tfersion Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P31	CHARGER	20180520	COMPAL	customer recommend	change PUB01 ver B to ver C	0.1
2	P31	CHARGER	20180628	COMPAL	MLCC downsize	Change the PRB11 from 2Ohm to 1Ohm Change the PCB07 from 1U_0603_25V to 2.2U_0402_25V Change the PCB011 from 0.022U_0402_25V to 0.033U_0402_25V Change the PCB06 and PCB18 from 0.22U_0603_25V to 0.47U_0402_25V	0.2
3	P36	VCCGI	20180628	COMPAL	Fine tune ICCMAX	Change the PRG28 from 46.4KOhm to 33khm Change the PRG39 from 100Ohm to 0Ohm	0.2
4	P36	VCCGI	20180628	COMPAL	Change SET2 for FSW adjustable for VIN=19.5V	Change the PRG02 from 3.92KOhm to 11.3KOhm Change the PRG07 from 12.1Ohm to 130Ohm Change the PRG14 from 3.57KOhm to 2KOhm Change the PRG38 from 12.1Ohm to 243Ohm	0.2
5	P36	VCCGI	20180628	COMPAL	Fine tune LL	Change the PRG17 from 59KOhm to 68KOhm Change the PRG21 from 1.37KOhm to 1.13KOhm	0.2
6	P36	VCCGI	20180628	COMPAL	Fine tune AC IMON	Change the PRG21 from 1.37KOhm to 1.13KOhm Change the PRG45 from 1.37KOhm to 976Ohm Change the PRG22 from 2.8KOhm to 2.32kOhm	0.2
7	P37	VNN	20180628	COMPAL	Change SET2 for FSW adjustable for VIN=19.5V	Change the PRZ03 from 30.1kOhm to 140kOhm Change the PRZ07 from 63.4Ohm to 1.54KOhm Change the PRZ16 from 27.4KOhm to 16KOhm Change the PRZ35 from 63.4Ohm to 0Ohm	0.2
8	P37	VNN	20180628	COMPAL	Fine tune ICCMAX	Change the PRZ24 from 64.9KOhm to 82.5KOhm Change the PRZ21 from 1.5KOhm to 560Ohm	0.2
9	P30	BATTERY	20180706	COMPAL	ESD request	Change the PD5 and PD6 from SCA00001W00 to SCA00002A00	0.3
10	P31	CHARGER	20180706	COMPAL	Design request	Change the PRB10 from 47KOhm to 52.3KOhm	0.3
11	P35	+1.8VALWP	20180706	COMPAL	HW request	Add the PR1808_0_0402_5%	0.3
12	P31	CHARGER	20180715	COMPAL	Material shortage	Add the PCB37_1U_0402_25V6K Change the PCB07 from 2.2U_0402_25V6K to 1U_0402_25V6K	0.3
13	P32	3.3/5VALWP	20180824	COMPAL	Delay start time	Add the PC317_1U_0402_25V	0.3
14	P31~P38	ALL power	20181016	COMPAL	Short pad	0 Ohm resistance change to short pad	0.4

Security Classification	Compal Secret Data		
Issued Date	2015/12/22	Deciphered Date	2017/01/31

Compal Electronics, Inc.

Title: Changed-List PWR History

Size: Document Number: Rev: X00

Date: Thursday, November 08, 2018 Sheet 38 of 39

tfersion Change List (P. I. R. List)

Design Change								
Item	Date	Page	Part reference	Change description	Reason	Schematic	BOM	Layout
				Based on DVT2 0824B				
1	2018/10/8	22	RE15	Board ID change to 20K			v	
2	2018/10/24	22	DE1	change to "@ESD@"	ESD reserved		v	
3	2018/10/24	16	R16	change location R16 to F5	for hinge up protection		v	
4	2018/11/6	16	R6	0 ohm change to short pad	it's for NPI debug			v
5	2018/11/6	27	R7	0 ohm change to short pad	it's for NPI debug			v
6	2018/11/6	16	R8	0 ohm change to short pad	it's for NPI debug			v
7	2018/11/6	38	R77	0 ohm change to short pad	it's for NPI debug			v
8	2018/11/6	16	R301	0 ohm change to short pad	it's for power consumption			v
9	2018/11/6	6	RC34	0 ohm change to short pad	it's for power consumption			v
10	2018/11/6	6	RC35	0 ohm change to short pad	it's for NPI debug			v
11	2018/11/6	7	RC42	0 ohm change to short pad	it's for NPI debug			v
12	2018/11/6	13	RC126	0 ohm change to short pad	it's for power consumption			v
13	2018/11/6	13	RC127	0 ohm change to short pad	it's for power consumption			v
14	2018/11/6	13	RC128	0 ohm change to short pad	it's for power consumption			v
15	2018/11/6	13	RC129	0 ohm change to short pad	it's for power consumption			v
16	2018/11/6	13	RC130	0 ohm change to short pad	it's for power consumption			v
17	2018/11/6	13	RC131	0 ohm change to short pad	it's for power consumption			v
18	2018/11/6	13	RC132	0 ohm change to short pad	it's for power consumption			v
19	2018/11/6	13	RC133	0 ohm change to short pad	it's for power consumption			v
20	2018/11/6	13	RC134	0 ohm change to short pad	it's for power consumption			v
21	2018/11/6	13	RC135	0 ohm change to short pad	it's for power consumption			v
22	2018/11/6	13	RC136	0 ohm change to short pad	it's for power consumption			v
23	2018/11/6	12	RC1143	0 ohm change to short pad	it's for NPI debug			v
24	2018/11/6	6	RC1149	0 ohm change to short pad	it's for NPI debug			v
25	2018/11/6	15	RD4	0 ohm change to short pad	it's for NPI debug			v
26	2018/11/6	15	RD5	0 ohm change to short pad	it's for NPI debug			v
27	2018/11/6	15	RD6	0 ohm change to short pad	it's for NPI debug			v
28	2018/11/6	20	RA1	0 ohm change to short pad	it's for power consumption			v
29	2018/11/6	20	RA33	0 ohm change to short pad	it's for power consumption			v
30	2018/11/6	20	RA34	0 ohm change to short pad	it's for power consumption			v
31	2018/11/6	20	RA35	0 ohm change to short pad	it's for power consumption			v
32	2018/11/6	20	RA36	0 ohm change to short pad	it's for power consumption			v
33	2018/11/6	20	RA62	0 ohm change to short pad	it's for power consumption			v
34	2018/11/6	20	RA65	0 ohm change to short pad	it's for NPI debug			v
35	2018/11/6	22	RE5	0 ohm change to short pad	it's for NPI debug			v
36	2018/11/6	22	RE19	0 ohm change to short pad	it's for NPI debug			v
37	2018/11/6	22	RE20	0 ohm change to short pad	it's for NPI debug			v
38	2018/11/6	22	RE42	0 ohm change to short pad	it's for NPI debug			v
39	2018/11/6	18	RW25	0 ohm change to short pad	it's for NPI debug			v
40	2018/11/6	19	RL5	0 ohm change to short pad	it's for NPI debug			v
41	2018/11/6	19	RL13	0 ohm change to short pad	it's for NPI debug			v
42	2018/11/6		R17,R18,L4,RU18,RU21,LU7,LU12,RU19,RU24,LU11,LU8,LI1,LI2,LI3,LI4	Co-lay function add solder mask	DFX requirement			v
43	2018/11/8	24	RS61	change to "@"	not support devslp function		v	

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Compal Electronics, Inc.			
Title	Changed-List PWR History		
Size	Document Number	LA-G094PR10	Rev 1.0
Date:	Thursday, November 08, 2018	Sheet 39 of 39	