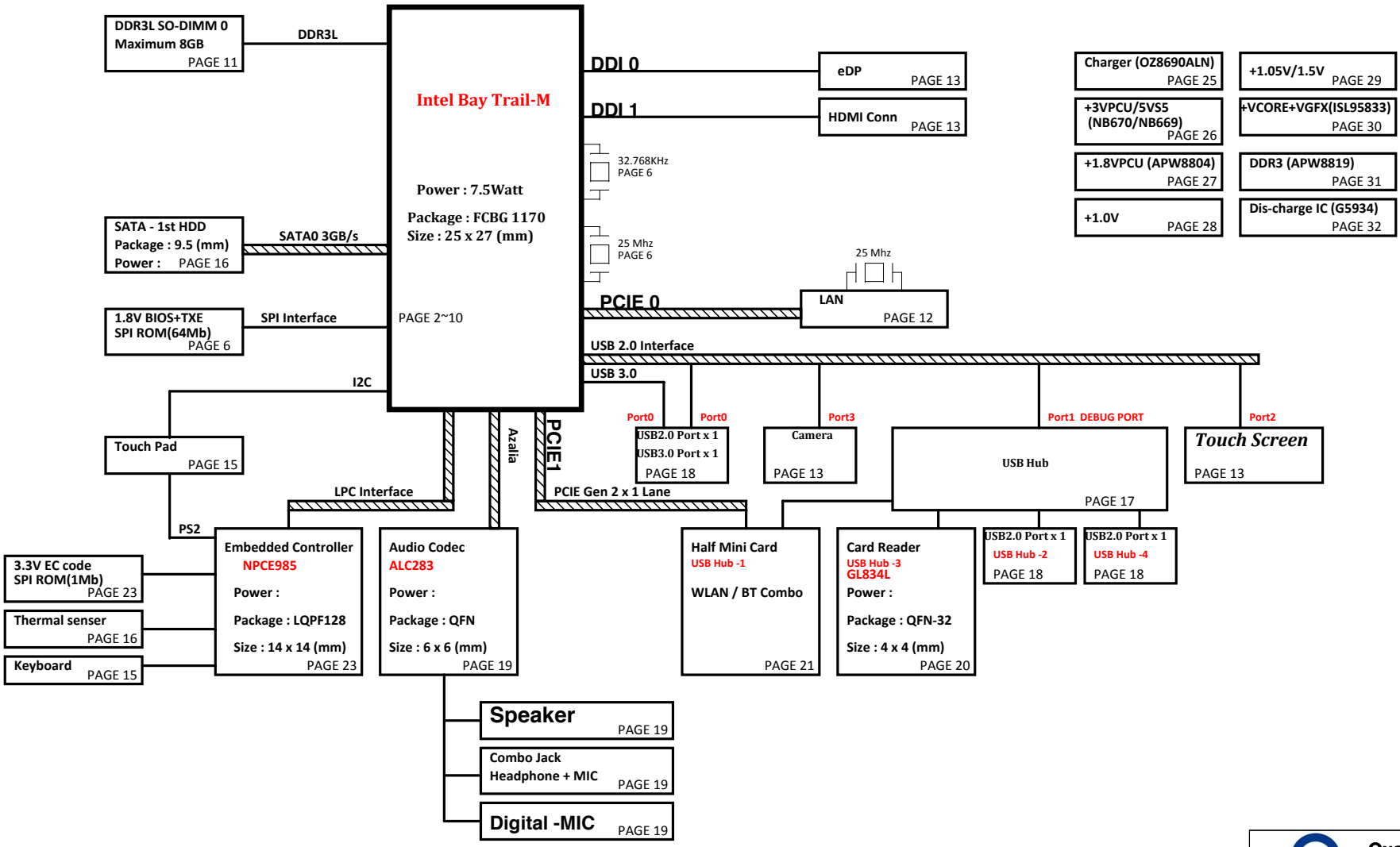
Roxy UMA(11.6")
Intel Bay Trail-M Platform Block Diagram

01

PCB 6L STACK UP

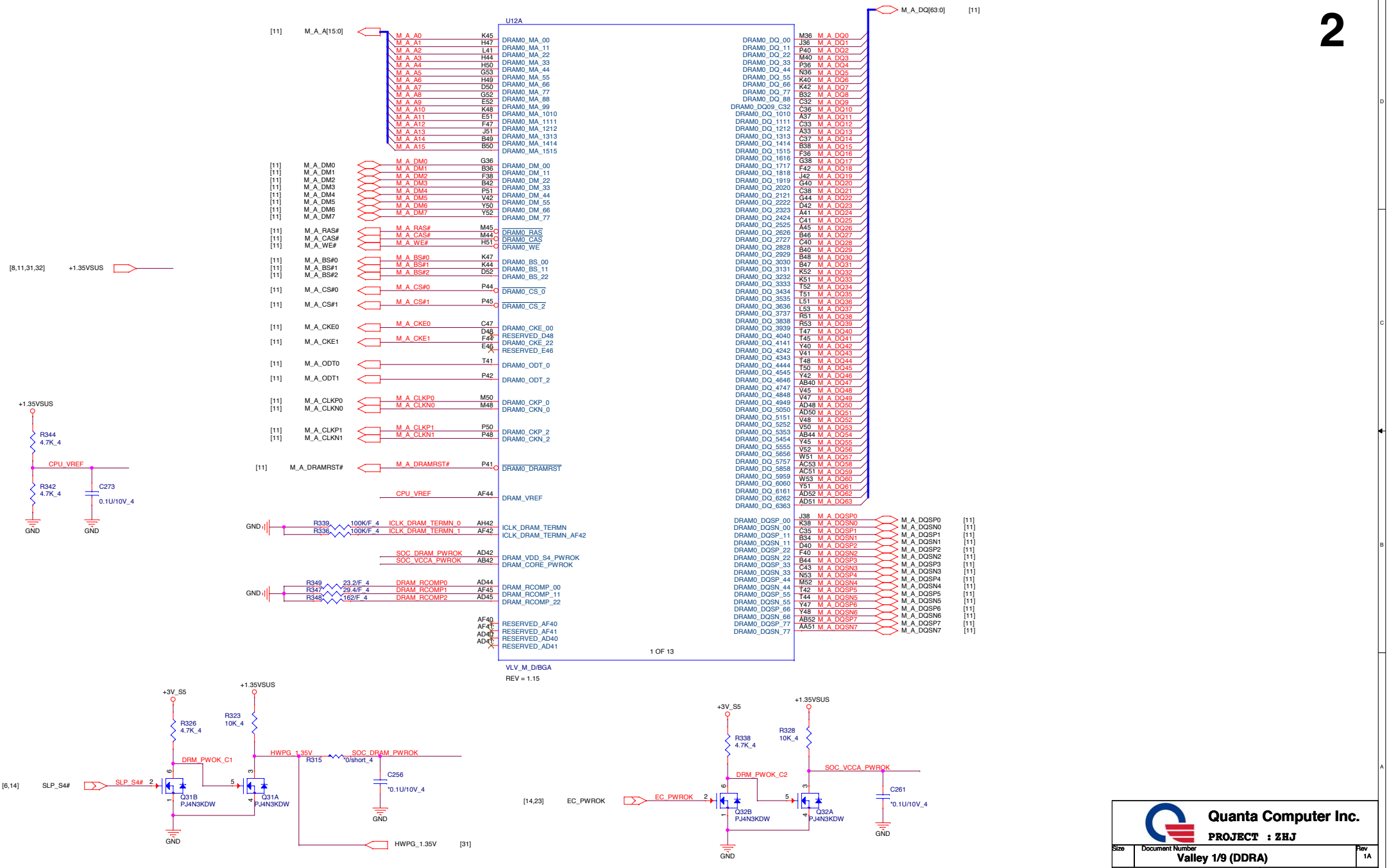
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT



Quanta Computer Inc.
PROJECT : ZHJ

Size	Document Number	Rev
	Intel Block Diagram	1A

Date: Tuesday, January 28, 2014 Sheet 1 of 33


2
U12A
M_A_DQ[63:0]
[11]
M_A_A[15:0]
M_A_A0
M_A_A1
M_A_A2
M_A_A3
M_A_A4
M_A_A5
M_A_A6
M_A_A7
M_A_A8
M_A_A9
M_A_A10
M_A_A11
M_A_A12
M_A_A13
M_A_A14
M_A_A15
M_A_DM0
M_A_DM1
M_A_DM2
M_A_DM3
M_A_DM4
M_A_DM5
M_A_DM6
M_A_DM7
M_A_RAS#
M_A_CAS#
M_A_WE#
M_A_BS#0
M_A_BS#1
M_A_BS#2
M_A_CS#0
M_A_CS#1
M_A_CKE0
M_A_CKE1
M_A_ODT0
M_A_ODT1
M_A_CLKP0
M_A_CLKN0
M_A_CLKP1
M_A_CLKN1
M_A_DRAMRST#
CPU_VREF
R339 100K/F_4
R336 100K/F_4
ICLK_DRAM_TERMN_0
ICLK_DRAM_TERMN_1
SOC_DRAM_PWROK
SOC_VCCA_PWROK
R349 23.2/F_4
R347 29.4/F_4
R348 162/F_4
DRAM_RCOMP0
DRAM_RCOMP1
DRAM_RCOMP2
RESERVED_AF40
RESERVED_AF41
RESERVED_AD40
RESERVED_AD41
1 OF 13
VLV_M_D/BGA
REV = 1.15
[8,11,31,32]
+1.35VSUS
R344 4.7K_4
R342 4.7K_4
C273 0.1U/10V_4
GND
+3V_S5
R326 4.7K_4
R323 10K_4
DRM_PWOK_C1
HWPG_1.35V
R315 *0/short_4
SOC_DRAM_PWROK
C256 *0.1U/10V_4
[6,14]
SLP_S4#
Q31B PJ4N3KDW
Q31A PJ4N3KDW
HWPG_1.35V
[31]
[14,23]
EC_PWROK
R338 4.7K_4
R328 10K_4
DRM_PWOK_C2
SOC_VCCA_PWROK
C261 *0.1U/10V_4
Q32B PJ4N3KDW
Q32A PJ4N3KDW
Quanta Computer Inc.
PROJECT : ZHJ
Size
Document Number
Valley 1/9 (DDRA)
Rev
1A
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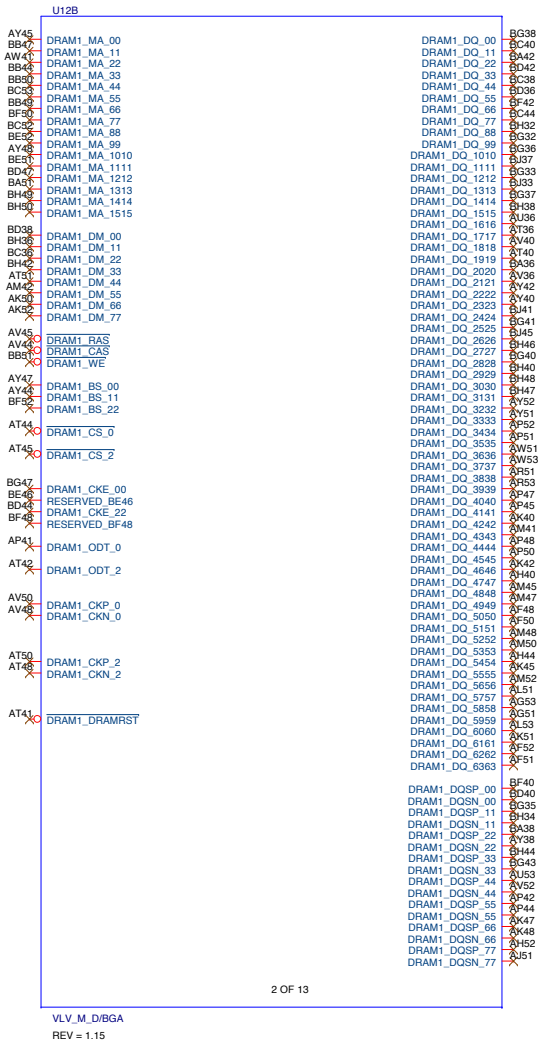
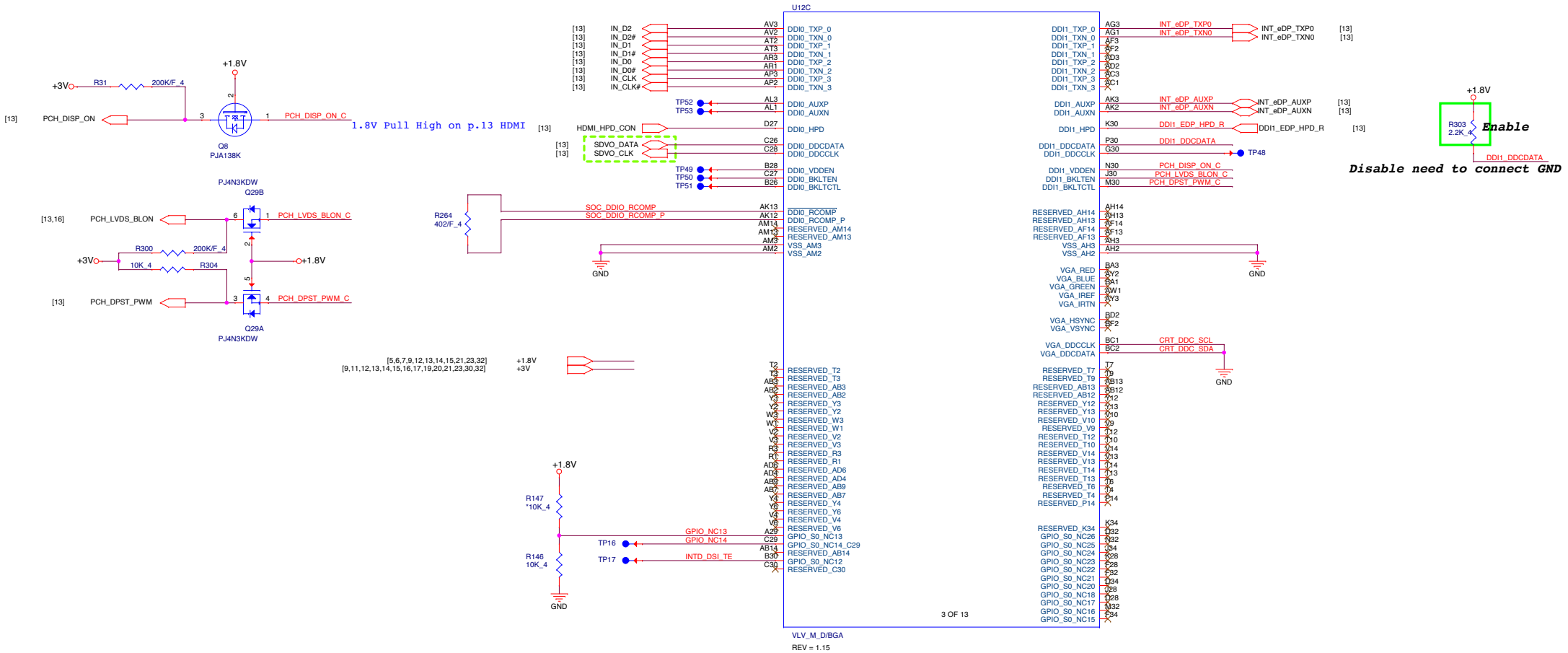
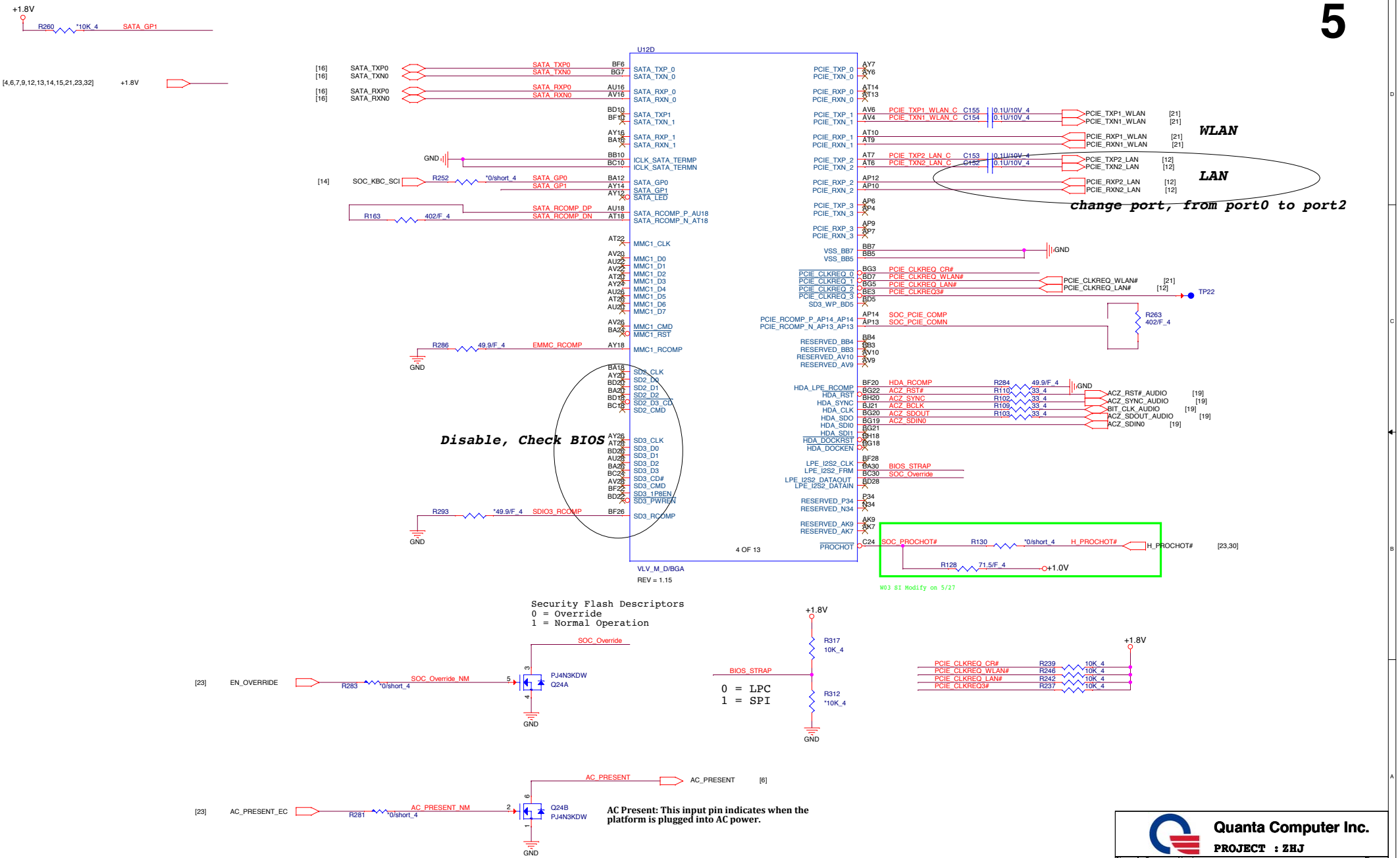


Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: Valley 2/9 (DDRB)	Rev: 1A
Date: Tuesday, January 28, 2014	Sheet 3 of 33	



Quanta Computer Inc.
PROJECT : ZHJ

Size	Document Number	Rev
	Valley 3/9 (Display)	2A
Date: Tuesday, January 28, 2014	Sheet 4 of 33	



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PROJECT : ZHJ

Size	Document Number	Rev
	Valley 4/9 (SD/PCIE/SATA)	2A
Date: Tuesday, January 28, 2014	Sheet 5 of 33	

WLAN clk

LAN clk

BOARD ID

BOARD_ID1 No use (Defaul "L")
BOARD_ID2 "Hi" W/ touch panel; "Low " W/O touch panel
BOARD_ID3 " H" for TPM

Note: To Touch pad intrrupt: change pin location

To Touch pad intrrupt

Internal pull up 20K to 1.8V allways

RTC Circuitry(RTC)

20mils

30mils

20MIL

20MIL

20MIL

ML1220 Coin type
AHL03001424 FDK (SAY) 15mAH
AHL03017100 Panasonic (MAT) 17mAH

20120109 change footprint.

RTC Clock 32.768KHz

2013/07/25
change package , P/N change
from BG332768224 to
BG332768453

sot323_213-2_1-1_3-2n7002w

SPI NOR FLASH

SPI_FLASH
soic8-7_9-1_27
AKE5EZN0N00
IC FLASH (8P) W25Q64FWSSIG (SOIC)

Close SPI ROM

Close APU

1.8V EC --> Chnage to 22ohm

O_1.8VA

To Touch Screen Select

Close APU

Close POWER side ,have enable.

Lay out Note:

SVID_ALERT#
SVID_DATA
SVID_CLK

20111129 contact to EC thougth series resistor.

U12E
5 OF 13
VLW_M_D/BGA
REV = 1.15

Quanta Computer Inc.	PROJECT : ZHJ
Size	Document Number: Valley 5/9 (SPI/GPIO/CLK)
Rev	2A
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[6,9,14,23,32] +1.8V_S5

[4,5,6,9,12,13,14,15,21,23,32] +1.8V

[4,9,11,12,13,14,15,16,17,19,20,21,23,30,32] +3V

U12F

+1.8V_S5

R48 *10K_4 SOC_PWR_BUT

Port 1 is debug port

USB 2.0 / 3.0 Base

HUB1

Touch Panel

CAMERA

[18] USBP0+ M16 USB_DP0

[18] USBP0- K16 USB_DN0

[17] USB_H1_P J14 USB_DP1

[17] USB_H1_N G14 USB_DN1

[13] USBP2+ K12 USB_DP2

[13] USBP2- J12 USB_DN2

[13] USBP3+ K10 USB_DP3

[13] USBP3- H10 USB_DN3

R249 1K/F_4 ICLK_USB_TERMN_0 D10 ICLK_USB_TERMN_D10

R248 1K/F_4 ICLK_USB_TERMN_1 F10 ICLK_USB_TERMN

GND

[18] SOC_USB_OC0

R105 10K_4

R104 10K_4

+1.8V_S5

C20 USB_OC_00

B20 USB_OC_11

[18] SOC_USB_OC1

R247 45.3/F_4 USB_RCOMP D6 USB_RCOMPO

C7 USB_RCOMPI

GND

R270 *0/J_4 M13 USB_PLL_MON

GND

B4 USB_HSIC0_DATA

B5 USB_HSIC0_STROBE

E2 USB_HSIC1_DATA

D2 USB_HSIC1_STROBE

GND R55 45.3/F_4 USB_HSIC_RCOMP A7 USB_HSIC_RCOMP

R285 49.9/F_4

LPC_RCOMP BF18

12.5 Ohm

[15,21,23] LAD0 BH16 LPC_RCOMP

[15,21,23] LAD1 BJ17 ILB_LPC_AD_00

[15,21,23] LAD2 BJ13 ILB_LPC_AD_11

[15,21,23] LAD3 BG14 ILB_LPC_AD_22

[15,21,23] LFRAME# BG17 ILB_LPC_AD_33

ILB_LPC_FRAME

[15] PCLK_TPM R98 22_4 SOC_CLKOUT_0 BG15 ILB_LPC_CLK_00

[23] CLK_24M_KBC R90 22_4 SOC_CLKOUT_1 BH14 ILB_LPC_CLK_11

[21] CLK_24M_DEBUG R274 22_4 SOC_CLKRUN# BG16 ILB_LPC_CLKRUN

[15,23] CLKRUN# R279 22_4 [14] SOC_SERIRQ SOC_SERIRQ BG13 ILB_LPC_SERIRQ

[14] SMB_SOC_DATA

[14] SMB_SOC_CLK

+1.8V

R79 2.2K_4 SMB_SOC_DATA BG12 PCU_SMB_DATA

R73 2.2K_4 SMB_SOC_CLK BH10 PCU_SMB_CLK

R80 2.2K_4 SMB_SOC_ALERTB_C BG11 PCU_SMB_ALERT

R7386 follow CRB and check list change to 2.2K

6 OF 13

VLV_M_D/BGA

REV = 1.15

RESERVED_M10 M10

RESERVED_M9 M9

RESERVED_P7 P7

RESERVED_P6 P6

RESERVED_M7 M7

USB3_REXT0 M12 USB3_P0_REXT R258 1.24K/F_4

GND

RESERVED_P10 P10

RESERVED_P12 P12

RESERVED_M4 M4

RESERVED_M6 M6

USB3_RXP0 D4 USB30_RX1+ [18]

USB3_RXN0 E3 USB30_RX1- [18]

USB3_TXP0 K6 USB30_TX1+ [18]

USB3_TXN0 K7 USB30_TX1- [18]

RESERVED_H8 H8

RESERVED_H7 H7

RESERVED_H5 H5

RESERVED_H4 H4

+1.8V

TOUCH_PANEL_SOC_RST# R269 *10K_4

SOC_SENSOR_HUB_WAKE R265 *10K_4

Top Swap (A16 Override)
0 = Top address bit is unchanged
1 = Top address bit is inverted

+1.8V

R253 *10K_4

GPIO_S0_SC_55 BD12

GPIO_S0_SC_56 BC12 GPIO_S0_SC_56

GPIO_S0_SC_57 BD14 SOC_UART_TX

GPIO_S0_SC_58 BC14

GPIO_S0_SC_59 BF14 SOC_SENSOR_HUB_WAKE

GPIO_S0_SC_60 BD16 TOUCH_PANEL_SOC_RST#

GPIO_S0_SC_61 BC16 SOC_UART_RX

R254 *10K_4

GND

ILB_8254_SPKR BH12 ACZ_SPKR [19]

SOC_UART_TX R273 *0_4 SOC_UART_RX

Un-Stuff for Test Only

+1.8V

I2C_6_SDA R118 560_4

I2C_6_SCL R119 560_4

I2C_1_SDA R123 *2.2K_4

I2C_1_SCL R125 *2.2K_4

I2C_2_SDA_R R126 *2.2K_4

I2C_2_SCL_R R132 *2.2K_4

I2C_3_SDA R136 *2.2K_4

I2C_3_SCL R137 *2.2K_4

I2C_4_SDA R142 *2.2K_4

I2C_4_SCL R141 *2.2K_4

I2C_5_SDA R140 *2.2K_4

I2C_5_SCL R145 *2.2K_4

I2C_66_SDA R151 *2.2K_4

I2C_66_SCL R152 *2.2K_4

TP_NC R155 *2.2K_4

TP_NC1 R156 *2.2K_4

SIO_I2C0_DATA BH22 I2C_0_SDA R108 22_4 I2C_6_SDA I2C_6_SDA [14]

SIO_I2C0_CLK BG23 I2C_0_SCL R117 22_4 I2C_6_SCL I2C_6_SCL [14]

SIO_I2C1_DATA BG24 I2C_1_SDA

SIO_I2C1_CLK BH24 I2C_1_SCL

SIO_I2C2_DATA BG25 I2C_2_SDA_R

SIO_I2C2_CLK BJ25 I2C_2_SCL_R

SIO_I2C3_DATA BG26 I2C_3_SDA

SIO_I2C3_CLK BH26 I2C_3_SCL

SIO_I2C4_DATA BF27 I2C_4_SDA

SIO_I2C4_CLK BG27 I2C_4_SCL

SIO_I2C5_DATA BH28 I2C_5_SDA

SIO_I2C5_CLK BG28 I2C_5_SCL

SIO_I2C6_DATA BJ29 I2C_66_SDA

SIO_I2C6_CLK BG29 I2C_66_SCL

GPIO_S0_SC_092 BH30 TP_NC

GPIO_S0_SC_093 BG30 TP_NC1

I2C pull up:
Standard/ Fast Mode --> 560 ohm
Hight speed mode --> CLK- 560 ohm;
DATA- 910 ohm

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	Valley 6/9 (USB/LPC/I2C)	2A
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[22,30] +VCC_CORE
[9,22,30] +VCC_GFX
[2,11,31,32] +1.35VSUS

+VCC_GFX +VCC_CORE
R236 100/F_4
R296 100/F_4
VCC_SENSE
VCC_AXG_SENSE
VSS_SENSE
R314 100/F_4
GND

[30] VCC_SENSE
[30] VCC_AXG_SENSE
[30] VSS_SENSE
[30] VSS_AXG_SENSE
R290 *0/short_4

+1.35VSUS_VSM
R334 *0/short_4
+1.35VSUS

+VCC_CORE
+1.35VSUS_VSM
C269 1U/6.3V_4
C270 4.7U/6.3V_6
C267 0.1U/10V_4
GND

C237 10U/6.3V_6
C230 4.7U/6.3V_6
C167 4.7U/6.3V_6
C231 2.2U/6.3V_6
C176 2.2U/6.3V_6
C179 22U/6.3V_6
C175 22U/6.3V_6
C178 22U/6.3V_6
GND

C166 22U/6.3V_6
C177 22U/6.3V_6
C169 22U/6.3V_6
C168 22U/6.3V_6

TP26 SOC_CORE_PINAF30

U12G

VCC_SENSE	P28	CORE_VCC_SENSE_P28
VCC_AXG_SENSE	BB8	UNCORE_VNN_SENSE
VSS_SENSE	N28	CORE_VSS_SENSE_N28
VSS_AXG_SENSE		
	AD38	DRAM_VDD_S4_AD38
	AF38	DRAM_VDD_S4_AF38
	A48	DRAM_VDD_S4
	AK38	DRAM_VDD_S4_AK38
	AM38	DRAM_VDD_S4_AM38
	AV41	DRAM_VDD_S4_AV41
	AV42	DRAM_VDD_S4_AV42
	BB46	DRAM_VDD_S4_BB46
	AA27	CORE_VCC_S0IX_AA27
	AA29	CORE_VCC_S0IX_AA29
	AA30	CORE_VCC_S0IX_AA30
	AC27	CORE_VCC_S0IX_AC27
	AC29	CORE_VCC_S0IX_AC29
	AC30	CORE_VCC_S0IX_AC30
	AD27	CORE_VCC_S0IX_AD27
	AD29	CORE_VCC_S0IX_AD29
	AD30	CORE_VCC_S0IX_AD30
	AF27	CORE_VCC_S0IX_AF27
	AF29	CORE_VCC_S0IX_AF29
	AG27	CORE_VCC_S0IX_AG27
	AG29	CORE_VCC_S0IX_AG29
	AG30	CORE_VCC_S0IX_AG30
	P26	CORE_VCC_S0IX_P26
	P27	CORE_VCC_S0IX_P27
	U27	CORE_VCC_S0IX_U27
	U29	CORE_VCC_S0IX_U29
	V27	CORE_VCC_S0IX_V27
	V29	CORE_VCC_S0IX_V29
	V30	CORE_VCC_S0IX_V30
	Y27	CORE_VCC_S0IX_Y27
	Y29	CORE_VCC_S0IX_Y29
	Y30	CORE_VCC_S0IX_Y30
TP_CORE_V1P05_S4		

7 OF 13

VLV_M_D/BGA
REV = 1.15

DRAM_VDD_S4_BD49	BD49	
DRAM_VDD_S4_BD52	BD52	
DRAM_VDD_S4_BD53	BD53	
DRAM_VDD_S4_BF44	BF44	
DRAM_VDD_S4_BG51	BG51	
DRAM_VDD_S4_BJ48	BJ48	
DRAM_VDD_S4_C51	C51	
DRAM_VDD_S4_D44	D44	
DRAM_VDD_S4_F49	F49	
DRAM_VDD_S4_F52	F52	
DRAM_VDD_S4_F53	F53	
DRAM_VDD_S4_H46	H46	
DRAM_VDD_S4_M41	M41	
DRAM_VDD_S4_M42	M42	
DRAM_VDD_S4_V38	V38	
DRAM_VDD_S4_Y38	Y38	
UNCORE_VNN_S3_AA24	AA24	
UNCORE_VNN_S3_AC22	AC22	
UNCORE_VNN_S3_AC24	AC24	
UNCORE_VNN_S3_AD22	AD22	
UNCORE_VNN_S3_AD24	AD24	
UNCORE_VNN_S3_AF22	AF22	
UNCORE_VNN_S3_AF24	AF24	
UNCORE_VNN_S3_AG22	AG22	
UNCORE_VNN_S3_AG24	AG24	
UNCORE_VNN_S3_AJ22	AJ22	
UNCORE_VNN_S3_AJ24	AJ24	
UNCORE_VNN_S3_AK22	AK22	
UNCORE_VNN_S3_AK24	AK24	
UNCORE_VNN_S3_AK25	AK25	
UNCORE_VNN_S3_AK27	AK27	
UNCORE_VNN_S3_AK29	AK29	
UNCORE_VNN_S3_AK30	AK30	
UNCORE_VNN_S3_AK32	AK32	
UNCORE_VNN_S3_AM22	AM22	
TP2_CORE_VCC_S0IX	AA22	SOC_CORE_PIN_AA22

TP25

+1.35VSUS
C277 2.2U/6.3V_6
C271 2.2U/6.3V_6
C293 2.2U/6.3V_6
C292 2.2U/6.3V_6
C295 1U/6.3V_4
C294 0.1U/10V_4
GND

+VCC_GFX
C158 10U/6.3V_6
C50 10U/6.3V_6
C58 10U/6.3V_6
C229 1U/6.3V_4
C214 1U/6.3V_4
C218 1U/6.3V_4
C244 0.1U/10V_4
C234 0.1U/10V_4
C151 0.1U/10V_4
GND

Near CPU
C212 22U/6.3V_6
C213 22U/6.3V_6
C163 22U/6.3V_6
C54 22U/6.3V_6
C29 *330u/2V_7343

IO Thrm Protect

+3VPCU
R345 *10K/J_4
default 25 degree for detect temperature
THRM_MOINTOR [23]
R337 *0_4
C274 *0.1u/10V_4
THER_CPU
R327 *10K_6_NTC

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	Valley 7/9 (Power 1)	2A
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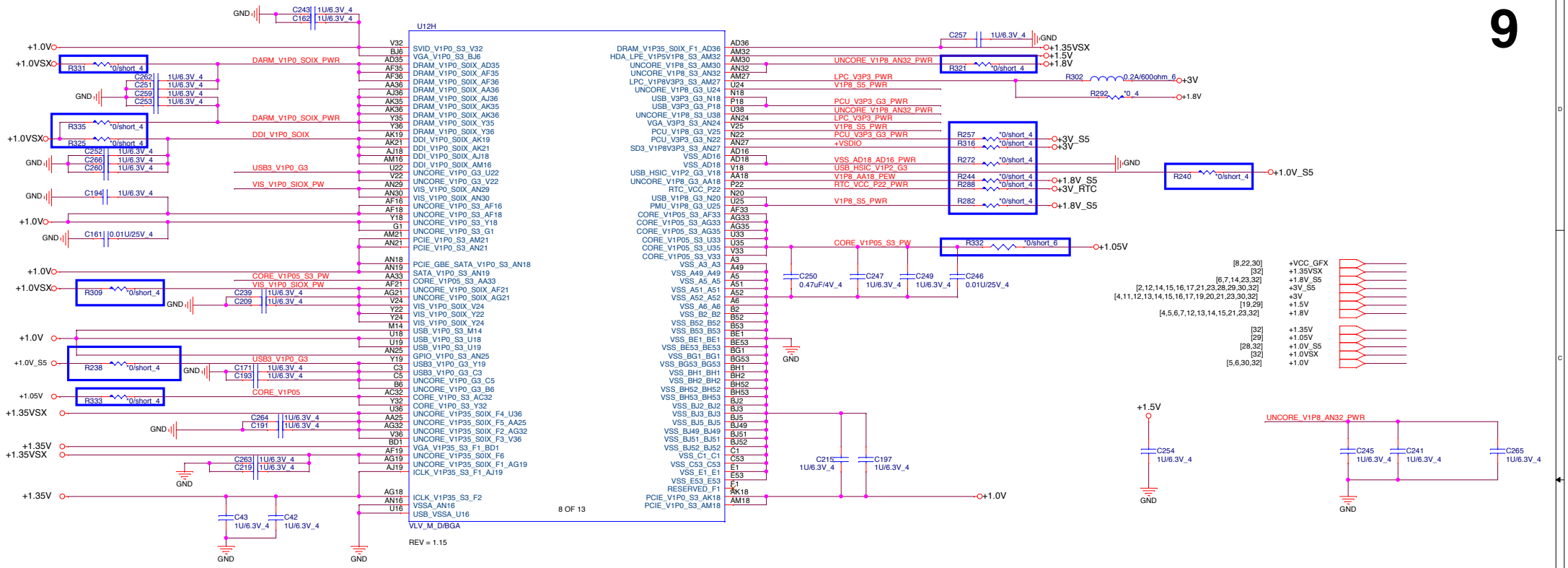
U12H
8 OF 13
VLV_M_D/BGA
REV = 1.15
+1.0V
+1.0VSX
+1.35VSX
+1.35V
+1.05V
+1.0V_S5
+1.8V_S5
+3V_S5
+3V_RTC
+3V
+1.8V
+1.5V
+VCC_GFX
+VSDIO
GND
DARM_V1P0_SOIX_PWR
DDI_V1P0_SOIX
USB3_V1P0_G3
VIS_V1P0_SIOX_PW
CORE_V1P05_S3_PW
CORE_V1P05
UNCORE_V1P8_AN32_PWR
LPC_V3P3_PWR
V1P8_S5_PWR
PCU_V3P3_G3_PWR
VSS_AD18_AD16_PWR
USB_HSIC_V1P2_G3
V1P8_AA18_PEW
RTC_VCC_P22_PWR
Quanta Computer Inc.
PROJECT : ZHJ
Valley 8/9 (Power 2)
Rev 1A
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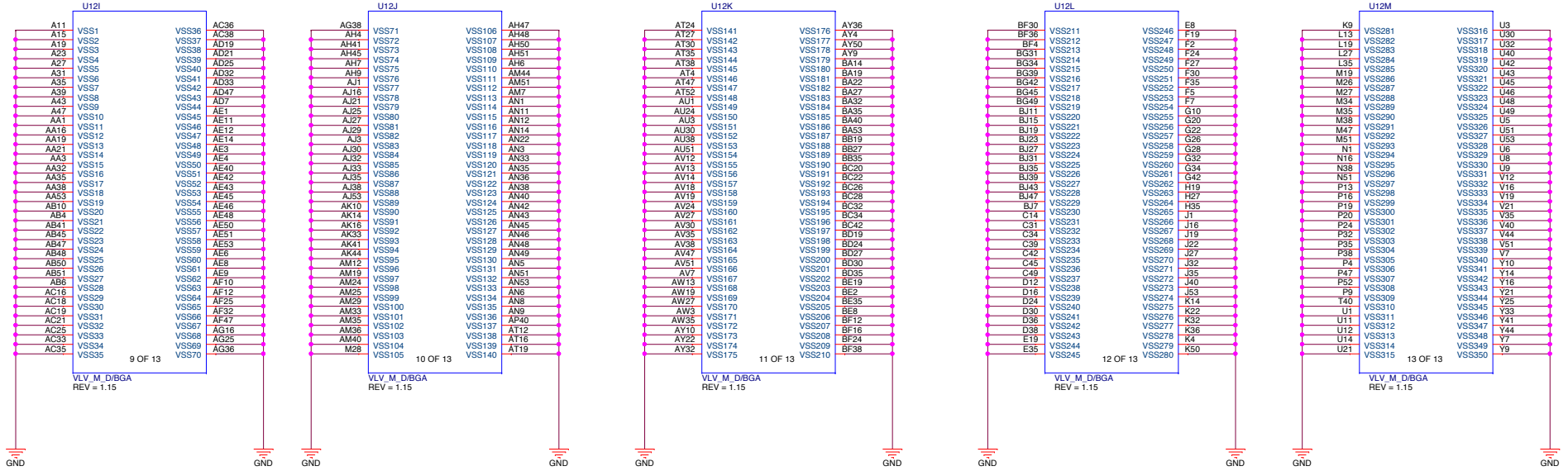
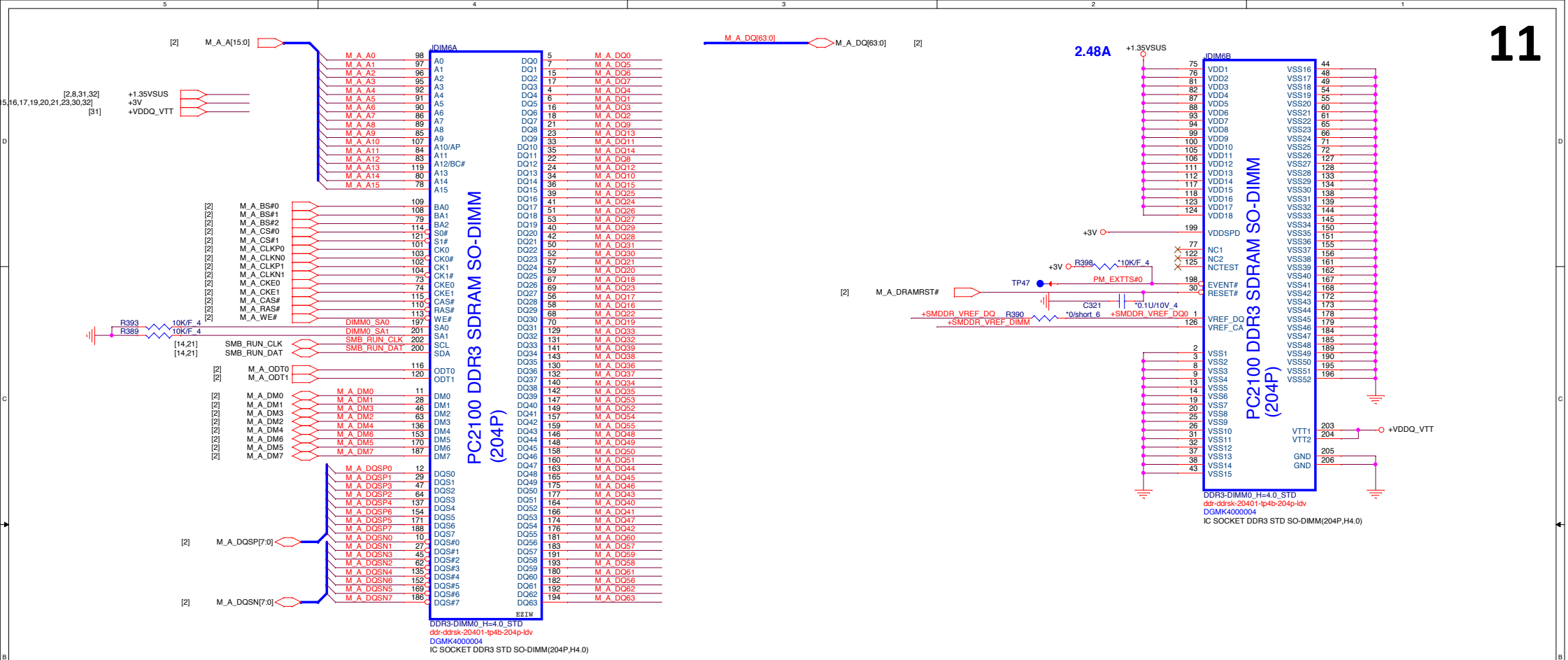


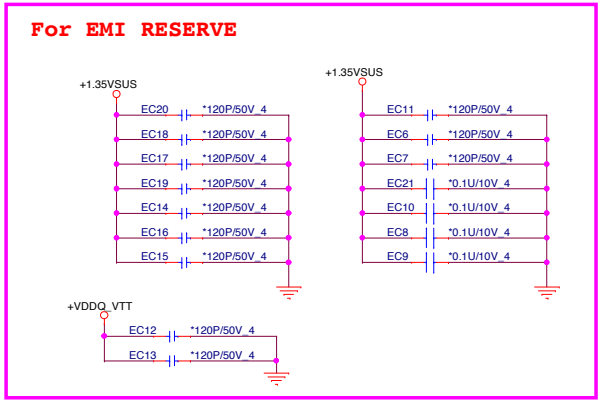
Quanta Computer Inc.

PROJECT : ZHJ

Size	Document Number	Rev
	Valley 9/9 (GND)	1A
Date: Tuesday, January 28, 2014	Sheet 10 of 33	

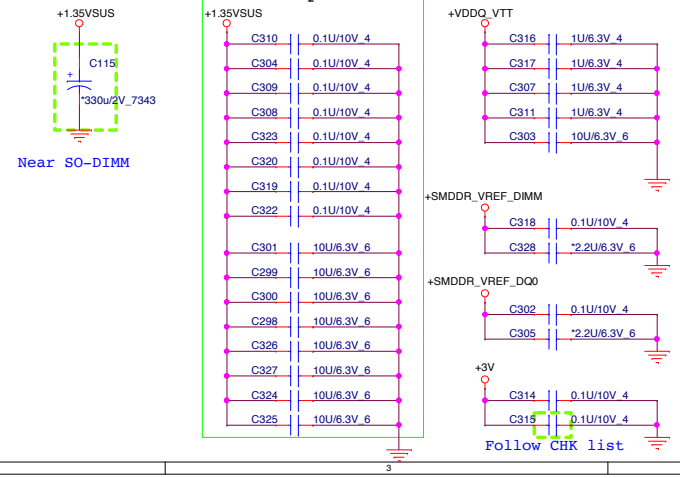


For EMI RESERVE

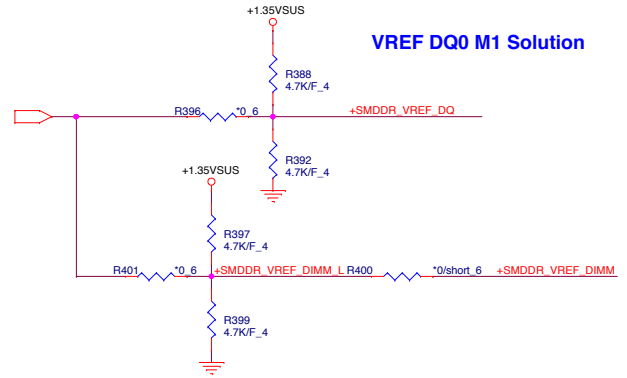


Place these Caps near So-Dimm0.

0.1uF/10uF 4pcs on each side of connector



VREF DQ0 M1 Solution



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PROJECT : ZHJ

Size	Document Number	Rev
	DDR3 DIMM0-STD(4.0H)	1A
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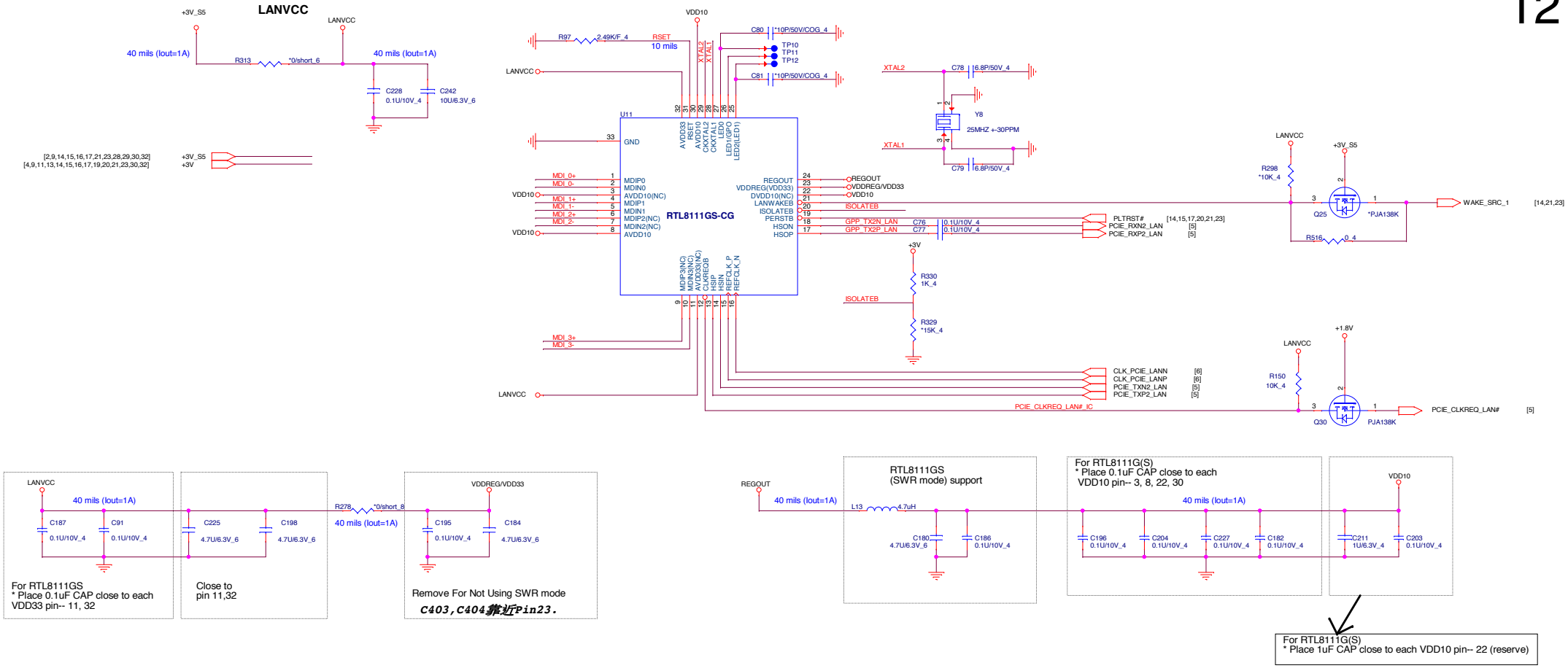
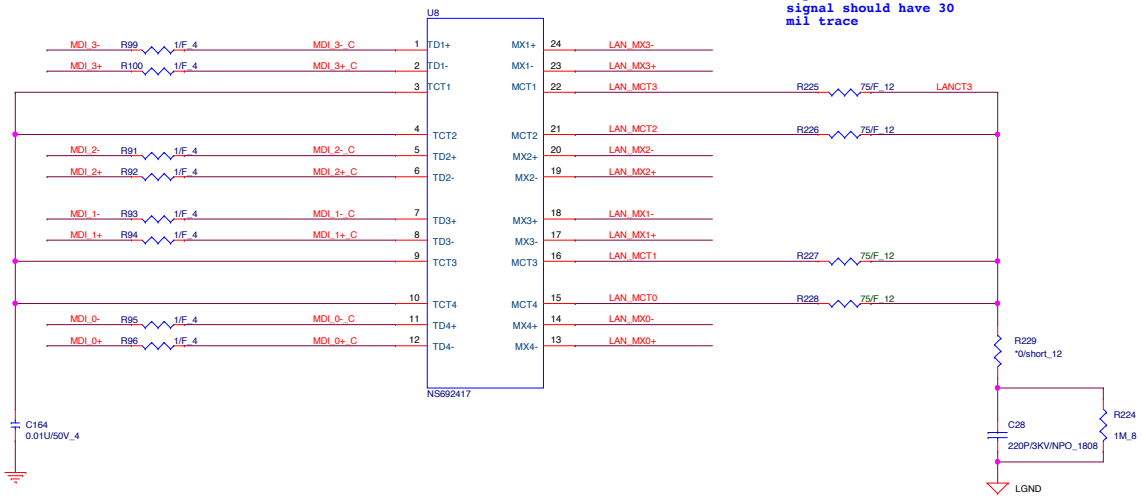
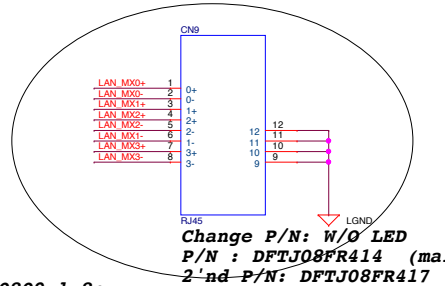


Tramsformer



Layout:All termination signal should have 30 mil trace

RJ45 Connector



Change P/N: W/O LED
P/N : DFTJ08FR414 (main)
2'nd P/N: DFTJ08FR417
change footprint

rj45-c100mp-10809-1-8p

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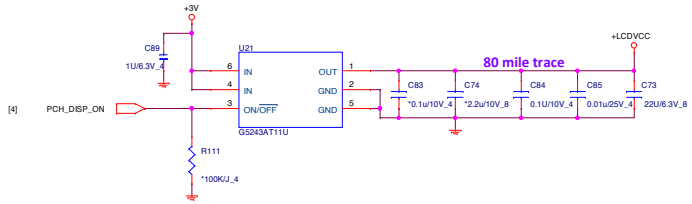
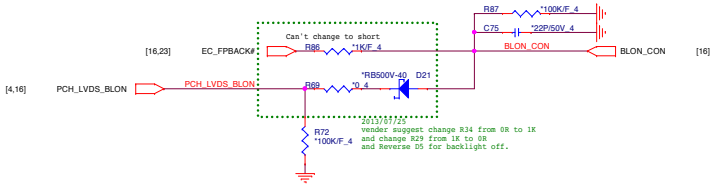
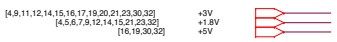
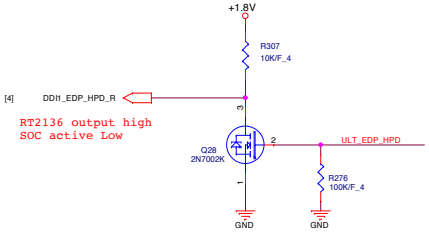
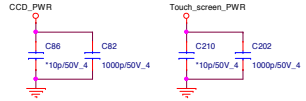
LVDS Conn.

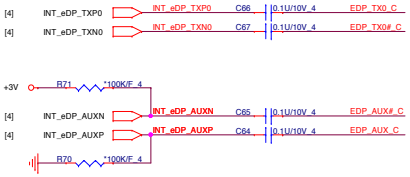


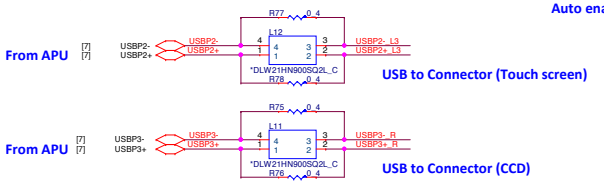


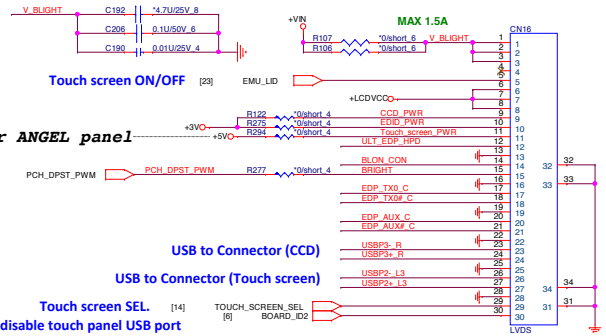




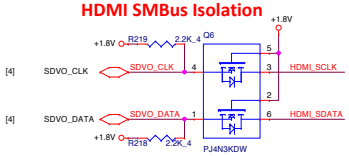


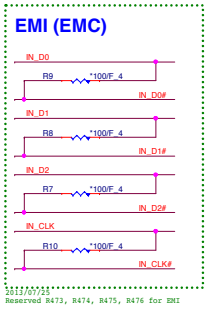


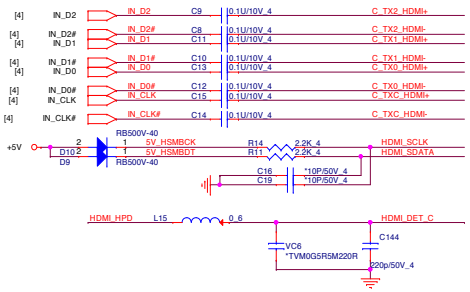


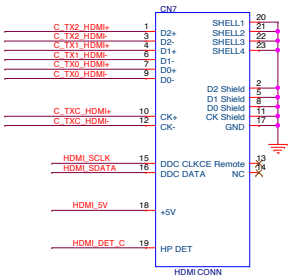


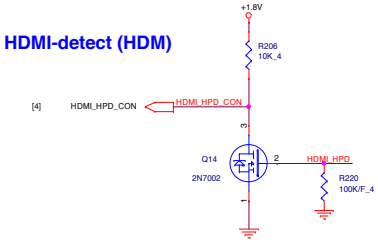
HDMI Conn.

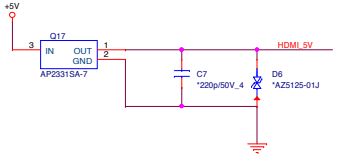


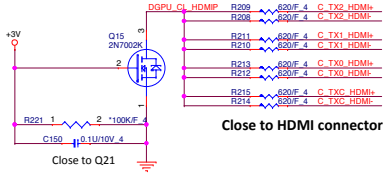


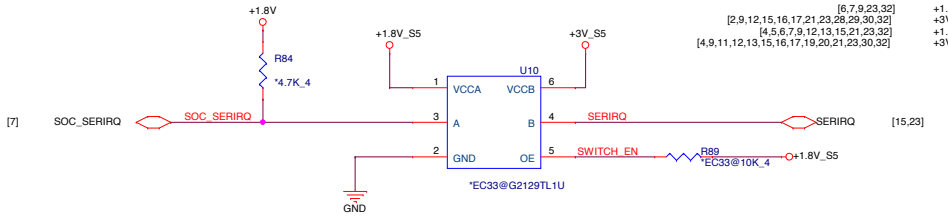


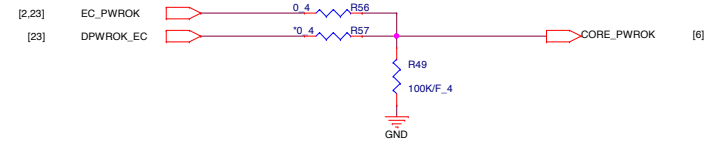


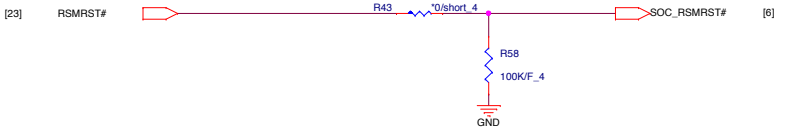


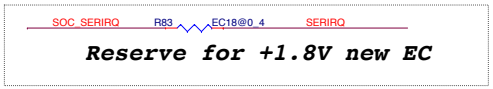


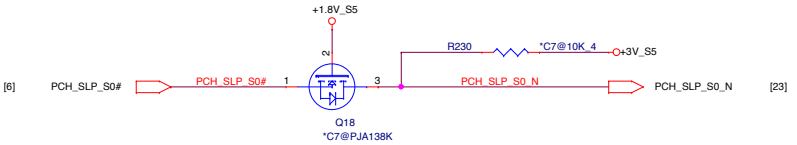


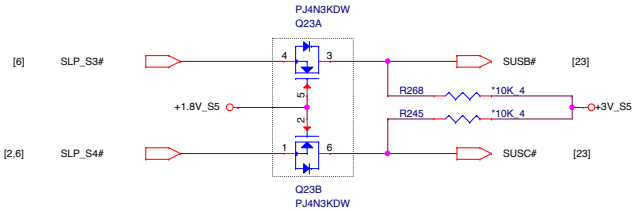


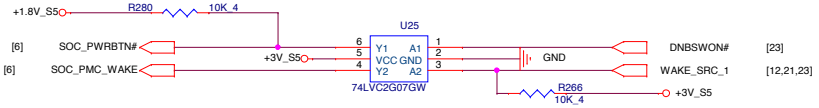


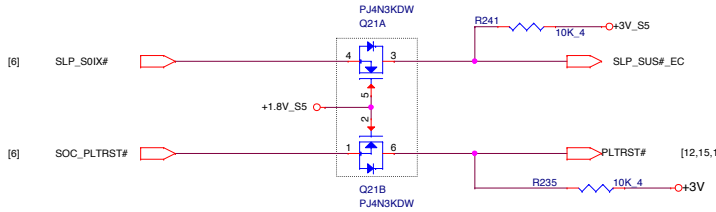


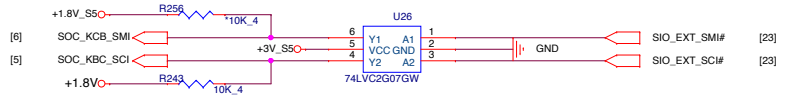


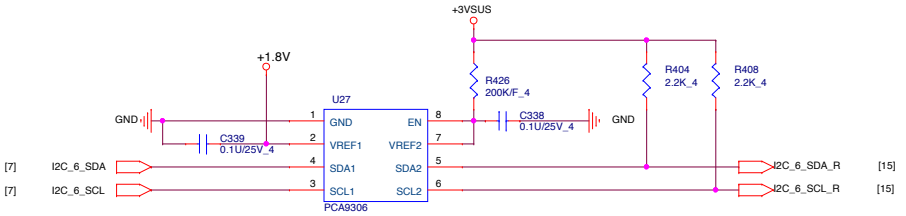


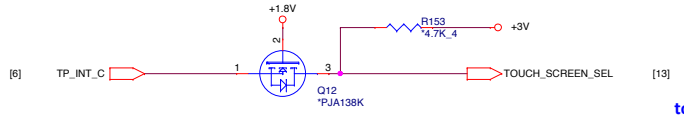




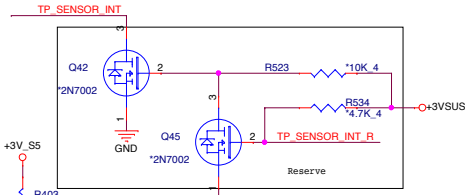


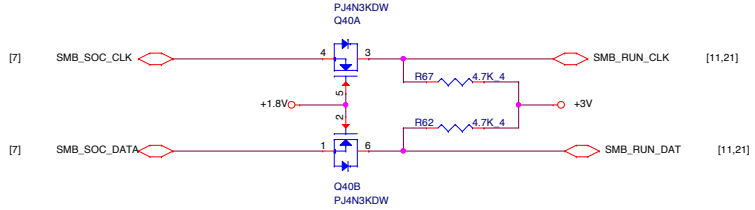


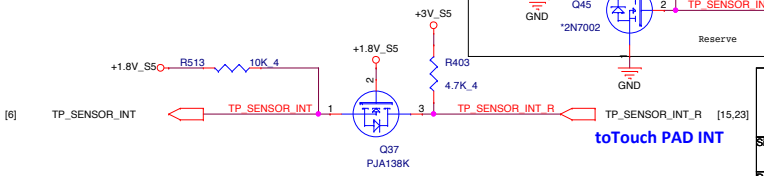




toTouch screen INT







toTouch PAD INT

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KEYBOARD (KBC)

<20110214(E1A)>
Change CP1~CP6 footprint from
8p4r-0402-smt to 8P4R, for SMT open issue.

<EMI>

CN17

KB CONN

0603 size

INTERNAL KEYBOARD STRIP SET (KBC)

RP6 10K_10P8R

UnStuff

R394 *10K_4

TOUCH PAD (TPD)

note: change to +3V_S5
other level sheft need to change power rail

15

40mil

CN18

TP_CN

ACER DEFINE
VDD
PS2-CLK
PS2-DATA
GND
I2C-DATA
I2C-CLK
ATTN (INT)
SER-OFF.

Touch pad I2C

Touch pad INT

Touch pad ON/OFF

TPM (TPM)

U16

U24

*TPM_S@NPCT620/650_TSSOP28

AL000650K00 : NPCT650AA0WX
AL009655K01 : SNI SLB9655TT1.2

*TPM@G2129TL1U

TPM_I for 英飛凌---- default

TPM_N for 新 唐

note: serie need to add level shift

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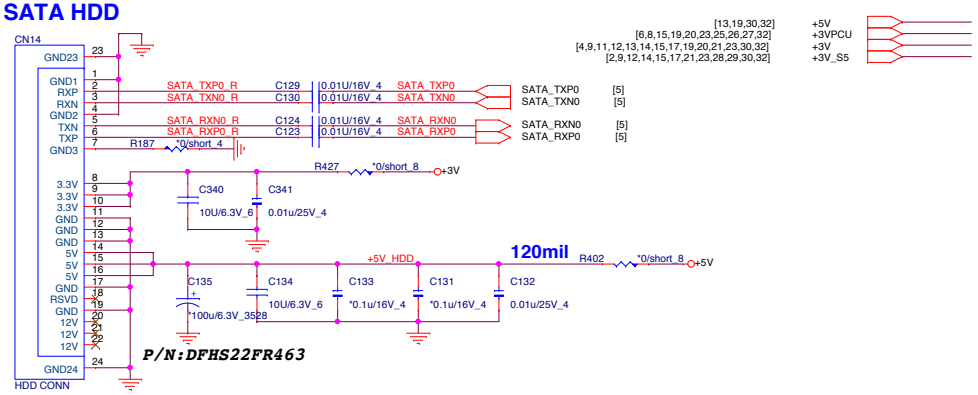
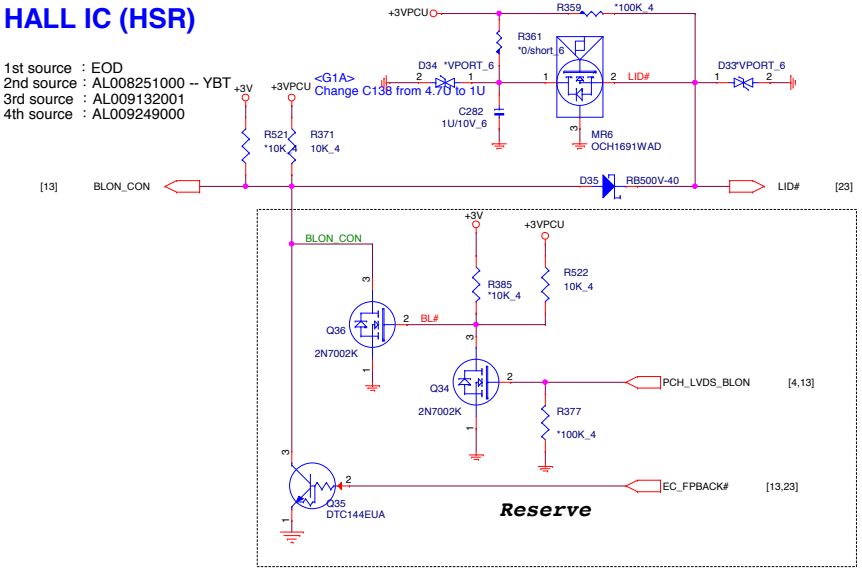
SATA HDD



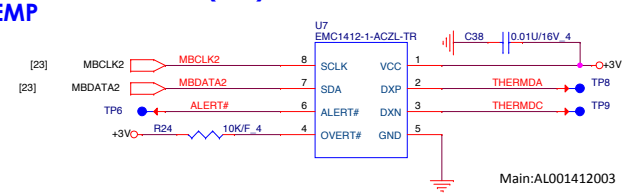
eMMC

HALL IC (HSR)

1st source : EOD
2nd source : AL008251000 -- YBT
3rd source : AL009132001
4th source : AL009249000

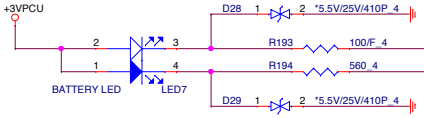


CPU Thermal sensor(THS) / MB Local TEMP



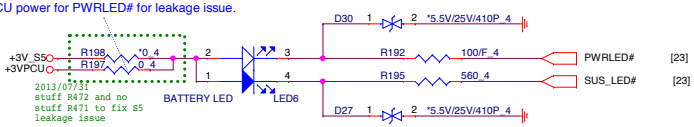
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

Battery indicator

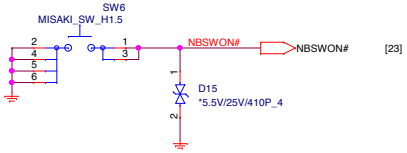


PWR indicator

<20130722> Reserve +3VPCU power for PWRLED# for leakage issue.



PWR button



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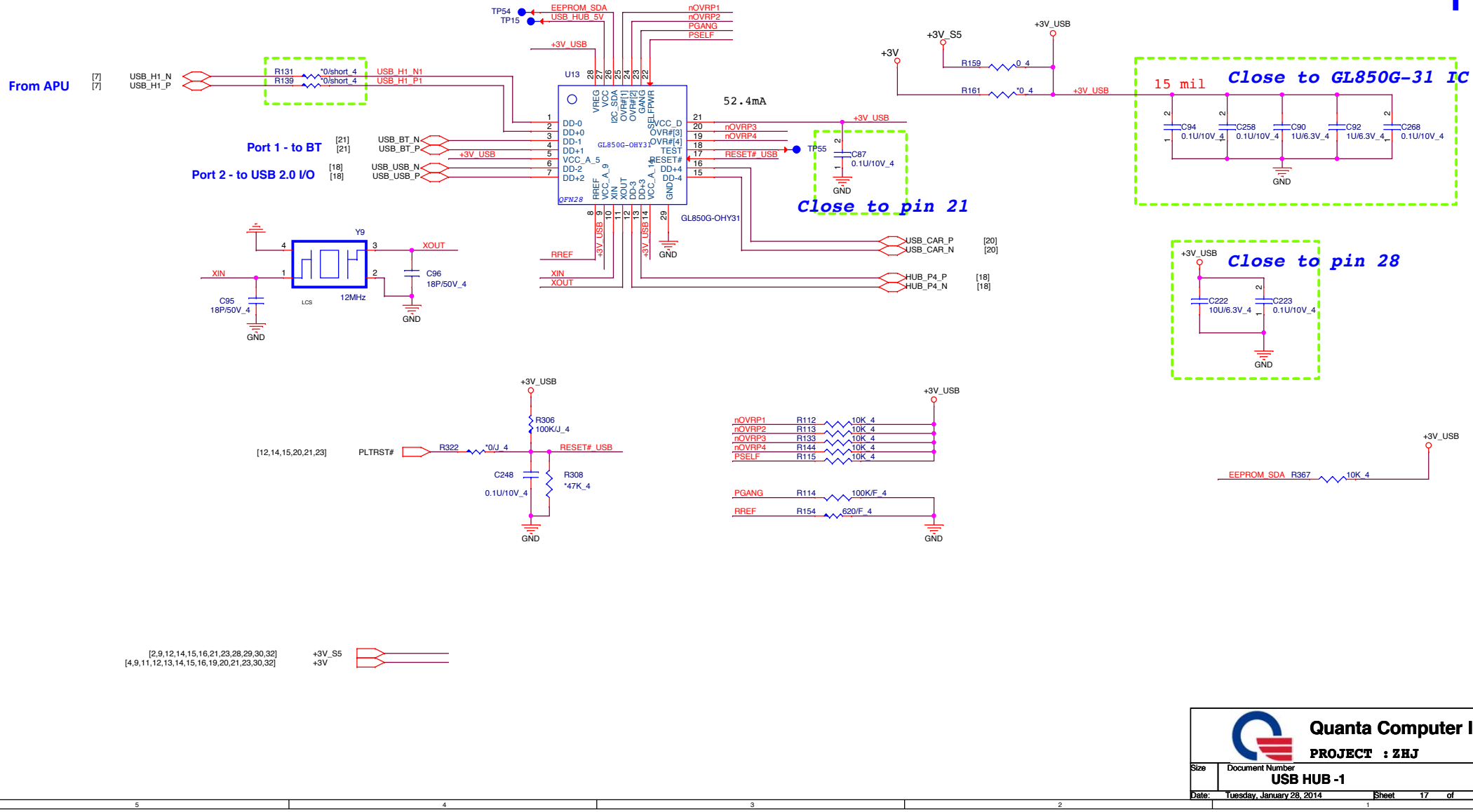

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	USB HUB -1	1A

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[6,26,28,29,30,31,32] +5V_S5

Close USB3.0

5VUSB_0 — C149 470P/50V_4 — C148 0.1U/10V_4 — C20 100U/6.3V_1206

USB2.0 connector P/N:
DFHS04FR487

CN6 USB3.0 CONN
1 VBUS
2 D-
3 D+
4 GND
5 SSRX-
6 SSRX+
7 GND
8 SSTX-
9 SSTX+

USB 3.0 Connector

From APU
[7] USBP0-
[7] USBP0+
R18 0_4
R17 0_4
USBP0-_R
USBP0+_R

USB30_RX1-
USB30_RX1+
R12 18_4
R13 18_4
USB30_RX1-_R
USB30_RX1+_R

From APU
[7] USB30_TX1-
[7] USB30_TX1+
C25 0.1U/10V_4
C26 0.1U/10V_4
USB30_TX1-_C
USB30_TX1+_C
R19 18_4
R20 18_4
USB30_TX1-_R
USB30_TX1+_R
C17 *1.6P/50V_4
C18 *1.6P/50V_4

From APU
[7] USB30_RX1-
[7] USB30_RX1+
C23 *1.6P/50V_4
C22 *1.6P/50V_4

USB 2.0 Connector

+5V_S5 — C146 4.7U/10V_6 — U19 G524B2T11U (IN, OUT, GND, EN, /OC) — 5VUSB_0

G547E2P81U: Enable: Low Active /2.5A
P2 - USB 2.0
2A

[23] USBON#
[7] SOC_USB_OC0
From HUB

C21 100U/6.3V_1206
C145 0.1U/10V_4 <Layout note> Close to CONN

USBP1-_CN
USBP1+_CN
D7 *5V/30V/0.2p_4
D8 *5V/30V/0.2p_4

CN8 USB_CON (VDD, D-, D+, GND4, GND5, GND6, GND7, GND8)

EMI

[17] USB_USB_N
[17] USB_USB_P
L7 EMI@MCM2012B900GBE/400mA/90ohm
USBP1-_CN
USBP1+_CN

+5V_S5 — C93 4.7U/10V_6 — U14 G524B2T11U (IN, OUT, GND, EN, /OC) — 5VUSB_1

G547E2P81U: Enable: Low Active /2.5A
P4 - USB 2.0
2A

USBON#
[7] SOC_USB_OC1
SOC_USB_OC1
From HUB

C100 100U/6.3V_1206
C88 0.1U/10V_4 <Layout note> Close to CONN

USBP4-_CN
USBP4+_CN
D23 *5V/30V/0.2p_4
D22 *5V/30V/0.2p_4

CN12 USB_CON (VDD, D-, D+, GND4, GND5, GND6, GND7, GND8)

USB 2.0 Connector

change P/N, footprint OK

EMI@MCM2012B900GBE/400mA/90ohm
[17] HUB_P4_N
[17] HUB_P4_P
L16
USBP4-_CN
USBP4+_CN

EMI

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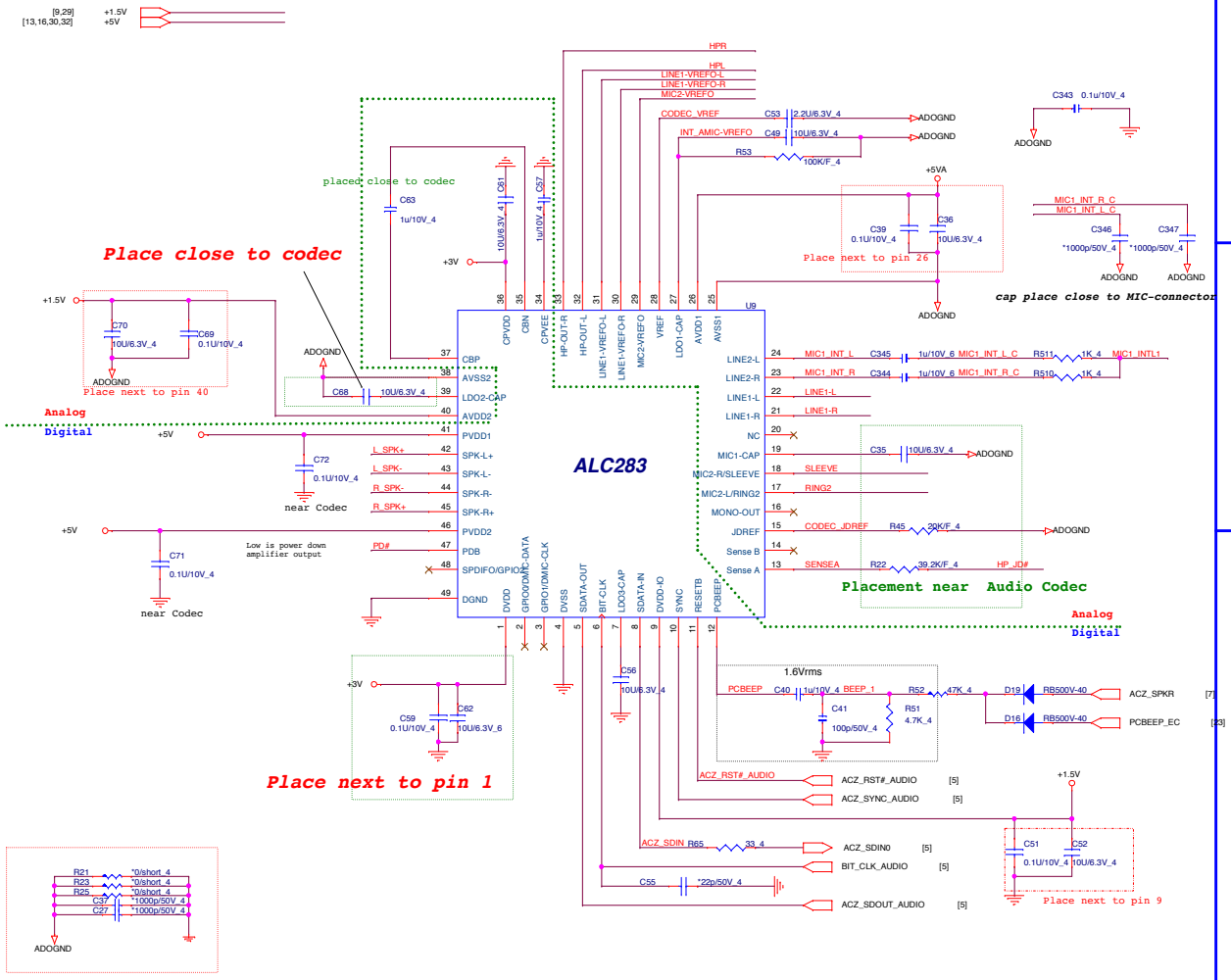
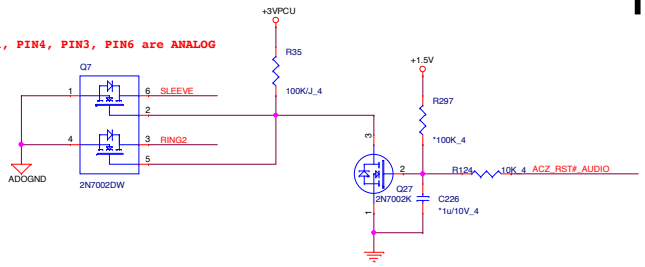
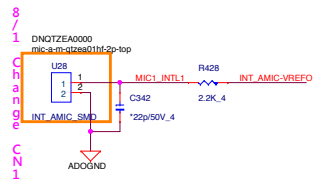
Codec(ADO)



Grounding circuit(ADO)



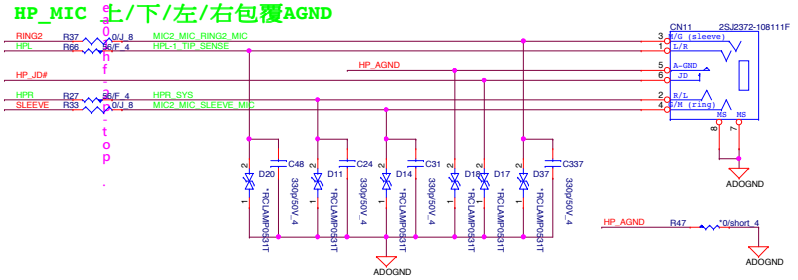
INT MIC array

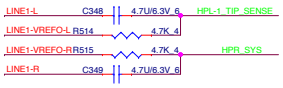


8/1 Change CN1 footprint to mic-a-m-qtzea01hf-2p-top.

note : change next P/N: DFTJ06FR653
CONN DIP PHONE JACK 6P FR(H4.5)
foot print: phjk-2sj3072-108111f-6p

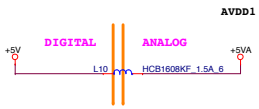
HP_MIC 七/下/左/右包覆AGND



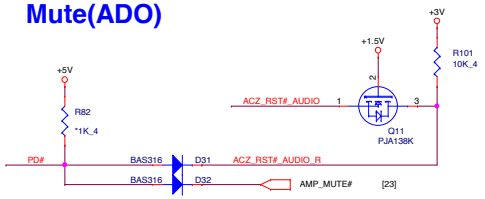


Close to Audio Jack

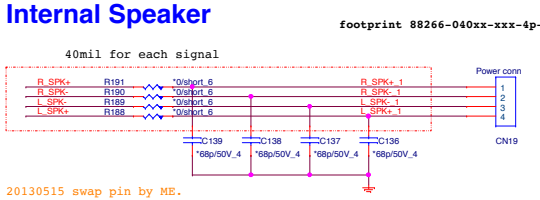
Codec PWR 5V(ADO)



Mute(ADO)



Internal Speaker



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	ALC283/HP/SPK	2A
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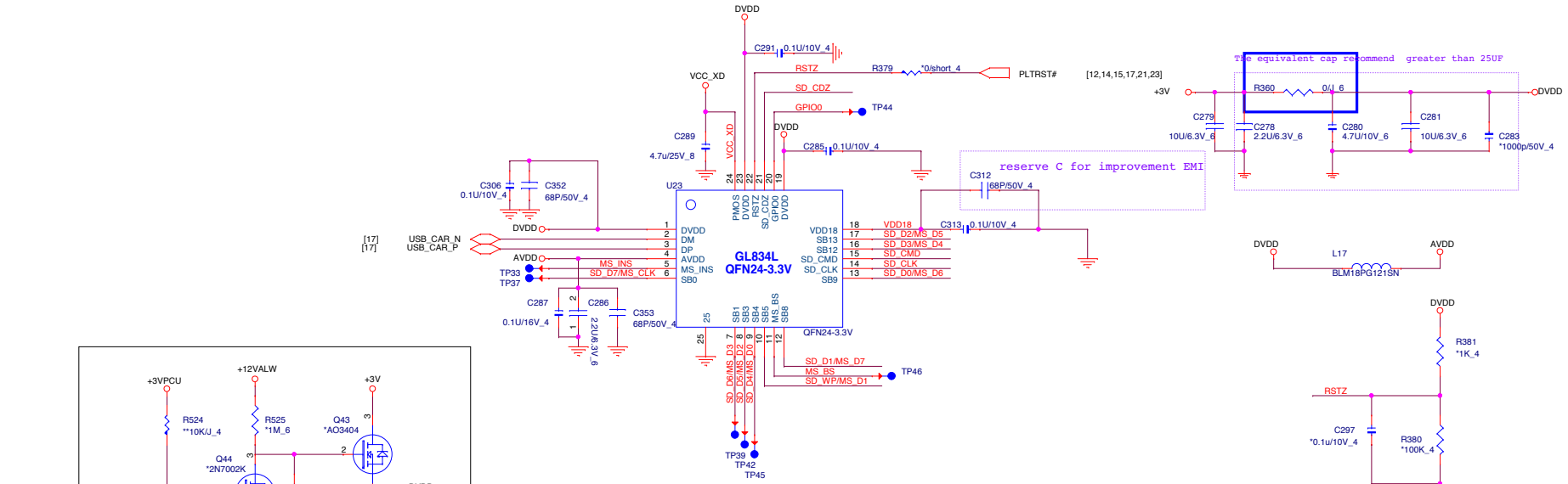
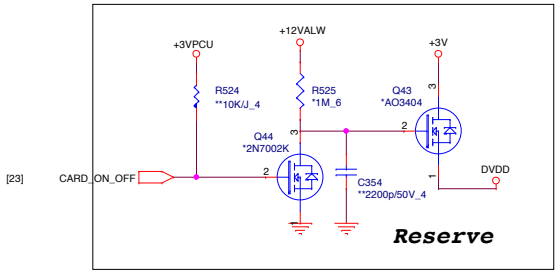
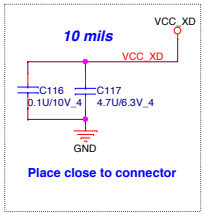
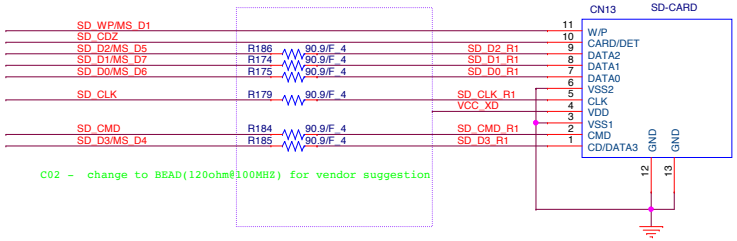
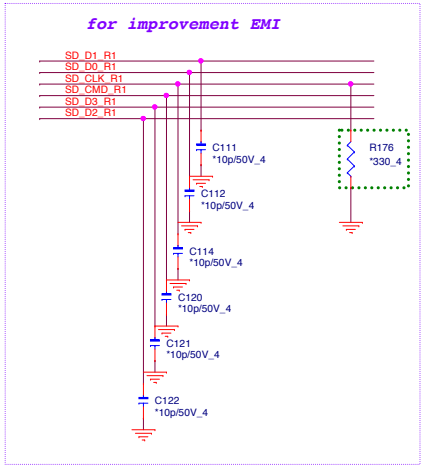




SD/MMC CARD READER (MMC)







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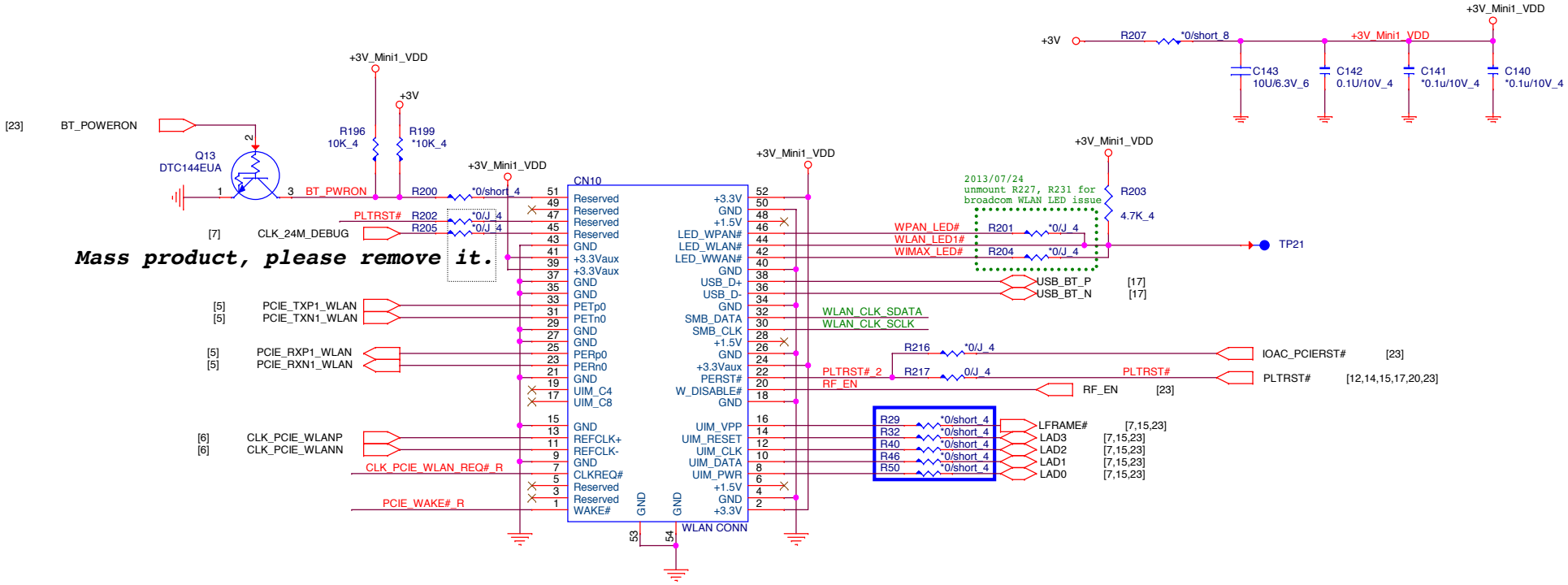
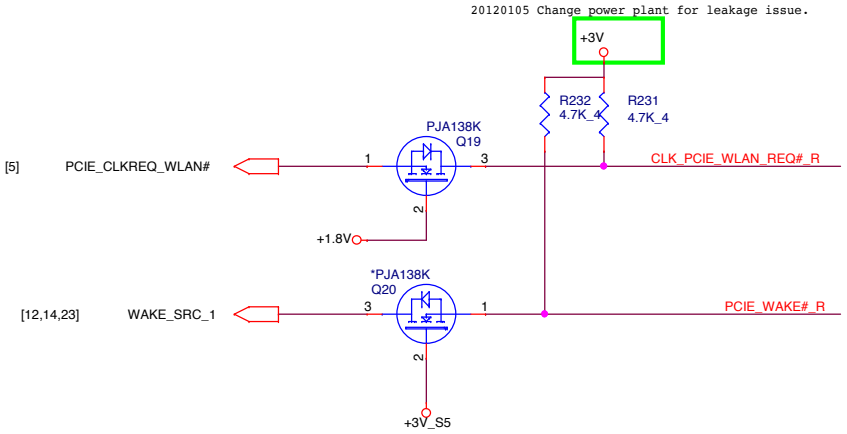
WLAN

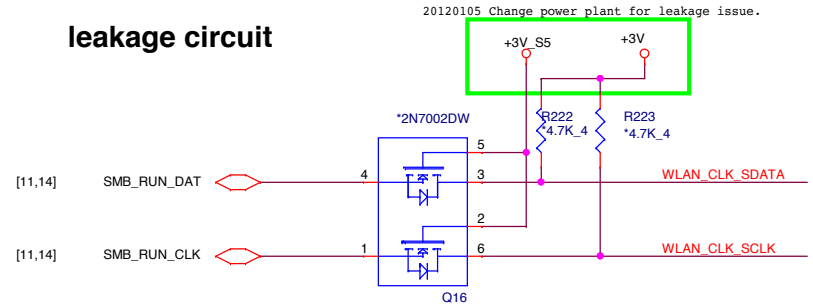


20120105 Change power plant for leakage issue.



leakage circuit

20120105 Change power plant for leakage issue.



[4,5,6,7,9,12,13,14,15,23,32] +1.8V
[4,9,11,12,13,14,15,16,17,19,20,23,30,32] +3V
[2,9,12,14,15,16,17,23,28,29,30,32] +3V_S5

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	WiFi & BT	1A
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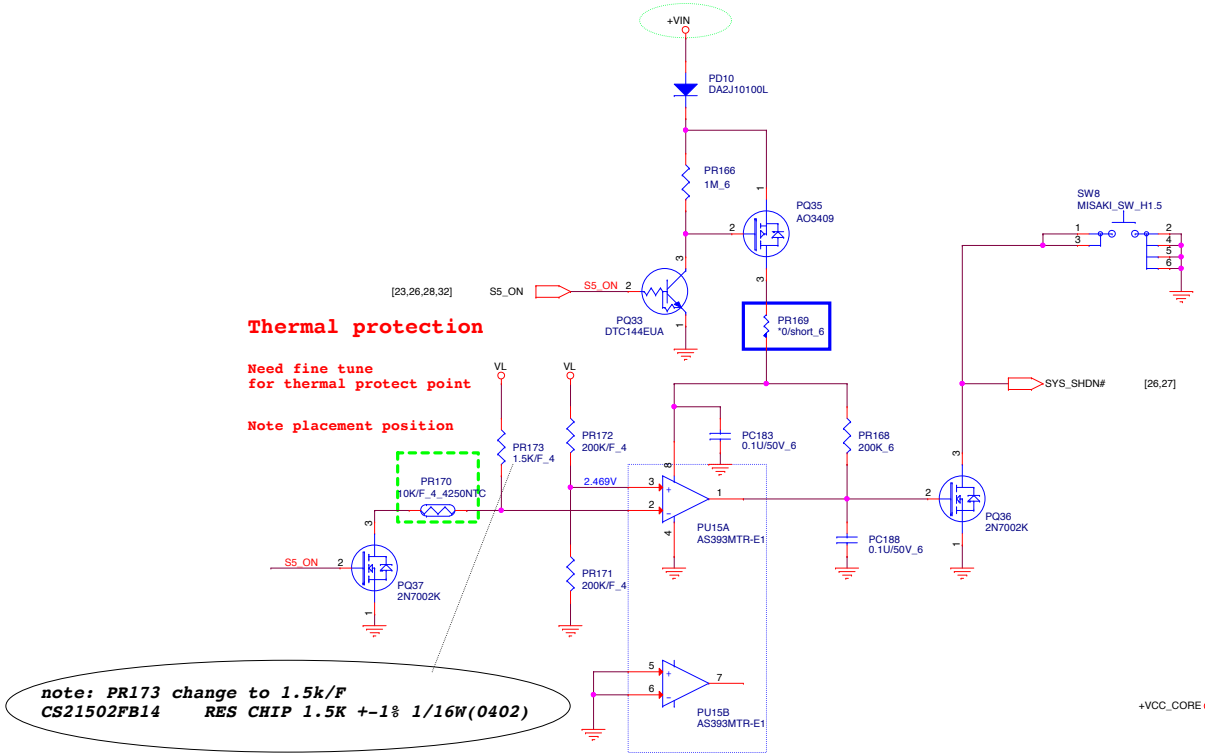
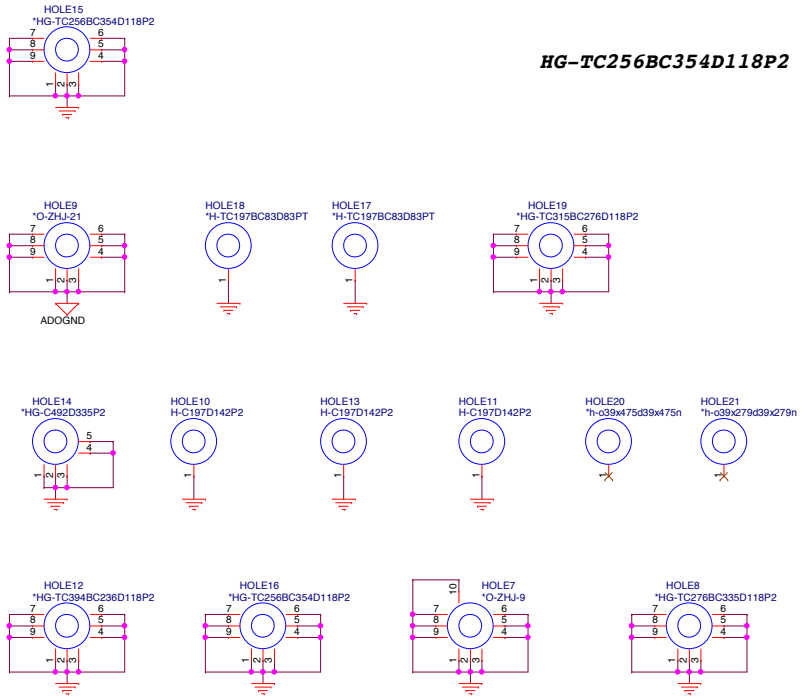
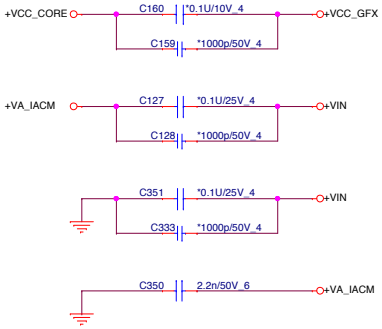
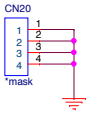


For EC control thermal protection (output 3.3V)







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PROJECT : ZHJ

Size	Document Number	Rev
	Thermal / Hole	2A

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1.8V p/n: AJ009850F02
Discription:IC CONTROLLER(128P)NPCE985LB1DX(LQFP)

note:
GPIO75 EMU_LIDTouch panel enable/disable#Follow ZEA -->ZHJ None
GPIO70 TP_EN_ECTouch pad enable/disable# -->ok
GPIO27 TP_INT_EC#Touch pad interrupt

EC(KBC)

985L-A0 connects to +3v / 985L-B1 connects to +1.8v

note:change EC p/n: into AJ009850F02

30mil

0.03A(30mils)

220121130 change to 39p capacitor for ESD

985L-A0 connects to +3vpcu / 985L-B1 connects to +1.8v_s5

2013/07/30
Reserve R477, R478 for EC chip PU function issue.

note: gpio27 -->TOUCH_PAD_INT

Reserve for writing ME ROM

PECI interface should be used on Bay Trail platform, thus VTT pin can wire to GND and PECI signal can be left un-connected.

prevent leakage : EC internal pull high

Q41 2N7002K

Note: GPIO75 (pin82) for TOUCHPANEL_ON

pin91 in 985L is 1.8V only

<20090721_FAE suggestion> Stuff 100K and close to EC side for improving power consumption

20111129 add 33ohm series resistor and for EC FAE suggestion contact to SPI 4M ROM and close to Flash.

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU

SM BUS PU(KBC)

2013/07/31 SMBus Tr fail (spec 1000 ns max, result 1046 ns) Change PU resister(R424,R428) from 10K to 4.7K

H_PROCHOT#

Q47 need Replacement at BOT layer.

SPI NOR FLASH

soic8-6-1_27-pm25lv010a
AKE35ZN0N00
IC FLASH(8P) W25X10CLSNIG(SOIC)

985L-A0 connects to +3vPCU / 985L-B1 connects to +1.8v_s5

HWPG(KBC)

<20130722>Change power from +3V to +3V_S5 for power sequence issue

20120217 Change R630 from10k to 47k for S5 current reduce..

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PROJECT : ZHJ

Size	Document Number	Rev
	NPCE885/FLASH	2A

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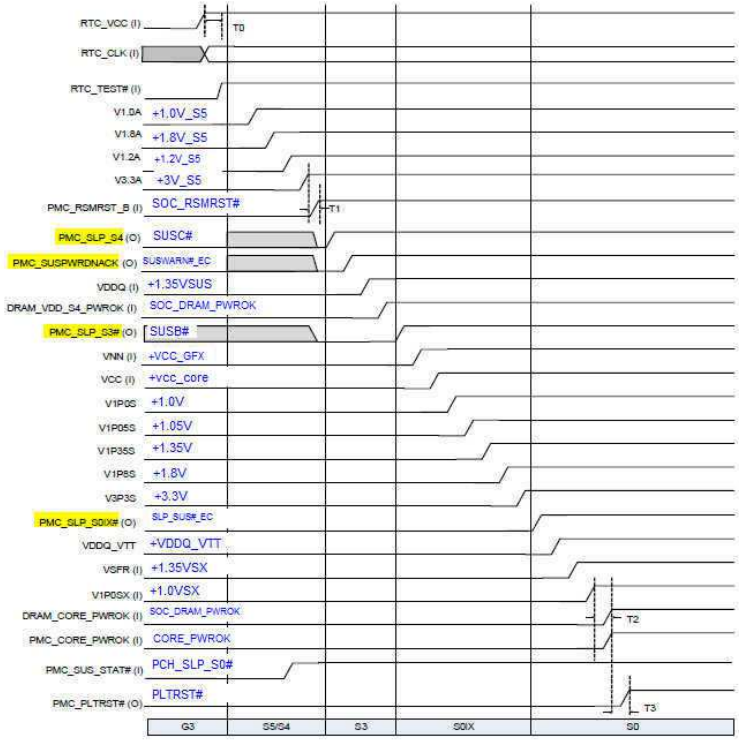
Bay Trail-M S4/S5 to S0 (Power Up) Sequence



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Size	Document Number	Rev
	Power sequence	1A

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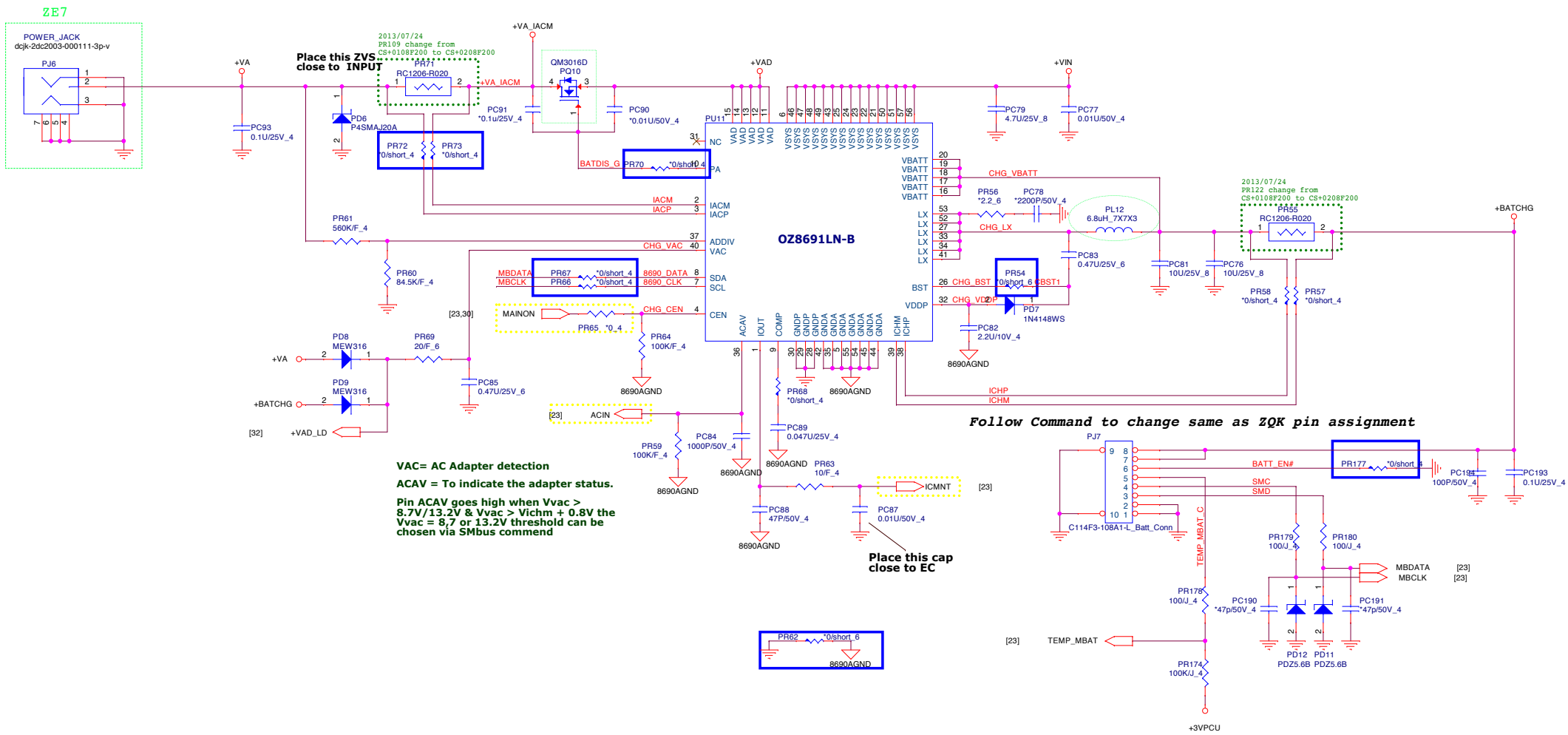

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PROJECT : ZHJ

Size	Document Number	Rev
	Charger (OZ8690ALN)	1A

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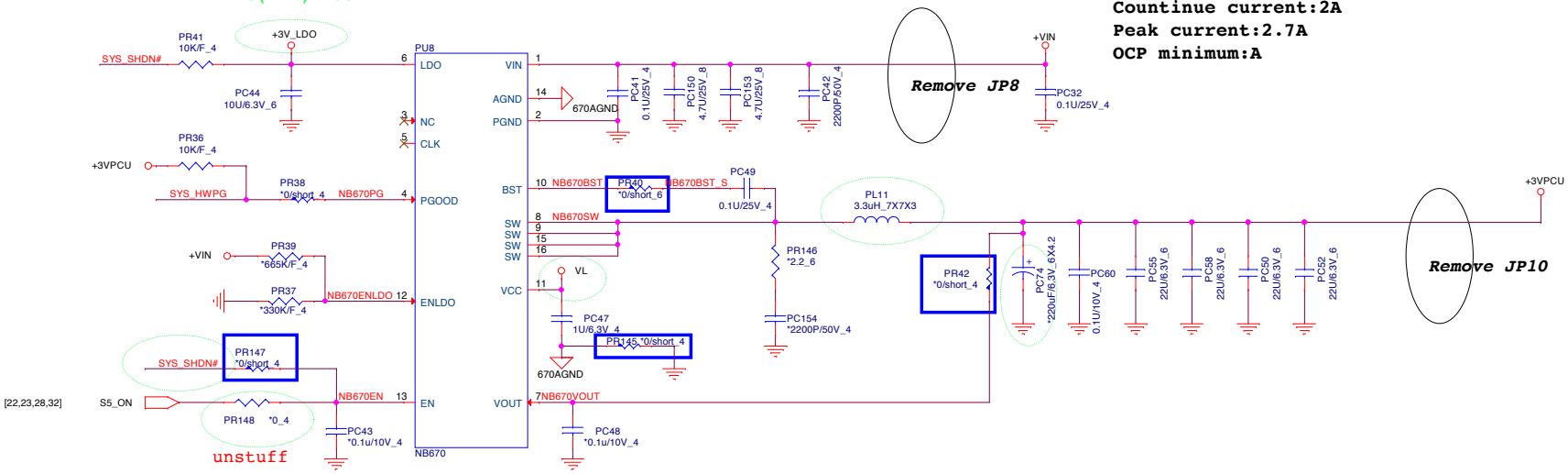
DC/DC +3VPCU/+5V_S5

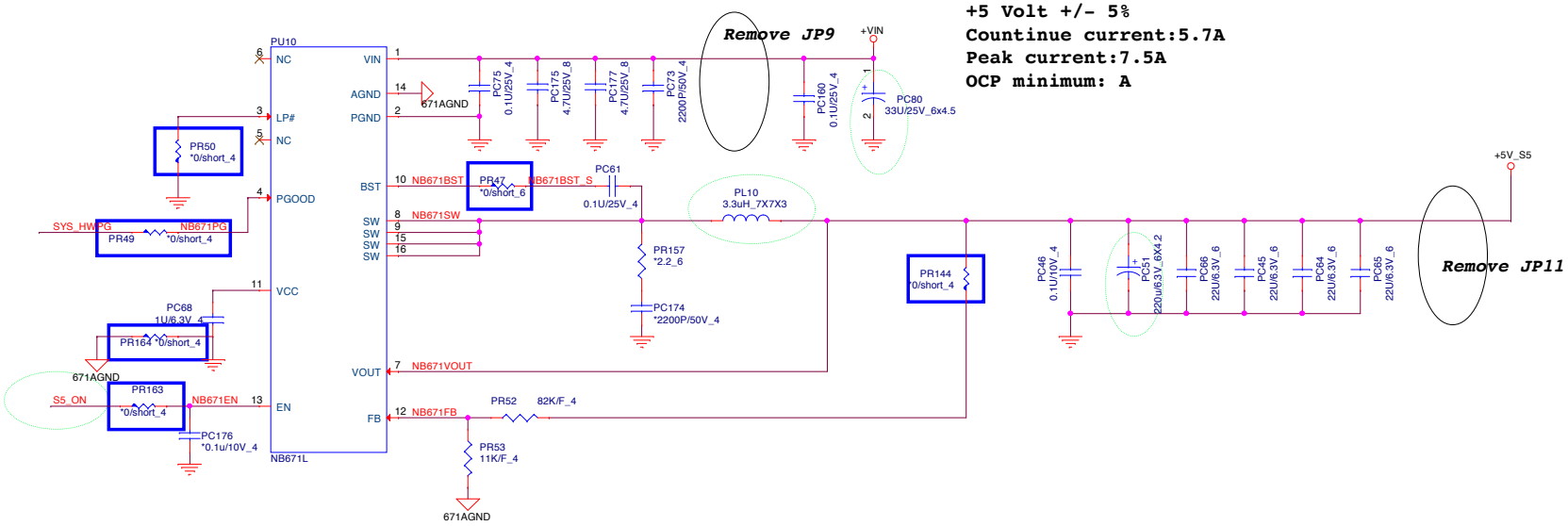
+3VPCU [6,8,15,16,19,20,23,25,27,32]
+5V_S5 [6,18,28,29,30,31,32]
SYS_SHDN# [22,27]

LDO(MAX)=100mA

+3.3 Volt +/- 5%
Countinue current:2A
Peak current:2.7A
OCP minimum:A



+5 Volt +/- 5%
Countinue current:5.7A
Peak current:7.5A
OCP minimum: A



Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: 3/5VS5 (NB670/NB669)	Rev: 1A
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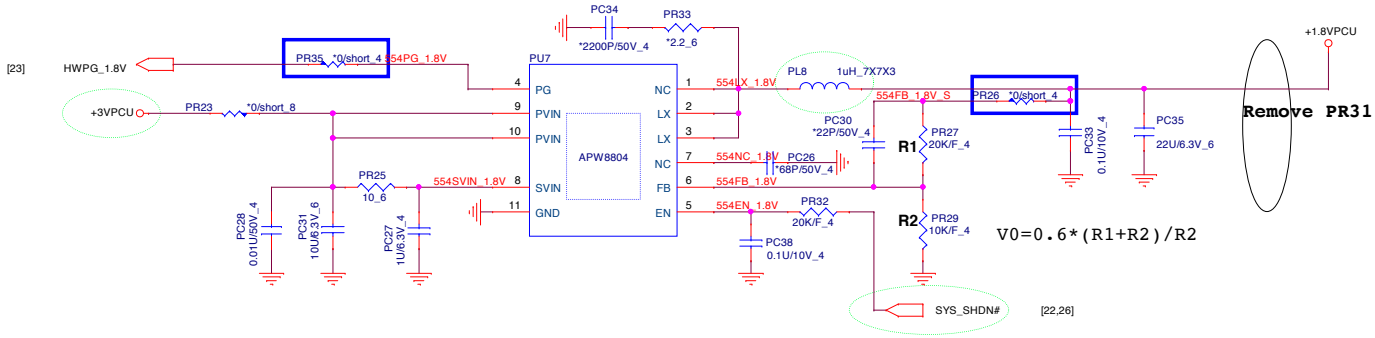
[32] +1.8VPCU

[6,8,15,16,19,20,23,25,26,32] +3VPCU

+1.8V Volt +/- 5%
Countinue current:0.08A
Peak current:0.11A
OCP minimum:A



Quanta Computer Inc.			
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Size	Document Number +1.8VPCU		Rev 1A
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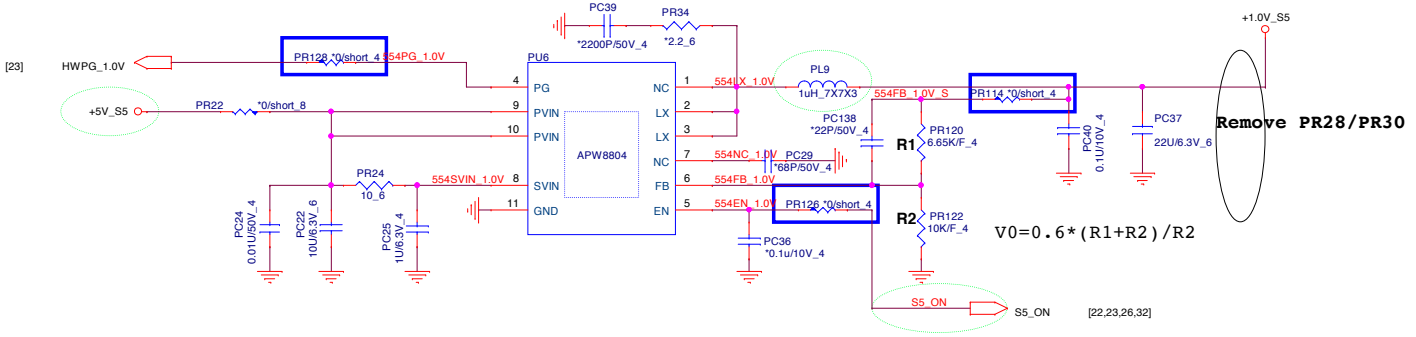
[9,32] +1.0V_S5
[6,18,26,29,30,31,32] +5V_S5
[2,9,12,14,15,16,17,21,23,29,30,32] +3V_S5

+1.0V Volt +/- 5%
Countinue current:2.4A
Peak current:3.2A
OCP minimum:A



Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: +1.0V	Rev: 1A
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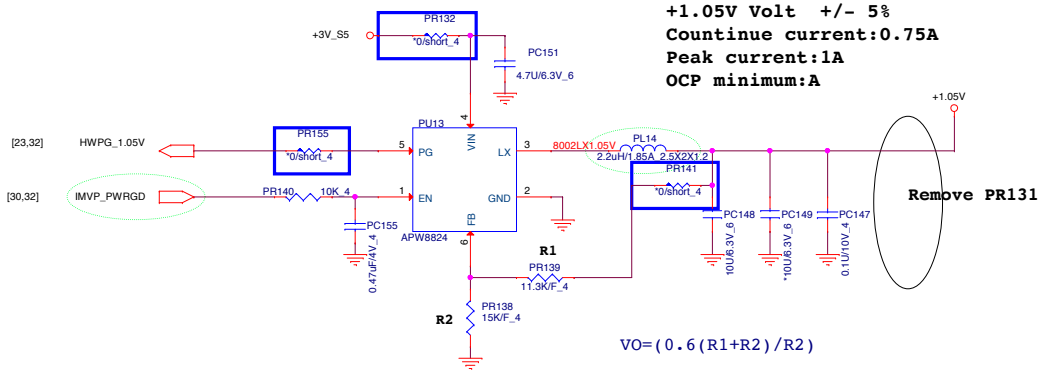
[2,9,12,14,15,16,17,21,23,28,30,32] +3V_S5

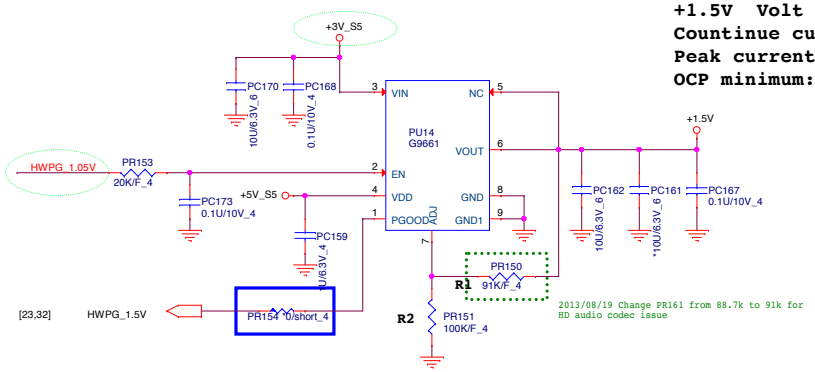
[9] +1.05V

[9,19] +1.5V



+1.05V Volt +/- 5%
Countinue current:0.75A
Peak current:1A
OCP minimum:A

VO=(0.6(R1+R2)/R2)



+1.5V Volt +/- 5%
Countinue current:0.023A
Peak current:0.03A
OCP minimum:A

VO=(0.8(R1+R2)/R2)
R2<120Kohm

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PROJECT : ZHJ

Size	Document Number	Rev
	+1.05V/1.5V	1A

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20130617 Change +1.05V to +1.0V

Close to VR

VR_SVID_ALERT# close to CPU

VR_SVID_DATA and VR_SVID_CLK close to VR

[5,6,9,32] +1.0V
[8,9,22] +VCC_GFX
[13,22,25,26,31,32] +VIN
[6,18,26,28,29,31,32] +5V_S5

Parallel

Close to the CPU side.

PU12 ISL95833HRTZ-T

AXG

Remove JP6

+VCC_GFX
TDC : A
PEAK : 14A
OCP : A
Width : mil

GFX_CORE Load Line : -5.9mV/A for 2.xW SDP

Close to the VR side.

Close with AXG inductor

Core

Remove JP7

delete PC11

+VCC_CORE
TDC : A
PEAK : 12A
OCP : A
Width : mil

VCORE Load Line : -5.9mV/A for 2.xW SDP

Close to the VR side.

Close with phase1 inductor

Close to the CPU side.

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Size | Document Number: +VCC_CORE/+VGFX (ISL95833) | Rev 2A
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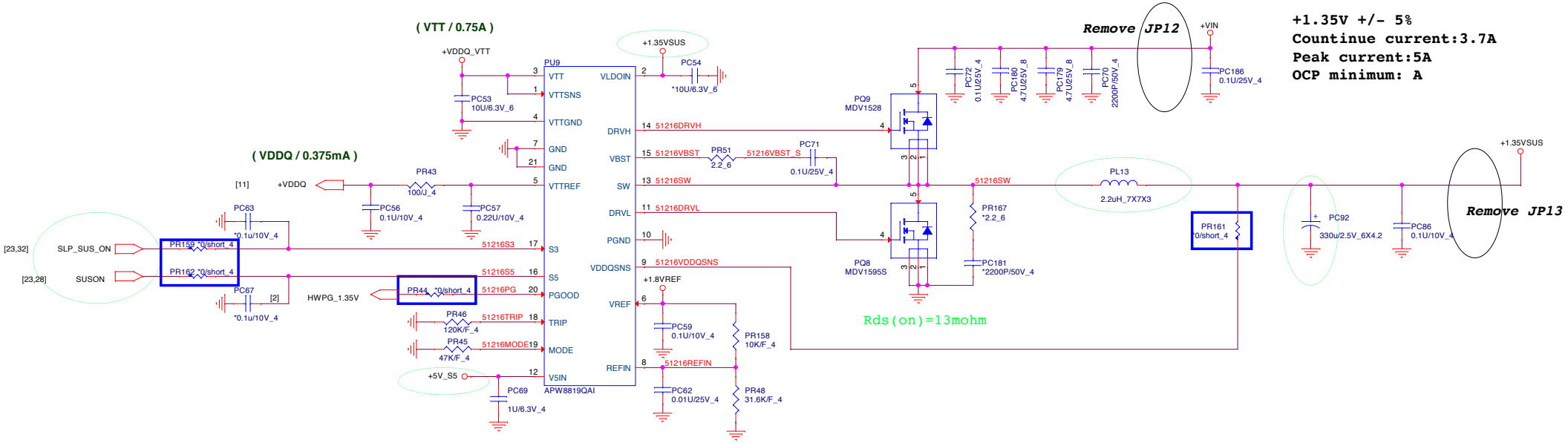
[2,8,11,32] +1.35VSUS

[11] +VDDQ_VTT

[6,18,26,28,29,30,32] +5V_S5



Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: DDR3 (APW8819)	Rev: 1A
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20130620 Reserved RC delay

PU16
G5934RZ1U

2.8A
2.5A
0.281A
1.43A
0.038A
0.056A
0.008A
0.034A
0.64A

20130717 no S0ix power plane

Quanta Computer Inc.	
PROJECT : ZHJ	
Size	Document Number: Dis-charge IC (G5934)
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B stage:

1. Page4 ,SWAP DDI0 DDI1 port
2. Page5 , Delete NGFF function , C517,C516,C272,C275,R234,R233
3. Page6 , Mount R310,R311,R353,R354 for 1.8V EC
4. Page7 , Change R118 & R119 value form *2.2K to *560K (NC)
5. Page8 , Delete C60
6. Page12 , Change CN9 (LAN) of P/N; Add R516 ; Off*R298, *Q25
7. Page13 , Add toutch sreen ON/OFF net " EMU_LID" to CN16
8. Page14 ,Change power for TP wakeup function, mount R58,Delete Q9,Q10 Add Q40 for 0C issue.
   Delete Q26,Q22,Q38; Add U25, U26, U27 C339, C338, R426; chamge R404 & R408 value to 560 Ohm ;
   mount R266; remove R256; Add R513 for TP-int.
   not mount R89,U10,mount R83 for 1.8V of EC
9. Page15 , Change power rial , change/add *R172 (0 Ohm) of value, Add U24 & R419; Delete R410,R409 short pad; remove R407, Add R411
10. Page16 , Add C340, C341 & R427 for NGFF/SSD
11. Page19 , Change CN11(Audio) of P/N & footprint ; Add D37 & C337 ; delete R34,R28,U6,D12,D13,C6,C30,C34;
    Change R27,R66 value; Add U28,R428,R511,R510,R514,R515,C342,C344,C345,C348,C349.
12. Page22 ,Remove SW7, change PR173 of value
13. Page23 , Change EC of P/N; add R420 for TP_INT to EC ; Cgange R391 value from 47K to 4.7K
    Add Q41 prevent leakage (EC internal pull high); mount R395,R370 for EC
    not mount R167,R169,R170,R168,R355,R366,U15 for 1.8V of EC
    mount C284, R165,R357,R350,R351,R356,R364 for 1.8V of EC
14. Page30 ,Rmove PC11 for RF request

C stage:

Change 0 hm to short pad : PR100,PR105,PR110,PR132,PR177,PR22,PR23,PR78,PR97,R106,R107
R107,R122,R130,R131,R134,R139,R173,R188,R189,R190,R191,R200,R207
R229,R238,R240,R244,R257,R275,R281,R282,R283,R288,R290,R294,R309
R313,R315,R316,R321,R325,R331,R332,R333,R335,R36,R361,R372,R373
R375,R379,R390,R400,R402,R427,R43

1. Page5 , Mount R286
2. Page6 , Mount R41, Delete *R64
3. Page13 , Remove R86,R87,R69,R72,D21,C75 for LDC BLON
4. Page16 , chage R371 power rail to 3VPCU, remove *R385 & add R522 ; Mount Q34,Q35,Q36, R385,R377 for LDC BLON
5. Page17 , Remove R369
6. Page19 , R66,R27 change P/N from 47 to 56 Ohm; change R37 & R33 footprint from 0402 to 0805
7. Page20 , C312 chage to 68P, Add C352, C286 68P; change R184,R185,R186,R174,R175,R179 to 91 Ohm for vendor suggestion
8. Page26 , Remove JP8,JP9,JP10,JP11
9. Page27 , Remove PR31
10. Page28 , Remove PR28,PR30
11. Page29 , Remove PR131
12. Page30 , Remove JP6,JP7
13. Page26 , Remove JP12,JP13
14. Page21 , Remove Q20

D stage:

1. Page4 ,change R31 & R300 to 200K
2. Page6 ,change CLK port0 to port2 ; change D36 footprint change P/N
3. Page13 ,Remove R111
4. Page14 ,Add *R523,*R534,*Q42 & *Q45 for +3vsus ;
   Q12 gate change to 1.8V ; Remove R153 & Q12
5. Page15 , Change R407 power reail to +3vsus; Delete R177; TPM co-layout
6. Page16 , change R192,R193 from 33 to 100 Ohm; R194,R195 from 220 to 560 Ohm; Remove R377
7. Page17 , Delete *U17,*R363,*R369,*C113, chage R154 of value
8. Page18 , Delete L6,L8,L9, R16,R15,mount L7 ; Delete 320, R324, mount L16 for EMI; Change R12,R13,R19,R20 of value from 0 to 18 Ohm
9. Page20 , not mount C111,C112,C114,C120,C121,C122 & R176,Add R360
   Reserve *R524,*R525,*Q43,*Q44,*C354 for card reader on/off; Swap CN13 Pin10 & Pin11 net name
10. Page22 , Mount C350 for EMI request
11. Page30 , Change PU12 footprin; Add *PR186,*PR187,*PR188,*PC198,*PC199,*PQ38,*PQ39,*PQ40.

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PROJECT : ZHJ		
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