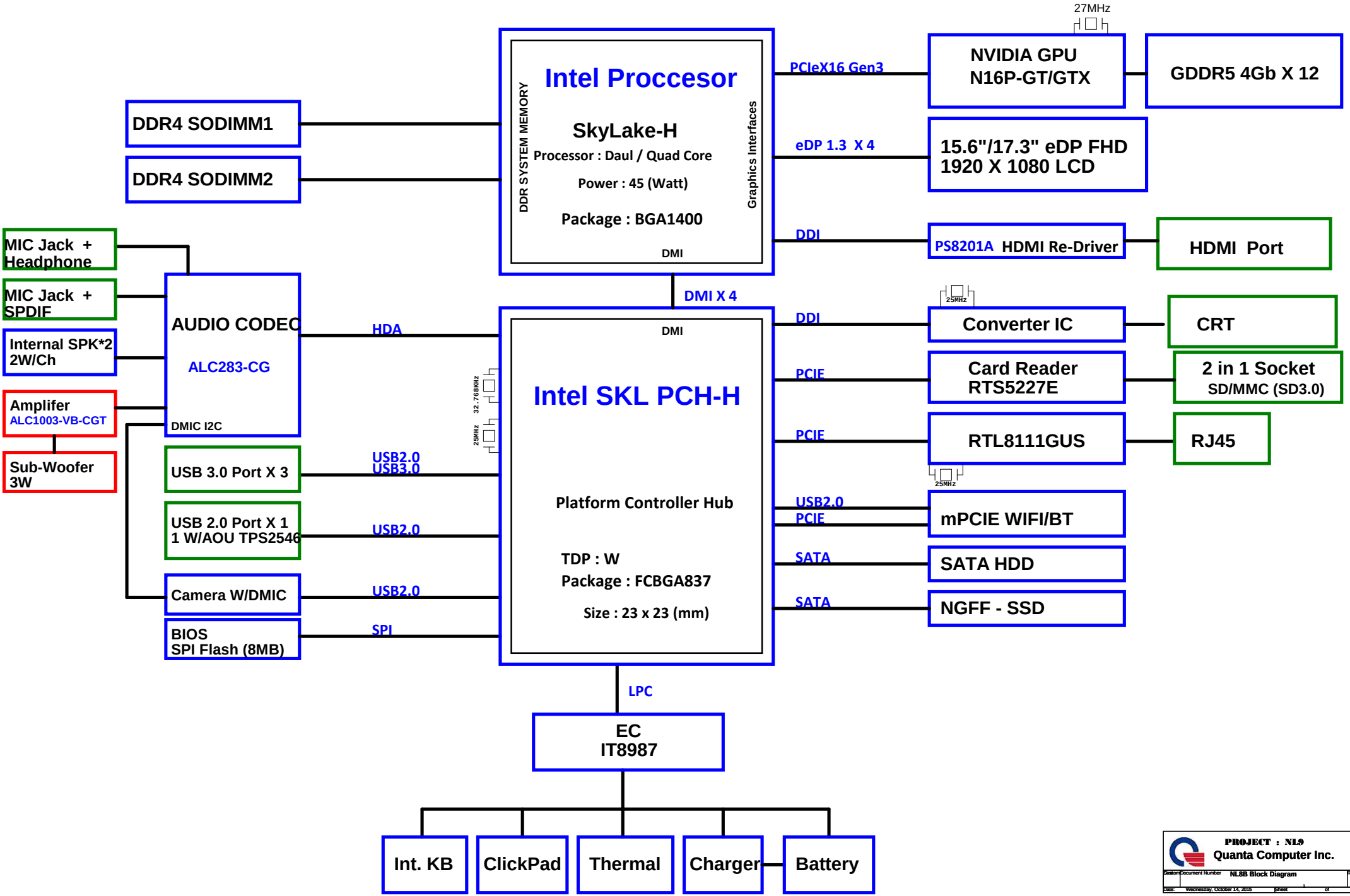
NL9 Block Diagram

01



PROJECT : NL9
Quanta Computer Inc.
System Document Number NL8B Block Diagram Rev A
Date: Wednesday, October 14, 2015 Sheet 1 of 61

SKYLAKE Processor (CLK,MISC,JTAG)

02

Host CLK:
Trace length < 11000 MILS
Trace spacing = 15 ,20 MILS, Impendence 90 ohm

HPECI Ra,Ca need placement close to PCH.
H_PECI (50ohm) Trace Length: <0.5 iches
(11) PCH_PECI
(32) EC_PECI
R504 12.1/F_4
Ra
C812 *47P/50V_4
Ca
EC_PECI

PROCHOT# (50ohm)
Trace Length <11 inches
(32,33,39,49) H_PROCHOT#
R388 499K/F_4
H_PROCHOT# R
C663 *47P/50V_4
Cb
Cb need placment near VR
(16) DDR_VTT_CNTL
DDR_VTT_CNTL

CPU RESET#
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches
(11) CPU_PLTRST#R
(12,20,24,27,29,30,32,50) PLTRST#
R363 *1.5K/F_4
R367 *750/F_4

PROCPWRGD (50ohm)
Trace Length: 1~11.25 inches
(10) PROCPWRGD
R25 *10K_4

PM_SYNC (50ohm)
Trace Length: 1~11.25 inches
(11) PM_SYNC

THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches
(11,16,17,32) PM_THRMTRIP#

(13) SKTOCC_N_R
R372 *0_4/S
SKTOCC_N

+VCCSTPLL
R375 *10K_4
CATERR#

(11) H_PM_DOWN
R389 20_4
H_PM_DOWN_R

U20E
SKYLAKE_HALO
BGA1440
5 OF 14
SKL_H_BGA_BGA

(11) CLK_CPU_BCLKP	CLK_CPU_BCLKP	B31 BCLKP
(11) CLK_CPU_BCLKN	CLK_CPU_BCLKN	A32 BCLKN
(11) CPU_PCI_BCLKP	CPU_PCI_BCLKP	D35 PCI_BCLKP
(11) CPU_PCI_BCLKN	CPU_PCI_BCLKN	C36 PCI_BCLKN
(11) CLK_DPLL_NSCCLKP	CLK_DPLL_NSCCLKP	E31 CLK24P
(11) CLK_DPLL_NSCCLKN	CLK_DPLL_NSCCLKN	D31 CLK24N
H_CPU_SVIDALRT#		BH31 VIDALERT#
VR_SVID_CLK_R		BH32 VIDSCK
H_CPU_SVIDDAT		BH29 VIDSOUT
H_PROCHOT# R		BR30 PROCHOT#
DDR_VTT_CNTL		BT13 DDR_VTT_CNTL
H_VCCST_PWRGD		H13 VCCST_PWRGD
PROCPWRGD		BT31 PROCPWRGD
PM_SYNC		BP35 RESET#
H_PM_DOWN_R		BM34 PM_SYNC
EC_PECI		BP31 PM_DOWN
PM_THRMTRIP#		BT34 PECI
SKTOCC_N_R		J31 THERMTRIP#
PROC_SEL#		BR33 SKTOCC#
+VCCSTPLL		BN1 PROC_SELECT#
CATERR#		BM30 CATERR#

CFG[0]	BN25 CFG0	TP8
CFG[1]	BN27 CFG1	
CFG[2]	BN26 CFG2	
CFG[3]	BN28 CFG3	
CFG[4]	BR20 CFG4	
CFG[5]	BM20 CFG5	
CFG[6]	BT20 CFG6	
CFG[7]	BP20 CFG7	
CFG[8]	BR23	
CFG[9]	BR22	
CFG[10]	BT23	
CFG[11]	BT22	
CFG[12]	BM19	
CFG[13]	BR19	
CFG[14]	BP19	
CFG[15]	BT19	
CFG[17]	BN23	
CFG[16]	BP23	
CFG[19]	BP22	
CFG[18]	BN22	
BPM#[0]	BR27 XDP_BPM0	TP3
BPM#[1]	BT27 XDP_BPM1	TP1
BPM#[2]	BM31 XDP_BPM2	TP7
BPM#[3]	BT30 XDP_BPM3	TP44
PROC_TDO	BT28 XDP_TDO_CPU	
PROC_TDI	BL32 XDP_TDI_CPU	
PROC_TMS	BP28 XDP_TMS_CPU	
PROC_TCK	BR28 XDP_TRST#_CPU	
PROC_TRST#	BP30 XDP_TRST#	XDP_TRST# (15)
PROC_PREQ#	BL30 XDP_PREQ#	XDP_PREQ# (15)
PROC_PRDY#	BP27 XDP_PRDY#	XDP_PRDY# (15)
CFG_RCOMP	BT25 CFG_RCOMP 49.9/F_4 R382	

Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

Processor pull-up (CPU)

H_PROCHOT# 1K_4 R373 +1.0V

XDP_TDO_CPU	R371	*51_4	+1.0V
XDP_TMS_CPU	R370	*51_4	
XDP_TDI_CPU	R21	*51_4	
XDP_PREQ#	R369	*51_4	
XDP_TRST#_CPU	R378	51_4	
XDP_TRST#	R23	51_4	

+VCCSTPLL
Ra
R360 *10K_4
Ra(R10804) Not install in SKL-H
PROC_SEL#
R365 *0_4

CPU CORE SVID

Layout note: need routing together and ALERT need between CLK and DATA.

+VCCSTPLL
CLOSE TO CPU
PLACE THE PU RESISTORS
R358 56.2/F_4
SVID ALERT
H_CPU_SVIDALRT# R362 220/F_4 VR_SVID_ALERT# (39)
C657 *0.1U/10V_4

PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE
+VCCSTPLL
R357 *54.9/F_4
SVID CLK
VR_SVID_CLK_R R361 *0_4/S VR_SVID_CLK (39)

CLOSE TO CPU
PLACE THE PU RESISTORS
+VCCSTPLL
R359 100/F_4
SVID DATA
H_CPU_SVIDDAT R364 *0_4/S VR_SVID_DATA (39)

CFG

0 Enable; SET DFX ENABLED BIT IN DEBUG
1 , Disable;
CFG3 R24 *1K_4

Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a OxM board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	CFG2 R26 1K_4
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	CFG4 R385 1K_4
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	CFG6 R390 *1K_4 CFG5 R379 *1K_4
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	CFG7 R384 *1K_4

HWPD

R10479 close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"

+1.0V
+VCCSTPLL
R377 1K_4
R368 *1K_4
(10,32,34,35,36,38,46) HWPG
D111 2 RB501V-40
H_VCCST_PWRGD_R R374 60.4/F_4 H_VCCST_PWRGD
C658 *10P/50V_4

CPU VDDQ

+1.2VSUS
Placement close to CPU.
C143 0.1U/16V_4
C172 *0.1U/10V_4
Note: please keep plane is enough for VDDQ 2.8A

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Quanta Computer Inc.

Size	Document Number	Custom	02 -- SKYPAKE 1/20(eDP/DDI)	Rev	1A
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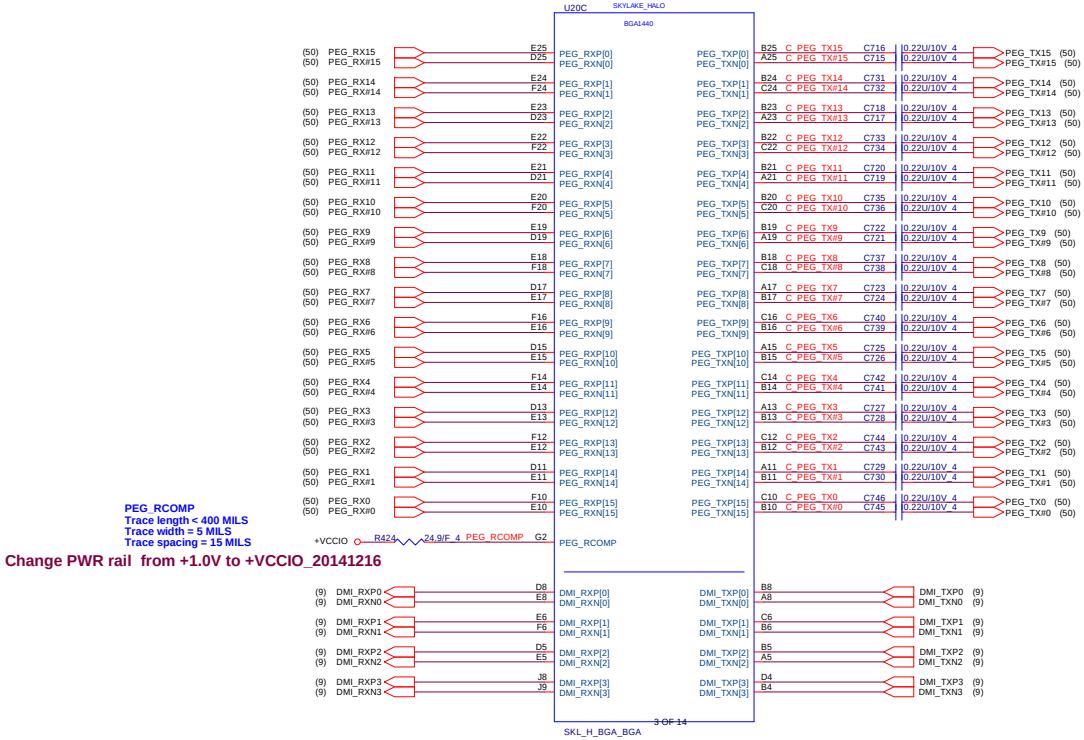
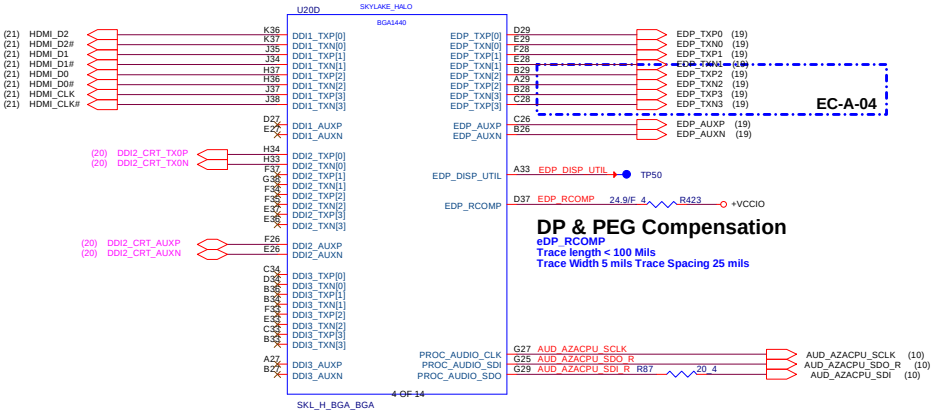
SKYLAKE Processor (DMI,PEG,FDI)

03



PEG_RCOMP
Trace length < 400 MILS
Trace width = 5 MILS
Trace spacing = 15 MILS

Change PWR rail from +1.0V to +VCCIO_20141216



CRT

EC-A-04

DP & PEG Compensation

eDP_RCOMP
Trace length < 100 Mils
Trace Width 5 mils Trace Spacing 25 mils

+VCCIO (6,37)
+1.2VSUS (2,6,10,16,17,35,44,47)
+3V_S5 (10,12,14,18,24,27,31,32,34,35,37,
+3V (9,10,11,12,13,14,16,17,19,20,21,2

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Size	Document Number: SNB 1/5 (PCIE&DMI&FDI)		Rev 2A
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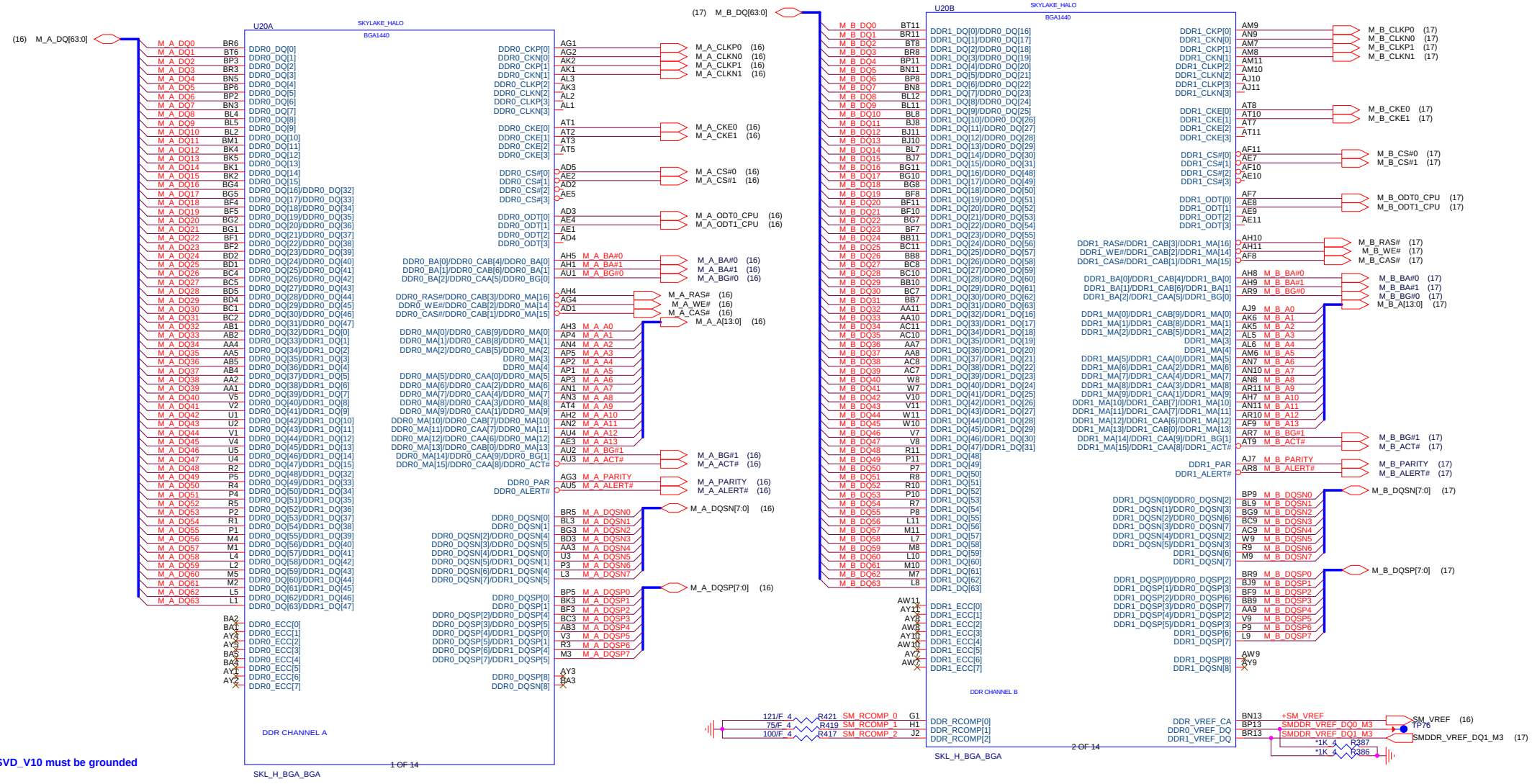
SKYLAKE Processor (DDR3)

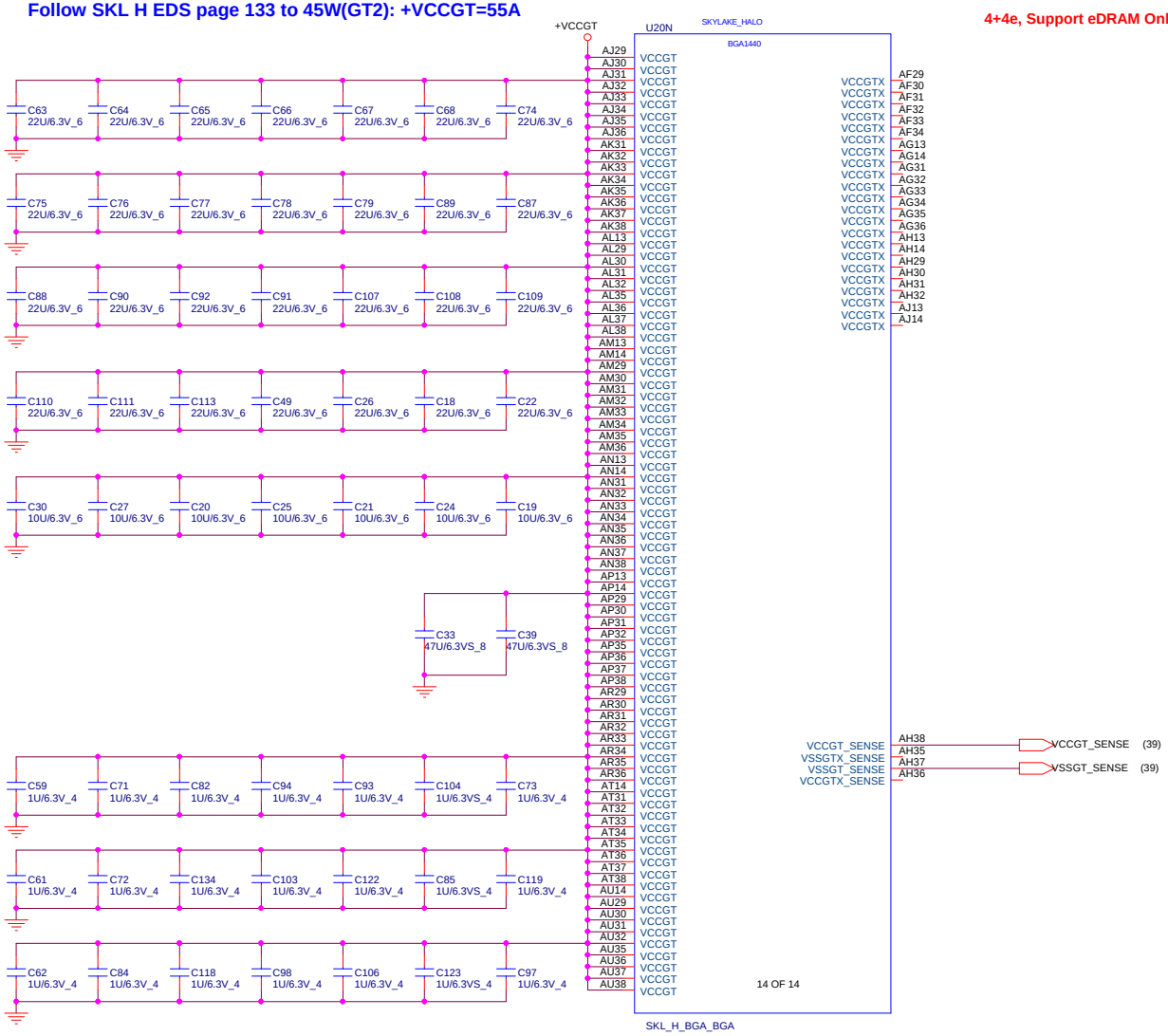


SKYLAKE Processor (POWER)

Follow SKL H EDS page 133 to 45W(GT4+OPC): +VCCGT=104A/12A (GTx)
Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

4+4e, Support eDRAM Only, GTX 12A

+VCC_CORE (7,40,44)
+1.2VSUS (2,6,10,16,17,35,44,47)



VCC Output Decoupling Recommendations		

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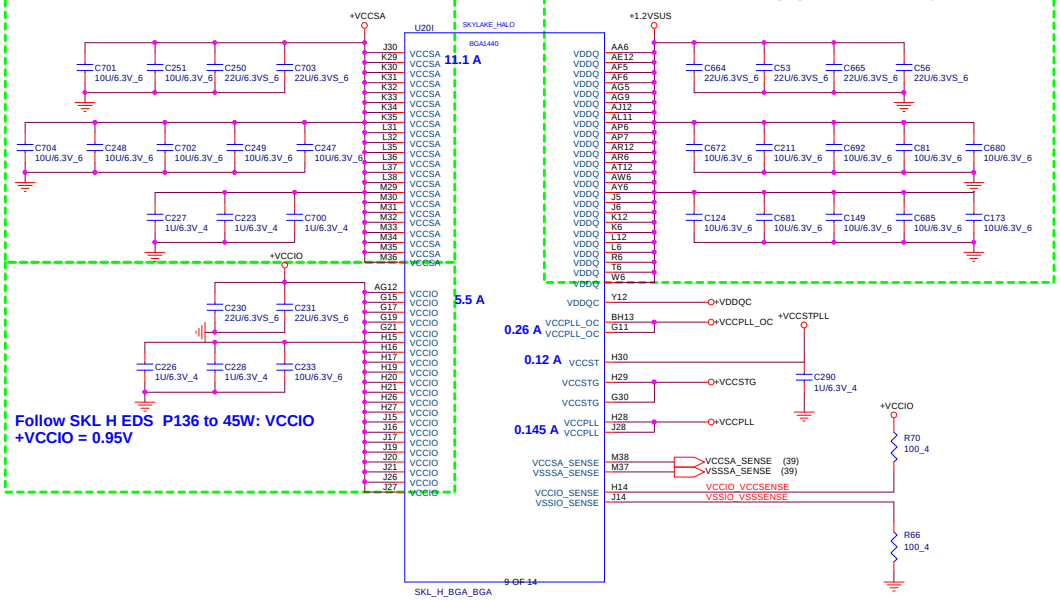
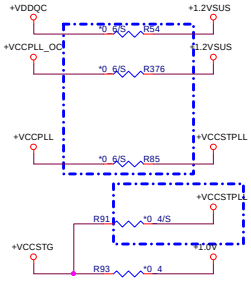
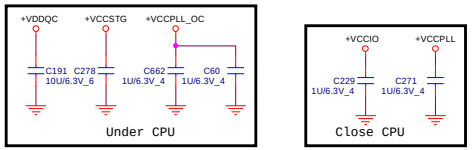
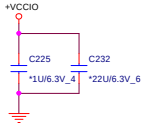
Follow SKL H EDS page 135 to 45W(GT2): VCCSA=11.1A (GTx)

Follow SKL H EDS page 135 45W: VDDQ=2.8A

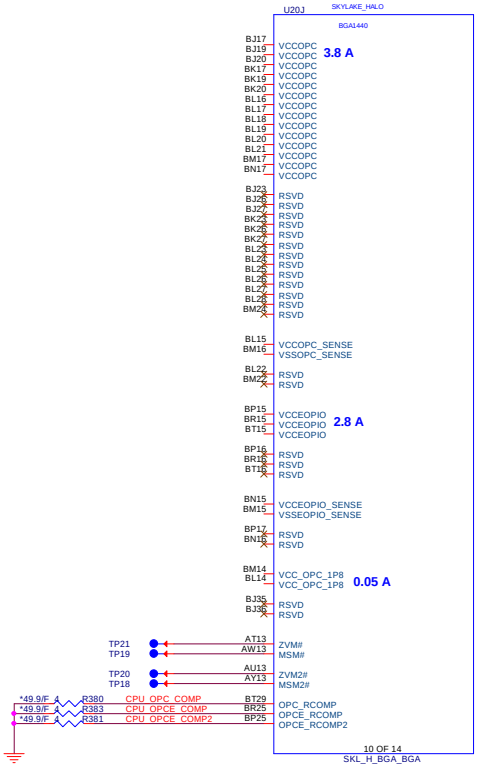








EDRAM Only, PLACE CAPS IN ACK SIDE



Unconnected for Processors without OPC.

PROJECT : NL9

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	SNB 4/5 (POWER & GND)	2A
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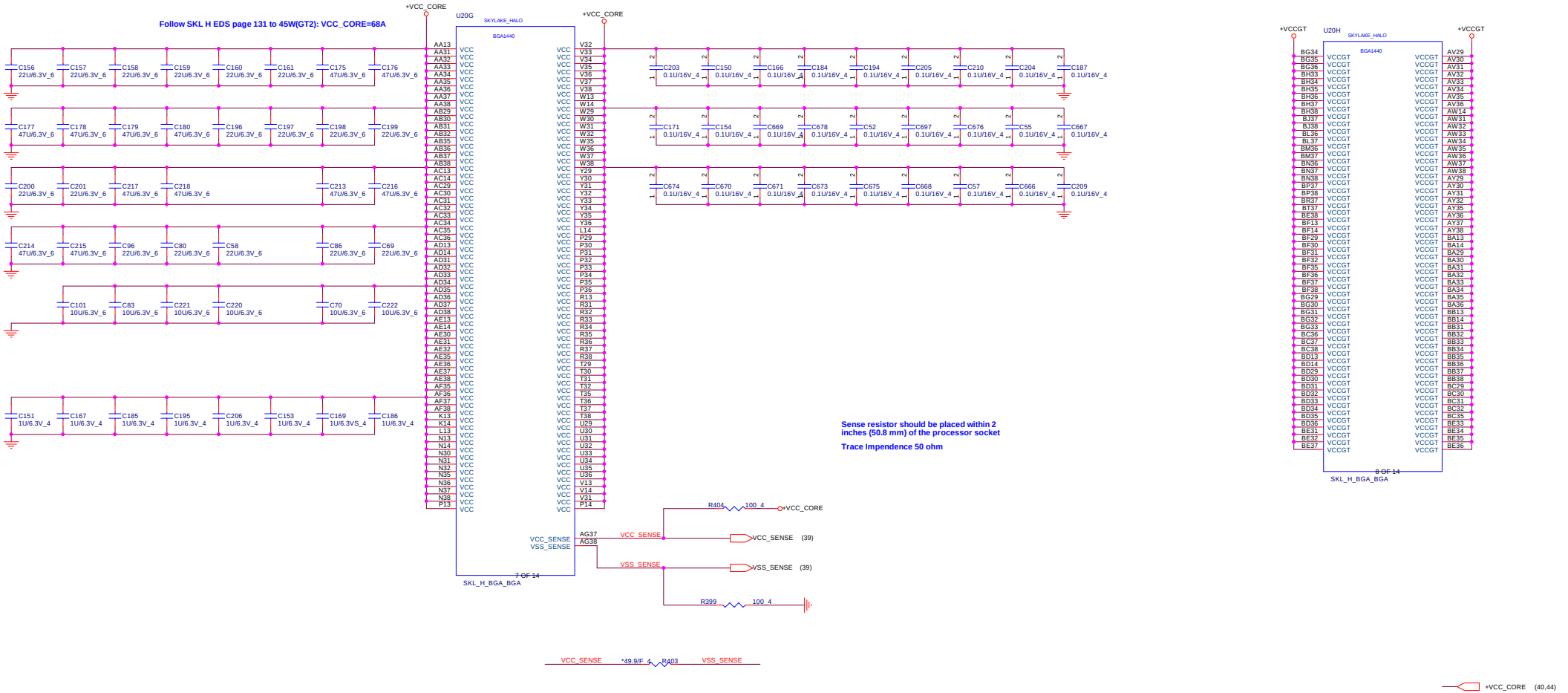

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Quanta Computer Inc.			
Size	Document Number	SNB 4/5 (POWER & GND)	Rev 2A
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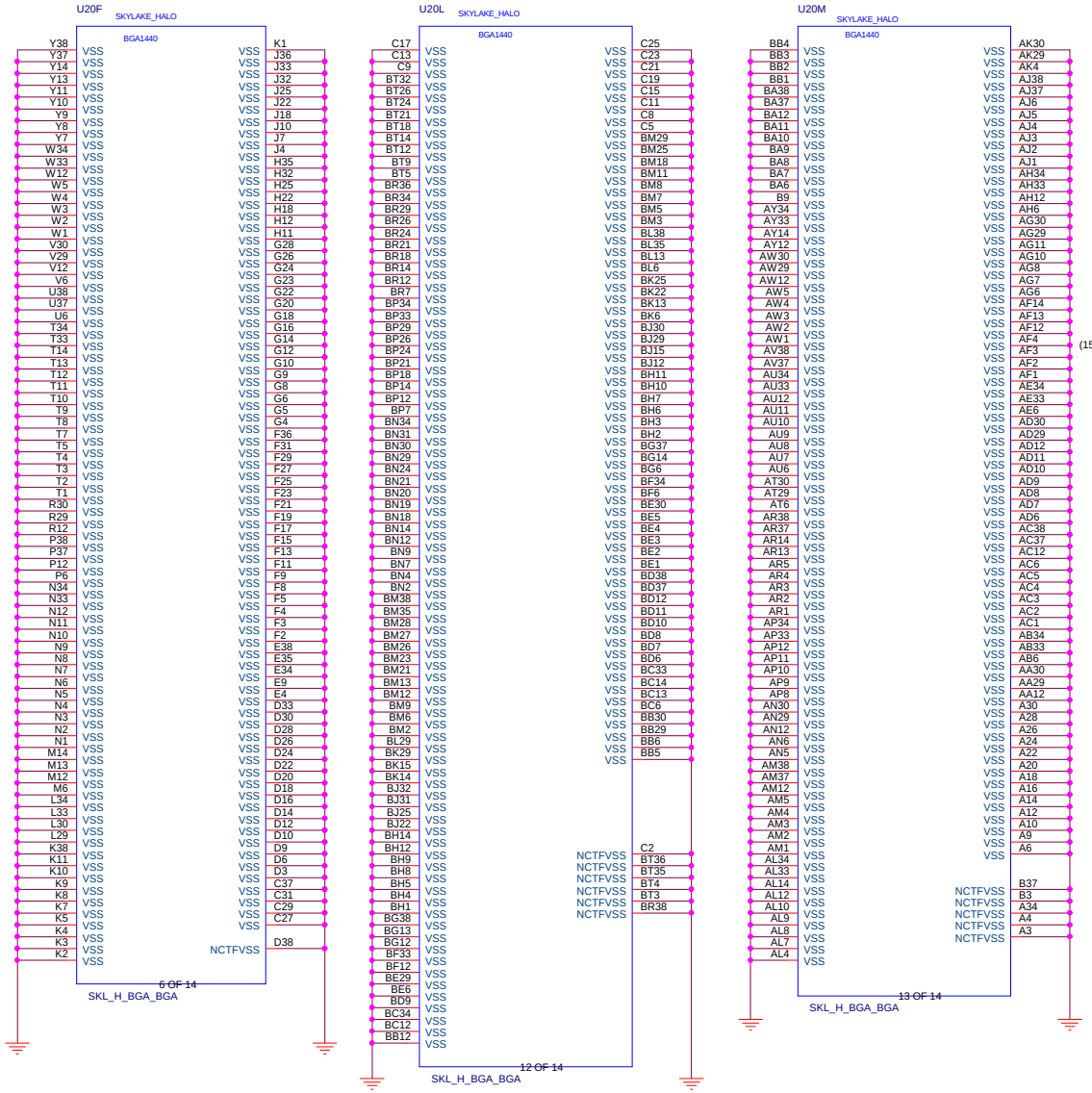
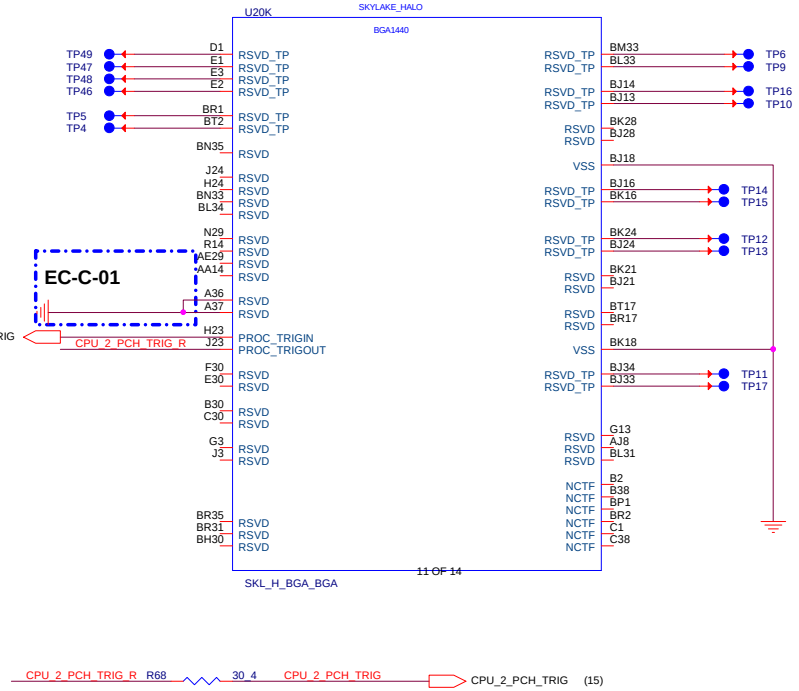
Haswell Processor (GND)



Haswell Processor (RESERVED, CFG)



08

PROJECT : NL9

Quanta Computer Inc.

Size	Document Number	Rev
	SNB 5/5 (GND)	2A
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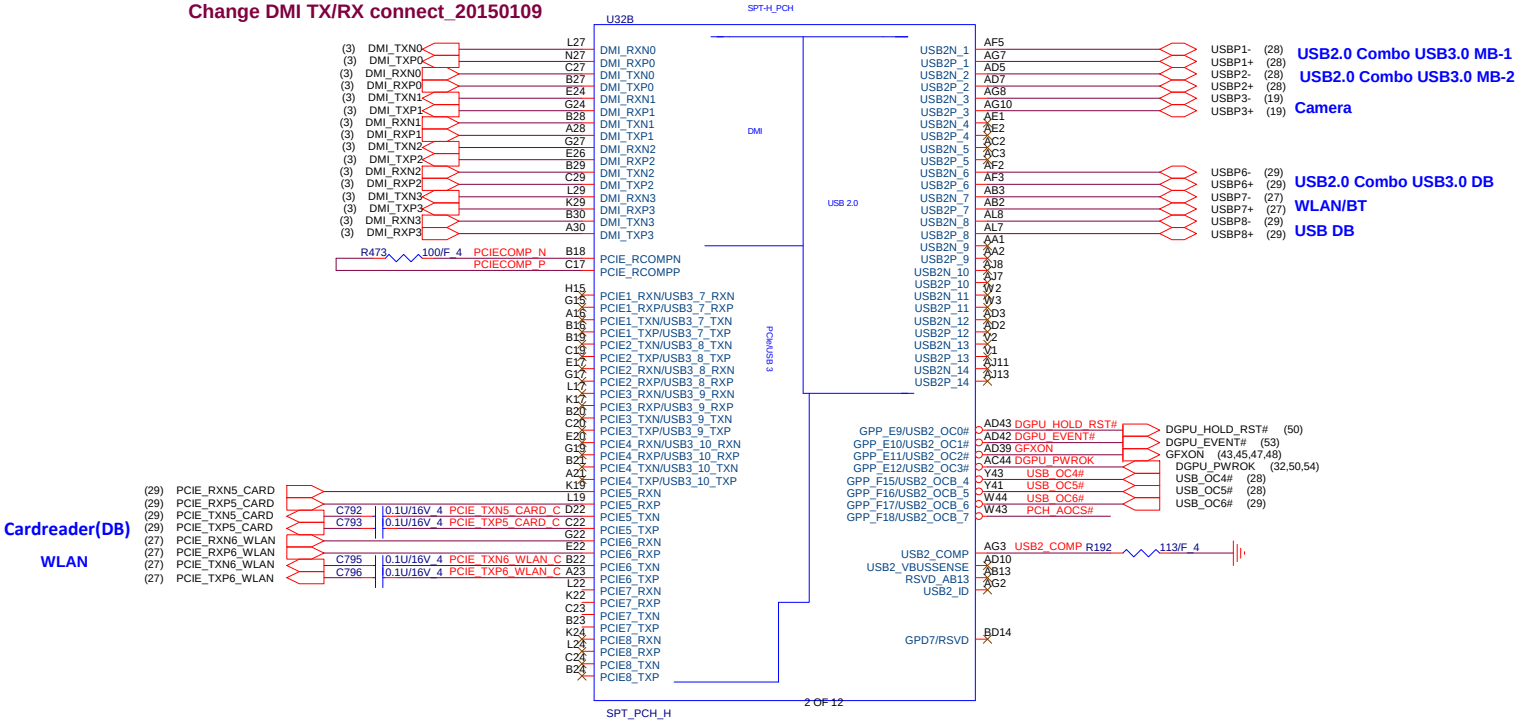
Change DMI TX/RX connect_20150109



GPU Strap

DFX TEST MODE
XTAL INPUT IS SINGLE ENDED IF
SAMPLED LOW ELSE DIFFERENTIAL

DGPU_PWROK *10K_4 R496

RING OSCILLATOR BYPASS

DGPU_HOLD_RST# 100K_4 R502

XTAL INPUT FREQUENCY[0]

DGPU_EVENT# *100K_4 R498

XTAL INPUT FREQUENCY[1]

GFXON *10K_4 R190

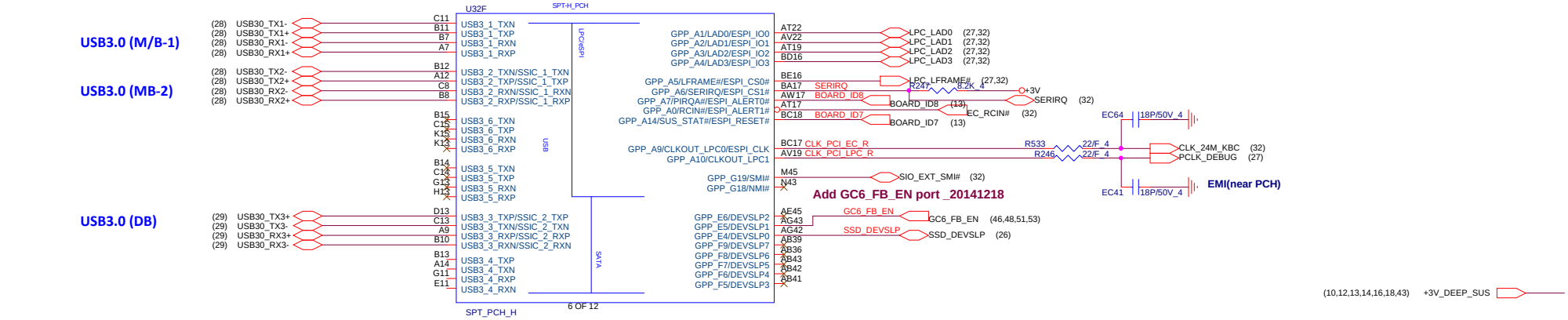
DGPU_EVENT#-- For BIOS check

+3V

DGPU_EVENT# *10K_4 R497
DGPU_HOLD_RST# *10K_4 R501
GFXON 10K_4 R193
DGPU_PWROK *10K_4 R495
SIO_EXT_SMI# 10K_4 R489
EC_RCIN# 10K_4 R249

+3V_DEEP_SUS

USB_OC4# 10K_4 R494
USB_OC5# 10K_4 R491
USB_OC6# 10K_4 R493
PCH_AOCS# 10K_4 R492



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	PCH 1/6 (DMI/FDI/VIDEO)	2A
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HDA Bus(CLG)

(22) ACZ_BIT_CLK_AUDIO — R550 33_4 — ACZ_BCLK
(22) ACZ_RST#_AUDIO — R544 33_4 — ACZ_RST#
(12) ACZ_SDOUT
(22) ACZ_SDOUT_AUDIO — R541 33_4 — ACZ_SDOUT
(22) ACZ_SYNC_AUDIO — R538 33_4 — ACZ_SYNC
R539 *1M_4

Reserve for EMI

EC63 *10P/50V_4

(22) ACZ_SDIN0

Change R2032 from 33 to 30_20141218

+3V_DEEP_SUS

Add PU _20141212

R225 2.2K_4 SMB_ME0_CLK
R230 2.2K_4 SMB_ME0_DAT
R516 2.2K_4 SMB_ME1_CLK
R521 2.2K_4 SMB_ME1_DAT
R216 2.2K_4 SMB_PCH_CLK
R209 2.2K_4 SMB_PCH_DAT

R542 10K_4 RF_OFF_PCH
R608 10K_4 SUSWARN#
R600 *10K_4 SUSACK#

(32) GPIO33_EC — R535 1K_4 — ACZ_SDOUT

DDR3_DRAMRST# — RV16 *EGA-0402
PCIE_WAKE# — RV17 *EGA-0402
SYS_RESET# — RV18 *EGA-0402

RSMRST# — C543 *220P/50V_4
EC_PWROK — C534 *220P/50V_4

(3) AUD_AZACPU_SDO_R — R510 30_4 — AUD_AZACPU_SDO
(3) AUD_AZACPU_SDI — AUD_AZACPU_SDI
(3) AUD_AZACPU_SCLK — R512 30_4 — AUD_AZACPU_SCLK_R

AUD_AZACPU_SCLK

EMI

EC61 *33P/50V_4

+3V_DEEP_SUS
R536 *4.7K_4

ACZ_SDOUT

RTC_RST# — SRTC_RST#
PCH_PWROK — RSMRST#
(32) RSMRST#
DSWROK_EC_R — SMLOALERT#
SMB_PCH_CLK
SMB_PCH_DAT
DRAMRST_CNTRL_PCH
SMB_ME0_CLK
SMB_ME0_DAT
SMB_ME1_CLK
SMB_ME1_DAT
(12) SML0ALERT#
(12) DRAMRST_CNTRL_PCH
(12) SML1ALERT#_R — SML1ALERT# R — TP42

U32D — SPT-H_PCH

HDA_BCLK — ACZ_BCLK
HDA_RST# — ACZ_RST#
HDA_SDI0
HDA_SDI1
HDA_SDO — ACZ_SDOUT
HDA_SYNC — ACZ_SYNC
RSVD_BD1
RSVD_BE2
DISPA_SDO
DISPA_SDI
DISPA_BCLK
GPP_D8/I2S0_SCLK
GPP_D7/I2S0_RXD
GPP_D6/I2S0_TXD
GPP_D5/I2S0_SFRM
GPP_D20/DMIC_DATA0
GPP_D19/DMIC_CLK0
GPP_D18/DMIC_DATA1
GPP_D17/DMIC_CLK1
RTCRST#
SRTCRST#
PCH_PWROK
RSMRST#
DSW_PWROK
GPP_C2/SMBALERT#
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C5/SML0ALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_B23/SML1ALERT#/PCHHOT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA

AUDIO
SMBUS
JTAG

GPP_A12/BMBUSY#/ISH_GP6/SX_EXIT_HOLDOFF#
GPP_A8/CLKRUN#
GPD11/LANPHYPC
GPD9/SLP_WLAN#
DRAM_RESET#
GPP_B2/VRALERT#
GPP_B1
GPP_B0
GPP_G17/ADR_COMPLETE
GPP_B11
SYS_PWROK
WAKE#
GPD6/SLP_A#
SLP_LAN#
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
GPD8/SUSCLK
GPD0/BATLOW#
GPP_A15/SUSACK#
GPP_A13/SUSWARN#/SUSPWRDNACK
GPD2/LAN_WAKE#
GPD1/ACPRESENT
SLP_SUS#
GPD3/PWRBTN#
SYS_RESET#
GPP_B14/SPKR
PROCPWRGD
ITP_PMODE
JTAGX
JTAG_TMS
JTAG_TDO
JTAG_TDI
JTAG_TCK

TP66 — CLKRUN# (32)
TP39
TP38
DDR3_DRAMRST# (16,17)
PCIE_WAKE# (24,27,32)
SLP_A# (18)
PCH_SLP_S0_N (18,32,37)
SUSB# (18,32)
SUSC# (18,32)
SLP_S5# (18)
TP37
RF_OFF_PCH (27)
SUSACK#_EC (32)
SUSWARN#_EC (32)
SUSWARN#
AC_PRESENT (32,53)
SLP_SUS#_EC (32)
DNBSWON# (32)
SYS_RESET# (18)
ACZ_SPKR (12,22)
PROCPWRGD (2)
TP2
+1.0V_DEEP_SUS
TP58
TP59
TP56
TP57
TP55

+1.2VSUS
R543 470/F_4

SYS_RESET# R531 10K_4
GPP_B2 R607 10K_4
+3V
+1.0V
R527 51_4
R522 51_4
R517 51_4
JTAG_TMS_PCH
JTAG_TDI_PCH
JTAG_TDO_PCH
JTAG_TCK_PCH
R528 *51_4
R523 *51_4
R518 *51_4
R515 51_4

4 OF 12

SPT_PCH_H

CPU heat pipe local thermal sensor
DDR thermal sensor
EC

Q47
(32) MBCLK2 — SMB_ME1_CLK
(32) MBDATA2 — SMB_ME1_DAT
*2N7002DW

XDP
DDR3-L

Q23
+3V R235 4.7K_4 — (16,17) SMB_RUN_DAT — SMB_PCH_DAT
+3V R207 4.7K_4 — (16,17) SMB_RUN_CLK — SMB_PCH_CLK
2N7002KDW

System PWR_OK(CLG)

+3V_S5
C552 *0.1U/10V_4
PCH_PWROK
IMVP_PWRGD — IMVP_PWRGD (39)
EC_PWROK — EC_PWROK (22,32)
U10 TC7SH08FU
R215 100K_4
R229 *0_4

For DS3 Sequence

For DS3 -->Ra
Non-DS3 -->Rb
Rb
RSMRST# R218 *0_4
(32) DSWROK_EC — R210 *0_4/S — DSWROK_EC_R
Ra

+3V_S5
R556 1K_4 PCIE_WAKE#
R557 10K_4 AC_PRESENT
+3V
R239 8.2K/F_4 CLKRUN#
RSMRST# R222 10K_4
DSWROK_EC R211 100K_4
IMVP_PWRGD R217 *100K_4

RTC Circuitry(RTC)

RTC Power trace width 20mils.
30mils

+3V_RTC_0
+3V_RTC_0 — R653 1K_4 — +3V_RTC_1
CN25
RTC_B
D15 BAT54CW
+3VPCU
C841 1U/6.3V_4

+3V_RTC
R617 20K/F_4
J1 *SOLDERJUMPER-2
RTC_RST#
C842 1U/6.3V_4
R612 20K/F_4
SRTC_RST#
C843 1U/6.3V_4

Q50 2N7002K
RTC_RST# — RTC_RST# (18)
EC_RTC_RST (32)
R620 10K_4

For HWPG Sequence

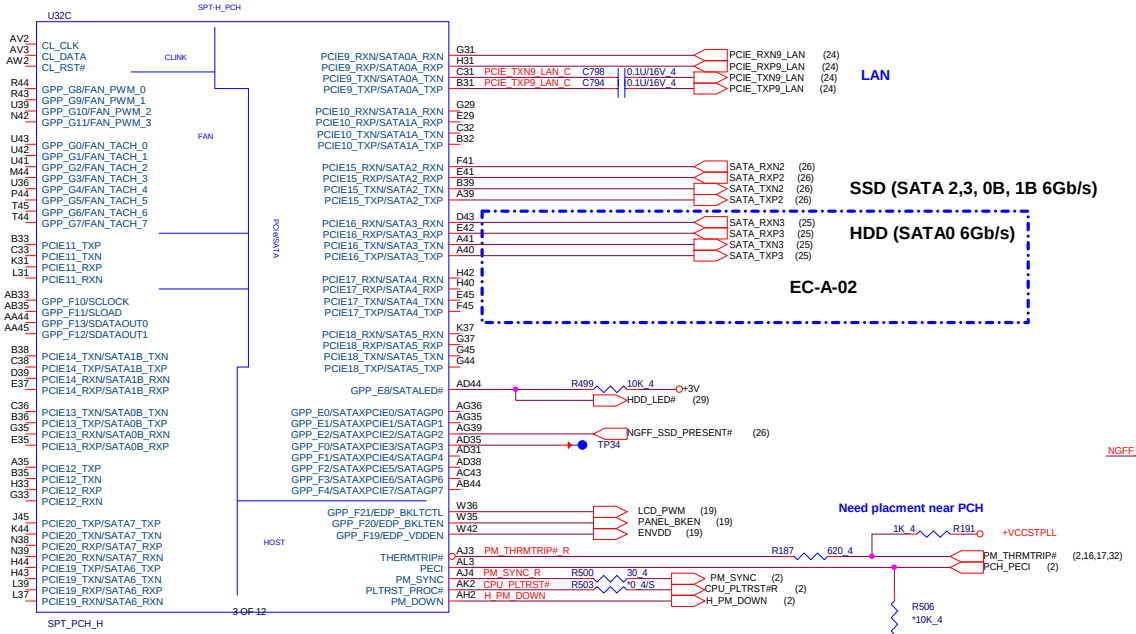
+1.0V
R274 15K/F_4
C563 0.1U/16V_4
R273 100K_4

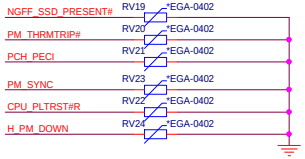
+5V_S5
R275 100K_4
+1.0V_PWRGD_G2
+1.0V_PWRGD_G1
Q27 METR3904-G

+3V_S5
R265 10K_4
HWPG — HWPG (2,32,34,35,36,38,46)
Q26 2N7002K
R266 100K_4

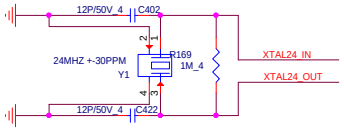
PROJECT : NL9
Quanta Computer Inc.

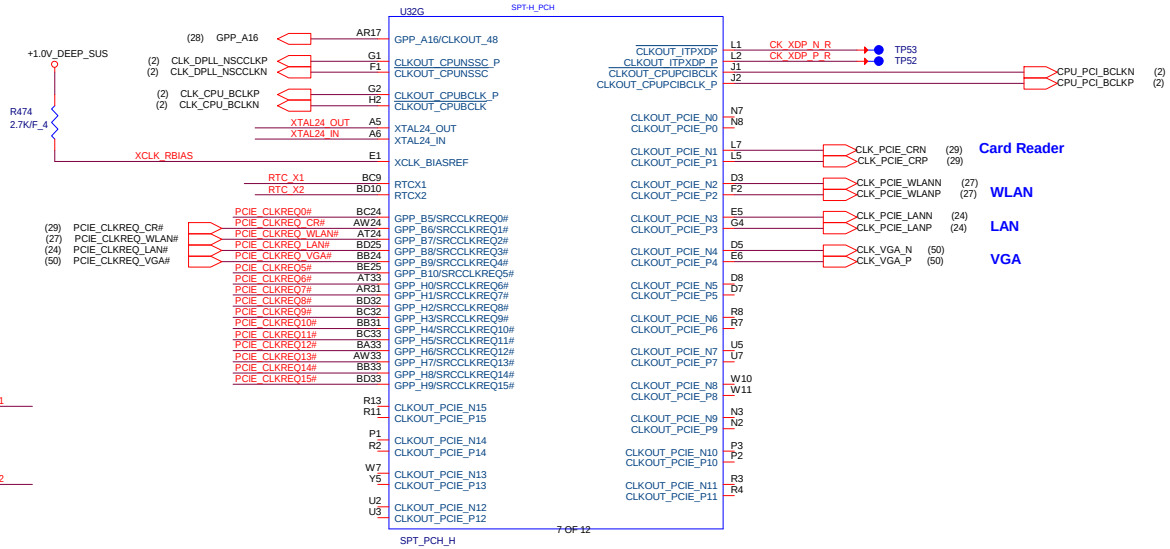
Size	Document Number	Rev
	PCH 2/6 (SATA/HDA/SPI)	2A
Date: Wednesday, October 14, 2015	Sheet 10 of 61	



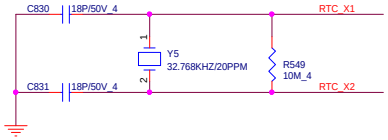


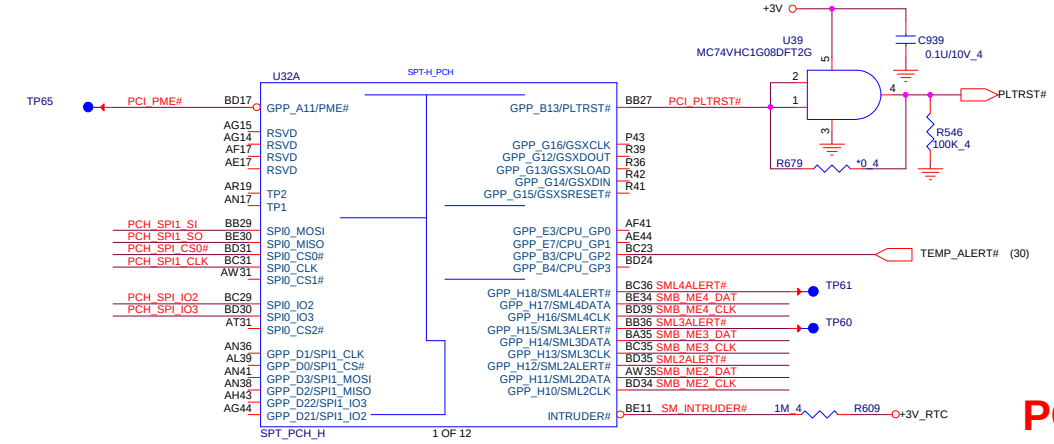
The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.





RTC Clock 32.768KHz



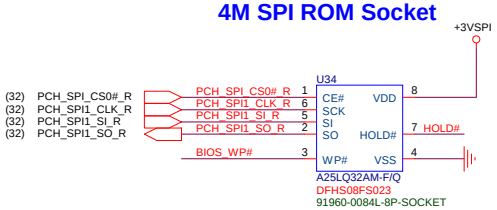


PCH Strap Pin

PCH SPI ROM(CLG)

Vender	Size	P/N
EON	8MB	
Winbond	16MB	AKE3DZN0N01
GigaDevice	8MB	
Socket		DFHS08FS023

4M SPI ROM Socket

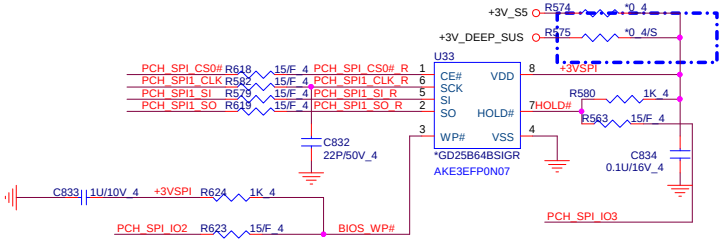


TP66-71 need place to TOP

TP67 PCH_SPI_CS0#_R
TP63 PCH_SPI1_CLK_R
TP64 PCH_SPI1_SI_R
TP68 PCH_SPI1_SO_R
TP69 BIOS_WP#
TP62 HOLD#

U2003&U2004 footprint must overlap

PCH SPI ROM(CLG)



TOP SWAP OVERRIDE STRAP

HIGH:TOP SWAP ENABLED (CRB)
LOW:TOP SWAP DISABLED(DEFAULT)

+3V
R566
*150K/F_4
(10,22) ACZ_SPKR
ACZ_SPKR
R564
20K/F_4

BOOT SELECT STRAP

HIGH:LPC
LOW: SPI. (Default)

+3V_DEEP_SUS
R263
*4.7K_4
(13) S_GPIO
S_GPIO
R254
20K/F_4

NO REBOOT IF SAMPLED HIGH

HIGH:Enable No Reboot mode.
This function is useful when running ITP/XDP.

LOW: Disable "No Reboot" mode. (Default)

+3V
R611
*4.7K_4
(13) BBS_BIT1
BBS_BIT1
R610
20K/F_4

ESPI/LPC SELECT STRAP

HIGH:eSPI Is selected for EC.
LOW: LPC Is selected for EC. (Default)

+3V_DEEP_SUS
R257
*4.7K_4
(10) DRAMRST_CNTRL_PCH
DRAMRST_CNTRL_PCH
R242
4.7K_4

TLS CONFIDENTIALITY ENABLED

HIGH:T Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)
LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

+3V_DEEP_SUS
R256
*4.7K_4
(10) SML0ALERT#
SML0ALERT#
R241
*20K/F_4

RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V_DEEP_SUS
R598
*20K/F_4
PCH_SPI1_SI
R597
*4.7K_4

RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V_DEEP_SUS
R594
*20K/F_4
PCH_SPI1_SO
R593
*4.7K_4

RESERVED

This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V_DEEP_SUS
R269
*4.7K_4
(10) SML1ALERT#_R
SML1ALERT#_R
R271
*20K/F_4

RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V_DEEP_SUS
R606
*20K/F_4
PCH_SPI_IO2
R605
*4.7K_4

RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V_DEEP_SUS
R590
*20K/F_4
PCH_SPI_IO3
R589
100_4

ESPI FLASH SHARING MODE

HIGH:SLAVE ATTACEHD FLASH SHARING
LOW: 0: MASTER ATTACHED FLASH SHARING

This strap should sample LOW.
driving it to opposite direction during strap sampling.
There should NOT be any on-board device

+3V_DEEP_SUS
R545
*4.7K_4
SML2ALERT#
R562
*20K/F_4

DFX TEST MODE QUALIFIER FOR OTHER DFX STRAP WHEN SAMPLED LOW

+3V_DEEP_SUS
R264
1K_4
(15) PGDMON
PGDMON
R260
1K_4

TLS CONFIDENTIALITY ENABLED

HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.(CRB)

LOW: security measures defined in the Flash Descriptor. (Default)

+3V_DEEP_SUS
R537
1K_4
(10) ACZ_SDOUT
ACZ_SDOUT
R540
1K_4

PROJECT : NL9
Quanta Computer Inc.

Size	Document Number	PCH 4/6 (GPIO/MISC)	Rev
		Wednesday, October 14, 2015	12 61
Date:		Sheet	of

(9,10,12,14,16,18,43) +3V_DEEP_SUS

Need check PCI_GNT3#_20141119

(12) S_GPIO — S_GPIO — TP41 — PCI_GNT3#

(12) BBS_BIT1 — BBS_BIT1
(16) PM_EXTTS#0
(16) EXTTS#1

U32K — SPT-H_PCH

GPP_B22/GSPI1_MOSI AT29
GPP_B21/GSPI1_MISO AR29
GPP_B20/GSPI1_CLK AV29
GPP_B19/GSPI1_CS# BC27
GPP_B18/GSPI0_MOSI BD28
GPP_B17/GSPI0_MISO BD27
GPP_B16/GSPI0_CLK AW27
GPP_B15/GSPI0_CS# AR24
GPP_C9/UART0_TXD AV44
GPP_C8/UART0_RXD BA41
GPP_C11/UART0_CTS# AU44
GPP_C10/UART0_RTS# AV43
GPP_C15/UART1_CTS#/ISH_UART1_CTS# AU41
GPP_C14/UART1_RTS#/ISH_UART1_RTS# AT44
GPP_C13/UART1_TXD/ISH_UART1_TXD AT43
GPP_C12/UART1_RXD/ISH_UART1_RXD AU43
GPP_C23/UART2_CTS# AN43
GPP_C22/UART2_RTS# AN44
GPP_C21/UART2_TXD AR39
GPP_C20/UART2_RXD AR45
GPP_C19/I2C1_SCL AR41
GPP_C18/I2C1_SDA AR44
GPP_C17/I2C0_SCL AR38
GPP_C16/I2C0_SDA AT42
GPP_D4/ISH_I2C2_SDA/ISH_I2C3_SDA AM44
GPP_D23/ISH_I2C2_SCL/ISH_I2C3_SCL AJ44

GPP_D9 AL44
GPP_D10 AL36 — CAM_EN_R — R208 *0_4/S — CAM_EN (19) — TP35
GPP_D11 AL35 — RF_OFF
GPP_D12 AJ39 — BT_OFF — BT_OFF (27)
GPP_D16/ISH_UART0_CTS# AJ43
GPP_D15/ISH_UART0_RTS# AL43
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C2_SCL AK44
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C2_SDA AK45
GPP_H20/ISH_I2C0_SCL BC38
GPP_H19/ISH_I2C0_SDA BB38
GPP_H22/ISH_I2C1_SCL BD38
GPP_H21/ISH_I2C1_SDA BE39
GPP_A23/ISH_GP5 BC22 — BOARD_ID6
GPP_A22/ISH_GP4 BD18 — BOARD_ID5
GPP_A21/ISH_GP3 BE21 — BOARD_ID4
GPP_A20/ISH_GP2 BD22 — BOARD_ID3
GPP_A19/ISH_GP1 BD21 — BOARD_ID2
GPP_A18/ISH_GP0 BB22 — BOARD_ID1
GPP_A17/ISH_GP7 BC19 — BOARD_ID0

11 OF 12

SPT_PCH_H

+3V_DEEP_SUS

BT_OFF — R200 — 10K_4

BOARD_ID0 (19)

R551 *10K_4 BOARD_ID0 — R568 10K_4 — +3V_DEEP_SUS
R588 *10K_4 BOARD_ID1 — R602 10K_4
R587 *10K_4 BOARD_ID2 — R601 10K_4
R554 10K_4 BOARD_ID3 — R571 *10K_4
R552 *10K_4 BOARD_ID4 — R569 10K_4
R555 10K_4 BOARD_ID5 — R572 *10K_4
R553 10K_4 BOARD_ID6 — R570 *10K_4
R586 10K_4 BOARD_ID7 — R596 *10K_4
R259 10K_4 BOARD_ID8 — R262 *10K_4

BOARD_ID7 — BOARD_ID7 (9)
BOARD_ID8 — BOARD_ID8 (9)

+3V_DEEP_SUS
R511 49.9K/F_4
R514 49.9K/F_4
+3V_DEEP_SUS — R507 — 10K_4
(32) SIO_EXT_SCI# — SIO_EXT_SCI#

(28) UART2_TXD — UART2_TXD
(28) UART2_RXD — UART2_RXD

Model	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4]	BOARD_ID[3:2]	BOARD_ID[1:0]
Definition	Reserve (Default = 00)	Reserve (Default = 00)	0:DDR3 (EOL) 1:DDR4 (default)	00 GPU950 01 GPU960 10 GPU970	10 : NL8 11 : NL9 Cable detect

Reserve EDP_HPD opposites circuit!

+3V
R227 10K/F_4
EDP_HPD
R228 100K_4

U32E — SPT-H_PCH

(21) HDMI_HPD_CON — HDMI_HPD_CON — GPP_I0/DDPB_HPD0 AW4
(20) DDI2_CRT_HPD_Q — GPP_I1/DDPC_HPD1 AY2
GPP_I2/DDPD_HPD2 AV4
GPP_I3/DDPE_HPD3 BA4
(19) EDP_HPD — EDP_HPD — GPP_I4/EDP_HPD BD7

GPP_I7/DDPC_CTRLCLK BB3 — DDPC_CTRLDATA
GPP_I8/DDPC_CTRLDATA BD6
GPP_I5/DDPB_CTRLCLK BA5 — HDMI_SCL (21)
GPP_I6/DDPB_CTRLDATA BC4 — HDMI_SDA (21)
GPP_I9/DDPD_CTRLCLK BE5
GPP_I10/DDPD_CTRLDATA BE6 — DDPD_CTRLDATA — TP40
GPP_F14 Y44 — SKTOCC_N_R — SKTOCC_N_R (2)
GPP_F23 Y44
GPP_F22 W39
GPP_G23 L43
GPP_G22 L44
GPP_G21 U35
GPP_G20 R35
GPP_H23 BD36

5 OF 12

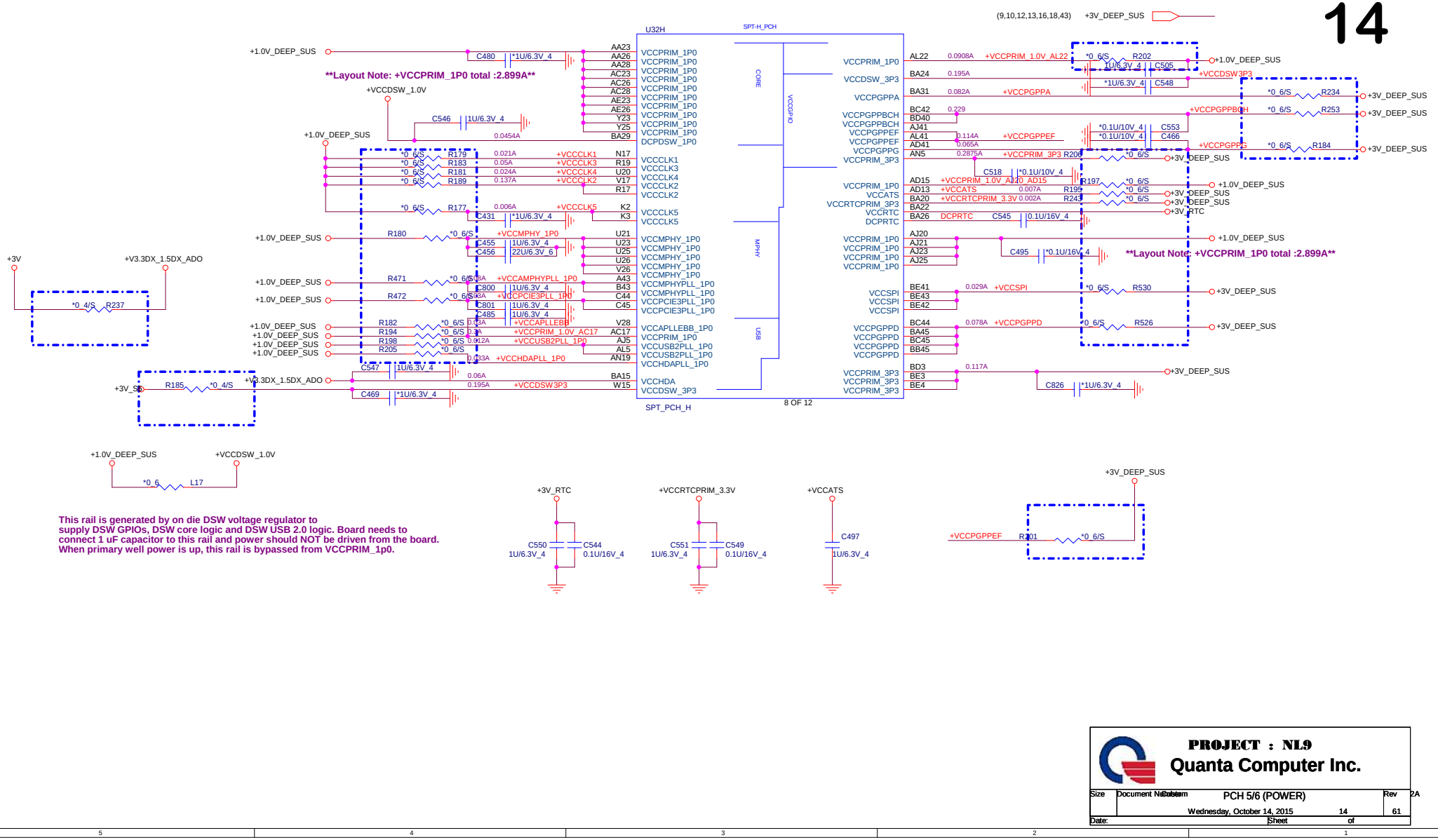
SPT_PCH_H

This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.

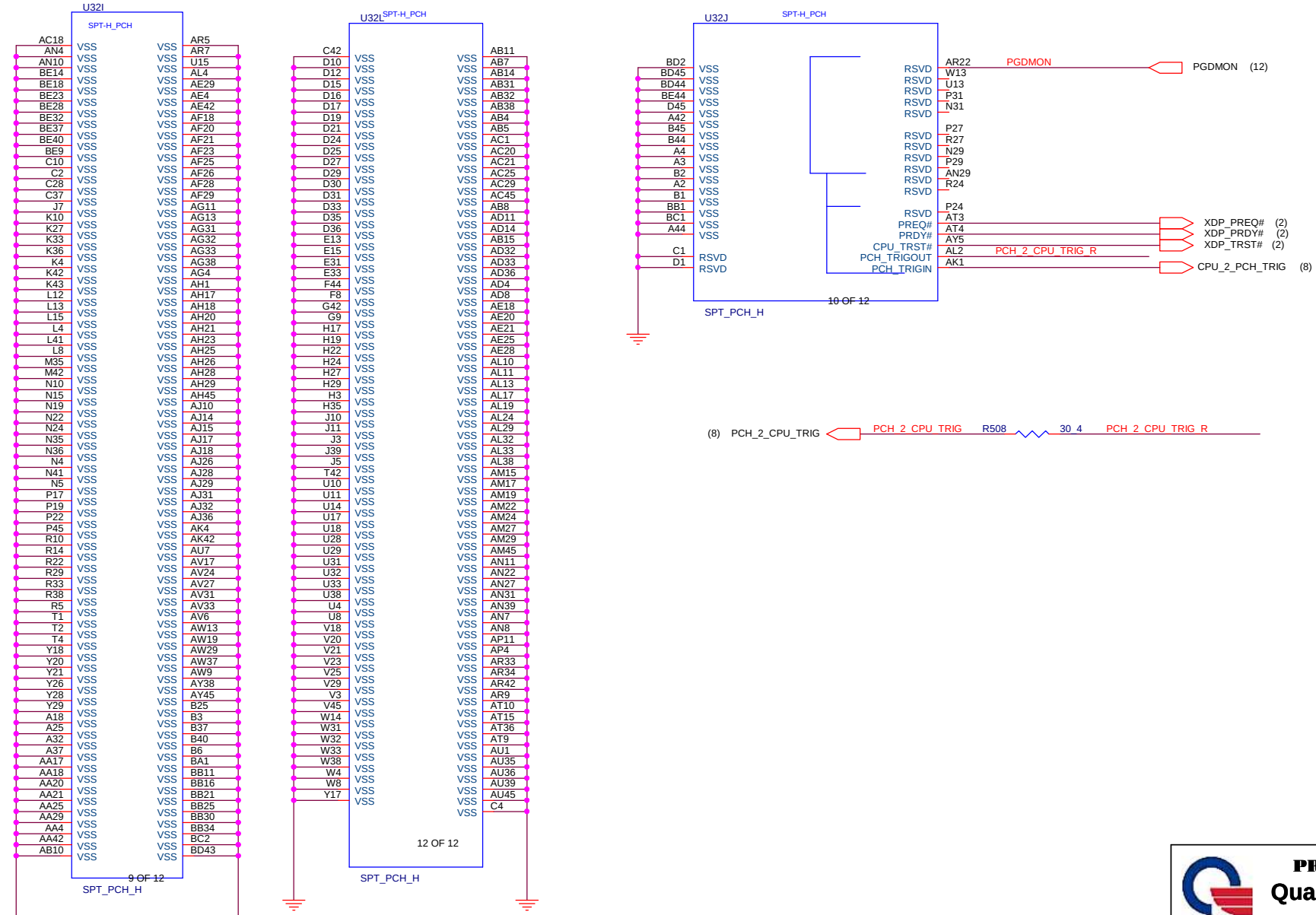
+3V
DDPC_CTRLDATA — R231 — 2.2K_4

PROJECT : NL9
Quanta Computer Inc.

Size	Document Number	PCH 4/6 (GPIO/MISC)	Rev	2A
Date:	Wednesday, October 14, 2015	Sheet 13 of 61		



PROJECT : NL9			
Quanta Computer Inc.			
Size	Document Number	PCH 5/6 (POWER)	Rev 2A
		Wednesday, October 14, 2015	Sheet 14 of 61
Date:			

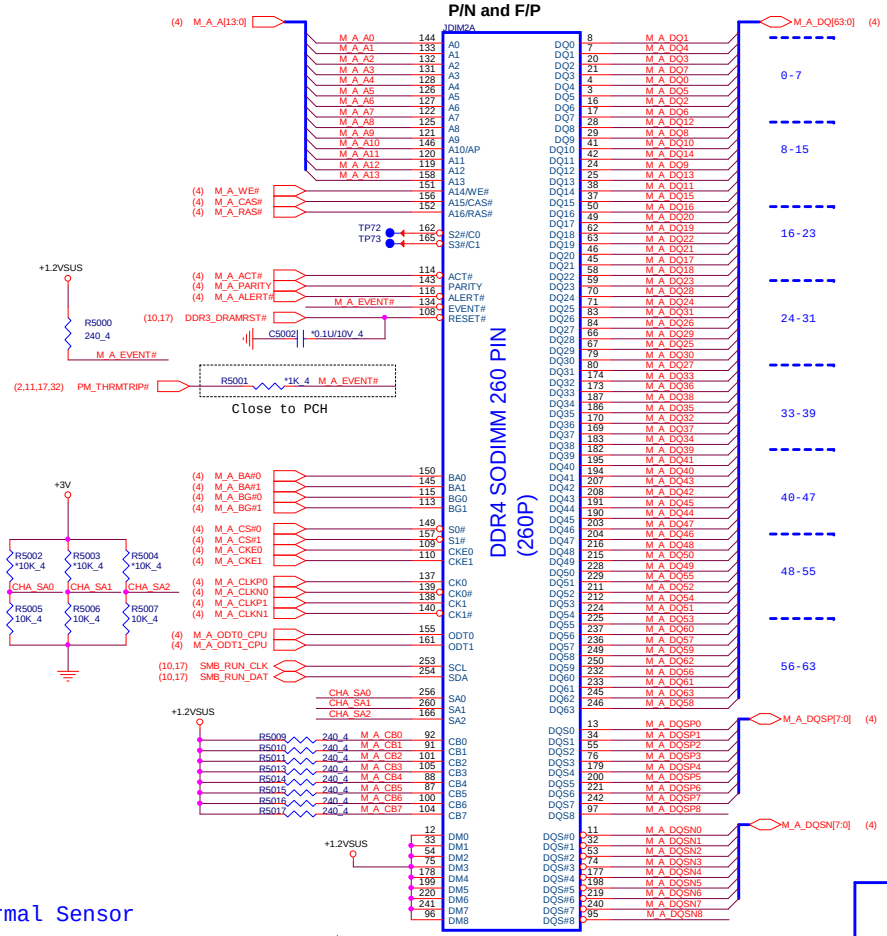


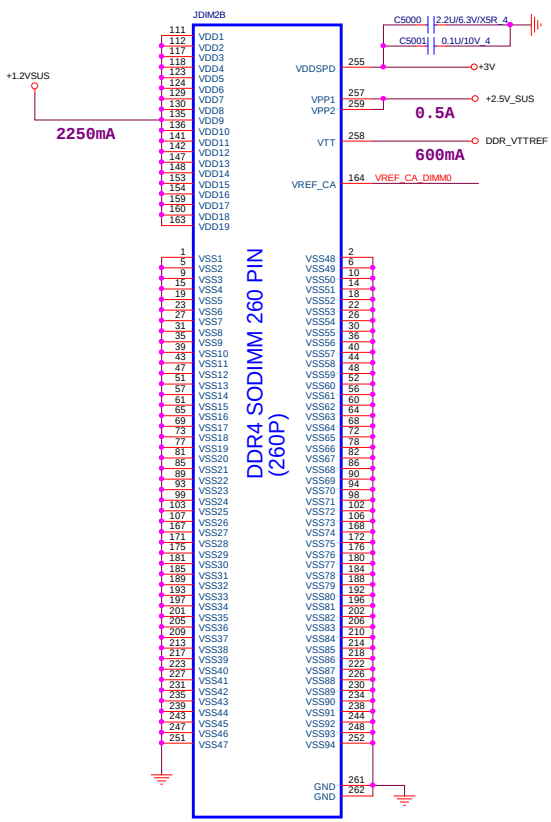
PROJECT : NL9

Quanta Computer Inc.

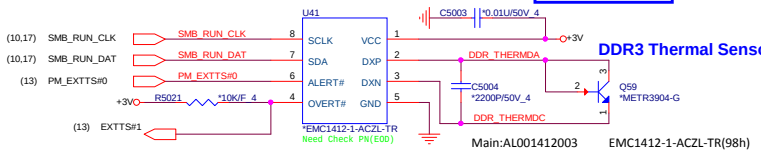
Size	Document Number	PCH 6/6 (GND)	Rev
			2A
Date: Wednesday, October 14, 2015	Sheet 15	of 61	

P/N and F/P





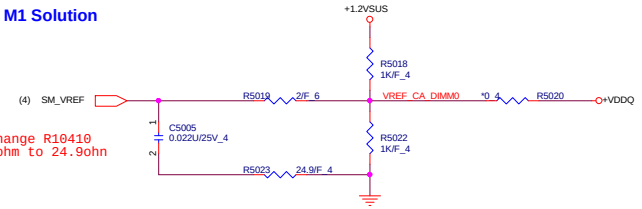
Local Thermal Sensor



Main:AL001412003 EMC1412-1-ACZL-TR(98h)

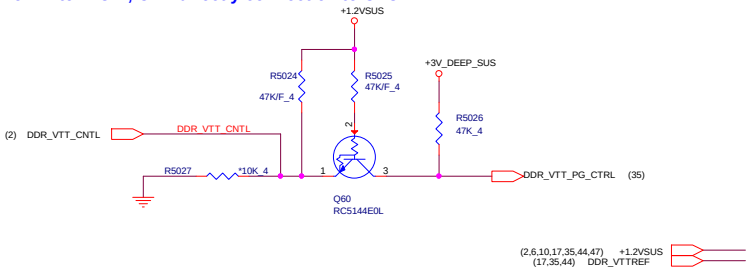
2nd:AL000431014 TMP431ADGKR(98h)

VREF DQ0 M1 Solution



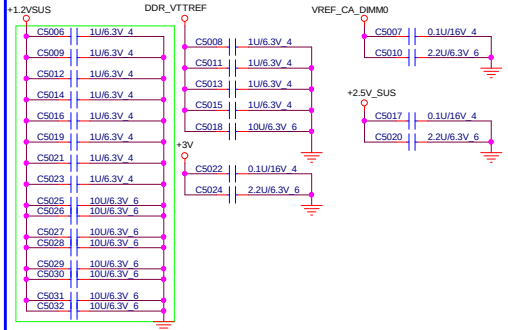
1023 Change R10410
from 2ohm to 24.9ohn

Co-lay for ODT
From Intel MOW, ODT directly connection to CPU



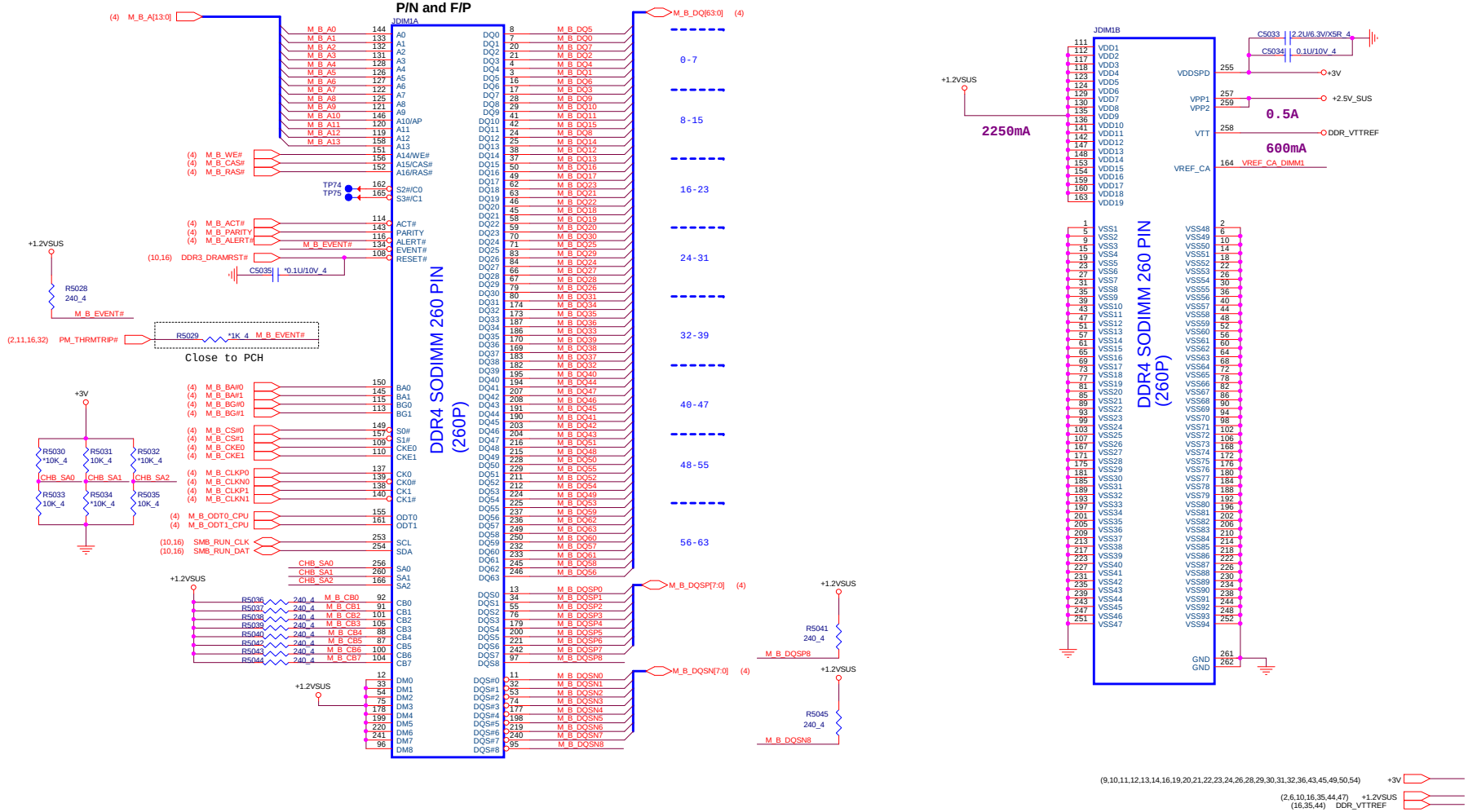
Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector



	PROJECT :ZRY Quanta Computer Inc.	
Size: Custom	Document Number: 18 -- DDR3 DIMM1-RVS(8.0H)	Rev: 1A
Date: Wednesday, October 14, 2015	Sheet 16 of 61	

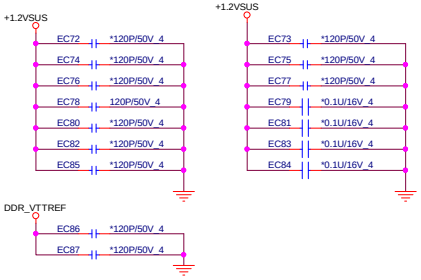
P/N and F/P



(9,10,11,12,13,14,16,19,20,21,22,23,24,26,28,29,30,31,32,36,43,45,49,50,54) +3V

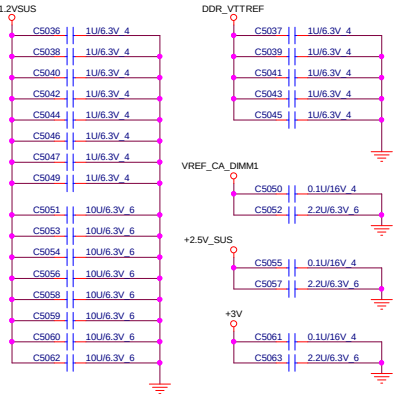
(2,6,10,16,35,44,47) +1.2VSUS
(16,35,44) DDR_VTTREF

For EMI RESERVE

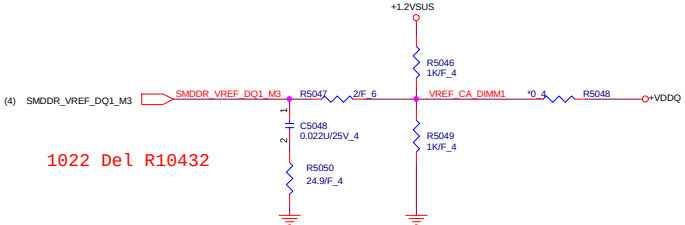


Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector



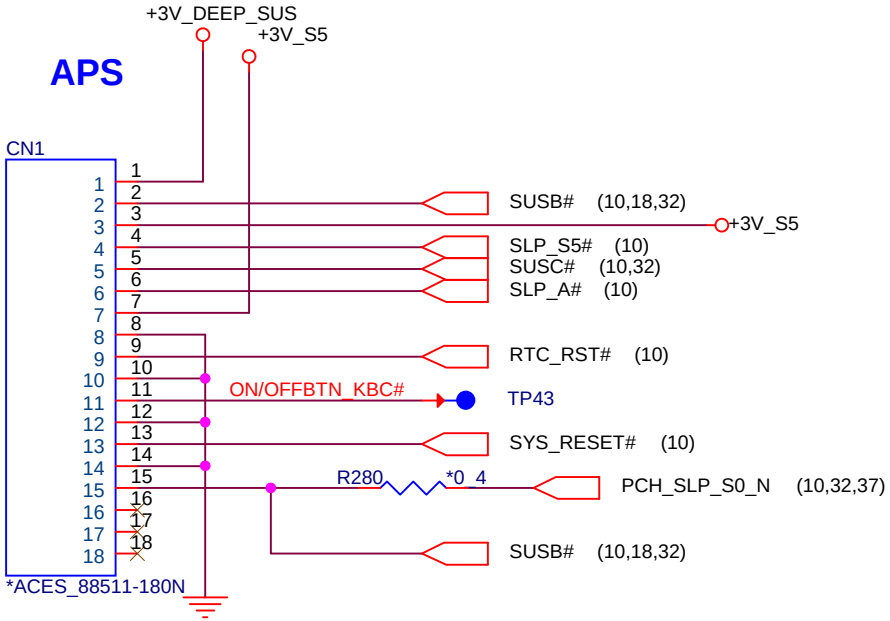
VREF DQ1 M1 Solution



1022 Del R10432

PROJECT :ZRY
Quanta Computer Inc.

Size	Document Number	Rev
Custom	17 – DDR3 DIMM0-STD(4.0H)	1A
Date: Wednesday, October 14, 2015	Sheet 17 of 61	



(9,10,12,13,14,16,43) +3V_DEEP_SUS

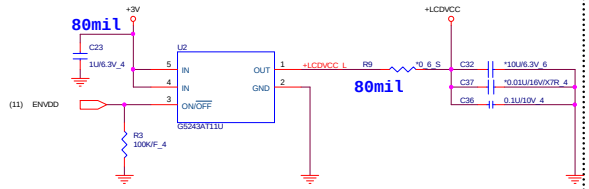
PROJECT : NL9

Quanta Computer Inc.

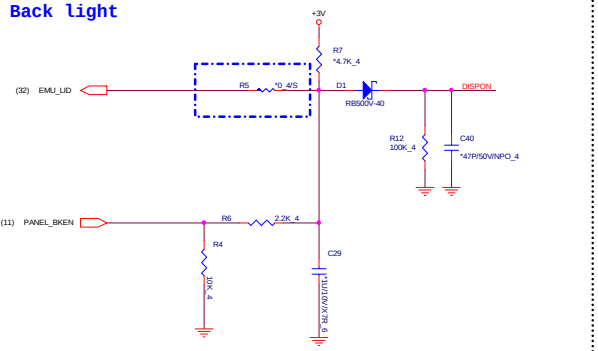
Size	Document Number	22 -- HSW XDP & APS	Rev	1A
		Wednesday, October 14, 2015 18	61	
Date:		Sheet of		

(9,10,11,12,13,14,16,17,20,21,22,23,24,26,28,29,30,31,32,36,43,45,49,50,54) +3V
(10,22,29,31,32,33,34) +3VPCU
(33,34,35,36,39,40,41,42,46,47,49,58) +VIN
(22) +V3.3DX_AUDIO

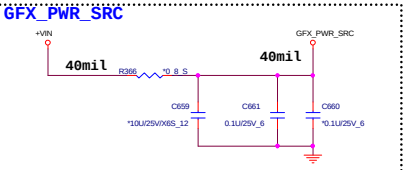
LCDVCC

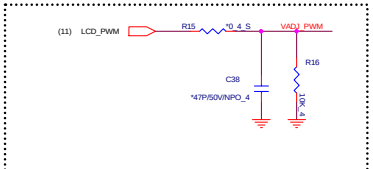


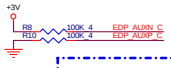
Back light



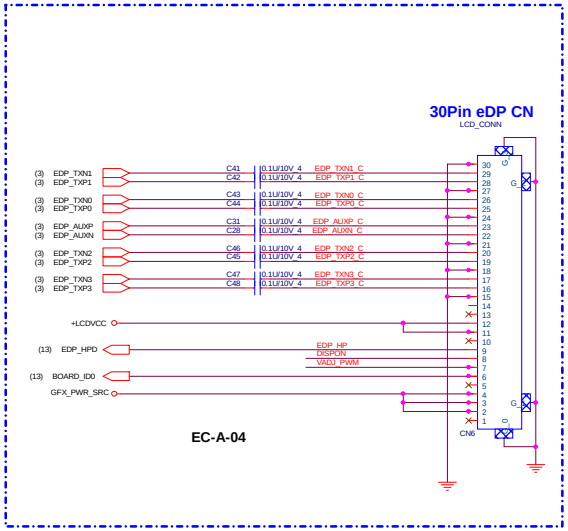
GFX_PWR_SRC





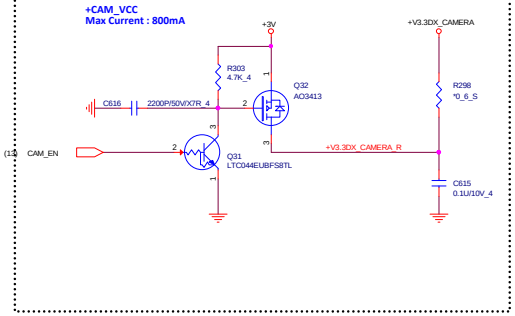


30Pin eDP CN

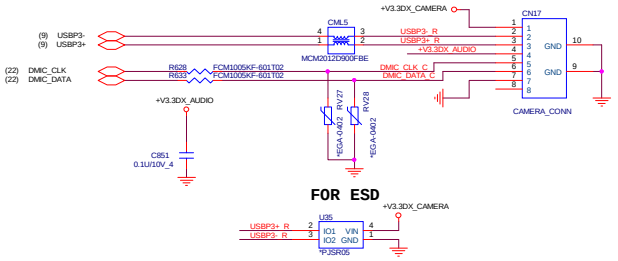


EC-A-04

CAMERA VCC Control



CAMERA/DMIC CONN



FOR ESD

PROJECT : NL9
Quanta Computer Inc.
Size: Custom
Document Number: eDP LCD/CAMERA
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ESD PROTECTION

U22 *SP0504SHTG: VGA_CON_GREEN → VGA_CON_RED; VGA_HSYNC_R → VGA_SDA
U23 *SP0504SHTG: VGA_VSYNC_R → VGA_CON_BLUE; VGA_SCL
+5V_CRT
C267 *0.1U/16V_4

+5V → D7 RB500V-40 → +5V_CRT
C275 0.1U/10V_4
F2 FUSE1A8V_POLY
CRT_VCC
C262 0.1U/10V_4

+3V
R430 *100K/F_4
R431 *100K/F_4
(3) DDI2_CRT_AUXN → C711 0.1U/16V_4 → DDI2_CRT_AUXN_C
(3) DDI2_CRT_AUXP → C712 0.1U/16V_4 → DDI2_CRT_AUXP_C

100 ohm differential impedance

(3) DDI2_CRT_TX0P → C709 0.1U/16V_4 → DDI2_CRT_TX0P_C
(3) DDI2_CRT_TX0N → C710 0.1U/16V_4 → DDI2_CRT_TX0N_C

Confirm to delete Q9.
+5V
Q12 *BSS138
(13) DDI2_CRT_HPD_Q
R62 *0 4/S
R67 100K/F_4
DDI2_CRT_HPD

U24A ANX6210FN-AB-R/QFN40
DP_RX_AUXN, DP_RX_AUXP, DP_RX_L0P, DP_RX_L0N, DP_RX_HPD
VGA_SDA, VGA_SCL
RED_L, RED, GRN_L, GRN, BLUE_L, BLUE, HSYNC, VSYNC
VGA_RED_L, VGA_RED, VGA_GREEN_L, VGA_GREEN, VGA_BLUE_L, VGA_BLUE, VGA_HSYNC, VGA_VSYNC

+5V_CRT
R416 4.7K_4
R425 4.7K_4

Layout Note : Refer chip spec page-20 ~ 23.

It is strongly recommended to shield RGB with ground.

L3 BLM15BA470SN1D VGA_CON_RED
L2 BLM15BA470SN1D VGA_CON_GREEN
L4 BLM15BA470SN1D VGA_CON_BLUE

CN8 CRT CONN

R426 37.4/F_4
R427 37.4/F_4
R428 37.4/F_4
R79 75/F_4
R75 75/F_4
R77 75/F_4
C246 4.7P/50V_4
C237 4.7P/50V_4
C239 4.7P/50V_4
C252 2.2P/50V_4
C235 2.2P/50V_4
C234 2.2P/50V_4

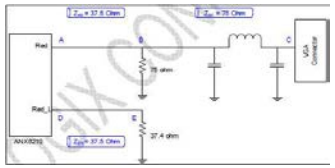
Place Rc,Rd,Re as close as possible to relative pins of ANX6210.

Place Rx,Ry,Rz as close as possible to the R/G/B pins of VGA header.

CRT_VCC
C707 0.1U/16V_4

R73 15/F_4 VGA_HSYNC_R
R74 15/F_4 VGA_VSYNC_R

Route the VGA_RED, VEA_BLUE, VGA_GREEN, VGA_CON_RED, VGA_CON_BLUE, VGA_CON_GREEN by 75 Ohm impendance.



+1.05V_CRTLDO

1.05V_CRT_DVDD
L5 *0 4/S
C269 4.7U/6.3V_4
C263 0.1U/16V_4
C268 1000P/50V_4
C257 0.1U/16V_4
C254 0.01U/50V_4
C245 1000P/50V_4

1.05V_CRT_AVDD
L6 *0 4/S
C270 4.7U/6.3V_4
C272 0.1U/16V_4
C261 1000P/50V_4
C253 0.1U/16V_4
C243 0.01U/50V_4
C256 1000P/50V_4

3V_CRT_AVDD
L28 *0 4/S
C699 4.7U/6.3V_4
C705 0.1U/16V_4
C708 1000P/50V_4
C706 0.1U/16V_4
C289 0.1U/16V_4
C285 0.01U/50V_4
C281 1000P/50V_4

3V_CRT_DVDD
L9 *0 4/S
C284 4.7U/6.3V_4
C288 0.1U/16V_4
C280 1000P/50V_4
C695 0.1U/16V_4
C260 0.01U/50V_4

20 mil

Pin-26 / LDO
LDO 1.05V output, can be connected to AVDD10/DVDD10 input.

U24C ANX6210FN-AB-R/QFN40
DVDD10 ×2, LDO, DVSS_PLL, AVDD10 ×3, AVSS ×4, AVDD33 ×4, EP, DVDD33 ×2
C286 10U/6.3V_4

3V_CRT_DVDD
Ra R414 4.7K_4
Rb R415 *10K_4
R413 4.7K_4
Rf R90 12K/F_4
C279 *0.1U/16V_4

Place Rf as close to the R_BIAS pin as possible.

Case 1: Keep Ra and remove Rb; ANX6210 in HPD process mode;
Case 2: Keep Rb and remove Ra; Use IRQ to inform source of VGA plug/unplug events

U24B ANX6210FN-AB-R/QFN40
R_BIAS, CFG_SCL, CFG_SDA, XTAL_IN, XTAL_OUT, TEST_EN, RESETN, GPIO
CRT_XIN, CRT_XOUT
R418 1M_4
Y2 27MHZ +-10PPM
C698 18P/50V_4
C696 15P/50V_4
R420 10K_4
R429 *6.2K_4
R422 4.7K_4
(2,12,24,27,29,30,32,50) PLTRST#
R432 *0 4/S
C714 *0.1U/16V_4

Pin-11 / GPIO
1: I2C Address is 0x50 and 0x8C
0: 4.7KΩ resistor to pull down, I2C address is 0x52 and 0x8E

(9,10,11,12,13,14,16,17,19,21,22,23,24,26,28,29,30,31,32,36,43,45,49,50,54) +3V
(21,22,23,25,30,31,43,45,49,58) +5V

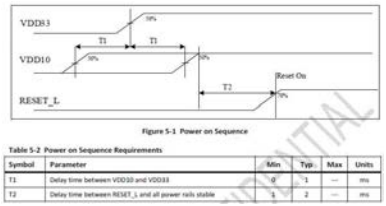


Figure 5-1 Power on Sequence

Table 5-2 Power on Sequence Requirements

Symbol	Parameter	Min	Typ	Max	Units
T1	Delay time between VDD10 and VDD33	0	1	—	ms
T2	Delay time between RESET_L and all power rails stable	1	2	—	ms

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Quanta Computer Inc.
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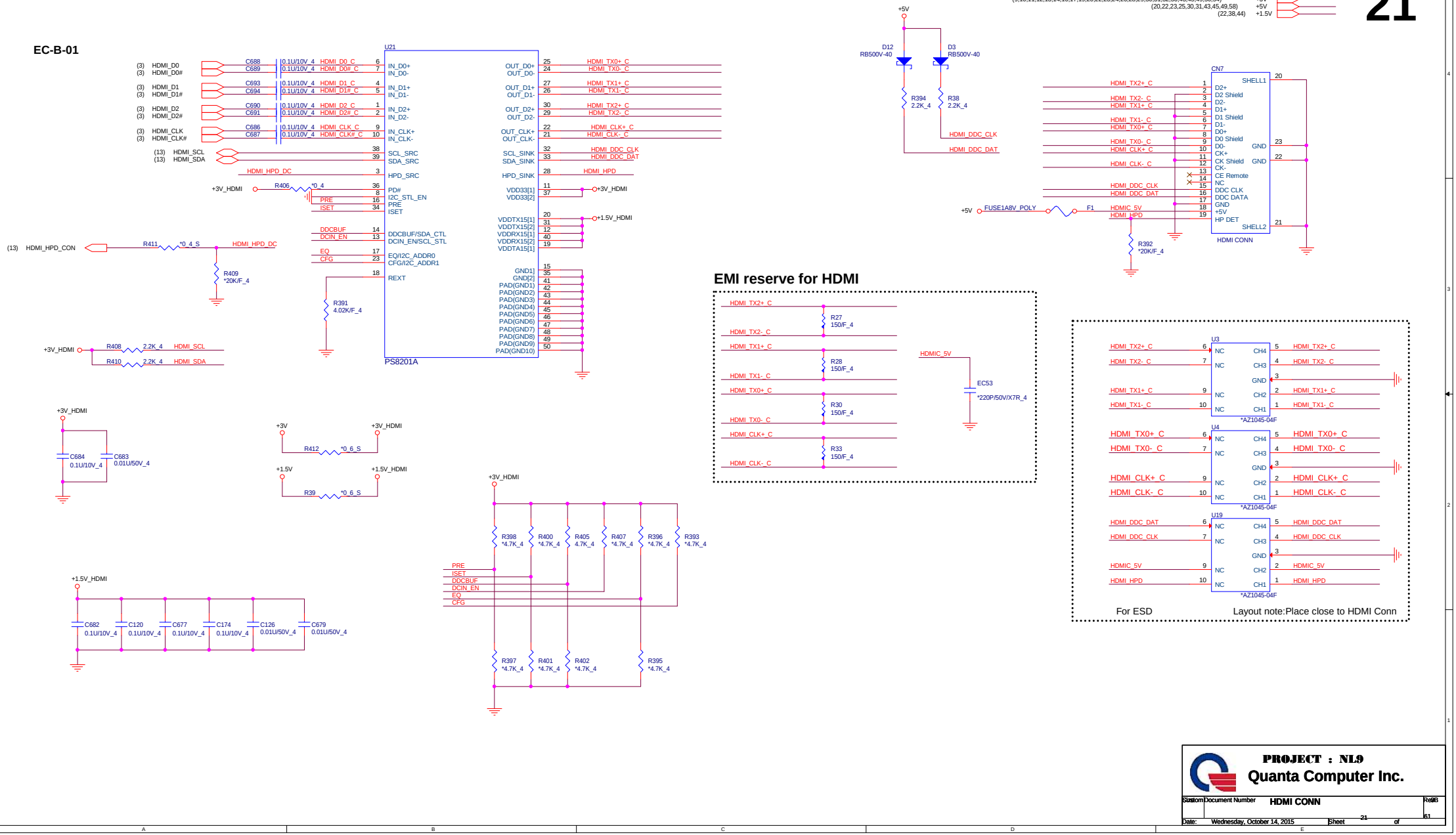
EC-B-01



EMI reserve for HDMI

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Quanta Computer Inc.

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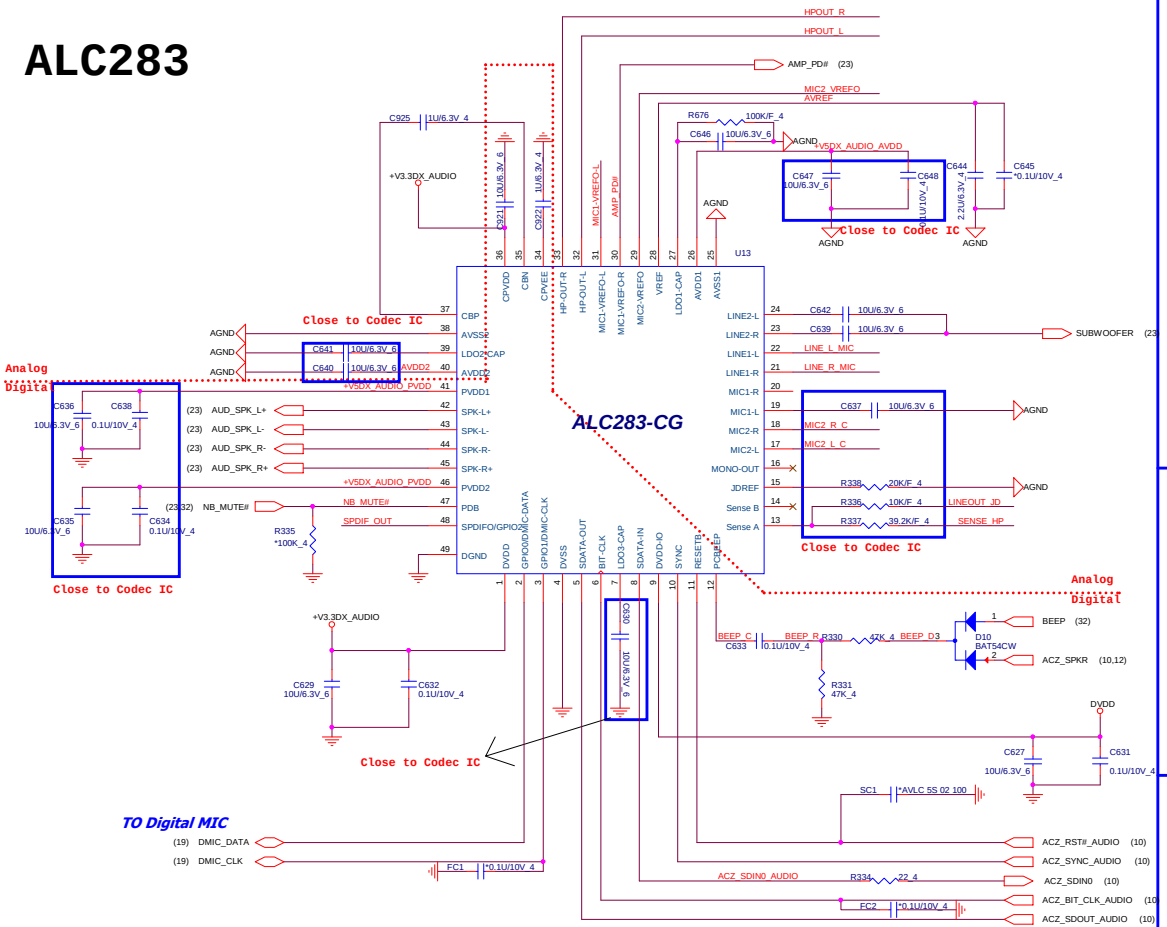
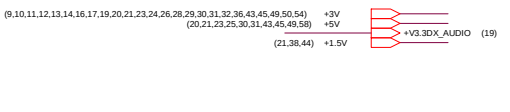
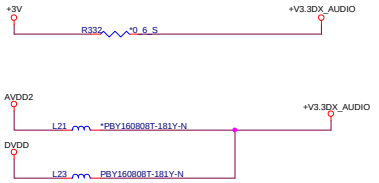
ALC283

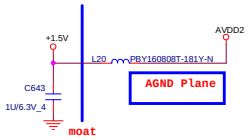




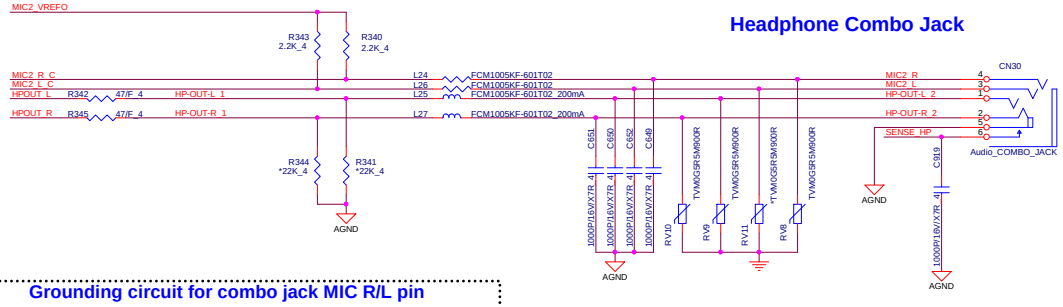
CODEC 5V POWER

+3.3V_AUDIO_CODEC
Max Current : 419mA

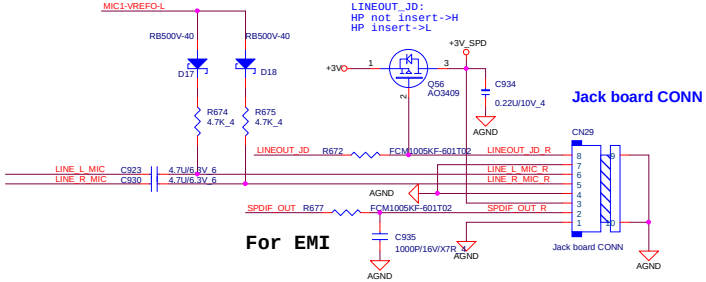




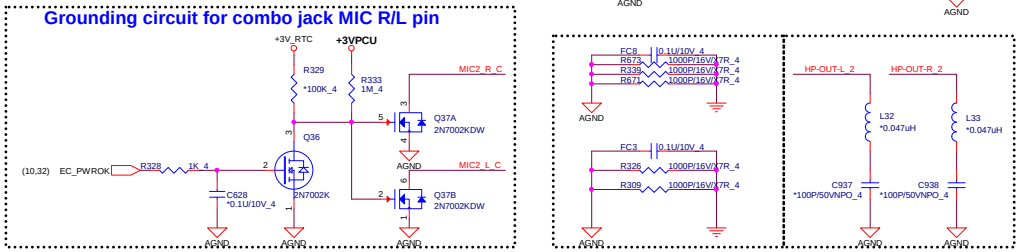
Headphone Combo Jack

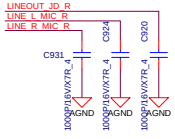


External MIC+SPDIF



Grounding circuit for combo jack MIC R/L pin





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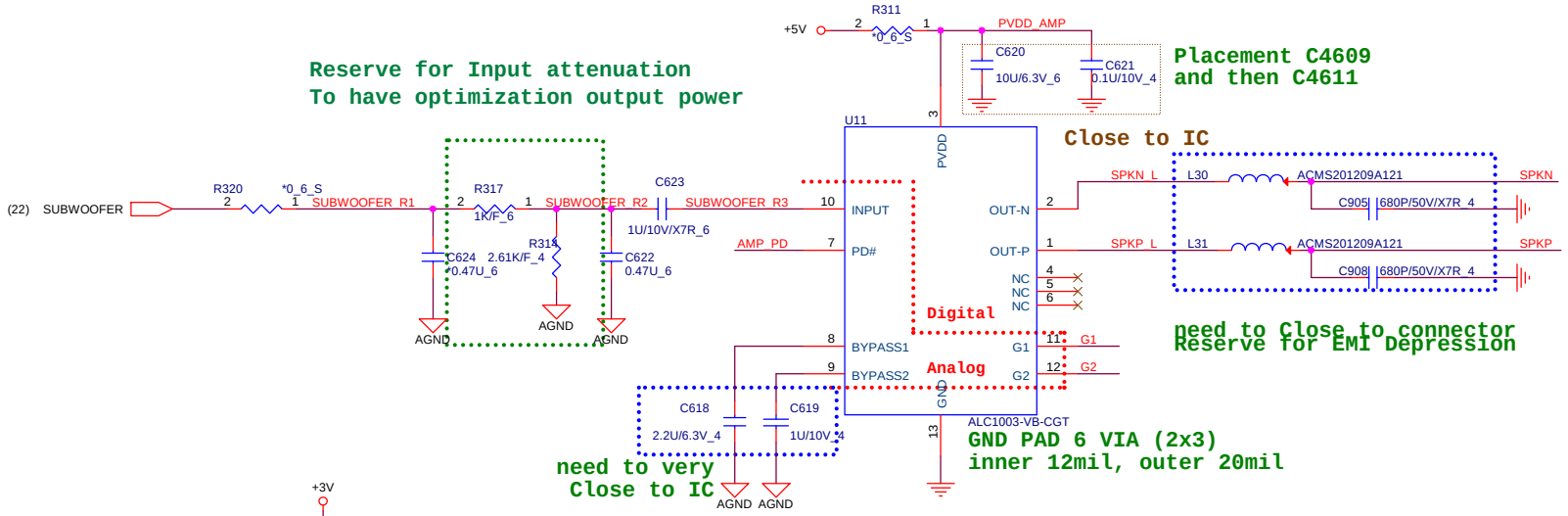
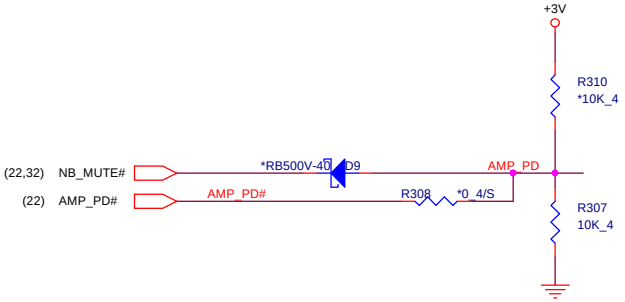
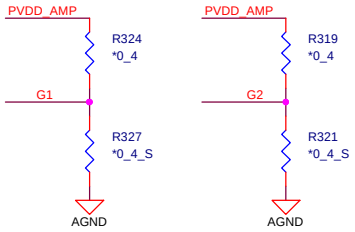
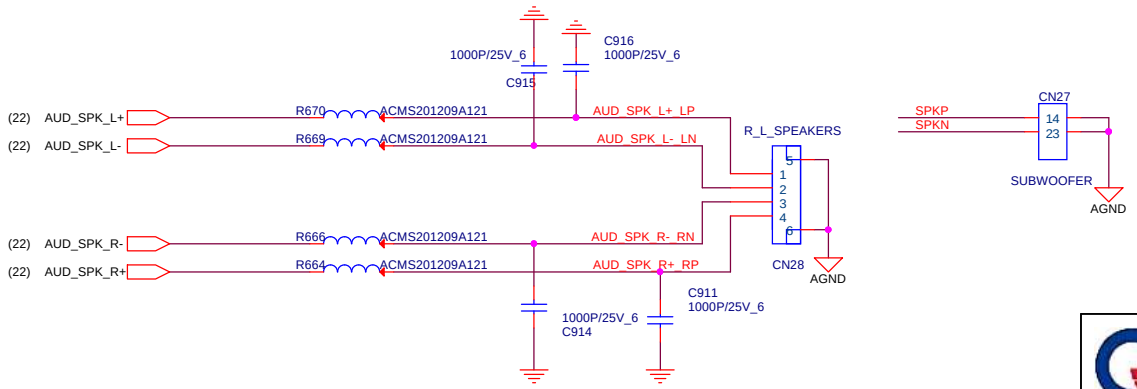






Output Gain Table

R364	R363	R373	R372	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB



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Quanta Computer Inc.

Size: Custom	Document Number: Amplifer(ALC1003)		Rev: 3B
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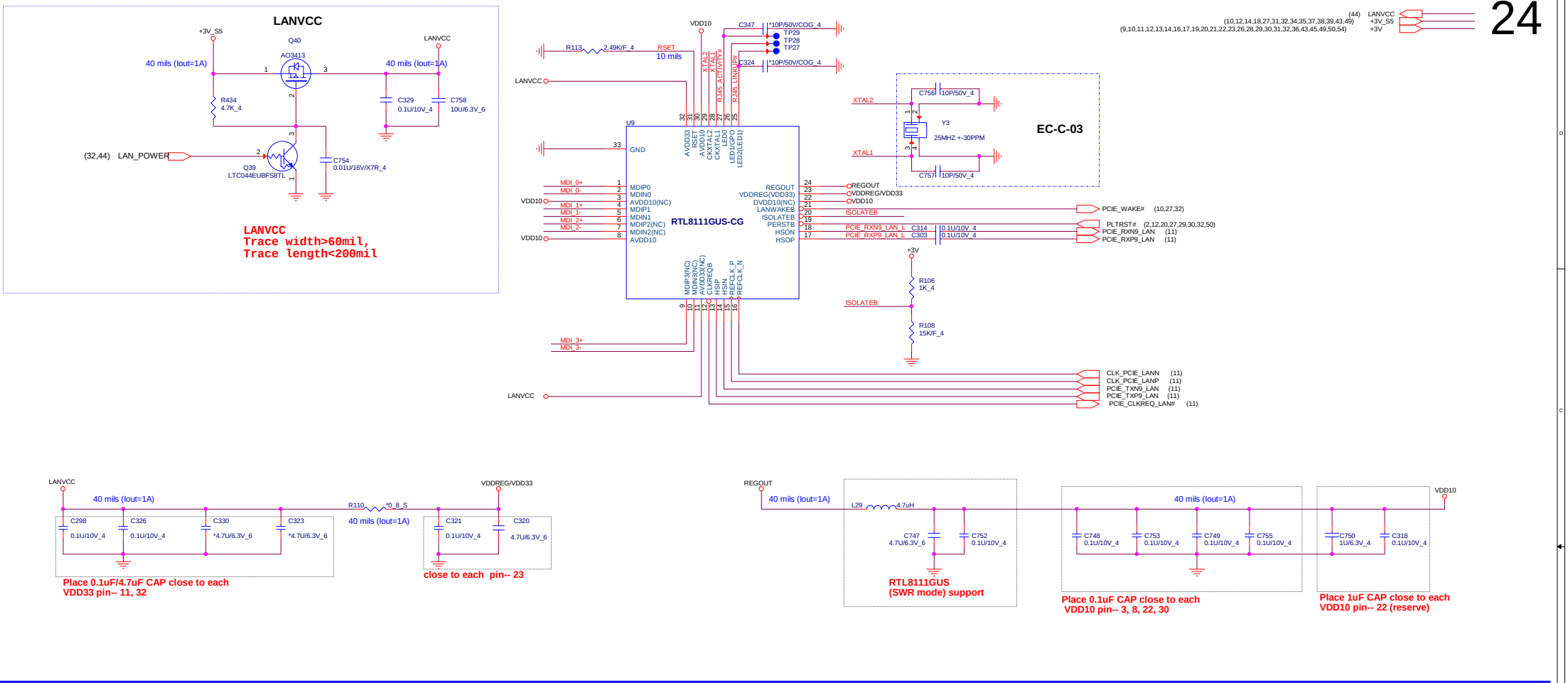
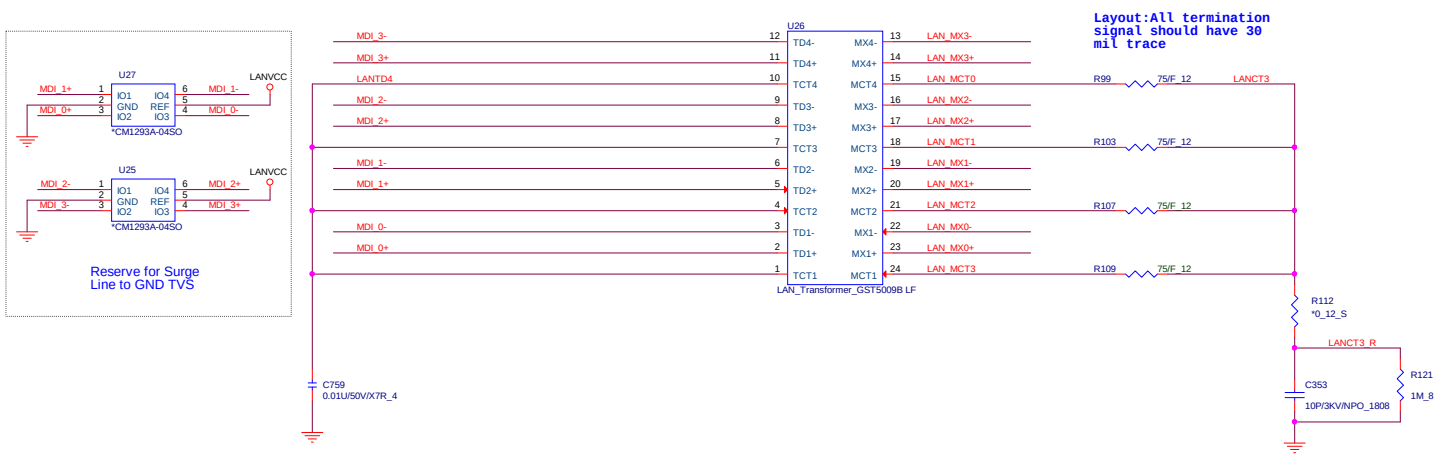
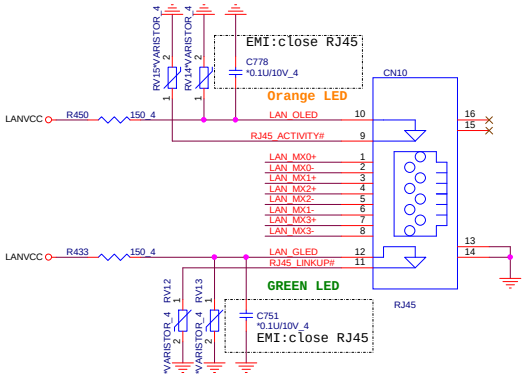


Tramsformer



RJ45 Connector



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Quanta Computer Inc.

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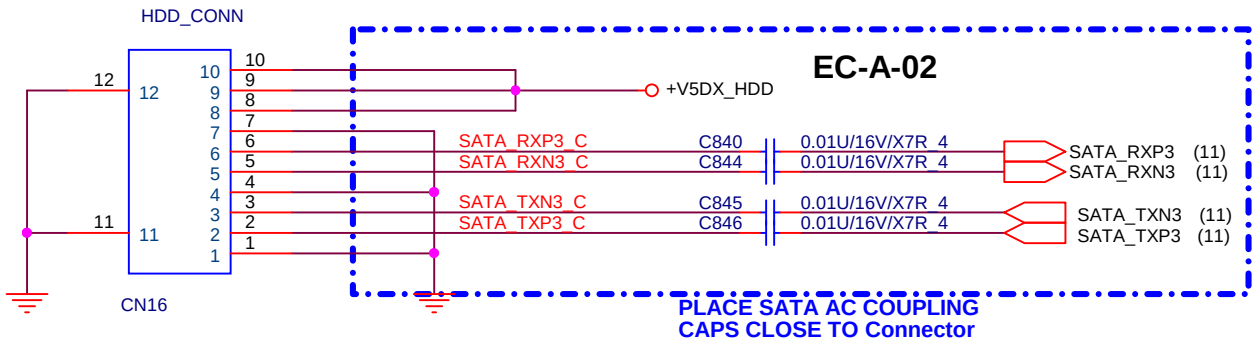
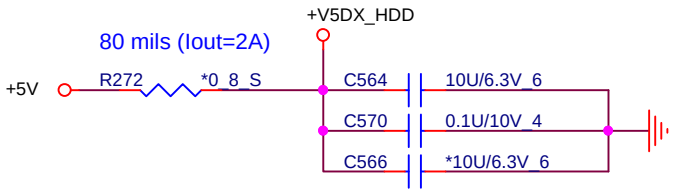
HDD

(20,21,22,23,30,31,43,45,49,58) +5V

25



DC Current rating: 2 A (MAX)



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Quanta Computer Inc.

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Custom	SATA HDD	3B

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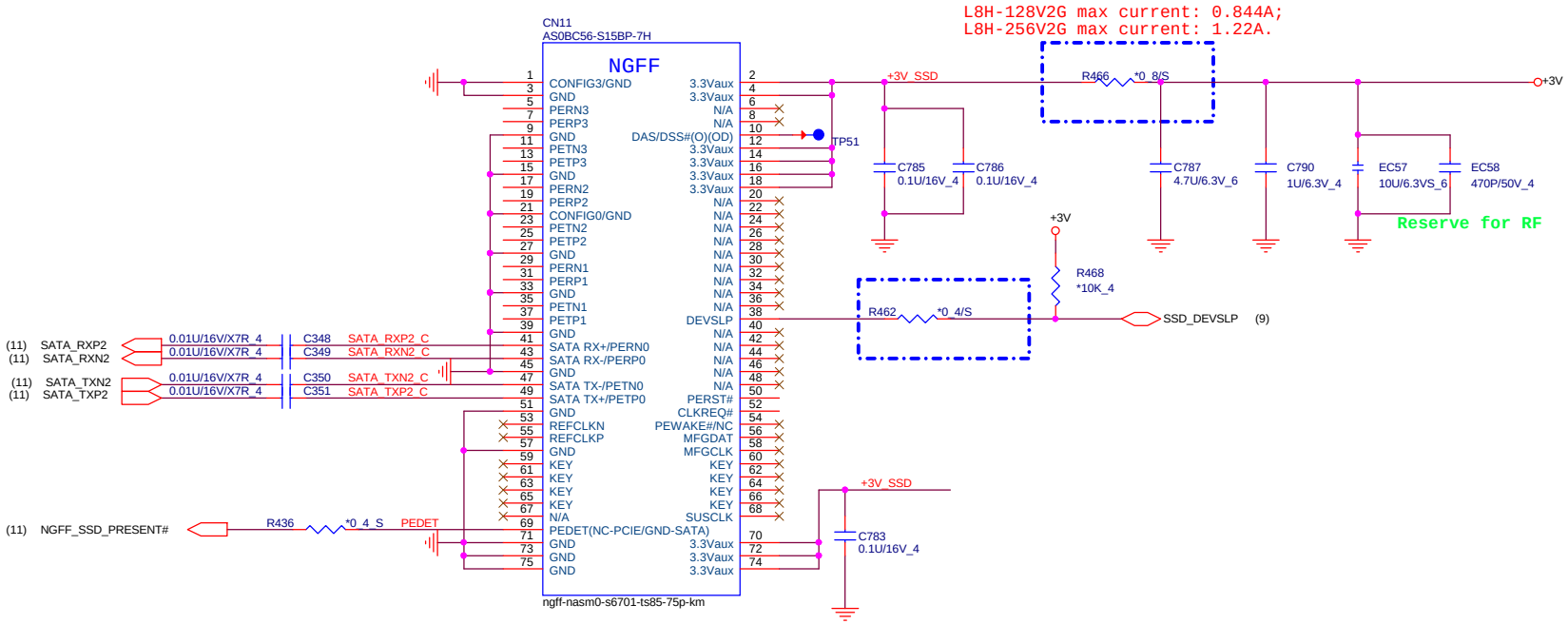

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Quanta Computer Inc.

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Custom	SSD mSATA X2	3B

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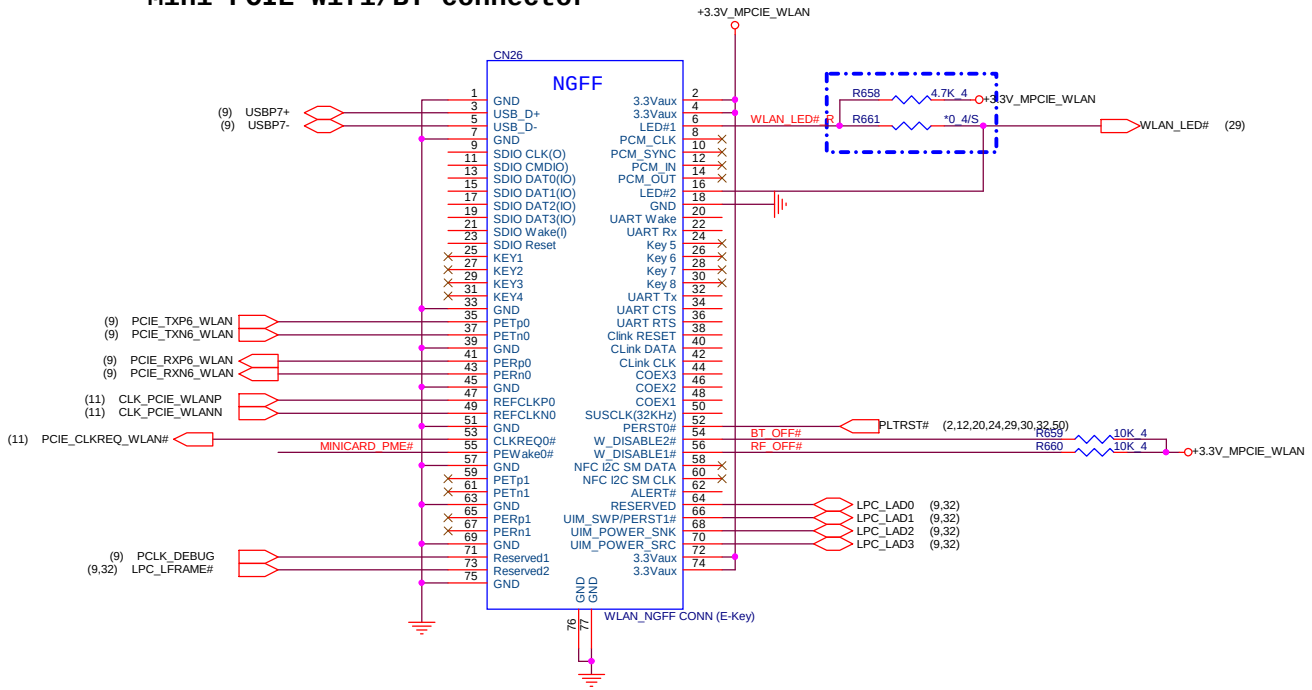
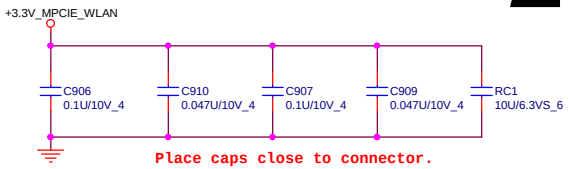
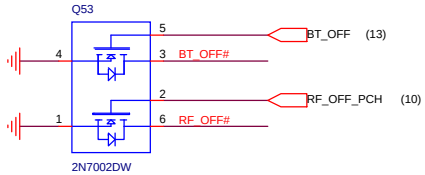
Mini PCIE Wifi/BT connector

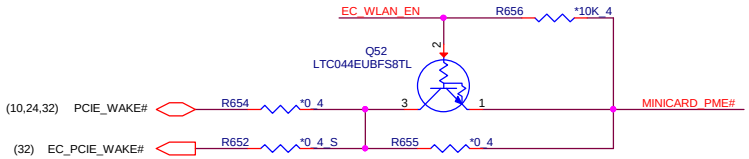


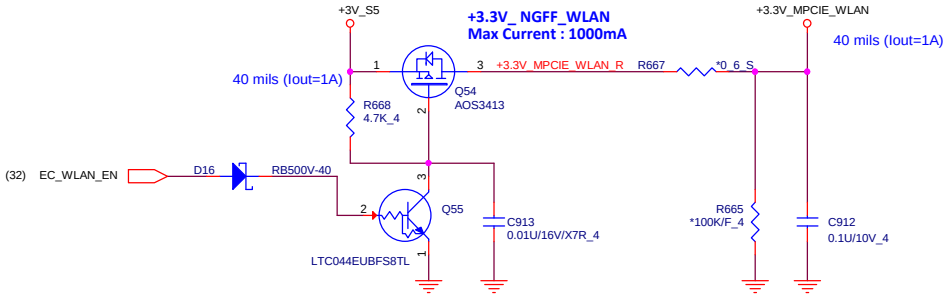
(10,12,14,18,24,31,32,34,35,37,38,39,43,49) +3V_S5
(21,22,38,44) +1.5V



Place caps close to connector.







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Quanta Computer Inc.

Size:	Document Number: Wifi/BT MiniPCIE		Rev: 3B
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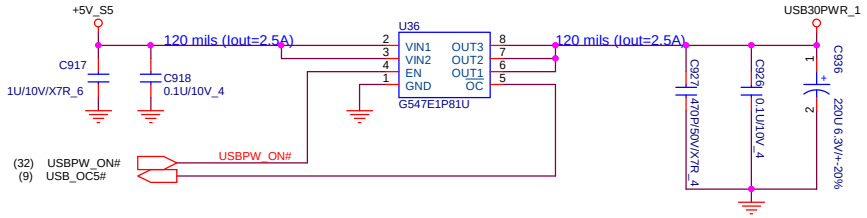
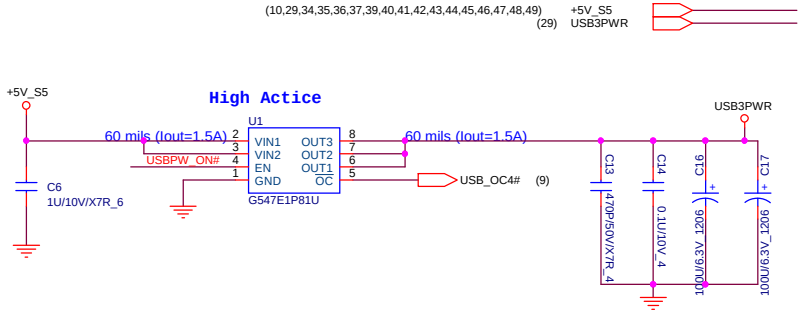
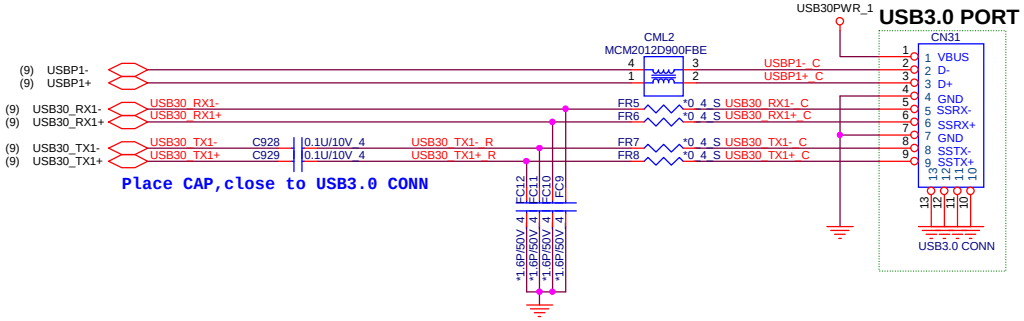
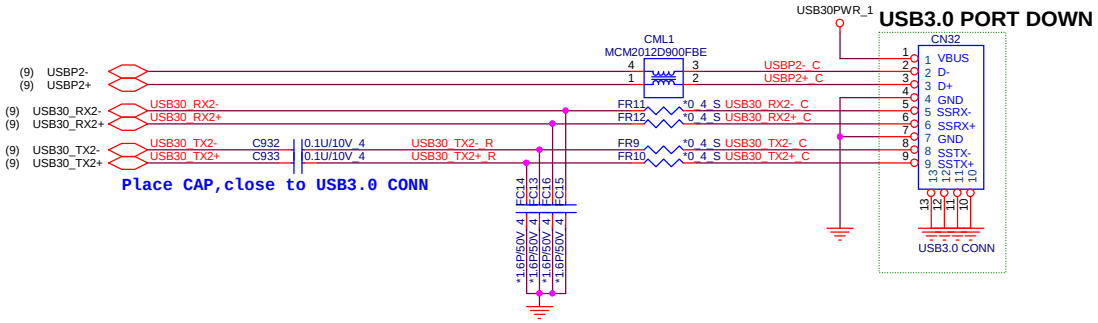
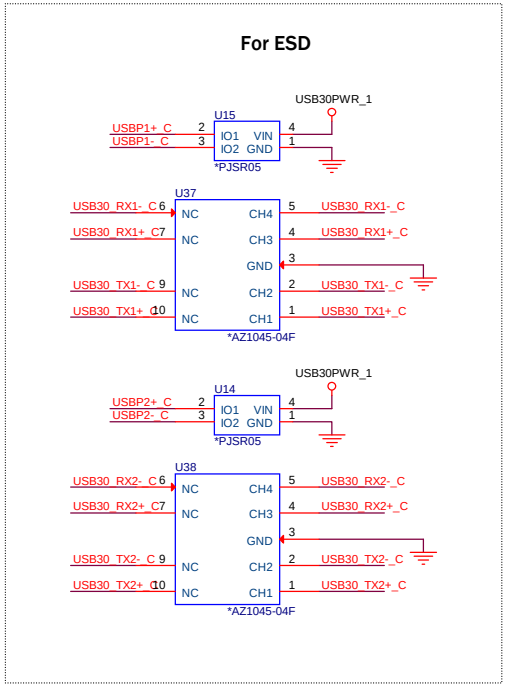


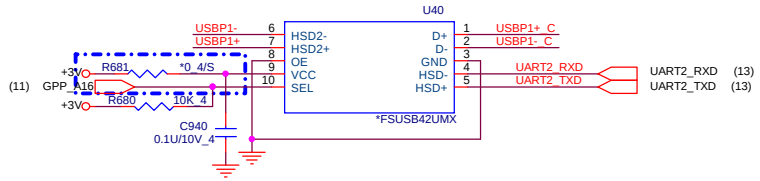








UART for DEBUG



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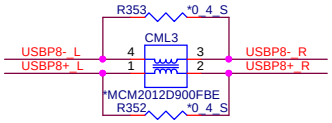
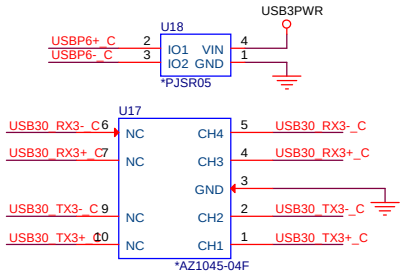
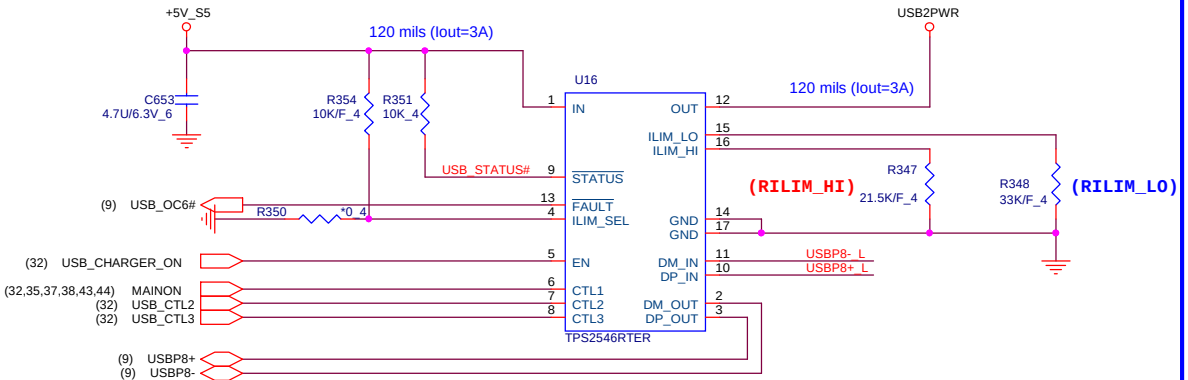




USB Charger 2.0 Port



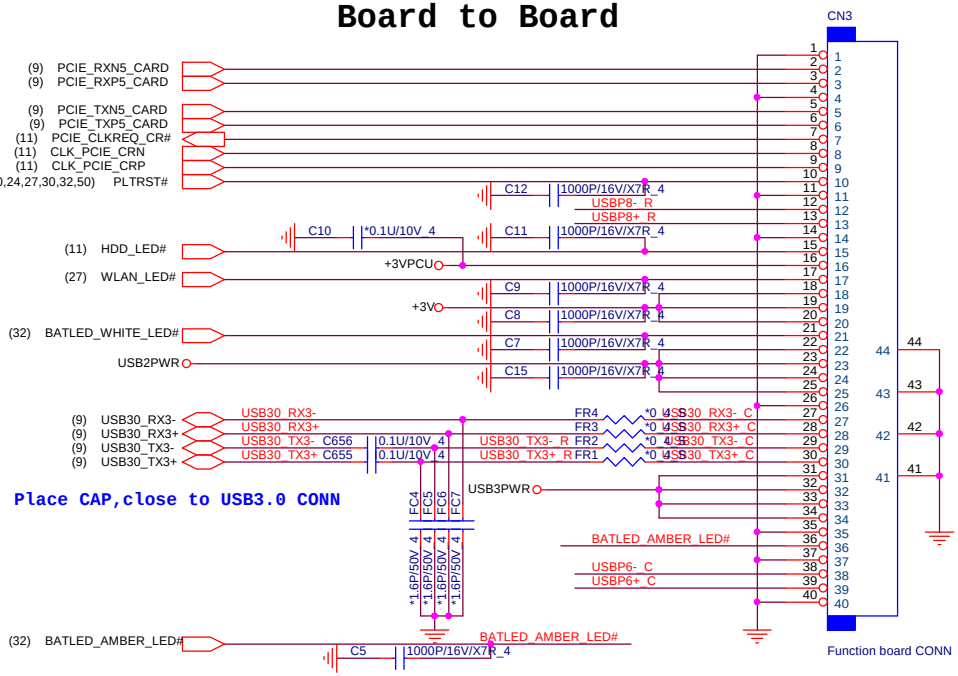
RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

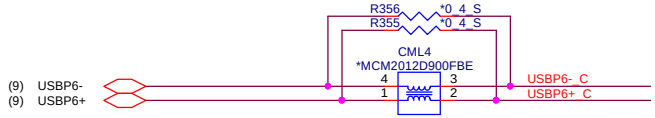
$$I_{OS\_typ}(mA) = \frac{50{,}500}{(R_{ILIM\_XX}(k\Omega) + 0.1)}$$

(28) USB3PWR
(10,28,34,35,36,37,39,40,41,42,43,44,45,46,47,48,49) +5V_S5
(9,10,11,12,13,14,16,17,19,20,21,22,23,24,26,28,30,31,32,36,43,45,49,50,54) +3V

29

Board to Board





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Quanta Computer Inc.

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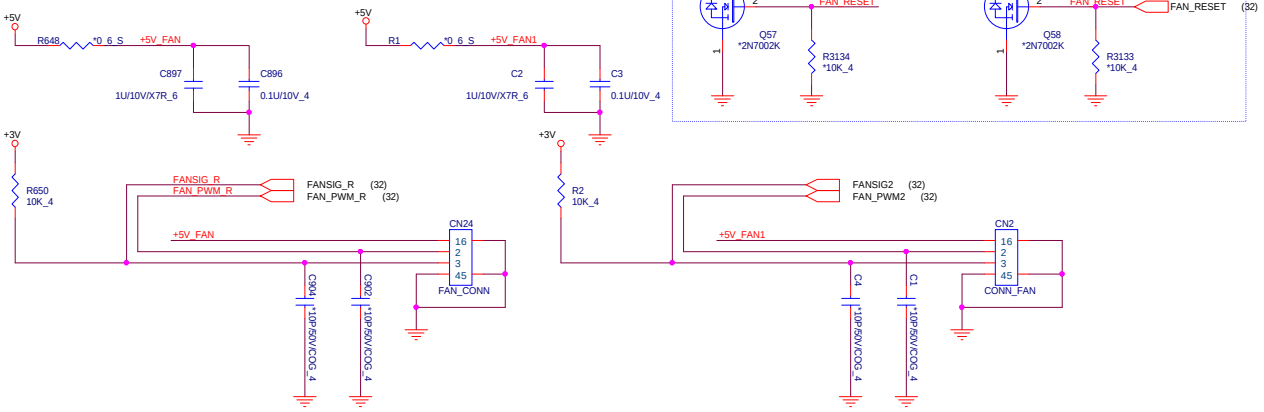
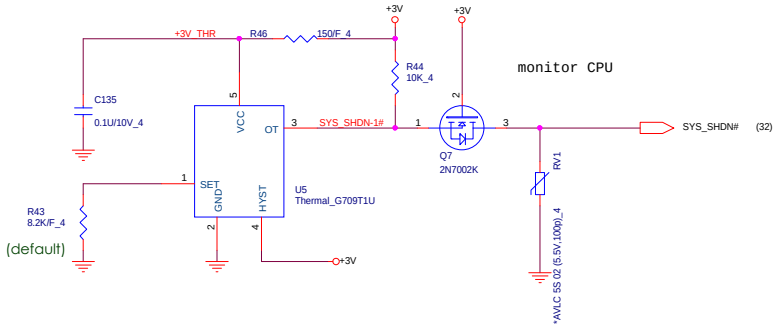
FAN CONTROL

(9,10,11,12,13,14,16,17,19,20,21,22,23,24,26,28,29,31,32,36,43,45,49,50,54) +3V
(20,21,22,23,25,31,43,45,49,58) +5V

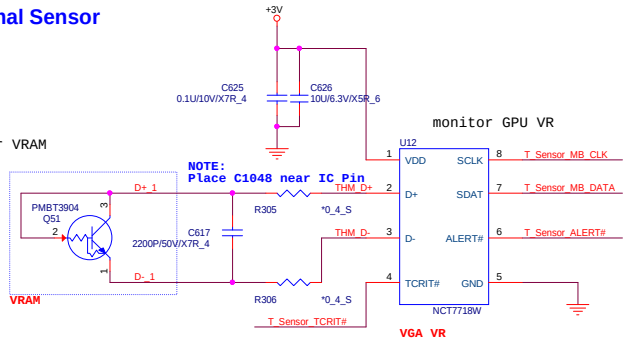


Thermal Sensor



Thermal Sensor

monitor VRAM

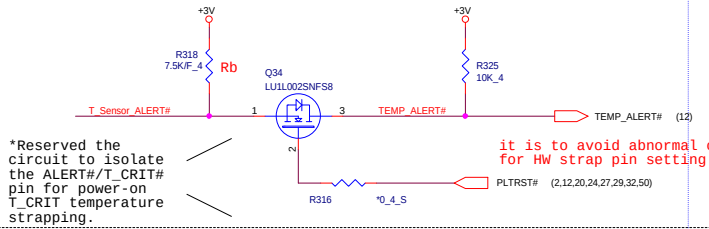


monitor GPU VR

VGA VR

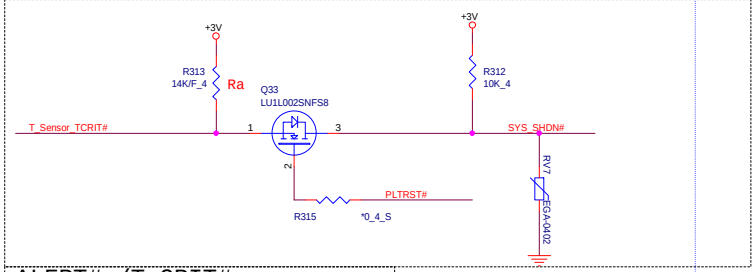
ADDRESS: 98

EC-A-06



*Reserved the circuit to isolate the ALERT#/T_CRIT# pin for power-on T_CRIT temperature strapping.

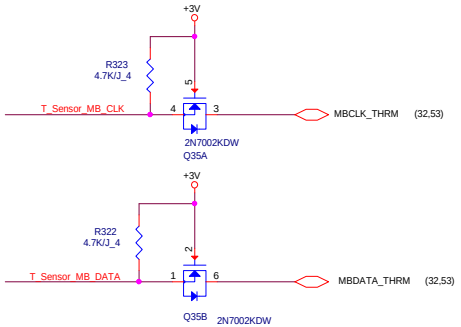
it is to avoid abnormal operation when power on within 100ms for HW strap pin setting HW Shut-down Temp. 109 ℃



ALERT# /T_CRIT# Pull-up Resistor

Rb \ Ra	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

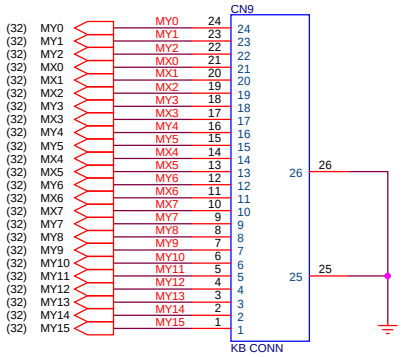


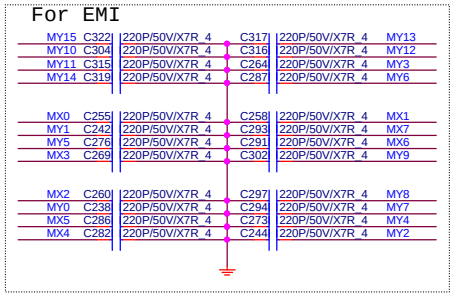
PROJECT : NL9

Quanta Computer Inc.

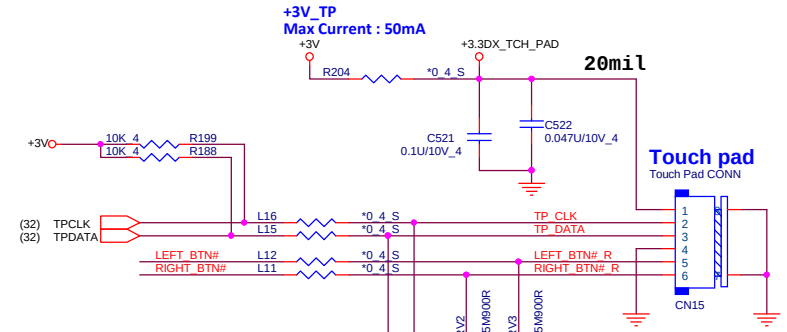
Size: Custom	Document Number: FAN/Thermal		Rev: 3B
Date: Wednesday, October 14, 2015	Sheet: 30	of: 61	

KEYBOARD

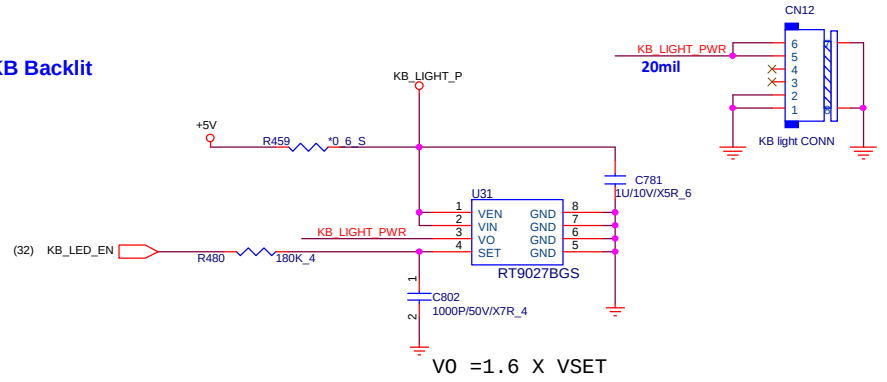


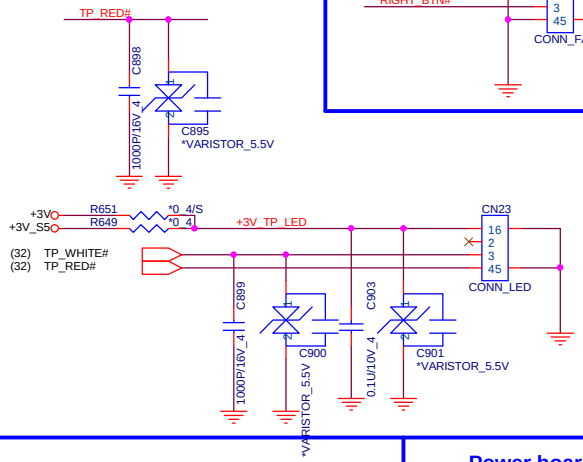


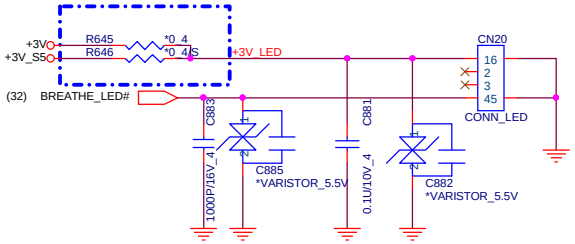
(20,21,22,23,25,30,43,45,49,58) +5V
(9,10,11,12,13,14,16,17,19,20,21,22,23,24,26,28,29,30,32,36,43,45,49,50,54) +3V
(10,22,29,32,33,34) +3VPCU
(10,12,14,18,24,27,32,34,35,37,38,39,43,49) +3V_S5



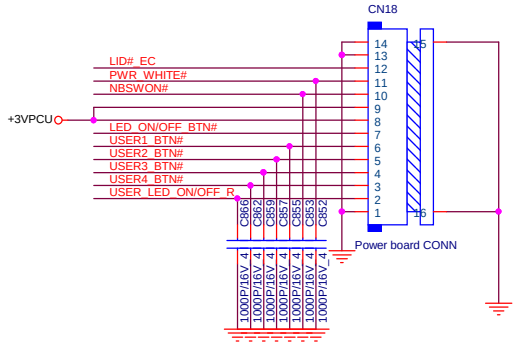
KB Backlit



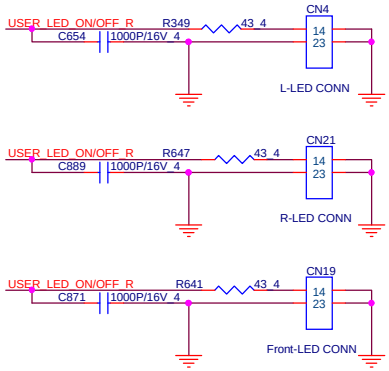




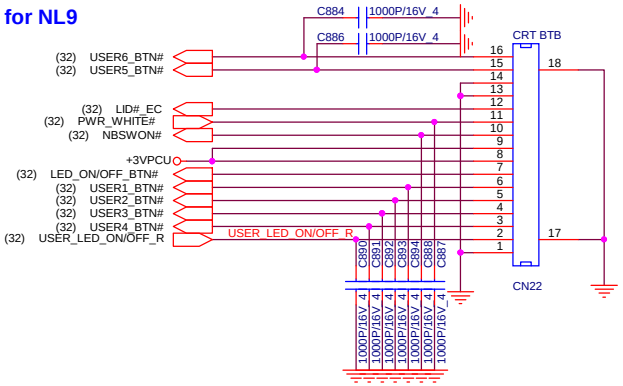
Power board for NL8



LED CONN



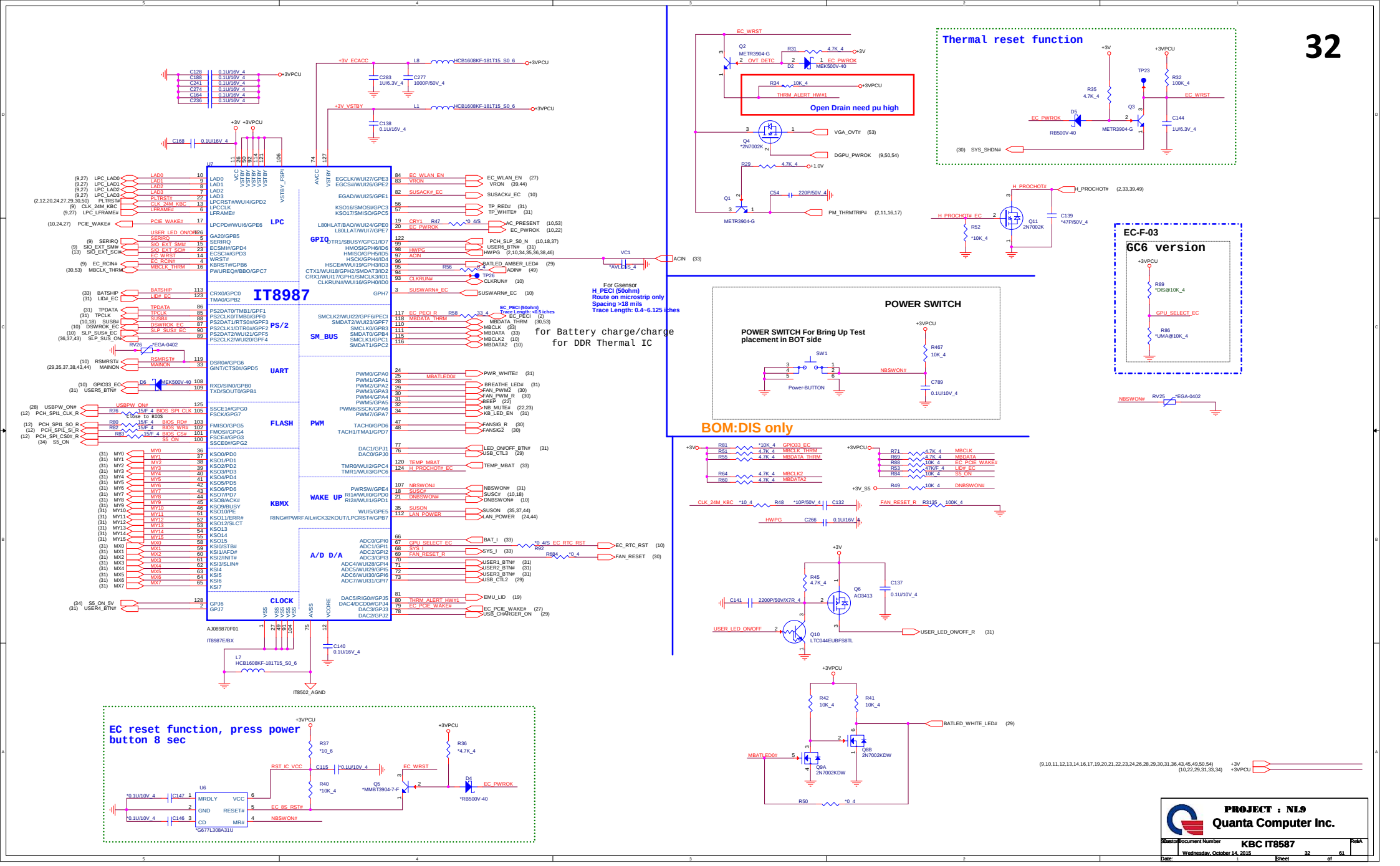
Power board for NL9



PROJECT : NL9

Quanta Computer Inc.

Custom Document Number	KB/TP/LID	Rev 3B
Date: Wednesday, October 14, 2015	Sheet 31 of 61	


IT8987
LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK
for Battery charge/charge
for DDR Thermal IC
Thermal reset function
Open Drain need pu high
POWER SWITCH
POWER SWITCH For Bring Up Test
placement in BOT side
BOM:DIS only
EC-F-03
GC6 version
EC reset function, press power
button 8 sec
PROJECT : NL9
Quanta Computer Inc.
KBC IT8587

(49,58) +VA
(19,34,35,36,39,40,41,42,46,47,49,58) +VIN
(10,22,29,31,32,34) +3VPCU

180W for N16E-GT
150W for N16P-GX
120W for N16P-GT

Do Not add test pad on BATDIS_G signal

EMI request for ISN

120W&150W follow 180W setting

Place this ZVS close to Diode away +VIN

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

For ISN

ACDET=17.2V

VIDCHG = 8 or 16 × (VSRN – VSRP)

16.5K 180W for N16E-GT
20K 150W for N16P-GX
25K 120W for N16P-GT

BQ24780SRUYR

CN14 CONN_DCIN

PQ42 AON7401

PQ9 MMDT2907A

PQ26 QM3016D

PQ29 QM3016D

PD12 SS3040HE

PD13 P4SMA20A

PD11 *P4SMAJ20A

PD20 PDZ8.2B

PQ27 EMB20N03V

PQ28 EMB20N03V

PQ2 *2N7002K

PJP8 *SHORTPAD

PJP7 *SHORTPAD

PD5 PDZ5.6B

PD4 PDZ5.6B

PL4 3.3uH/6A(PCMC063T-3R3MN)

CN5 51279-01001-V01

PR195 RC1206-R005

PR3129 16P-GX@20K/F_4

PR3129 16P-GT@24.9K/F_4

(19,33,35,36,39,40,41,42,46,47,49,58) +VIN
(10,28,29,35,36,37,39,40,41,42,43,44,45,46,47,48,49) +5V_S5
(10,22,29,31,32,33) +3VPCU
(10,12,14,18,24,27,31,32,35,37,38,39,43,49) +3V_S5

5 Volt
Fsw : 400KHz
Peak : 11.4A
OCP : 15A

3.3 Volt
Fsw : 475KHz
Peak : 6.9A
OCP: 9A

Place these CAPs close to FETs

Place these CAPs close to FETs

PU18 TPS51285BRUKR

PQ16 TPCC8067

PQ17 TPCC8065

PQ19 TPCC8065

PQ20 TPCC8067

PJP3 *SHORTPAD

PJP4 *SHORTPAD

PJP15 *SHORTPAD

PJP16 *SHORTPAD

PL22 ETQP3W1R5WFN-1.5

PL23 NIMS0603N-2R2M

(32) S5_ON_5V

S5_ON (32)

HWPG (2,10,32,35,36,38,46)

*ANC SS 02 (5.9V-10V)_4

PROJECT : NL8A
Quanta Computer Inc.
Size: Custom
Document Number: 3V/5V (TPS51285BRUKR)
Rev: 3B
Date: Wednesday, October 14, 2015
Sheet 34 of 61

(2,6,10,16,17,44,47) +1.2VSUS
(10,28,29,34,36,37,39,40,41,42,43,44,45,46,47,48,49) +5V_S5
(19,33,34,36,39,40,41,42,46,47,49,58) +VIN

+1.2VSUS
1.2 Volt +/- 5%
TDC : 8A
PEAK : 10A
OCP : 15A
Width : 280mil

TDC : 0.45A
PEAK : 0.6A
Width : 40mil

(3mA)

Rds(on) 3.8m ohm(max)

Vo=(0.675*(1+(R1/R2))

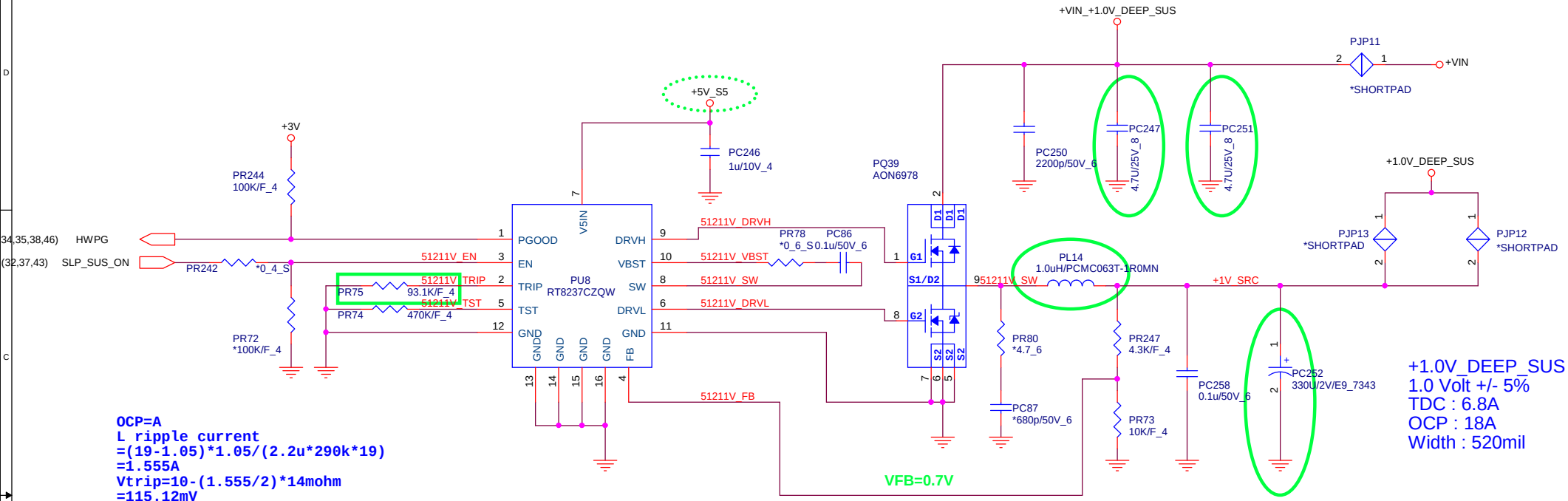
7/09 Chaneg DDR3L to DDR4
Adding +2.5V Power Rail

+2.5V_SUS
2.5Volt +/- 5%
TDC : 0.75A
PEAK : 1A
Width : 40mil

Vo=(0.6(R1+R2)/R2)

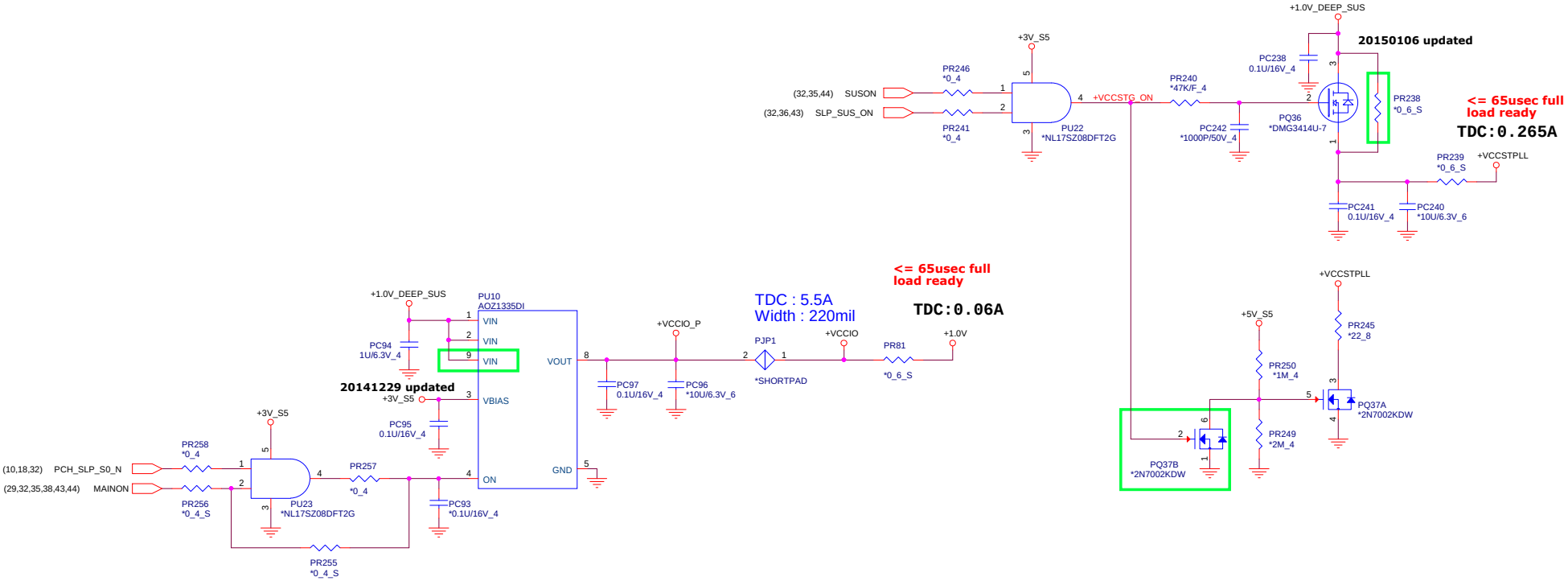
PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8231B)	3B
Date: Wednesday, October 14, 2015	Sheet 35 of 61	



Quanta Computer Inc.		
PROJECT : ZRW		
Size	Document Number: +1V_S5 (RT8237CZQW)	Rev: 1A
Date: Wednesday, October 14, 2015	Sheet 36 of 61	

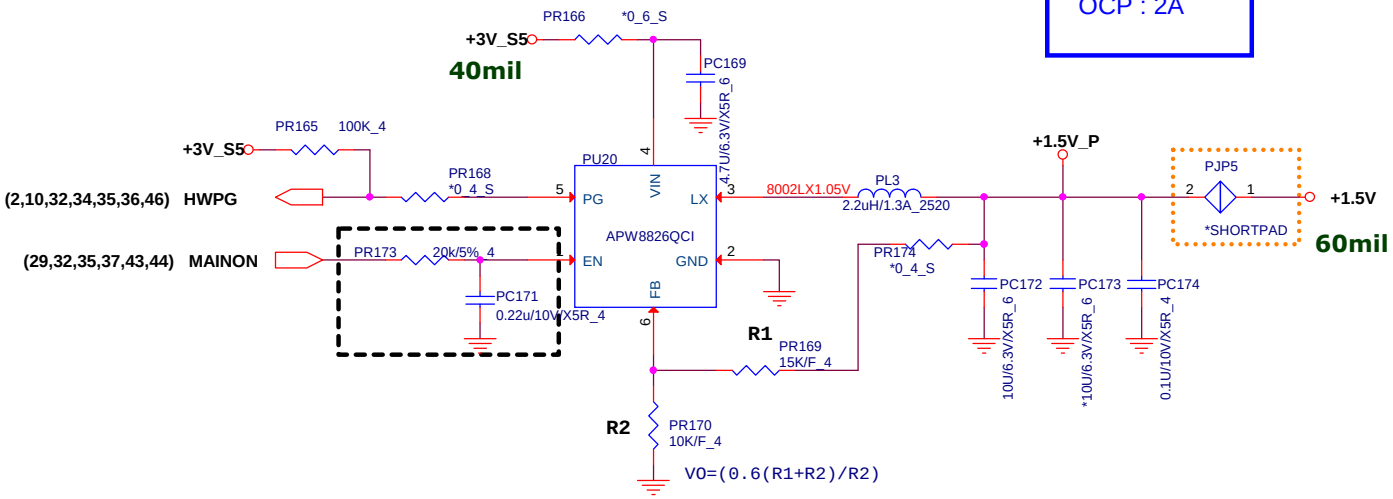
+1.0V (2,6,10,32)
+3V_S5 (10,12,14,18,24,27,31,32,34,35,38,39,43,49)
+5V_S5 (10,28,29,34,35,36,39,40,41,42,43,44,45,46,47,48,49)
+VCCIO (3,6)
+VCCSTPLL (2,6,11)
+1.0V_DEEP_SUS (10,11,14,36,39,44)



NB5	PROJECT : X1B-10L Quanta Computer Inc.	
Size: Custom	Document Number: +1.0V/+VCCSTPLL	Rev: 1A
Date: Wednesday, October 14, 2015	Sheet 37 of 61	

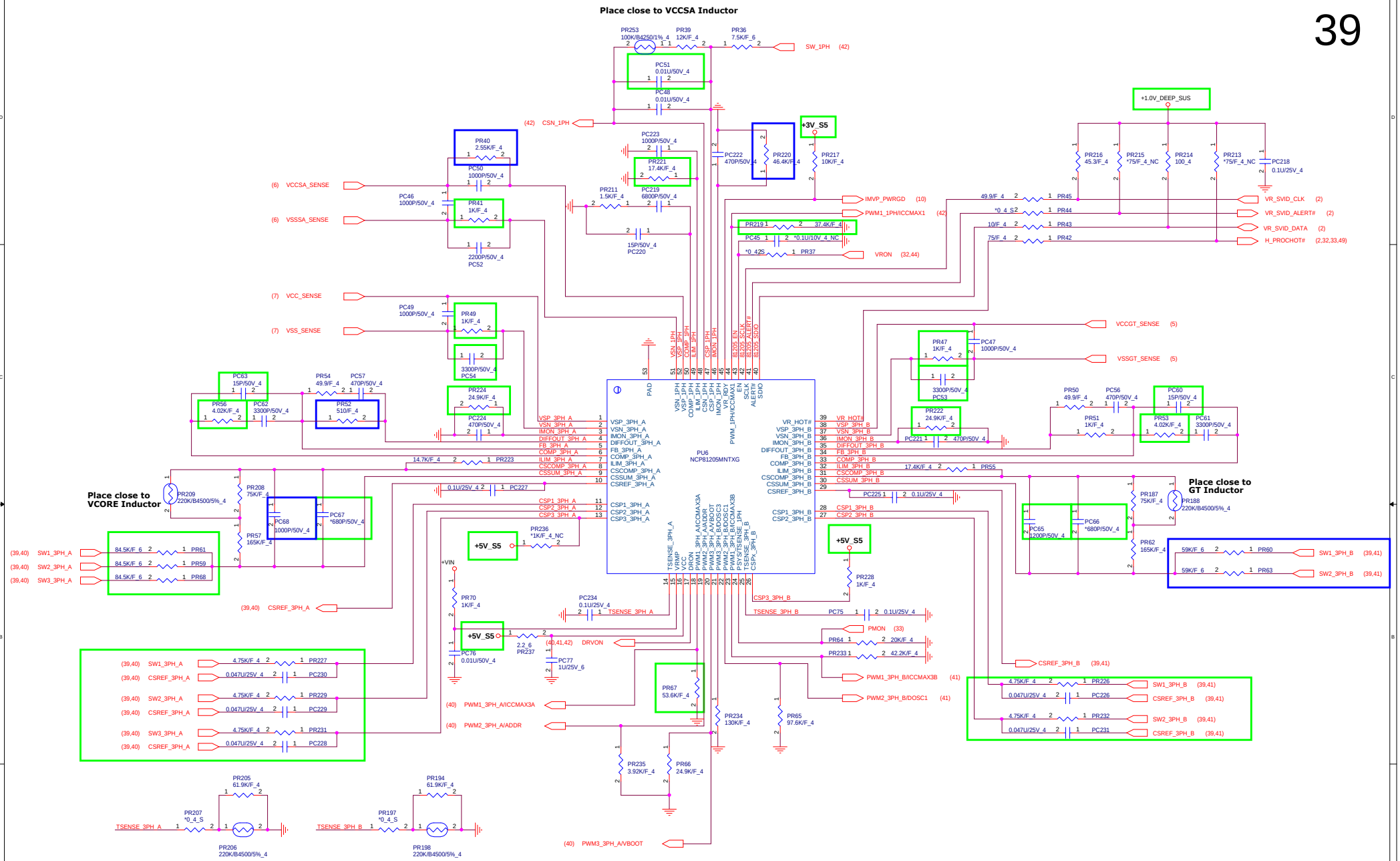
(10,28,29,34,35,36,37,39,40,41,42,43,44,45,46,47,48,49) +5V_S5
(19,33,34,35,36,39,40,41,42,46,47,49,58) +VIN

+1.5V
Fsw : 1.5MHz
Peak : 1A
OCP : 2A

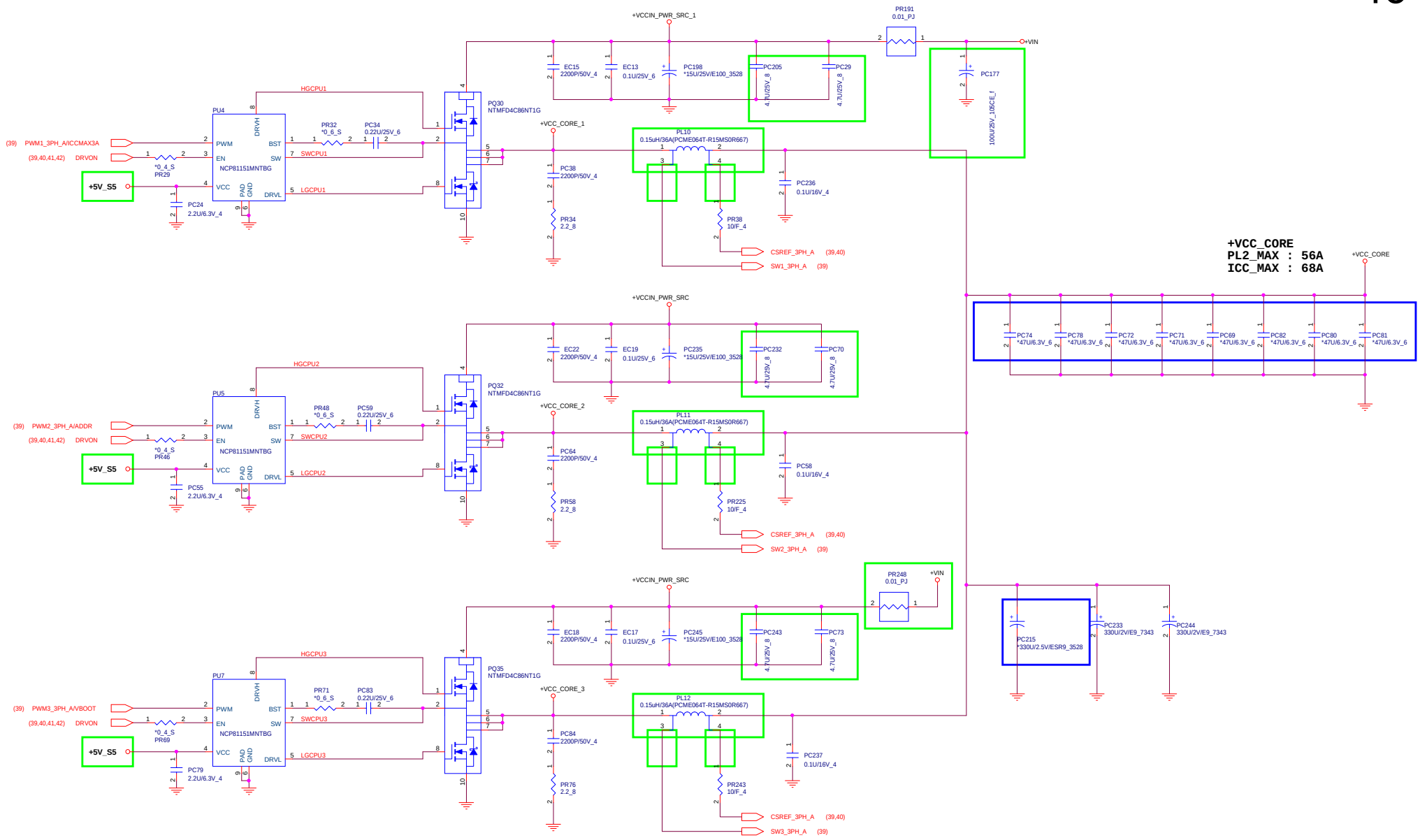


PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.8V (APW8713)	3B
Date: Wednesday, October 14, 2015	Sheet 38 of 61	



Quanta Computer Inc.			
PROJECT : AM9A			
Size	Document Number		Rev
	IMVP8 VR (NCP81205)		A
Date: Wednesday, October 14, 2015	Sheet 39 of 61		

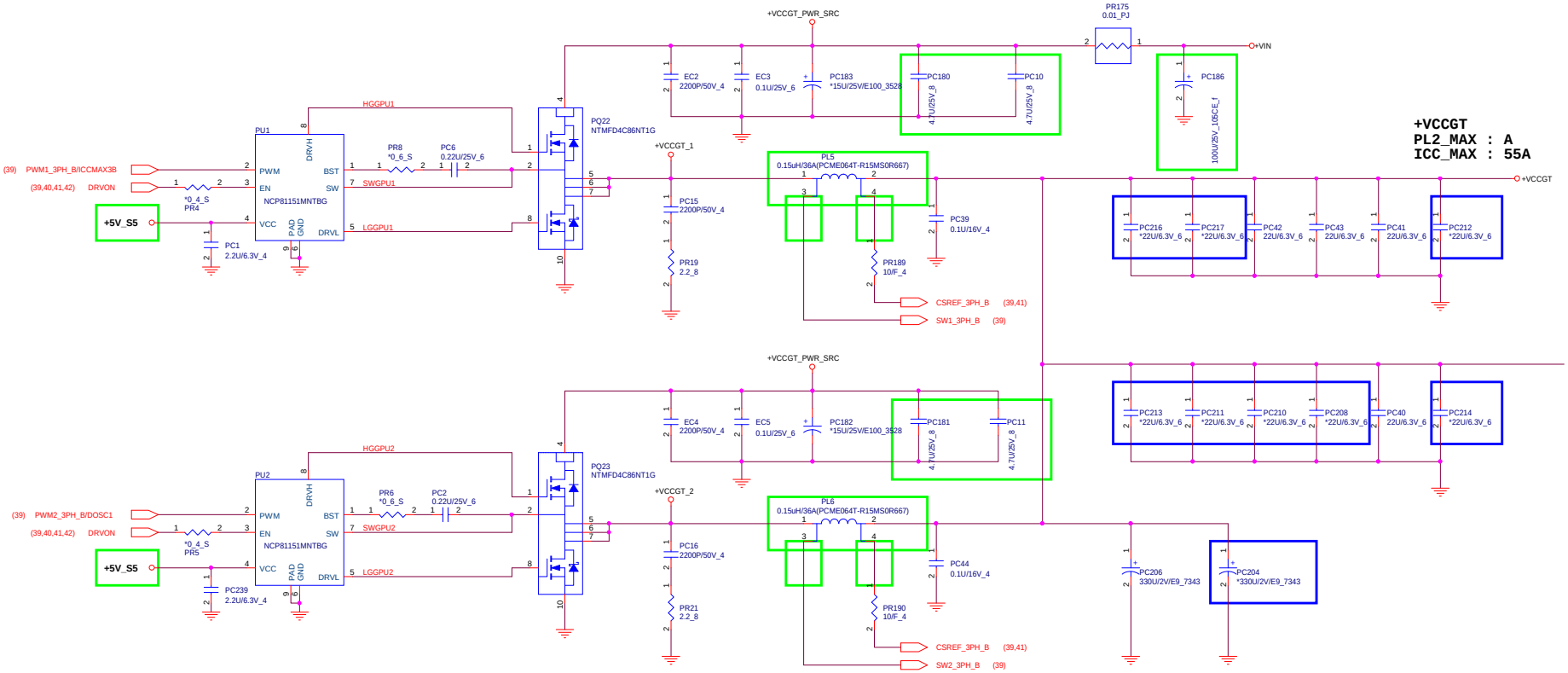


Quanta Computer Inc.

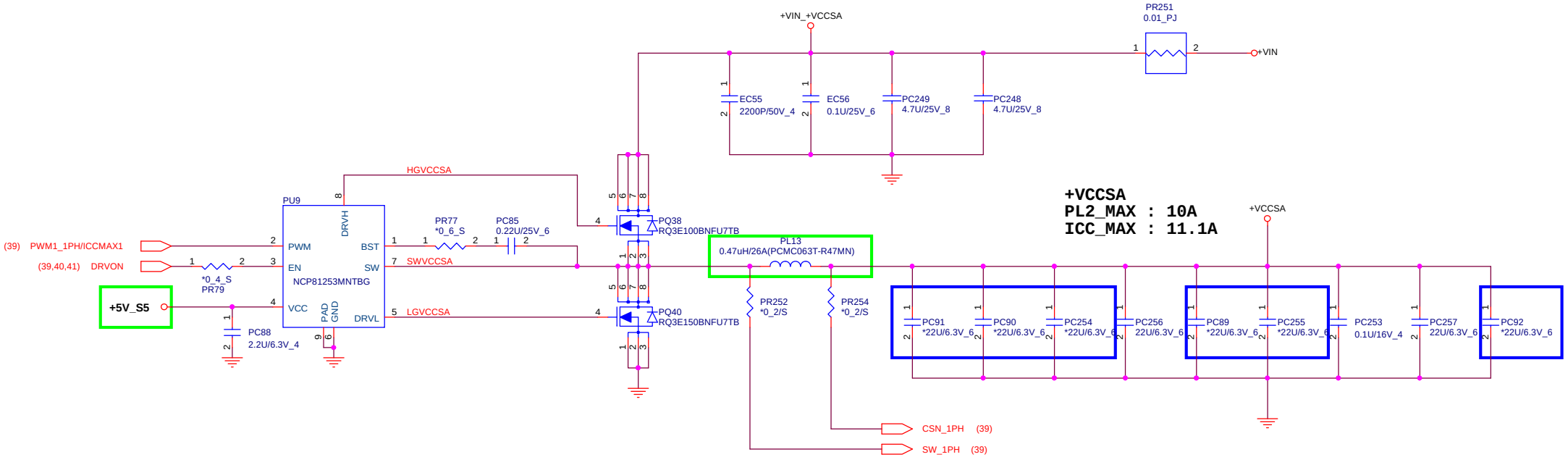
PROJECT : AM9A

Size	Document Number	Rev
	VCCIA 3-Phase Power Stage	A

Date: Wednesday, October 14, 2015 Sheet 40 of 61



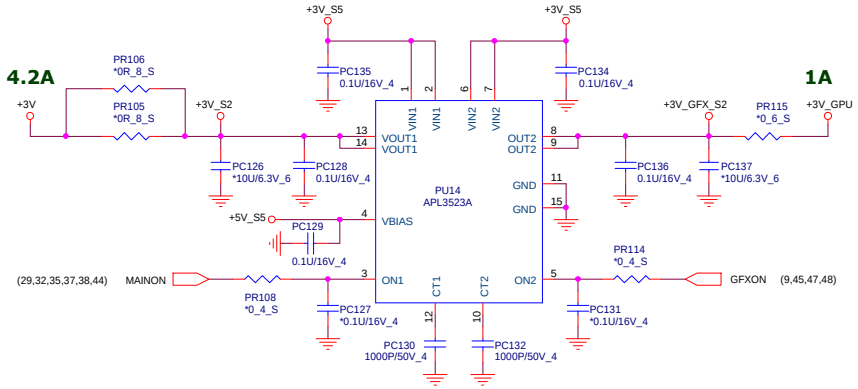
Quanta Computer Inc.		
PROJECT : AM9A		
Size	Document Number: VCCGT 2-Phase Power Stage	Rev: A
Date: Wednesday, October 14, 2015	Sheet 41 of 61	

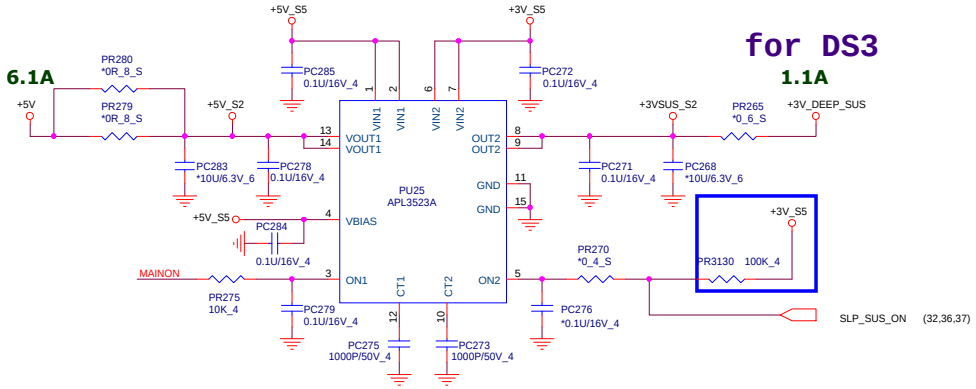


Quanta Computer Inc.		
PROJECT : AM9A		
Size	Document Number: VCCSA 1-Phase Power Stage	Rev: A
Date: Wednesday, October 14, 2015	Sheet 42 of 61	

+3V (9,10,11,12,13,14,16,17,19,20,21,22,23,24,26,28,29,30,31,32,36,45,49,50,54)
+5V (20,21,22,23,25,30,31,45,49,58)
+3V_S5 (10,12,14,18,24,27,31,32,34,35,37,38,39,49)
+5V_S5 (10,28,29,34,35,36,37,39,40,41,42,44,45,46,47,48,49)

+VIN (19,33,34,35,36,39,40,41,42,46,47,49,58)





NB5

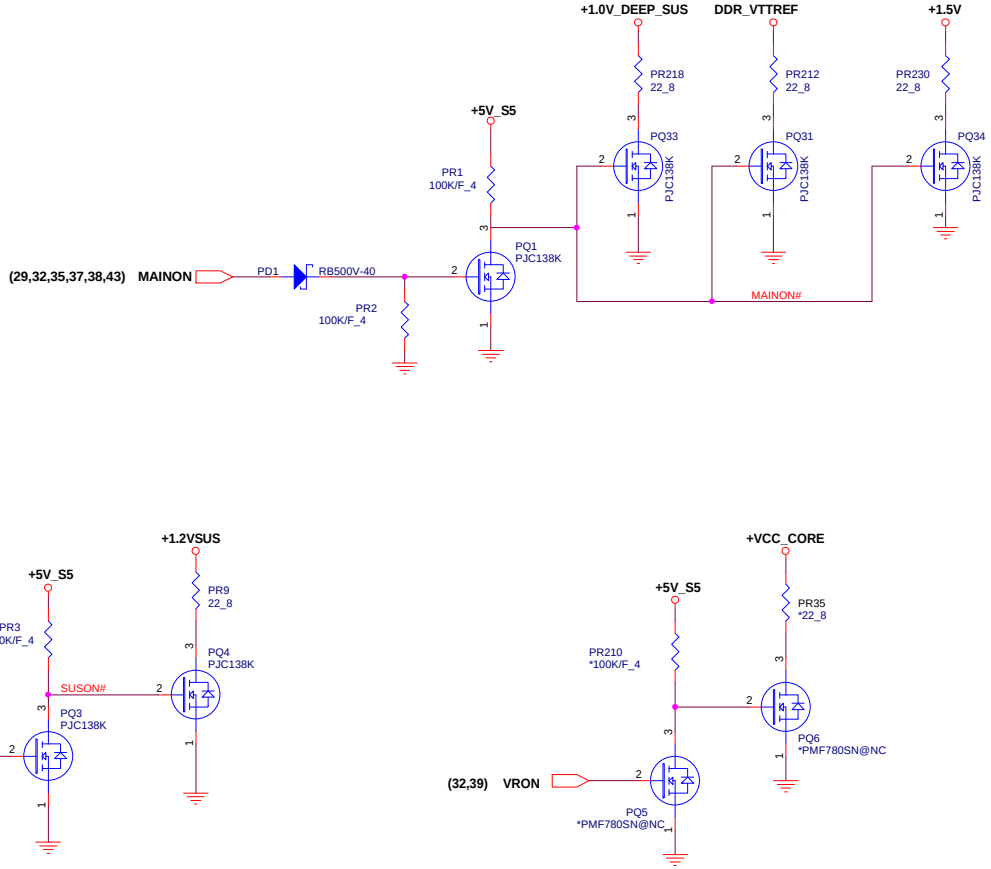
PROJECT : X1B-10L
Quanta Computer Inc.

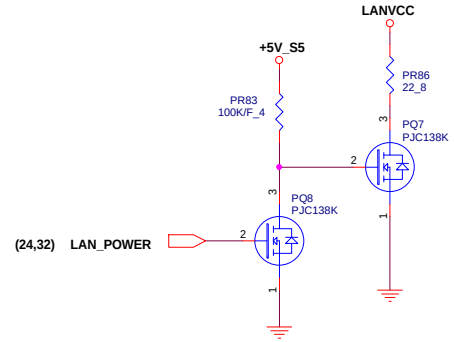
Size	Document Number	Rev
Custom	Dis-charge IC (SLG55448)	1A

Date: Wednesday, October 14, 2015 | Sheet 43 of 61

DISCHARGE

(20,21,22,23,25,30,31,43,45,49,58) +5V
(9,10,11,12,13,14,16,17,19,20,21,22,23,24,26,28,29,30,31,32,36,43,45,49,50,54) +3V
(10,11,14,36,37,39) +1.0V_DEEP_SUS
(16,17,35) DDR_VTTREF
(21,22,38) +1.5V
(2,6,10,16,17,35,47) +1.2VSUS
(10,28,29,34,35,36,37,39,40,41,42,43,45,46,47,48,49) +5V_S5
(7,40) +VCC_CORE
(24) LANVCC





PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge	3B
Date: Wednesday, October 14, 2015	Sheet 44 of 61	

(10,28,29,34,35,36,37,39,40,41,42,43,44,46,47,48,49) +5V_S5
(1,10,11,12,13,14,16,17,19,20,21,22,23,24,26,28,29,30,31,32,36,43,49,50,54) +3V
(46) +VIN_NV
(48,54) +VGACORE

VIN2P (46)
VIN2N (46)

PU17
RT8813AGQW

PR128 1_6 +5V_S5 8813PVCC 21 PVCC
PC148 0.22U/6.3V_4
PR155 1_6 +VIN_VGACORE
PR146 499K/F_4 8813TON 9 TON
PC166 0.22U/25V_6
PR290 10K/F_4 +3V
(46,48) DGPU_VC_EN 16 PGOOD
EC-D-21
(47,54) 3V_MAIN_PWGD
(9,43,47,48) GFXON
PR94 *0_4_S
PR95 *0_4
PR137 10K/F_4
PD10 RB501V-40
PC155 0.22U/6.3V_4 3 EN
(53) DGPU_PSI PR294 *0_4/S 8813PSI 4 PSI
(53) DGPU_PWM_VID PR296 *0_4/S 8813VID 5 VID
8813VREF
PR145 20K/F_4
PR142 20K/F_4
PC165 2700P/50V_4
PC162 0.1U/10V_4 8813VREF 8 VREF
8813REFADJ 6 REFADJ
PR147 2K/F_4
PR302 *0_4/S
PR303 18K/F_4
PR301 *5.1K/F_4
8813REFIN 7 REFIN
PC163 *0.01U/16V_4
PR305 *0_4/P
TP71
PQ21 *2N7002K
PR304 *10K/F_4

UGATE1 2 8813UGATE1 PR136 1_6 8813UGATE1_1
PC151 0.22U/25V_6 1 8813BOOT1 BOOT1
24 8813PHASE1 PHASE1
PQ49 TPCA8064-H
PQ48 TPCA8056-H
PR121 2.2_6
PC139 2200P/50V_4
PR130 16.9K/F_4
POP Ri, Cb and NC Rh for 2phase
23 8813LGAT1 LGATE1
15 8813ISEN1 VCC/ISEN1 PR289 10K/F_4

UGATE2 17 8813UGATE2 8813UGATE2_1 PR135 1_6
PQ52 TPCA8064-H
PC150 0.22U/25V_6 18 8813BOOT2 BOOT2
19 8813PHASE2 PHASE2
PQ51 TPCA8056-H
PR127 2.2_6
PC141 2200P/50V_4
20 8813LGAT2 LGATE2
POP Ra and NC Rb for 2phase
PR293 *30K/F_4 Ra
Rb PR291 10K/F_4
14 8813ISEN2 TALERT/ISEN2 +5V

11 8813VOUT1 VSNS PC160 56P/50V_4 PC301 *100P/50V_4
PR306 *0_4_S PR307 *0_4_S PR308 100/F_4 PR309 100/F_4
+VGACORE
VGPU_CORE_SENSE (50)
VSS_GPU_SENSE (50)
10 8813RGN RGND PC161 56P/50V_4
12 8813SS SS PC159 56P/50V_4

22 8813PWM3 GND/PWM3 PR272 *0_4_S 9610PWM3 5
Rc PR129 0_4 +5V PR266 *0_4_S 9610EN 1
25 GND
13 TSNS/ISEN3
PR102 10_8 +5V_S5 9610VCC 8
PC270 1U/6.3V_4
POP Rc for 2phase
PR299 10K/F_4 Rg
NC Rg for 2phase

PU24
RT9610BZQW
PWM EN VCC GND GND
UGATE 3 9610UGATE3 PR269 1_6 9610UGTE3_1
BOOT 4 9610BOOT3 PC274 0.22U/25V_6 PD14 RB501V-40 +5V_S5
PHASE 2 9610PHASE3
LGATE 7 9610LGATE3
PQ43 TPCA8064-H
PQ45 TPCA8056-H
PR101 *2.2_6
PC113 *2200P/50V_4
3Phase application

+VIN_VGACORE
PC144 4.7U/25V_8 PC292 4.7U/25V_8
PC142 0.1U/25V_4 PC291 2200P/50V_4
PJP18 *SHORTPAD
PR286 *0_2/S PR284 *0_2/S
PC281 100U/25V_105CE_f PC288 100U/25V_105CE_f
PC133 0.1U/25V_4
+VIN_NV
PL19 0.22uH/50A
+VGACORE
PC264 560U/2V/ESR4.5_7343 PC263 560U/2V/ESR4.5_7343

+VIN_VGACORE
PC294 4.7U/25V_8 PC146 4.7U/25V_8
PC145 0.1U/25V_4 PC293 2200P/50V_4
PL21 0.22uH/50A
+VGACORE
PC104 0.1U/10V_4 PC261 560U/2V/ESR4.5_7343

+VIN_VGACORE
PC266 4.7U/25V_8 PC109 4.7U/25V_8
PC265 0.1U/25V_4 PC106 2200P/50V_4
PL18 0.22uH/50A
+VGACORE
PC262 330u_2.5V_7343

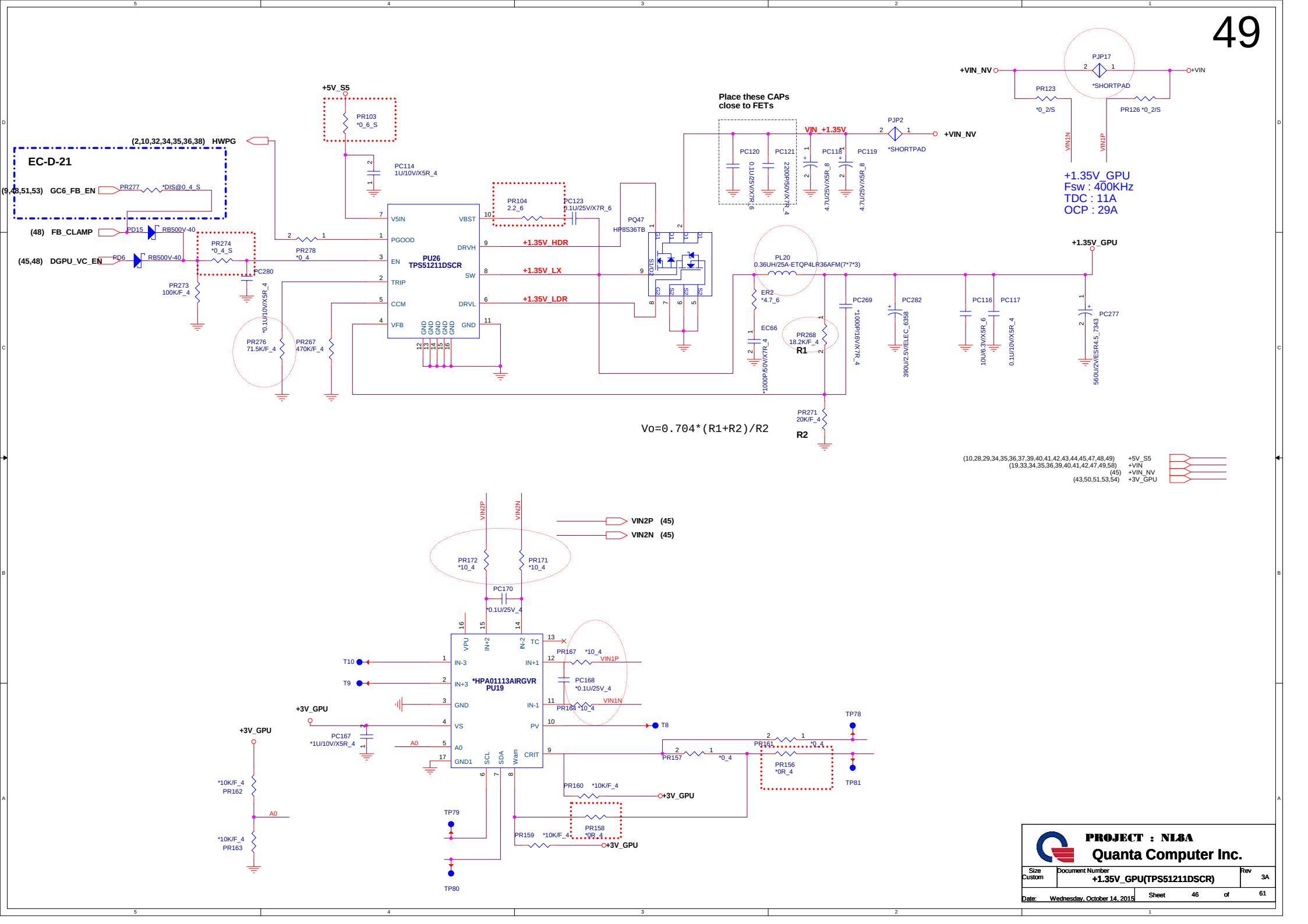
+VGA_CORE
N16E-GT (50W~60W)
Countinue current: 76A
Peak current: 135A
OCP minimum 150A

+VGA_CORE
N16P-GX (35W~50W)
Countinue current: 49A
Peak current: 76A
OCP minimum 90A

+VGA_CORE
N16P-GT (25W~40W)
Countinue current: 49A
Peak current: 76A
OCP minimum 90A

PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE_N15PGX(RT8813A)	3B
Date: Wednesday, October 14, 2015	Sheet 45 of 61	



PROJECT : NL8A		
Quanta Computer Inc.		
Size: Custom	Document Number: +1.35V_GPU(TPS51211DSCR)	Rev: 3A
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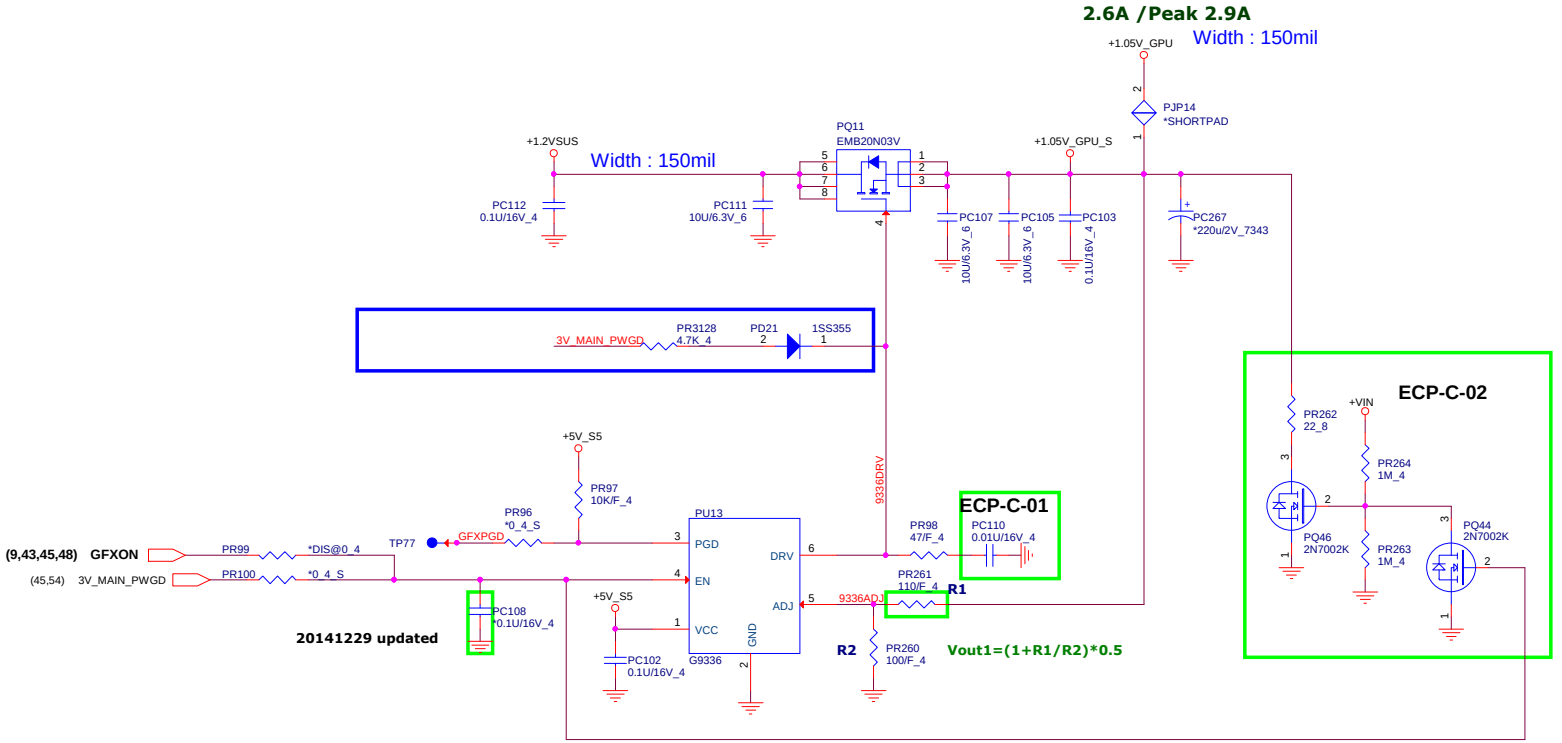
+VIN (19,33,34,35,36,39,40,41,42,46,49,58)
+3V_S5 (10,12,14,18,24,27,31,32,34,35,37,38,39,43,49)
+5V_S5 (10,28,29,34,35,36,37,39,40,41,42,43,44,45,46,48,49)
+3V_GPU (43,46,50,51,53,54)

+1.2VSUS (2,6,10,16,17,35,44)
+1.05V_GPU (48,50,51,52,54)



PROJECT : X1B-10L		
Quanta Computer Inc.		
NB5	Size: Custom	Document Number: 1.05V_VGA/3V_VGA
	Rev: 1A	
Date: Wednesday, October 14, 2015	Sheet 47 of 61	

(43,46,50,51,53,54) +3V_GPU
(45,54) +VGACORE
(47,50,51,52,54) +1.05V_GPU
(46,51,54,55,56) +1.35V_GPU
(50,53,54) +3V_MAIN_GPU

Discrete only

+5V_S5
PR113
DIS@100K/F_4
GFXON#
PQ12
DIS@PJC138K
(9,43,45,47) GFXON
PD9
RB500V-40
PR112
DIS@100K/F_4

+VGACORE
PR110
*DIS@22_8
PQ13
*DIS@PMF780SN

+1.05V_GPU
PR93
DIS@22_8
PQ10
DIS@PJC138K

+3V_MAIN_GPU
PR259
*DIS@22_8
PQ41
*DIS@PJC138K
(54) 3V_MAIN_EN#

EC-D-21
(9,46,51,53) GC6_FB_EN
PR109
*DIS@0_4_S

(46) FB_CLAMP
PD8
RB500V-40

(45,46) DGPU_VC_EN
PD7
RB500V-40

PR281
100K/F_4

PC286
*0.01U/16V_4

+5V_S5
PR107
100K_4
PQ14
DIS@PJC138K

+1.35V_GPU
PR111
DIS@22_8
PQ15
DIS@PJC138K

PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discrete Discharge	3B
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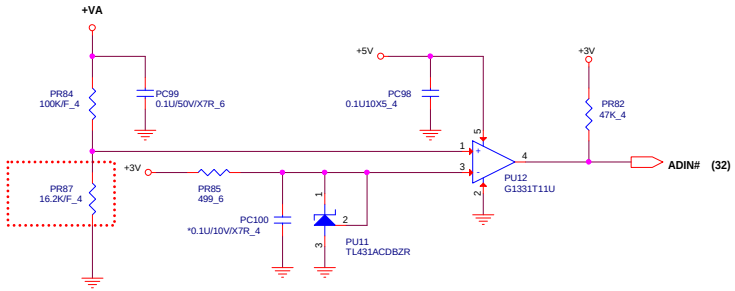
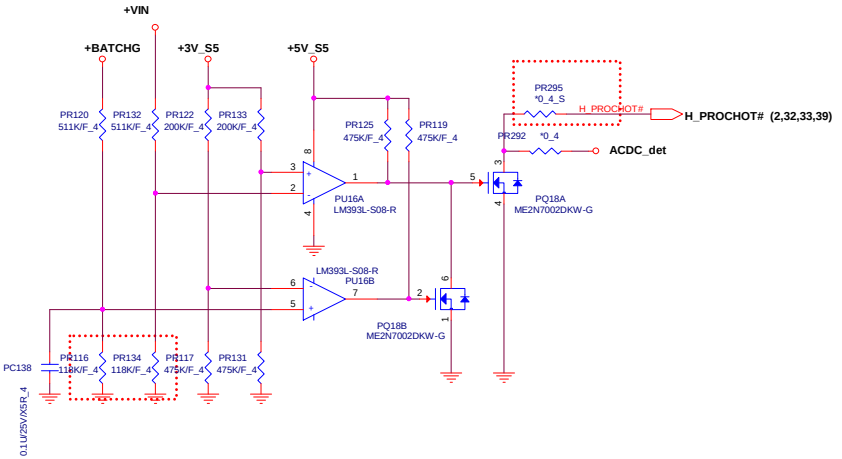
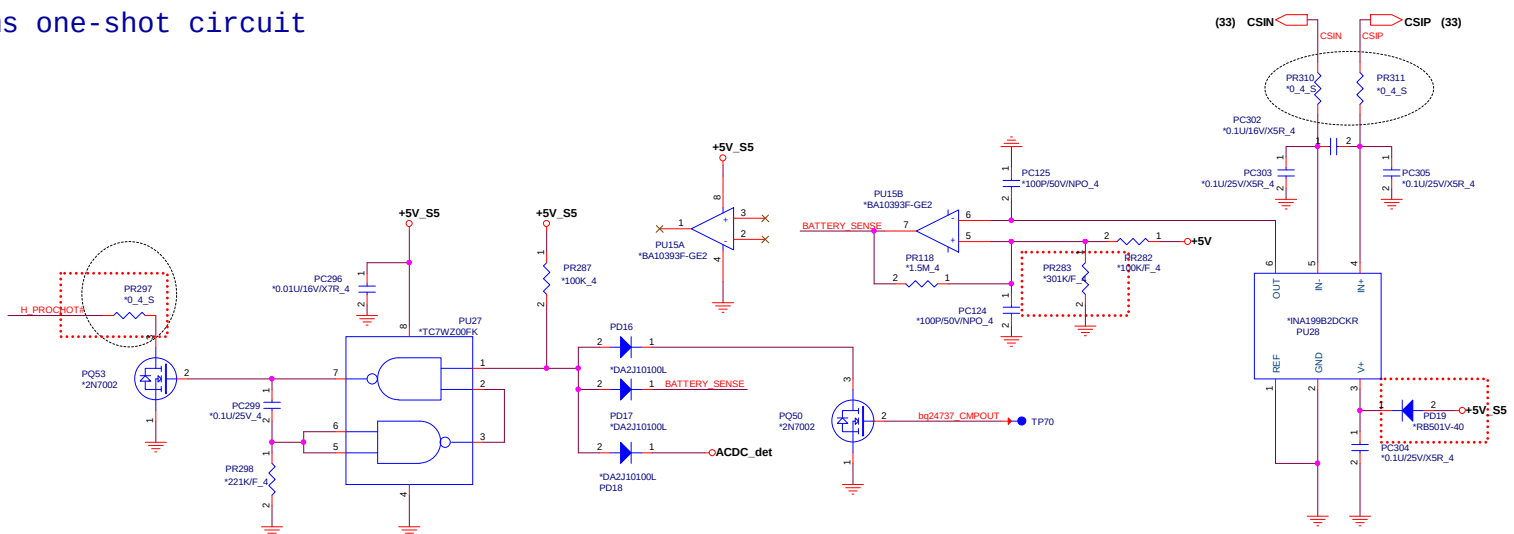




10ms one-shot circuit



PROJECT : NL8A		
Quanta Computer Inc.		
Size: Custom	Document Number: 10ms	Rev: 3B
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(43,46,51,53,54) +3V_GPU
(47,48,51,52,54) +1.05V_GPU
(9,10,11,12,13,14,16,17,19,20,21,22,23,24,26,28,29,30,31,32,36,43,45,49,54) +3V

PEX_IOVDD/Q : 3300mA
+1.05V_GPU
To be placed no further from the GPU than bewteen the PS and GPU
C3067 22U/6.3VS_6
C3205 22U/6.3VS_6
C3209 22U/6.3VS_6
C3201 22U/6.3VS_6
C3116 10U/6.3VS_6
C3107 10U/6.3VS_6
C3208 10U/6.3VS_6
C3207 10U/6.3VS_6
PLACE UNDER BGA
C3059 1U/6.3V_4
C3203 1U/6.3V_4
C3202 1U/6.3V_4
C3086 1U/6.3V_4
PLACE NEAR BALLS
C3072 4.7U/6.3V_6
C3093 4.7U/6.3V_6

U3002A
[PEG Interface]

AG19 PEX_IOVDD_1
AG21 PEX_IOVDD_2
AG22 PEX_IOVDD_3
AG24 PEX_IOVDD_4
AH21 PEX_IOVDD_5
AH25 PEX_IOVDD_6
AG13 PEX_IOVDDQ_1
AG15 PEX_IOVDDQ_2
AG16 PEX_IOVDDQ_3
AG18 PEX_IOVDDQ_4
AG25 PEX_IOVDDQ_5
AH15 PEX_IOVDDQ_6
AH18 PEX_IOVDDQ_7
AH26 PEX_IOVDDQ_8
AH27 PEX_IOVDDQ_9
AJ27 PEX_IOVDDQ_10
AK27 PEX_IOVDDQ_11
L27 PEX_IOVDDQ_12
AM28 PEX_IOVDDQ_13
AN28 PEX_IOVDDQ_14

PEX_RX0 AN12 PEG_TX0 (3)
PEX_RX0_N AM12 PEG_TX#0 (3)
PEX_RX1 AN14 PEG_TX1 (3)
PEX_RX1_N AM14 PEG_TX#1 (3)
PEX_RX2 AP14 PEG_TX2 (3)
PEX_RX2_N AP15 PEG_TX#2 (3)
PEX_RX3 AN15 PEG_TX3 (3)
PEX_RX3_N AM15 PEG_TX#3 (3)
PEX_RX4 AN17 PEG_TX4 (3)
PEX_RX4_N AM17 PEG_TX#4 (3)
PEX_RX5 AP17 PEG_TX5 (3)
PEX_RX5_N AP18 PEG_TX#5 (3)
PEX_RX6 AN18 PEG_TX6 (3)
PEX_RX6_N AM18 PEG_TX#6 (3)
PEX_RX7 AN20 PEG_TX7 (3)
PEX_RX7_N AM20 PEG_TX#7 (3)
PEX_RX8 AP20 PEG_TX8 (3)
PEX_RX8_N AP21 PEG_TX#8 (3)
PEX_RX9 AN21 PEG_TX9 (3)
PEX_RX9_N AM21 PEG_TX#9 (3)
PEX_RX10 AN23 PEG_TX10 (3)
PEX_RX10_N AM23 PEG_TX#10 (3)
PEX_RX11 AP23 PEG_TX11 (3)
PEX_RX11_N AP24 PEG_TX#11 (3)
PEX_RX12 AN24 PEG_TX12 (3)
PEX_RX12_N AM24 PEG_TX#12 (3)
PEX_RX13 AN26 PEG_TX13 (3)
PEX_RX13_N AM26 PEG_TX#13 (3)
PEX_RX14 AP26 PEG_TX14 (3)
PEX_RX14_N AP27 PEG_TX#14 (3) (2,12,20,24,27,29,30,32) PLTRST#
PEX_RX15 AN27 PEG_TX15 (3)
PEX_RX15_N AM27 PEG_TX#15 (3)

PEX_TX0 AK14 C_PEG_RX0 C3146 0.22U/10V_4 PEG_RX0 (3)
PEX_TX0_N AJ14 C_PEG_RX#0 C3147 0.22U/10V_4 PEG_RX#0 (3)
PEX_TX1 AH14 C_PEG_RX1 C3148 0.22U/10V_4 PEG_RX1 (3)
PEX_TX1_N AG14 C_PEG_RX#1 C3149 0.22U/10V_4 PEG_RX#1 (3)
PEX_TX2 AK15 C_PEG_RX2 C3135 0.22U/10V_4 PEG_RX2 (3)
PEX_TX2_N AJ15 C_PEG_RX#2 C3145 0.22U/10V_4 PEG_RX#2 (3)
PEX_TX3 AL16 C_PEG_RX3 C3130 0.22U/10V_4 PEG_RX3 (3)
PEX_TX3_N AK16 C_PEG_RX#3 C3134 0.22U/10V_4 PEG_RX#3 (3)
PEX_TX4 AK17 C_PEG_RX4 C3126 0.22U/10V_4 PEG_RX4 (3)
PEX_TX4_N AJ17 C_PEG_RX#4 C3120 0.22U/10V_4 PEG_RX#4 (3)
PEX_TX5 AH17 C_PEG_RX5 C3112 0.22U/10V_4 PEG_RX5 (3)
PEX_TX5_N AG17 C_PEG_RX#5 C3118 0.22U/10V_4 PEG_RX#5 (3)
PEX_TX6 AK18 C_PEG_RX6 C3110 0.22U/10V_4 PEG_RX6 (3)
PEX_TX6_N AJ18 C_PEG_RX#6 C3105 0.22U/10V_4 PEG_RX#6 (3)
PEX_TX7 AL19 C_PEG_RX7 C3103 0.22U/10V_4 PEG_RX7 (3)
PEX_TX7_N AK19 C_PEG_RX#7 C3089 0.22U/10V_4 PEG_RX#7 (3)
PEX_TX8 AK20 C_PEG_RX8 C3087 0.22U/10V_4 PEG_RX8 (3)
PEX_TX8_N AJ20 C_PEG_RX#8 C3074 0.22U/10V_4 PEG_RX#8 (3)
PEX_TX9 AH20 C_PEG_RX9 C3073 0.22U/10V_4 PEG_RX9 (3)
PEX_TX9_N AG20 C_PEG_RX#9 C3068 0.22U/10V_4 PEG_RX#9 (3)
PEX_TX10 AK21 C_PEG_RX10 C3060 0.22U/10V_4 PEG_RX10 (3)
PEX_TX10_N AJ21 C_PEG_RX#10 C3066 0.22U/10V_4 PEG_RX#10 (3)
PEX_TX11 AL22 C_PEG_RX11 C3057 0.22U/10V_4 PEG_RX11 (3)
PEX_TX11_N AK22 C_PEG_RX#11 C3056 0.22U/10V_4 PEG_RX#11 (3)
PEX_TX12 AK23 C_PEG_RX12 C3055 0.22U/10V_4 PEG_RX12 (3)
PEX_TX12_N AJ23 C_PEG_RX#12 C3046 0.22U/10V_4 PEG_RX#12 (3)
PEX_TX13 AH23 C_PEG_RX13 C3044 0.22U/10V_4 PEG_RX13 (3)
PEX_TX13_N AG23 C_PEG_RX#13 C3041 0.22U/10V_4 PEG_RX#13 (3)
PEX_TX14 AK24 C_PEG_RX14 C3040 0.22U/10V_4 PEG_RX14 (3)
PEX_TX14_N AJ24 C_PEG_RX#14 C3039 0.22U/10V_4 PEG_RX#14 (3)
PEX_TX15 AL25 C_PEG_RX15 C3038 0.22U/10V_4 PEG_RX15 (3)
PEX_TX15_N AK25 C_PEG_RX#15 C3037 0.22U/10V_4 PEG_RX#15 (3)

AC6 NC_1
AJ28 NC_2
AJ4 NC_3
AJ5 NC_4
AL11 NC_5
C15 NC_6
D19 NC_7
D20 NC_8
D23 NC_9
D26 NC_10
H31 NC_11
T8 NC_12
V32 NC_13

PLACE UNDER GPU
C3139 0.1U/10V_4
PLACE NEAR GPU
C3142 1U/6.3V_4
C3144 4.7U/6.3V_6

VDD33 : 85mA
+3V_GPU J8 VDD3V3_1
K8 VDD3V3_2
+3V_MAIN_GPU L8 VDD33_1
M8 VDD33_2

PLACE NEAR GPU
C3128 4.7U/6.3V_6
C3141 1U/6.3V_4
PLACE UNDER GPU
C3129 0.1U/10V_4
C3140 0.1U/10V_4

PEX_REFCLK AL13 CLK_VGA_P (11)
PEX_REFCLK_N AK13 CLK_VGA_N (11)

PEX_TSTCLK_OUT AJ26 PEX_TSTCLK R3077 *200_4
PEX_TSTCLK_OUT_N AK26 PEX_TSTCLK#

PEX_WAKE(NC) AJ11
PEX_RST_N AJ12 PEGX_RST#

PEX_CLKREQ_N AK12 PEX_CLKREQ# R3078 10K_4 +3V_GPU
PEX_TERMP AP29 PEX_TERMP R3076 2.49K/F_4
TESTMODE AK11 TESTMODE R3079 10K_4

+1.05V_GPU
R3075 *0_6
L3003 BLM15PX330SN1D(33,3000MA)
EC-C-02

PEX_PLLVDD AG26 PEX_PLLVDD PEX_PLLVDD : 150mA
C3197 4.7U/6.3V_6 PLACE NEAR BGA CLOSE TO CAPS
C3051 1U/6.3V_4 PLACE UNDER BGA
C3042 0.1U/10V_4 PLACE NEAR BALLS

PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12
PEX_SVDD_3V3 : 210mA
0.1U/10V_4 C3123
4.7U/6.3V_6 C3119
4.7U/6.3V_6 C3157
PLACE NEAR BGA
+3V_GPU

3.3V_AUX_NC P8

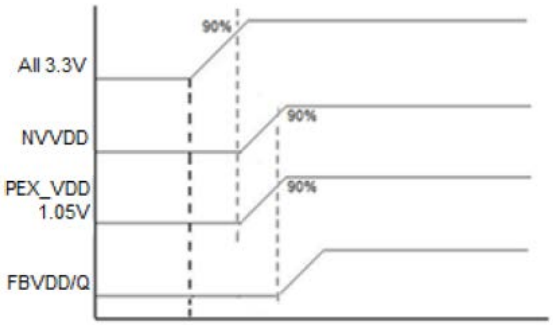
VDD_SENSE L4 VGPU_CORE_SENSE (45)
GND_SENSE L5 VSS_GPU_SENSE (45)

N15P_0

DGPU_PWROK (9,32,54)
PEX_CLKREQ# 1 2 3 PCIE_CLKREQ_VGA# (11)
Q3006
2N7002

+3V
C3171 0.1U/10V_4
(9) DGPU_HOLD_RST#
SYS_PEX_RST_MON#
SYS_PEX_RST_MON# (53)
U3001
TC7SH08FU

+3V
C3172 0.1U/10V_4
SYS_PEX_RST_MON#
(53) GPU_PEX_RST_HOLD#
PEGX_RST#
PEGX_RST# (53)
U3000
TC7SH08FU
R3054 100K_4



PROJECT : NL9
Quanta Computer Inc.

Size	Document Number	Rev
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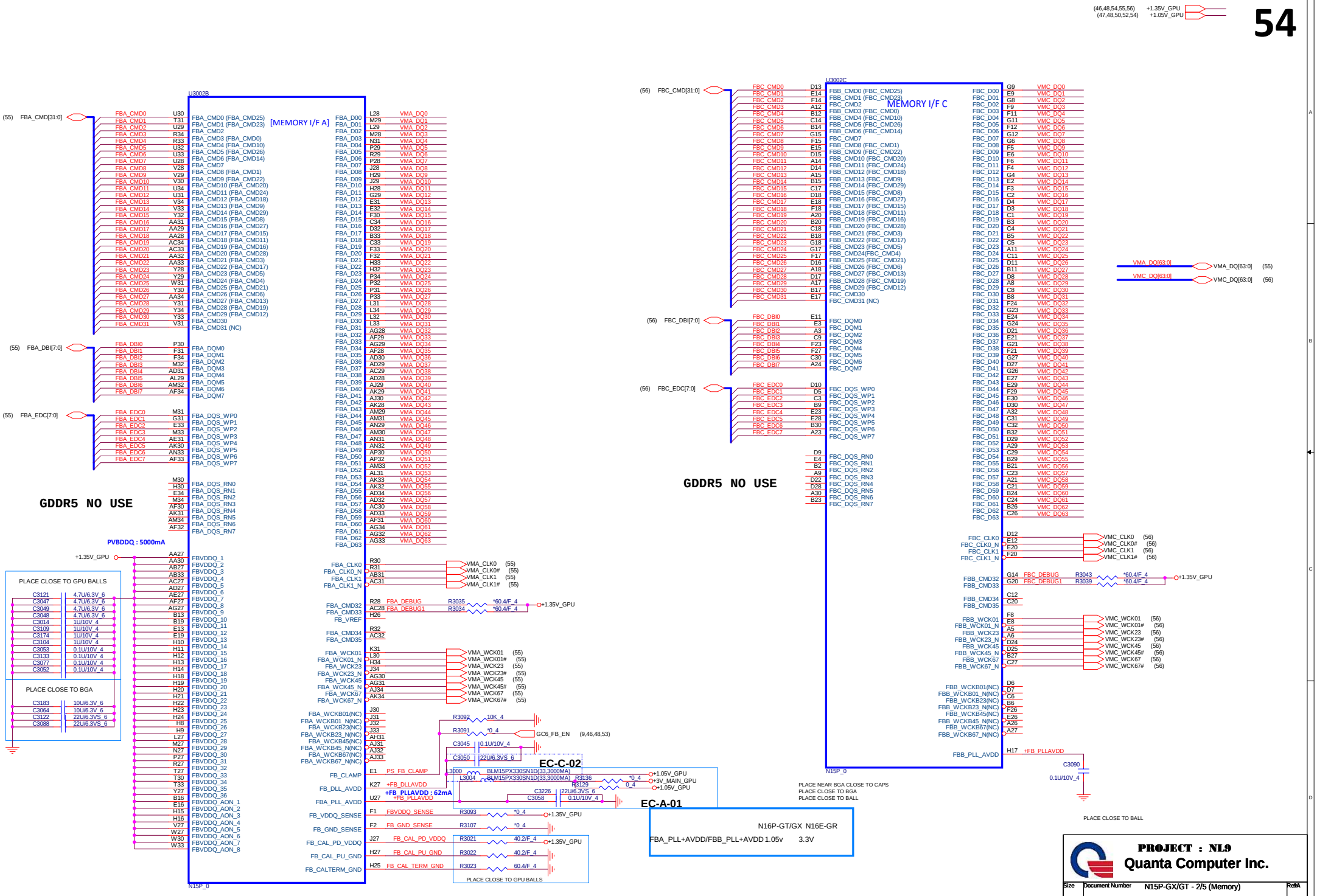
(46,48,54,55,56) +1.35V_GPU
(47,48,50,52,54) +1.05V_GPU
U3002B
[MEMORY I/F A]
GDDR5 NO USE
PVBDDQ : 5000mA
+1.35V_GPU
PLACE CLOSE TO GPU BALLS
PLACE CLOSE TO BGA
N15P_0
U3002C
MEMORY I/F C
GDDR5 NO USE
N15P_0
PLACE NEAR BGA CLOSE TO CAPS
PLACE CLOSE TO BGA
PLACE CLOSE TO BALL
EC-C-02
EC-A-01
+FB_PLLAVDD : 62mA
PLACE CLOSE TO GPU BALLS
PLACE CLOSE TO BALL
N16P-GT/GX N16E-GR
FBA_PLL+AVDD/FBB_PLL+AVDD 1.05v 3.3V
PROJECT : NL9
Quanta Computer Inc.
Size
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N15P-GX/GT - 2/5 (Memory)
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(47,48,50,51,54) +1.05V_GPU

U3002D

[IFPA/B_LVDS]
AH8 IFPAB_PLLVDD
AG8 IFPA_IOVDD
AG9 IFPB_IOVDD
AJ8 IFPAB_RSET
IFPA_TXC AM6
IFPA_TXC_N AN6
IFPA_TXD0 AP3
IFPA_TXD0_N AN3
IFPA_TXD1 AN5
IFPA_TXD1_N AM5
IFPA_TXD2 AL6
IFPA_TXD2_N AK6
IFPA_TXD3 AJ6
IFPA_TXD3_N AH6
IFPB_TXC AJ9
IFPB_TXC_N AH9
IFPB_TXD4 AP6
IFPB_TXD4_N AP5
IFPB_TXD5 AM7
IFPB_TXD5_N AL7
IFPB_TXD6 AN8
IFPB_TXD6_N AM8
IFPB_TXD7 AK8
IFPB_TXD7_N AL8

[IFPC/D_TMDS]
AF7 IFPC_PLLVDD
AG7 IFPD_PLLVDD
AF6 IFPC_IOVDD
AG6 IFPD_IOVDD
AF8 IFPC_RSET
AN2 IFPD_RSET(NC)
IFPC_AUX_I2CW_SCL AG3
IFPC_AUX_I2CW_SDA_N AG2
IFPC_L0 AK1
IFPC_L0_N AJ1
IFPC_L1 AJ3
IFPC_L1_N AJ2
IFPC_L2 AH3
IFPC_L2_N AH4
IFPC_L3 AG5
IFPC_L3_N AG4
IFPD_AUX_I2CX_SCL AK3
IFPD_AUX_I2CX_SDA_N AK2
IFPD_L0 AM1
IFPD_L0_N AM2
IFPD_L1 AM3
IFPD_L1_N AM4
IFPD_L2 AL3
IFPD_L2_N AL4
IFPD_L3 AK4
IFPD_L3_N AK5

[IFPE/F_DP]
AB8 IFPEF_PLLVDD
AC7 IFPE_IOVDD
AC8 IFPF_IOVDD
AD6 IFPEF_RSET
IFPE_AUX_I2CY_SCL AB3
IFPE_AUX_I2CY_SDA_N AB4
IFPE_L0 AD2
IFPE_L0_N AD3
IFPE_L1 AD1
IFPE_L1_N AC1
IFPE_L2 AC2
IFPE_L2_N AC3
IFPE_L3 AC4
IFPE_L3_N AC5
IFPF_AUX_I2CZ_SCL AF3
IFPF_AUX_I2CZ_SDA_N AF2
IFPF_L0 AE3
IFPF_L0_N AE4
IFPF_L1 AF4
IFPF_L1_N AF5
IFPF_L2 AD4
IFPF_L2_N AD5
IFPF_L3 AG1
IFPF_L3_N AF1

[DACA/B_CRT]
AG10 DACA_VDD
AP9 DACA_VREF
AP8 DACA_RSET
DACA_RED AK9
DACA_GREEN AL10
DACA_BLUE AL9
DACA_HSYNC AM9
DACA_VSYNC AN9
I2CA_SCL
I2CA_SDA

R4 I2CA_SCL R3111 2.2K_4
R5 I2CA_SDA R3055 2.2K_4

PLLVDD : 200mA

+1.05V_GPU L3001 BLM15PX330SN1D(33.3000MA) NV_PLLVDD AD8 PLLVDD
R3049 *0_4
C3152 22U/6.3VS_6
C3138 0.1U/10V_4
SP_PLLVDD AE8 SP_PLLVDD
EC-C-02
+1.05V_GPU L3002 BLM15PX330SN1D(33.3000MA) VID_PLLVDD AD7 VID_PLLVDD
C3151 22U/6.3VS_6
C3153 4.7U/6.3V_6
C3137 0.1U/10V_4
C3136 0.1U/10V_4
PLACE CLOSE TO GPU
PLACE CLOSE TO BALLS
N15P_0

[XTAL IN]
XTAL_IN
XTAL_OUT
XTAL_OUTBUFF
XTAL_SSIN
H3 VGA_XTALIN
H2 VGA_XTALOUT
J4 R3057 10K_4
H1 R3094 10K_4
Y3000
27MHZ +-10PPM
C3163 10P/50V_4
C3164 10P/50V_4

PROJECT : NL9
Quanta Computer Inc.

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4.99K/F_4: CS24992FB26 RES CHIP 4.99K 1/16W +1%(0402)
10K/F_4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)
15K/F_4: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)
24.9K/F_4: CS32492FB16 RES CHIP 24.9K 1/16W +-1%(0402)
30.1K/F_4: CS33012FB18 RES CHIP 30.1K 1/16W +-1%(0402)
34.8K/F_4: CS33482FB22 RES CHIP 34.8K 1/16W +-1% (0402)
45.3K/F_4: CS34532FB18 RES CHIP 45.3K 1/16W +-1% (0402)

Logical Strap Bit Mapping

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Table 9. N14P-GV/GT/GS/LP/GE GDDR5 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed WCK (MHz)	Memory Date Code Minimum	Status
128Mx16 GDDR5	Hynix	0x4	1.5 V/ 1.5 V	H5GQ2H24AFR-T2C	2500	N/A	Production Candidate
		0x6	1.35V/ 1.35V	H5GQ2H24AFR-T2C	2000	N/A	Production Candidate
	Samsung	0x5	1.5 V/ 1.5 V	K4G20325FD-FC04	2500	1219	Production Candidate
		0x7	1.35V/ 1.35V	K4G20325FD-FC04	2000	1219	Production Candidate

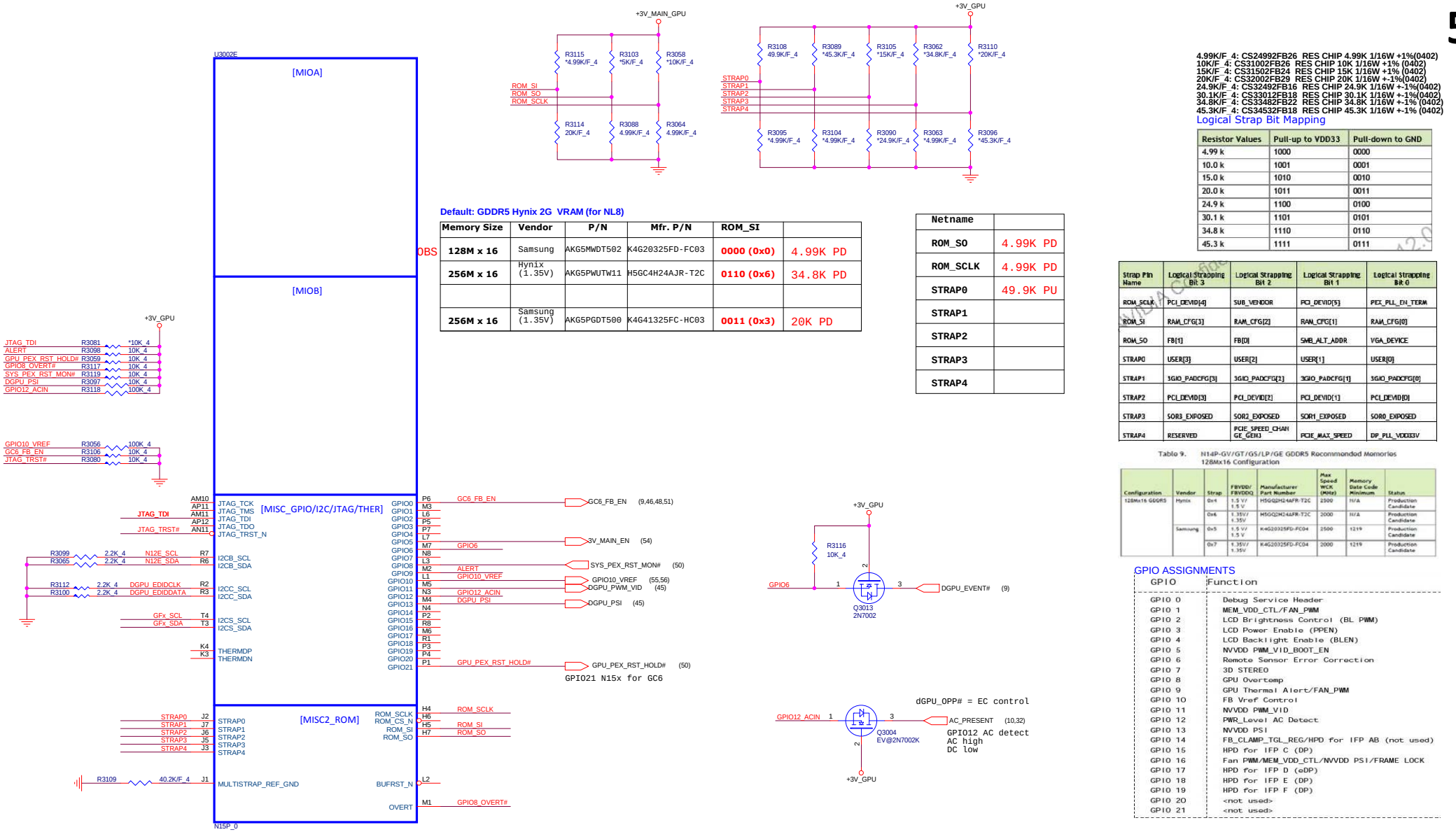
Default: GDDR5 Hynix 2G VRAM (for NL8)

Memory Size	Vendor	P/N	Mfr. P/N	ROM_SI	
128M x 16	Samsung	AKG5MWDT502	K4G20325FD-FC03	0000 (0x0)	4.99K PD
256M x 16	Hynix (1.35V)	AKG5PWUTW11	H5GC4H24AJR-T2C	0110 (0x6)	34.8K PD
256M x 16	Samsung (1.35V)	AKG5PGDT500	K4G41325FC-HC03	0011 (0x3)	20K PD

Netname	
ROM_SO	4.99K PD
ROM_SCLK	4.99K PD
STRAP0	49.9K PU
STRAP1	
STRAP2	
STRAP3	
STRAP4	

GPIO ASSIGNMENTS

GPIO	Function
GPIO 0	Debug Service Header
GPIO 1	MEM_VDD_CTL/FAN_PWM
GPIO 2	LCD Brightness Control (BL PWM)
GPIO 3	LCD Power Enable (PPEN)
GPIO 4	LCD Backlight Enable (BLEN)
GPIO 5	NVVDD PWM_VID_BOOT_EN
GPIO 6	Remote Sensor Error Correction
GPIO 7	3D STEREO
GPIO 8	GPU Overtemp
GPIO 9	GPU Thermal Alert/FAN_PWM
GPIO 10	FB Vref Control
GPIO 11	NVVDD PWM_VID
GPIO 12	PWR_Level AC Detect
GPIO 13	NVVDD PSI
GPIO 14	FB_CLAMP_TGL_REG/HPD for IFP AB (not used)
GPIO 15	HPD for IFP C (DP)
GPIO 16	Fan PWM/MEM_VDD_CTL/NVVDD PSI/FRAME LOCK
GPIO 17	HPD for IFP D (eDP)
GPIO 18	HPD for IFP E (DP)
GPIO 19	HPD for IFP F (DP)
GPIO 20	<not used>
GPIO 21	<not used>



PROJECT : NL9
Quanta Computer Inc.

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VDD/XVDD : 25.72A

+VGACORE

U3002F [GPU VDD] N15P_0

AA12	VDD_001	XVDD_001	U1
AA14	VDD_002	XVDD_002	U2
AA16	VDD_003	XVDD_003	U3
AA19	VDD_004	XVDD_004	U4
AA21	VDD_005	XVDD_005	U5
AA23	VDD_006	XVDD_006	U6
AB13	VDD_007	XVDD_007	U7
AB15	VDD_008	XVDD_008	U8
AB17	VDD_009	XVDD_009	V1
AB18	VDD_010	XVDD_010	V2
AB20	VDD_011	XVDD_011	V3
AB22	VDD_012	XVDD_012	V4
AC12	VDD_013	XVDD_013	V5
AC14	VDD_014	XVDD_014	V6
AC16	VDD_015	XVDD_015	V7
AC19	VDD_016	XVDD_016	V8
AC21	VDD_017	XVDD_017	W2
AC23	VDD_018	XVDD_018	W3
M12	VDD_019	XVDD_019	W4
M14	VDD_020	XVDD_020	W5
M16	VDD_021	XVDD_021	W7
M19	VDD_022	XVDD_022	W8
M21	VDD_023	XVDD_023(NC)	Y1
M23	VDD_024	XVDD_024(NC)	Y2
N13	VDD_025	XVDD_025(NC)	Y3
N15	VDD_026	XVDD_026	Y4
N17	VDD_027	XVDD_027	Y5
N18	VDD_028	XVDD_028	Y6
N20	VDD_029	XVDD_029	Y7
N22	VDD_030	XVDD_030	Y8
P12	VDD_031	XVDD_031(NC)	AA1
P14	VDD_032	XVDD_032(NC)	AA2
P16	VDD_033	XVDD_033(NC)	AA3
P19	VDD_034	XVDD_034(NC)	AA4
P21	VDD_035	XVDD_035(NC)	AA5
P23	VDD_036	XVDD_036(NC)	AA6
R13	VDD_037	XVDD_037(NC)	AA7
R15	VDD_038	XVDD_038(NC)	AA8
R17	VDD_039		
R18	VDD_040		
R20	VDD_041		
R22	VDD_042		
T12	VDD_043		
T14	VDD_044		
T16	VDD_045		
T19	VDD_046		
T21	VDD_047		
T23	VDD_048		
U13	VDD_049		
U15	VDD_050		
U17	VDD_051		
U18	VDD_052		
U20	VDD_053		
U22	VDD_054		
V13	VDD_055		
V15	VDD_056		
V17	VDD_057		
V18	VDD_058		
V20	VDD_059		
V22	VDD_060		
W12	VDD_061		
W14	VDD_062		
W16	VDD_063		
W19	VDD_064		
W21	VDD_065		
W23	VDD_066		
Y13	VDD_067		
Y15	VDD_068		
Y18	VDD_069		
Y17	VDD_070		
Y20	VDD_071		
Y22	VDD_072		

+VGACORE

U3002G [GPU GND] N15P_0

A2	GND_1	GND_101	D2
AA17	GND_2	GND_102	D31
AA18	GND_3	GND_103	D33
AA20	GND_4	GND_104	E10
AA22	GND_5	GND_105	E22
AB12	GND_6	GND_106	E25
AB14	GND_7	GND_107	E5
AB16	GND_8	GND_108	E7
AB19	GND_9	GND_109	F28
AB2	GND_10	GND_110	F7
AB21	GND_11	GND_111	G10
A33	GND_12	GND_112	G13
AB23	GND_13	GND_113	G16
AB28	GND_14	GND_114	G19
AB30	GND_15	GND_115	G2
AB32	GND_16	GND_116	G22
AB5	GND_17	GND_117	G25
AB7	GND_18	GND_118	G28
AC13	GND_19	GND_119	G3
AC15	GND_20	GND_120	G30
AC17	GND_21	GND_121	G32
AC18	GND_22	GND_122	G33
AA13	GND_23	GND_123	G5
AC20	GND_24	GND_124	G7
AC22	GND_25	GND_125	K2
AE2	GND_26	GND_126	K28
AE28	GND_27	GND_127	K30
AE30	GND_28	GND_128	K32
AE32	GND_29	GND_129	K33
AE33	GND_30	GND_130	K5
AE5	GND_31	GND_131	K7
AE7	GND_32	GND_132	M13
AH10	GND_33	GND_133	M15
AA15	GND_34	GND_134	M17
AH13	GND_35	GND_135	M18
AH16	GND_36	GND_136	M20
AH19	GND_37	GND_137	M22
AH2	GND_38	GND_138	N12
AH22	GND_39	GND_139	N14
AH24	GND_40	GND_140	N16
AH28	GND_41	GND_141	N19
AH29	GND_42	GND_142	N2
AH30	GND_43	GND_143	N21
AH32	GND_44	GND_144	N23
AH33	GND_45	GND_145	N28
AH5	GND_46	GND_146	N30
AH7	GND_47	GND_147	N32
AJ7	GND_48	GND_148	N33
AK10	GND_49	GND_149	N5
AK7	GND_50	GND_150	N7
AL12	GND_51	GND_151	P13
AL14	GND_52	GND_152	P15
AL15	GND_53	GND_153	P17
AL17	GND_54	GND_154	P18
AL18	GND_55	GND_155	P20
AL2	GND_56	GND_156	P22
AL20	GND_57	GND_157	R12
AL21	GND_58	GND_158	R14
AL23	GND_59	GND_159	R16
AL24	GND_60	GND_160	R19
AL26	GND_61	GND_161	P21
AL28	GND_62	GND_162	R23
AL30	GND_63	GND_163	T13
AL32	GND_64	GND_164	T15
AL33	GND_65	GND_165	T17
AL5	GND_66	GND_166	T18
AM13	GND_67	GND_167	T2
AM16	GND_68	GND_168	T20
AM19	GND_69	GND_169	T22
AM22	GND_70	GND_170	AG11
AM25	GND_71	GND_171	T28
AN1	GND_72	GND_172	T32
AN10	GND_73	GND_173	T5
AN13	GND_74	GND_174	T7
AN16	GND_75	GND_175	U12
AN19	GND_76	GND_176	U14
AN22	GND_77	GND_177	U16
AN25	GND_78	GND_178	U19
AN30	GND_79	GND_179	U21
AN34	GND_80	GND_180	U23
AN4	GND_81	GND_181	V12
AN7	GND_82	GND_182	V14
AP2	GND_83	GND_183	V16
AP33	GND_84	GND_184	V19
B1	GND_85	GND_185	V21
B10	GND_86	GND_186	V23
B22	GND_87	GND_187	W13
B25	GND_88	GND_188	W15
B28	GND_89	GND_189	W17
B31	GND_90	GND_190	W18
B34	GND_91	GND_191	W20
B4	GND_92	GND_192	W22
B7	GND_93	GND_193	W28
C10	GND_94	GND_194	Y12
C13	GND_95	GND_195	Y14
C19	GND_96	GND_196	Y16
C22	GND_97	GND_197	Y19
C25	GND_98	GND_198	Y21
C28	GND_99	GND_199	Y23
C7	GND_100	GND_200	AH11
			C16
		GND_OPT_1	
			W32
		GND_OPT_2	

+VGACORE

PLACE UNDER GPU

C3117	1U/6.3V_4
C3131	1U/6.3V_4
C3127	1U/6.3V_4
C3111	1U/6.3V_4
C3075	1U/6.3V_4
C3108	0.1U/10V_4
C3115	0.1U/10V_4
C3094	0.1U/10V_4
C3078	0.1U/10V_4
C3132	4.7U/6.3V_6
C3143	4.7U/6.3V_6
C3069	4.7U/6.3V_6
C3159	4.7U/6.3V_6
C3065	4.7U/6.3V_6
C3155	4.7U/6.3V_6
C3063	4.7U/6.3V_6
C3076	4.7U/6.3V_6
C3156	4.7U/6.3V_6
C3062	4.7U/6.3V_6
C3061	4.7U/6.3V_6
C3158	4.7U/6.3V_6
C3070	4.7U/6.3V_6
C3216	4.7U/6.3V_6
C3125	4.7U/6.3V_6

PLACE NEAR GPU

C3162	4.7U/10V_6
C3102	4.7U/10V_6
C3101	4.7U/10V_6
C3161	4.7U/10V_6
C3214	4.7U/10V_6
C3217	22U/6.3VS_6
C3215	22U/6.3V_6_S

C3114	100U/6.3V_1206

PLACE TO GPU CENTER

(45,48) +VGACORE
(47,48,50,51,52) +1.05V_GPU
(46,48,51,55,56) +1.35V_GPU
(43,46,50,51,53) +3V_GPU
(9,10,11,12,13,14,16,17,19,20,21,22,23,24,26,28,29,30,31,32,36,43,45,49,50) +3V

for meet Power down sequence for +3V_GFX

+VGACORE — D3000 — RB500V-40 — +3V_GPU
+1.35V_GPU — D3001 — *RB500V-40

3V MAIN POWER

ECP-C-02

+3V_GPU — R3087 10K_4 — R3086 0_4_S — Q3011 AO3413 — +3V_MAIN_GPU
R3113 10K_4 — (48) 3V_MAIN_EN# — Q3010 2N7002K
(53) 3V_MAIN_EN
C3212 0.022U/25V_4
C3213 0.022U/25V_4

+3V_GPU — R3123 4.7K_4 — 3V_MAIN_PWGD — 3V_MAIN_PWGD (45,47)
+3V — R3125 4.7K_4 — C3224 1000P/16V/X7R_4
R3122 100K/F_4
+3V_MAIN_GPU — R3124 4.7K_4 — C3225 *1000p/50V_4 — Q3014 METR3904-G
Q3015 DDTC144EUA

+1.05V_GFX and GPU core power EN

+3V_GPU — R3082 4.7K_4 — DGPU_PWROK (9,32,50)
+3V — R3085 4.7K_4 — Q3007 — R3083 *100K/F_4
DGPU_PGOOK-1
+1.05V_GPU — R3084 4.7K_4 — DGPU_POK4 — Q3008 MMBT3904-7-F — C3206 1000P/16V/X7R_4
C3210 1000P/16V/X7R_4
LTC044EUBFSTL
+1.35V_GPU — R3101 4.7K_4 — DGPU_POK2 — Q3009 MMBT3904-7-F — C3218 1000P/16V/X7R_4

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Quanta Computer Inc.

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CHANNEL A: 2G/4G GDDR5

(51) VMA_DQ[63..0] — VMA_DQ[63..0]
(51) FBA_CMD[31:0]
(51) FBA_DBI[7..0] — FBA_DBI[7..0]
(51) FBA_EDC[7..0] — FBA_EDC[7..0]

Channel 0 <0-31>
MF=0 Non-mirrored

QD16~23 / QD0~7

VRAM3004 — GDDR5

Channel 0 <32-63>
MF=1 Mirrored

QD8~15 / QD24~31

VRAM3000 — GDDR5

Channel 1 <0-31>
MF=0 Non-mirrored

QD48~55 / QD32~39

VRAM3001 — GDDR5

Channel 1 <32-63>
MF=1 Mirrored

QD40~47 / QD56~63

VRAM3005 — GDDR5

+1.35V_GPU

VREFD_VMA1 0.4MM=16mils
VREFC_VMA1 0.4MM=16mils
VREFD_VMA2 0.4MM=16mils
VREFC_VMA2 0.4MM=16mils

R3073 80.6/F_4 (VMA_CLK0# / VMA_CLK0)
R3074 80.6/F_4 (VMA_CLK1# / VMA_CLK1)

VREF_VMA1_MOS — R3018 549/F_4, R3015 931/F_4, R3070 549/F_4, R3072 931/F_4, R3017 1.33K/F_4, R3071 1.33K/F_4, C3018 820p/50V_4, C3177 820p/50V_4
VREF_VMA2_MOS — R3010 549/F_4, R3011 931/F_4, R3003 549/F_4, R3005 931/F_4, R3012 1.33K/F_4, R3004 1.33K/F_4, C3015 820p/50V_4, C3003 820p/50V_4

Q3009 2N7002K — GPIO10_VREF (53,56)
Q3008 2N7002K — GPIO10_VREF

11/26 change to 100U_1206 *2

C3189 100u_6.3V_1206; C3192 *330U/2.5V_3528; C3178 0.1u/10V_4; C3172 10u/6.3V_6; C3019 10u/6.3V_6; C3184 10u/6.3V_6
20120117 Add C764 for EMI suggestion.

C3191 1u/6.3V_4; C3006 1u/6.3V_4; C3004 1u/6.3V_4; C3186 0.047u/10V_4; C3178 0.047u/10V_4; C3188 0.1u/10V_4; C3187 0.1u/10V_4; C3175 0.1u/10V_4; C3020 0.1u/10V_4

C3181 1u/6.3V_4; C3185 1u/6.3V_4; C3182 1u/6.3V_4; C3180 1u/6.3V_4; C3025 0.047u/10V_4; C3021 0.047u/10V_4; C3002 0.1u/10V_4; C3001 0.1u/10V_4; C3005 0.1u/10V_4; C3190 0.1u/10V_4

C3010 1u/6.3V_4; C3009 1u/6.3V_4; C3026 1u/6.3V_4; C3022 1u/6.3V_4; C3011 0.1u/10V_4; C3190 0.1u/10V_4; C3007 0.1u/10V_4; C3008 *0.1u/10V_4; C3176 *0.1u/10V_4; C3000 *0.1u/10V_4

C3030 *1u/6.3V_4; C3029 1u/6.3V_4; C3028 1u/6.3V_4; C3027 1u/6.3V_4; C3024 0.047u/10V_4; C3023 0.047u/10V_4; C3013 0.1u/10V_4; C3012 0.1u/10V_4; C3016 0.1u/10V_4; C3017 0.1u/10V_4

FBVDDQ_MEM: 1 X 10uF, 4 X 1uF, 6 X 0.1uF
FBVDD: 1 X 10uF, 4 X 1uF

FBA_CMD14 R3002 10K_4; FBA_CMD30 R3007 10K_4
FBA_CMD13 R3001 10K_4; FBA_CMD29 R3008 10K_4
CKE* is strap pin to set ODT value of memory chip
RST PD place @ the end of daisy-chain.

GDDR5 Mode H Mapping

< 0-31 >	< 32-63 >	Memory
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*

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Quanta Computer Inc.
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CHANNEL B: 2G/4G GDDR5

(51) VMC_DQ[63..0] — VMC_DQ[63..0]
(51) FBC_CMD[31:0] — FBC_DBI[7..0]
(51) FBC_DBI[7..0] — FBC_EDC[7..0]
(51) FBC_EDC[7..0]

Channel 0 <0-31>
MF=0 Non-mirrored

QD16~23
QD0~7

Channel 0 <32-63>
MF=1 Mirrored

QD8~15
QD24~31

Channel 1 <0-31>
MF=0 Non-mirrored

QD48~55
QD32~39

Channel 1 <32-63>
MF=1 Mirrored

QD40~47
QD56~63

+1.35V_GPU

VRAM3007 (GDDR5)
VRAM3003 (GDDR5)
VRAM3002 (GDDR5)
VRAM3006 (GDDR5)

(51) VMC_WCK01 — VMC_WCK01
(51) VMC_WCK01# — VMC_WCK01#
(51) VMC_WCK23 — VMC_WCK23
(51) VMC_WCK23# — VMC_WCK23#
(51) VMC_CLK0# — VMC_CLK0#
(51) VMC_CLK0 — VMC_CLK0
(51) VMC_WCK45 — VMC_WCK45
(51) VMC_WCK45# — VMC_WCK45#
(51) VMC_WCK67 — VMC_WCK67
(51) VMC_WCK67# — VMC_WCK67#
(51) VMC_CLK1# — VMC_CLK1#
(51) VMC_CLK1 — VMC_CLK1

R3102 120/F_4 1K_4 SEN_C
R3046 1K_4
R3042 1K_4
R3061 120/F_4 SEN_C
R3041 1K_4
R3025 120/F_4 1K_4 SEN_D
R3033 1K_4
R3040 1K_4
R3029 120/F_4 SEN_D
R3038 1K_4

R3060 80.6/F_4
R3027 80.6/F_4

VREF_VMC1_MOS
R3053 549/F_4
R3051 931/F_4
R3048 549/F_4
R3050 931/F_4
R3052 1.33K/F_4
R3047 1.33K/F_4
VREFD_VMC1
VREFC_VMC1
C3154 820p/50V_4
C3150 820p/50V_4

VREF_VMC2_MOS
R3026 549/F_4
R3028 931/F_4
R3032 549/F_4
R3030 931/F_4
R3024 1.33K/F_4
R3031 1.33K/F_4
VREFD_VMC2
VREFC_VMC2
C3033 820p/50V_4
C3036 820p/50V_4

Q3002 2N7002K
GPIO10_VREF (53,55)

R3045 10K_4
R3036 10K_4
R3044 10K_4
R3037 10K_4

CKE* is strap pin to set ODT value of memory chip

RST PD place @ the end of daisy-chain.

C3194 330U/2.5V_3528
C3219 330U/2.5V_3528
C3196 0.1u/10V_4
C3091 10u/6.3V_6
C3204 10u/6.3V_6
C3195 10u/6.3V_6
11/26 change to 100U_1206 *2
20120117 Add C764 for EMI suggestion.

C3160 1u/6.3V_4
C3211 1u/6.3V_4
C3223 1u/6.3V_4
C3165 0.047u/10V_4
C3222 0.047u/10V_4
C3198 0.1u/10V_4
C3199 0.1u/10V_4
C3221 0.1u/10V_4
C3220 0.1u/10V_4

C3032 1u/6.3V_4
C3031 1u/6.3V_4
C3034 1u/6.3V_4
C3035 1u/6.3V_4
C3200 0.047u/10V_4
C3092 0.047u/10V_4
C3085 0.1u/10V_4
C3124 0.1u/10V_4
C3113 0.1u/10V_4
C3106 0.1u/10V_4

C3100 1u/6.3V_4
C3084 1u/6.3V_4
C3170 1u/6.3V_4
C3167 1u/6.3V_4
C3166 0.1u/10V_4
C3043 0.1u/10V_4
C3169 0.1u/10V_4
C3168 *0.1u/10V_4
C3071 *0.1u/10V_4
C3054 *0.1u/10V_4

C3097 0.1u/10V_4
C3081 1u/6.3V_4
C3096 1u/6.3V_4
C3080 1u/6.3V_4
C3095 0.047u/10V_4
C3079 0.047u/10V_4
C3098 0.1u/10V_4
C3082 0.1u/10V_4
C3099 0.1u/10V_4
C3083 0.1u/10V_4

GDDR5 Mode H Mapping

< 0-31 >	< 32-63 >	Memory
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*

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	N15P-GX/GT GDDR5 VRAM 2/2	
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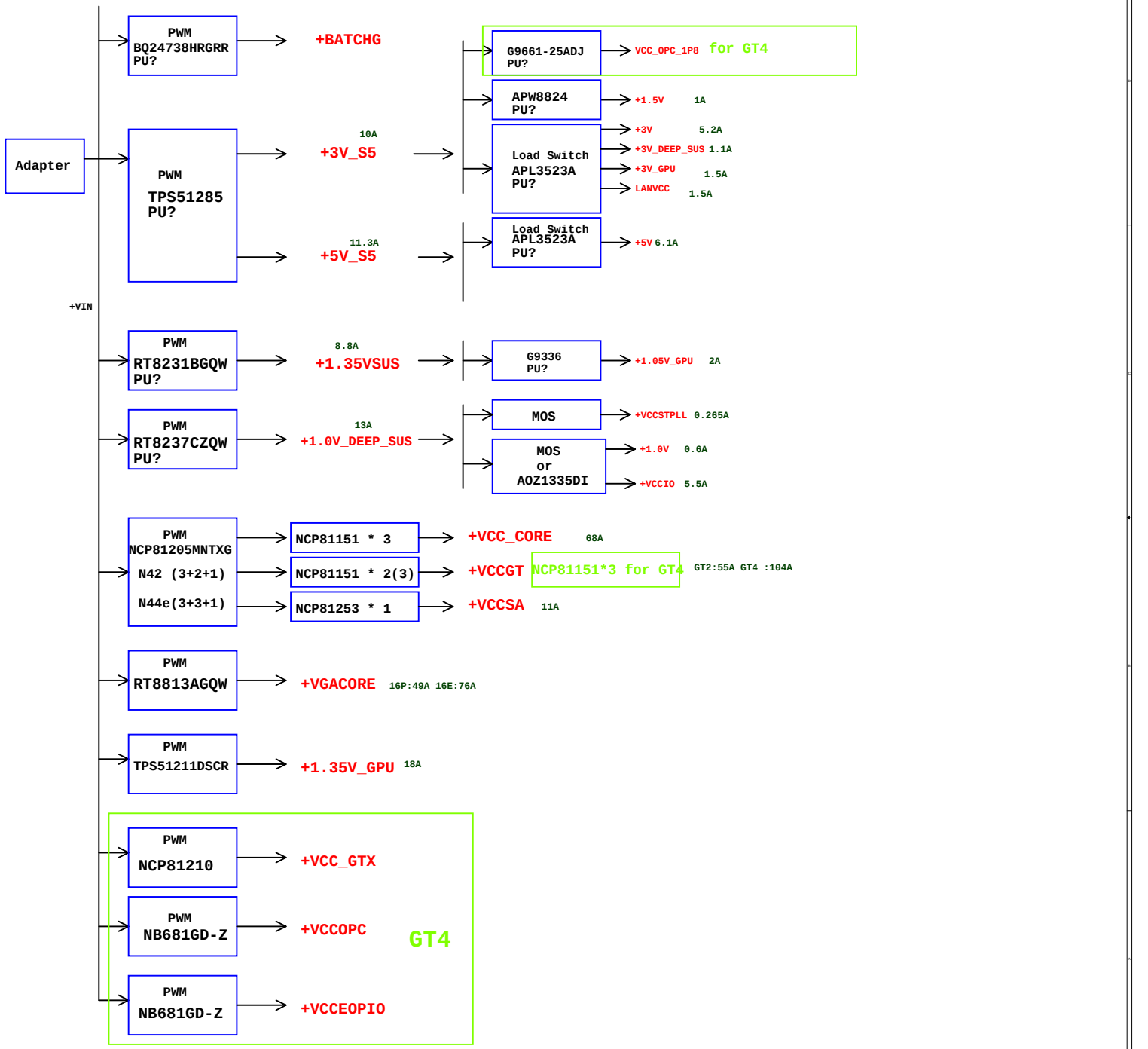
Power Delivery Map



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(20,21,22,23,25,30,31,43,45,49) +5V
(19,33,34,35,36,39,40,41,42,46,47,49) +VIN

29

CPU BRACKET

H21
*H-TC197BC276D150P2

H22
*H-TC197BC276D150P2

H25
*H-TC197BC276D150P2

H24
*H-TC209X189BC296X276D170X150P2

H5
*h-c83d83n

VGA BRACKET

H12
*h-tc315ic150bc150d150pt

H8
*h-tc315ic150bc150d150pt

R3126
*0_4_S

R3127
*0_4_S

H37
*H-TC315IC150BC150D150PT

H19
*HG-TC236BC315D110P2

H18
*HG-TC236BC315D110P2

H2
*hg-ts2bc236d110p2

H6
*spad-nl8-2np

H7
*hg-ts3bc315d110p2

H9
*SPAD-RE200X25

+ADPIN

H13
*hg-ts1bc236d110p2

H3
*spad-c315np

H36
*HG-C315IC245D110P2

H28
*H-TC236IC150BC315D110P2

H23
*spad-nl8-1np

H34
*h-o102x83d102x83n

H26
*HG-C315D110P2

H16
*SPAD-NL8-4-NP

H33
H-TC197IC87BC59D59P2

H38
*SPAD-C236NP

H30
H-TC197IC87BC59D59P2

H20
*spad-c236np

H1
*h-ts1bc83d83pt

H29
SPAD-re118x157np

H15
*SPAD-NL8-3-NP

H10
*h-tc315ic150bc150d150pt

H32
*SPAD-NL8-3NP

H4
*spad-re196x340np

H11
*SPAD-RE110X140

+VA

H14
*spad-c315np

H35
*spad-c236np

EMI

+5V

EC46	*0.1U/10V_4
EC48	*0.1U/10V_4
EC47	*0.1U/10V_4
EC54	*0.1U/10V_4
EC36	*0.1U/10V_4
EC35	*0.1U/10V_4
EC40	*0.1U/10V_4
EC39	*0.1U/10V_4
EC42	*0.1U/10V_4

+VAD

EC59	0.1U/10V_4
EC60	0.1U/10V_4
EC7	0.1U/10V_4
EC6	0.1U/10V_4
EC1	0.1U/10V_4

+VIN

EC49	0.1U/10V_4
EC52	0.1U/10V_4
EC50	0.1U/10V_4
EC51	0.1U/10V_4
EC16	0.1U/10V_4
EC65	0.1U/10V_4
EC45	0.1U/10V_4
EC44	0.1U/10V_4

ESD

R657	*0_4_S
R678	*0_4_S
R346	*0_4_S
R304	*0_4_S

AGND

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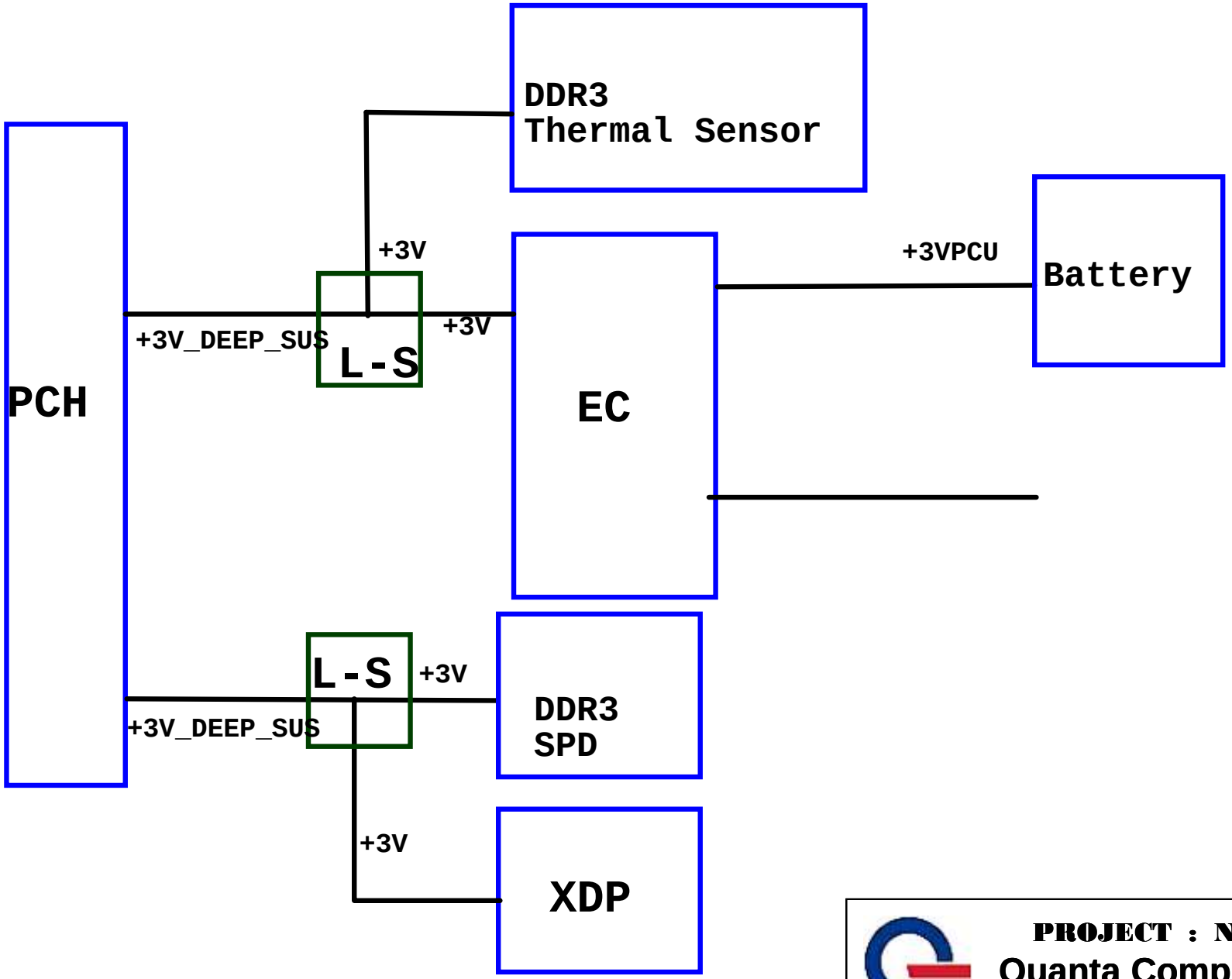

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			59
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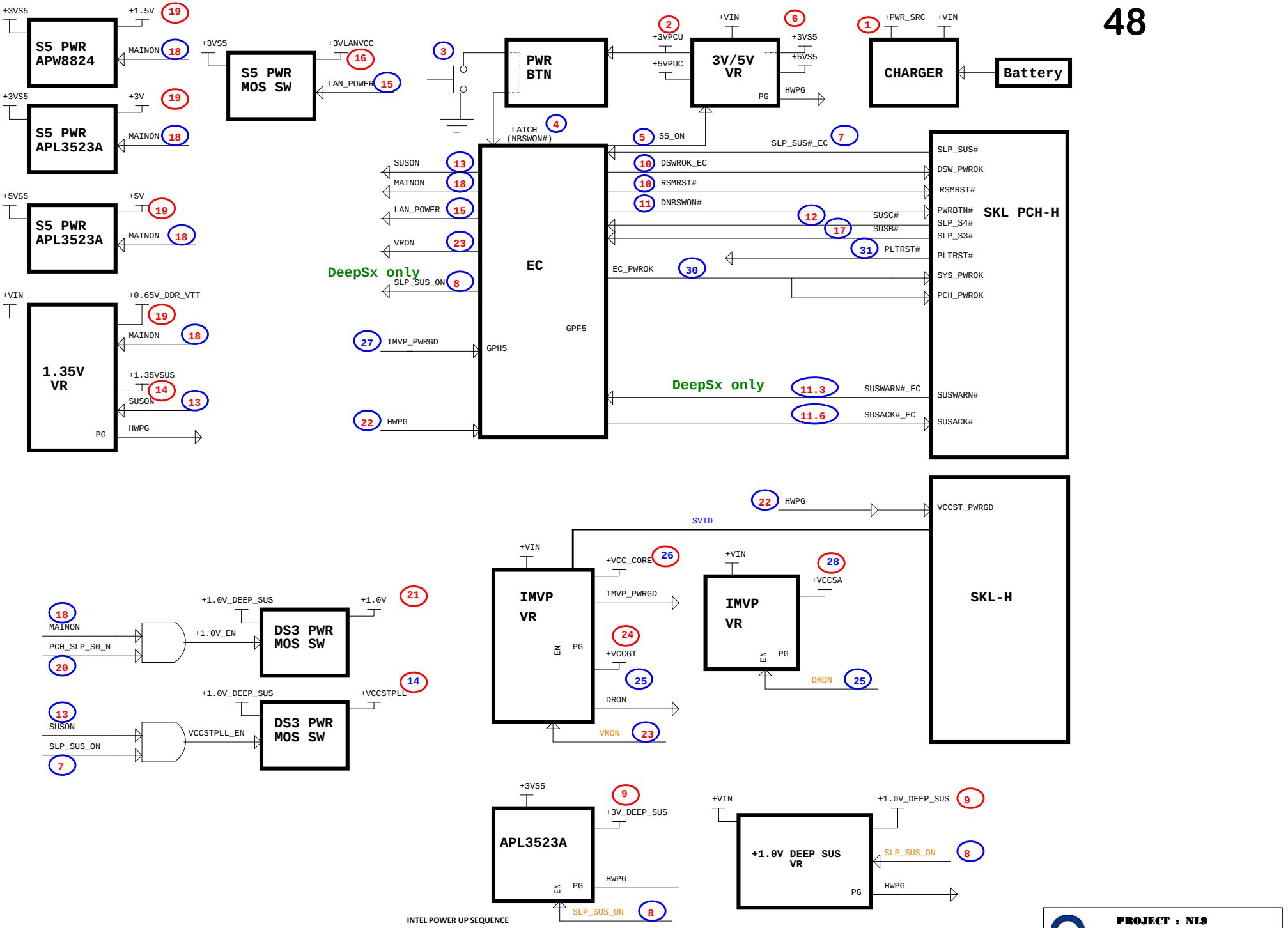

INTEL POWER UP SEQUENCE

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Size	Document Number	Rev
C	Power sequencce diagram	1A

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	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
2015 SDV	EC-A-01	32	7/30	L3004 C3226	reserve N16E-GR power rail
	EC-A-02	11,25	8/12		SATA port4 change to port3 for HM170
	EC-A-03				N16E only
	EC-A-04	3,19	8/14	C45,c46,c47,c48	reserve for UHD panel
	EC-A-05		8/24		0ohm change to shortpad
	EC-A-06	30	8/26	Q51,Q35,Q33,Q34,U12,C617,C625,C626 ,R312,R313,R318,R325,R323,R322	ASM GPU thermal HW protect
SIT	EC-C-01	8	9/30		A36,A37 pin contact GND
	EC-C-02		9/30	L3000,L3001,L3002,L3003,L3004	EOD,change to CX5PX330000/CX330T30000 RC0402
	EC-C-03	24	9/30	C756,C757	change to 10p for crystal report
	ECP-C-01	50	10/12	PC110	change to 0.01u for GC6
	EC-C-05	30	10/08	R3129,R3130,R3131,R3132,Q57,Q58 (All no ASM)	Thermal request
	EC-C-06		10/12	C3212,C3213	ASM for GC6
	ECP-C-02	50	10/14	PQ44,PQ46,PR262,PR263,PR264(All ASM)	for UVP

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Custom	EC list-1	1A

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