LCFC Confidential

L340-IRH +N17P-G0 MB Schematics Document

Coffee Lake-R with DDR4 + Nvidia N17P-G0-K1-A1

2019-03-20

REV:1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title: Cover Page

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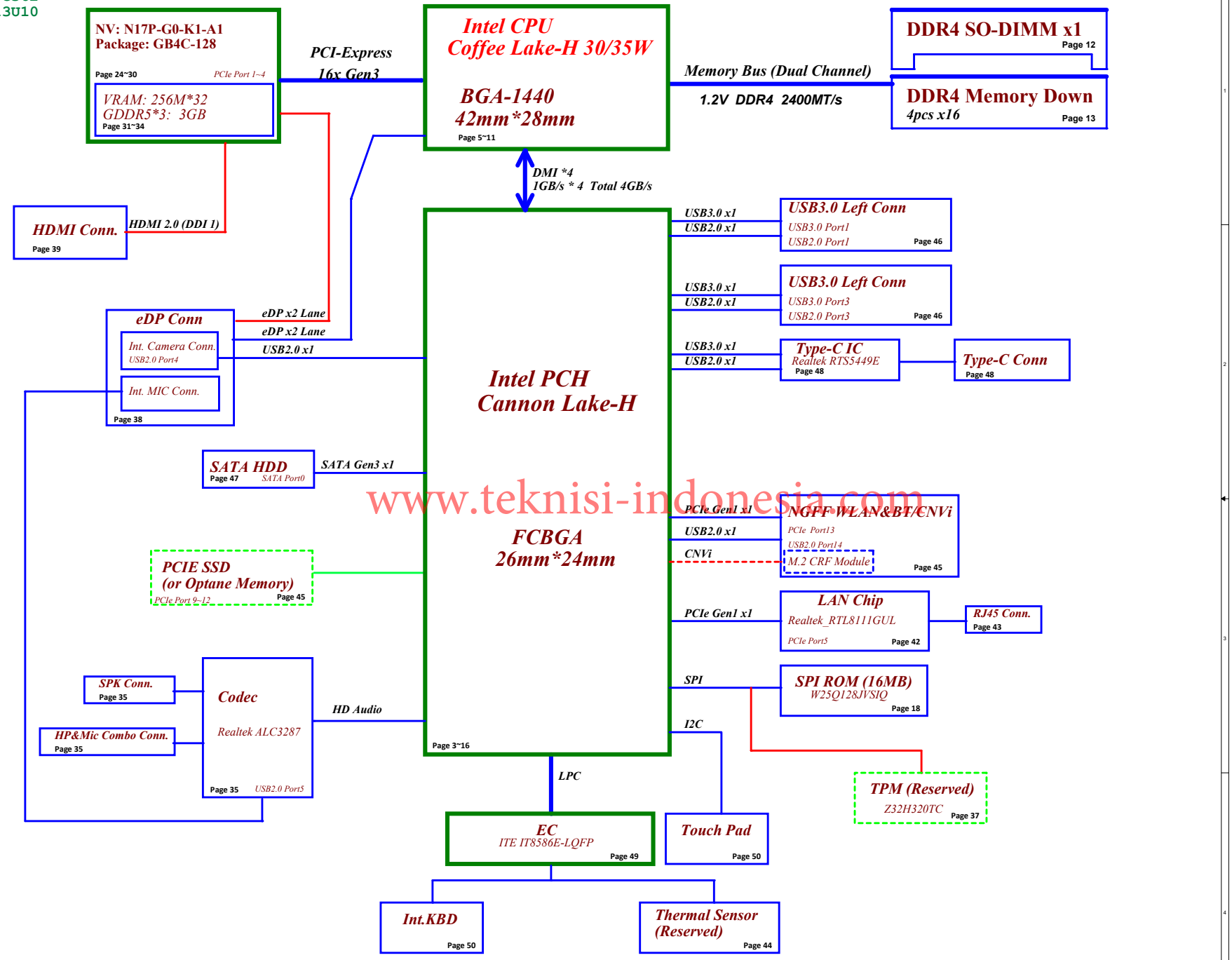
LCFC confidential

Board name:NM-C362
MB P/N:DA800013U10



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Title: Block Diagram

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

HSIO PORT		Function
USB3.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	4	USB Type-C
USB2.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	8	Camera
	14	Bluetooth
PCIE	0~15 X16 PCIE CPU	DGPU
	14	LAN
	13	WLAN
	9~12 X4 PCIE	Optane Memory
SATA	4	HDD

BOM Structure	BTO Item
@	Not stuff
15or17@	For 15" or 17" part
I5@	For I5 CPU
I7@	For I7 CPU
ES_CPU@	For ES CPU
CD@	For C cost down
EMC@	For EMC part
EMC_NS@	For EMC nu-stuff part
ME@	For ME part
OPT@	For NV GPU part
OPT_NS@	For NV GPU not stuff part
TPM@	For TPM part
8111GUL@	For 8111GUL LAN
8111H@	For 8111H LAN
NM-C362@	For PCB P/N
GST@	For GST Transformer
INPAQ@	For INPAQ Transformer
AJOHO@	For AJOHO Transformer
M8GX3@	For Micron VRAM X76
S8GX3@	For Samsung VRAM X76
H8GX3@	For Hynix VRAM X76
S8G_VR@	For Samsung VRAM
H8G_VR@	For Hnix VRAM
M8G_VR@	For Micron VRAM
DRAM_S8G@	For Samsung DRAM X76
DRAM_M8G@	For Micron DRAM X76
DRAM_H8G@	For Hynix DRAM X76
MD_S8Gb@	For Samsung DRAM
MD_H8Gb@	For Hnix DRAM
MD_M8Gb@	For Micron DRAM
USB@	For USB part
DEBUG@	For USB DEBUG part
RF@	For RF part
RF_NS@	For RF unstuff part
CNVI@	For CNVI part
BL@	For BL part
NON_BL@	For NON-BL part
AOAC@	For AOAC part
SDP@	For SDP memory part
DDP@	For DDP memory part
CNL_H@	For CNL PCH part
MD@	For memory down part
DCI@	For DCI part
UART@	For UART part

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
PCH	need to update
DGPU	need to update

EC SMBus3 address

Device	Address
PMIC	need to update

PCH SM Bus address

Device	Address
DDR4 SODIMM	need to update
Wlan	Reserved

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Title: **Notes List**

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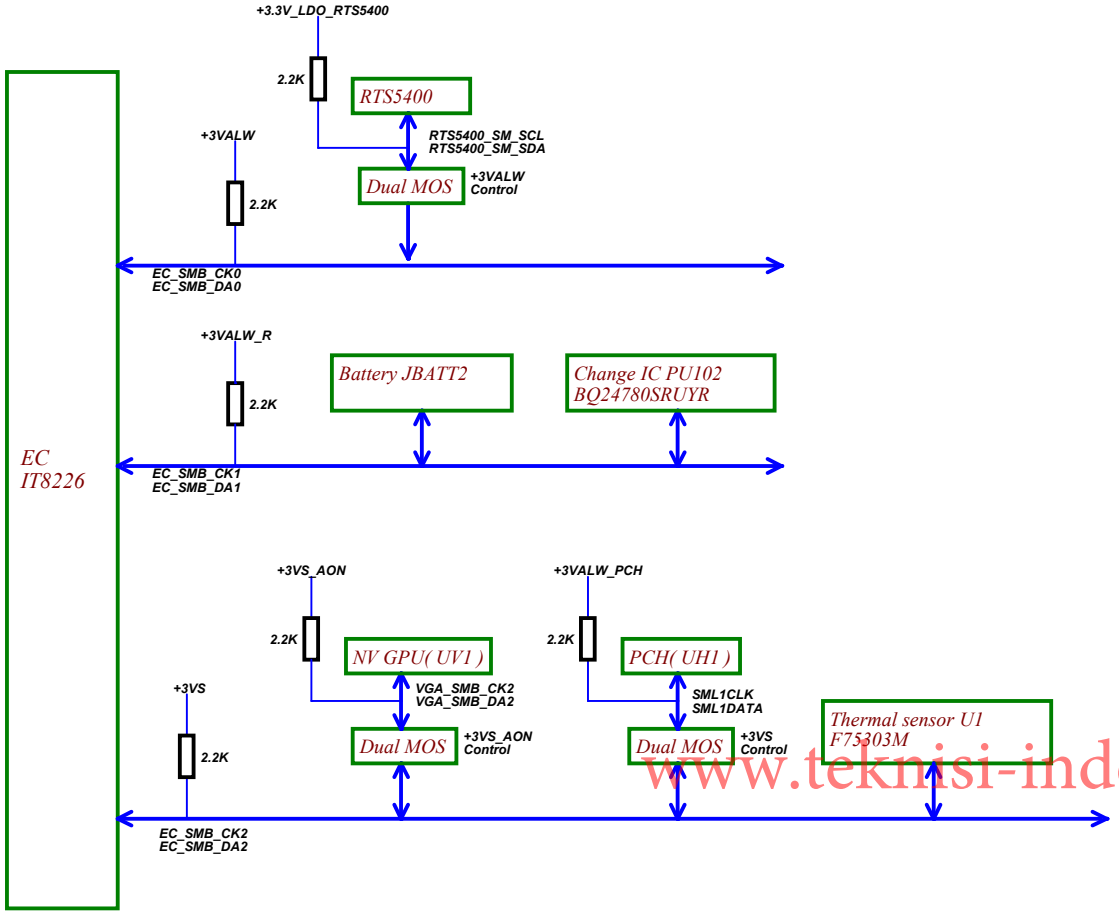

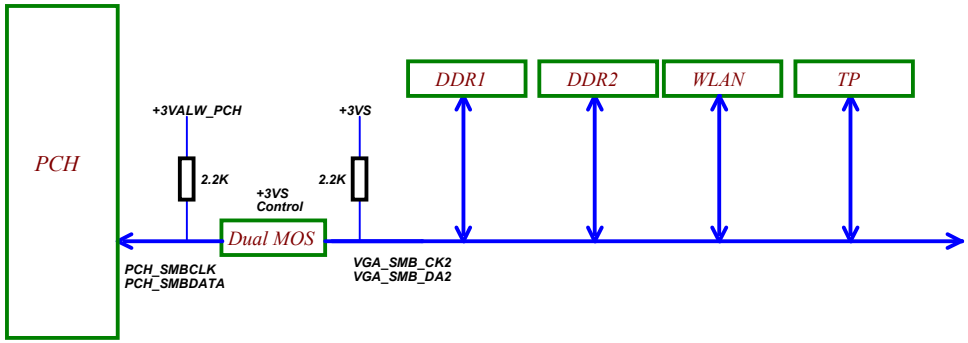

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8226 +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8226 +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	V +3VALW_PCH	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

EC SM Bus1 address

Device	
Smart Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001_100xb
VGA	0x41(default)
PCH	need to update
RTS5400	0xD4

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb
WLAN	Rsvd

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Title: Blank4

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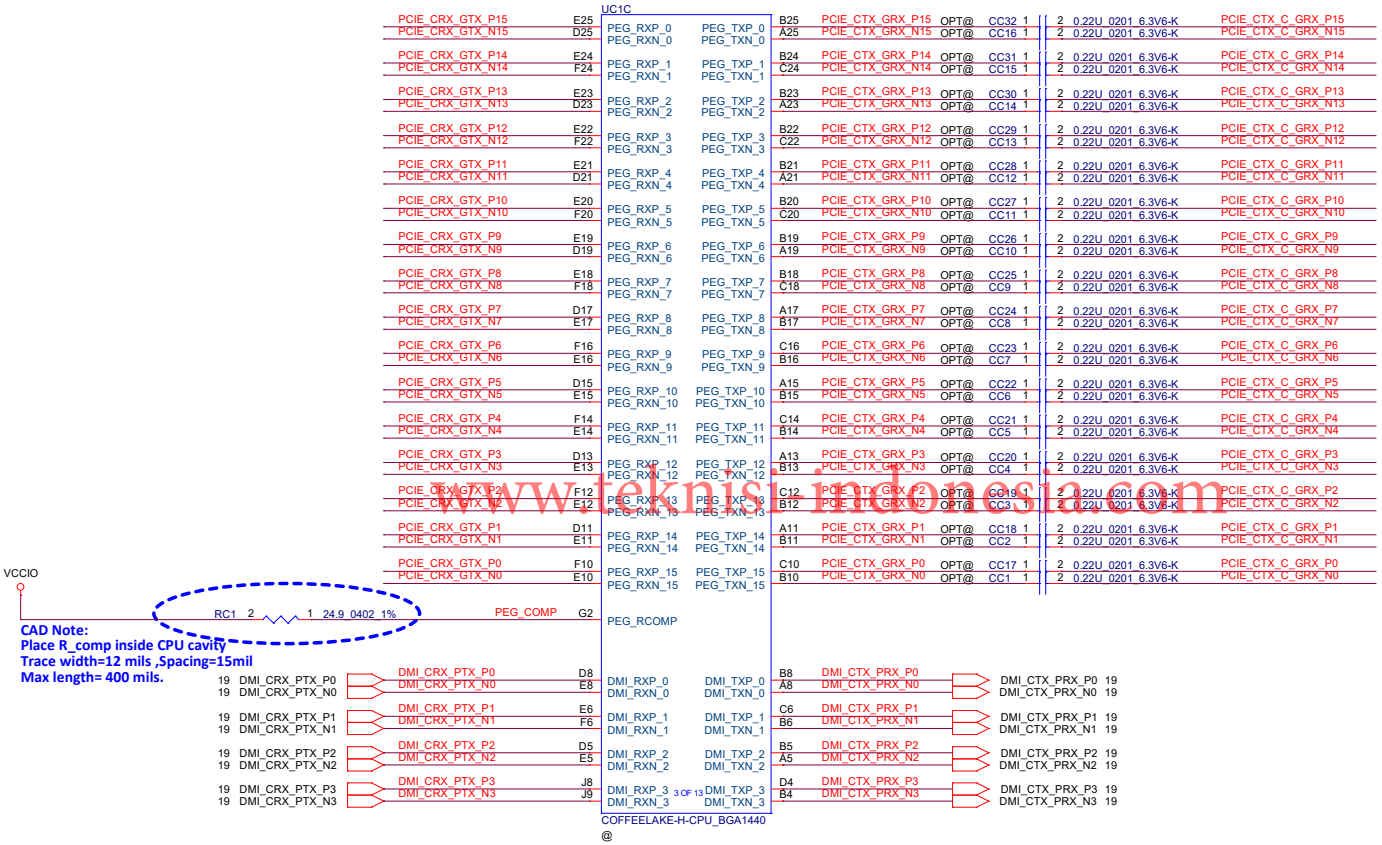
25 PCIE_CRX_GTX_N[0..15]
25 PCIE_CRX_GTX_P[0..15]

PCIE_CTX_C_GRX_N[0..15] 25
PCIE_CTX_C_GRX_P[0..15] 25



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Issued Date	2015/02/26	Deciphered Date	2018/09/20

Title: CPU (1/7) DMI,PEG

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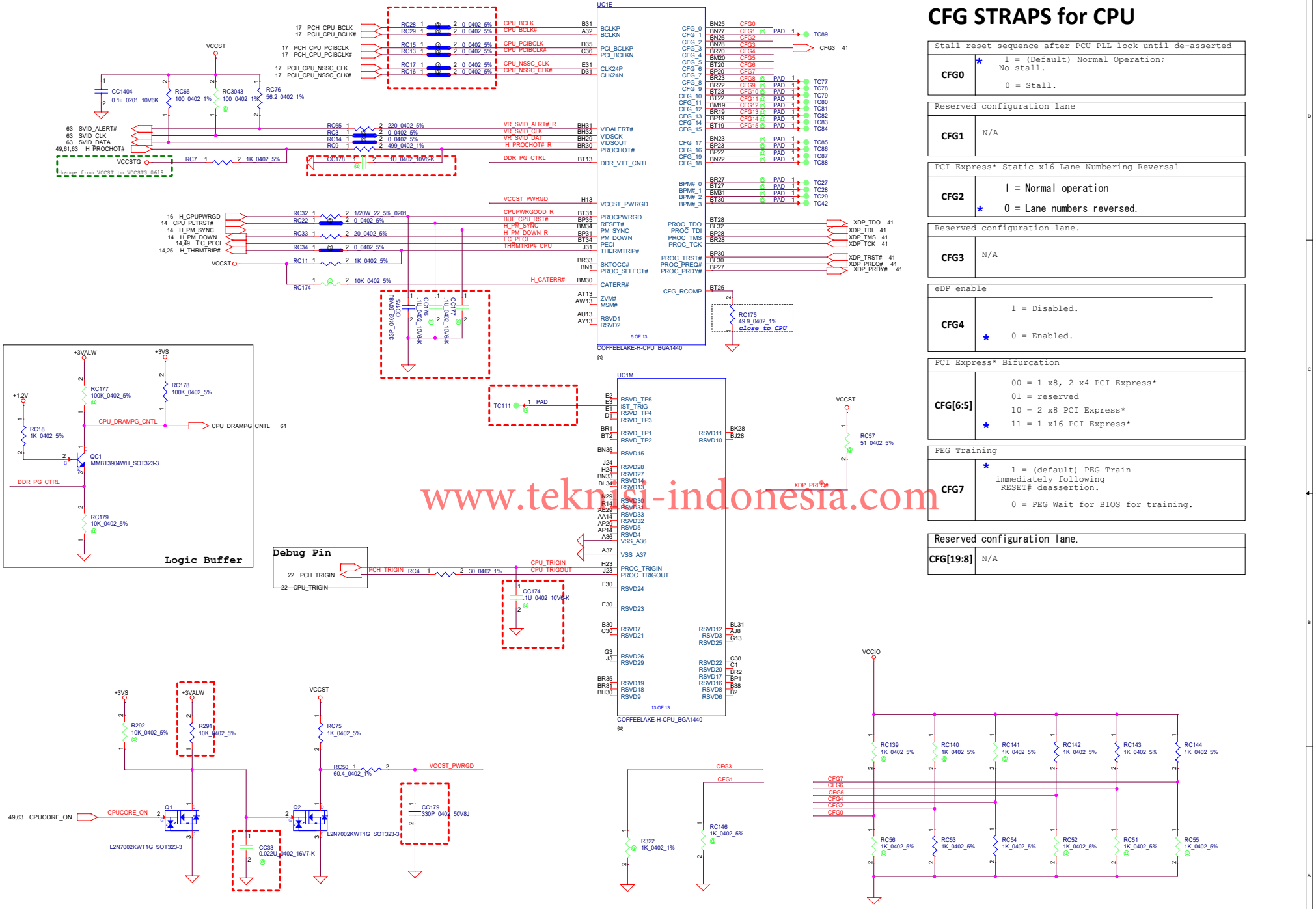

CFG STRAPS for CPU

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	* 1 = (Default) Normal Operation; No stall. 0 = Stall.
Reserved configuration lane	
CFG1	N/A
PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation * 0 = Lane numbers reversed.
Reserved configuration lane.	
CFG3	N/A
eDP enable	
CFG4	1 = Disabled. * 0 = Enabled.
PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* * 11 = 1 x16 PCI Express*
PEG Training	
CFG7	* 1 = (default) PEG Train immediately following RESET# deassertion. 0 = PEG Wait for BIOS for training.
Reserved configuration lane.	
CFG[19:8]	N/A

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Title: CPU (2/7) PM, XDP, CLK, CFG

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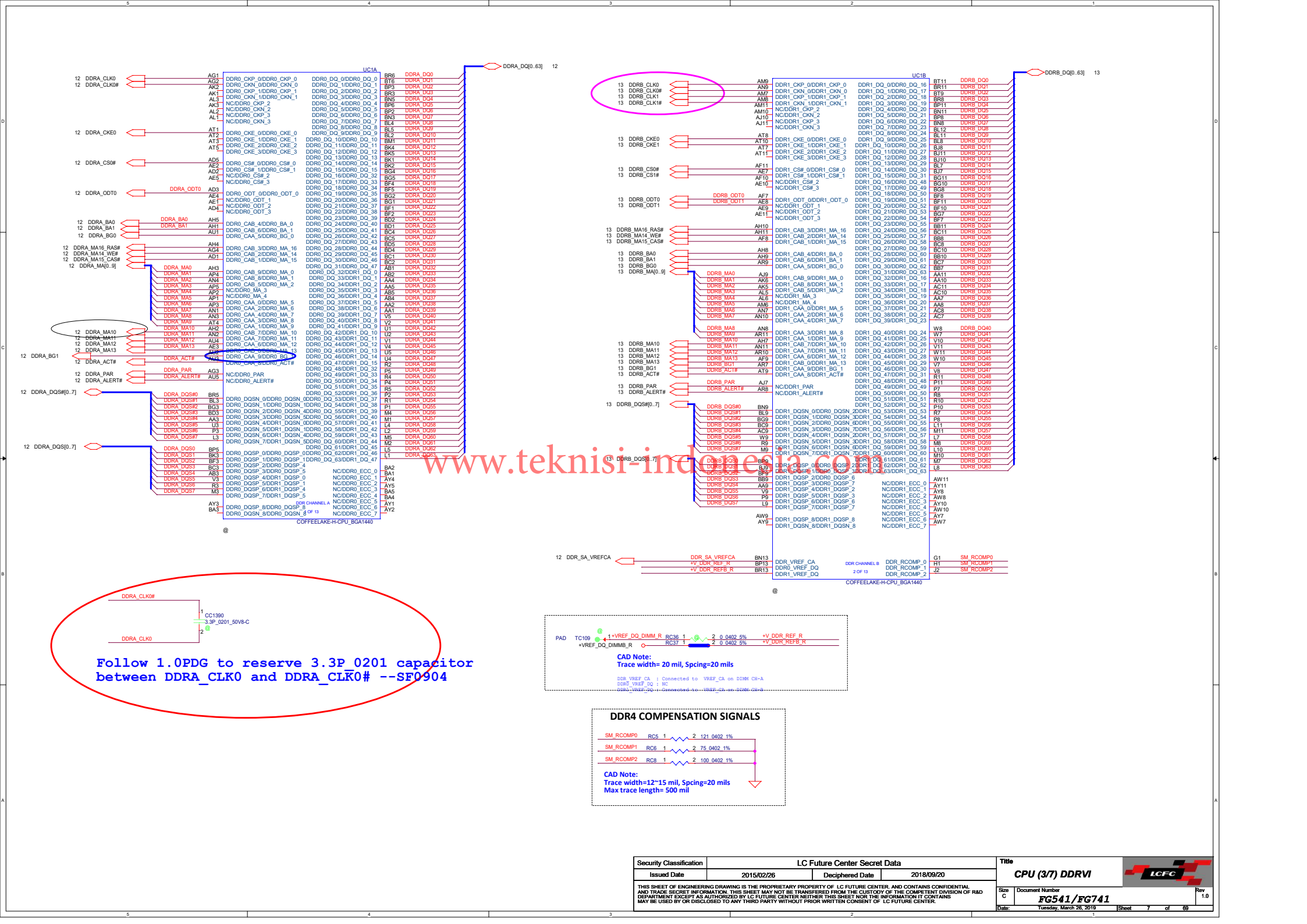

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2018/09/20

Title: CPU (3/7) DDRVI

Size	Document Number	Rev
C	FG541/FG741	1.0

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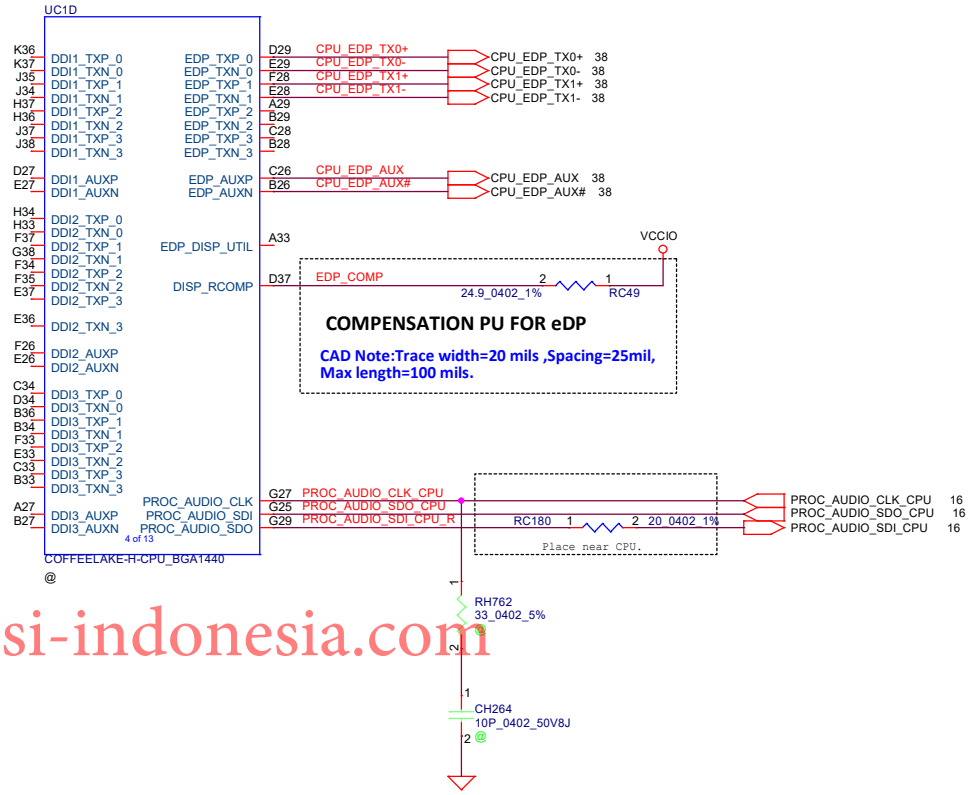

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Title: CPU (4/7) eDP, DDI

Size	Document Number	Rev
A3	FG541/FG741	1.0

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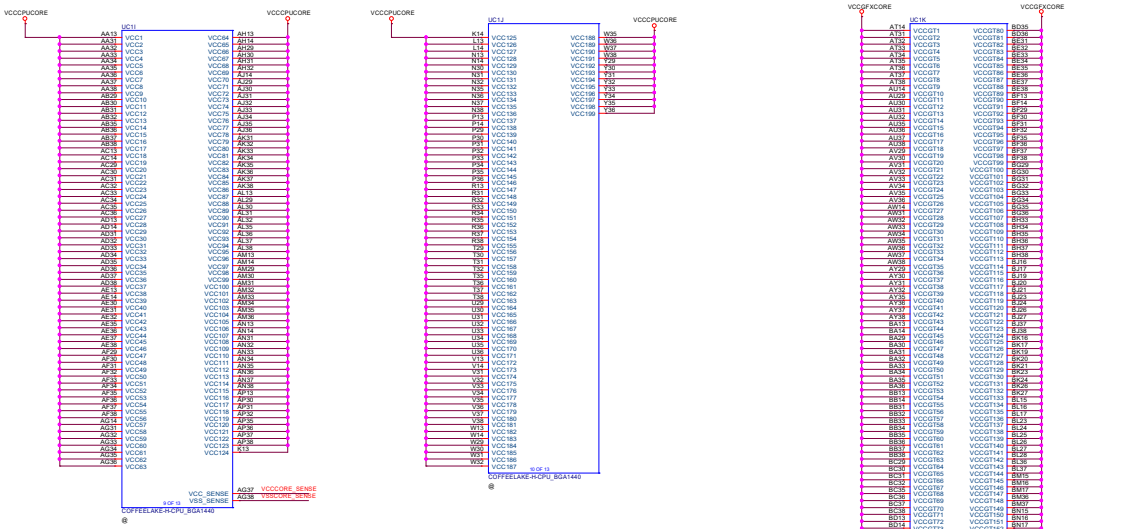

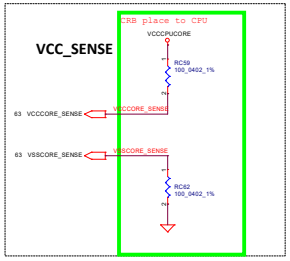

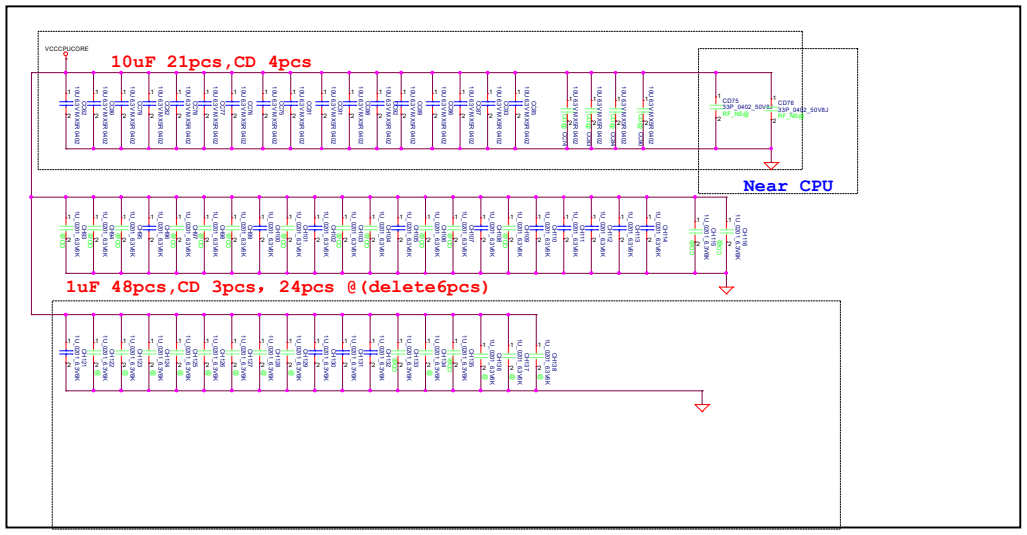

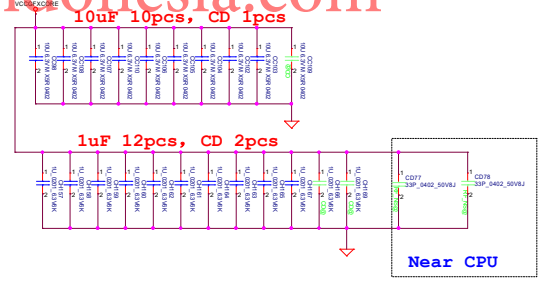

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Title: CPU (5/7) PWR, BYPASS

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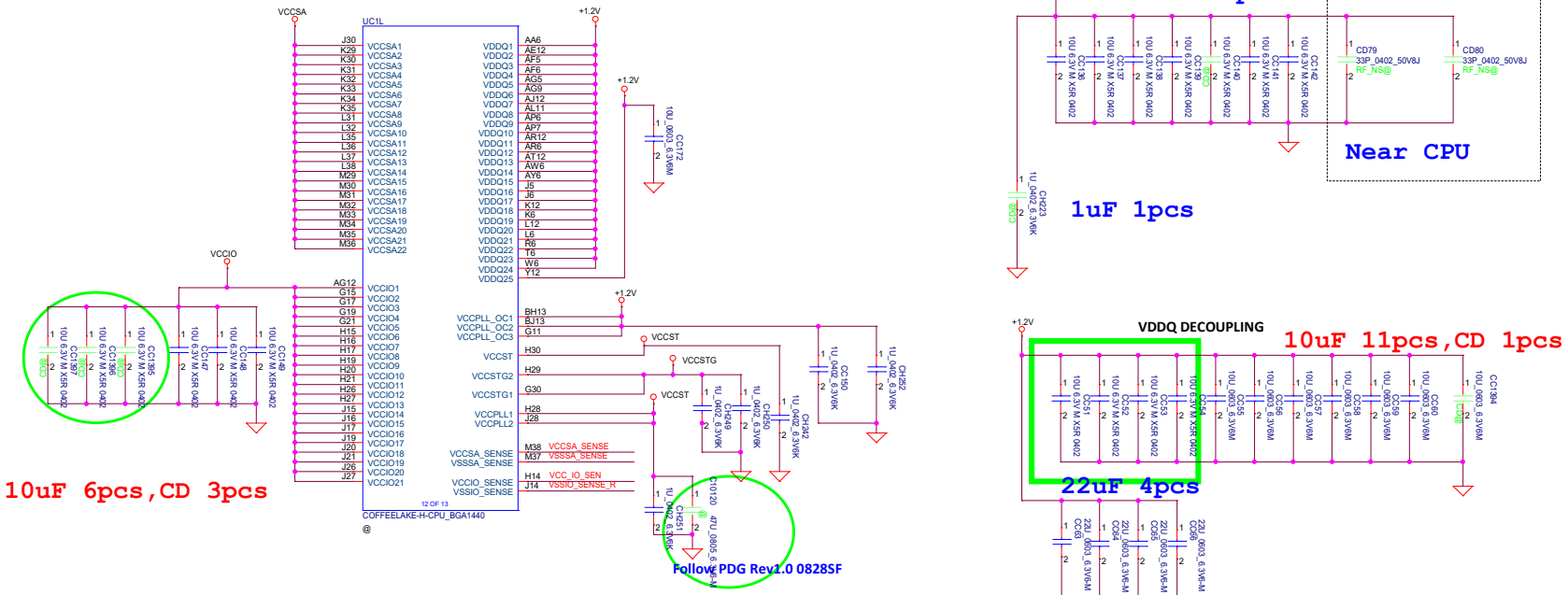

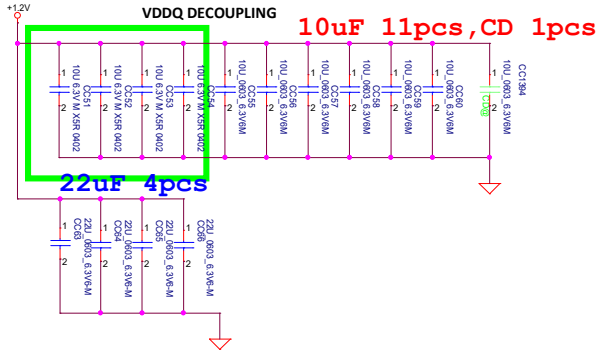

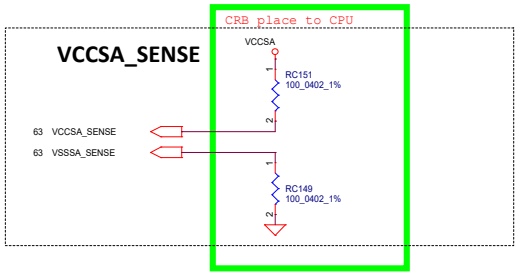

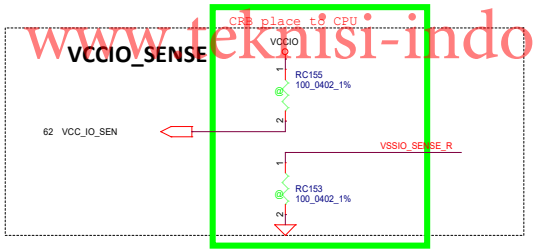

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Title	CPU (6/7) PWR, BYPASS		
Size	Document Number		Rev
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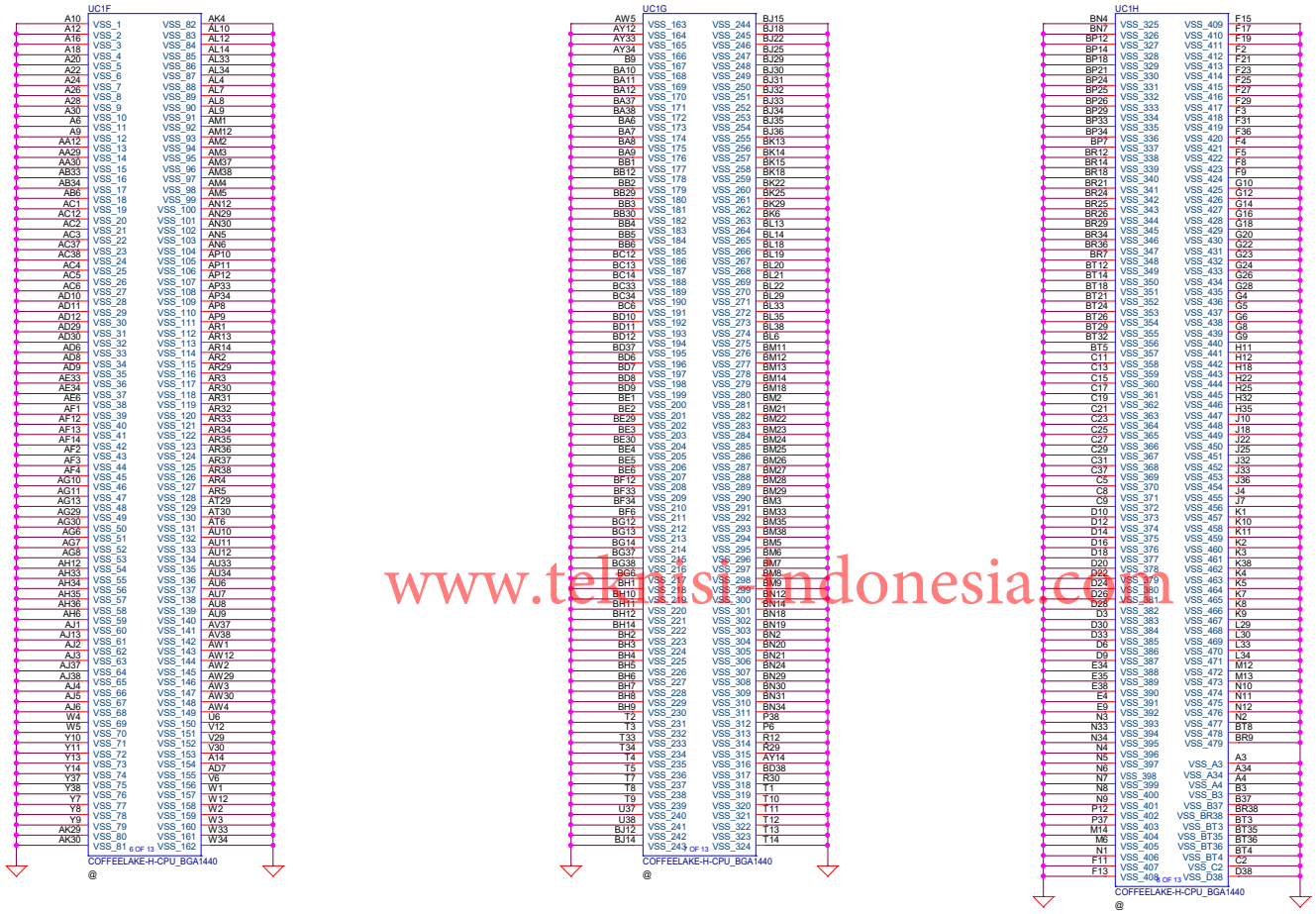

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Title: **CPU (6/7) PWR, VSS**

Size	Document Number	Rev
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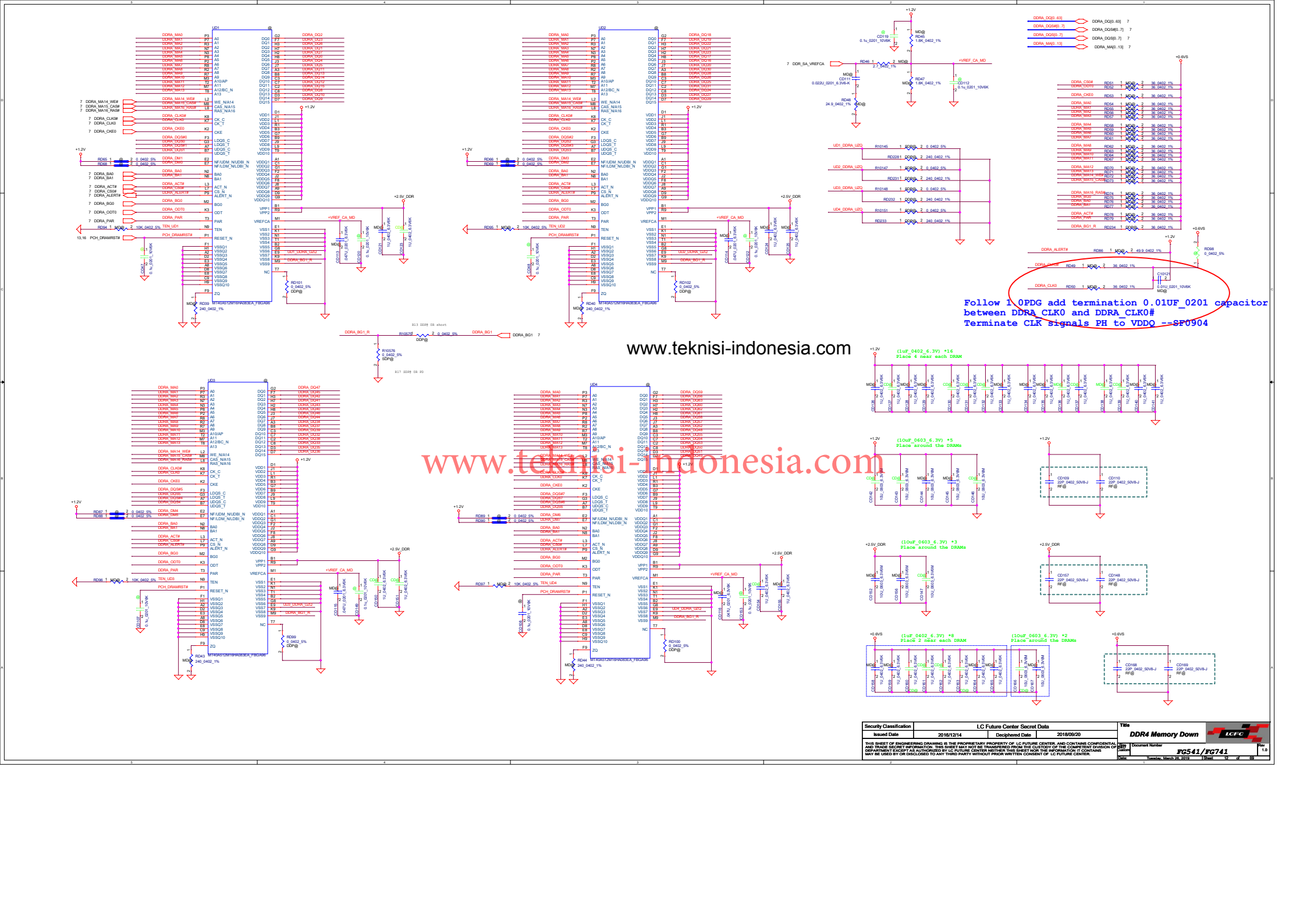
Follow 1.0PDG add termination 0.01UF_0201 capacitor
between DDRA_CLK0 and DDRA_CLK0#
Terminate CLK signals PH to VDDQ --SF0904
www.teknisi-indonesia.com
www.teknisi-indonesia.com
(1uF_0402_6.3V) *16
Place 4 near each DRAM
(10uF_0603_6.3V) *5
Place around the DRAMs
(10uF_0603_6.3V) *3
Place around the DRAMs
(1uF_0402_6.3V) *8
Place 2 near each DRAM
(10uF_0603_6.3V) *2
Place around the DRAMs
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2016/12/14
Deciphered Date
2018/09/20
DDR4 Memory Down
FG541/FG741
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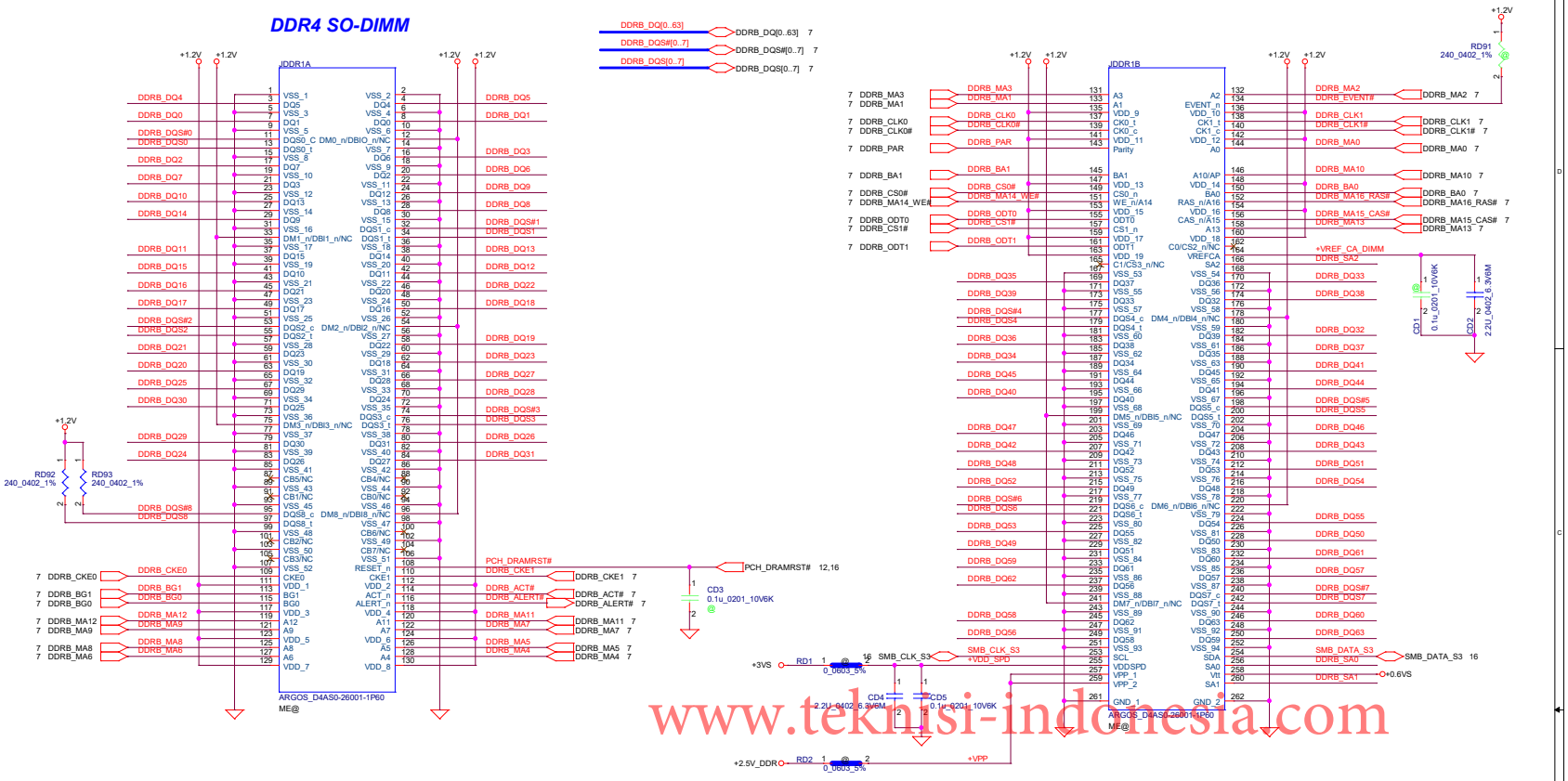
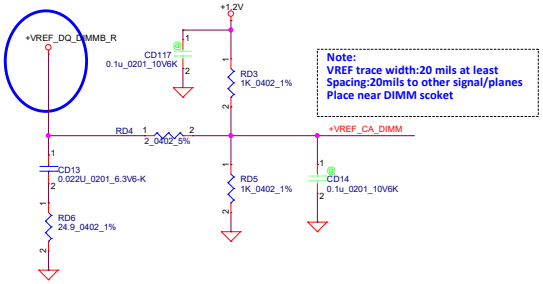
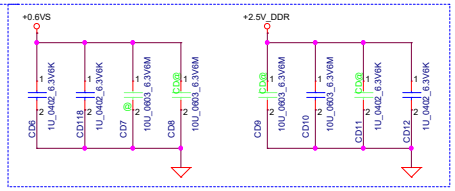
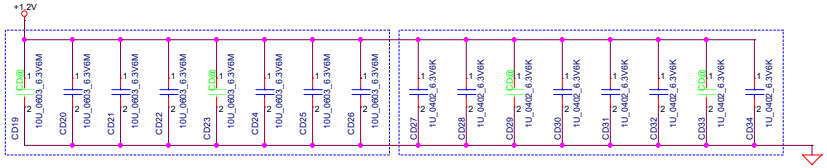
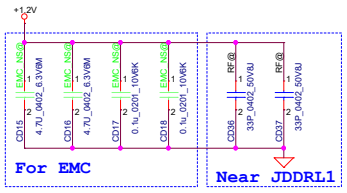
DDR4 SO-DIMM

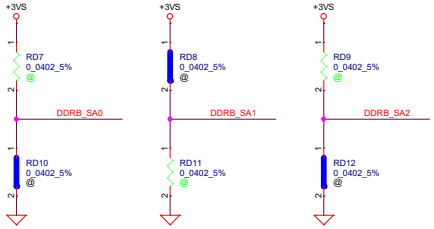












SPD Address = 2H

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Title: DDR4 SO-DIMM

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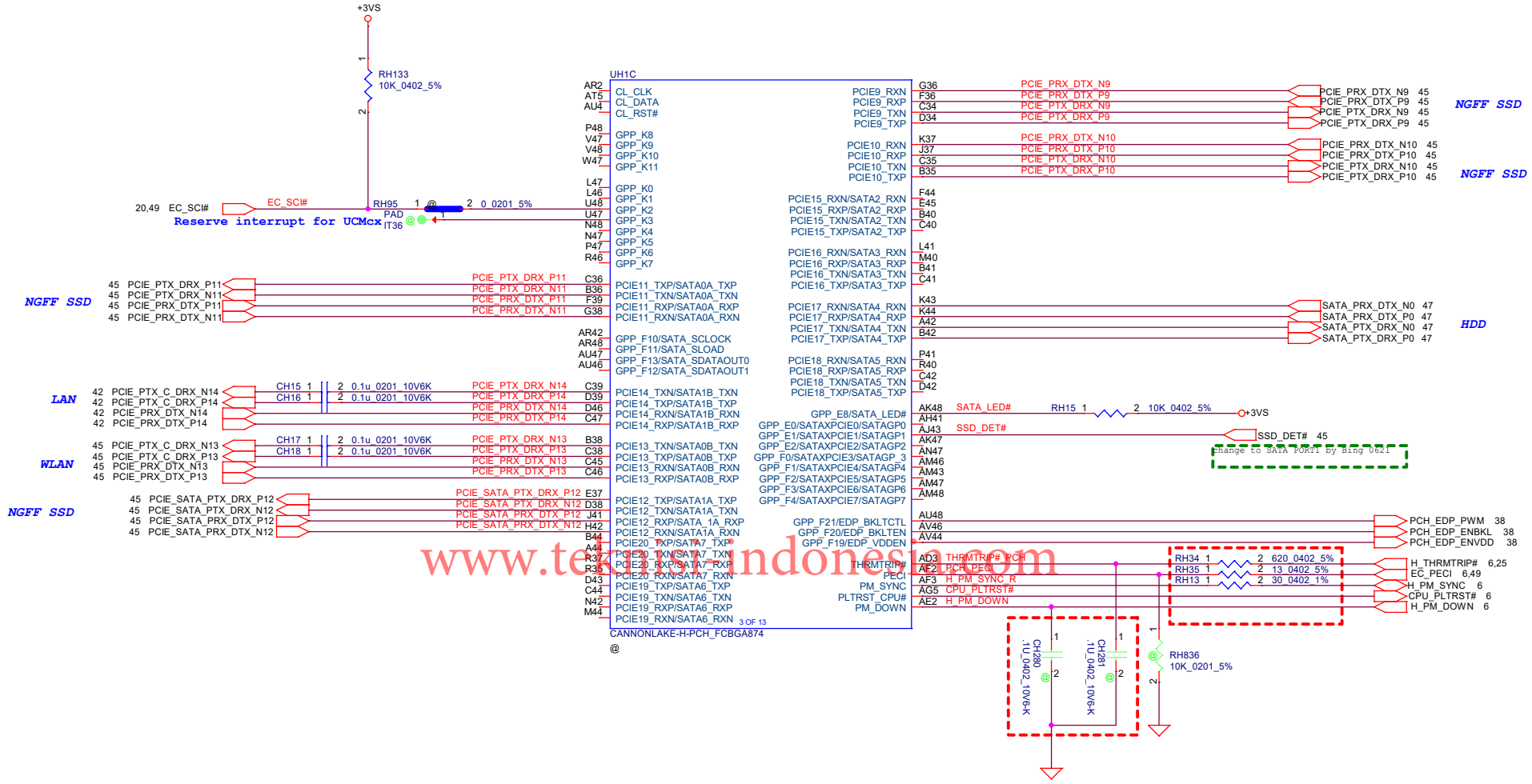

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Title: PCH (1/9) PCIe/SATA/GPPFG

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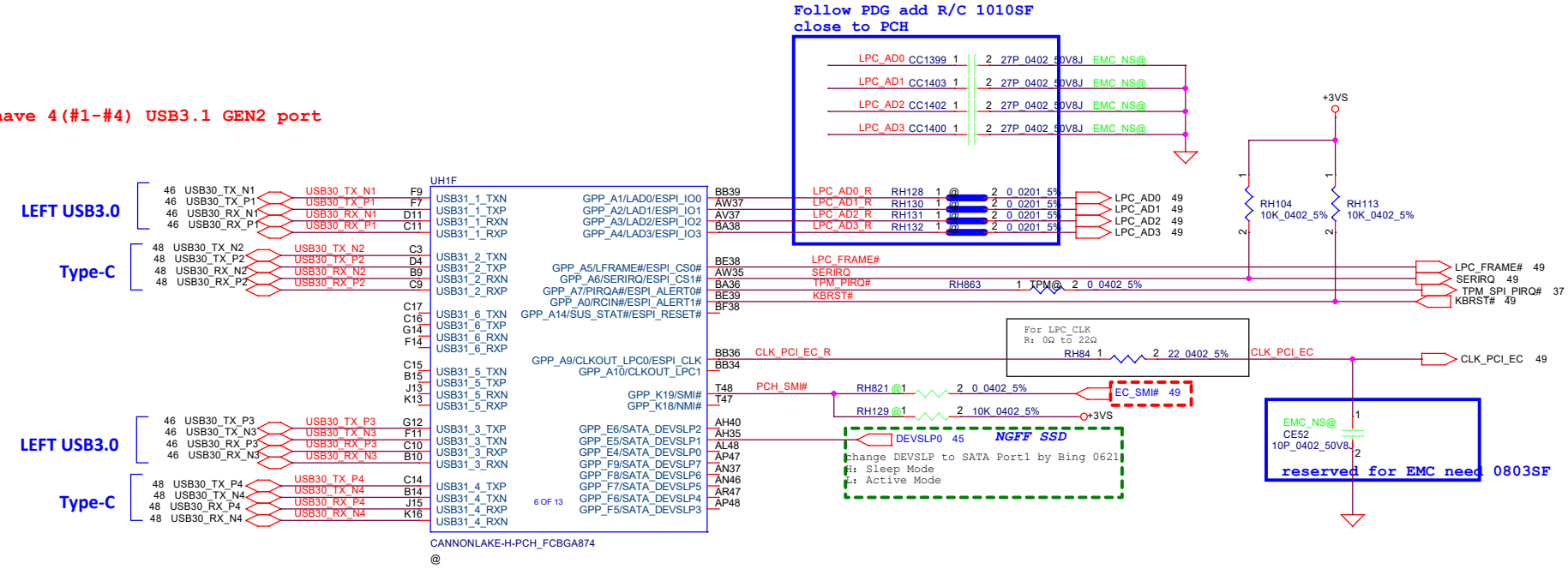
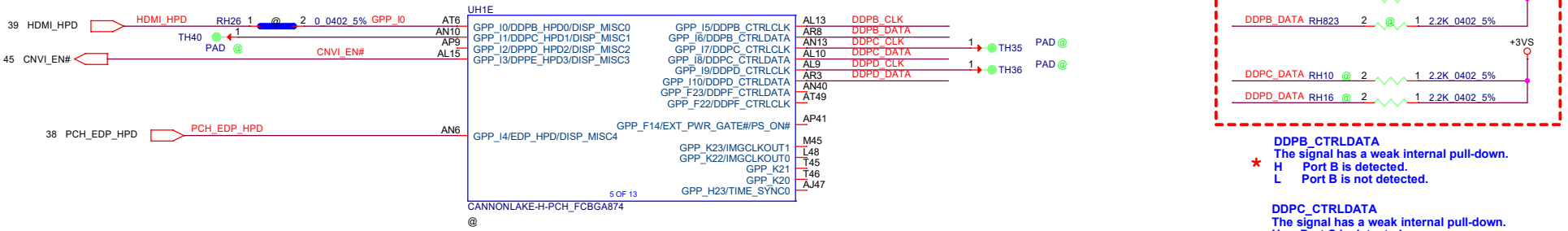
HM370 only have 4(#1-#4) USB3.1 GEN2 port

Follow PDG add R/C 1010SF close to PCH





DDPB_CTRLDATA
The signal has a weak internal pull-down.
* H Port B is detected.
L Port B is not detected.

DDPC_CTRLDATA
The signal has a weak internal pull-down.
* H Port C is detected.
L Port C is not detected. (Default)

DDPD_CTRLDATA
The signal has a weak internal pull-down.
* H Port D is detected.
L Port D is not detected. (Default)

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2018/09/20

Title: PCH (2/9) USB3/GPPAEFGHI

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A3	FG541/FG741	1.0

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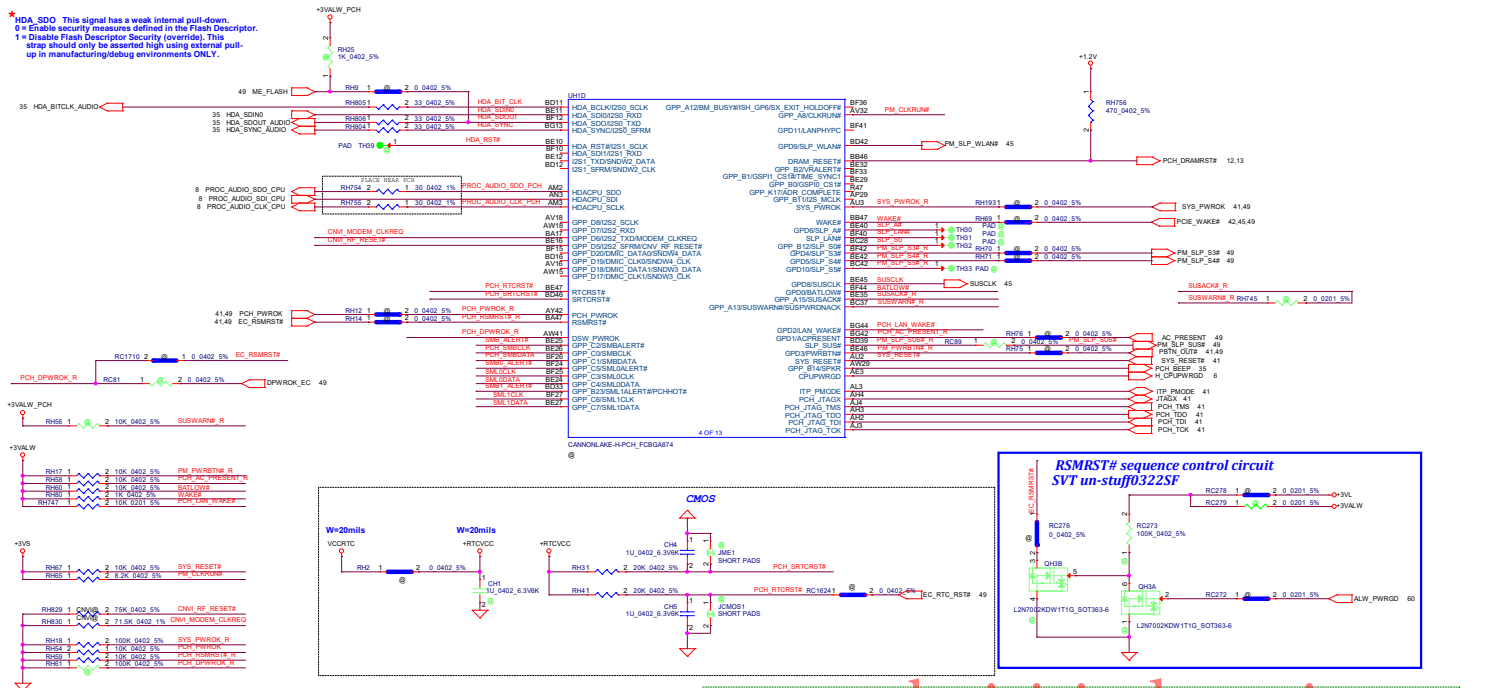

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2018/09/20

Title: PCH (3/9) HDA,RTC,SMBUS,PM

Size: Custom	Document Number: FG541/FG741		Rev: 1.0
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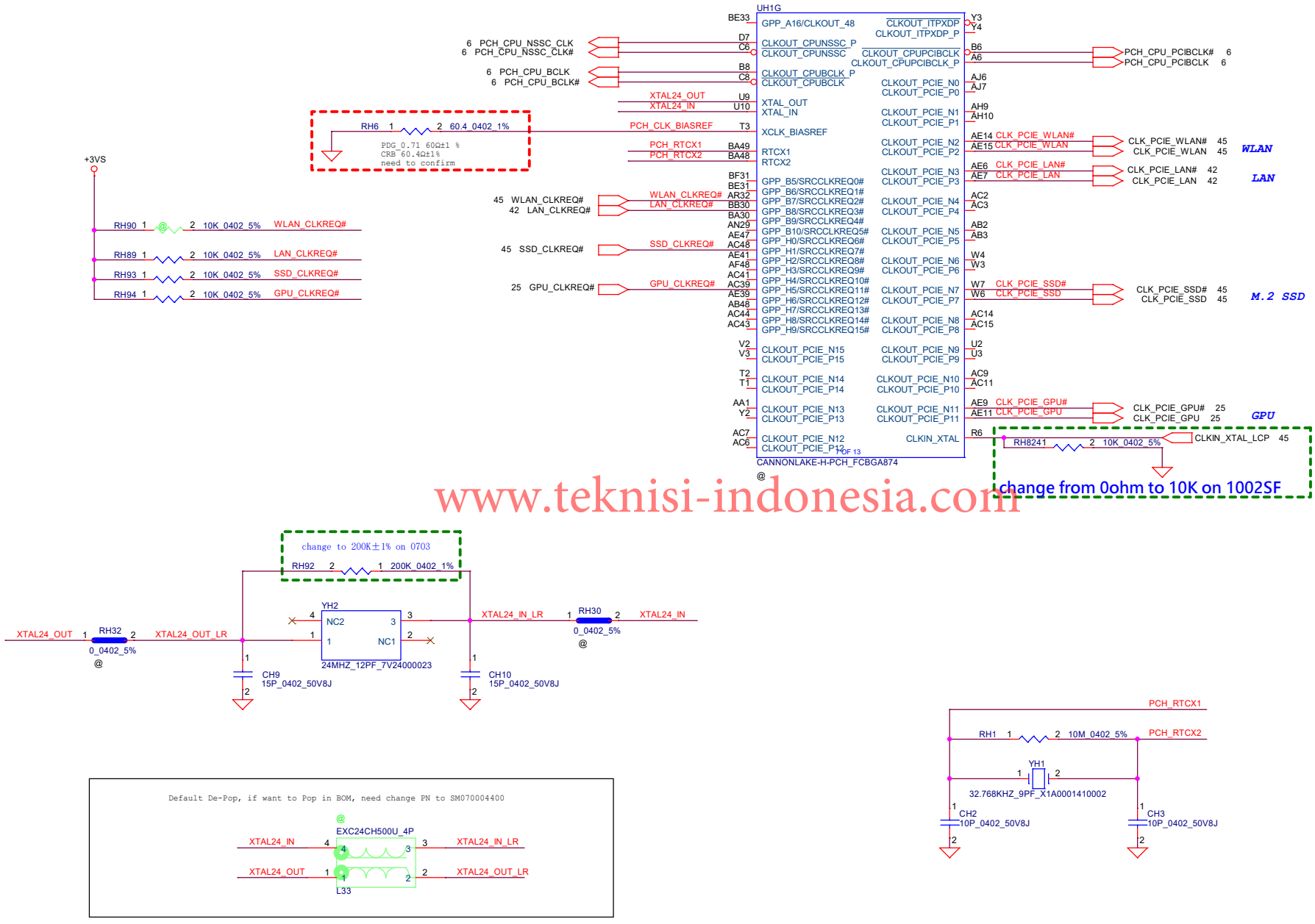

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2018/09/20

Title	PCH (3/9) CLOCK,GPPBH		
Size	Document Number		Rev
A3	FG541/FG741		1.0
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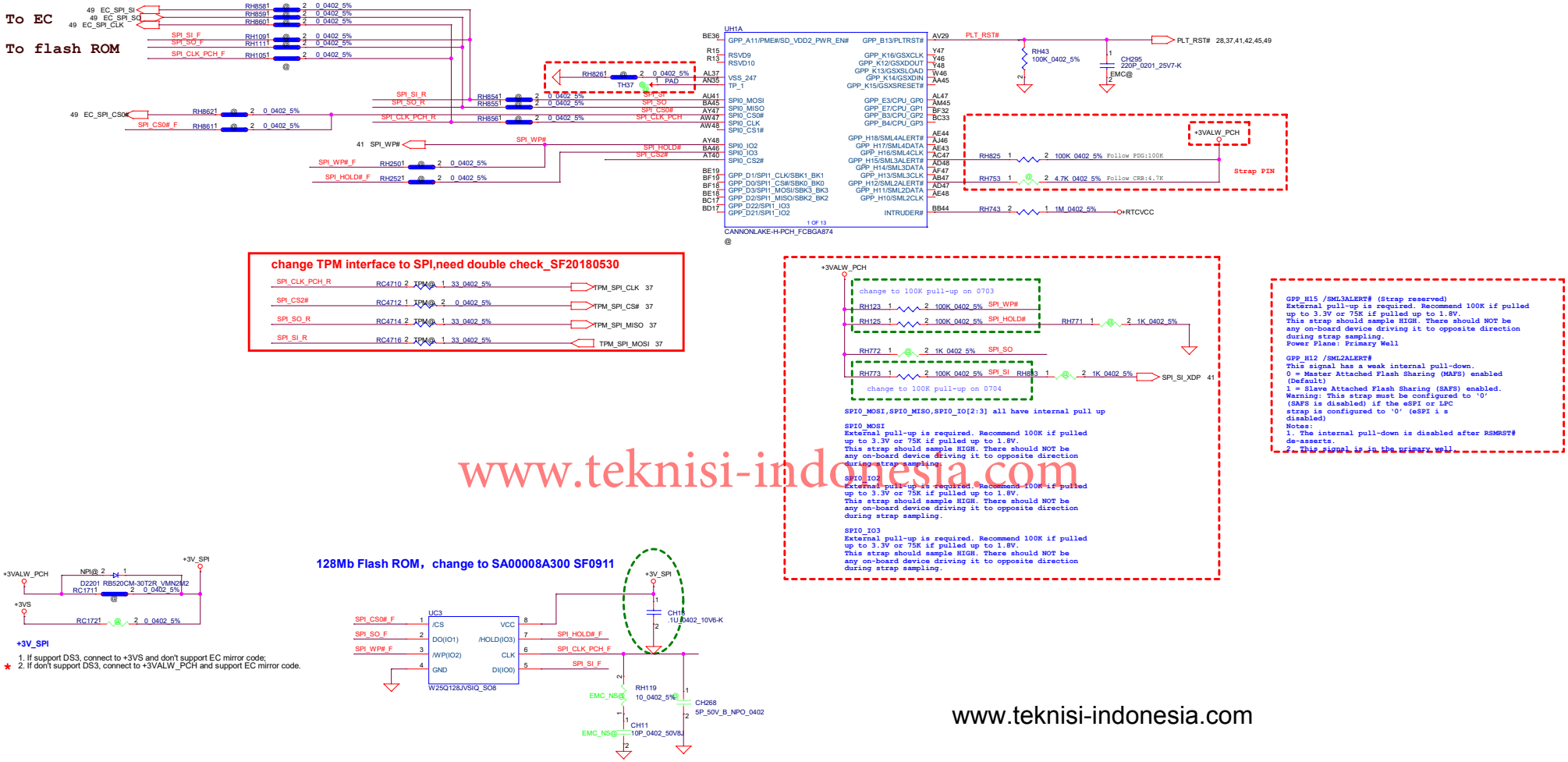

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2018/09/20

Title	PCH (5/9) SPI,SMBUS,GPPBEGH		
Size A2	Document Number FG541/FG741		Rev 1.0
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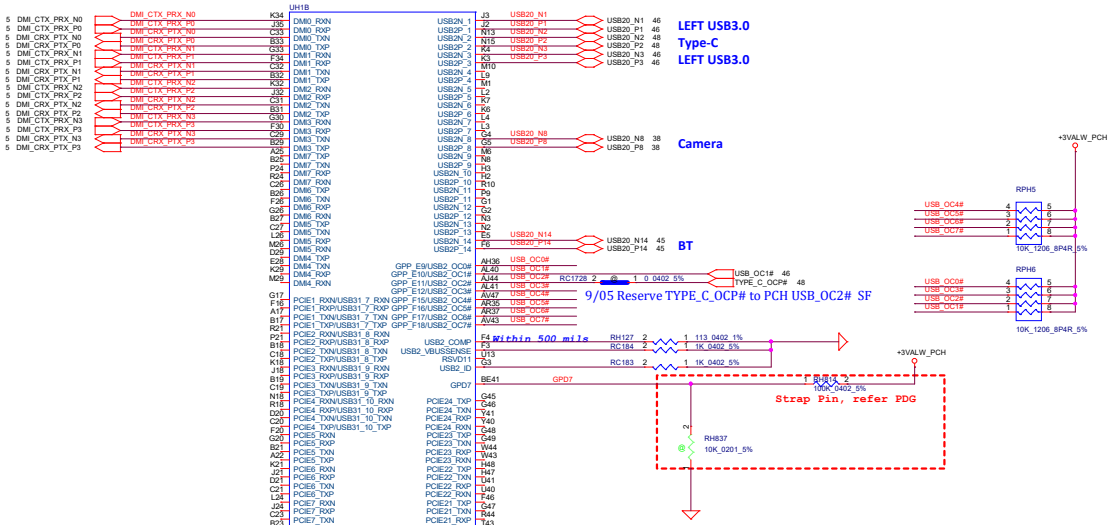

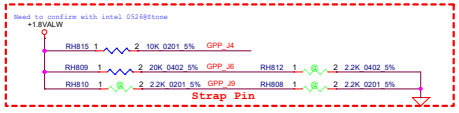

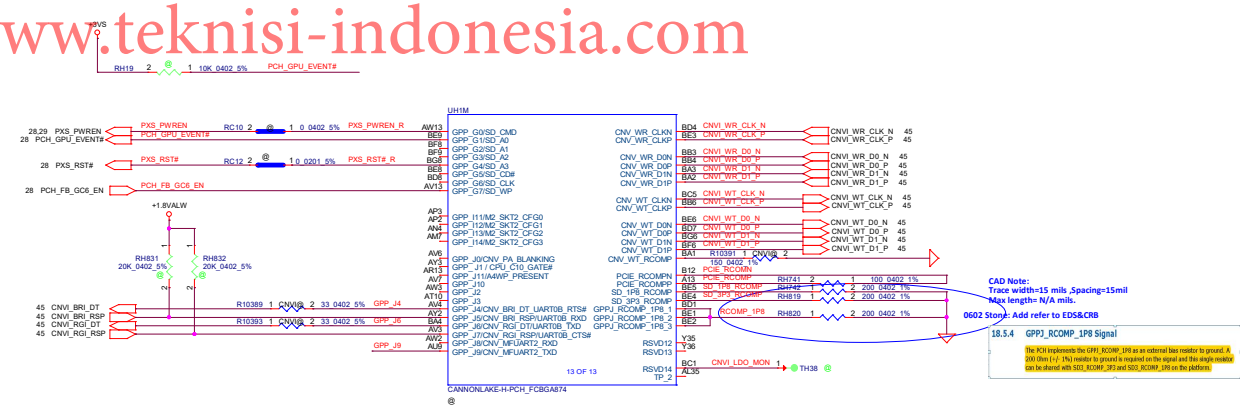

Primary Well Group J (1.8 V Only)

Signal	Usage	When Sampled	Comment
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCPSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail ***Note:*** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

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Issued Date	2015/02/26	Deciphered Date	2018/09/20

Title	Blank		
Size	Document Number		Rev
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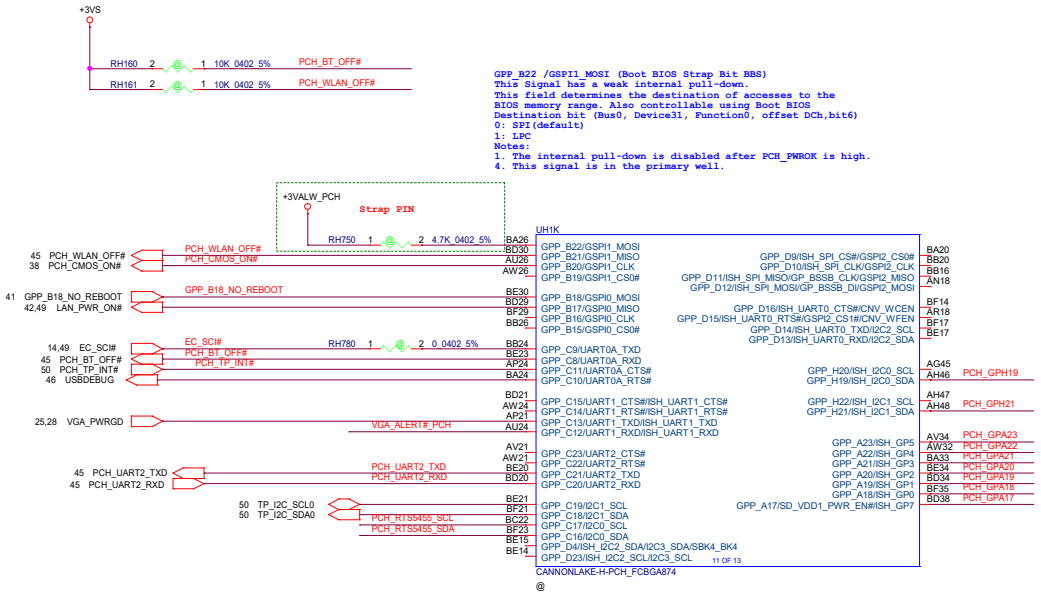
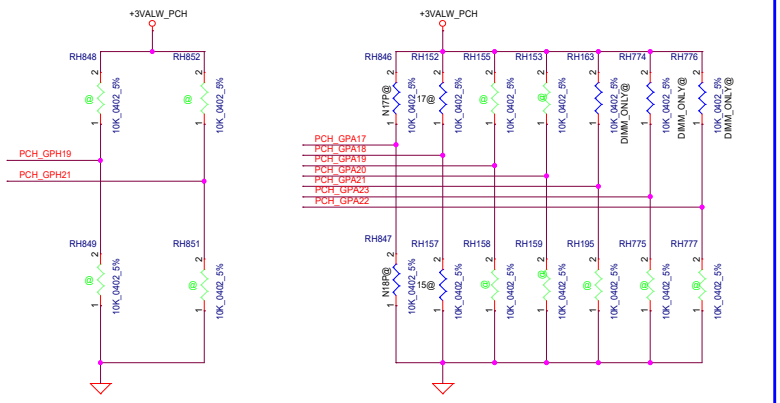
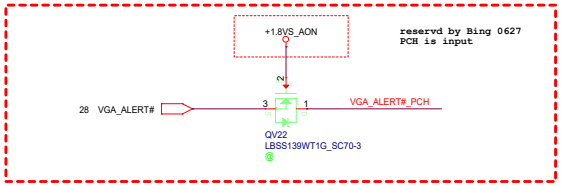
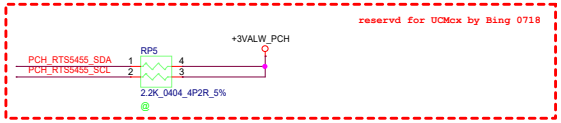


Bit 6	Boot BIOS Destination
0	SPI (Default)
1	LPC

Add Board ID reserve 1130SF







SKU ID

Board ID		Description	Stuff R
PCH_GPA18	0	15" EG530	RH157
	1	17" EG730	RH152
PCH_GPA19	0	Reserved	RH158
	1	Reserved	RH155
PCH_GPA20	0	non-KB BL	RH159
	1	KB BL	RH153
PCH_GPA17	0	Reserved	RH847
	1	Reserved	RH846
PCH_GPH19	0	Reserved	RH849
	1	Reserved	RH848
PCH_GPH21	0	Reserved	RH851
	1	Reserved	RH852

DRAM	Memory Down(DDR4)		DRAMCFG	PCH_GPA23	PCH_GPA22	PCH_GPA21
8Gb	Samsung 8Gb 2666 MT/s	K4A8G165WC-BCTD	0(0x000)	L/RH775	L/RH777	L/RH195
	Hynix 8Gb 2666 MT/s	H5AN8G6NCJR-VKC	1(0x001)	L/RH775	L/RH777	H/RH163
	Micron 8Gb 2666 MT/s	MT40A512M16LY-075:E	2(0x010)	L/RH775	H/RH776	L/RH195
	HT Micron 8Gb 2666 MT/s	HTH5AN8G6NAFR-VKD	3(0x011)	L/RH775	H/RH776	H/RH163
	Smart 8Gb 2666 MT/s	SDQC8G8W16XCTD9N1T	4(0x100)	H/RH774	L/RH777	L/RH195
			5(0x101)	H/RH774	L/RH777	H/RH163
			6(0x110)	H/RH774	H/RH776	L/RH195
	SODIMM only		7(0x111)	H/RH774	H/RH776	H/RH163

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Title: PCH (6/9) GPPPABCD, I2C

Size: C | Document Number: FG541/FG741 | Rev: 1.0

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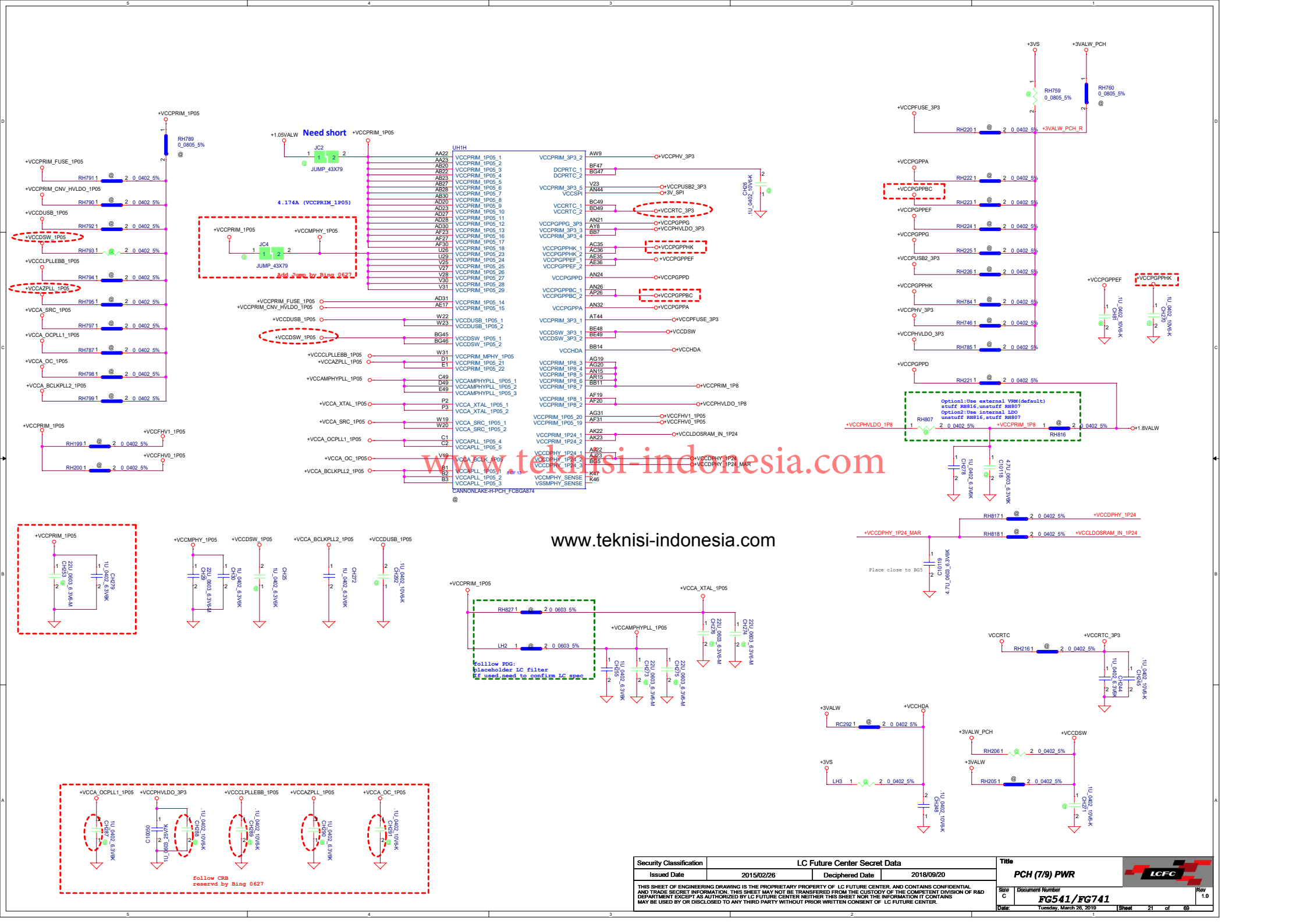

Title	PCH (7/9) PWR		
Size C	Document Number FG541/FG741		Rev 1.0
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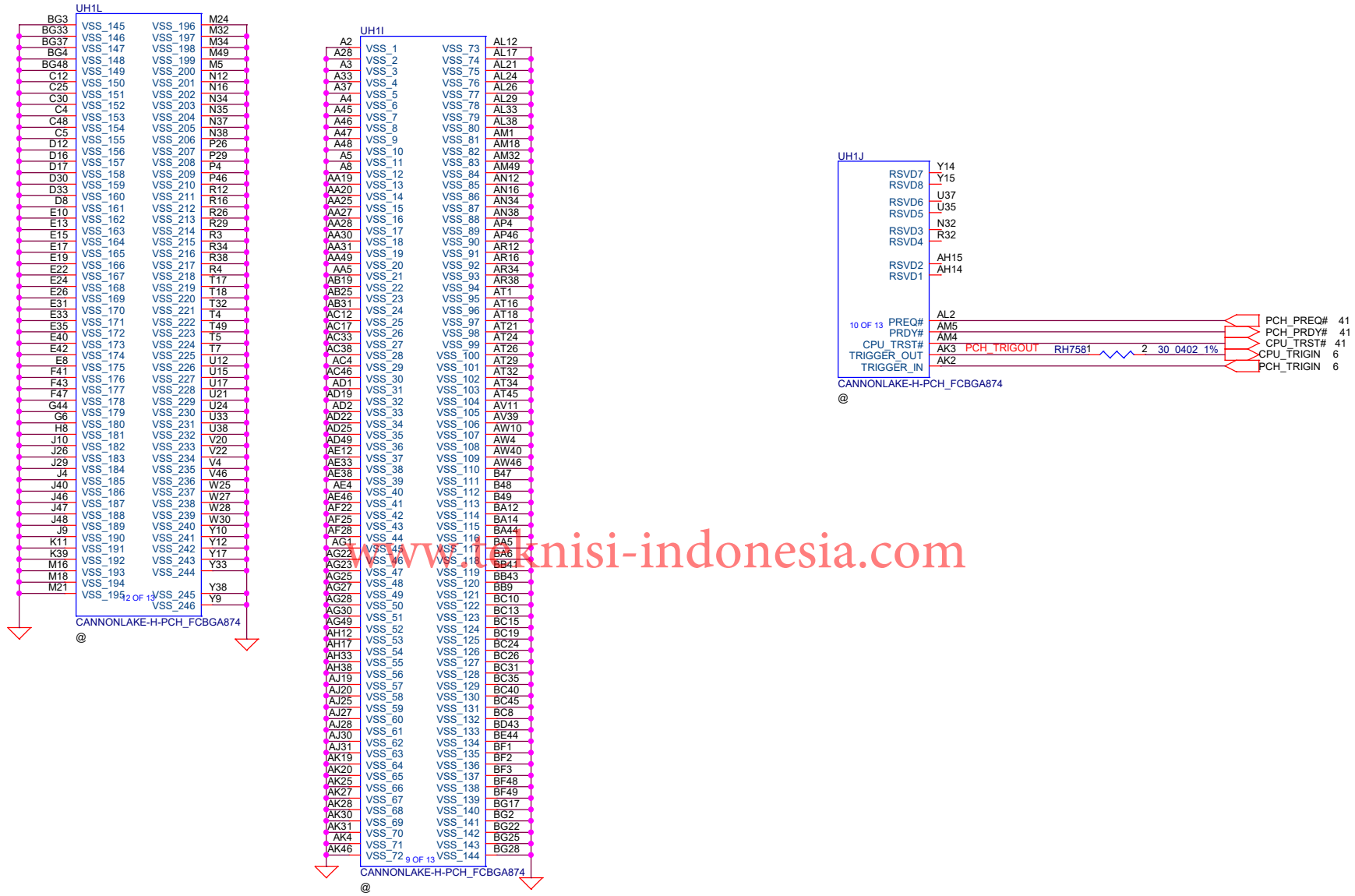

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Issued Date	2015/02/26	Deciphered Date	2018/09/20

Title: **PCH (9/9) VSS**

Size	Document Number	Rev
B	FG541/FG741	1.0

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Title: **Cover Page**

Size	Document Number	Rev
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N17P-G1 GPIO

GPIO	I/O	ACTIVE	Function Description	I/O Termination
GPIO0	OUT	-	PWM Output to control NVVDD	
GPIO1	OUT	-	FB Enable for GC6 2.1	
GPIO2	IN	-	GPU wake signal for GC6 2.1	
GPIO3	OUT	-	PWM Output to control the SRAM power supply	
GPIO4	OUT	-	GPU power sequencing for GC6 2.1 --- 1V8_MAIN_EN	
GPIO5	IN	N/A	Active low Frame Lock	
GPIO6	OUT	-	Phase Shedding, NVVDD_PSI	
GPIO7	OUT	N/A	Panel Backlight enable	
GPIO8	OUT	-	Memory voltage Control	
GPIO9	I/O	-	Active Low Thermal Alert	
GPIO10	OUT	-	Memory VREF Control (100K pull Down)	
GPIO11	OUT	-	Panel Power enable	
GPIO12	IN	-	AC power detect or power supply overdraw input	(10K pull High)
GPIO13	OUT	N/A	LCD Panel Backlight Enable	
GPIO14	IN	N/A	Hot Plug Detect for IFPA	
GPIO15	IN	N/A	Hot Plug Detect for IFPB	
GPIO16	OUT	-	System side PCIe reset monitor	
GPIO17	IN	N/A	Hot Plug Detect for IFPD	
GPIO18	IN	N/A	Hot Plug Detect for IFPE	
GPIO19	OUT	N/A	3D Vision L/R Signal	
GPIO20		N/A	GC5_MODE	
GPIO21	I/O	N/A	UNUSED	
GPIO22	I/O	N/A	UNUSED	
GPIO23	OUT	-	GPU PCIe self-reset control	
GPIO24	IN	N/A	Hot Plug Detect for IFPF	
GPIO25		N/A	UNUSED	
GPIO26		N/A	UNUSED	
GPIO27	IN	N/A	Hot Plug Detect for IFPC	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	1111 DEFAULT
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

1:ENABLE 0:DISABLE

SOR0/1/2/3 ENABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

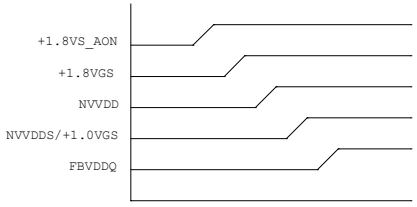
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

N17P-G1 Power Sequence

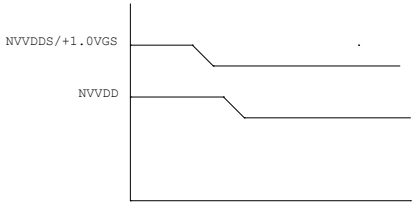


1. All power rail ramp up time should be larger than 40us and is recommended to be less than 2ms.

2. T (from 1V8_MAIN_EN to PEX_DVDD/NVVDD_Pgood) must NOT exceed 4ms.

3. All 3.3V devices that connect to the GPU must be powered after 1V8_AON; GPU can NOT have any 3.3V leakage path before 1V8_AON present.

4. The previous power rail must ramp up to 90% before the next power rail can start ramping up.



1. NVVDDS/PEX_DVDD must ramp down before NVVDD, all other power rails can ramp down together with NVVDD.

2. All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1V8_AON and 1.8V_MAIN power down.

3. The previous power rail must ramp down to 10% before the next power rail can start ramping down.

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Title: VGA Notes List

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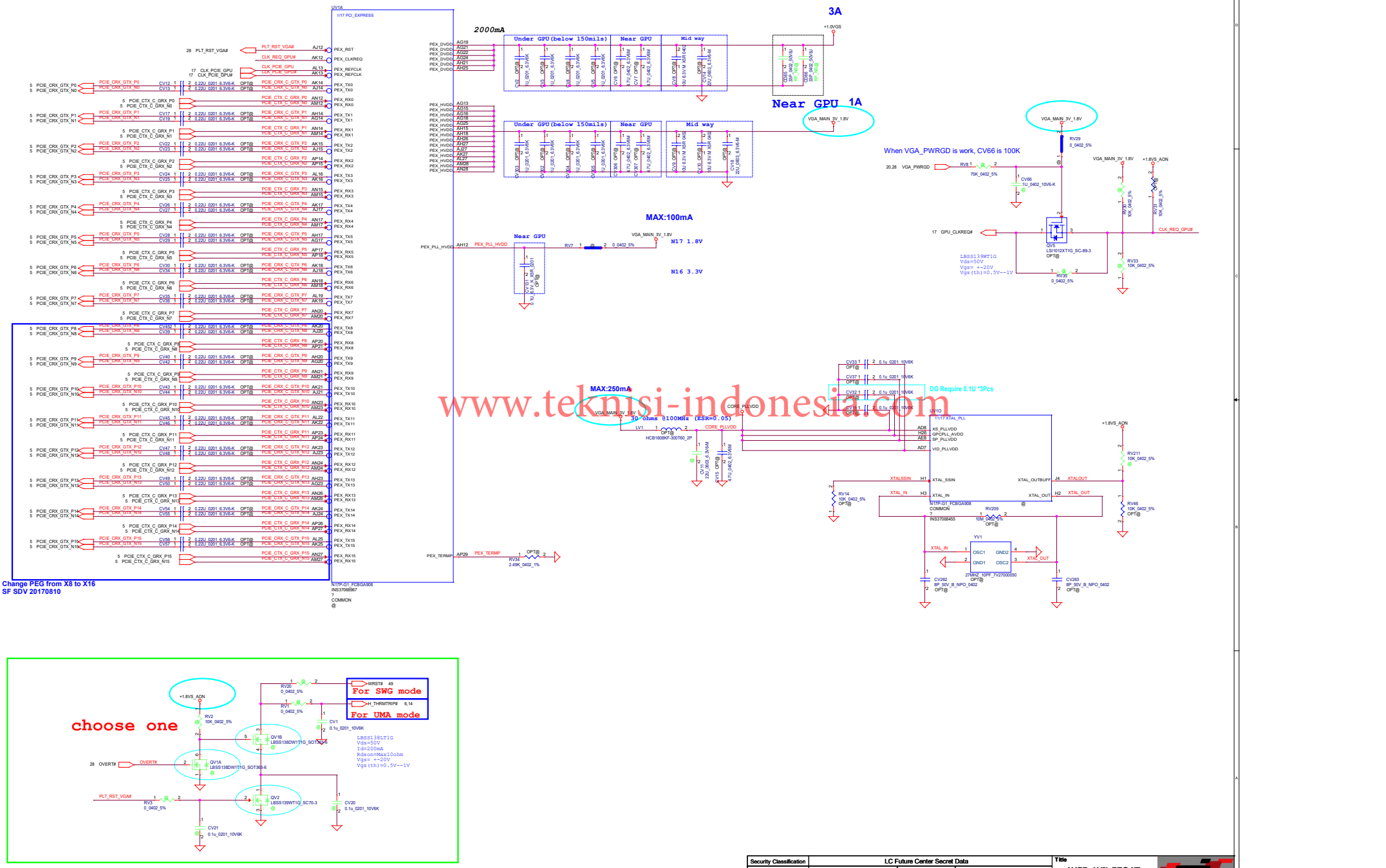

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Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	N17P_(1/6):PEG I/F		
Size: Custom	Document Number: FG541/FG741		Rev: 1.0
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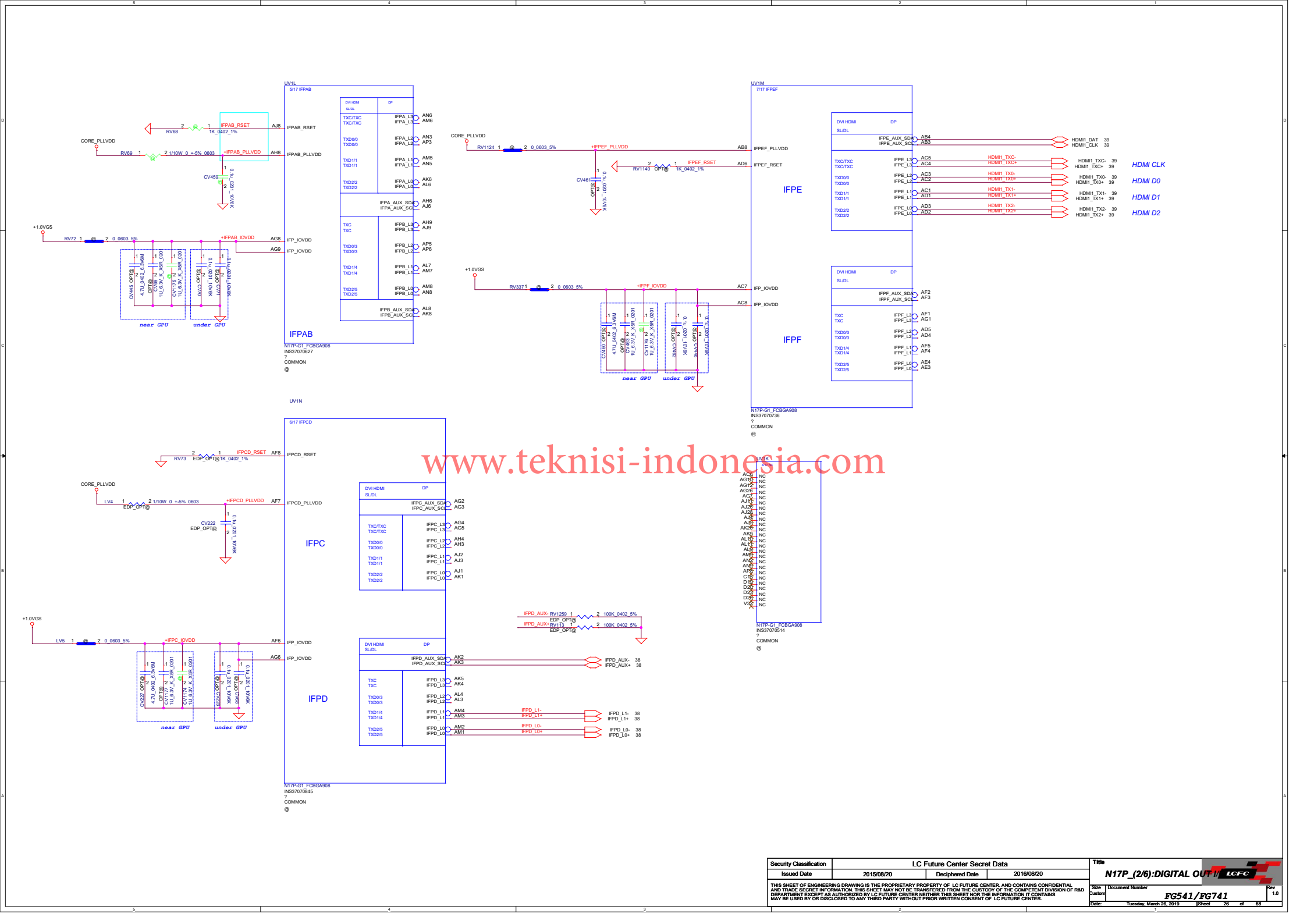

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Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	N17P_(2/6):DIGITAL OUT		
Size: Custom	Document Number: FG541/FG741		Rev: 1.0
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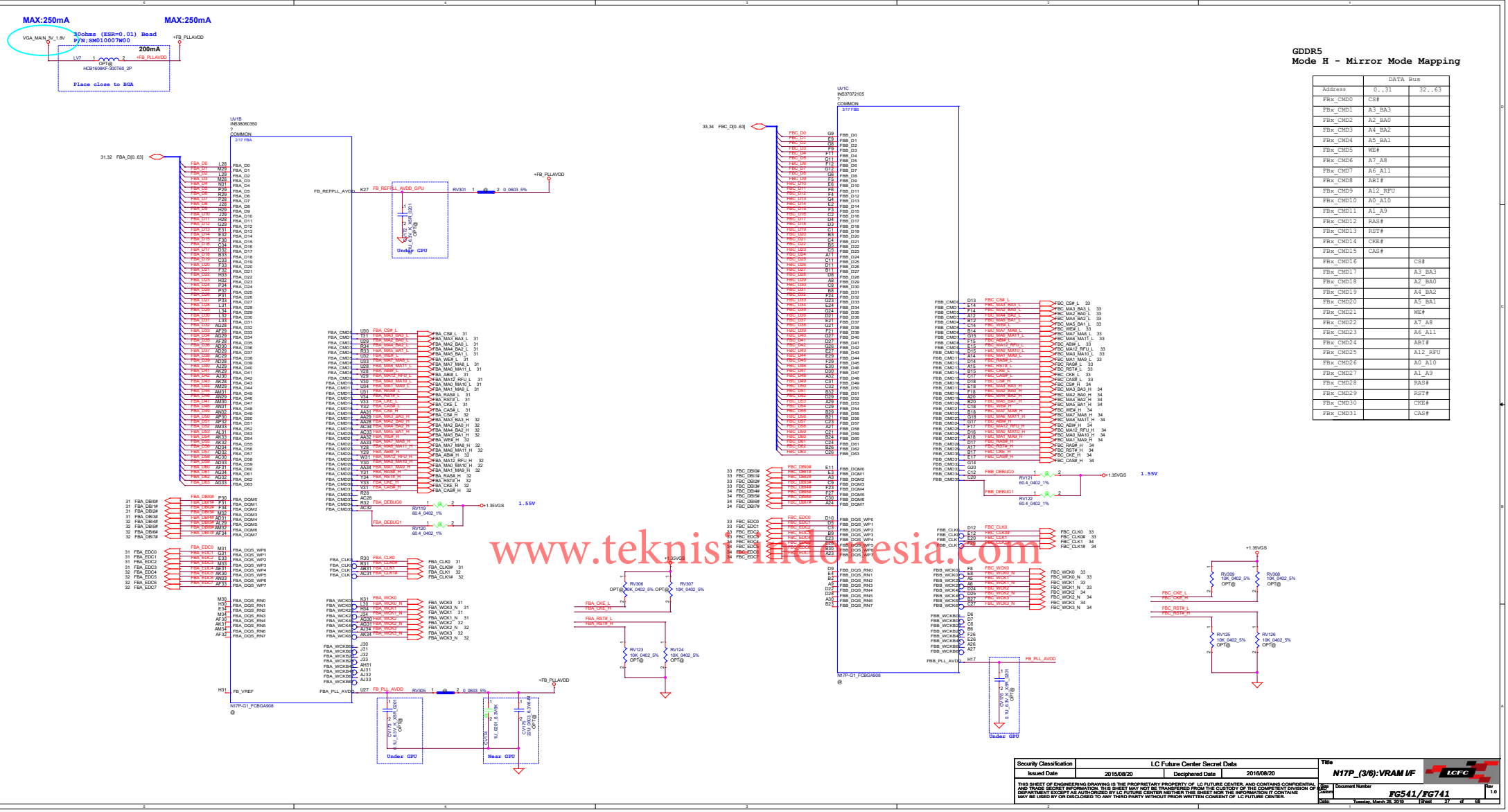
MAX:250mA
MAX:250mA
VGA_MAIN_3V_1.8V
30ohms (ESR=0.01) Bead
P/N:SM010007W00
200mA
+FB_PLLAVDD
LV7
OPT@
HCB1608KF-300T60_2P
Place close to BGA
GDDR5
Mode H - Mirror Mode Mapping
DATA Bus
Address
0..31
32..63
FBx_CMD0 CS#
FBx_CMD1 A3_BA3
FBx_CMD2 A2_BA0
FBx_CMD3 A4_BA2
FBx_CMD4 A5_BA1
FBx_CMD5 WE#
FBx_CMD6 A7_A8
FBx_CMD7 A6_A11
FBx_CMD8 ABI#
FBx_CMD9 A12_RFU
FBx_CMD10 A0_A10
FBx_CMD11 A1_A9
FBx_CMD12 RAS#
FBx_CMD13 RST#
FBx_CMD14 CKE#
FBx_CMD15 CAS#
FBx_CMD16 CS#
FBx_CMD17 A3_BA3
FBx_CMD18 A2_BA0
FBx_CMD19 A4_BA2
FBx_CMD20 A5_BA1
FBx_CMD21 WE#
FBx_CMD22 A7_A8
FBx_CMD23 A6_A11
FBx_CMD24 ABI#
FBx_CMD25 A12_RFU
FBx_CMD26 A0_A10
FBx_CMD27 A1_A9
FBx_CMD28 RAS#
FBx_CMD29 RST#
FBx_CMD30 CKE#
FBx_CMD31 CAS#
UV1B
INS38060350
COMMON
2/17 FBA
UV1C
INS37072105
COMMON
3/17 FBB
N17P-G1_FCBGA908
Under GPU
Near GPU
+1.35VGS
1.55V
+FB_PLLAVDD
FB_PLL_AVDD
FB_VREF
FB_REFPLL_AVDD_GPU
RV306
RV307
RV123
RV124
RV309
RV308
RV125
RV126
10K_0402_5%
OPT@
www.teknisi-indonesia.com
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N17P_(3/6):VRAM I/F
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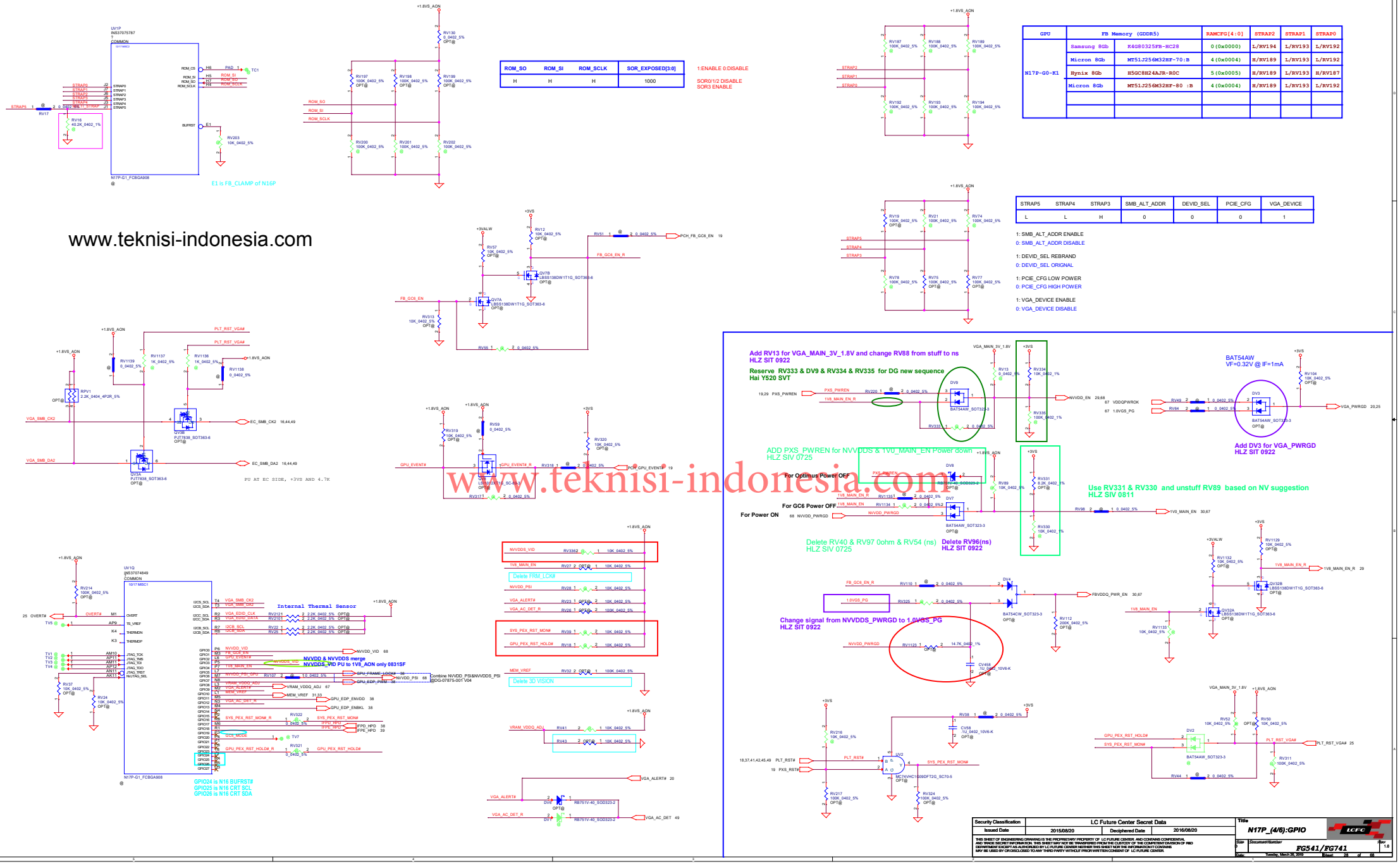

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
H	H	H	1000

1:ENABLE 0:DISABLE

SOR0/1/2 DISABLE
SOR3 ENABLE

GPU	FB Memory (GDDR5)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
N17P-G0-K1	Samsung 8Gb	K4G80325FB-HC28	0 (0x0000)	L/RV194	L/RV193	L/RV192
	Micron 8Gb	MT51J256M32HF-70:B	4 (0x0004)	H/RV189	L/RV193	L/RV192
	Hynix 8Gb	H5GC8H24AJR-R0C	5 (0x0005)	H/RV189	L/RV193	H/RV187
	Micron 8Gb	MT51J256M32HF-80 :B	4 (0x0004)	H/RV189	L/RV193	L/RV192

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	H	0	0	0	1

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE

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Title: N17P_(4/6):GPIO

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5A Peak 8A

Under GPU(below 150mils)

Cost down list:
1U 3Pcs

Under GPU(below 150mils)

Near GPU

Near GPU

1.8V Total 1A (AON+MAIN)

0.5A

Under GPU

Near GPU

0.5A

Under GPU

Near GPU

NVVDD & NVVDDS merge test point only 0831SF

trace width: 16mils
differential voltage sensing.
differential signal routing.

CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm

Place near balls

PLACE MIDWAY BETWEEN FBA AND FBB

19A Peak 42A

Cost down list:
4.7U 1Pcs
1U 1Pcs

POSCAP

Near GPU

Under GPU

Follow NV suggestion for NVVDDS Hai Y520 SVT

Add +1.8V-AON discharger circuit HLZ SIV 0811

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Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: N17P_(5/6):PWR

Size: Custom | Document Number: FG541/FG741 | Rev: 1.0

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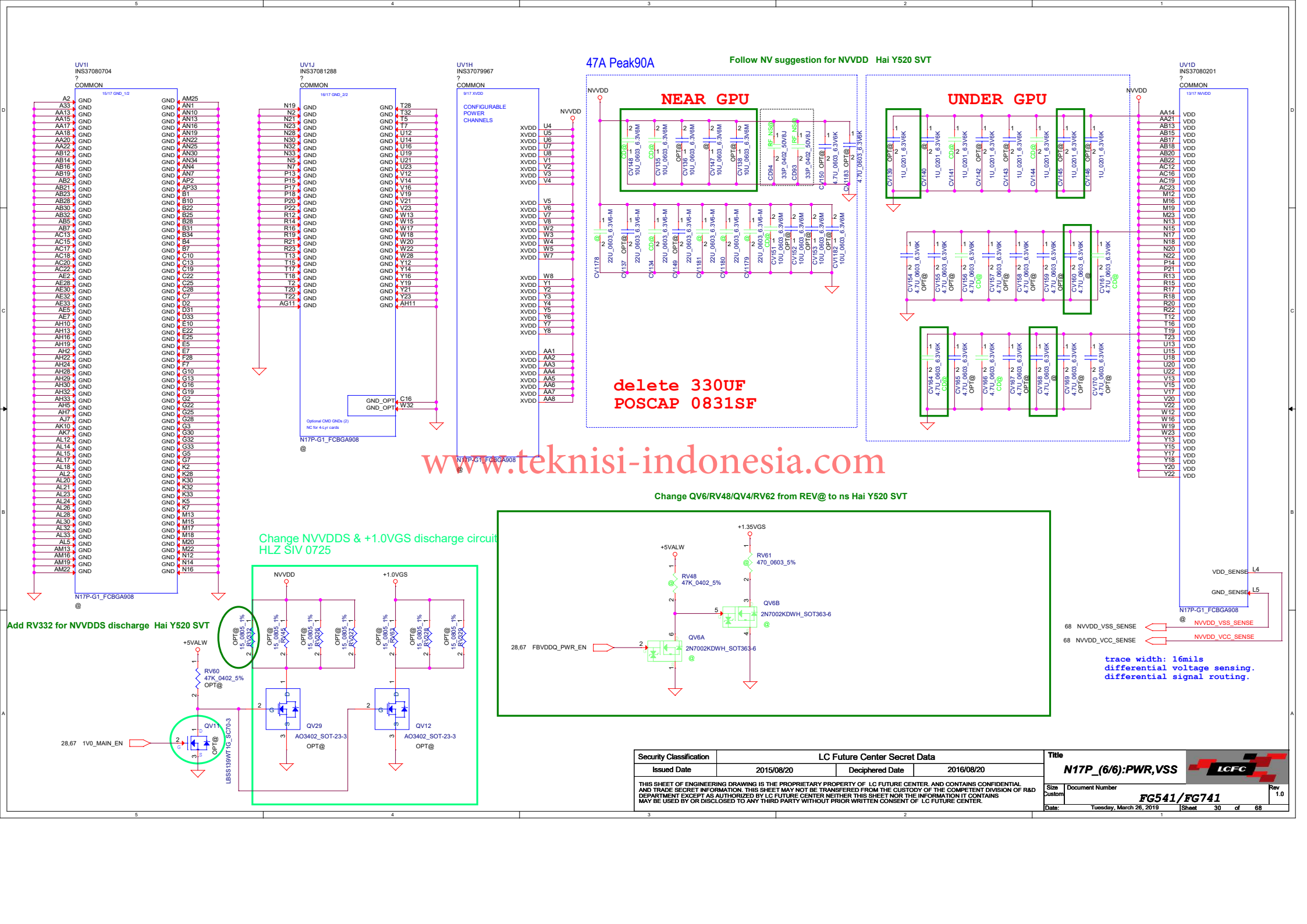
47A Peak90A
Follow NV suggestion for NVVDD Hai Y520 SVT
NEAR GPU
UNDER GPU
delete 330UF
POSCAP 0831SF
www.teknisi-indonesia.com
Change NVVDDS & +1.0VGS discharge circuit
HLZ SIV 0725
Add RV332 for NVVDDS discharge Hai Y520 SVT
Change QV6/RV48/QV4/RV62 from REV@ to ns Hai Y520 SVT
trace width: 16mils
differential voltage sensing.
differential signal routing.
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2015/08/20
Deciphered Date
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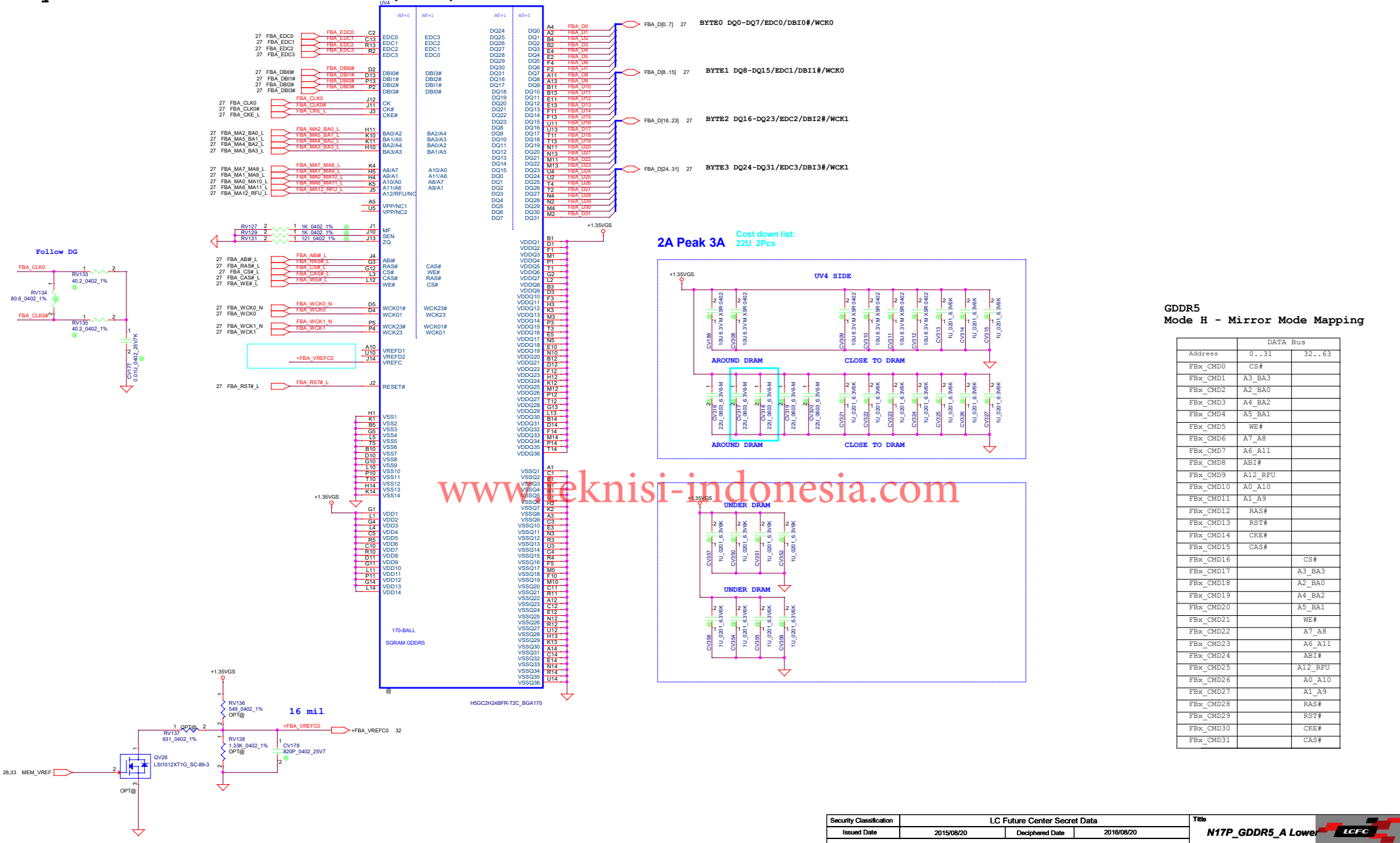
Memory Partition A - Lower 64 bits(MF=0)



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Title: N17P_GDDR5_A Lower
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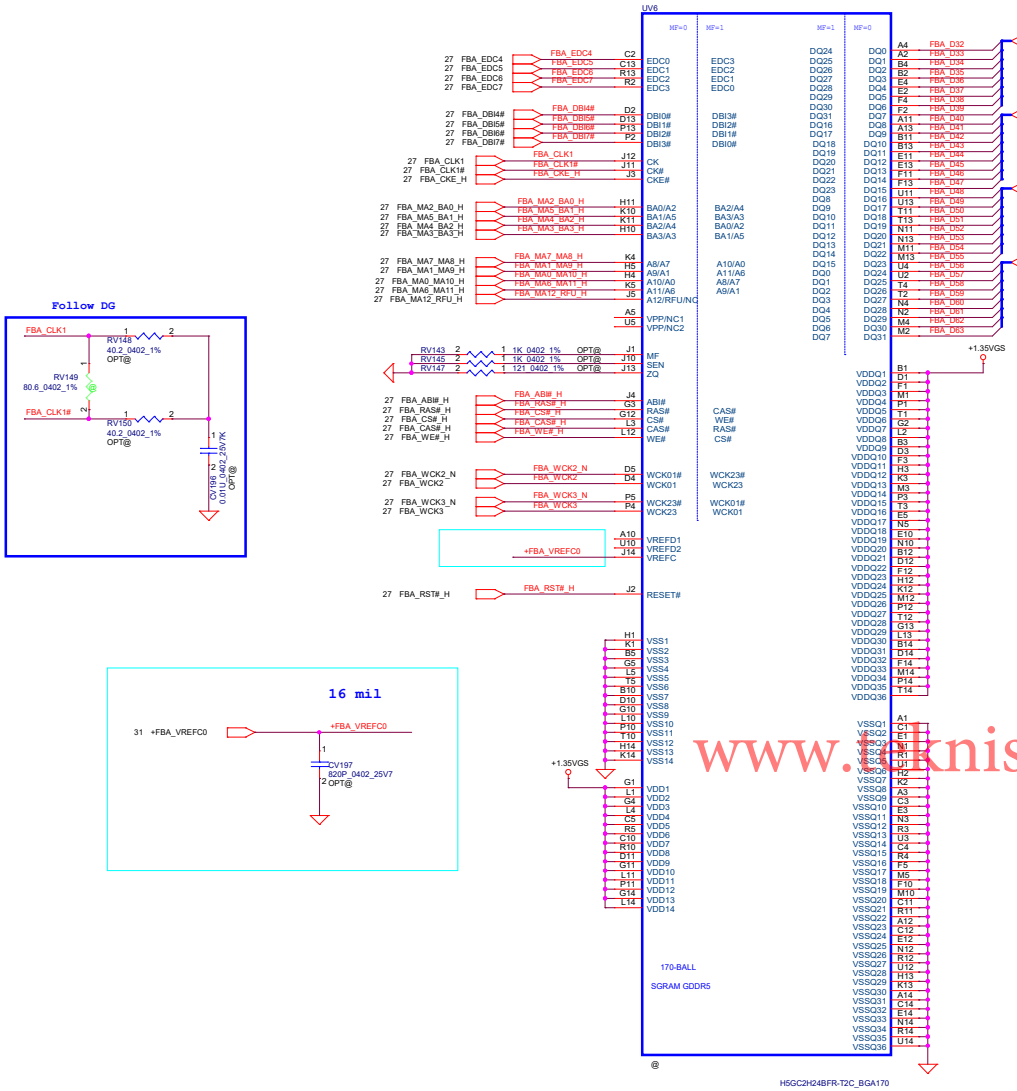
Memory Partition A- Upper 64 bits(MF=0)



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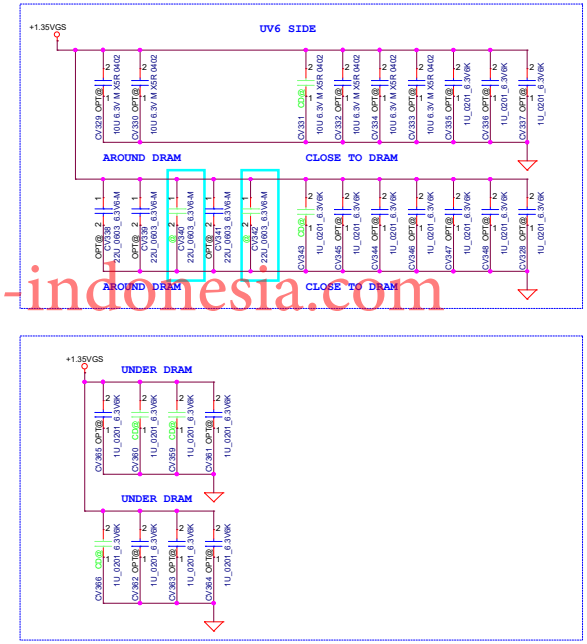
2A Peak 3A

Cost down list:
22U 2Pcs



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

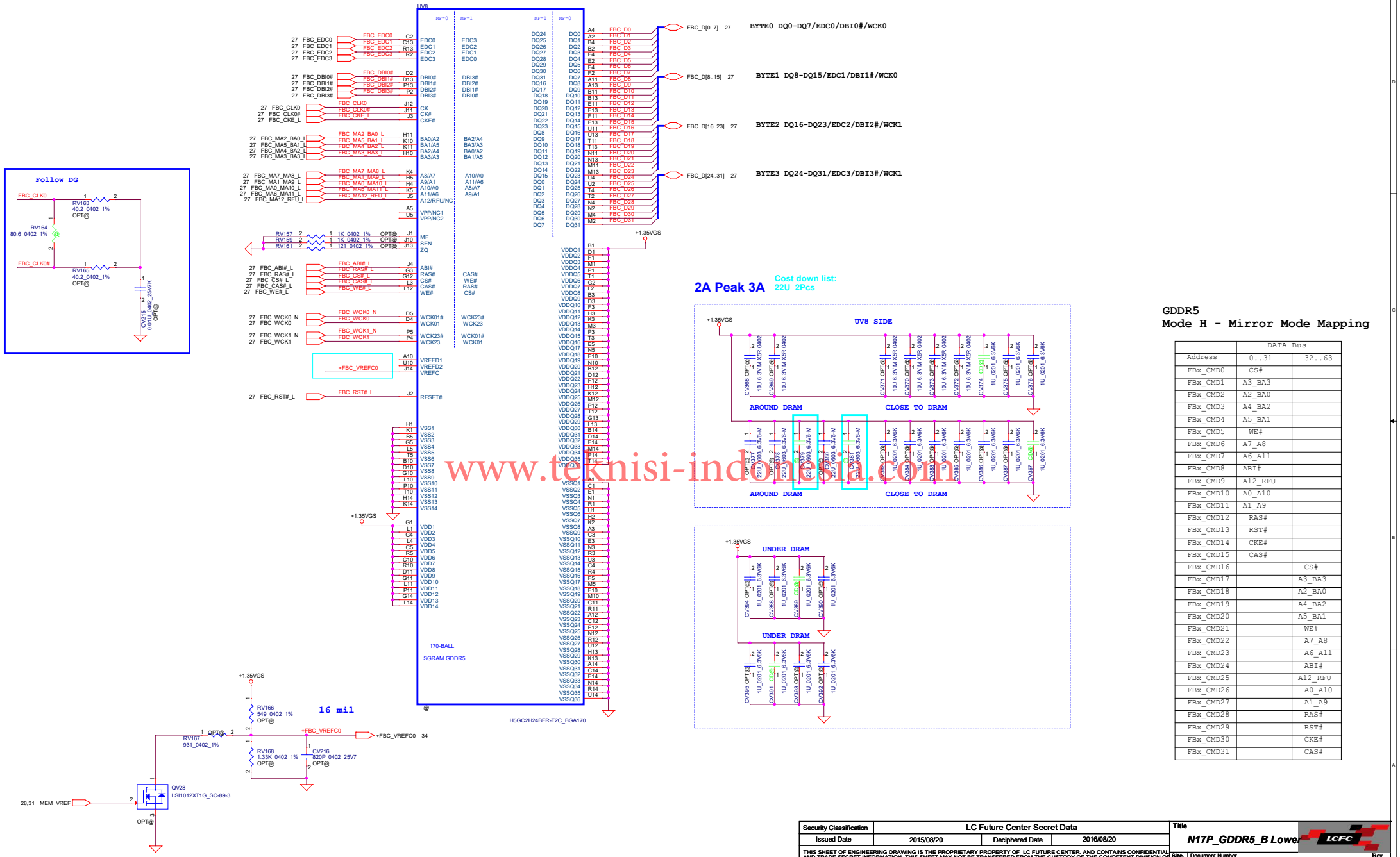
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: N17P_GDDR5_A Upper

Size: Custom | Document Number: FG541/FG741 | Rev: 1.0

Date: Tuesday, March 26, 2019 | Sheet 32 of 68

Memory Partition B - Lower 32 bits(MF=0)



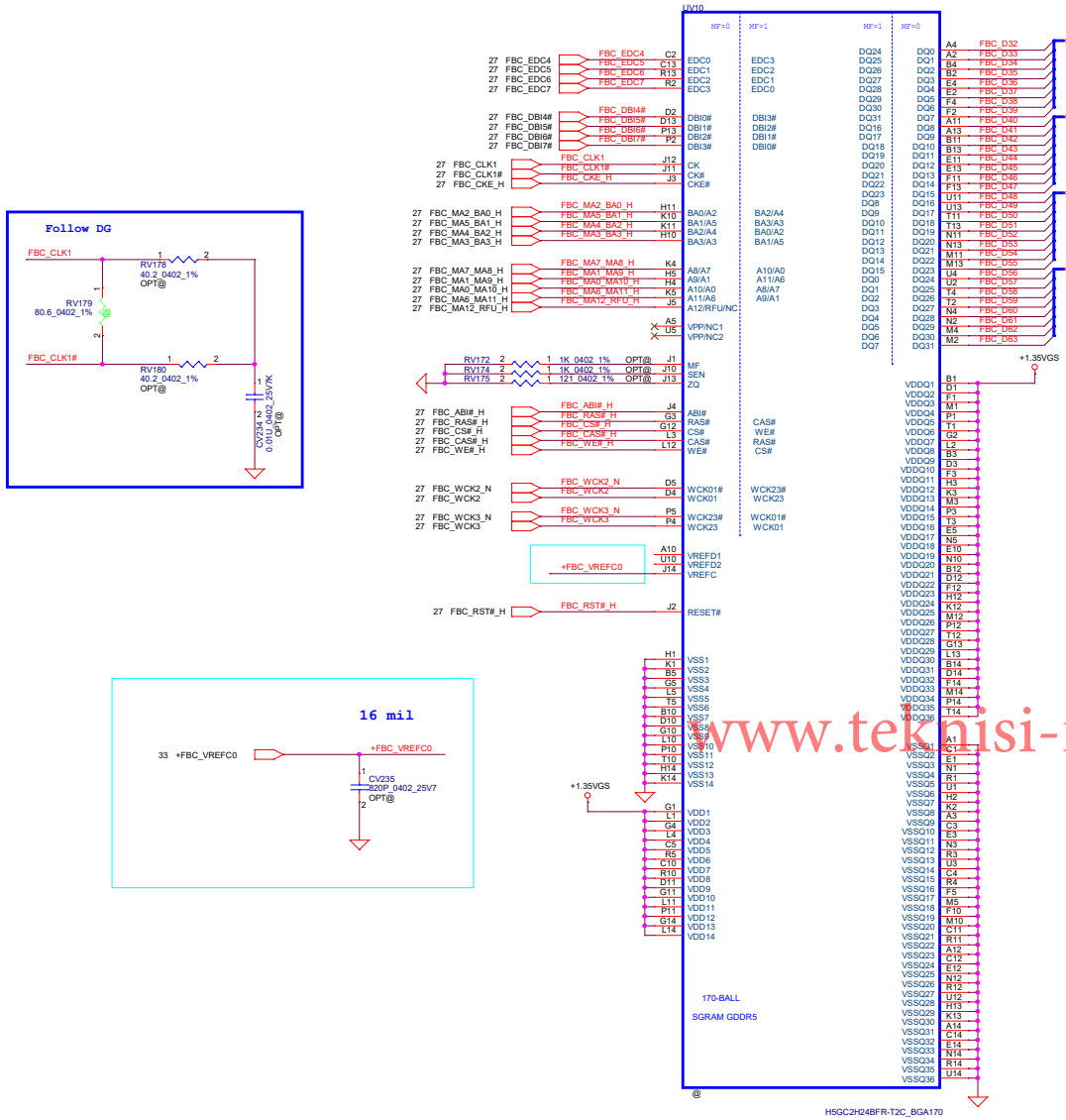
GDDR5
Mode H - Mirror Mode Mapping

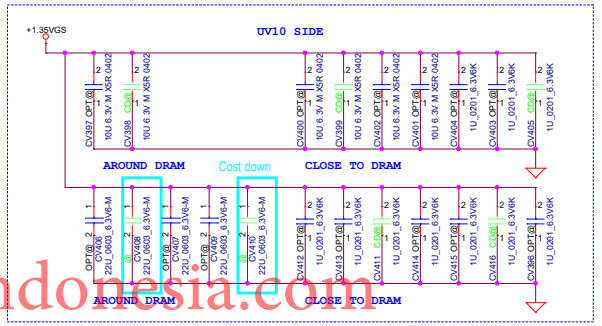
	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	N17P_GDDR5_B Lower		
Size: Custom	Document Number: FG541/FG741		Rev: 1.0
Date: Tuesday, March 26, 2019	Sheet 33 of 68		

Memory Partition B - Upper 32 bits(MF=0)





GDDR5
Mode H - Mirror Mode Mapping

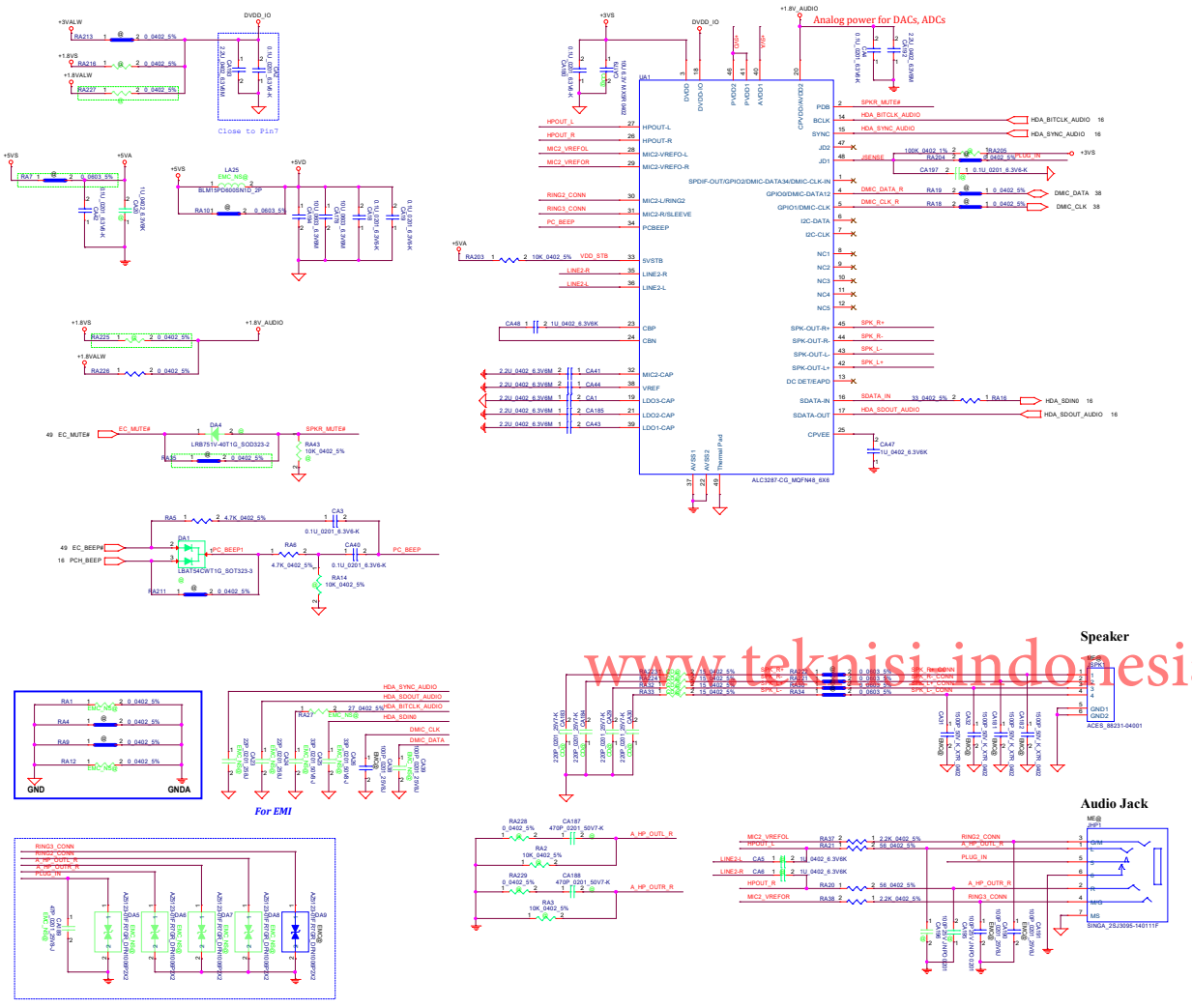
	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: N17P_GDDR5_B Upper

Size: Custom | Document Number: FG541/FG741 | Rev: 1.0

Date: Tuesday, March 26, 2019 | Sheet 34 of 68



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/09/20

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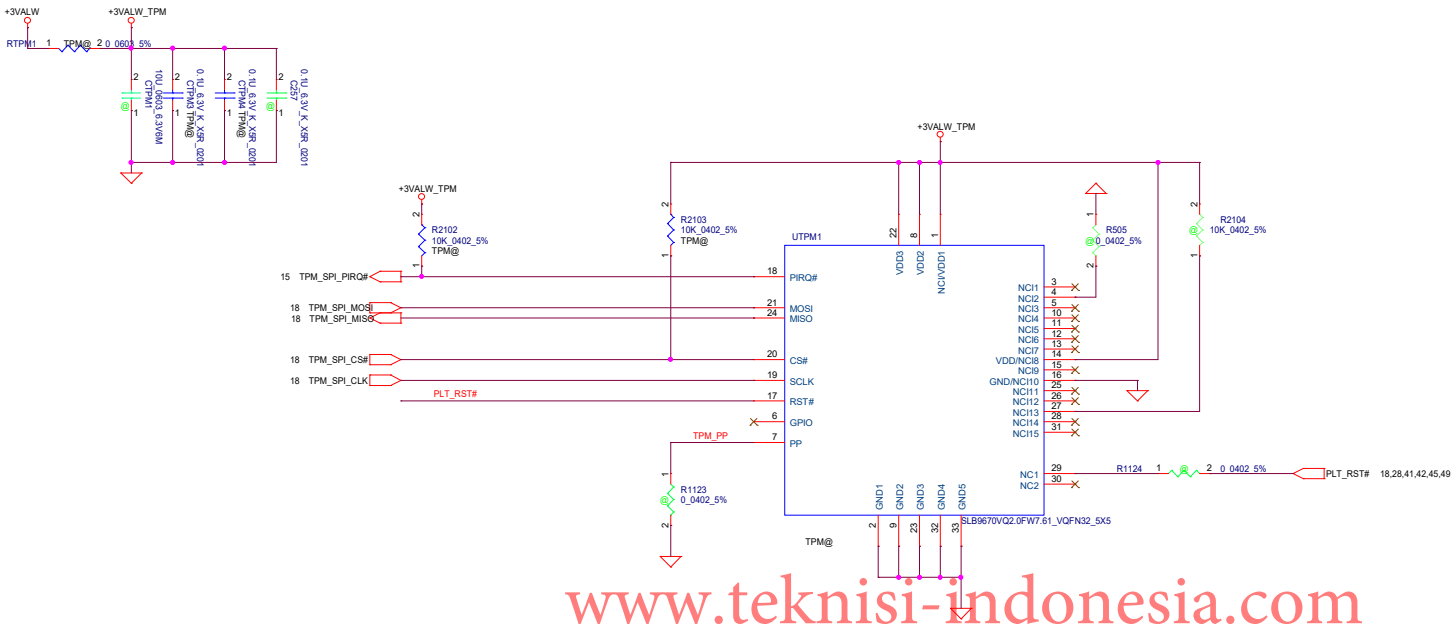
Title	Codec & CR_RTS5199		
Size	Document Number		Rev
D	FG541/FG741		1.0
Date:	Tuesday, March 26, 2019	Sheet 35 of 69	

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

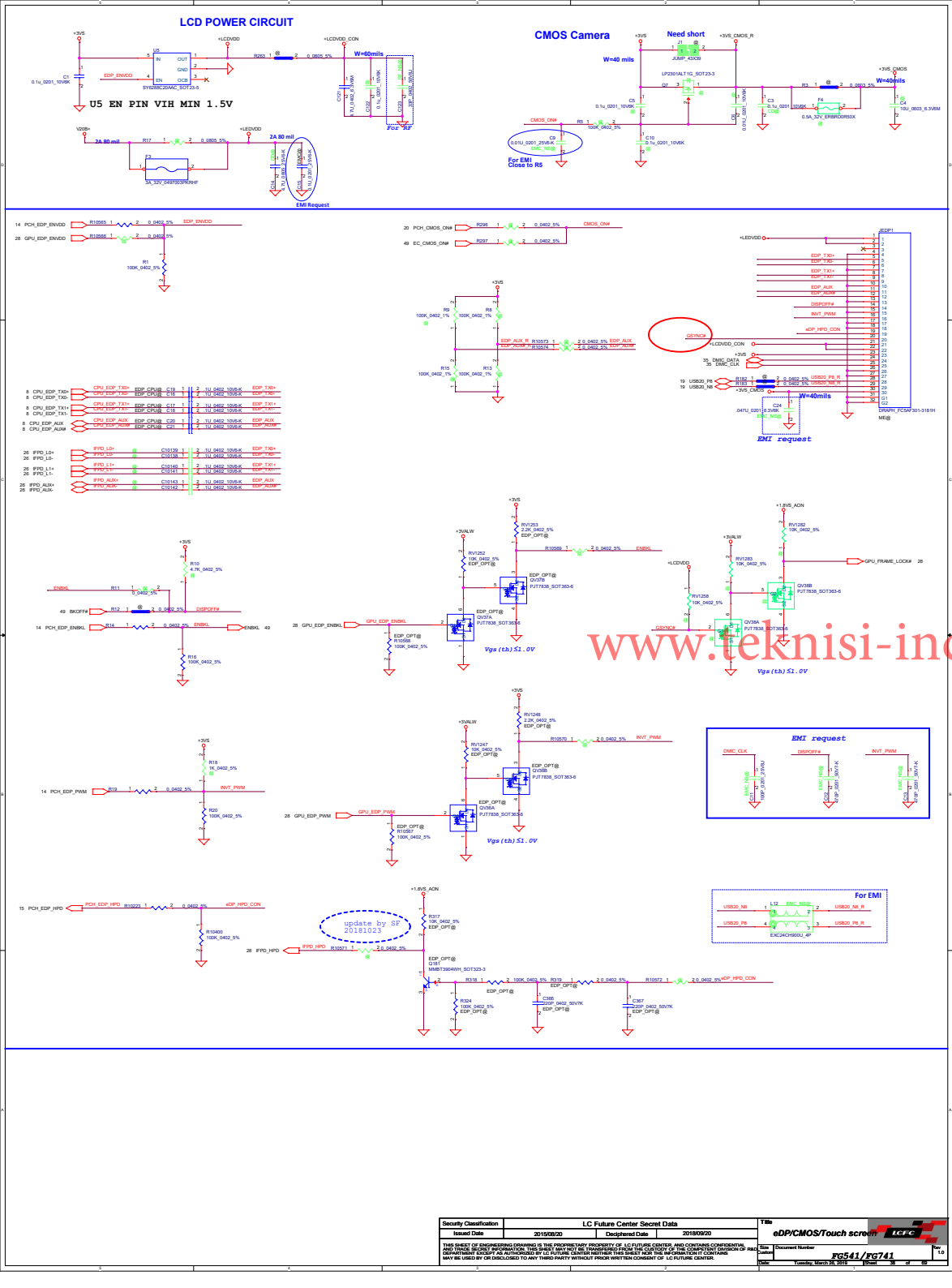
Title: *Cardreader*

Size: Custom	Document Number: FG541/FG741	Rev: 1.0
Date: Tuesday, March 26, 2019	Sheet 36 of 69	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title	TPM		
Size	Document Number		Rev
C	FG541/FG741		1.0
Date:	Tuesday, March 26, 2019	Sheet	37 of 69



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

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Title: eDP/CMOS/Touch screen

Size	Document Number	Rev
Custom	FG541/FG741	1.0

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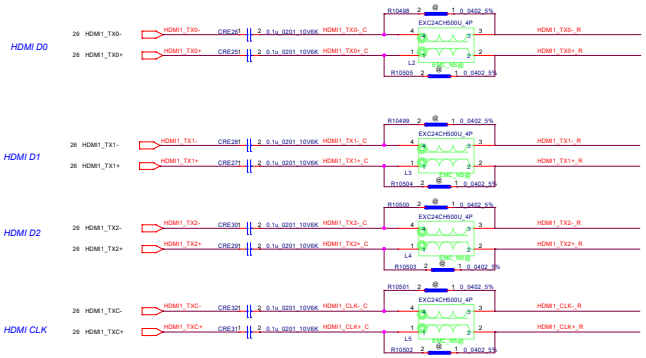

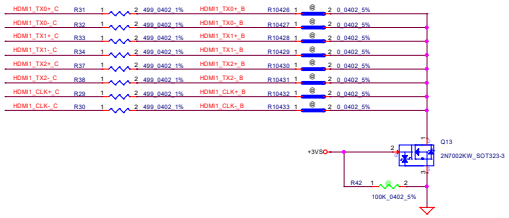

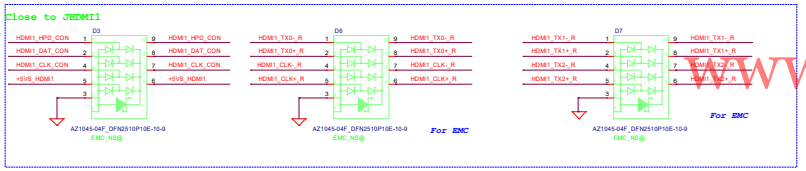

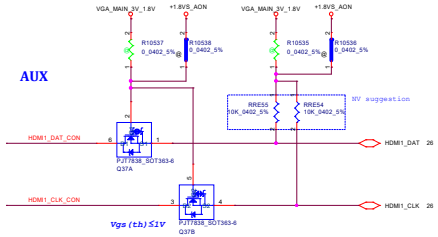

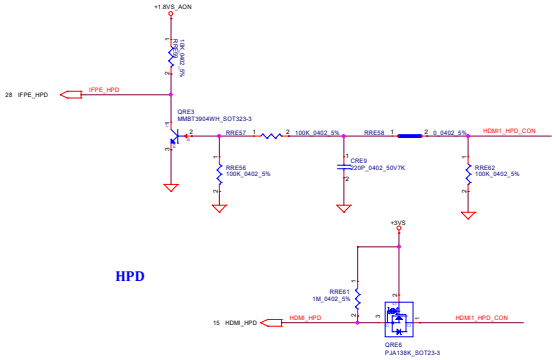

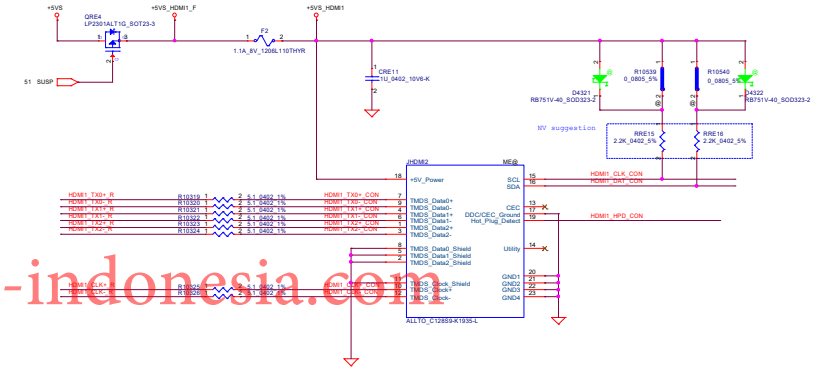

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/09/20

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Title: HDMI_CONN

Size: D | Document Number: FG541/FG741 | Rev: 1.0

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title: **P35-Blank**

Size: Custom	Document Number: FG541/FG741	Rev: 1.0
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TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

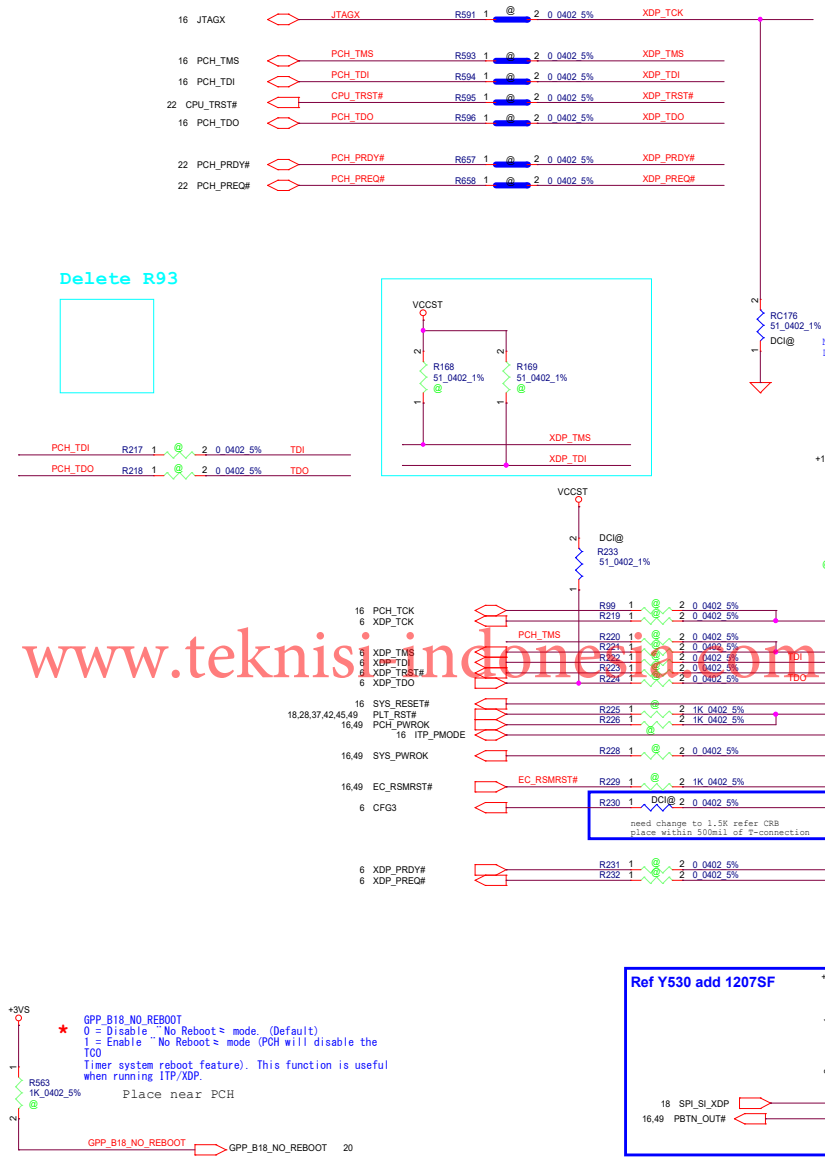
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title: **Blank**

Size	Document Number	Rev
C	FG541/FG741	1.0

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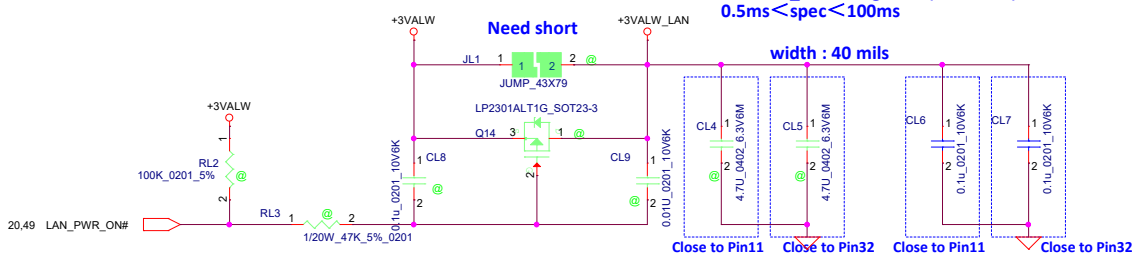
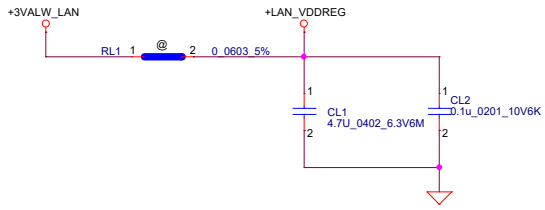
+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
0.5ms＜spec＜100ms

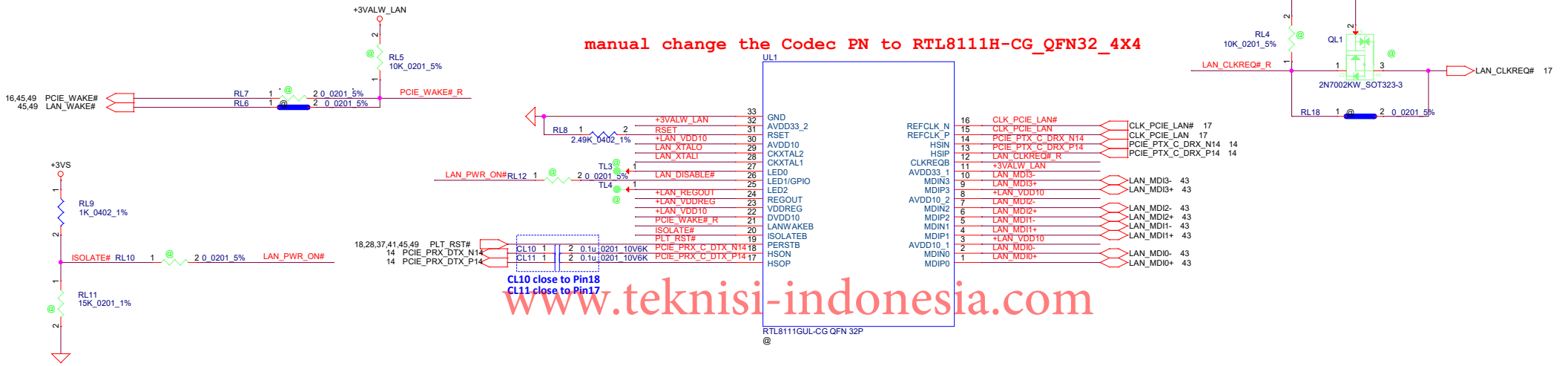
Need short

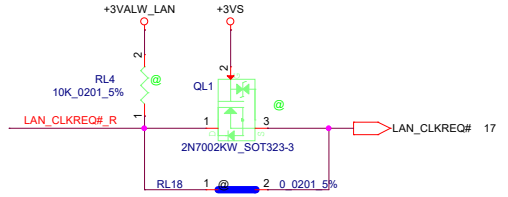
width : 40 mils

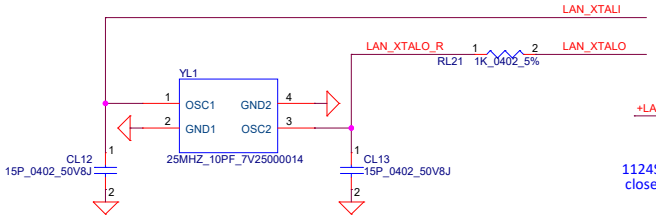


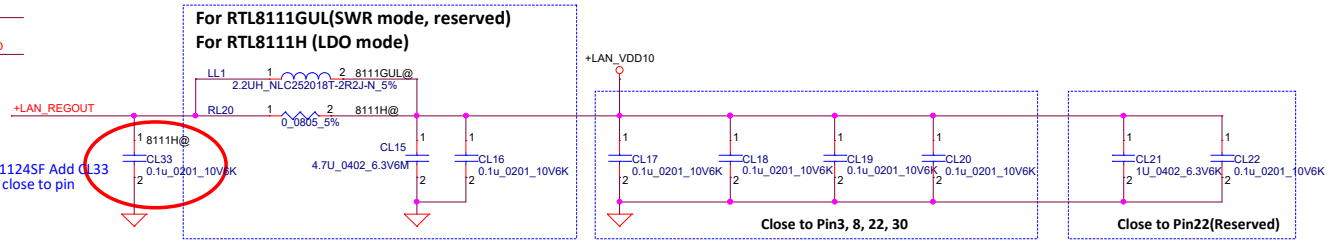


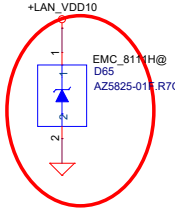
manual change the Codec PN to RTL8111H-CG_QFN32_4X4











21180125SF Add D65 For EMC
Need change to AZ5815/
SC40000BM00, S DIO_ESD
AZ5815-01F.R7GR DFN1006P2E, A.2,EG531

D65 only change P/N from SC40000BM00 to SC400007X00 2019/1/23

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title: LAN_RTL8111H_CG

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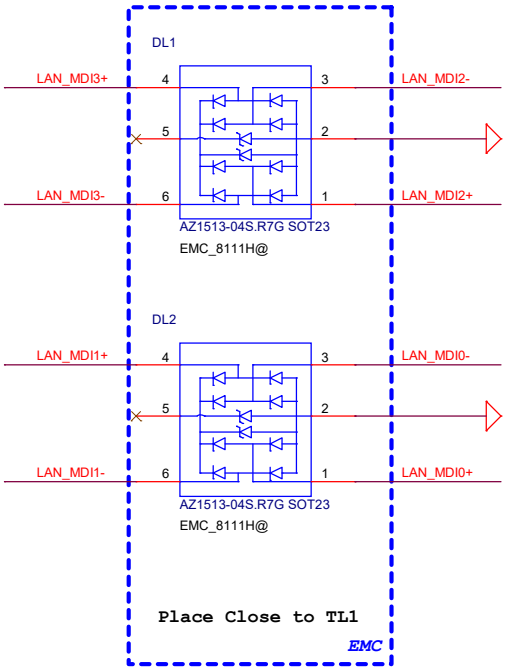
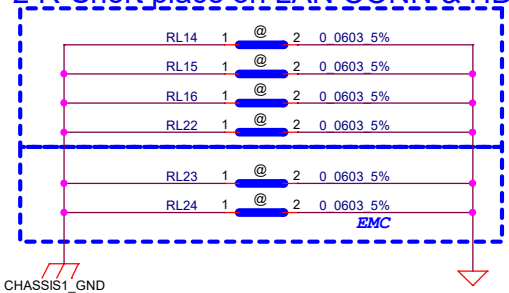
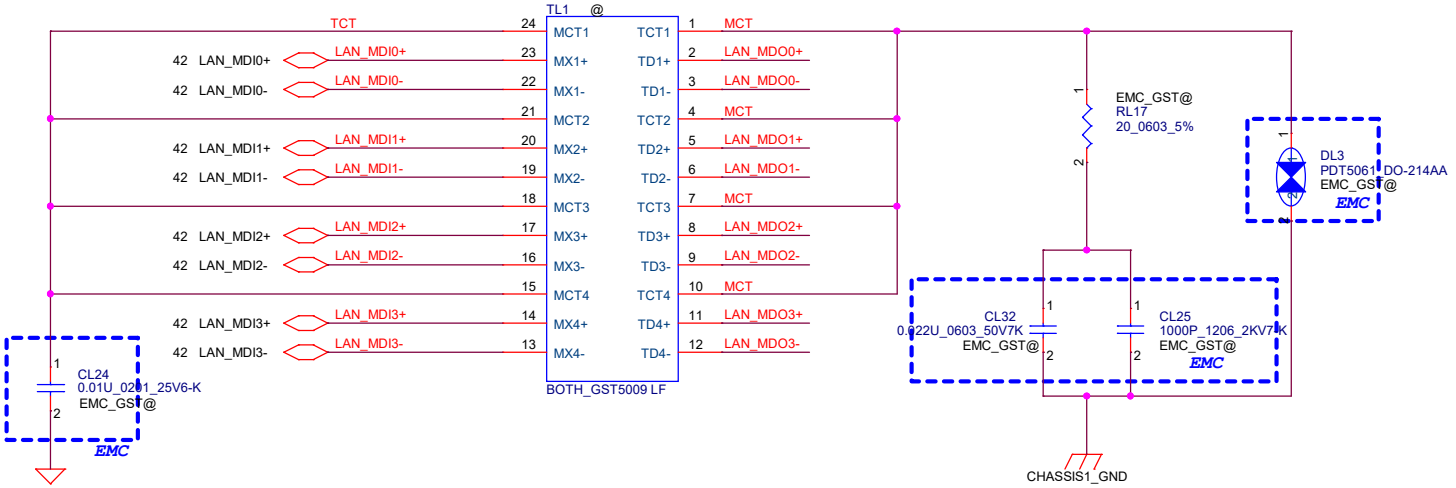
0907SF change DL1/DL2 to
S DIO(BR) AZ1215-04S.R7G SOT23-6L
PN:SC300005900 for 8111H

DL1 & DL2 only change P/N from SC300006100 to SC300006N00 2019/1/23



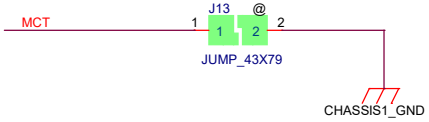
1204SF update,
4 R-Short place on DC-IN CONN & LAN CONN,
2 R-Short place on LAN CONN & HDMI CONN

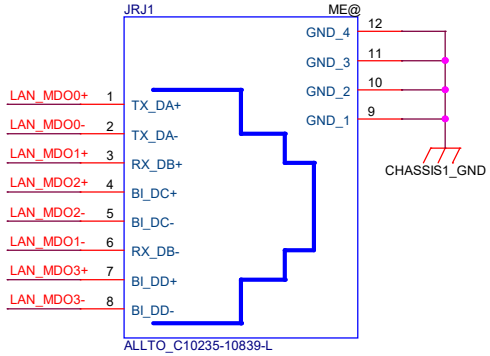




Add TL2 co-lay TL1 1009SF

If stuff TL2,, J13 need short





8/16 Update RJ45 P/N DC021608091 wei

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title	LAN_Transformer		
Size B	Document Number	FG541/FG741	Rev 1.0
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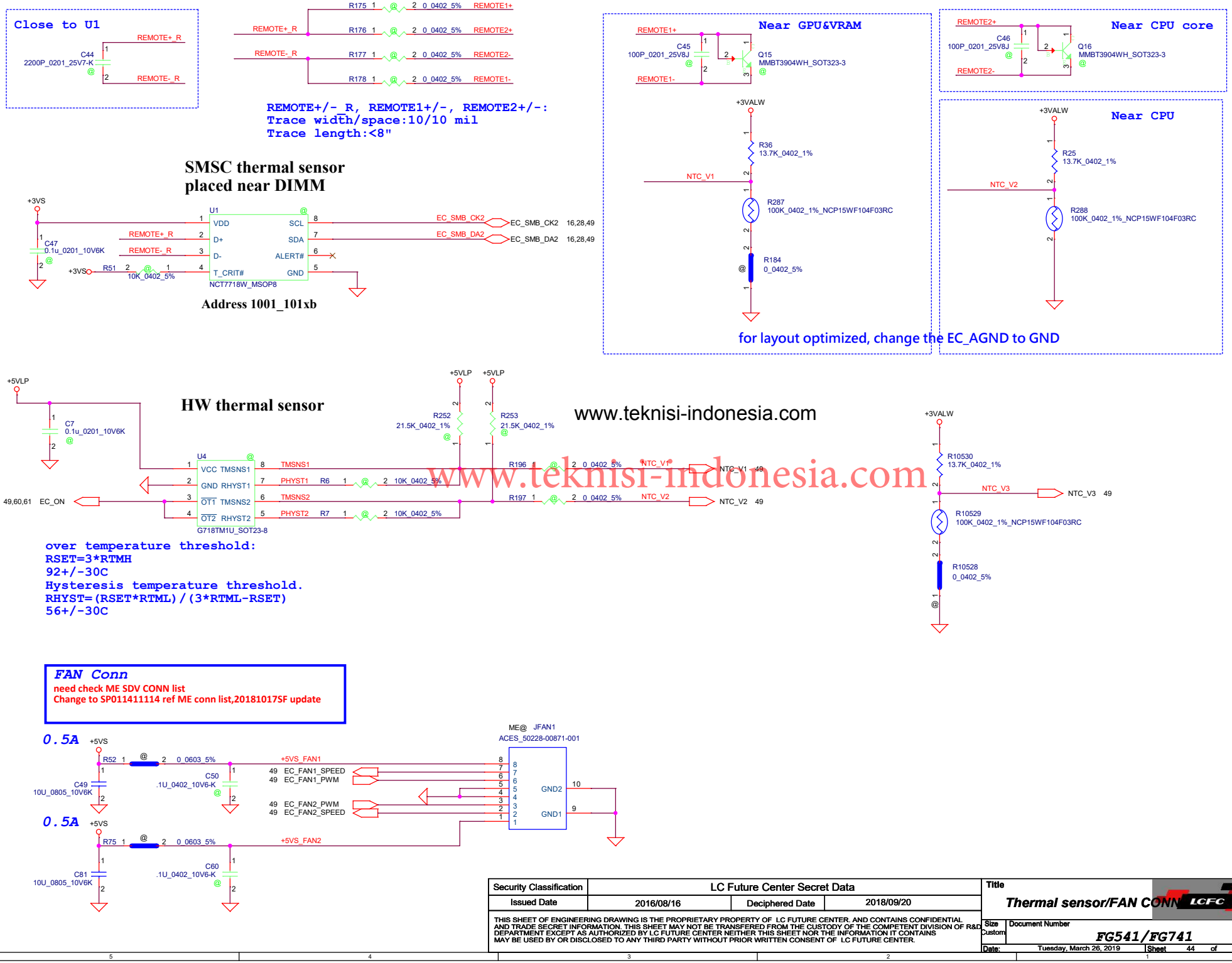

Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2018/09/20

Title: Thermal sensor/FAN CONN

Size: Custom	Document Number: FG541/FG741	Rev: 1.0
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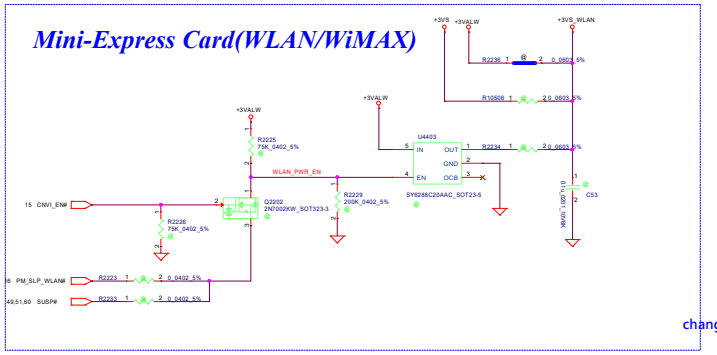
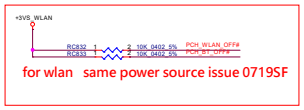
Mini-Express Card(WLAN/WiMAX)

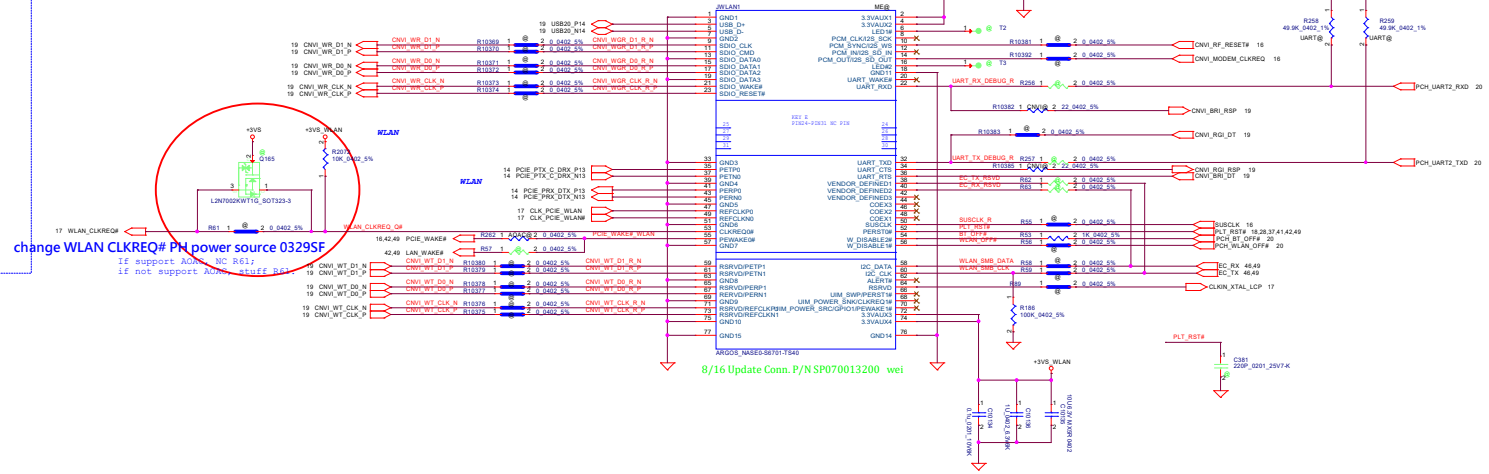


for wlan same power source issue 0719SF



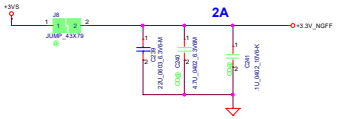
change WLAN CLKREQ# PH power source 0329SF

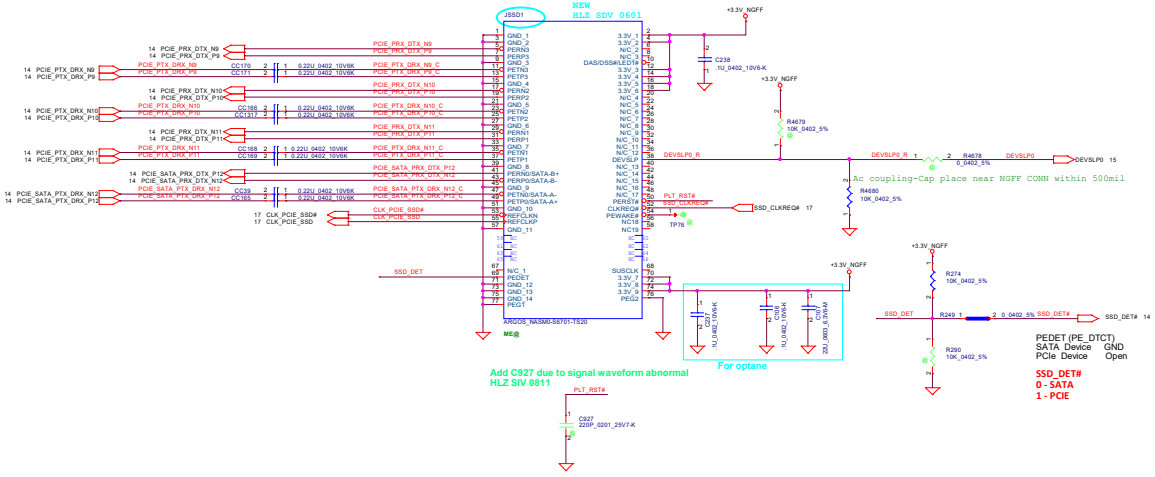
If support ASPM, NC R61;
If not support ASPM, stuff R61



8/16 Update Conn. P/N SP070013200 wei

M.2 SSD(SATA/PCIE)





Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2016/09/20

Title	NGFF WLAN&SSD		
Size	Document Number		Rev
D	FG541/FG741		1.0
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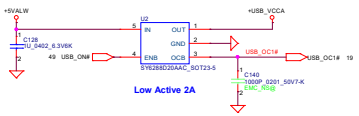
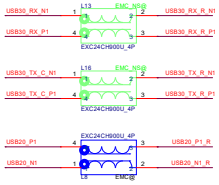
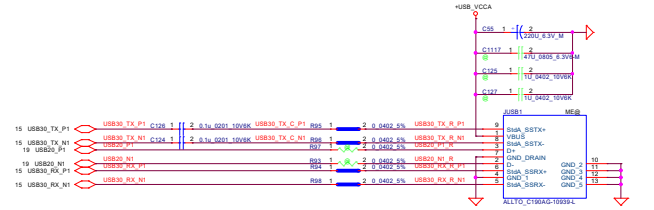
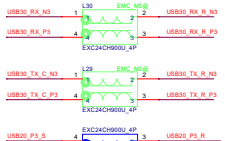
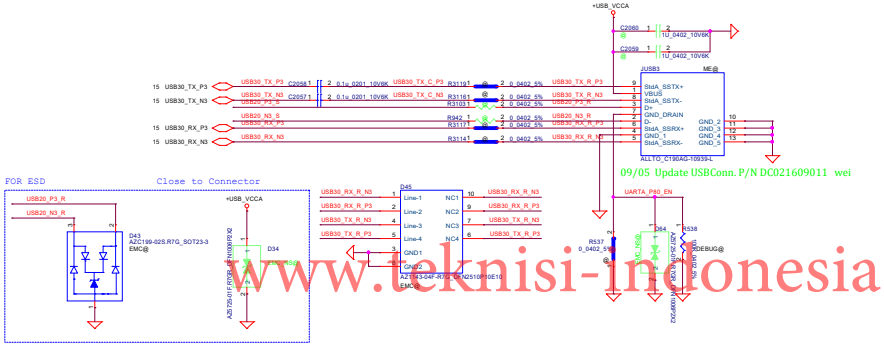
LEFT SIDE USB3.0 PORT x2





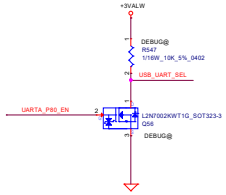


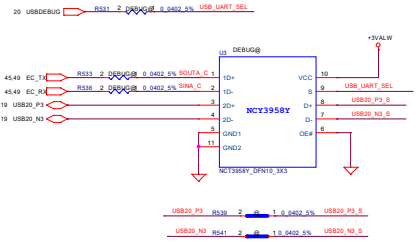




For USB Debug Function

09/20SF add USB debug follow TINY5
change from SA00007WL0D to SA00007WL00 SF1001
SVT non-staff0322SF





USBDEBUG	Kernel debug
Set input	Set input
Set output low	ENABLE

UARTA_P80_EN	POST 80
Set input	DISABLE
Set output low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D1+/-1 to D2+/-
L	H	D1+/-1 to D3+/-

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/09/20

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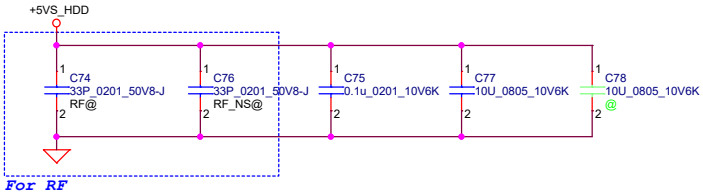
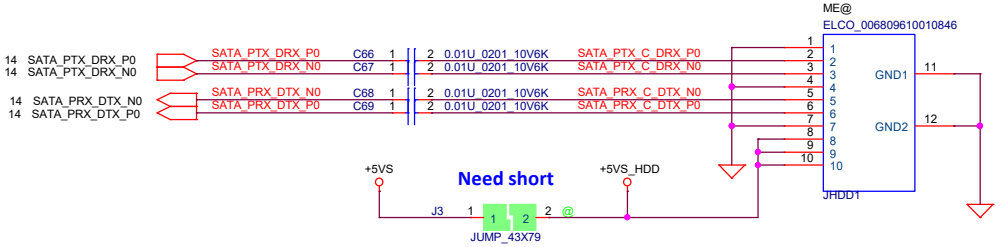
Title: **USB3.0 PORT (LEFT)**

Size: D | Document Number: **FG541/FG741** | Rev: 1.0

Date: Tuesday, March 26, 2019 | Sheet 48 of 69

SATA HDD Conn.

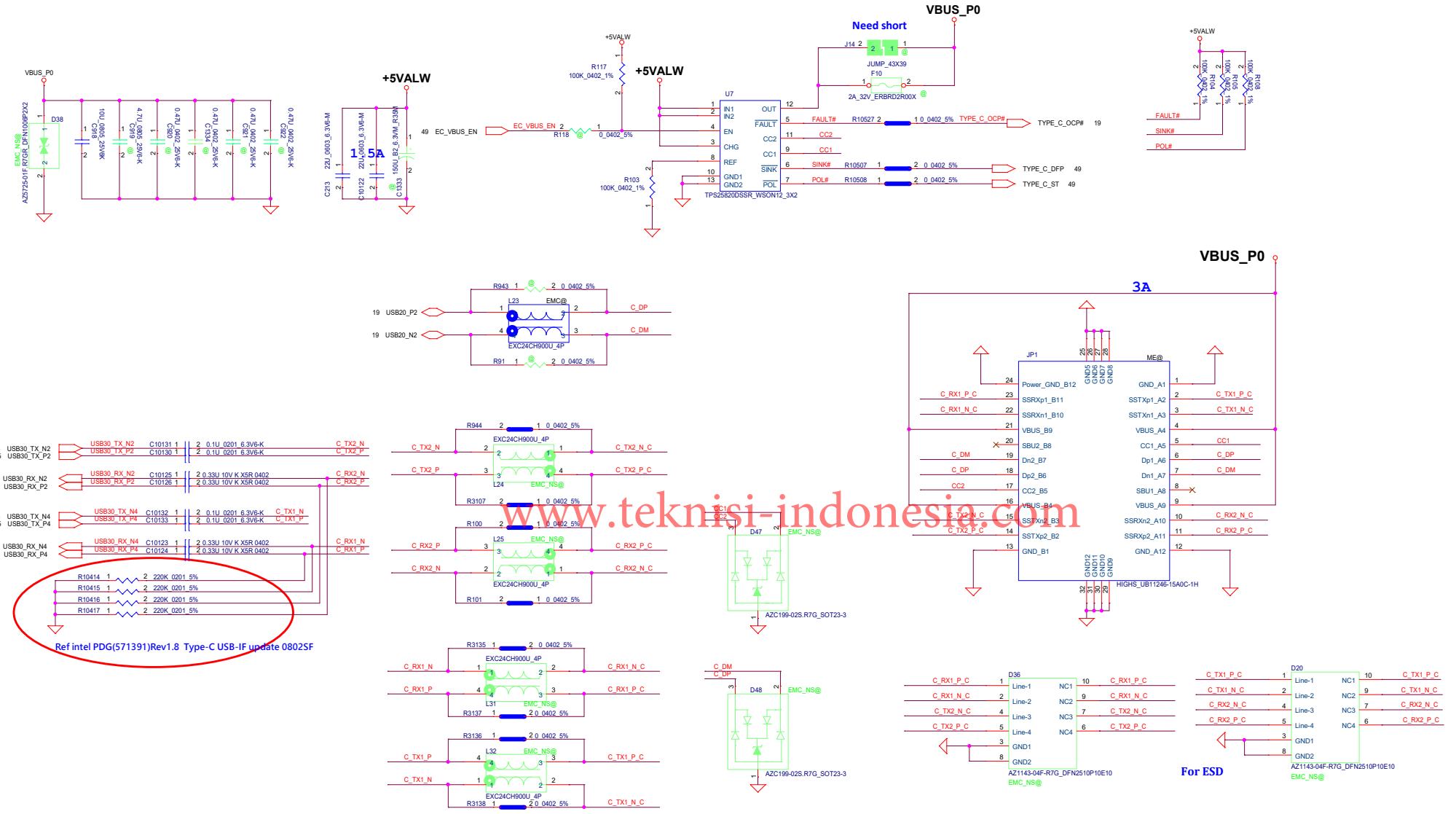




Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title: **HDD/ODD CONN**

Size: Custom	Document Number: FG541/FG741	Rev: 1.0
Date: Tuesday, March 26, 2019	Sheet 47 of 69	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title: 3D Camera

Size	Document Number	Rev
C	FG541/FG741	1.0

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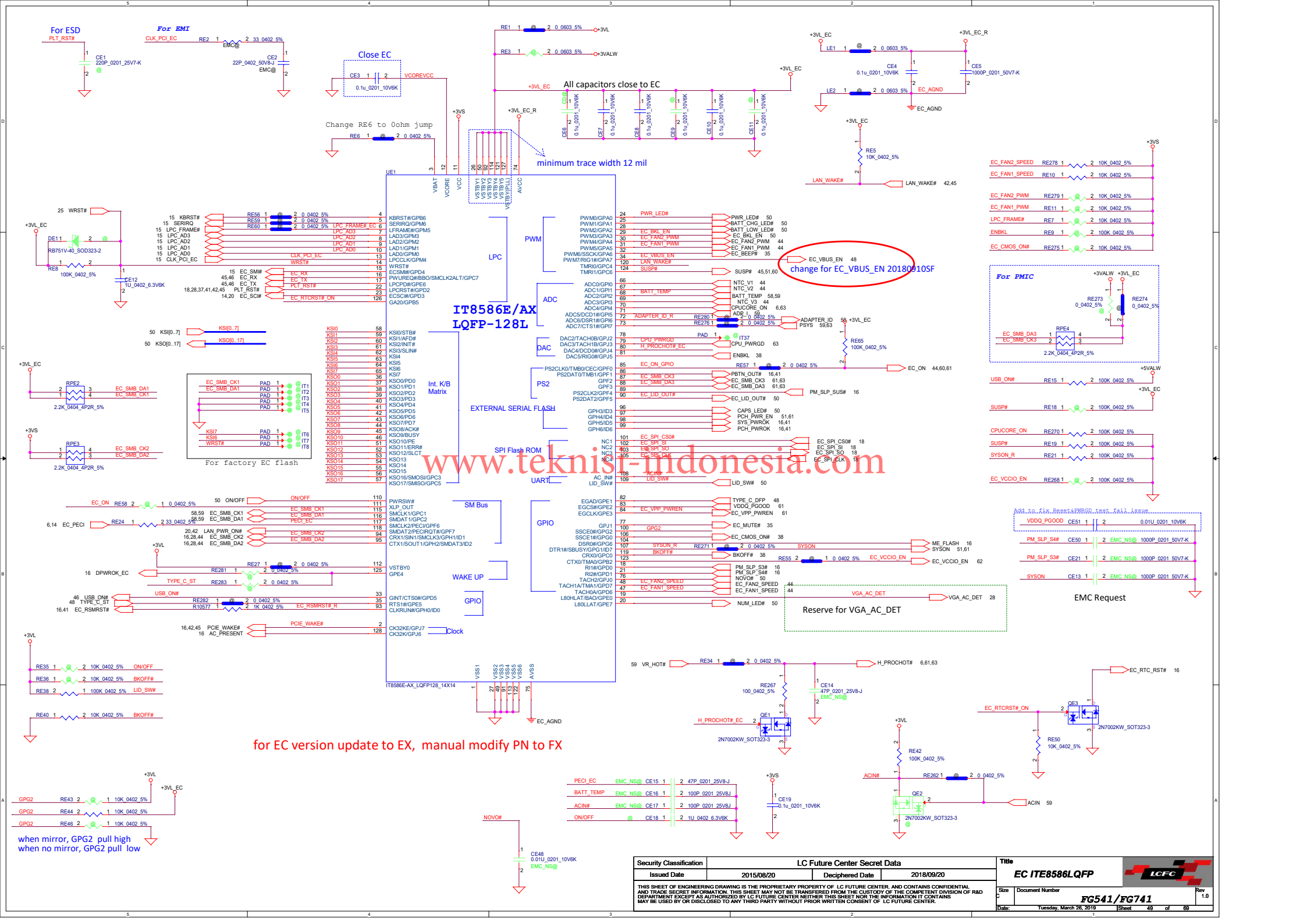

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

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Title	EC ITE8586LQFP		
Size	Document Number		Rev
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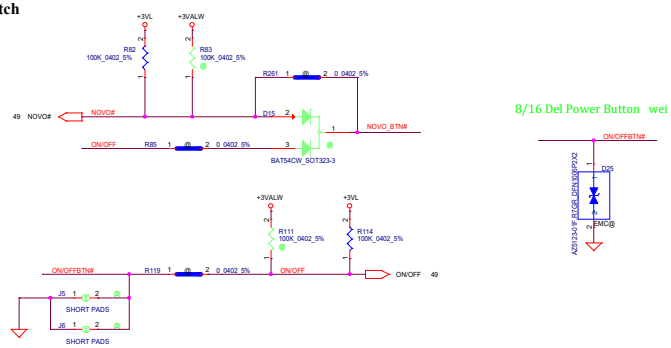
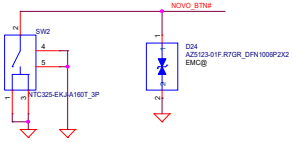
Date:	Tuesday, March 26, 2019	Sheet	49 of 69

ON/OFF switch



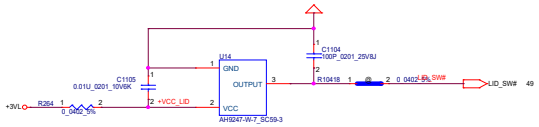
8/16 Del Power Button wei

Novo button

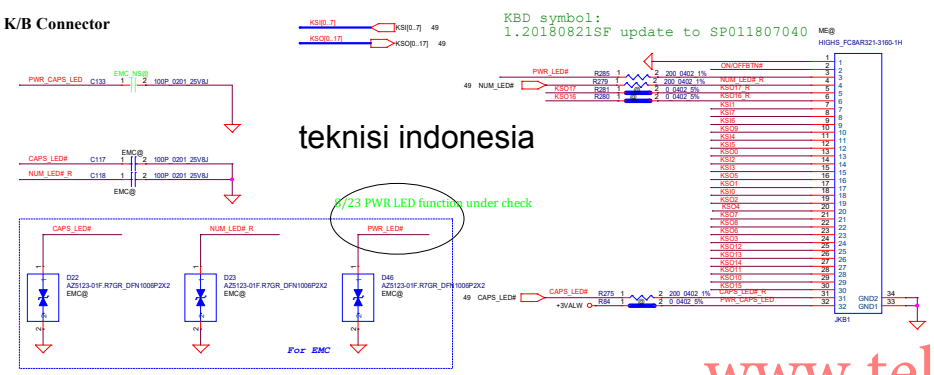


8/31 Update the P/N SN100008W00 wei

LID switch



K/B Connector



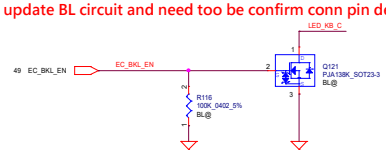
teknisi indonesia

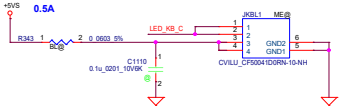
8/23 PWR LED function under check

KBD symbol:
1.20180821SF update to SP011807040

KB Backlight Connector

update BL circuit and need too be confirm conn pin define 0925SF

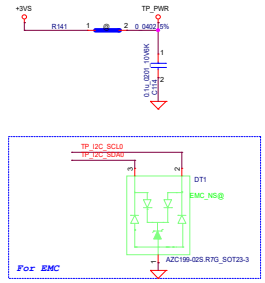


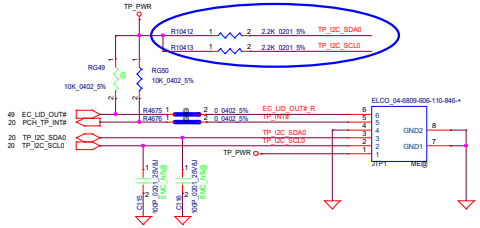


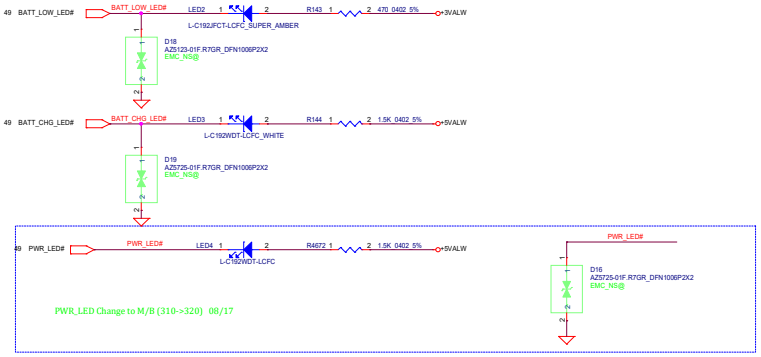
Finger Print Connector

follow OD V1.5 delete finger print function 0927SF

TP/B Connector







Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title	KBD/PWR/IO/LED/TP Conn.		
Size: Custom	Document Number: FG541/FG741		Rev: 1.0
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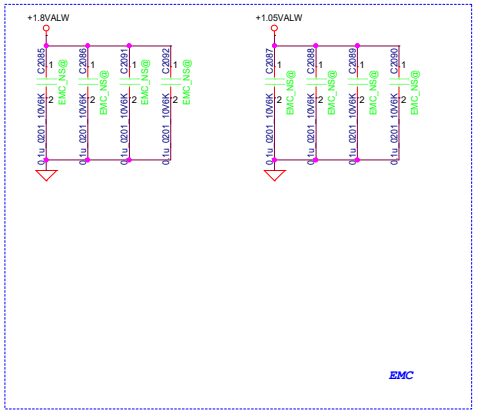
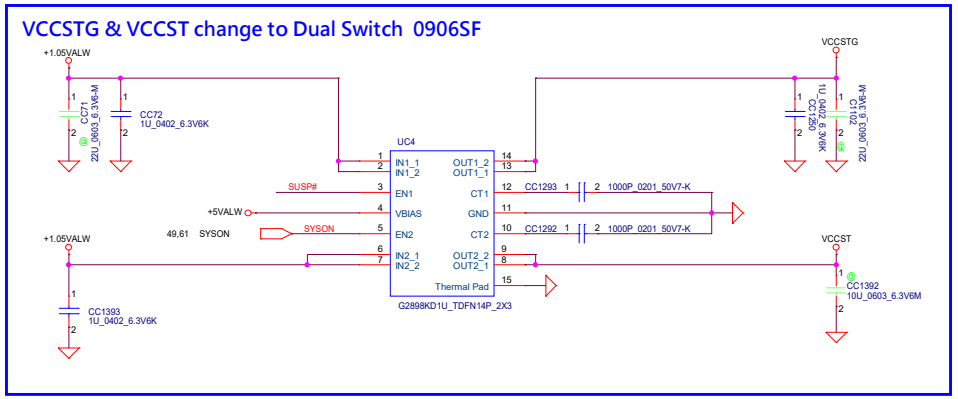
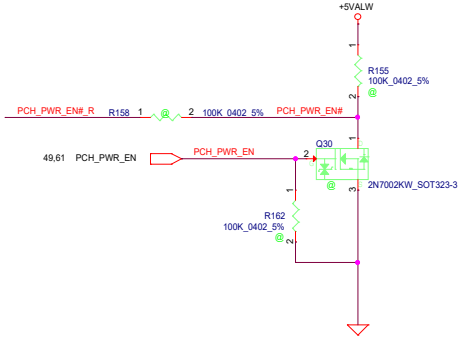
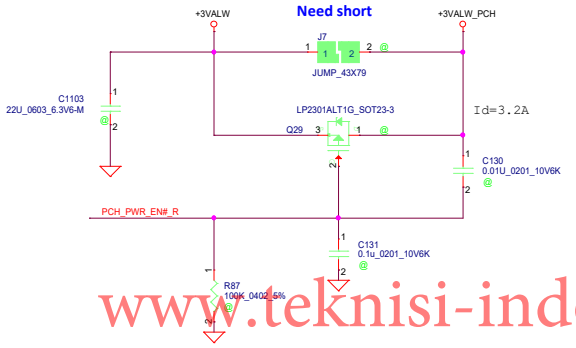
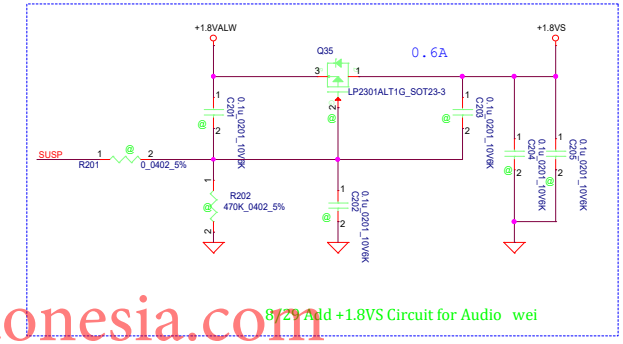


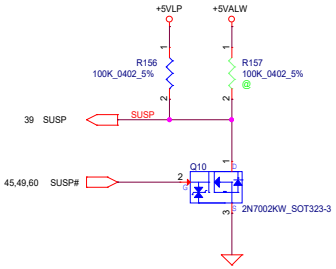




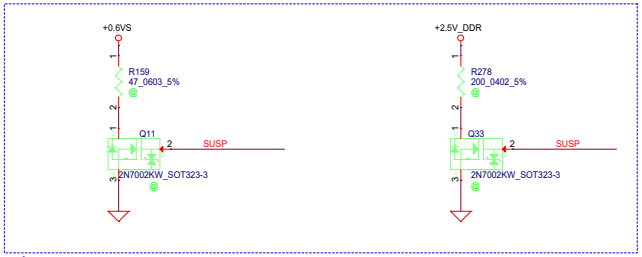




08/29 Add +1.8VS Circuit for Audio wei



For DisCharge



08/29: Need double check enable signal and the resistance

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title: DC V TO VS INTERFACE

Size: C	Document Number: FG541/FG741	Rev: 1.0
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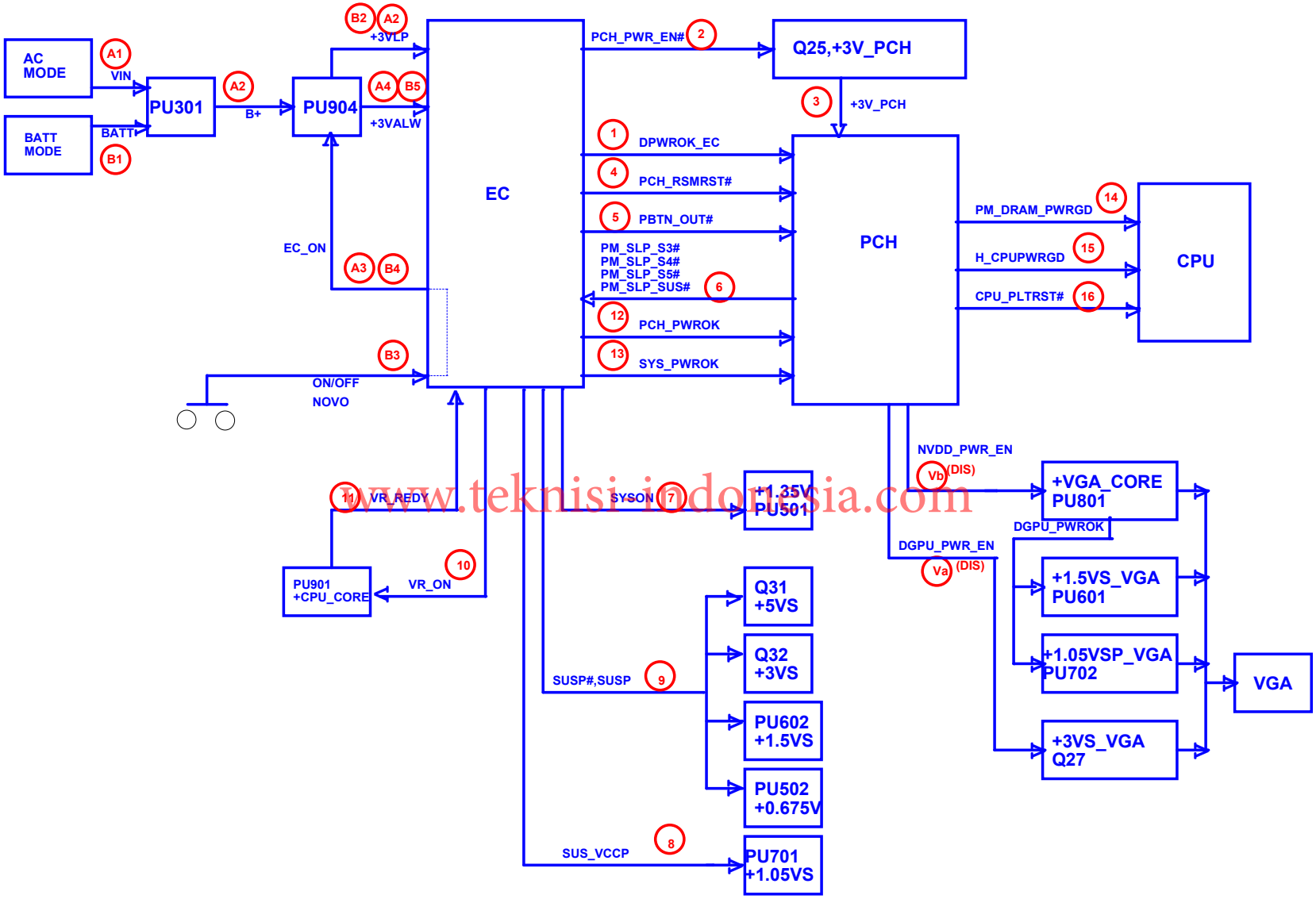

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title: **Power sequence block**

Size	Document Number	Rev
Custom	FG541/FG741	1.0

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ZZ1 PCB@
PCB_1B4 NM-C362 REV1 M/B
DA8B001SU10
PCB_MB

ZZZ8 HDMI@
HDMI PN
RC000004UJ
HDMI Logo

UC1 I5_MP@
S IC CL8068404121905 SRF6X U0 2.4G 12 !
SA0003A0P10

UC1 I7_MP@
S IC CL8068404121817 SRF6U U0 2.6G 12!
SA0003A0R10

MP CPU

UC1 I5_QS@
S IC CL8068404121905 QRR5 U0 2.4G BGA
SA0003A0P50

QS CPU

UL1 8111H@
RTL8111H-CG
SA0002749W00

UL1 8111GUL@
RTL8111GUL-CG
SA0003060V00

LAN Chip

UH1 PCH_MP@
S IC FH82HM370 SR40B B0 BGA 874P PCH 12!
SA0003AG00

MP PCH

UH1 PCH_QS@
S IC FHHM370 QNYF B0 FCBGA 874P PCH
SA0003BP50

QS PCH

TL1 GST@
BOTH GST5009 LF
SP050009BG00

TL1 2ND_TR@
BOTH GST5009 LF
SP050009BM00

Transformer

TL2 AJCHO@
FORM N-8660GR
SP050009N200

TL2 INPAQ@
FORM IN-8660GR
SP050009J200

New Transformer

UV1 GPU@
N17P-G0-K1-A1
SA0003KY200

GPU

ZZZ4 DRAM_S8G@
ALT_GROUP PARTS SAMSUNG D4G FG541
X7646T1200A

ZZZ2 DRAM_M8G@
ALT_GROUP PARTS MICRON D4G FG541
X7646T1200B

ZZZ3 DRAM_H8G@
ALT_GROUP PARTS HYNIX D4G FG541
X7646T1200C

DRAM X76 BOM

ZZZ9 M8GX3@
ALT_GROUP PARTS MICRON V3G FG541
X7646T12007

ZZZ11 S8GX3@
ALT_GROUP PARTS SAMSUNG V3G FG541
X7646T12008

ZZZ10 H8GX3@
ALT_GROUP PARTS HYNIX V3G FG541
X7646T12009

VRAM X76 BOM

UD1 MD_S8Gb@ K4A8G165WC-BCTD SA0003BPE00
UD2 MD_S8Gb@ K4A8G165WC-BCTD SA0003BPE00
UD3 MD_S8Gb@ K4A8G165WC-BCTD SA0003BPE00
UD4 MD_S8Gb@ K4A8G165WC-BCTD SA0003BPE00
RH775 MD_S8Gb@ 10K_0402_5% SD028100Z8J
RH777 MD_S8Gb@ 10K_0402_5% SD028100Z8J
RH195 MD_S8Gb@ 10K_0402_5% SD028100Z8J

2666MT/s DRAM_Samsung 8G

UV10 S8G_VR@ K4G80325FB-HC28 SA0003B1C00
UV6 S8G_VR@ K4G80325FB-HC28 SA0003B1C00
UV8 S8G_VR@ K4G80325FB-HC28 SA0003B1C00
RV194 S8G_VR@ 100K_0402_5% SD028100Z8J
RV193 S8G_VR@ 100K_0402_5% SD028100Z8J
RV192 S8G_VR@ 100K_0402_5% SD028100Z8J
PR5512 S8G_VR@ 41.2K_0402_1% SD000009K0J

VRAM_Samsung 8GX3

UD1 MD_H8Gb@ H5AN8G6NCJR-VKC SA0003B9T10
UD2 MD_H8Gb@ H5AN8G6NCJR-VKC SA0003B9T10
UD3 MD_H8Gb@ H5AN8G6NCJR-VKC SA0003B9T10
UD4 MD_H8Gb@ H5AN8G6NCJR-VKC SA0003B9T10
RH775 MD_H8Gb@ 10K_0402_5% SD028100Z8J
RH777 MD_H8Gb@ 10K_0402_5% SD028100Z8J
RH163 MD_H8Gb@ 10K_0402_5% SD028100Z8J

2666MT/s DRAM_Hynix 8G

UV10 H8G_VR@ H5GC8H24AJR-R0C SA0003B1630
UV6 H8G_VR@ H5GC8H24AJR-R0C SA0003B1630
UV8 H8G_VR@ H5GC8H24AJR-R0C SA0003B1630
RV189 H8G_VR@ 100K_0402_5% SD028100Z8J
RV193 H8G_VR@ 100K_0402_5% SD028100Z8J
RV187 H8G_VR@ 100K_0402_5% SD028100Z8J
PR5512 H8G_VR@ 41.2K_0402_1% SD000009K0J

VRAM_Hynix 8GX3

UD1 MD_M8Gb@ MT40A512M16LY-075:E SA0003BF930
UD2 MD_M8Gb@ MT40A512M16LY-075:E SA0003BF930
UD3 MD_M8Gb@ MT40A512M16LY-075:E SA0003BF930
UD4 MD_M8Gb@ MT40A512M16LY-075:E SA0003BF930
RH775 MD_M8Gb@ 10K_0402_5% SD028100Z8J
RH776 MD_M8Gb@ 10K_0402_5% SD028100Z8J
RH195 MD_M8Gb@ 10K_0402_5% SD028100Z8J

2666MT/s DRAM_Micron 8G

UV10 M8G_VR@ MT51J256M32HF-70:B SA0003B1730
UV6 M8G_VR@ MT51J256M32HF-70:B SA0003B1730
UV8 M8G_VR@ MT51J256M32HF-70:B SA0003B1730
RV189 M8G_VR@ 100K_0402_5% SD028100Z8J
RV193 M8G_VR@ 100K_0402_5% SD028100Z8J
RV192 M8G_VR@ 100K_0402_5% SD028100Z8J
PR5512 M8G_VR@ 41.2K_0402_1% SD000009K0J

VRAM_Micron 8GX3

NEW DRAM X76

ZZZ14 M8GX3_NEW@
ALT_GROUP PARTS MIC V3GB FG541
X7646T12008

NEW VRAM X76 BOM

UD1 MD_HTM8Gb@ HTH5AN8G6NAFR-VKD SA0003A3C00
UD2 MD_HTM8Gb@ HTH5AN8G6NAFR-VKD SA0003A3C00
UD3 MD_HTM8Gb@ HTH5AN8G6NAFR-VKD SA0003A3C00
UD4 MD_HTM8Gb@ HTH5AN8G6NAFR-VKD SA0003A3C00
RH775 MD_HTM8Gb@ 10K_0402_5% SD028100Z8J
RH776 MD_HTM8Gb@ 10K_0402_5% SD028100Z8J
RH163 MD_HTM8Gb@ 10K_0402_5% SD028100Z8J

NEW DRAM **2666MT/s DRAM_Micron 8G**

UV10 M8G_VR1@ MT51J256M32HF-80 :B SA0003T2930
UV6 M8G_VR1@ MT51J256M32HF-80 :B SA0003T2930
UV8 M8G_VR1@ MT51J256M32HF-80 :B SA0003T2930
RV189 M8G_VR1@ 100K_0402_5% SD028100Z8J
RV193 M8G_VR1@ 100K_0402_5% SD028100Z8J
RV192 M8G_VR1@ 100K_0402_5% SD028100Z8J
PR5512 M8G_VR@ 41.2K_0402_1% SD000009K0J

NEW VRAM **VRAM_Micron 8GX3**

UD1 MD_SMT8Gb@ SDQC8G8W16XCTD9N1T SA0003RR00
UD2 MD_SMT8Gb@ SDQC8G8W16XCTD9N1T SA0003RR00
UD3 MD_SMT8Gb@ SDQC8G8W16XCTD9N1T SA0003RR00
UD4 MD_SMT8Gb@ SDQC8G8W16XCTD9N1T SA0003RR00
RH774 MD_SMT8Gb@ 10K_0402_5% SD028100Z8J
RH777 MD_SMT8Gb@ 10K_0402_5% SD028100Z8J
RH195 MD_SMT8Gb@ 10K_0402_5% SD028100Z8J

NEW DRAM **2666MT/s DRAM_SMART 8G**

GPU	FB Memory (GDDR5)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
N17P-G0-K1	Samsung 8Gb	K4G80325FB-HC28	0(0x0000)	L/RV194	L/RV193	L/RV192
	Micron 8Gb	MT51J256M32HF-70:B	4(0x0004)	H/RV189	L/RV193	L/RV192
	Hynix 8Gb	H5GC8H24AJR-R0C	5(0x0005)	H/RV189	L/RV193	H/RV187
	Micron 8Gb	MT51J256M32HF-80 :B	4(0x0004)	H/RV189	L/RV193	L/RV192

DRAM	Memory Down(DDR4)		DRAMCFG	PCH_GPA23	PCH_GPA22	PCH_GPA21
8Gb	Samsung 8Gb 2666 MT/s	K4A8G165WC-BCTD	0(0x000)	L/RH775	L/RH777	L/RH195
	Hynix 8Gb 2666 MT/s	H5AN8G6NCJR-VKC	1(0x001)	L/RH775	L/RH777	H/RH163
	Micron 8Gb 2666 MT/s	MT40A512M16LY-075:E	2(0x010)	L/RH775	H/RH776	L/RH195
	Micron 8Gb 2666 MT/s	HTH5AN8G6NAFR-VKD	3(0x011)	L/RH775	H/RH776	H/RH163
	Smart 8Gb 2666 MT/s	SDQC8G8W16XCTD9N1T	4(0x100)	H/RH774	L/RH777	L/RH195
			5(0x101)	H/RH774	L/RH777	H/RH163
			6(0x110)	H/RH774	H/RH776	L/RH195
	SODIMM only		7(0x111)	H/RH774	H/RH776	H/RH163

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title	Virtual symbol		
Size	Document Number		Rev
Custom	FG541/FG741		1.0
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GPU Thermal Holex2 Close to RJ45 DC-IN x2

CPU Thermal Holex3 WLAN Standoff

PCB Fedical Mark PAD

FD1 FD2 FD3 FD4 FD5 FD6

H1 HOLEA PAD_D2P4
H2 HOLEA PAD_D2P4
H3 HOLEA PAD_D2P4
H10 HOLEA PAD_CT5P5B6P0D2P4
H11 HOLEA PAD_CT5P5B6P0D2P4
H4 HOLEA PAD_C6P0D4P0
H5 HOLEA PAD_C6P0D4P0
H6 HOLEA PAD_C6P0D4P0
H7 HOLEA PAD_C6P0D4P0
H8 HOLEA PAD_C6P0D4P0
H13 HOLEA PAD_C6P0D3P3
H14 HOLEA PAD_C6P0D3P3
H9 HOLEA PAD_C2P7D2P7N
H12 HOLEA PAD_CT6P0B7P0D3P7
H15 HOLEA PAD_D3P4x2P7
H16 HOLEA PAD_CT5P6B7P0D3P0
H17 HOLEA PAD_CT5P6B7P0D3P0 CHASSIS1_GND
H18 HOLEA PAD_C7P0D3P0

Close to Audio jack

follow layout list update 20181010SF

USB3.0 Shielding

SH7 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH8 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH9 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH10 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH11 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH12 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P

DDR4 Shielding

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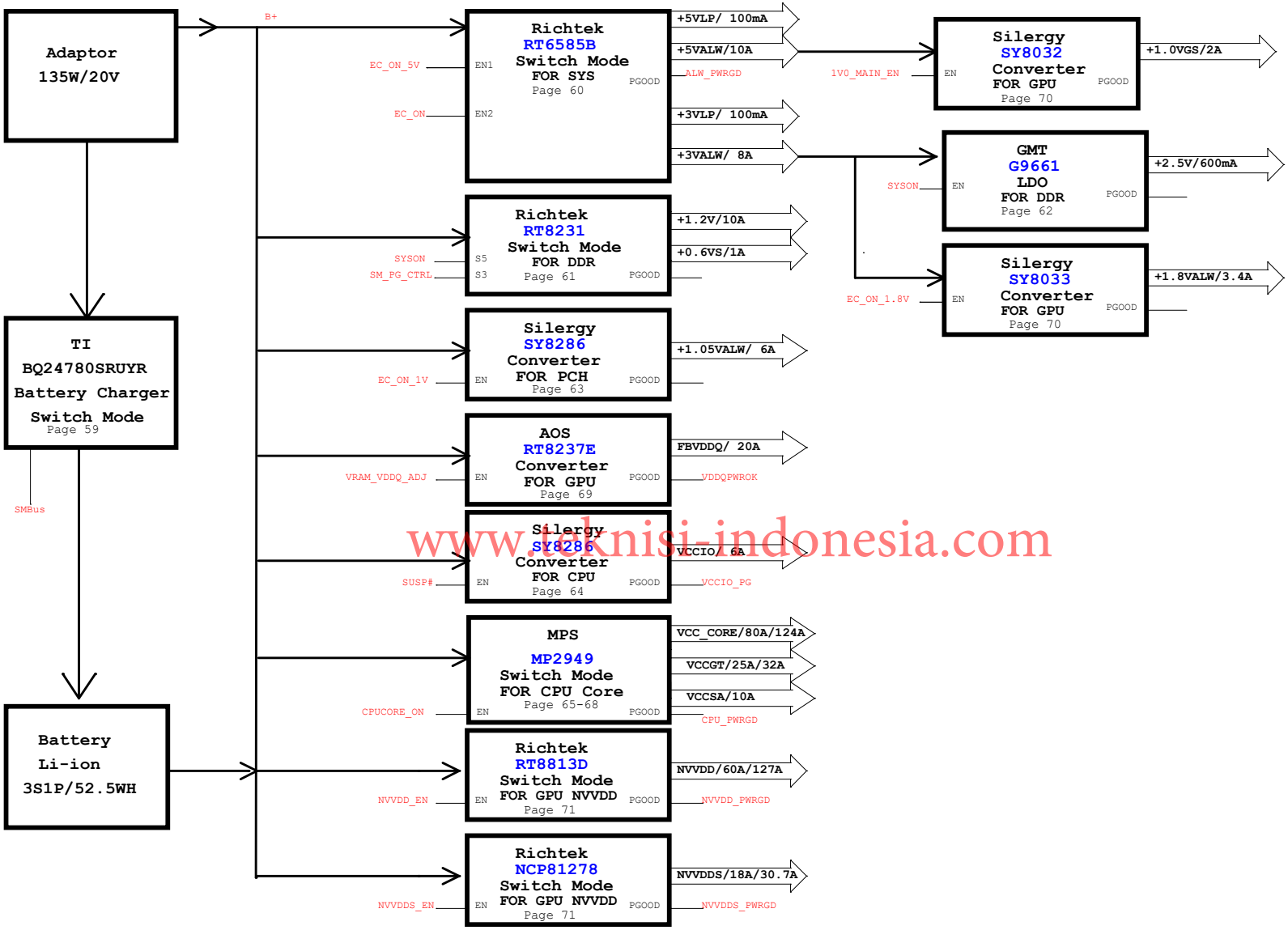

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Title: **Power Diagram**

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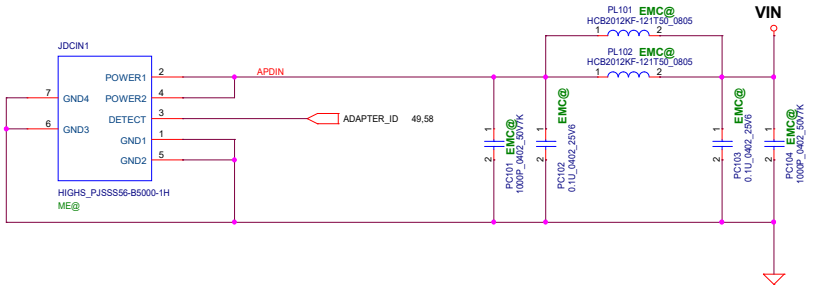
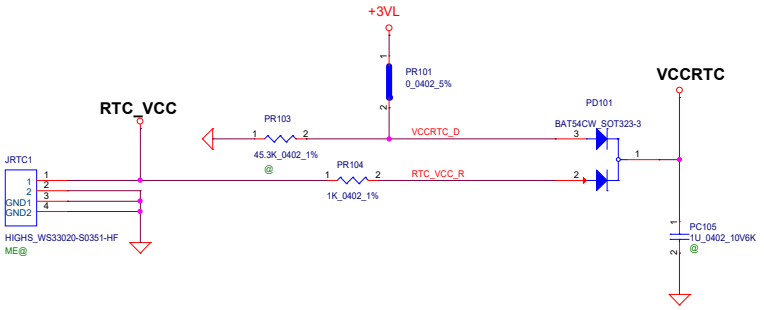
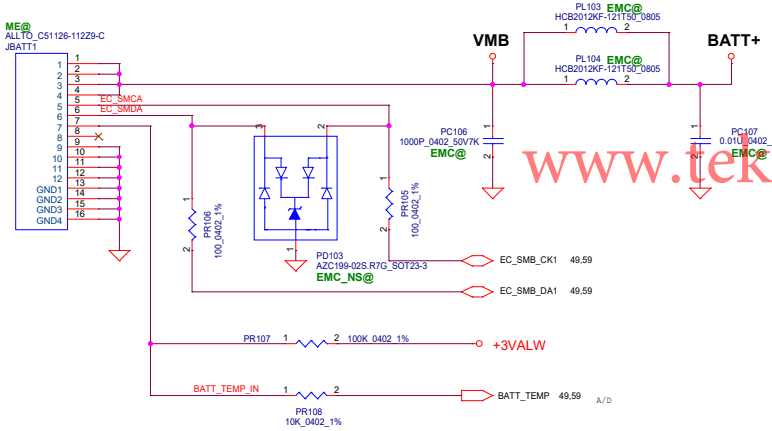


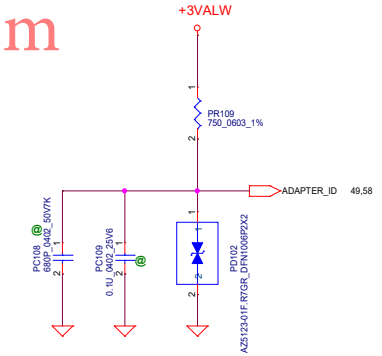
DC IN: 1.DC IN connect apply for PN HIGHS_PJSSS56-B5000-1H_5P-T ,need replace connector rate current 7A



RTC: 1. 0ohm delete
2.the max VCCRTC < 3.2V specification
3.RTC cable 35mm



battery IN:
1.20180821SF update to SP011808066
2.battery connector 12pin per pin 4.5A



ADP_ID:1. cost down solution
2.EC initial ID function

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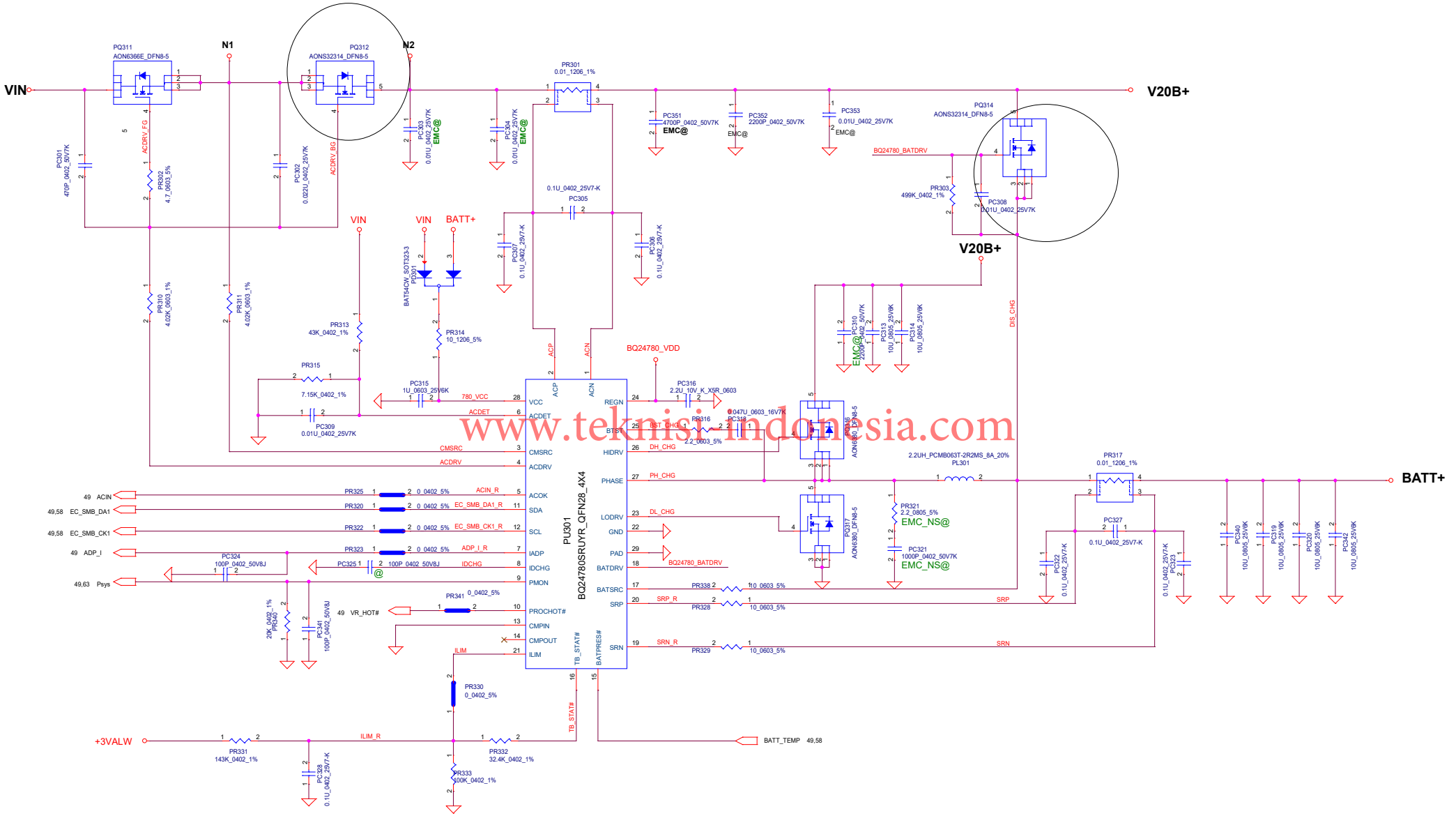

charge current: 1C 5A
charge voltage: 12.6V
charge frequency: 800K
ILIM pin: charge7A, turbo-discharge-10A

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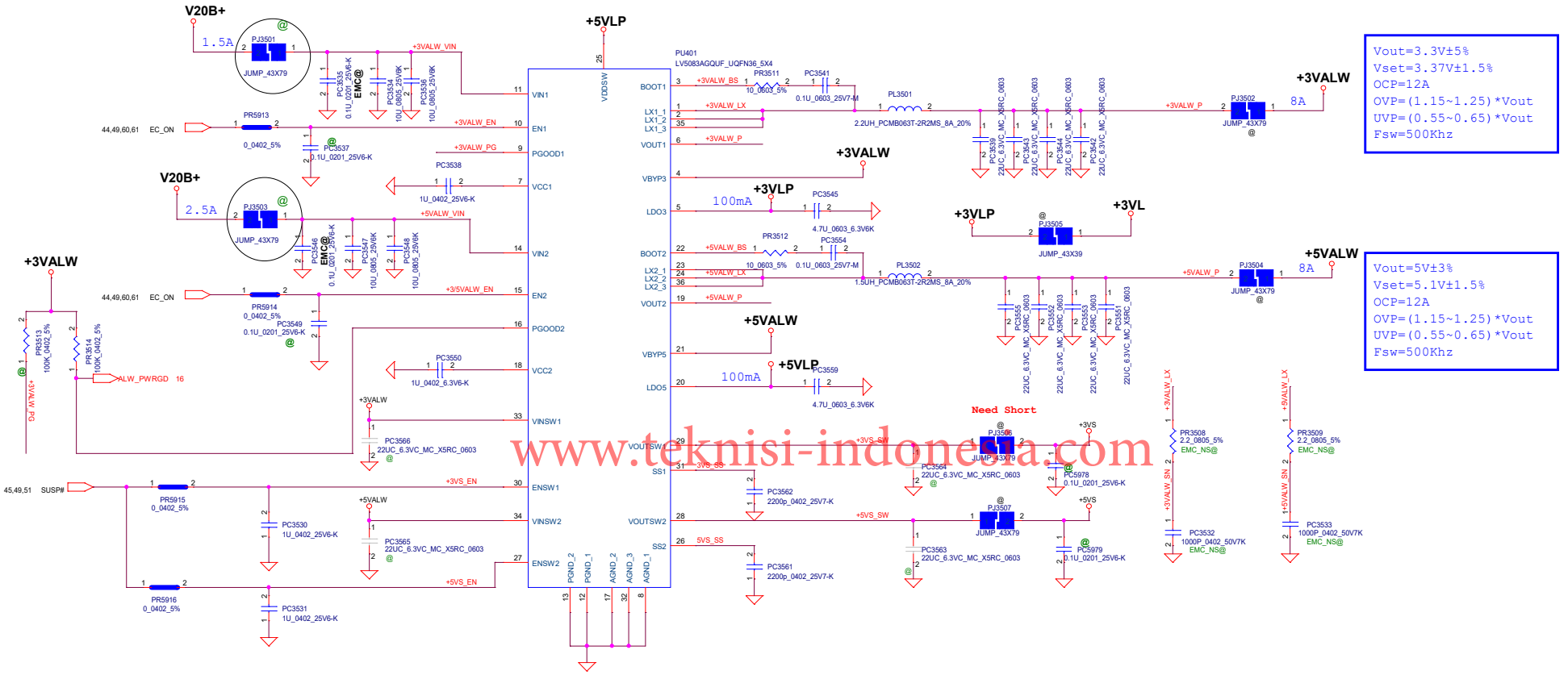

VOUT=3.07V
TDC=6A
OCP=10A
Fsw=600Khz

VOUT=5.01V
TDC=8A
OCP=12A
Fsw=600Khz

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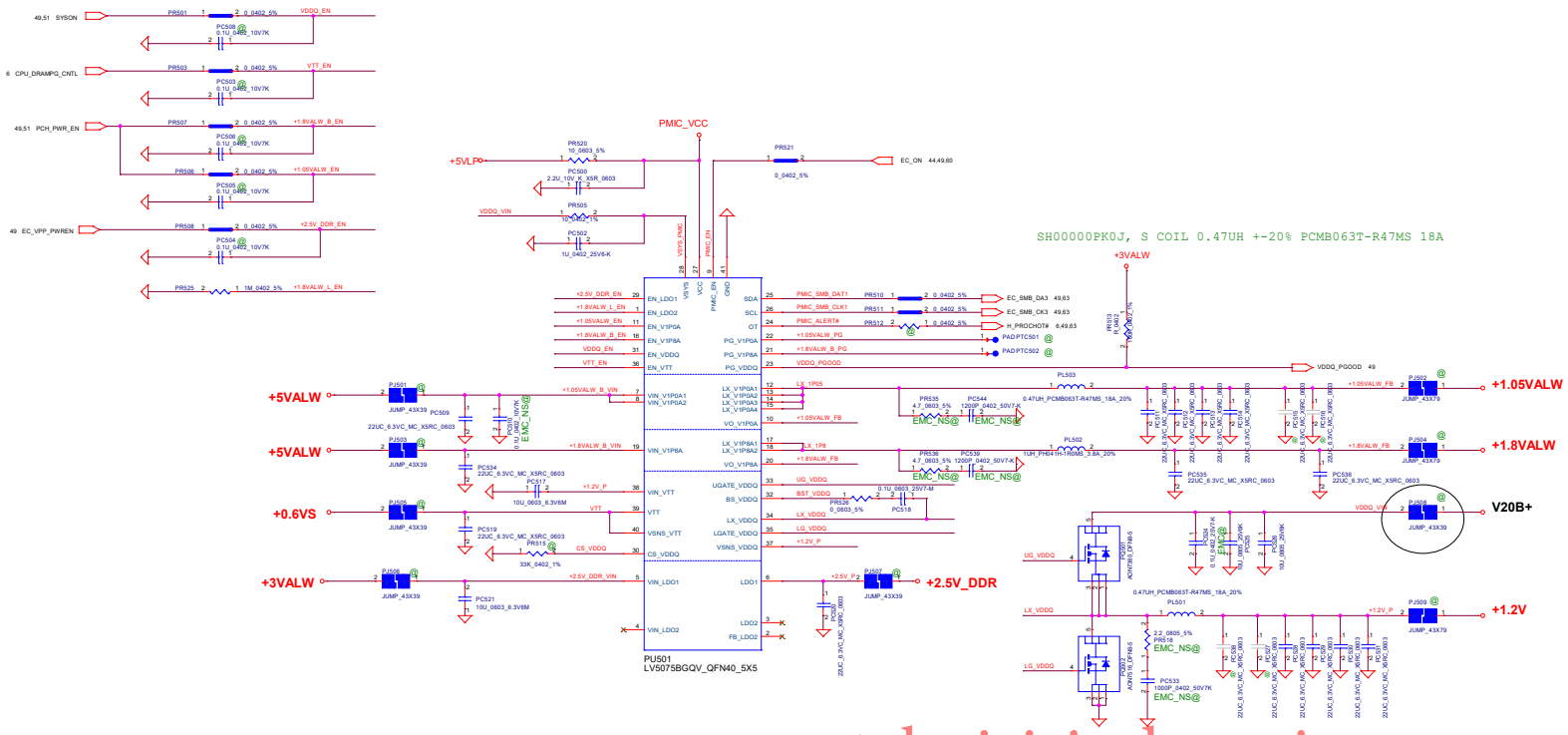

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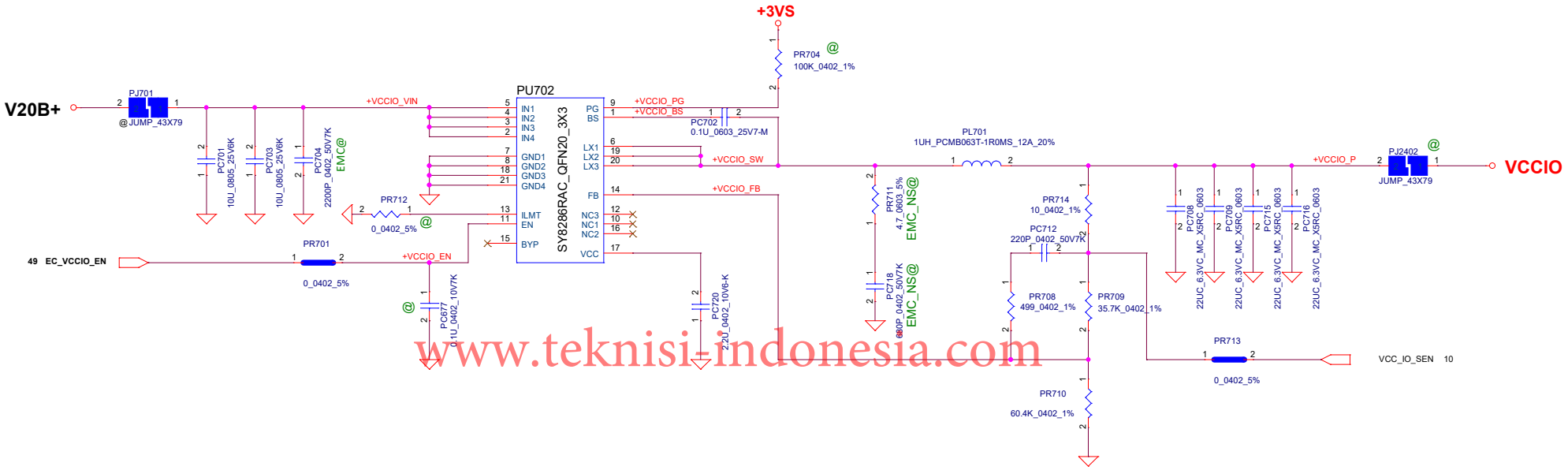

VCCIO:FB=0.6V/0.954V
TDC=6A
OCP:10A
OVP:120%
frequency:500Khz
remove sense pull high in power side

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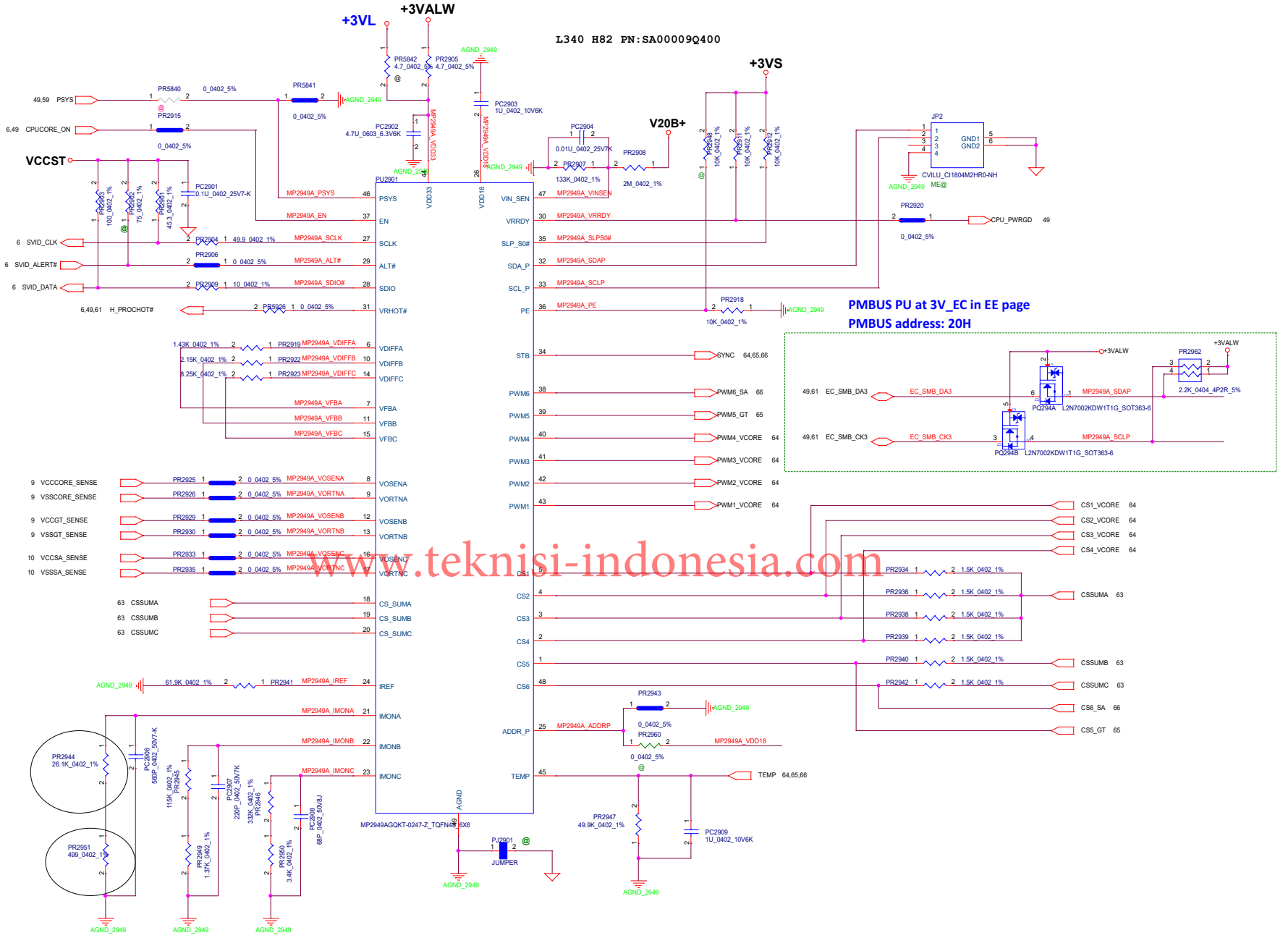

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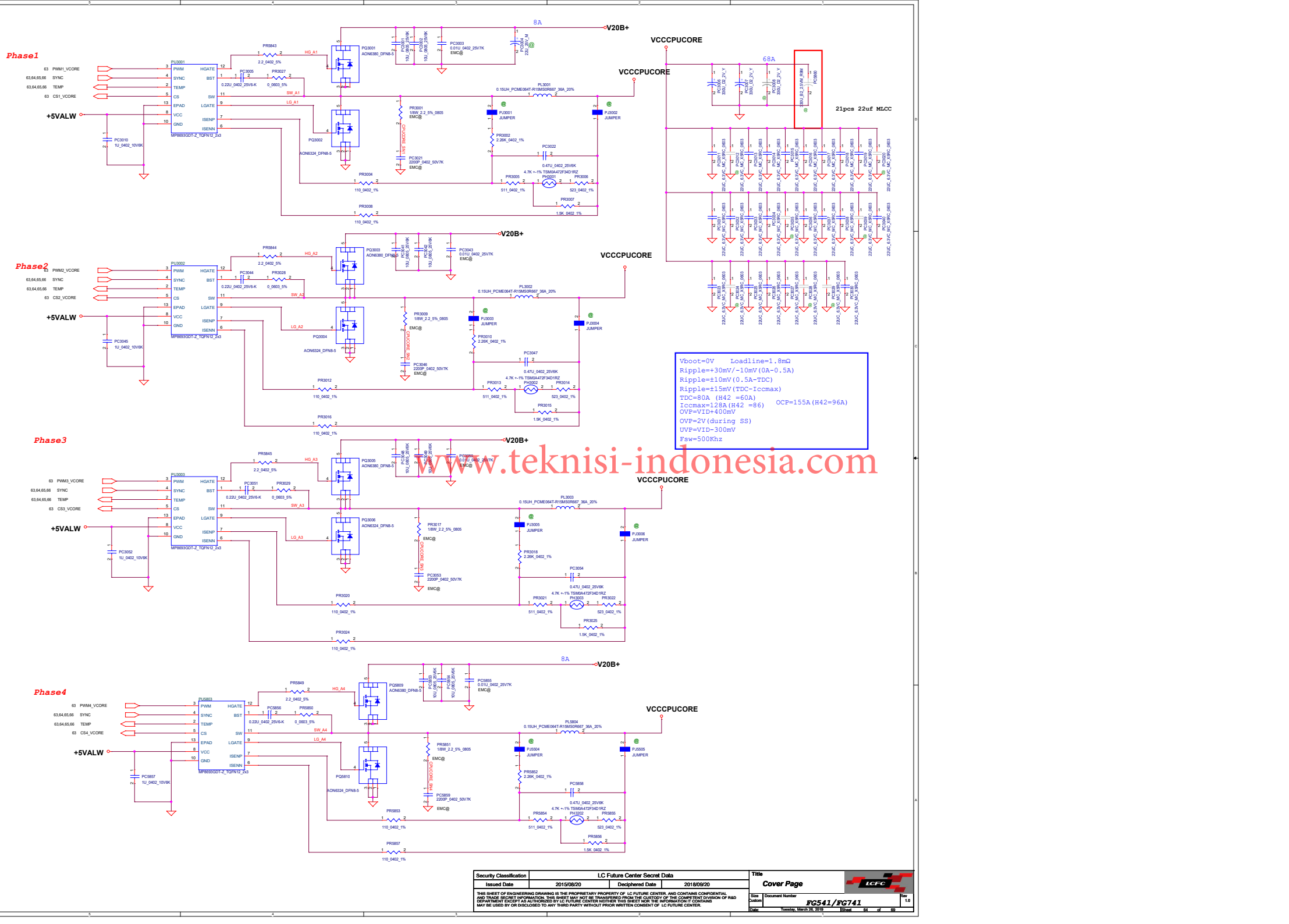

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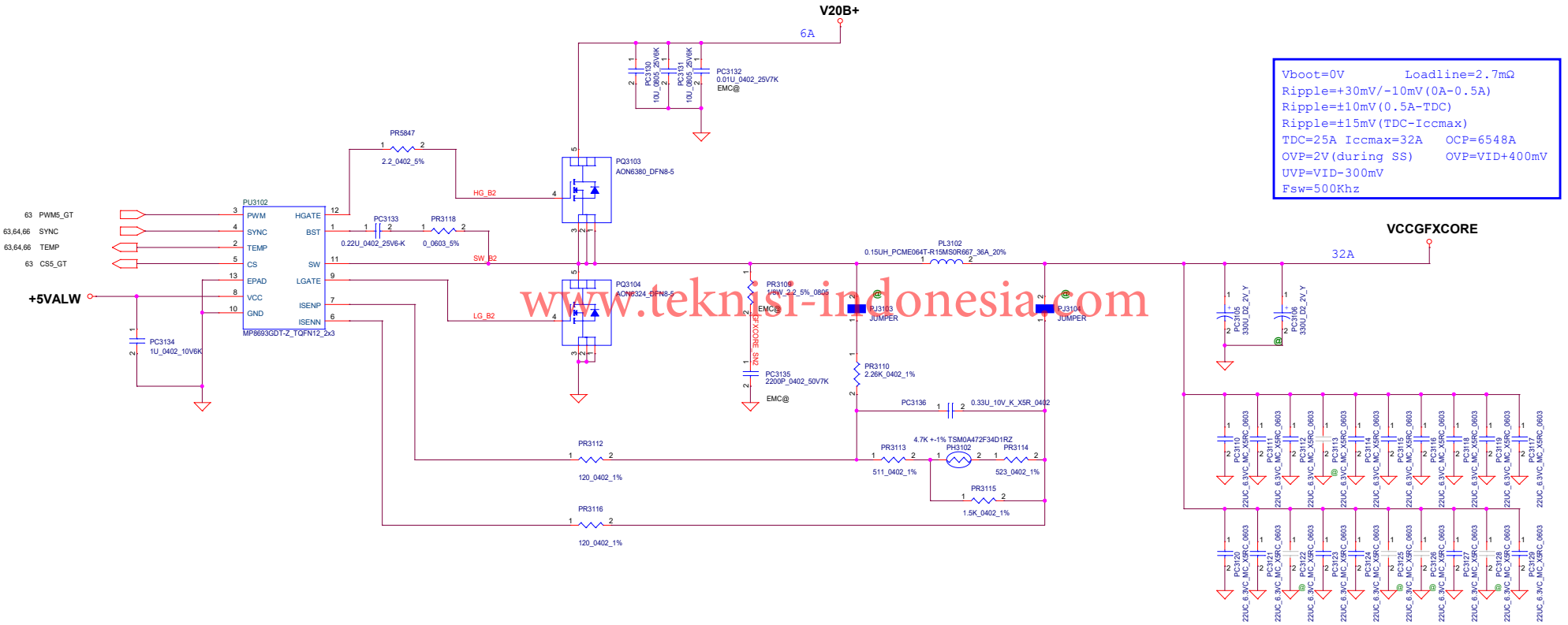

Vboot=0V Loadline=2.7mΩ
Ripple=+30mV/-10mV(0A-0.5A)
Ripple=±10mV(0.5A-TDC)
Ripple=±15mV(TDC-Iccmax)
TDC=25A Iccmax=32A OCP=6548A
OVP=2V(during SS) OVP=VID+400mV
UVP=VID-300mV
Fsw=500Khz

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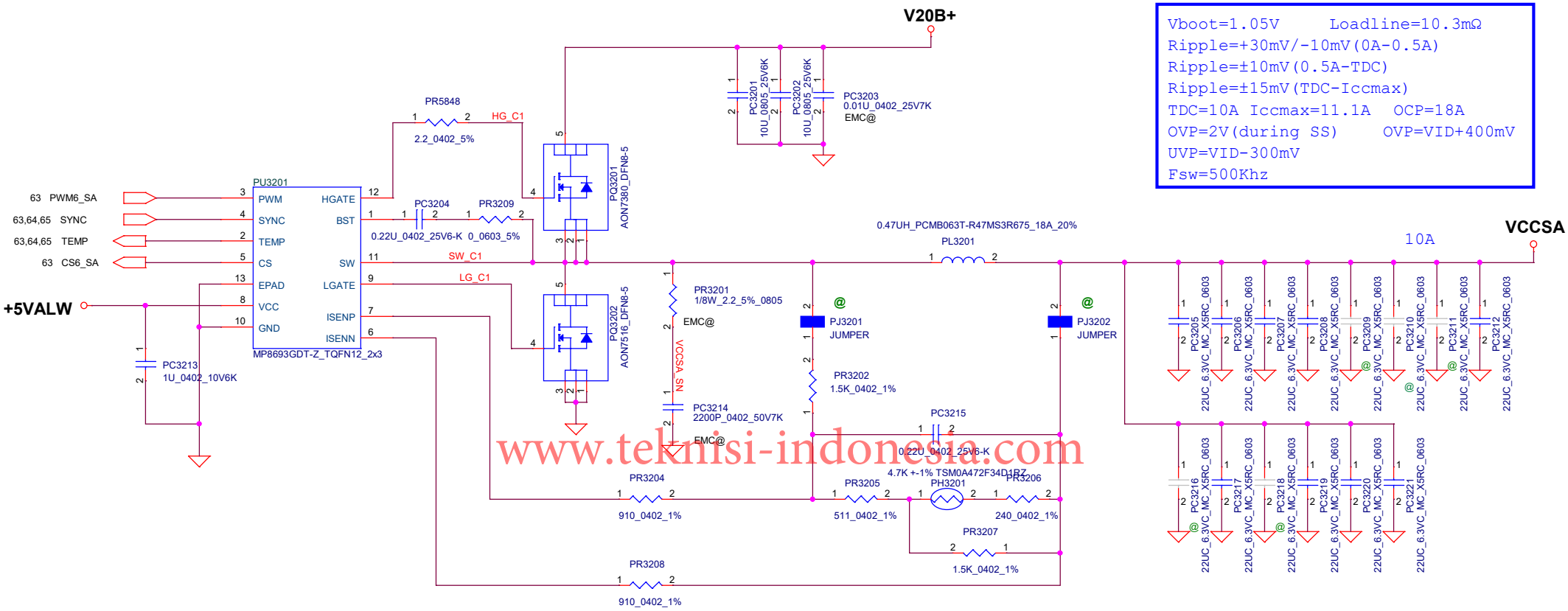

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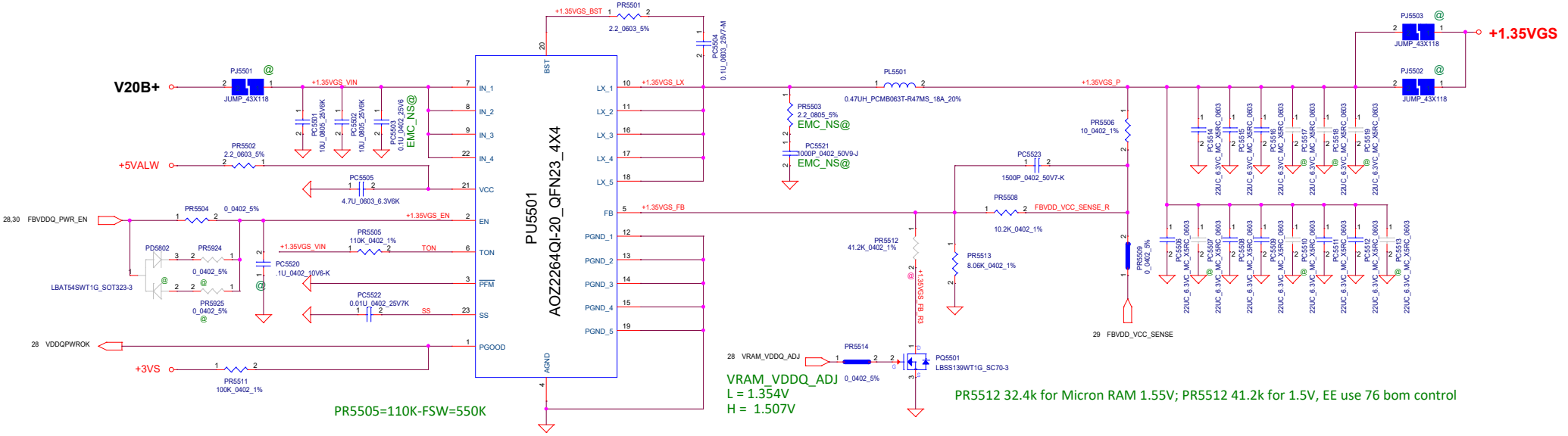

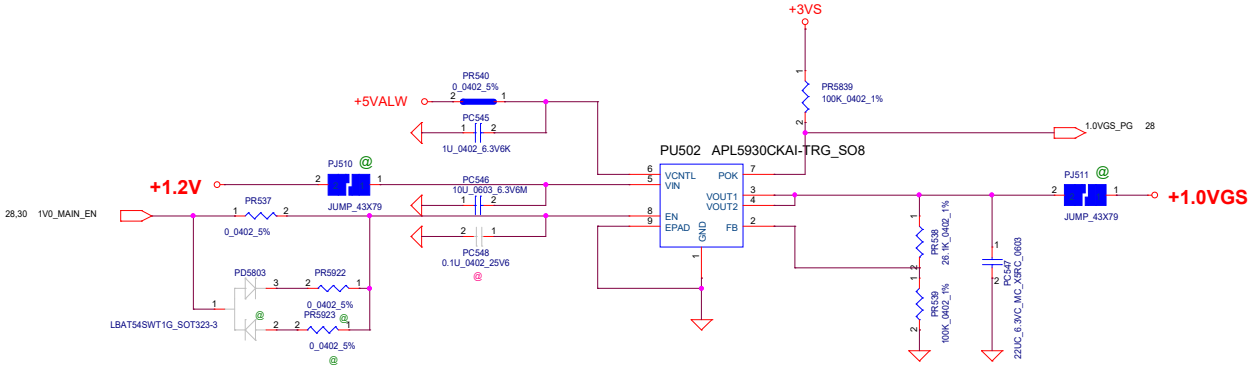

1.35VGS
FB:0.6V/1.35V
TDC=11A
ICCMAX=20A
OCP=25A
FSW=550K

LDO-1.0VGS
TDC:1A
iccmax:1.1A
FB:0.8V/1.0V

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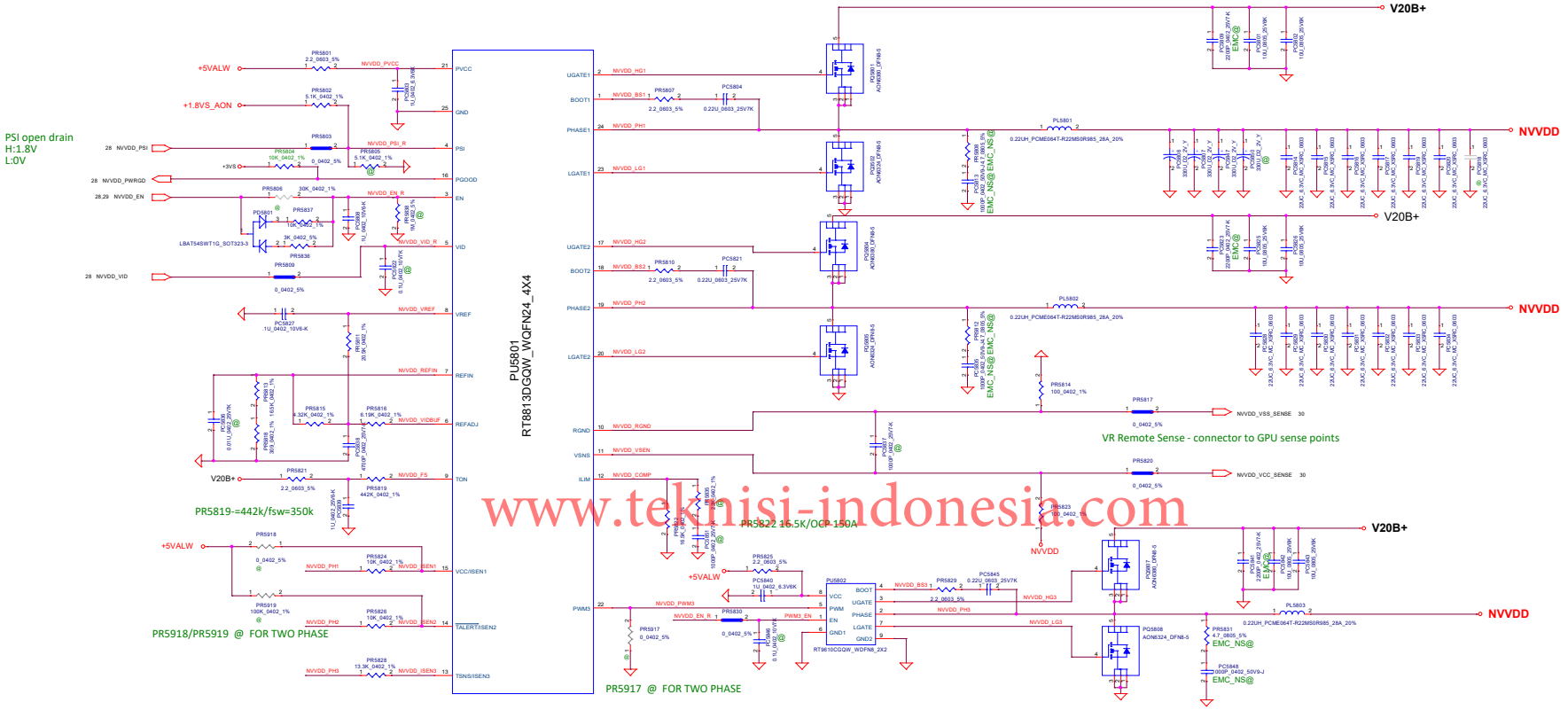

VBOOT:0.8V
VID voltage:0.3V~1.3V
TDC:50A
ICCMAX:100A
OCP:50A*3=150A
frequency:350K*3=1050khz

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