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GPC52 MB Schematic Document

LA-J643P

Version 1.0

Date : 2020/03/13

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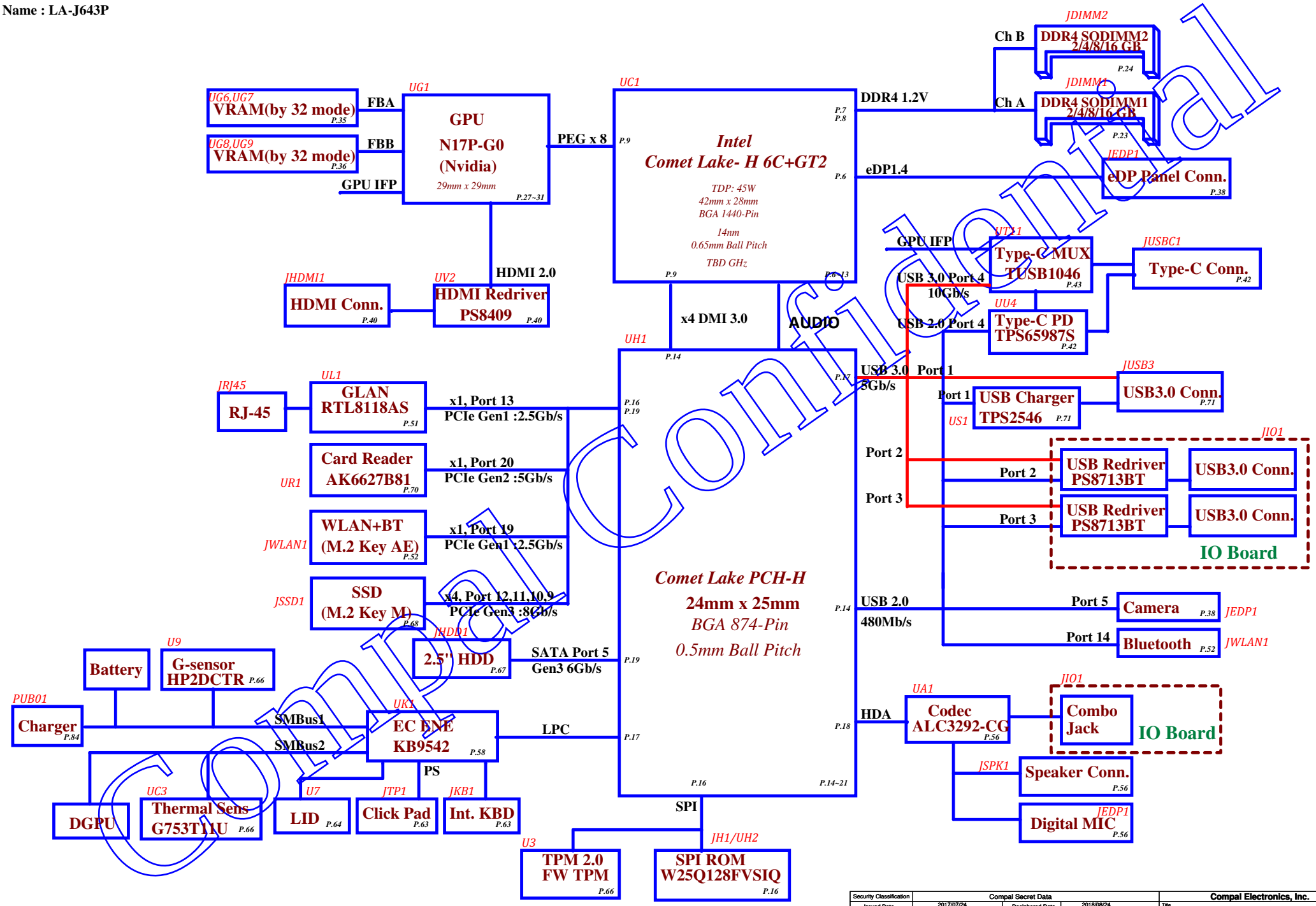
Model Name :Cyprus 1.1

File Name : LA-J643P



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Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID /PCB Revision	Rb	V_{AD_BID} min	V_{AD_BID} TYP	V_{AD_BID} Max	EC AD3
0 --> 0.1	0		0 V	0.300 V	0x00 - 0x13
1 --> 0.2	12K +/- 1%	0.347 V	0.354 V	0.36 V	0x14 - 0x1E
2 --> 0.3	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3 --> 0.4	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4 --> 0.5	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5 --> 0.6	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6 --> 0.7	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7 --> 0.8	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8 --> 0.9	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9 --> 1.0	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10 --> 1.1	130K +/- 1%	1.849 V	1.865 V	1.881V	0x88 - 0x96
11 --> 1.2	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12 --> 1.3	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13 --> 1.4	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14 --> 1.5	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15 --> 1.6	330K +/- 1%	2.521 V	2.533V	2.544 V	0xC0 - 0xC9
16 --> 1.7	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17 --> 1.8	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18 --> 1.9	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19 --> 2.0	NC	3.000 V	3.000 V		0xF1 - 0xFF

HSIO Port Table(CPU)

HSIO Port	Device	PCIE CLK&CLKREQ	HPD
PEG	DGPU (DIS)	CLK4 & & CLKREQ#4	
DDI1	TYPE-C PORT		DDPB_HPD0
DDI2	---		DDPC_HPD1
DDI3	---		
eDP	embedded Display		EDP_HPD

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCH SMBUS Address Table

PCH_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
PCH_SMBCLK PCH_SMBDATA	+3V_PCH_PRIM	JDIMM1	0X50	0XA0	0XA1
		JDIMM3	0X52	0XA4	0XA5
		TOUCH PAD			
PCH_SML0CLK PCH_SML0DATA	+3V_PCH_PRIM	NA			
PCH_SML1CLK PCH_SML1DATA	+3V_PCH_PRIM	EC	TBC	TBC	TBC
		GPU	0x41		

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBUS Port1	+3V_SMBUS	BAT	0x16	TBC	TBC
		CHGR	0x09	0x12	0x13
		G-Sensor	0x29	0x52	0x53
		PCH	TBC		
		GPU	0x41		
SMBUS Port2	+3VL	THERMAL	0x48	0X90	0x91
		PD	0x3F	0X71	0x70
		Type-C MUX	0x10 0x11	0X20 0X22	0x21 0x23

I2C Address Table

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
I2C_0_SCL I2C_0_SDA	+3VS				
I2C_1_SCL I2C_1_SDA	+3VS				

BOM Structure Table (1/2)

Function	Stuff	Un-Stuff
CFL-H SKU	CFL_H@	
DGPU SKU	DIS@	
VRAM STRAP/3G	3G@	
VRAM STRAP/6G	6G@	
GC6	GC6@	@GC6@
Touch		TS@
eSPI I/F	LPC@	FSPI@
TPM 9665	9665@	@9665@
TPM 9670	9670@	@9670@
CNVI	CNVI@	@CNVI@
EMI Components	EMI@ VGAEMI@	@EMI@
ESD Components	ESD@	@ESD@
RF Components	RF@	@RF@
XDP	XDP@	
ME Connector	CONN@	
STANDOFF	STD@	
For Signal Test	MP@	
VGA POWER SKU	VGA@	

HSIO Port Table(PCH)

HSIO Port	Capable	USB3.0	PCIE	SATA	Device	PCIE CLK&CLKREQ	NOTE
0	USB3.1_1(OTG)	1			USB3.1 PORT 1		
1	USB3.1_2 /	2			USB3.1 PORT 2		
2	USB3.1_3	3			USB3.1 PORT 3		
3	USB3.1_4	4			TYPE-C PORT		
4	USB3.1_5	5					
5	USB3.1_6	6					
6	USB3.1_7 / PCIE_1	7	1				
7	USB3.1_8 / PCIE_2	8	2				
8	USB3.1_9 / PCIE_3	9	3				
9	USB3.1_10 / PCIE_4	10	4				
10	PCIE_5 / GbE		5				
11	PCIE_6		6				
12	PCIE_7		7				
13	PCIE_8		8				
14	PCIE_9 / GbE		9				
15	PCIE_10		10				
16	PCIE_11 / SATA_0A		11	0	NGFF SSD Optane memory SSD	CLK2 & CLKREQ#2	Support SATA function on SATA#1
17	PCIE_12 / GbE / SATA_1A		12	1			
18	PCIE_13 / GbE / SATA_0B		13	0	LAN	CLK5 & CLKREQ#5	
19	PCIE_14 / SATA_1B		14	1			
20	PCIE_15 / SATA_2		15	2			
21	PCIE_16 / SATA_3		16	3			
22	PCIE_17 / SATA_4		17	4			
23	PCIE_18 / SATA_5		18	5	HDD		
24	PCIE_19		19		WLAN	CLK1 & CLKREQ#1	
25	PCIE_20		20		CARD READER	CLK3 & CLKREQ#3	
26	PCIE_21		21				
27	PCIE_22		22				
28	PCIE_23		23				
29	PCIE_24		24				

USB2.0 Port Table

USB2	Function
1	USB3.1 PORT 1
2	USB3.1 PORT 2
3	USB3.1 PORT 3
4	TYPE-C PORT
5	IR Camera
6	
7	Touch Panel
8	
9	
10	
11	
12	
13	
14	WLAN+BT Module

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	DS3
VIN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF
+VCC_SA	System Agent voltage Supply	ON	OFF	OFF	OFF	OFF
+VCC_GT/+VCC_GTX	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+VCC_EOPIO/+VCC_EDRAM	Processor EOPIO/EDRAM supply	ON	OFF	OFF	OFF	OFF
+1.05VALW	System +1.0V power rail	ON	ON	ON	ON*	OFF
+0.95VS_VCCIO	+1.0VS IO power rail	ON	ON	OFF	OFF	OFF
+1.05V_VCCMPHY	+1.0V power for PCH MODPHY rails	ON/OFF	ON/OFF	ON/OFF	ON/OFF	OFF
+0.95VS_DGPU	+0.95VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	ON	OFF	ON
+1.5VS_MEM_GFX	+1.5VS power rail for GPU/VRAM	ON	OFF	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*	OFF
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+2.5V	DDR4 +2.5Vpp power rail	ON	ON	ON	OFF	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VALW	+3VALW power for PCH suspend rails	ON	ON	ON	ON*	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON	ON
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

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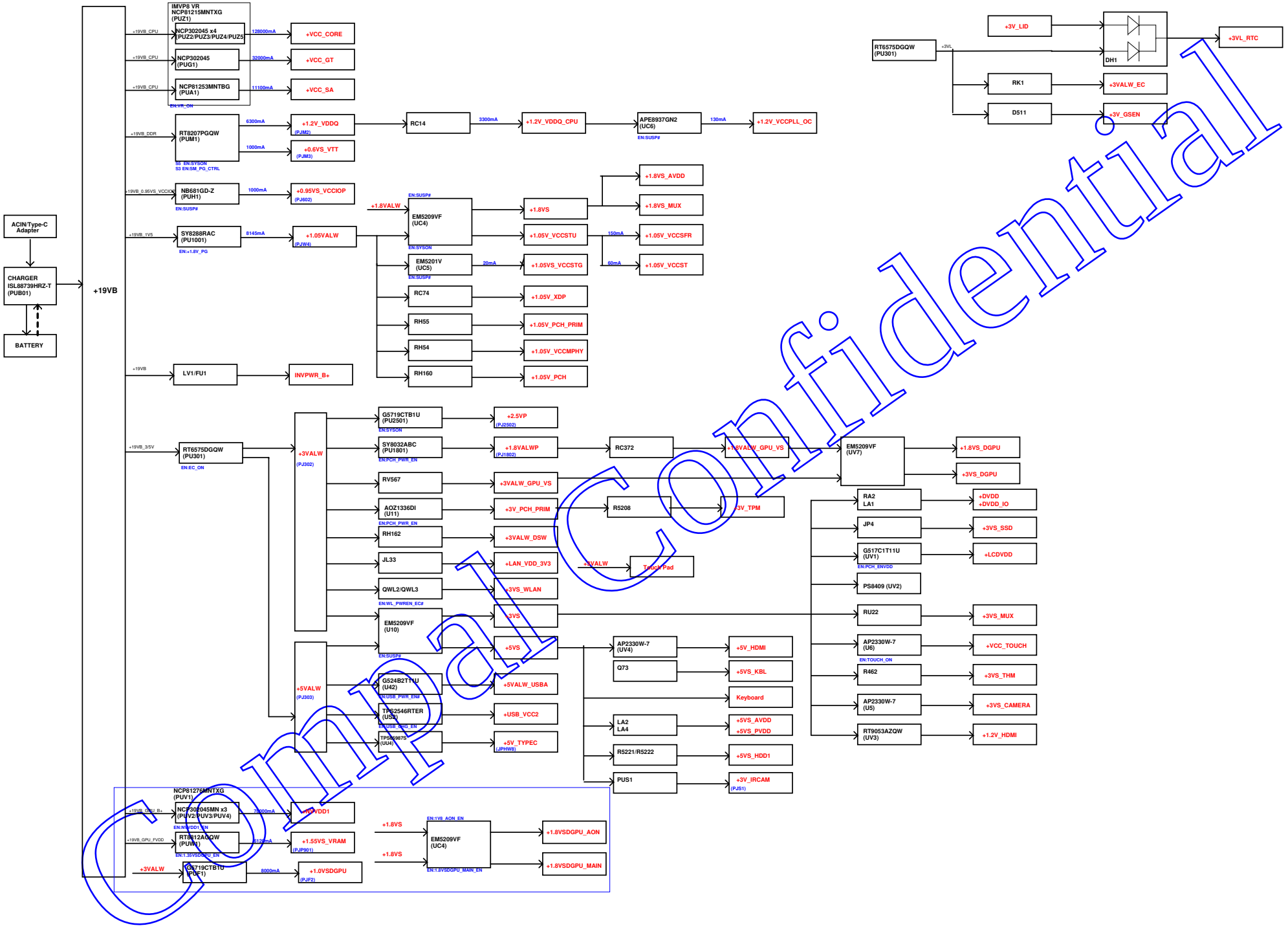

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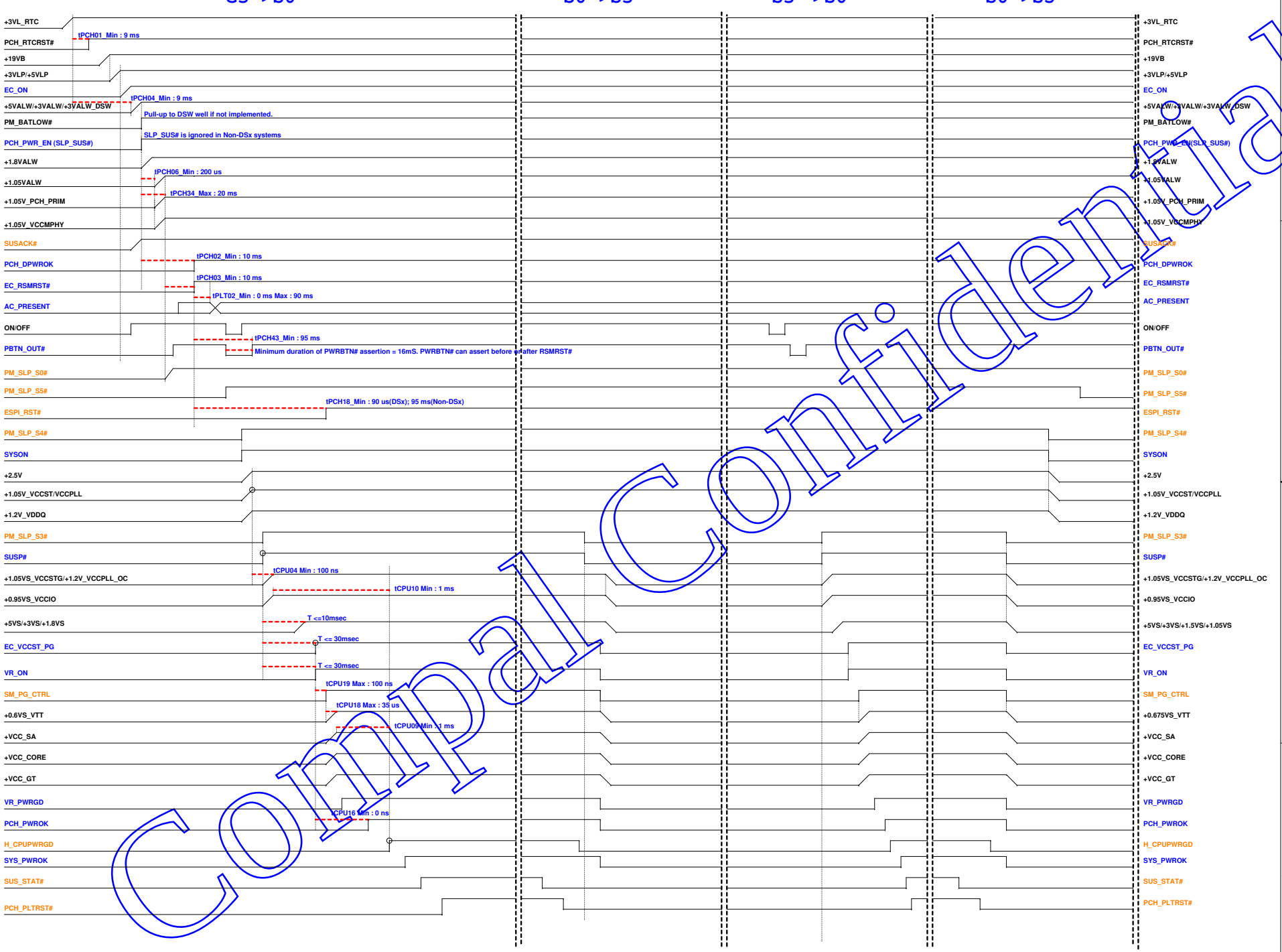
[DDX03 PWR Sequence_CFL-H 6+2_DDR4]



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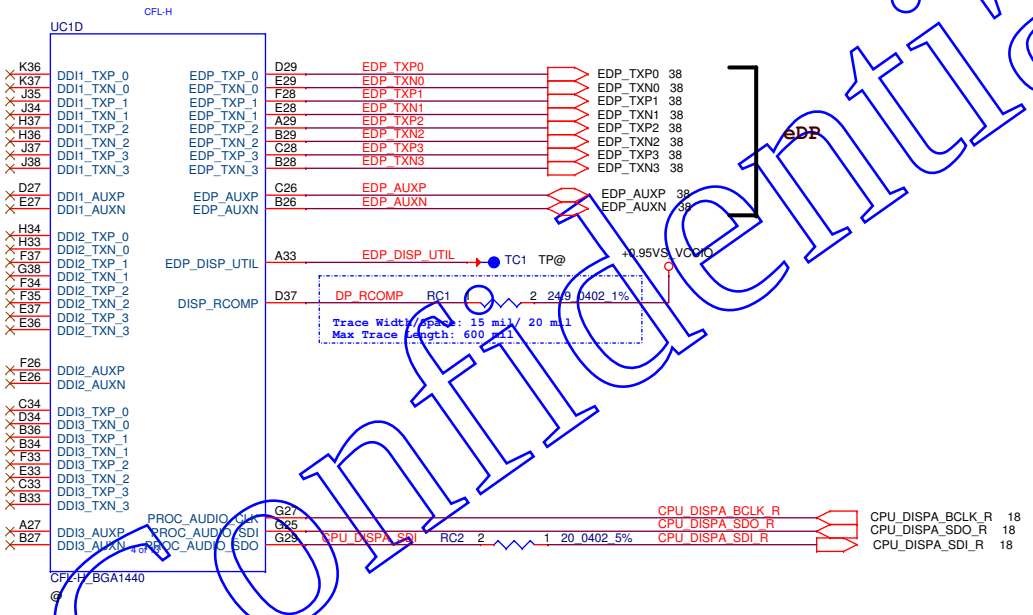

Comet Lake-H CPU SKU

UC1

CML-H_BGA1440

ES2@ SA0000D3N00

S IC A32 CL8070104398908 QTJ2 R0 2.4G S

UC1

CML-H_BGA1440

QU9W@ SA0000DCP00

S IC A32 CL8070104399510 QU9W R1 2.5G S

UC1

CML-H_BGA1440

QU9U@ SA0000DCN00

S IC A32 CL8070104399315 QU9U R1 2.6G S

R3

UC1

CFL-H_BGA1440

SRF6X@ SA0000COG30

S IC CL8068404121905 SRF6X U0 2.4G A32

UC1

CFL-H_BGA1440

SRF6U@ SA0000COF40

S IC CL8068404121817 SRF6U U0 2.6G A32!

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CHANNEL-A

Interleaved Memory

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CHANNEL-B

Interleaved Memory

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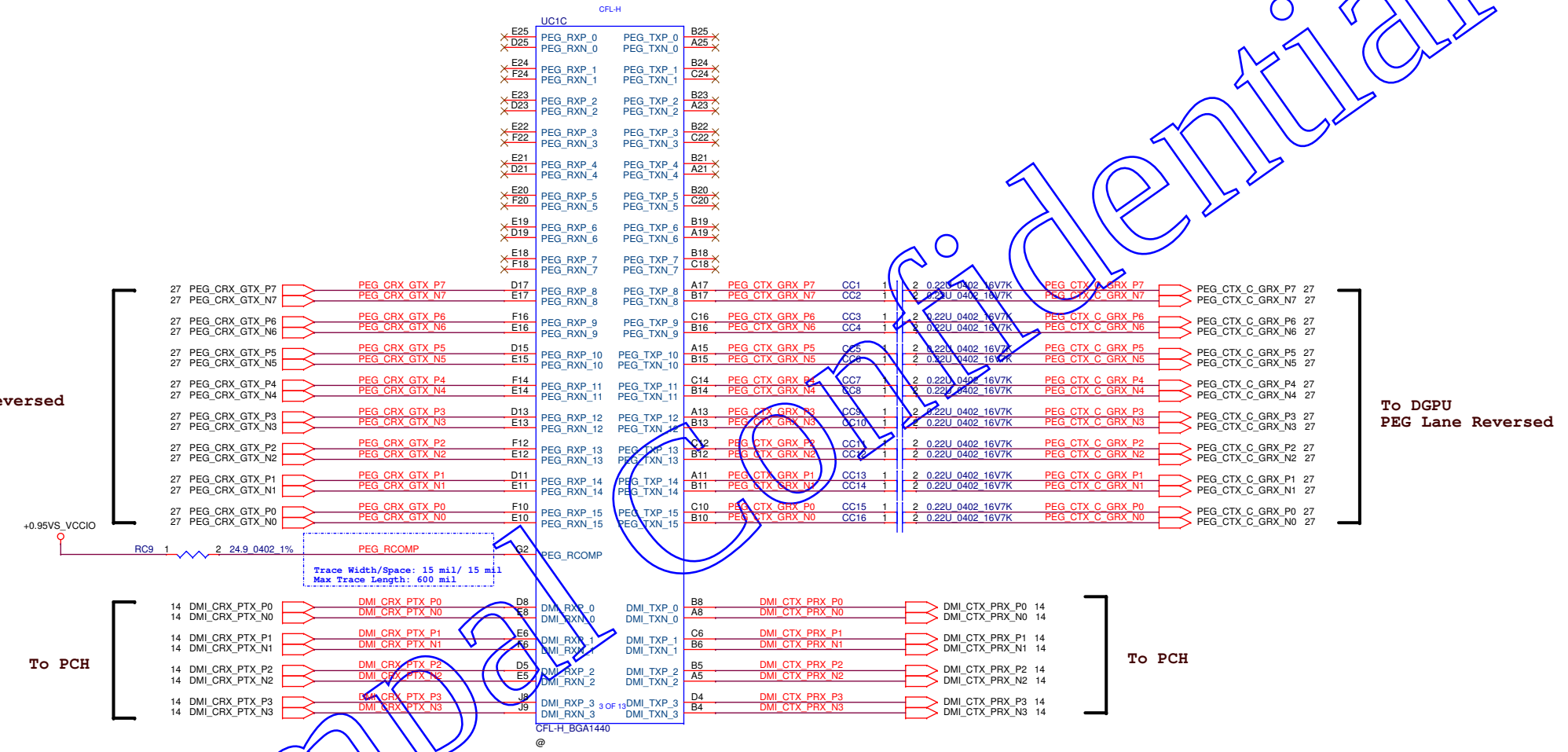

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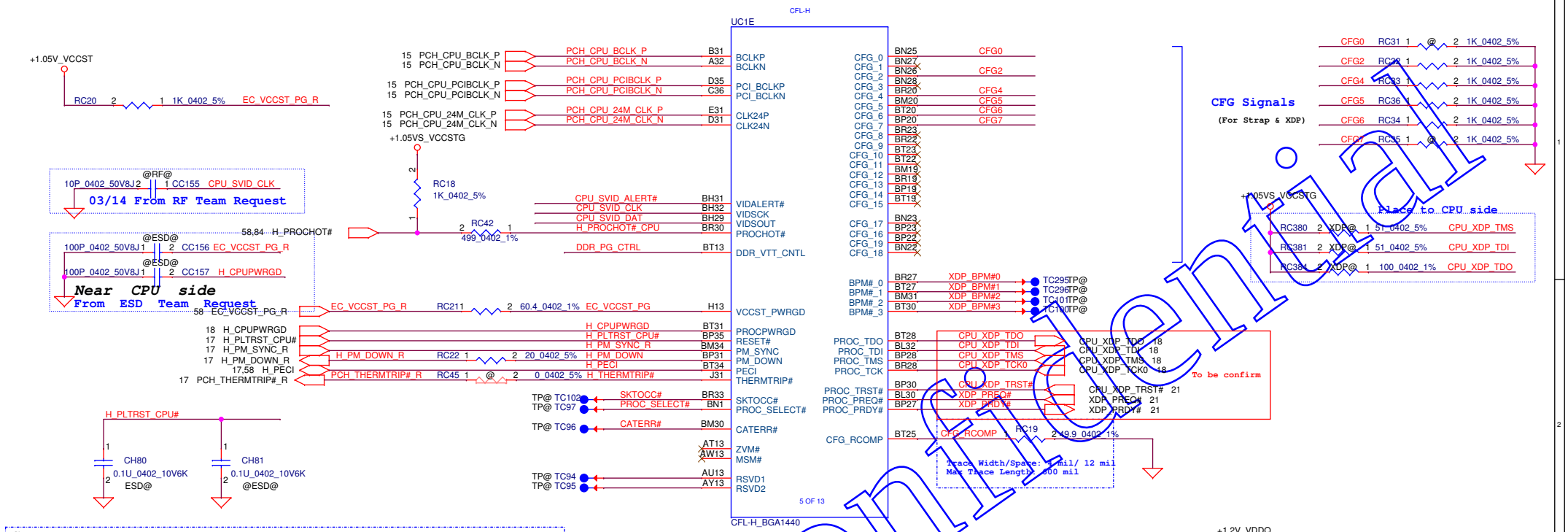

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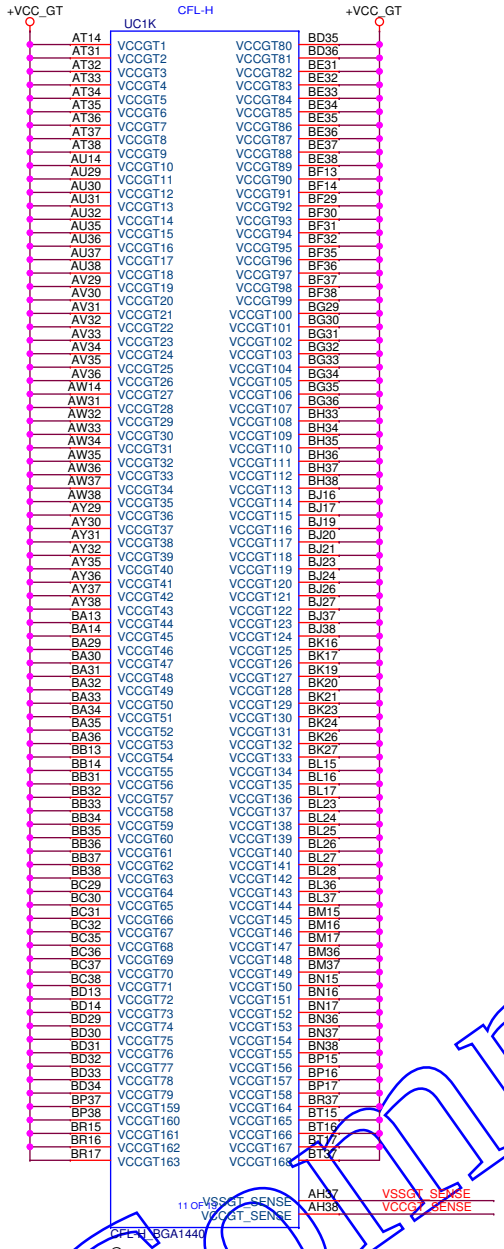
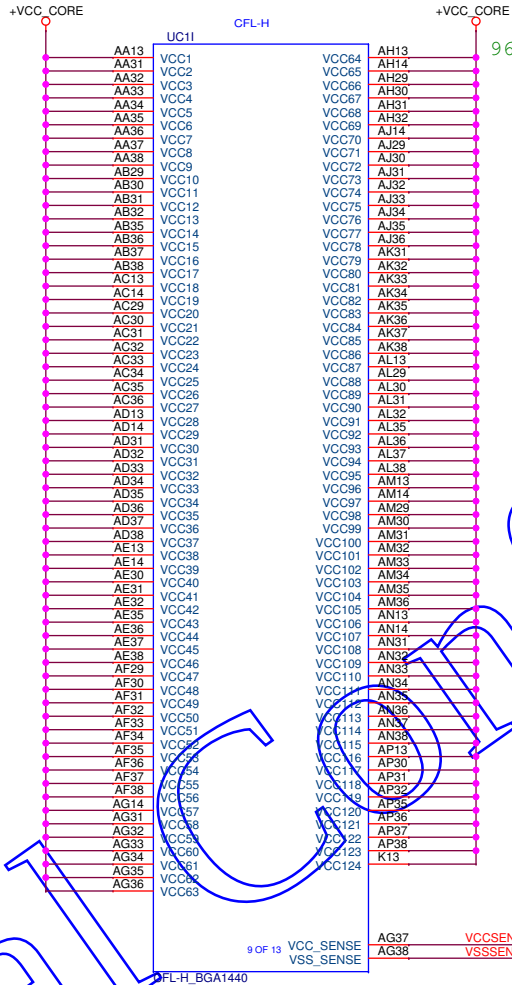
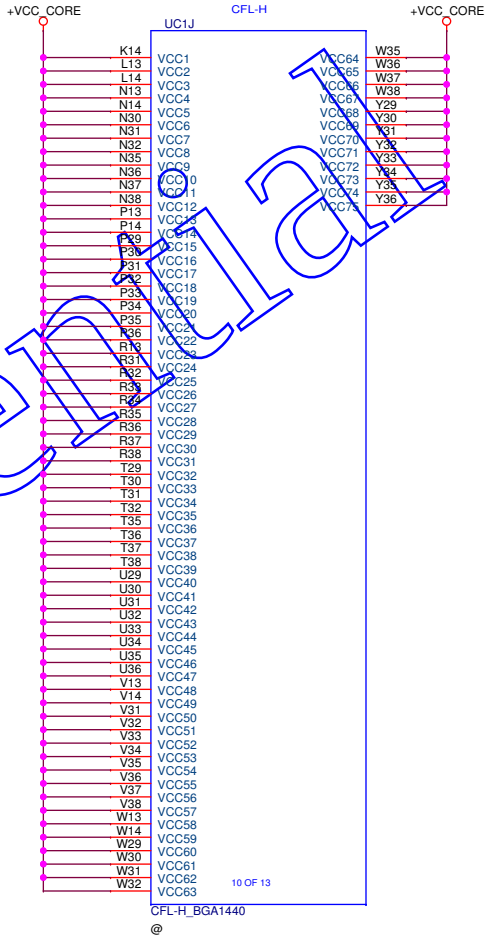
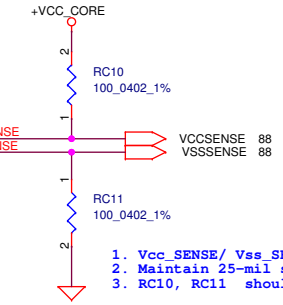
GT
55000mA(Hexa Core GT2)



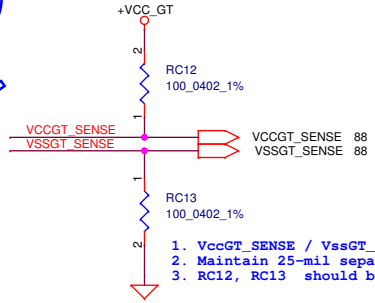


96000mA(Hexa Core GT2)





1. Vcc_SENSE/ Vss_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC10, RC11 should be placed within 2 inches (50.8 mm) of CPU



1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC12, RC13 should be placed within 2 inches (50.8 mm) of CPU

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Title: CFL-H(6/8)VCC CORE/GT

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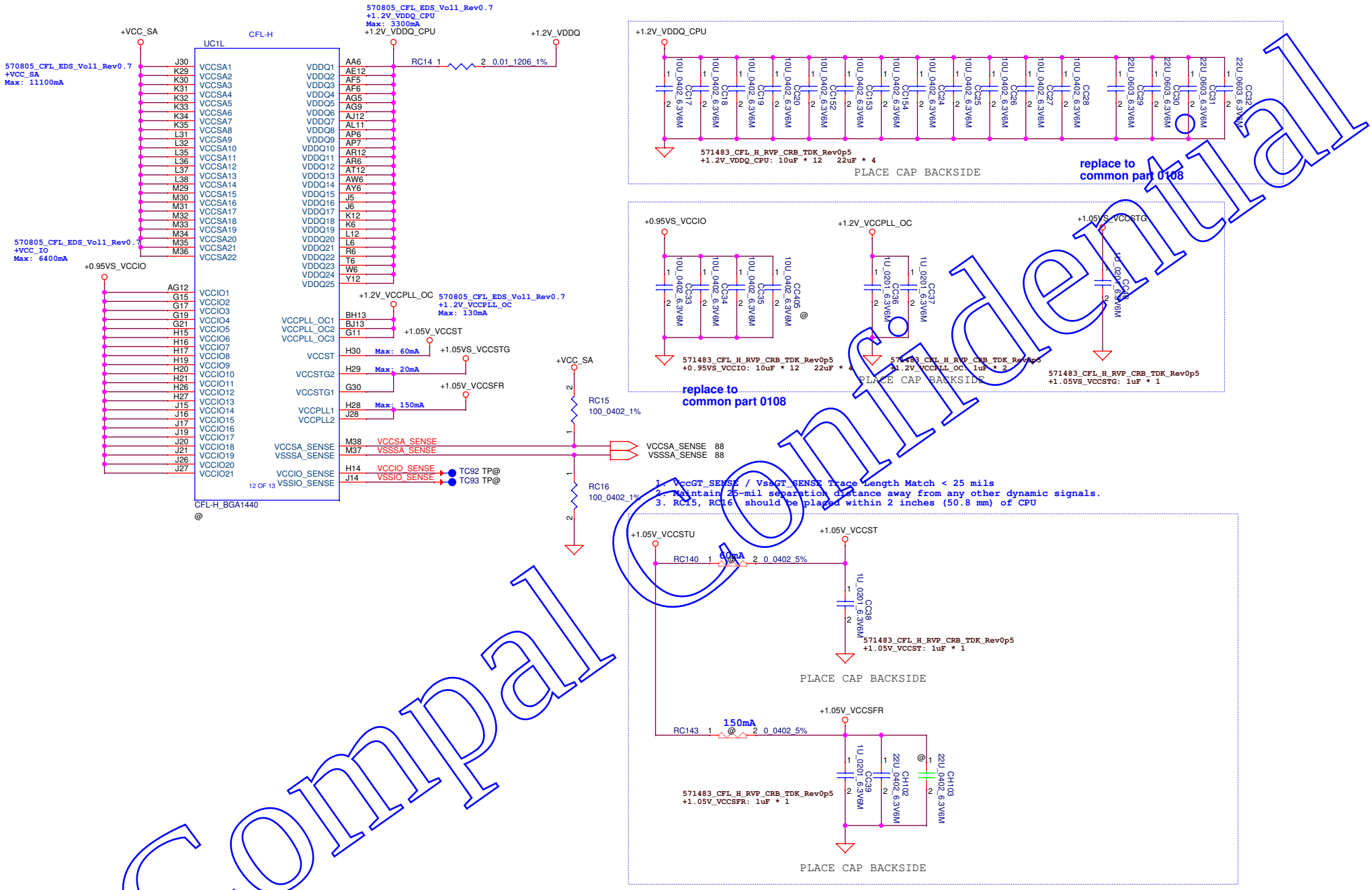

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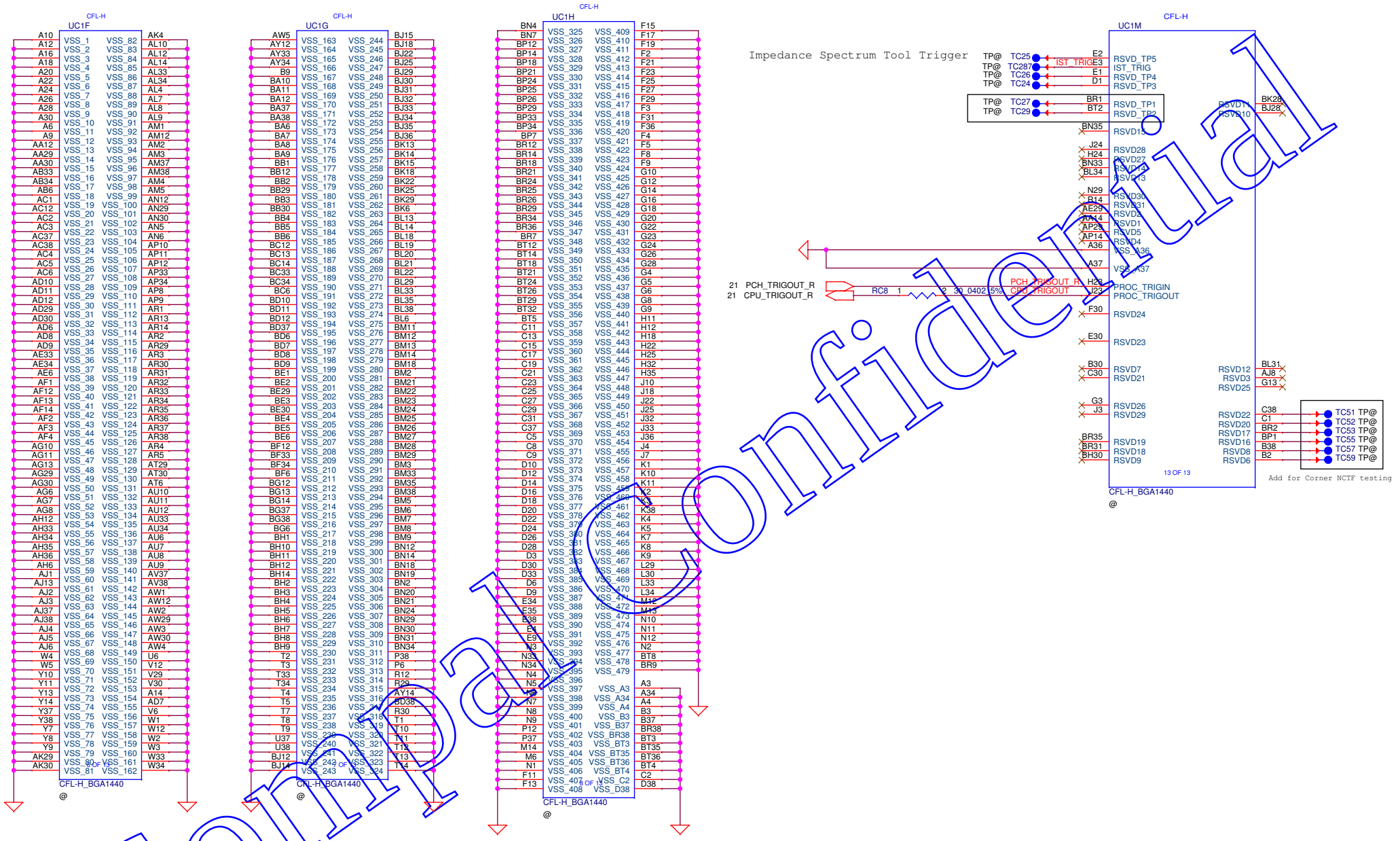

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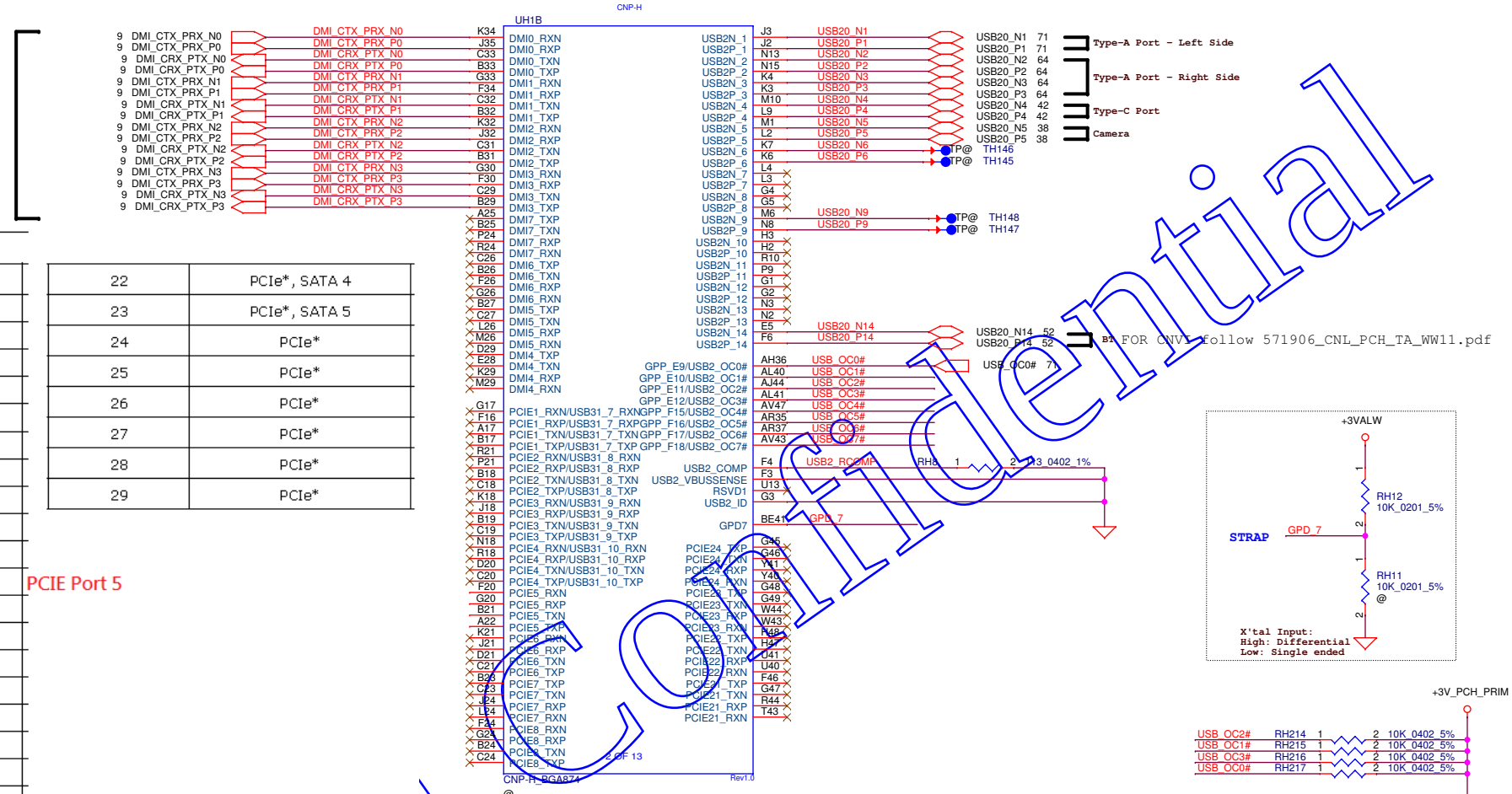
Title	CFL-H(8/8)GND/RSVD		
Size: Custom	Document Number: LA-J643P		Rev: 1.0
Date: Friday, March 13, 2020	Sheet 13 of 100		



Flex I/O Lane	HM370
0	USB3.1 Gen1/Gen2
1	USB3.1 Gen1/Gen2
2	USB3.1 Gen1/Gen2
3	USB3.1 Gen1/Gen2
4	USB3.1 Gen1
5	USB3.1 Gen1
6	USB3.1 Gen1
7	USB3.1 Gen1
8	N/A
9	N/A
10	GbE
11	N/A
12	N/A
13	N/A
14	PCIe*, GbE
15	PCIe*
16	PCIe*, SATA 0A
17	PCIe*, GbE, SATA 1A
18	PCIe*, GbE, SATA 0B
19	PCIe*, SATA 1B
20	PCIe*
21	PCIe*

PCIE Port 5

22	PCIe*, SATA 4
23	PCIe*, SATA 5
24	PCIe*
25	PCIe*
26	PCIe*
27	PCIe*
28	PCIe*
29	PCIe*

PCH-H Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3 Cycle Router #1				PCIe* Controller #4				PCIe* Controller #5 Cycle Router #3				PCIe* Controller #6 Cycle Router #2			
Flex I/O Lane #		6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
HM370	1x4									RP 9				RP 13				RP 17				RP 21			
	1x4 LR									RP 9				RP 13				RP 17				RP 21			
	2x2									RP 9		RP 11		RP 13		RP 15		RP 17		RP 19		RP 21		RP 23	
	1x2+2x1									RP 9		RP 11	RP 12	RP 13		RP 15	RP 16	RP 17		RP 19	RP 20	RP 21		RP 23	RP 24
	2x1+1x2									RP 12	RP 11	RP 9		RP 16	RP 15	RP 13		RP 20	RP 19	RP 17		RP 24	RP 23	RP 21	
	4x1									RP 9	RP 10	RP 11	RP 12	RP 13	RP 14	RP 15	RP 16	RP 17	RP 18	RP 19	RP 20	RP 21	RP 22	RP 23	RP 24
QM370	1x4						RP 5			RP 9				RP 13				RP 17				RP 21			
	1x4 LR						RP 5			RP 9				RP 13				RP 17				RP 21			
	2x2						RP 5		RP 7	RP 9		RP 11		RP 13		RP 15		RP 17		RP 19		RP 21		RP 23	
	1x2+2x1						RP 5		RP 7	RP 8	RP 9		RP 11	RP 12	RP 13		RP 15	RP 16	RP 17		RP 19	RP 20	RP 21		RP 23	RP 24
	2x1+1x2					RP 8	RP 7		RP 5	RP 12	RP 11	RP 9		RP 16	RP 15	RP 13		RP 20	RP 19	RP 17		RP 24	RP 23	RP 21	
	4x1					RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12	RP 13	RP 14	RP 15	RP 16	RP 17	RP 18	RP 19	RP 20	RP 21	RP 22	RP 23	RP 24
CM246	1x4		RP 1				RP 5			RP 9				RP 13				RP 17				RP 21			
	1x4 LR		RP 1				RP 5			RP 9				RP 13				RP 17				RP 21			
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9		RP 11		RP 13		RP 15		RP 17		RP 19		RP 21		RP 23	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12	RP 13		RP 15	RP 16	RP 17		RP 19	RP 20	RP 21		RP 23	RP 24
	2x1+1x2	RP 4	RP 3		RP 1	RP 8	RP 7		RP 5	RP 12	RP 11	RP 9		RP 16	RP 15	RP 13		RP 20	RP 19	RP 17		RP 24	RP 23	RP 21	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12	RP 13	RP 14	RP 15	RP 16	RP 17	RP 18	RP 19	RP 20	RP 21	RP 22	RP 23	RP 24

The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
—A maximum of 16 PCIe* Ports (or devices) can be enabled
• When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 – GbE (0 or 1)
– PCIe* Lanes 1–4 (PCIe* Controller #1), 5–8 (PCIe* Controller #2), 9–12 (PCIe* Controller #3), 13–16 (PCIe* Controller #4), 17–20 (PCIe* Controller #5), and 21–24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
– A maximum of 6 SATA Ports (or devices) can be enabled
– SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
– SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
– A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
– A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (IntelR Rapid Storage Technology) PCIe* storage devices
– x2 and x4 PCIe* NVMe SSD
– x2 IntelR Optane? Memory Device
– See the "PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers,configurations , and lanes that can be used for IntelR Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the IntelR Flash Image Tool (FIT) tool.

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Title: PCH(1/8)DMI/PCIE/USB2

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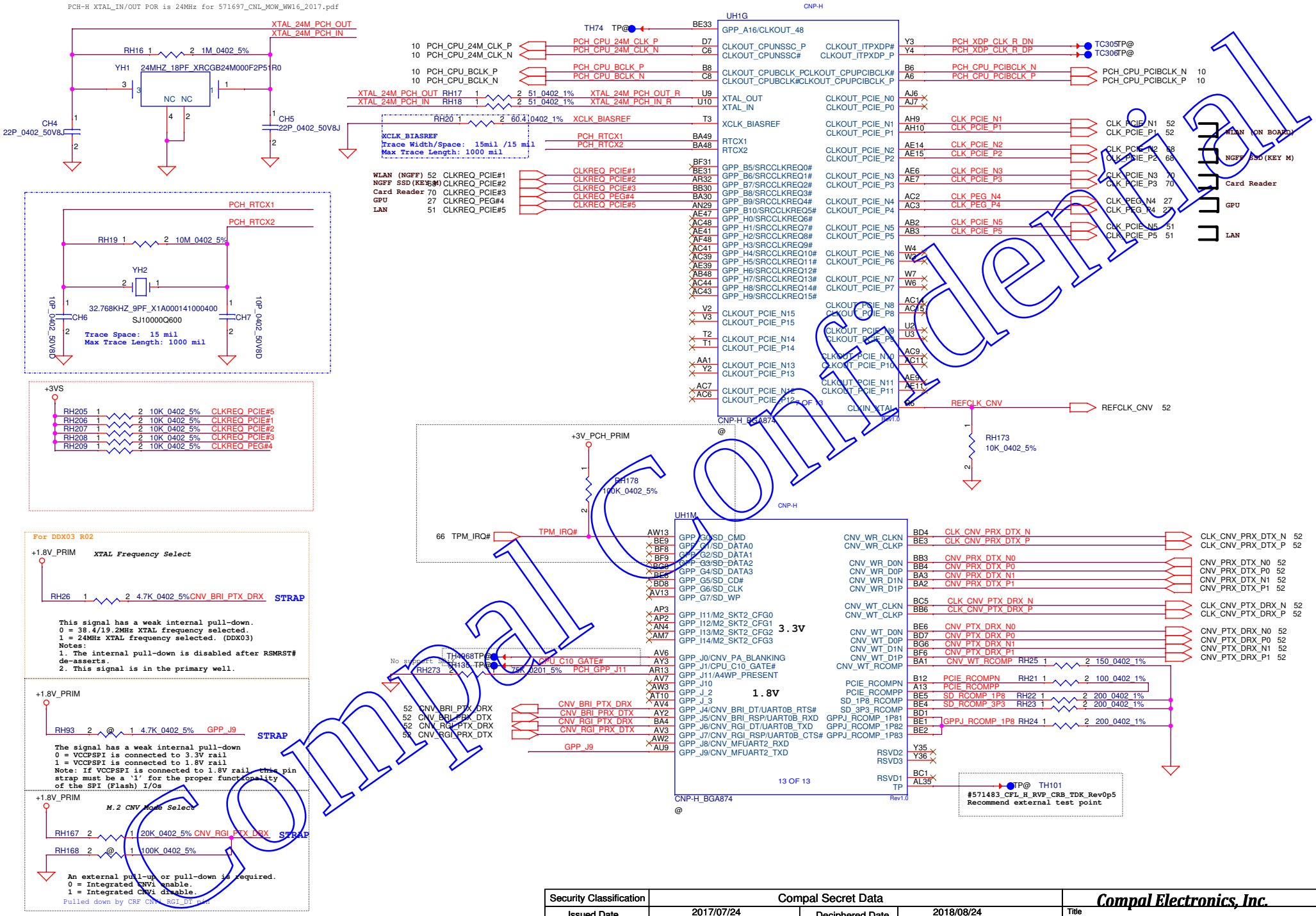

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Compal Electronics, Inc.

Title: **PCH(2/8)CLK/CNVI**

Size	Document Number	Rev
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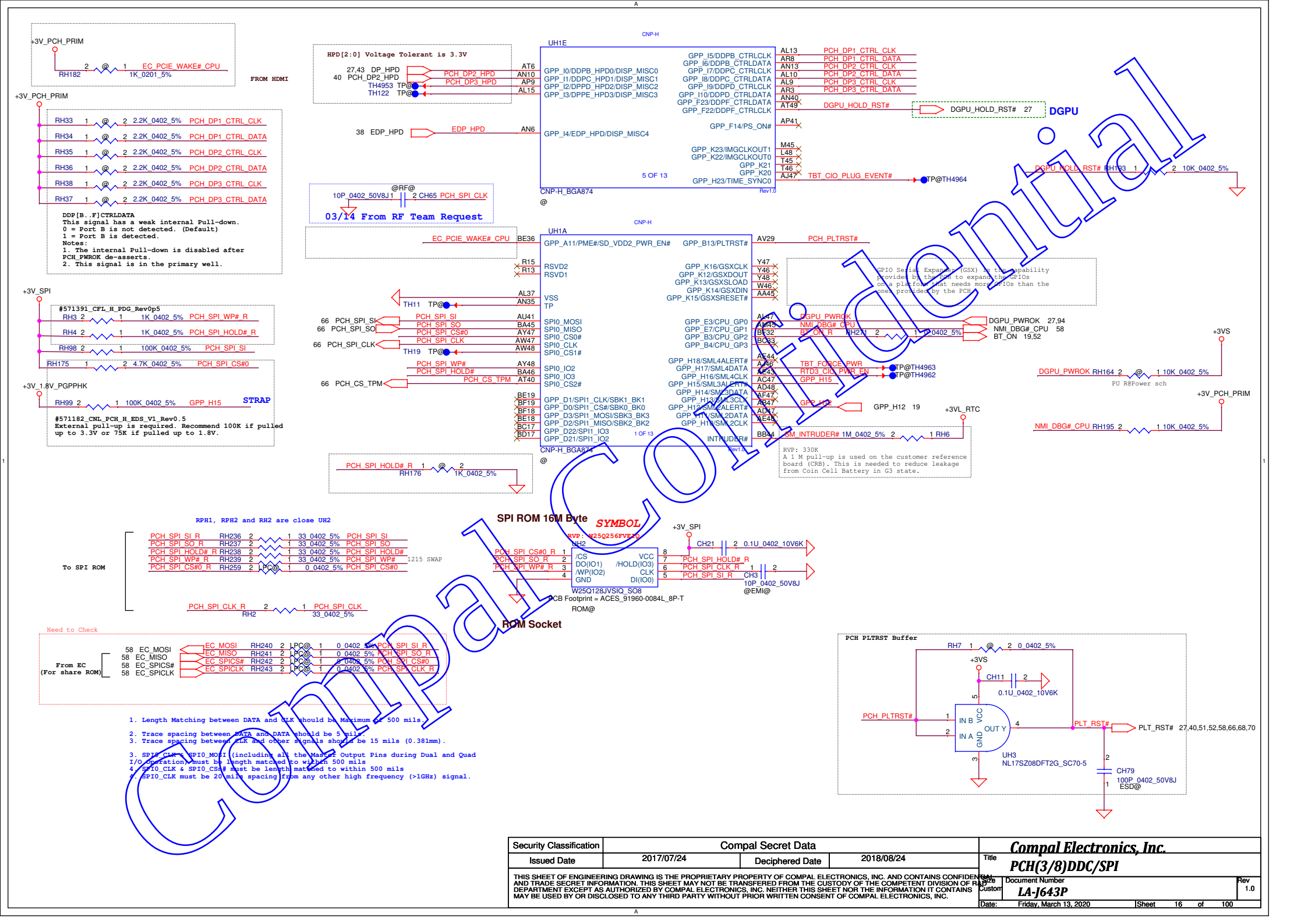
Date: Friday, March 13, 2020	Sheet 15 of 100	



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Title: PCH(3/8)DDC/SPI			
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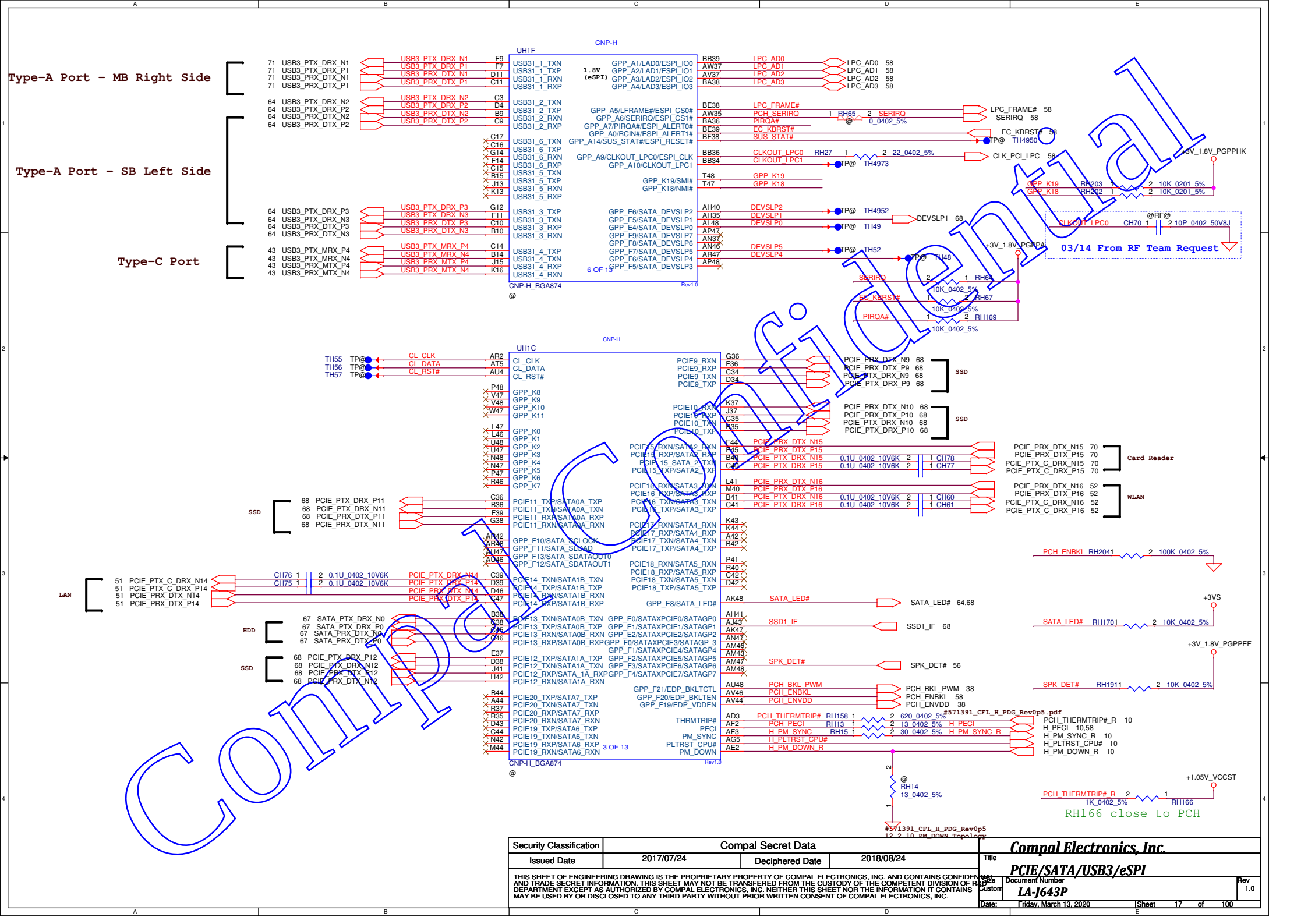
Date: Friday, March 13, 2020	Sheet 16 of 100		


Type-A Port - MB Right Side
Type-A Port - SB Left Side
Type-C Port
CNP-H
UH1F
CNP-H_BGA874
6 OF 13
UH1C
3 OF 13
LAN
HDD
SSD
Card Reader
WLAN
03/14 From RF Team Request
RH166 close to PCH
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Compal Electronics, Inc.
PCIE/SATA/USB3/eSPI
LA-J643P
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Issued Date 2017/07/24
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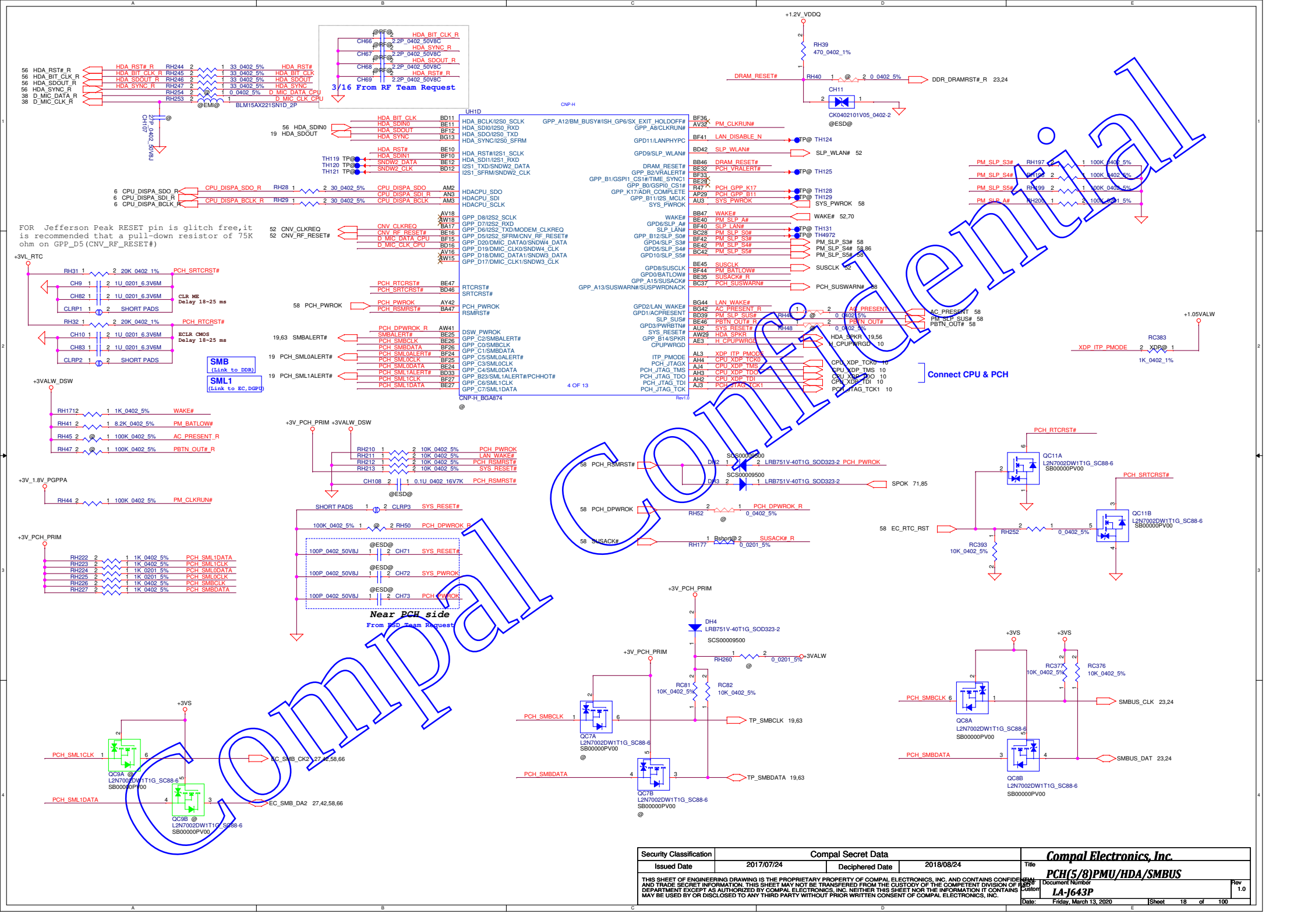

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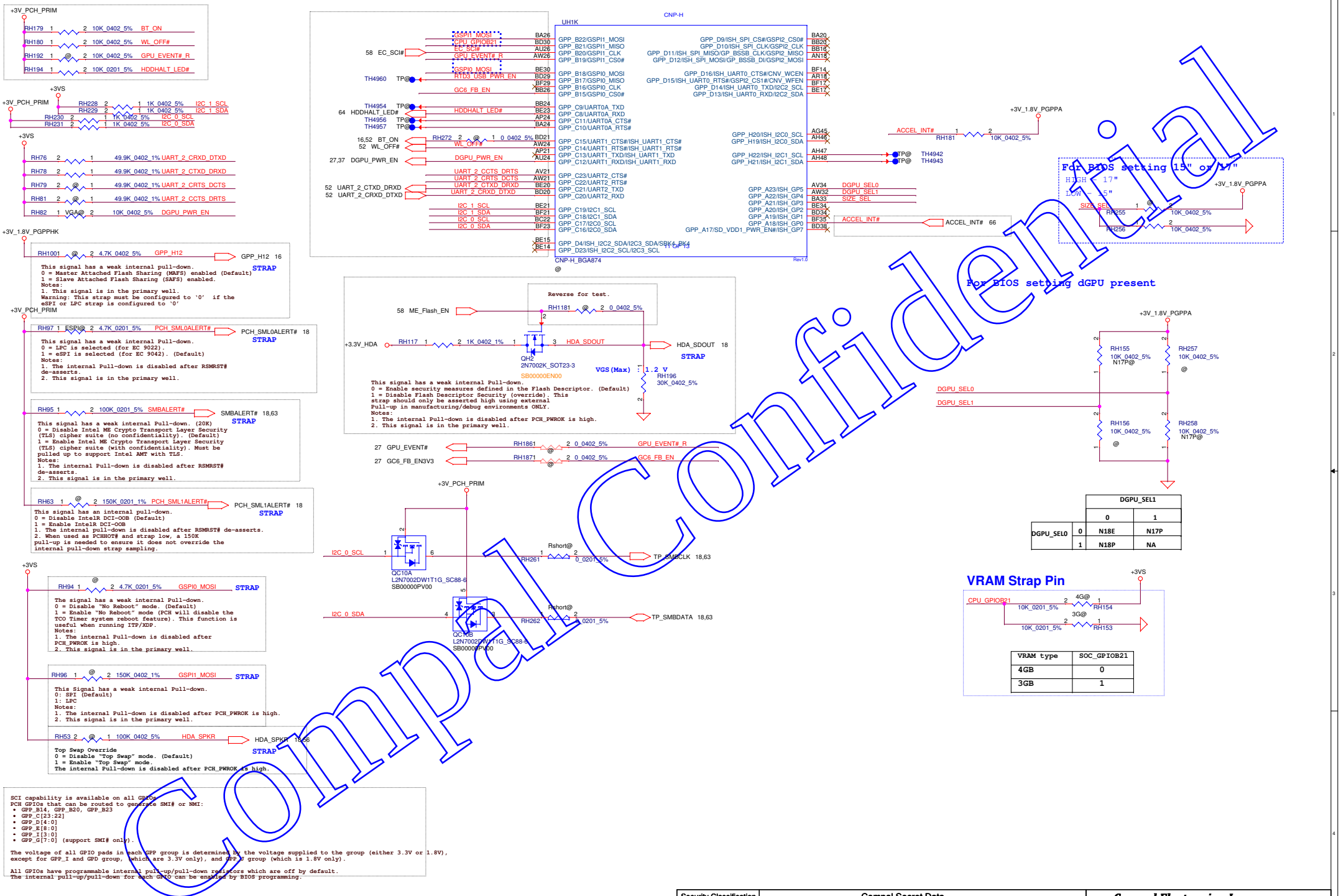
Date: Friday, March 13, 2020	Sheet 18 of 100		



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Title: PCH(6/8)GPIO/I2C/UART/STRAP			
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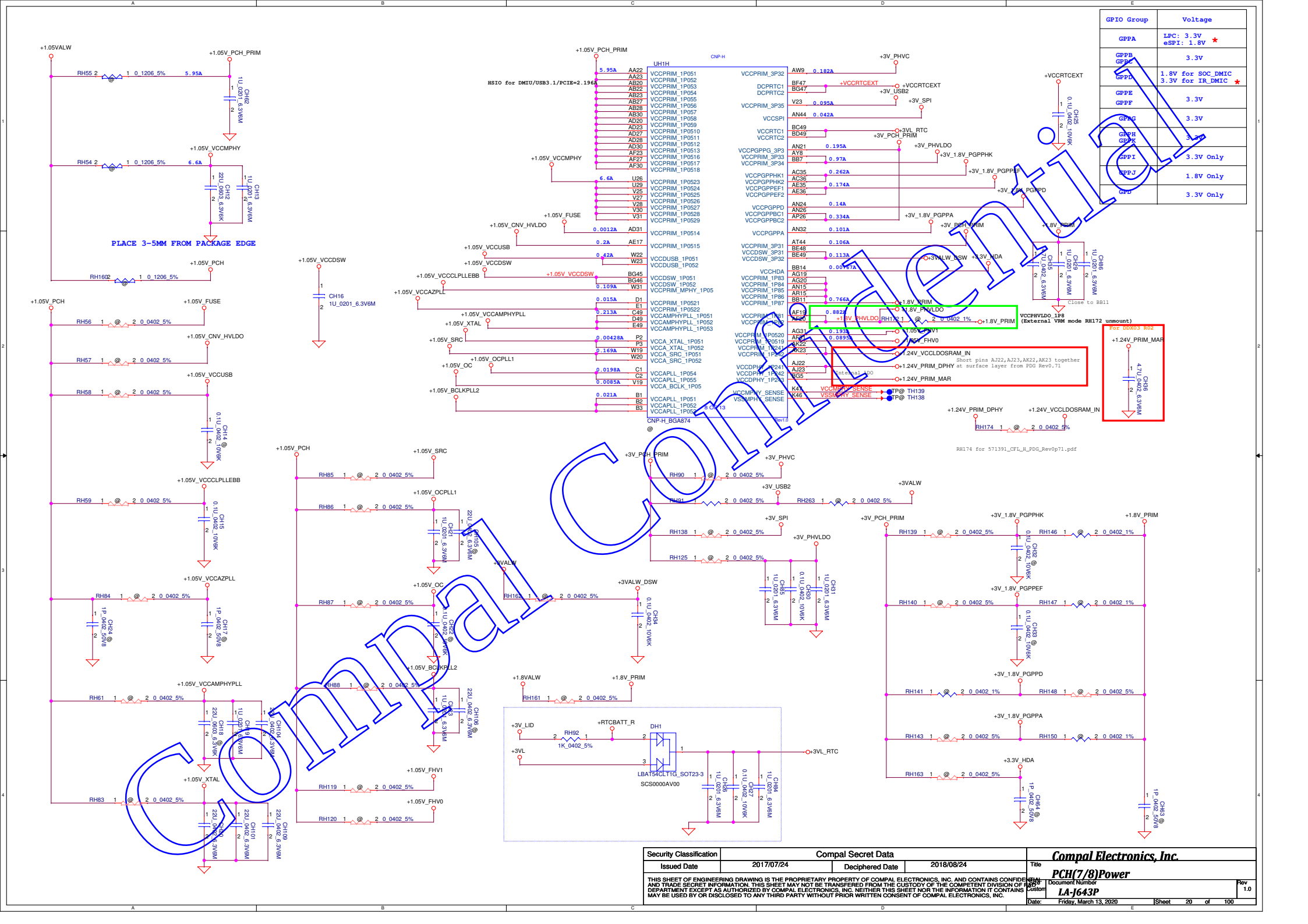
Date: Friday, March 13, 2020	Sheet 19 of 100		


GPIO Group
Voltage
GPPA
LPC: 3.3V
eSPI: 1.8V
GPPB
GPPC
3.3V
GPPD
1.8V for SOC_DMIC
3.3V for IR_DMIC
GPPE
GPPF
3.3V
GPPG
3.3V
GPPH
GPPK
3.3V
GPPI
3.3V Only
GPPJ
1.8V Only
GPD
3.3V Only
PLACE 3-5MM FROM PACKAGE EDGE
HSIO for DMIU/USB3.1/PCIE=2.196A
UH1H
CNP-H
CNP:H_BGA874
VCCPHVLDO_1P8
(External VRM mode RH172 unmount)
For DDX03 R02
Short pins AJ22,AJ23,AK22,AK23 together at surface layer from PDG Rev0.71
RH174 for 571391_CFL_H_PDG_Rev0p71.pdf
Close to BB11
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PCH(7/8)Power
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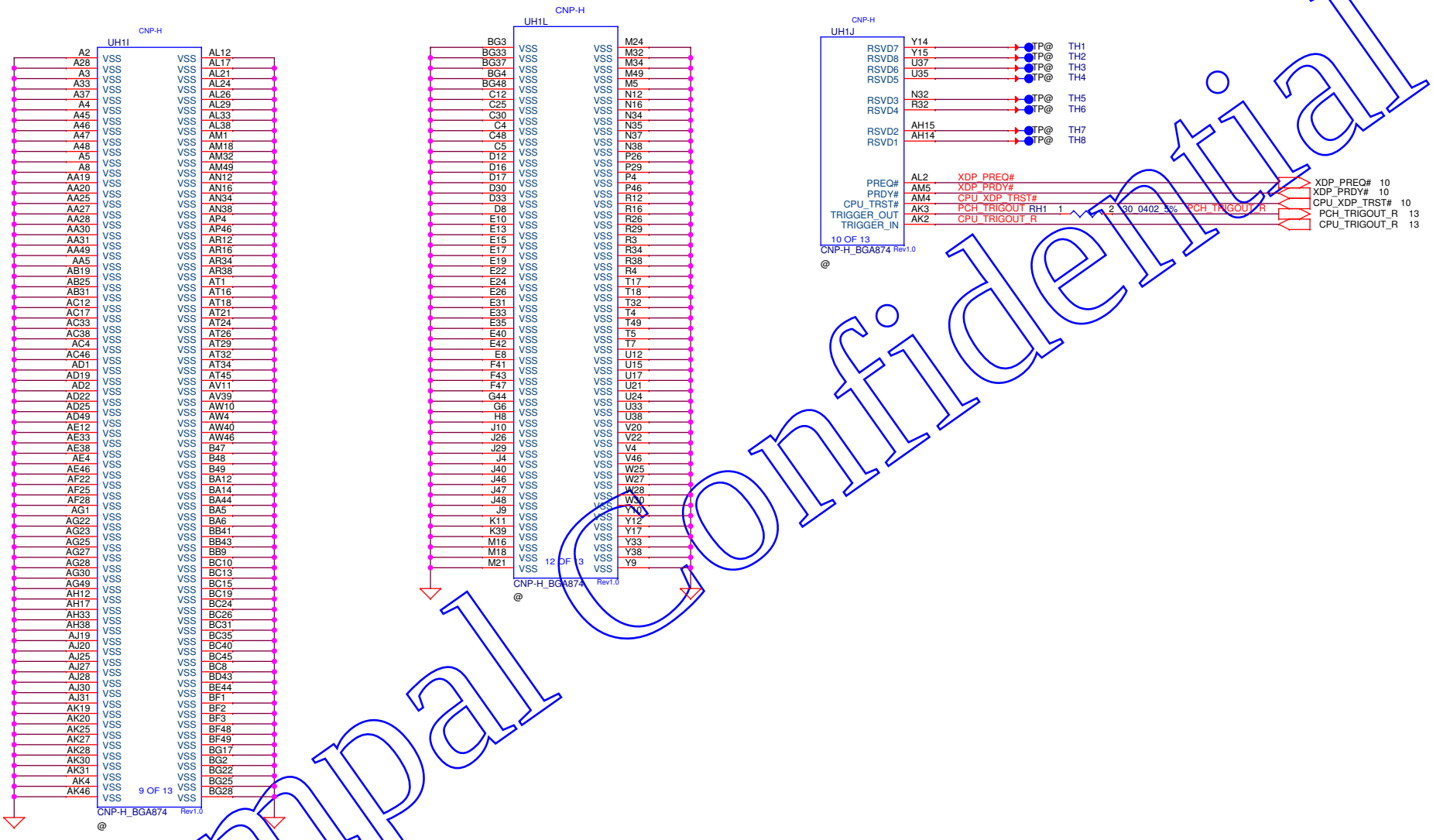

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CHANNEL-A

TOP REVERSE TYPE (4 mm)

Interleaved Memory

TOP: JDIMM1 CONN Non-ECC DIMM

PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

RD1 0_0402_5% SA0_CHA_DIM1
RD4 0_0402_5% SA1_CHA_DIM1
RD2 0_0402_5% SA2_CHA_DIM1
RD3 0_0402_5%
RD5 0_0402_5%
RD6 0_0402_5%

SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

PLACE NEAR TO PIN

Layout Note: Place near JDIMM1.257,259

Layout Note: Place near JDIMM1.258

Layout Note: PLACE THE CAP near JDIMM1. 164

Layout Note: Place near JDIMM1

JDIMM1B REVERSE

JDIMM1A REVERSE

ARGOS_D4AR0-26015-1P40 CONN@

For ECC DIMM

PLACE NEAR TO SODIMM

DIMM Side

CPU Side

VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

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Compal Electronics, Inc.	
Title	DDRIV_CHA: DIMM0
Document Number	LA-J643P
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Date:	Friday, March 13, 2020
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CHANNEL-B

TOP: JDIMM2 CONN Non-ECC DIMM

Interleaved Memory

TOP STD (4 mm)

PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.258

Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2

Layout Note:
Place near JDIMM2

PLACE NEAR TO PIN

For ECC DIMM

DIMM Side

CPU Side

VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

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Issued Date	2017/07/24	Deciphered Date	2018/08/24

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Title: DDRIV_CHB: DIMM0

Document Number: LA-J643P

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Title: Reserve		
Size: Custom	Document Number: LA-J643P	Rev: 1.0
Date: Friday, March 13, 2020	Sheet 25 of 100	

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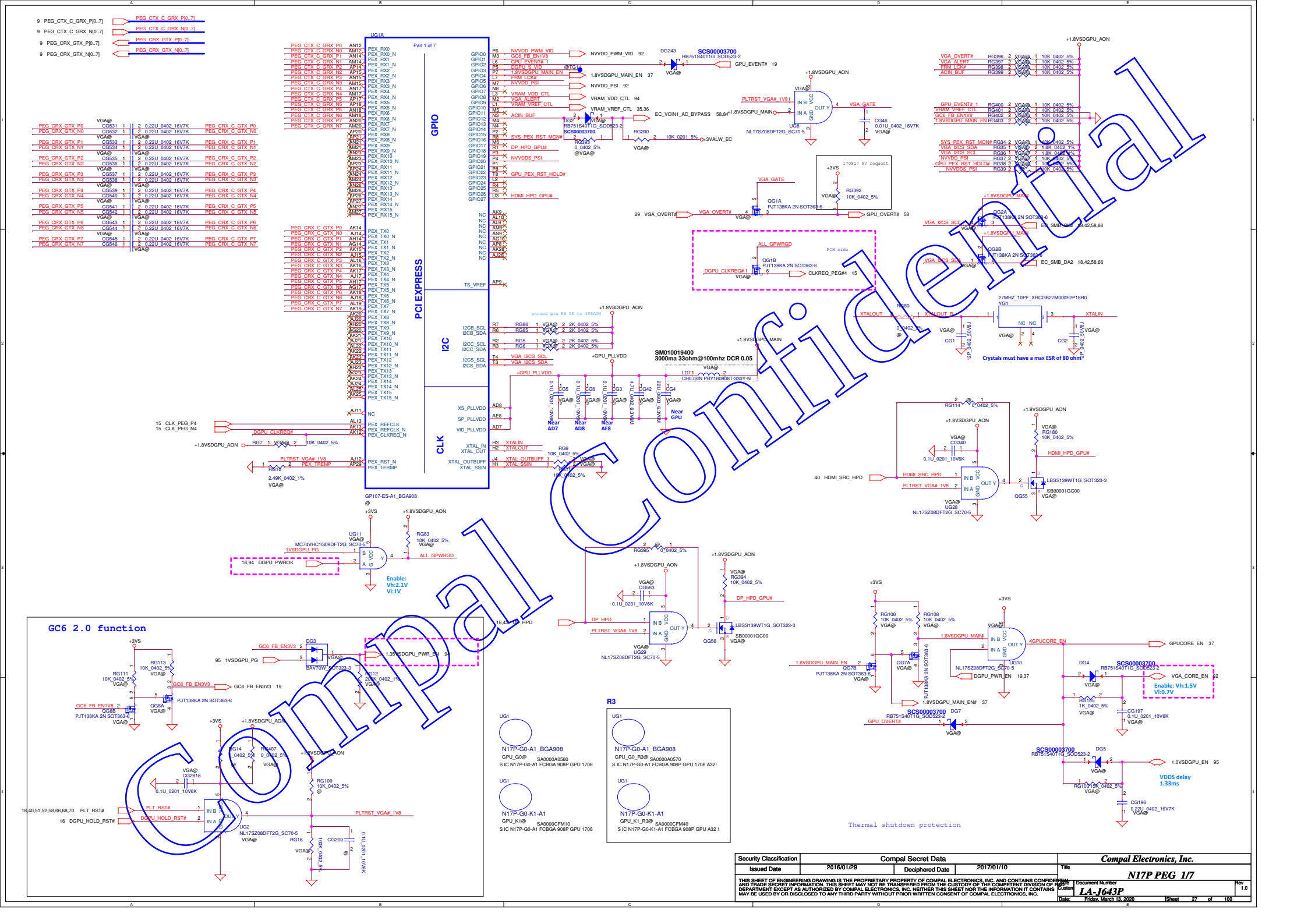
Title: Reserve		
Size: Custom	Document Number: LA-J643P	Rev: 1.0
Date: Friday, March 13, 2020	Sheet 26 of 100	



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Issued Date	2016/01/29	Deciphered Date 2017/01/10	Title N17P PEG 1/7
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			Date: Friday, March 13, 2020 / Sheet 27 of 100

GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

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Title: N17P VRAM 2/7			
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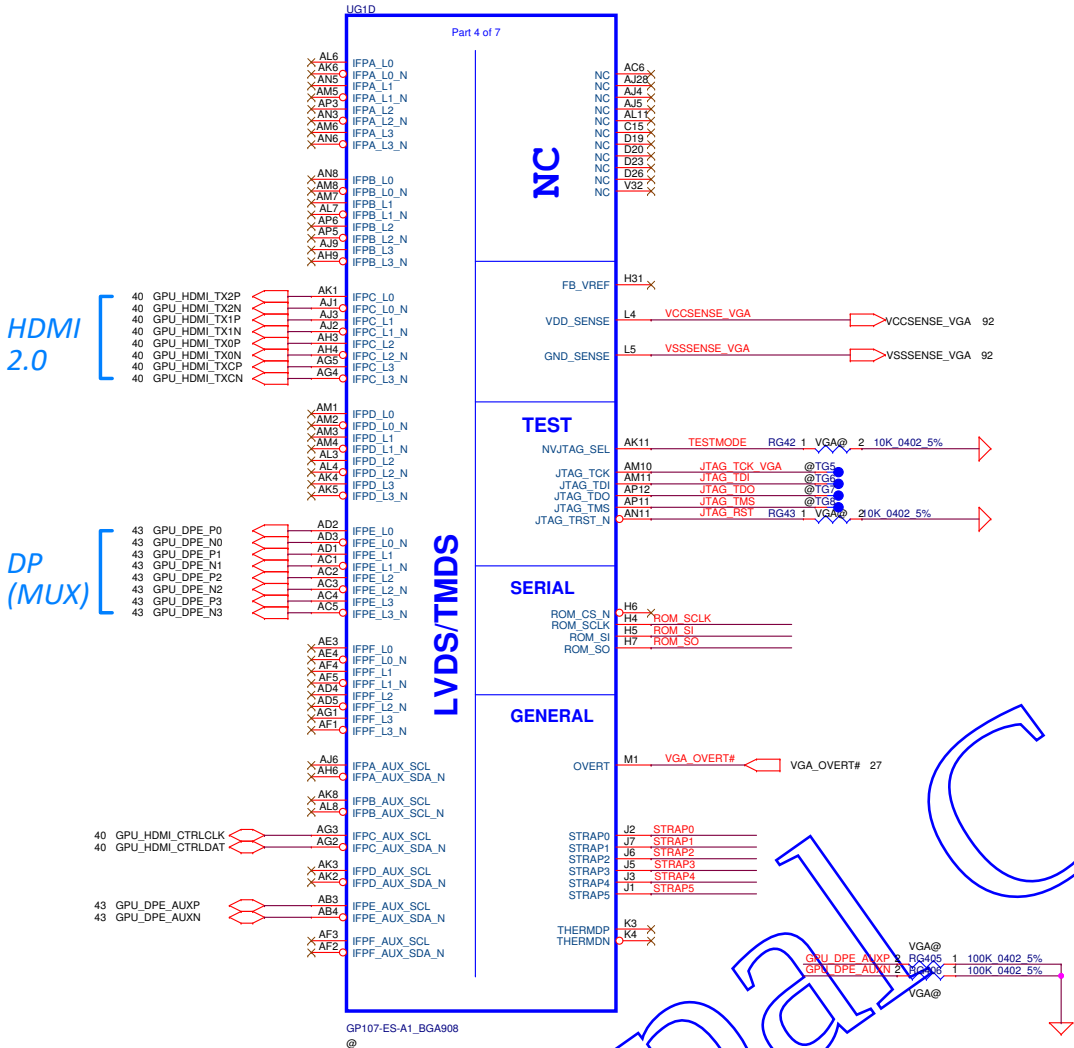

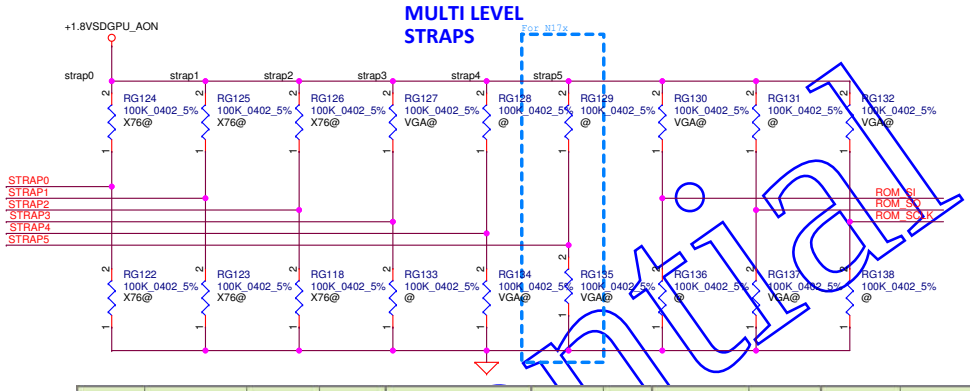

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V[2]	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
			Micron	MT51J256M32HF-70:B	B-die	0x4	7 Gbps	N/A	Full	Post production ready
			Micron	MT51J256M32HF-80:B	B-die	0x4	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
			Hynix	H5GC8H24AJR-R0C	A-die	0x5	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0x5	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
4 Gb	128Mx32	1.35V and 1.5V[2]	Samsung	K4G41325FE-HC28	E-die	0x7	7 Gbps	N/A	Full	Production ready
			Samsung	K4G41325FE-HC25	E-die	0x7	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5.4 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

	SMB_ATL_ADDR	
*	LOW	Single GPU
	High	Dual GPU
	DEVID_SEL	
*	LOW	Orig. Device ID
	High	Support G-Sync GPUID
	VGA_DEVICE	
	LOW	3D Device
*	High	VGA Device
	PCIE_CFG	
*	LOW	Normal signal swing
	High	Reduce the signal amplitude

HDMI /DP audio output

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Compal - HP Notebook 2016-09-1 23:22
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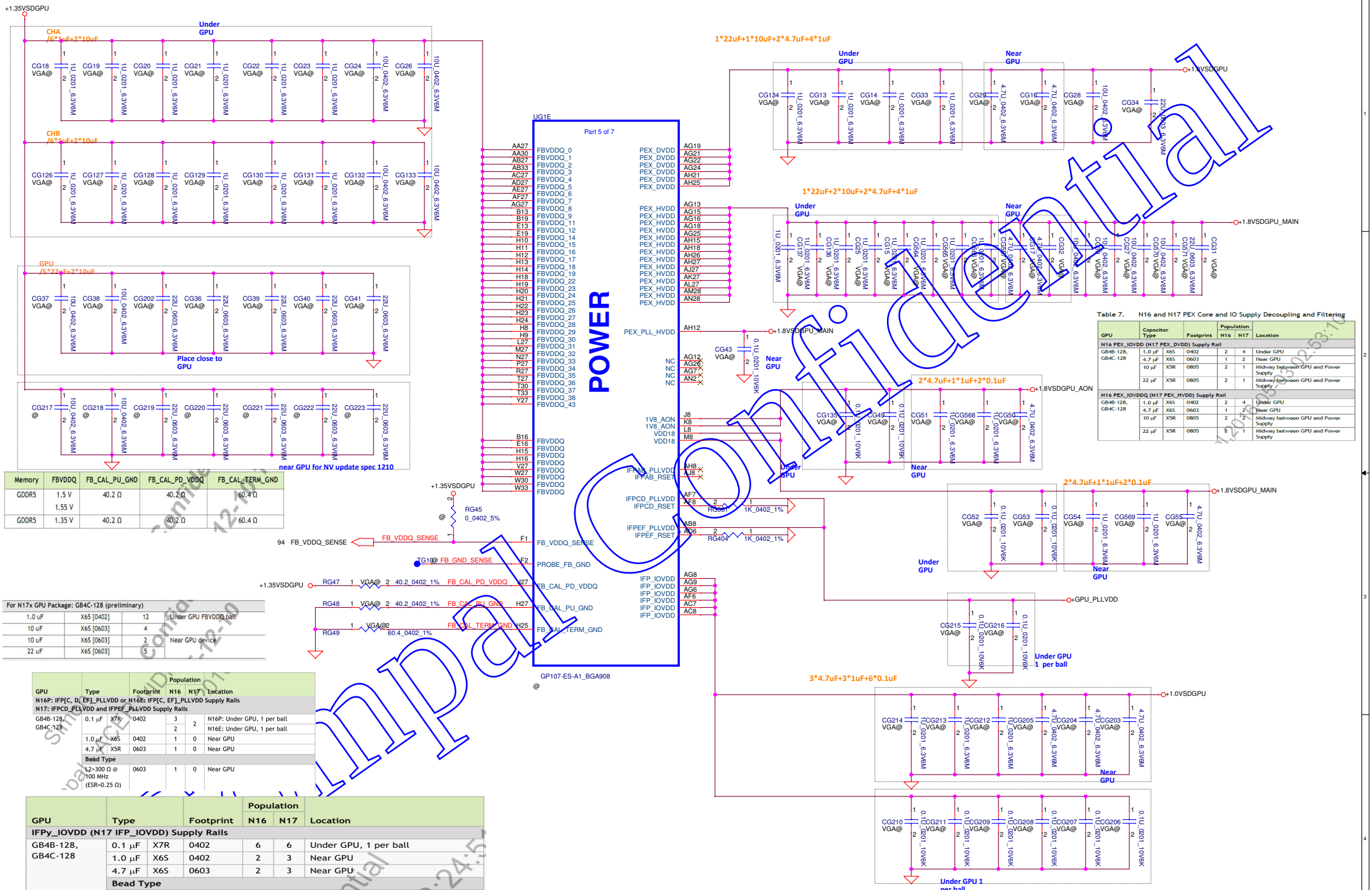

Memory	FBVDDQ	FB_CAL_PU_GND	FB_CAL_PD_VDDQ	FB_CAL_TERM_GND
GDDR5	1.5 V 1.55 V	40.2 Ω	40.2 Ω	60.4 Ω
GDDR5	1.35 V	40.2 Ω	40.2 Ω	60.4 Ω

Table 7. N16 and N17 PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail					
GB4B-128, GB4C-128	1.0 µF	X6S	0402	2	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X5R	0805	2	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	2	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail					
GB4B-128, GB4C-128	1.0 µF	X6S	0402	2	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X5R	0805	2	2	Midway between GPU and Power Supply
	22 µF	X5R	0805	2	1	Midway between GPU and Power Supply

For N17x GPU Package: GB4C-128 (preliminary)			
1.0 uF	X6S [0402]	12	Under GPU FBVDDQ ball
10 uF	X6S [0603]	4	
10 uF	X6S [0603]	2	Near GPU device
22 uF	X6S [0603]	5	

GPU	Type	Footprint	Population N16	Population N17	Location
N16P: IFP[C, D, EF]_PLLVDD or N16E: IFP[C, EF]_PLLVDD Supply Rails N17: IFPCD_PLLVDD and IFPEF_PLLVDD Supply Rails					
GB4B-128, GB4C-128	0.1 µF X7R	0402	3	2	N16P: Under GPU, 1 per ball
			2		N16E: Under GPU, 1 per ball
	1.0 µF X6S	0402	1	0	Near GPU
	4.7 µF X5R	0603	1	0	Near GPU
	Bead Type				
	L2=300 Ω @ 100 MHz (ESR=0.25 Ω)	0603	1	0	Near GPU

GPU	Type	Footprint	Population N16	Population N17	Location
IFPy_IOVDD (N17 IFP_IOVDD) Supply Rails					
GB4B-128, GB4C-128	0.1 µF X7R	0402	6	6	Under GPU, 1 per ball
	1.0 µF X6S	0402	2	3	Near GPU
	4.7 µF X6S	0603	2	3	Near GPU
	Bead Type				
	L1=180 Ω @ 100 MHz (ESR=0.2 Ω)	0603	2	0	Near GPU

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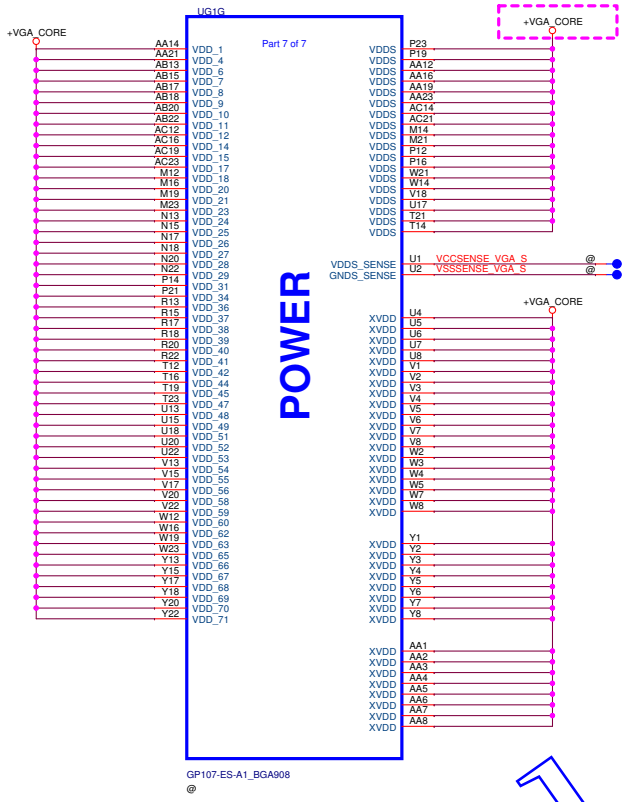
N17P VDDS
1uF*5/4.7uF*5 (under GPU)
330uF*1/22uF*3/10uF*2/4.7uF*2



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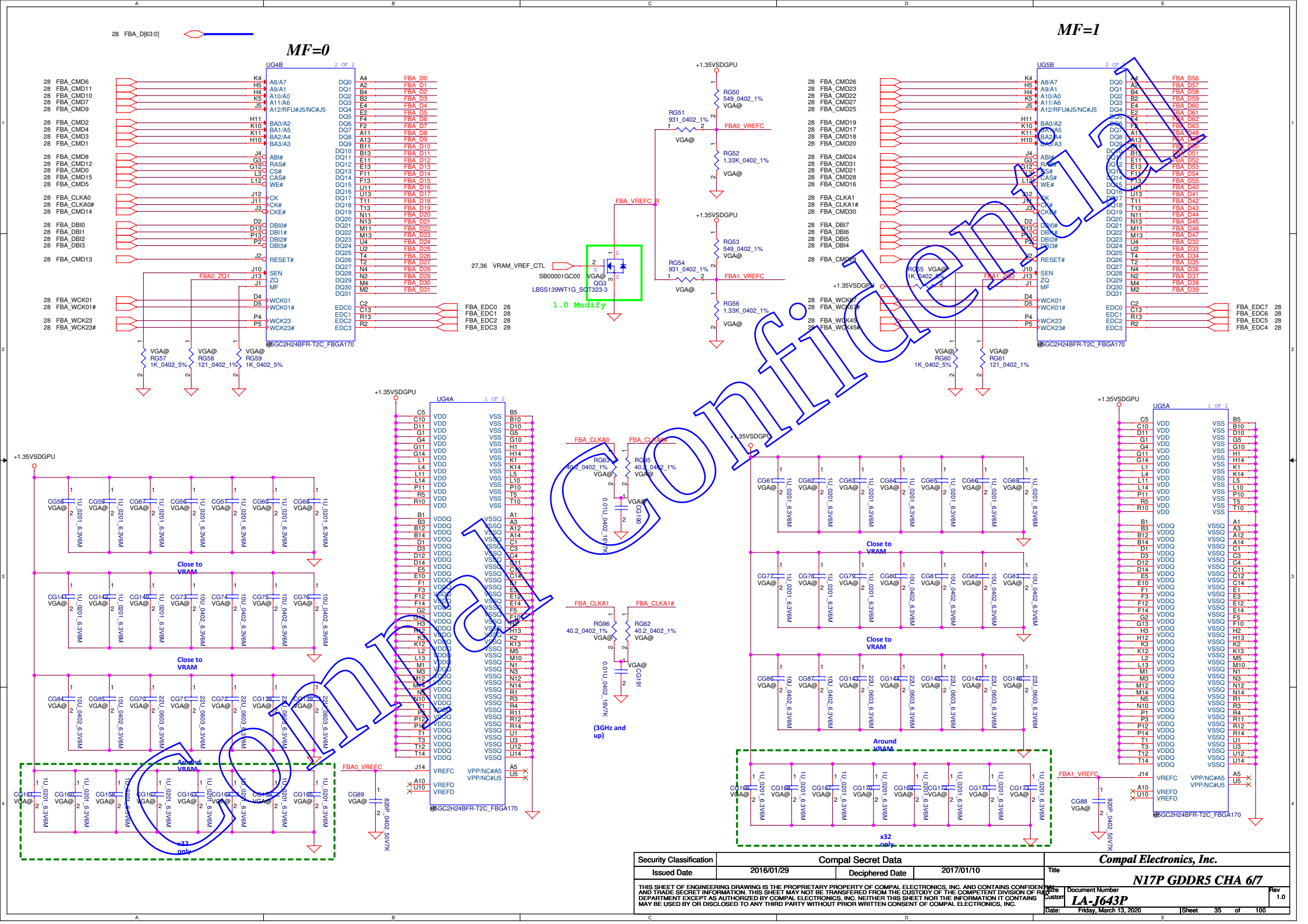

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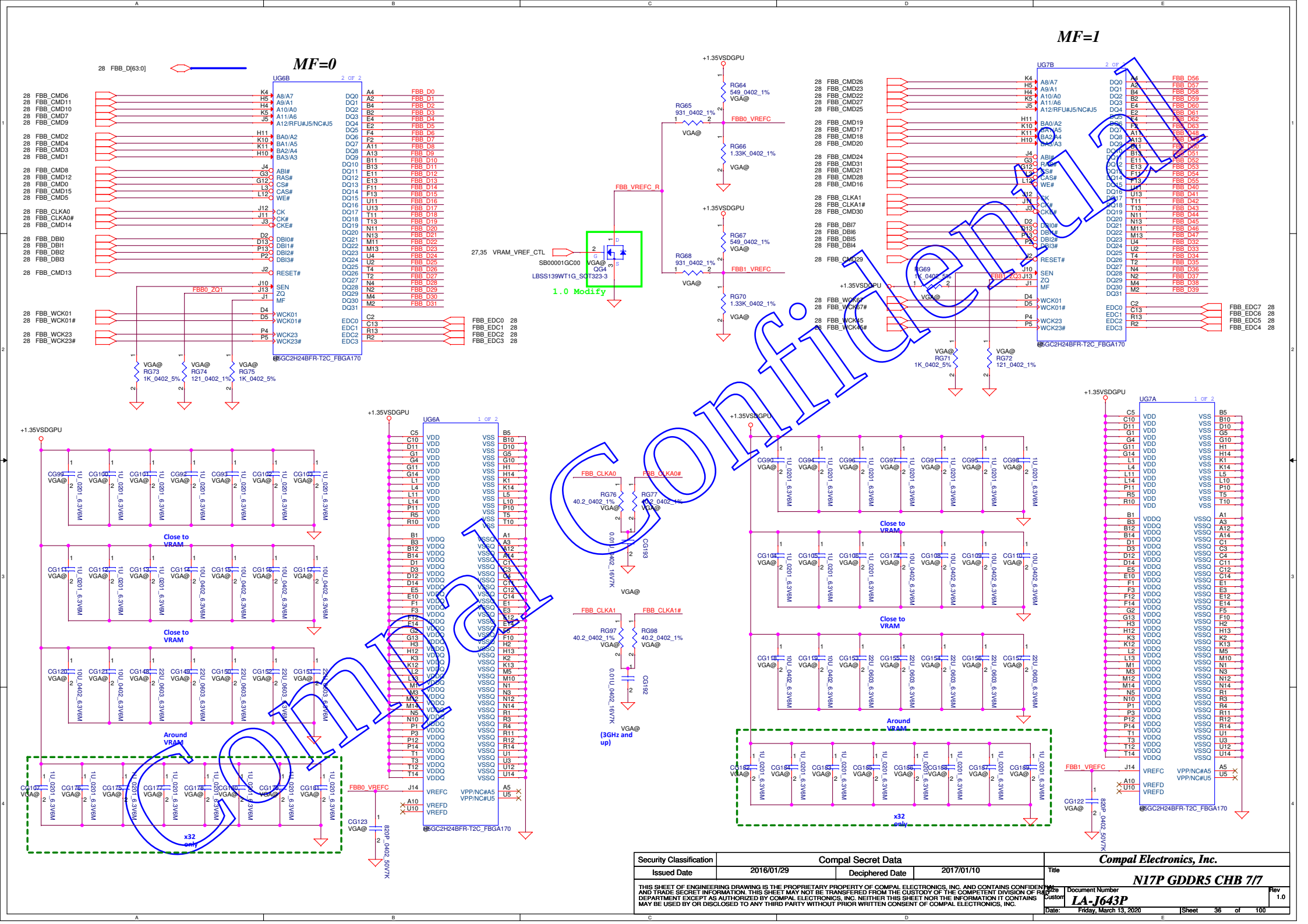

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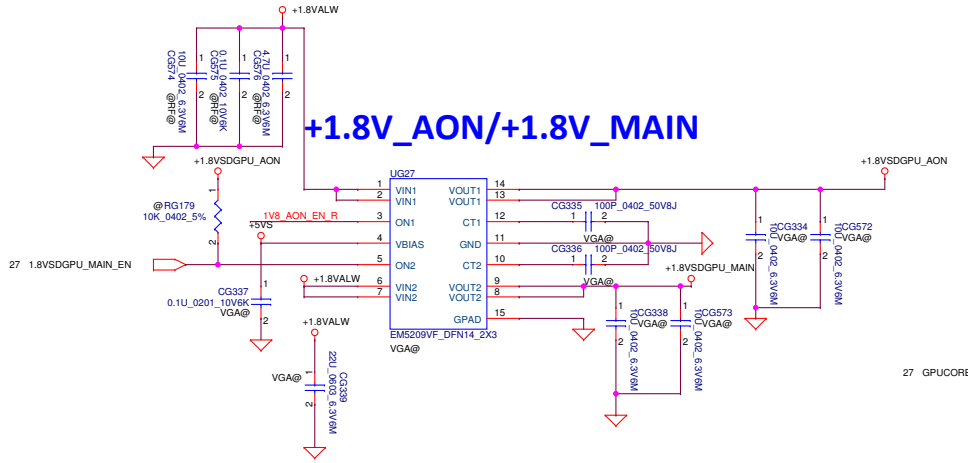

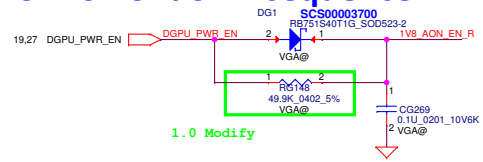

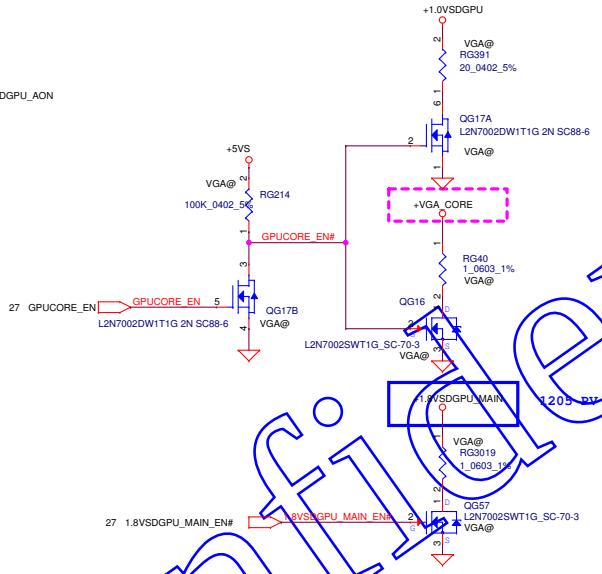

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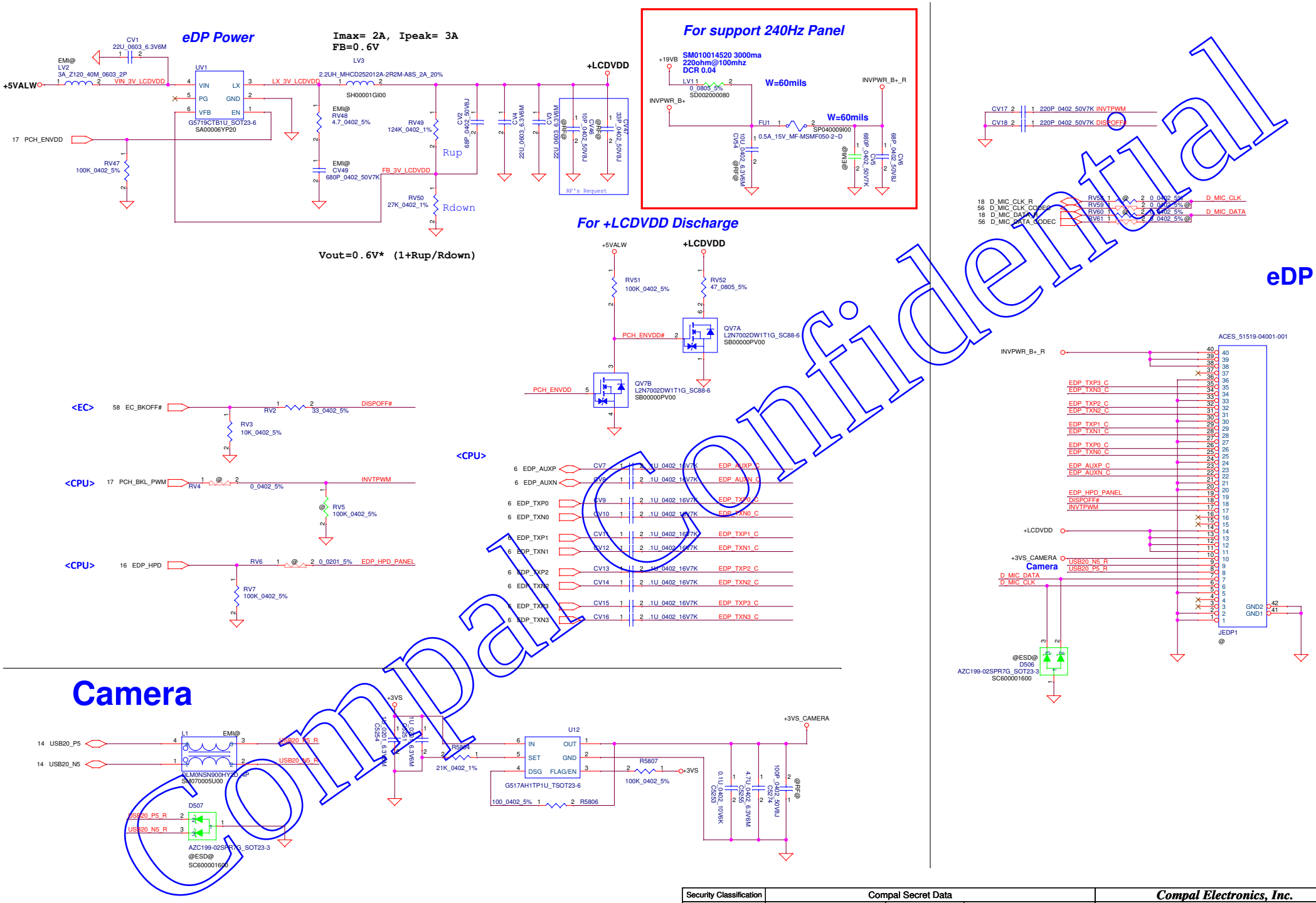

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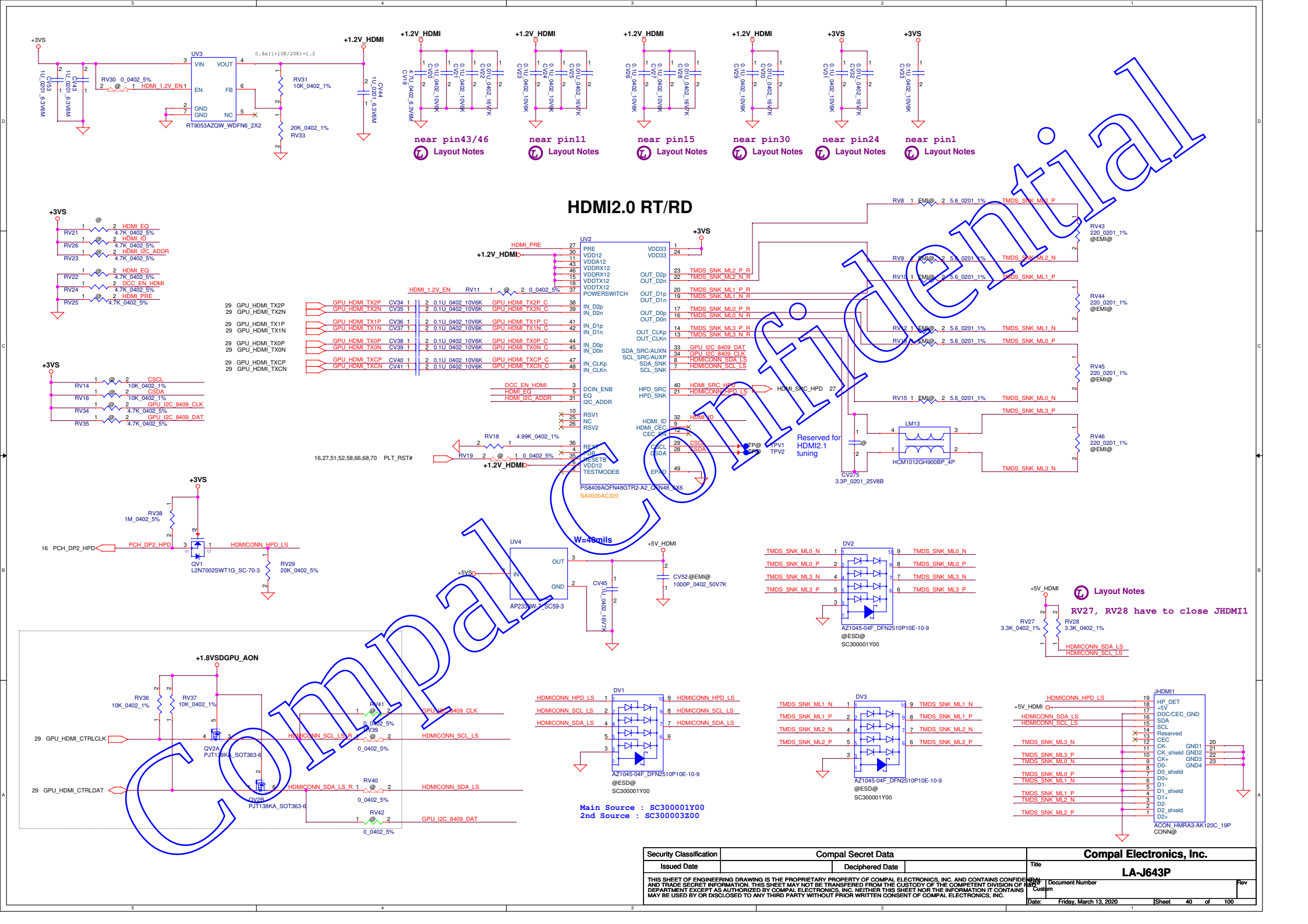

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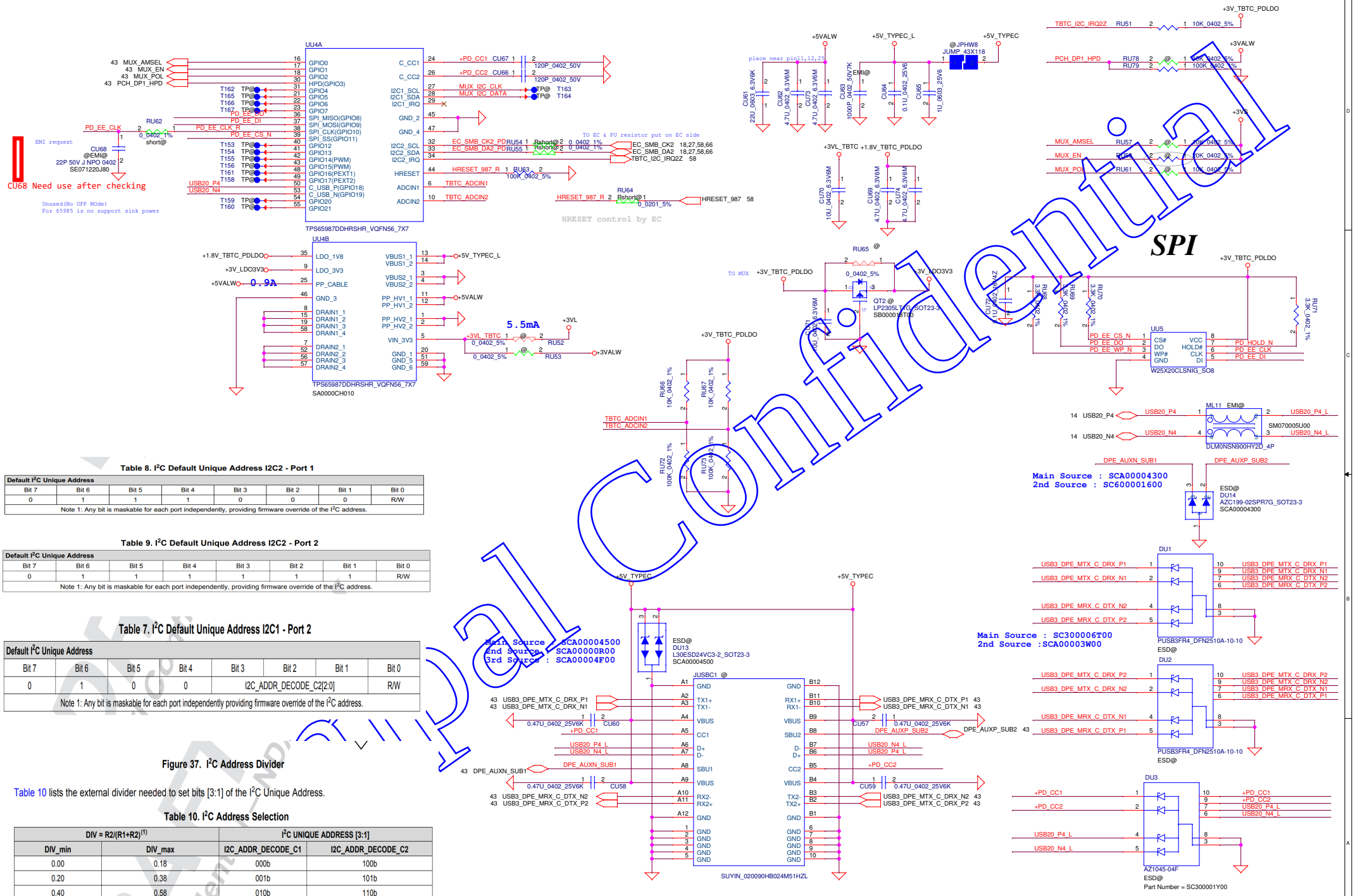

Table 8. I²C Default Unique Address I2C2 - Port 1

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	0	0	0	R/W
Note 1: Any bit is maskable for each port independently, providing firmware override of the I²C address.							

Table 9. I²C Default Unique Address I2C2 - Port 2

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	1	1	1	R/W
Note 1: Any bit is maskable for each port independently, providing firmware override of the I²C address.							

Table 7. I²C Default Unique Address I2C1 - Port 2

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	I2C_ADDR_DECODE_C2[2:0]			R/W
Note 1: Any bit is maskable for each port independently providing firmware override of the I²C address.							

Figure 37. I²C Address Divider

Table 10 lists the external divider needed to set bits [3:1] of the I²C Unique Address.

Table 10. I²C Address Selection

DIV = R2/(R1+R2)(1)		I²C UNIQUE ADDRESS [3:1]	
DIV_min	DIV_max	I2C_ADDR_DECODE_C1	I2C_ADDR_DECODE_C2
0.00	0.18	000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
0.60	1.00	011b	111b

(1) External resistor tolerance of 1% is required. Resistor values should be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

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GPIO/I2C mode

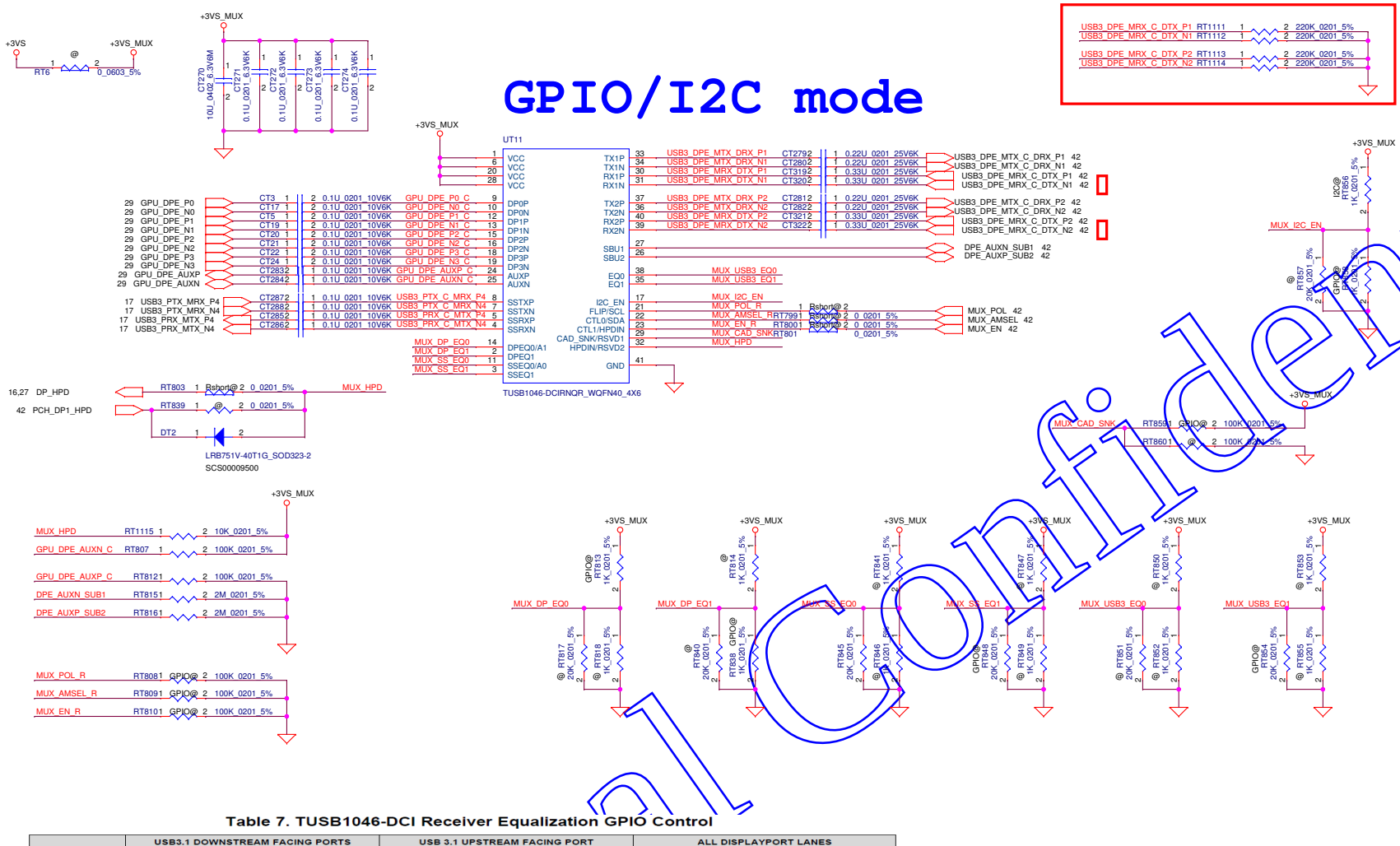

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Table 7. TUSB1046-DCI Receiver Equalization GPIO Control

Equalization Setting #	USB3.1 DOWNSTREAM FACING PORTS			USB 3.1 UPSTREAM FACING PORT			ALL DISPLAYPORT LANES		
	EQ1 PIN LEVEL	EQ0 PIN LEVEL	EQ GAIN at 5 GHz (dB)	SSEQ1 PIN LEVEL	SSEQ0 PIN LEVEL	EQ GAIN at 5 GHz (dB)	DPEQ1 PIN LEVEL	DPEQ0 PIN LEVEL	EQ GAIN at 4.05 GHz (dB)
0	0	0	-3.9	0	0	-1.8	0	0	1.0
1	0	R	-1.7	0	R	0.2	0	R	3.3
2	0	F	-0.1	0	F	1.7	0	F	4.9
3	0	1	1.4	0	1	3.2	0	1	6.5
4	R	0	2.4	R	0	4.2	R	0	7.5
5	R	R	3.5	R	R	5.3	R	R	8.6
6	R	F	4.4	R	F	6.1	R	F	9.5
7	R	1	5.2	R	1	7.0	R	1	10.4
8	F	0	5.9	F	0	7.7	F	0	11.1
9	F	R	6.6	F	R	8.3	F	R	11.7
10	F	F	7.1	F	F	8.8	F	F	12.3
11	F	1	7.6	F	1	9.3	F	1	12.8
12	1	0	8.0	1	0	9.7	1	0	13.2
13	1	R	8.5	1	R	10.1	1	R	13.6
14	1	F	8.8	1	F	10.4	1	F	14.0
15	1	1	9.2	1	1	10.8	1	1	14.4

Table 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 KΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 KΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 KΩ 5%to V_{CC}. Option 2: Tie directly to V_{CC}.

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+LAN_VDD_3V3 Rising time (10~90%)
need>0.5mS and <100mS

CL9, CL20 close to UL1 Pin 11
CL5 & CL19 close to UL1: Pin 32
Note: CL19/CL20 are reserved for surge test

CL10& CL16 close to UL1: Pin 23

CL8, CL23 close LL2.
CL26 close UL1 Pin 3.
CL12 close UL1 Pin 8.
CL13 ~ CL15 close UL1 Pin 22.
CL11, CL27 close UL1 Pin 30.

+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil

(SA000084T00) RTL8111HSH-CG Giga

SP050005L00 Footprint

11/22 使 用SP050006B 10

Main Source : SCA00004300
2nd Source : SC600001600

powe rail need to check

Main Source : SC300001G00
2nd Source : SC300003V00

Side Light
Vf=1.9~2.4V

Side Light
Vf=2.9~3.15V

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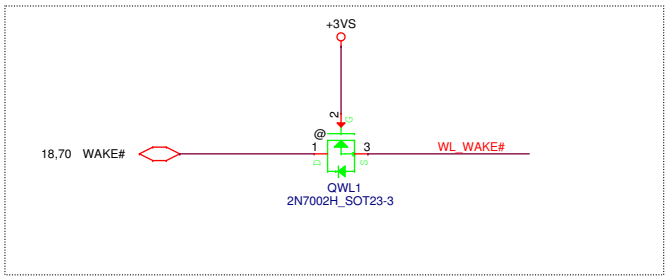
WLAN KEY-E



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+3VS
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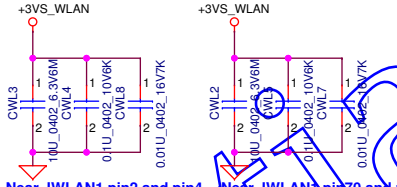
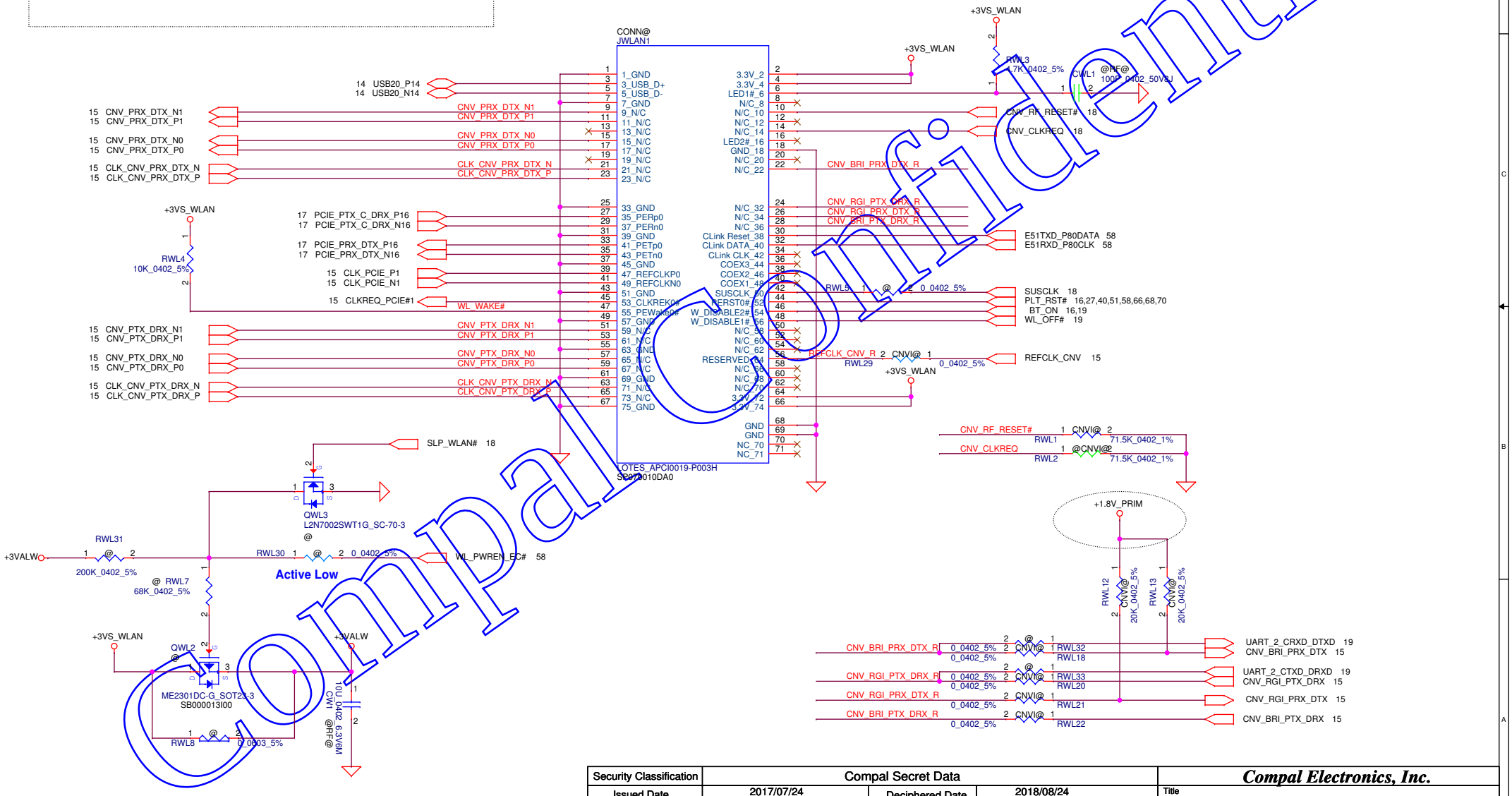
+3VALW





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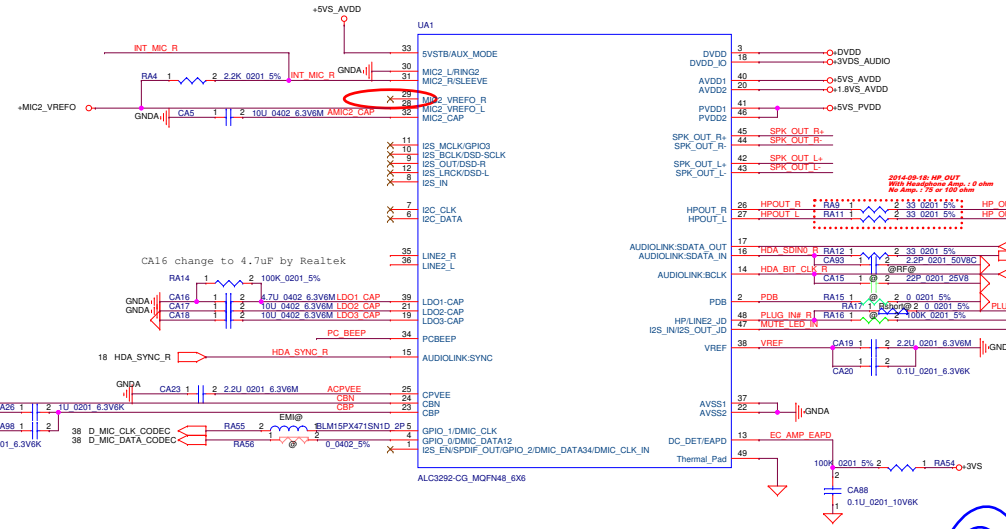

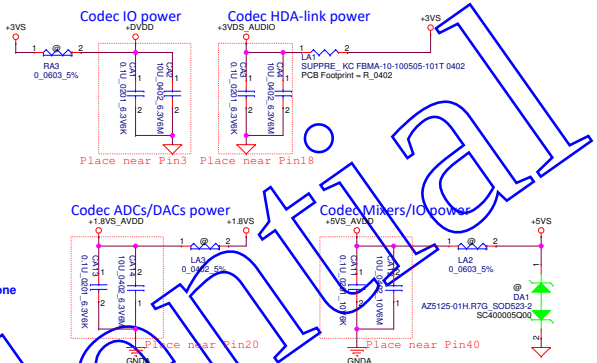

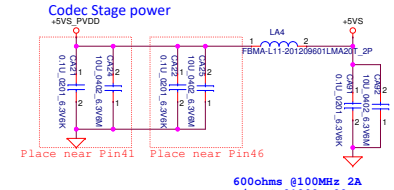

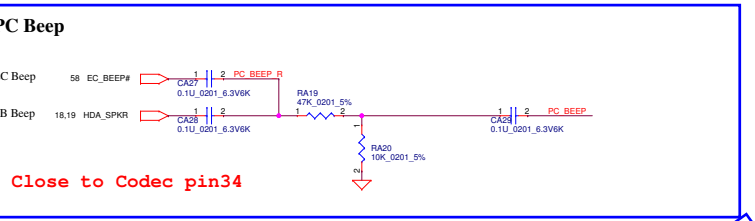

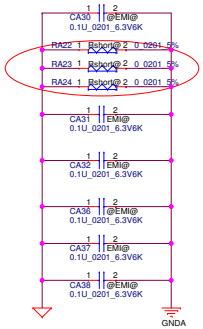

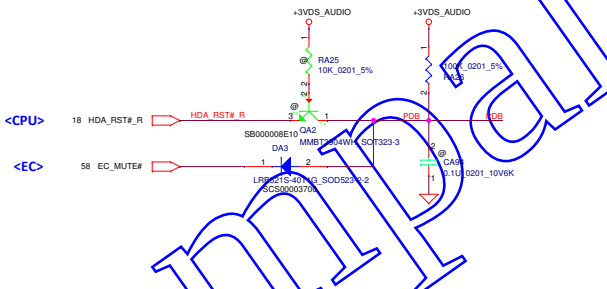

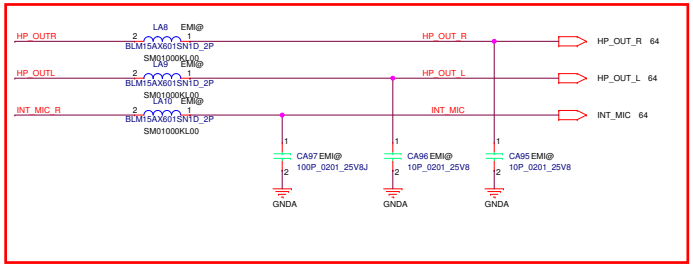

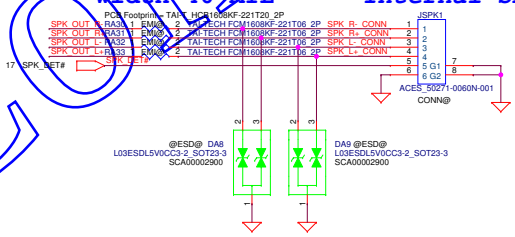

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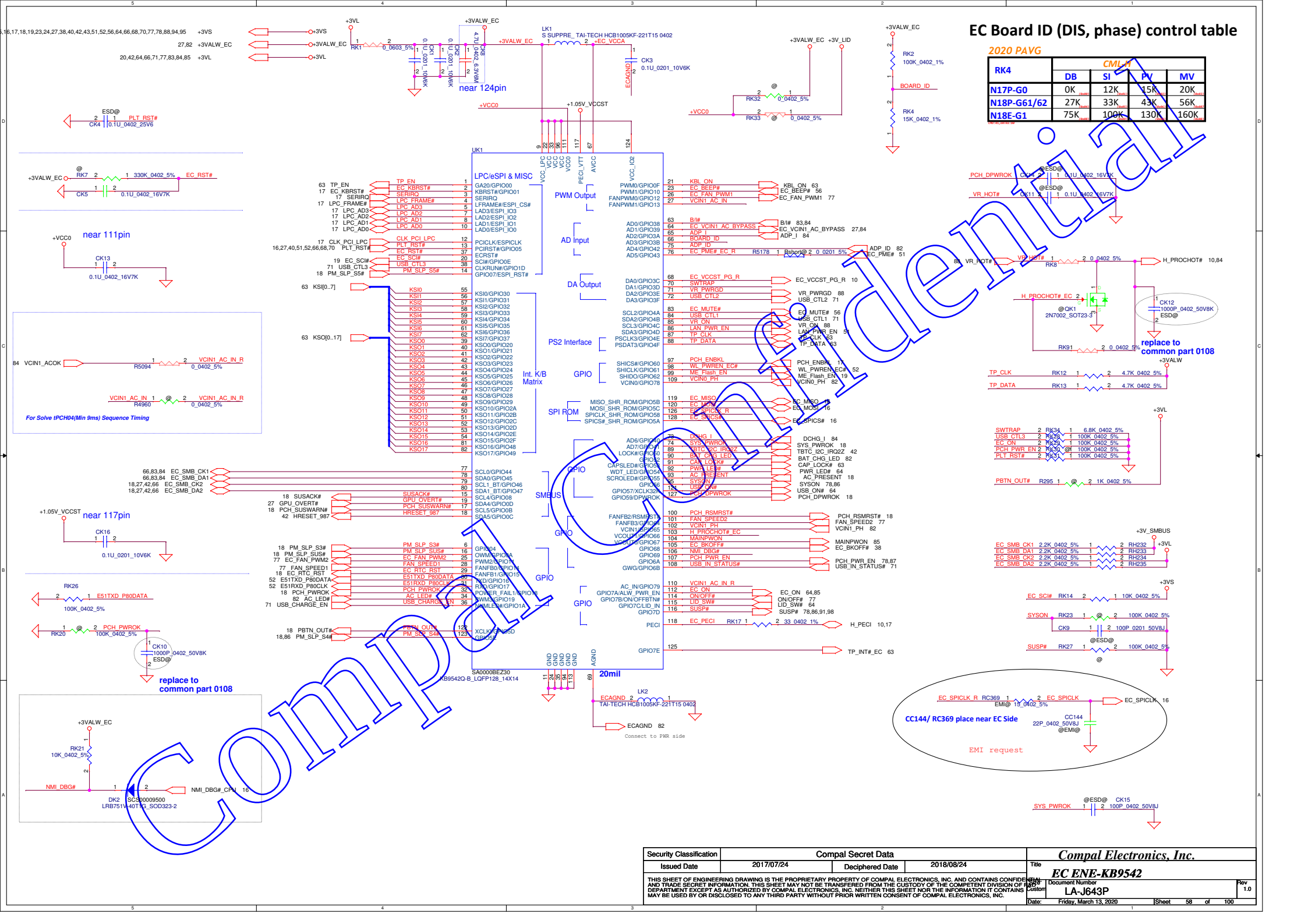
EC Board ID (DIS, phase) control table
2020 PAVG
RK4
CMLA
DB
SI
PV
MV
N17P-G0
0K
12K
15K
20K
N18P-G61/62
27K
33K
43K
56K
N18E-G1
75K
100K
130K
160K
UK1
LPC/eSPI & MISC
PWM Output
AD Input
DA Output
PS2 Interface
GPIO
Int. K/B Matrix
SPI ROM
SMBUS
near 124pin
near 111pin
near 117pin
20mil
SA0000BEZ30
KB9542Q-B_LQFP128_14X14
replace to common part 0108
CC144/ RC369 place near EC Side
EMI request
Connect to PWR side
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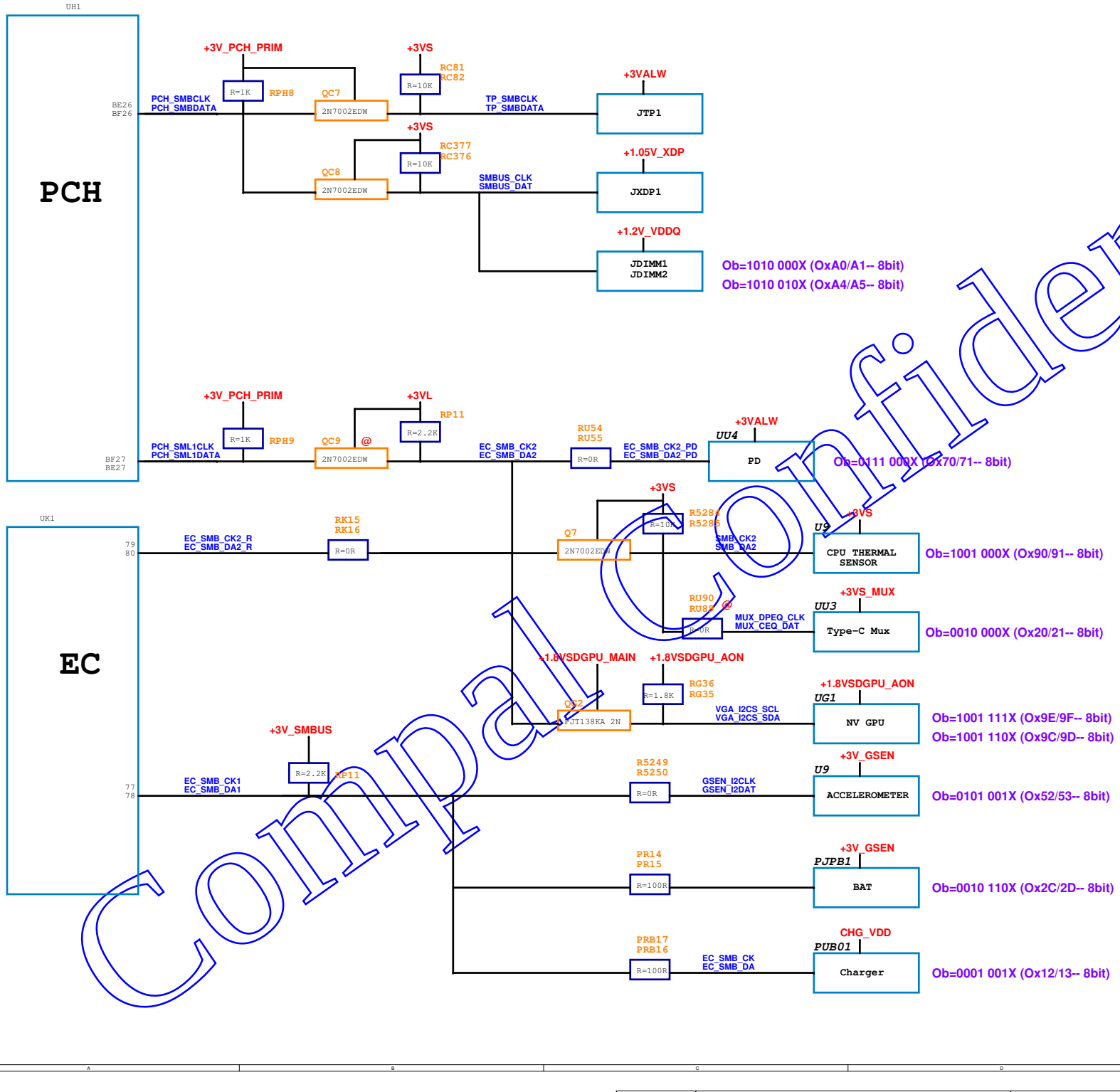

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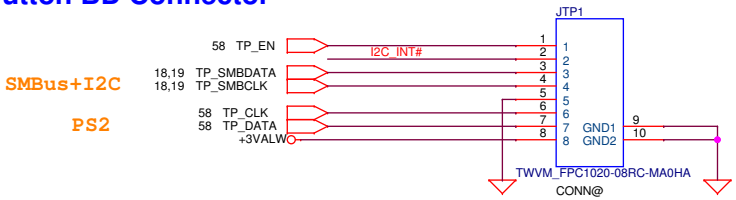
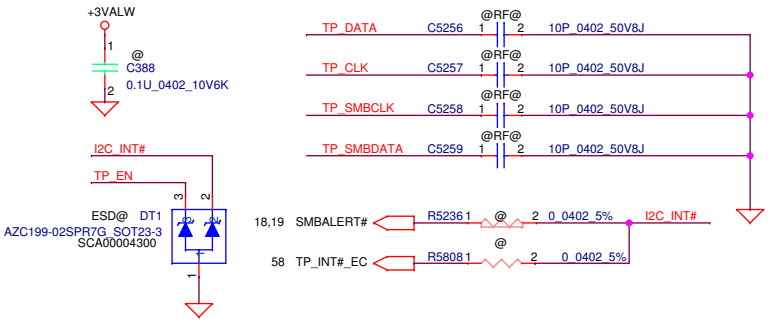
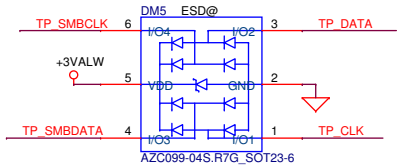
TP Button BD Connector



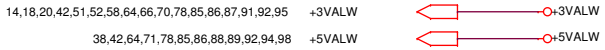


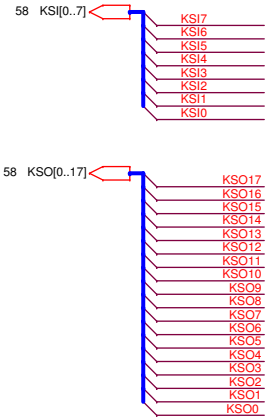


Main Source : SC300001G00
2nd Source : SC300003I00
3rd Source : SC300003S00

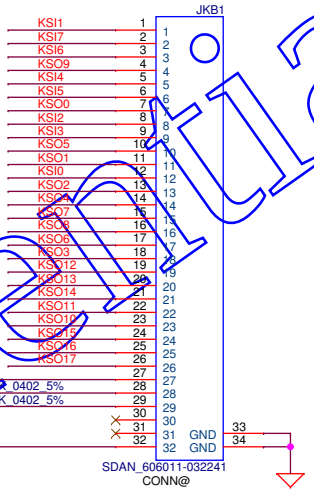
Pin Assignment and Description			
Pin#	Signal	I/O	Description
1	VDD_3.3V	Power	3.3V +/-5%. Power ripple: 100 mVpp max. Power sequence: See section 4.6.
2	PS2_DATA	I/O	PS2 data
3	PS2_CLK	I/O	PS2 clock
4	GND	GND	Ground
5	SMB_CLK	I/O	SMBUS clock I_{Drive} or I_{Sink}: 8 mA max.
6	SMB_DATA	I/O	SMBUS data. I_{Drive} or I_{Sink}: 8 mA max.
7	/INT (/ATTN)	O	For SMBus application, low active, indicates touchpad likes to send data to system (host) if go low.
8	LID_CLOSE (TP Disable/Enable)	I	Enable or disable touchpad, low active Low: Disable TP High: Enable TP

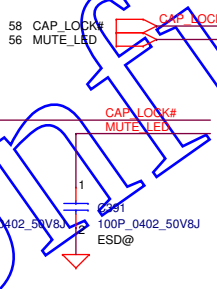
Keyboard conn

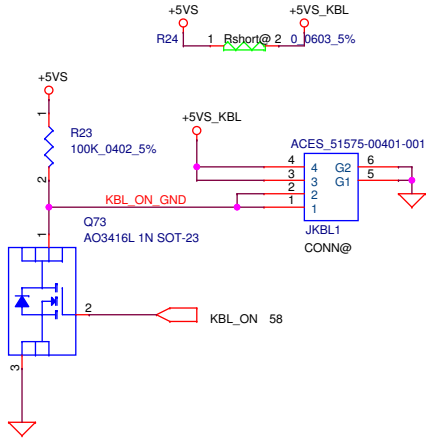




	JKB1	KB Spec
Pin1	5V	KSI1
Pin32	KSI1	5V







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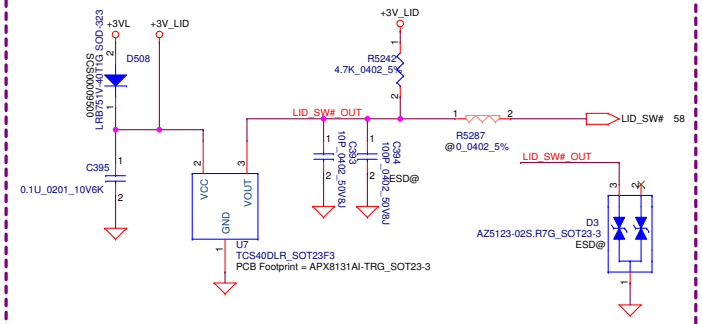
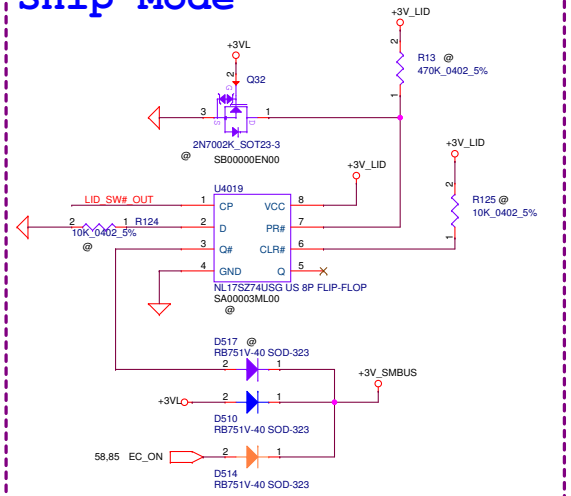
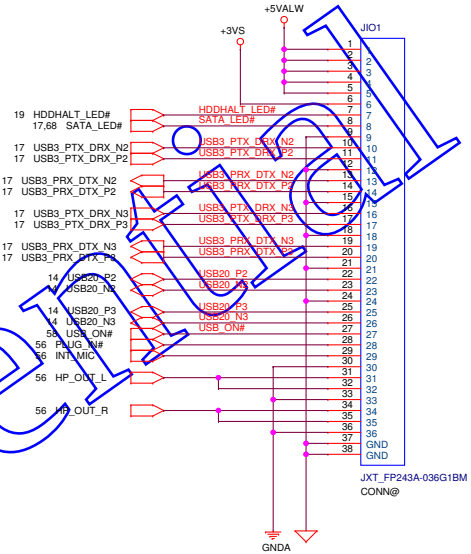
Lid Switch (Hall Effect Sensor)

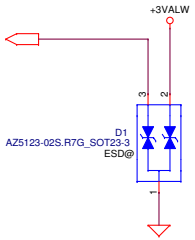


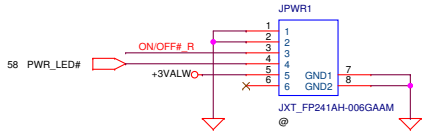
Ship Mode



To IO Board







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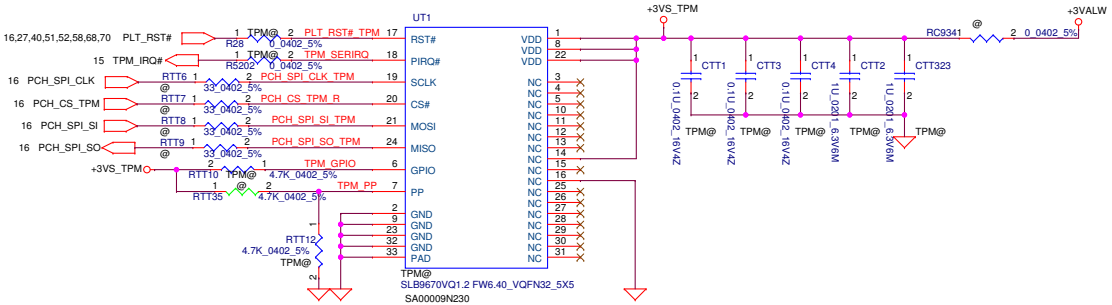
TPM2.0



ACCELEROMETER
ST Micro HP2DC

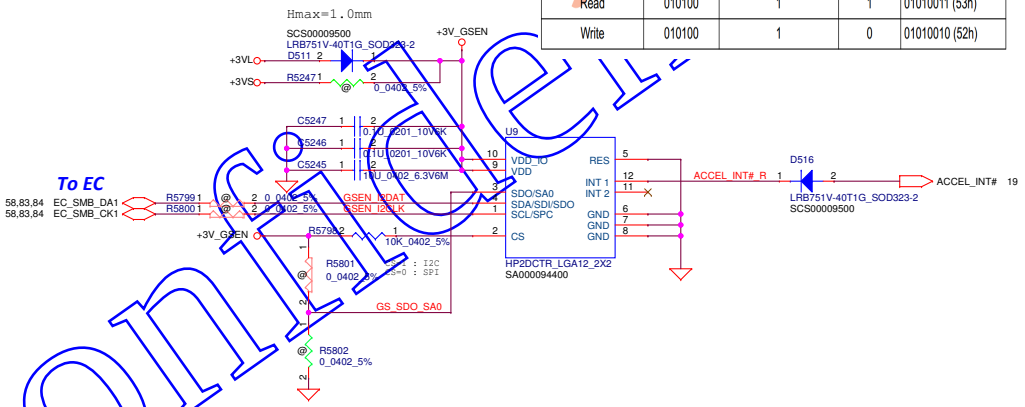
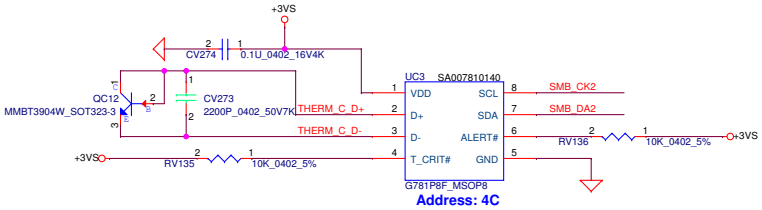
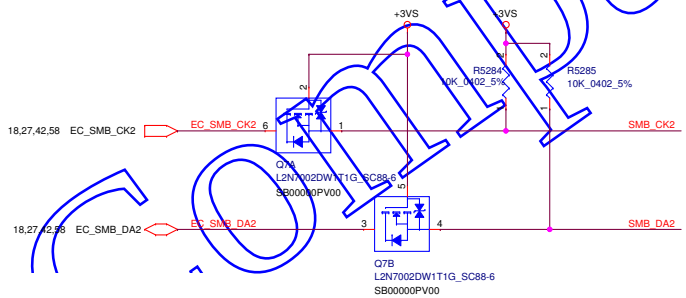


Table 12. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

CPU THERMAL SENSOR





Slave Address

The G753 appears to the SMBus as one device having a common address for both ADC channels.
The G753 has the following SMBus slave address:

	A6	A5	A4	A3	A2	A1	A0
G753	1	0	0	1	0	0	0

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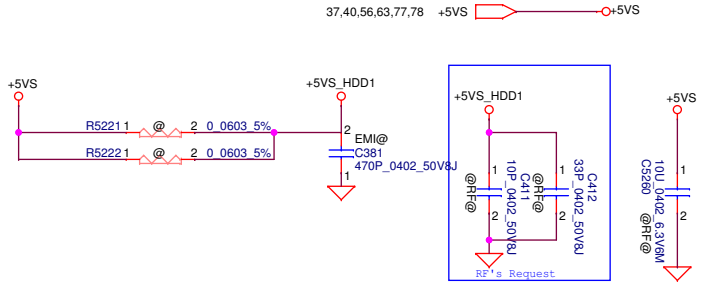
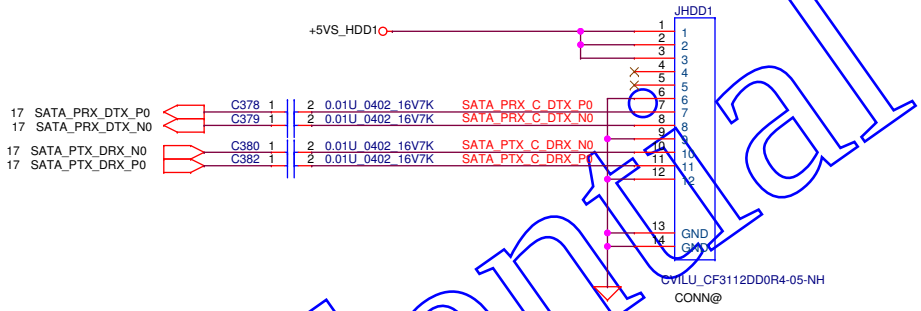
2.5" SATA HDD





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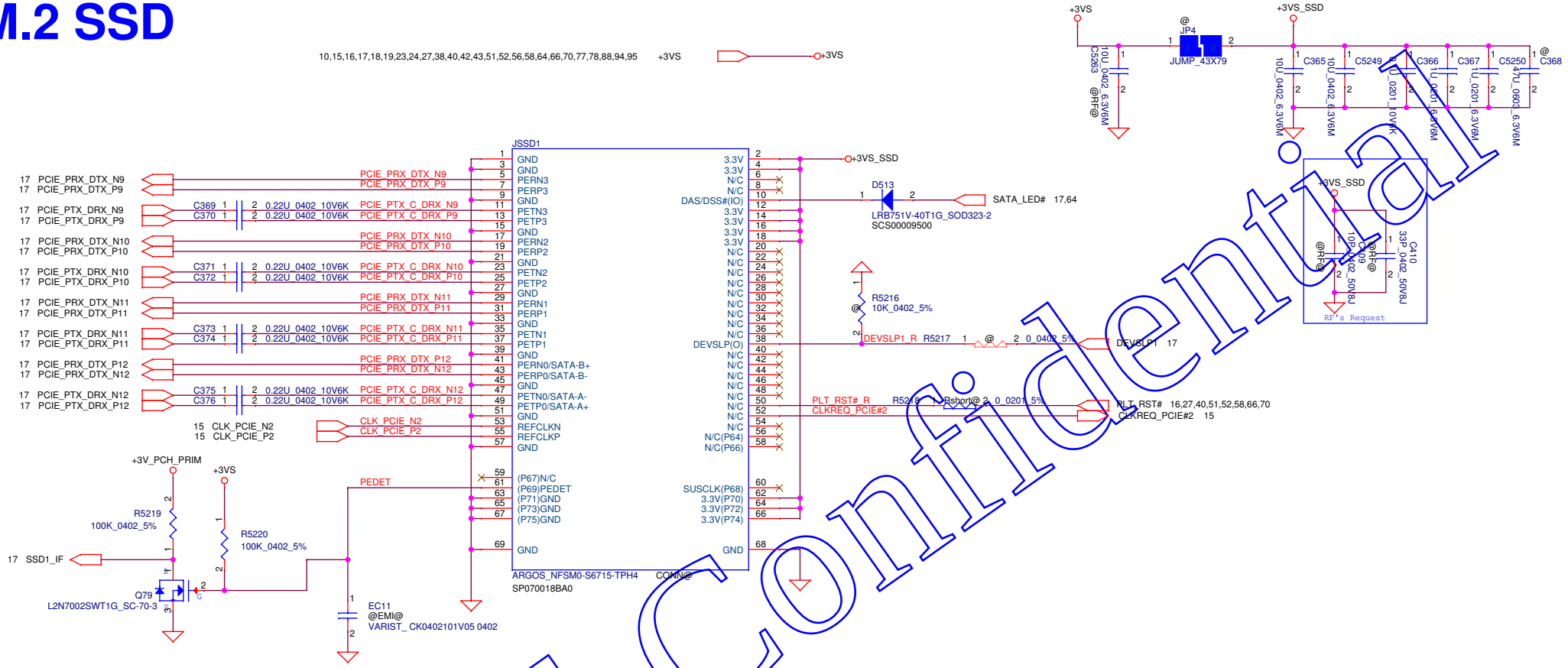
M.2 SSD



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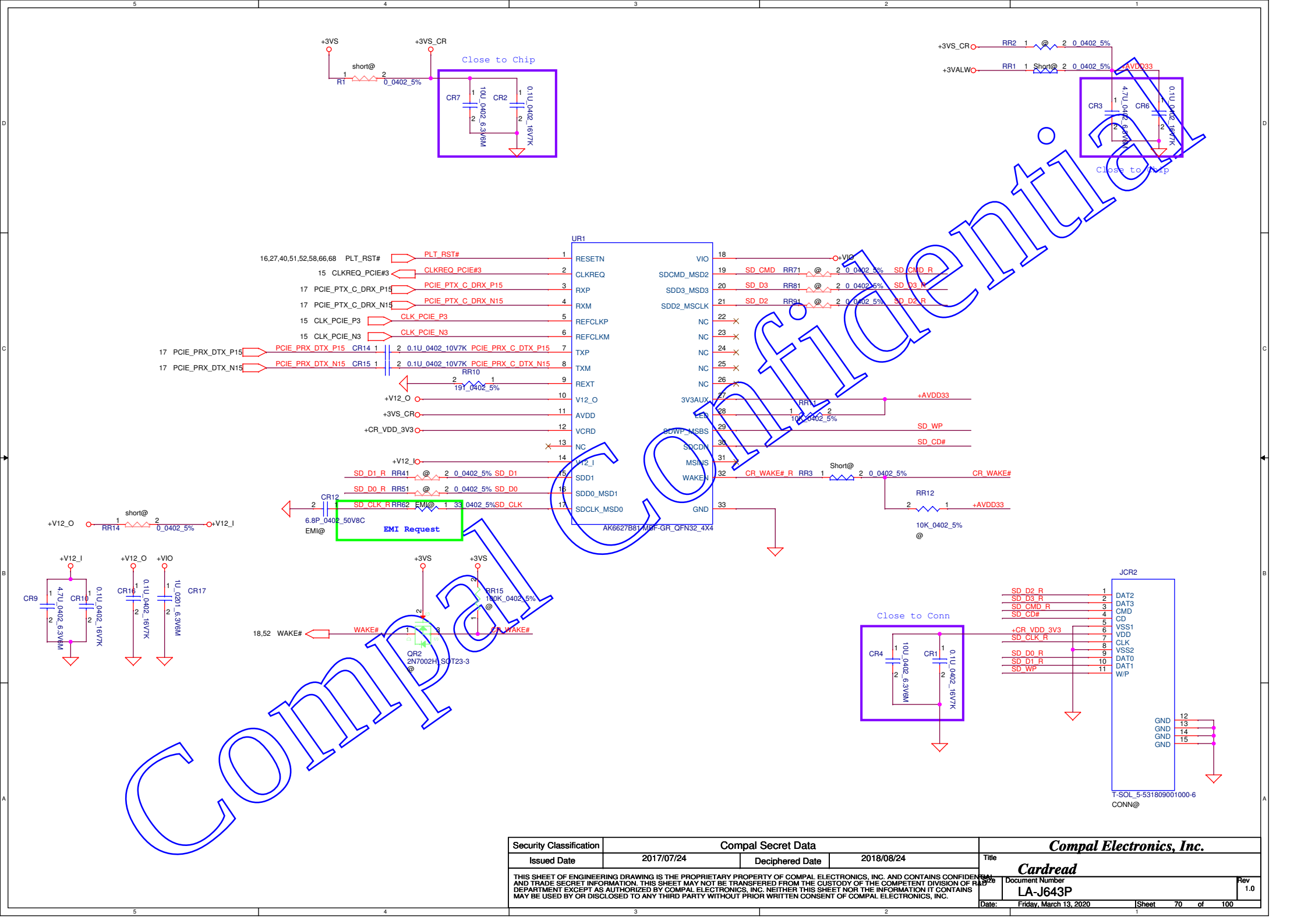

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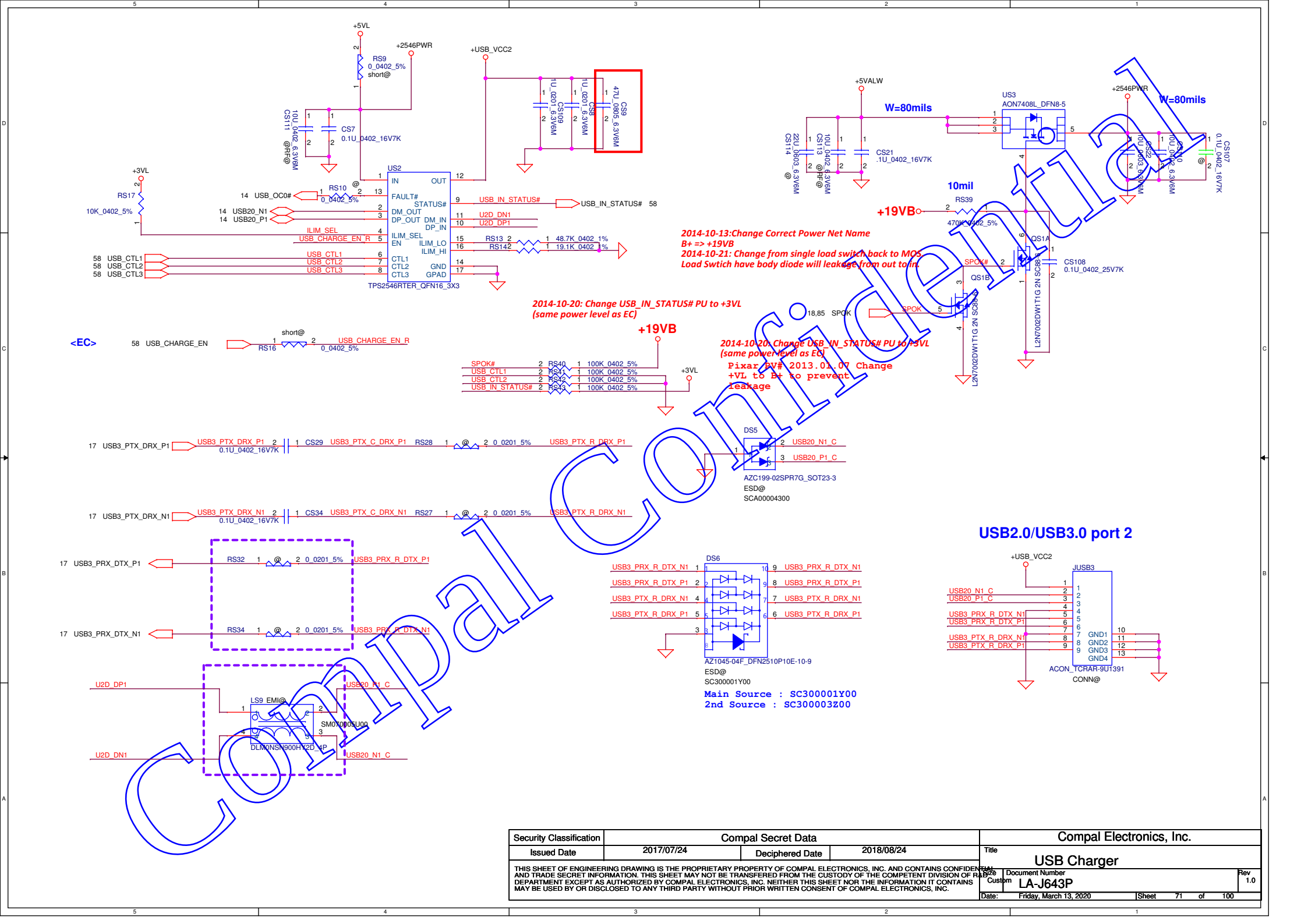

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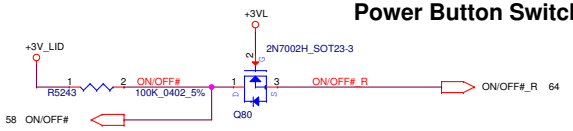
Power Button Switch



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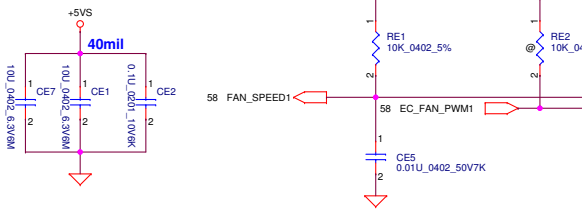

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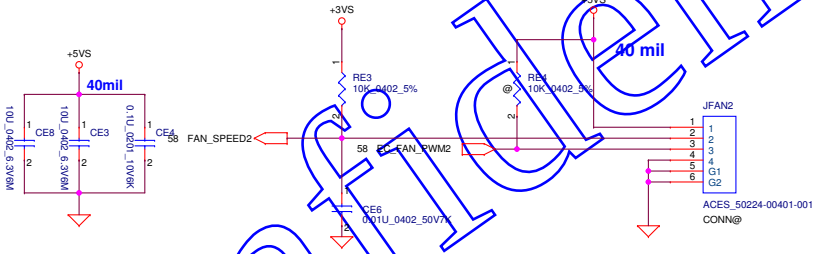
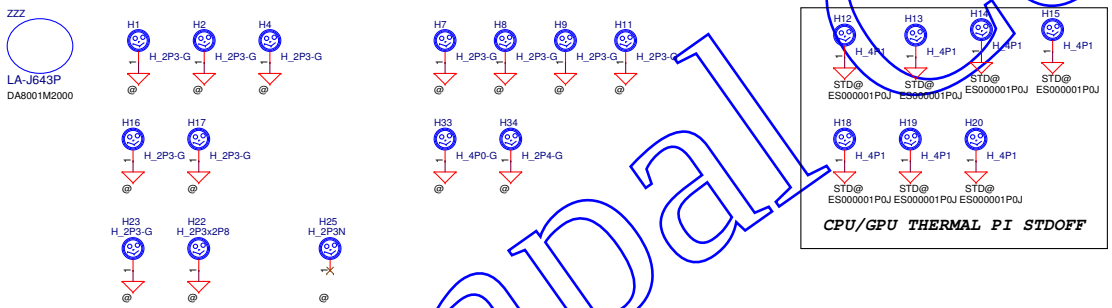


PCB Screw Hole



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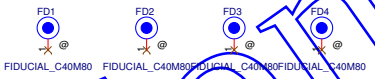

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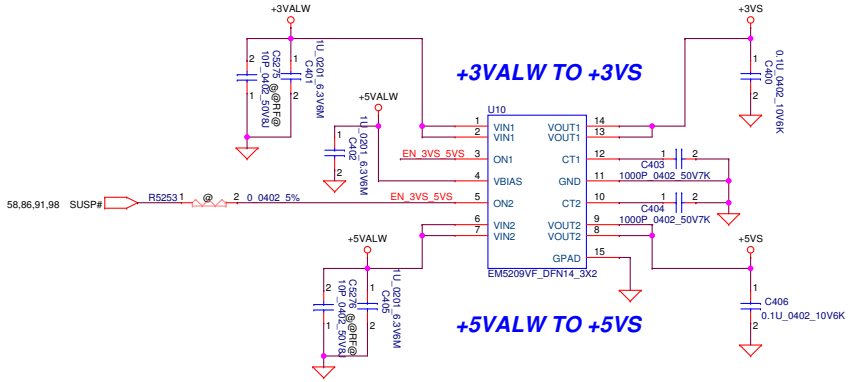

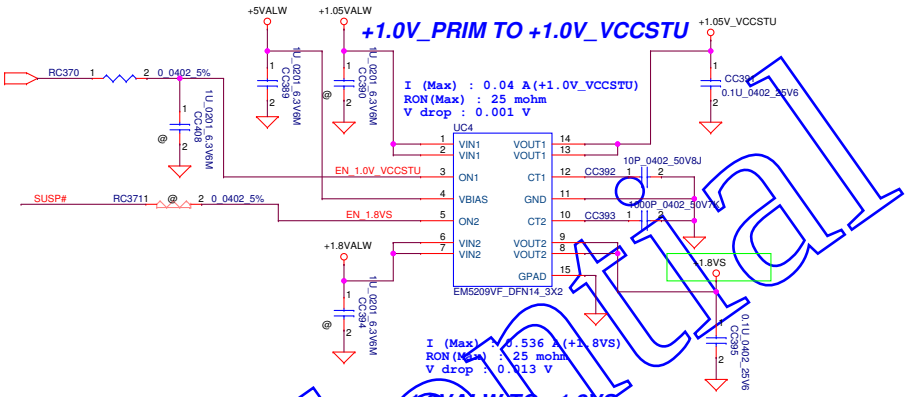

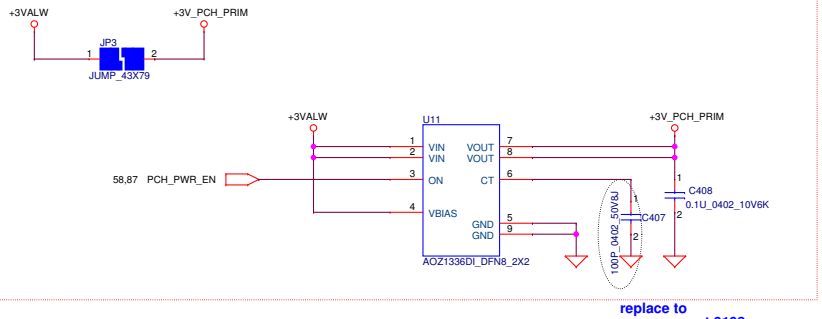

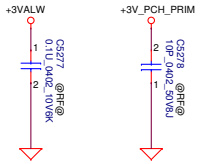

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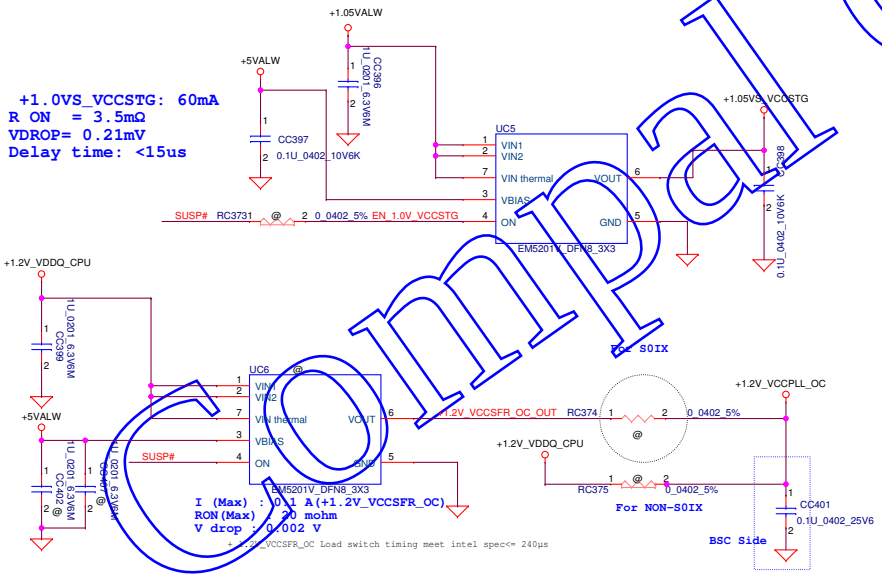

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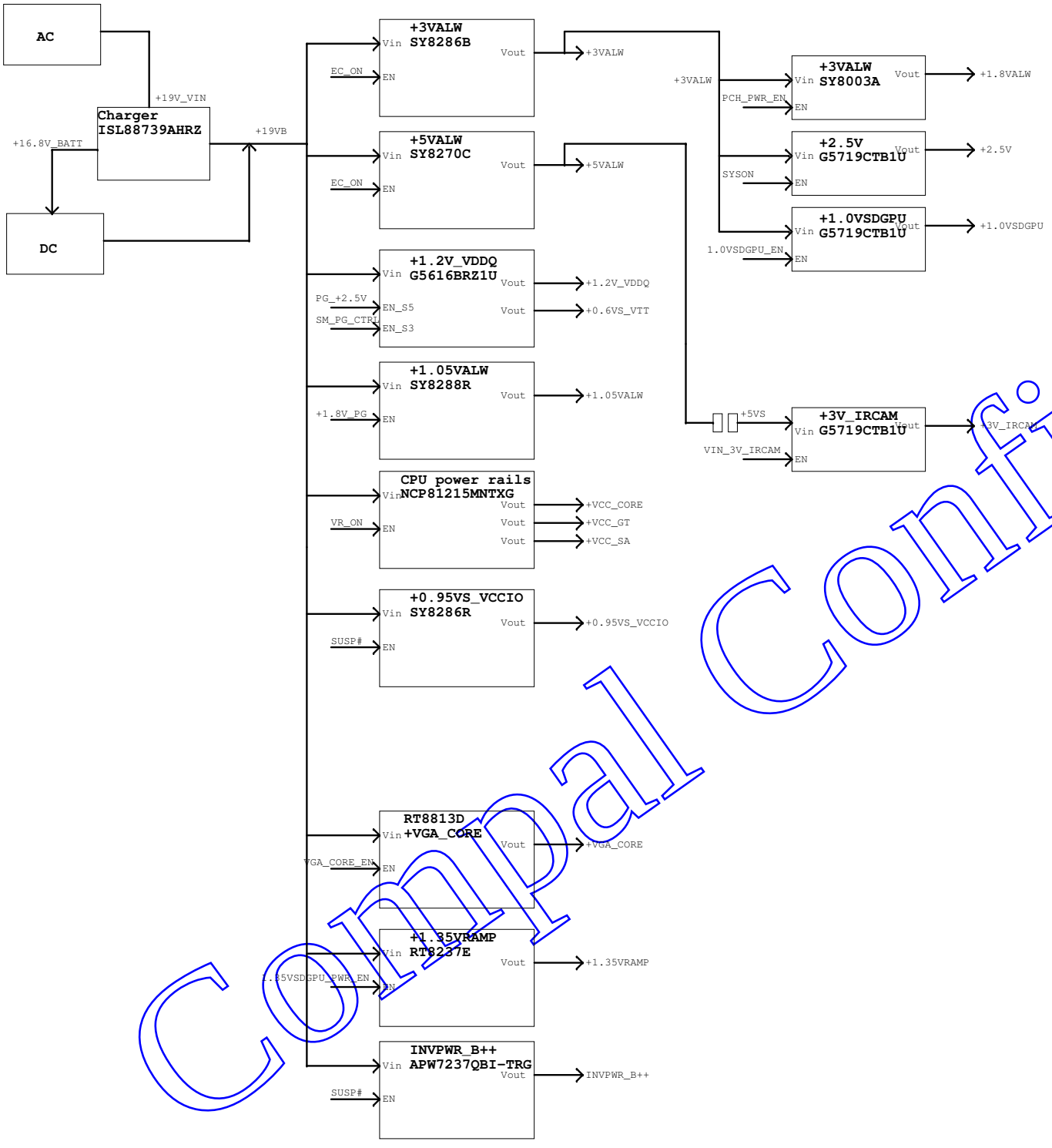
Title: Reserve		
Size: Custom	Document Number: LA-J643P	Rev: 1.0
Date: Friday, March 13, 2020	Sheet 80 of 100	



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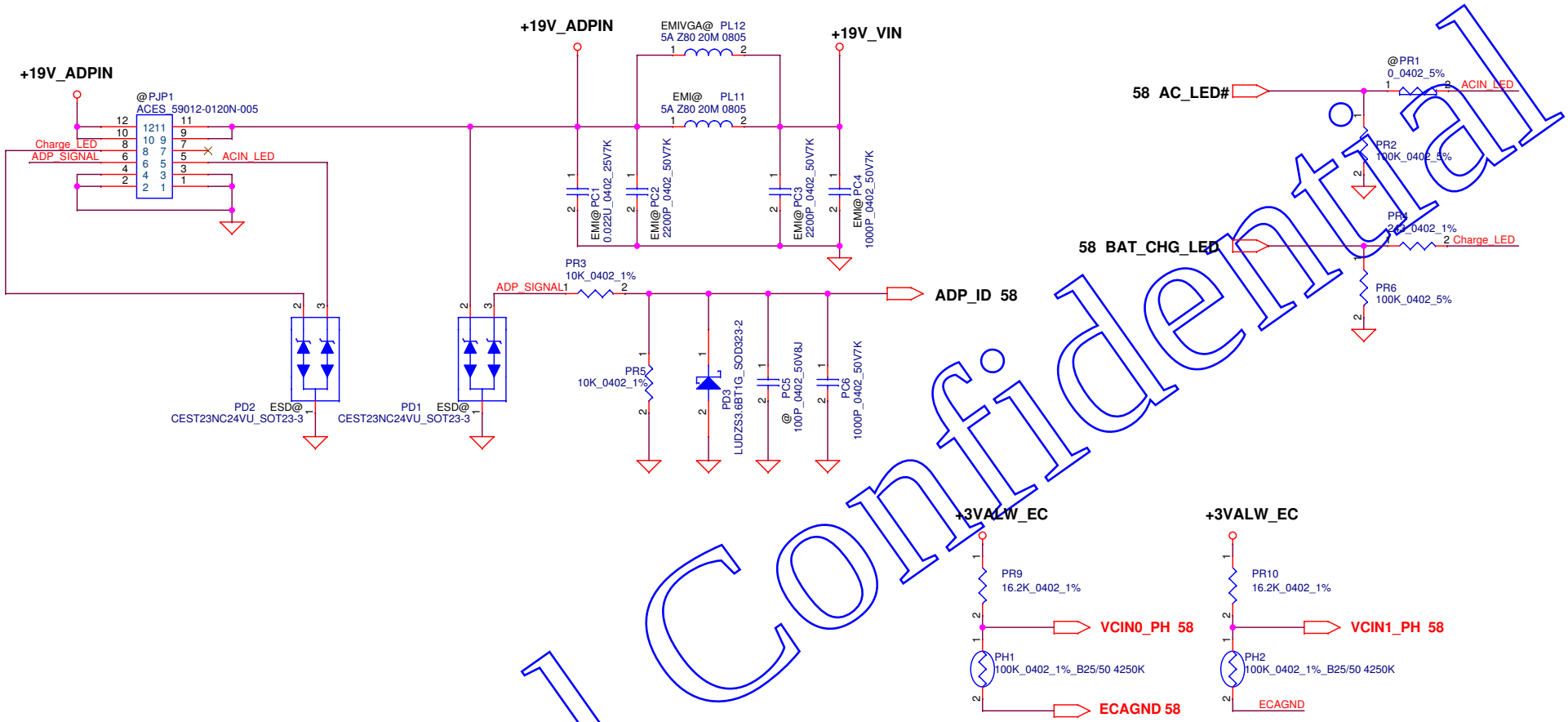

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Issued Date	2018/12/1	Deciphered Date	2020/08/24	Title: DC Conn
				Size: Document Number: Rev: 0.1
				Date: Friday, March 13, 2020 Sheet 82 of 100

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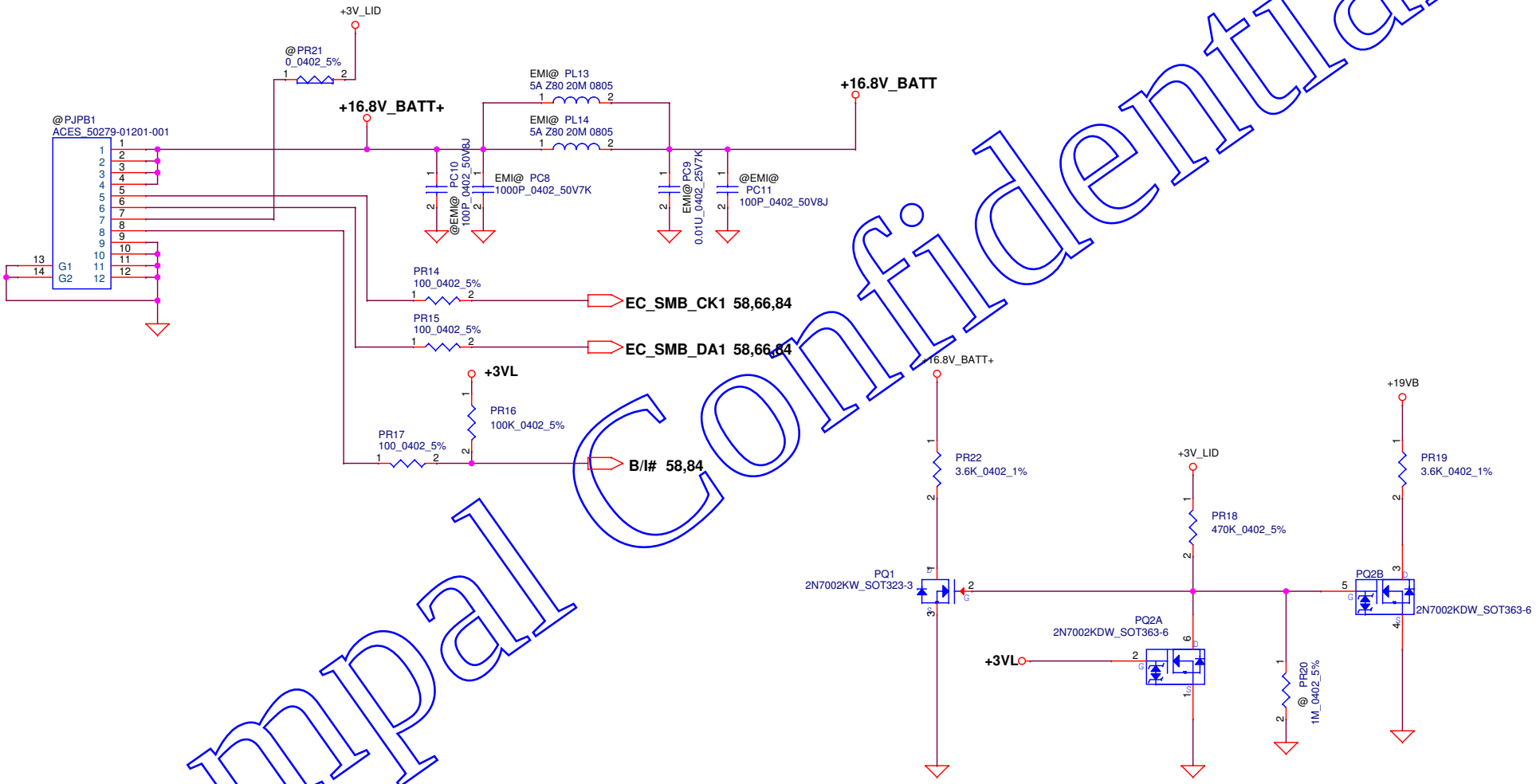

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Compal Electronics, Inc.

Title: BATT Conn

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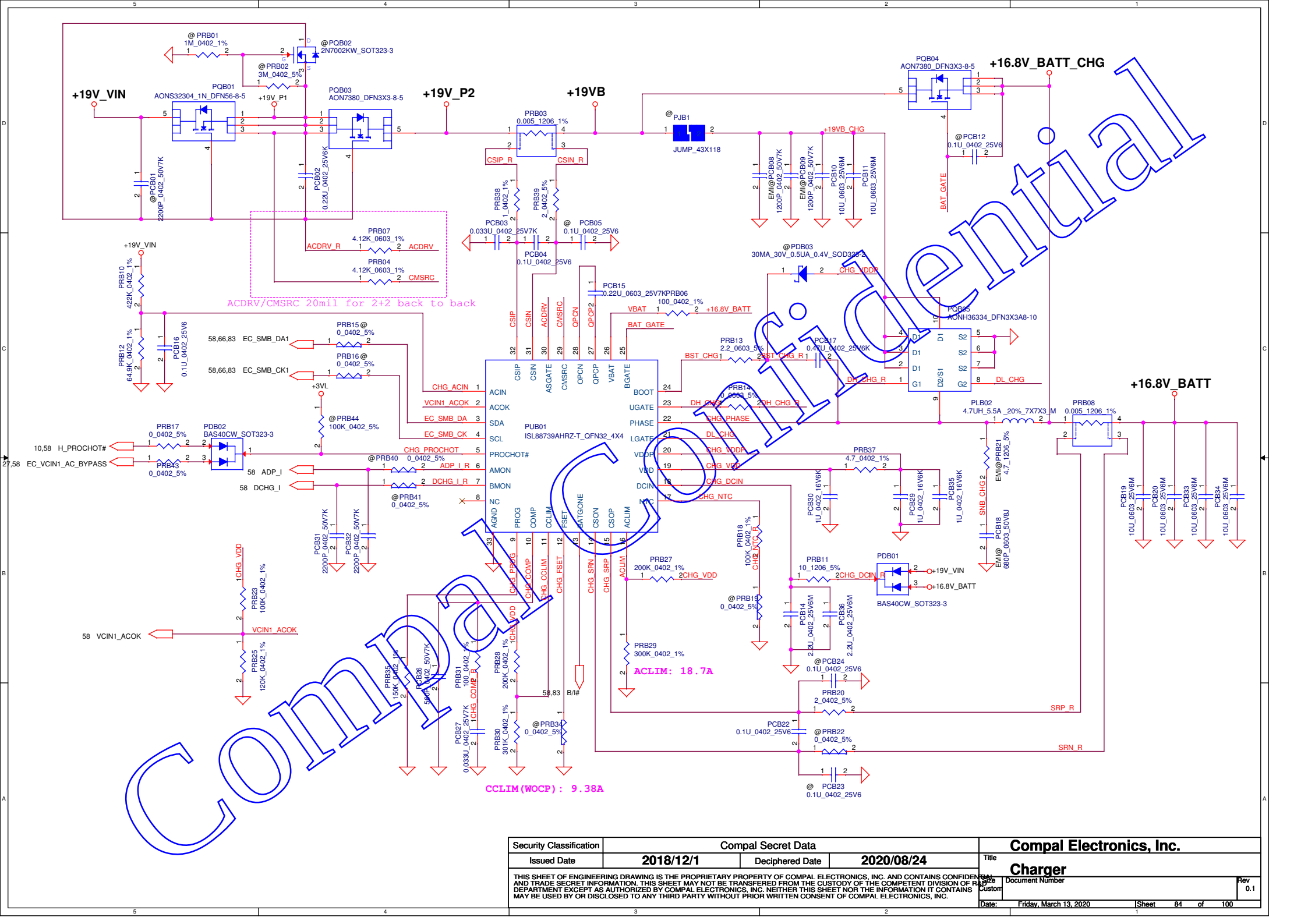

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Compal Electronics, Inc.

Title: **Charger**

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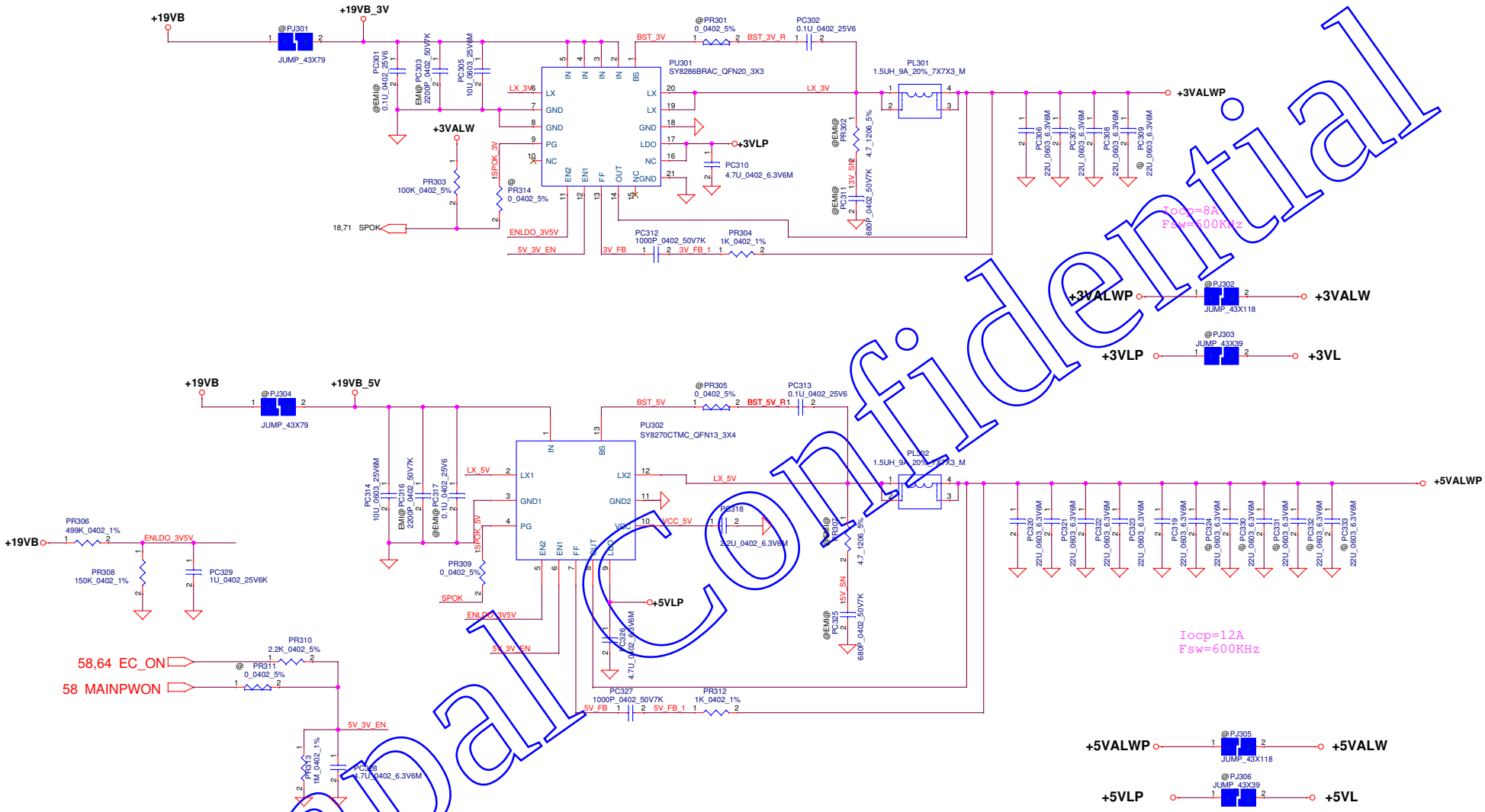

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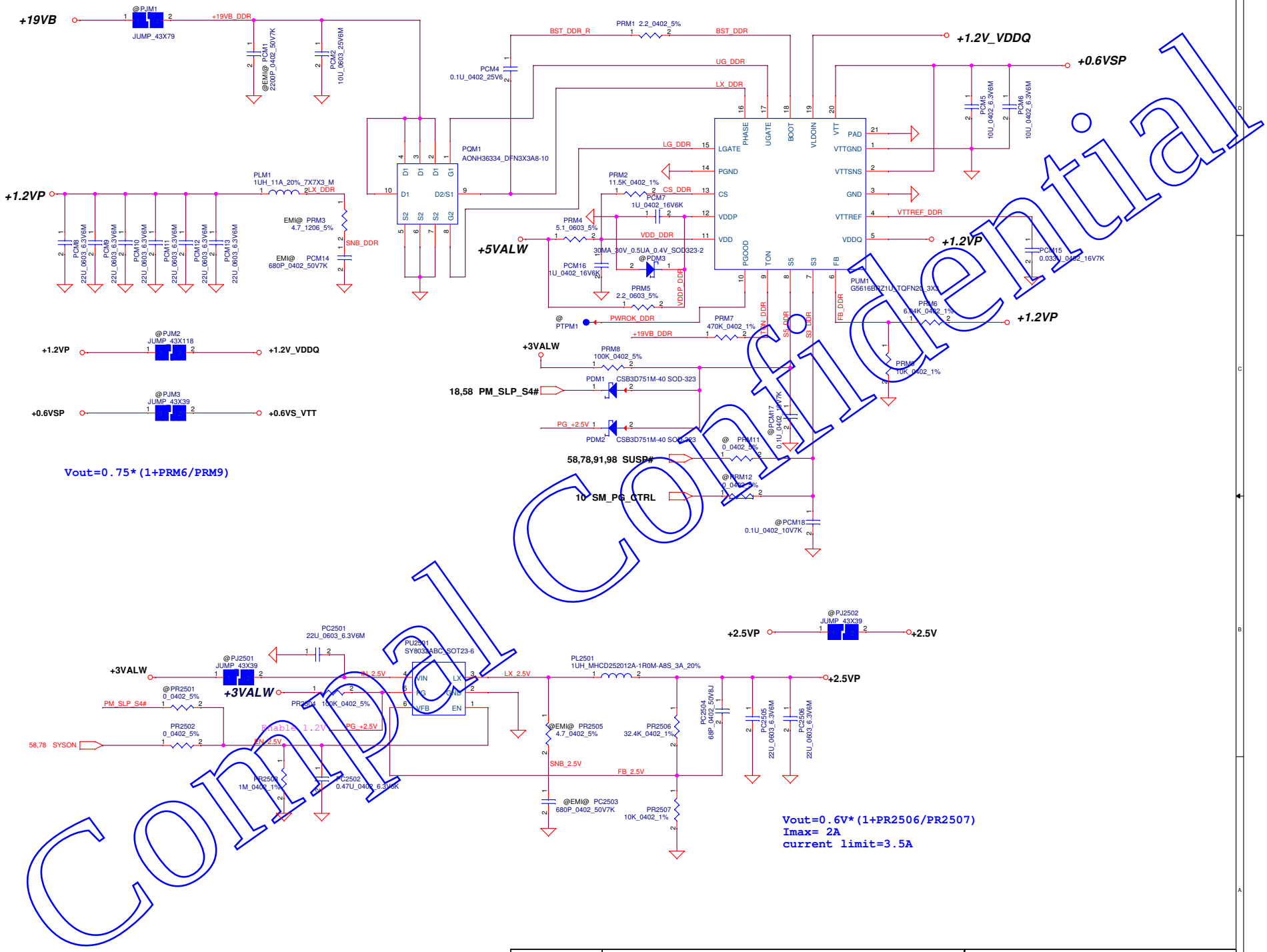
Compal Electronics, Inc.

Title: 3VALW/5VALW

Size: Custom | Document Number | Rev: 0.1

Date: Friday, March 13, 2020 | Sheet 85 of 100



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Compal Electronics, Inc.

Title: 1.2VP/0.6VSP/2.5V

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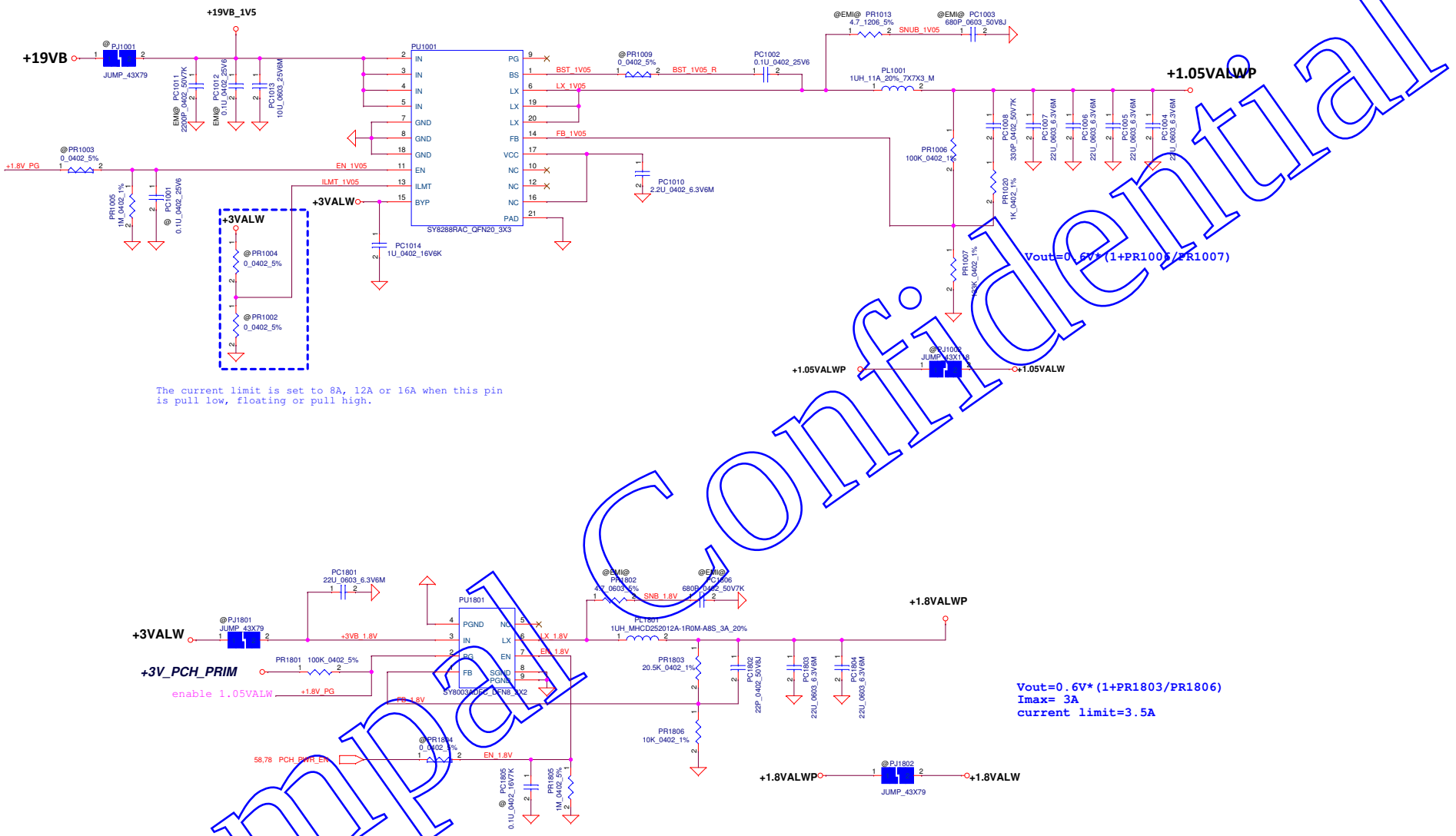

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Compal Electronics, Inc.

Title: 1.05V/1.8V

Size: C | Document Number | Rev: 0.1

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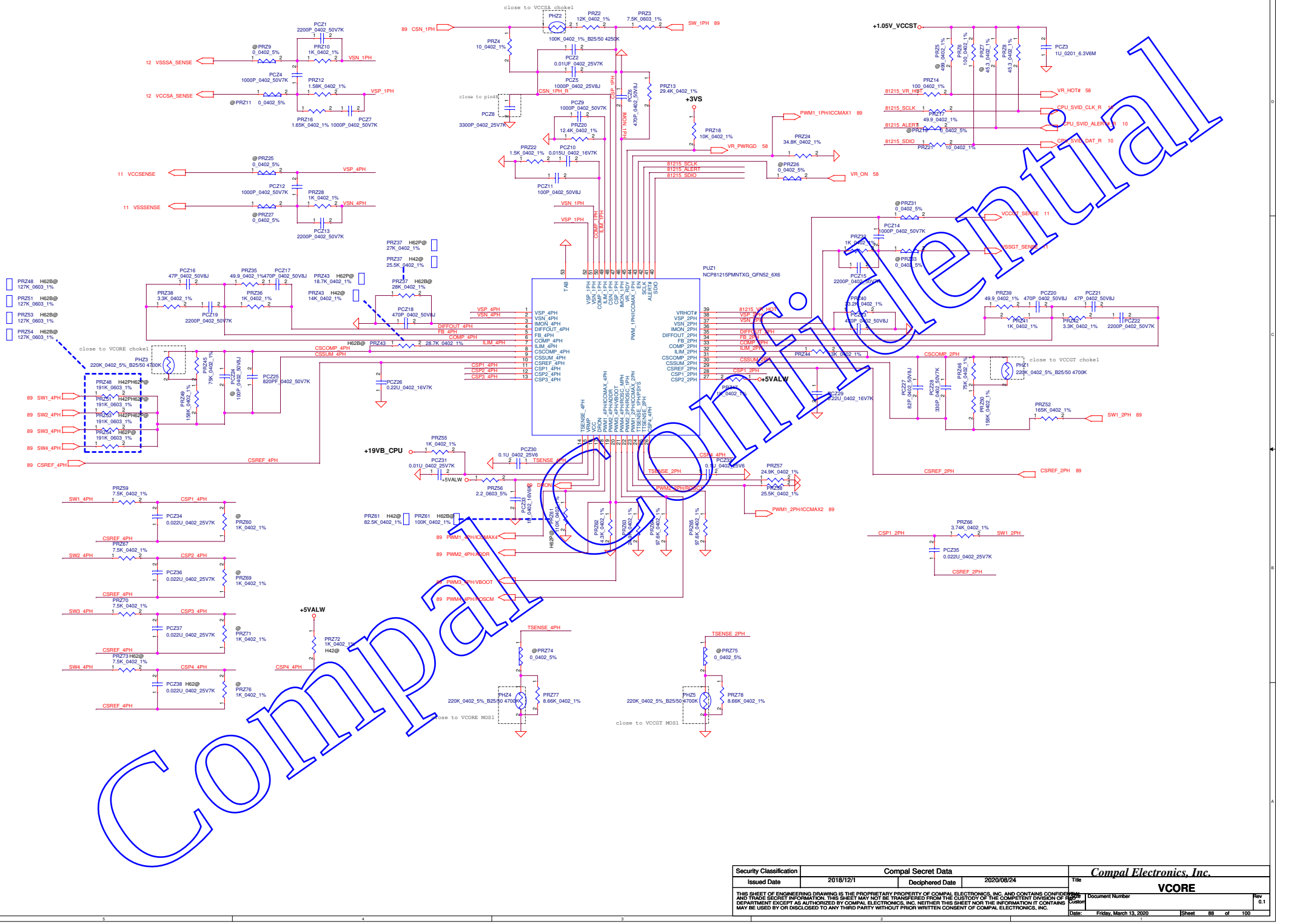

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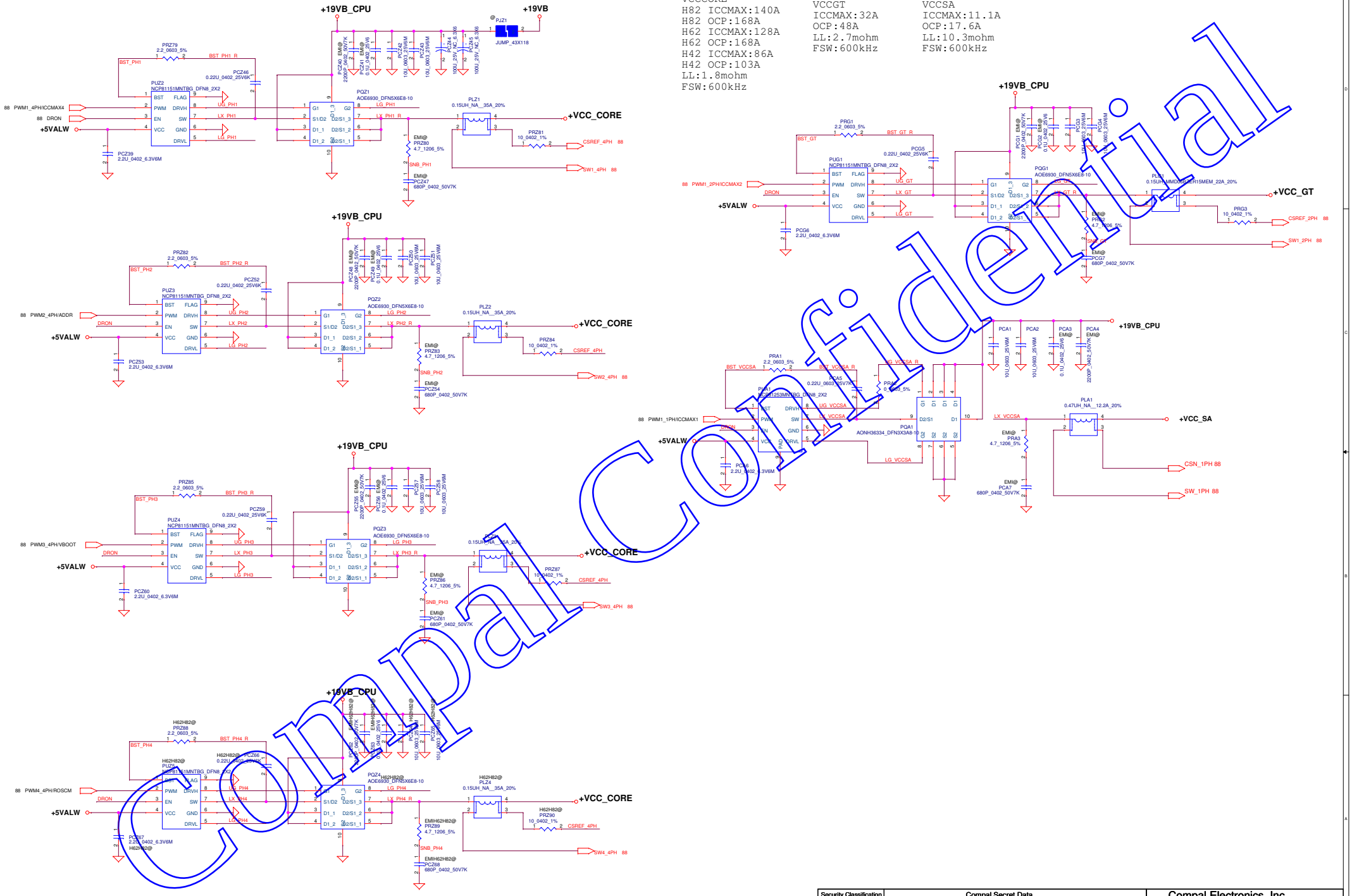
VCCCORE
H82 ICCMAX:140A
H82 OCP:168A
H62 ICCMAX:128A
H62 OCP:168A
H42 ICCMAX:86A
H42 OCP:103A
LL:1.8mohm
FSW:600kHz

VCCGT
ICCMAX:32A
OCP:48A
LL:2.7mohm
FSW:600kHz

VCCSA
ICCMAX:11.1A
OCP:17.6A
LL:10.3mohm
FSW:600kHz



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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/12/1	Deciphered Date 2020/08/24	Title VCORE SW

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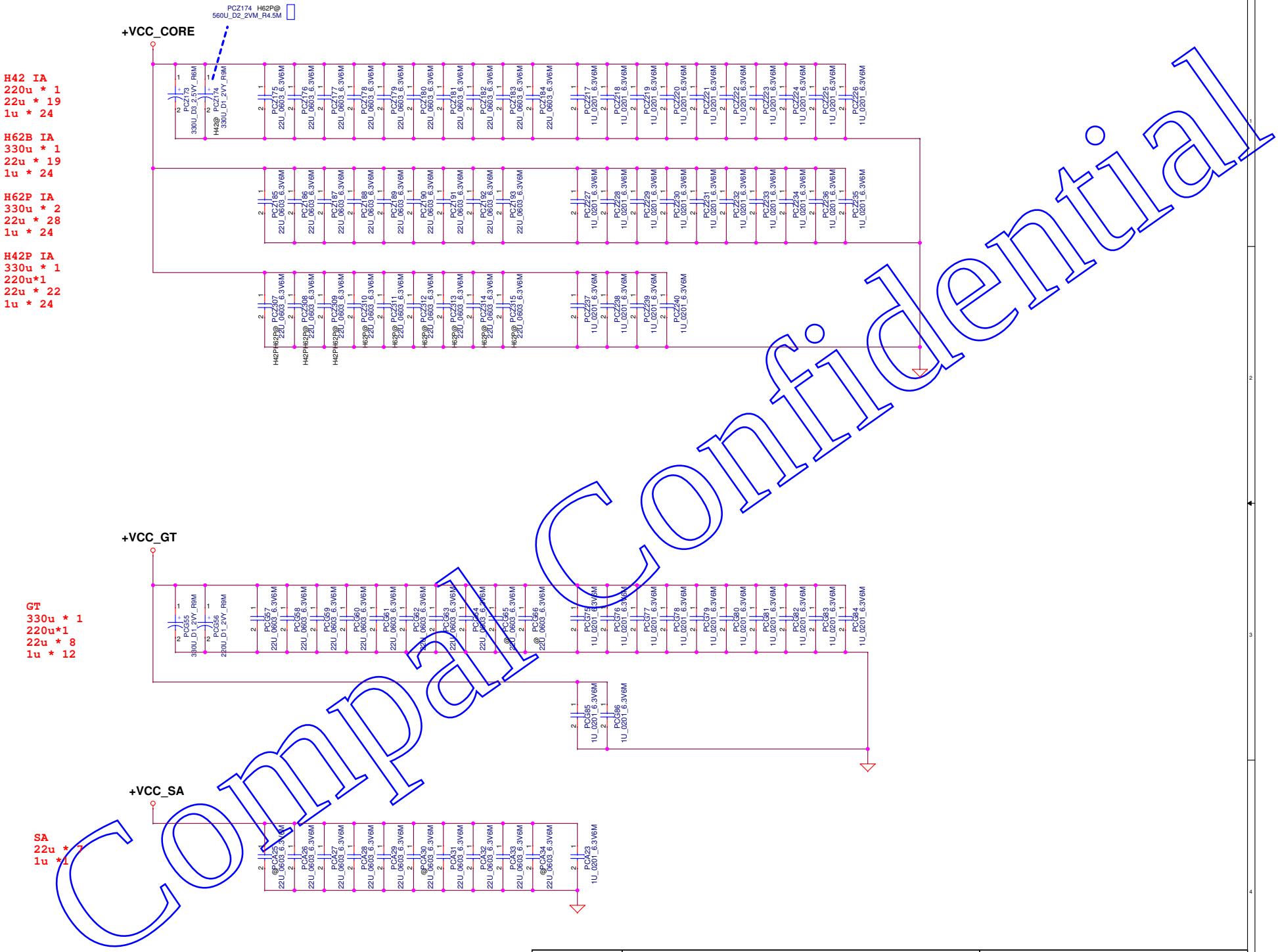

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Compal Electronics, Inc.

Title: **VCORE Decoupling**

Size: Custom | Document Number | Rev: 0.1

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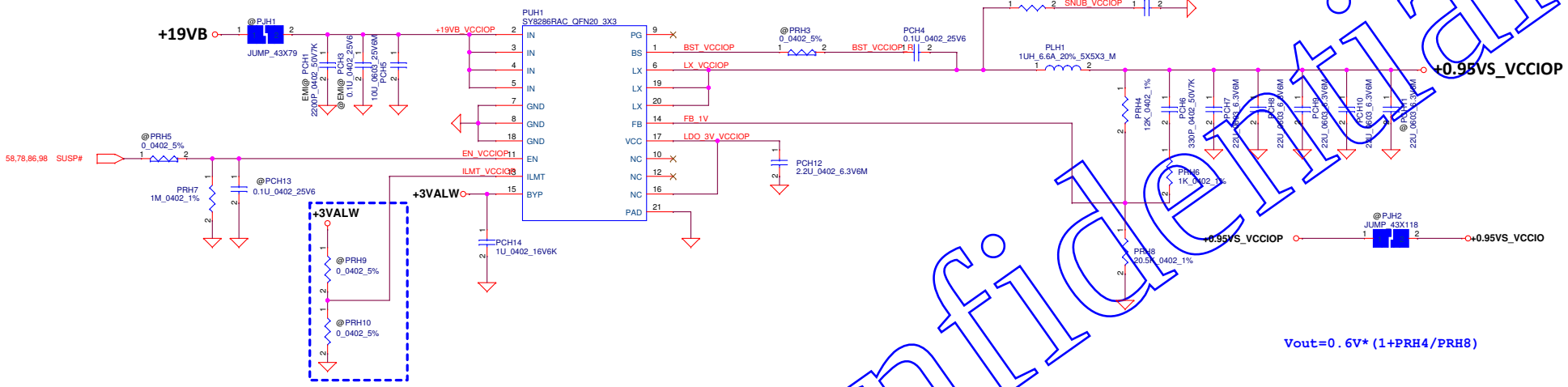

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Title: **VCCIO**

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Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

Module model information:
RT8813D_V2A for IC module
RT8813D_V2B for SW module

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

R1, R2, R3, R4, R5, C are based on VGA type to set.

+VGA_CORE
EDP Continuous 59A/N17P-G0, 50A/N17P-G1
EDP Peak 124A/N17P-G0, 90A/N17P-G1
OCP 130A
Please base on GPU spec to calculate.

PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

PWM VID Pull high on HW side

High: >1.6V
Low: <0.8V

Switching frequency setting:
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)=352Khz

Current Limit threshold setting
Rocset= (Ivalley * Rds(on) +40mv) / Iocset

Please base on GPU spec to modify output cap.

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Compal Electronics, Inc.

Title: VGA_COREP

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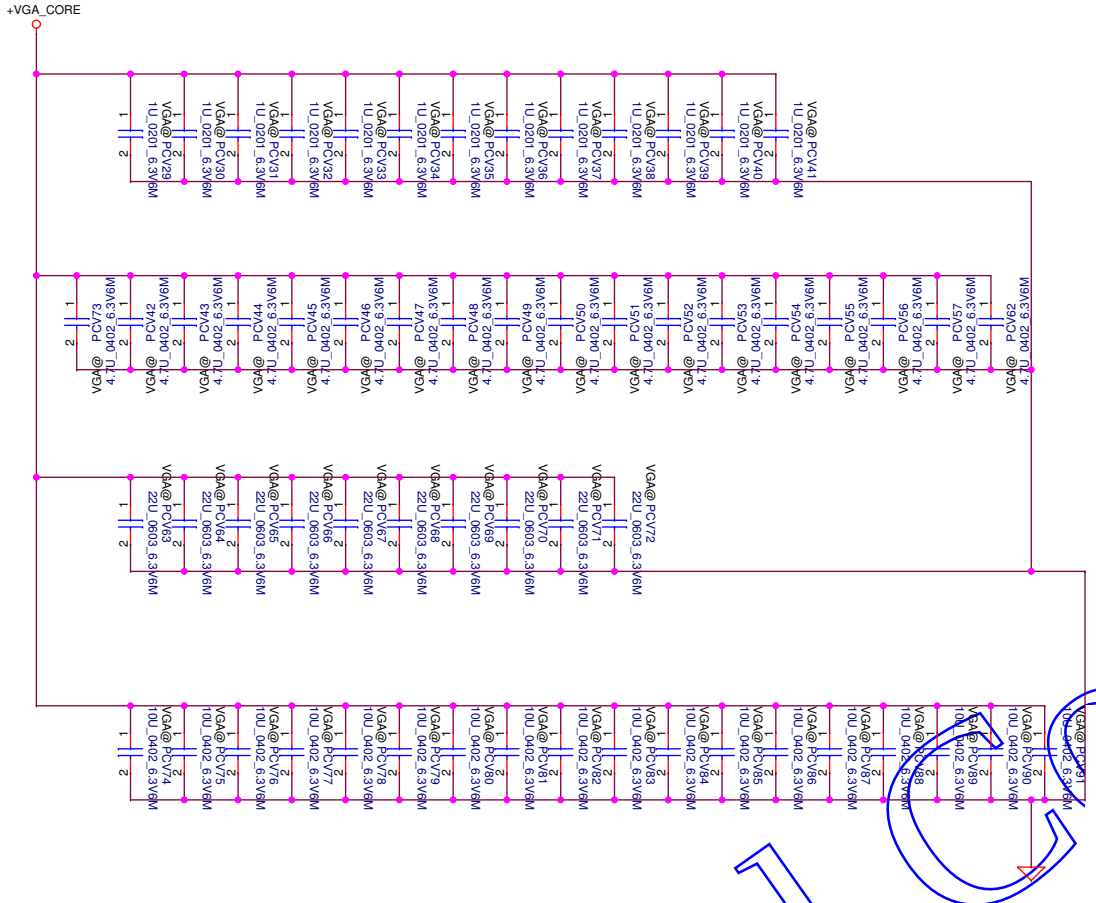

+VGA_CORE
330uF X 4
4.7uF_0603X 18
22uF_0603 X 9
10uF_0603 X 16
1uF_0402X 13

Please base on GPU spec to modify output cap.

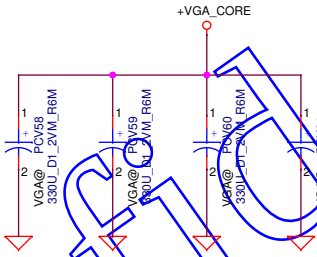

Table 7.17 GB4C-128 Package: Power Rail Filtering

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
NVVDD		Varies	8 X 1uF (0402 X6S) 16 X 4.7uF (0603 X6S)	9 X 10uF (0603 X6S) 7 X 22uF (0805 X6S) 1 X 330uF (Poscap)
NVVDDS		Varies	5 X 1uF (0402 X6S) 5 X 10uF (0603 X6S)	2 X 10uF (0603 X6S) 3 X 22uF (0805 X6S)

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Title: **VGA DECOUPLING**

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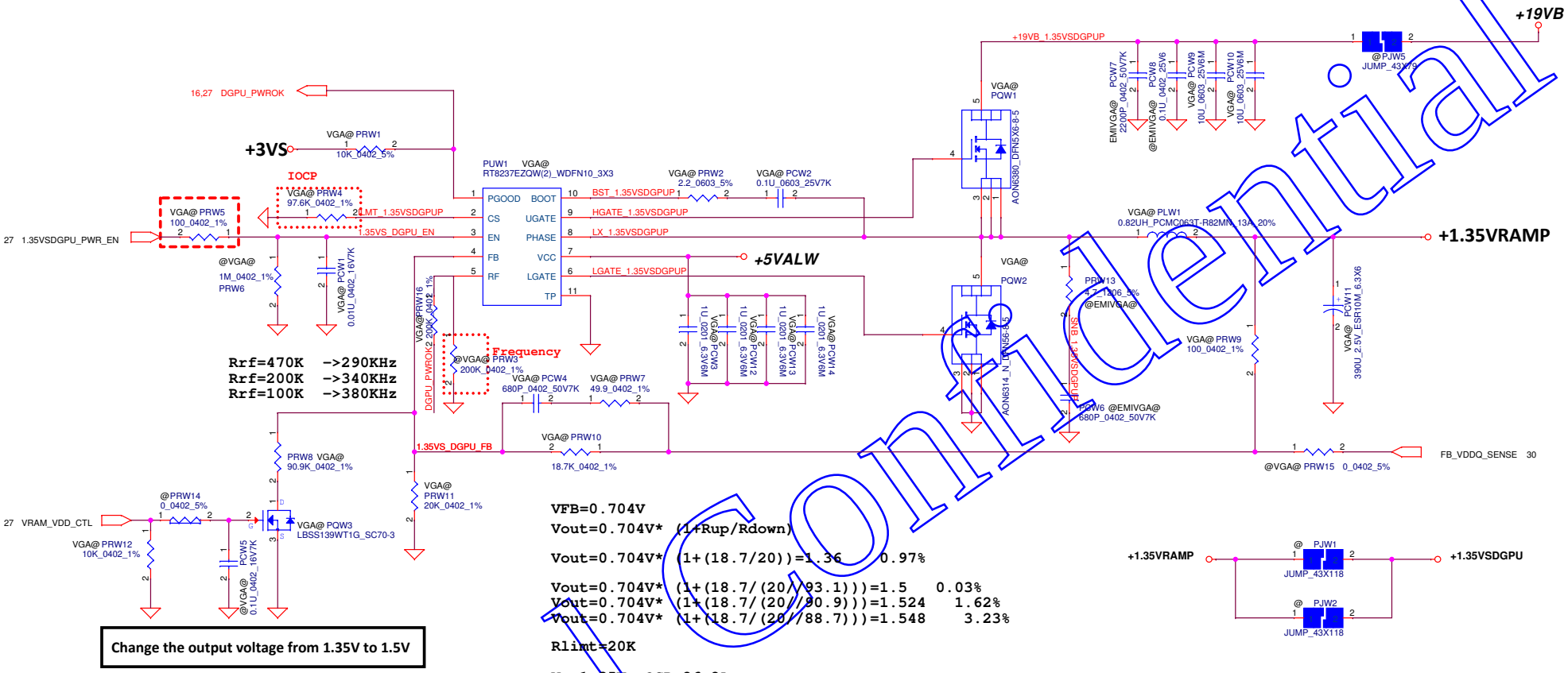

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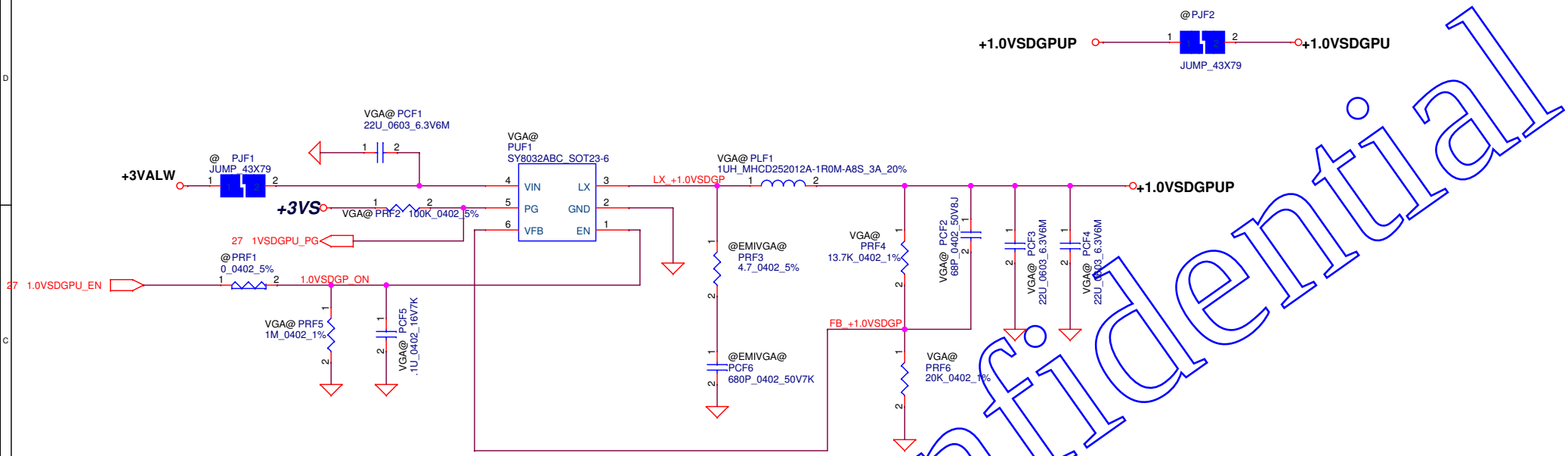
Title: *1.35VRAM*

Size: C | Document Number: <Doc> | Rev: 0.1

Date: Friday, March 13, 2020 | Sheet 94 of 100



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Title: **+1.0VSDGPUP**

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Title: **Reserve for PWR**

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SI

Item	Title	Change Description	Date
1	Charger Design change	Change PR812 from 53.6K_0402 to 64.9K_0402	2019/10/14
2	ESD Team requirements	Change PD1 PD2 from SZA0000Q500 to SZA0000O4500	2019/10/15
3	EMI Team requirements	Change PR821 PC818 from unpop to pop	2019/10/16
4	COMPAL sourcer requirements	Change PC818 from SE025681K80 to SE024681J80	2019/10/17

PV

		N17P	
Item	Title	Change Description	Date
1	CPU transient	Change PR237 from 25.5K to 27K(5%UP) Change PCA25 from pop to unpop	2019/11/13
2	Charger design change	Add PCB42 0.22U_0402	2019/11/13

MV

		N17P	
Item	Title	Change Description	Date
1	CPU transient	Change PC2173 from 220u to 330u(SH2) Change PC2174 from 330u to 560u(SH2)	2020/2/6

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Security Classification	Compal Secret Data		Compal Electronics, Inc.
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Title	PIR		
Size	Document Number		Rev
B			1.0
Date: Friday, March 19, 2021	Sheet 61 of 66		

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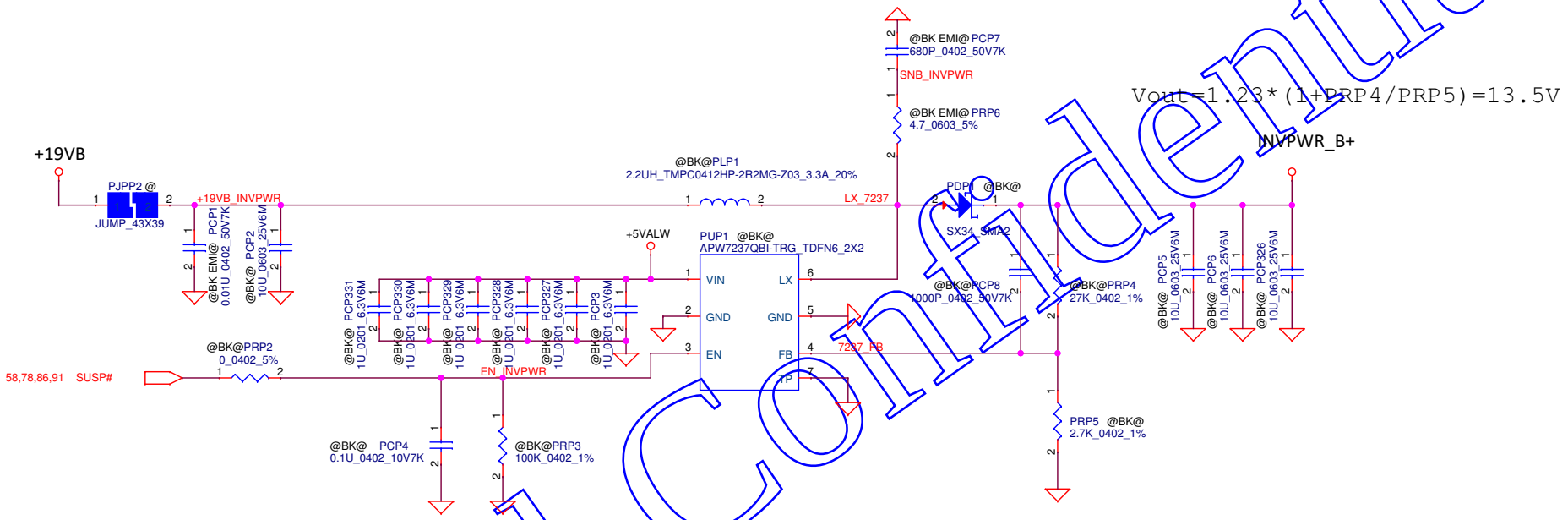

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Compal Electronics, Inc.

Title: **INVPWR_B++**

Size: B | Document Number | Rev: 0.1

Date: Friday, March 13, 2020 | Sheet 98 of 100

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Title	Reserve for PWR	
Size A	Document Number <Doc>	Rev 0.1
Date: Friday, March 13, 2020	Sheet 99 of 100	

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Title: **Reserve for PWR**

Size	Document Number	Rev
B		0.1

Date: Friday, March 13, 2020 Sheet 100 of 100