AMD AM4 B550

M-ATX (243.84 X 243.84)

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MS-7C95

Size: Custom | Document Description: 01 Cover Sheet | Rev: 20

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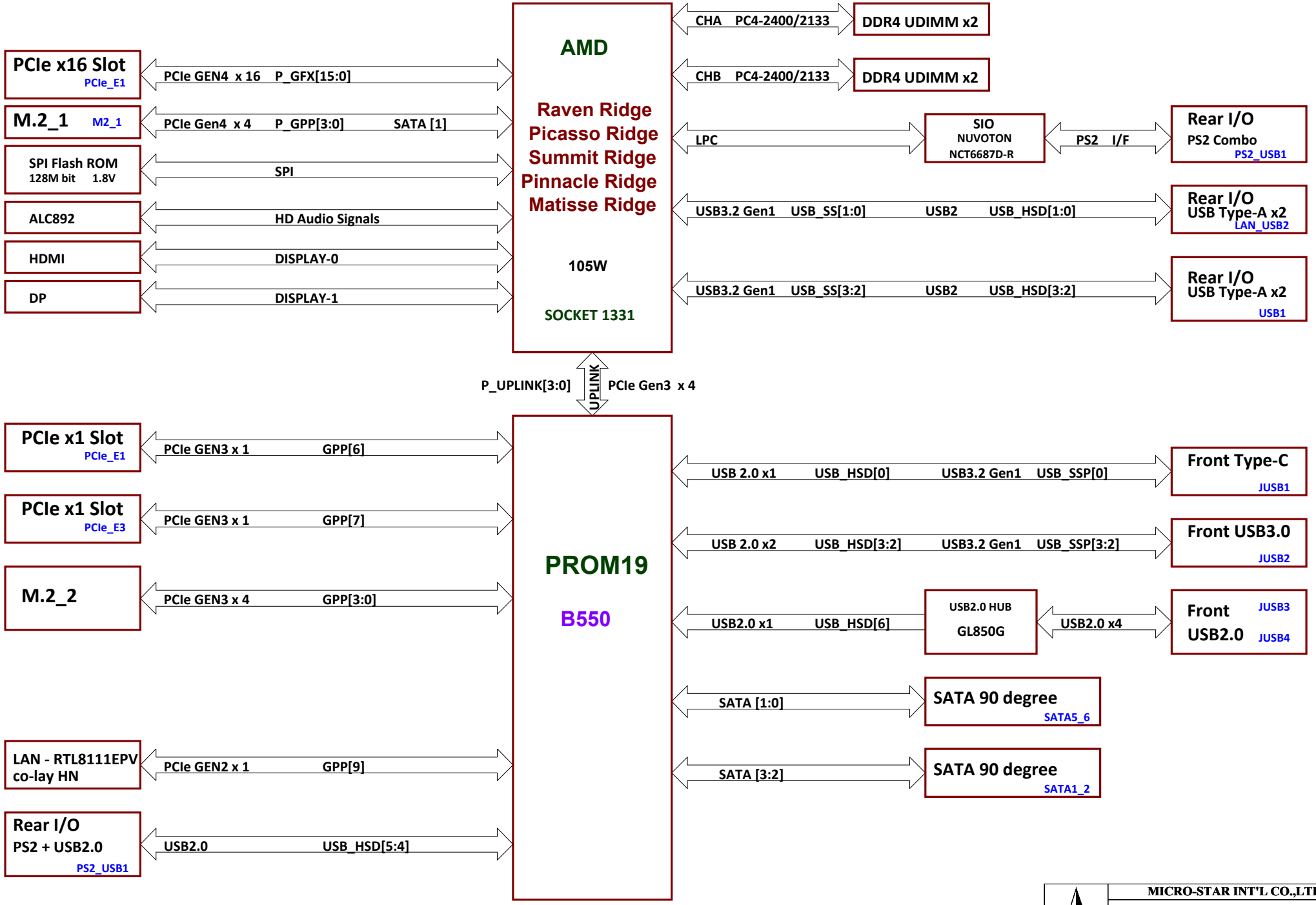

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MS-7C95

Size	Document Description	Rev
Custom	02 Block Diagram	20

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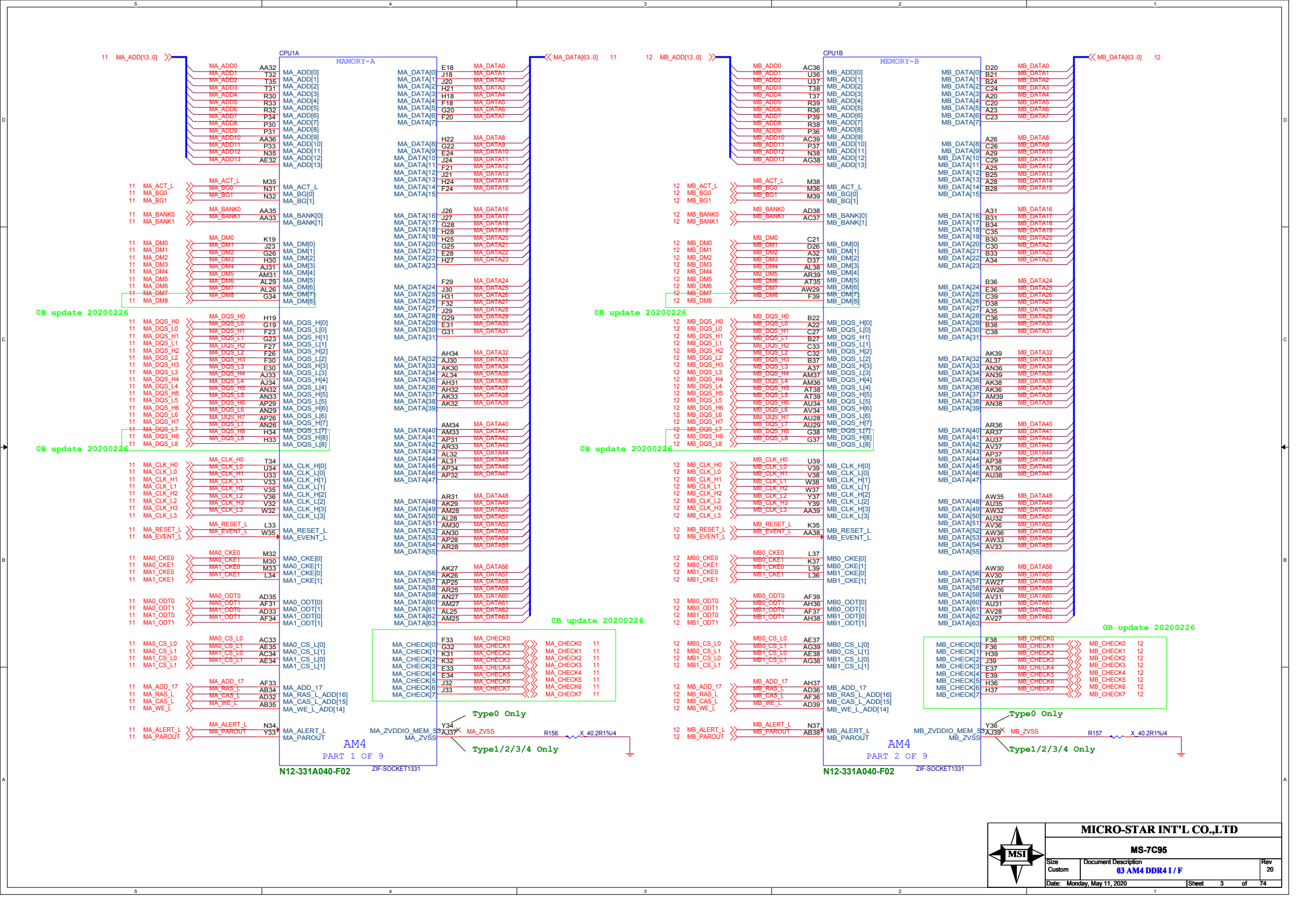
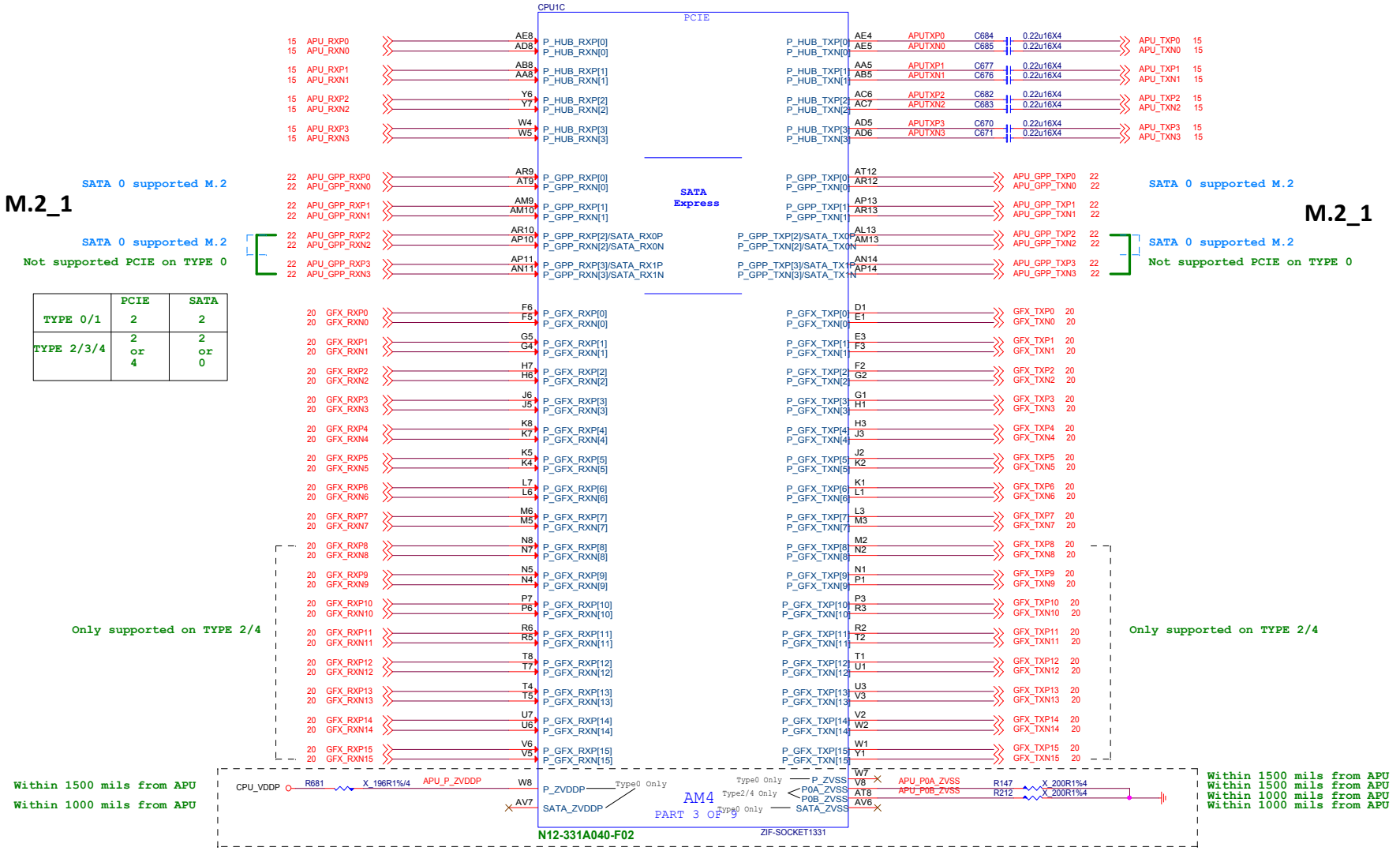

CPU1A
MEMORY-A
CPU1B
MEMORY-B
0B update 20200226
Type0 Only
Type1/2/3/4 Only
AM4
PART 1 OF 9
PART 2 OF 9
N12-331A040-F02
ZIF-SOCKET1331
MICRO-STAR INT'L CO.,LTD
MS-7C95
03 AM4 DDR4 I / F
Monday, May 11, 2020



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MS-7C95

Size	Document Description	Rev
Custom	04 AM4 PCIE / SATAE	20

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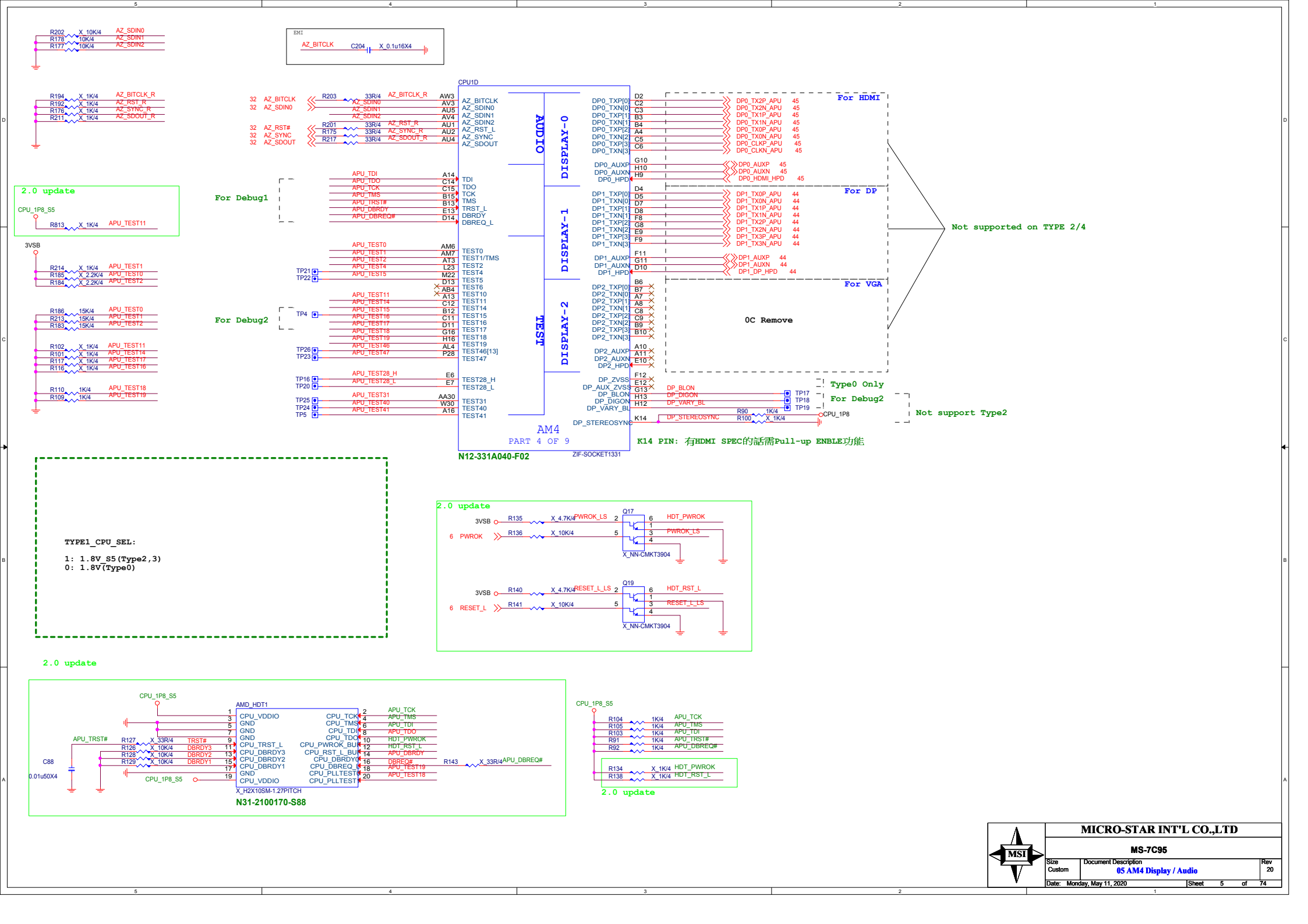

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Size	Document Description	Rev
Custom	05 AM4 Display / Audio	20
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Closed FAN , by S0ix.

25,27,28,29,30 FAN_EN

CPU_S0_IDLE

Q34 X_2N7002

R301 100K/4

3VSB C226 0.1u16X4

U18 AHCT1G126GV_SOT23-5-RH

25,34,44,52,54,57,61 SLP_S3#

R207 100K/4

APU_S0A3_GPIO R181 2.2K/4

APU_SLP_S3# R180 100K/4

T33-1G12629-T07

APU_SLP_S3#
1:See APU_S0A3_GPIO
0:High-IMpedance

AVL:T33-1G12619-N78

SLP_S3# R206 X_0R/4 APU_SLP_S3#

2.0 update FIX SMBUS PK-PK issue

3VSB R743 10K/4

Q84 2N7002D

25,54,65 CHIP_PWGD

+12V R734 2.7K/4

C1658 0.1u16X4

Q82 2N7002

SCLK0_3VSB 31,40,64

SCLK0 6,11,22,59

Q81 2N7002

SDATA0_3VSB 31,40,64

SDATA0 6,11,22,59

VCC3

SCLK0_R R279 4.7K/4

SDATA0_R R283 4.7K/4

SCLK0_3VSB R384 4.7K/4

SDATA0_3VSB R396 4.7K/4

SCLK1 R162 2.2K/4

SDATA1 R163 2.2K/4

PE2_PE3_WAKE# R678 10K/4

PEGX16_WAKE# R680 10K/4

M22_PE4_WAKE# R679 10K/4

LAN_WAKE# R165 10K/4

VCC3

R107 1K/4 APU_ALERT#

R78 1K/4 APU_PROCHOT#

R111 1K/4 APU_THERMTRIP#

CPU_1P8

Within 500mils

R94 1K/4 APU_SIC

R95 1K/4 APU_SID

R106 300R/4 PWROK

R108 300R/4 RESET_L

Follow CRB

Add for HDT and close to PIN E16 & B16

5 PWROK PWROK

5 RESET_L RESET_L

3VSB

R209 10K/4 PWRBTN#

R234 X_10K/4 APU_AM4R1

R220 10K/4 BLINK

R200 10K/4 APU_WAKE#

R195 10K/4 PCIE_RST

C216 100p50N4 PCIE_REST#

CPU_1P8_S5A

R224 22K/4 RSMRST#

C637 10u6.3X6

C233 1u6.3X4

C68 X_0.1u16X4 APU_PWROK

新 Qogir_RevD, 新 C2470,膚 不上件

0C Remove

For Moderm Standby Fail Use

APU_WAKE# PE2_PE3_WAKE#	R799 R800	X_0R/4 0R/4	PE2_PE3_WK#	PE2_PE3_WK#	21
APU_WAKE# PEGX16_WAKE#	R801 R802	X_0R/4 0R/4	PEGX16_WK#	PEGX16_WK#	20
APU_WAKE# M22_PE4_WAKE#	R803 R804	X_0R/4 0R/4	M22_PE4_WK#	M22_PE4_WK#	23
APU_WAKE# LAN_WAKE#	R805 R806	X_0R/4 0R/4	LAN_WK#	LAN_WK#	31

0C Add 20200331

CPU1E

47 APU_SVC	D17	SVC	SVI
47 APU_SVD	C17	SVD	
47 APU_SVT	A17	SVT	
47 APU_PWROK	E16	PWROK	ACPI
54 ALL_PWR_PWRGD	AM3	PWR_GOOD	
	B16	RESET_L	
25,47 APU_PROCHOT#	H15	PROCHOT_L	
	A19	THERMTRIP_L	
25,34,55,57,61 SLP_S5#	AT2	SLP_S3_L	GPIO
	AP2	SLP_S5_L	
APU_S0A3_GPIO	AR3	S0A3_GPIO/AGPIO10/SGPIO0_CLK	
S5_MUX_CTRL	AP4	S5_MUX_CTRL/EGPIO42	
25 PWRBTN#	AN5	PWR_BTN_L/AGPIO0	
BLINK	AT5	BLINK/AGPIO11	
62 SPKR	AW23	SPKR/AGPIO91	
25,54 RSMRST#	AP5	RSMRST_L	MISC
7,54,58,62 SYSRESET#	AM4	SYS_RESET_L/AGPIO1	
7,17,20,22,31 PCIE_REST#	AL7	PCIE_RST_L/EGPIO26	
25 KBRST#	AN24	ESPI_RESET_L/KBRST_L	
17,22 APU_WAKE#	AL5	WAKE_L/AGPIO2	
17,25 APU_LPC_PME#	AL2	LPC_PME_L/AGPIO22	
25 APU_SIC	B18	SIC	
25 APU_SID	C18	SID	
APU_ALERT#	D16	ALERT_L	
53,55,61 APU_AM4R1	AL8	AM4R1	
CORETYPE0	AM24	CORETYPE[0]	OC
CORETYPE1	AN9	CORETYPE[1]	
TP30 AGPIO84	AN23	FANIN0/AGPIO84	FAN
	AP23	FANOUT0/AGPIO85	
7 RTCCLK	AP8	RTCCLK	RTC
APU_32K_X1	AW5	X32K_X1	
APU_32K_X2	AW6	X32K_X2	
	AM4		SENSE
	PART 5 OF 9		

N12-331A040-F02

ZIF-SOCKET1331

0B update 20200313

R797 X_R/2

TP28

Turn off power when BIOS into deep mode

Q61 2N7002

25,57,61 DEEP_S5

Level 1.8V S5 Domain

0B update 20200313

AU25 SCLK0_R	R792	0R/4	R280 X_0R/4 SIO_SMB_MSCL 25,47,59
AV25 SDATA0_R	R793	0R/4	R284 X_0R/4 SIO_SMB_MSDA 25,47,59
			SDATA0 6,11,22,59
SCL0/I2C2_SCL/EGPIO113			
SDA0/I2C2_SDA/EGPIO114			
AK3 SCL1/I2C3_SCL/AGPIO19			SCLK1 20,31
AK2 SDA1/I2C3_SDA/AGPIO20			SDATA1 20,31

AT6	PE2_PE3_WAKE#	
AR6 AGPIO3		M2_1_SATA_DET 22
AP22 AGPIO4		DEVSLP1 22
AN8 AGPIO5/DEVSLP0		CPU_S0_IDLE 55
AP7 AGPIO6		LAN_ISOLATEB 31
AN2 AGPIO8	AGPIO9	
AN3 AGPIO9/SGPIO0_DATAOUT	PEGX16_WAKE#	
AR4 AGPIO23/SGPIO0_LOAD	M22_PE4_WAKE#	
AW17 AGPIO40/SGPIO0_DATAIN		
AV22 AGPIO86	GENINT1_L	M2_1_CARD_DET 22
AU23 GENINT1_L/AGPIO89		
AM22 GENINT2_L/AGPIO90		
SATA_ACT_L/AGPIO130		SATA_LED# 62
AT18		
AW11 EGPIO70		PM_PESLOT_AUX_RST# 21
AV12 EGPIO95		PEGX16_AUX_RST# 20
AW12 EGPIO96		EGPIO96_DRAM 63
AU13 EGPIO97		PM19_AUX_RST# 17
AV13 EGPIO98		M21_AUX_RST# 22
AT14 EGPIO99		LAN_AUX_RST# 31
EGPIO100		

0C Remove

For Select Auto or Manual

VCC3 R232 8.2K/4 GENINT1_L

R223 X_10K/4

AMD Hardware Validated Boot (HVB)
0 or NC:Disable
1:Enable

AT23 CLK_REQ0		
AV24 CLK_REQ1_M.2	CLK_REQ1_M.2	22
AT24 CLK_REQ2		
AL23 PM19_CLK_REQ_L	PM19_CLK_REQ_L	17
AR22 CLK_REQG	CLK_REQG	20
CLK_REQ0_L/SATA_IS0_L/SATA_ZP0_L/AGPIO115		
CLK_REQ1_L/AGPIO116		
CLK_REQ2_L/AGPIO117		
CLK_REQ3_L/SATA_IS1_L/SATA_ZP1_L/EGPIO118		
CLK_REQG_L/OSCIN/EGPIO132		

M2_1

RROM19 X16

AL1 APU_OC0		
AM1 LAN_WAKE#		
AR1		
AP1		
USB_OC0_L/AGPIO10	APU_OC0	43
USB_OC1_L/TDI/AGPIO17		
USB_OC2_L/TCK/AGPIO18		
USB_OC3_L/TDO/AGPIO24		

3VSB APU_OC0 R164 200K/4

F14	VDDCR_CPU_SENSE+	26,47
E15	VDDCR_SOC_SENSE+	47
VDDCR_CPU_SENSE		
VDDCR_SOC_SENSE		
G14	VDDIO_MEM_S3_SENSE	55
F15 VSS_SENSE_A	VDDCR_CPU_SENSE-	47
VDDIO_MEM_S3_SENSE	VDDCR_SOC_SENSE-	47
VSS_SENSE_A		
AL22 CPU_VDDP_SENSE	CPU_VDDP_SENSE	53
AM23 VSS_SENSE_B	TP27	
VDDP_SENSE		
VSS_SENSE_B		

CP18 X_COPPER

CP17 X_COPPER

VCC3

R252 560R/4 SATA_LED#

R250 10K/4 CLK_REQ1_M.2

R253 X_10K/4 CLK_REQ2

R248 10K/4 CLK_REQG

R442 10K/4 PM19_CLK_REQ_L

R238 X_10K/4 CLK_REQ0

R246 X_10K/4 CLK_REQ1_M.2

R249 X_10K/4 CLK_REQ2

R653 X_10K/4 PM19_CLK_REQ_L

R237 X_10K/4 CLK_REQG

Layout:Place x'tal within 1.5 inch of APU

APU_32K_X2

Y2 32.768KHZ12.5p

APU_32K_X1

R196 20M/6

C207 12p50N6

C206 12p50N6

PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2

AM4 CPU TYPE Circuit

3VSB R227 1K/4

CORETYPE1

ATX_5VSB R404 47K/4

TYPE0_CPU_SEL 7,53,54

TYPE0_CPU_SEL
0:RV
1:BR/SR/PR/MTS

CPU_1P8_S5 R414 1K/4

CORETYPE0 R415 4.7K/4 CORETYPE0R

Q47 2N3904

CORETYPE0
0:BR/SR/PR/MTS
1:RV

IB=(CPU_1P8_S5-Vbe)/5.7k
(1.8-0.95)/5.7k=0.149mA

IC=(VCC5-Vce)/47k
(5-0.2)/47k=0.102mA

CPU	TYPE	CORETYPE 1	CORETYPE 0
BR	0	0	0
NA	X	1	1
SR	2	1	0
RV/ZP	3	1	1
MTS	4	1	0

3VSB PWR_1P8_SW

R273 10K/4

R274 10K/4

AGPIO9

N-PM514BA Q33

TPM_HOLD# 7

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Size: Custom | Document Description: 06 AM4 SVI / ACPI / GPIO | Rev: 20

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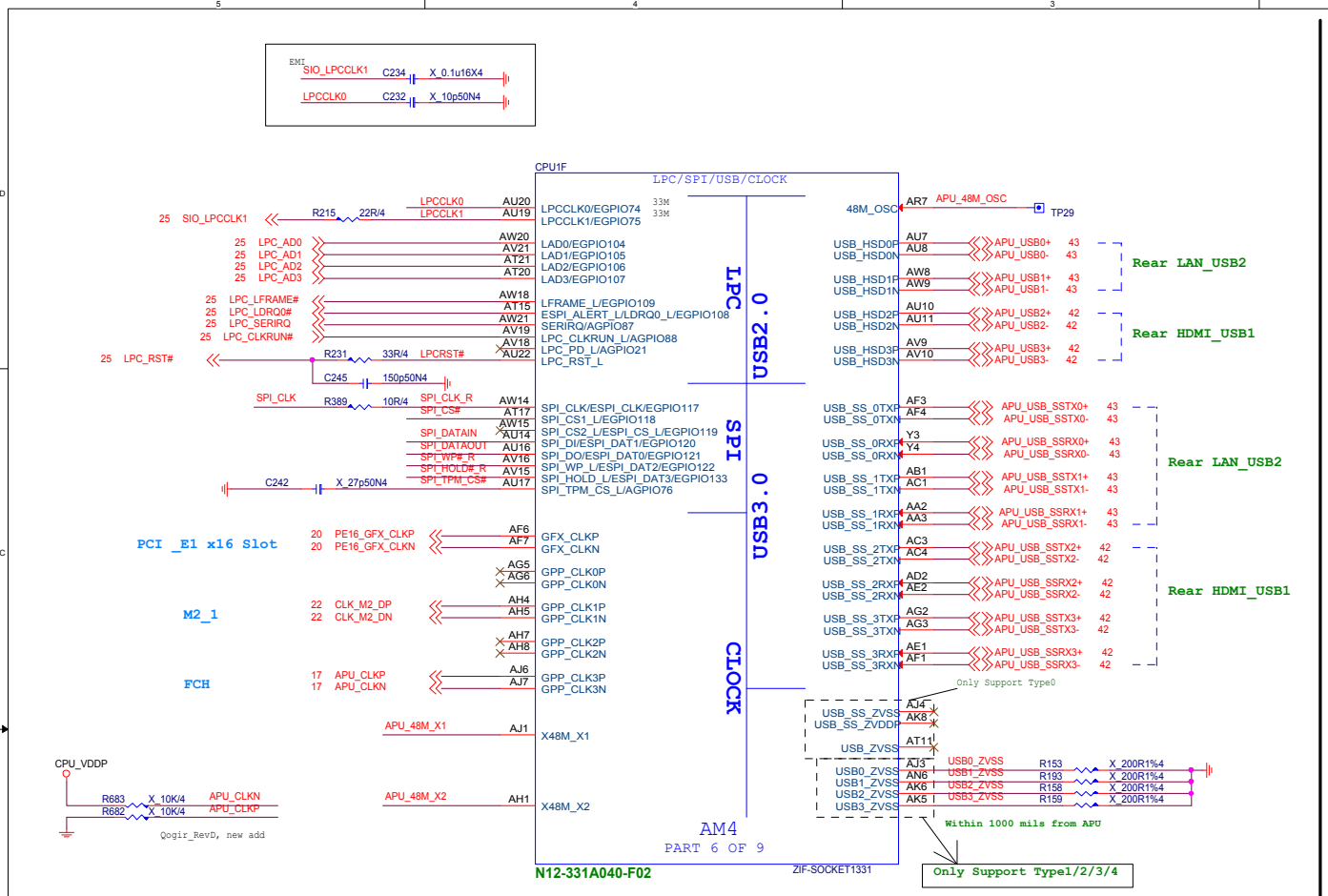
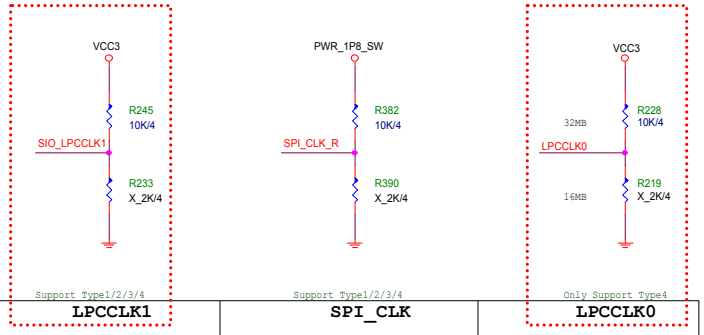


Strapping Options

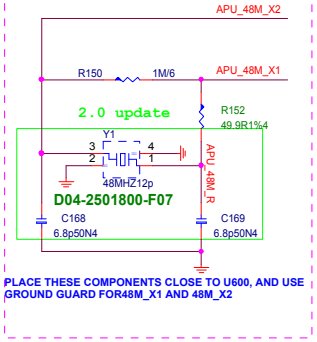


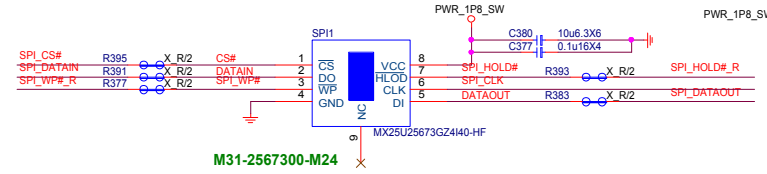
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image **(Default)**
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]

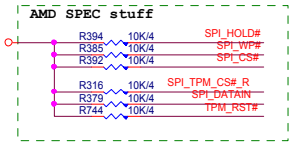
	AGPIO3	LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic	SPI ROM **(Default)**	Normal reset mode **(Default)**
PULL LOW	**(Default)** Traditional Reset logic	LPC ROM	short reset mode

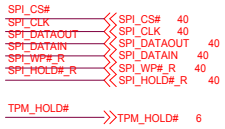
SPI ROM(1.8V)

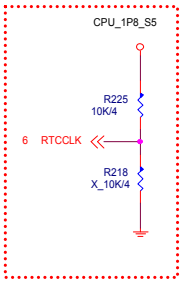
D04-2501800-F07 (Main)
D04-2501000-T16 (AVL)



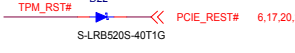


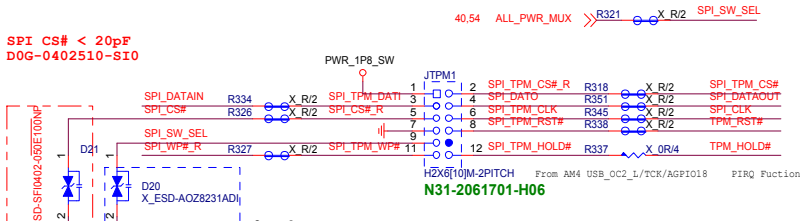


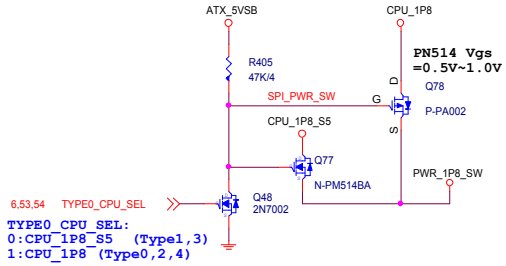




	RTCCLK
PULL HIGH	RTCCLK is input and is used as the bypass clock **(Default)**
PULL LOW	Normal Mode: Use 32Khz xtal as the source of RTC clock







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MS-7C95

Size	Document Description	Rev
Custom	07 AM4 LPC / SPI /USB/CLK/STRAP	20
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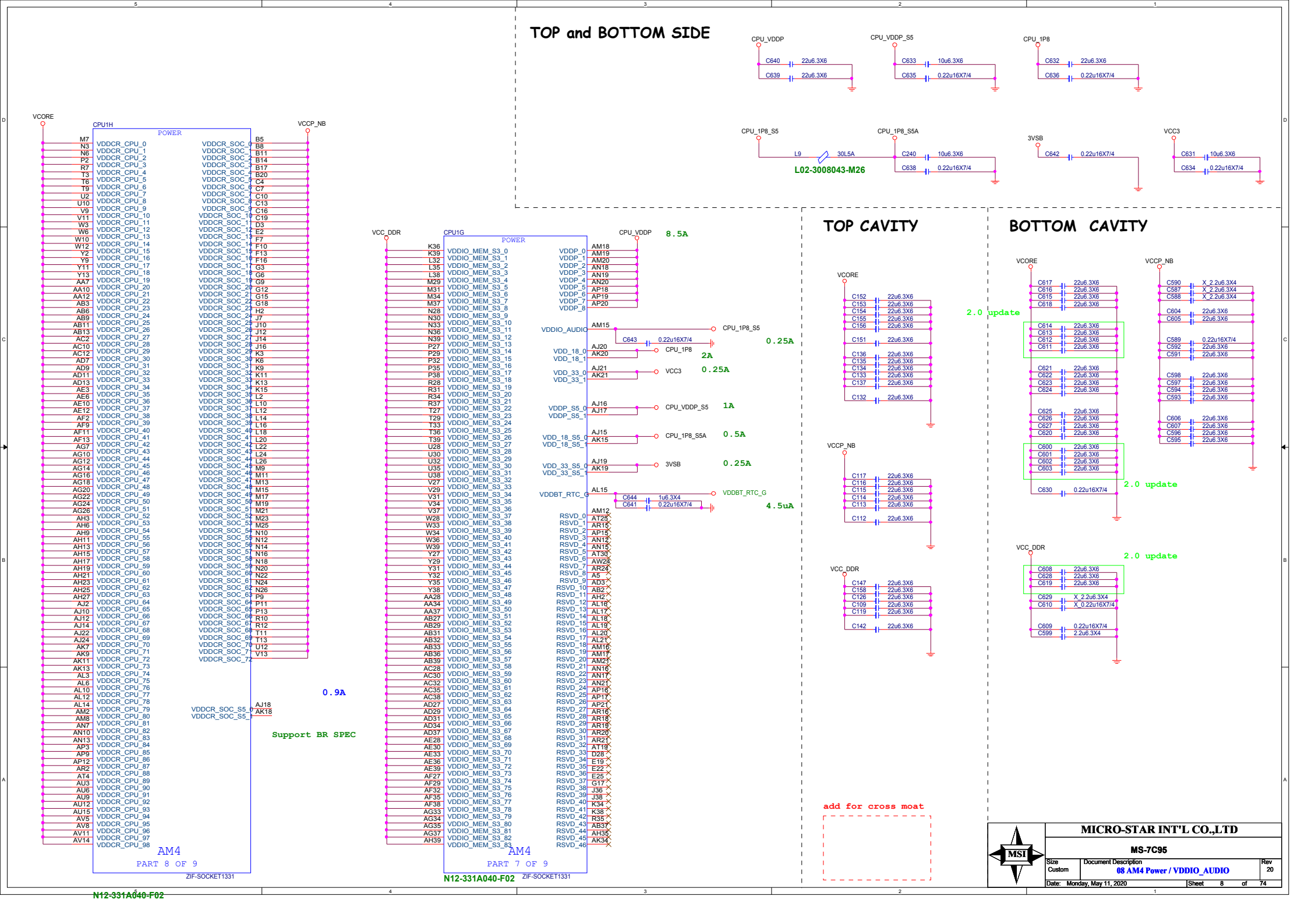
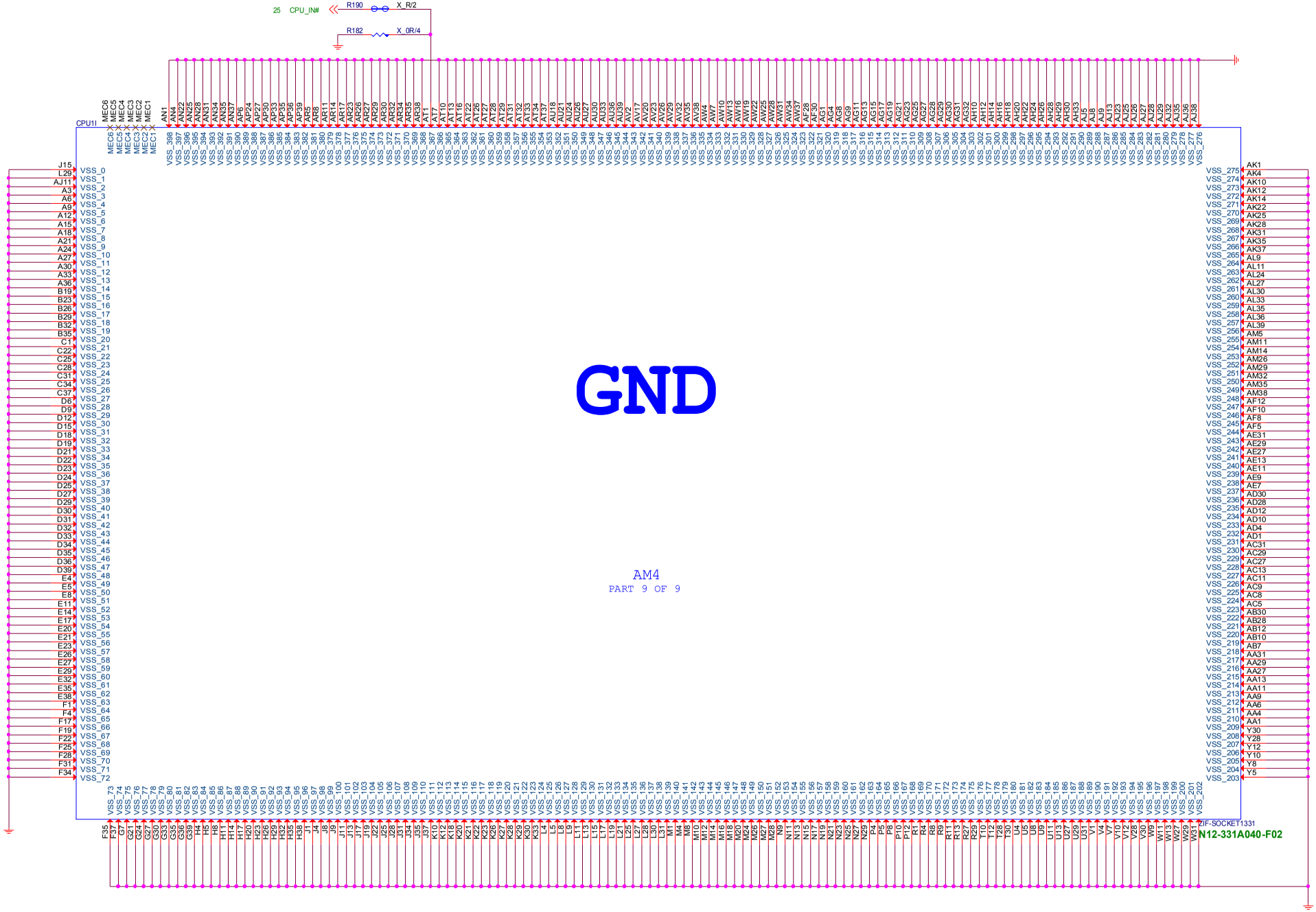
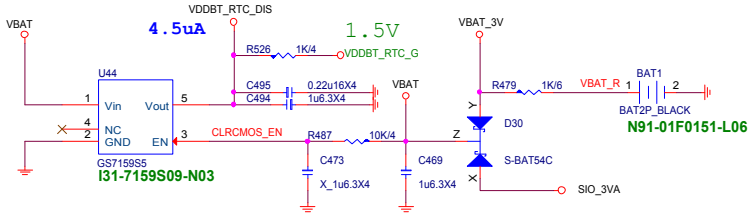

TOP and BOTTOM SIDE
CPU_VDDP
C640 22u6.3X6
C639 22u6.3X6
CPU_VDDP_S5
C633 10u6.3X6
C635 0.22u16X7/4
CPU_1P8
C632 22u6.3X6
C636 0.22u16X7/4
CPU_1P8_S5
L9 30L5A
L02-3008043-M26
CPU_1P8_S5A
C240 10u6.3X6
C638 0.22u16X7/4
3VSB
C642 0.22u16X7/4
VCC3
C631 10u6.3X6
C634 0.22u16X7/4
VCORE
CPU1H
POWER
VCCP_NB
VDDCR_CPU_0 VDDCR_CPU_1 VDDCR_CPU_2 VDDCR_CPU_3 VDDCR_CPU_4 VDDCR_CPU_5 VDDCR_CPU_6 VDDCR_CPU_7 VDDCR_CPU_8 VDDCR_CPU_9 VDDCR_CPU_10 VDDCR_CPU_11 VDDCR_CPU_12 VDDCR_CPU_13 VDDCR_CPU_14 VDDCR_CPU_15 VDDCR_CPU_16 VDDCR_CPU_17 VDDCR_CPU_18 VDDCR_CPU_19 VDDCR_CPU_20 VDDCR_CPU_21 VDDCR_CPU_22 VDDCR_CPU_23 VDDCR_CPU_24 VDDCR_CPU_25 VDDCR_CPU_26 VDDCR_CPU_27 VDDCR_CPU_28 VDDCR_CPU_29 VDDCR_CPU_30 VDDCR_CPU_31 VDDCR_CPU_32 VDDCR_CPU_33 VDDCR_CPU_34 VDDCR_CPU_35 VDDCR_CPU_36 VDDCR_CPU_37 VDDCR_CPU_38 VDDCR_CPU_39 VDDCR_CPU_40 VDDCR_CPU_41 VDDCR_CPU_42 VDDCR_CPU_43 VDDCR_CPU_44 VDDCR_CPU_45 VDDCR_CPU_46 VDDCR_CPU_47 VDDCR_CPU_48 VDDCR_CPU_49 VDDCR_CPU_50 VDDCR_CPU_51 VDDCR_CPU_52 VDDCR_CPU_53 VDDCR_CPU_54 VDDCR_CPU_55 VDDCR_CPU_56 VDDCR_CPU_57 VDDCR_CPU_58 VDDCR_CPU_59 VDDCR_CPU_60 VDDCR_CPU_61 VDDCR_CPU_62 VDDCR_CPU_63 VDDCR_CPU_64 VDDCR_CPU_65 VDDCR_CPU_66 VDDCR_CPU_67 VDDCR_CPU_68 VDDCR_CPU_69 VDDCR_CPU_70 VDDCR_CPU_71 VDDCR_CPU_72 VDDCR_CPU_73 VDDCR_CPU_74 VDDCR_CPU_75 VDDCR_CPU_76 VDDCR_CPU_77 VDDCR_CPU_78 VDDCR_CPU_79 VDDCR_CPU_80 VDDCR_CPU_81 VDDCR_CPU_82 VDDCR_CPU_83 VDDCR_CPU_84 VDDCR_CPU_85 VDDCR_CPU_86 VDDCR_CPU_87 VDDCR_CPU_88 VDDCR_CPU_89 VDDCR_CPU_90 VDDCR_CPU_91 VDDCR_CPU_92 VDDCR_CPU_93 VDDCR_CPU_94 VDDCR_CPU_95 VDDCR_CPU_96 VDDCR_CPU_97 VDDCR_CPU_98
VDDCR_SOC_0 VDDCR_SOC_1 VDDCR_SOC_2 VDDCR_SOC_3 VDDCR_SOC_4 VDDCR_SOC_5 VDDCR_SOC_6 VDDCR_SOC_7 VDDCR_SOC_8 VDDCR_SOC_9 VDDCR_SOC_10 VDDCR_SOC_11 VDDCR_SOC_12 VDDCR_SOC_13 VDDCR_SOC_14 VDDCR_SOC_15 VDDCR_SOC_16 VDDCR_SOC_17 VDDCR_SOC_18 VDDCR_SOC_19 VDDCR_SOC_20 VDDCR_SOC_21 VDDCR_SOC_22 VDDCR_SOC_23 VDDCR_SOC_24 VDDCR_SOC_25 VDDCR_SOC_26 VDDCR_SOC_27 VDDCR_SOC_28 VDDCR_SOC_29 VDDCR_SOC_30 VDDCR_SOC_31 VDDCR_SOC_32 VDDCR_SOC_33 VDDCR_SOC_34 VDDCR_SOC_35 VDDCR_SOC_36 VDDCR_SOC_37 VDDCR_SOC_38 VDDCR_SOC_39 VDDCR_SOC_40 VDDCR_SOC_41 VDDCR_SOC_42 VDDCR_SOC_43 VDDCR_SOC_44 VDDCR_SOC_45 VDDCR_SOC_46 VDDCR_SOC_47 VDDCR_SOC_48 VDDCR_SOC_49 VDDCR_SOC_50 VDDCR_SOC_51 VDDCR_SOC_52 VDDCR_SOC_53 VDDCR_SOC_54 VDDCR_SOC_55 VDDCR_SOC_56 VDDCR_SOC_57 VDDCR_SOC_58 VDDCR_SOC_59 VDDCR_SOC_60 VDDCR_SOC_61 VDDCR_SOC_62 VDDCR_SOC_63 VDDCR_SOC_64 VDDCR_SOC_65 VDDCR_SOC_66 VDDCR_SOC_67 VDDCR_SOC_68 VDDCR_SOC_69 VDDCR_SOC_70 VDDCR_SOC_71 VDDCR_SOC_72
VDDCR_SOC_S5_0 VDDCR_SOC_S5_1
0.9A
Support BR SPEC
AM4
PART 8 OF 9
ZIF-SOCKET1331
N12-331A040-F02
VCC_DDR
CPU1G
POWER
CPU_VDDP
8.5A
VDDIO_MEM_S3_0 VDDIO_MEM_S3_1 VDDIO_MEM_S3_2 VDDIO_MEM_S3_3 VDDIO_MEM_S3_4 VDDIO_MEM_S3_5 VDDIO_MEM_S3_6 VDDIO_MEM_S3_7 VDDIO_MEM_S3_8 VDDIO_MEM_S3_9 VDDIO_MEM_S3_10 VDDIO_MEM_S3_11 VDDIO_MEM_S3_12 VDDIO_MEM_S3_13 VDDIO_MEM_S3_14 VDDIO_MEM_S3_15 VDDIO_MEM_S3_16 VDDIO_MEM_S3_17 VDDIO_MEM_S3_18 VDDIO_MEM_S3_19 VDDIO_MEM_S3_20 VDDIO_MEM_S3_21 VDDIO_MEM_S3_22 VDDIO_MEM_S3_23 VDDIO_MEM_S3_24 VDDIO_MEM_S3_25 VDDIO_MEM_S3_26 VDDIO_MEM_S3_27 VDDIO_MEM_S3_28 VDDIO_MEM_S3_29 VDDIO_MEM_S3_30 VDDIO_MEM_S3_31 VDDIO_MEM_S3_32 VDDIO_MEM_S3_33 VDDIO_MEM_S3_34 VDDIO_MEM_S3_35 VDDIO_MEM_S3_36 VDDIO_MEM_S3_37 VDDIO_MEM_S3_38 VDDIO_MEM_S3_39 VDDIO_MEM_S3_40 VDDIO_MEM_S3_41 VDDIO_MEM_S3_42 VDDIO_MEM_S3_43 VDDIO_MEM_S3_44 VDDIO_MEM_S3_45 VDDIO_MEM_S3_46 VDDIO_MEM_S3_47 VDDIO_MEM_S3_48 VDDIO_MEM_S3_49 VDDIO_MEM_S3_50 VDDIO_MEM_S3_51 VDDIO_MEM_S3_52 VDDIO_MEM_S3_53 VDDIO_MEM_S3_54 VDDIO_MEM_S3_55 VDDIO_MEM_S3_56 VDDIO_MEM_S3_57 VDDIO_MEM_S3_58 VDDIO_MEM_S3_59 VDDIO_MEM_S3_60 VDDIO_MEM_S3_61 VDDIO_MEM_S3_62 VDDIO_MEM_S3_63 VDDIO_MEM_S3_64 VDDIO_MEM_S3_65 VDDIO_MEM_S3_66 VDDIO_MEM_S3_67 VDDIO_MEM_S3_68 VDDIO_MEM_S3_69 VDDIO_MEM_S3_70 VDDIO_MEM_S3_71 VDDIO_MEM_S3_72 VDDIO_MEM_S3_73 VDDIO_MEM_S3_74 VDDIO_MEM_S3_75 VDDIO_MEM_S3_76 VDDIO_MEM_S3_77 VDDIO_MEM_S3_78 VDDIO_MEM_S3_79 VDDIO_MEM_S3_80 VDDIO_MEM_S3_81 VDDIO_MEM_S3_82 VDDIO_MEM_S3_83
VDDP_0 VDDP_1 VDDP_2 VDDP_3 VDDP_4 VDDP_5 VDDP_6 VDDP_7 VDDP_8
VDDIO_AUDIO
CPU_1P8_S5
C643 0.22u16X7/4
0.25A
VDD_18_0 VDD_18_1
CPU_1P8
2A
VDD_33_0 VDD_33_1
VCC3
0.25A
VDDP_S5_0 VDDP_S5_1
CPU_VDDP_S5
1A
VDD_18_S5_0 VDD_18_S5_1
CPU_1P8_S5A
0.5A
VDD_33_S5_0 VDD_33_S5_1
3VSB
0.25A
VDDBT_RTC_0
C644 1u6.3X4
C641 0.22u16X7/4
VDDBT_RTC_G
4.5uA
RSVD_0 RSVD_1 RSVD_2 RSVD_3 RSVD_4 RSVD_5 RSVD_6 RSVD_7 RSVD_8 RSVD_9 RSVD_10 RSVD_11 RSVD_12 RSVD_13 RSVD_14 RSVD_15 RSVD_16 RSVD_17 RSVD_18 RSVD_19 RSVD_20 RSVD_21 RSVD_22 RSVD_23 RSVD_24 RSVD_25 RSVD_26 RSVD_27 RSVD_28 RSVD_29 RSVD_30 RSVD_31 RSVD_32 RSVD_33 RSVD_34 RSVD_35 RSVD_36 RSVD_37 RSVD_38 RSVD_39 RSVD_40 RSVD_41 RSVD_42 RSVD_43 RSVD_44 RSVD_45 RSVD_46
AM4
PART 7 OF 9
ZIF-SOCKET1331
N12-331A040-F02
TOP CAVITY
VCORE
C152 C153 C154 C155 C156 22u6.3X6
C151 22u6.3X6
C136 C135 C134 C133 C137 22u6.3X6
C132 22u6.3X6
VCCP_NB
C117 C116 C115 C114 C113 22u6.3X6
C112 22u6.3X6
VCC_DDR
C147 C158 C126 C109 C119 22u6.3X6
C142 22u6.3X6
add for cross moat
BOTTOM CAVITY
VCORE
C617 C616 C615 C618 22u6.3X6
2.0 update
C614 C613 C612 C611 22u6.3X6
C621 C622 C623 C624 22u6.3X6
C625 C626 C627 C620 22u6.3X6
C600 C601 C602 C603 22u6.3X6
C630 0.22u16X7/4
2.0 update
VCCP_NB
C590 C587 C588 X_2.2u6.3X4
C604 C605 22u6.3X6
C589 C592 C591 22u6.3X6
C598 C597 C594 C593 22u6.3X6
C606 C607 C596 C595 22u6.3X6
VCC_DDR
2.0 update
C608 C628 C619 22u6.3X6
C629 C610 X_2.2u6.3X4
X_0.22u16X7/4
C609 C599 0.22u16X7/4
2.2u6.3X4
MICRO-STAR INT'L CO.,LTD
MS-7C95
Size Custom
Document Description
08 AM4 Power / VDDIO_AUDIO
Rev 20
Date: Monday, May 11, 2020
Sheet 8 of 74

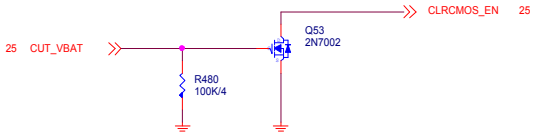


MICRO-STAR INT'L CO.,LTD	
MS-7C95	
Size: Custom	Document Description: 09 AM4 GND
Rev: 20	
Date: Monday, May 11, 2020	Sheet 9 of 74

RTC & Clear CMOS Circuit

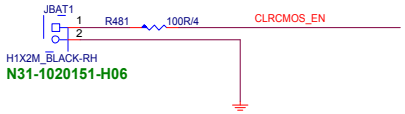
VDDBT_RTC_G	1.50	All	4.5uA	–	–





RTC Backup

Clear CMOS button

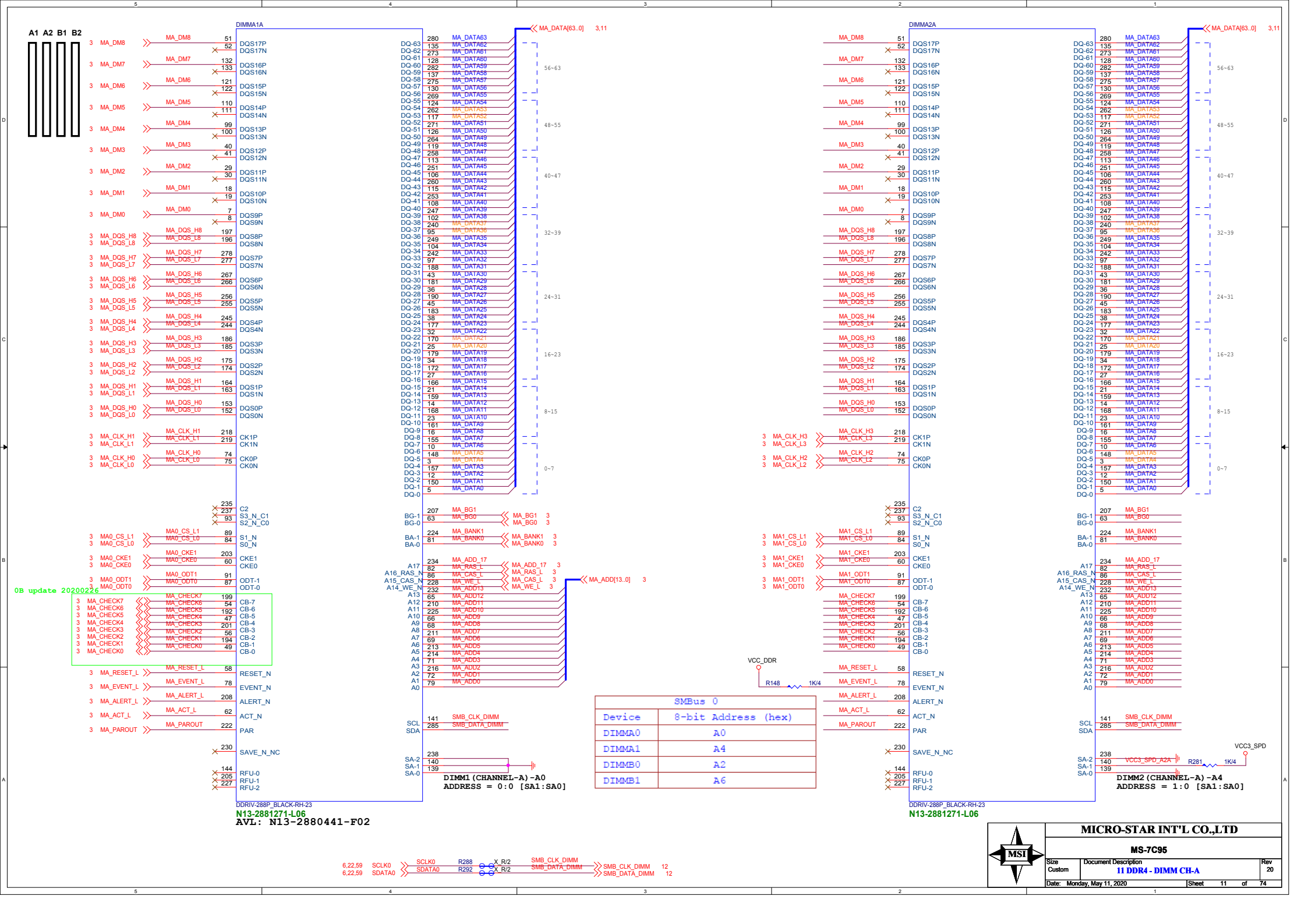


MICRO-STAR INT'L CO.,LTD

MS-7C95

Size	Document Description	Rev
Custom	10 RTC / CMOS	20

Date: Monday, May 11, 2020 Sheet 10 of 74


A1 A2 B1 B2
DIMMA1A
DIMMA2A
MA_DATA[63..0] 3,11
MA_ADD[13..0] 3
0B update 20200226
VCC_DDR
R148 1K/4
SMBus 0
Device 8-bit Address (hex)
DIMMA0 A0
DIMMA1 A4
DIMMB0 A2
DIMMB1 A6
DIMM1 (CHANNEL-A)-A0
ADDRESS = 0:0 [SA1:SA0]
DIMM2 (CHANNEL-A)-A4
ADDRESS = 1:0 [SA1:SA0]
VCC3_SPD
R281 1K/4
DDRIV-288P_BLACK-RH-23
N13-2881271-L06
AVL: N13-2880441-F02
MICRO-STAR INT'L CO.,LTD
MS-7C95
Size Custom
Document Description 11 DDR4 - DIMM CH-A
Rev 20
Date: Monday, May 11, 2020
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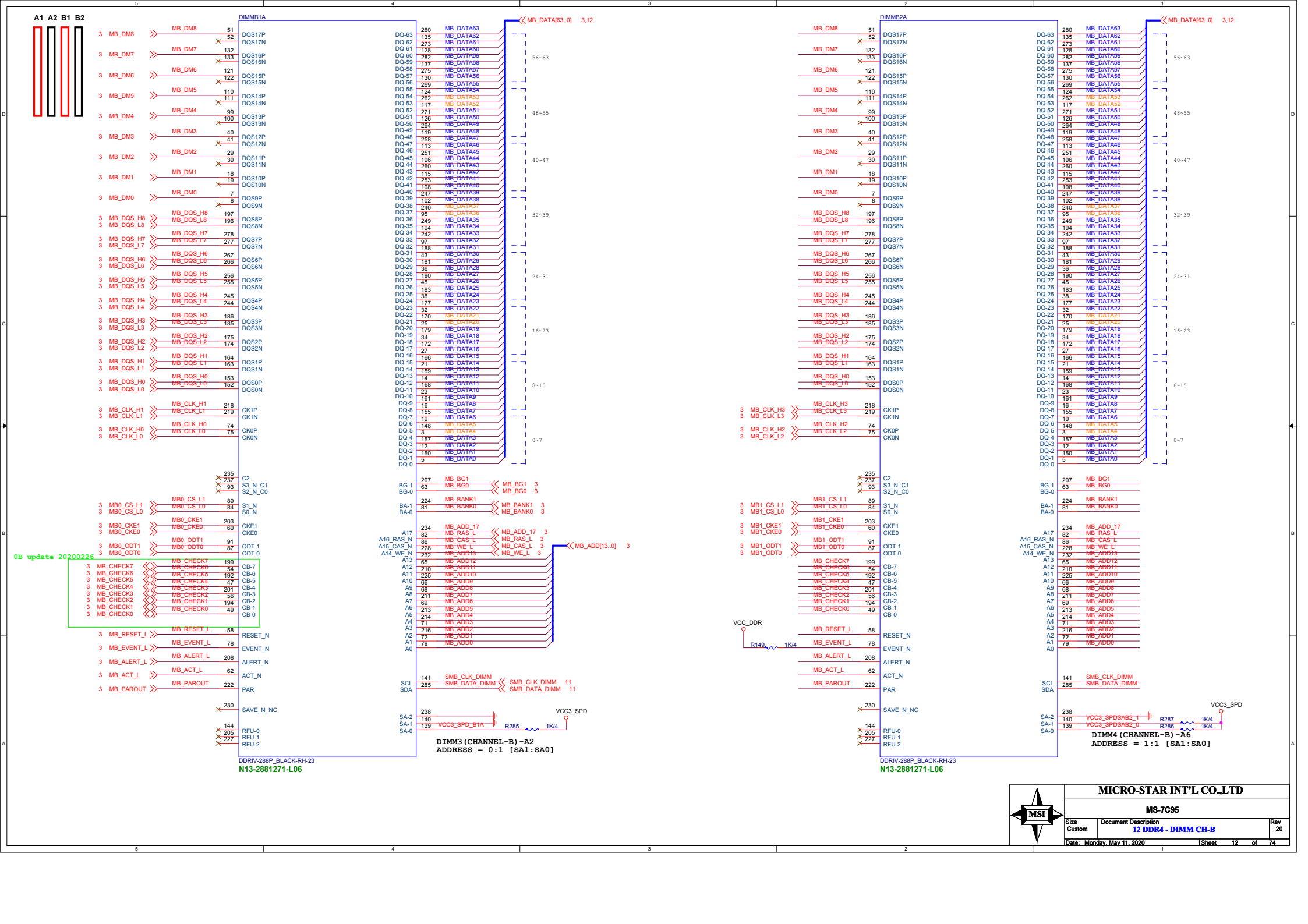
A1 A2 B1 B2
DIMMB1A
DIMMB2A
MB_DATA[63..0] 3,12
MB_ADD[13..0] 3
0B update 20200226
VCC_DDR
R149 1K/4
VCC3_SPD
R285 1K/4
R287 1K/4
R286 1K/4
DIMM3(CHANNEL-B)-A2
ADDRESS = 0:1 [SA1:SA0]
DIMM4(CHANNEL-B)-A6
ADDRESS = 1:1 [SA1:SA0]
DDRIV-288P_BLACK-RH-23
N13-2881271-L06
MICRO-STAR INT'L CO.,LTD
MS-7C95
Size Custom
Document Description 12 DDR4 - DIMM CH-B
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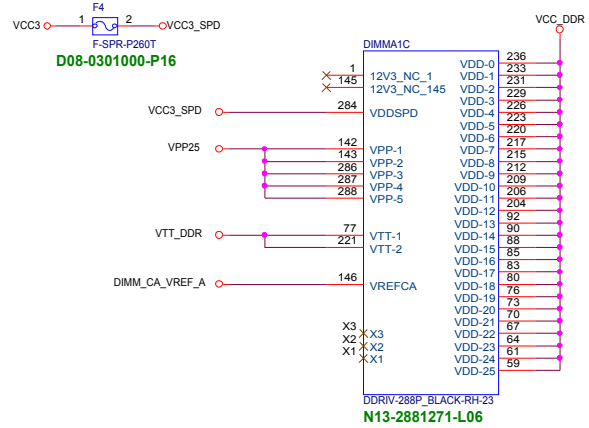
avl:D08-0301100-B07

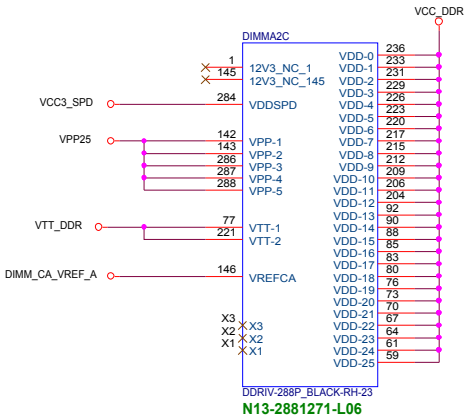
F4
VCC3 1 2 VCC3_SPD
F-SPR-P260T

D08-0301000-P16

DIMM SLOT PN BY SPEC



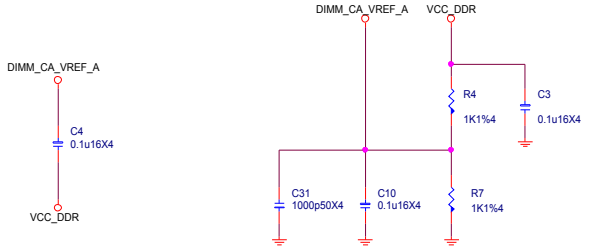
N13-2881271-L06

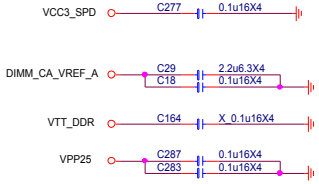


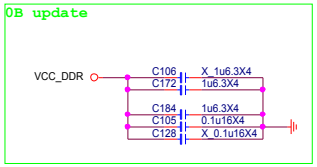
N13-2881271-L06

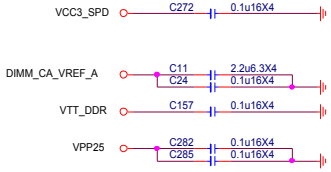
DDR VREF

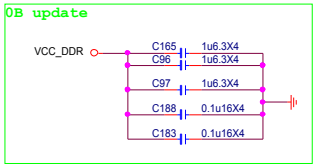
(place resistors close to DIMMs)

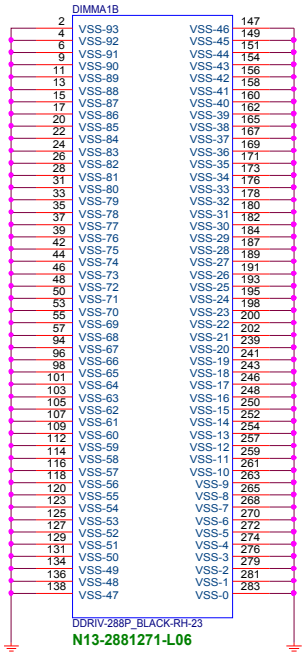




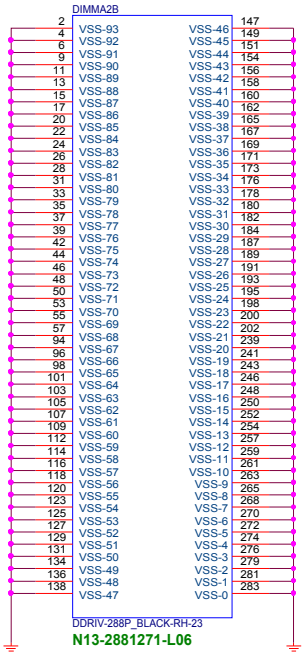








N13-2881271-L06



N13-2881271-L06

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	13 DDR4 - POWER/GND-1	20

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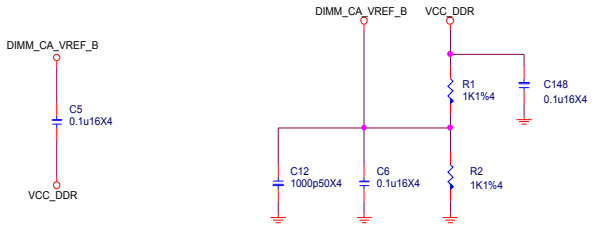
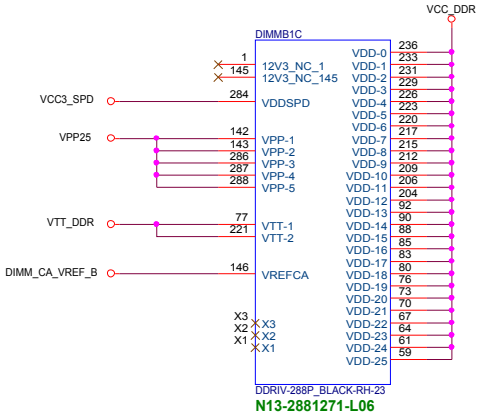
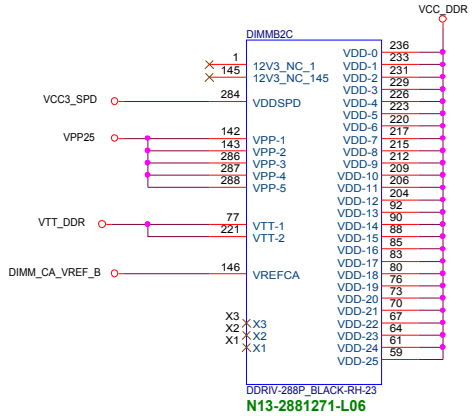
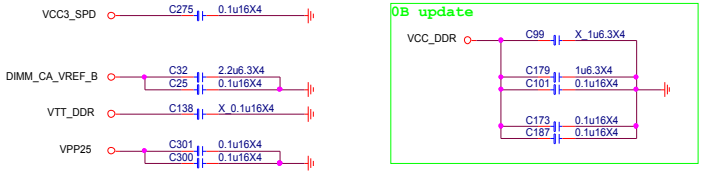
DDR VREF

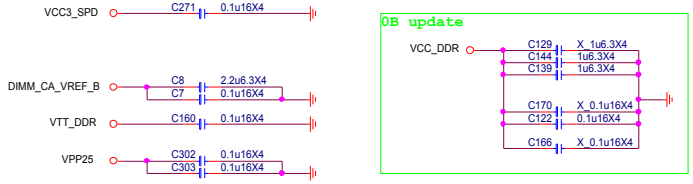
(place resistors close to DIMMs)

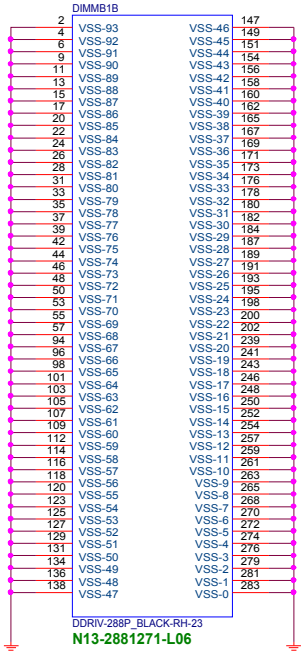


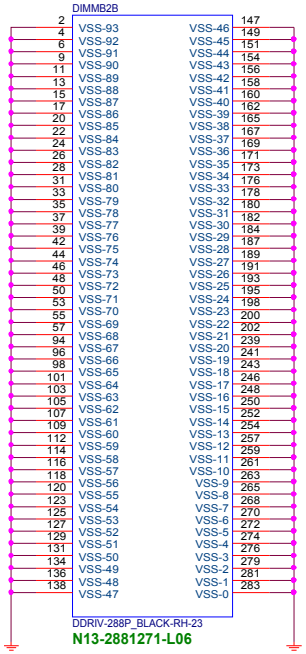












MICRO-STAR INT'L CO.,LTD

MS-7C95

Size	Document Description	Rev
Custom	14 DDR4 - POWER/GND-2	20

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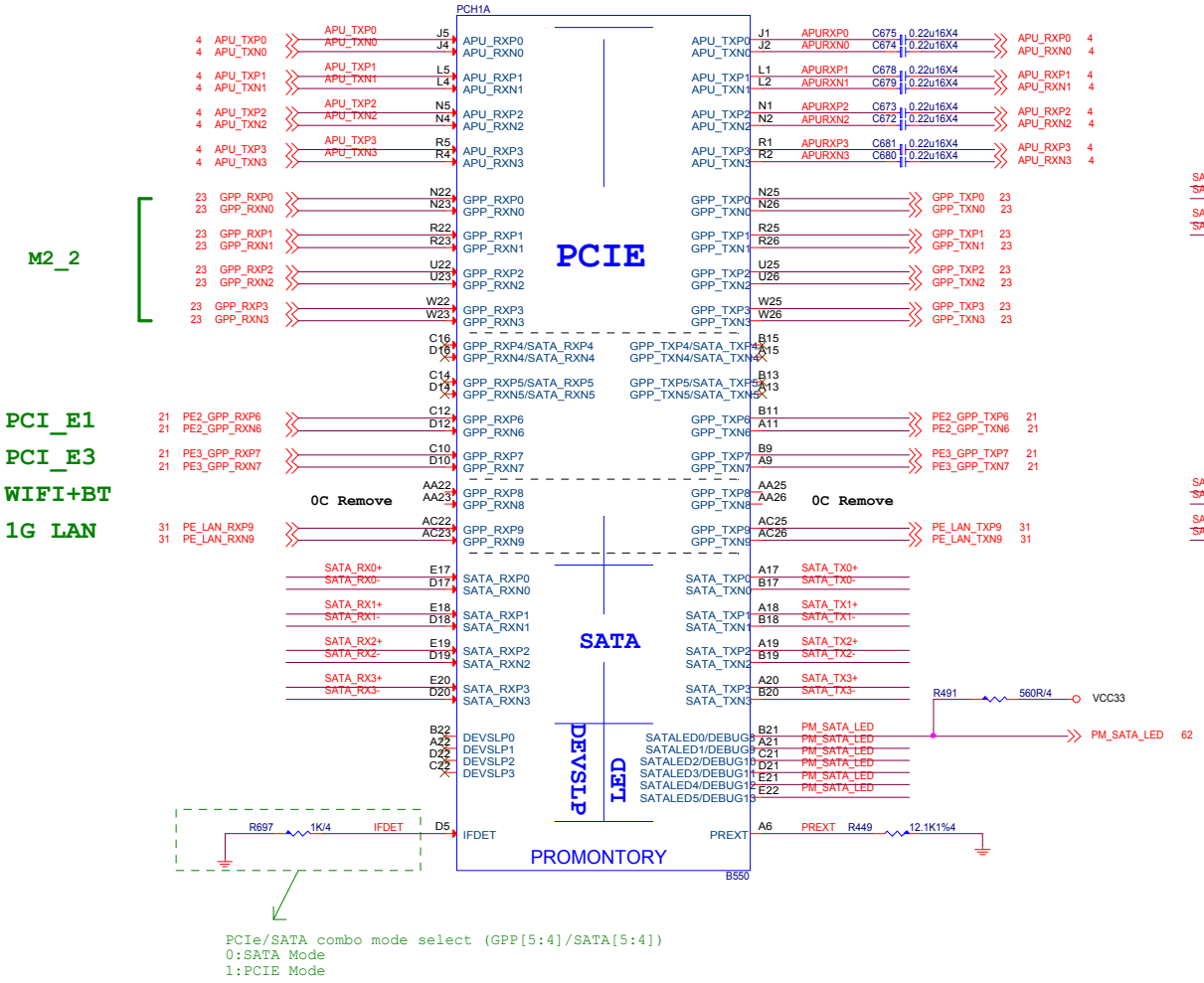
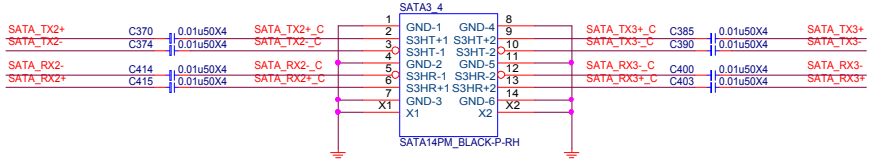


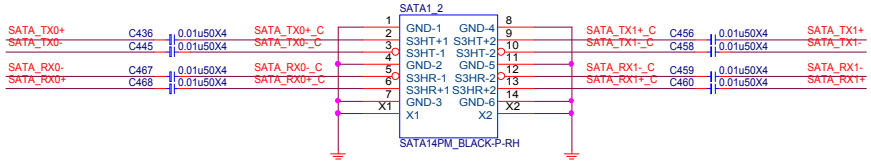
SATA Connector

SATA3_4



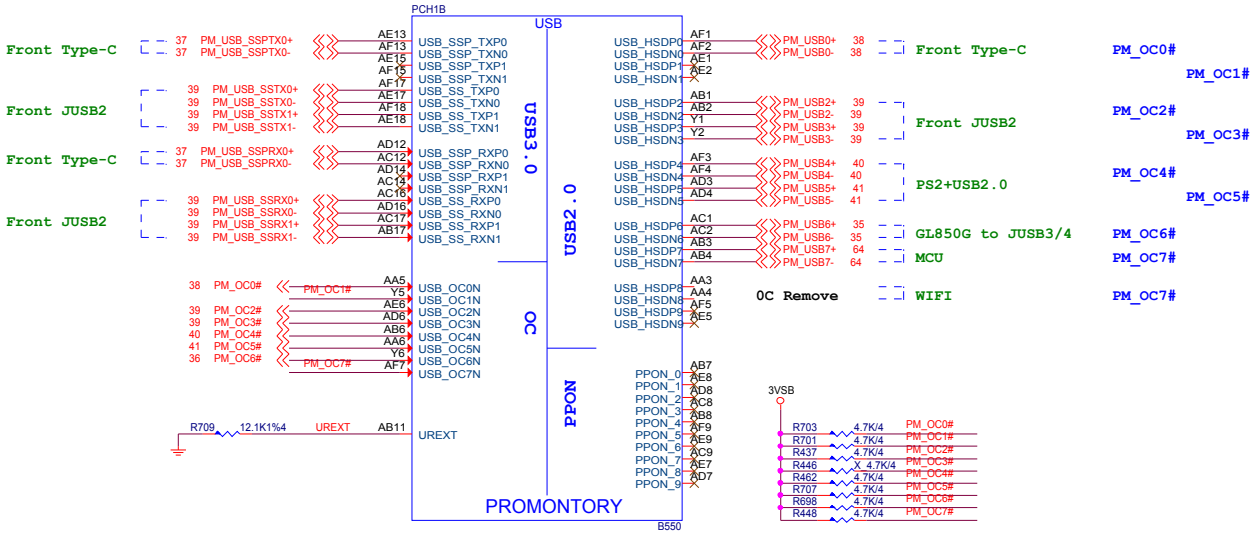
AVL:N5N-14M0201-L06

SATA1_2



AVL:N5N-14M0201-L06

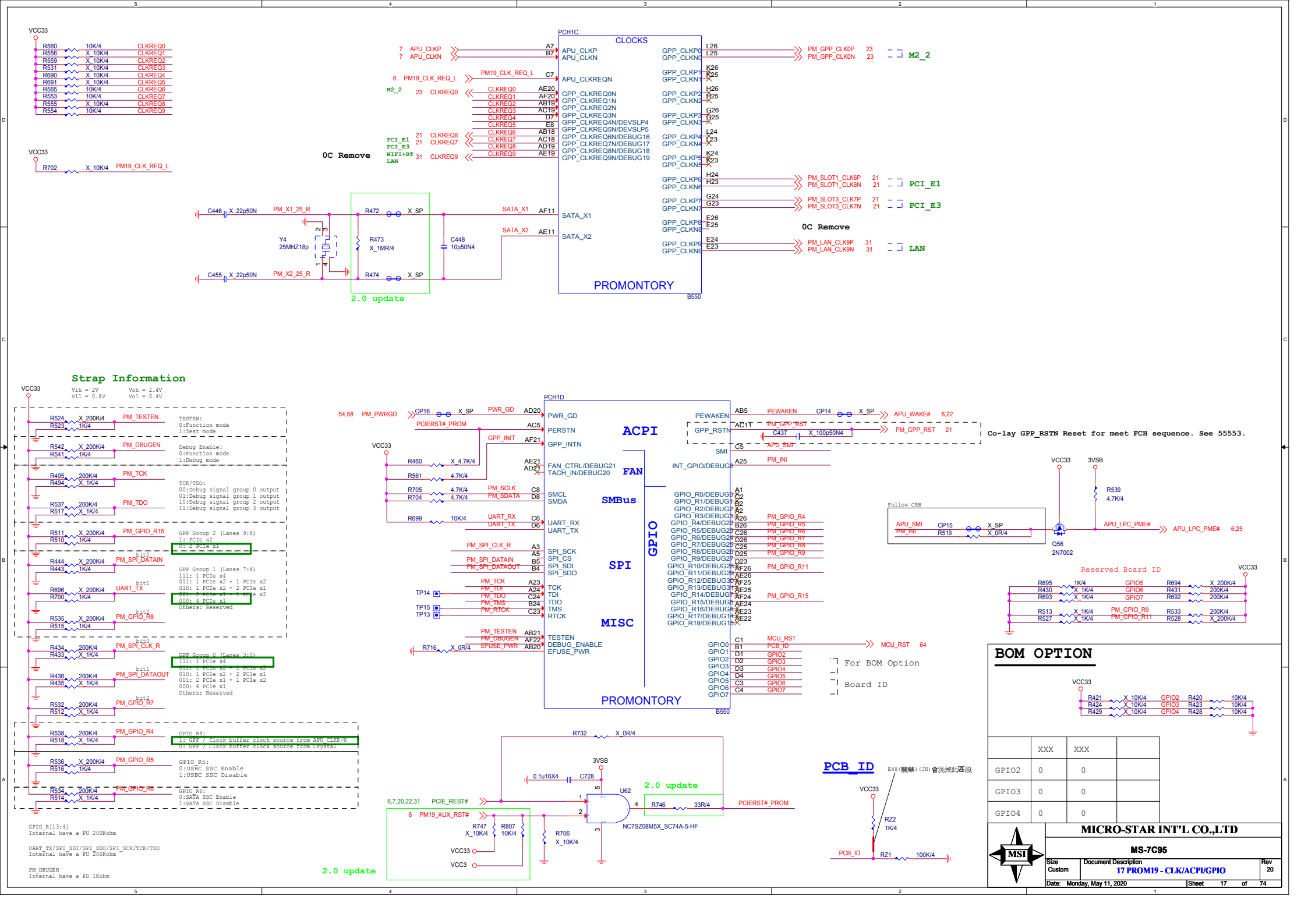
MICRO-STAR INT'L CO.,LTD		
MS-7C95		
Size: Custom	Document Description: 15 PROM19 - PCIE/SATA	Rev: 20
Date: Monday, May 11, 2020	Sheet 15 of 74	

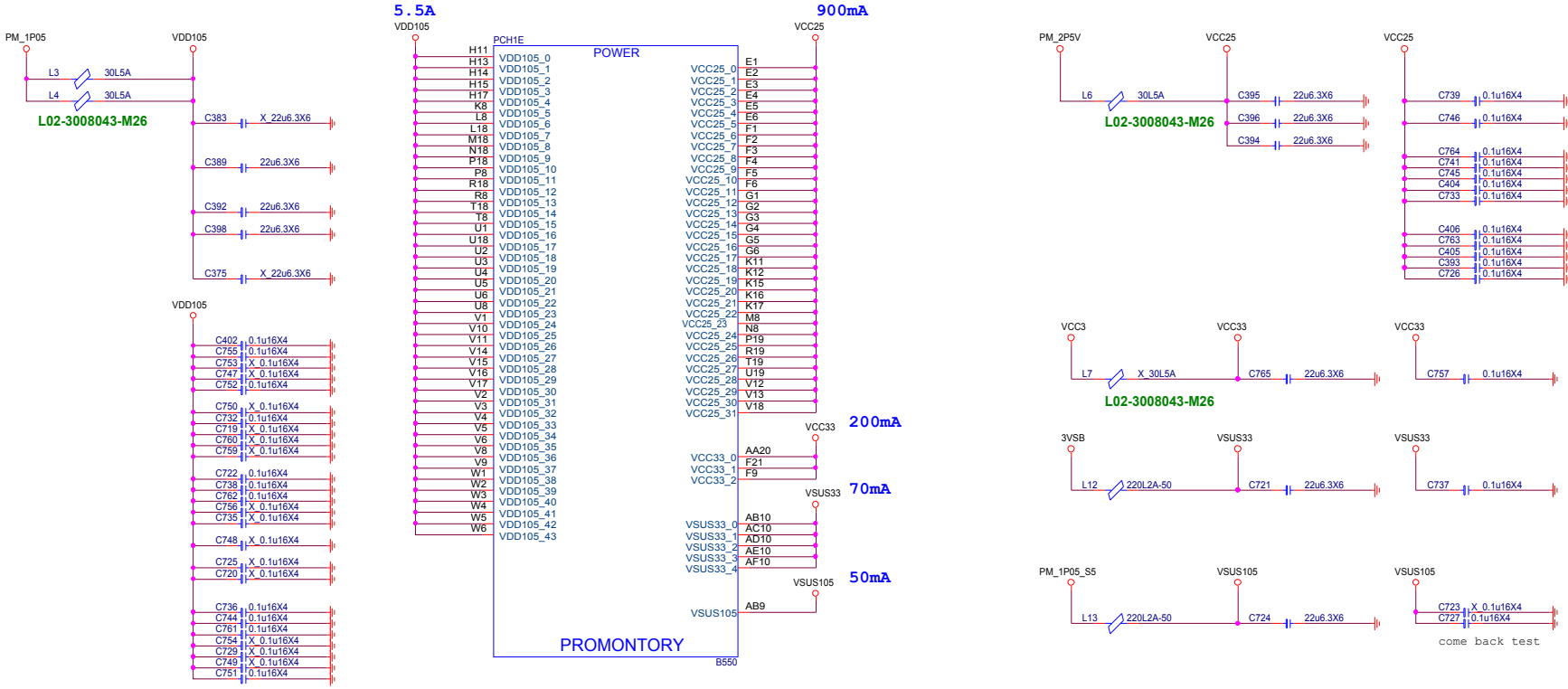


USB mapping

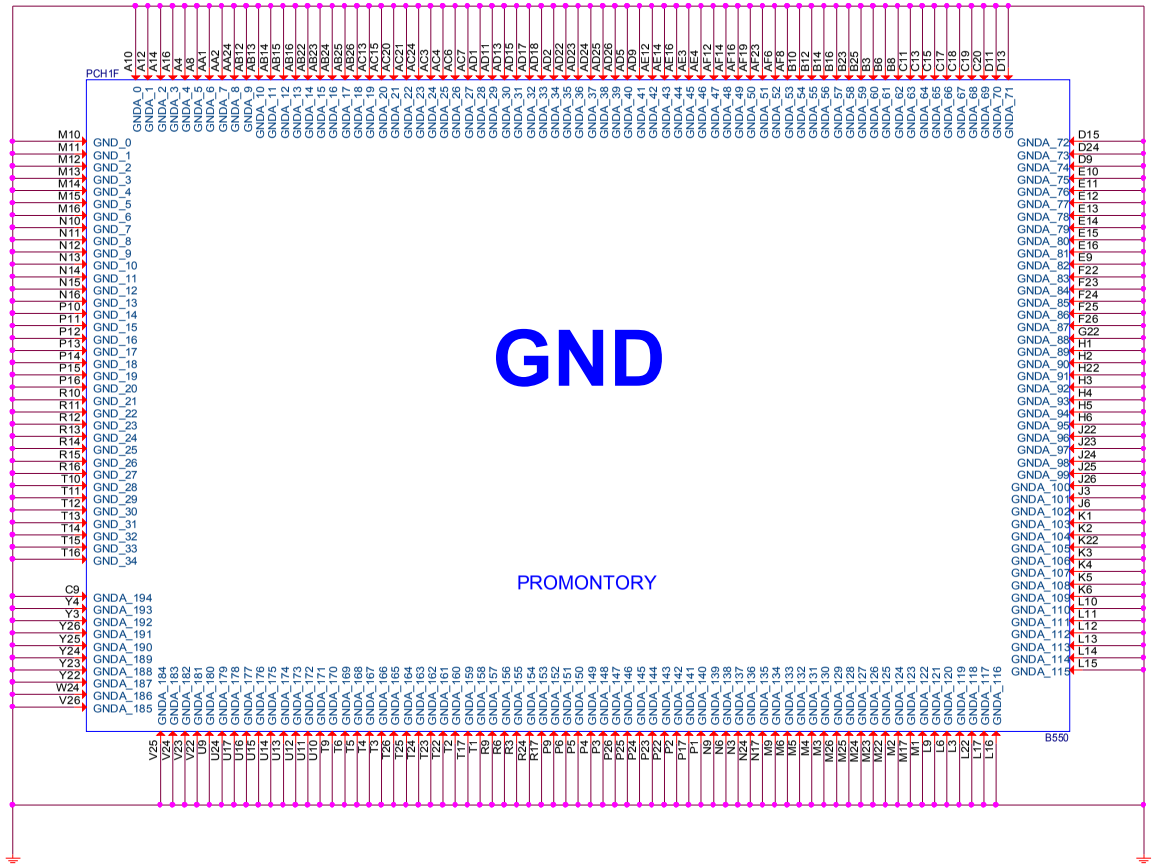
```
USB_SSP_TX/RX[0] + USB_HSDP/N[0] + USB_OC0N
USB_SSP_TX/RX[1] + USB_HSDP/N[1] + USB_OC1N

USB_SS_TX/RX[0] + USB_HSDP/N[2] + USB_OC2N
USB_SS_TX/RX[1] + USB_HSDP/N[3] + USB_OC3N
                  USB_HSDP/N[4] + USB_OC4N
                  USB_HSDP/N[5] + USB_OC5N
                  USB_HSDP/N[6] + USB_OC6N
                  USB_HSDP/N[7] + USB_OC7N
                  USB_HSDP/N[8] + USB_OC7N
                  USB_HSDP/N[9] + USB_OC7N
```

MICRO-STAR INT'L CO.,LTD	
MS-7C95	
Size: Custom	Document Description: 16 PROM19 - USB/OC
Rev: 20	
Date: Monday, May 11, 2020	Sheet 16 of 74


VCC33
R560 10K/4 CLKREQ0
R556 X_10K/4 CLKREQ1
R559 X_10K/4 CLKREQ2
R531 X_10K/4 CLKREQ3
R690 X_10K/4 CLKREQ4
R691 X_10K/4 CLKREQ5
R565 10K/4 CLKREQ6
R553 10K/4 CLKREQ7
R555 X_10K/4 CLKREQ8
R554 10K/4 CLKREQ9
R702 X_10K/4 PM19_CLK_REQ_L
0C Remove
PCH1C
CLOCKS
APU_CLKP
APU_CLKN
APU_CLKREQN
GPP_CLKREQ0N
GPP_CLKREQ1N
GPP_CLKREQ2N
GPP_CLKREQ3N
GPP_CLKREQ4N/DEVSLP4
GPP_CLKREQ5N/DEVSLP5
GPP_CLKREQ6N/DEBUG16
GPP_CLKREQ7N/DEBUG17
GPP_CLKREQ8N/DEBUG18
GPP_CLKREQ9N/DEBUG19
GPP_CLKP0
GPP_CLKN0
GPP_CLKP1
GPP_CLKN1
GPP_CLKP2
GPP_CLKN2
GPP_CLKP3
GPP_CLKN3
GPP_CLKP4
GPP_CLKN4
GPP_CLKP5
GPP_CLKN5
GPP_CLKP6
GPP_CLKN6
GPP_CLKP7
GPP_CLKN7
GPP_CLKP8
GPP_CLKN8
GPP_CLKP9
GPP_CLKN9
PM_GPP_CLK0P
PM_GPP_CLK0N
M2_2
PM_SLOT1_CLK6P
PM_SLOT1_CLK6N
PCI_E1
PM_SLOT3_CLK7P
PM_SLOT3_CLK7N
PCI_E3
0C Remove
PM_LAN_CLK9P
PM_LAN_CLK9N
LAN
C446 X_22p50N PM_X1_25_R
C455 X_22p50N PM_X2_25_R
Y4 25MHZ18p
R472 X_SP
R473 X_1MR/4
R474 X_SP
C448 10p50N4
SATA_X1
SATA_X2
2.0 update
PROMONTORY
B550
Strap Information
Vih = 2V Voh = 2.4V
Vil = 0.8V Vol = 0.4V
PM_TESTEN
TESTEN:
0:Function mode
1:Test mode
PM_DBUGEN
Debug Enable:
0:Function mode
1:Debug mode
PM_TCK
PM_TDO
TCK/TDO:
00:Debug signal group 0 output
01:Debug signal group 1 output
10:Debug signal group 2 output
11:Debug signal group 3 output
PM_GPIO_R15
GPP Group 2 (Lanes 9:8)
1: PCIe x2
0: 2 PCIe x1
PM_SPI_DATAIN
UART_TX
PM_GPIO_R8
GPP Group 1 (Lanes 7:4)
111: 1 PCIe x4
011: 1 PCIe x2 + 1 PCIe x2
010: 1 PCIe x2 + 2 PCIe x1
001: 2 PCIe x1 + 1 PCIe x2
000: 4 PCIe x1
Others: Reserved
PM_SPI_CLK_R
PM_SPI_DATAOUT
PM_GPIO_R7
GPP Group 0 (Lanes 3:0)
111: 1 PCIe x4
010: 1 PCIe x2 + 2 PCIe x1
001: 2 PCIe x1 + 1 PCIe x2
000: 4 PCIe x1
Others: Reserved
PM_GPIO_R4
GPIO_R4:
1: GPP_7 Clock buffer clock source from APU CLKP/N
0: GPP_7 Clock buffer clock source from Crystal
PM_GPIO_R5
GPIO_R5:
0:USBC SSC Enable
1:USBC SSC Disable
PM_GPIO_R6
GPIO_R6:
0:SATA SSC Enable
1:SATA SSC Disable
GPIO_R[13:4]
Internal have a PU 200Kohm
UART_TX/SPI_SDI/SPI_SDO/SPI_SCK/TCK/TDO
Internal have a PD 200Kohm
PM_DBUGEN
Internal have a PD 1Kohm
PCH1D
ACPI
FAN
SMBus
SPI
GPIO
MISC
PWR_GD
PERSTN
GPP_INTN
FAN_CTRL/DEBUG21
TACH_IN/DEBUG20
SMCL
SMDA
UART_RX
UART_TX
SPI_SCK
SPI_CS
SPI_SDI
SPI_SDO
TCK
TDI
TDO
TMS
RTCK
TESTEN
DEBUG_ENABLE
EFUSE_PWR
PEWAKEN
GPP_RSTN
SMI
INT_GPIO/DEBUG6
PROMONTORY
B550
PM_PWRGD
PCIERST#_PROM
GPP_INIT
PM_SCLK
PM_SDATA
PM_SPI_DATAOUT
PM_TDI
PM_TMS
PM_RTCK
PM_DBUGEN
EFUSE_PWR
APU_WAKE#
PM_GPP_RST
Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.
APU_SMI
PM_INI
Follow CRB
Q56 2N7002
APU_LPC_PME#
Reserved Board ID
MCU_RST
PCB_ID
For BOM Option
Board ID
BOM OPTION
R732 X_0R/4
3VSB
0.1u16X4 C728
U62
NC7SZ08M5X_SC74A-5-HF
R746 33R/4
R747 X_10K/4
R807 10K/4
R706 X_10K/4
2.0 update
PCB_ID
RZ2 1K/4
RZ1 100K/4
E48(變華)(JH)會洗掉此區段
XXX
GPIO2 0 0
GPIO3 0 0
GPIO4 0 0
MICRO-STAR INT'L CO.,LTD
MS-7C95
Size Custom
Document Description
17 PROM19 - CLK/ACPI/GPIO
Rev 20
Date: Monday, May 11, 2020
Sheet 17 of 74



MICRO-STAR INT'L CO.,LTD		
MS-7C95		
Size: Custom	Document Description: 18 PROM19 - Power	Rev: 20
Date: Monday, May 11, 2020	Sheet 18 of 74	



MICRO-STAR INT'L CO.,LTD	
MS-7C95	
Size: Custom	Document Description: 19 PROM19 - GND
Rev: 20	
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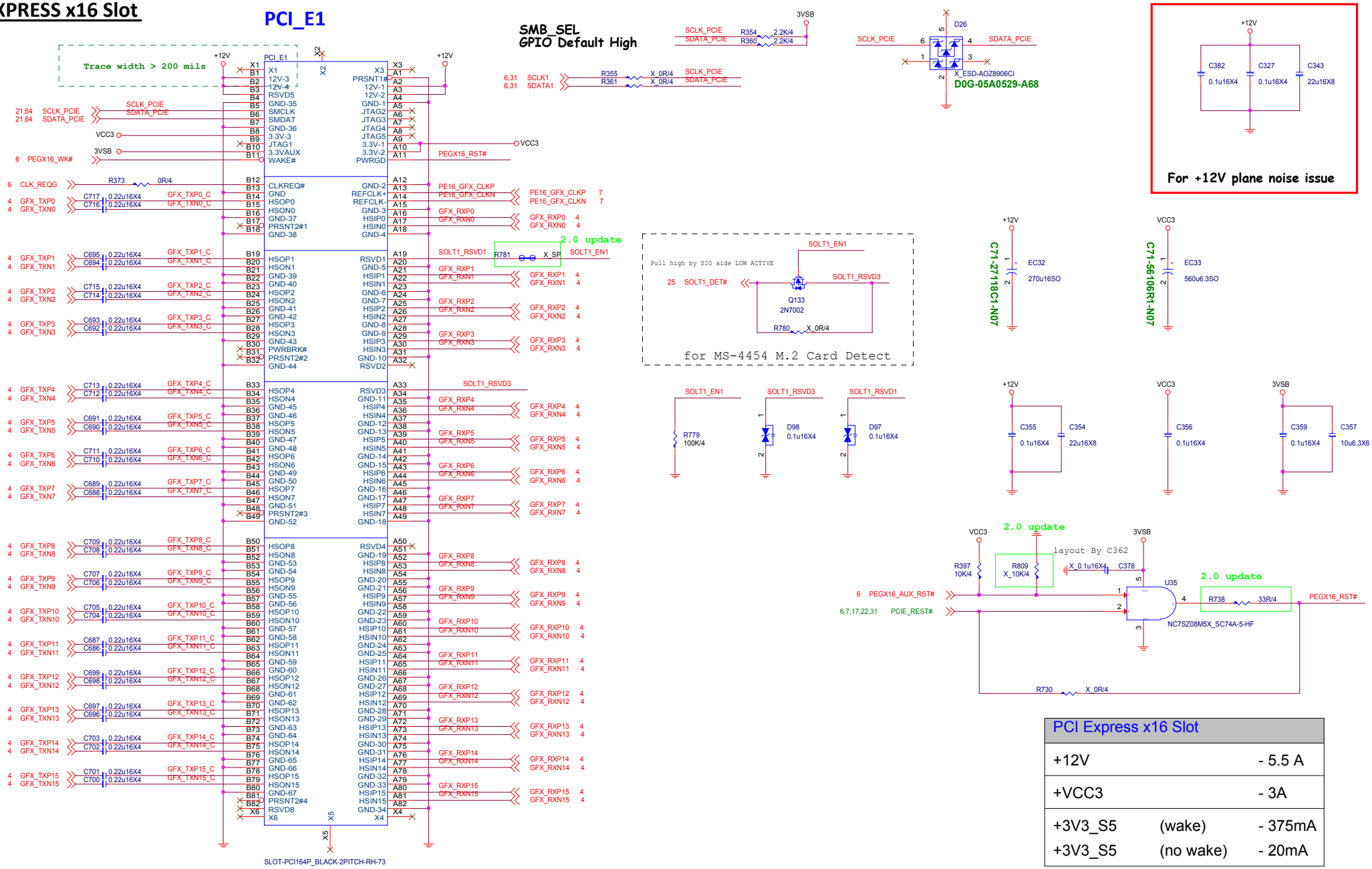
PCI EXPRESS x16 Slot



PCI Express x16 Slot		
+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

MICRO-STAR INT'L CO.,LTD

MS-7C95

Size	Document Description	Rev
Custom	20 PCI_E1 (X16)	20

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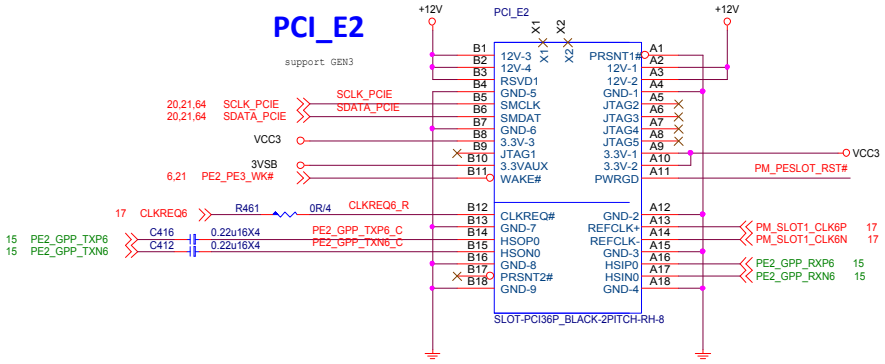
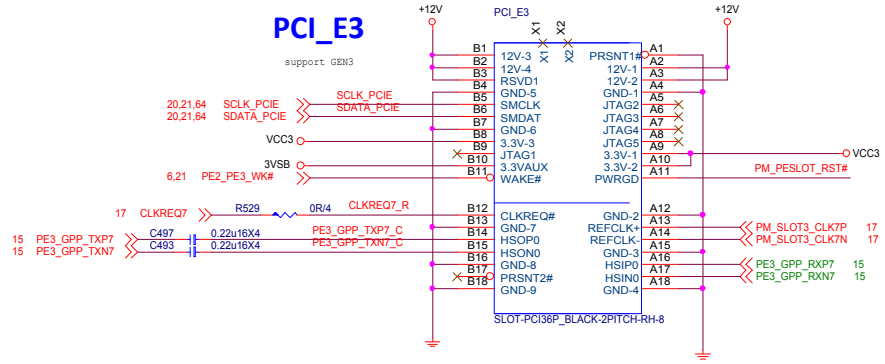
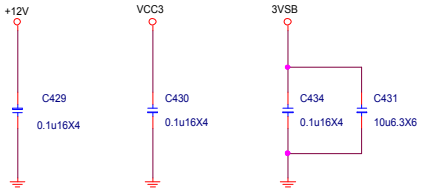
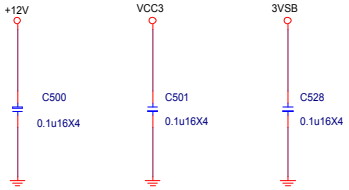
PCI EXPRESS X1 SLOT





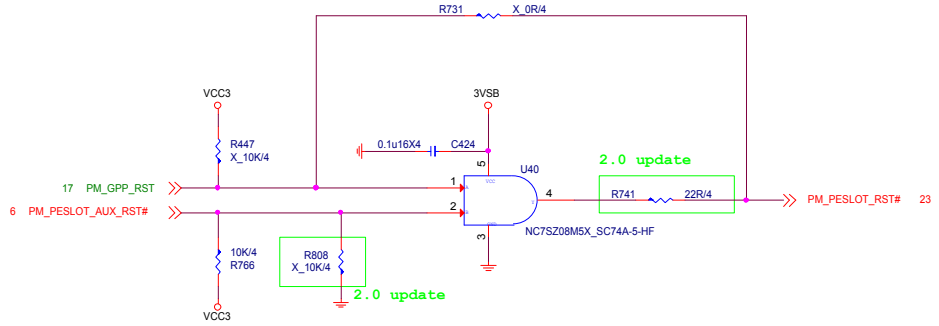




12V - 0.5A

VCC3 - 3A

3VSBV - 375mA



PCI Express x1 Slot *3		
+12V		- 1.5 A
+VCC3		- 9A
+3V3_S5	(wake)	- 1125mA
+3V3_S5	(no wake)	- 20mA

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C95	
Size: Custom	Document Description: 21 PCI_E2 (X1) / PCI_E3 (X1)	Rev: 20
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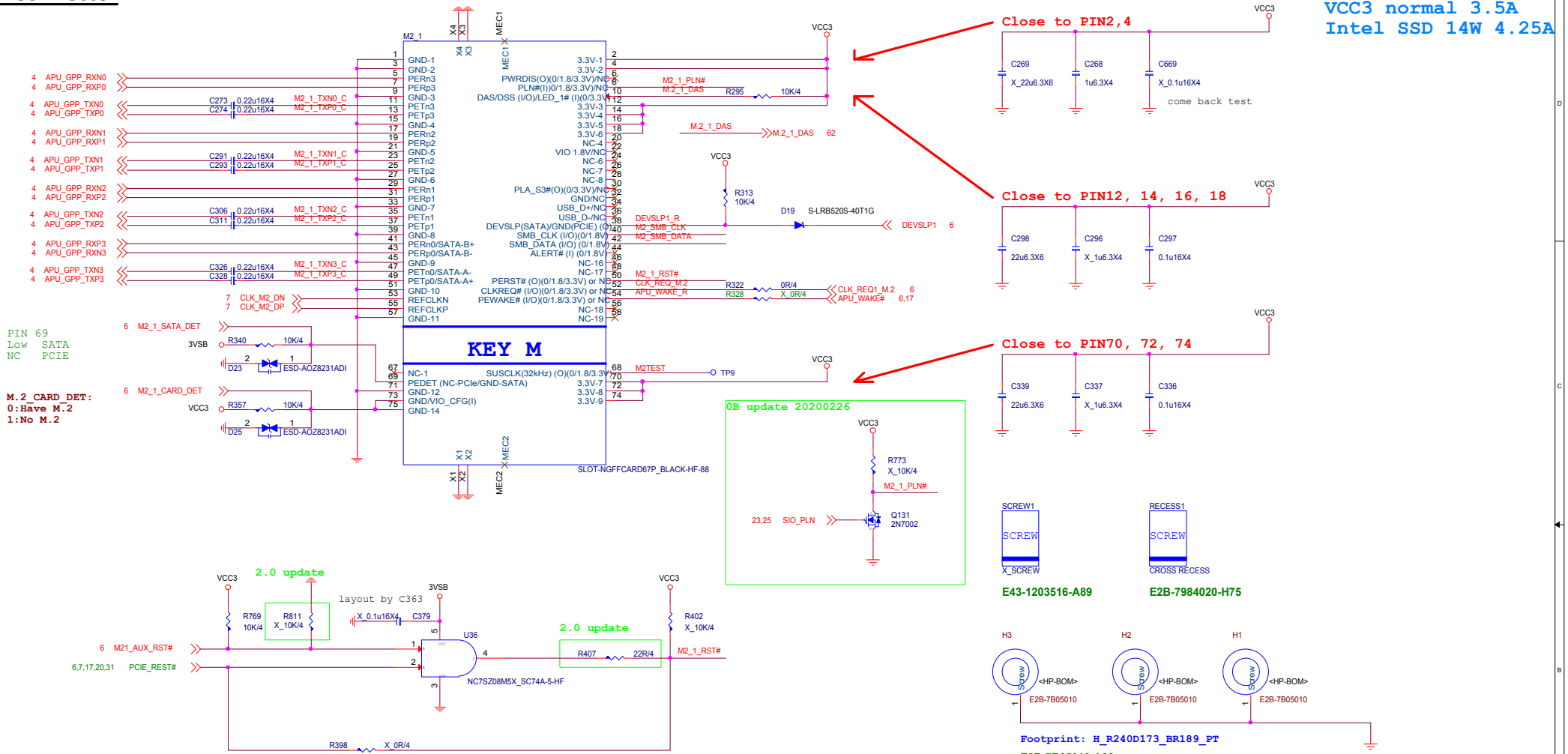
M.2_1 Connector

M2下方零件擺放限　要小於0.9mm的零件

VCC3 peak 7A
VCC3 normal 3.5A
Intel SSD 14W 4.25A

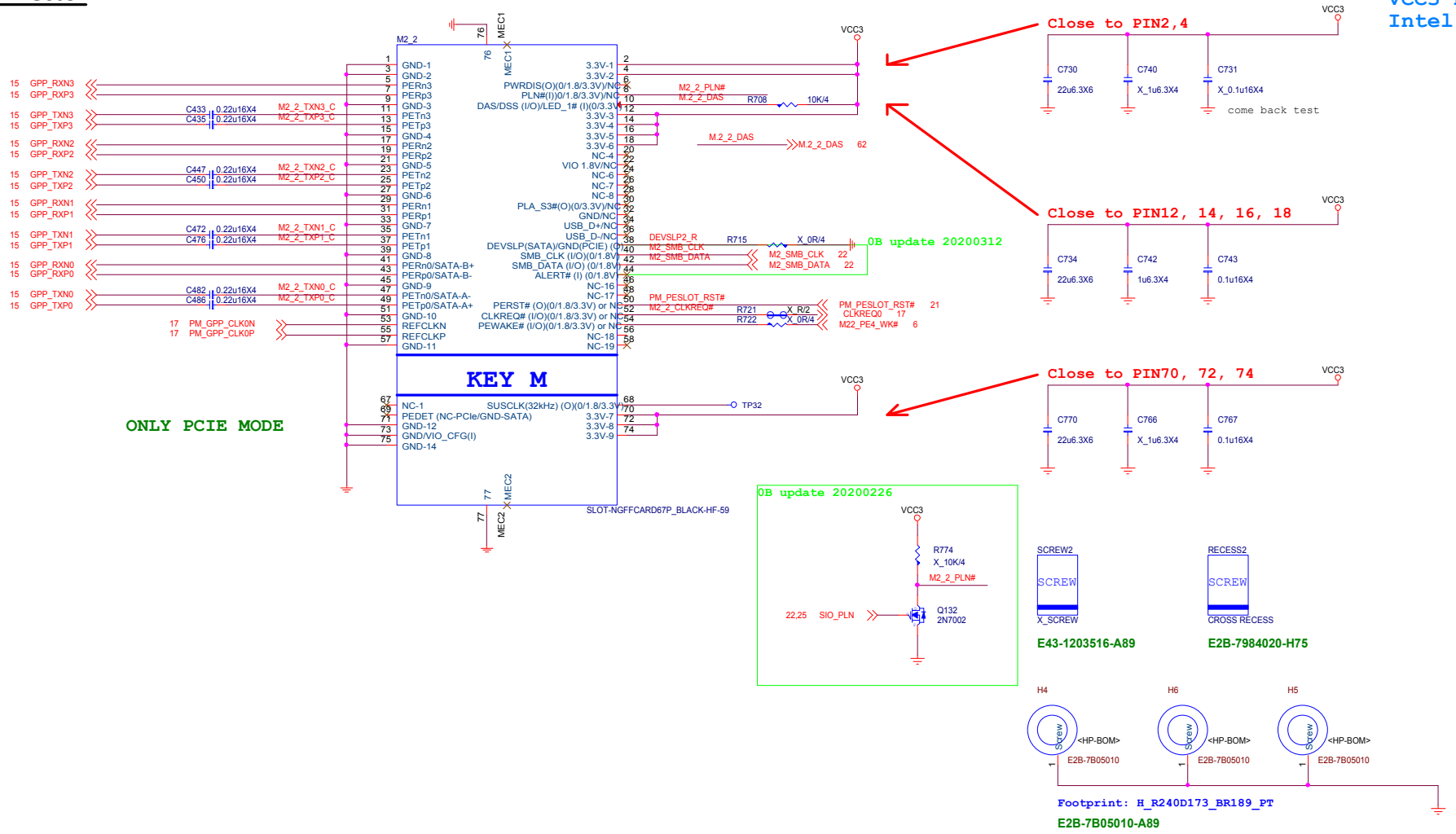


MICRO-STAR INT'L CO.,LTD	
MS-7C95	
Size: Custom	Document Description: 22 M2_1 PCIE / SATA
Date: Monday, May 11, 2020	Sheet 22 of 74
	Rev: 20

M.2_2 Connector

M2下方零件擺放限　要小於0.9mm的零件

VCC3 peak 7A
VCC3 normal 3.5A
Intel SSD 14W 4.25A



MICRO-STAR INT'L CO.,LTD			
MS-7C95			
Size: Custom	Document Description: 23 M2_2 PCIE		Rev: 20
Date: Monday, May 11, 2020		Sheet 23 of 74	

0C Remove

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C95	
Size: Custom	Document Description: 24 M2_WIFI1 (KEY_E)	Rev: 20
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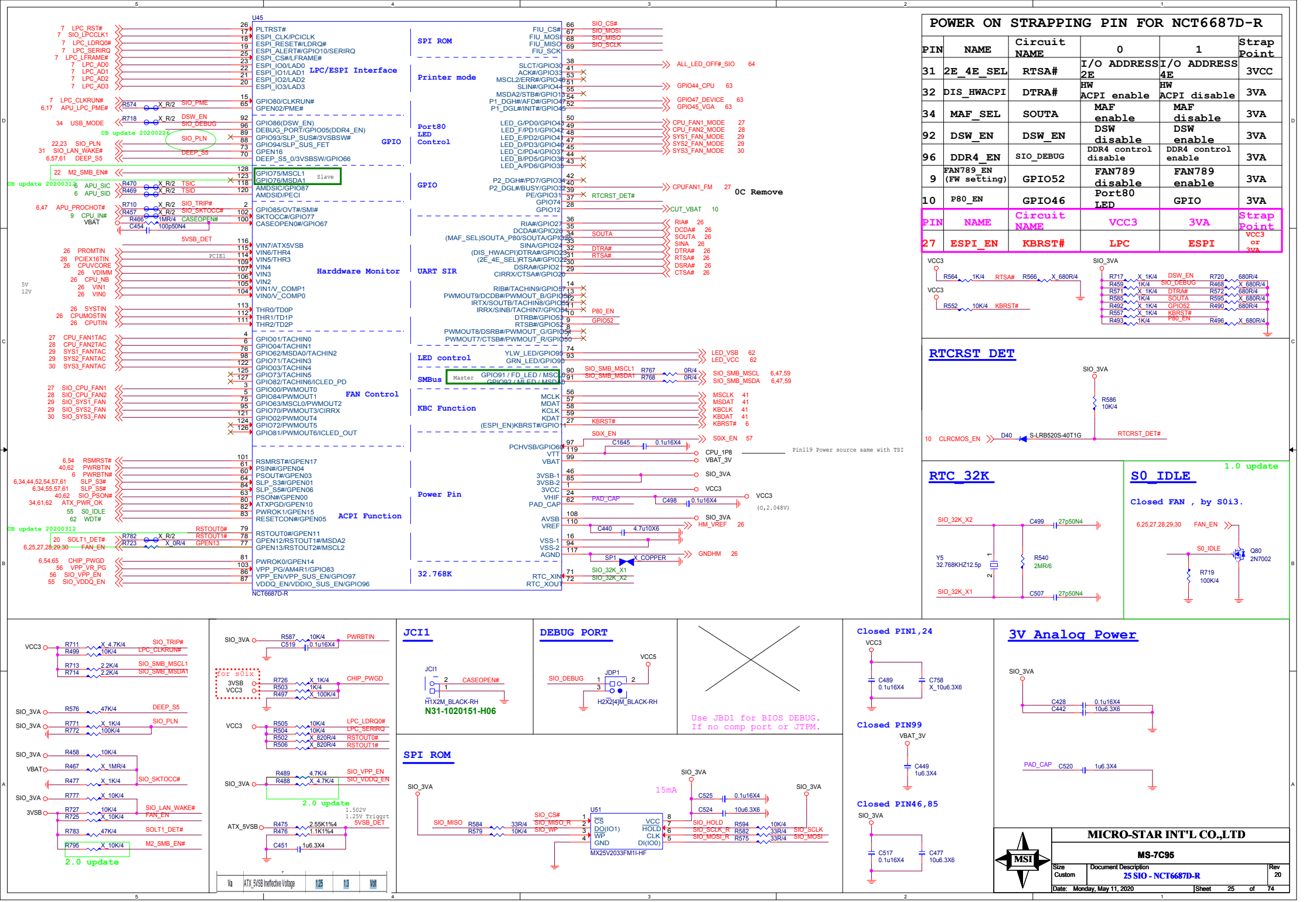

POWER ON STRAPPING PIN FOR NCT6687D-R

PIN	NAME	Circuit NAME	0	1	Strap Point
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	3VCC
32	DIS_HWACPI	DTRA#	HW ACPI enable	HW ACPI disable	3VA
34	MAF_SEL	SOUTA	MAF enable	MAF disable	3VA
92	DSW_EN	DSW_EN	DSW disable	DSW enable	3VA
96	DDR4_EN	SIO_DEBUG	DDR4 control disable	DDR4 control enable	3VA
9	FAN789_EN (FW setting)	GPIO52	FAN789 disable	FAN789 enable	3VA
10	P80_EN	GPIO46	Port80 LED	GPIO	3VA
PIN	NAME	Circuit NAME	VCC3	3VA	Strap Point
27	ESPI_EN	KBRST#	LPC	ESPI	VCC3 or 3VA

RTCRST_DET

RTC_32K

S0_IDLE

1.0 update

Closed FAN , by S0i3.

JCI1

N31-1020151-H06

DEBUG PORT

Use JBD1 for BIOS DEBUG.
If no comp port or JTPM.

SPI ROM

Closed PIN1,24

Closed PIN99

Closed PIN46,85

3V Analog Power

MICRO-STAR INT'L CO.,LTD	
MS-7C95	
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Rev: 20	
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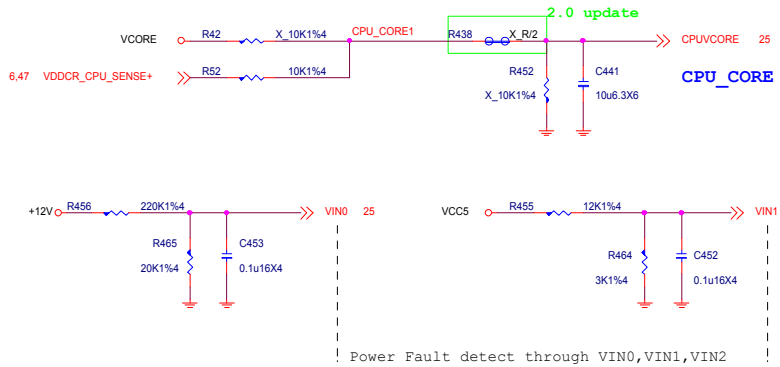
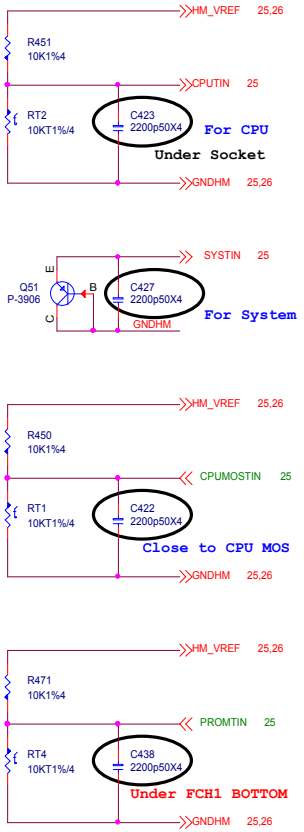
HW Monitor - Voltage

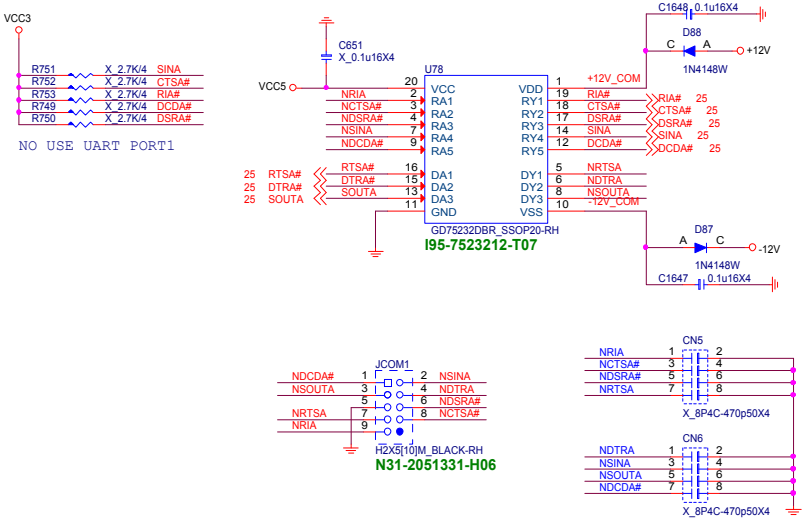
SIO HM Voltage over 2.048V will not detect



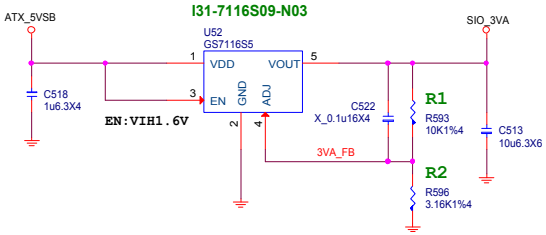
TEMP SENSOR



COM PORT



SIO_3VA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V

MSI	MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: 26 SIO - HW Monitor / RESET	Rev: 20
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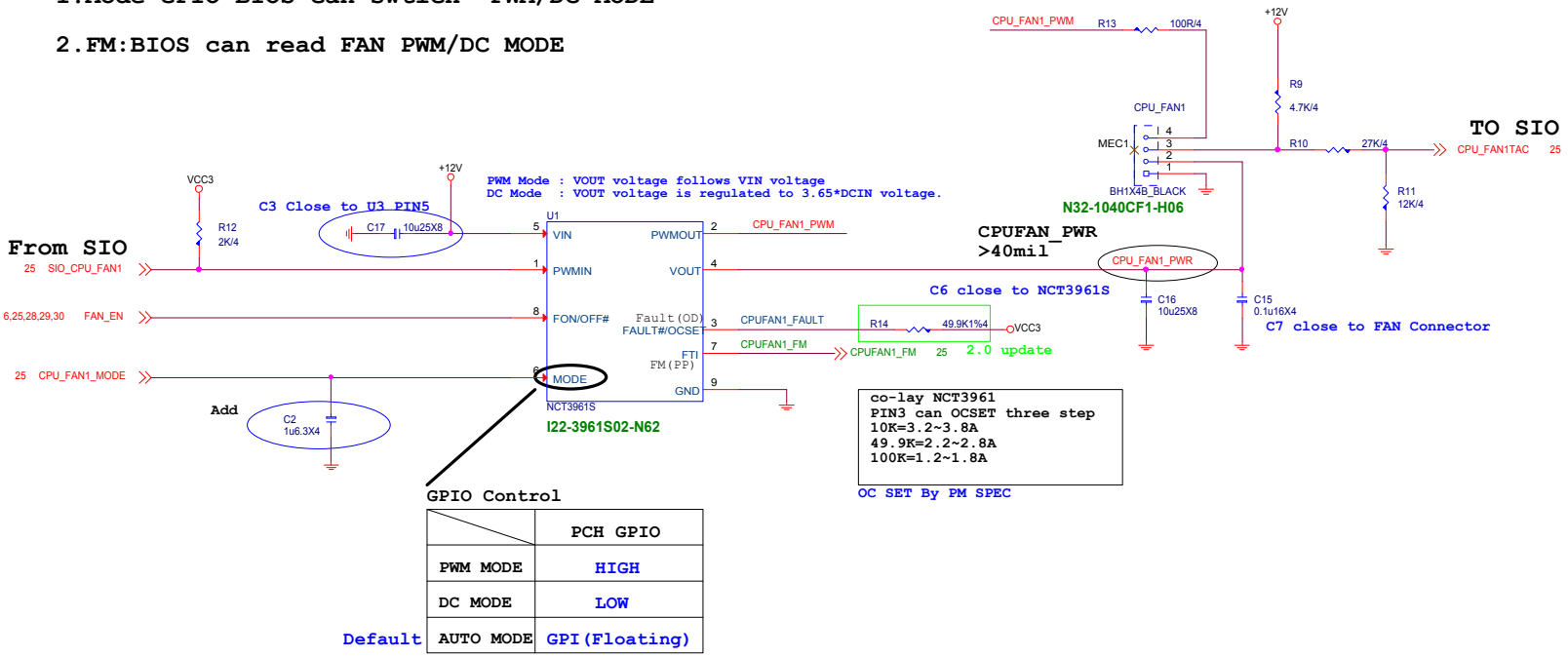
CPUFAN1 TYPE N : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

2.FM:BIOS can read FAN PWM/DC MODE



co-lay NCT3961
PIN3 can OCSET three step
10K=3.2~3.8A
49.9K=2.2~2.8A
100K=1.2~1.8A

OC SET By PM SPEC

GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD	
MS-7C95	
Size: Custom	Document Description: 27 FAN TYPE-N CPUFAN1
Rev: 20	
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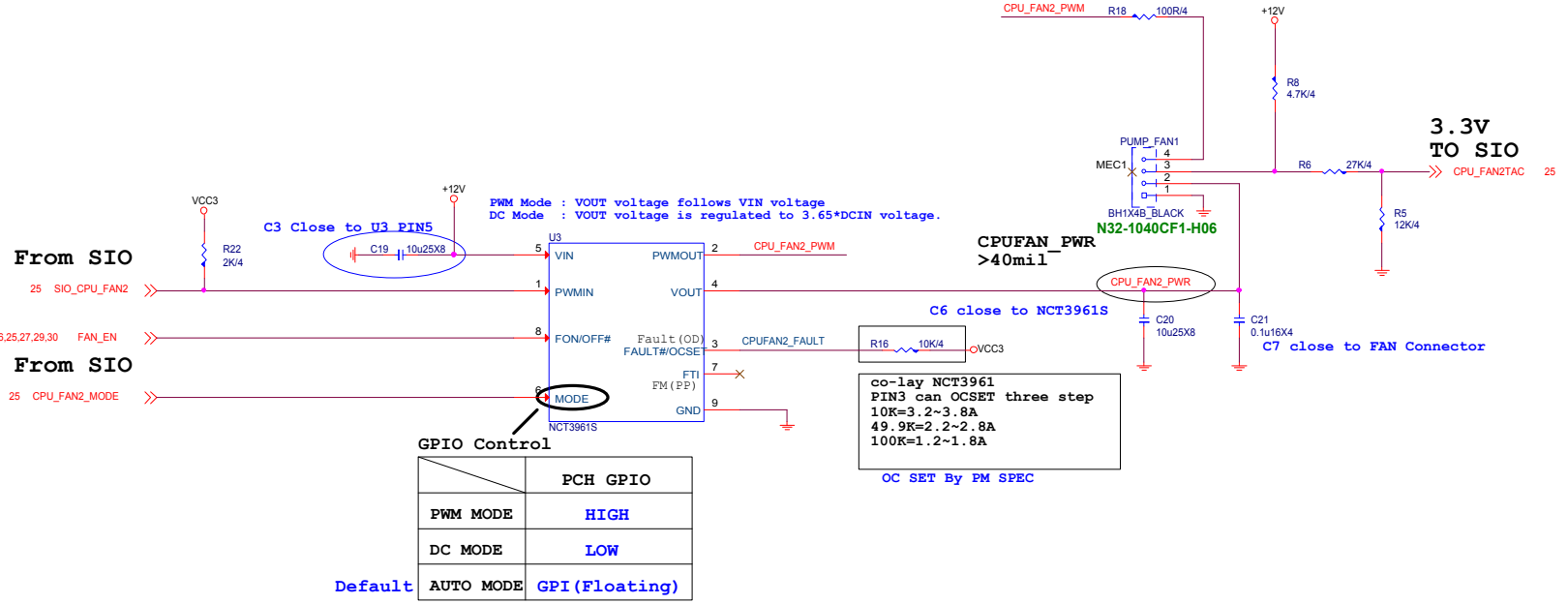
PUMPFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

MS-7C95

Size: Custom | Document Description: 28 FAN TYPE-M PUMPFAN1 | Rev: 20

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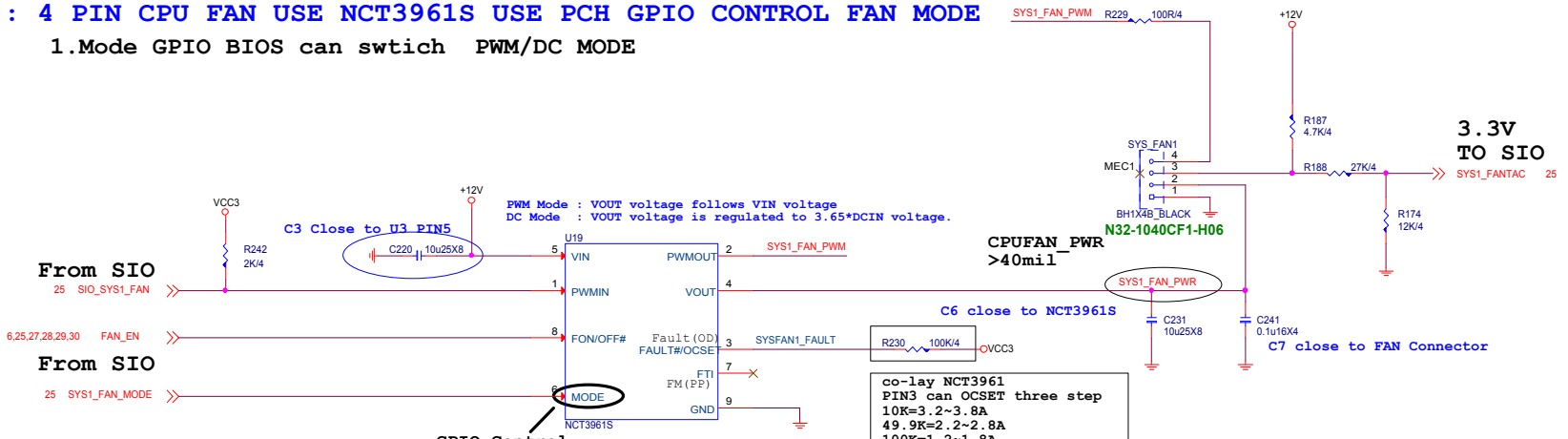
SYSFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

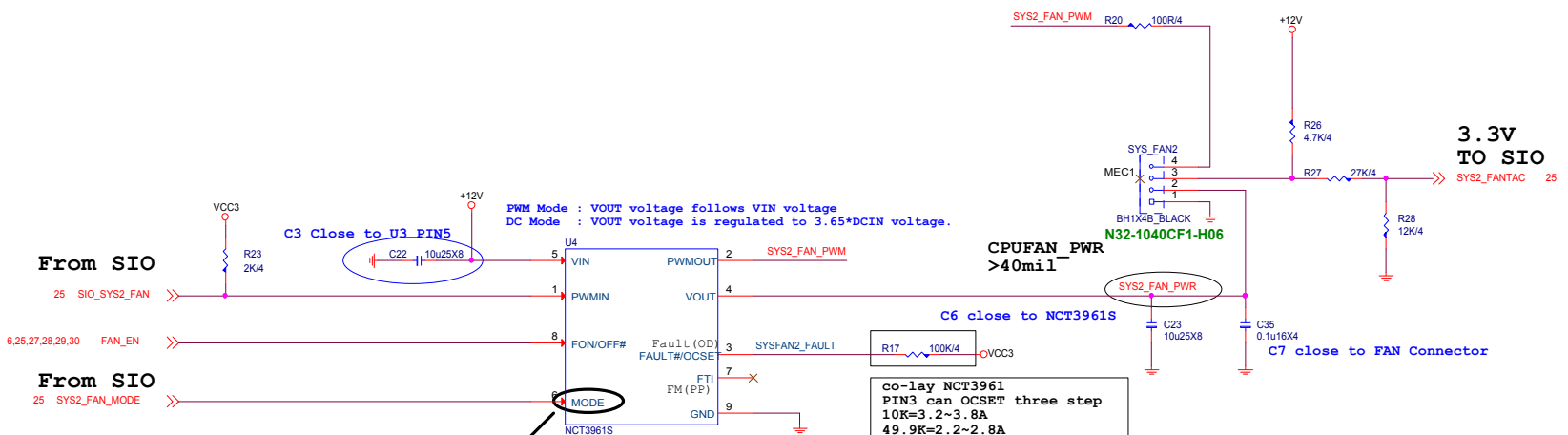


	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

SYSFAN2

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD	
MS-7C95	
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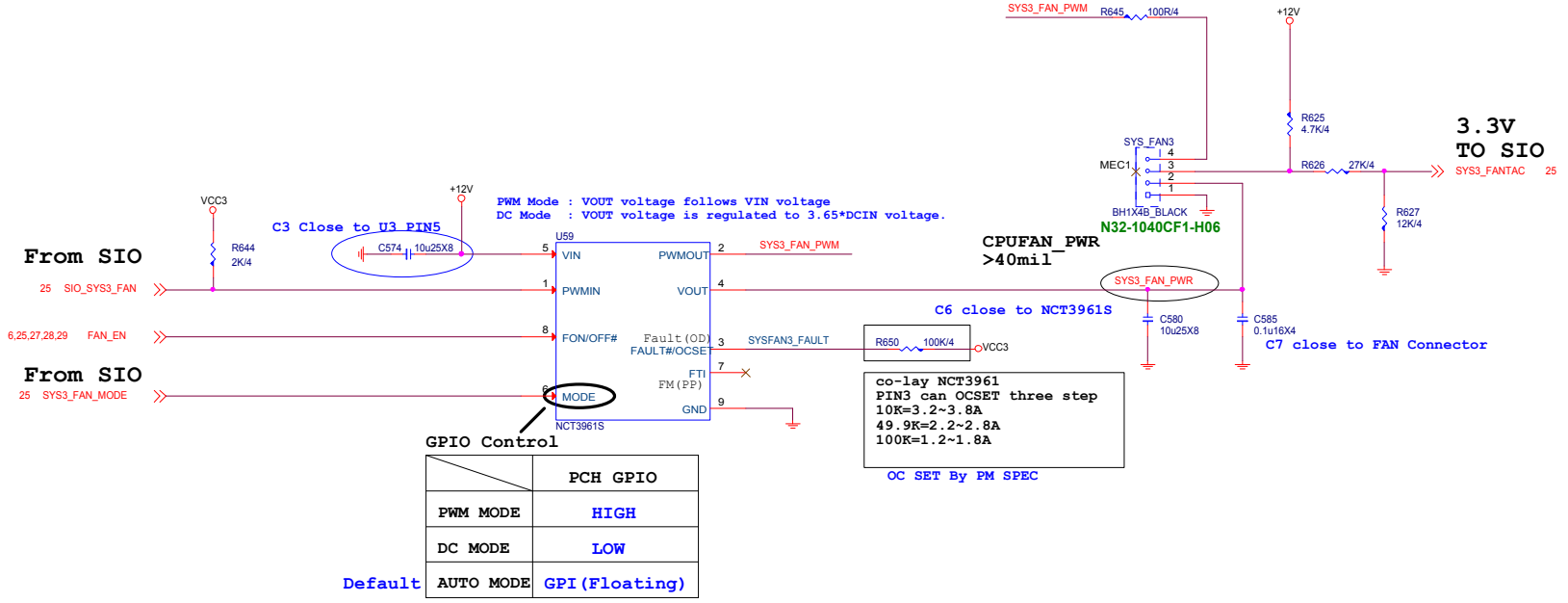
SYSFAN3

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD	
MS-7C95	
Size: Custom	Document Description: 30 FAN TYPE-M SYSFAN3
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RTL8111EPV(default) coly RTL8111HN Giga LAN

LAN Connector

close to IC

UL1 — RTL8111DP-VC-CG

PCIE interface: HSIP, HSIN, HSOP, HSON, REFCLK_P, REFCLK_N, PERSTB, CLKREQB

PM: ISOLATEB, LANWAKEB

Regulator: RSET, VDDREG-1, VDDREG-2, REGOUT

POWER: DVDD33, DVDD10, AVDD10, AVDD33, GND, NC

Transceiver Interface: MDIP0/MDIN0, MDIP1/MDIN1, MDIP2/MDIN2, MDIP3/MDIN3

LED: JTRSTN/LED0, JTDI/LED1, JTMS/LED2

EEPROM: SPICSB, SPISO, SPISI, SPISCK

SMB GPIO: SMBCLK, SMBDATA, JCLK/GPIO1/SMBALERT, JTDO/GPIO0

CLOCK: CKXTAL1, CKXTAL2

unstuff for debug only

stuff for debug only

RTD3 USE

EPV:stuff HN:unstuff

0XC8

ASF Device use

Main:D0G-1020530-I05
AVL:D0G-8010510-SI0

D0G-1020530-I05

ESD-VPORT0603L102KV05

LAN_USB2B — RJ45_USBX2_LEDX2_TX-RH-93

20180409 Change to N58-32F0721-F02.

ESD Protect

close to connector

U76 / U77 — ESD-AOZ8906CI

D0G-05A0529-A68
avl:D0G-45B0510-I14

2.0 update

U33 — NC7SZ08M5X_SC74A-5-HF

MAX: mA

3.3v Power on rise time : 0.5~100ms.

MAX: 70mA

close pin 12 39 42 47 48

EPV:unstuff HN:stuff

come back test

20141217 update
CHOKEL1: L04-47A70E0-T19
AVL: L04-47A7870-C08
L04-47A7690-M26

MAX: 500mA

width>60mil

CH-4.7u2A70mS-HF-2

CHOKE20

CHOKE20 close to Pin 36 within 200 mil

CL63,CL64 close to CHOKE12 within 200 mil

close pin 3 6 9 13 41 45 29

close pin 21 21

EPV:unstuff HN:stuff

come back test

pin 35 — pin 24 — pin 30

pin 27 — pin 29

For EMI

GN:stuff

EPV:unstuff

EPV:stuff

GN:unstuff

X_MX25L8006EM2I-12G-HF

Configuration Table	RL34	RL43	RL42	RL41	RL40	RL45	RL44	RL65	RL64
8111HN	O	O	X		X	O	X	O	X
8111EPV (default)	X	X	O		O	X	O	X	O

Configuration Table	RL21	RL48	RL53	RL52
8111HN	O	X	X	O
8111EPV (default)	X	X	X	X
8111EPV (debug only)	X	O	X	O

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ALC892

Follow APU power well

CPU_1P8_S5

11mA

Closed Codec

VCC3

LDOOUT

SMD CAP: Fail to test THD+N
EL/SOLID cap: Test THD+N will Pass

Closed pin9

CA15 X_10u6.3X6 CA18 0.1u16X4

CA24 10u6.3X6 CA23 0.1u16X4

CA25 0.1u16X4 CA26 10u6.3X6

CA14 22u6.3X6 closed PIN25

closed PIN38

C91-1011051-N07

UA5

33 EAPD — EAPD — 47 EAPD/SPDIFI

48 SPDIF-OUT

5 AZ_SDOUT
5 AZ_SDIN0 — RA31 22R/4 — SDIN0 — 8 SDATA-OUT

5 AZ_SYNC — 10 SDATA-IN
5 AZ_RST# — 11 SYNC

CA19 X_10p50N4 — 5 AZ_BITCLK — 6 RESET# / BCLK

damping close to FCH

CA21 10u6.3X6 — REGREF — 2 GPIO0/DMIC-CLK/SPDIF-OUT2 / 3 REGREF

SENSE_A — 13 SENSE A
33 SENSE_B — SENSE_B — 34 SENSE B

33 MIC2_VREFO — MIC1-VREFO-R — 32 MIC1-VREFO-R
MIC1-VREFO-L — 28 MIC2-VREFO
37 MIC1-VREFO-L

45.8mA — LDOVDD — 33 LINE2_VREFO — 31 PIN37-VREFO
VREF — 27 LDO-IN
33 LINE2-VREFO
JDREF — 40 VREF
33 SENSE C
JDREF

CA17 X_0.1u16X4 — CA16 10u6.3X6 — RA63 20K1%4

12 BEEP

GPIO1/DMIC-DATA — DVSS — AVSS — AVSS

ALC892-CG-RH

B05-LC89214-R09

DVDD — DVDD-IO — LDO-OUT1 — LDO-OUT2

FRONT-R 36 — A_LOUT_R+ — ECA11 1+ — 2 CD100u10SO — ALOUT_R
FRONT-L 35 — A_LOUT_L+ — ECA12 1+ — 2 CD100u10SO — ALOUT_L
ALOUT_R 33
ALOUT_L 33

SURR-R 41
SURR-L 39

CENTER 43
LFE 44

SIDE-R 46
SIDE-L 45

LINE1-R 24 — A_LINE_IN_R — CA8 10u6.3X6 — LINE_IN_R
LINE1-L 23 — A_LINE_IN_L — CA9 10u6.3X6 — LINE_IN_L

C91-1011051-N07

LINE2-R 15 — A_LINE2_R — ECA6 1+ — 2 CD100u10SO — ALINE2_R
LINE2-L 14 — A_LINE2_L — ECA10 1+ — 2 CD100u10SO — ALINE2_L
ALINE2_R 33
ALINE2_L 33

MIC1-R 22 — A_MIC1_R — CA10 10u6.3X6 — MIC1_R
MIC1-L 21 — A_MIC1_L — CA11 10u6.3X6 — MIC1_L

MIC2-R 17 — A_MIC2_R — CA12 10u6.3X6 — MIC2_R
MIC2-L 16 — A_MIC2_L — CA13 10u6.3X6 — MIC2_L
MIC2_R 33
MIC2_L 33

CD-R 20
CD-GND 19
CD-L 18

892,887/4.7uF: Test THD+N will Pass
898/10uF: Test THD+N will Pass

Closed Codec Pin 27

Closed Codec

SENSE_A — RA26 5.1K1%4 — FRONT_JD
RA64 10K1%4 — LINE1_JD
RA27 20K1%4 — MIC1_JD

EMI

CA7 X_0.1u16X4
CA32 X_1000p50X4

CPA5 X_COPPER
CPA6 X_COPPER

Digital *Analog*

5VDUAL — LA5 0R/8 — 45.8mA — LDOVDD
ATX_5VSB — LA1 X_0R/8
DA5 X_TVS
CA58 10u6.3X6 CA57 0.1u16X4

CA58,CA57 close to LA1,LA5

AUDIO1A

LINE_IN_L — RA5 75R/4 — LINE_IN_LA
LINE_IN_R — RA6 75R/4 — LINE1_JD — LINE_IN_RA

CA29 100p50N4 CA30 100p50N4

13 12 11 10 3 — 15 14 16

JACK-AUDIOX3F_PK/LIME/LIGHT/BU-RH
LIN_IN

AUDIO1B

33 LOUT_L — LOUT_L — RA13 75R/4 — LOUT_LA
33 LOUT_R — LOUT_R — RA17 75R/4 — FRONT_JD — LOUT_RA

DA12 ESD-MLVS0402L04-HF
D0G-2710510-I05
DA13 ESD-MLVS0402L04-HF
D0G-2710510-I05

9 8 7 6

JACK-AUDIOX3F_PK/LIME/LIGHT/BU-RH
LIN_OUT

AUDIO1C

MIC1-VREFO-L — RA30 2.2K/4 — MIC1_LA
MIC1-VREFO-R — RA68 2.2K/4 — MIC1_RA

MIC1_L — RA29 75R/4 — MIC1_LA
MIC1_R — RA67 75R/4 — MIC1_JD — MIC1_RA

CA33 100p50N4 CA34 100p50N4

5 4 2 1 — 17 18

JACK-AUDIOX3F_PK/LIME/LIGHT/BU-RH
MIC1

LOUT_LA — LOUT_RA — RA14 22K/4 — RA18 22K/4

D LIN_IN
E LIN_OUT
F MIC1

N54-13F0271-K06

MICRO-STAR INT'L CO.,LTD

MS-7C95

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Custom	32 Audio ALC892	20

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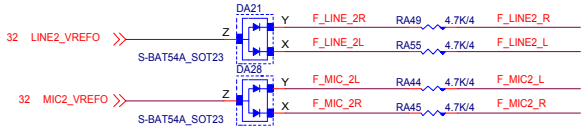
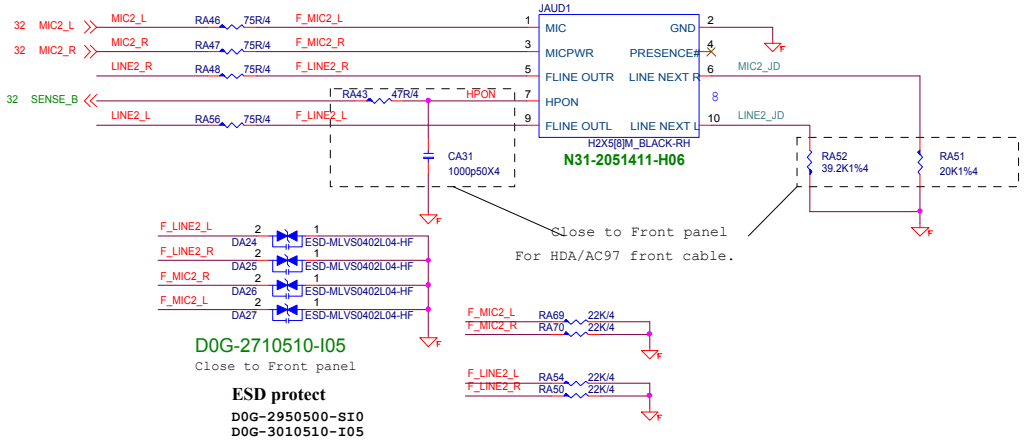
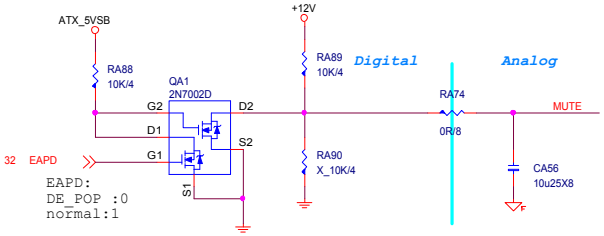
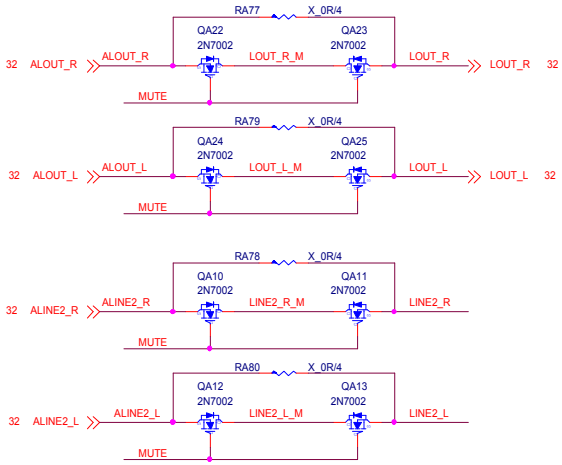




Rear Line OUT De-POP circuit

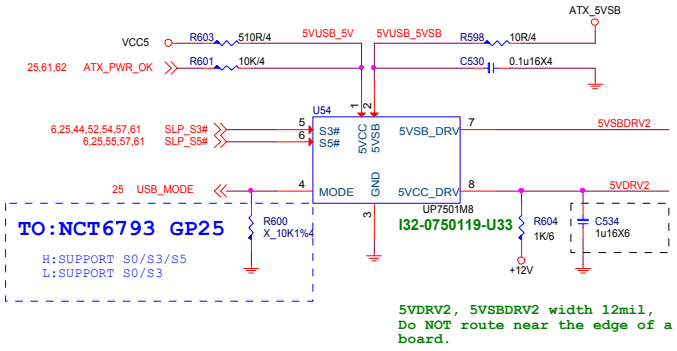
(De-pop circuit for Rear Line out & Front Headphone out)

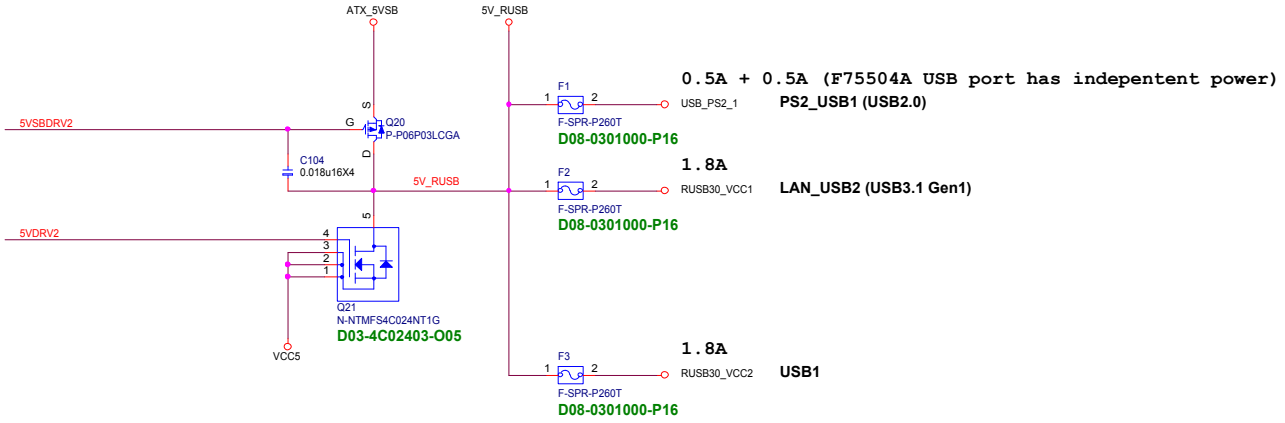




MICRO-STAR INT'L CO.,LTD	
MS-7C95	
Size: Custom	Document Description: 33 Audio DePoP
Rev: 20	
Date: Monday, May 11, 2020	Sheet 33 of 74

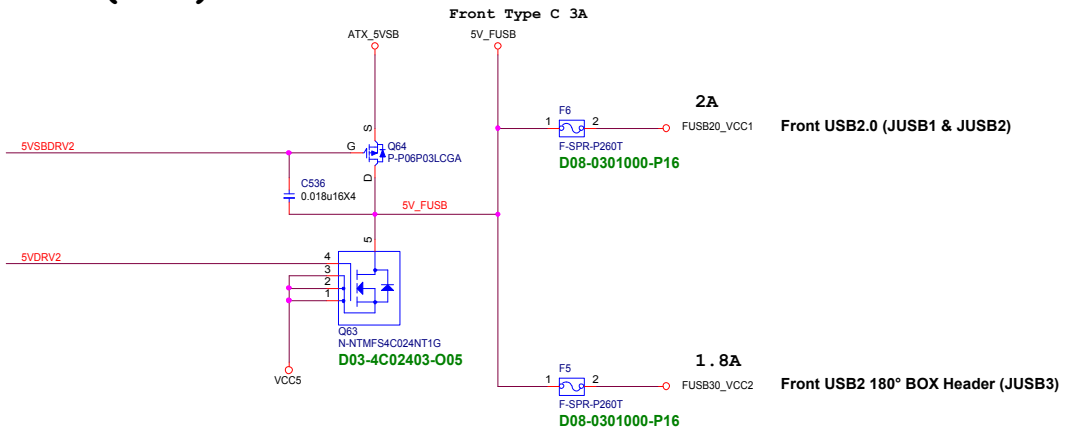
USB Power





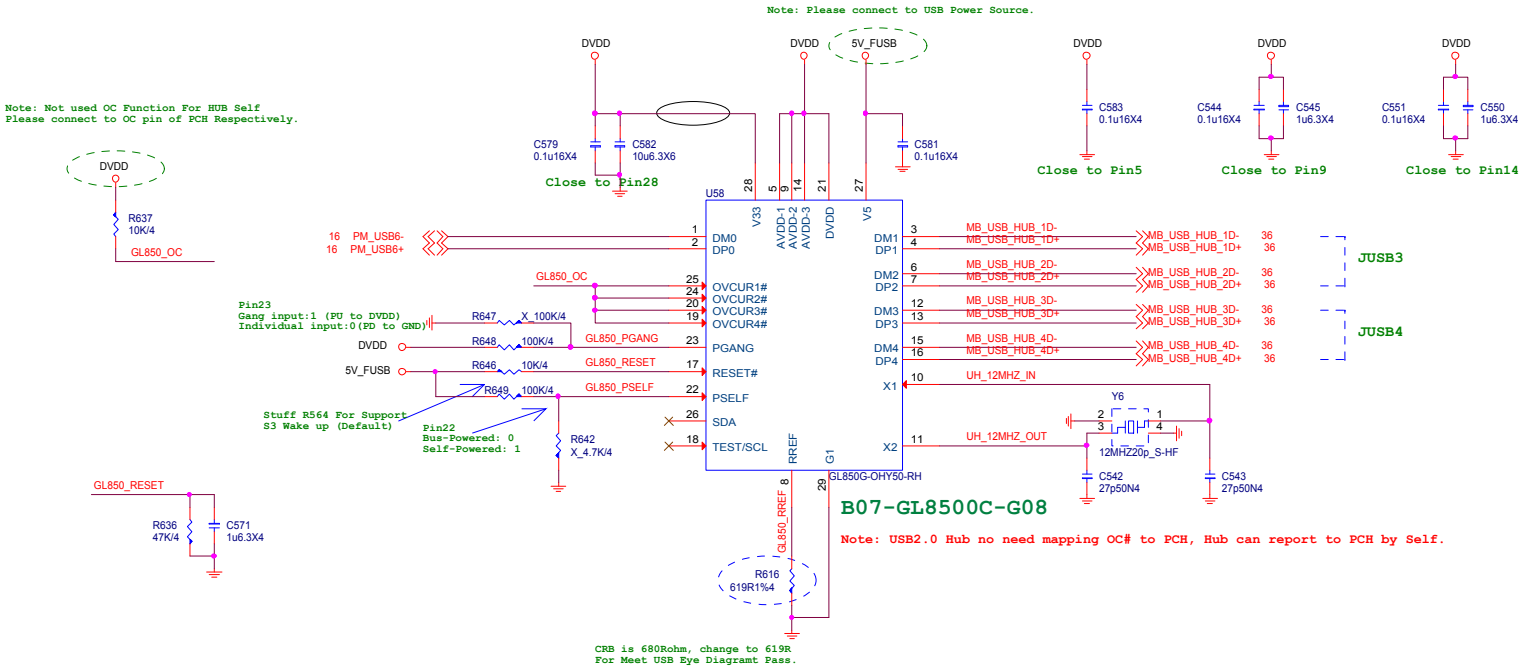
Rear (4.6A)

Front (6.8A)



MICRO-STAR INT'L CO.,LTD		
MS-7C95		
Size: Custom	Document Description: 34 USB Power - UP7501	Rev: 20
Date: Monday, May 11, 2020	Sheet 34 of 74	

GL850G USB2.0 HUB



B07-GL8500C-G08

Note: USB2.0 Hub no need mapping OC# to PCH, Hub can report to PCH by Self.

MICRO-STAR INT'L CO.,LTD		
MS-7C95		
Size: Custom	Document Description: 35 GL850G - USB2.0 HUB	Rev: 20
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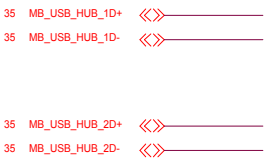
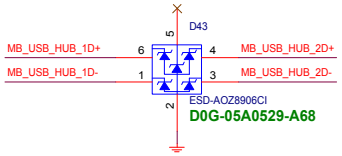
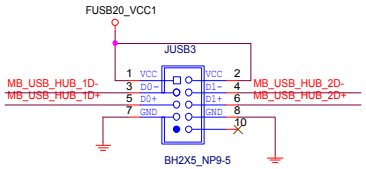
Front USB2.0(JUSB1)

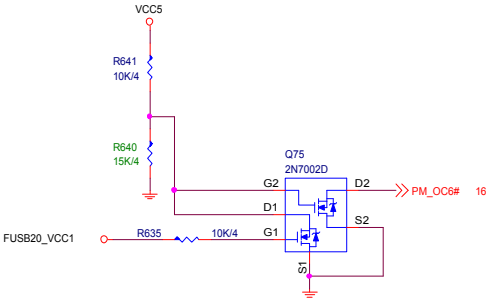
Form GL850G USB2.0 HUB

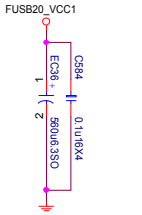
5V@1A







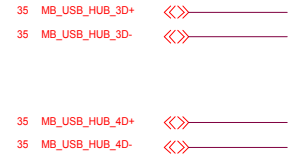


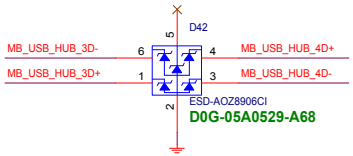


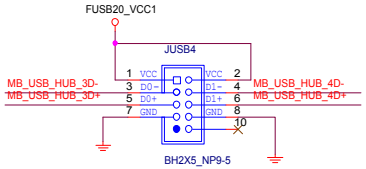
Front USB2.0(JUSB2)

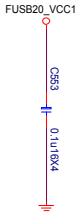
Form GL850G USB2.0 HUB

5V@1A









MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C95	
Size: Custom	Document Description: 36 Front USB2.0 Header	Rev: 20
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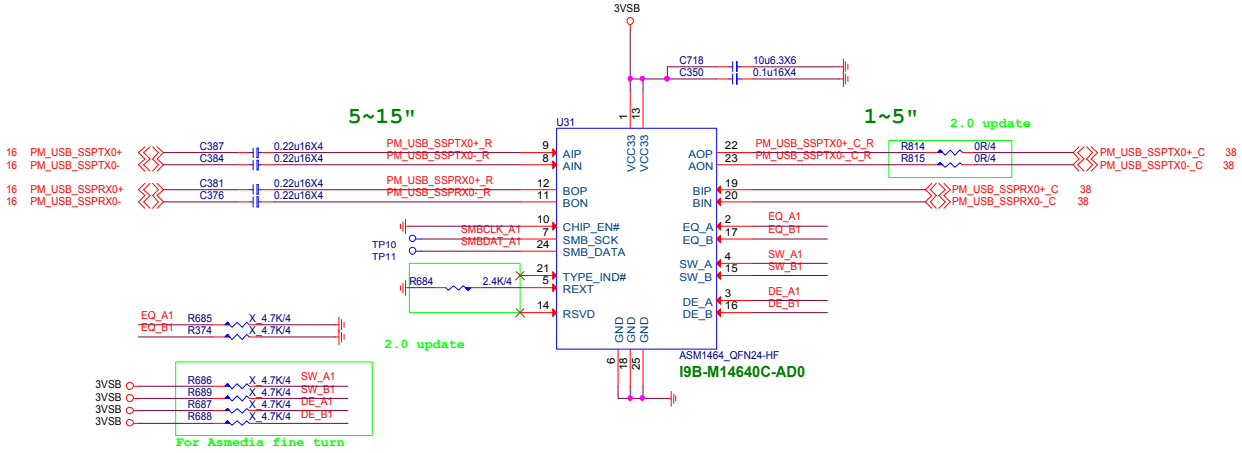
USB3.1 Gen1 Redriver for Type-C

0.13A



MICRO-STAR INT'L CO.,LTD		
MS-7C95		
Size: Custom	Document Description: 37 ASM1464 - USB3.1 Redriver	Rev: 20
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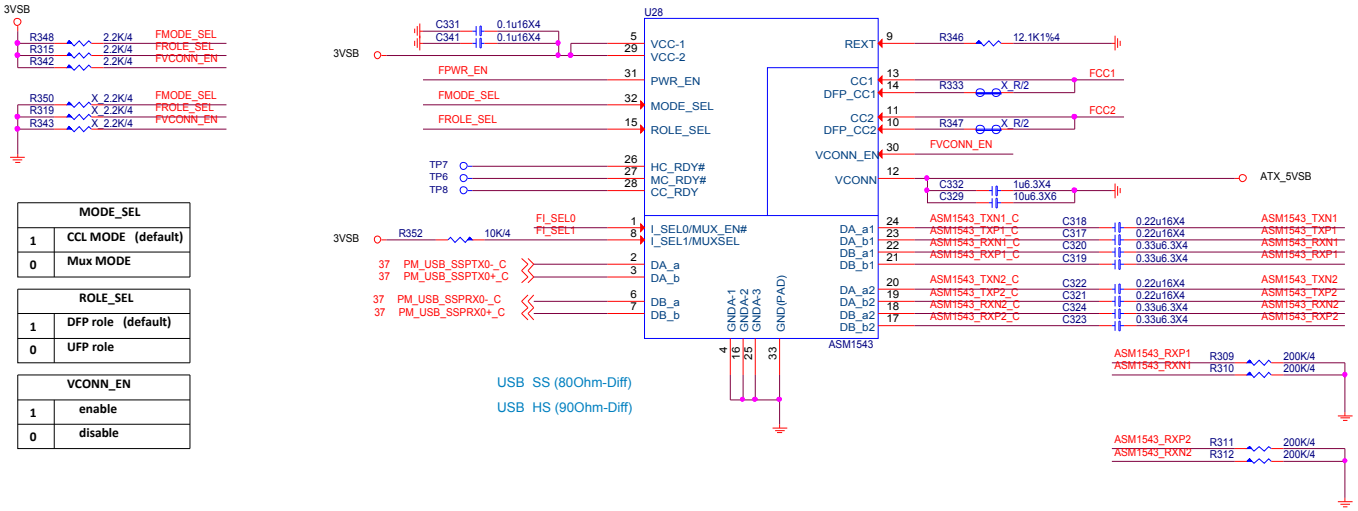
USB 3.1-Type-C

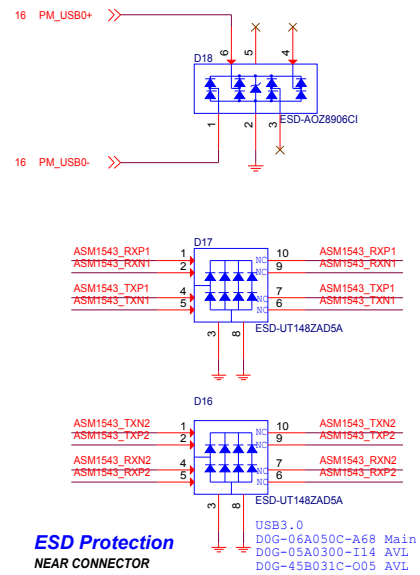
USB Type-C MUX with Configuration Channel (CC)



MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

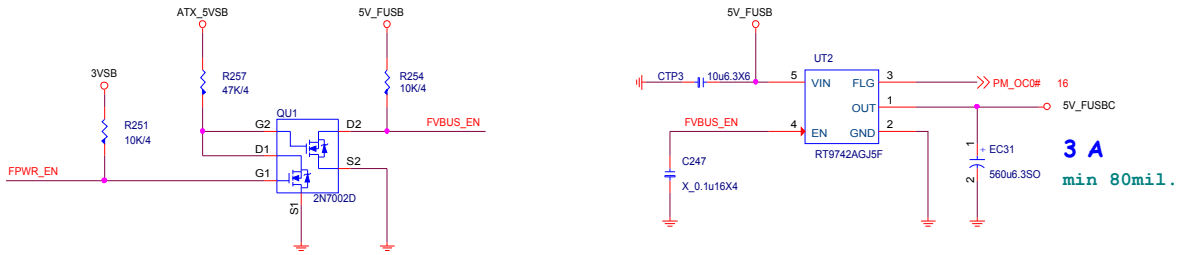
VCONN_EN	
1	enable
0	disable



VBUS OC# LEVEL SHIFT

VBUS EN

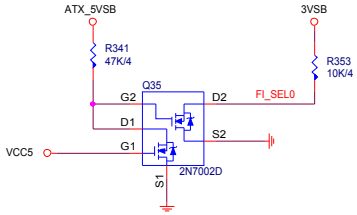
VCOM OC#

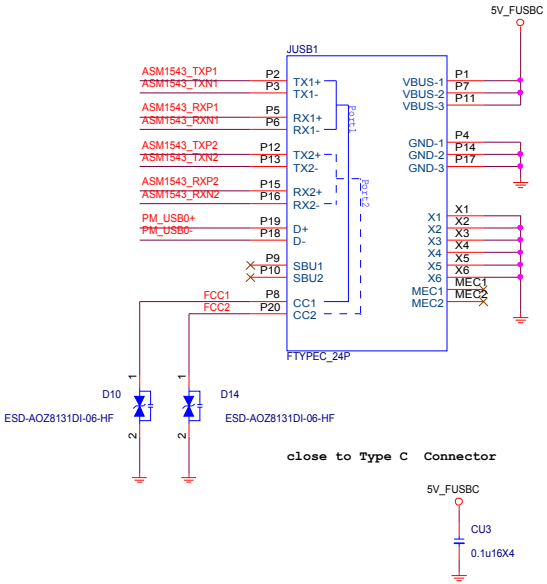


Current Mode

I_SEL0	I_SEL1	
X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

1.5A under S3 mode
3A under S0 mode





MICRO-STAR INT'L CO.,LTD

MS-7C95

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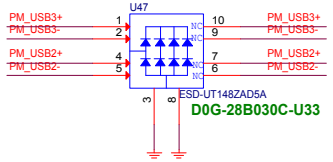
Front USB3 180° BOX Header(JUSB3)

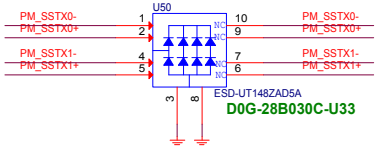
5V@1.8A

16 PM_USB2+
16 PM_USB2-
16 PM_USB3+
16 PM_USB3-

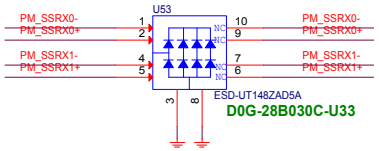
16 PM_USB_SSTX0+ — C514 0.22u16X4 — PM_SSTX0+
16 PM_USB_SSTX0- — C523 0.22u16X4 — PM_SSTX0-
16 PM_USB_SSRX0+ — C532 0.33u6.3X4 — PM_SSRX0+
16 PM_USB_SSRX0- — C533 0.33u6.3X4 — PM_SSRX0-
16 PM_USB_SSTX1+ — C510 0.22u16X4 — PM_SSTX1+
16 PM_USB_SSTX1- — C512 0.22u16X4 — PM_SSTX1-
16 PM_USB_SSRX1+ — C529 0.33u6.3X4 — PM_SSRX1+
16 PM_USB_SSRX1- — C531 0.33u6.3X4 — PM_SSRX1-



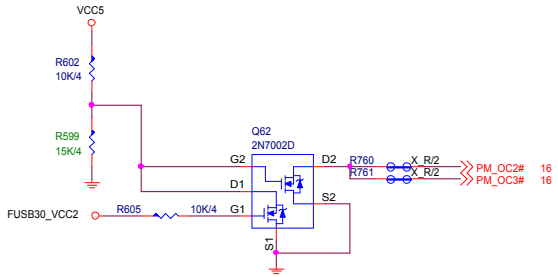
D0G-28B030C-U33

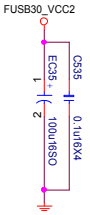


D0G-28B030C-U33

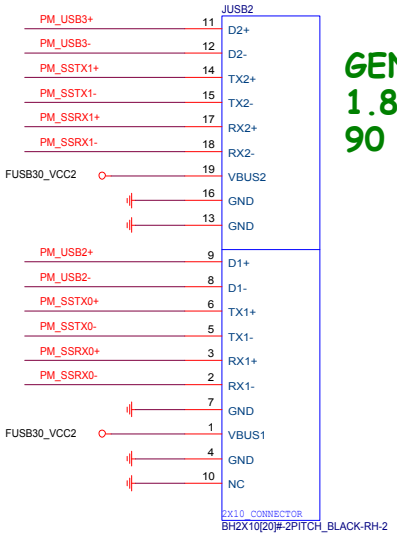


D0G-28B030C-U33





C71-1011761-N07



N32-2101581-H06

GEN1
1.8A
90 degree

MICRO-STAR INT'L CO.,LTD		
MS-7C95		
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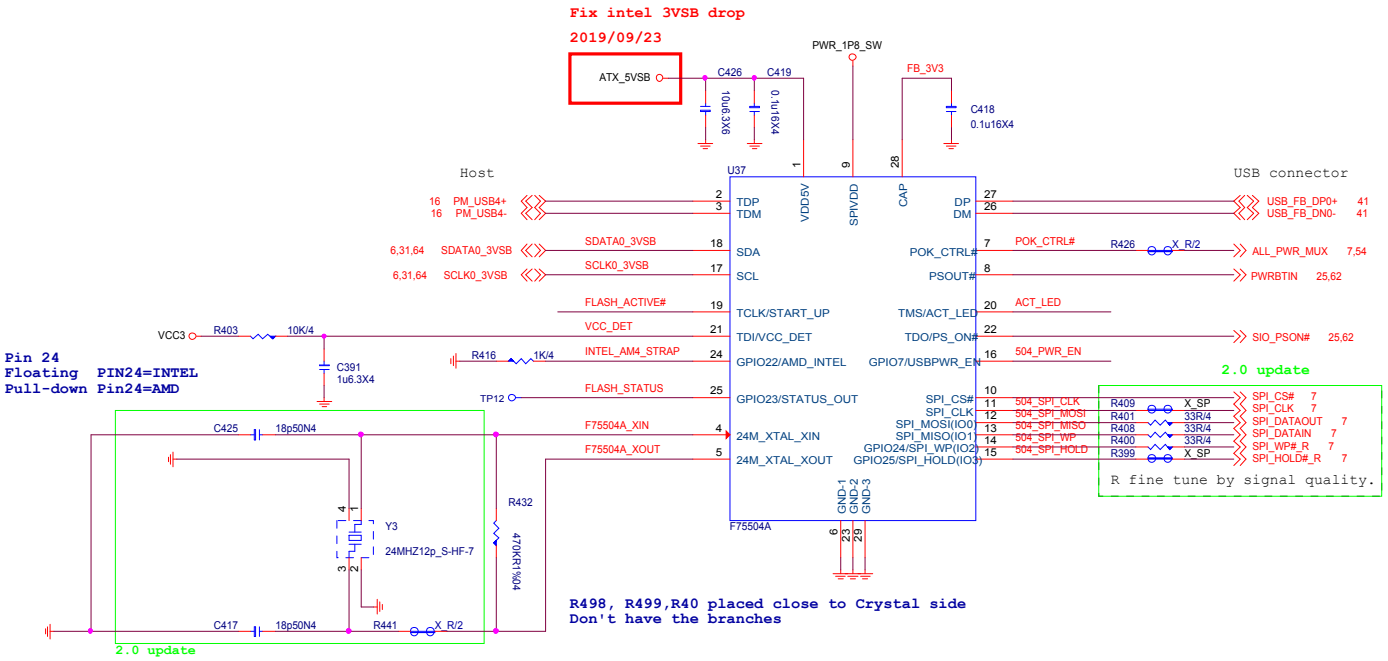
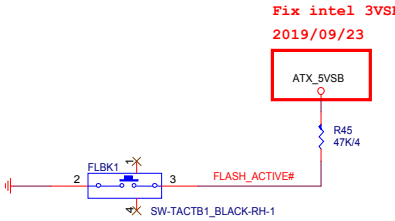
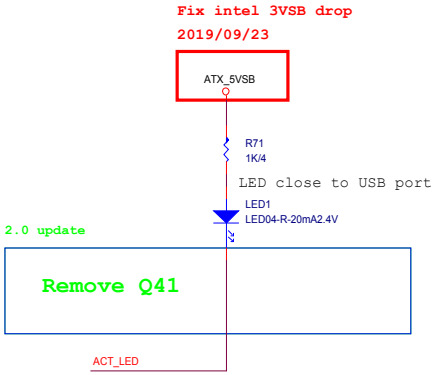
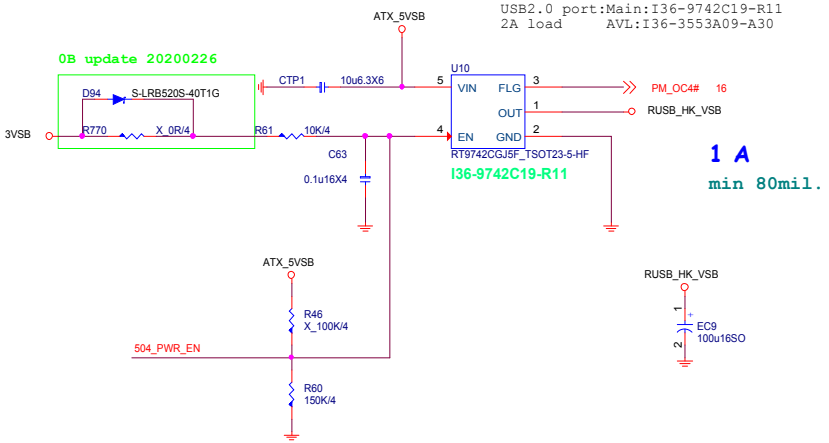
F75504A

F75504A/F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.









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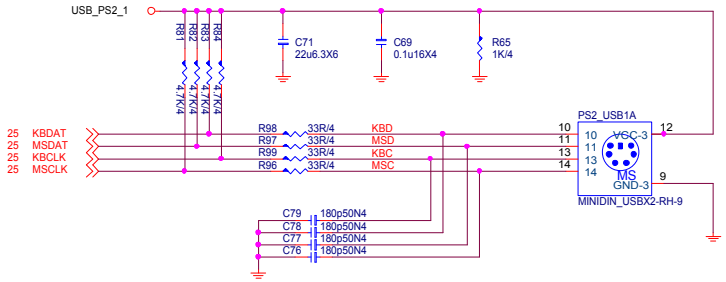
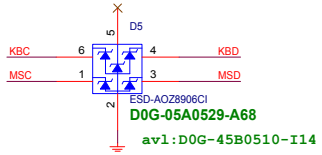
PS2+USB (USB2.0)

5V@1A

layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

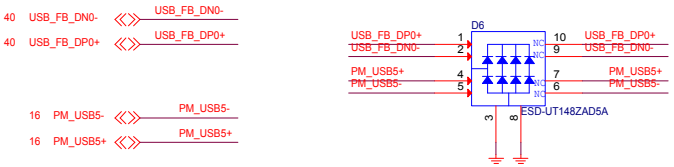


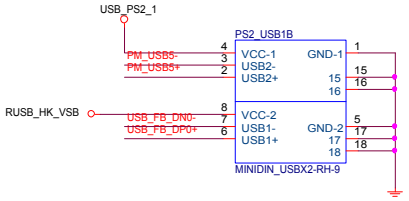


D0G-05A0529-A68

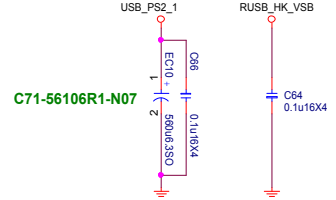
avl:D0G-45B0510-I14

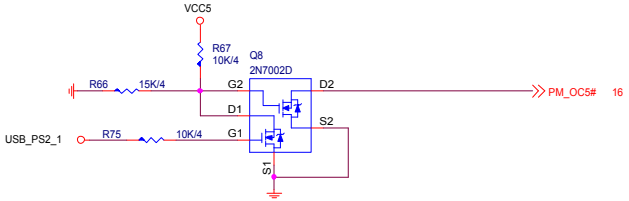
ESD close to connector.





1A **USB Flash BIOS**





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MS-7C95		
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Rear USB3.1 GEN2 5V@1.8A

TYPE A+C from CPU PI3EQX1004 Redriver

APU_USB2+ 7,42
APU_USB2- 7,42

APU_USB3+ 7,42
APU_USB3- 7,42

7 APU_USB_SSTX2+ — C224 0.22u16X4 — SSTX2+
7 APU_USB_SSTX2- — C218 0.22u16X4 — SSTX2-

7 APU_USB_SSRX2+ — C215 0.33u6.3X4 — SSRX2+
7 APU_USB_SSRX2- — C211 0.33u6.3X4 — SSRX2-

7 APU_USB_SSTX3- — C209 0.22u16X4 — SSTX3-
7 APU_USB_SSTX3+ — C203 0.22u16X4 — SSTX3+

7 APU_USB_SSRX3- — C200 0.33u6.3X4 — SSRX3-
7 APU_USB_SSRX3+ — C198 0.33u6.3X4 — SSRX3+

U66
7,42 APU_USB3+ — 1 — 10 — APU_USB3+
7,42 APU_USB3- — 2 — 9 — APU_USB3-
7,42 APU_USB2+ — 4 — 7 — APU_USB2+
7,42 APU_USB2- — 5 — 6 — APU_USB2-
3, 8 — ESD-UT148ZAD5A
D0G-28B030C-U33

U65
SSTX3+ — 1 — 10 — SSTX3+
SSTX3- — 2 — 9 — SSTX3-
SSTX2+ — 4 — 7 — SSTX2+
SSTX2- — 5 — 6 — SSTX2-
3, 8 — ESD-UT148ZAD5A
D0G-28B030C-U33

U64
SSRX2+ — 1 — 10 — SSRX2+
SSRX2- — 2 — 9 — SSRX2-
SSRX3+ — 4 — 7 — SSRX3+
SSRX3- — 5 — 6 — SSRX3-
3, 8 — ESD-UT148ZAD5A
D0G-28B030C-U33

1.8A
RUSB30_VCC2

HDMI_USB1B

APU_USB3+	31	D1+	VBUS-1	20	
APU_USB3-	30	D1-		26	
			GND_DRAIN-1		
SSTX3+	37	STAD_SSTX1+			
SSTX3-	36	STAD_SSTX1-	GND-1	23	
		UP			
SSRX3+	34	STAD_SSRX1+	SHELL-5	X5	
SSRX3-	33	STAD_SSRX1-	SHELL-6	X6	
APU_USB2+	22	D0+	VBUS-2	29	
APU_USB2-	21	D0-		35	
			GND_DRAIN-2		
SSTX2+	28	STAD_SSTX0+			
SSTX2-	27	STAD_SSTX0-	GND-2	32	
		DOWN			
SSRX2+	25	STAD_SSRX0+	SHELL-7	X7	
SSRX2-	24	STAD_SSRX0-	SHELL-8	X8	

USB3.0X2_HDMI_BRASS-RH

RUSB30_VCC2
EC25 560u6.3SO — C180 0.1u16X4 — C181 1u6.3X4

C71-56106R1-N07

MICRO-STAR INT'L CO.,LTD		
MS-7C95		
Size: Custom	Document Description: 42 Rear USB3.0 Type A HDMI_USB1	Rev: 20
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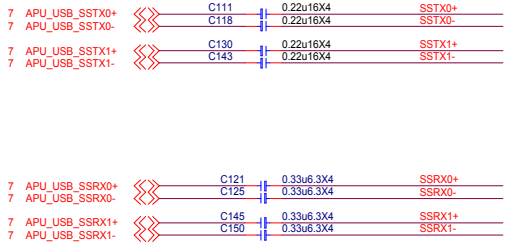
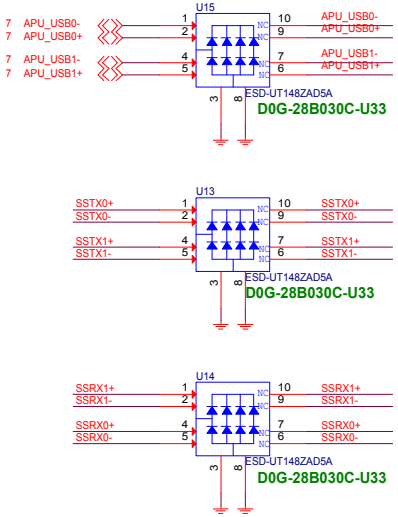
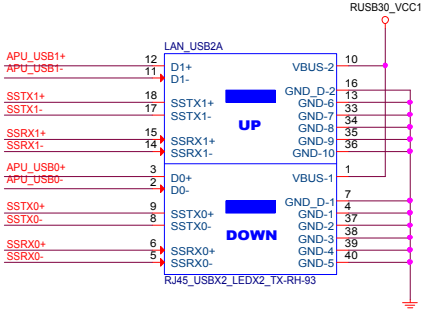
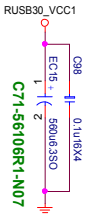
Rear USB3.1 GEN1 5V@1.8A
TYPE-A X2 from CPU



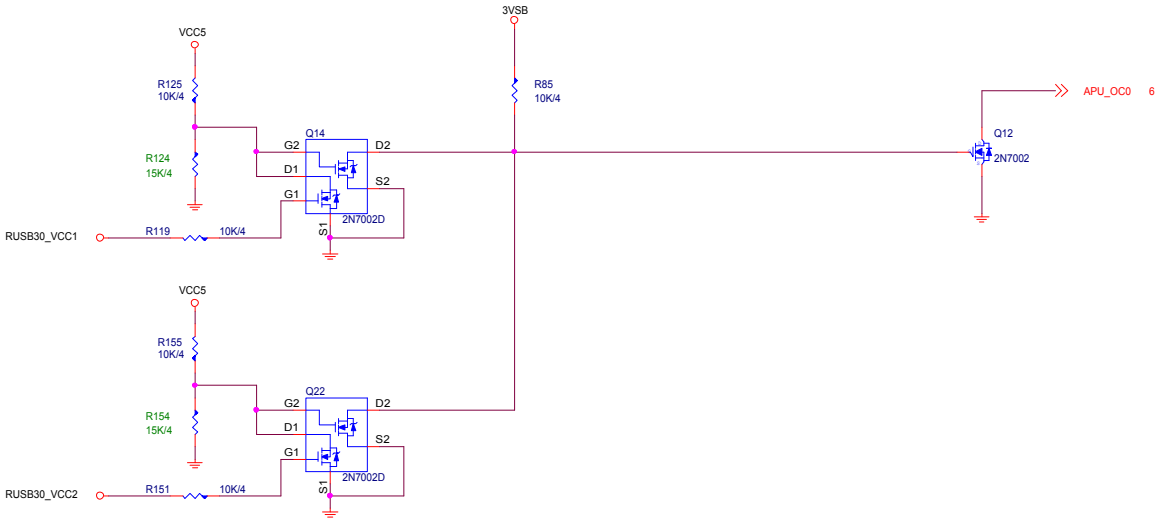


LAN下方
GEN1 1.8A





CPU OC Logic



Type1/2/3/4 High Active

	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

MICRO-STAR INT'L CO.,LTD

MS-7C95

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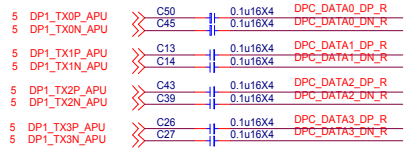
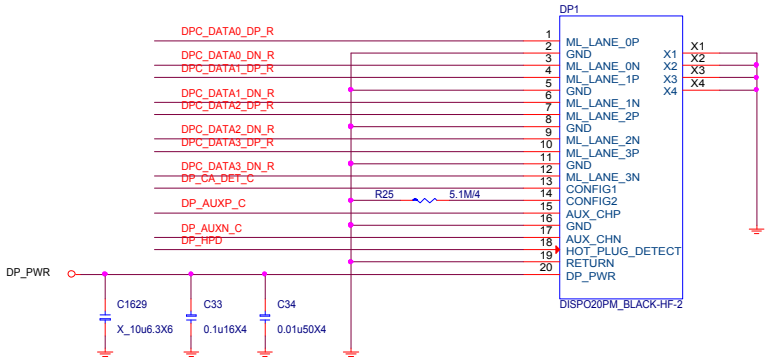
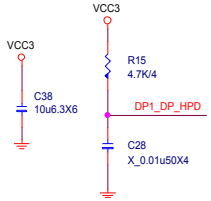
DP CONNECTOR

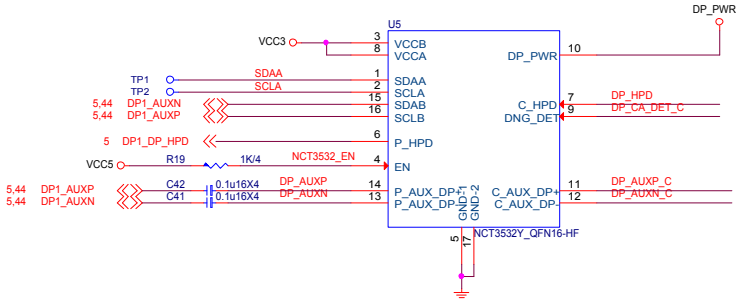


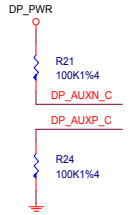


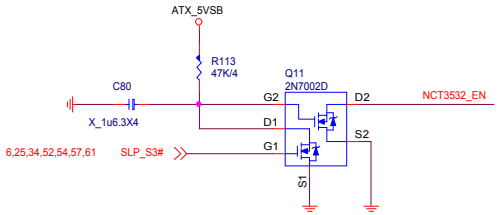
DP AUX & HPD Circuit

Support HDMI Dongle

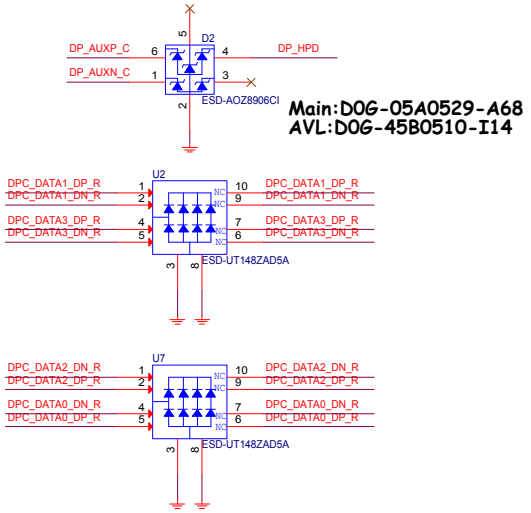








ESD



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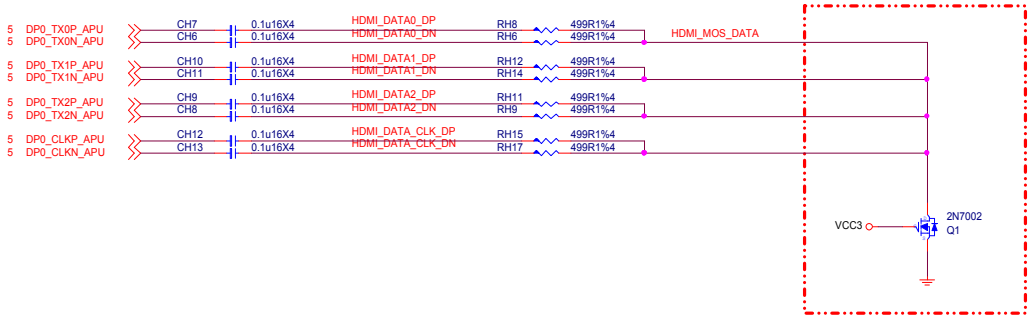
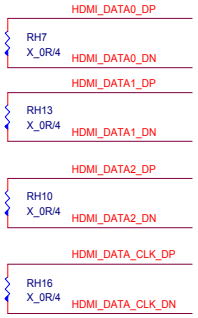
HDMI CONNECTOR

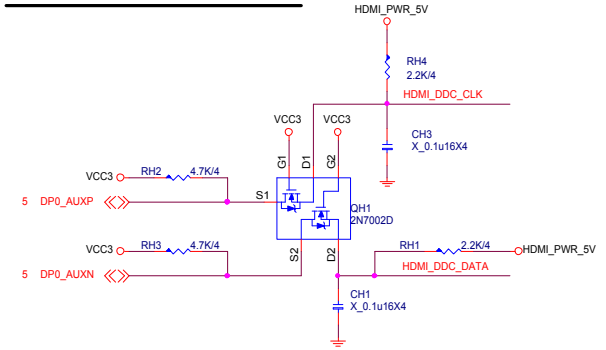
For HDMI 1.4



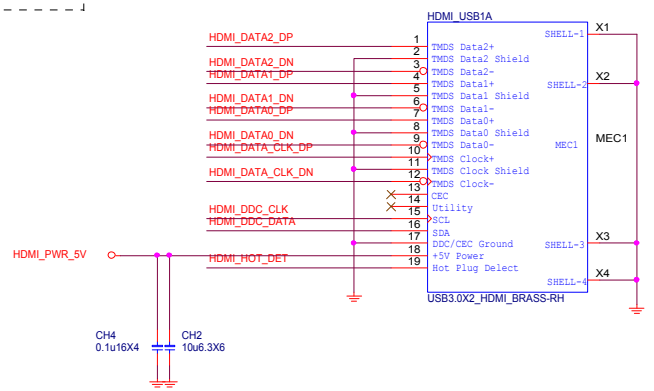


HDMI_MOS_DATA trace length <500mil
other platform please check design guide

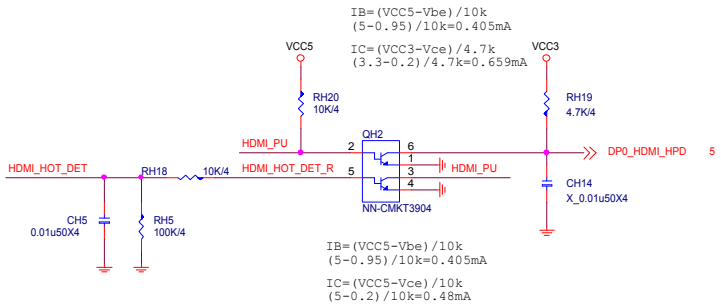
AUX Level Shifter



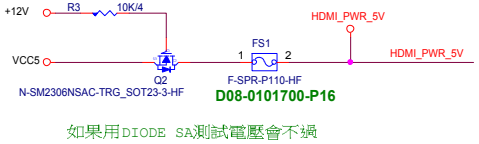
Connector



HPD Circuit

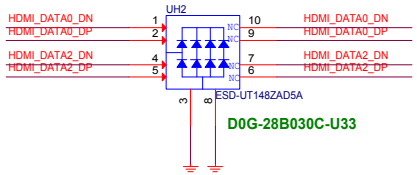


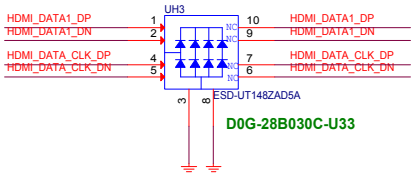
Connector Power



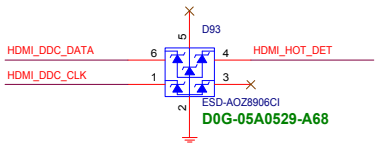
如果用DIODE SA測試電壓會不過

For EMI





注意:耐壓5V零件



MICRO-STAR INT'L CO.,LTD		
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0C Remove

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Vcore GROUP G TDC:95A,EDC:140A
NB GROUP C TDC:50A,EDC75A

Note: VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

0X40

Diff pair

Diff pair

VR18,VR27 change LL R↑ LL↓

VR87,VR84change LL R↑ LL↓

I32-8894J0C-R11

RT8894AGQW_WQFN56-HF

SET1 control ICCMAX,OCP setting
SET2 control Internal compensation

VCORE IccMAX: 140A =>OCP=>180A (4 x 45A)
LL=1.3m ohm
VCC_NB IccMAX: 75A =>OCP=> 90A
LL 2.1m ohm
FSK:250K

VRHOT=150 degree, 115 degree reset
Close to PWM
Close to MOSFET

VRHOT=125 degree, 90 degree reset
Close to PWM
Close to MOSFET

close to PWM
close to phase1 CHOKE

close to PWM
close to phase1 CHOKE

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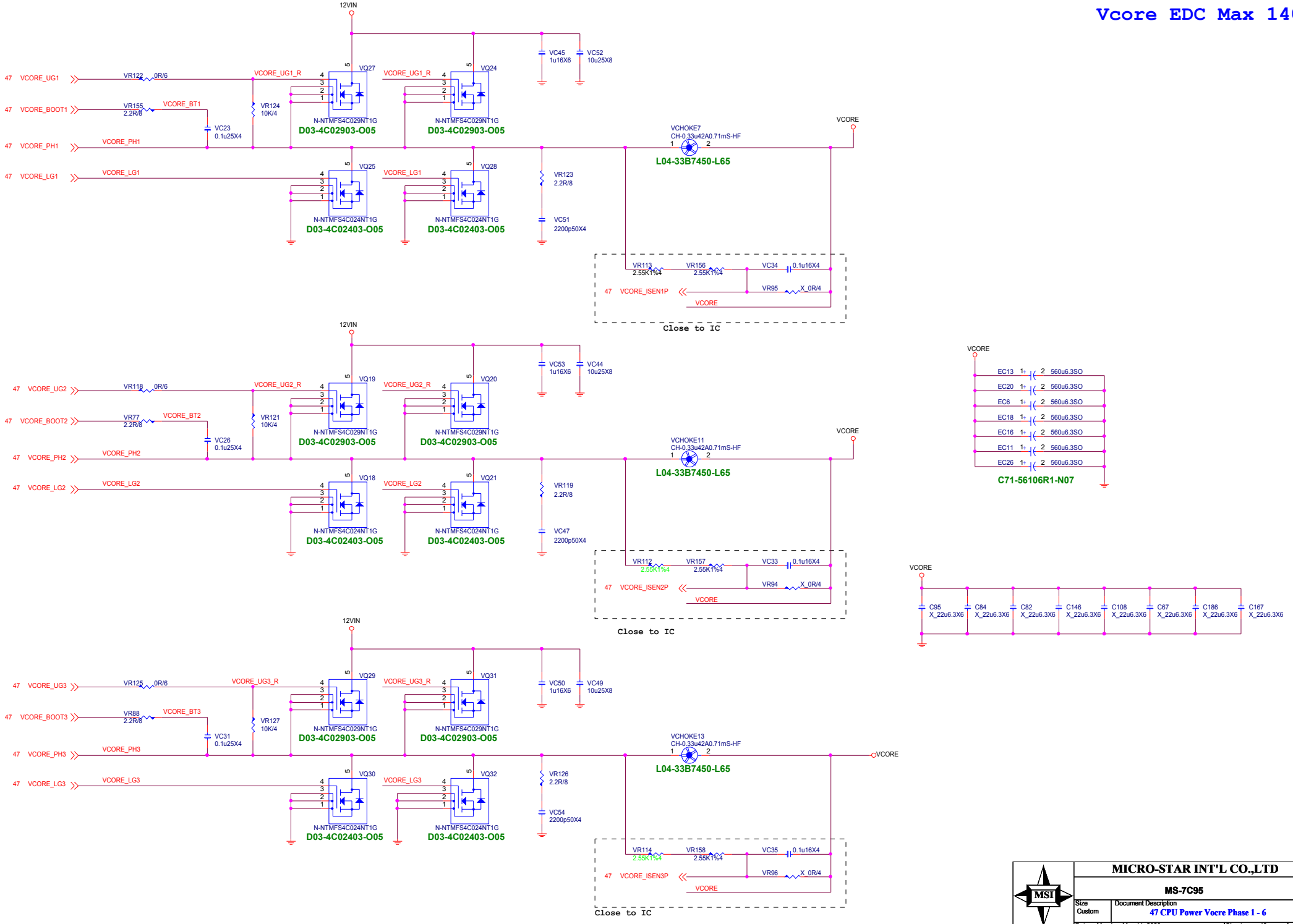
Vcore EDC Max 140A



MICRO-STAR INT'L CO.,LTD

MS-7C95

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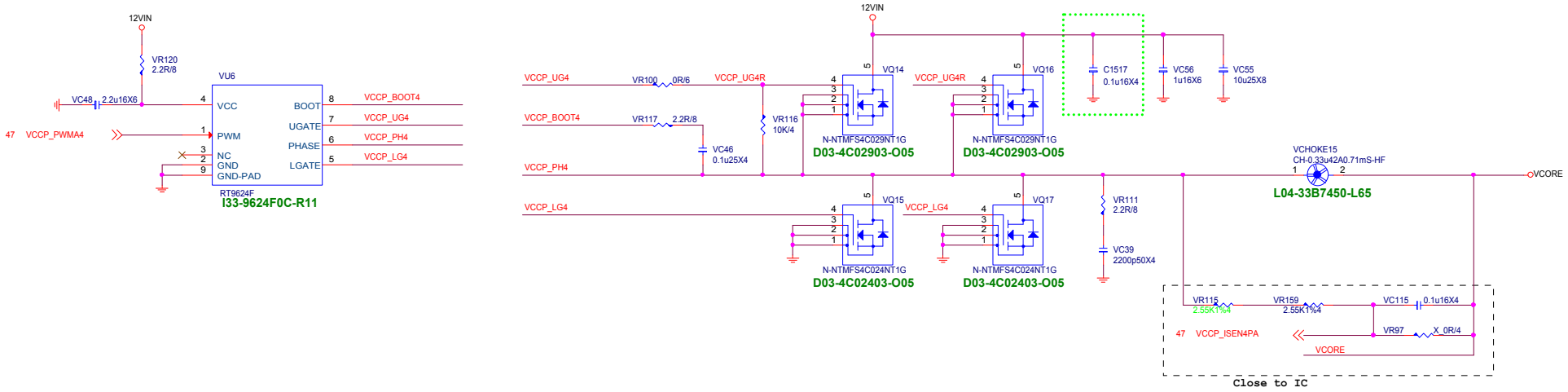

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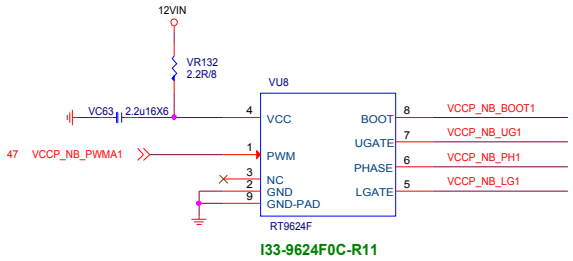
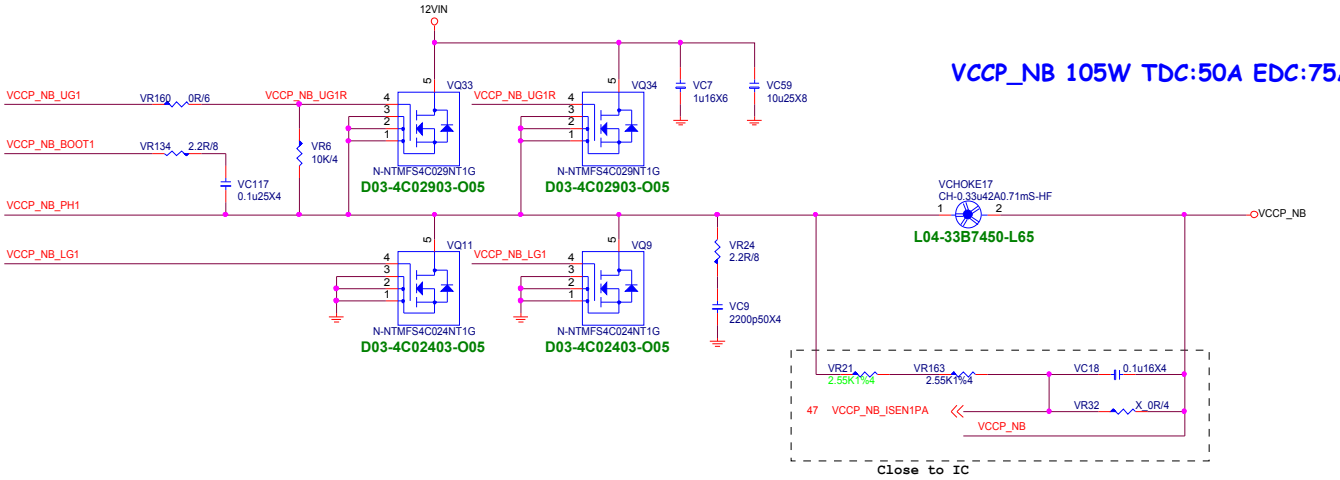
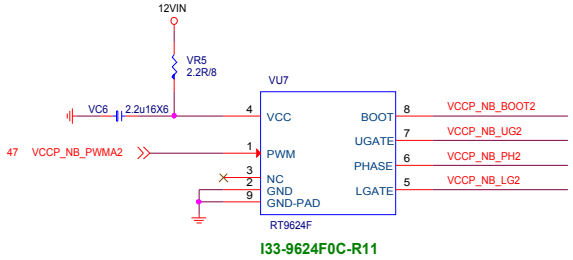
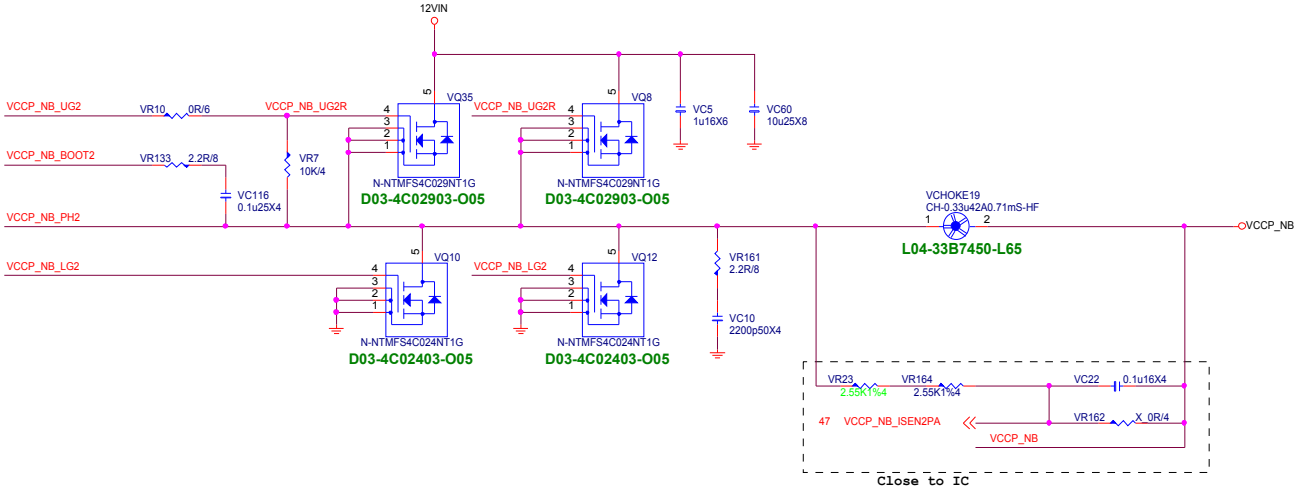
SOC EDC Max 75A

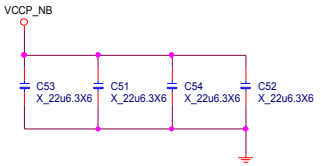
VCCP_NB 105W TDC:50A EDC:75A

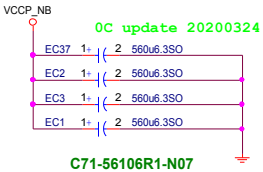












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Size: Custom	Document Description: 49 CPU Power NB Phase 1-2	Rev: 20
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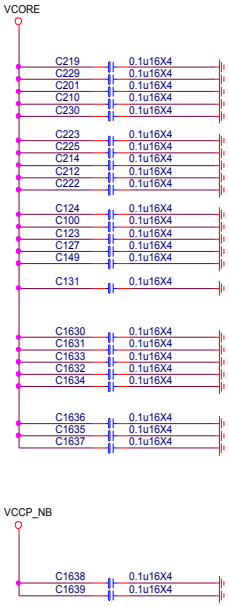

MICRO-STAR INT'L CO.,LTD		
MS-7C95		
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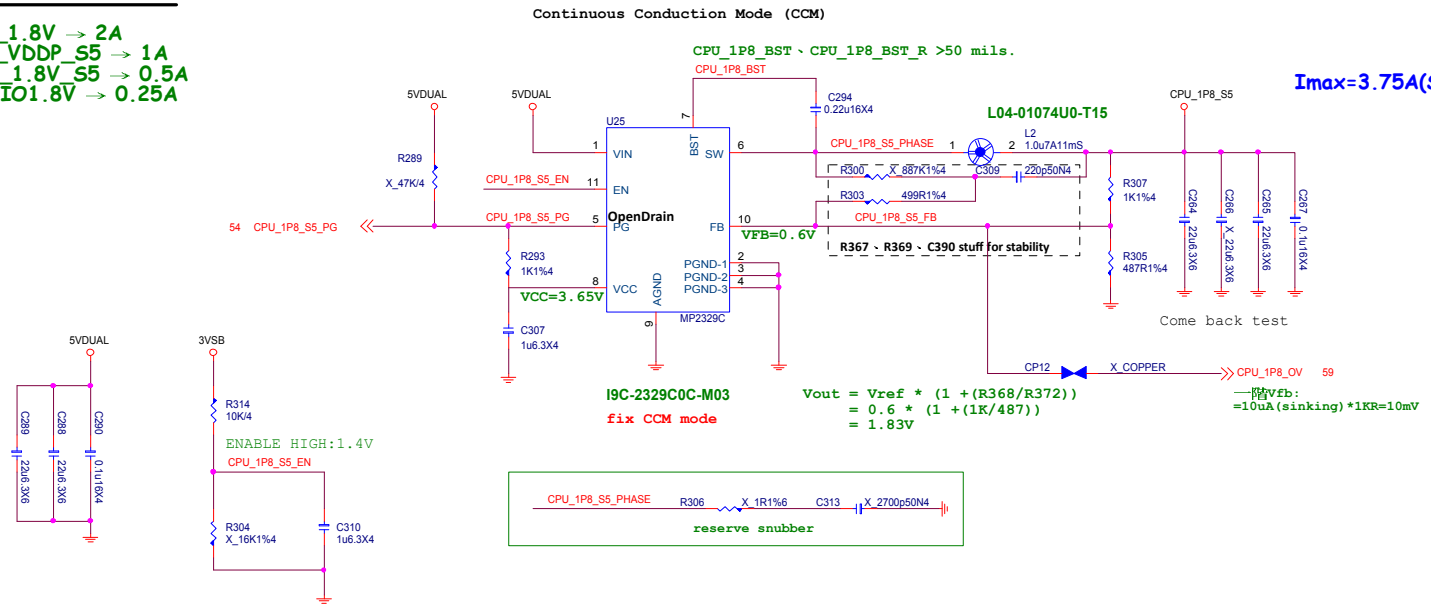
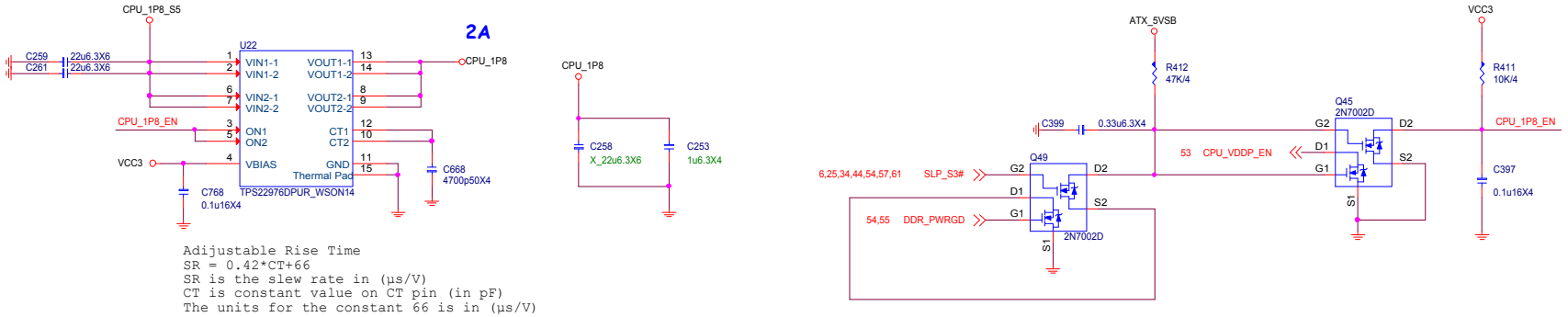
CPU 1.8V S5

CPU_1.8V → 2A
CPU_VDDP_S5 → 1A
VDD_1.8V_S5 → 0.5A
AUDIO1.8V → 0.25A



CPU 1.8V S0

CPU 1.8V_S0@2A



DDR_PWRGD
CPU_VDDP
CPU_1P8

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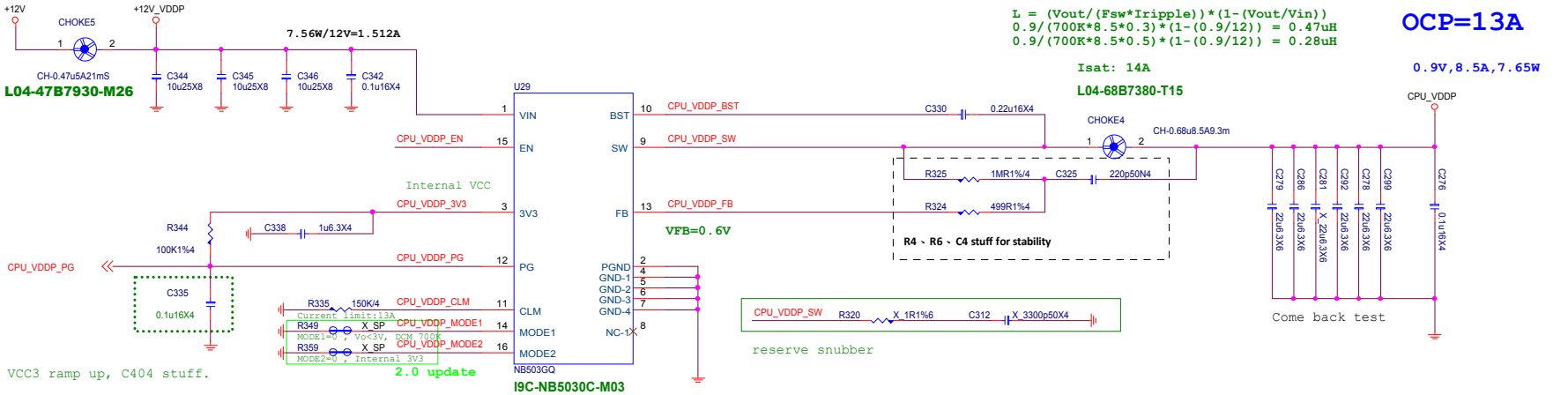
CPU_VDDP_S0

0.9V@S0:8.5A

S0:8.5A

```
Input Current = (13A*0.9V)/12V/0.8 = 1.22A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A
```




```
L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
0.9/(700K*8.5*0.3)*(1-(0.9/12)) = 0.47uH
0.9/(700K*8.5*0.5)*(1-(0.9/12)) = 0.28uH
```

OCP=13A

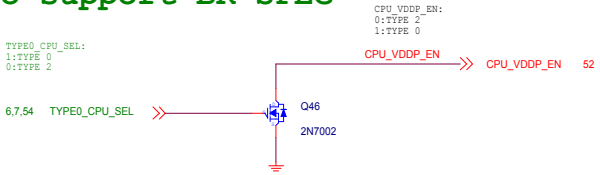
Isat: 14A

L04-68B7380-T15

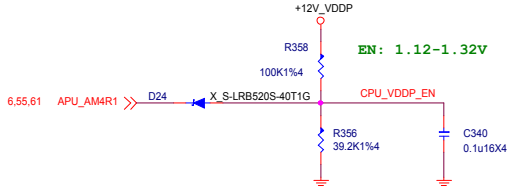
0.9V,8.5A,7.65W

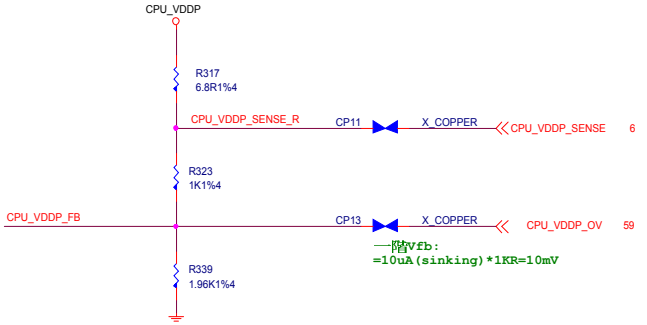
```
20180822
fix PG glitch when VCC3 ramp up, C404 stuff.
```

No support BR SPEC



CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN	
BR	0	1	0	1	SPEC no Support
NA	X	0	0	0	
SR	2	1	1	0	NOT SUPPORT TYPE2
RV/ZP	3	0	1	1	
MTS	4	1	1	1	NOT SUPPORT TYPE4



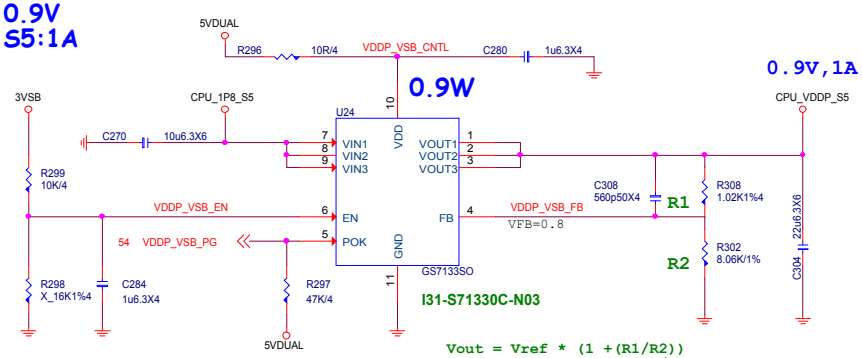



```
Vout = Vref + (R1*R4*Vref)/(R2*(R1+R4))
     = 0.6+(1k*1000k*0.6)/(1.96K*(1k+1000k))
     = 0.9058V
```

CPU_VDDP_S5

0.9V

S5:1A




```
Vout = Vref * (1 +(R1/R2))
     = 0.8 * (1 +(1.02K/8.06K))
     = 0.9V
```

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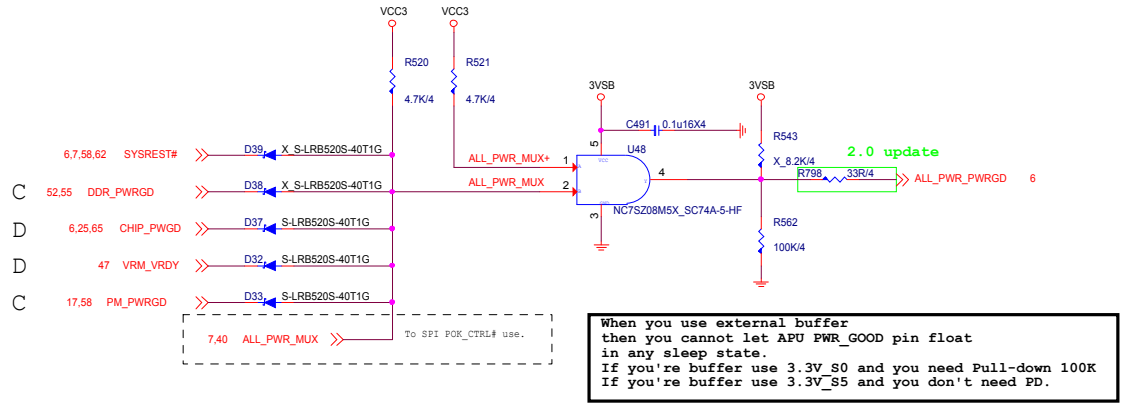
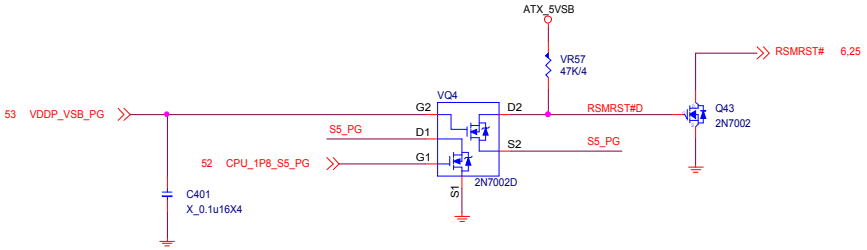
ALL POWER GOOD MUX

S0 PG



When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

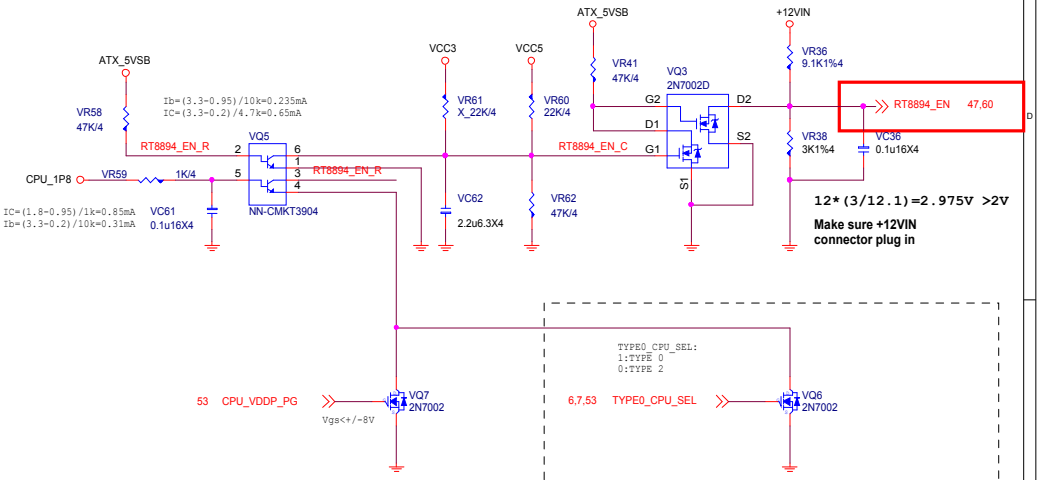
S5 PG



VRM_Enable circuit

2.0 update

remove D3



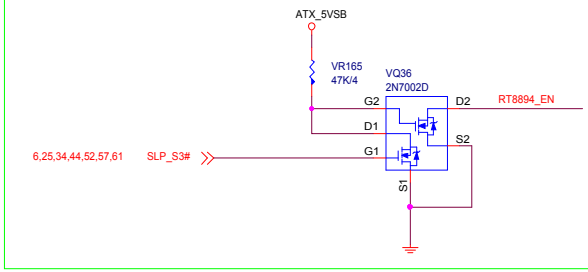
SPEC no Support

CPU VDDP NOT SUPPORT TYPE2

CPU VDDP NOT SUPPORT TYPE4

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0
MTS	4	1	1

2.0 update



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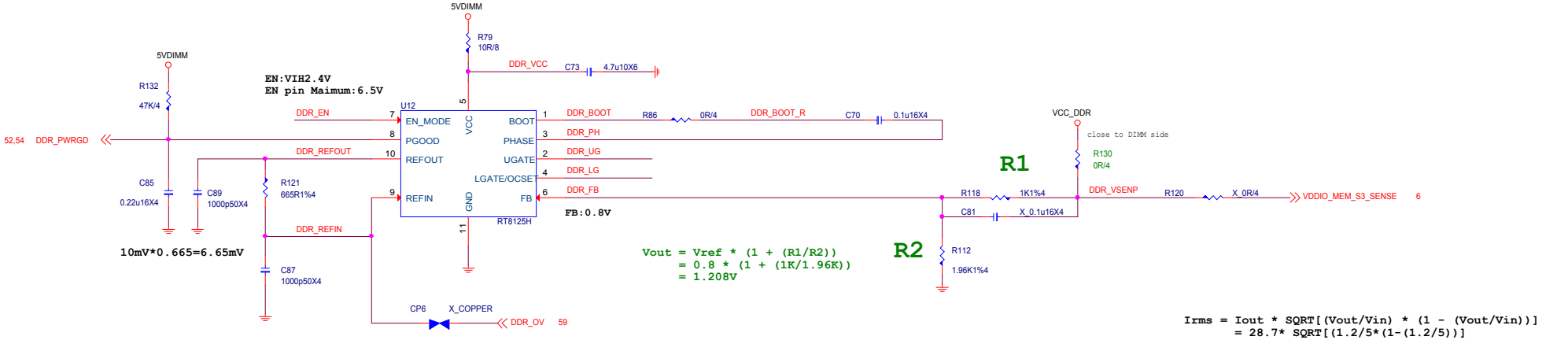
DDR4_1.2V@28.7A

18A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT

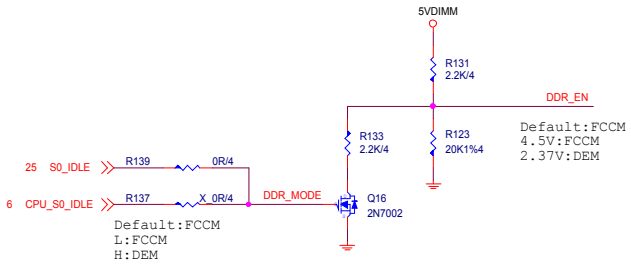
OCP = 35A; Choke Isat=42A

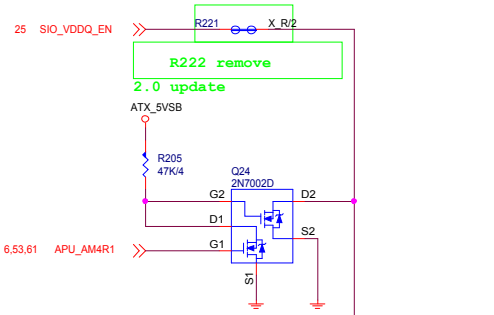
Rocset = 1.5 * Imax * Rdson(low) / Iocset
R649 = 1.5 * 28.7 * 2mohm / 10uA
R649 = 8.61K

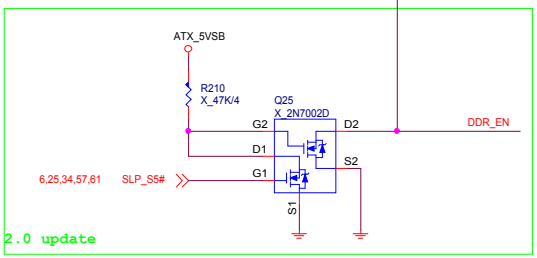
Rdson(Low Side) 5V
D03-4C02403-O05:3.3 ~ 4mohm

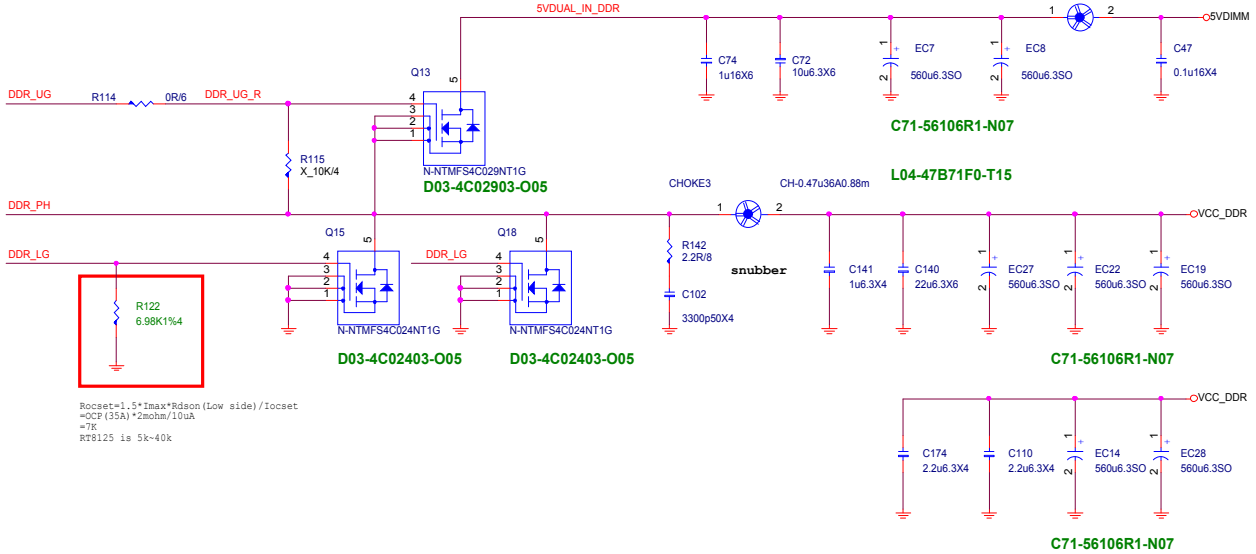


Irms = Iout * SQRT[(Vout/Vin) * (1 - (Vout/Vin))]
= 28.7* SQRT[(1.2/5*(1-(1.2/5))]
= 11.15A









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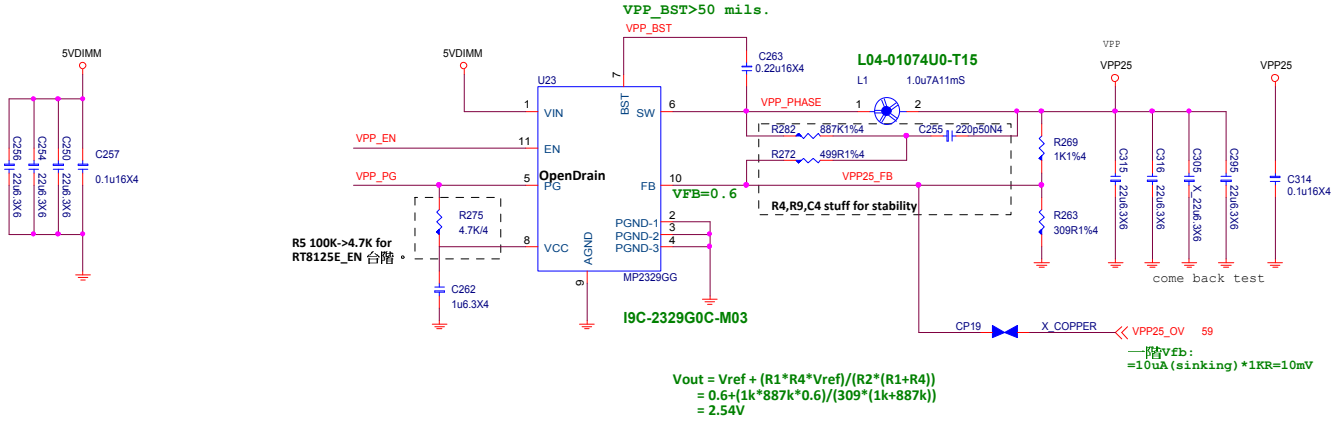
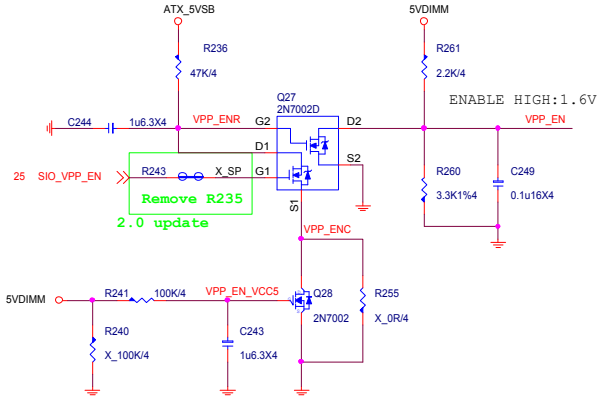
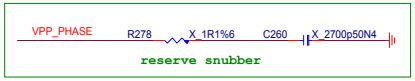
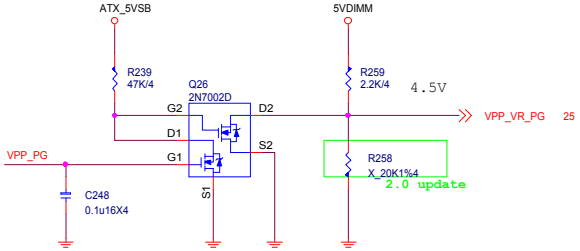
4DIMM : VPP25

2.5V@2.24A



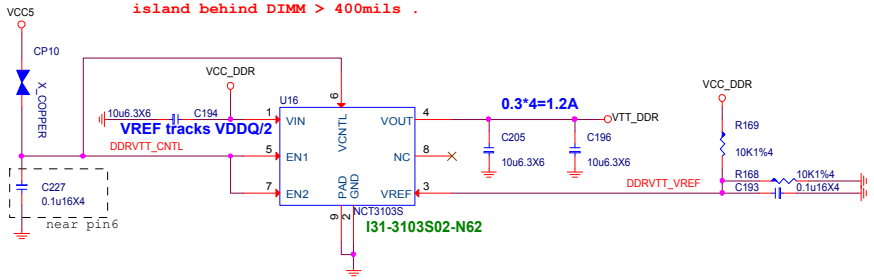


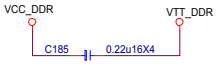




DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .





MICRO-STAR INT'L CO.,LTD

MS-7C95

Size	Document Description	Rev
Custom	55 DDR PWR - VPP25 / VTT	20

Date: Monday, May 11, 2020 Sheet 56 of 74

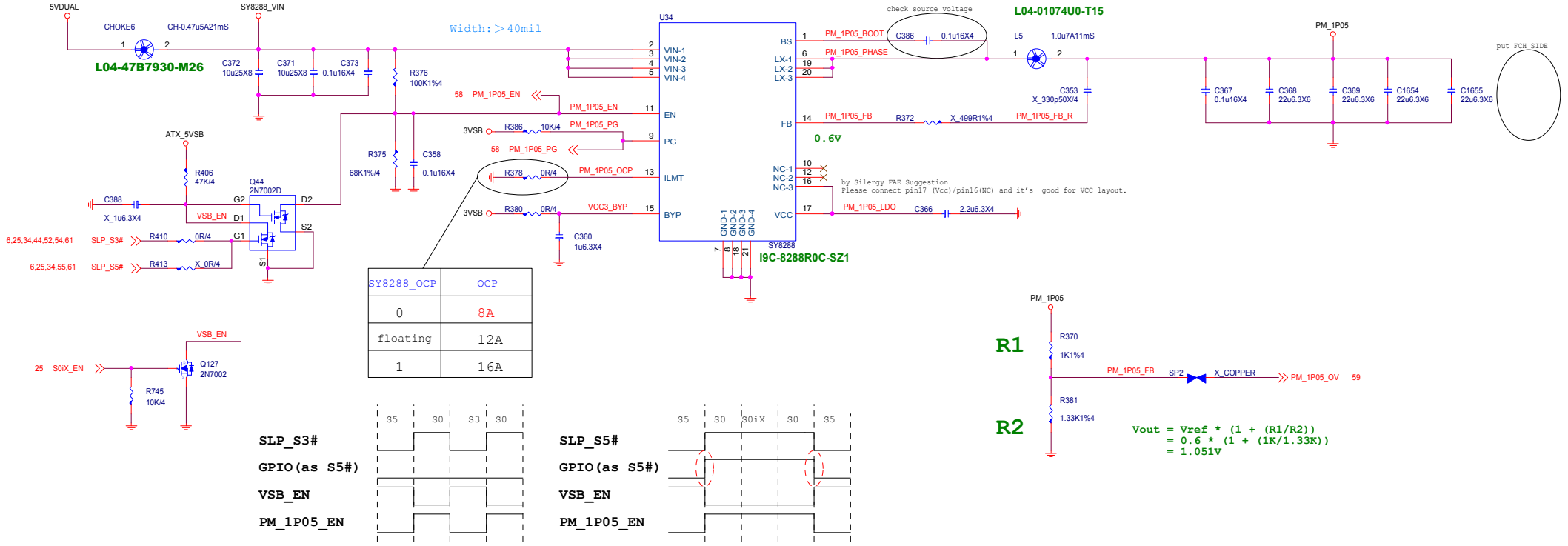
FOR Promontory 1.05V_S0

1.05V
S0:5.5A

Input Current= (8A*1.05V)/5V/0.85=1.976A

OCP=8A

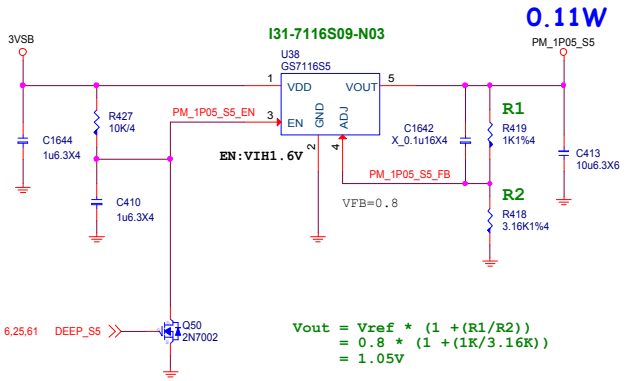
1.05V@5.5A



SY8288_OCP	OCP
0	8A
floating	12A
1	16A

FOR PROM PM_1P05_S5

1.05V@0.05A



MSI	MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: 56 PM - SY8288/PM_1P05		Rev: 20
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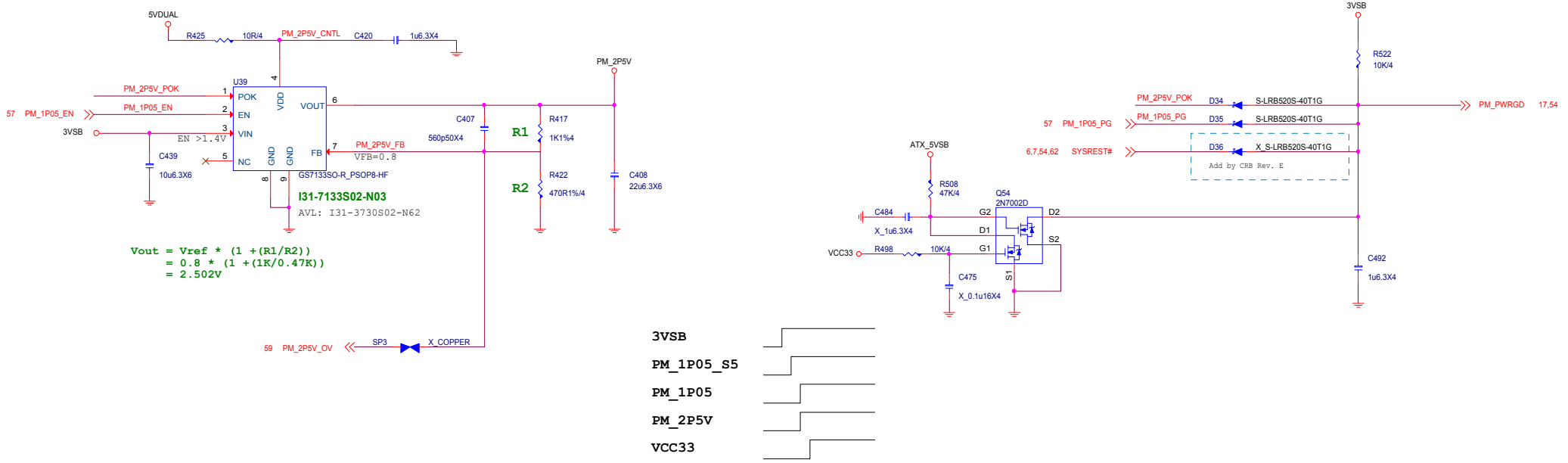
Promontory-2.5V

2.5V@900mA



3VSB

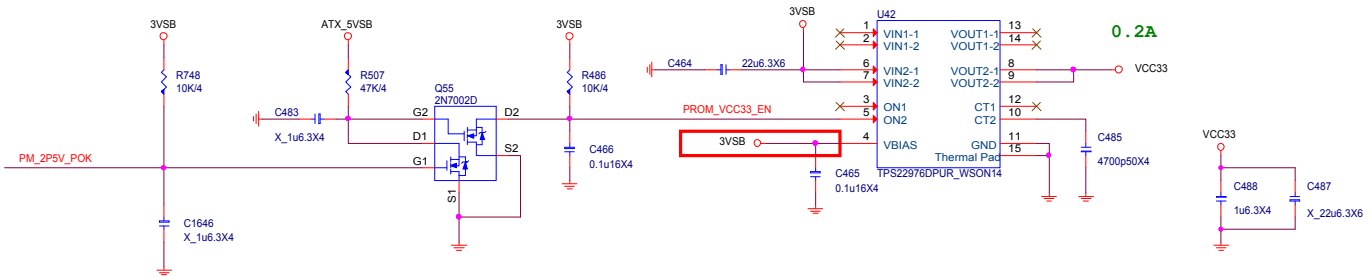
PM_1P05_S5

PM_1P05

PM_2P5V

VCC33

VCC33 VCC33@0.2A



Adijustable Rise Time
SR = 0.42*CT+66
SR is the slew rate in (μs/V)
CT is constant value on CT pin (in pF)
The units for the constant 66 is in (μs/V)

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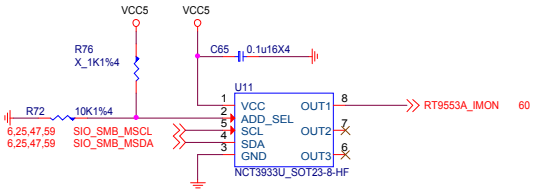
Over Voltage Control IC

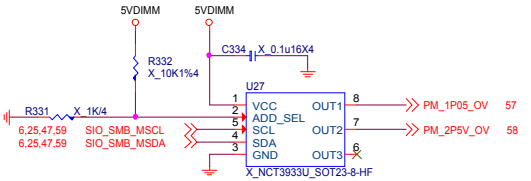
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

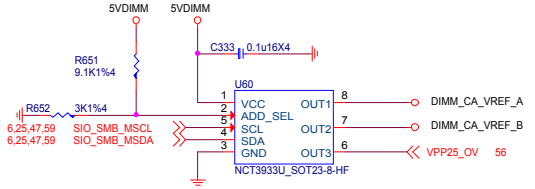
0x2A:RH=OPEN,RL=10K



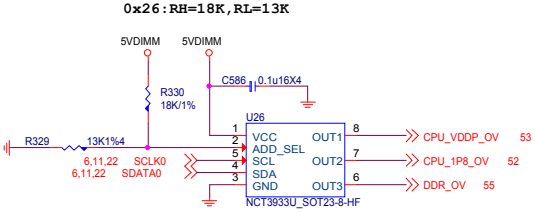
0x20:RH=10K,RL=OPEN



0x28:RH=9.1K,RL=3K



0x26:RH=18K,RL=13K



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Size: Custom	Document Description: 58 OV Control - NCT3933	Rev: 20
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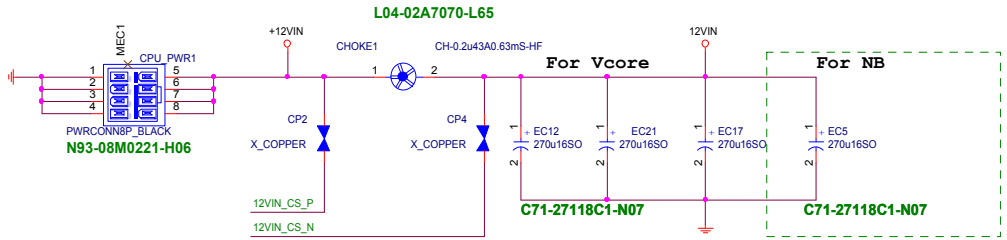
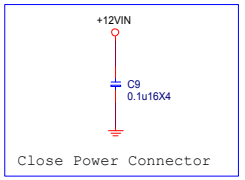
CPU POWER CONNECTOR

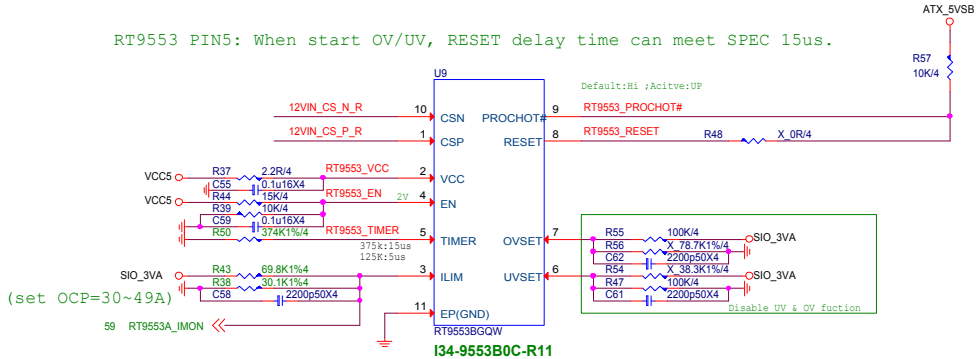


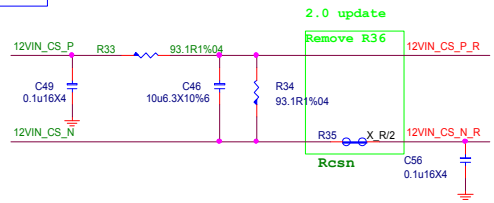
Vcore			
D=Vout/Vin			
Vin	= 12		> input voltage
Vout	= 2		> output Vcore
D	= 0.166667		
I o = Icore(max)*0.8			
I core(max)	= 200		> Vcore current
I avg.	= 160	A	
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	= 10	phase	
I ripple	= 5.962848	A	
How many pcs. Of Cap.			
I ripple(cap)	= 4700	m A	
COE TEMP	= 1		
Input Cap.	= 2	pcs.	

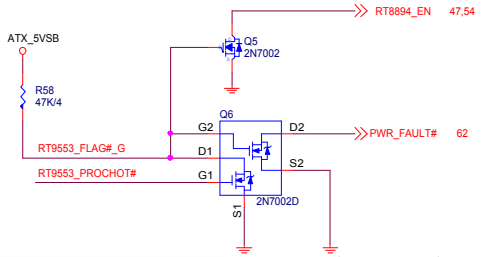
SOC			
D=Vout/Vin			
Vin	= 12		> input voltage
Vout	= 1.55		> output Vcore
D	= 0.129167		
I o = Icore(max)*0.8			
I core(max)	= 75		> Vcore current
I avg.	= 60	A	
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	= 2	phase	
I ripple	= 10.06153	A	
How many pcs. Of Cap.			
I ripple(cap)	= 4700	m A	
COE TEMP	= 1		
Input Cap.	= 3	pcs.	



RT9553B CURRENT SENSE







ΔVILIM=10uA*[(69.8K*30.1K)/(69.8K+30.1K)]
=210mV

Isense = VILIM / 100*Rsense
ΔIsense=210mV/(100*0.63m)=3.3333A

DCR Network				
Parameter	Value	Unit	Note	
C_real (Effective capacitance)	7	uF	Please note the effective capacitance must to consider de-rating.	
L_select	0.2	uH		
DCR_real	0.63	mΩ	Tolerance (±)	20
Current sense signal ratio (τ)	0.5			
R1_cal	90.70	Ω		
R2_cal	90.70	Ω		
R1_select	93.1	Ω	"R1_select" must > "R1_cal"	
R1_select range is ok or not	PASS			
R2_select	93.1	Ω		
R2_select range is ok or not	PASS			
Real current sense signal ratio (τ)	0.5			
Real time constant	1.0264275			
Temperature of L	25.00	℃	Consider DCR variation with temperatur	
DCR with Temperature	0.63	mΩ		
VCC	3.3	V		

OCP Trigger Level (Consider the external component variation)				
Parameter	Min	TYP	Max	Unit
VCC	NA	3.3	NA	V
OCP Trigger Level_set	30.21465202	38	49.70597583	A
ILIM_cal	NA	996.84	NA	mv
OCP error band_cal	-20.48775783	0	30.80519955	%
Roc1_cal	NA	69.79	NA	KΩ
Roc2_cal	NA	30.21	NA	KΩ
Roc1_select	NA	69.8	NA	KΩ
Roc2_select	NA	30.1	NA	KΩ
ILIM_real	NA	994.29	NA	mV
OCP Trigger Level_real	30.15	37.92	49.60	A
OCP error band_real	-20.49	0.00	30.81	%

MICRO-STAR INT'L CO.,LTD

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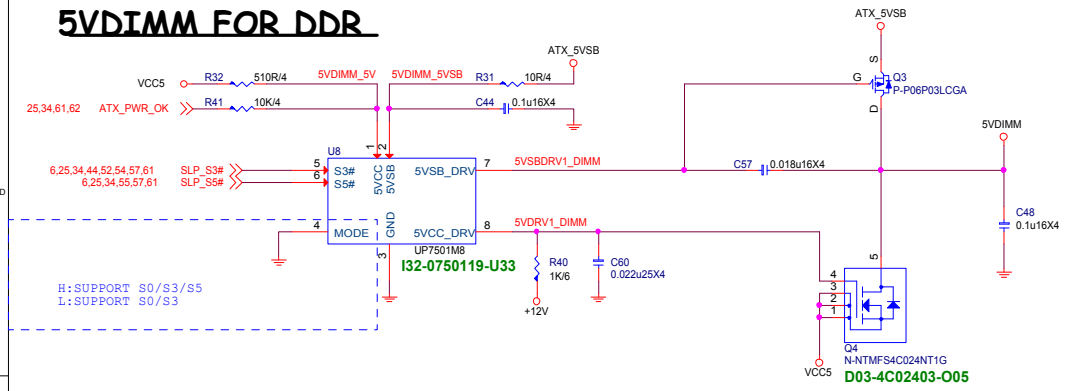
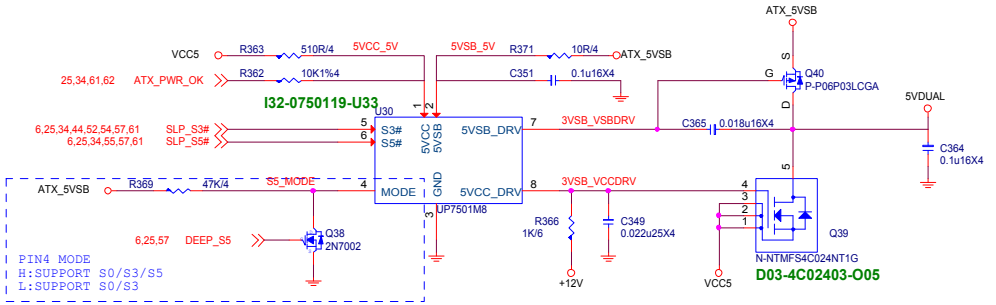
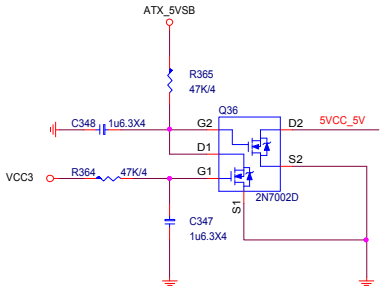
5VDIMM FOR DDR



S0IX

5VDUAL For 3VSB/CPU1.8V/VDDP



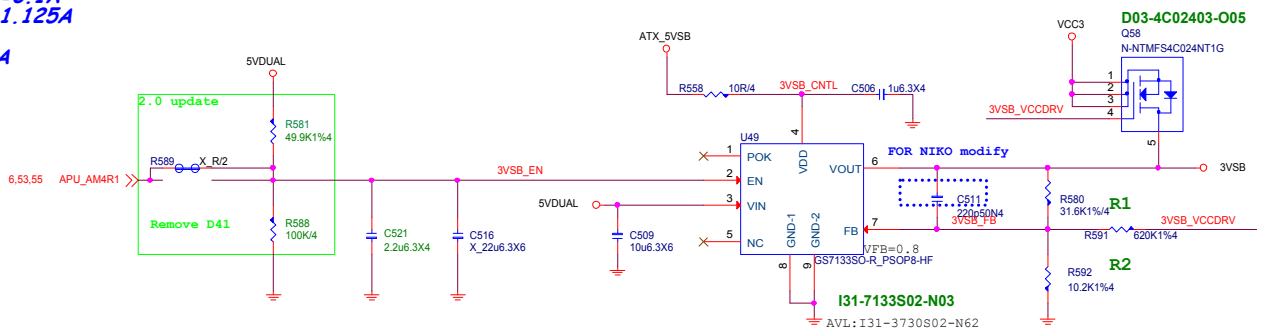


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

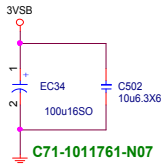
3VSB cost down

3.3V@2.32A

CPU:VDD_33_S5=0.25A
CHIP:VDD_33_S5=0.1A
*PCIE=(375mA*3)=1.125A*
M.2WIFI= 0.78A
RTL8111H=0.065A



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(31.6K/10.2K))
= 3.328V



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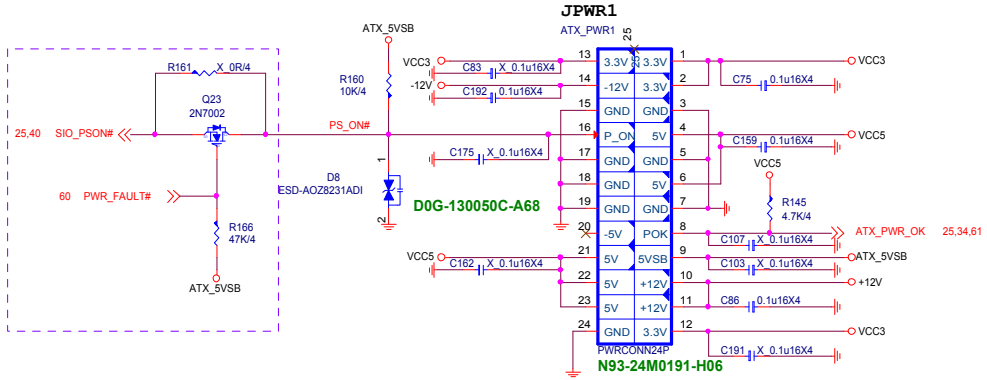
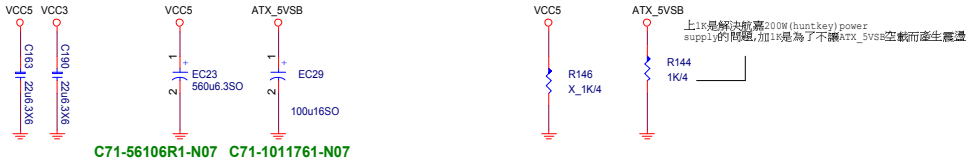
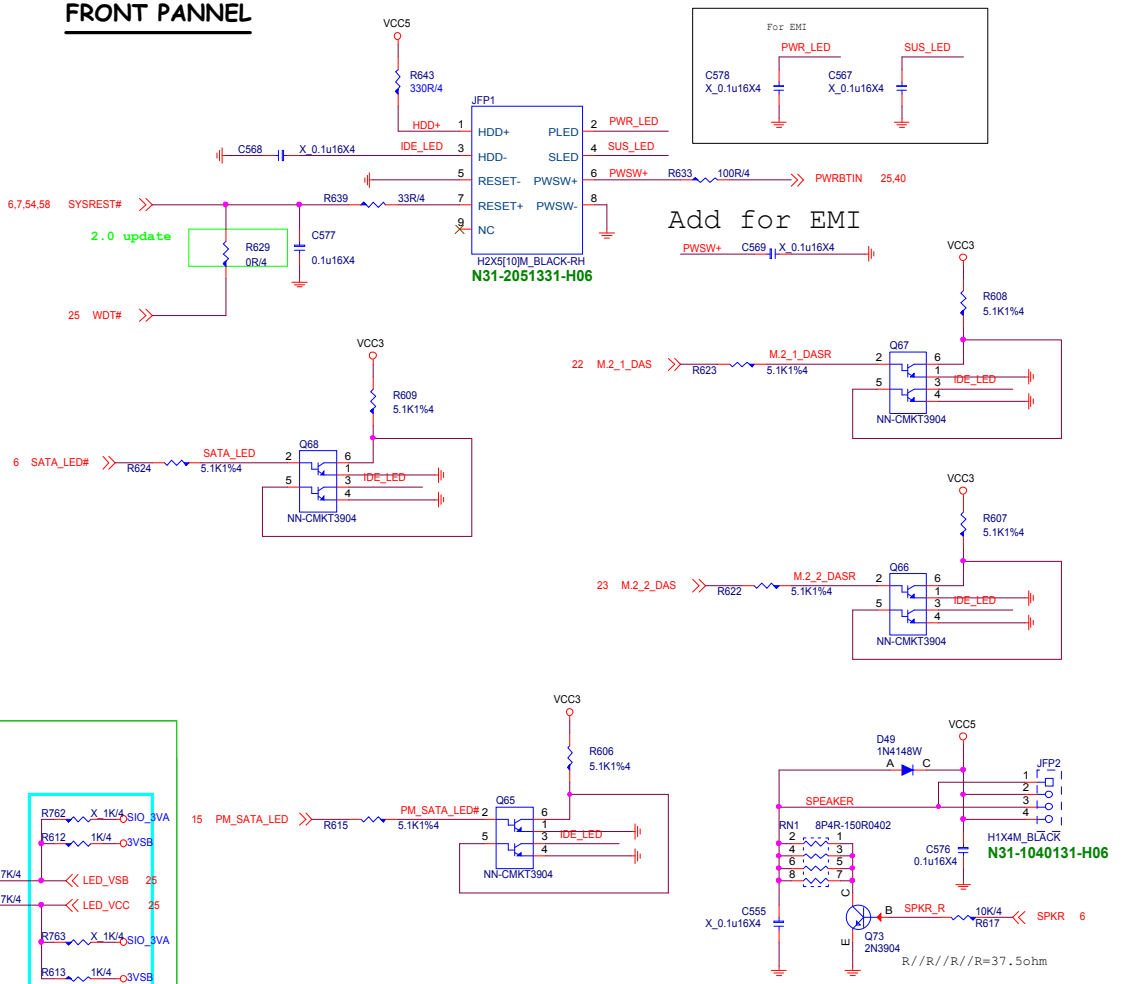
ATX POWER CONNECTOR



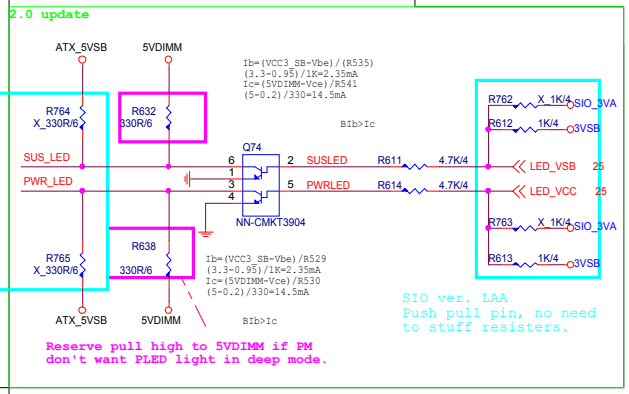


FRONT PANNEL



TPM

LED (for NCT6797D)



Voltage Mearsure Point

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	MS-7C95	
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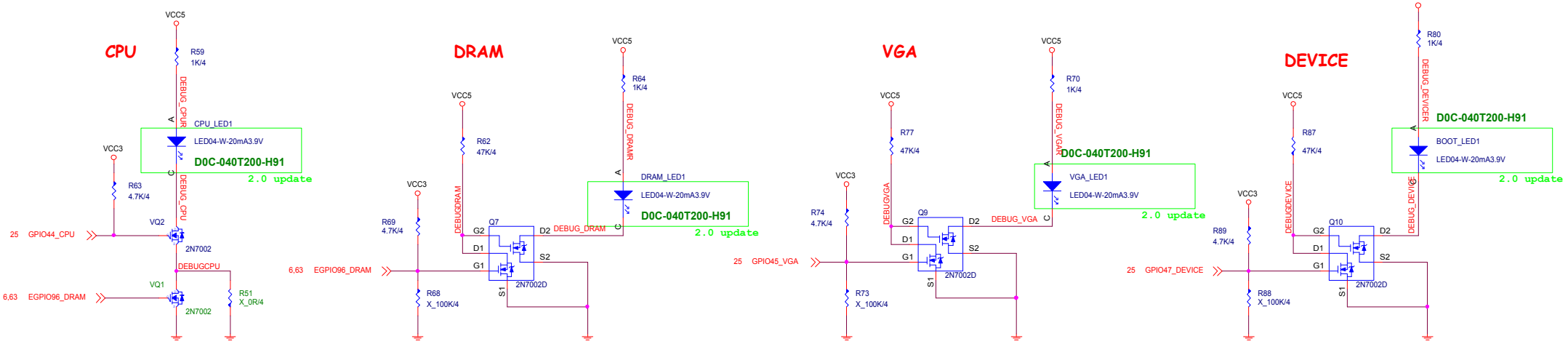
EZ Debug LED



LEDGPIO	GPIO46	EGPIO96	GPIO44	GPIO13
亮	OPEN-Drain	GPO LOW	GPO LOW	GPO LOW
滅	GPO LOW	GPO HIGH	OPEN-Drain	OPEN-Drain

default Input

LED亮燈時同時將CPU LED關掉

DIMM_SLOT FORM SIO

D0C-040P100-H91/D0C-040S500-E07

AMD AMP Detect LED

MICRO-STAR INT'L CO.,LTD

MS-7C95

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Custom	62 LED - EZ DEBUG / AMP	20

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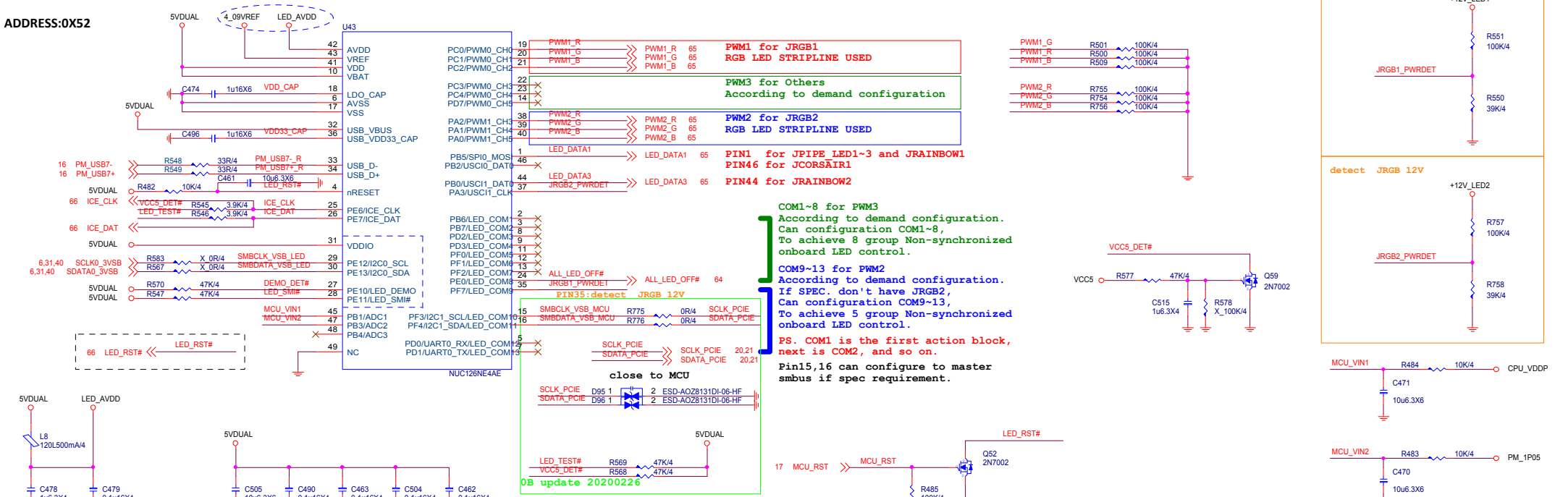
48 PIN LED MCU

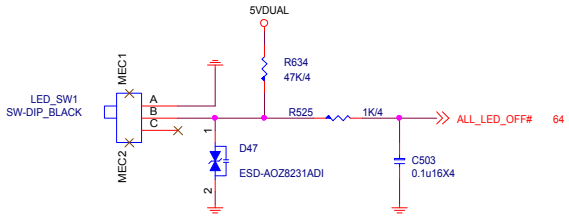
If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.

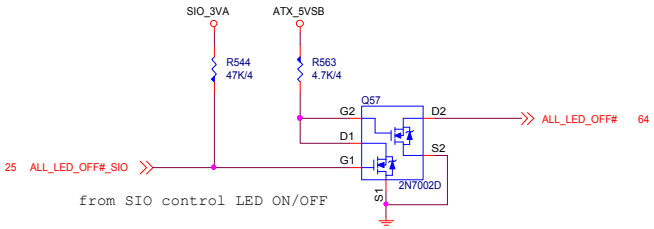
ADDRESS:0X52



LED_SW1 for ALL LED OFF

B-C: LED ON(default)
B-A: LED OFF





Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2

MICRO-STAR INT'L CO.,LTD

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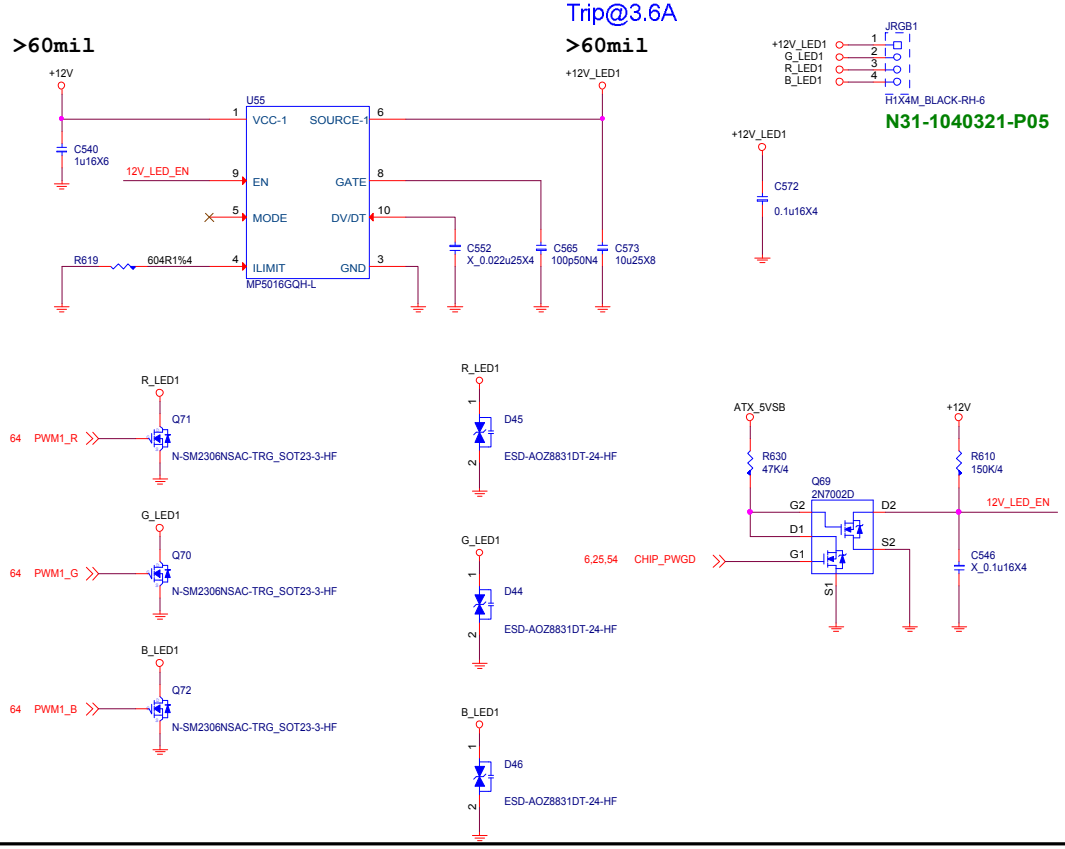
JRGB1

Trip@3.6A

>60mil

>60mil

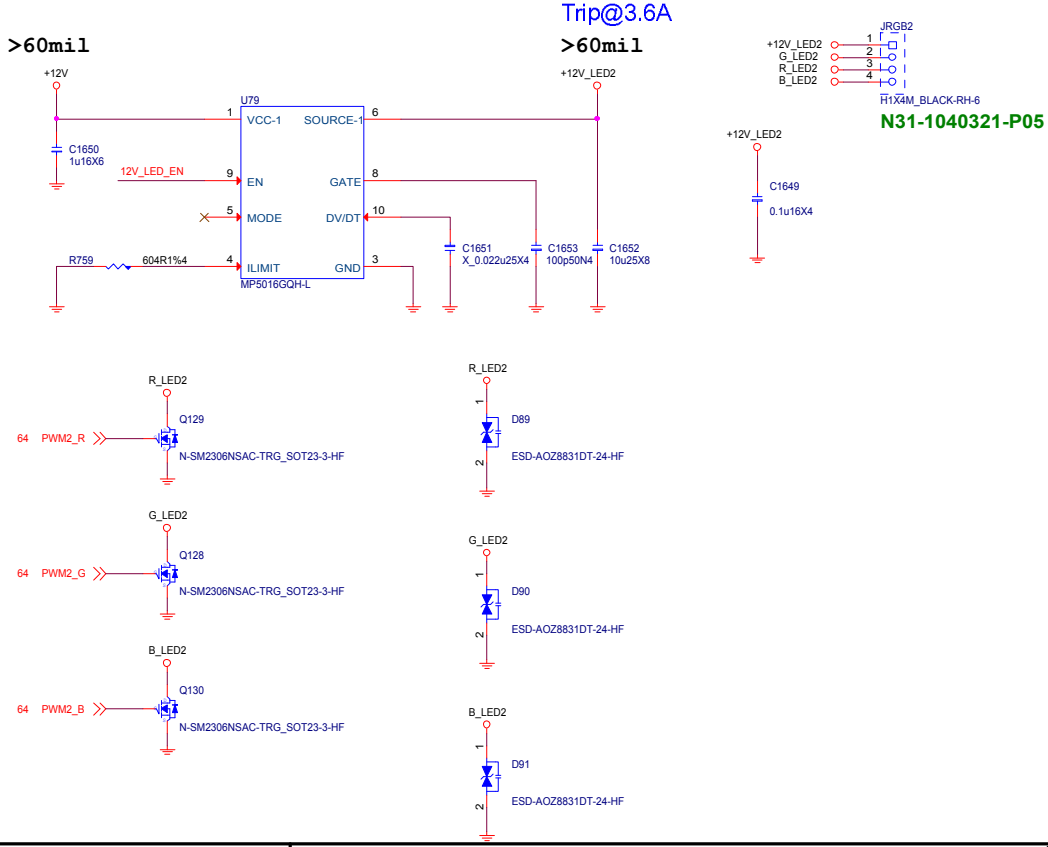


JRGB2

Trip@3.6A

>60mil

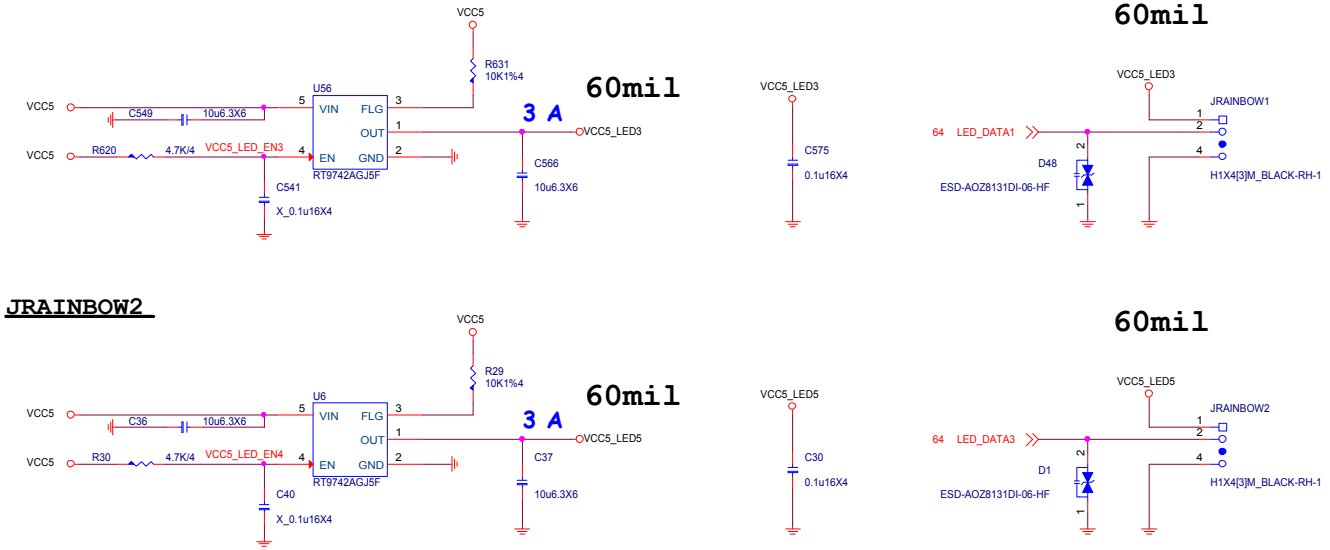
>60mil



JRAINBOW1

60mil

60mil



JRAINBOW2

60mil

60mil

JCORSAIR1

MICRO-STAR INT'L CO.,LTD

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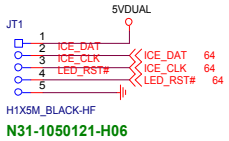
JT1 for FW update



EXTERNAL POWER INPUT

IF no JPWRLED1 & JPIPE_LED spec

MCU can powered by 5VDUAL directly.
LED_VCC5 replace with 5VDUAL.

JF1 for Factory test

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CPU Socket

CPU2

E95-0000022-A91

E95-0000022-A91

Simulation

X_JS2

SIM1

X_PIN1*2

X_JS1

SIM2

X_PIN1*2

FM6 FM8 FM5

X_FM120 X_FM120 X_FM120

FM2 FM1 FM3

X_FM120 X_FM120 X_FM120

FM4 FM7

X_FM120 X_FM120

Optics Orientation Holes

MH1 MH2 MH3

MH5 MH6

MH4 MH8 MH7

X_MH001

C508 0.1u16X4

C481 0.1u16X4

MANUAL PART

UEFI1

G51-M1SPXXA-A09

G51-M1SPXXA-A09

HDMI_LA1

Label

HDMI

HDMI LABEL

Y01-RHDMI03-000

BAT1_X1

BAT-BCR2032P

PCB

PCB

PCB1

7C95_20

2020/05/062020/05/13PD0-07C9520-G37,精成-深圳,1,微星_中和廠(MSI)4,black

PCH HEATSINK

MOS HEATSINK

1.0 update

HS_PCH1

MEC1 MEC1

MEC2 MEC2

HS-0410600-RH

HS_W1

MEC1 MEC1

MEC2 MEC2

HS-0507000-RH

DASH BOM

LAN99

LAN

X_RTL8111HN-CG-RH

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