RIYA Discrete Schematics Document

AMD Giffin CPU S1G2

VGA ATI M92S2-LP

RS780M + SB700

2009-08-25

REV : A00

DY : Nopop Component

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Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
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DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/08/22	A00	28	48	Change U4801 from 72.25X16.A01 to 72.25Q16.001		0909
		29	48	Del PWR_LED_B AFTE Pad,ADD AFTP5 test point to GND,move EC4802,EC4803		
						0903
						0903
						0903
						0903
						0903
						0903
						0908
						0908
						0908
						0908

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Title: Change List - Power

Size: Custom | Document Number: Riya Discrete | Rev: A00

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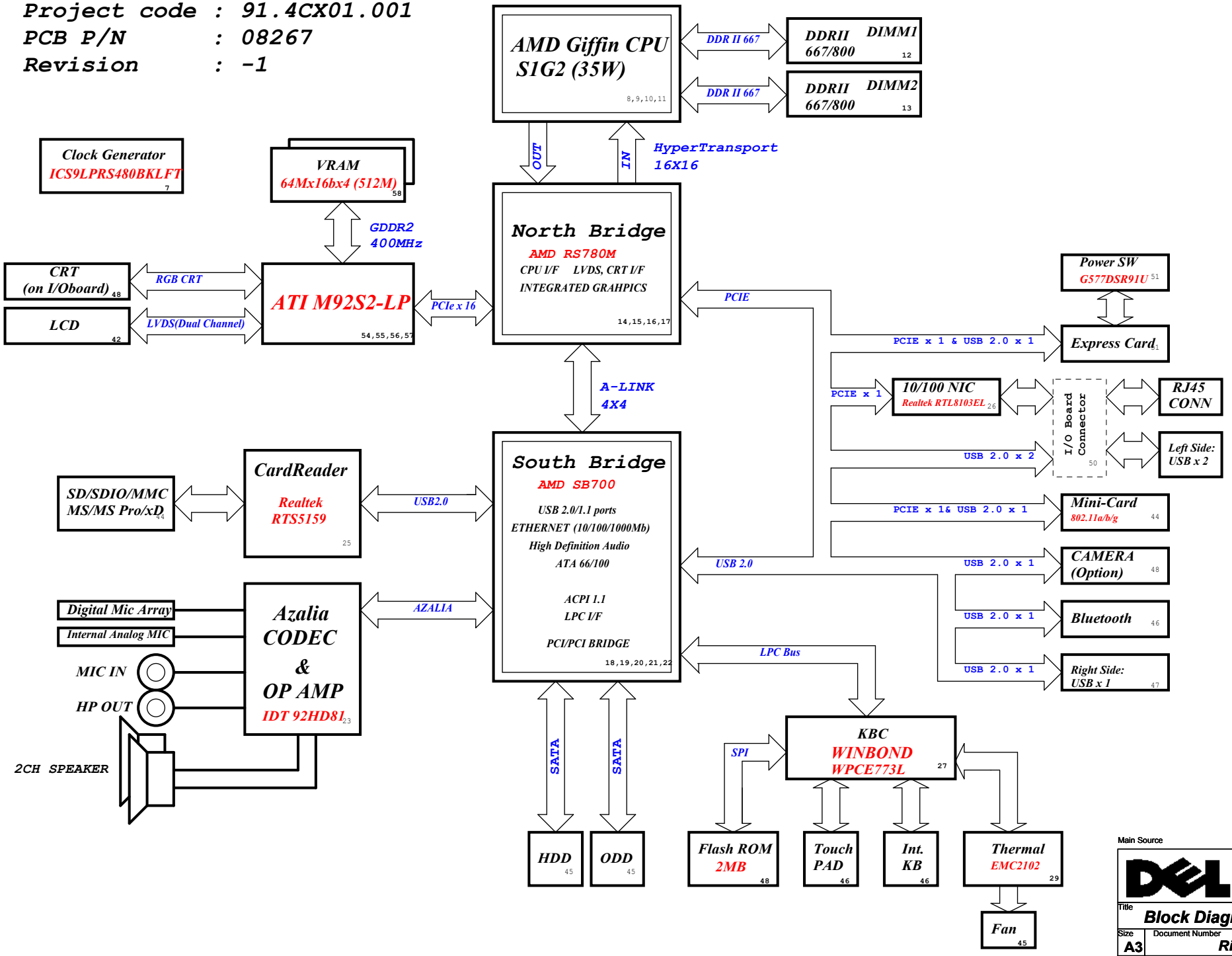
RIYA Discrete Block Diagram

Project code : 91.4CX01.001
PCB P/N : 08267
Revision : -1



CHARGER	
MAX8731AETI-GP	33
INPUTS	OUTPUTS
+DC_IN_SS +CHAGER_SRC	+PWR_SRC

SYSTEM DC/DC	
TPS51125RGER-GP	34
INPUTS	OUTPUTS
+PWR_SRC	+5V_AUX +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

AMD SB700 S5 POWER	
RT9013-12PB-GP	34
INPUTS	OUTPUTS
+3.3V_ALW	+1.2V_ALW

CPU CORE	
ISL6265AHRTZ-T-GP	35
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE0 +VCC_CORE1 +VDDNB

AMD RS780M CORE	
RT8209BGQW-GP	37
INPUTS	OUTPUTS
+PWR_SRC	+1.1V_RUN

AMD SB700 CORE	
RT8209BGQW-GP	38
INPUTS	OUTPUTS
+PWR_SRC	+1.2V_RUN

DDR II SUS&VTT	
RT8209BGQW-GP	39
INPUTS	OUTPUTS
+PWR_SRC	+1.8V_SUS

DDR II SUS&VTT	
TPS51100DGQR-GP	39
INPUTS	OUTPUTS
+1.8V_SUS	+0.9V_VTT

DDR II SUS&VTT	
TPS51100DGQR-GP	41
INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE

PCB LAYER
L1: Top
L2: GND
L3: Signal
L4: Signal
L5: VCC
L6: Signal
L7: GND
L8: Bottom

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Title: Block Diagram

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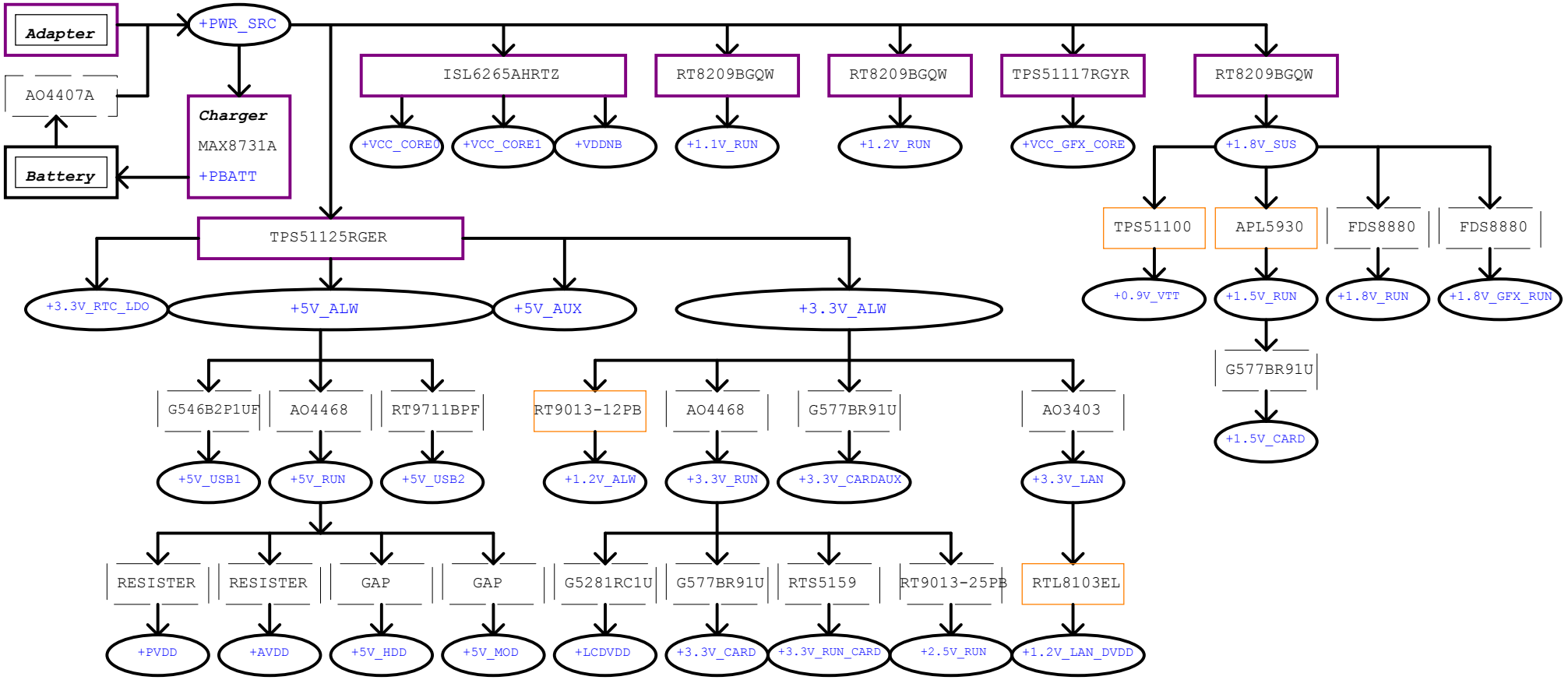
Power Block Diagram

Power Shape

Regulator | LDO | Switch



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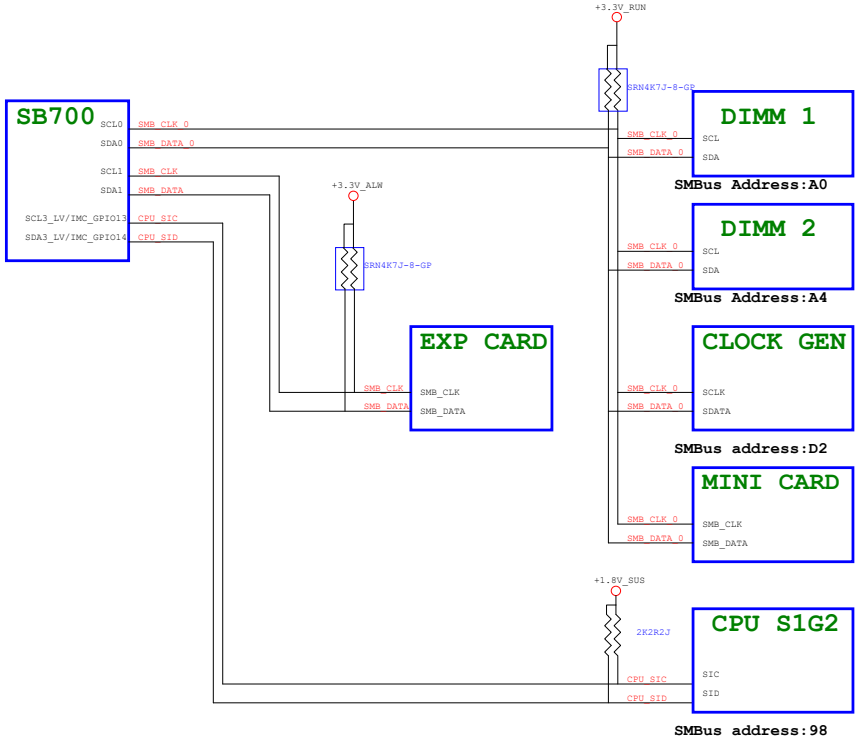
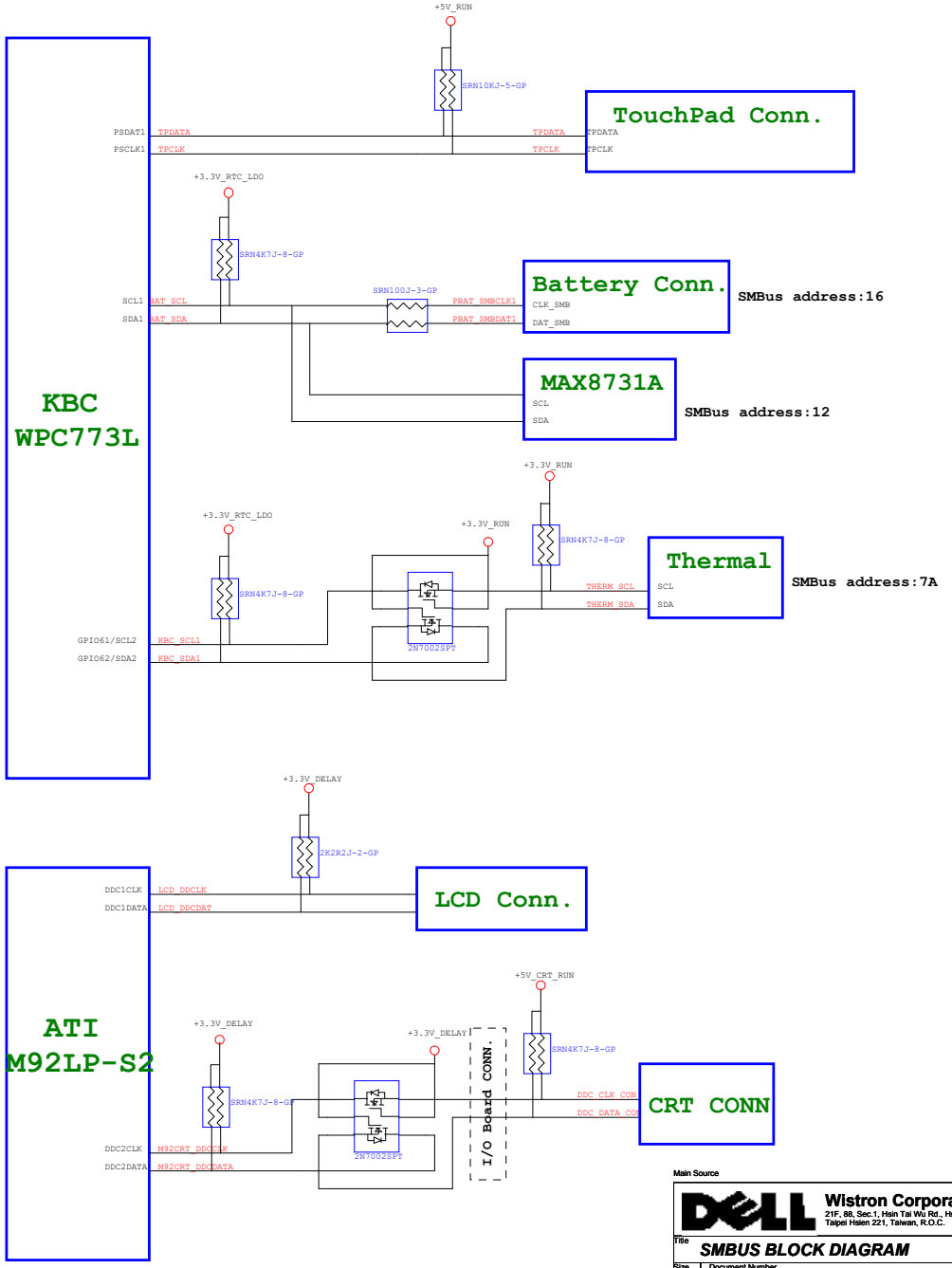
SB700 SMBus Block Diagram



KBC SMBus Block Diagram



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Title	SMBUS BLOCK DIAGRAM	
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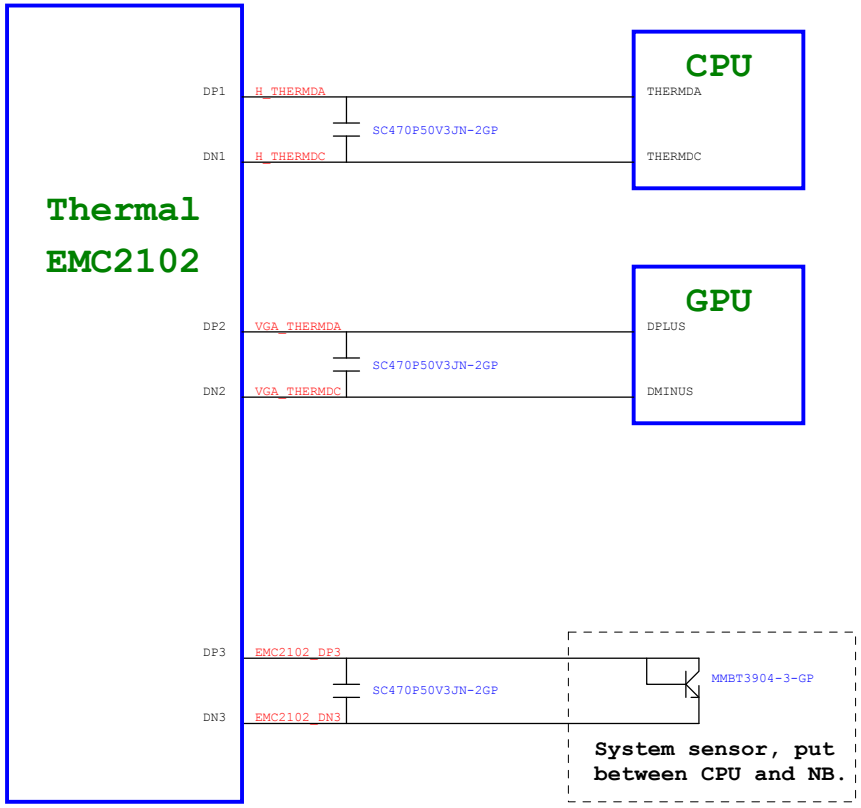
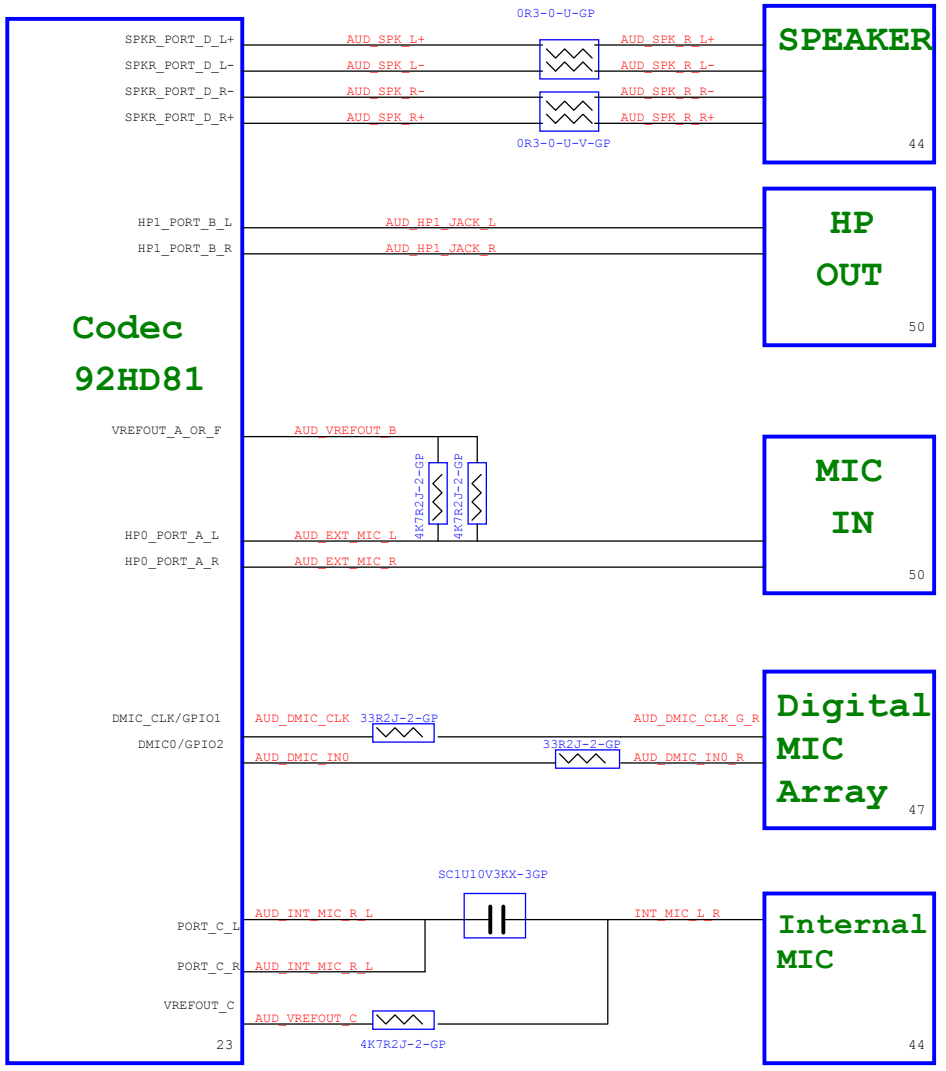
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM		
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SB700 MULTIFUNCTION and GPIO Definitions

SB700 45215_sb710_ds_nda Rev.1.05

MULTIFUNCTION PINS	FUNCTION	I/O	POWER DOMAIN
REQ3#/GPIO70	-	I/O	3.3V-5V_S0/15K PU
REQ4#/GPIO71	TP	I/O	3.3V-5V_S0/15K PU
GNT3#/GPIO72	-	I/O	3.3V-5V_S0
GNT4#/GPIO73	TP	I/O	3.3V-5V_S0
INTE#/GPIO33	-	I/O	3.3V-5V_S0/8.2K PU
INTF#/GPIO34	-	I/O	3.3V-5V_S0/8.2K PU
INTG#/GPIO35	-	I/O	3.3V-5V_S0/8.2K PU
INTH#/GPIO36	-	I/O	3.3V-5V_S0/8.2K PU
LDRQ1#/GNT5#/GPIO68	TP	I/O	3.3V-5V_S0/15K PU
BMREQ#/REQ5#/GPIO65	SB700_GPIO65	I/O	3.3V-5V_S0
PCI_PME#/GEVENT4#	TP	I/O	3.3V_S5/10K PU
RI#/EXTEVNT0#	KBC_ECSWI#	I/O	3.3V_S5/10K PU
SLP_S2/GPM9#	TP	I/O	3.3V_S5/10K PD
GA20IN/GEVENT0#	A20GATE	I/O	3.3V-5V_S0/8.2K PU
KBRST#/GEVENT1#	KBRCIN#	I/O	3.3V-5V_S0/8.2K PU
LPC_PME#/GEVENT3#	KBC_ECSCI#	I/O	3.3V_S5/10K PU
LPC_SMI#/EXTEVNT1#	TP	I/O	3.3V-5V_S0/8.2K PU
S3_STATE/GEVENT5#	-	I/O	3.3V_S5/10K PU
SYS_RESET#/GPM7#	TP	I/O	3.3V_S5/10K PU
WAKE#/GEVENT8#	PCIE_WAKE#	I/O	3.3V_S5/10K PU
BLINK/GPM6#	KBC_ECSMI#	I/O	3.3V_S5/10K PU
SMBALERT#/THRMTRIP#/GEVENT2#	SB_THERMTRIP#	I/O	3.3V_S5/10K PU
SATA_IS0#/GPIO10	TP	I/O	3.3V-5V_S0
CLK_REQ3#/SATA_IS1#/GPIO6	TP	I/O	3.3V-5V_S0
SMARTVOLT/SATA_IS2#/GPIO4	TP	I/O	3.3V-5V_S0
CLK_REQ0#/SATA_IS3#/GPIO0	TP	I/O	3.3V-5V_S0/10K PD
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39	TP	I/O	3.3V-5V_S0/10K PD
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40	TP	I/O	3.3V-5V_S0/10K PD
SPKR/GPIO2	SB_SPKR	I/O	3.3V-5V_S0
SCL0/GPOC0#	TP	I/O	3.3V-5V_S0
SDA0/GPOC1#	TP	I/O	3.3V-5V_S0
SCL1/GPOC2#	SMB_CLK	I/O	3.3V_S5
SDA1/GPOC3#	SMB_DATA	I/O	3.3V_S5
DDC1_SCL/GPIO9	TP	I/O	3.3V-5V_S0
DDC1_SDA/GPIO8	TP	I/O	3.3V-5V_S0
LLB#/GPIO66	TP	I/O	3.3V_S5/10K PU
SHUTDOWN#/GPIO5	TP	I/O	3.3V-5V_S0
DDR3_RST#/GEVENT7#	-	I/O	3.3V_S5/10K PU
USB_OC6#/IR_TX1/GEVENT6#	TP	I/O	3.3V_S5/10K PU
USB_OC5#/IR_TX0/GPM5#	TP	I/OD	3.3V_S5
USB_OC4#/IR_RX0/GPM4#	CPPE#	I/O	3.3V_S5/10K PU
USB_OC3#/IR_RX1/GPM3#	TP	I/O	3.3V_S5/10K PU
USB_OC2#/GPM2#	TP	I/O	3.3V_S5/10K PU
USB_OC1#/GPM1#	USB_OC_2_#	I/O	3.3V_S5/10K PU
USB_OC0#/GPM0#	USB_OC_01_#	I/O	3.3V_S5/10K PU
SCL0/GPOC0#	TP	I/O	3.3V-5V_S0
SDA0/GPOC1#	TP	I/O	3.3V-5V_S0
SCL1/GPOC2#	SMB_CLK	I/O	3.3V_S5
SDA1/GPOC3#	SMB_DATA	I/O	3.3V_S5
AZ_SDIN0/GPIO42	SB_AZ_CODEC_SDIN0	I/O	3.3V_S5/50K PD
AZ_SDIN1/GPIO43	-	I/O	3.3V_S5/50K PD
AZ_SDIN2/GPIO44	-	I/O	3.3V_S5/50K PD
AZ_SDIN3/GPIO46	-	I/O	3.3V_S5/50K PD
AZ_DOCK_RST#/GPM8#	-		10K PU
SPI_CS2#/IMC_GPIO2	TP	I/O	3.3V_S5/10K PU
IDE_RST#/F_RST#/IMC_GPO3	IDE_RST#	OD	3.3V-5V_S5
IMC_GPIO4	TP	I/O	3.3V-5V_S5
IMC_GPIO5	TP	I/O	3.3V-5V_S5
IMC_GPIO6	TP	I/O	3.3V-5V_S5
IMC_GPIO7	TP	I/O	3.3V-5V_S5
IMC_GPIO8	-	I/O	3.3V_S5
IMC_GPIO9	-	I/O	3.3V_S5
IMC_PWM0/IMC_GPIO10	-	I/O	3.3V_S5
SCL2/IMC_GPIO11	-	OD	3.3V-5V_S5
SDA2/IMC_GPIO12	-	OD	3.3V-5V_S5
SCL3_LV/IMC_GPIO13	CPU_SIC	OD	3.3V_S5
SDA3_LV/IMC_GPIO14	CPU_SID	OD	3.3V_S5
IMC_PWM1/IMC_GPIO15	-	I/O	3.3V_S5
IMC_PWM2/IMC_GPO16	SB_GPO16	I/O	3.3V-5V_S5
IMC_PWM3/IMC_GPO17	SB_GPO17	I/O	3.3V-5V_S5
IMC_GPIO18	-	I/O	3.3V_S5
IMC_GPIO19	-	I/O	3.3V_S5
IMC_GPIO20	-	I/O	3.3V_S5
IMC_GPIO21	-	I/O	3.3V_S5

SB700 45215_sb710_ds_nda Rev.1.05

MULTIFUNCTION PINS	FUNCTION	I/O	POWER DOMAIN
IMC_GPIO22	-	I/O	3.3V_S5
IMC_GPIO23	-	I/O	3.3V_S5
IMC_GPIO24	-	I/O	3.3V_S5
IMC_GPIO25	-	I/O	3.3V_S5
IMC_GPIO26	-	I/O	
IMC_GPIO27	-	I/O	3.3V_S5
IMC_GPIO28	-	I/O	3.3V_S5
IMC_GPIO29	-	I/O	3.3V_S5
IMC_GPIO30	-	I/O	3.3V_S5
IMC_GPIO31	-	I/O	3.3V_S5
IMC_GPIO32	-	I/O	3.3V_S5
IMC_GPIO33	-	I/O	3.3V_S5
IMC_GPIO34	-	I/O	3.3V_S5
IMC_GPIO35	-	I/O	3.3V_S5
IMC_GPIO36	-	I/O	3.3V_S5
IMC_GPIO37	-	I/O	3.3V_S5
IMC_GPIO38	-	I/O	3.3V_S5
IMC_GPIO39	-	I/O	3.3V_S5
IMC_GPIO40	-	I/O	3.3V_S5
IMC_GPIO41	-	I/O	3.3V_S5
SATA_ACT#/GPIO67	TP	I/O	
IDE_D0/GPIO15	-	I/O	
IDE_D1/GPIO16	-	I/O	
IDE_D2/GPIO17	-	I/O	
IDE_D3/GPIO18	-	I/O	
IDE_D4/GPIO19	-	I/O	
IDE_D5/GPIO20	-	I/O	
IDE_D6/GPIO21	-	I/O	
IDE_D7/GPIO22	-	I/O	
IDE_D8/GPIO23	-	I/O	
IDE_D9/GPIO24	-	I/O	
IDE_D10/GPIO25	-	I/O	
IDE_D11/GPIO26	-	I/O	
IDE_D12/GPIO27	-	I/O	
IDE_D13/GPIO28	-	I/O	
IDE_D14/GPIO29	-	I/O	
IDE_D15/GPIO30	-	I/O	
SPI_DI/GPIO12	TP	I/O	3.3V_S5/10K PD
SPI_DO/GPIO11	TP	I/O	3.3V_S5/10K PD
SPI_CLK/GPIO47	TP	I/O	3.3V_S5/10K PD
SPI_HOLD#/GPIO31	TP	I/O	3.3V_S5/10K PU
SPI_CS#/GPIO32	TP	I/O	3.3V_S5/10K PU
LAN_RST#/GPIO13	TP	I/O	3.3V-5V_S0
ROM_RST#/GPIO14	TP	I/O	3.3V-5V_S0
FANOUT0/GPIO3	TP	I/O	3.3V-5V_S0/8.2K PU
FANOUT1/GPIO48	SB_GPIO48	I/O	3.3V-5V_S0/8.2K PU
FANOUT2/GPIO49	TP	I/O	3.3V-5V_S0/8.2K PU
FANIN0/GPIO50	-	I/O	3.3V-5V_S0
FANIN1/GPIO51	TP	I/O	3.3V-5V_S0
FANIN2/GPIO52	TP	I/O	3.3V-5V_S0
TEMPIN0/GPIO61	TP	I/O	3.3V_S5
TEMPIN1/GPIO62	-	I/O	3.3V_S5
TEMPIN2/GPIO63	-	I/O	3.3V_S5
TEMPIN3/TALERT#/GPIO64	TALERT#	I/O	3.3V_S5
VIN0/GPIO53	-	I/O	3.3V_S5
VIN1/GPIO54	-	I/O	3.3V_S5
VIN2/GPIO55	-	I/O	3.3V_S5
VIN3/GPIO56	-	I/O	3.3V_S5
VIN4/GPIO57	-	I/O	3.3V_S5
VIN5/GPIO58	-	I/O	3.3V_S5
VIN6/GPIO59	-	I/O	3.3V_S5
VIN7/GPIO60	-	I/O	3.3V_S5

WPCE773L MULTIFUNCTION and GPIO Definitions

WPCE773L Preliminary Datasheet - Revision 0.8

MULTIFUNCTION PINS	FUNCTION	I/O	POWER DOMAIN
GPIO01/TB2	PM_SLP_S3#	I/O	3.3V-5V_AUX
GPIO03	KBC_PWRBTN#	I/O	3.3V_AUX
GPIO04	SYS_THERMTRIP#	I/O	3.3V_AUX
GPIO05	LCD_EC_DET	I/O	3.3V_AUX
GPIO06	AC_IN#	I/O	3.3V-5V_AUX
GPIO07	LID_CLOSE#	I/O	3.3V_AUX
GPIO10/LPCPD#	ADAPT_TRIP_SEL	I/O	3.3V-5V_AUX
GPIO11/CLKRUN#	PM_CLKRUN#	I/O	3.3V-5V_AUX
GPIO12/PSDAT3	KB_DET#	I/O	3.3V-5V_AUX
GPIO13/C_PWM	BRIGHTNESS	I/O	3.3V-5V_AUX
GPIO14/TB1	PSID_EC	I/O	3.3V-5V_AUX
GPIO15/A_PWM	KBC_BEEP	I/O	3.3V-5V_AUX
GPIO16	PM_LAN_ENABLE	I/O	3.3V-5V_AUX
GPIO17/SCL1	BAT_SCL	I/O	3.3V-5V_AUX
GPIO20/TA2	PM_PWRBTN#	I/O	3.3V-5V_AUX
GPIO21/B_PWM	BATLOW_LED	I/O	3.3V-5V_AUX
GPIO22/SDA1	BAT_SDA	I/O	3.3V-5V_AUX
GPIO23	1.8V_GFX_RUN_PWRGD#	I/O	3.3V-5V_AUX
GPIO25/PSCLK3	LCD_CBL_DET#	I/O	3.3V-5V_AUX
GPIO26/PSCLK2	LCD_TST	I/O	3.3V-5V_AUX
GPIO30	EC_SPI_WP#_R	I/O	3.3V-5V_AUX
GPIO31	RUNPWROK	I/O	3.3V-5V_AUX
GPIO32/D_PWM	PWRLED	I/O	3.3V-5V_AUX
GPIO33/H_PWM	HP_MUTE	I/O	3.3V-5V_AUX
GPIO35/PSDAT1	TPDATA	I/O	3.3V-5V_AUX
GPIO36	S5_ENABLE	I/O	3.3V-5V_AUX
GPIO37/PSCLK1	TPCLK	I/O	3.3V-5V_AUX
GPIO40/F_PWM	3.3V_DELAY_EN	I/O	3.3V-5V_AUX
GPIO41	BAT_IN#	I/O	3.3V-5V_AUX
GPIO42/TCK	AD_OFF	I/O	3.3V-5V_AUX
GPIO43/TMS	KBC_RSMRST#	I/O	3.3V-5V_AUX
GPIO44/TDI	PM_SLP_S5#	I/O	3.3V-5V_AUX
GPIO45/E_PWM	KBC_PLTRST_DELAY#	I/O	3.3V-5V_AUX
GPIO46/TRST#	3V_5V_POK	I/O	3.3V-5V_AUX
GPIO50/TDO	PSID_DISABLE#	I/O	3.3V-5V_AUX
GPIO52/RDY#	BLON_OUT	I/O	3.3V-5V_AUX
ECSCI#/GPIO54	KBC_D_ECSCI#	I/O	3.3V-5V_AUX
GPIO55/CLKOUT	AMP_MUTE#	I/O	3.3V_AUX
GPIO56/TA1	LCD_TST_EN	I/O	3.3V-5V_AUX
GPIO65/SMI#	PANEL_BKEN	I/O	3.3V-5V_AUX
GPIO66/G_PWM	1.8V_GFX_RUN_EN	I/O	3.3V-5V_AUX
GPIO67/PWUREQ#	KBC_D_ECSWI#	I/O	3.3V-5V_AUX
GPIO70	KBC_D_ECSMI#	I/O	3.3V-5V_AUX
GPIO71	GFX_CORE_EN	I/O	3.3V-5V_AUX
GPIO73/SCL2	KBC_SCL1	I/O	3.3V-5V_AUX
GPIO74/SDA2	KBC_SDA1	I/O	3.3V-5V_AUX
GPIO75	WIFI_RF_EN	I/O	3.3V-5V_AUX
GPIO76/SHBM	KBC_SHBM	O	3.3V-5V_AUX
GPIO77	BLUETOOTH_EN	I/O	3.3V-5V_AUX
GPIO81	1.1V_GFX_RUN_EN	I/O	3.3V-5V_AUX
GP82/TRIS#	USB_PWR_EN#	O	3.3V-5V_AUX
GP83/SOUT_CR/BADDR1	E51_TxD	O	3.3V-5V_AUX
GPIO87/SIN_CR	E51_RxD	I/O	3.3V-5V_AUX
GPI90/AD0	AD_IA	I	3.3V_AUX
GPI92/AD2	THERMTRIP_VGA#	I	3.3V_AUX
GPI93/AD3	ADAPT_OC	I	3.3V_AUX
GPI94	PCB_VER0	I	3.3V_AUX
GPI95	PCB_VER1	I	3.3V_AUX
GPI96	PCB_VER2	I	3.3V_AUX
GPI97	CAMERA_DET#	I	3.3V_AUX

USB Table

Pair	Controllers		Device
0	EHCI Dev.19	OHCI 0	I/O BOARD Left Side
1			I/O BOARD Left Side
2			Camera
3		OHCI 1	RESERVED
4			Express Card
5			RESERVED
6	EHCI Dev.18	OHCI 0	BLUETOOTH
7			RESERVED
8			RESERVED
9		OHCI 1	Card Reader
10			MINI CARD
11			USB Port Right Side
12	OHCI Dev.20		RESERVED
13			RESERVED

PCIE Routing

Pair	Device
PE_GPP1	LAN
PE_GPP2	MINI Card
PE_GPP3	EXP Card

CIRCUIT NOTE

For Circuit

For Layout

For EMI

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Table of Content

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SSID = CLOCK

1'nd 68.00084.A31(MURATA)
2'nd

+3.3V_CLK_VDD (40 mils)

A00
8/24
Change R701,R702,R704 from 0 ohm to short pad

X01
04/15 Add
1.Add EC703 For EMI

XTAL
1'nd 82.30005.901
2'nd 82.30005.A51

X01
04/08 modify
1.Change Clk gen,Mini Card SMBus from Ch1 to Ch0

X01
03/31 modify
1.Change R709/R710 from 33 ohm to 22 ohm

71.08628.003

A00
08/22 modify
change U702 to 71.08628.003.
2nd source is 71.09480.A03

CLKREQ# MAP

CLKREQ0#	No use
CLKREQ1#	CLKSRC1 MINI1
CLKREQ2#	CLKSRC2 EXPCARD
CLKREQ3#	No use
CLKREQ4#	No use

NBGPP(100MHz)
WLAN(100MHz)
EXP(100MHz)
LAN(100MHz)
VGA(27MHz)
VGA(100MHz)
CPU_CLK(200MHz)
CardReader(48MHz)
SB700_USB(48MHz)
NB OSCIN(14MHz)
SB OSCIN(14MHz)
For EMI

	OSC_14M_NB
RS780M	1.1V 158R/90.9R

SB TYPE	R716
*SB700	EMPTY
SB710	STUFF

*DEFAULT

NB ALINK (100MHz)
SB PCIE (100MHz)
VGA M92 (27MHz)

SEL_HTT66 FS0	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA FS1	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27MHz FS2	1*	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0	100MHz differential spreading SRC clock

* default

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator ICS9LPRS480
Size: Custom | Document Number: Riya Discrete | Rev: A00
Date: Tuesday, August 25, 2009 | Sheet 7 of 65

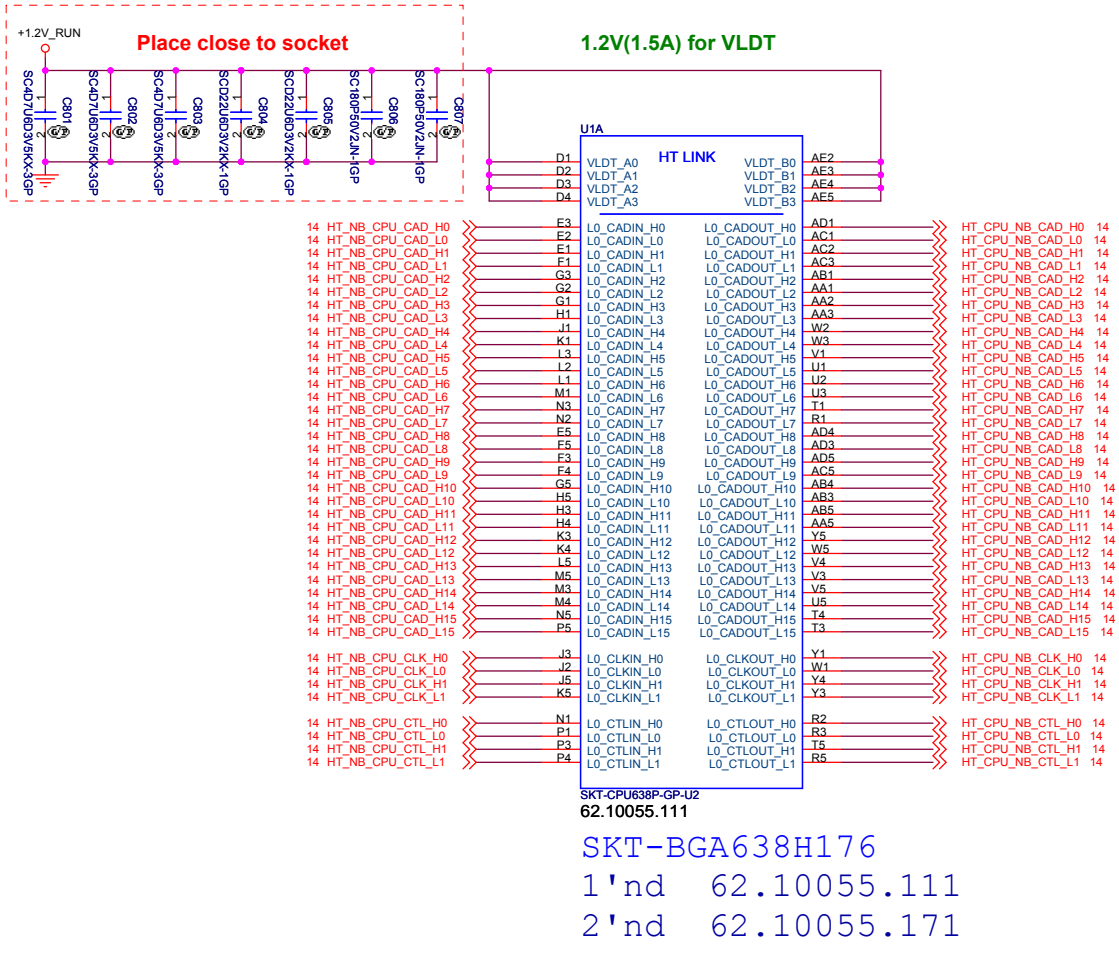
SSID = CPU

CPU HT3.0

CPU TYPE	C801~C803
*Griffin	4.7uF
Tigris	10uF

*DEFAULT

State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V



62.10055.111

SKT-BGA638H176

1'nd 62.10055.111

2'nd 62.10055.171

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_HT_LINK I/F_(1/4)	
Size: Custom	Document Number: Riya Discrete	Rev: A00
Date: Wednesday, August 26, 2009	Sheet 8 of 65	

SSID = CPU

Place near to CPU

+0.9V_VTT

C901 SC4D7U6D3V5KX-3GP
C916 SC4D7U6D3V5KX-3GP
C902 SC4D7U6D3V5KX-3GP
C903 SC4D7U6D3V5KX-3GP
C904 SC22U6D3V2KX-1GP
C905 SC22U6D3V2KX-1GP
C906 SC22U6D3V2KX-1GP
C907 SC22U6D3V2KX-1GP
C908 SC100P50V3JN-GP-U
C909 SC100P50V3JN-GP-U
C910 SC100P50V3JN-GP-U
C911 SC100P50V3JN-GP-U
C912 SC180P50V2JN-1GP
C913 SC180P50V2JN-1GP
C914 SC180P50V2JN-1GP
C915 SC180P50V2JN-1GP

+0.9V_VTT

0.9V(750mA) for VTT

U1B

MEM:CMD/CTRL/CLK

VTT1 D10
VTT2 C10
VTT3 B10
VTT4 AD10
VTT5 W10
VTT6 AC10
VTT7 AB10
VTT8 AA10
VTT9 A10

+1.8V_SUS

R901 1 39D2R2F-L-GP MEMZP
R903 1 39D2R2F-L-GP MEMZN

MEMZP AF10
MEMZN AE10
RSVD_M1 H16
VTT_SENSE Y10 TP_CPU_VTT_SUS_FB
MEMVREF W17
RSVD_M2 B18 TP_MEM_RSVD_M2

TP_MEM_RSVD_M1

13 MEM_MA0_ODT0 T19 MA0_ODT0
13 MEM_MA0_ODT1 V22 MA0_ODT1
U21 MA1_ODT0
V19 MA1_ODT1
MB0_ODT0 W26 MEM_MB0_ODT0 12
MB0_ODT1 W23 MEM_MB0_ODT1 12
MB1_ODT0 Y26

13 MEM_MA0_CS#0 T20 MA0_CS_L0
13 MEM_MA0_CS#1 U19 MA0_CS_L1
U20 MA1_CS_L0
V20 MA1_CS_L1
MB0_CS_L0 V26 MEM_MB0_CS#0 12
MB0_CS_L1 W25 MEM_MB0_CS#1 12
MB1_CS_L0 U22

13 MEM_MA_CKE0 J22 MA_CKE0
13 MEM_MA_CKE1 J20 MA_CKE1
MB_CKE0 J25 MEM_MB_CKE0 12
MB_CKE1 H26 MEM_MB_CKE1 12

N19 MA_CLK_H5
N20 MA_CLK_L5
13 MEM_MA_CLK0_P E16 MA_CLK_H1
13 MEM_MA_CLK0_N F16 MA_CLK_L1
13 MEM_MA_CLK1_P Y16 MA_CLK_H7
13 MEM_MA_CLK1_N AA16 MA_CLK_L7
P19 MA_CLK_H4
P20 MA_CLK_L4
MB_CLK_H5 P22
MB_CLK_L5 R22
MB_CLK_H1 A17 MEM_MB_CLK0_P 12
MB_CLK_L1 A18 MEM_MB_CLK0_N 12
MB_CLK_H7 AE18 MEM_MB_CLK1_P 12
MB_CLK_L7 AF17 MEM_MB_CLK1_N 12
MB_CLK_H4 R26
MB_CLK_L4 R25

13 MEM_MA_ADD0 N21 MA_ADD0
13 MEM_MA_ADD1 M20 MA_ADD1
13 MEM_MA_ADD2 N22 MA_ADD2
13 MEM_MA_ADD3 M19 MA_ADD3
13 MEM_MA_ADD4 M22 MA_ADD4
13 MEM_MA_ADD5 L20 MA_ADD5
13 MEM_MA_ADD6 M24 MA_ADD6
13 MEM_MA_ADD7 L21 MA_ADD7
13 MEM_MA_ADD8 L19 MA_ADD8
13 MEM_MA_ADD9 K22 MA_ADD9
13 MEM_MA_ADD10 R21 MA_ADD10
13 MEM_MA_ADD11 L22 MA_ADD11
13 MEM_MA_ADD12 K20 MA_ADD12
13 MEM_MA_ADD13 V24 MA_ADD13
13 MEM_MA_ADD14 K24 MA_ADD14
13 MEM_MA_ADD15 K19 MA_ADD15
MB_ADD0 P24 MEM_MB_ADD0 12
MB_ADD1 N24 MEM_MB_ADD1 12
MB_ADD2 P26 MEM_MB_ADD2 12
MB_ADD3 N23 MEM_MB_ADD3 12
MB_ADD4 N26 MEM_MB_ADD4 12
MB_ADD5 L23 MEM_MB_ADD5 12
MB_ADD6 N25 MEM_MB_ADD6 12
MB_ADD7 L24 MEM_MB_ADD7 12
MB_ADD8 M26 MEM_MB_ADD8 12
MB_ADD9 K26 MEM_MB_ADD9 12
MB_ADD10 T26 MEM_MB_ADD10 12
MB_ADD11 L26 MEM_MB_ADD11 12
MB_ADD12 L25 MEM_MB_ADD12 12
MB_ADD13 W24 MEM_MB_ADD13 12
MB_ADD14 J23 MEM_MB_ADD14 12
MB_ADD15 J24 MEM_MB_ADD15 12

13 MEM_MA_BANK0 R20 MA_BANK0
13 MEM_MA_BANK1 R23 MA_BANK1
13 MEM_MA_BANK2 J21 MA_BANK2
MB_BANK0 R24 MEM_MB_BANK0 12
MB_BANK1 U26 MEM_MB_BANK1 12
MB_BANK2 J26 MEM_MB_BANK2 12

13 MEM_MA_RAS# R19 MA_RAS_L
13 MEM_MA_CAS# T22 MA_CAS_L
13 MEM_MA_WE# T24 MA_WE_L
MB_RAS_L U25 MEM_MB_RAS# 12
MB_CAS_L U24 MEM_MB_CAS# 12
MB_WE_L U23 MEM_MB_WE# 12

SKT-CPU638P-GP-U2

62.10055.111

+0.9V_SUS_CPU_M_VREF

+1.8V_SUS

SC1U10V2KX-4GP C917
1KR3F-GP R902
SC1U10V2KX-4GP C919
1KR3F-GP R905
SC1000P50V3JN-GP-U C918

+V_DDR_VREF_M

R904 0 Do Not Stuff

CLOSE TO CPU

TP901 1 TP_MEM_RSVD_M1
TP902 1 TP_CPU_VTT_SUS_FB
TP903 1 TP_MEM_RSVD_M2

U1C

MEM:DATA

13 MEM_MA_DATA0	G12	MA_DATA0	MB_DATA0	C11	MEM_MB_DATA0 12
13 MEM_MA_DATA1	F12	MA_DATA1	MB_DATA1	A11	MEM_MB_DATA1 12
13 MEM_MA_DATA2	H14	MA_DATA2	MB_DATA2	A14	MEM_MB_DATA2 12
13 MEM_MA_DATA3	G14	MA_DATA3	MB_DATA3	B14	MEM_MB_DATA3 12
13 MEM_MA_DATA4	H11	MA_DATA4	MB_DATA4	G11	MEM_MB_DATA4 12
13 MEM_MA_DATA5	H12	MA_DATA5	MB_DATA5	E11	MEM_MB_DATA5 12
13 MEM_MA_DATA6	C13	MA_DATA6	MB_DATA6	D12	MEM_MB_DATA6 12
13 MEM_MA_DATA7	E13	MA_DATA7	MB_DATA7	A13	MEM_MB_DATA7 12
13 MEM_MA_DATA8	H15	MA_DATA8	MB_DATA8	A15	MEM_MB_DATA8 12
13 MEM_MA_DATA9	E15	MA_DATA9	MB_DATA9	A16	MEM_MB_DATA9 12
13 MEM_MA_DATA10	E17	MA_DATA10	MB_DATA10	A19	MEM_MB_DATA10 12
13 MEM_MA_DATA11	H17	MA_DATA11	MB_DATA11	A20	MEM_MB_DATA11 12
13 MEM_MA_DATA12	E14	MA_DATA12	MB_DATA12	C14	MEM_MB_DATA12 12
13 MEM_MA_DATA13	F14	MA_DATA13	MB_DATA13	D14	MEM_MB_DATA13 12
13 MEM_MA_DATA14	C17	MA_DATA14	MB_DATA14	C18	MEM_MB_DATA14 12
13 MEM_MA_DATA15	G17	MA_DATA15	MB_DATA15	D18	MEM_MB_DATA15 12
13 MEM_MA_DATA16	G18	MA_DATA16	MB_DATA16	D20	MEM_MB_DATA16 12
13 MEM_MA_DATA17	C19	MA_DATA17	MB_DATA17	A21	MEM_MB_DATA17 12
13 MEM_MA_DATA18	D22	MA_DATA18	MB_DATA18	D24	MEM_MB_DATA18 12
13 MEM_MA_DATA19	E20	MA_DATA19	MB_DATA19	C25	MEM_MB_DATA19 12
13 MEM_MA_DATA20	E18	MA_DATA20	MB_DATA20	B20	MEM_MB_DATA20 12
13 MEM_MA_DATA21	F18	MA_DATA21	MB_DATA21	C20	MEM_MB_DATA21 12
13 MEM_MA_DATA22	B22	MA_DATA22	MB_DATA22	B24	MEM_MB_DATA22 12
13 MEM_MA_DATA23	C23	MA_DATA23	MB_DATA23	C24	MEM_MB_DATA23 12
13 MEM_MA_DATA24	F20	MA_DATA24	MB_DATA24	E23	MEM_MB_DATA24 12
13 MEM_MA_DATA25	F22	MA_DATA25	MB_DATA25	E24	MEM_MB_DATA25 12
13 MEM_MA_DATA26	H24	MA_DATA26	MB_DATA26	G25	MEM_MB_DATA26 12
13 MEM_MA_DATA27	J19	MA_DATA27	MB_DATA27	G26	MEM_MB_DATA27 12
13 MEM_MA_DATA28	F21	MA_DATA28	MB_DATA28	C26	MEM_MB_DATA28 12
13 MEM_MA_DATA29	F22	MA_DATA29	MB_DATA29	D26	MEM_MB_DATA29 12
13 MEM_MA_DATA30	H20	MA_DATA30	MB_DATA30	G23	MEM_MB_DATA30 12
13 MEM_MA_DATA31	H22	MA_DATA31	MB_DATA31	G24	MEM_MB_DATA31 12
13 MEM_MA_DATA32	Y24	MA_DATA32	MB_DATA32	AA24	MEM_MB_DATA32 12
13 MEM_MA_DATA33	AB24	MA_DATA33	MB_DATA33	AA23	MEM_MB_DATA33 12
13 MEM_MA_DATA34	AB22	MA_DATA34	MB_DATA34	AD24	MEM_MB_DATA34 12
13 MEM_MA_DATA35	AA21	MA_DATA35	MB_DATA35	AF24	MEM_MB_DATA35 12
13 MEM_MA_DATA36	W22	MA_DATA36	MB_DATA36	AA26	MEM_MB_DATA36 12
13 MEM_MA_DATA37	W21	MA_DATA37	MB_DATA37	AA25	MEM_MB_DATA37 12
13 MEM_MA_DATA38	Y22	MA_DATA38	MB_DATA38	AD26	MEM_MB_DATA38 12
13 MEM_MA_DATA39	AA22	MA_DATA39	MB_DATA39	AE25	MEM_MB_DATA39 12
13 MEM_MA_DATA40	Y20	MA_DATA40	MB_DATA40	AC22	MEM_MB_DATA40 12
13 MEM_MA_DATA41	AA20	MA_DATA41	MB_DATA41	AD22	MEM_MB_DATA41 12
13 MEM_MA_DATA42	AA18	MA_DATA42	MB_DATA42	AE20	MEM_MB_DATA42 12
13 MEM_MA_DATA43	AB18	MA_DATA43	MB_DATA43	AF20	MEM_MB_DATA43 12
13 MEM_MA_DATA44	AB21	MA_DATA44	MB_DATA44	AF24	MEM_MB_DATA44 12
13 MEM_MA_DATA45	AD21	MA_DATA45	MB_DATA45	AF23	MEM_MB_DATA45 12
13 MEM_MA_DATA46	AD19	MA_DATA46	MB_DATA46	AC20	MEM_MB_DATA46 12
13 MEM_MA_DATA47	Y18	MA_DATA47	MB_DATA47	AD20	MEM_MB_DATA47 12
13 MEM_MA_DATA48	AD17	MA_DATA48	MB_DATA48	AD18	MEM_MB_DATA48 12
13 MEM_MA_DATA49	W16	MA_DATA49	MB_DATA49	AE18	MEM_MB_DATA49 12
13 MEM_MA_DATA50	W14	MA_DATA50	MB_DATA50	AC14	MEM_MB_DATA50 12
13 MEM_MA_DATA51	Y14	MA_DATA51	MB_DATA51	AD14	MEM_MB_DATA51 12
13 MEM_MA_DATA52	Y17	MA_DATA52	MB_DATA52	AE19	MEM_MB_DATA52 12
13 MEM_MA_DATA53	AB17	MA_DATA53	MB_DATA53	AC18	MEM_MB_DATA53 12
13 MEM_MA_DATA54	AB15	MA_DATA54	MB_DATA54	AE16	MEM_MB_DATA54 12
13 MEM_MA_DATA55	AD15	MA_DATA55	MB_DATA55	AE15	MEM_MB_DATA55 12
13 MEM_MA_DATA56	AB13	MA_DATA56	MB_DATA56	AF13	MEM_MB_DATA56 12
13 MEM_MA_DATA57	AD13	MA_DATA57	MB_DATA57	AC12	MEM_MB_DATA57 12
13 MEM_MA_DATA58	Y12	MA_DATA58	MB_DATA58	AB11	MEM_MB_DATA58 12
13 MEM_MA_DATA59	W11	MA_DATA59	MB_DATA59	Y11	MEM_MB_DATA59 12
13 MEM_MA_DATA60	AB14	MA_DATA60	MB_DATA60	AE14	MEM_MB_DATA60 12
13 MEM_MA_DATA61	AA14	MA_DATA61	MB_DATA61	AE14	MEM_MB_DATA61 12
13 MEM_MA_DATA62	AB12	MA_DATA62	MB_DATA62	AF11	MEM_MB_DATA62 12
13 MEM_MA_DATA63	AA12	MA_DATA63	MB_DATA63	AD11	MEM_MB_DATA63 12
13 MEM_MA_DM0	E12	MA_DM0	MB_DM0	A12	MEM_MB_DM0 12
13 MEM_MA_DM1	C15	MA_DM1	MB_DM1	B16	MEM_MB_DM1 12
13 MEM_MA_DM2	E19	MA_DM2	MB_DM2	A22	MEM_MB_DM2 12
13 MEM_MA_DM3	F24	MA_DM3	MB_DM3	E25	MEM_MB_DM3 12
13 MEM_MA_DM4	AC24	MA_DM4	MB_DM4	AB26	MEM_MB_DM4 12
13 MEM_MA_DM5	Y19	MA_DM5	MB_DM5	AE22	MEM_MB_DM5 12
13 MEM_MA_DM6	AB16	MA_DM6	MB_DM6	AC16	MEM_MB_DM6 12
13 MEM_MA_DM7	Y13	MA_DM7	MB_DM7	AD12	MEM_MB_DM7 12
13 MEM_MA_DQS0_P	G13	MA_DQS_H0	MB_DQS_H0	C12	MEM_MB_DQS0_P 12
13 MEM_MA_DQS0_N	H13	MA_DQS_L0	MB_DQS_L0	B12	MEM_MB_DQS0_N 12
13 MEM_MA_DQS1_P	G16	MA_DQS_H1	MB_DQS_H1	D16	MEM_MB_DQS1_P 12
13 MEM_MA_DQS1_N	G15	MA_DQS_L1	MB_DQS_L1	C16	MEM_MB_DQS1_N 12
13 MEM_MA_DQS2_P	C22	MA_DQS_H2	MB_DQS_H2	A24	MEM_MB_DQS2_P 12
13 MEM_MA_DQS2_N	C21	MA_DQS_L2	MB_DQS_L2	A23	MEM_MB_DQS2_N 12
13 MEM_MA_DQS3_P	G22	MA_DQS_H3	MB_DQS_H3	F26	MEM_MB_DQS3_P 12
13 MEM_MA_DQS3_N	G21	MA_DQS_L3	MB_DQS_L3	E26	MEM_MB_DQS3_N 12
13 MEM_MA_DQS4_P	AD23	MA_DQS_H4	MB_DQS_H4	AC25	MEM_MB_DQS4_P 12
13 MEM_MA_DQS4_N	AC23	MA_DQS_L4	MB_DQS_L4	AC26	MEM_MB_DQS4_N 12
13 MEM_MA_DQS5_P	AB19	MA_DQS_H5	MB_DQS_H5	AF21	MEM_MB_DQS5_P 12
13 MEM_MA_DQS5_N	AB20	MA_DQS_L5	MB_DQS_L5	AF22	MEM_MB_DQS5_N 12
13 MEM_MA_DQS6_P	Y15	MA_DQS_H6	MB_DQS_H6	AE16	MEM_MB_DQS6_P 12
13 MEM_MA_DQS6_N	W15	MA_DQS_L6	MB_DQS_L6	AD16	MEM_MB_DQS6_N 12
13 MEM_MA_DQS7_P	W12	MA_DQS_H7	MB_DQS_H7	AF12	MEM_MB_DQS7_P 12
13 MEM_MA_DQS7_N	W13	MA_DQS_L7	MB_DQS_L7	AE12	MEM_MB_DQS7_N 12

SKT-CPU638P-GP-U2

62.10055.111

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_DDR_(2/4)

Size	Document Number	Rev
Custom	Riya Discrete	A00

Date: Wednesday, August 26, 2009 Sheet 9 of 65

SSID = CPU

LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

2.5V(250mA) for VDDA

X01
04/14 Del
1.Del R1001 ,reserve closed-gap.
Del R1002 ,reserve closed-gap.
Del R1003 ,reserve closed-gap.

CPU TYPE	R1004
*Griffin	STUFF
Tigris	EMPTY

*DEFAULT

CPU_CLK(200MHz)

For HDT DBG

Close CPU

CPU TYPE	R1015 R1017
*Griffin	300 ohm
Tigris	510 ohm

*DEFAULT

X01
04/09 Modify
1.Change CPU SID/SIC from SB_SMBus_Ch1 to SCL3_LV/SDA3_LV.
2.Del Q1001,R1027,Q1003,R1028.

X01
04/14 BOM
1.Dummy R1022.

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

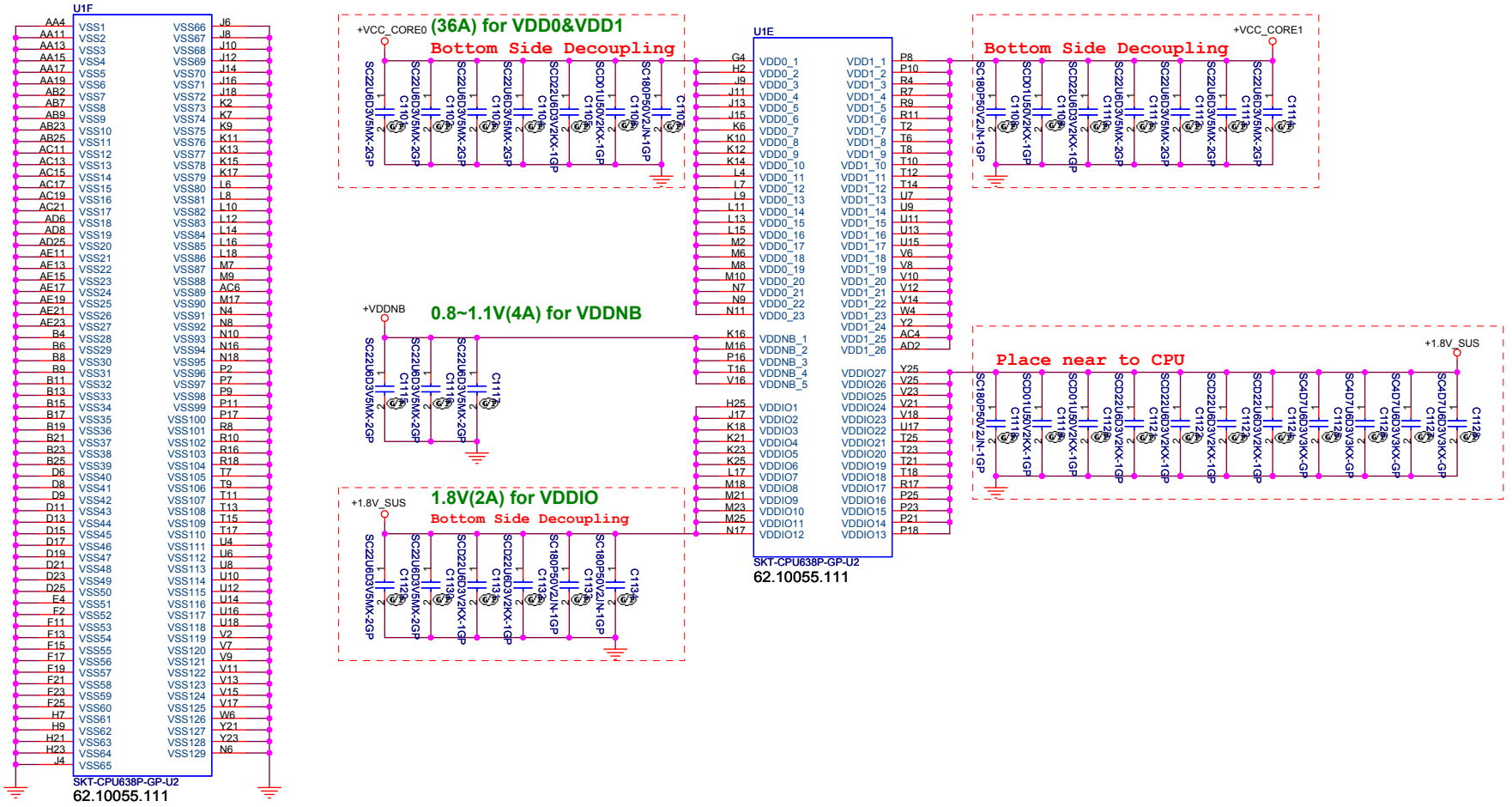
HDT Connectors

Main Source

Title	CPU_Control&Debug_(3/4)
Size	Custom
Document Number	Riya Discrete
Rev	A00
Date:	Wednesday, August 26, 2009
Sheet	10 of 65

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

SSID = CPU

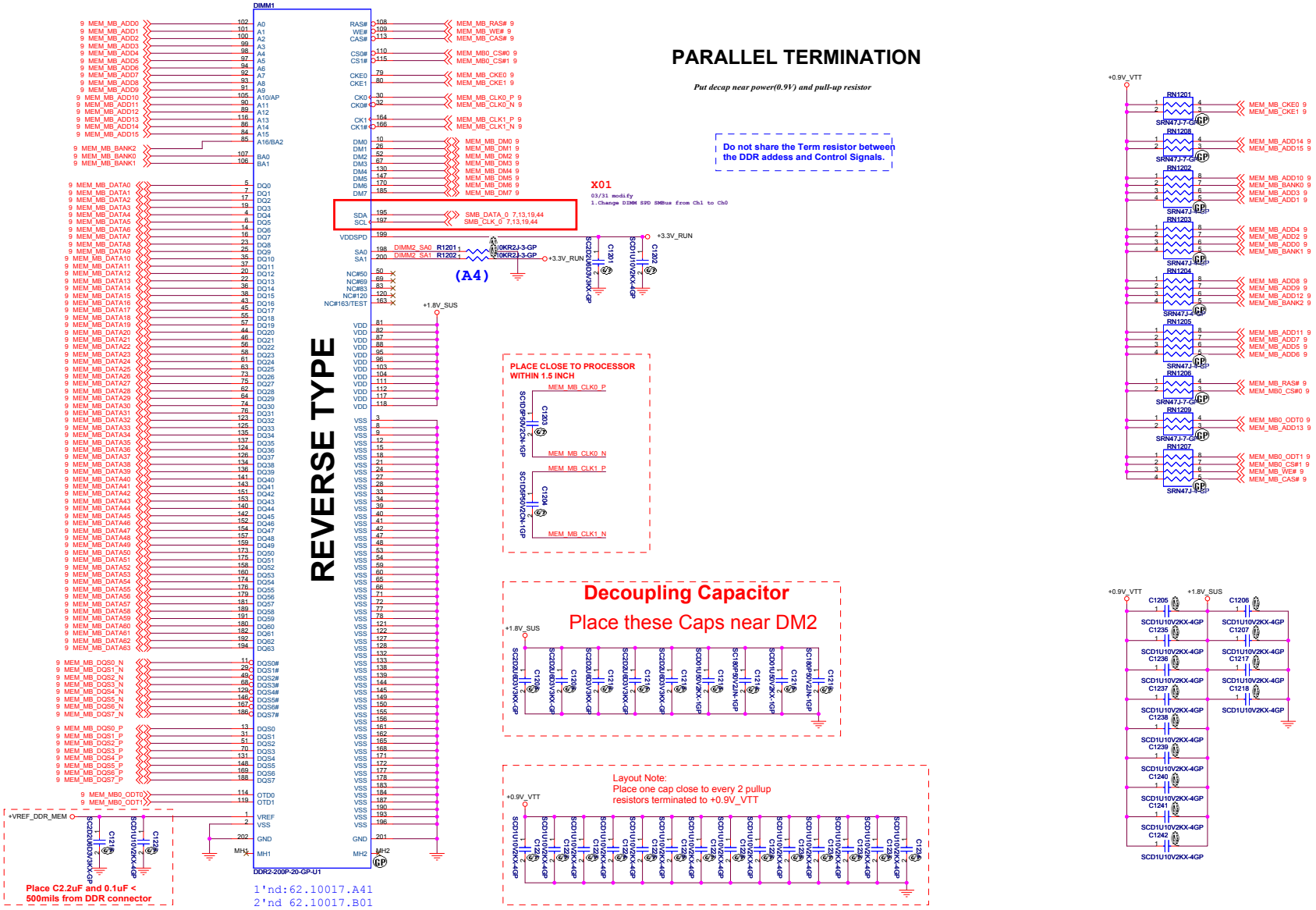


Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU_Power_(4/4)		
Size: A3	Document Number: Riya Discrete	Rev: A00
Date: Tuesday, September 08, 2009	Sheet 11 of 65	

SSID = MEMORY

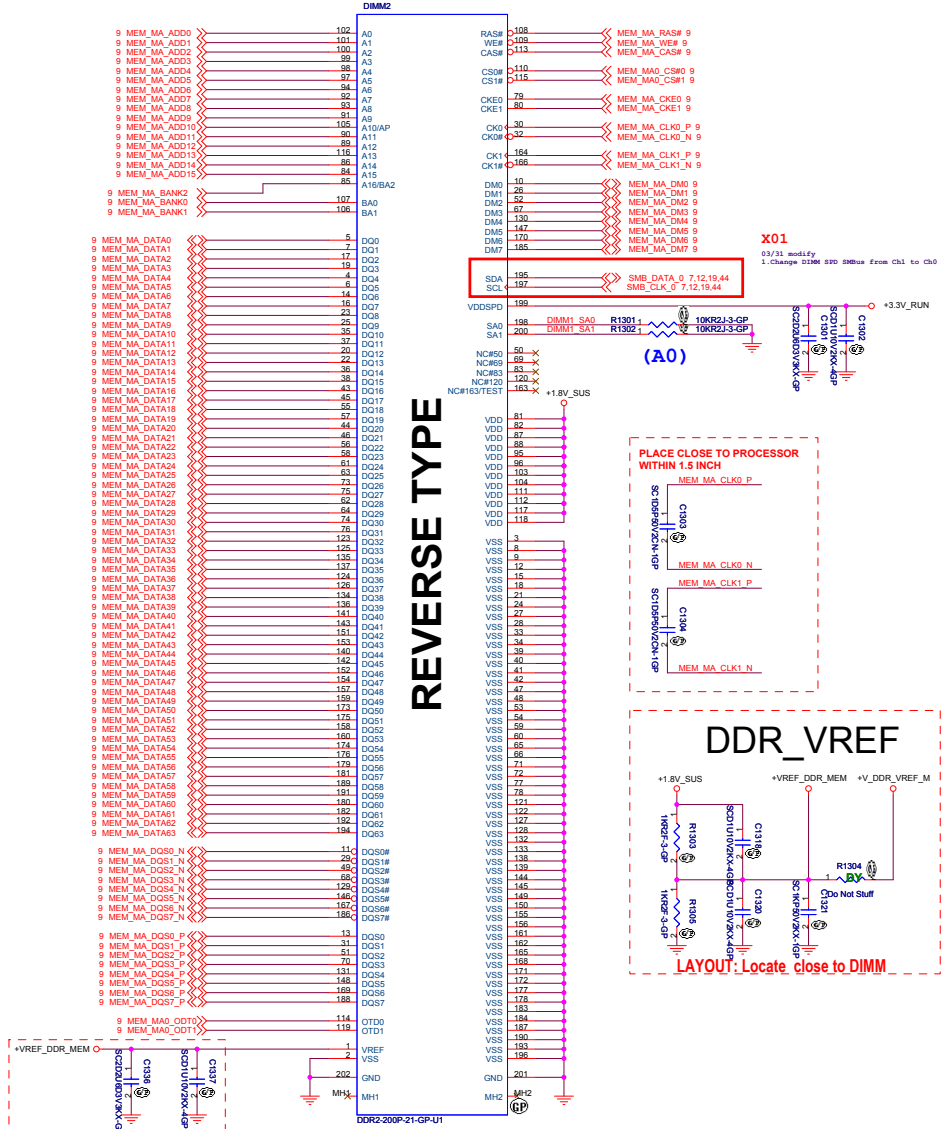


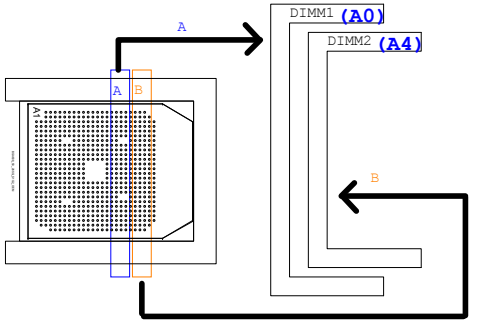
Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
DDR_DIMM1		
Size: A2	Document Number: Riya Discrete	Rev: A00
Date: Wednesday, August 26, 2009	Sheet 12 of 65	

SSID = MEMORY

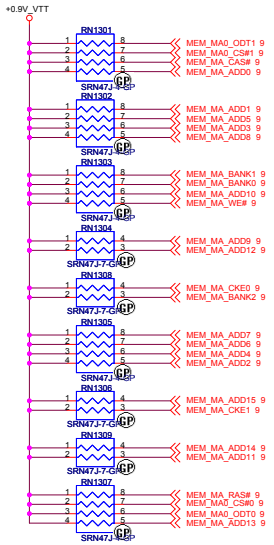


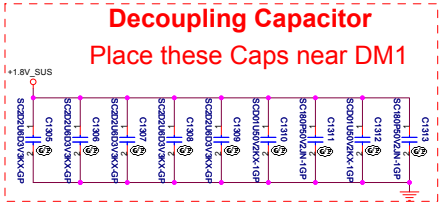


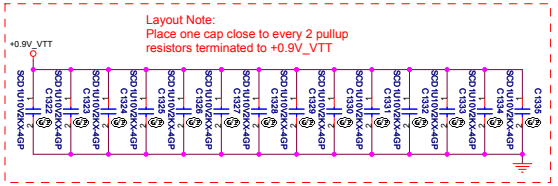
PARALLEL TERMINATION

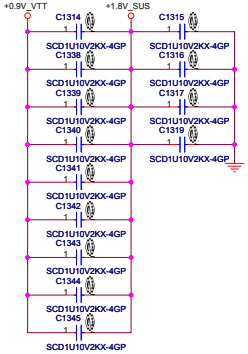
Put decap near power(0.9V) and pull-up resistor

Do not share the Term resistor between the DDR addess and Control Signals.









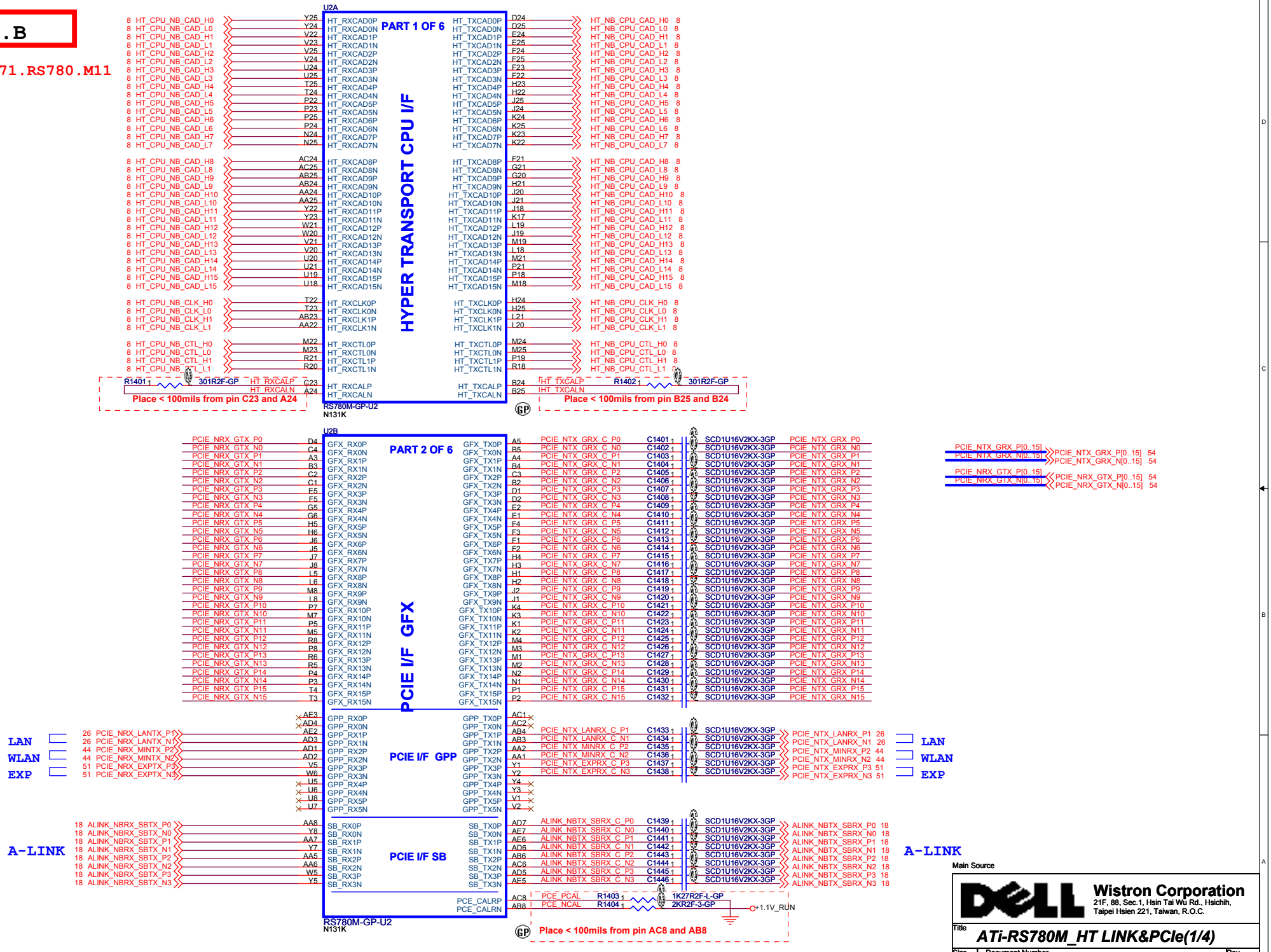
Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR_DIMM2	
Size: A2	Document Number: Riya Discrete	Rev: A00
Date: Wednesday, August 26, 2009	Sheet 13 of 65	

SSID = N.B

RS780M A13 : 71.RS780.M11



Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_HT LINK&PCIe(1/4)

Size	Document Number	Rev
Custom	Riya Discrete	A00

Date: Thursday, September 03, 2009 Sheet 14 of 65

SSID = N.B

STRAP_DEBUG_BUS_GPIO_ENABLE# (RS780M use DAC_VSYNC)

Enables debug bus access through memory I/O pads and GPIOs.
0 : Enable * 1 : Disable

SIDE_PORT_EN# (RS780M use DAC_HSYNC)

0 : Available * 1 : Not available

LOAD_EEPROM_STRAPS#(RS780M use SUS_STAT#)

Selects Loading of STRAPS From EEPROM
* 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected

*DEFAULT

+1.8V_RUN — L1503 BLM15AG221SS1D-GP 220 ohm 300mA — +1.8V_VDDA18HTPLL — C1506 SC2D2U6D3V3KX-GP, C1508 SCD1U10V2KX-4GP — 15 mil

+1.8V_RUN — L1504 BLM15AG221SS1D-GP 220 ohm 300mA — +1.8V_VDDA18PCIEPLL — C1507 SC2D2U6D3V3KX-GP, C1509 SCD1U10V2KX-4GP — 15 mil

Layout Note

+3.3V_RUN — R1502 3KR2J-2-GP — R1503 3KR2J-2-GP — NB_VGA_VSYNC, NB_VGA_HSYNC

R1504 Do Not Stuff — R1505 Do Not Stuff

A00
8/22
Change R1509 from 0 ohm to short pad

X01
04/17 Del
1.Del R1508, No reserve

+3.3V_RUN — R1506 Do Not Stuff — R1507 Do Not Stuff

R1501 715R2F-GP — DAC_RSET

R1509 Do Not Stuff

10 CPU_R_LDT_STOP# — R1510 Do Not Stuff
10,18 ALLOW_LDTSTOP — R1511 Do Not Stuff

18 PLT_RST#
30 1D8_NB_PWRGD

X01
04/14 Del
1.Del R1510 ,reserve closed-gap.
Del R1511 ,reserve closed-gap.

+1.1V_RUN — R1512 Do Not Stuff — R1513 Do Not Stuff — NB_REFCLK_N

+3.3V_RUN — R1515 Do Not Stuff — R1516 150R2F-1-GP

GPIO MODE

STRP_DATA	VCC_NB
* 1	1.0V
0	1.1V

*DEFAULT

U2C — RS780M-GP-U2 N131K — PART 3 OF 6

CRT/TVOUT: AVDD1, AVDD2, AVDDDI, AVSSDI, AVDDQ, AVSSQ, C_Pr, Y, COMP_Pb, RED, REDb, GREEN, GREENb, BLUE, BLUEb, DAC_HSYNC, DAC_VSYNC, DAC_SCL, DAC_SDA, DAC_RSET

PLL PWR: PLLVDD, PLLVDD18, PLLVSS, VDDA18HTPLL, VDDA18PCIEPLL1, VDDA18PCIEPLL2

LVTM: SYSRESET#, POWERGOOD, LDTSTOP#, ALLOW_LDTSTOP, TXOUT_L0P/N, TXOUT_L1P/N, TXOUT_L2P/N, TXOUT_L3P/N, TXOUT_U0P/N, TXOUT_U1P/N, TXOUT_U2P/N, TXOUT_U3P/N, TXCLK_LP/LN/UP/UN, VDDLTP18, VSSLTP18, VDDLT18_1, VDDLT18_2, VDDLT33_1, VDDLT33_2, VSSLT1–VSSLT7

CLOCKs PM: HT_REFCLKP, HT_REFCLKN, REFCLK_P/OSCIN, REFCLK_N, GFX_REFCLKP, GFX_REFCLKN, GPP_REFCLKP, GPP_REFCLKN, GPPSB_REFCLKP, GPPSB_REFCLKN

MIS.: I2C_CLK, I2C_DATA, DDC_DATA0/AUX0N, DDC_CLK0/AUX0P, DDC_CLK1/AUX1P, DDC_DATA1/AUX1N, STRP_DATA, RESERVED, AUX_CAL, TMDS_HPD, HPD, SUS_STAT#, THERMALDIODE_P, THERMALDIODE_N, TESTMODE

LVDS_DIGON, LVDS_BLON, LVDS_ENA_BL

NB_VGA_HSYNC, NB_VGA_VSYNC

7 CLK_NBHT_CLK, 7 CLK_NBHT_CLK#
7 NB_14M_CLK
7 NB_GFX_CLK, 7 NB_GFX_CLK#
7 NB_GPP_CLK, 7 NB_GPP_CLK#
7 NB_GPPSB_CLK, 7 NB_GPPSB_CLK#

TP_NB_DDC_DATA0, TP_NB_DDC_CLK0, TP_NB_DDC_CLK1, TP_NB_DDC_DATA1, STRP_DATA, TP_NB_RESERVED, RS780_AUX_CAL

SYSRESET#, NB_LDT_STOP#, NB_ALLOW_LDTSTOP

+3.3V_RUN — R1514 3KR2J-2-GP — NB_SUS_STAT#

R1517 1K8R2F-GP — TESTMODE_NB

GP

TP1501 TP_NB_DDC_DATA0
TP1502 TP_NB_DDC_CLK0
TP1503 TP_NB_DDC_CLK1
TP1504 TP_NB_DDC_DATA1
TP1505 TP_NB_RESERVED

Main Source

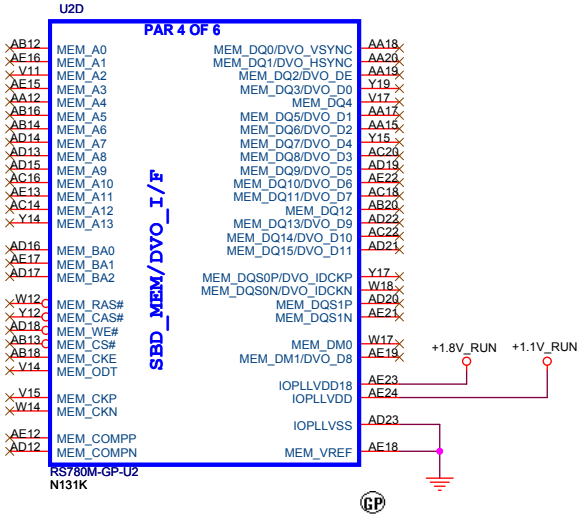
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_LVDS&CRT_(2/4)

Size	Document Number	Rev
A3	Riya Discrete	A00

Date: Thursday, September 03, 2009 Sheet 15 of 65

SSID = N.B



Main Source

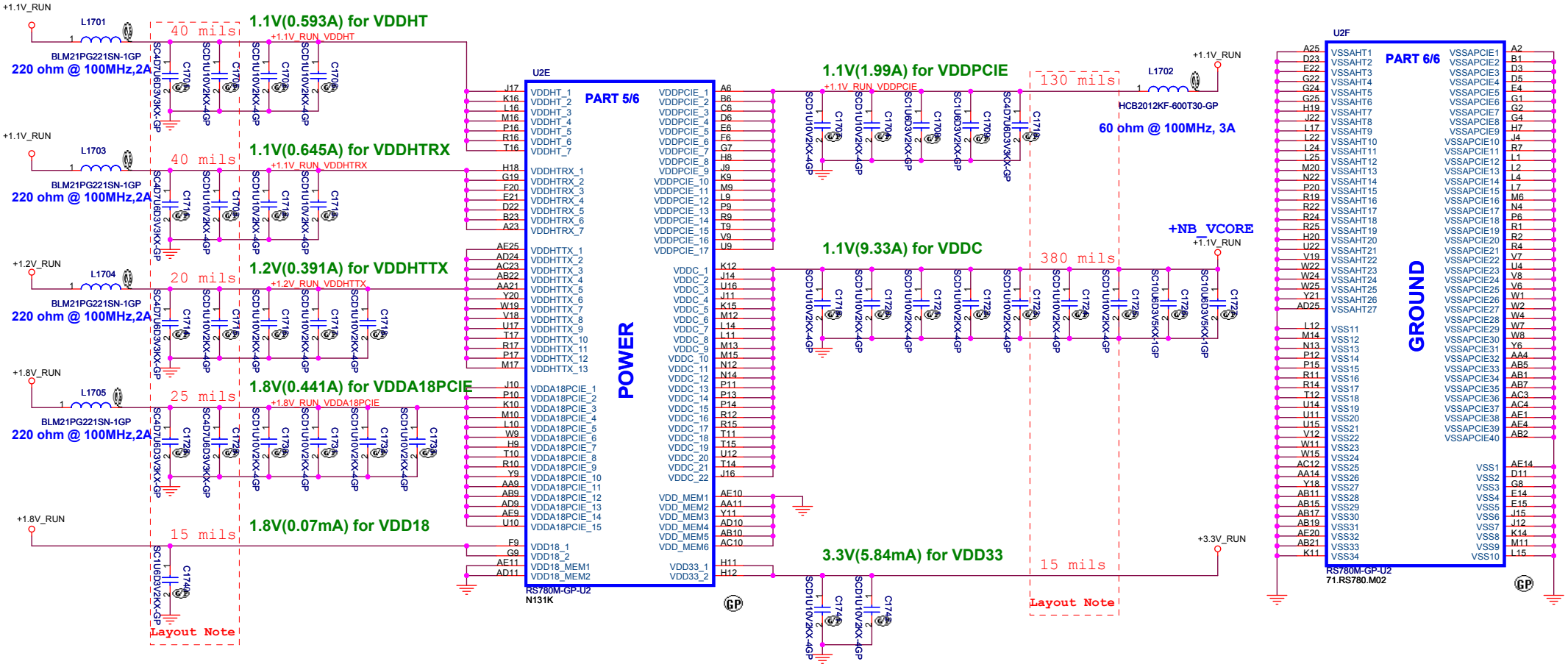
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_SidePort_(3/4)

Size	Document Number	Rev
A3	Riya Discrete	A00

Date: Thursday, September 03, 2009 Sheet 16 of 65

SSID = N.B



Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_PWR&GD_(4/4)

Size	Document Number	Rev
A3	Riya Discrete	A00

Date: Thursday, September 03, 2009 Sheet 17 of 65

SSID = S.B

SB700 A12 : 71.SB700.M05

U3A

SB700

Part 1 of 5

PCI EXPRESS INTERFACE

PCI CLKS

PCI INTERFACE

CLOCK GENERATOR

LPC

RTC XTAL

CPU

RTC

PCI CLK EMI

20mil Width

Place R <100mils form pins T25,T24

BLM15AG221SS1D-GP

220 ohm 300mA

X01

04/14 modify

1.Change C1810/C1812 from 18P to 15P

CPU TYPE	R1813
*Griffin	300 ohm
Tigris	1K ohm

*DEFAULT

A00

8/24

Change R1812 from 0 ohm to short pad

9/8

Add TP_25M_X1,TP_25M_X2

SB TYPE	RN1801
*SB700	STUFF
SB710	EMPTY

*DEFAULT

LPC Bus Routing first connects to MINICARD then connects to KBC

1'nd 73.01G08.DHG

2'nd 73.01G08.L04

Cloce To U38

X01

04/08 Del

1.Del R1817 (Card reader System reset depend on 3.3V_Run power rails, Not reserve for A_RST.)

SB700-1-GP-U1

Y708D

Main Source

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_PCIE&PCI_(1/5)

Size: A3 | Document Number: Riya Discrete | Rev: A00

Date: Tuesday, September 08, 2009 | Sheet 18 of 65

SSID = S.B

U3D

SB700

Part 4 of 5

SB700-1-GP-U1
Y708D

X01
04/14 Del
1.Del R1902 ,reserve closed-gap.

X01
03/31 modify
1.Change DIMM SPD SMBus from Ch1 to Ch0
04/08 modify
1.Change Clk gen,Mini Card SMBus from Ch1 to Ch0

A00
8/22
Change R1907, R1920,R1921 from 0 ohm to short pad

X01
04/06 Change
1.Change R1914 from 33 ohm to 47 ohm

Close SB

Close to SB700

TO STRAPS

Strap Pin / define to use LPC or SPI ROM

1%
Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.

Place these close SB700

A00
8/22
Change R1903 from 11.8k to 10.7k
9/3
Change R1903 from 10K7R2D to 10k7R2F

X01
03/31 modify
1.Change Bluetooth from USB Port-12 to Port-6

X01
04/09 Modify
1.Change CPU SID/SIC from SB_SMBus_Ch1 to SCL3_LV/SDA3_LV.

USB_FSD13P / USB_FSD13N	----->RESERVED
USB_FSD12P / USB_FSD12N	----->RESERVED
USB_HSD11P / USB_HSD11N	----->USB Port Right Side — USB_OC_2_#
USB_HSD10P / USB_HSD10N	----->MINI CARD
USB_HSD9P / USB_HSD9N	----->Card Reader
USB_HSD8P / USB_HSD8N	----->RESERVED
USB_HSD7P / USB_HSD7N	----->RESERVED
USB_HSD6P / USB_HSD6N	----->BLUETOOTH
USB_HSD5P / USB_HSD5N	----->RESERVED
USB_HSD4P / USB_HSD4N	----->Express Card
USB_HSD3P / USB_HSD3N	----->RESERVED
USB_HSD2P / USB_HSD2N	----->Camera
USB_HSD1P / USB_HSD1N	----->I/O BOARD Left Side — USB_OC_01_#
USB_HSD0P / USB_HSD0N	----->I/O BOARD Left Side — USB_OC_01_#

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_USB&GPIO_(2/5)

Size: Custom | Document Number: Riya Discrete | Rev: A00

Date: Thursday, September 03, 2009 | Sheet 19 of 65

SSID = S.B

X01
04/06 modify
1.Change SATA HD from Port-3 to Port-0

SATA HDD
SATA ODD

PLACE SATA AC DECOUPLING CAPS CLOSE TO SB700

X01
04/06 modify
1.Change C2009/C2010 from 10P to 12P

XTAL
1'nd 82.30020.851
2'nd 82.30020.791

Very Close to SB700

20mil Width
220 ohm 300mA

U3B
SB700
Part 2 of 5
SERIAL ATA
ATA 66/100/133
SPI ROM
SATA PWR
HW MONITOR
SB700-1-GP-U1
Y708D

X01
04/02 modify
1.Add SB GPIO48 To detect LCD Size
06/09 modify
1.Del R2009 R2010

A00
8/24
Change L2003 from 0 ohm to short pad

Layout Notice connect to cap then Gnd

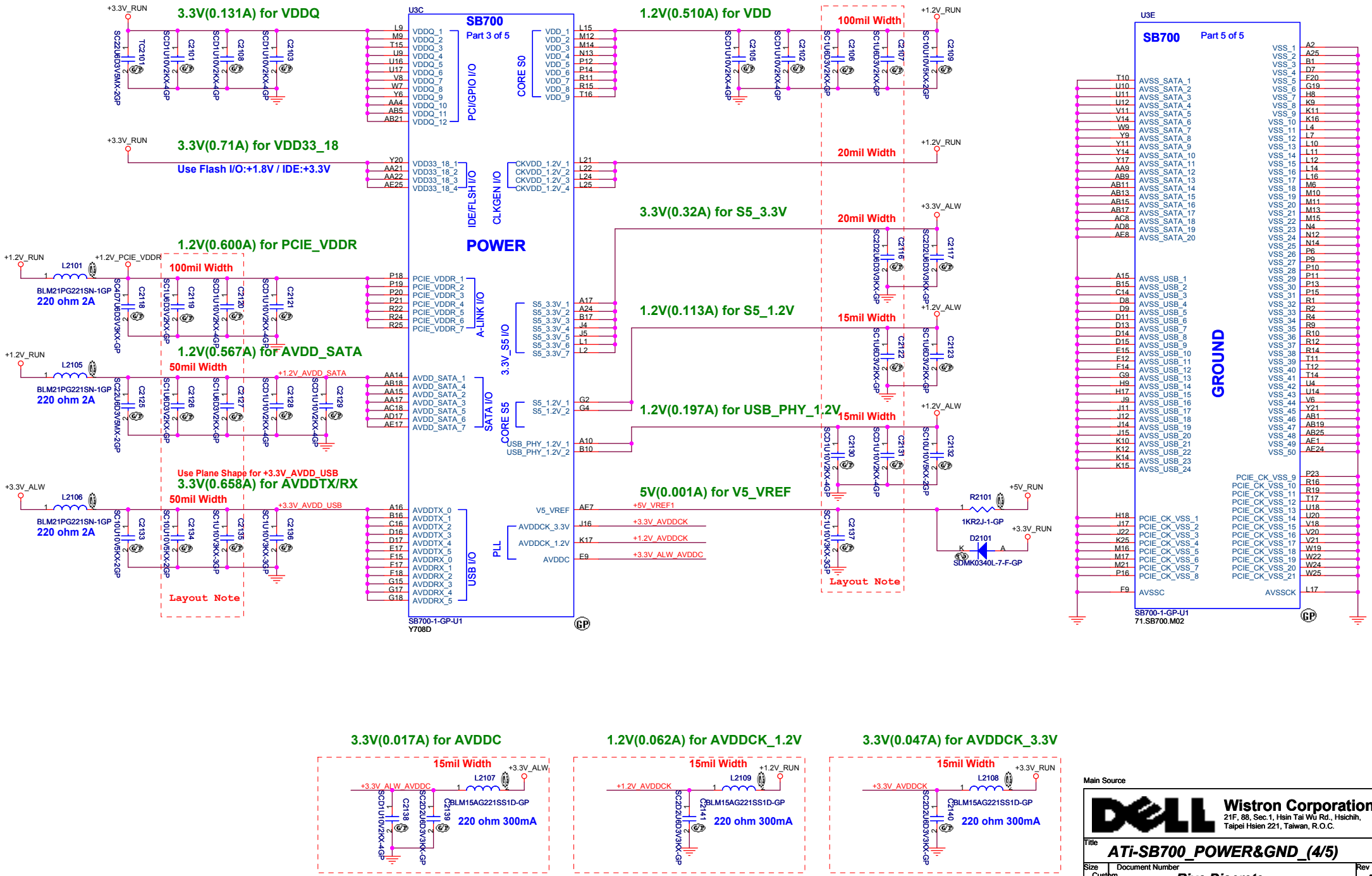
TP2001 TP_ROM_RST#
TP2002 TP_SPI_DI
TP2003 TP_SPI_DO
TP2004 TP_SPI_CLK
TP2005 TP_SPI_HOLD#
TP2006 TP_SPI_CS#
TP2007 TP_SB_SATA_ACT#
TP2008 TP_SB_GPIO13
TP2009 TP_SB_GPIO3
TP2011 TP_SB_GPIO49
TP2012 TP_SB_GPIO50
TP2013 TP_SB_GPIO52
TP2014 TP_SB_GPIO61

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_SATA-IDE_(3/5)
Size: Custom | Document Number: Riya Discrete | Rev: A00
Date: Thursday, September 03, 2009 | Sheet 20 of 65

SSID = S.B



Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

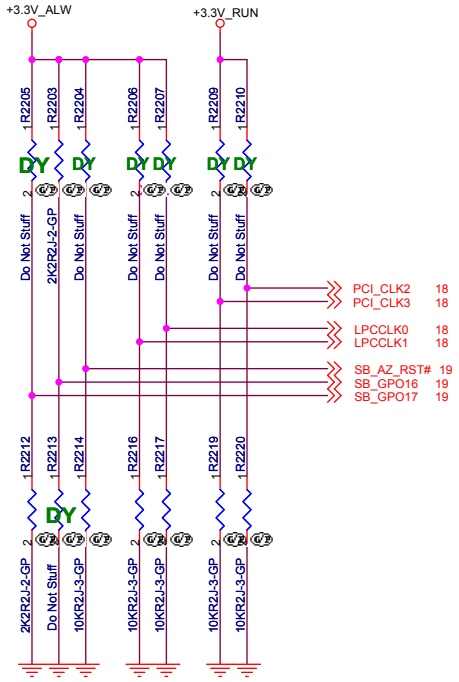
Title: ATi-SB700_POWER&GND_(4/5)

Size	Document Number	Rev
Custom	Riya Discrete	A00

Date: Thursday, September 03, 2009 Sheet 21 of 65

SSID = S.B

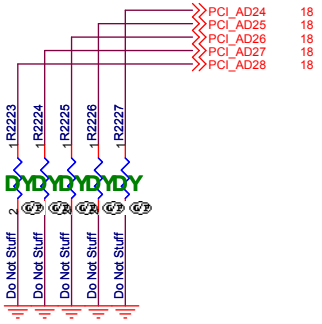
REQUIRED STRAPS



REQUIRED SYSTEM STRAPS

	PCI_CLK2	PCI_CLK3	LPCCLK0	LPCCLK1	SB_AZ_RST#	SB_GPO17 , SB_GPO16 ROM TYPE:
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	IMC ENABLED	CLKGEN ENABLED (Use Internal)	ENABLE PCI ROM BOOT	H, H = Reserved H, L = SPI ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	DISABLE PCI ROM BOOT DEFAULT	DEFAULT L, H = LPC ROM L, L = FWH ROM

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_STRAPPING_(5/5)

Size	Document Number	Rev
A3	Riya Discrete	A00

Date: Wednesday, August 26, 2009 Sheet 22 of 65

SSID = AUDIO

X01

06/16 modify
1.Change U2301 to new version

A00

9/8
Change U2301 to new version
from 71.92H81.E03 to 71.92H81.E03

A00

8/24
Change R2302,R2303,R2304 from 0 ohm to short pad

U2301

92HD81B1A5NLGXUAX8-GP

71.92H81.G03

Close to codec

Close to codec

AUD_DVDDCORE

AUD_PC_BEEP
Trace width>15 mils

Close to codec

From SB

From EC

Azalia I/F EMI

Close to Pin13

Close to Pin14

Main Source

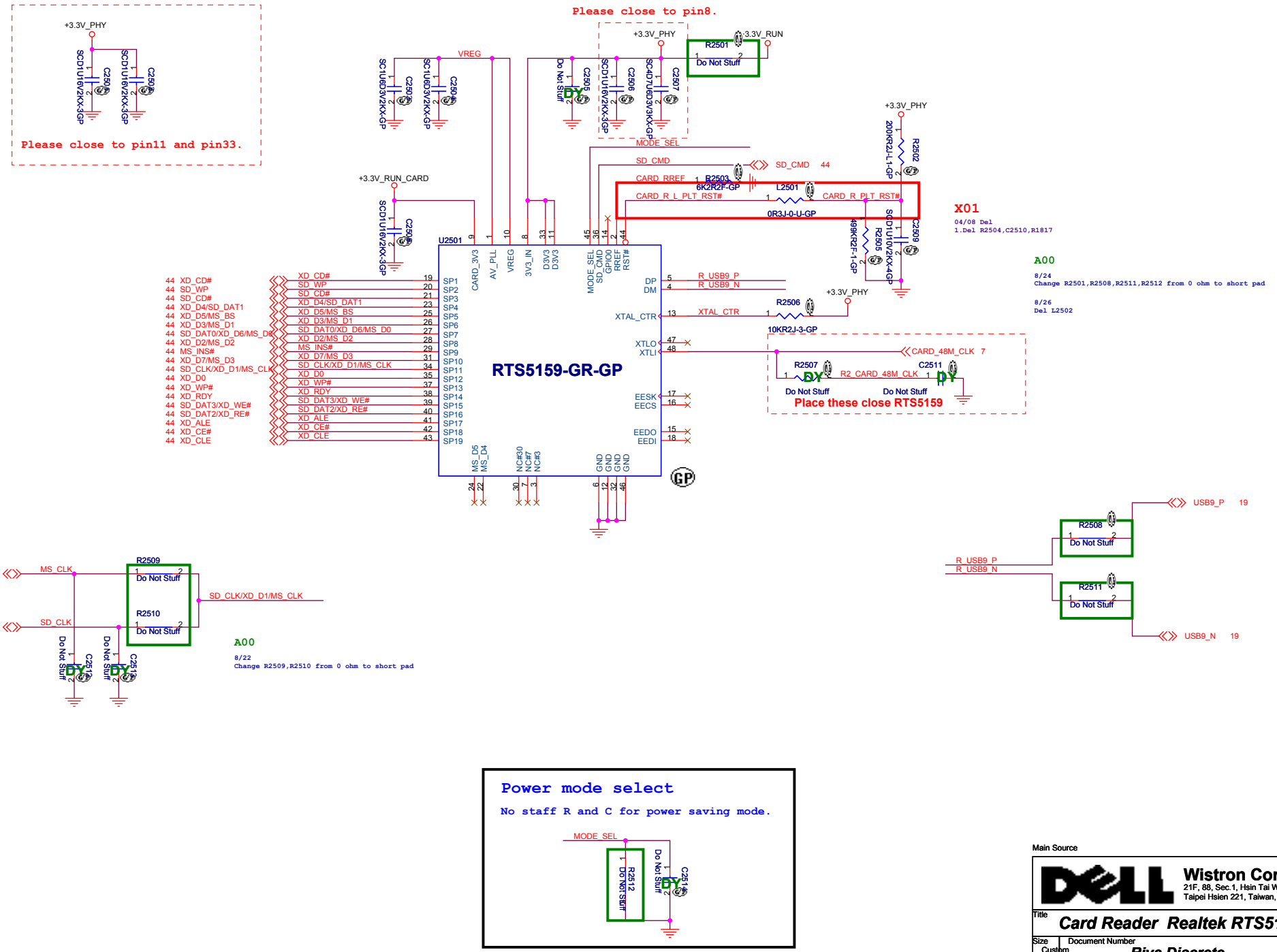
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC IDT-92HD81

Size: Custom | Document Number: Riya Discrete | Rev: A00

Date: Tuesday, September 08, 2009 | Sheet 23 of 65

SSID = SDIO



Main Source

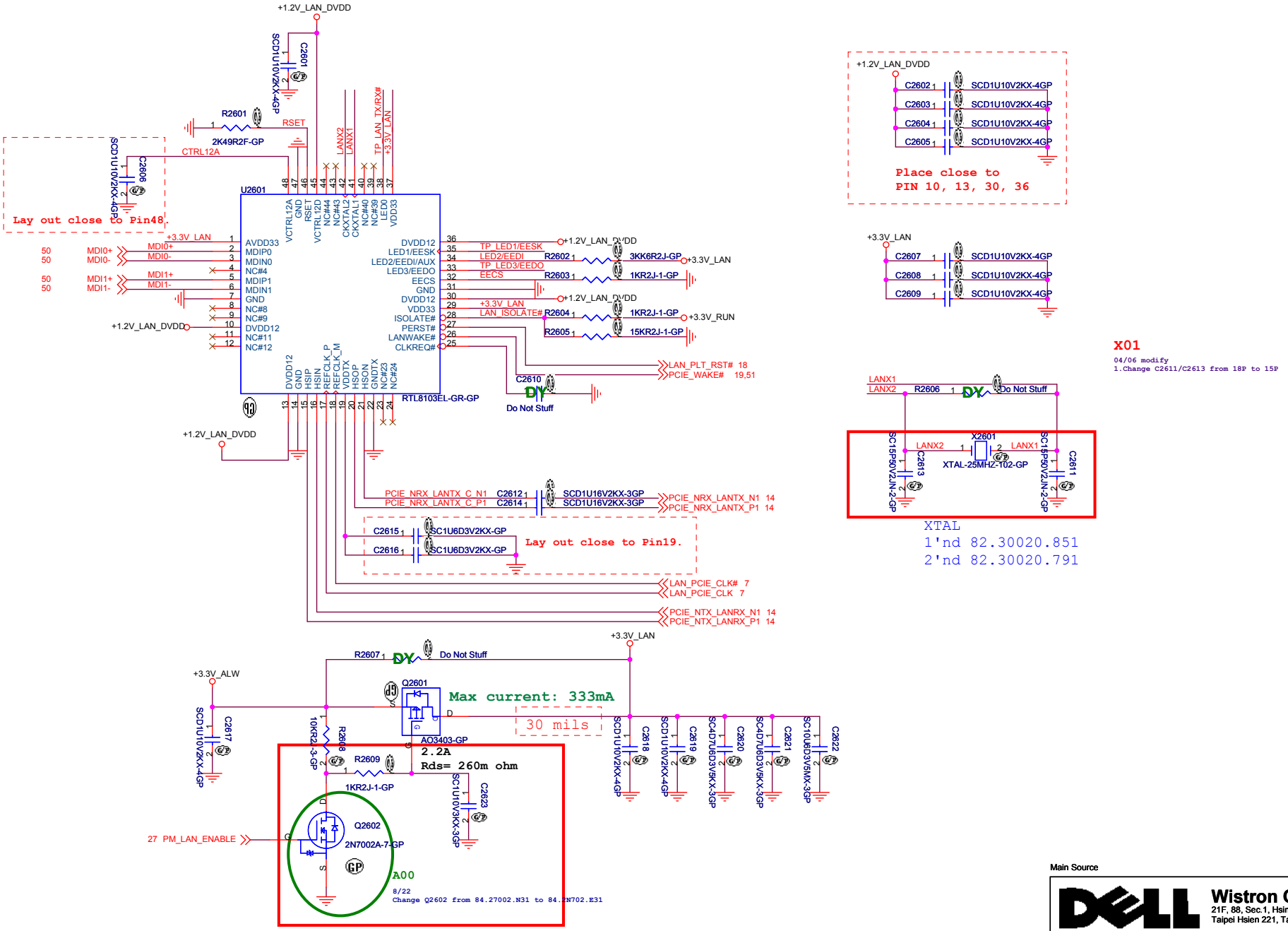
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Card Reader Realtek RTS5159**

Size	Document Number	Rev
Custom	Riya Discrete	A00

Date: Wednesday, August 26, 2009 Sheet 25 of 65

SSID = LOM



XTAL
1'nd 82.30020.851
2'nd 82.30020.791

X01
04/06 modify
1.Change C2611/C2613 from 18P to 15P

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Realtek RTL8103EL**

Size	Document Number	Rev
A3	Riya Discrete	A00

Date: Wednesday, August 26, 2009 Sheet 26 of 65

SSID = KBC

KBC_SHBM	SHBM
1 (EMPTY R2713)	Disables
*0 (STUFF R2713)	Enable

*DEFAULT

SB TYPE	D2704	R2734	R2735
*SB700	STUFF	STUFF	EMPTY
SB710	EMPTY	EMPTY	STUFF

*DEFAULT

MB VERSION ID	VER2	VER1	VER0
X00	0	0	0
X01	0	0	1
X02	0	1	0
* -1	0	1	1

*DEFAULT

X01
06/09 modify
1.Connect net LCD_EC_DET to I/O connector

X01
04/14 Change
1.Change netname from HP_MUTE to HP_MUTE#
04/14 Del
1.Del R2705 ,reserve closed-gap.

A00
8/22
Change U2702 from 84.27002.B3F to 84.DMN66.03F

A00
8/22
Change R2723,R2724 from 0 ohm to short pad

X01
04/06 modify
1.Add EC LCD_EC_DET To detect LCD Size
06/09 modify
1.Del R2736 R2737

X01
04/14 Del
1.Del R2731 ,reserve closed-gap.

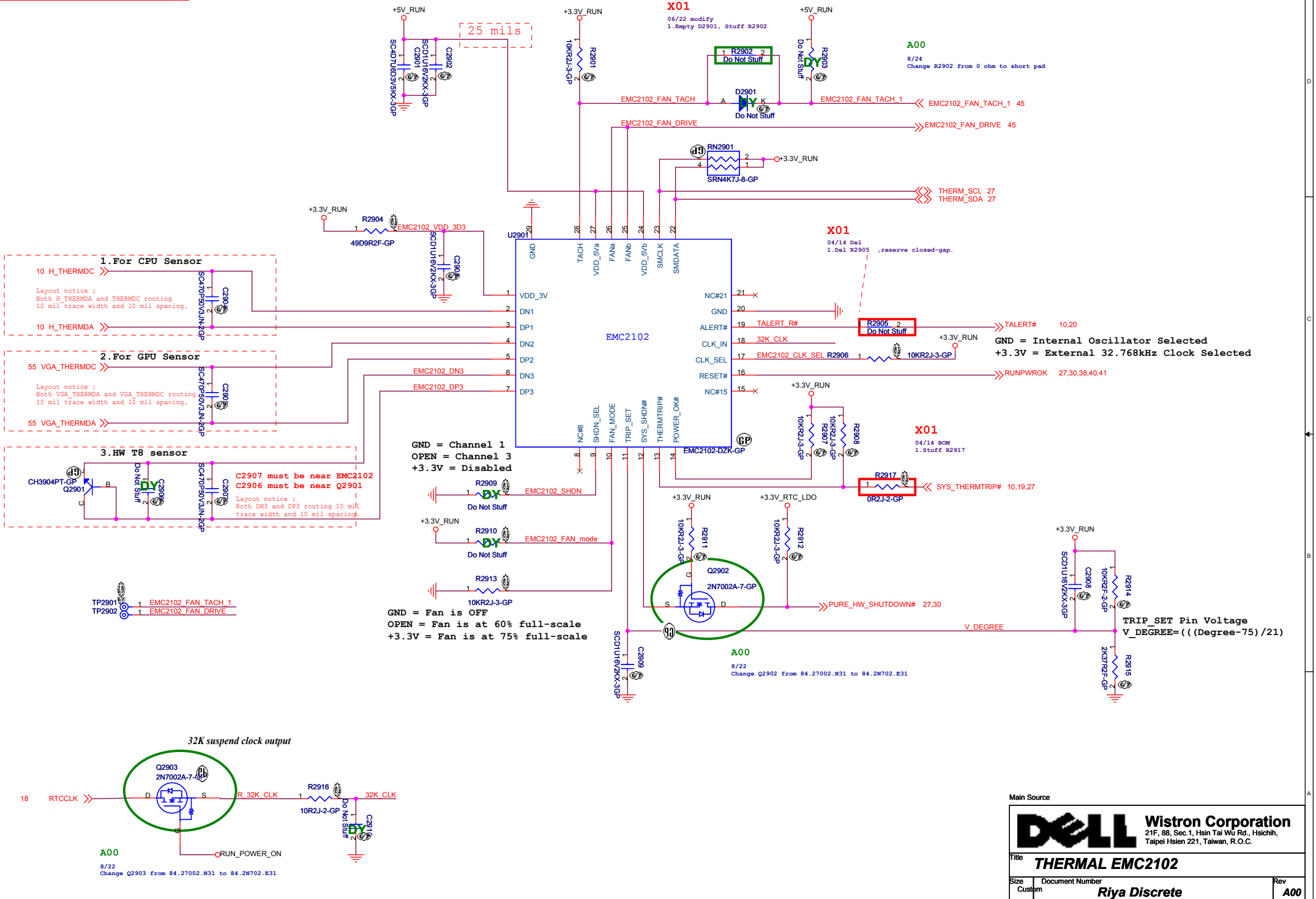
KBC CLK
EMI

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC WPCE773L
Size: Custom | Document Number: Riya Discrete | Rev: A00
Date: Wednesday, September 09, 2009 | Sheet 27 of 65

SSID = Thermal

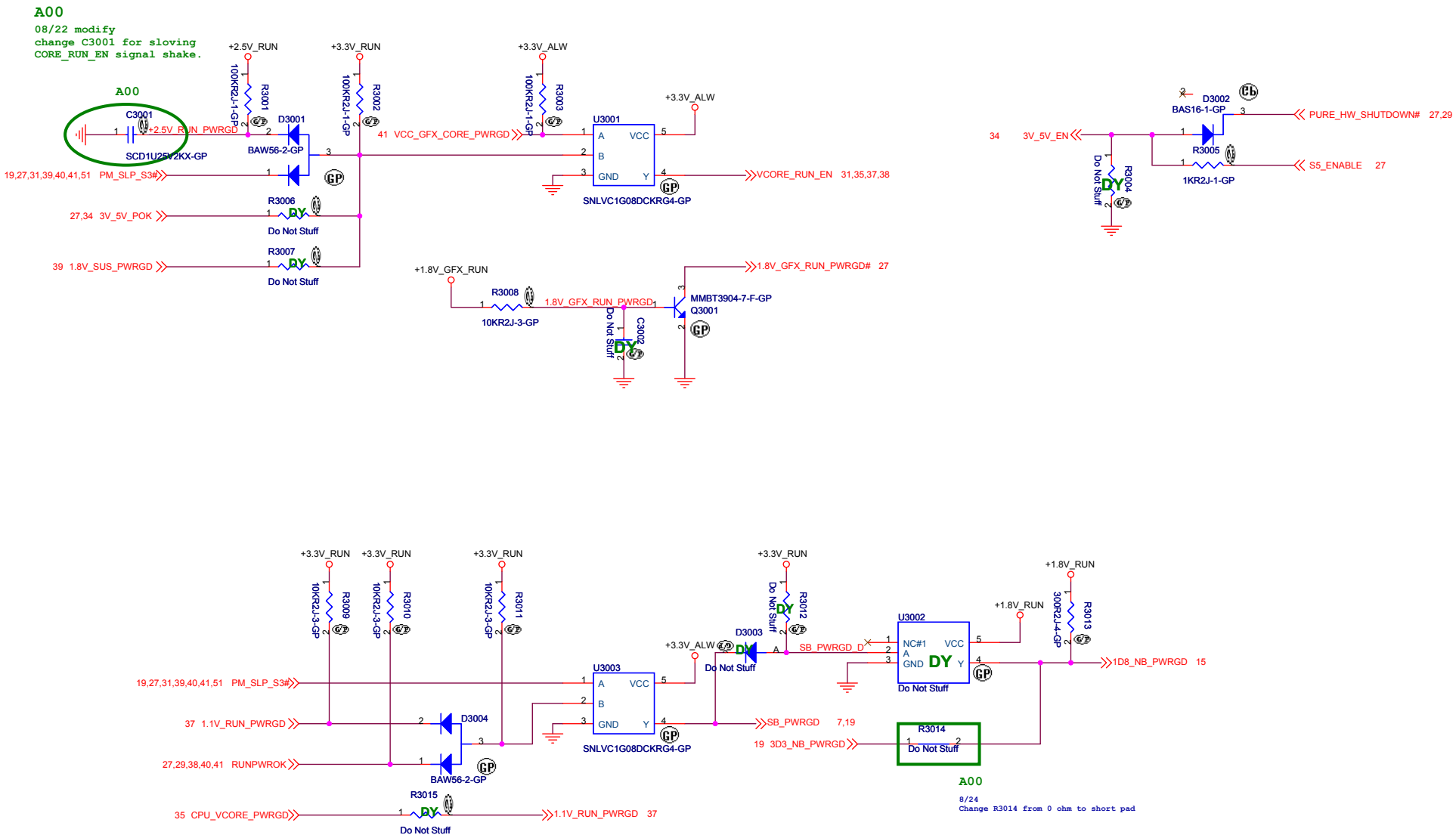


Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	THERMAL EMC2102	
Size: Custom	Document Number: Riya Discrete	Rev: A00
Date: Wednesday, August 26, 2009	Sheet 29 of 65	

SSID = Reset.Suspend

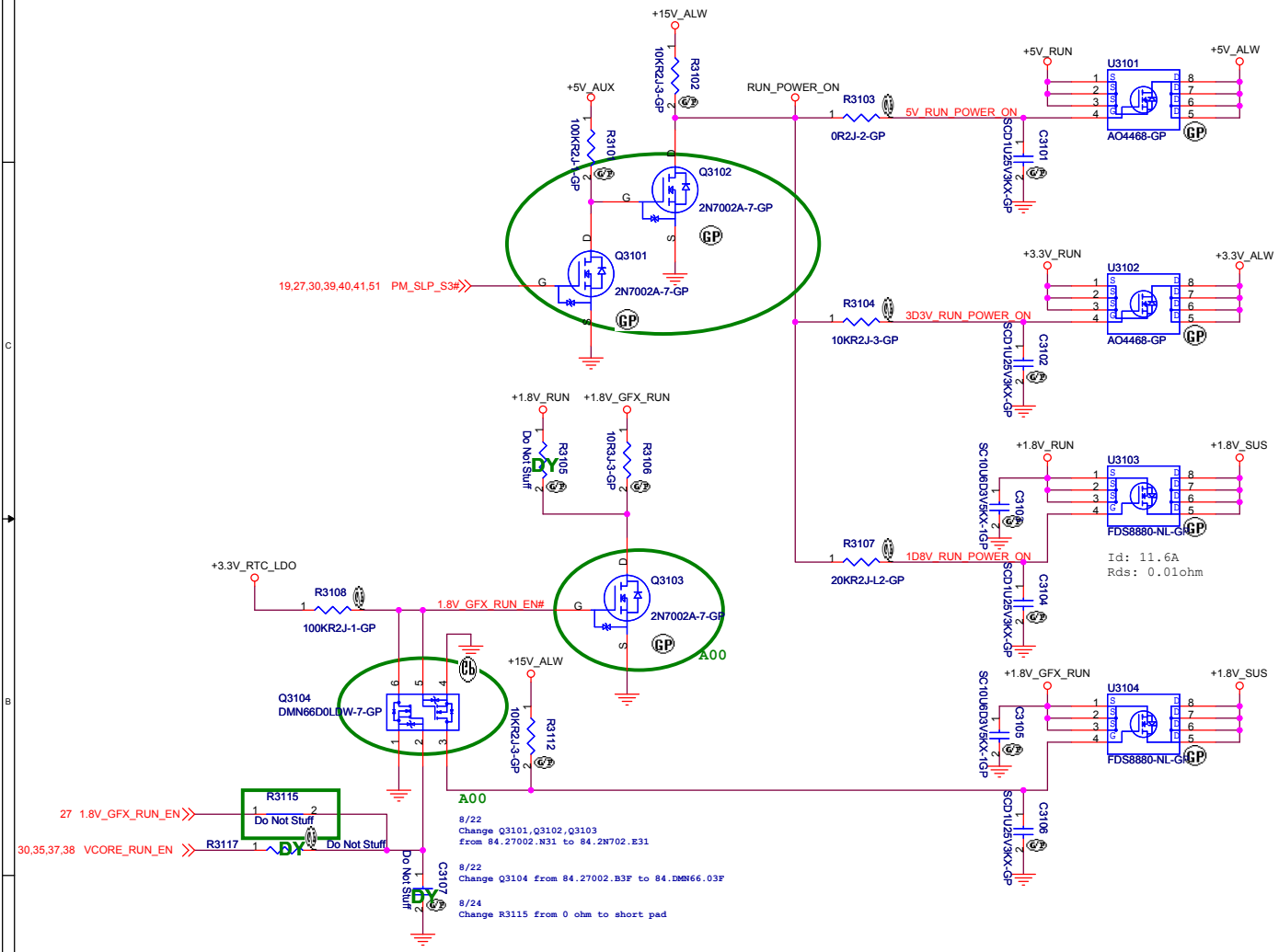


Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power On Logic***		
Size: A3	Document Number: ***Riya Discrete***	Rev: ***A00***
Date: Wednesday, August 26, 2009	Sheet 30 of 65	

Run Power



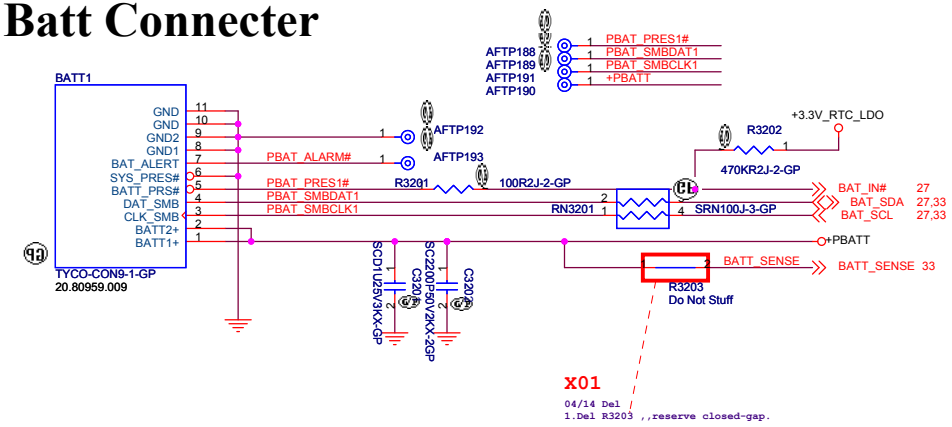
Main Source

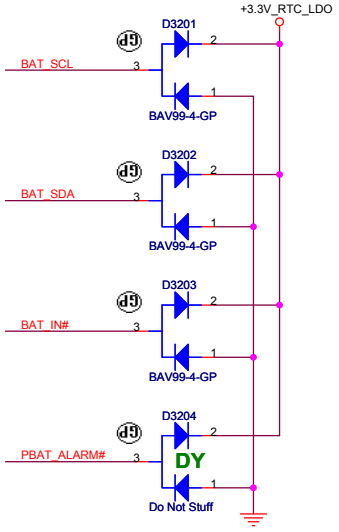
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Plane Enable***		
Size: Custom	Document Number: ***Riya Discrete***	Rev: ***A00***
Date: Wednesday, August 26, 2009	Sheet 31 of 65	

(Blanking)

Batt Connecter





Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC IN/BATT CONN		
Size: Custom	Document Number: Riya Discrete	Rev: A00
Date: Wednesday, August 26, 2009	Sheet 32 of 65	

Adaptor In Soft-Start Circuit

SSID = Charger

Id=-12A
Qg=-39nC
Rdson=38mohm

Layout Trace 250mil

Layout Trace 300mil

Layout Trace 300mil

Layout Trace 300mil

Id=-12A
Qg=-39nC
Rdson=38mohm

Id=9A
Qg=-13nC
Rdson=30mohm

DELTA
I=7A ΔL<50%
Rdson=24mohm

Id=9A
Qg=-13nC
Rdson=30mohm

X01
04/14 Del
1.Del PR3309 ,reserve closed-gap.

A00
8/22
Change PQ3301,PQ3302,PQ3303
from 84.27002.N31 to 84.2N702.E31

A00
8/24
Change PR3316 from 0 ohm to short pad

A00
9/8
Change PC3306,PC3307,PC3314,PC3315
from 78.10622.53L to 78.10622.52L

A00
8/22
Change PQ3304 from 84.27002.N31 to 84.2N702.E31

ADAPT_TRIP_SEL=1 Adapter is 90w
ADAPT_TRIP_SEL=0 Adapter is 65w

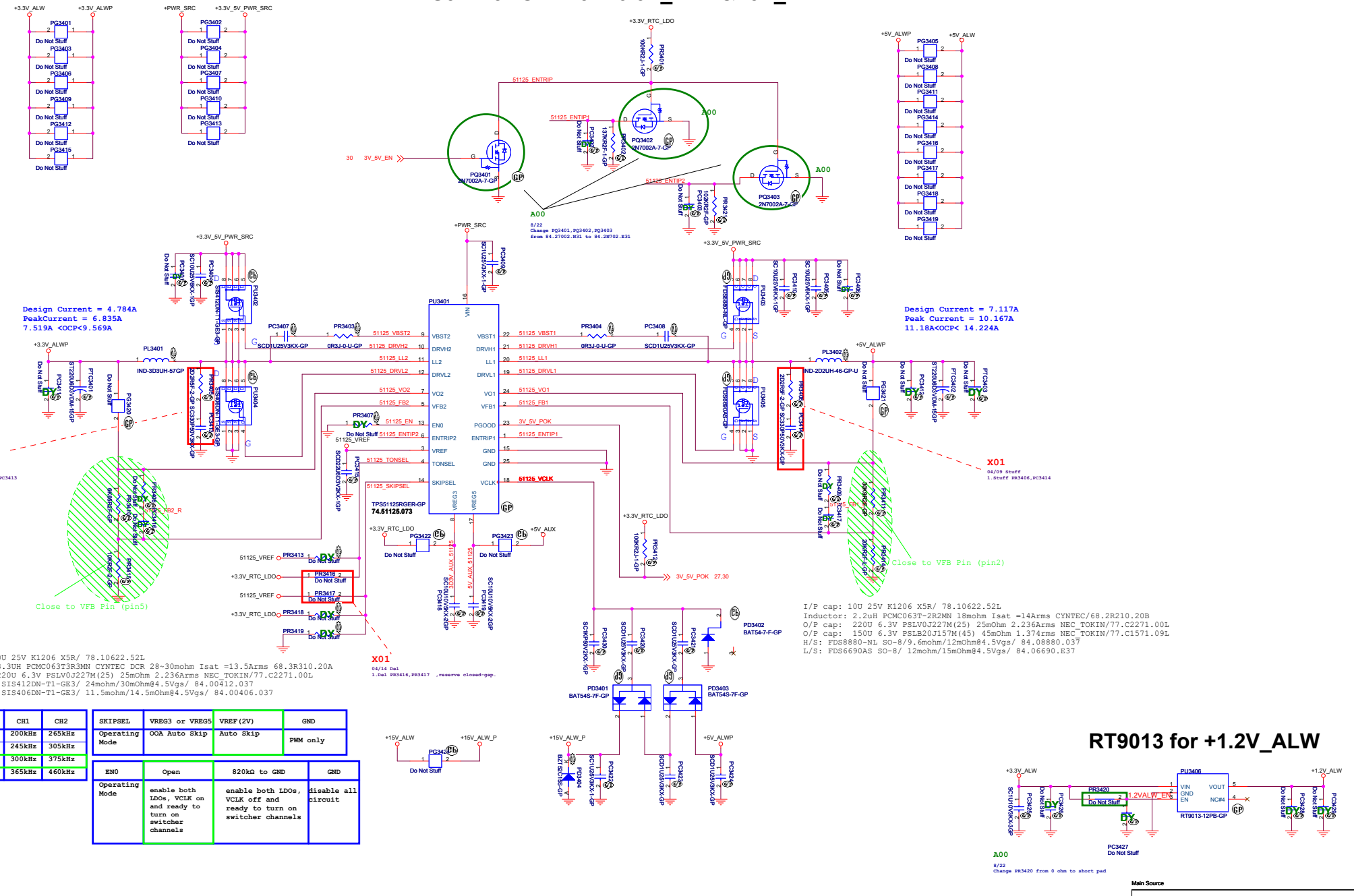
Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Charger MAX8731A	
Size: Custom	Document Number: Riya Discrete	Rev: A00
Date: Tuesday, September 08, 2009	Sheet 33 of 65	

SSID = PWR.Plane.Regulator_3p3v5v

TPS51125RGER for +3.3V_ALW&+5V_ALW



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMC063T3R3MN CYNTEC DCR 28~30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: 220U 6.3V PSLV0JJ227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
H/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S:VISHAY SIS406DN-T1-GE3/ 11.5mohm/14.5mOhm@4.5Vgs/ 84.00406.037

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN 18mohm Isat =14Arms CYNTEC/68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 150U 6.3V PSLB20J157M(45) 45mOhm 1.374rms NEC_TOKIN/77.C1571.09L
H/S: FDS8880-NL SO-8/9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

RT9013 for +1.2V_ALW

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: VREG : +3.3V_ALW&+5V_ALW

Size	Document Number	Rev
A2	Riya Discrete	A00

Date: Wednesday, August 26, 2009 Sheet 34 of 65

SSID = CPU.Regulator

ISL6265HRTZ-T for +VCC_CORE&+VDDNB

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor:4.7uH PCMC063T-4R7MN 35mohm Isat =10Arms CYNTEC/68.4R710.20D
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S:VISHAY SIS406DN-T1-GE3/ 11.5mohm/14.5mOhm@4.5Vgs/ 84.00406.037

X01
04/14 Del
1.Del PR3509 ,reserve closed-gap.

X01
04/14 Del
1.Del PR3517,PR3518 reserve closed-gap.

X01
04/06 Change
1.Change PR3507 from 4.53k to 3.32k.

X01
06/11 modify
1.Change PU3501 Ver. from ISL6265HRTZ to ISL6265AHRTZ

PU3501
ISL6265AHRTZ-T-GP

A00
8/22
Change PR3506,PR3514,PR3519,PR3529,PR3530,PR3532,PR3534 from 0 ohm to short pad
9/3
Change PR3520 from 100K to 93.1K
Change PR3521 from 18K to 24K

Parallel

Close to CPU socket

CPU TYPE	PR3536	PR3507
*Griffin	10 ohm	3K32 ohm
Tigris	10K ohm	4K53 ohm

*DEFAULT

X01
04/06 Change Spec
1.Reduced OCP setting value

For power team test

X01
04/07 Change
1.Change PC3505 Footprint from 1210 to 1206.

+VDDNB
Design Current: 2.1A
Peak current: 3A
OCP_min:5A

+VCC_CORE0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A

+VCC_CORE1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J CYNTEC DCR 1.05(+5%~-5%)mohm
Isat =60Arms 68.R3610.20C
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S:VISHAY SiR462DP/ POWERPAK-8.2/810mOhm/ 4.5Vgs/ 84.00462.037
L/S:VISHAY SI7658ADP/ POWERPAK-2.3/ 2.8mOhm/ 4.5Vgs/ 84.07658.037

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

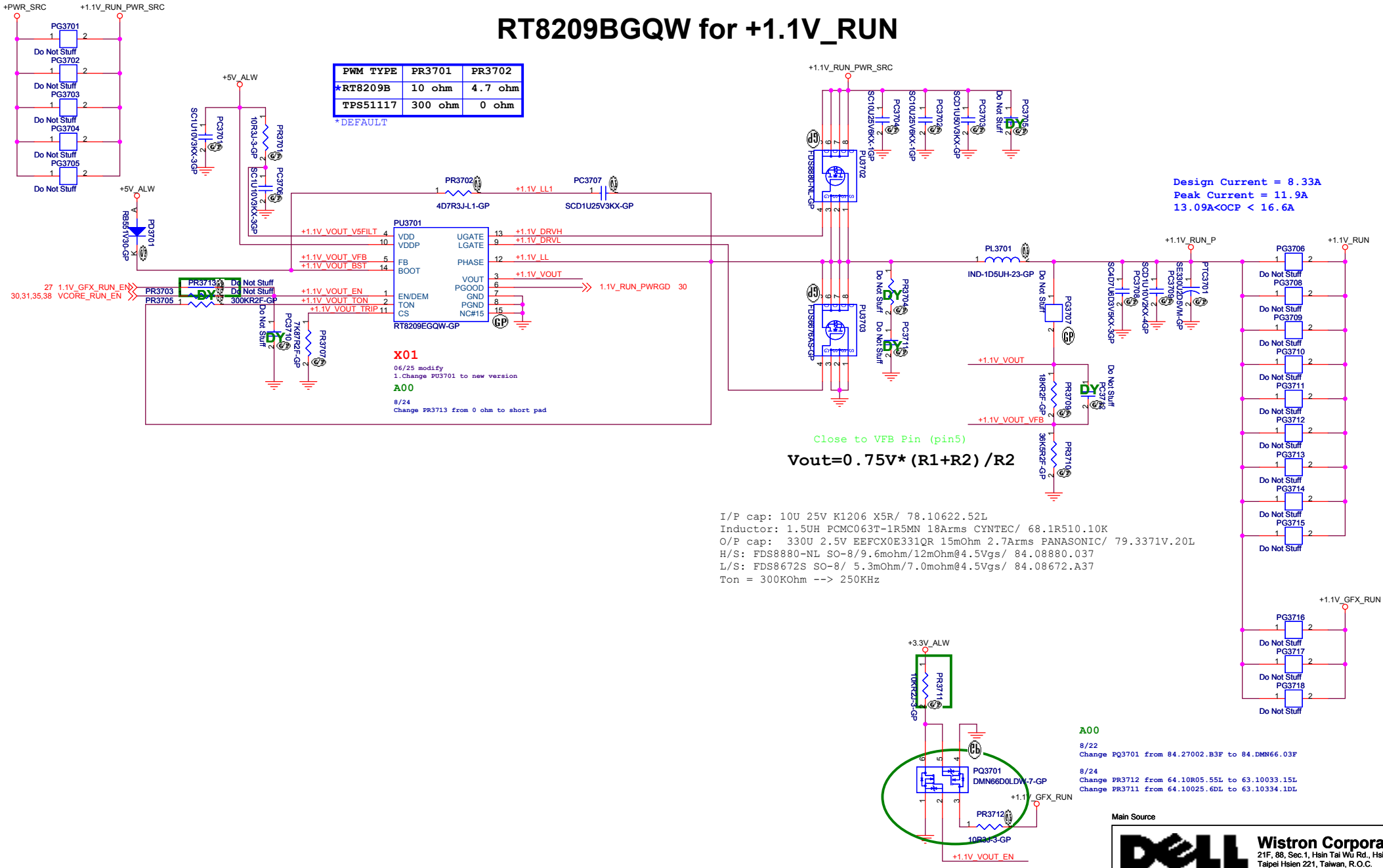
Title: VREG : +VCC_CORE&+VDDNB

Size	Document Number	Rev
A2	Riya Discrete	A00

Date: Thursday, September 03, 2009 Sheet 35 of 65

SSID = PWR.Plane.Regulator_+1.1V_RUN

RT8209BGQW for +1.1V_RUN



PWM TYPE	PR3701	PR3702
*RT8209B	10 ohm	4.7 ohm
TPS51117	300 ohm	0 ohm

*DEFAULT

X01

06/25 modify
1.Change PU3701 to new version

A00

8/24
Change PR3713 from 0 ohm to short pad

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC063T-1R5MN 18Arms CYNTEC/ 68.1R510.10K
O/P cap: 330U 2.5V EEFCX0E331QR 15mOhm 2.7Arms PANASONIC/ 79.3371V.20L
H/S: FDS8880-NL SO-8/9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Ton = 300KOhm --> 250KHz

A00

8/22
Change PQ3701 from 84.27002.B3F to 84.DMN66.03F

8/24
Change PR3712 from 64.10R05.55L to 63.10033.15L
Change PR3711 from 64.10025.6DL to 63.10334.1DL

Main Source

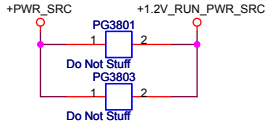
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

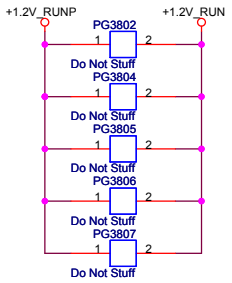
Title: VREG : +1.1V_RUN

Size	Document Number	Rev
Custom	Riya Discrete	A00

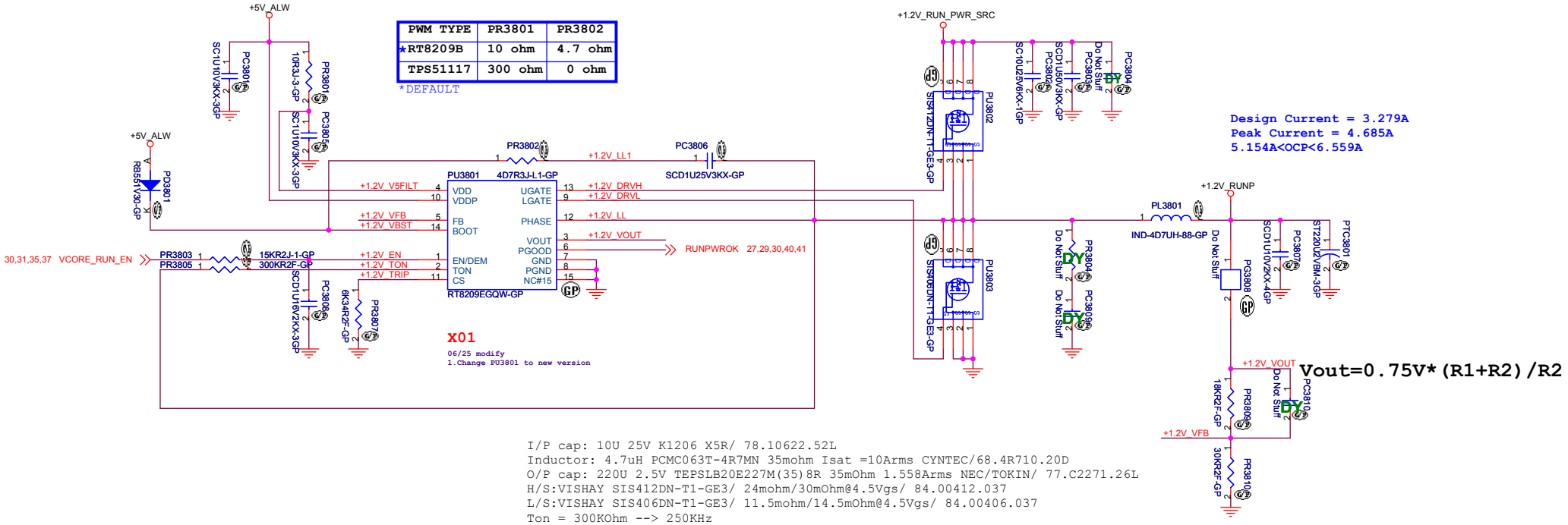
Date: Wednesday, August 26, 2009 Sheet 37 of 65

SSID = PWR.Plane.Regulator_+1.2V_RUN





RT8209BGQW for +1.2V_RUN



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 4.7uH PCMC063T-4R7MN 35mohm Isat =10Arms CYNTEC/68.4R710.20D
O/P cap: 220U 2.5V TEPSLB20E227M(35)8R 35mOhm 1.558Arms NEC/TOKIN/ 77.C2271.26L
H/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S:VISHAY SIS406DN-T1-GE3/ 11.5mohm/14.5mOhm@4.5Vgs/ 84.00406.037
Ton = 300KOhm --> 250KHz

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

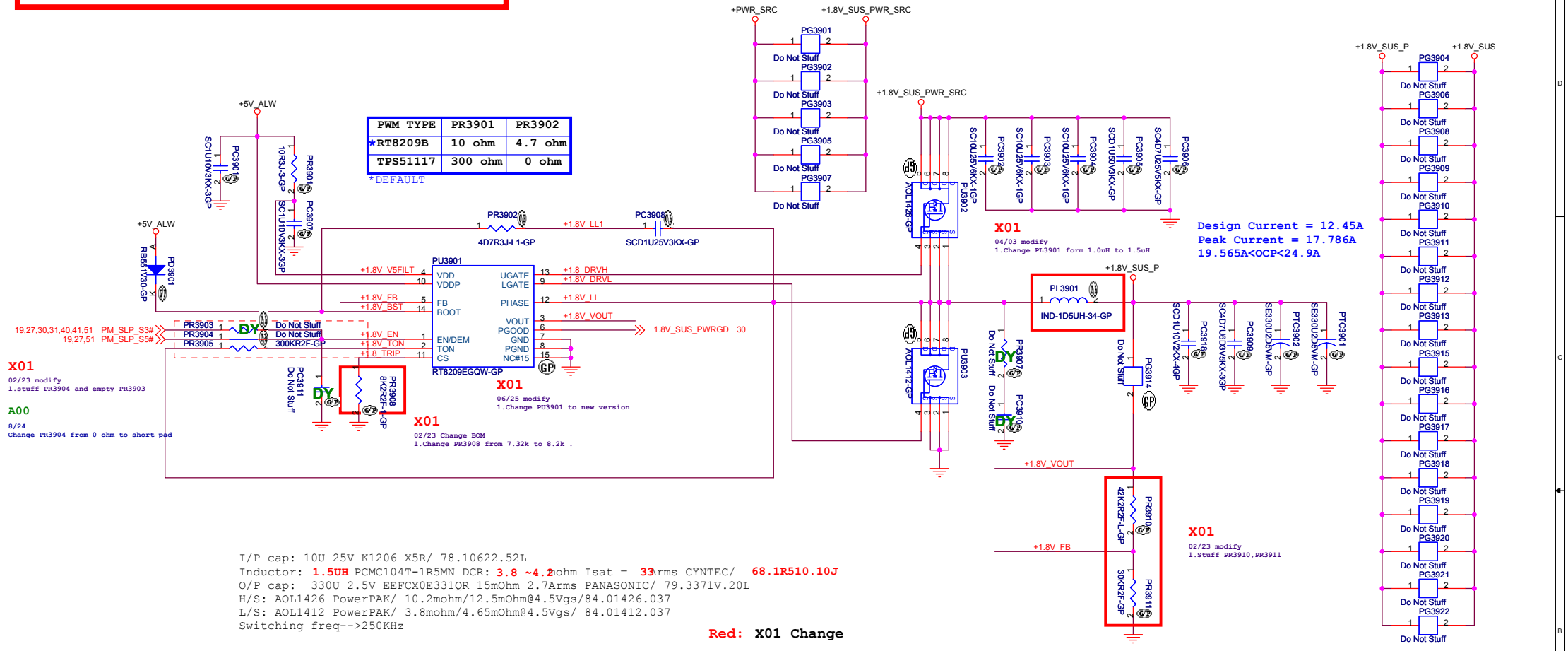
Title: VREG : +1.2V_RUN

Size	Document Number	Rev
Custom	Riya Discrete	A00

Date: Wednesday, August 26, 2009 Sheet 38 of 65

SSID = PWR.Plane.Regulator_+1.8V

RT8209BGQW for +1.8V_SUS



PWM TYPE	PR3901	PR3902
*RT8209B	10 ohm	4.7 ohm
TPS51117	300 ohm	0 ohm

*DEFAULT

X01
02/23 modify
1.stuff PR3904 and empty PR3903

A00
8/24
Change PR3904 from 0 ohm to short pad

X01
06/25 modify
1.Change PU3901 to new version

X01
02/23 Change BOM
1.Change PR3908 from 7.32k to 8.2k .

X01
04/03 modify
1.Change PL3901 form 1.0uH to 1.5uH

Design Current = 12.45A
Peak Current = 17.786A
19.565A<OCP<24.9A

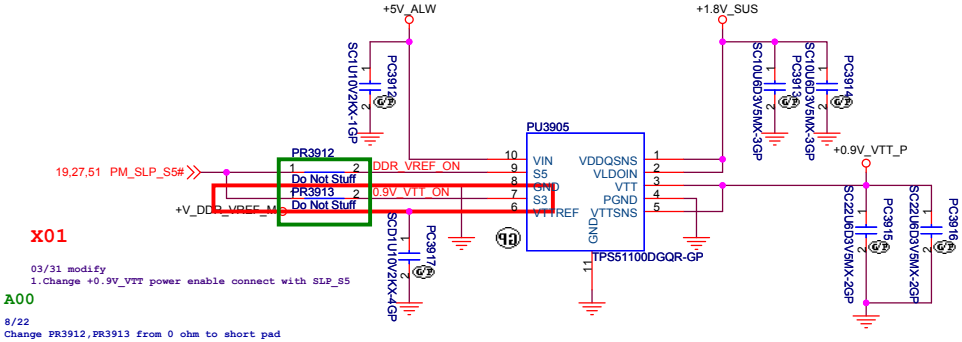
X01
02/23 modify
1.Stuff PR3910,PR3911

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN DCR: 3.8 ~4.2mohm Isat = 33Arms CYNTEC/ 68.1R510.10J
O/P cap: 330U 2.5V EEFCX0E331QR 15mOhm 2.7Arms PANASONIC/ 79.3371V.20L
H/S: AOL1426 PowerPAK/ 10.2mohm/12.5mOhm@4.5Vgs/84.01426.037
L/S: AOL1412 PowerPAK/ 3.8mohm/4.65mOhm@4.5Vgs/ 84.01412.037
Switching freq-->250KHz

Red: X01 Change

SSID = PWR.Plane.Regulator_+0.9V

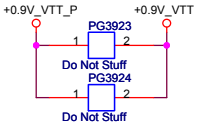
TPS51100 for +0.9V_VTT

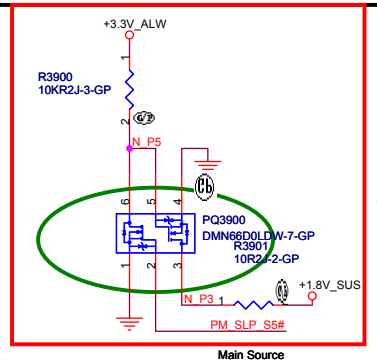


X01
03/31 modify
1.Change +0.9V_VTT power enable connect with SLP_S5

A00
8/22
Change PR3912,PR3913 from 0 ohm to short pad

Design Current = 1.225A
Peak Current = 1.75A





X01
04/15 modify
1.Use discharge circuit for power on/off.

A00
8/22
Change PQ3900 from 84.27002.B3F to 84.DMN66.03F

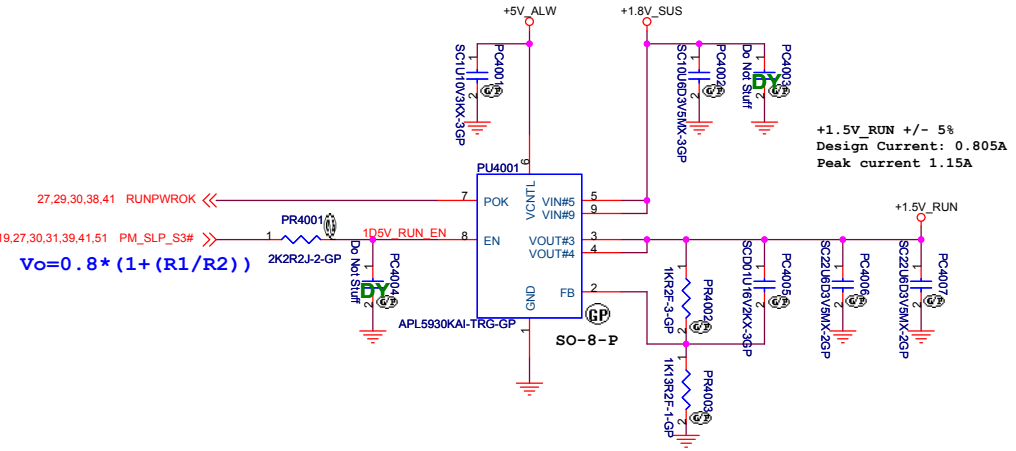
Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
VREG : +1.8V_SUS&+0.9V_VTT		
Size: Custom	Document Number: Riya Discrete	Rev: A00
Date: Wednesday, August 26, 2009	Sheet 39 of 65	

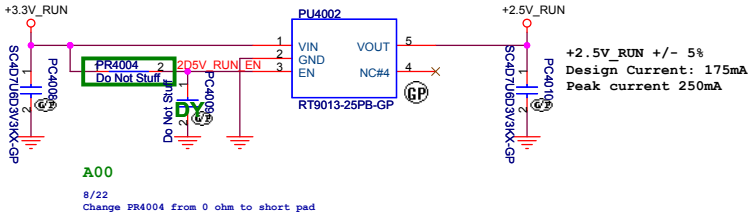
SSID = PWR.Plane.Regulator_1p5v

APL5930KAI for +1.5V_RUN



SSID = PWR.Plane.Regulator_2p5v

RT9013-25PB for +2.5V_RUN



Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VREG : +1.5V_RUN&+2.5V_RUN	
Size: Custom	Document Number: Riya Discrete	Rev: A00
Date: Wednesday, August 26, 2009	Sheet 40 of 65	

SSID = Video.PWR.Regulator

TPS51117RGYR for +VCC_GFX_CORE

+VCC_GFX_CORE +/- 5%
Design Current: 8.232A
Peak current 11.76A
12.936<OCP<16.464

X01
02/23 modify
1.change PR4103 from 3.3 ohm to 300 ohm

Please place near KBC U2701.

f=250kHz,Ton resister =300k

A00
8/24
Change PR4105 from 0 ohm to short pad

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
X	H	1.05V
X	X	
X	X	
X	L	0.90V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN DCR:3.8 ~4.2mohm Isat =33Arms CYNTEC/ 68.1R510.10J
O/P cap: 330U 2.5V EEFCX0E331QR 15mOhm 2.7Arms PANASONIC/ 79.3371V.20L
H/S: FDS8880-NL SO-8/9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq-->250KHz

A00
0903
Change PR4111 from 154K to 52.3K
Change PC4112 from 0.047u to 0.1u

X01
04/14 Del
1.Del PR4117,PR4122 ,reserve closed-gap.

A00
08/22 modify
1.DY PWRCNTL_0 circuit
2.change PR4117,PR4122 to short pad
3.change PQ4101 & PQ4104 to high level ESD MOS

Id: 2A
Rds: 0.15ohm

A00
8/22
Change PQ4103 from 84.27002.B3F to 84.DMN66.03F

A00
8/24
Change PR4101 from 0 ohm to short pad

Optional RC network
to fine tune PWR SEQ.

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

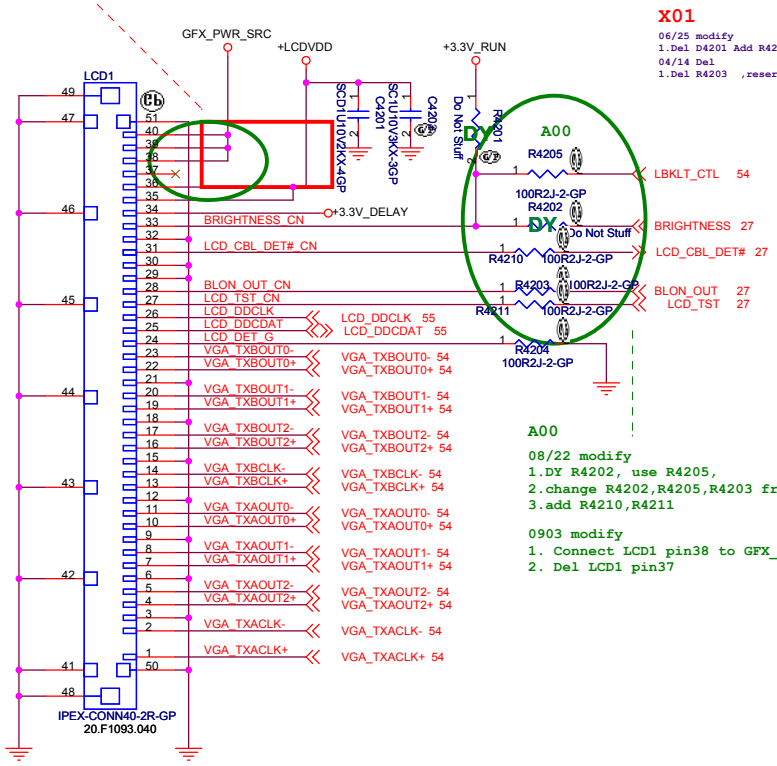
Title: VREG : +VCC_GFX_CORE
Size: A3 | Document Number: Riya Discrete | Rev: A00
Date: Tuesday, September 08, 2009 | Sheet 41 of 65

SSID = VIDEO

LVDS CONNECTOR

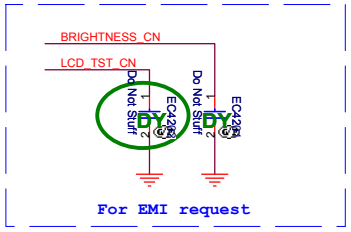
X01
06/09 modify
1. Connect LCD1 pin37 to +LCDVDD
2. Del LCD1 pin38

X01
06/25 modify
1.Del D4201 Add R4205
04/14 Del
1.Del R4203 ,reserve closed-gap



A00
08/22 modify
1.DY R4202, use R4205,
2.change R4202,R4205,R4203 from 0 to 100ohm
3.add R4210,R4211

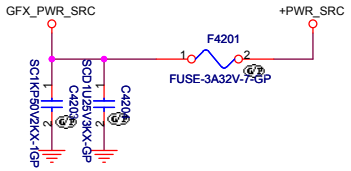
0903 modify
1. Connect LCD1 pin38 to GFX_PWR_SRC
2. Del LCD1 pin37



A00
08/27 modify
1.Chang EC4202 Pin1 from LCD_TST to LCD_TST_CN

SSID = Inverter

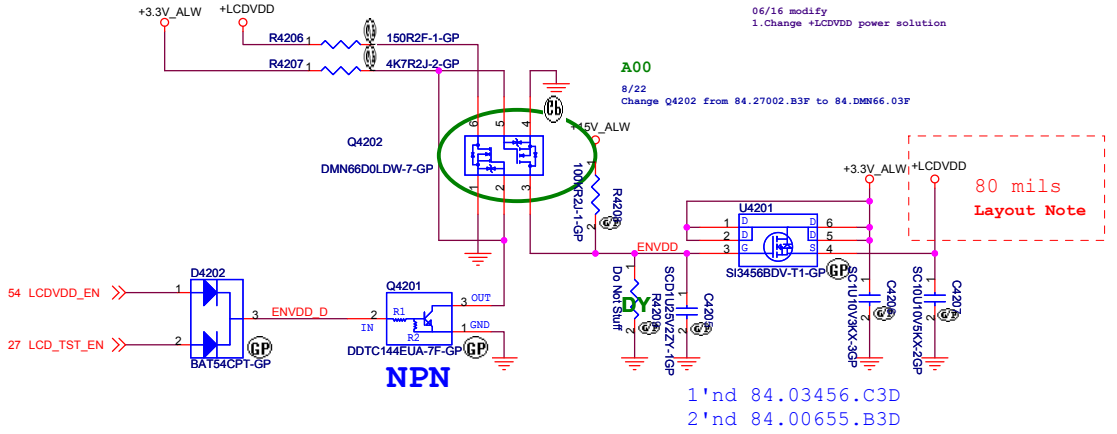
INVERTER POWER



SSID = VIDEO

LCD POWER

X01
06/16 modify
1.Change +LCDVDD power solution



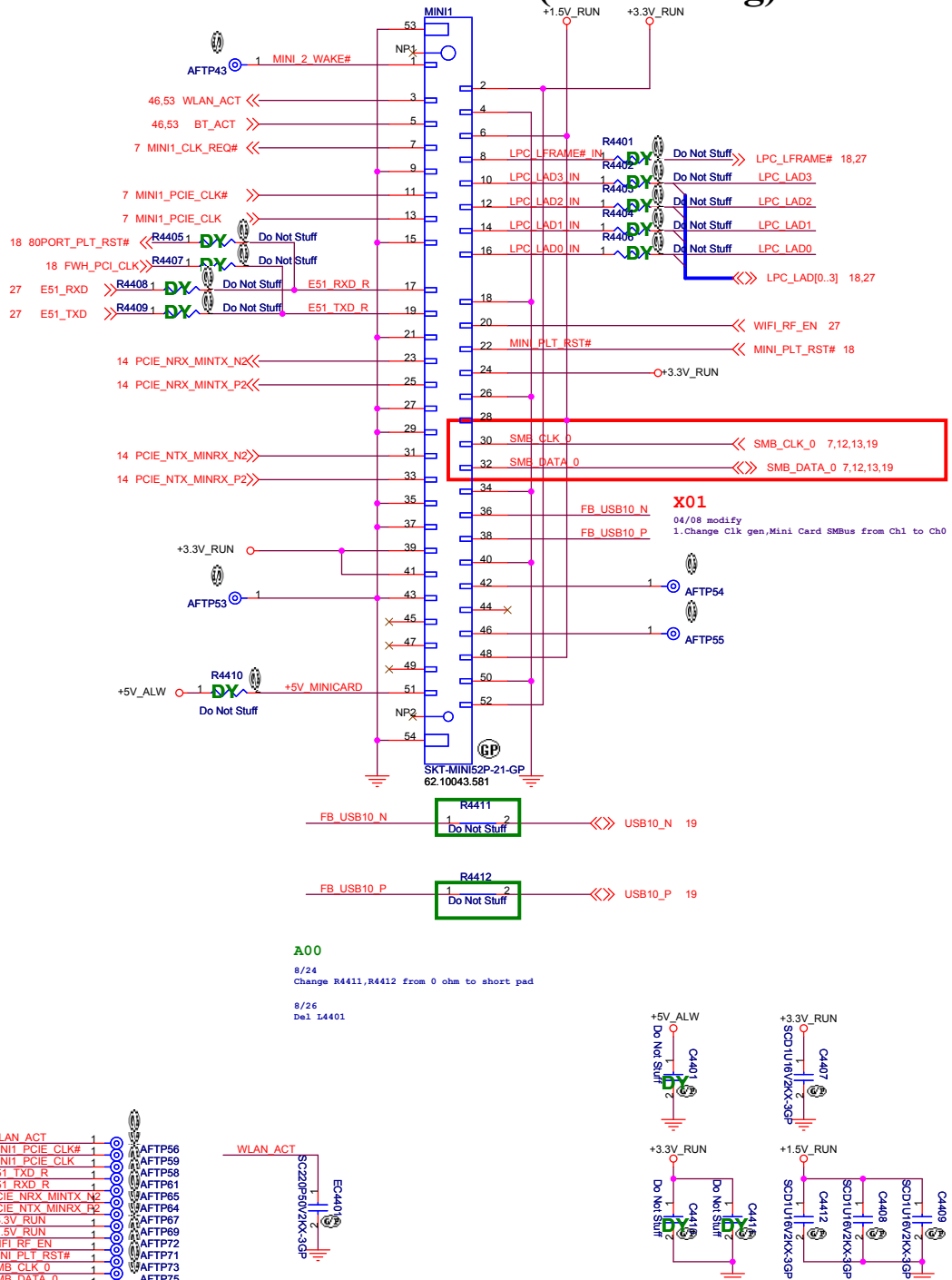
Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD&Inverter CONN	
Size: Custom	Document Number: Riya Discrete	Rev: A00
Date: Thursday, September 03, 2009	Sheet 42 of 65	

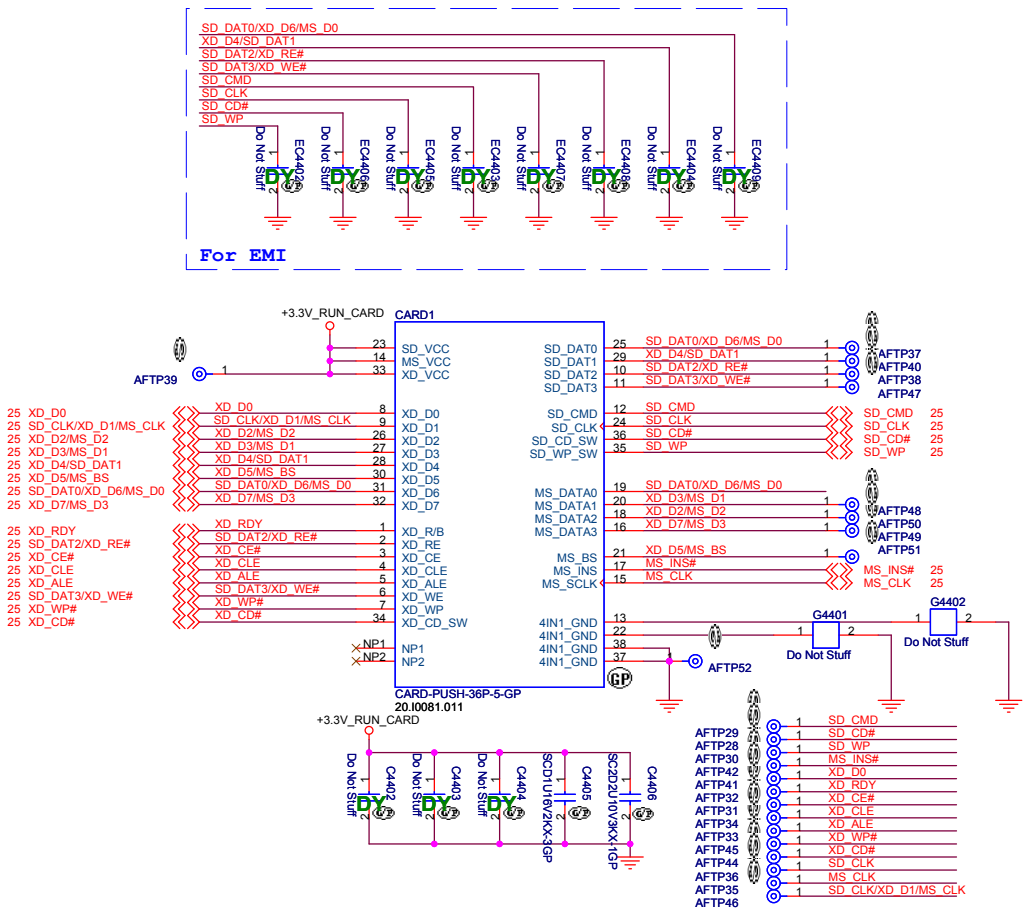
SSID = Wireless

Mini Card Connector(802.11a/b/g)



SSID = SDIO

SD/XD/MS Card Reader



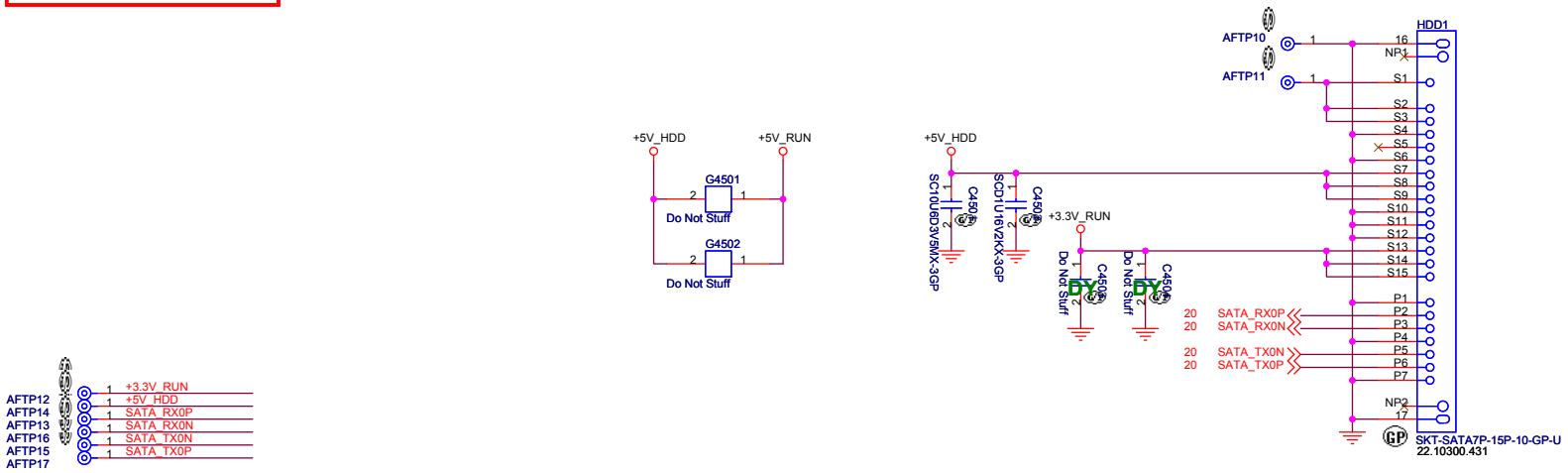
Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MiniCard&Card Reader CONN		
Size: Custom	Document Number: Riya Discrete		Rev: A00
Date: Wednesday, August 26, 2009	Sheet 44	of	65

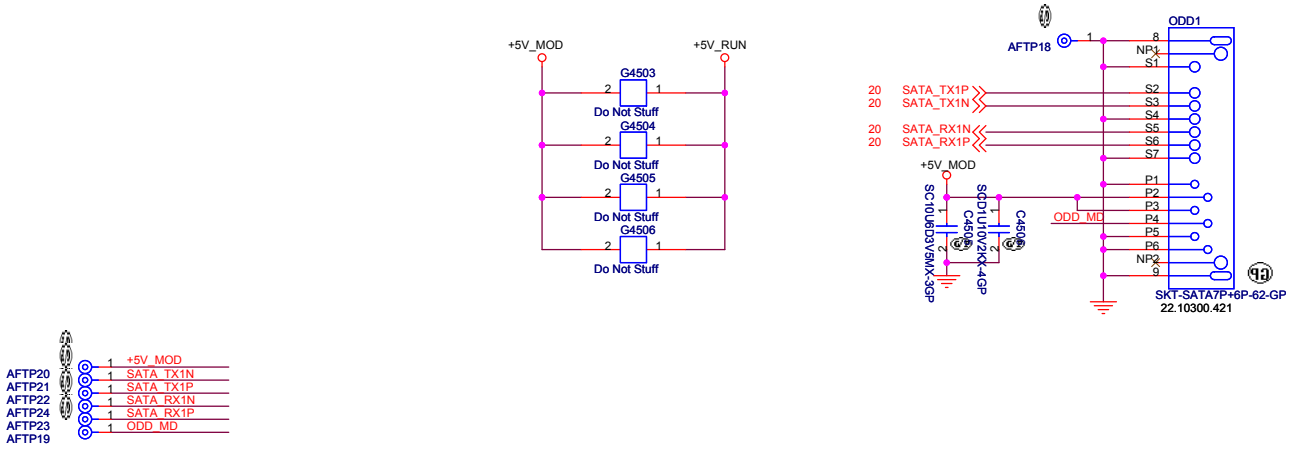
SSID = SATA

SATA HDD Connector



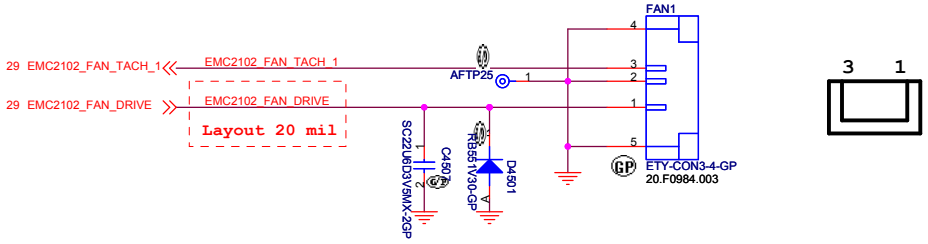
SSID = SATA

ODD Connector



SSID = Thermal

Fan Connector



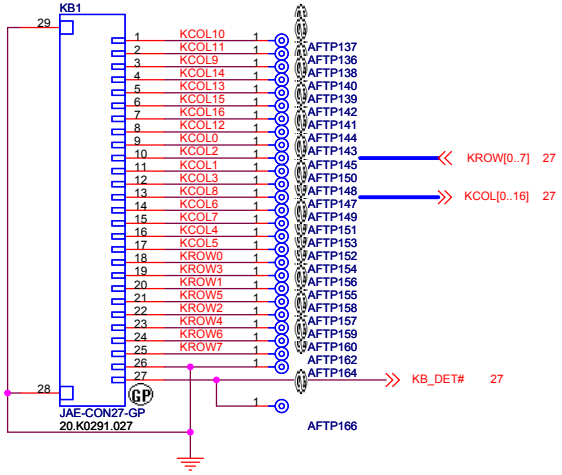
Main Source

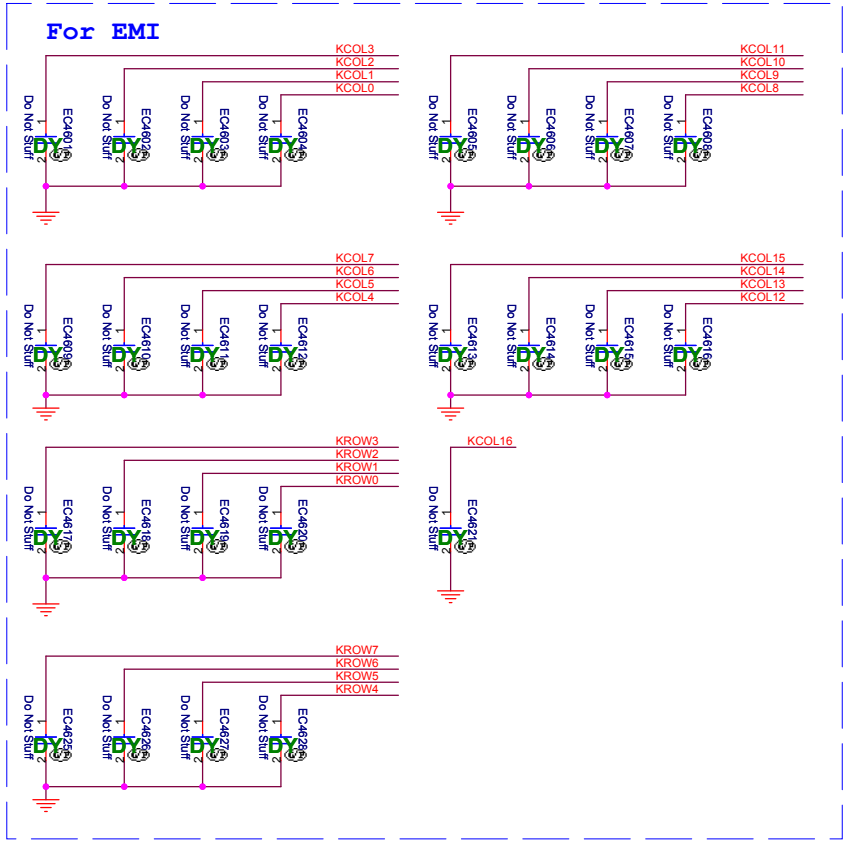
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD&ODD&FAN CONN		
Size: Custom	Document Number: Riya Discrete	Rev: A00
Date: Wednesday, August 26, 2009	Sheet 45 of 65	

SSID = KBC

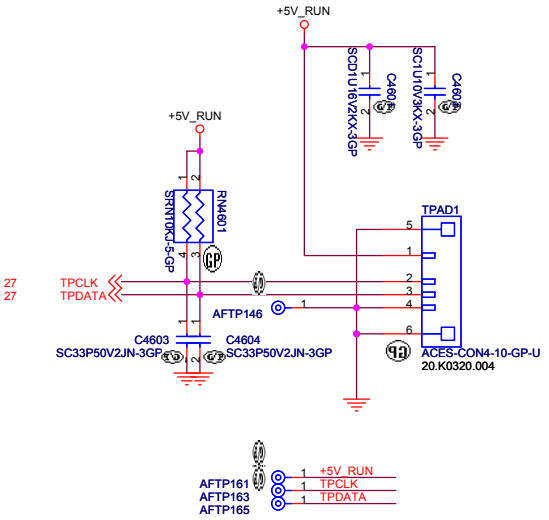
Internal KeyBoard Connector





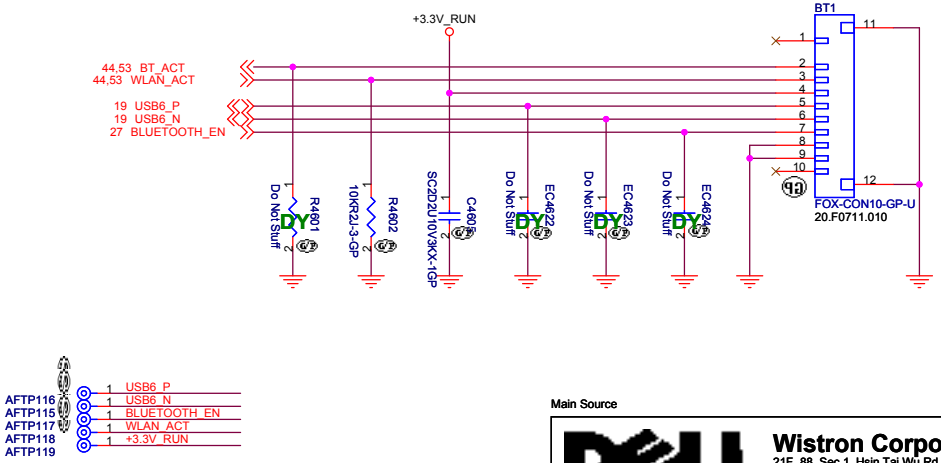
SSID = Touch.Pad

TouchPad Connector



SSID = User.Interface

Bluetooth Module conn.



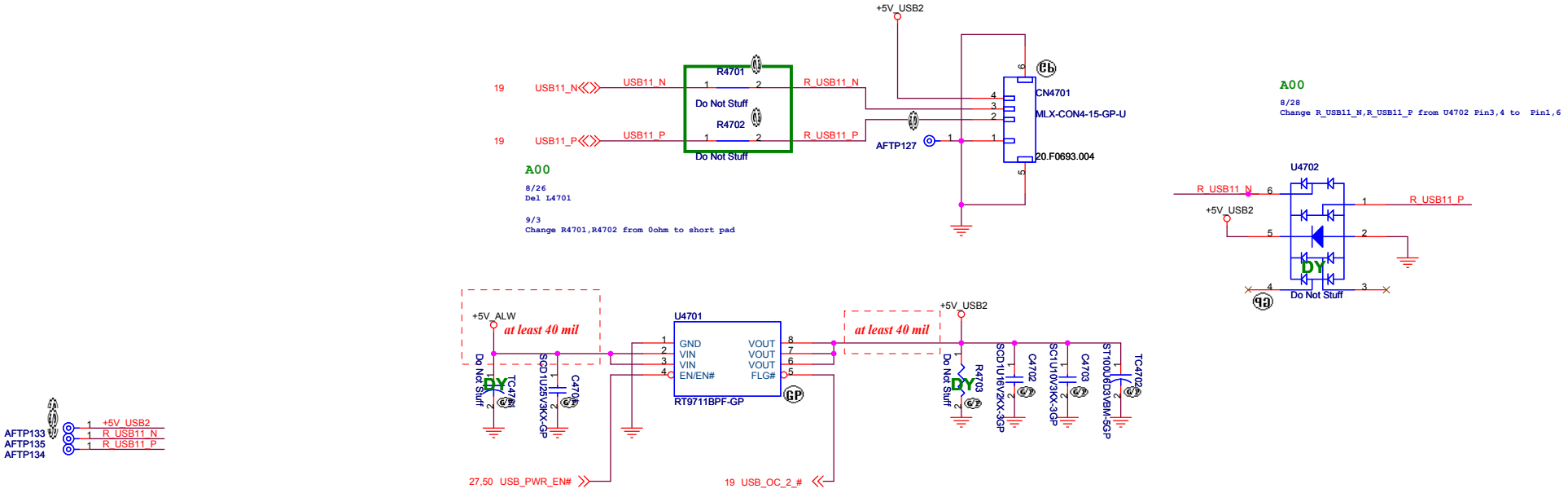
Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	KeyBoard&TouchPad&BT CONN	
Size: Custom	Document Number: Riya Discrete	Rev: A00
Date: Wednesday, August 26, 2009	Sheet 46 of 65	

SSID = USB

Right USB Port CONN



(Blanking)

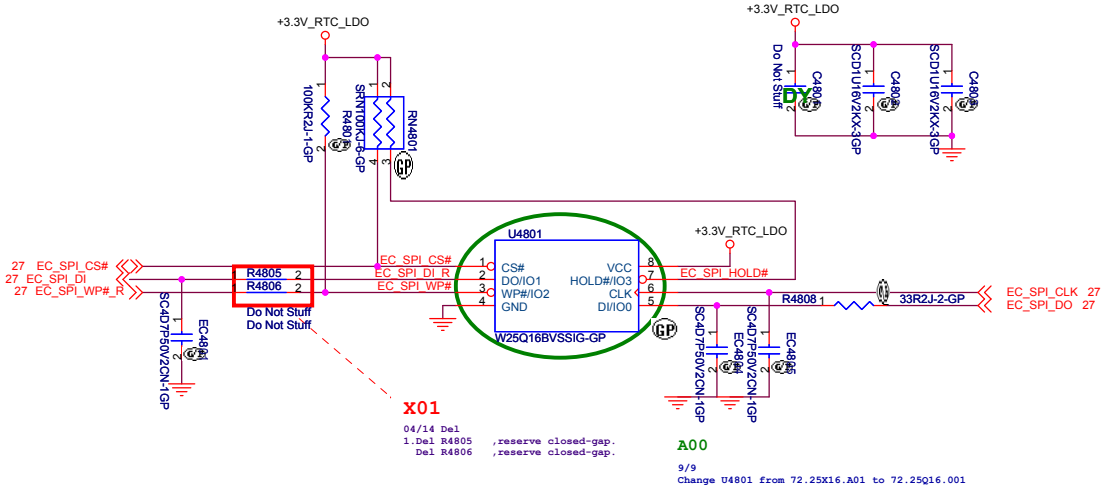
Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB CONN		
Size: Custom	Document Number: Riya Discrete	Rev: A00
Date: Thursday, September 03, 2009	Sheet 47 of 65	

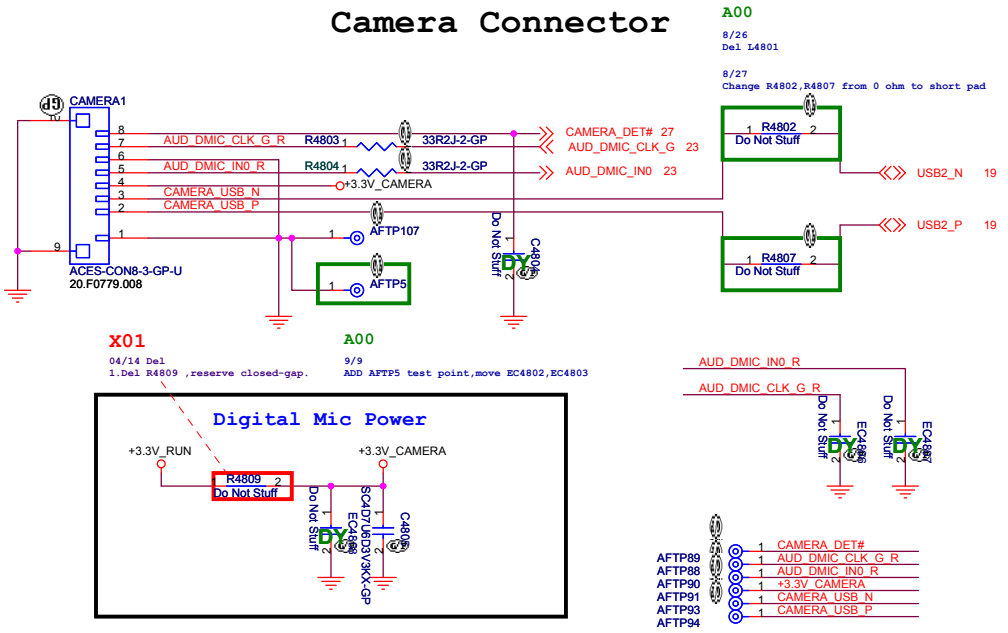
SSID = Flash.ROM

SPI FLASH ROM (16M bits)



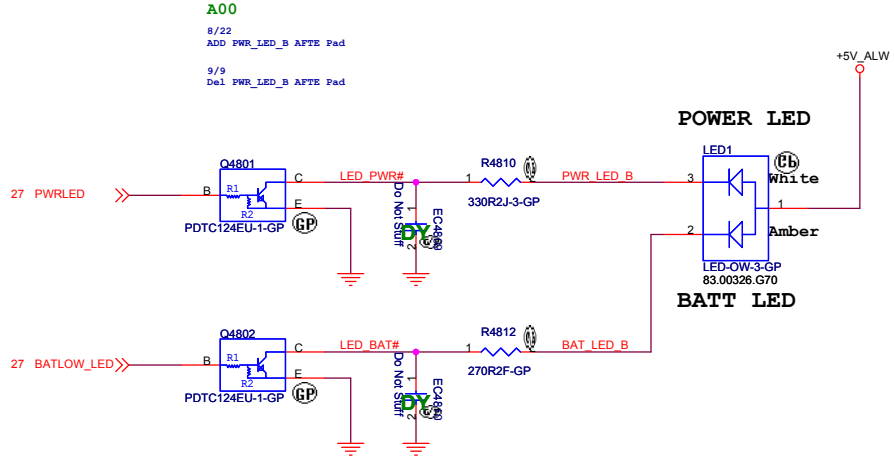
SSID = User.Interface

Camera Connector



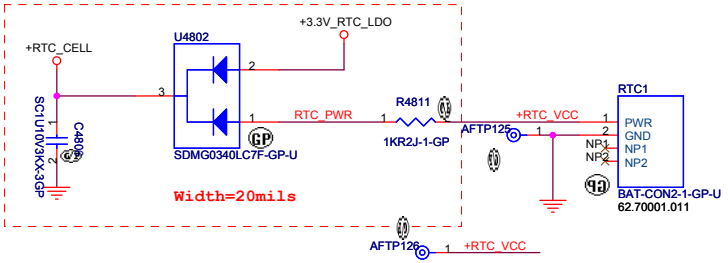
SSID = User.Interface

Power/Battery LED



SSID = RBATT

RTC Connector



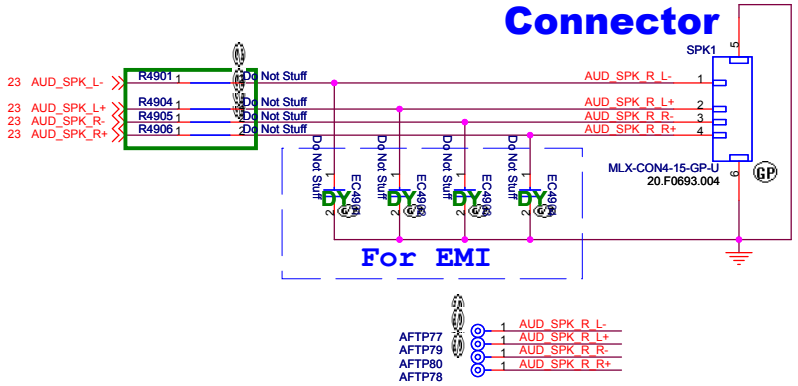
Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	EEPROM&LED&Camera&RTC CONN	
Size: Custom	Document Number: Riya Discrete	Rev: A00
Date: Wednesday, September 09, 2009	Sheet 48 of 65	

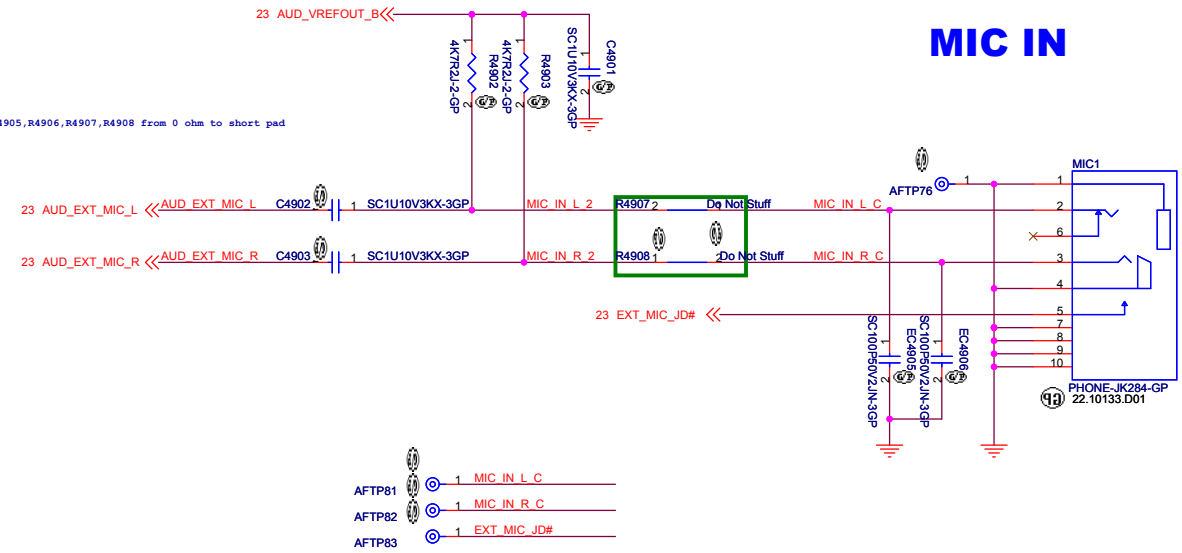
SSID = AUDIO

Speaker Connector

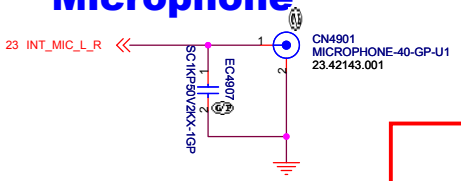


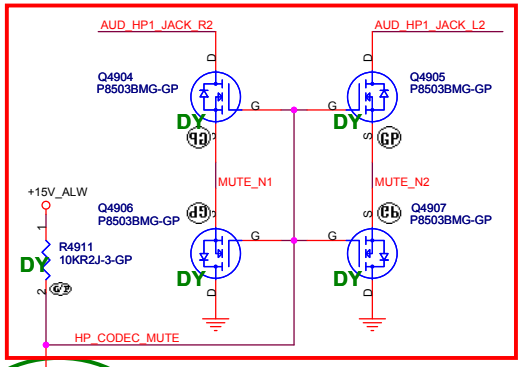
A00
8/24
Change R4901,R4904,R4905,R4906,R4907,R4908 from 0 ohm to short pad

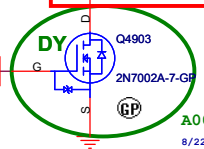
MIC IN



Internal Microphone







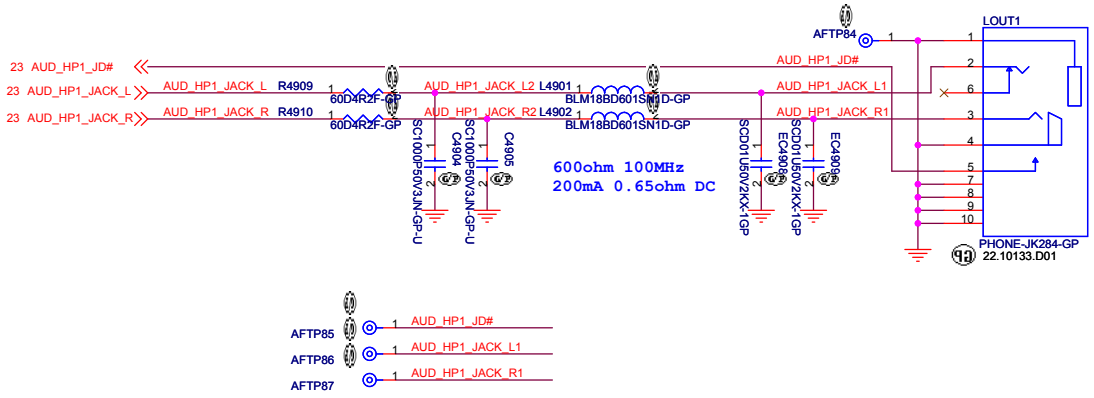
X01
04/14 Change
1.Change netname from HP_MUTE to HP_MUTE#

A00
8/22
Change Q4903 from 84.27002.N31 to 84.2N702.E31

9/8
DY Q4903,Q4904,Q4905,Q4906,Q4907.R4911

X01
03/31 modify
1.Use low RDS(on) MOSFET on audio de-pop circuit

LINE1 OUT



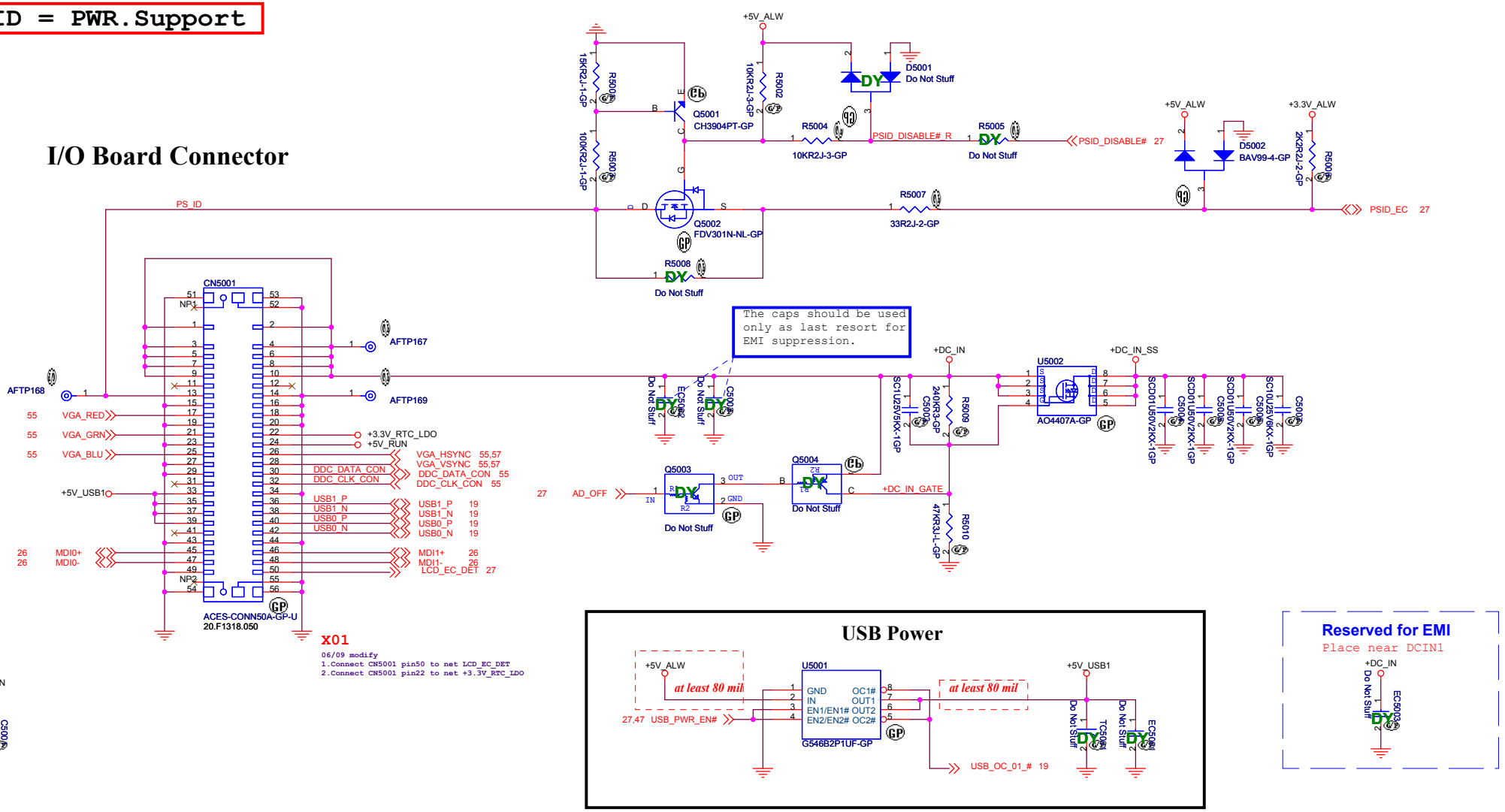
Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack		
Size: Custom	Document Number: Riya Discrete	Rev: A00
Date: Wednesday, September 09, 2009	Sheet 49 of 65	

SSID = PWR.Support

I/O Board Connector

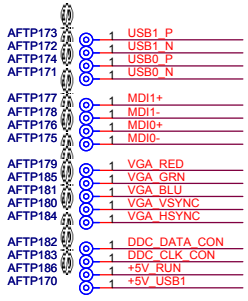


USB Power

Reserved for EMI

Place near DCIN1

+DC_IN



Main Source

DELL **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

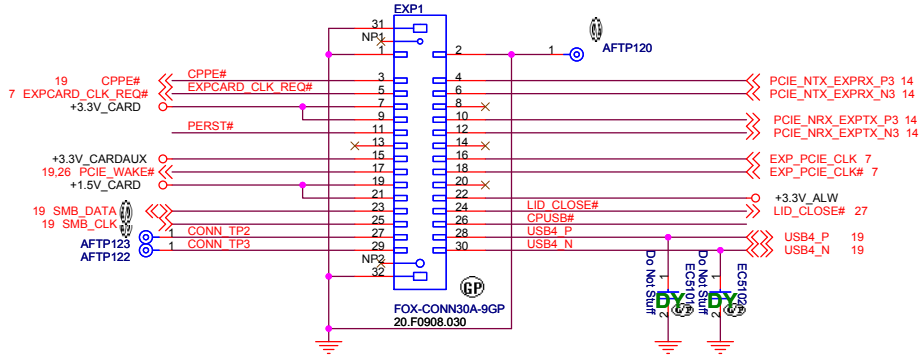
Title: **IO BOARD CONN**

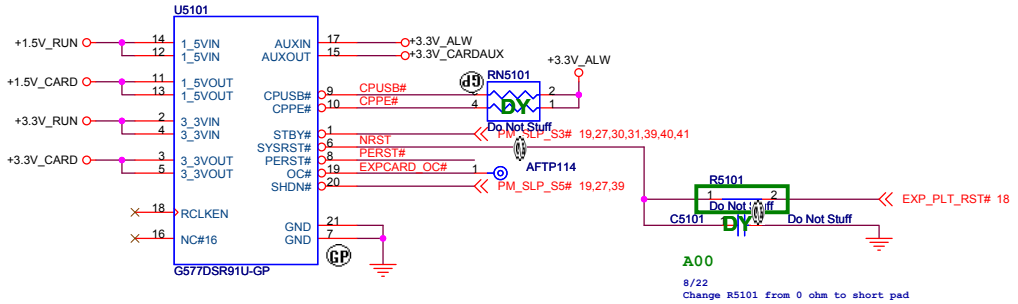
Size	Document Number	Rev
Custom	Riya Discrete	A00

Date: Wednesday, August 26, 2009 Sheet 50 of 65

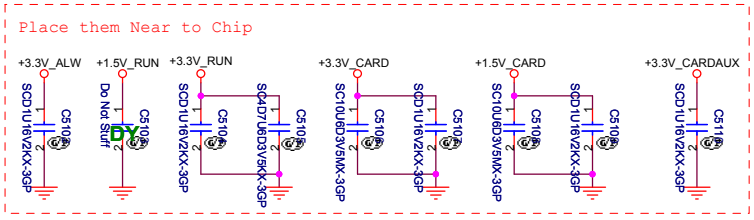
SSID = ExpressCard

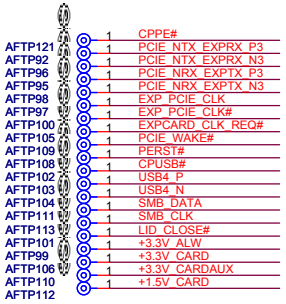
Express Card Connector





+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA





Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Express Card Board CONN

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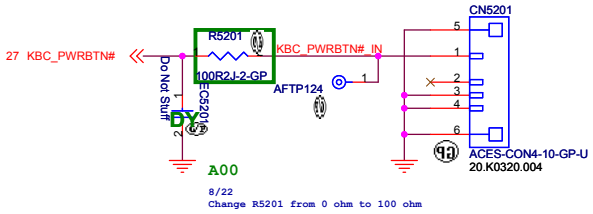
Date: Wednesday, August 26, 2009 | Sheet 51 of 65

(Blanking)

SSID = User.Interface

Power Board to Board CONN



(Blanking)

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Button&Hall Sensor&MDC		
Size: Custom	Document Number: Riya Discrete	Rev: A00
Date: Wednesday, August 26, 2009	Sheet 52 of 65	

SSID = Mechanical

For EMI

H5301 H5302 H5303 H5304 H5305 H5306
H5307 H5308 H5309 H5310 H5311
H5312 H5313

H5314 HOLE — BOTTOM
34.4W005.301
Mini Card BOSS

H5315 HOLE — TOP
34.4W004.501
New Card BOSS

H5316 HOLE — BOTTOM
34.4W001.201
NB Thermal BOSS

For BOSS

H5317 H5318 H5319 H5320

For S1G2 CPU SOCKET

SPR5301 SPRING-24-GP 34.45T31.001
SPR5302 SPRING-24-GP 34.45T31.001
SPR5303 SPRING-24-GP 34.45T31.001
SPR5304 SPRING-24-GP 34.45T31.001
SPR5305 SPRING-58-GP 34.4B312.002
SW5301 SPRING-24-GP 34.45T31.001

X01
04/16 Add
1.Add C5300,C5301,C5302,C5303,C5304,C5305

+5V_ALW: EC5313, EC5318, EC5331 (Do Not Stuff)
+3.3V_ALW
+VCC_GFX_CORE: EC5312, EC5321
+VCC_CORE0: EC5330
+3.3V_RTC_LDO: EC5301
+3.3V_RUN: SC47P50V2JN-3GP, EC5305, EC5306, EC5307, EC5308, EC5309
+5V_ALW: EC5310, EC5311
+5V_MOD: EC5316, EC5317
44,46 WLAN_ACT
44,46 BT_ACT
EC5314, EC5315
+0.9V_VTT: EC5332, EC5333, EC5334
+PWR_SRC: SCD1U25V3KX-GP, EC5322, EC5324
+PWR_SRC: EC5325, EC5326, EC5327, EC5328, EC5329
+5V_RUN: EC5356
+1.8V_SUS: EC5341, EC5342, EC5335, EC5336, EC5337, EC5338, EC5339, EC5340
+3.3V_RUN: EC5358, EC5360, EC5361, EC5362, EC5363, EC5364
+PWR_SRC: C5300, C5301, C5302, C5303, C5304, C5305

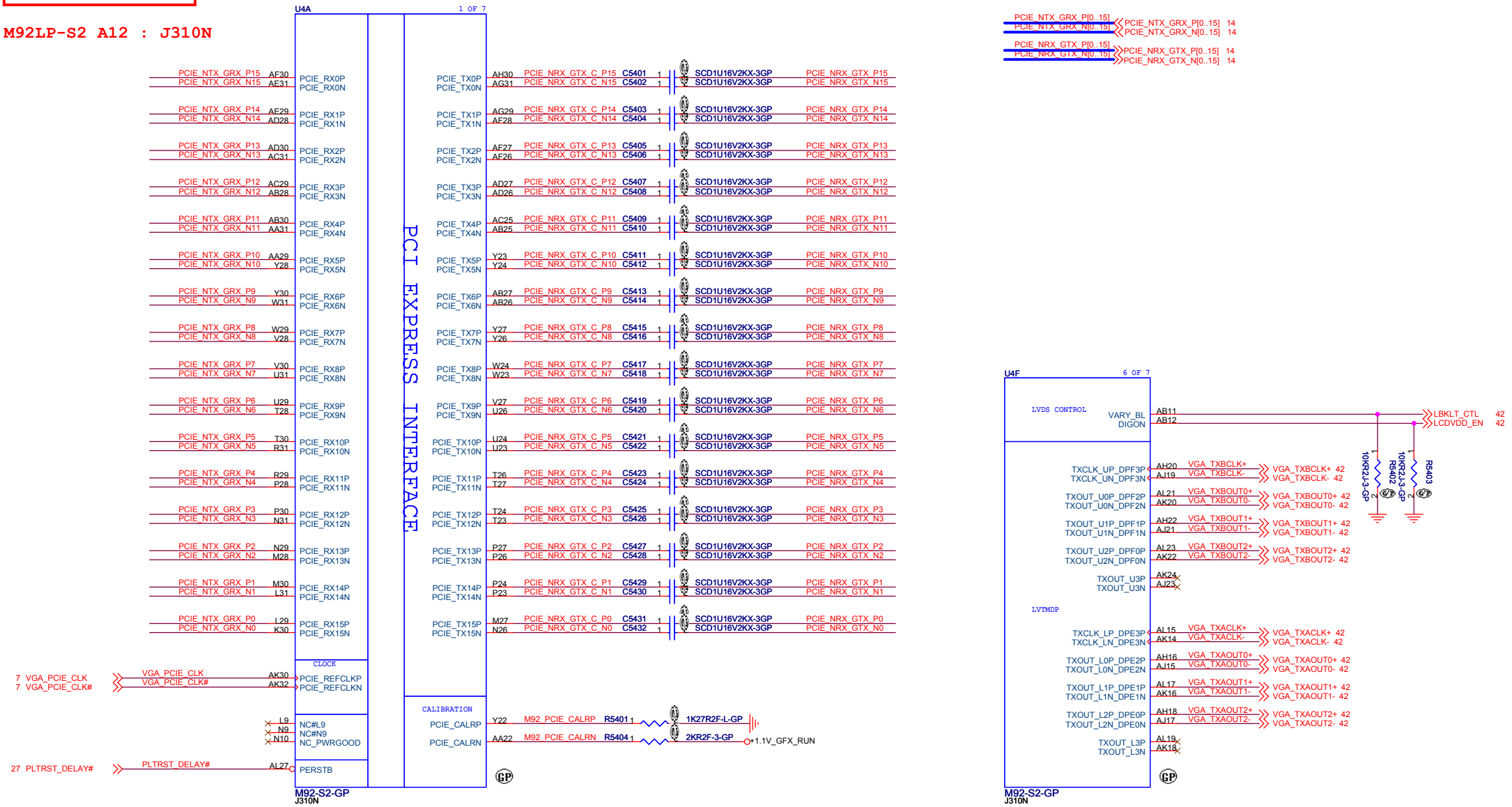
Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Miscellaneous Components
Size: Custom
Document Number: Riya Discrete
Rev: A00
Date: Wednesday, August 26, 2009
Sheet 53 of 65

SSID = VIDEO

M92LP-S2 A12 : J310N



Main Source

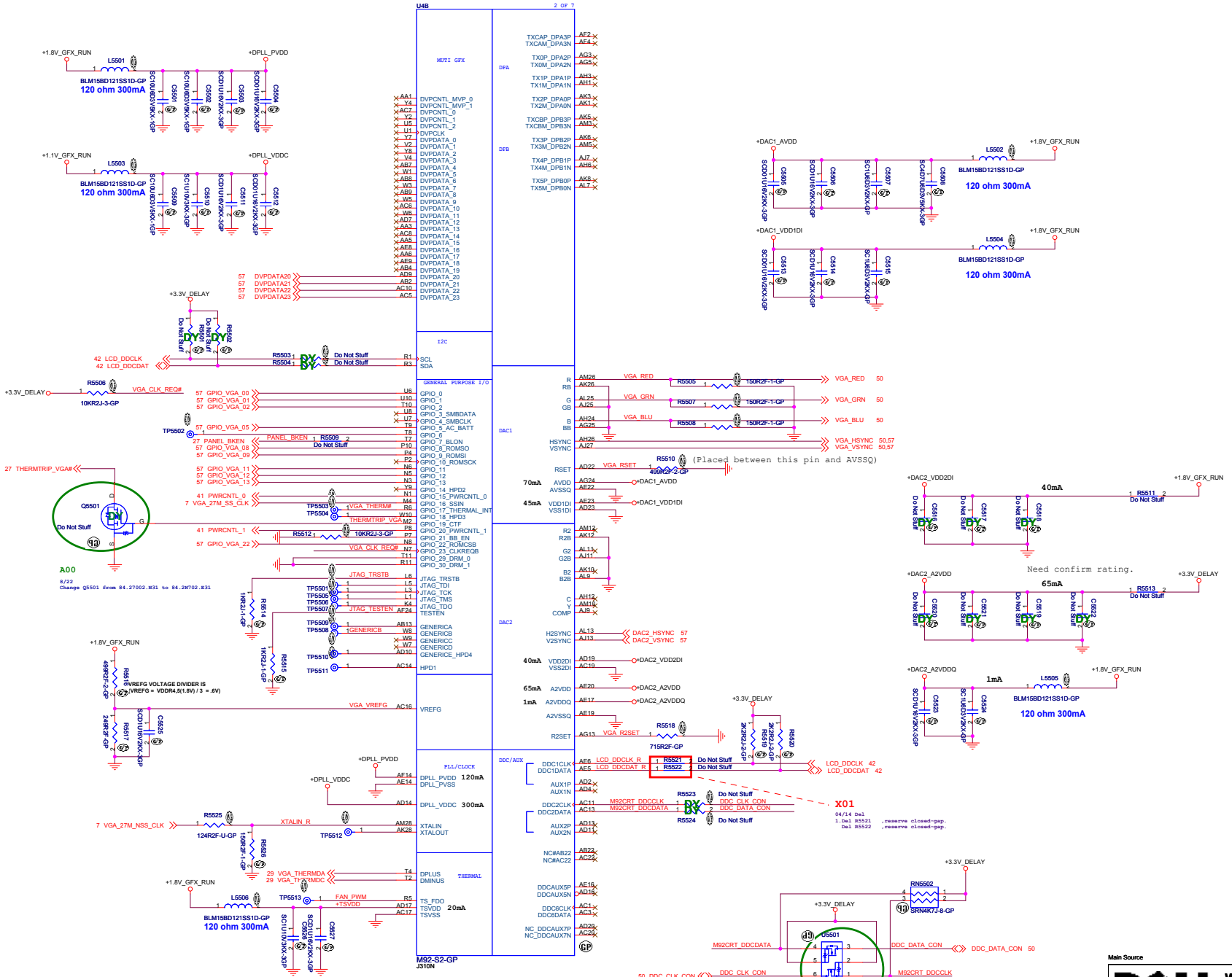
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VGA-PCIE/LVDS(1/4)**

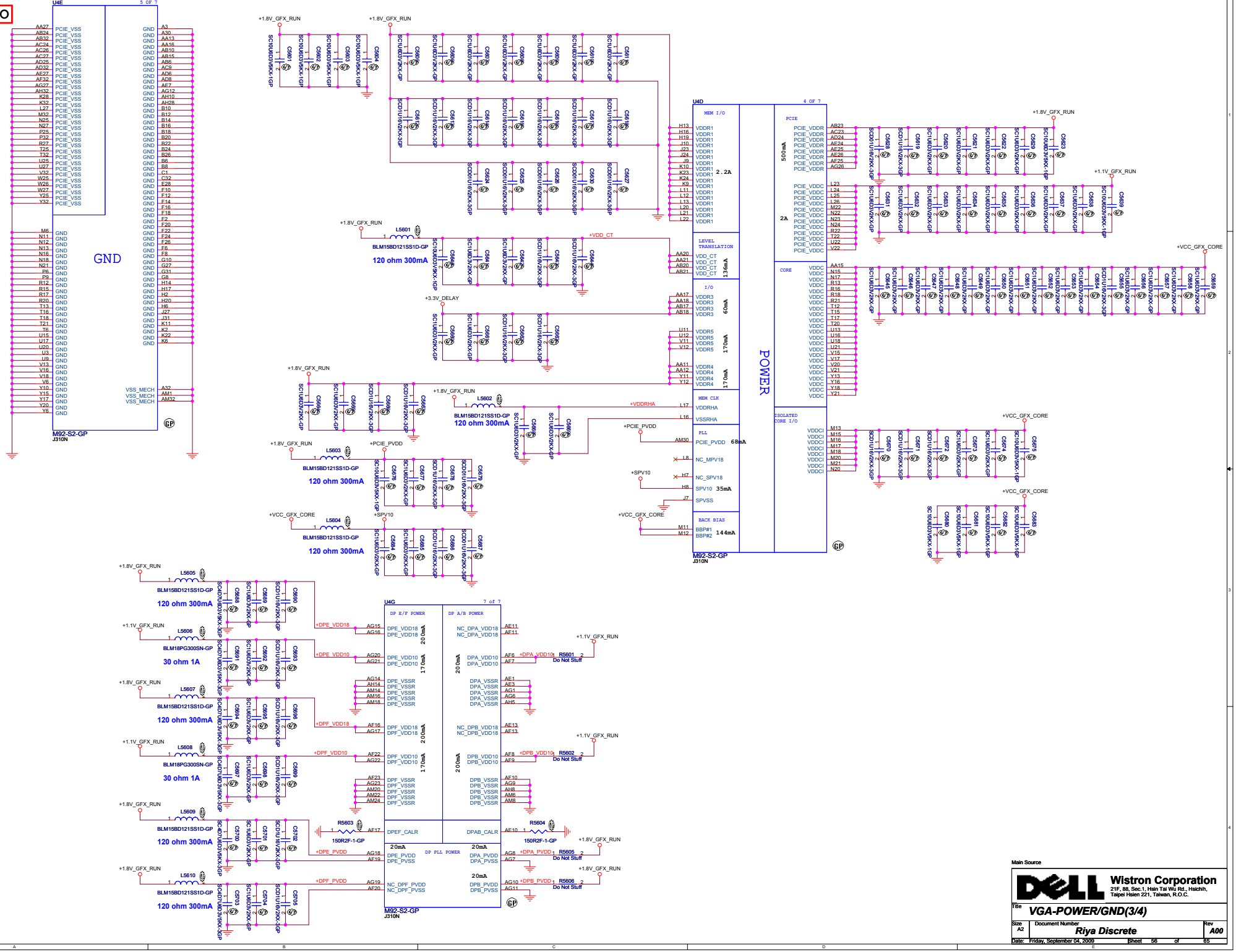
Size	Document Number	Rev
Custom	Riya Discrete	A00

Date: Wednesday, August 26, 2009 Sheet 54 of 65

SSID = VIDEO


U4B
2 OF 7
MUTI GFX
DPA
DPB
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
PLL/CLOCK
DDC/AUX
THERMAL
M92-S2-GP
J310N
+1.8V_GFX_RUN
+1.1V_GFX_RUN
+DPLL_PVDD
+DPLL_VDDC
+3.3V_DELAY
L5501
L5503
BLM15BD121SS1D-GP
120 ohm 300mA
VGA_RED
VGA_GRN
VGA_BLU
VGA_HSYNC
VGA_VSYNC
VGA_RSET
VGA_VREFG
VGA_CLK_REQ#
VGA_THERM#
THERMTRIP_VGA
JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
JTAG_TESTEN
GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4
HPD1
LCD_DDCLK
LCD_DDCDAT
XTALIN_R
FAN_PWM
+TSVDD
Q5501
Do Not Stuff
A00
8/22
Change Q5501 from 84.27002.N31 to 84.2N702.E31
VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = .6V)
(Placed between this pin and AVSSQ)
Need confirm rating.
+DAC1_AVDD
+DAC1_VDD1DI
+DAC2_VDD2DI
+DAC2_A2VDD
+DAC2_A2VDDQ
L5502
L5504
L5505
40mA
65mA
1mA
70mA
45mA
X01
04/14 Del
1.Del R5521 ,reserve closed-gap.
Del R5522 ,reserve closed-gap.
5V @ CRT side
DMN66D0LDW-7-GP
SRN4K7J-8-GP
Main Source
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VGA-TV/CRT/DP PORT(2/4)
Size
A2
Document Number
Riya Discrete
Rev
A00
Date: Wednesday, August 26, 2009
Sheet 55 of 85

SSID = VIDEO



Main Source

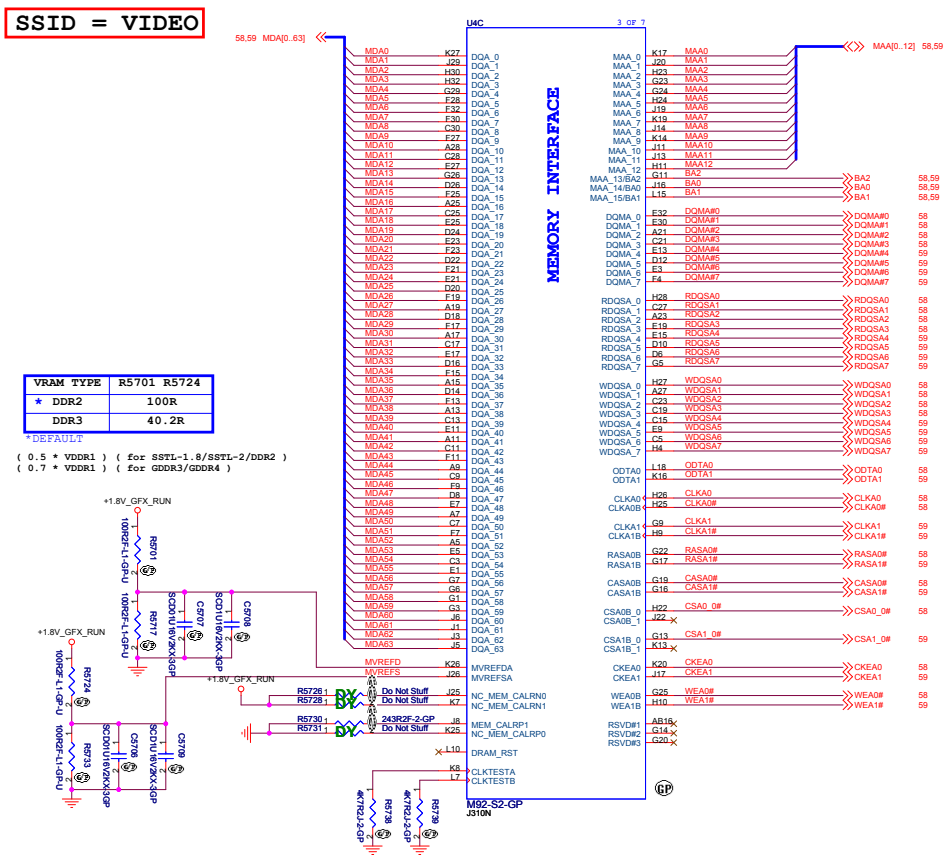
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-POWER/GND(3/4)

Size	Document Number	Rev
A2	Riya Discrete	A00

Date: Friday, September 04, 2009 Sheet 56 of 65

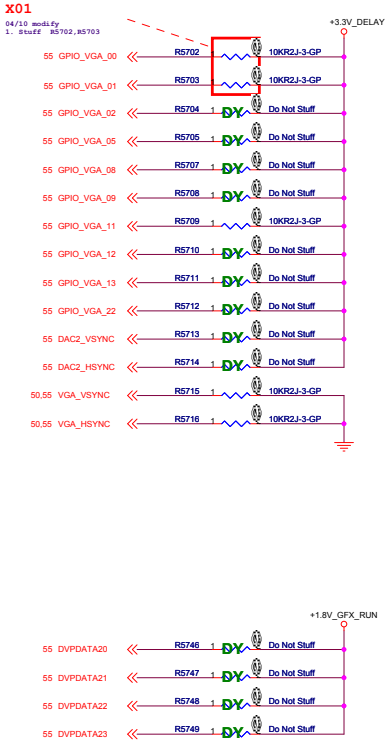
SSID = VIDEO



VRAM TYPE	R5701 R5724
★ DDR2	100R
DDR3	40.2R

*DEFAULT

(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR2)
(0.7 * VDDR1) (for GDDR3/GDDR4)



ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE

GPIO3 , H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
★ 128MB	x000	ST Microelectronics	M25P05A	x100
★ 256MB	x001		M25P10A	x101
64MB	x010		M25P20	x101
32MB	Not Supported		M25P40	x101
512MB	Not Supported		M25P80	x101
1GB	Not Supported			
2GB	Not Supported	Chingis (formerly PMC)	Pm25LV512A	x100
4GB	Not Supported		Pm25LV010A	x101

STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPIO0	Tansmitter Power Savings Enable 0= 50% Tx output swing ★ 1= Full Tx output swing
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled ★ 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPIO2	★ 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
BIF_CLK_PM_EN	GPIO8	★ 0= Disable CLKREQ#power management capability 1= Enable CLKREQ# power management capability
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	Enable external BIOS ROM device ★ 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] ★ 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI

STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPDATA(23:20) (Internal PD)	MEMORY TYPE,MAKE AND SIZE INFO ★ 0000 - GDDR2 64Mx16 500MHz HYNIX 0001 - GDDR2 64Mx16 500MHz SAMSUNG 0010 - Reserve 0011 - Reserve

*DEFAULT

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

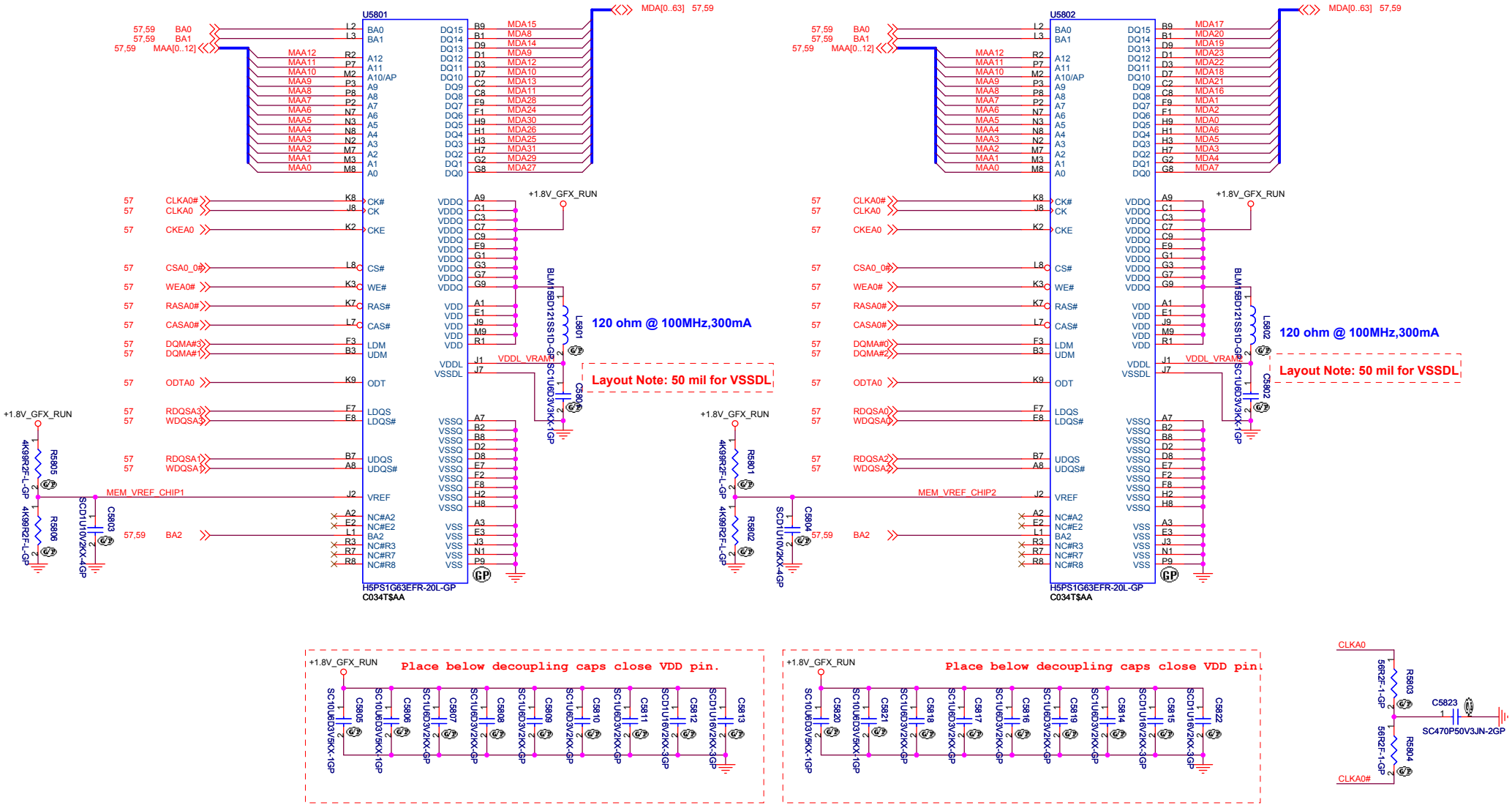
Title: VGA-MEMORY/STRAPS(4/4)

Size: A2 | Document Number: Riya Discrete | Rev: A00

Date: Wednesday, August 26, 2009 | Sheet 57 of 65

SSID = VIDEO

VRAM
1'st 72.51G63.A0U
2'nd 72.41164.G0U



Main Source

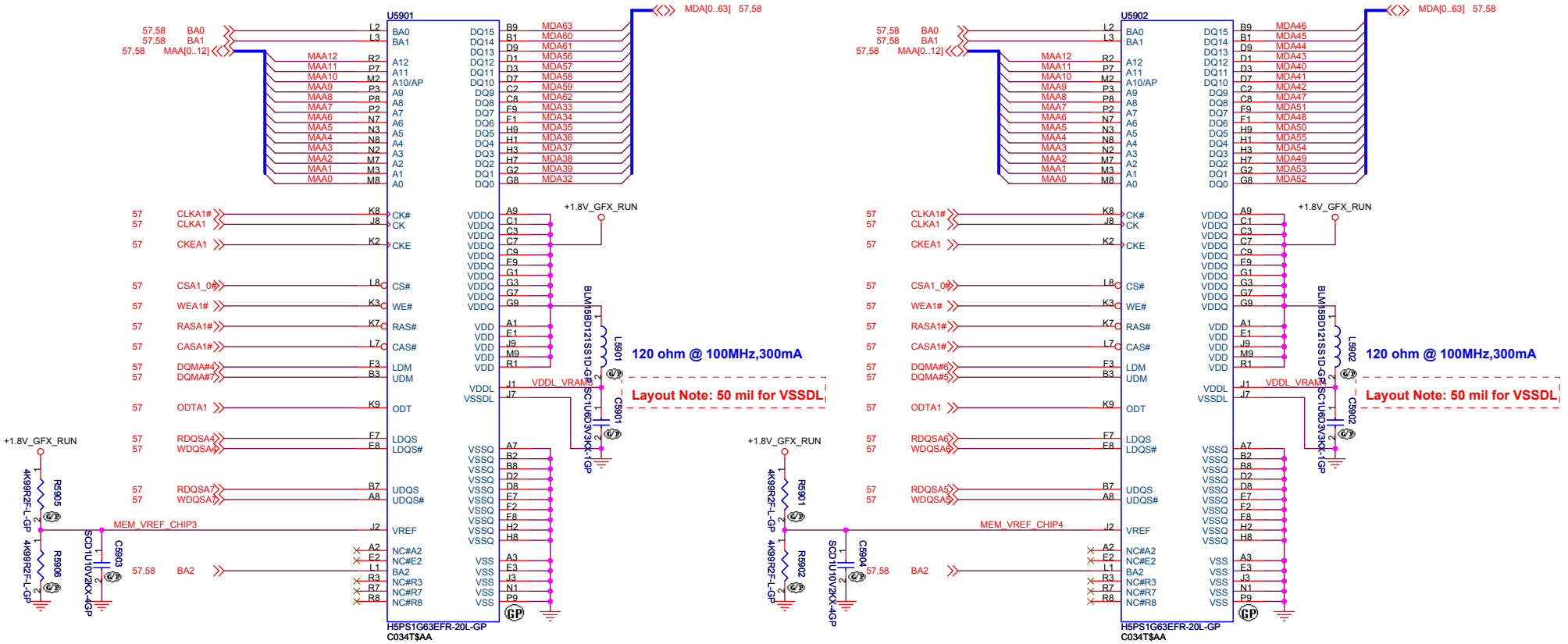
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

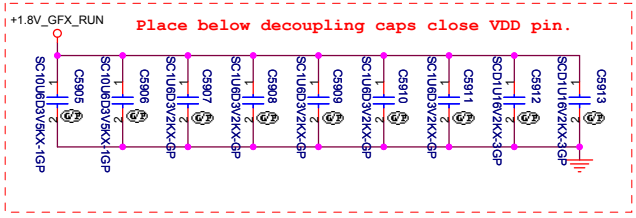
Title: VRAM_(1/2)

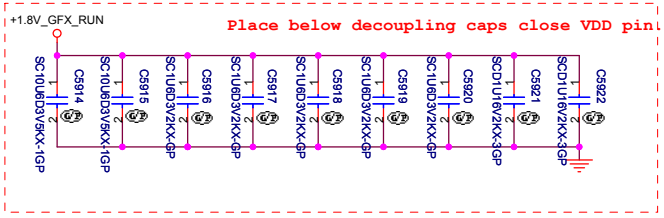
Size	Document Number	Rev
Custom	Riya Discrete	A00

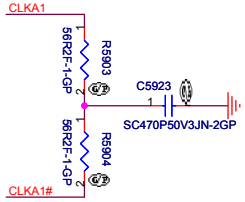
Date: Wednesday, September 09, 2009 Sheet 58 of 65

SSID = VIDEO







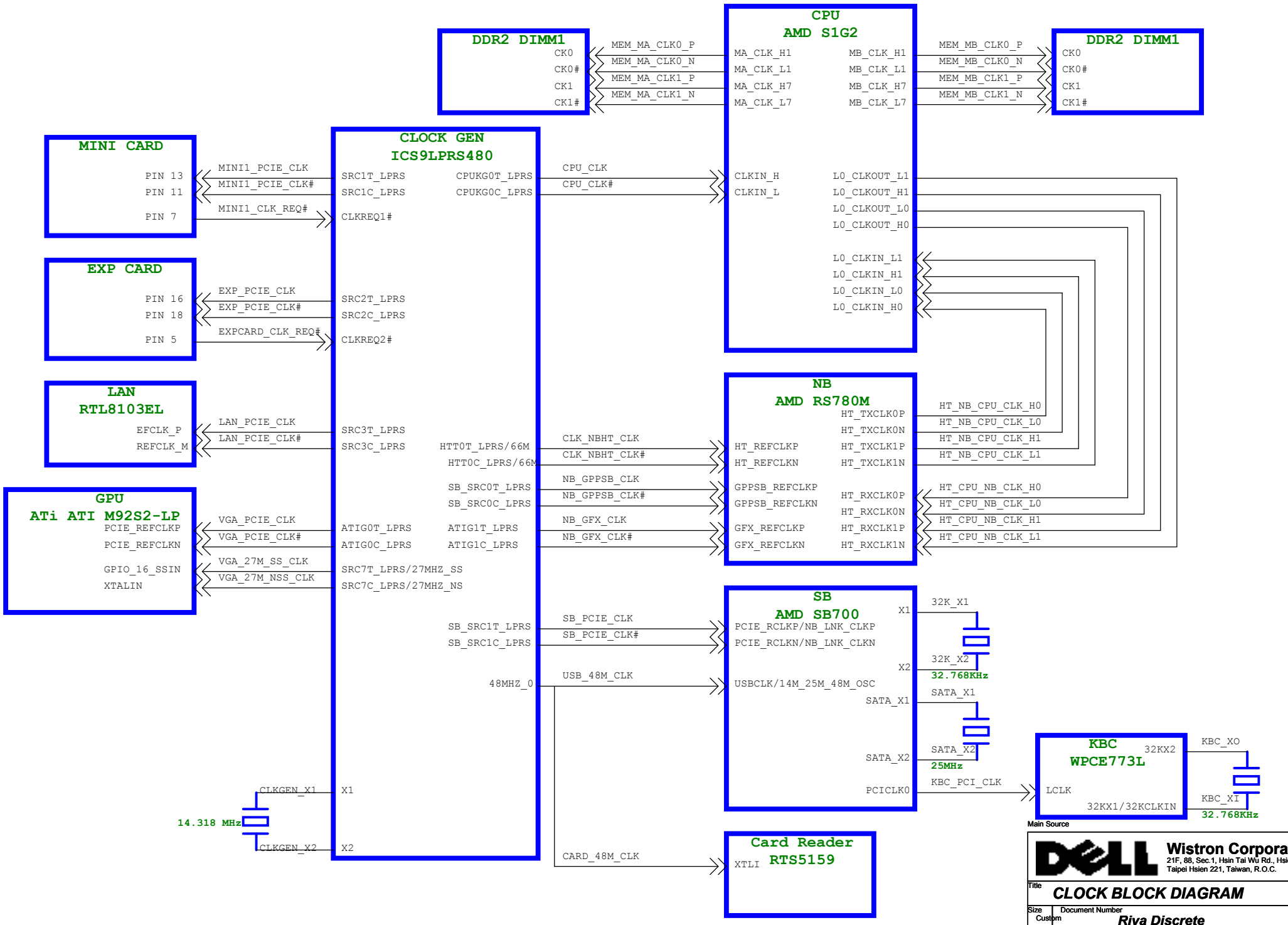


Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***VRAM_(2/2)***	
Size: Custom	Document Number: ***Riya Discrete***	Rev: ***A00***
Date: Wednesday, September 09, 2009	Sheet 59 of 65	

CLOCK BLOCK DIAGRAM

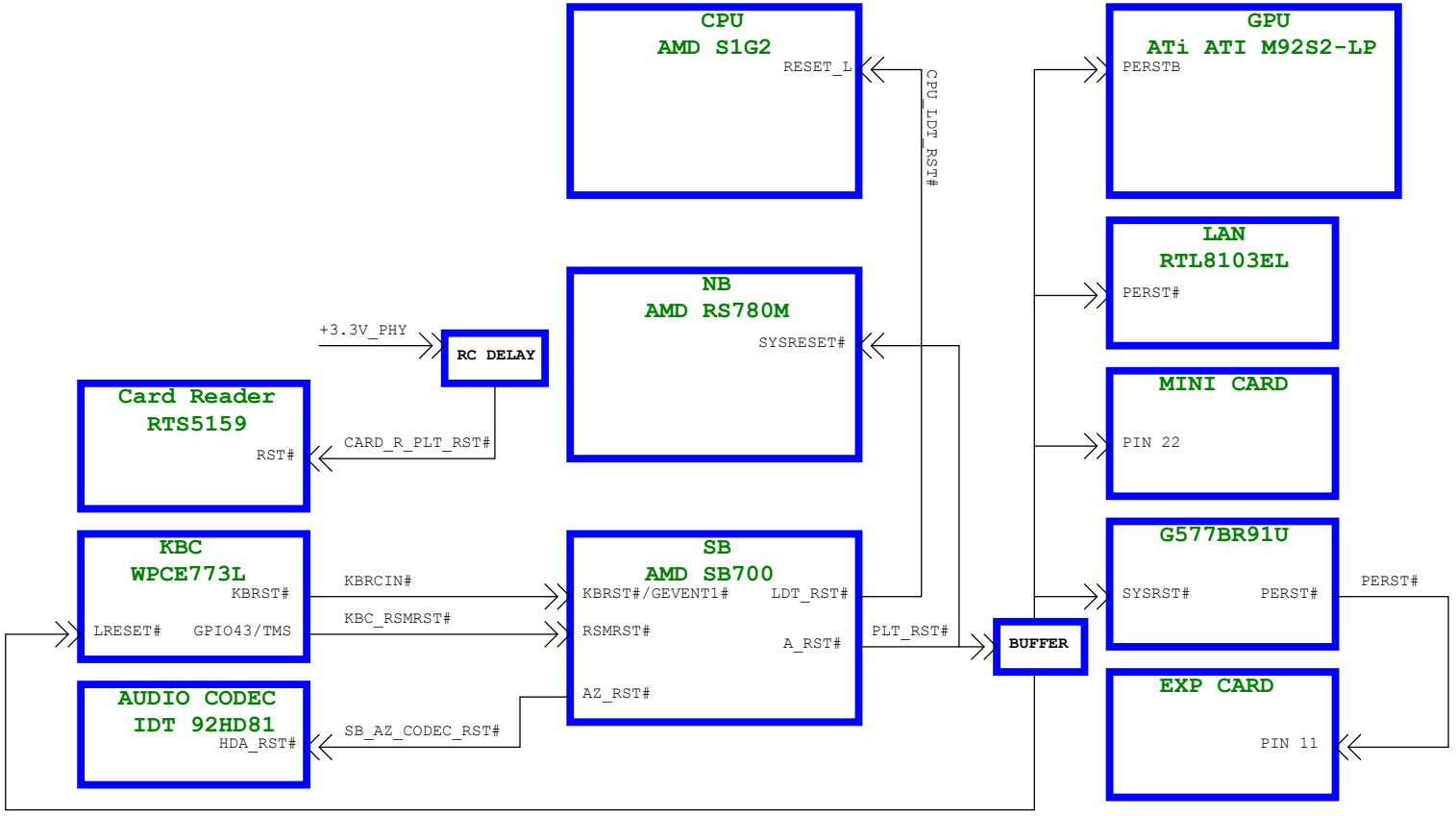


Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CLOCK BLOCK DIAGRAM	
Size: Custom	Document Number: Riya Discrete	Rev: A00
Date: Monday, August 24, 2009	Sheet 60 of 65	

RESET BLOCK DIAGRAM

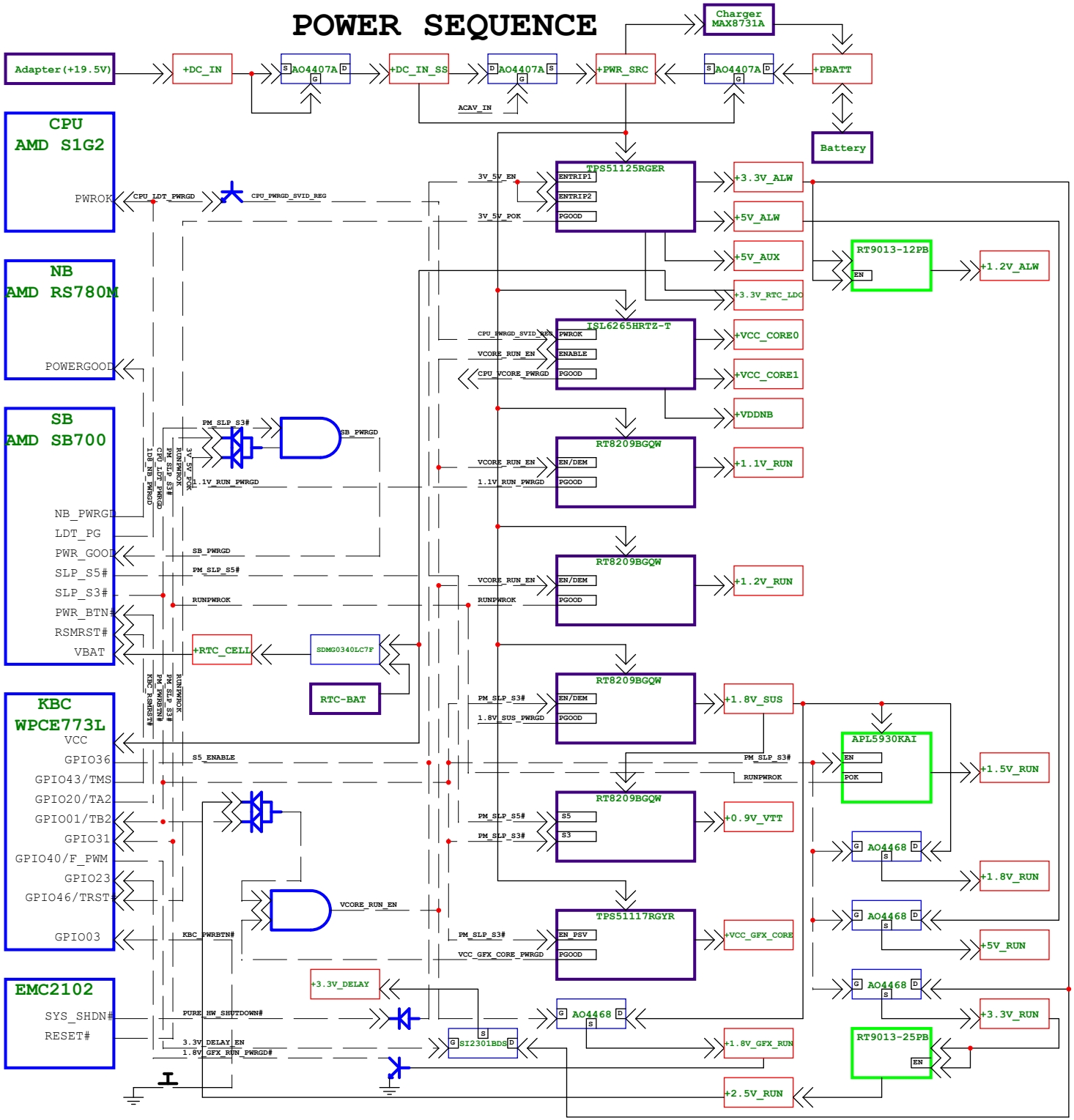


Main Source

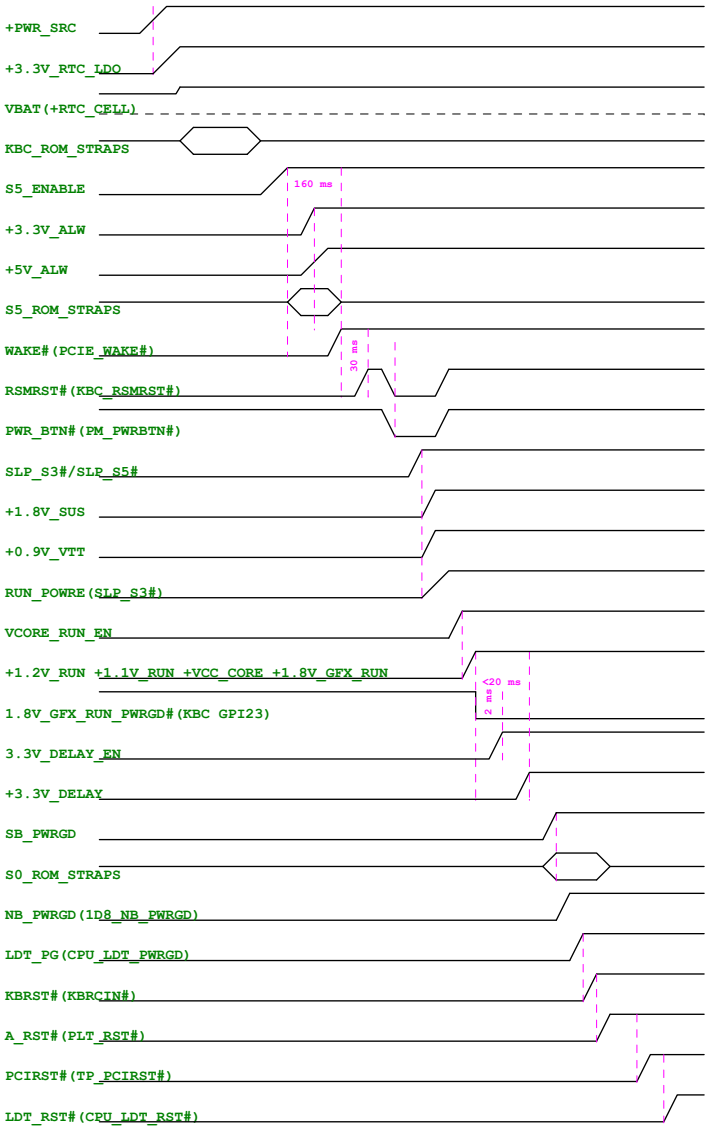
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RESET BLOCK DIAGRAM		
Size: Custom	Document Number: Riya Discrete	Rev: A00
Date: Monday, August 24, 2009	Sheet 61 of 65	

POWER SEQUENCE



AC MODE



Main Source

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER SEQUENCE		
Size: A3	Document Number: Riya Discrete	Rev: A00
Date: Monday, August 24, 2009	Sheet 62 of 65	

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/03/31	X01	1	19	Change DIMM SPD SMBus from Ch1 to Ch0	AGESA by default will look at SMBUS0 for SPD information	EE
		2	49	Use low RDS(on) MOSFET on audio de-pop circuit	Follow DA1's MOSFET to de-pop noise.	EE
		3	19	Change Bluetooth from USB Port-12 to Port-6	Per BIOS request, change bluetooth to port-6	BIOS,EE
		4	39	Change +0.9V_VTT power enable connect with SLP_S5	Per AMD design guideline, VTT should be turn on when S3,so VTT enable signal should tied to SLP_S5#.	EE
		5	20	Add SB GPIO48 To detect LCD Size	Add LCD Size detect Pin	EE
		6	7	Change R709/R710 from 33 ohm to 22 ohm	clock EA test report, vendor recommend change R709/R710 from 33 ohm to 22 ohm.	EE
		7	39	Stuff PR3904 and empty PR3903	Correct BOM errors on schematic	EE
			41	Change PR4103 from 3.3 ohm to 300 ohm		
			39	Stuff PR3910,PR3911		
		8	41	Stuff PR4105 Dummy PR4106,PC4109	Update schematic base on power on/off fine tune result.	EE
			37	Stuff PR3713 Dummy PR3703		
			31	Stuff R3115 Dummy R3117		
			31	Change R3107 from 200K to 20K ohm Change R3103 from 10K to 0 ohm		
			38	Change R3803 from 0 to 15K ohm		
				Stuff PC3808 to 0.1u		
2009/04/06		9	20	Change SATA HD from Port-3 to Port-0	Per BIOS request, change SATA HD to port-0	EE
		10	19	Change R1914 from 33 0hm to 47 ohm	Fine tune damping for HD Audio signal EA test result.	EE
		11	26	Change C2611/C2613 from 18P to 15P	Update crystal cap base on x'tal test report	EE
			20	Change C2009/C2010 from 10P to 12P		
		12	27	Add EC GPIO05 To detect LCD Size	Add LCD Size detect Pin	EE
2009/04/08		13	19	Change Clk gen,Mini Card SMBus from Ch1 to Ch0	reduce component quantity , decrease the production cost	EE
		14	18,25	Del R2504,C2510,R1817	Card reader System reset depend on 3.3V_Run power rails, Not reserve for A_RST.	EE
		15	31	Del R3109,R3110,R3111,R3113,R3114,R3116	Not reserve,for try Power Plane Enable.	EE
2009/04/09		16	10,19	Change CPU SID/SIC from SB_SMBus_Ch1 to SCL3_LV/SDA3_LV.	Reduce component quantity , save level shift circuit cost.	EE
2009/04/10		17	57	Stuff R5702	For GPU setting : Full Tx output swing	EE
				Stuff R5703	For GPU setting : Tx de-emphasis enabled	
2009/04/14		18	18	Change C1810/C1812 from 18P to 15P	Update crystal cap base on x'tal test report	EE
		19	27,49	Change netname from HP_MUTE to HP_MUTE#	This signal is low active, so we need to correct the Netname	EE
		20	29,10	Stuff R2917 Dummy R1022.	SYS_THERMTRIP# By THERMAL IC control	EE
		21	10,15	DEL R1001,R1002,R1003,R1510,R1511	Reduce component quantity , delete 0 ohm ,reserve closed-gap.	EE
			19,27,29	R1902,R2705,R2731,R2905		
			32,42	R3203,R4202,R4203		
			48,55	R4805,R4806,R4809,R5521,R5522		
2009/04/15		22	07	Add EC703 For EMI	This is the solution to solve 999MHz peak issue.	EMI,EE
		23	39	Add R3900,R3901,PQ3900	Use discharge circuit for power on/off.	EE
2009/04/16		24	53	Add C5300,C5301,C5302,C5303,C5304,C5305	Reserve for straddle mot.	EE
2009/04/17		25	15	Del R1508	Not Reserve LDT_RST connect to SYSRESET.	EE
2009/06/09		26	20	Del R2009 R2010		EE
		27	26	stuff C2623 add R2609		EE
		28	27	Del R2736 R2737		EE
		29	27	Connect net LCD_EC_DET to I/O connector		EE
		30	42	Connect LCD1 pin37 to +LCDVDD,Del LCD1 pin38		EE
		31	50	Connect CN5001 pin50 to net LCD_EC_DET,Connect CN5001 pin22 to net +3.3V_RTC_LDO		EE
2009/06/11		32	35	Change PU3501 Ver. from ISL6265HRTZ to ISL6265AHRTZ		EE
2009/06/16		33	23	Change U2301 to new version		EE
		34	42	Change +LCDVDD power solution		EE
2009/06/22		35	29	Empty D2901, Stuff R2902		EE
2009/06/25		36	37,38,39	Change PU3701 PU3801 PU3901 to new version		EE
		37	42	Del D4201 Add R4205		EE

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DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/03/31	X01	1	39	Change PL3901 (1.8V choke) form 1.0uH to 1.5uH	Update schematic base on power report fine tune result.	Power Team
2009/04/06		2	34	Stuff PR3405,PC3413	Reduced 3.3V H/S MOSFET Vds voltage	Power Team
		3	35	Change PR3507 from 4.53k to 3.32k.	Reduced OCP setting value	Power Team
		4	35	Change PC3505 Footprint from 1210 to 1206	Fine tune BOM , merge the same size,value component	Power Team
		5	39	Change PR3908 from 7.32k to 8.2k .	Increasing OCP setting value	Power Team
2009/04/09		6	34	Stuff PR3406,PC3414	Reduced 5V H/S MOSFET Vds voltage	Power Team
2009/04/14		7	35	DEL PR3509, PR3517, PR3518	Reduce component quantity , delete 0 ohm ,reserve closed-gap.	Power Team
			41	PR4117, PR4122		
			34	PR3416, PR3417		
			33	PR3309		

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DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/08/22	A00	1		change PQ3701,PQ3900,PQ4103,Q3104,Q4202,U2702,U5501 to 84.DMN66.03F	change low level ESD mos to high level material.	Power Team Power Team
		2		Change PQ3301,PQ3302,PQ3303,PQ3304,PQ3401,PQ3402,PQ3403, PQ4101,PQ4104,Q2602,Q2902,Q2903,Q3101,Q3102,Q3103,Q4903, Q5501 to 84.2N702.E31.	change low level ESD mos to high level material.	Power Team Power Team Power Team
		3	42	1.DY R4202, use R4205; 2.change R4202,R4205,R4203 from 0 to 100ohm 3.add R4210,R4211	protect KBC avoid LCD plug-in/out ESD damage.	Power Team Power Team
		4	30	change C3001 from 1uf to 0.1uf.	for sloving CORE_RUN_EN signal shake.	
		5	41	1.DY PWRCNTL_0 circuit 2.change PR4117,PR4122 to 0 ohm resistor.	change for GFX power control	
		6	27	DY R2720, add R2718	change PCB version	
		7	7	change U701 to 71.08628.003.	change CLK GEN main soure to Selligo	
		8	52	change R5201 from 0 ohm to 100 ohm.	for KBC ESD protect	
		9		change PR3420, PR3506, PR3514,PR3519,PR3529,PR3530,PR3532, PR3534,PR3912,PR3913,PR4004,R1509,R1920,R1921,R2509,R2510, R2724,R5101 from 0 ohm to short pad.	for cost down	
		10	19	Change R1903 from 11.8k to 10.7k	for USB issue	
		11	48	ADD PWR_LED_B AFTE Pad	for AFTE test	
		12		change R701,R702,R704,R1812,R1907,L2003,R2302,R2303, R2304,R2501,R2512,R2508,R2511,R2723,R2902, R3014,R3115,PR3316,PR3713,PR3904,PR4101,PR4105,R4411, R4412,R4901,R4904,R4905,R4906,R4907, R4908 from 0 ohm to short pad.	for cost down	
		13	37	Change PR3712 from 64.10R05.55L to 63.10033.15L Change PR3711 from 64.10025.6DL to 63.10334.1DL	for cost down	
		14		Del L2502,L4401.L4701,L4801	for PSE don't like co-layout	
		15	42	Chang EC4202 Pin1 from LCD_TST to LCD_TST_CN		
		16	48	Change R4802,R4807 from 0 ohm to short pad		
		17	49	Change R_USB11_N,R_USB11_P from U4702 Pin3,4 to Pin1,6		
		18	19	Change R1903 from 10K7R2D to 10k7R2F		0903
		19	35	Change PR3520 from 100K to 93.1K Change PR3521 from 18K to 24K	CPU_CORE OCP	0903
		20	41	Change PR4111 from 154K to 52.3K Change PC4112 from 0.047u to 0.1u	VGA_CORE OVP	0903
		21	42	1. Connect LCD1 pin38 to GFX_PWR_SRC 2. Del LCD1 pin37		0903
		22	47	Change R4701,R4702 from 0ohm to short pad		0903
		23		Change RS780 P/N to N131K,SB700 P/N to Y708D		0903
		24	18	Add TP_25M_X1,TP_25M_X2	ATE request	0908
		25	33	Change PC3306,PC3307,PC3314,PC3315 from 78.10622.53L to 78.10622.52L		0908
		26	49	DY Q4903,Q4904,Q4905,Q4906,Q4907.R4911		0908
		27	23	Change U2301 to new version,from 71.92H81.E03 to 71.92H81.G03		0908

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