Compal Confidential

MB Schematic Document

FH58F

LA-J251P

Rev:1.0

2019.06.26

Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.		
Title: Cover Sheet		
Size: Custom	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 1 of 101	

mDP Conn.

page 37

HDMI Conn.

page 40

eDP

page 38

eDP

Fan Control*2

page 77

Interleaved Memory

260 pin DDR4-SO-DIMM X1

BANK 0, 1, 2, 3 page 23

260pin DDR4-SO-DIMM X1

BANK 4, 5, 6, 7 page 24

Memory BUS

Dual Channel

1.2V DDR4 2400/2666

CoffeeLake H Processor

BGA1440

(42X28) (CFL-H_6+2)

Processor page 06~13

PEG x16

8GT/s

N18P-G0 with gDDR5 x4

page 25~36

HDMI x 4 lanes

DP x 4 lanes

USB 3.0

conn x1

USB (port 1)

X4 DMI

NGFF

WLAN

USB port 7

page 52

PCIE 1.0

2.5GT/s

port 15

page 68

PCIE 3.0 x4

8GT/s

Port 9-12

page 68

PCIE 3.0 x4

8GT/s

Port 21-24

USB 3.0

conn x1

USB (port 3)

USB 3.0

Type-C

USB (port 2)

CMOS

Camera

USB (port 5)

Flexible IO

page 51

PCIE 2.0

5GT/s

port 14

page 67

SATA3.0

6.0 Gb/s

port 4

Cannonlake PCH - H

FCBGA(25X24)

874pin FCBGA

page 14~21

USBx8

48MHz page 72

page 42, 43

page 38

Finger_Print

USB (port 8)

page 66

USB charger

SLGC55544

page 71

LAN(GbE)

Realtek 8118ASA

SATA Re-Driver

PARADE PS8527

HD Audio 3.3V 24MHz

RJ45 conn.

page 32.

SATA HDD Conn.

page 47

HDA Codec

ALC255

page 42

LPC/eSPI BUS

CLK=24MHz

ENE

KB9022

page 58

TPM

page 66

Int. Speaker

page 42

Int. DMIC

on Camera/B

page 48

UAJ

on Sub/B

page 48

SPI

RTC CKT.

page 20

Sub Board

HS/B

page 66

IO/B

page 73

TURBO/B

page 73

Touch Pad

PS2 / I2C

page 63

Int.KBD

page 63

SPI ROM x1

page 16

Power On/Off CKT.

page 63

DC/DC Interface CKT.

page 78

Power Circuit DC/DC

page 81~97

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.			
Title	Block Diagrams		
Size	Document Number		Rev
Custom	FH58F M/B LA-J251P		1.0
Date:	Monday, August 12, 2019	Sheet 2 of 101	

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 1%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD
0	0		0.000 V	0.300 V	0x00 – 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 – 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F – 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 – 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 – 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B – 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 – 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 – 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 – 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 – 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 – 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 – 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 – 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 – 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 – 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 – 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA – 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 – 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE – 0xF0
19	NC	3.000 V	3.000 V		0xF1 – 0xFF

I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit) Write	Address(8bit) Read
I2C_0 (+3VS)				
I2C_1 (+3VS)	TM-P3393-003 (Touch Pad)			
	SA577C-12A0 (Touch Pad)			
PCH_SMBCLK (+3VS)	DIMM1			
	DIMM2			
PCH_SML1CLK EC_SMB_CK2 (+3VS)	N18P-G0/N17P-G0-K1 (VGA)	0x9E		
	Thermal Sensor (NCT7718W)	1001_100xb	1001_1001b	1001_1000b
	PCH	0x90		
EC_SMB_CK1 (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		
EC_SMB_CK3 (+3VALW)	LED driver	0xC0		

BOM Structure Table

BOM Option Table	
Item	BOM Structure
Unpop	@
Connector	CONN@
CMC	CMC@
dGPU circuit	VGA@
N18P GPU	N18P@
N17P GPU	N17P@
TPM	TPM@
For Acer IOAC	IOAC@
No Acer IOAC	NIOAC@
KB backlight	KBLED@
KB LED driver	LED14P@
OVRM-ON	ON_X76@
OVRM-uPI	uPI_X76@
Thermal sensor	TMS@
for SW debug board	UART@
Intel CNVi	CNVI@
Finger Print	FP@
FinerPrint(with PBA)	PBA@
EMI requirement	EMI@
EMI require reserve	XEMI@
ESD requirement	ESD@
ESD require reserve	XESD@
FP ESD requirement	FPESD@
Pidgey ESD requirement	PGESD@
SATA HDD W REDRIVER	SATARD@
SATA HDD WO REDRIVER	SATANRD@
i5 CPU	i5@
i7 CPU	i7@
H62 CPU	H62@
H82 CPU	H82@
LAN LDO mode	LDO@
LAN Switch mode	SWR@

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Voltage Rails

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+1.05VALW	+1.05V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.05VS_VCCSTG	+1.05VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO +0.95VS power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+NVVDD1	Core voltage for VGA (merge core & core_s)	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.8VALW	System +1.8VALW always on power rail	ON	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

43 level BOM table

43 Level	Description	BOM Structure
431AC5BOL01	SMT MB AF952 DH53F I5PG1 4G 28P 8L HDMI	255@/CHG@/CMC@/CNVI@/FP@/G0@/I5@/IOAC@/LDO@/SATARD@/TYPEC@/V15@/VGA@/X76@

Auris BOARD ID Table

Board ID	PCB Revision	Board ID	PCB Revision
0	1650 Rev0.1+RGB	10	
1	1650 Rev1.0+RGB	11	
2		12	
3		13	
4		14	
5		15	
6		16	
7		17	
8	1660 Rev1.0+RGB	18	
9		19	

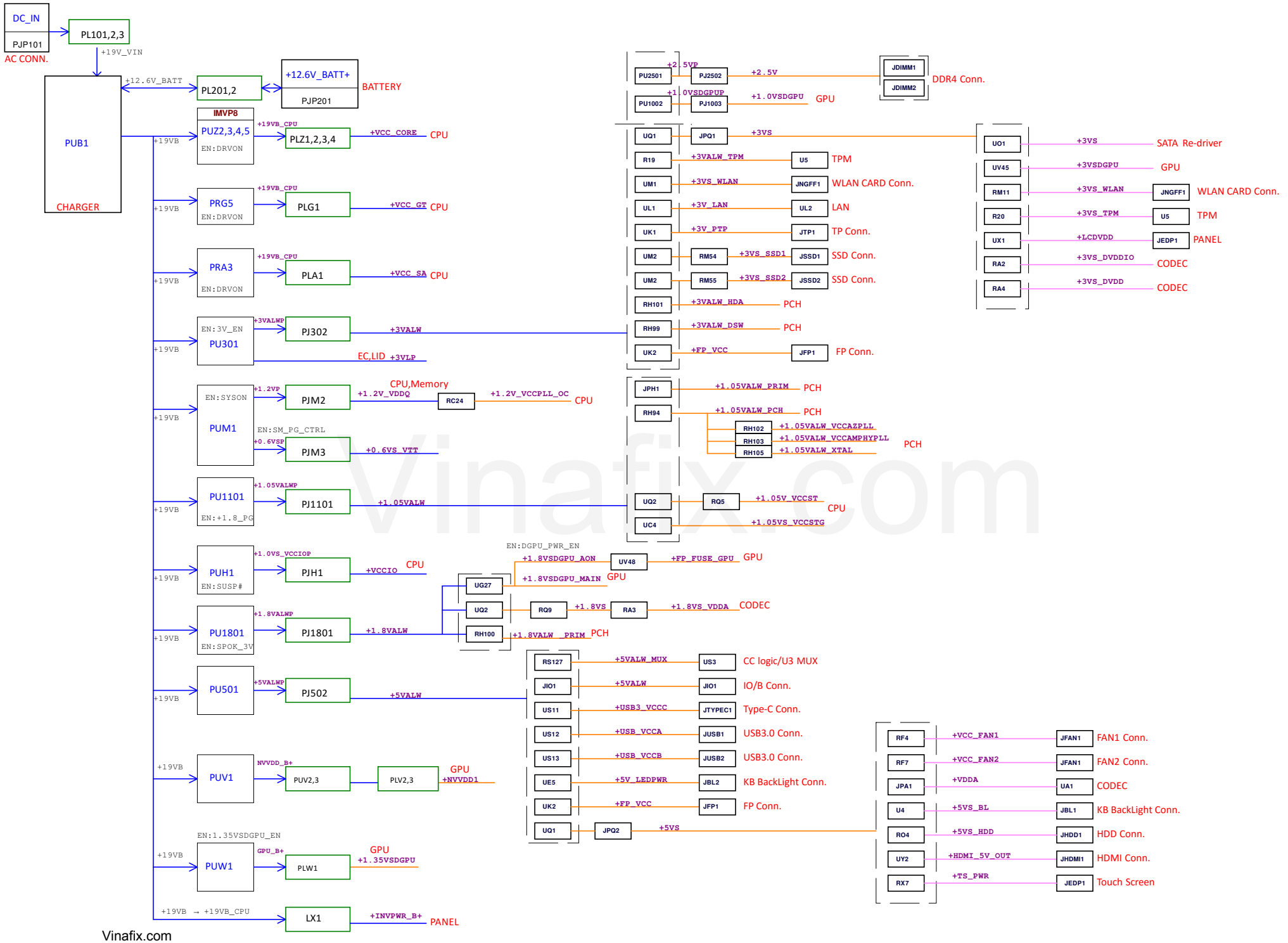
Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.

Title: Notes List

Size: Custom | Document Number: FH58F M/B LA-J251P | Rev: 1.0

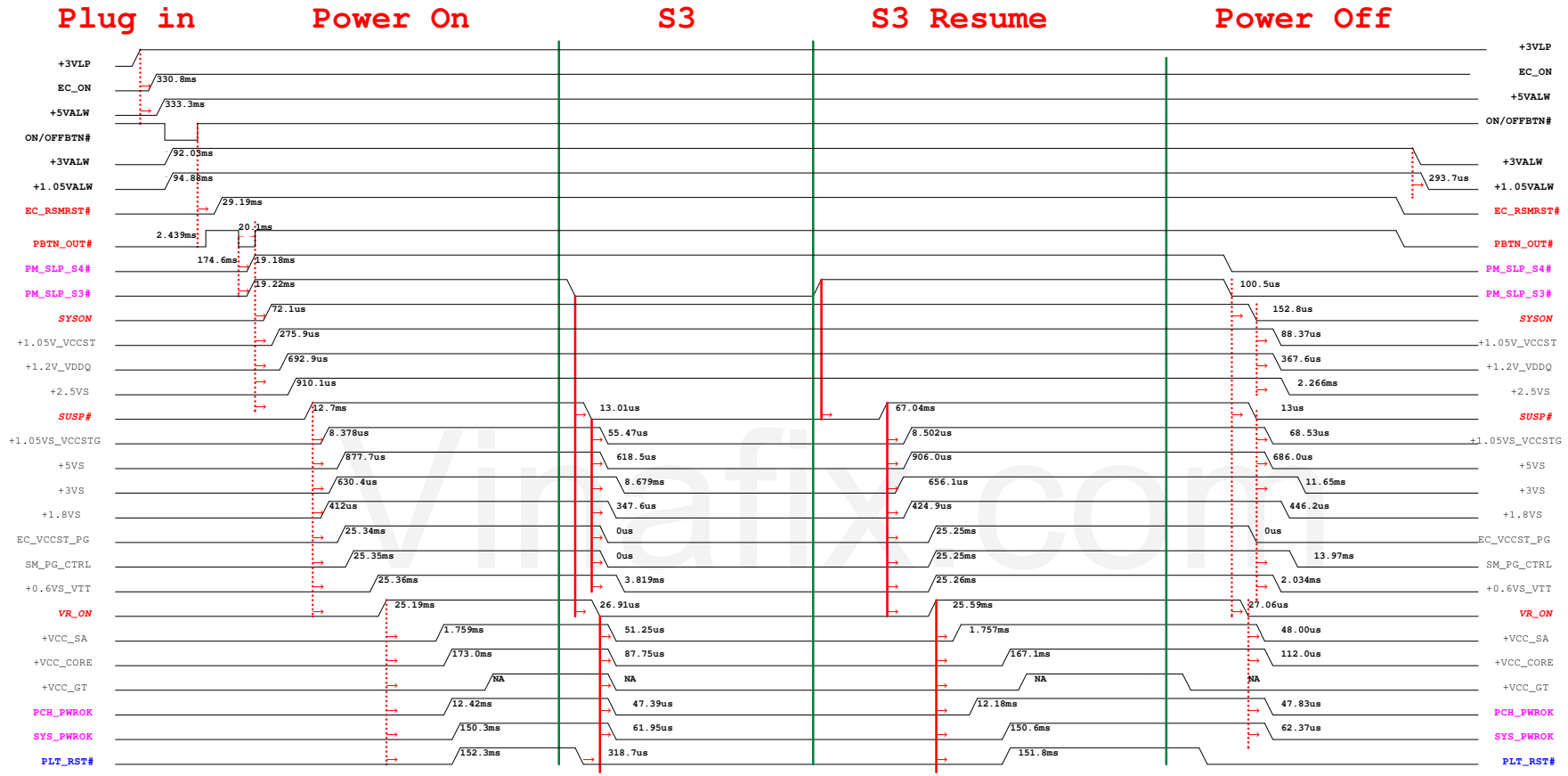
Date: Monday, August 12, 2019 | Sheet 3 of 101



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/10/30	Deciphered Date	2018/10/30
			Power Map
			FH58F M/B LA-J251P

DH5VF_EVT Power Sequence AC mode

BIOS ver: V0.02W1
EC: ver: V002AT04



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.

Title: Power Sequence

Size: Custom | Document Number: FH58F M/B LA-J251P | Rev: 1.0

Date: Monday, August 12, 2019 | Sheet 5 of 101

ZZZ
PCB10@
PCB EH5VF LA-H501P LS-H501P/H502P
DAZ2K700100

ZZZ1
PCB1A@
PCB EH5VF LA-H501P LS-H501P/H502P
DAZ2K700101

Coffee Lake-H CPU SKU

UC1
I5@
S IC CL8068403373522 SR3Z0 U0 2.3G ABO!
SA0000BPJ40

UC1
I7@
S IC CL8068403359524 SR3YY U0 2.2G ABO!
SA0000BPZ40

UC1
I5QS@
S IC CL8068403373522 QP89 U0 2.3G BGA
SA0000BPJ10

Re-fresh U0 stepping

UC1
I5RQS@
S IC CL8068404121905 QRR5 U0 2.4G FCBGA
SA0000COG00

UC1
I5R@
S IC CL8068404121905 SRF6X U0 2.4G ABO!
SA0000COG40

UC1
I7RQS@
S IC CL8068404121817 QRR2 U0 2.6G FCBGA 1440
SA0000COF10

UC1
I7R@
S IC CL8068404121817 SRF6U U0 2.6G ABO!
SA0000COF30

Re-fresh R0 stepping

UC1
I5VPROQS@
S IC CL8068404069511 QS6H R0 2.5G BGA
SA0000CQH00

UC1
I5NVPROQS@
S IC CL8068404069606 QSKC R0 2.4G FCBGA
SA0000CSZ20

UC1
I5NVPRO@
S IC CL8068404069606 SRFCR R0 2.4G ABO!
SA0000CSZ10

UC1
I7VPROQS@
S IC CL8068404069311 QRZS R0 2.6G FCBGA
SA0000COC00

UC1
I7NVPROQS@
S IC CL8068404069418 QSKB R0 2.6G FCBGA
SA0000CSU20

UC1
I7NVPRO@
S IC CL8068404069418 SRFCP R0 2.6G ABO!
SA0000CSU10

Cannon Lake PCH SKU

UH1
PCH@
S IC FH82HM370 SR40B B0 BGA 874P PCH-H ABO!
SA0000BVP10

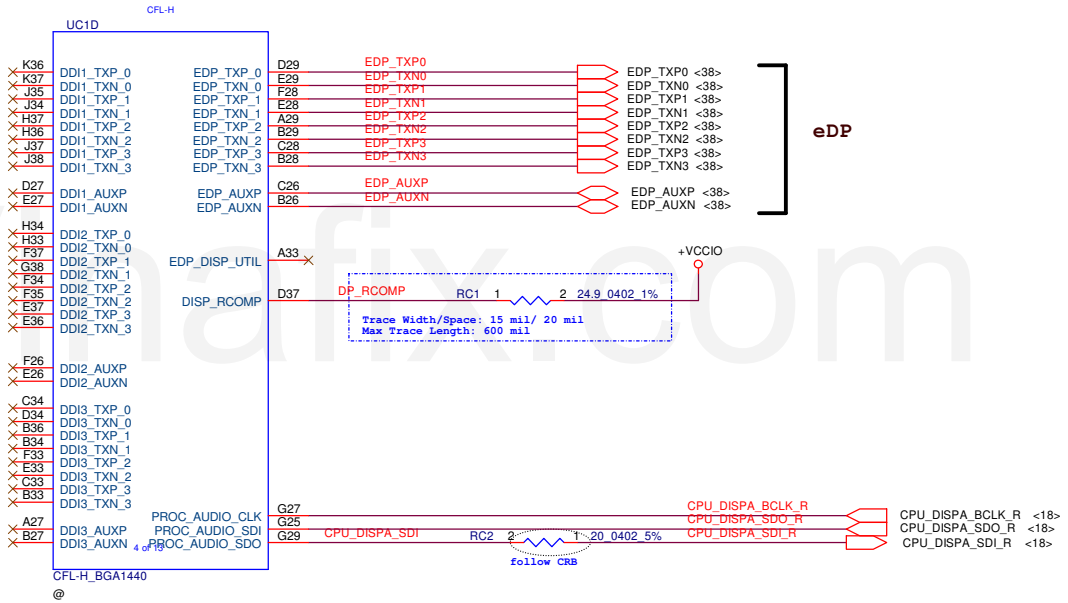
UH1
PCHQS@
S IC FHHM370 QNYF B0 BGA 874P PCH-H
SA0000BPF10

NV GPU SKU

UV1
N17P@
S IC N17P-G0-K1-A1 FCBGA 908P GPU ABO !
SA0000CFM20

UV1
N18PQS@
S IC N18P-G0-A1 QS FCBGA 960P GPU ABO !
SA0000CK210

UV1
N18PMP@
S IC N18P-G0-MP-A1 FCBGA 960P GPU ABO !
SA0000CK230



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.

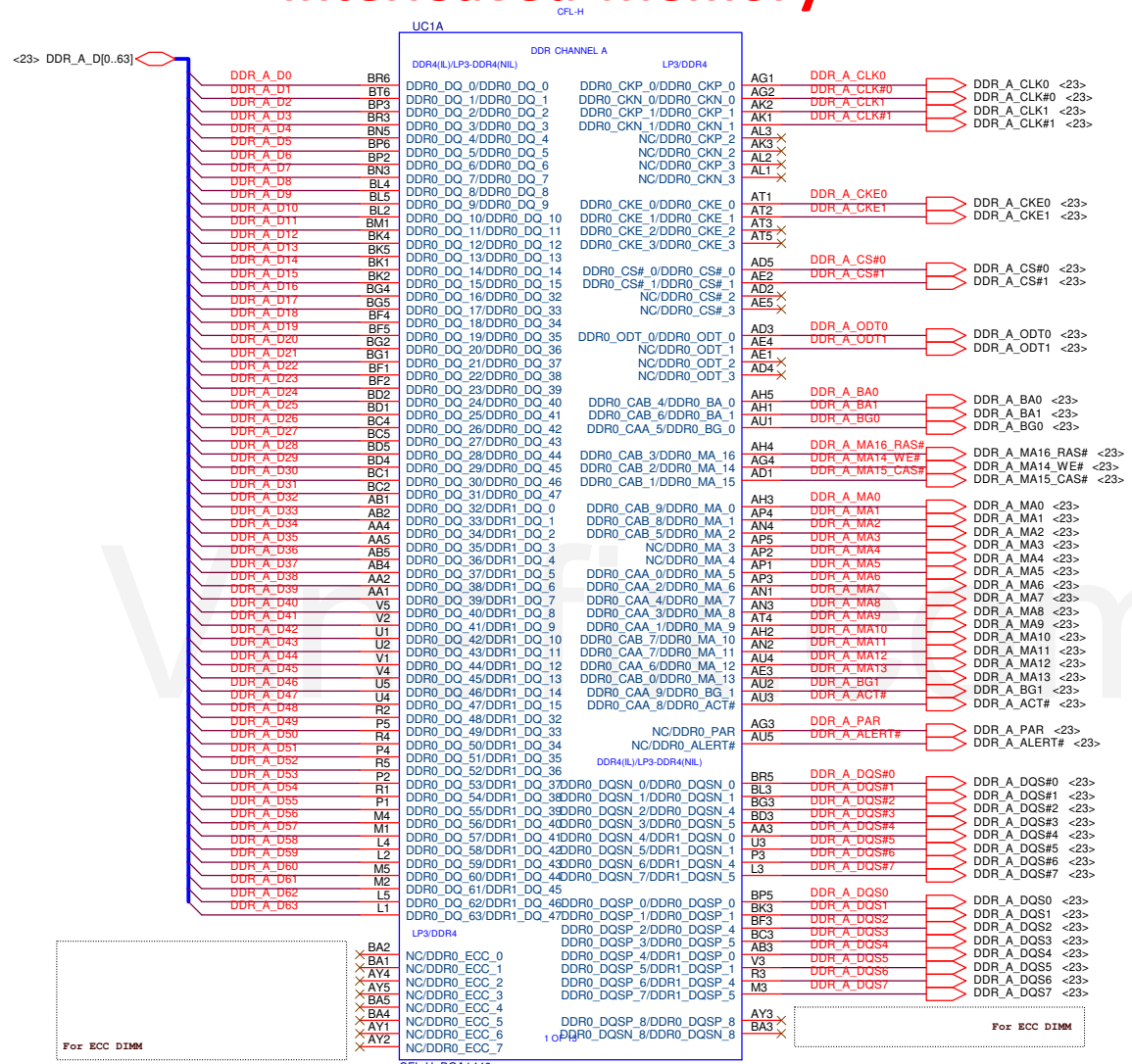
Title: CFL-H(1/8)DDI/eDP

Size: Custom | Document Number: FH58F M/B LA-J251P | Rev: 1.0

Date: Monday, August 12, 2019 | Sheet 6 of 101

CHANNEL-A

Interleaved Memory



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.

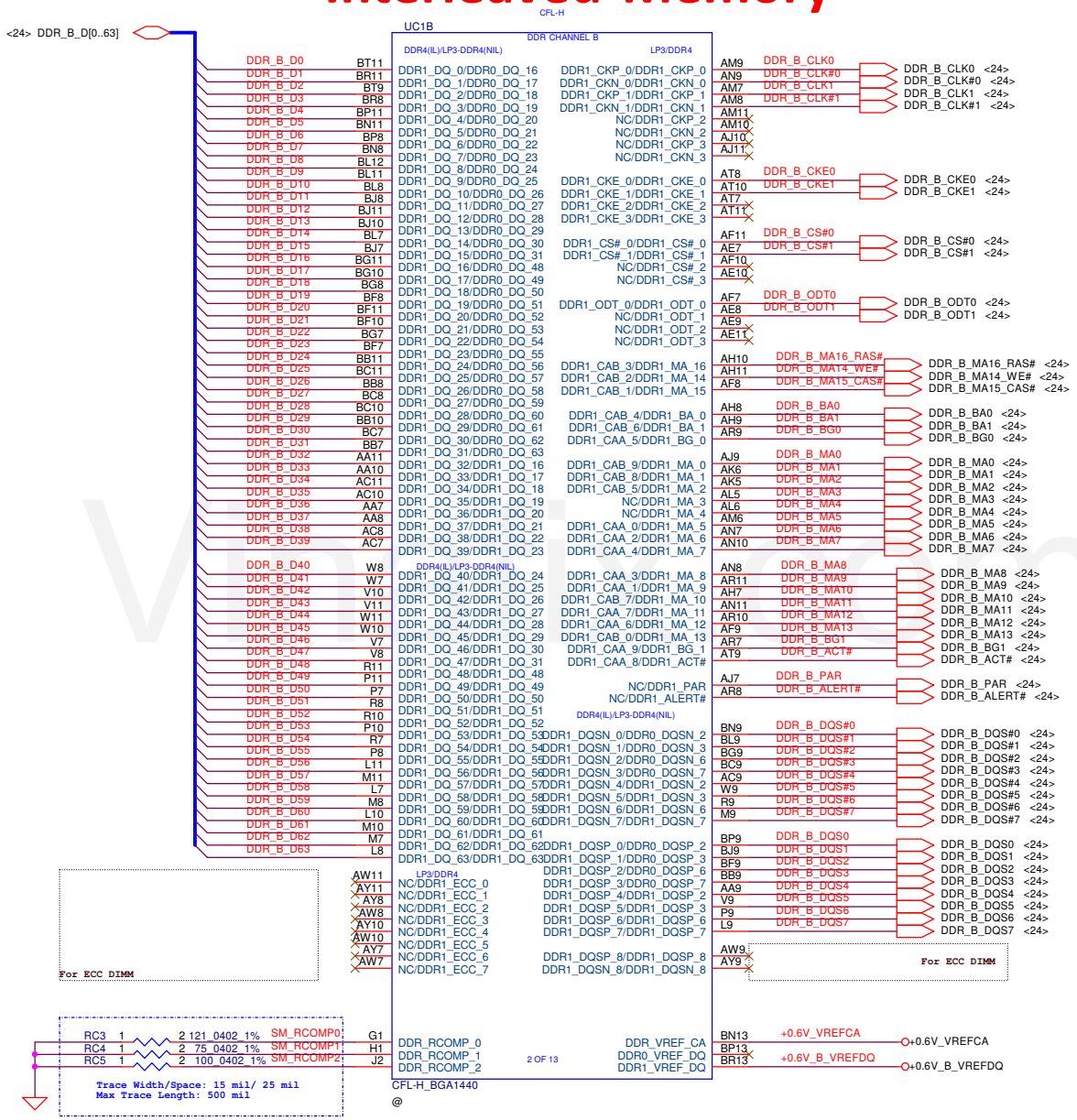
Title: **CFL-H(2/8)DIMMA**

Size: Custom | Document Number: **FH58F M/B LA-J251P** | Rev: 1.0

Date: Monday, August 12, 2019 | Sheet 7 of 101

CHANNEL-B

Interleaved Memory



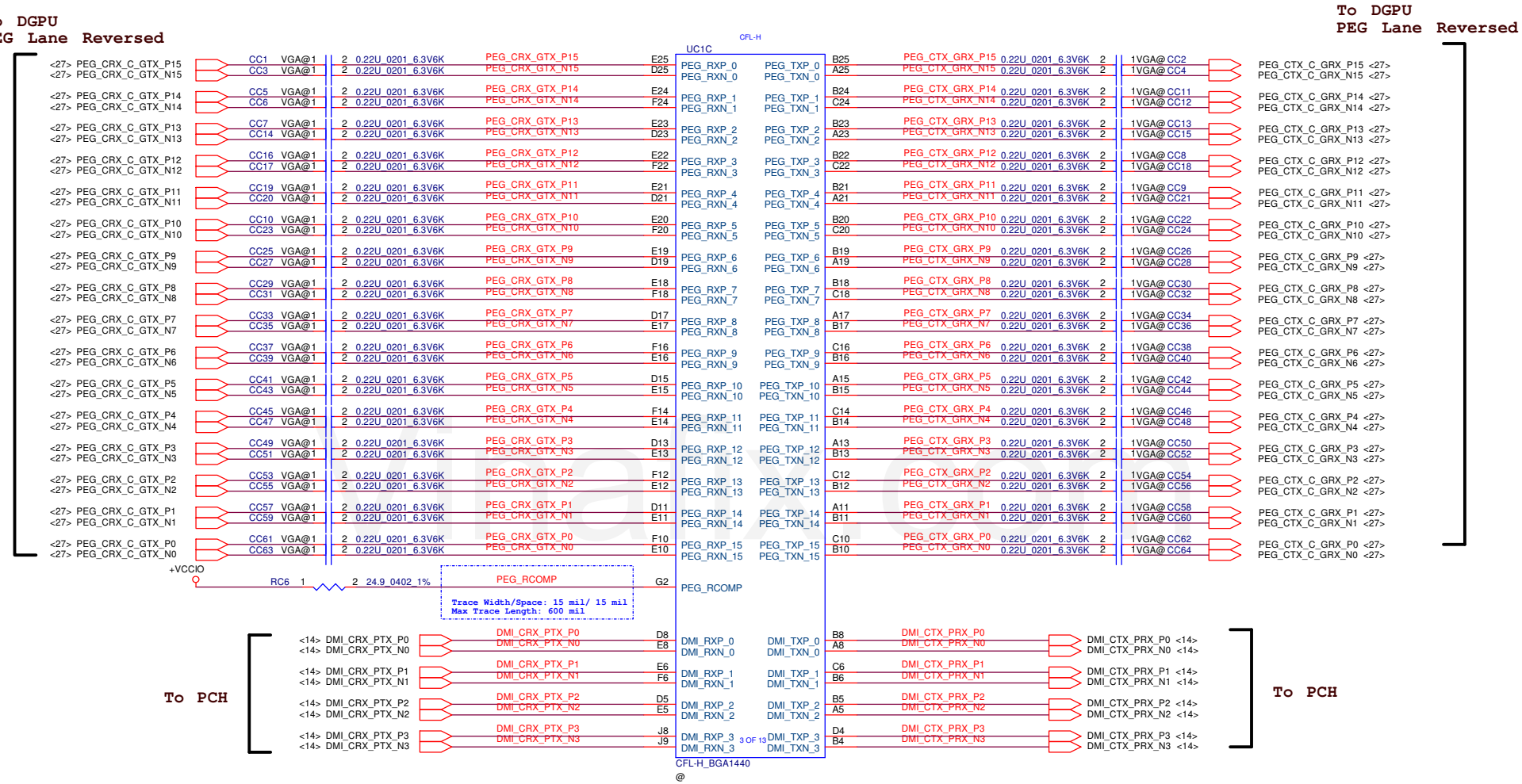
Compal Electronics, Inc.

Title: CFL-H(3/8)DIMMB

Size: Custom | Document Number: FH58F M/B LA-J251P | Rev: 1.0

Date: Monday, August 12, 2019 | Sheet 8 of 101

PEG&DMI



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.			
Title	PEG/DMI		
Size: Custom	Document Number: FH58F M/B LA-J251P		Rev: 1.0
Date: Monday, August 12, 2019	Sheet 9 of 101		

571391_CFL_H_PDG_Rev0p5
1. The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
2. Route the Alert signal between the Clock and the Data signals.
3. Place those resistors close CPU side.

UC1E
CFL-H
CFL-H_BGA1440
5 OF 13

PCH_CPU_BCLK_P / PCH_CPU_BCLK_N → BCLKP / BCLKN
PCH_CPU_PCIBCLK_P / PCH_CPU_PCIBCLK_N → PCI_BCLKP / PCI_BCLKN
PCH_CPU_24M_CLK_P / PCH_CPU_24M_CLK_N → CLK24P / CLK24N
CPU_SVID_ALERT# / CPU_SVID_CLK / CPU_SVID_DAT / H_PROCHOT#_R → VIDALERT# / VIDSCK / VIDSOUT / PROCHOT#
DDR_PG_CTRL → DDR_VTT_CNTL
EC_VCCST_PG → VCCST_PWRGD
H_CPUPWRGD / H_PLTRST_CPU# / H_PM_SYNC_R / H_PM_DOWN / H_PECI / H_THERMTRIP# → PROCPWRGD / RESET# / PM_SYNC / PM_DOWN / PECI / THERMTRIP#
SKTOCC# / CATERR# → SKTOCC# / CATERR#
ZVM# / MSM# / RSVD1 / RSVD2
CFG_0 … CFG_19 → CFG0 … CFG7
BPM#_0 … BPM#_3 → XDP_BPM#0 … XDP_BPM#3 → TC1 … TC4
PROC_TDO / PROC_TDI / PROC_TMS / PROC_TCK → CPU_XDP_TDO / CPU_XDP_TDI / CPU_XDP_TMS / CPU_XDP_TCK0
PROC_TRST# / PROC_PREQ# / PROC_PRDY# → CPU_XDP_TRST# / XDP_PREQ# / XDP_PRDY#
CFG_RCOMP → RC18 49.9_0402_1%

Sensitive
Sensitive

PROC_SELECT# should be unconnected on CFL processor
EDS1.2 8/21

Near CPU side
follow 1050 Request
8/21

PU 330K follow CRB
8/21

The CFG signals have a default value of '1' if not terminated on the board.

CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted
* 1 = (Default) Normal Operation;
0 = Stall.

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
* 0 = Lane numbers reversed.

CFG[4]: eDP enable:
1 = Disabled.
* 0 = Enabled.

CFG[6:5]: PCI Express* Bifurcation:
00 = 1 x8, 2 x4 PCI Express*
01 = reserved
10 = 2 x8 PCI Express*
* 11 = 1 x16 PCI Express*

CFG[7]: PEG Training:
* 1 = (default) PEG Train immediately following RESET# de assertion.
0 = PEG Wait for BIOS for training.

*CFG Pin Use CMC debug on DDX03 R02 Schematic.

To be confirm

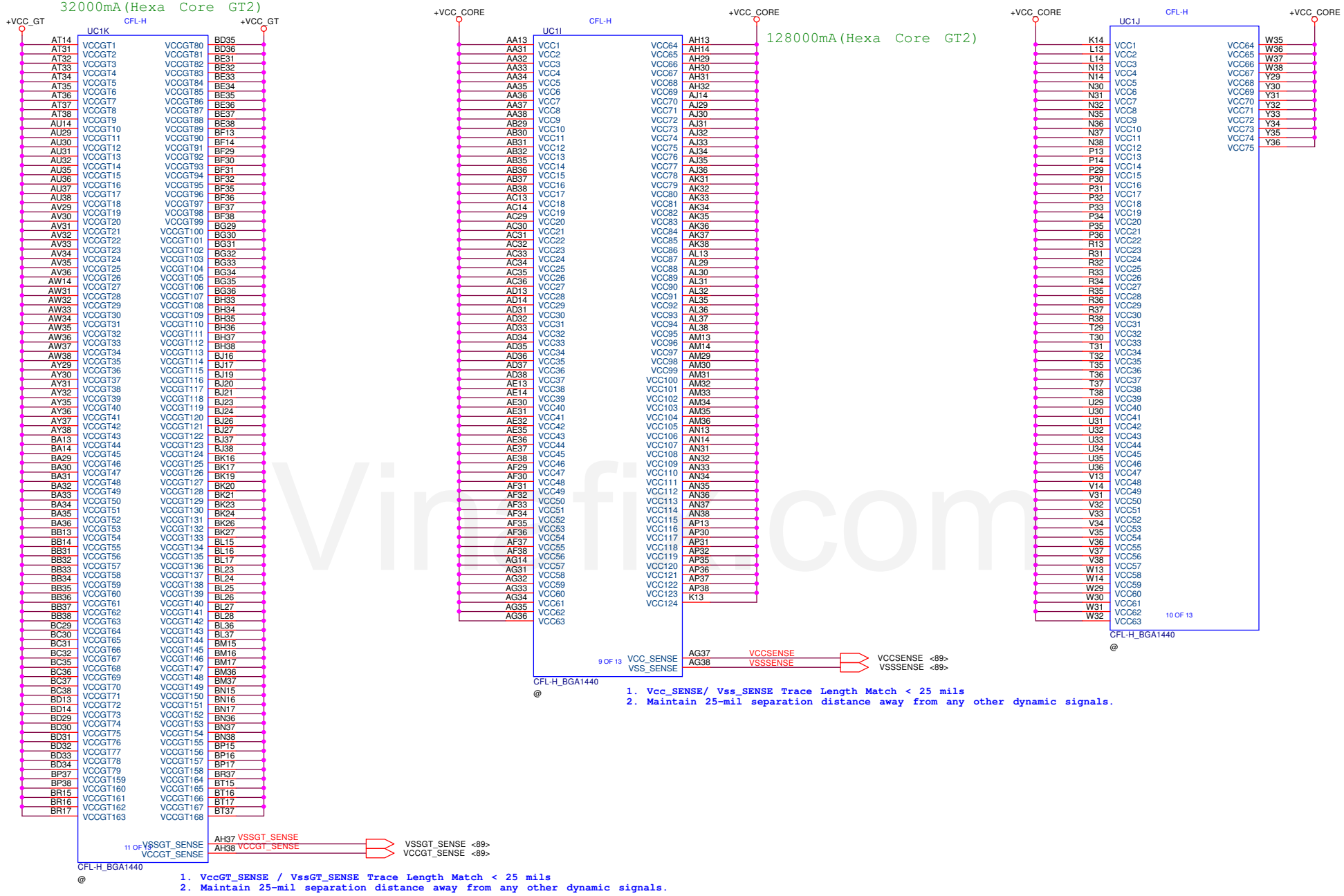
Trace Width/Space: 4 mil/ 12 mil
Max Trace Length: 600 mil

Place to CPU side
Place to CPU side

SVID

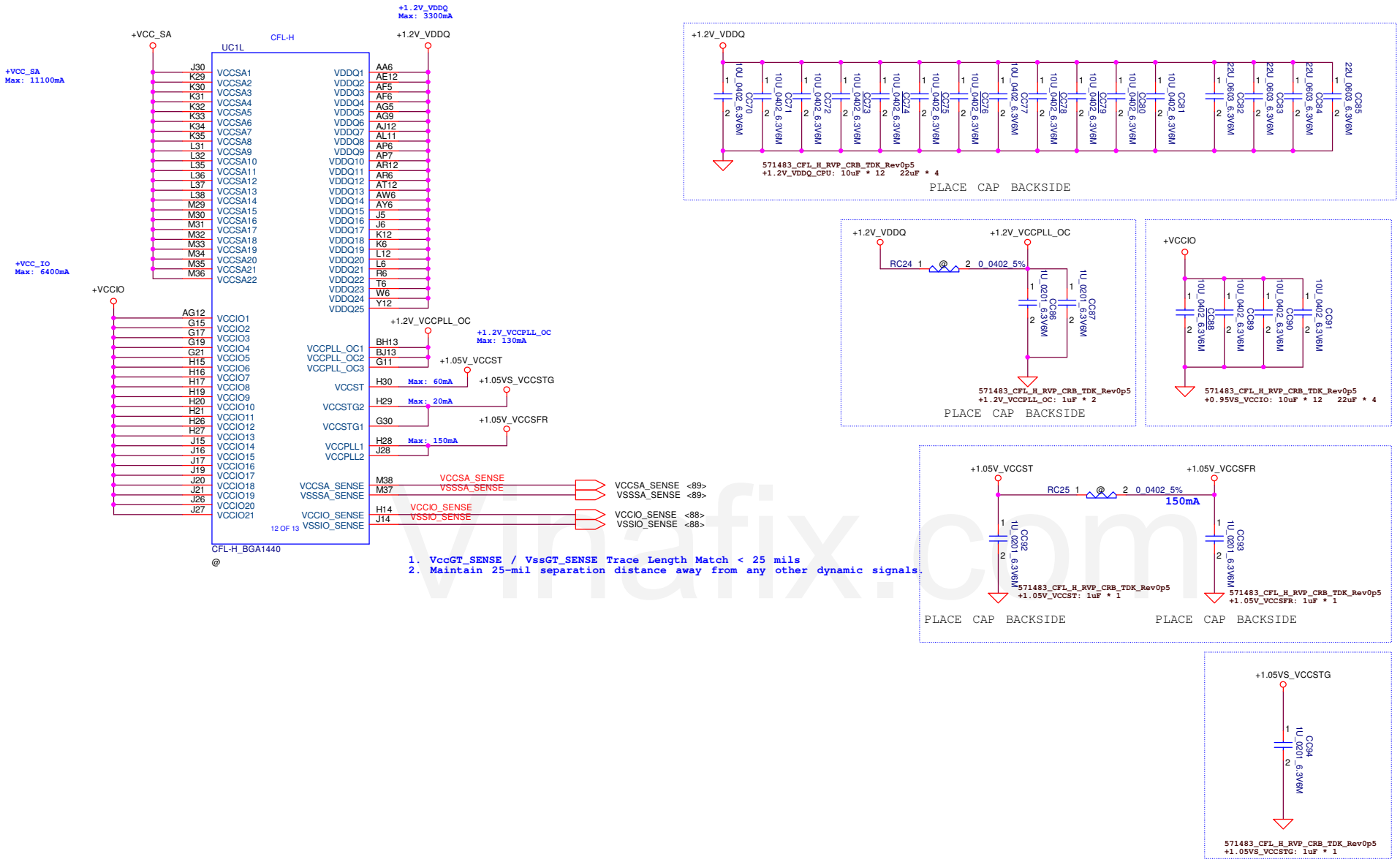
Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.
Title: CFL-H(5/8)CFG,SVID
Size: Custom | Document Number: FH58F M/B LA-J251P | Rev: 1.0
Date: Monday, August 12, 2019 | Sheet 10 of 101



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.			
Title: CFL-H(6/8)VCC CORE/GT			
Size: Custom	Document Number: FH58F M/B LA-J251P		Rev: 1.0
Date: Monday, August 12, 2019	Sheet 11 of 101		



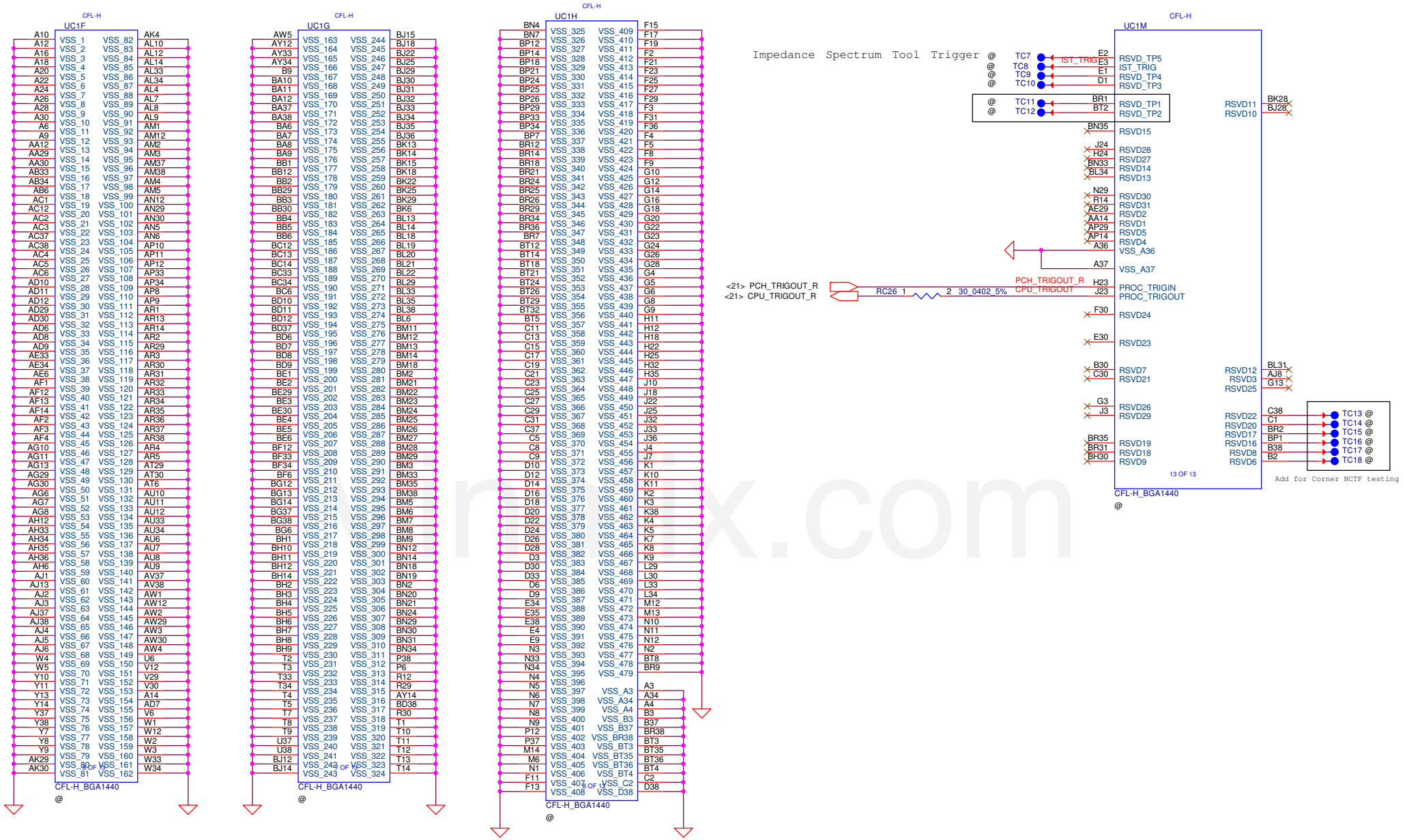
Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.

Title: CFL-H(7/8)VCCSA/VCCIO/VDDQ

Size	Document Number	Rev
Custom	FH58F M/B LA-J251P	1.0

Date: Monday, August 12, 2019 Sheet 12 of 101



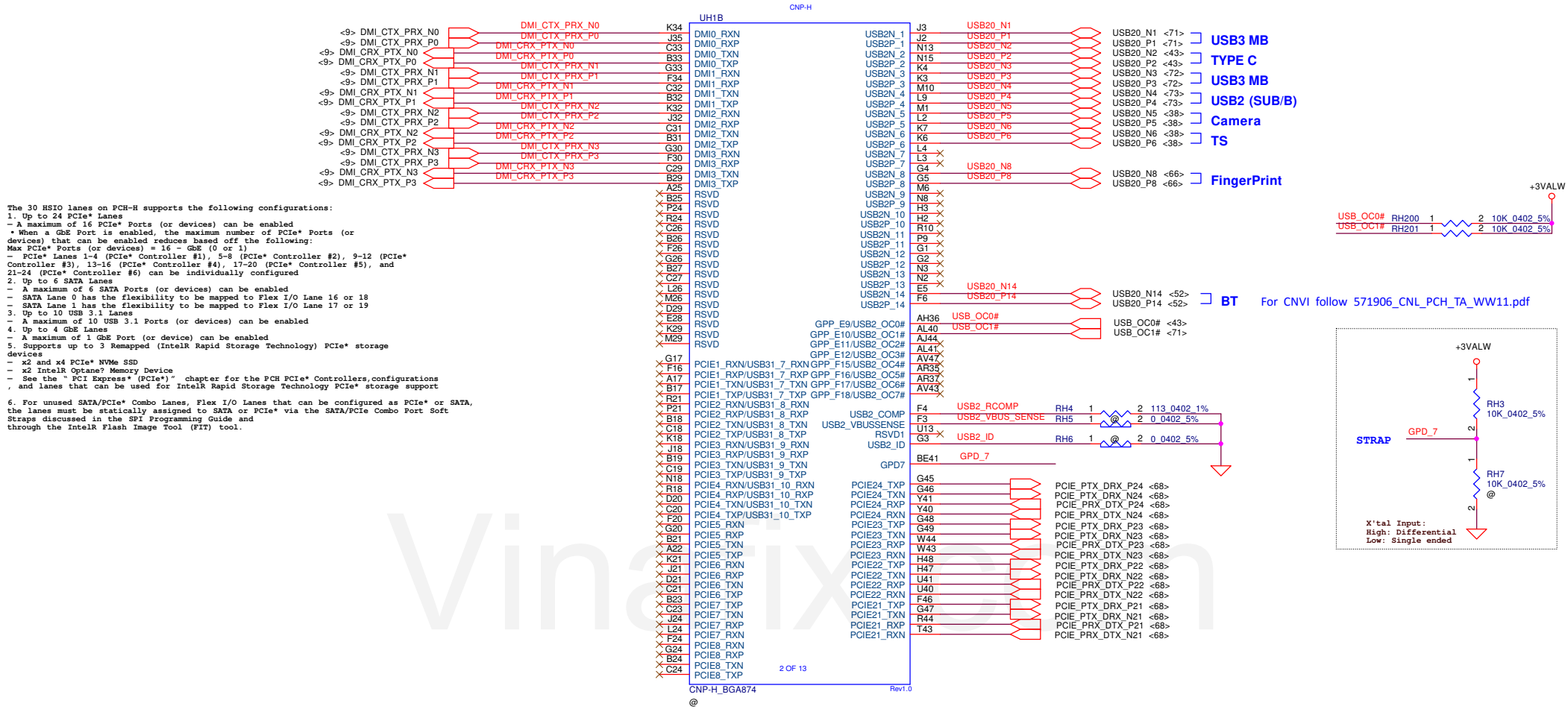
Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.

Title: **CFL-H(8/8)GND/RSVD**

Size	Document Number	Rev
Custom	FH58F M/B LA-J251P	1.0

Date: Monday, August 12, 2019 Sheet 13 of 101



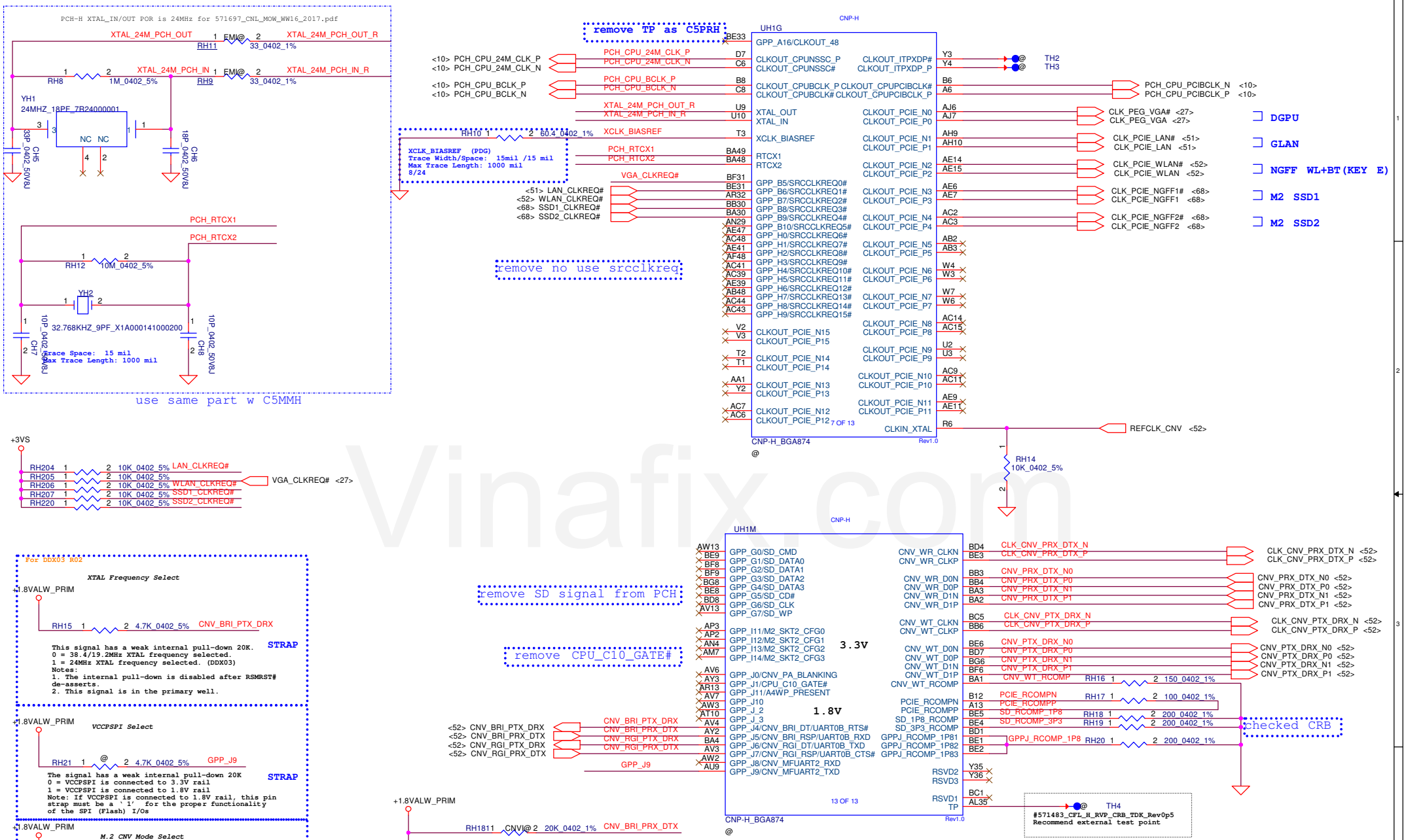
The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
– A maximum of 16 PCIe* Ports (or devices) can be enabled
  • When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 – GbE (0 or 1)
– PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
– A maximum of 6 SATA Ports (or devices) can be enabled
– SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
– SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
– A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
– A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (IntelR Rapid Storage Technology) PCIe* storage devices
– x2 and x4 PCIe* NVMe SSD
– x2 IntelR Optane? Memory Device
– See the " PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers,configurations , and lanes that can be used for IntelR Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the IntelR Flash Image Tool (FIT) tool.

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7 / PCIe* #1	USB3.1 #8 / PCIe* #2	USB3.1 #9 / PCIe* #3	USB3.1 #10 / PCIe* #4	PCIe* #5 / GbE	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9 / GbE	PCIe* #10	PCIe* #11 / SATA 0a	PCIe* #12 / SATA 1a / GbE	PCIe* #13 / SATA 0b / GbE	PCIe* #14 / SATA 1b	PCIe* #15 / SATA 2	PCIe* #16 / SATA 3	PCIe* #17 / SATA 4	PCIe* #18 / SATA 5	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
Intel® RST Support							No Support				No Support				Yes				No Support				Yes				Yes			

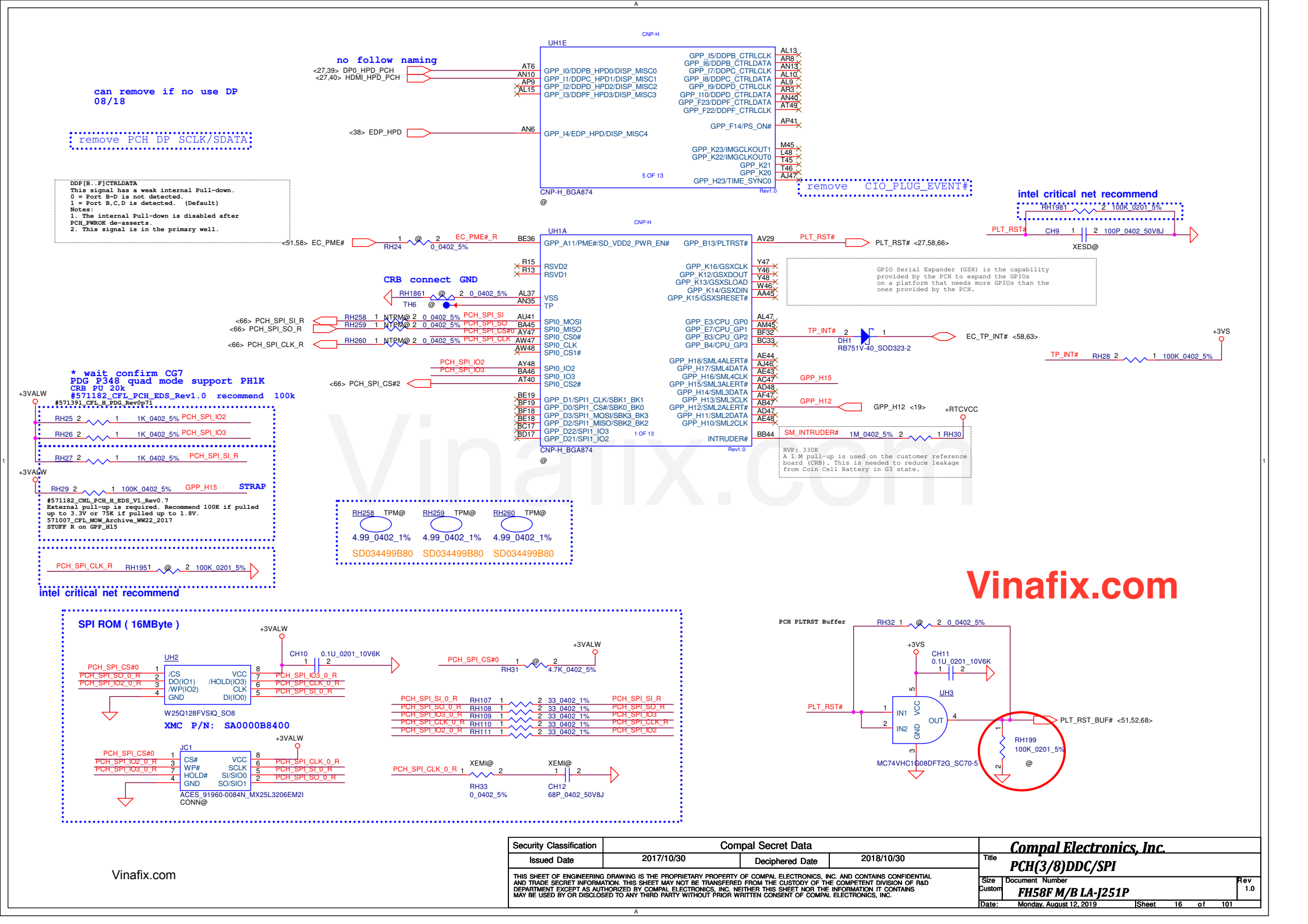
Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.			
Title	PCH(1/8)DMI/PCIE/USB2		
Size: Custom	Document Number: FH58F M/B LA-J251P		Rev: 1.0
Date: Monday, August 12, 2019	Sheet 14 of 101		



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.			
Title	PCH(2/8)CLK/CNVI/SD		
Size: Custom	Document Number: FH58F M/B LA-J251P		Rev: 1.0
Date: Monday, August 12, 2019	Sheet 15 of 101		



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.			
Title	PCH(3/8)DDC/SPI		
Size	Document Number		Rev
Custom	FH58F M/B LA-J251P		1.0
Date:	Monday, August 12, 2019	Sheet	16 of 101

#571391_CFL_H_PDG_Rev0p5
- eSPI clock and eSPI data mismatched: <500 mils.
- eSPI clock and eSPI chip select mismatched: <500 mils.
- eSPI signal maximum 9 Vias
* If DATA signals are entirely routed on MS, stuff the resistor with 15 Ohm.

USB3 MB
USB3 Type C
USB3 MB
LPC Bus
check straps
LPC : +3.3V
CONFIRM WITH SW
M.2 SSD PCIE L3
M.2 SSD PCIE L2
NGFF
WL+BT(KEY E)
M.2 SSD PCIE L1
HDD
GLAN
M.2 SSD PCIE L0
M.2 SSD PCIE/SATA select pin
CONFIRM WITH SW

	GPP_F13 DGPU_PRSNT#
DIS, Optimus	0
UMA	1

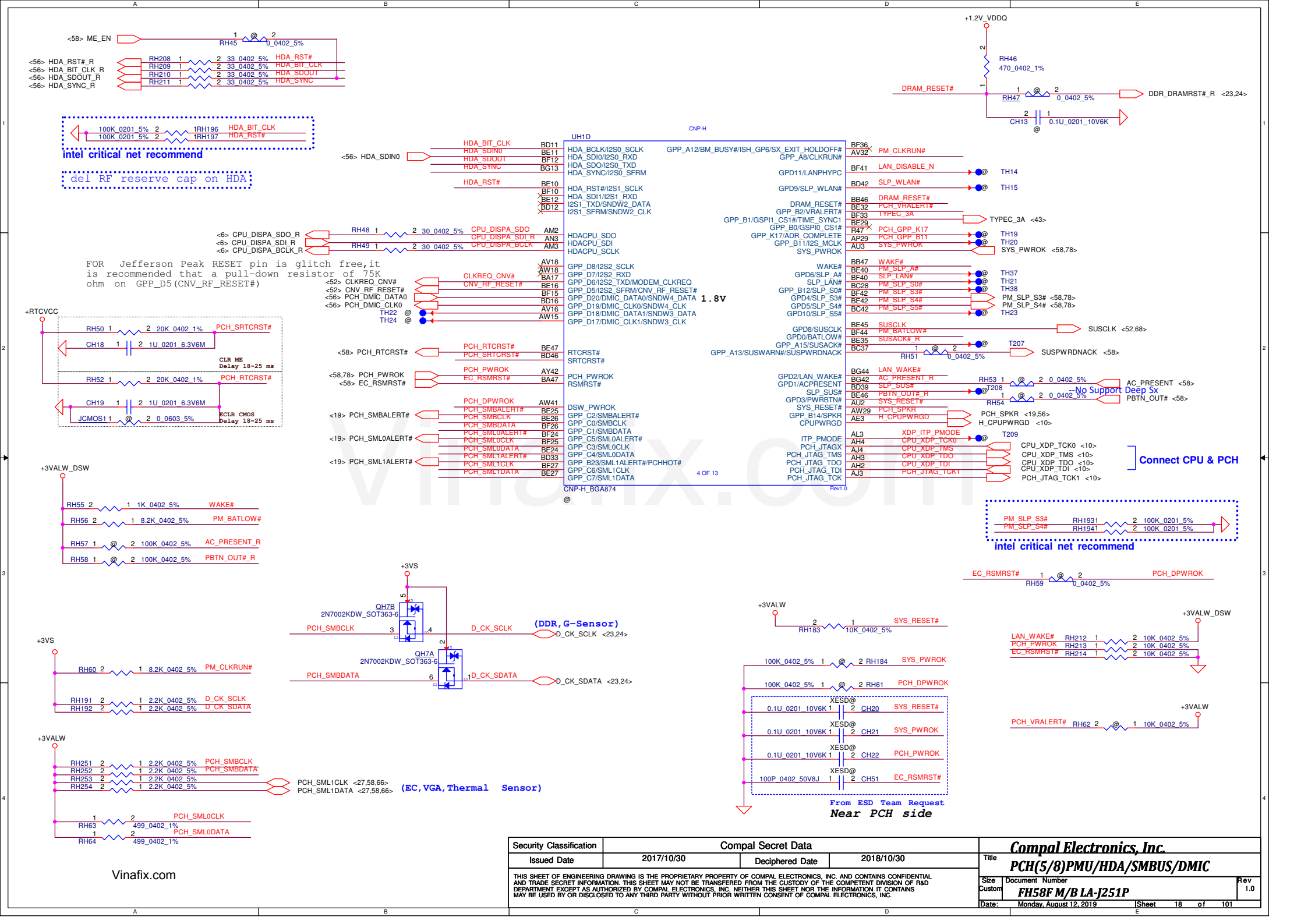
Security Classification	Compal Secret Data
Issued Date	2017/10/30
Deciphered Date	2018/10/30

Compal Electronics, Inc.

Title: PCIE/SATA/USB3/eSPI

Size: Custom | Document Number: FH58F M/B LA-J251P | Rev: 1.0

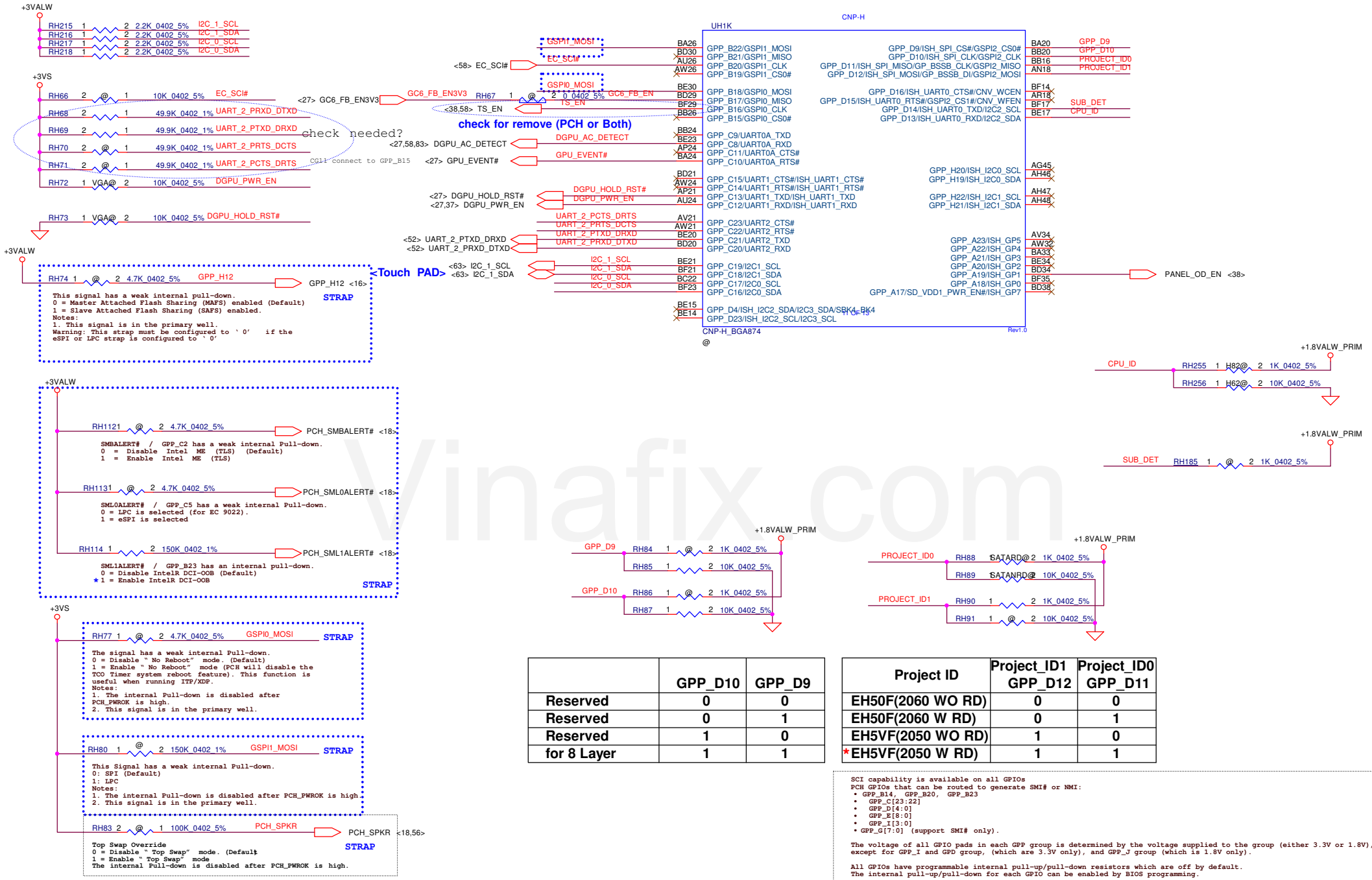
Date: Monday, August 12, 2019 | Sheet 17 of 101



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.			
Title	PCH(5/8)PMU/HDA/SMBUS/DMIC		
Size	Document Number		Rev
Custom	FH58F M/B LA-J251P		1.0
Date:	Monday, August 12, 2019	Sheet	18 of 101



	GPP_D10	GPP_D9
Reserved	0	0
Reserved	0	1
Reserved	1	0
for 8 Layer	1	1

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
EH50F(2060 WO RD)	0	0
EH50F(2060 W RD)	0	1
EH5VF(2050 WO RD)	1	0
*EH5VF(2050 W RD)	1	1

SCI capability is available on all GPIOs
PCH GPIOs that can be routed to generate SMI# or NMI:
- GPP_B14, GPP_B20, GPP_B23
- GPP_C[23:22]
- GPP_D[4:0]
- GPP_E[8:0]
- GPP_I[3:0]
- GPP_G[7:0] (support SMI# only).

The voltage of all GPIO pads in each GPP group is determined by the voltage supplied to the group (either 3.3V or 1.8V), except for GPP_I and GPD group, (which are 3.3V only), and GPP_J group (which is 1.8V only).

All GPIOs have programmable internal pull-up/pull-down resistors which are off by default.
The internal pull-up/pull-down for each GPIO can be enabled by BIOS programming.

Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.

Title: PCH(6/8)GPIO/I2C/UART/STRAP

Size	Document Number	Rev
Custom	FH58F M/B LA-J251P	1.0

Date: Monday, August 12, 2019 Sheet 19 of 101

GPIO Group	Voltage
GPPA	3.3V
GPPB GPPC	3.3V
GPPD	3.3V * 1.8V
GPPE GPPF	3.3V
GPPG	3.3V
GPPH GPPK	3.3V
GPPI	3.3V Only
GPPJ	1.8V Only
GPD	3.3V Only

Place Near UH1 VCCPRIM_1_0523~29
3-5MM FROM PACKAGE EDGE

place near VCCDUSB
FOR W22/W23

1-3MM FROM PACKAGE
VCCPRIM_MPHY W31

1-3MM FROM PACKAGE EDGE

1-5MM FROM PACKAGE EDGE
FOR VCCAPLL C1/C2

1-3MM FROM PACKAGE EDGE
FOR VCCA_BCLK V19

1-5MM FROM PACKAGE EDGE
FOR VCCAPLL B1/B2/B3

1-3MM FROM PACKAGE EDGE

LC filter close to pin
1uF 1-3MM FROM PACKAGE EDGE

change to 10k

reserve filter follow CRB
8/21

1-3MM FROM PACKAGE
FOR PGPPEF AE35/AE37

1-3MM FROM PACKAGE
FOR PGPPHK AC35/AC36

1-3MM FROM PACKAGE
FOR VCCPRIM AY8/BB7

reserved for cnvi

near AG19/AG20

SP02000RO00

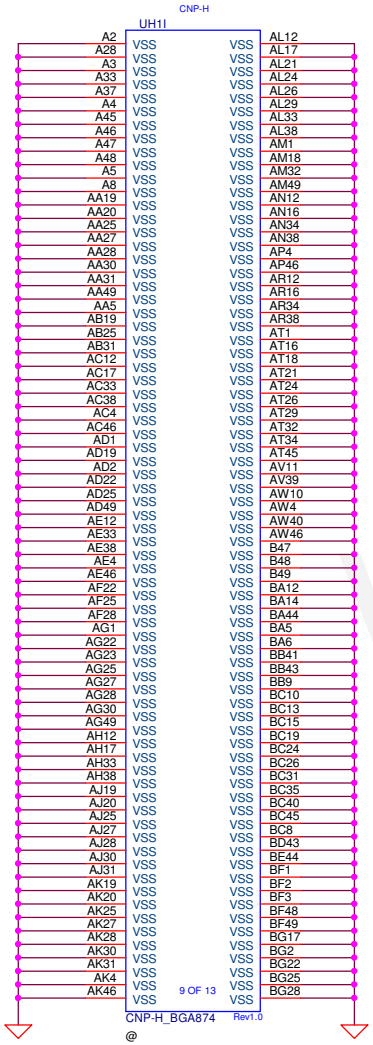
Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

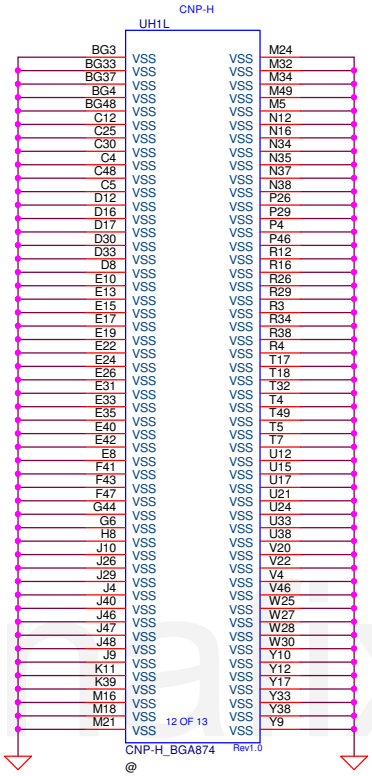
Compal Electronics, Inc.

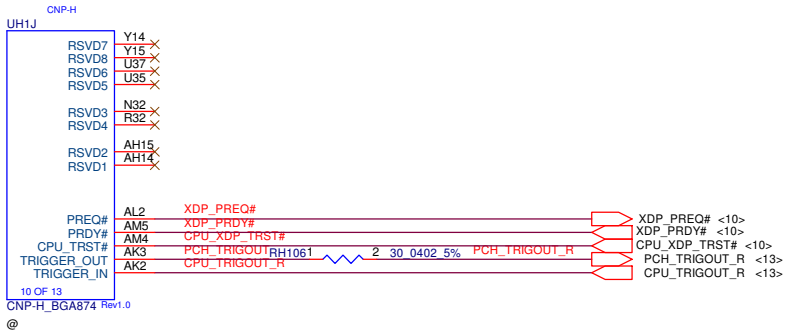
Title: PCH(7/8)Power

Size: Custom | Document Number: FH58F M/B LA-J251P | Rev: 1.0

Date: Monday, August 12, 2019 | Sheet 20 of 101







Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.

Title: PCH(8/8)GND/RSVD

Size: Custom | Document Number: FH58F M/B LA-J251P | Rev: 1.0

Date: Monday, August 12, 2019 | Sheet 21 of 101

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 22 of 101	

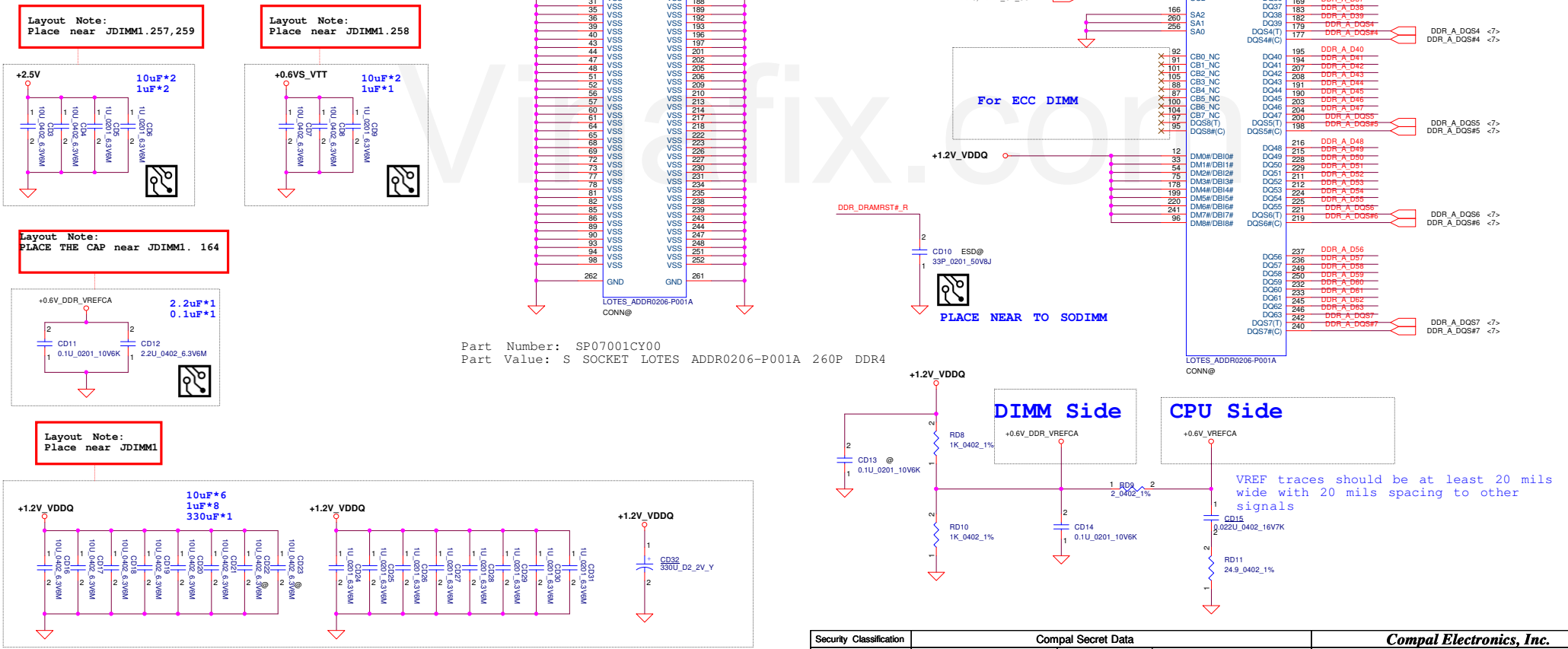
CHANNEL-A

BOT REVERSE TYPE (4 mm)

Interleaved Memory

TOP: JDIMM1 CONN Non-ECC DIMM

SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S



Part Number: SP07001CY00
Part Value: S SOCKET LOTES ADDR0206-P001A 260P DDR4

Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.			
Title	DDRIV_CHA: DIMM0		
Size	Document Number		Rev
	FH58F M/B LA-J251P		1.0
Date: Monday, August 12, 2019	Sheet 23 of 101		

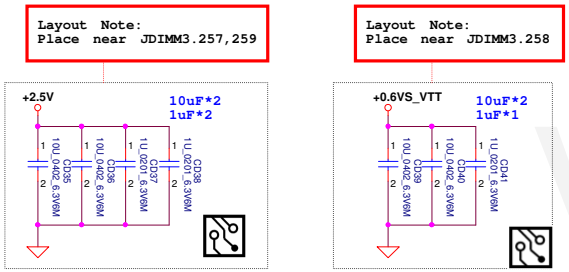
CHANNEL-B

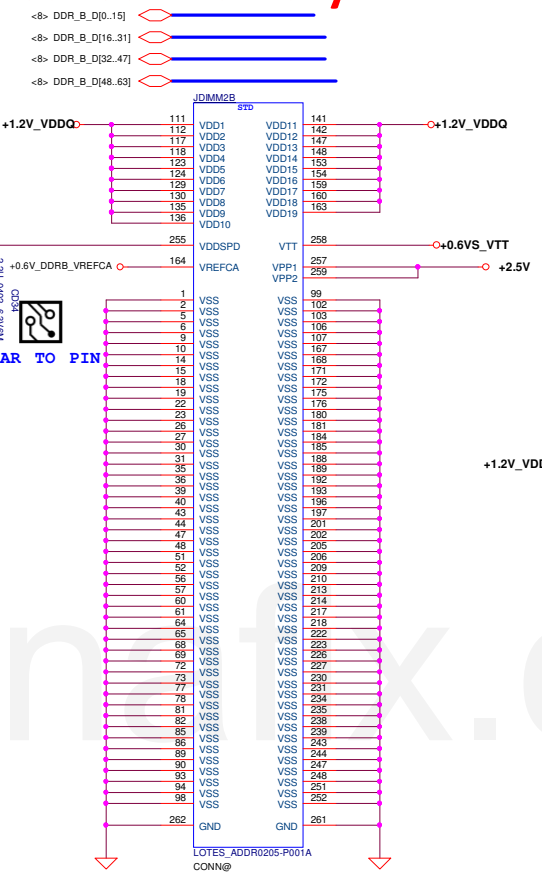
TOP: JDIMM2 CONN Non-ECC DIMM

Interleaved Memory

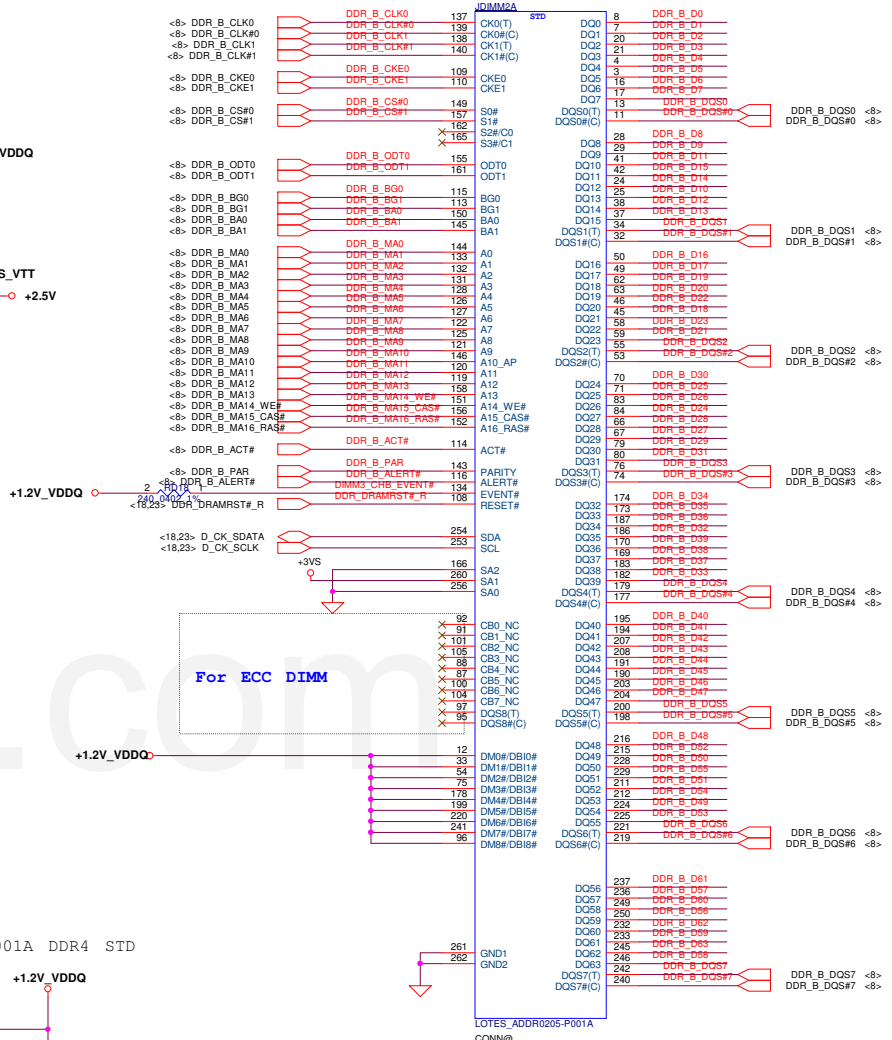
BOT STD (4 mm)

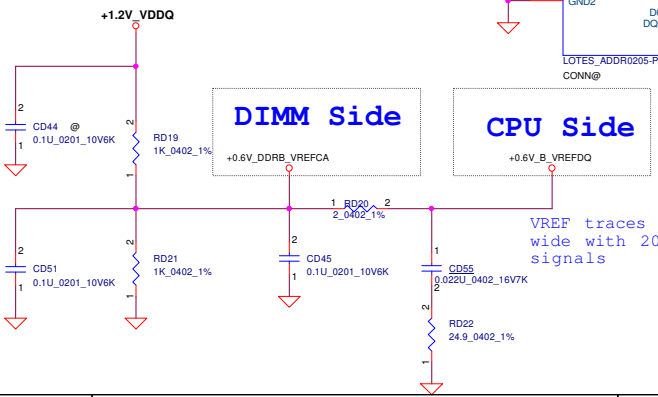
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S





Part Number: SP07001HW00
Part Value: S SOCKET LOTES ADDR0205-P001A DDR4 STD





Vinafix.com

Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.

Title: **DDRIV_CHB: DIMM0**

Size	Document Number	Rev
	FH58F M/B LA-J251P	1.0

Date: Monday, August 12, 2019 | Sheet 24 of 101

Reserve Page

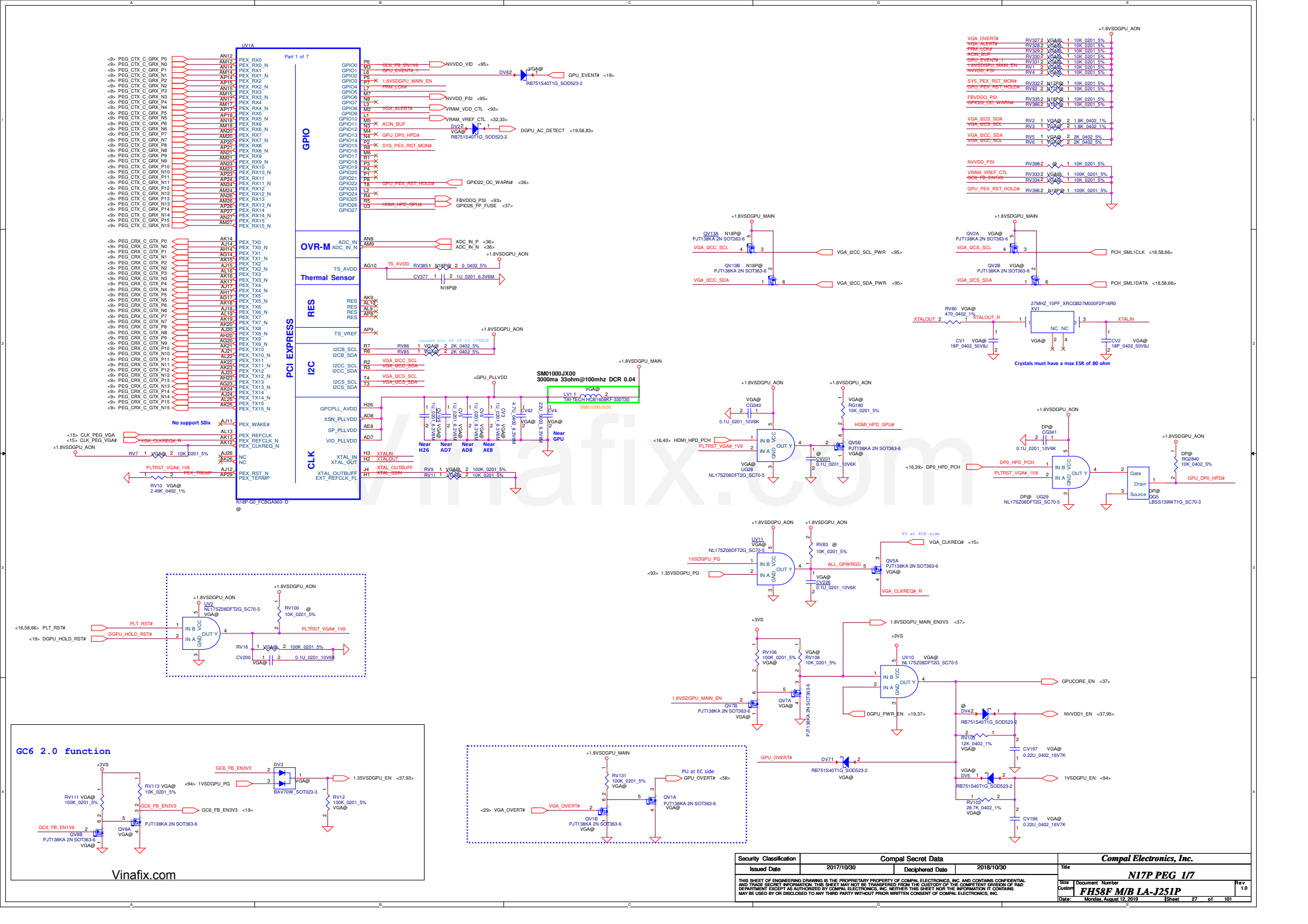
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 25 of 101	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

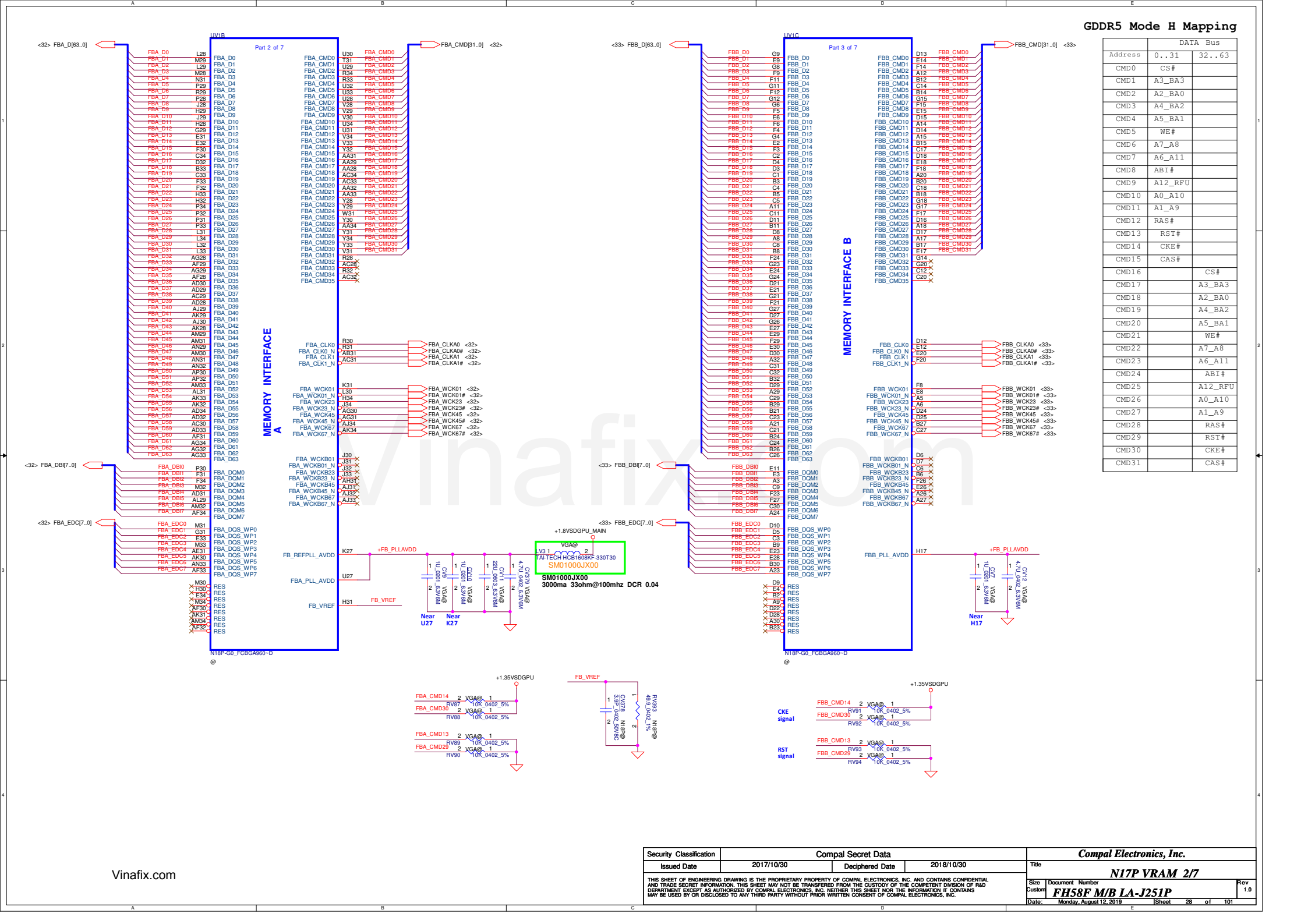
Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 26 of 101	

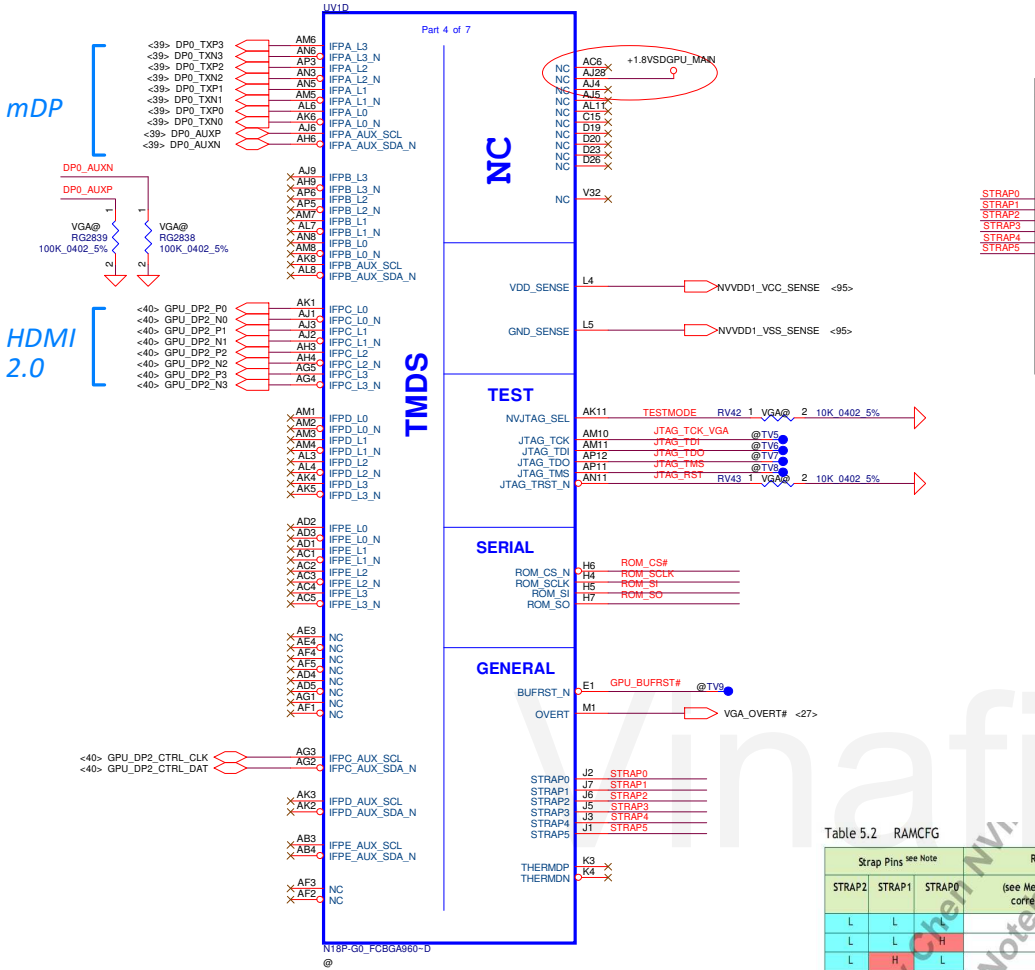


Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.	
Title	N17P PEG 1/7
Size: Custom	Document Number: FH58F M/B LA-J251P
Rev	1.0
Date: Monday, August 12, 2019	Sheet 27 of 101


GDDR5 Mode H Mapping
DATA Bus
Address
0..31
32..63
CMD0 CS#
CMD1 A3_BA3
CMD2 A2_BA0
CMD3 A4_BA2
CMD4 A5_BA1
CMD5 WE#
CMD6 A7_A8
CMD7 A6_A11
CMD8 ABI#
CMD9 A12_RFU
CMD10 A0_A10
CMD11 A1_A9
CMD12 RAS#
CMD13 RST#
CMD14 CKE#
CMD15 CAS#
CMD16 CS#
CMD17 A3_BA3
CMD18 A2_BA0
CMD19 A4_BA2
CMD20 A5_BA1
CMD21 WE#
CMD22 A7_A8
CMD23 A6_A11
CMD24 ABI#
CMD25 A12_RFU
CMD26 A0_A10
CMD27 A1_A9
CMD28 RAS#
CMD29 RST#
CMD30 CKE#
CMD31 CAS#
UV1B
Part 2 of 7
MEMORY INTERFACE A
N18P-G0_FCBGA960-D
UV1C
Part 3 of 7
MEMORY INTERFACE B
N18P-G0_FCBGA960-D
SM01000JX00
3000ma 33ohm@100mhz DCR 0.04
Near U27
Near K27
Near H17
CKE signal
RST signal
Vinafix.com
Security Classification
Compal Secret Data
Issued Date
2017/10/30
Deciphered Date
2018/10/30
Compal Electronics, Inc.
N17P VRAM 2/7
FH58F M/B LA-J251P
Rev 1.0
Monday, August 12, 2019
Sheet 28 of 101



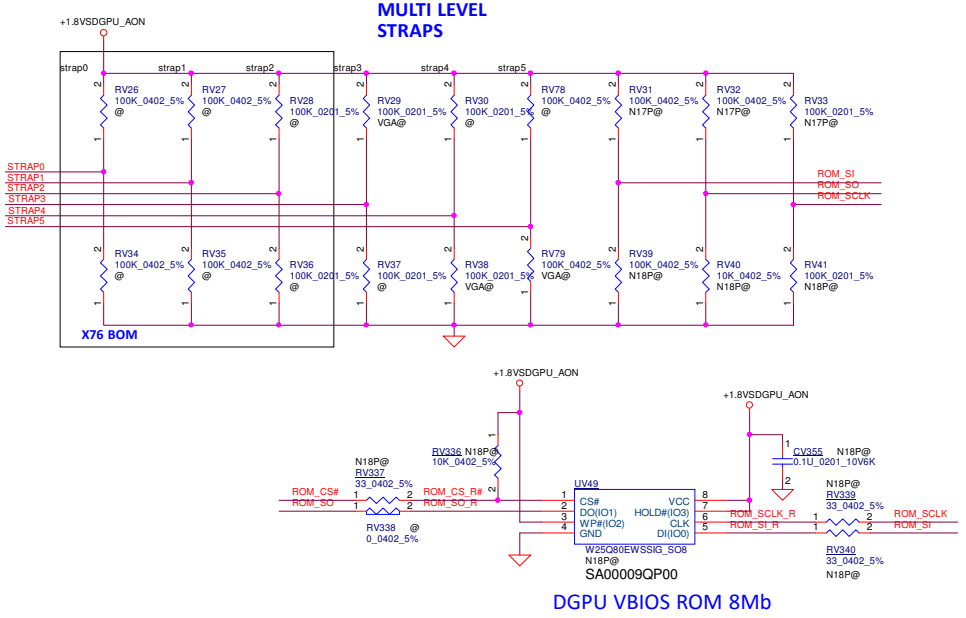


Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 3. N17P-G1/G0/G0-K1[4] GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V[2]	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
			Micron	MT51J256M32HF-70:B	B-die	0x4	7 Gbps	N/A	Full	Post production ready
			Micron	MT51J256M32HF-80:B	B-die	0x4	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
			Hynix	H5GC8H24AJR-R0C	A-die	0x5	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0x5	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]

Table 4. N18P-G0 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35 V and 1.5V[2]	Micron	MT51J256M32HF-80:B	B-die	0x1	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0x2	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V[2]	Samsung	K4G80325FC-HC25	C-die	0x0	8 Gbps	N/A	Full	Production candidate

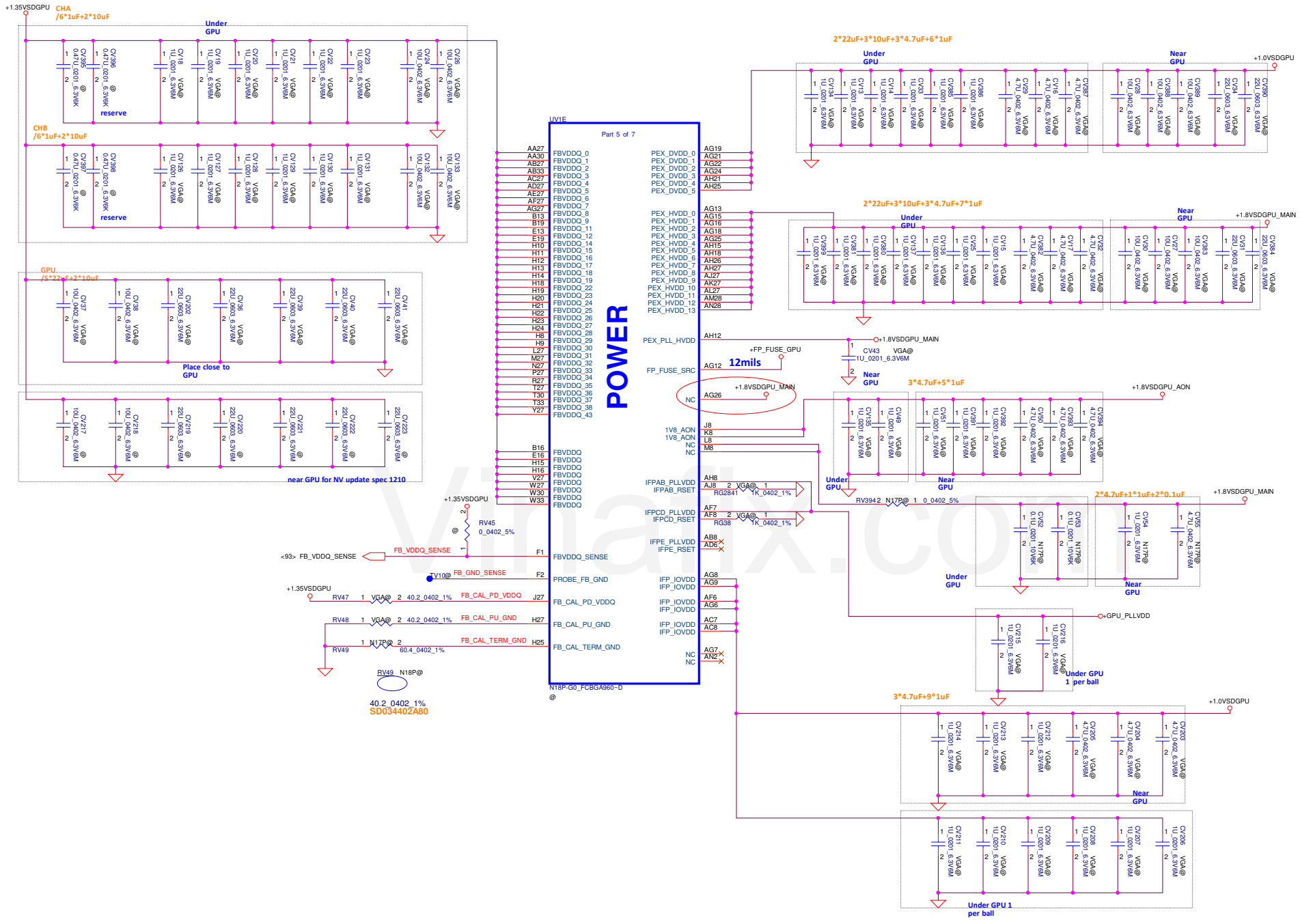
Notes:
1. For N18P-G0, the maximum allowable memory case temperature is 85 °C.
2. DV5 may be required to run WCLK > 3500 MHz. TBD.

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

	SMB_ATL_ADDR	
*	LOW	Single GPU
	High	Dual GPU
	DEVID_SEL	
*	LOW	Orig. Device ID
	High	Support G-Sync GPUID
	VGA_DEVICE	
	LOW	3D Device
*	High	VGA Device
	PCIE_CFG	
*	LOW	Normal signal swing
	High	Reduce the signal amplitude

Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

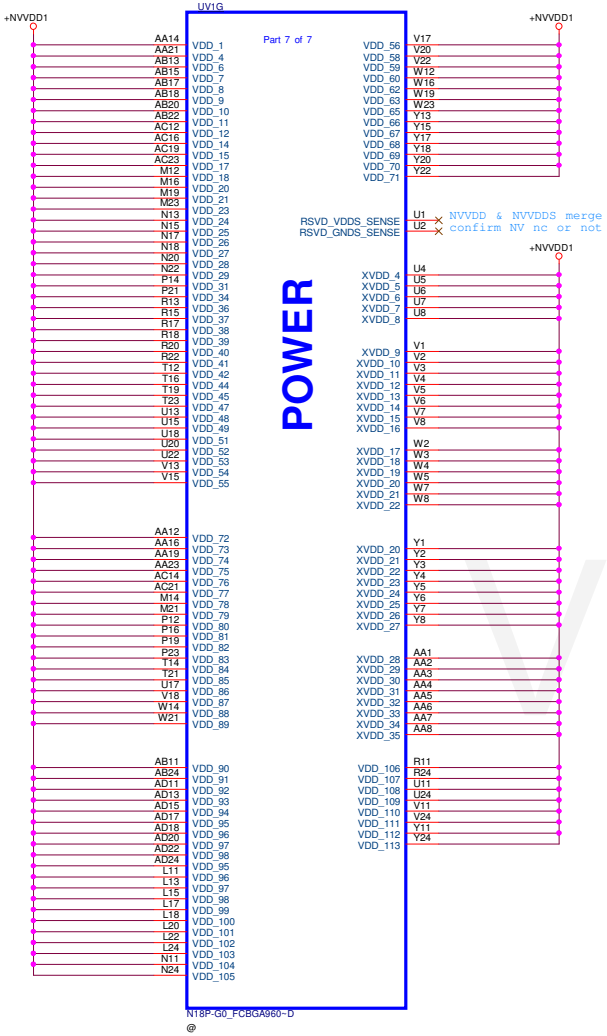
Compal Electronics, Inc.			
Title	N17P STRAP 3/7		
Size	Document Number		Rev
Custom	FH58F M/B LA-J251P		1.0
Date:	Monday, August 12, 2019	Sheet	29 of 101

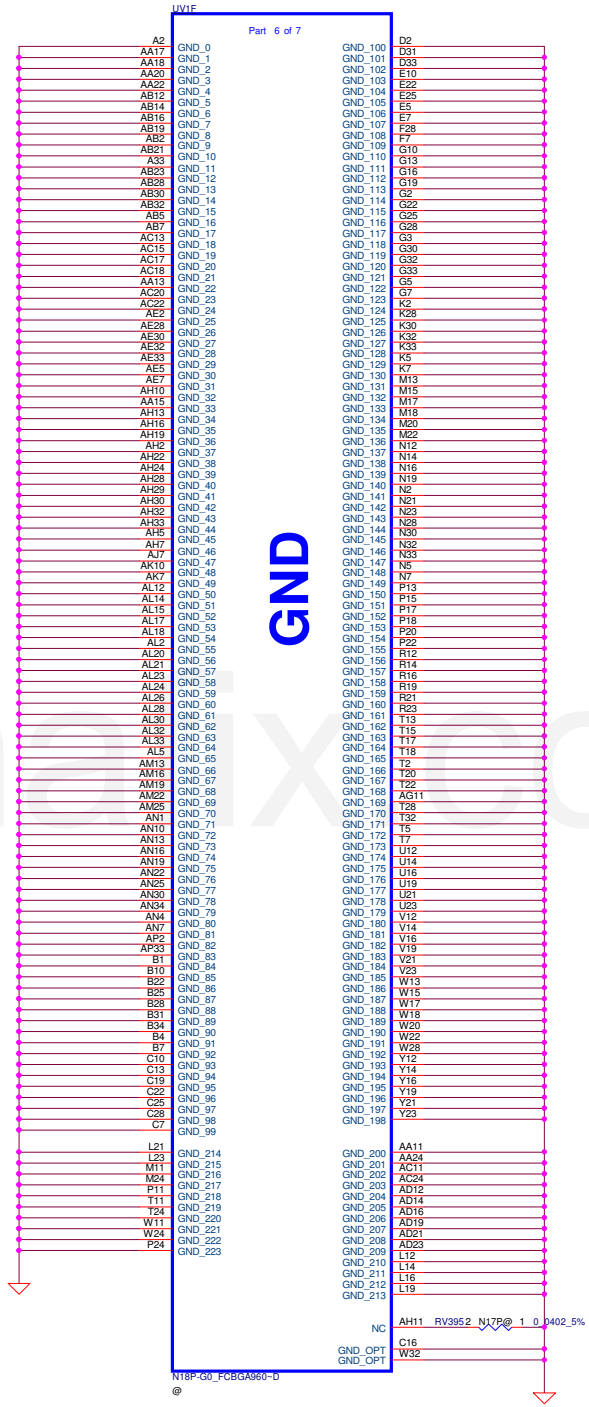


Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.			
Title	N17P POWER 4/7		
Size: Custom	Document Number: FH58F M/B LA-J251P		Rev: 1.0
Date: Monday, August 12, 2019	Sheet 30 of 101		

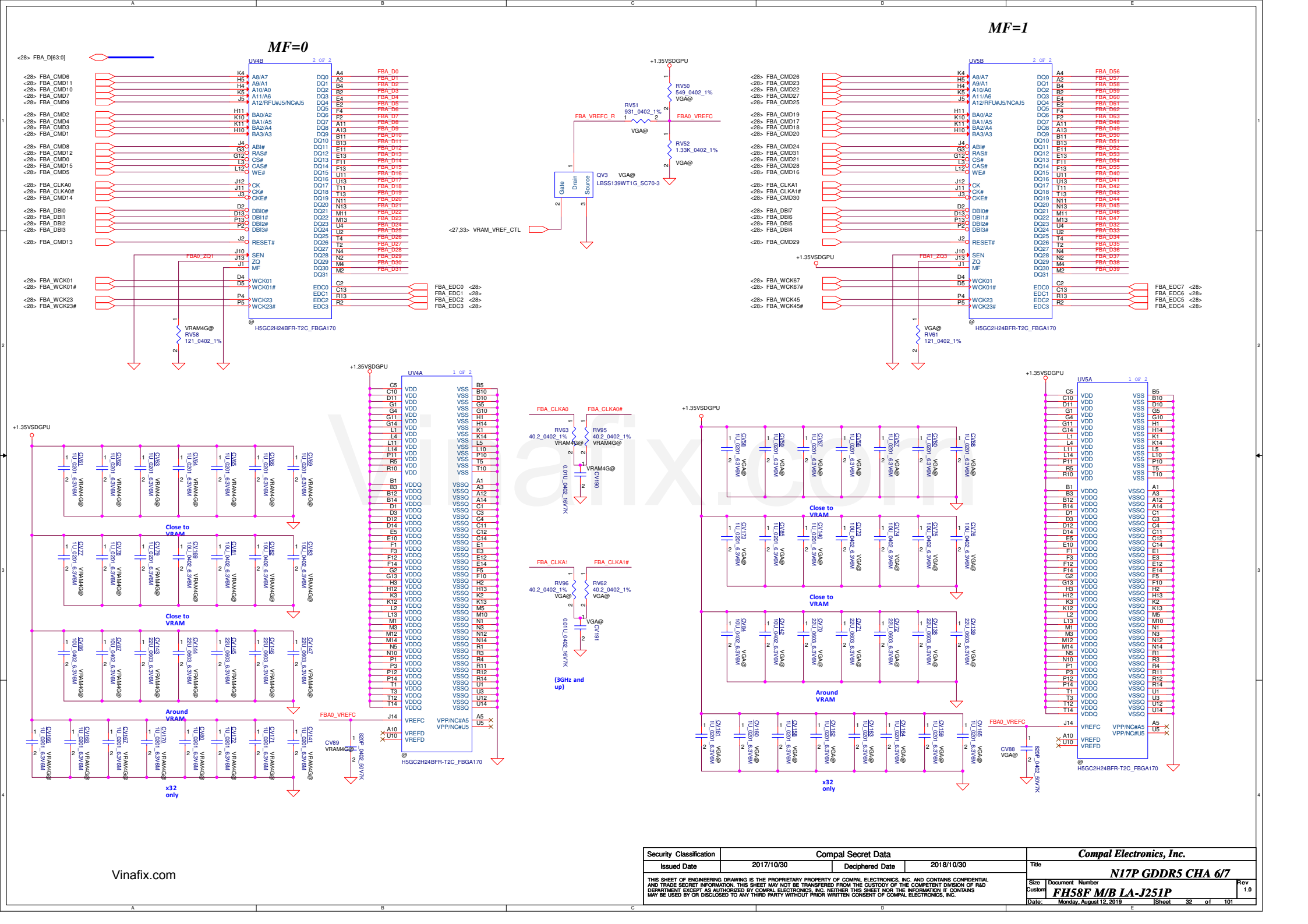
N17P VDDS
1uF*5/4.7uF*5 (under GPU)
330uF*1/22uF*3/10uF*2/4.7uF*2





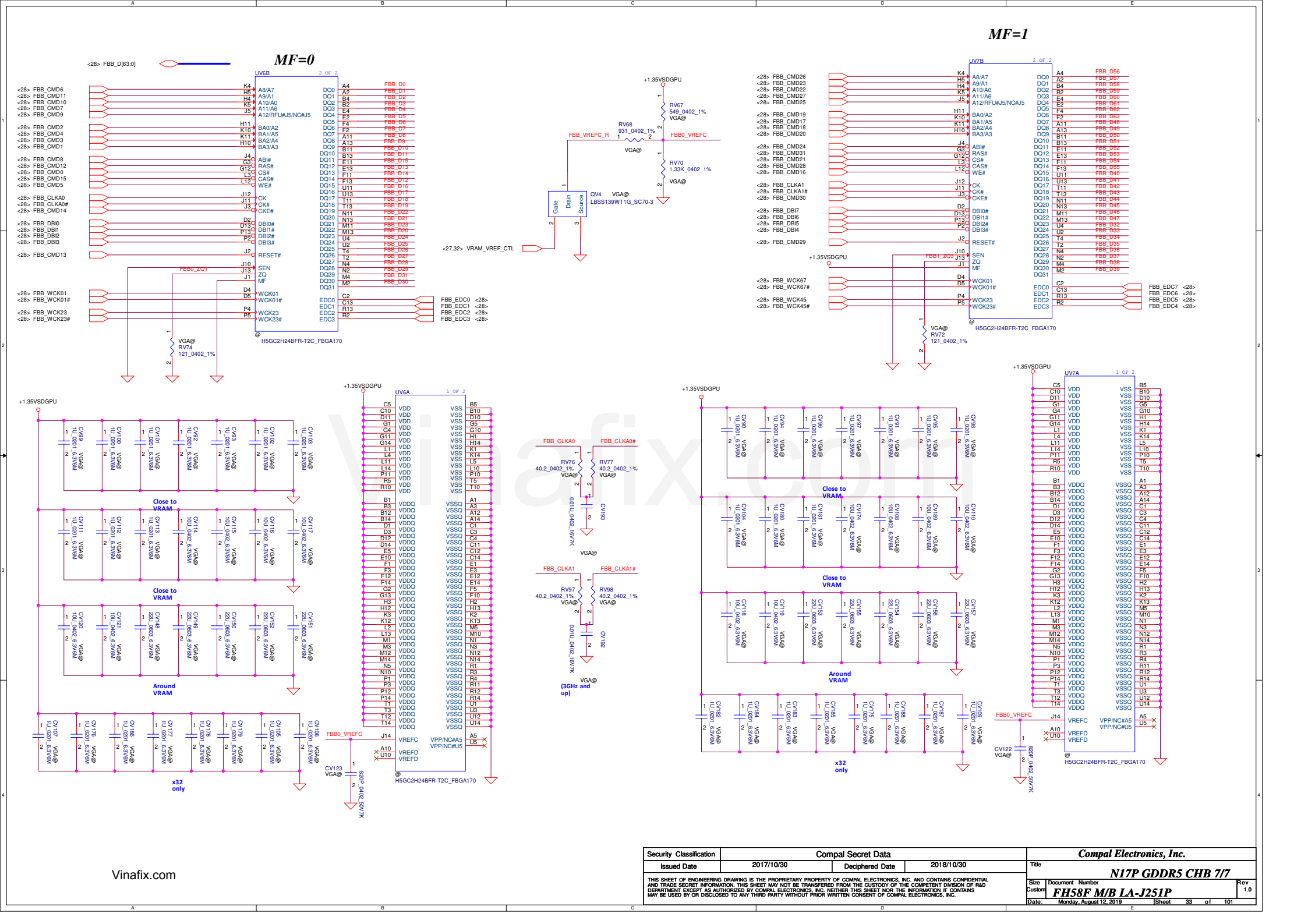
Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.		
Title	N17P POWER & GND 5/7	
Size: Custom	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 31 of 101	



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.			
Title	N17P GDDR5 CHA 6/7		
Size: Custom	Document Number: FH58F M/B LA-J251P		Rev: 1.0
Date: Monday, August 12, 2019	Sheet 32 of 101		



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.			
Title	N17P GDDR5 CHB 7/7		
Size: Custom	Document Number: FH58F M/B LA-J251P		Rev: 1.0
Date: Monday, August 12, 2019	Sheet 33 of 101		

Reserve Page

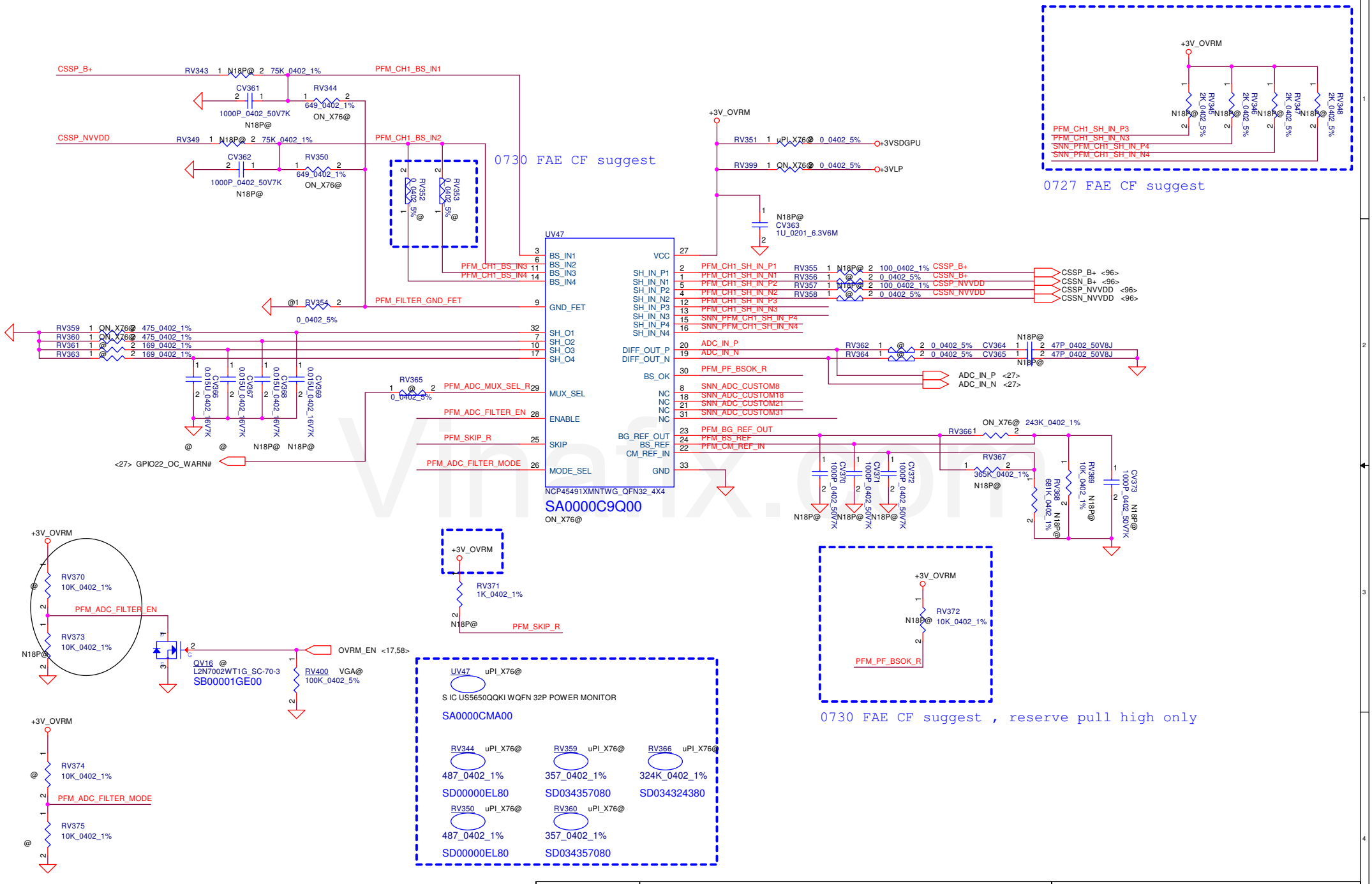
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 34 of 101	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 35 of 101	



Vinafix.com

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

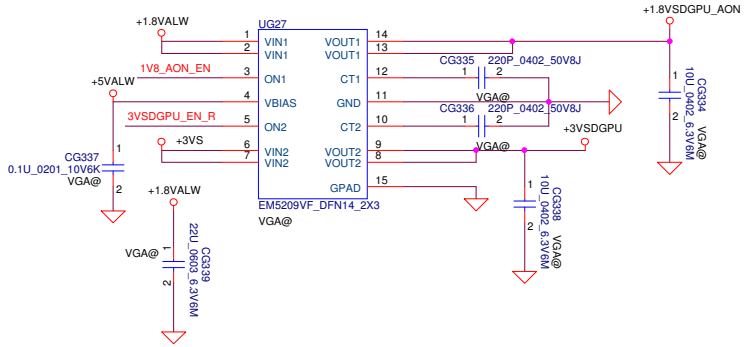
Compal Electronics, Inc.

Title: **OVR-M**

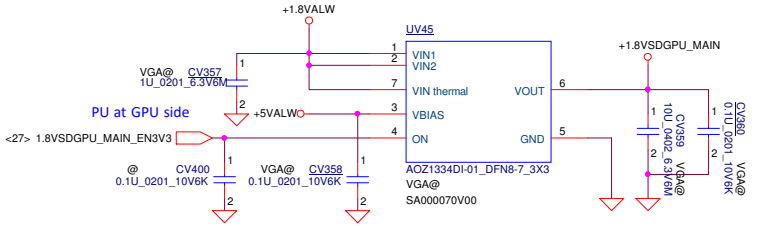
Size: Custom | Document Number: **FH58F M/B LA-J251P** | Rev: 1.0

Date: Monday, August 12, 2019 | Sheet 36 of 101

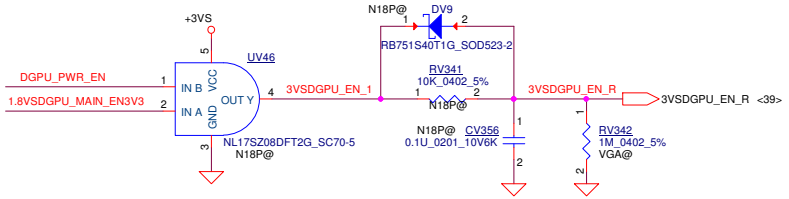
+1.8V_AON/+3VSDGPU



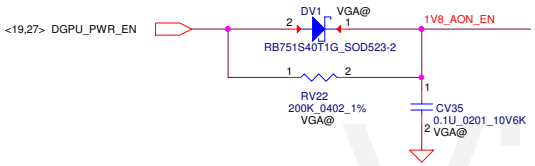
+1.8V_MAIN

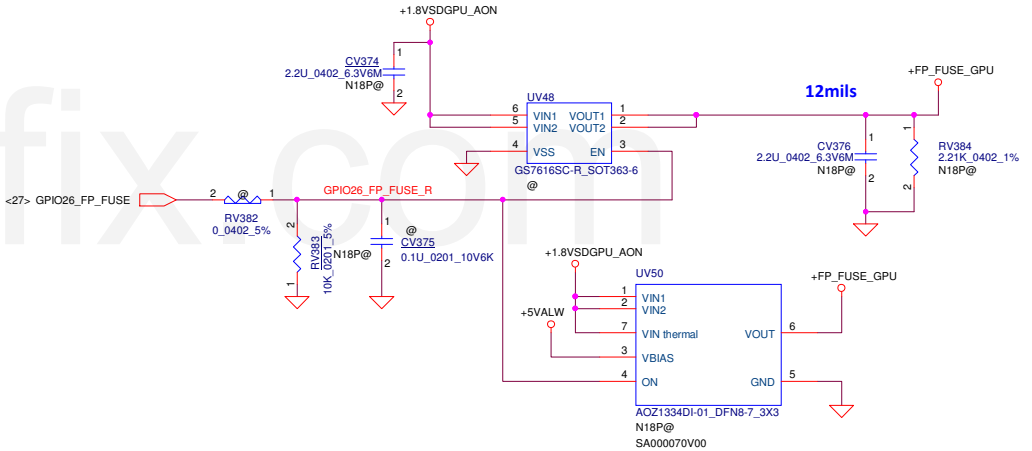


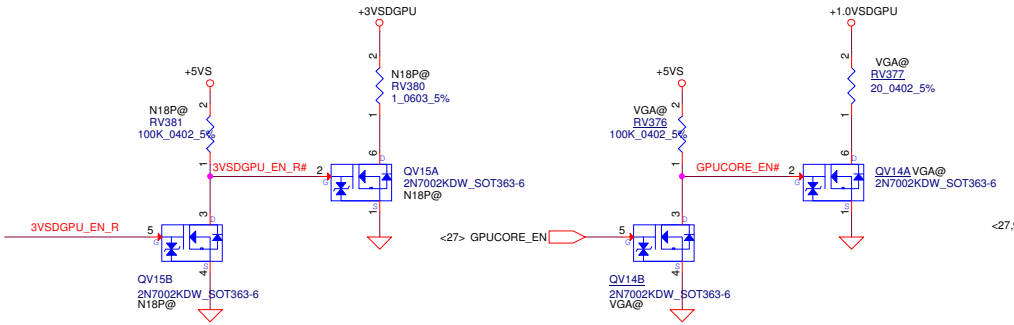
For Power down sequence

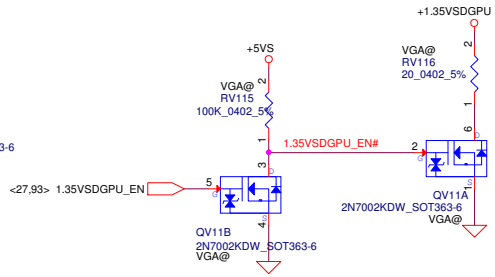


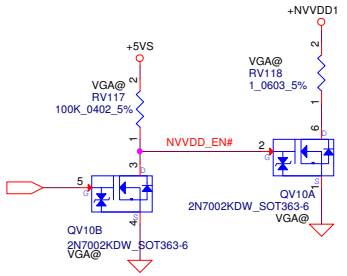
For Power down sequence











Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

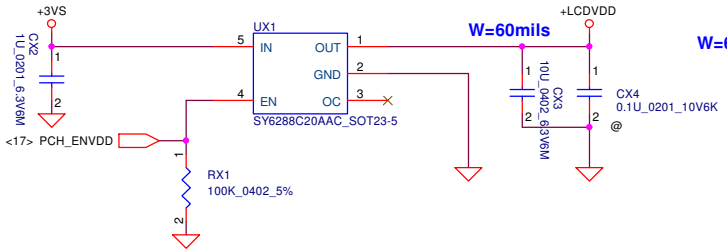
Compal Electronics, Inc.

Title: **GPU DC INTERFACE**

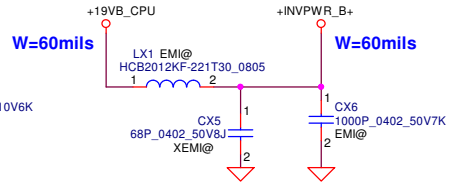
Size	Document Number	Rev
	FH58F M/B LA-J251P	1.0

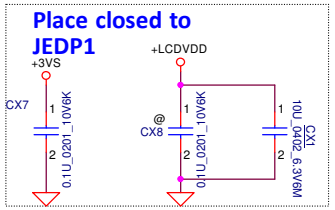
Date: Monday, August 12, 2019 Sheet 37 of 101

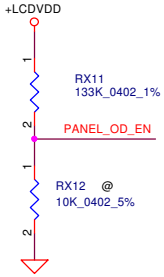
LCD POWER CIRCUIT

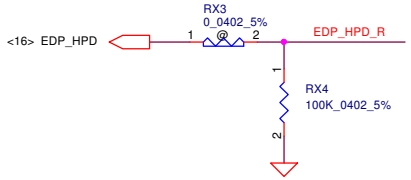


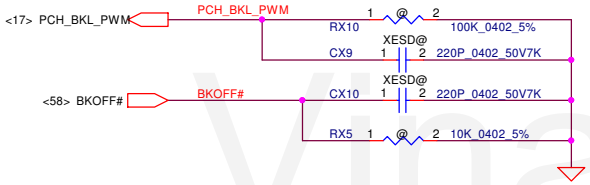
SM01000EJ00 3000ma
220ohm@100mhz
DCR 0.04



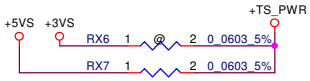




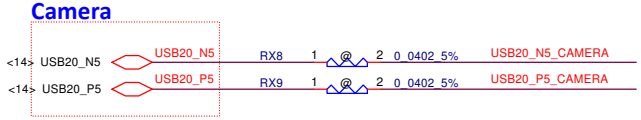




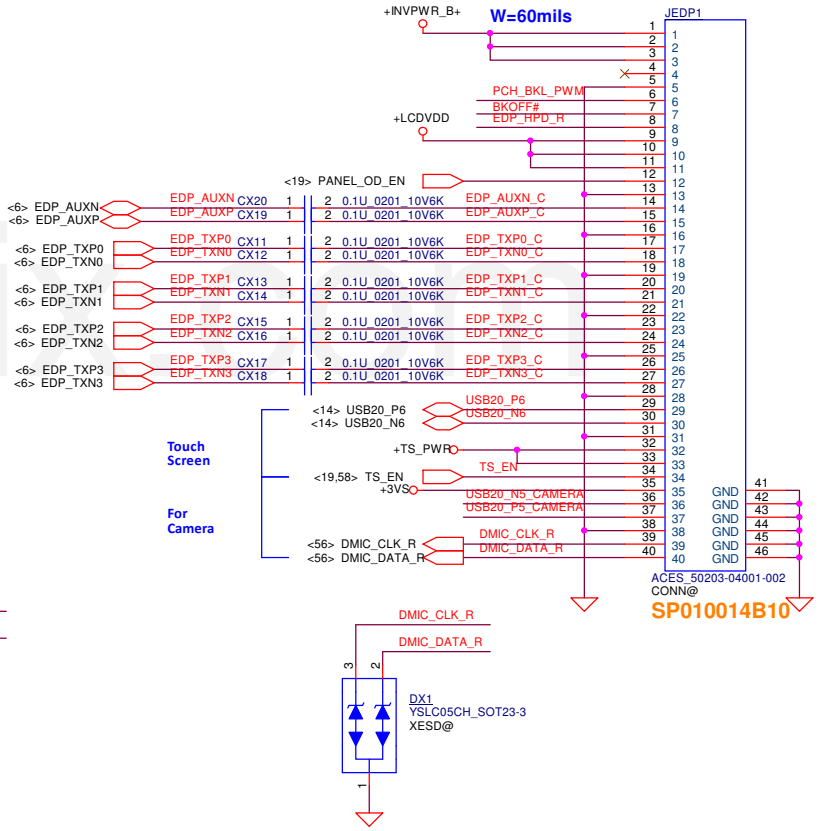
USB Touch Screen



Camera



LED PANEL Conn.



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

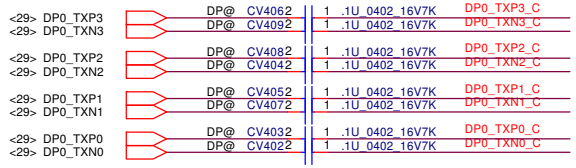
Compal Electronics, Inc.

Title: eDP CONN.

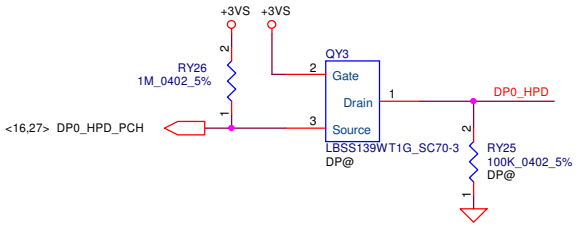
Size	Document Number	Rev
Custom	FH58F M/B LA-J251P	1.0

Date: Monday, August 12, 2019 Sheet 38 of 101

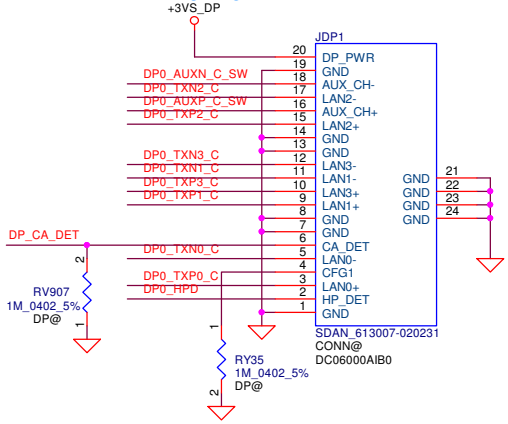
Display Port



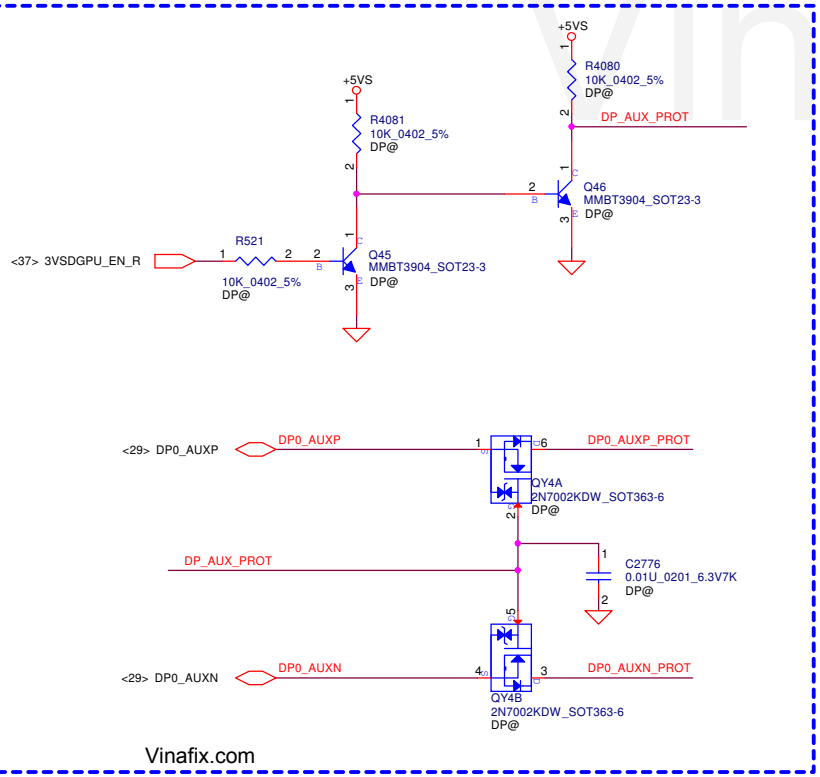
to PCH

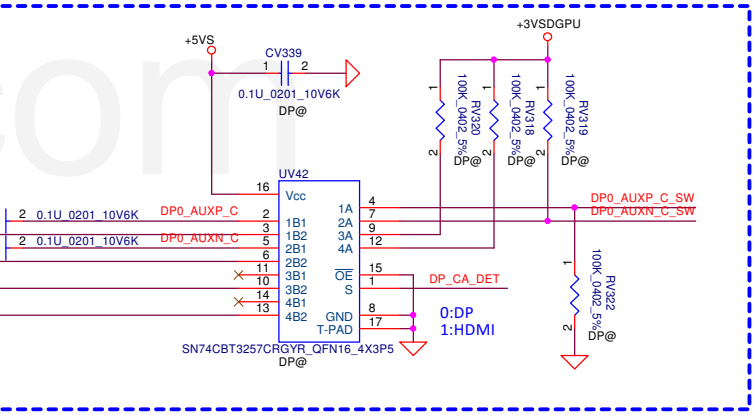


W=40mils

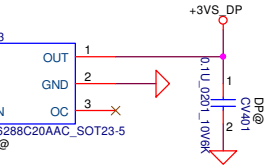


need check pin4 CFG1





W=40mils W=40mils



OE#	S	INPUT/OUTPUT A	Function
L	L	B1	A=B1
L	H	B2	A=B2
H	X	Z	NC

0921 change souce to +3VALW, CTRL to SUSP#

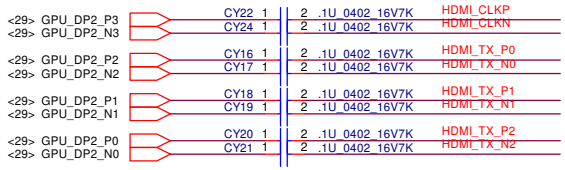
Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

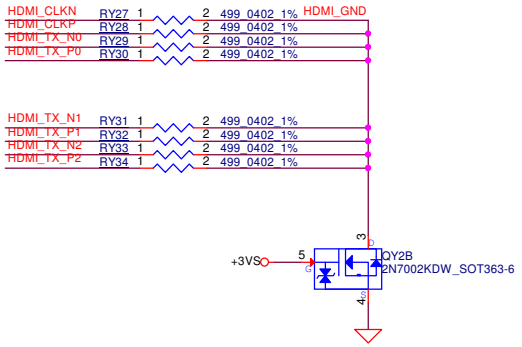
Compal Electronics, Inc.

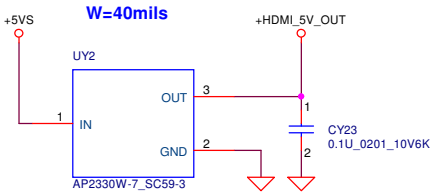
Title: DP CONN

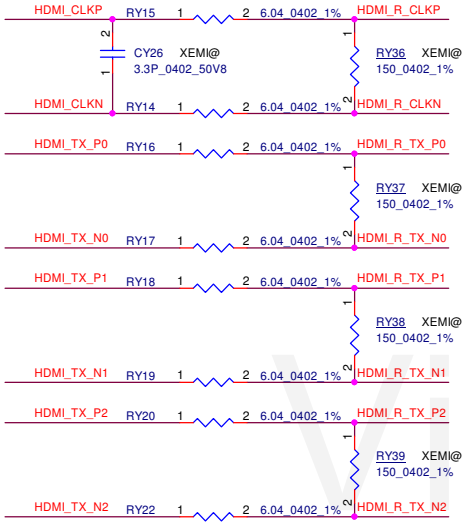
Size: Custom | Document Number: FH58F M/B LA-J251P | Rev: 1.0

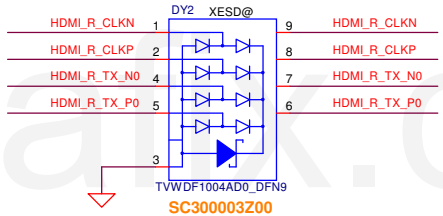
Date: Monday, August 12, 2019 | Sheet 39 of 100

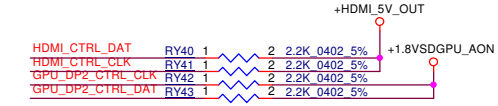


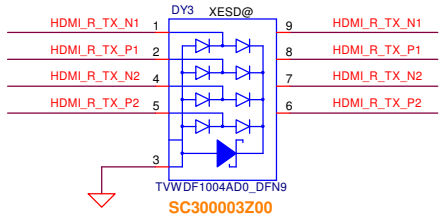


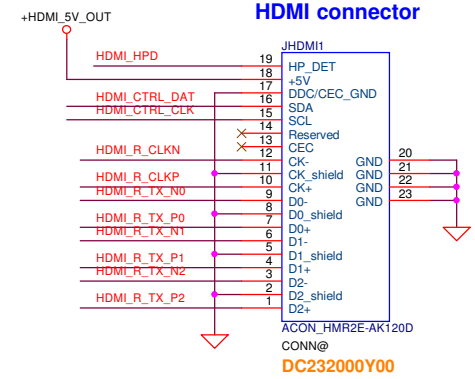


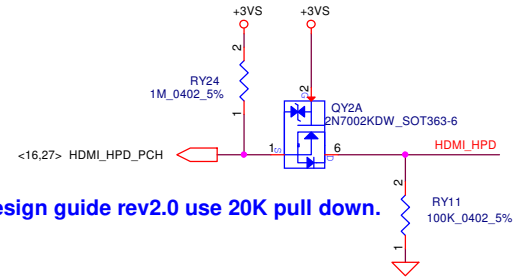


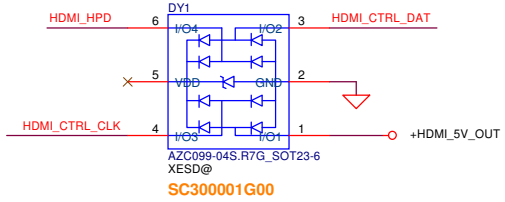


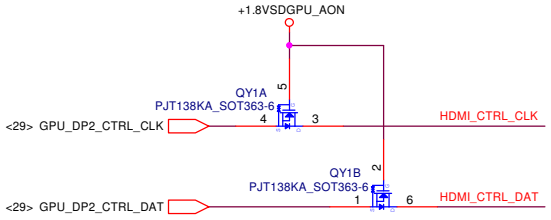












Vinafix.com

Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.

Title: HDMI CONN.

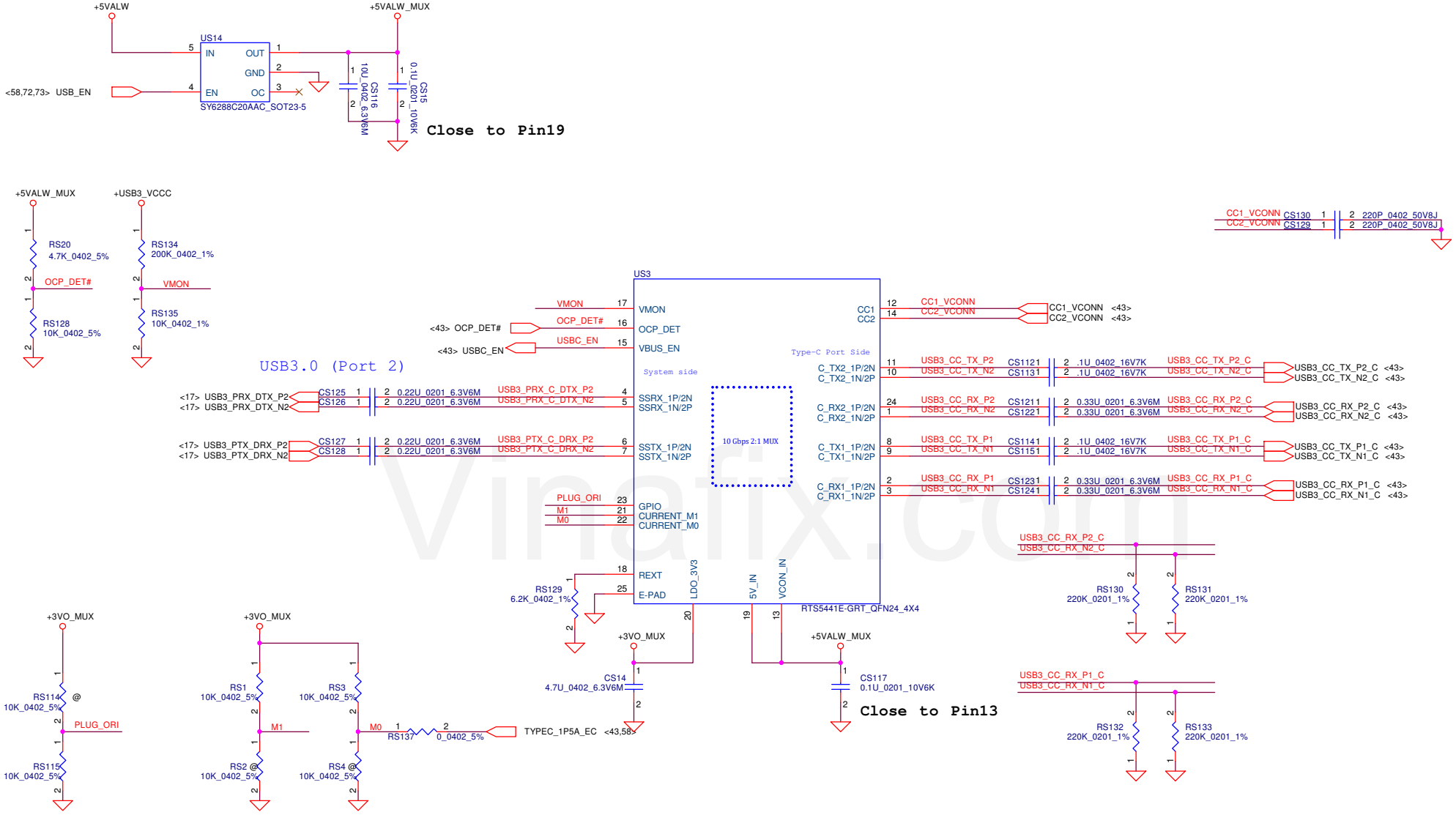
Size	Document Number	Rev
Custom	FH58F M/B LA-J251P	1.0

Date: Monday, August 12, 2019 Sheet 40 of 101

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 41 of 101	



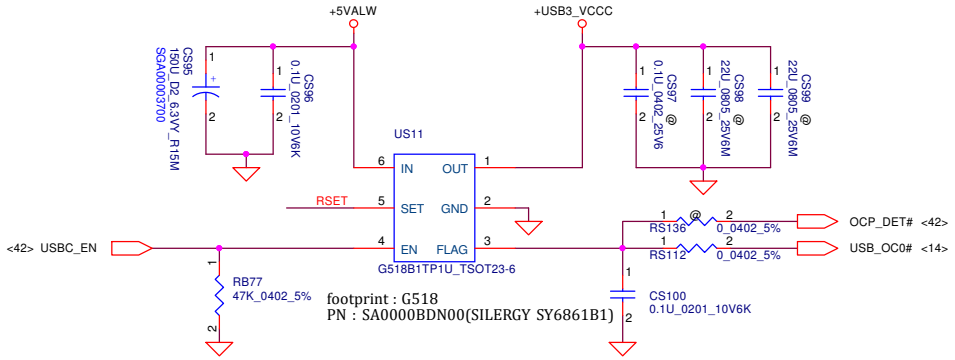
5441E Current Limit		
M1	M0	MODE
L	H	0.9A
H	L	1.5A
H	H	3A

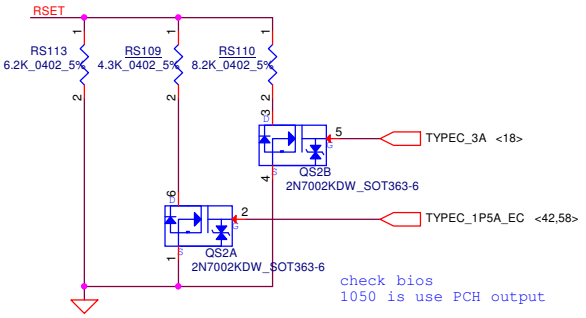
RTS5441 M0 truth table by 2018 BIOS spec			
TYPEC_1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery >30%
L	1.5A	1.92A	Battery <30% when DC mode

confirm realtek hand-shake

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

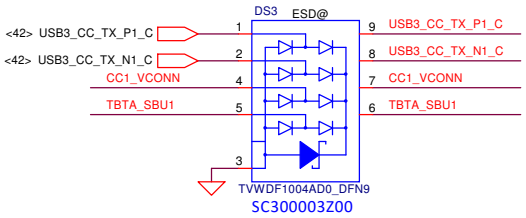
Compal Electronics, Inc.			
Title	CC+USB TYPE C		
Size: Custom	Document Number: FH58F M/B LA-J251P		Rev: 1.0
Date: Monday, August 12, 2019	Sheet 42 of 101		

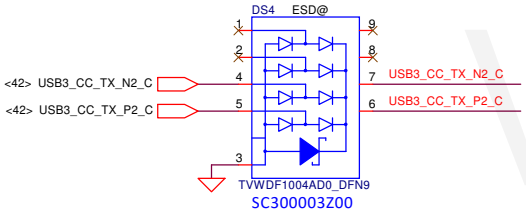


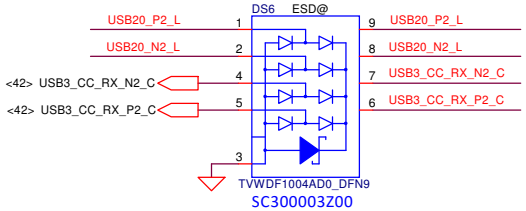


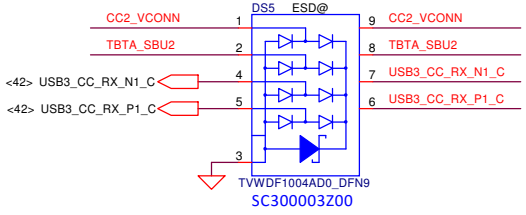
G518 MOS Current Limit				
GPP_B1 (TYPEC_1P5A)	GPP_B4 (TYPEC_3A)	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A

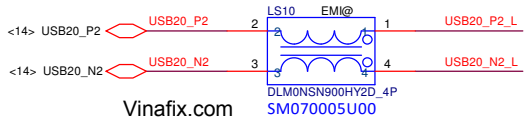
For ESD request

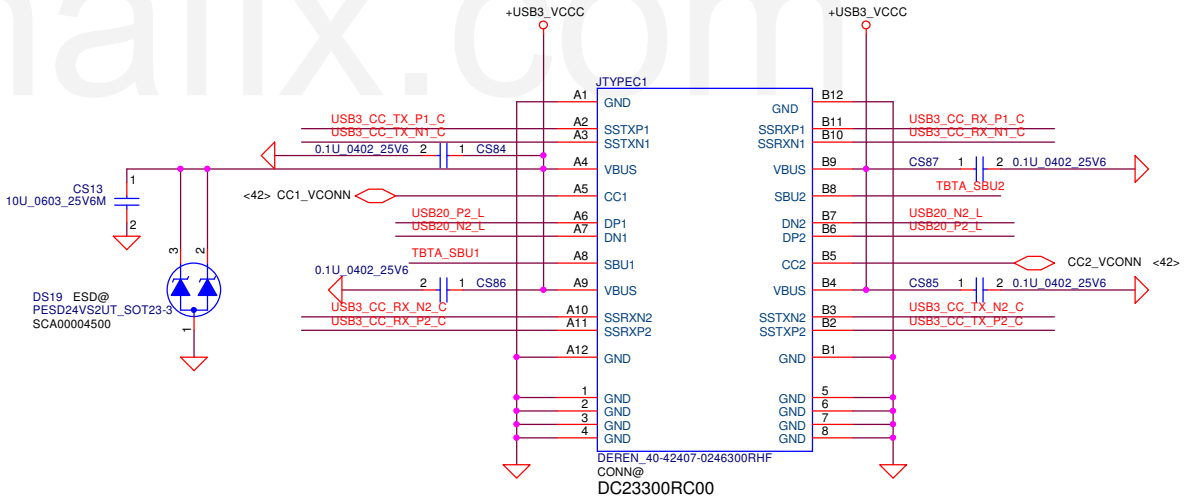












CC1_VCONN & CC2_VCONN need 20miil trace width.

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.

Title: **CC+USB TYPE C**

Size: Custom | Document Number: **FH58F M/B LA-J251P** | Rev: 1.0

Date: Monday, August 12, 2019 | Sheet 43 of 101

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 44 of 101	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 45 of 101	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 46 of 101	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 47 of 101	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 48 of 101	

Reserve Page

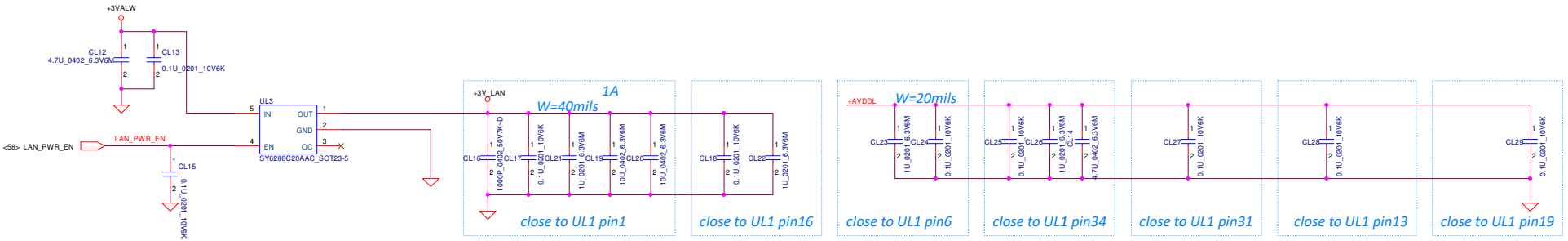
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

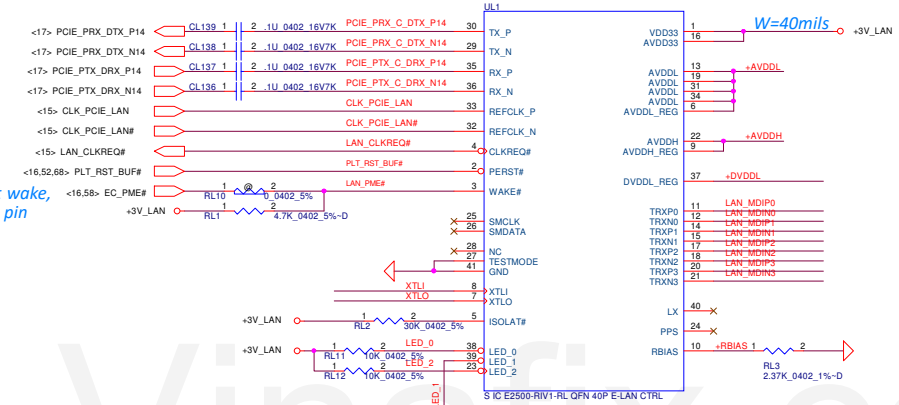
Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 49 of 101	

Reserve Page

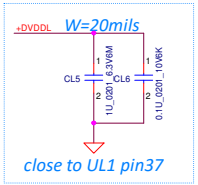
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

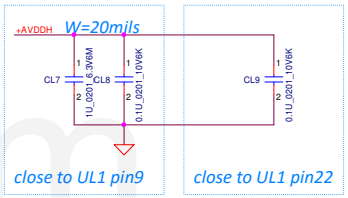
Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 50 of 101	

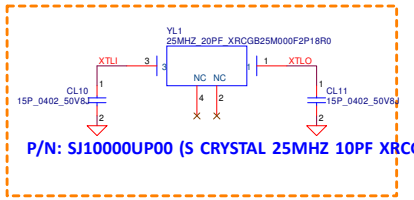




remind : if no support wake, don't monitor this pin







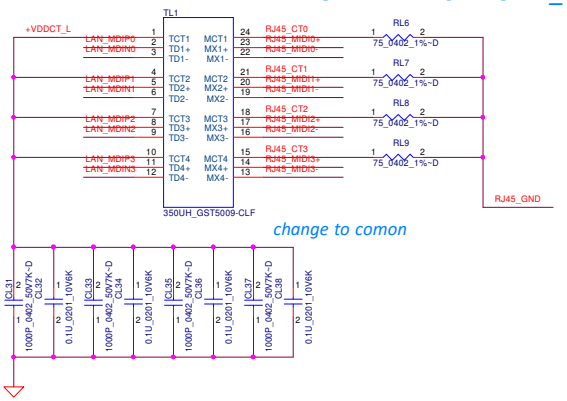
P/N: SJ10000UP00 (S CRYSTAL 25MHZ 10PF XRCGB25M000F2P34R0)

Table 2-2 Power-on strapping

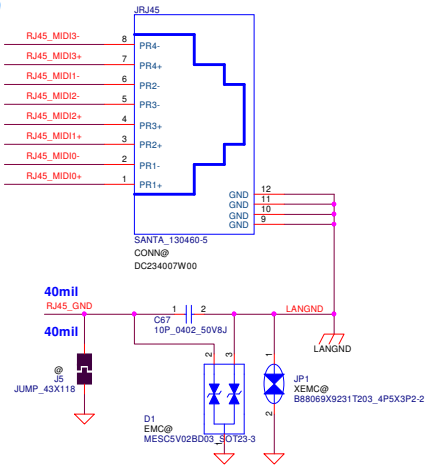
Pin	Configure signal		Description
LED[0]	Core voltage select	1	High core voltage
		0	Low core voltage
LED[1]	Regulator select	1	Switch mode regulator (SWR) select
		0	Linear regulator (LDO) select
LED[2]	External clock select	1	25 MHz external clock input
		0	48 MHz external clock input

check need power or not? 3/15

TIMAG: S X'FORM_ IH-160 LAN,SP050006F00
BOTHHAND: S X'FORM_ GST5009-E LF LAN,SP050006B10



LAN Connector



Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

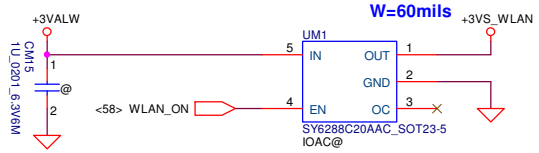
Compal Electronics, Inc.

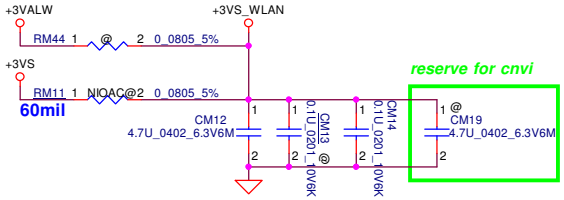
Title: LAN E2400

Size: | Document Number: FH58F M/B LA-J251P | Rev: 1.0

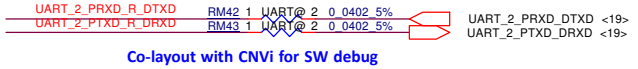
Date: Monday, August 12, 2019 | Sheet 51 of 100

Wireless LAN



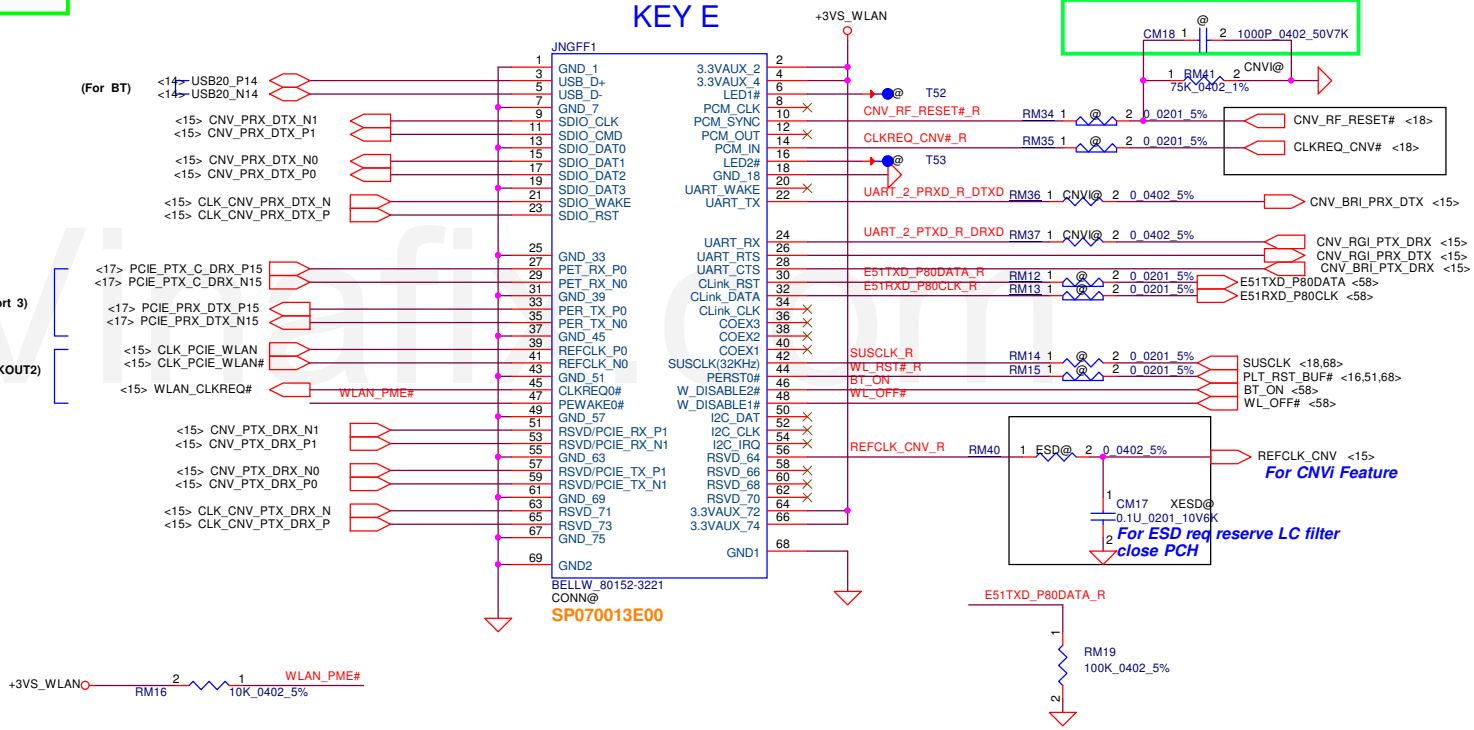


Vinafix

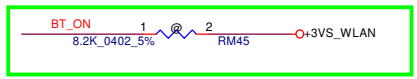


NGFF WL+BT (KEY E)

KEY E



reserve for BT_ON OD pull high (1.0)



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.			
Title: M.2 Key E (WLAN)			
Size: Custom	Document Number: FH58F M/B LA-J251P		Rev: 1.0
Date: Monday, August 12, 2019	Sheet 52 of 101		

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 53 of 101	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

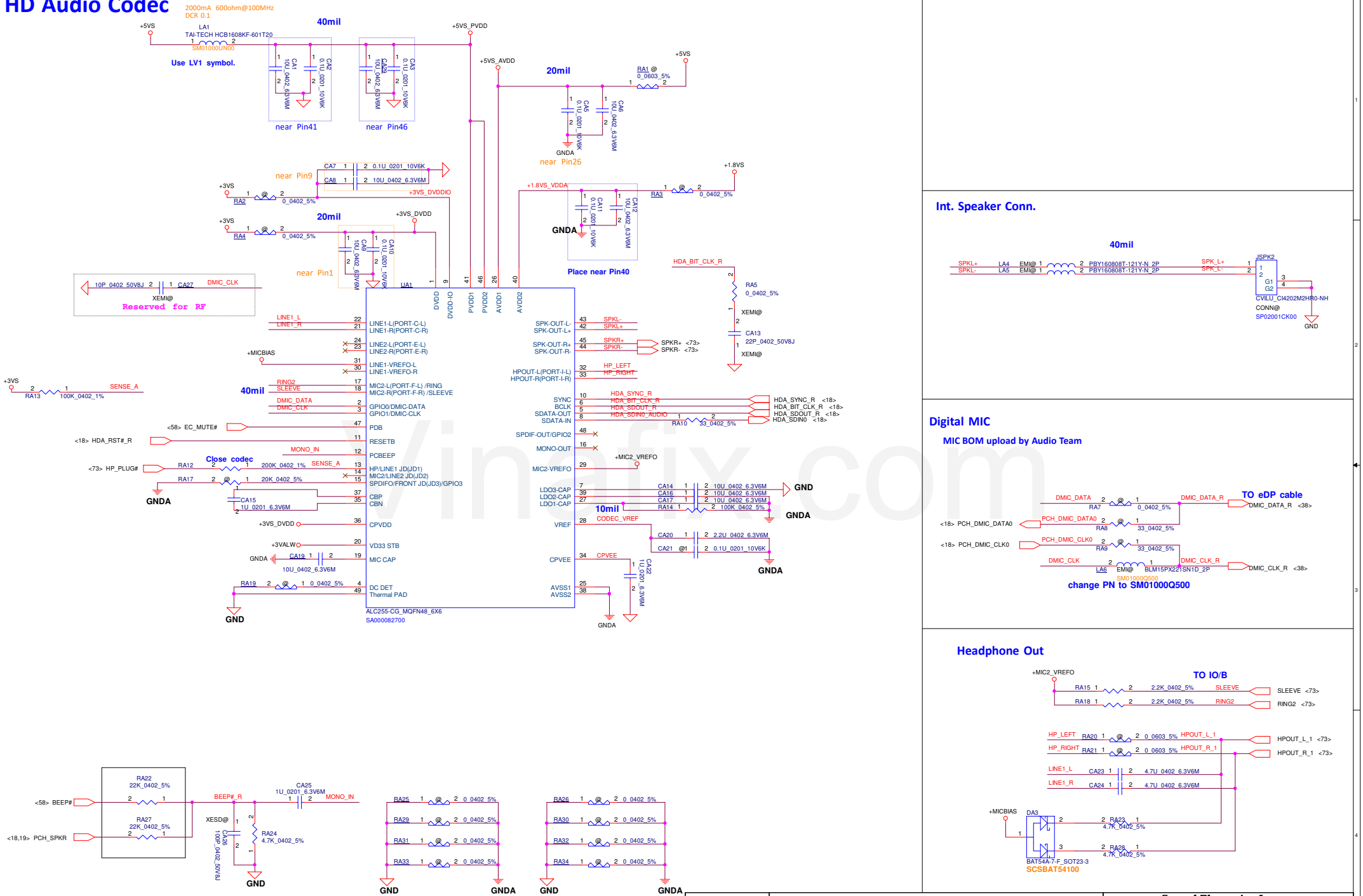
Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 54 of 101	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 55 of 101	

HD Audio Codec



Int. Speaker Conn.

Digital MIC

MIC BOM upload by Audio Team

Headphone Out

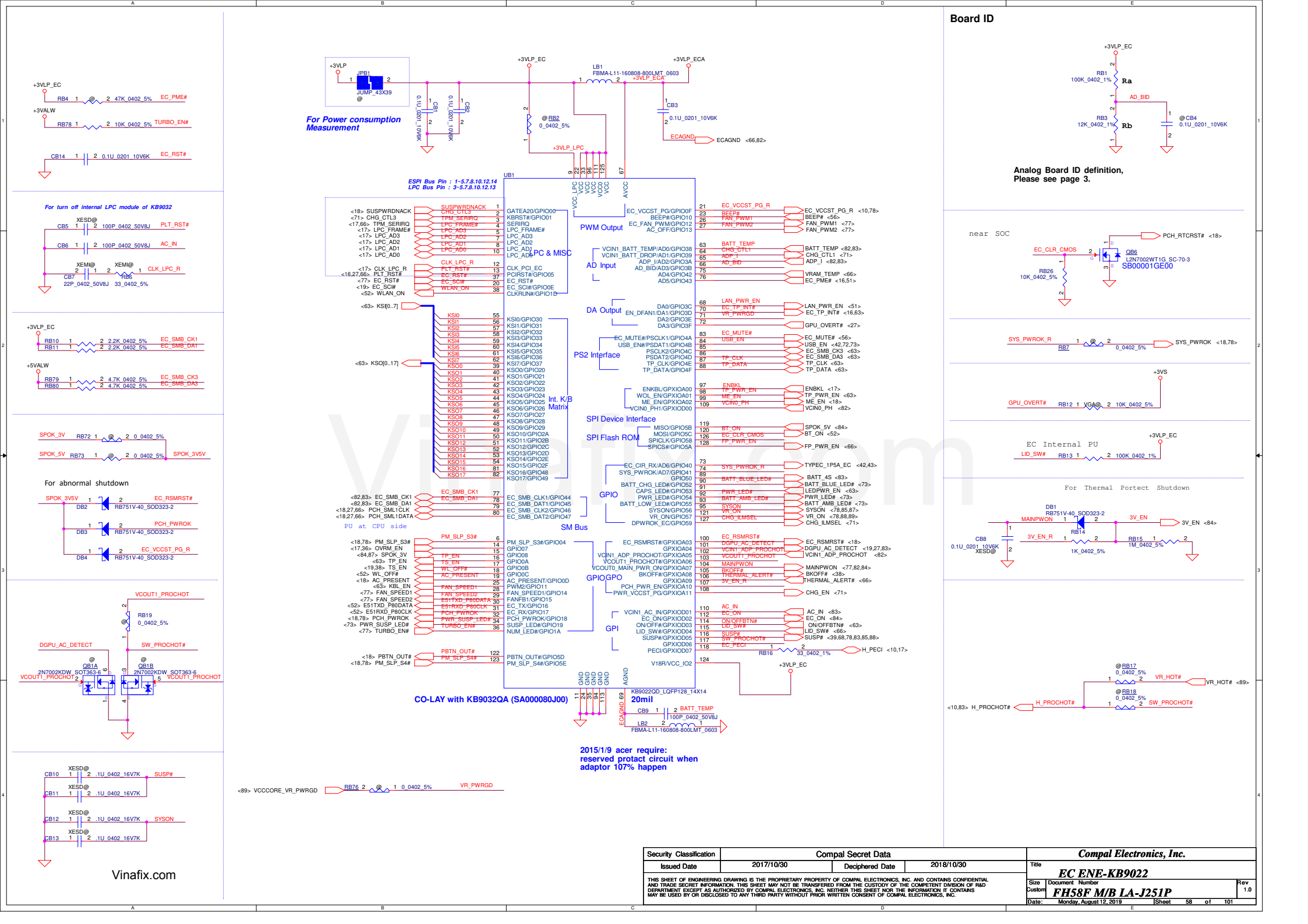
Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.			
Title	HD Audio Codec ALC255		
Size	Document Number		Rev
Custom	FH58F M/B LA-J251P		1.0
Date:	Monday, August 12, 2019	Sheet	56 of 101

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 57 of 101	



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: **EC ENE-KB9022**

Size: Custom | Document Number: **FH58F M/B LA-J251P** | Rev: 1.0

Date: Monday, August 12, 2019 | Sheet 58 of 101

Reserve Page

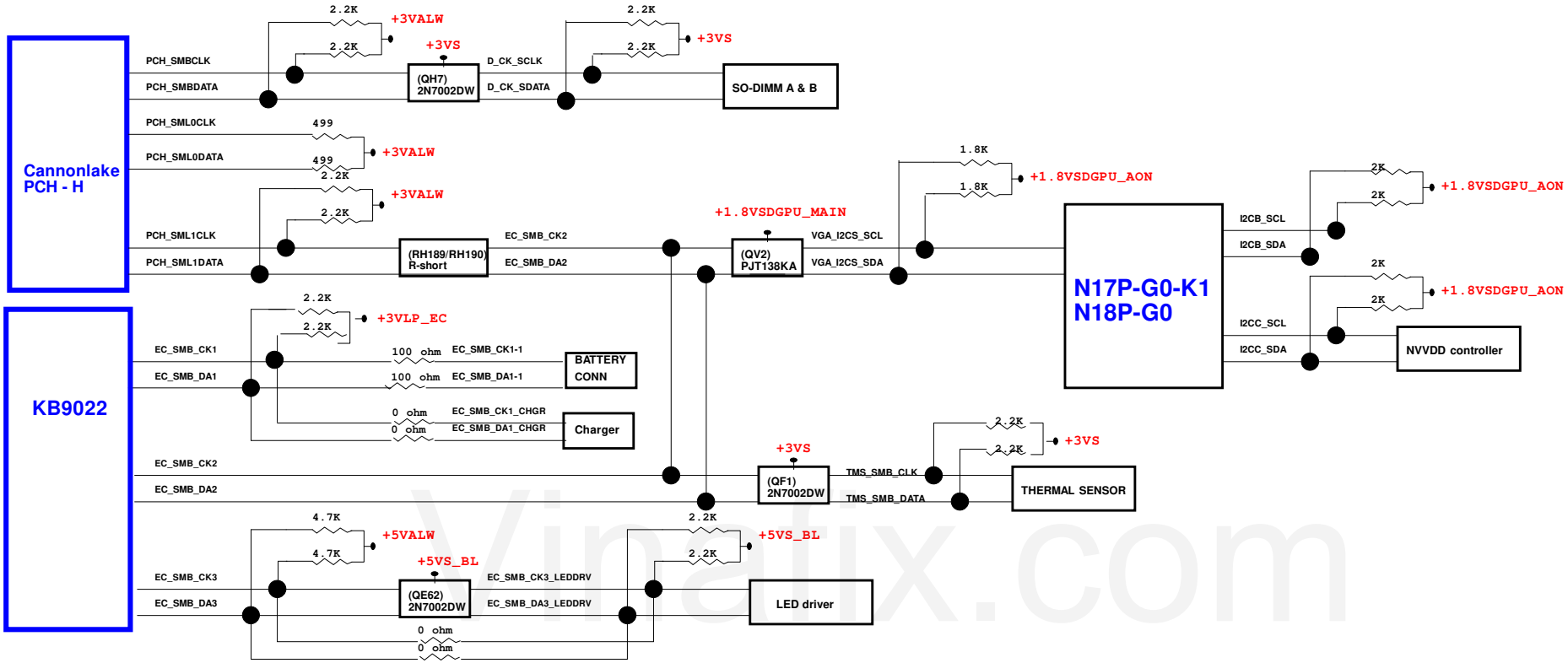
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 59 of 101	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 60 of 101	



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

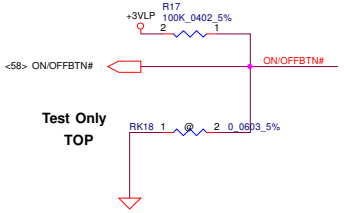
Compal Electronics, Inc.			
Title	N17E-GDDR5_D		
Size	Document Number	FH58F M/B LA-J251P	Rev 1.0
Date: Monday, August 12, 2019	Sheet 61 of 101		

Reserve Page

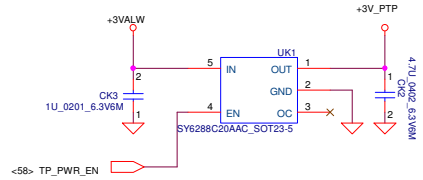
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 62 of 101	

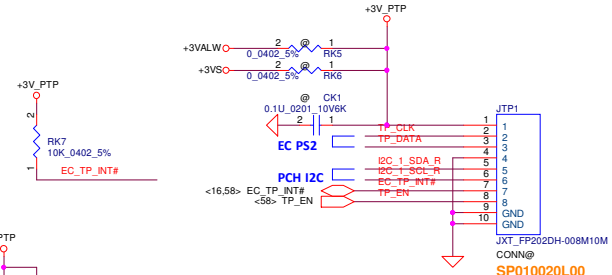
ON/OFF BTN

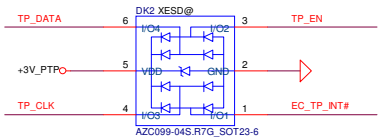


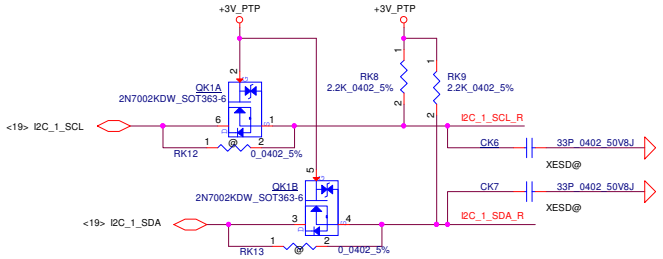
Touch Pad

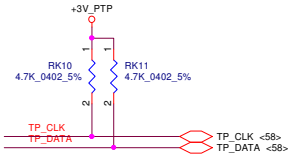


TP_PWR_EN follow SYSON behavior

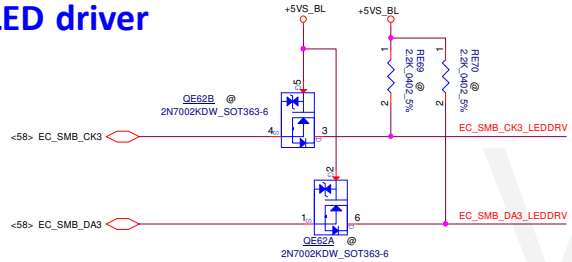


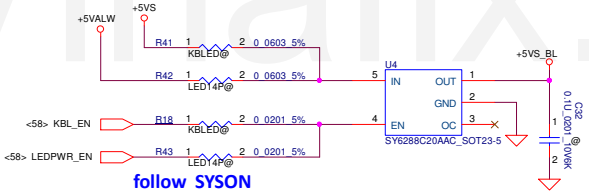






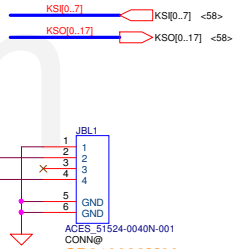
LED driver

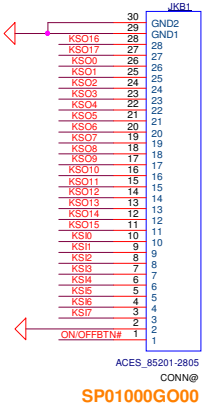


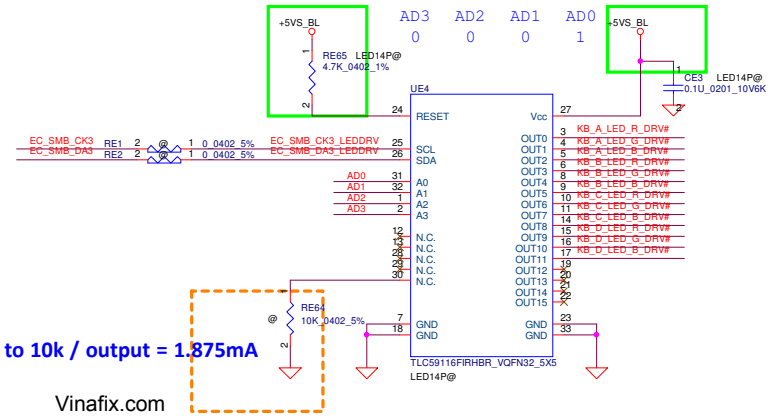


follow SYSON

KB Conn. / Backlight



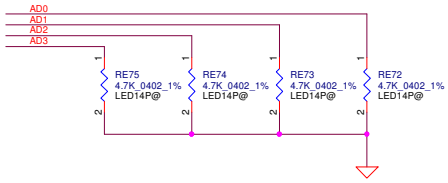


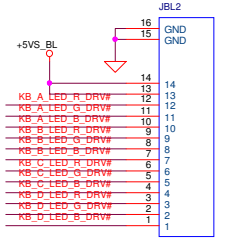


set RE7 to 10k / output = 1.875mA

Vinafix.com

Raptor: NC for 59116F





Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.	
Title	KB & TP & TPM Connector
Size / Custom	Document Number: FH58F M/B LA-J251P
Rev	1.0
Date: Monday, August 12, 2019	Sheet 63 of 101

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

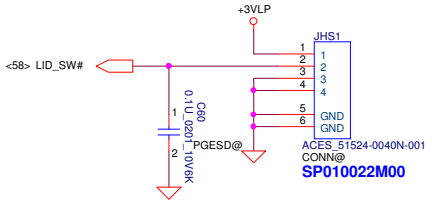
Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 64 of 101	

Reserve Page

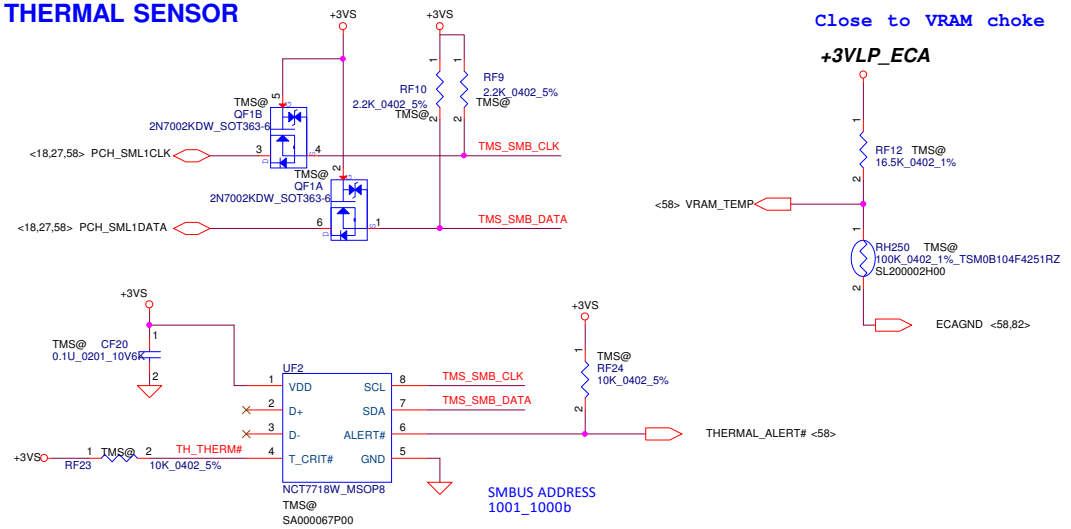
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 65 of 101	

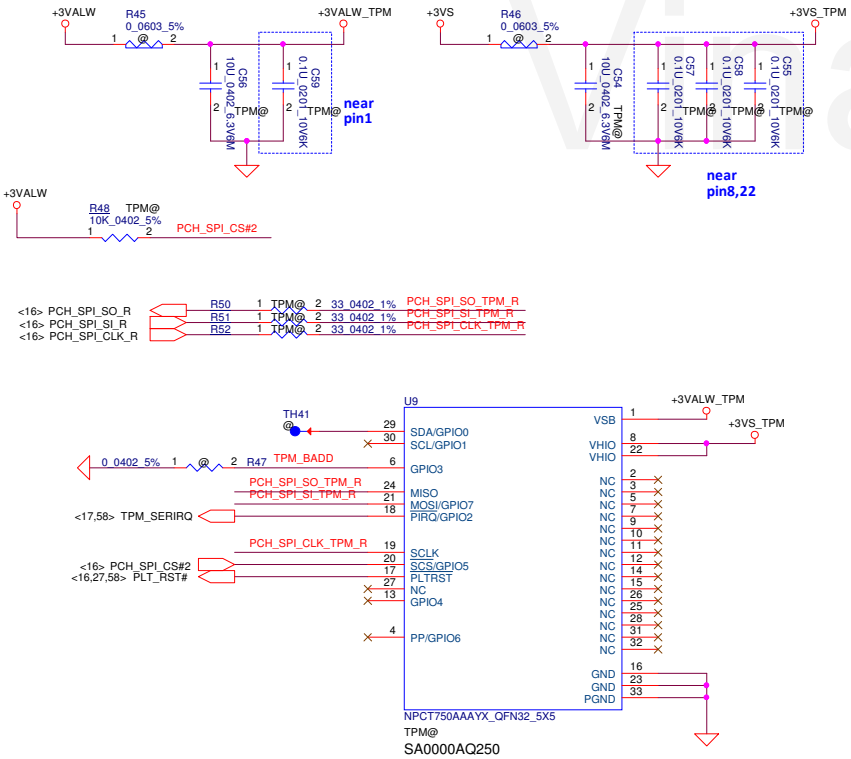
To Hall sensor/B



THERMAL SENSOR



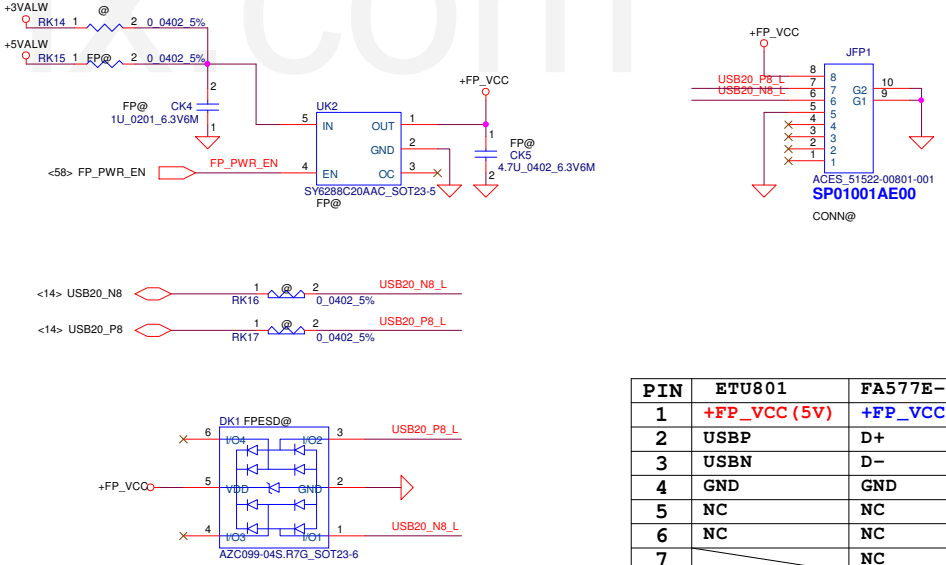
TPM



Vinafix.com

SA0000AQ250, S IC NPCT750AABYX QFN 32P TPM

Finger Print

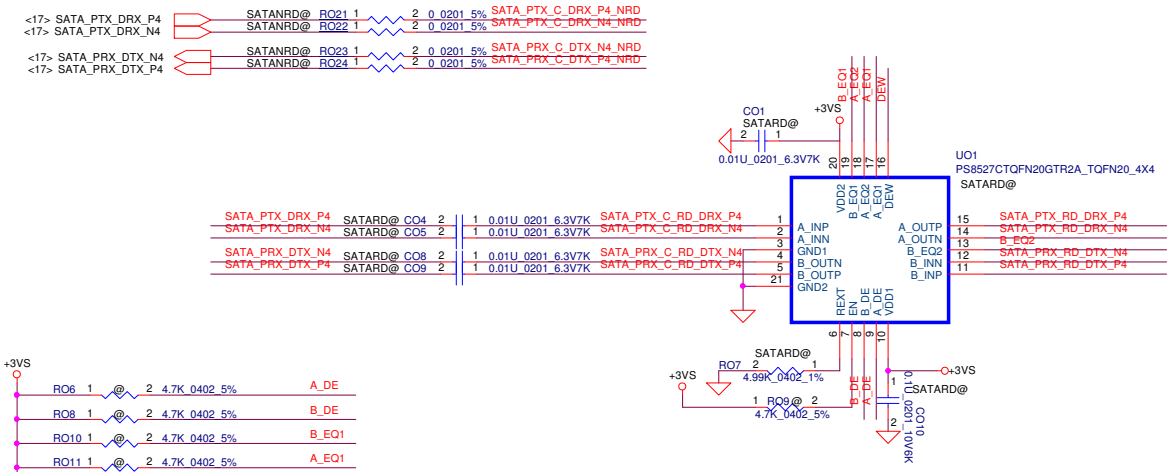


PIN	ETU801	FA577E-1200
1	+FP_VCC(5V)	+FP_VCC(3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC

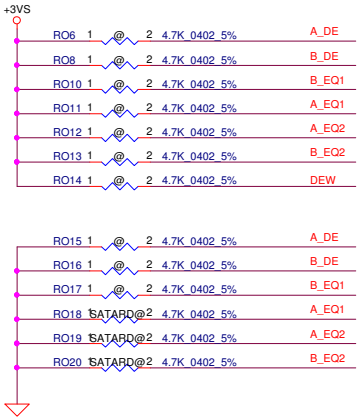
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.	
Title	Sensors/FP/TPM
Size	Document Number: FH58F M/B LA-J251P
Rev	1.0
Date:	Monday, August 12, 2019
Sheet	66 of 101

SATA Re-Driver and cable HDD Conn.



USE 8527 re-driver
SA00007JU10



Chip Enable. Internally pulled up at ~150KΩ

EN	Status
L	Chip disabled
H	Chip enabled(default)

Programmable output de-emphasis level setting for channel A.
Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.
Internally tied to VDD/2(M status).

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

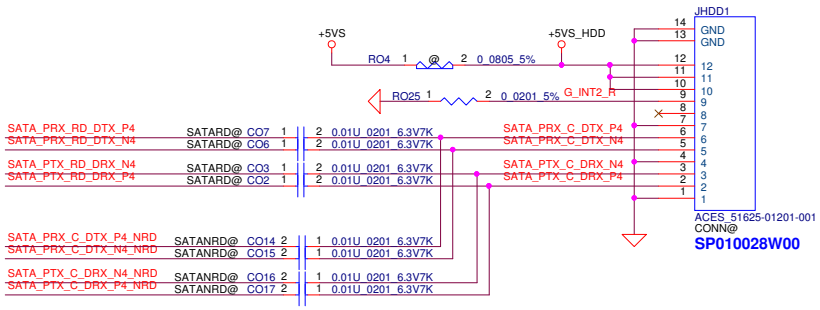
Equalizer control and program for channel A.
Internally tied to VDD/2 (M status).

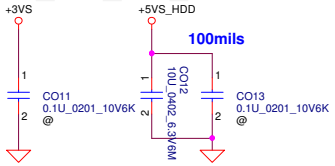
A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Equalizer control and program for channel B.
Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

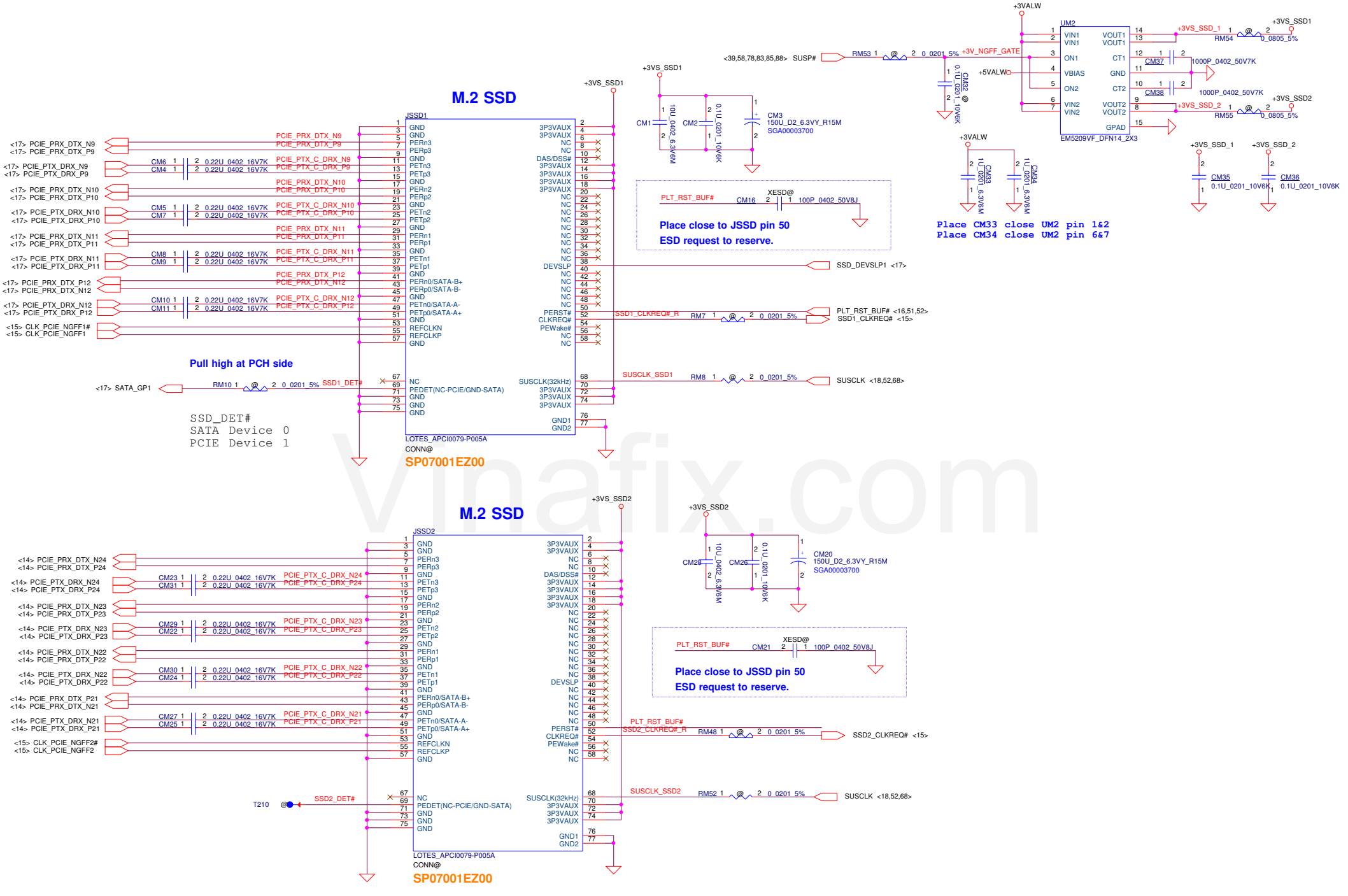
FFC Type





Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.	
Title	HDD/ Re-Driver/ G-sensor
Size: Custom	Document Number: FH58F M/B LA-J251P
Rev	1.0
Date: Monday, August 12, 2019	Sheet 67 of 101



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.			
Title	SATA/PCIE-SSD		
Size: Custom	Document Number: FH58F M/B LA-J251P		Rev: 1.0
Date: Monday, August 12, 2019	Sheet 68 of 101		

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

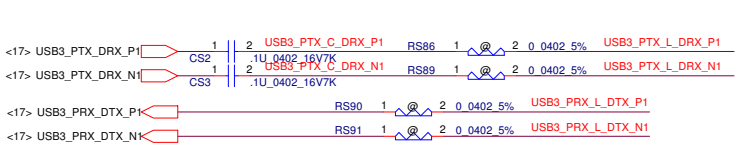
Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 69 of 101	

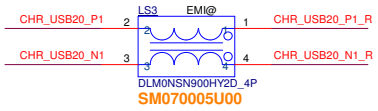
Reserve Page

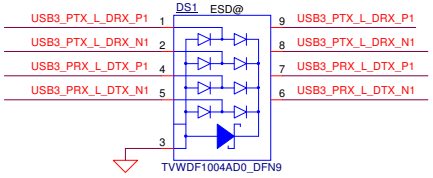
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

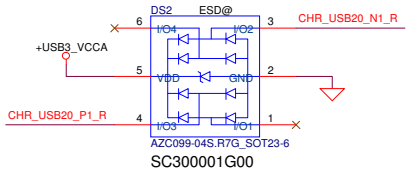
Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 70 of 101	

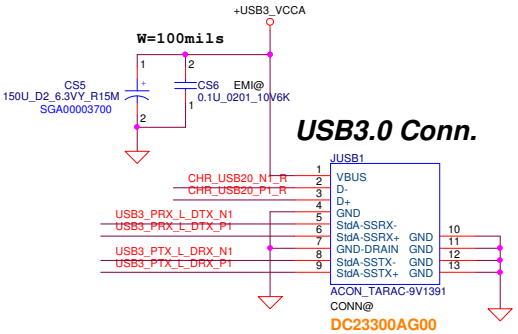
USB3.0



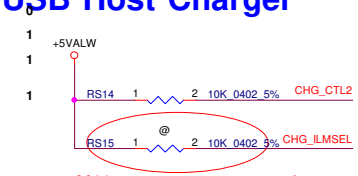




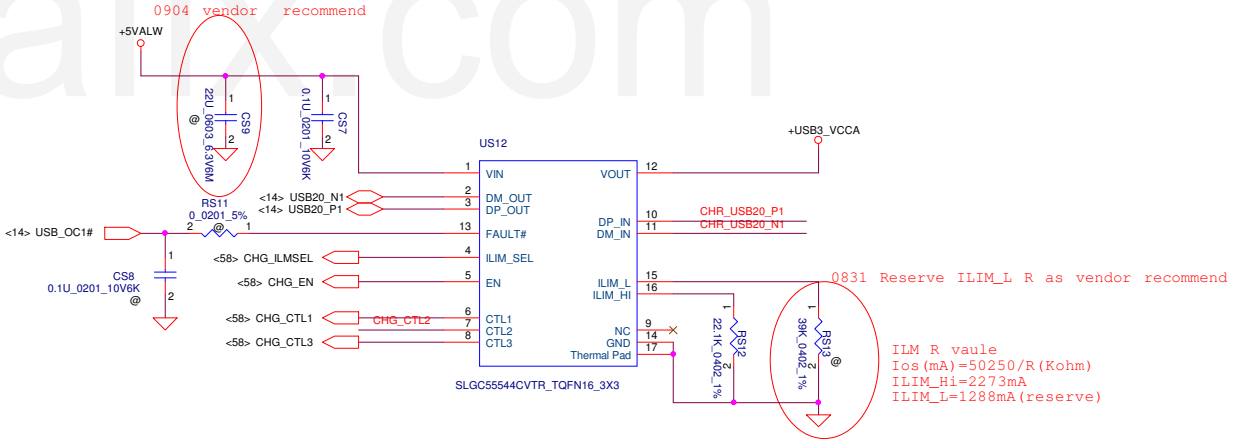




USB Host Charger



0911 Rerserve PU, vendor suggest to EC control if future need support SDP2



USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
	1	1	1	1	CDP	ILIM_H	Data Lines Connected

Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

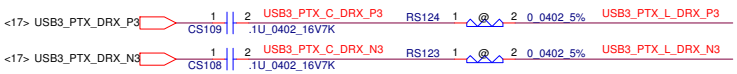
Compal Electronics, Inc.

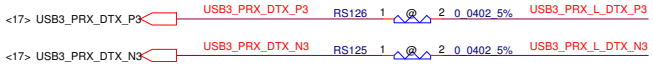
Title: USB3.0 Conn/USB Charger

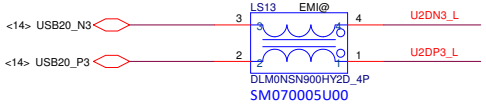
Size: Custom | Document Number: FH58F M/B LA-J251P | Rev: 1.0

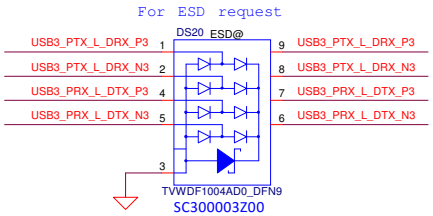
Date: Monday, August 12, 2019 | Sheet 71 of 101

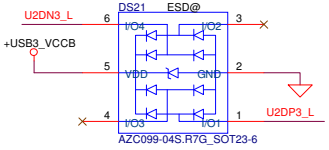
USB3.0

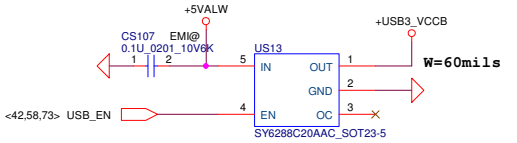


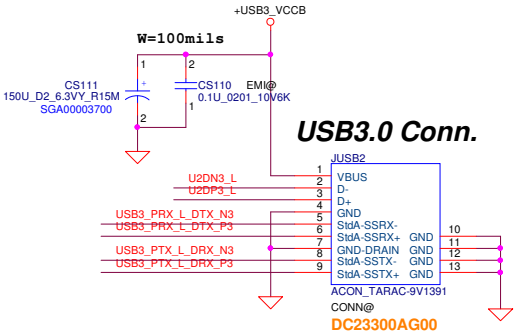








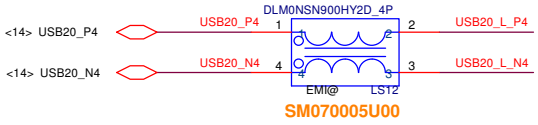


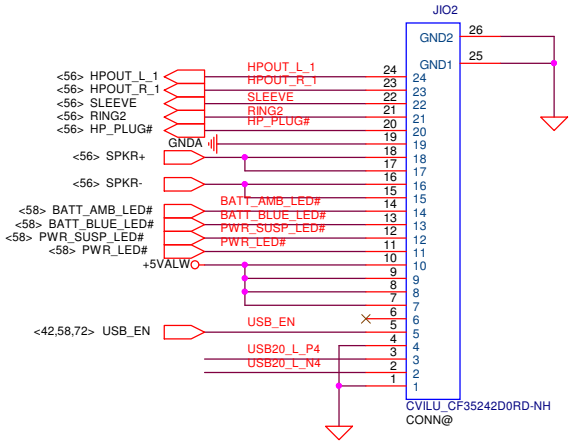


Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.	
Title	N18E-GDDR6_D
Size	Document Number: FH58F M/B LA-J251P
Rev	1.0
Date:	Monday, August 12, 2019
Sheet	72 of 101

IO/B CONN





Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.

Title: *IO/B*

Size: Custom | Document Number: *FH58F M/B LA-J251P* | Rev: 1.0

Date: Monday, August 12, 2019 | Sheet 73 of 101

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 74 of 101	

Reserve Page

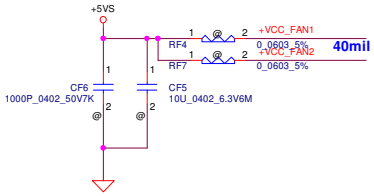
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 75 of 101	

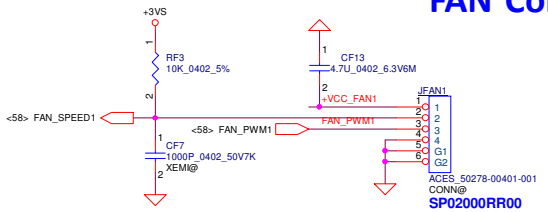
Reserve Page

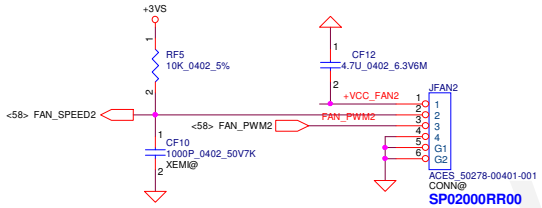
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 76 of 101	

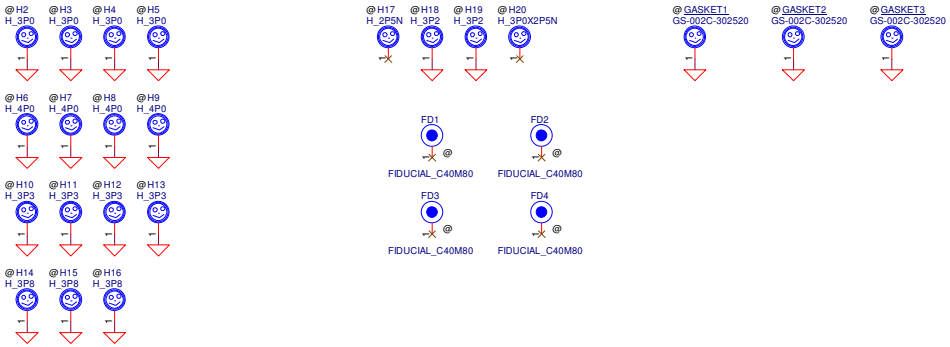


FAN Conn

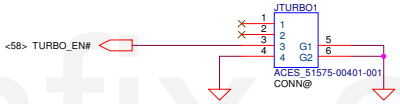




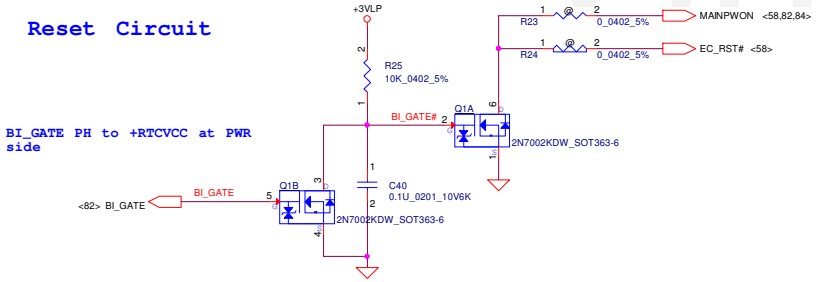
Screw Hole



Turbo Key

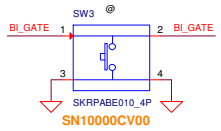


Reset Circuit



BI_GATE PH to +RTCVCC at PWR side

Reset Button



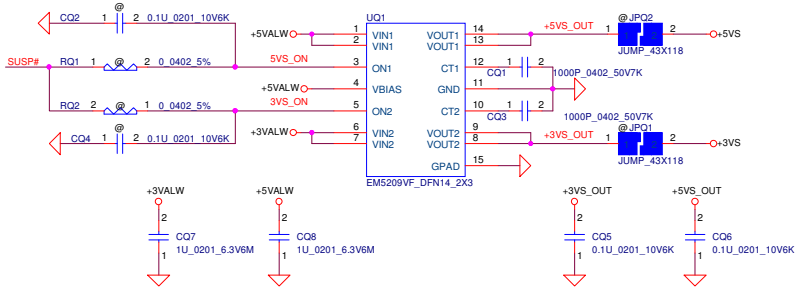
SN10000CV00

change PN to SN10000CV00

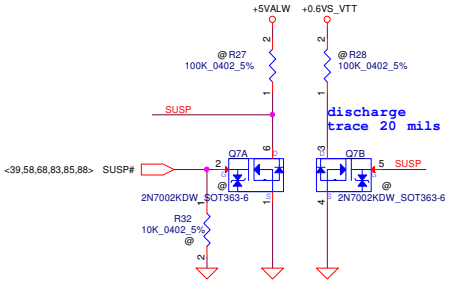
Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

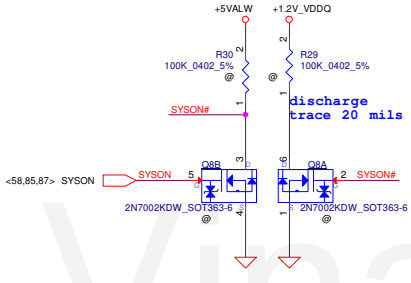
Compal Electronics, Inc.			
Title: FAN & Screw Hole			
Size: Custom	Document Number: FH58F M/B LA-J251P		Rev: 1.0
Date: Monday, August 12, 2019	Sheet 77 of 101		

System DC inferface

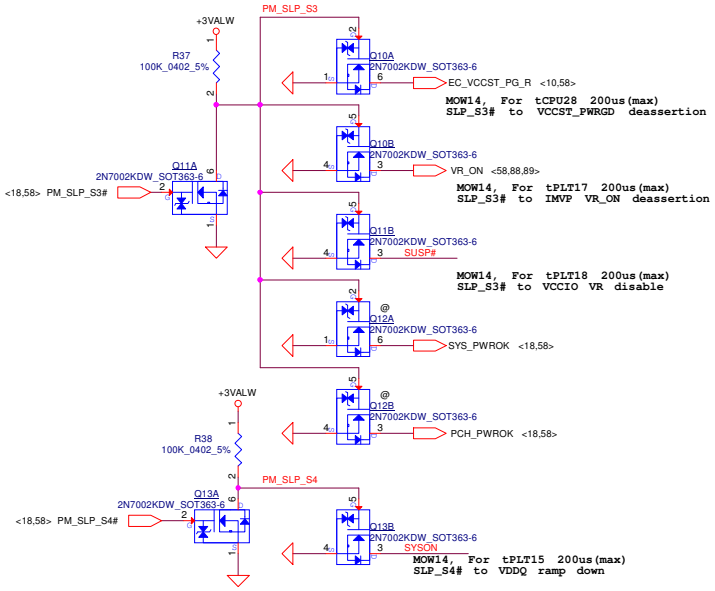


Place CQ7 close UQ1 pin 1&2
Place CQ8 close UQ1 pin 6&7



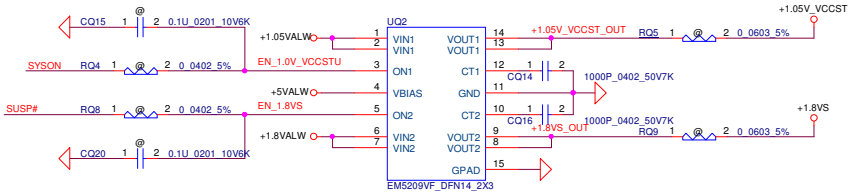


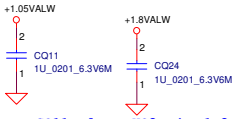
For Power ON/Off Sequence

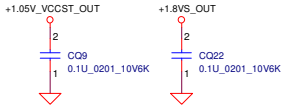


P/N: SB00000EO00 footprint use SB00000ZU00

+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS

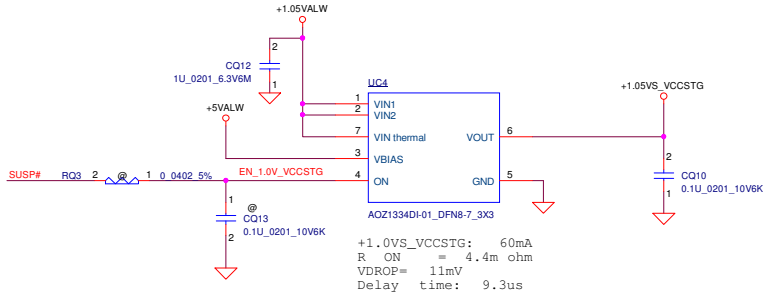






Place CQ11 close UQ2 pin 1&2
Place CQ24 close UQ2 pin 6&7

+1.05VALW TO +1.05VS_VCCSTG



+1.0VS_VCCSTG: 60mA
R ON = 4.4m ohm
VDROP= 11mV
Delay time: 9.3us

Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	FH58F M/B LA-J251P	1.0

Date: Monday, August 12, 2019 Sheet 78 of 101

Reserve Page

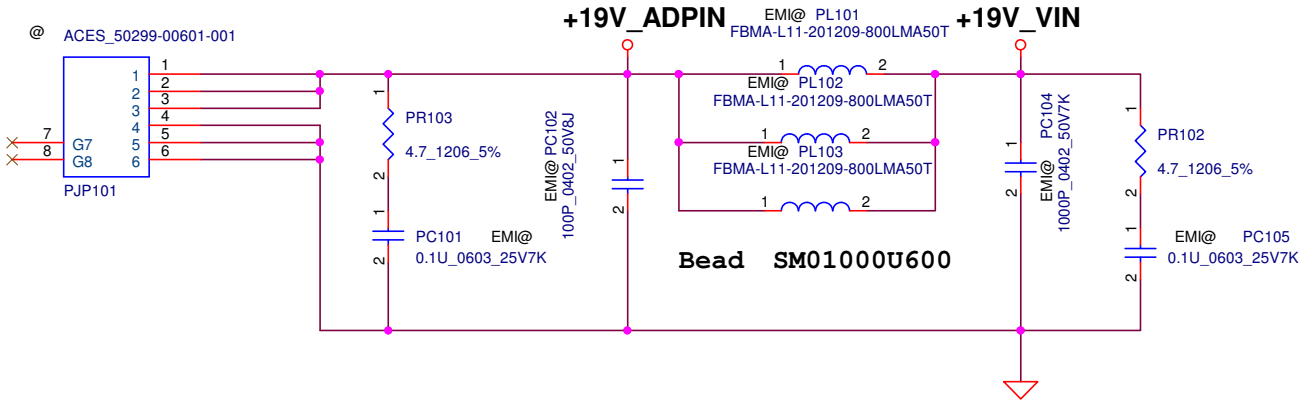
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

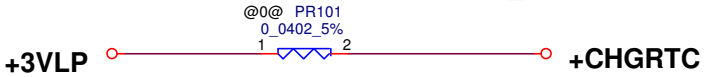
Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 79 of 101	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title	*N18E-GDDR6_D*	
Size	Document Number *FH58F M/B LA-J251P*	Rev 1.0
Date: Monday, August 12, 2019	Sheet 80 of 101	





Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

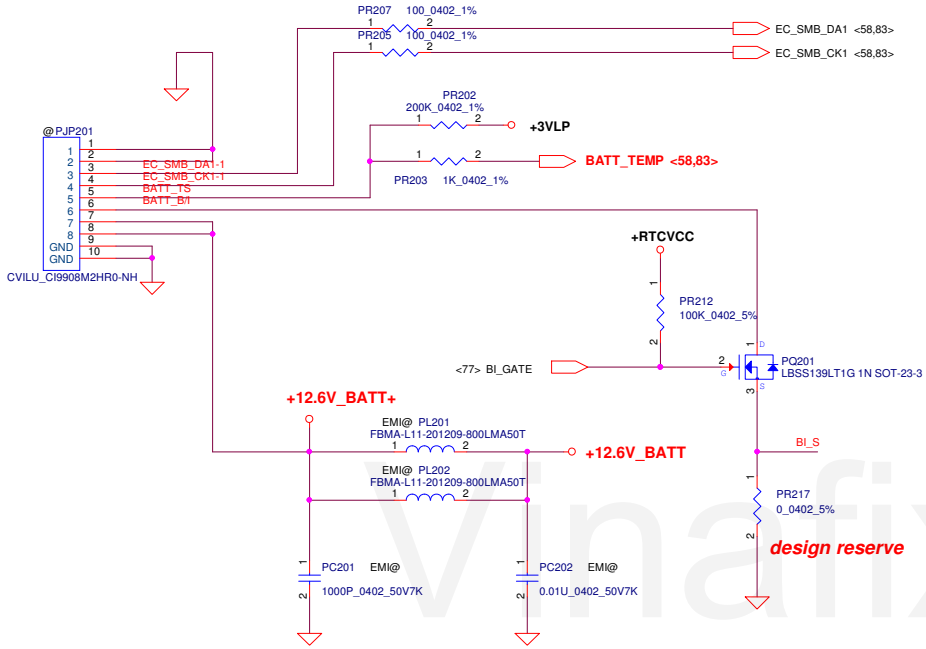
Title: DCIN

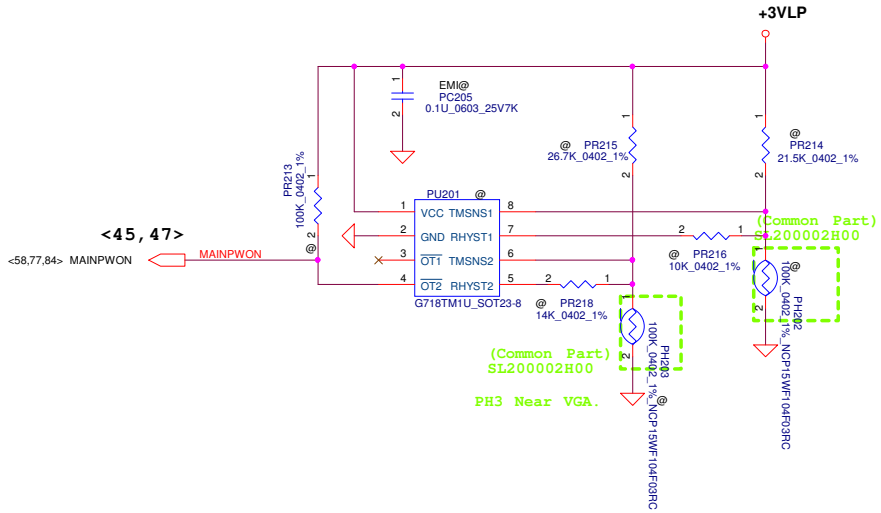
Size: Custom | Document Number: FH58F M/B LA-J251P | Rev: 1.0

Date: Monday, August 12, 2019 | Sheet 81 of 100

Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TEMP
PIN6 BI
PIN7 Batt+
PIN8 Batt+

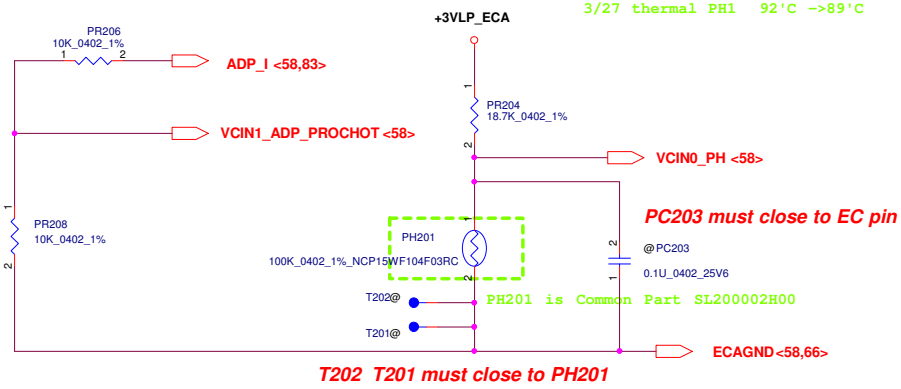




When PR204=18.7K

For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	89'C, 1V	56'C, 2V
PH202(ohm)	8.0524K	26.11K

3/27 thermal PH1 92'C ->89'C




```
ADP_I=20*I(adapter)*0.01
I(adapter)=adapter(W)*130%/19
```

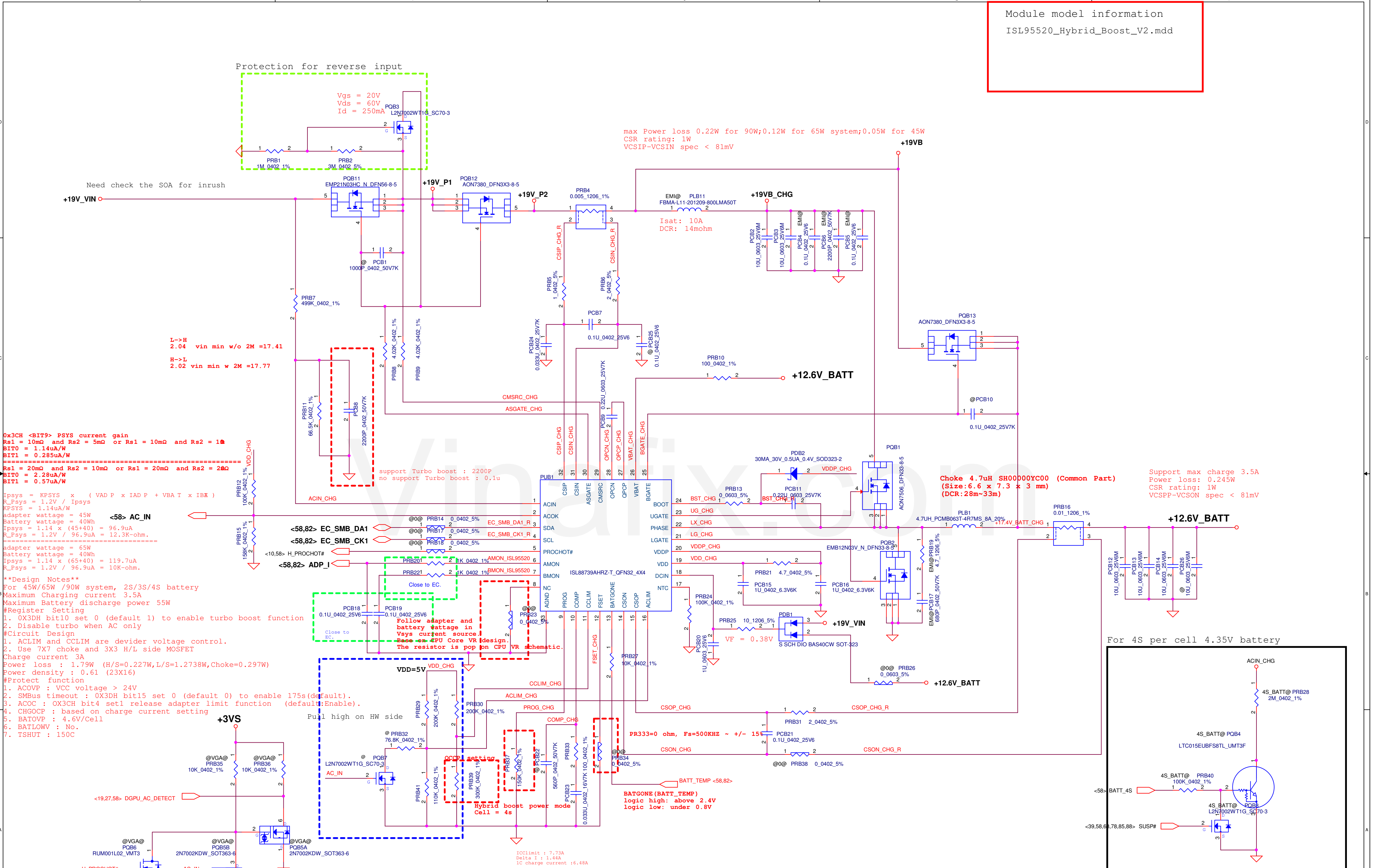

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: **BATTERY CONN/OTP**

Size: Custom | Document Number: **FH58F M/B LA-J251P** | Rev: 1.0

Date: Monday, August 12, 2019 | Sheet 82 of 100



ICClimit : 7.73A
Delta I : 1.44A
1C charge current :6.48A

Battery current limimed by CCLIm ~ 3.89A.
Adapter current limimed by ACLIm ~ 4.33A.
(PR779 and PQ741 are for change ACLIm when AC in)

(Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 20mΩ and Rs2 = 10mΩ).
CC_LIM = VccLIM / 64 x Rs2
==
(Rs1 = 10mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ)
CC_LIM = VccLIM / 32 x Rs2
==
AC_LIM = Vac_LIM / 32 x Rs1

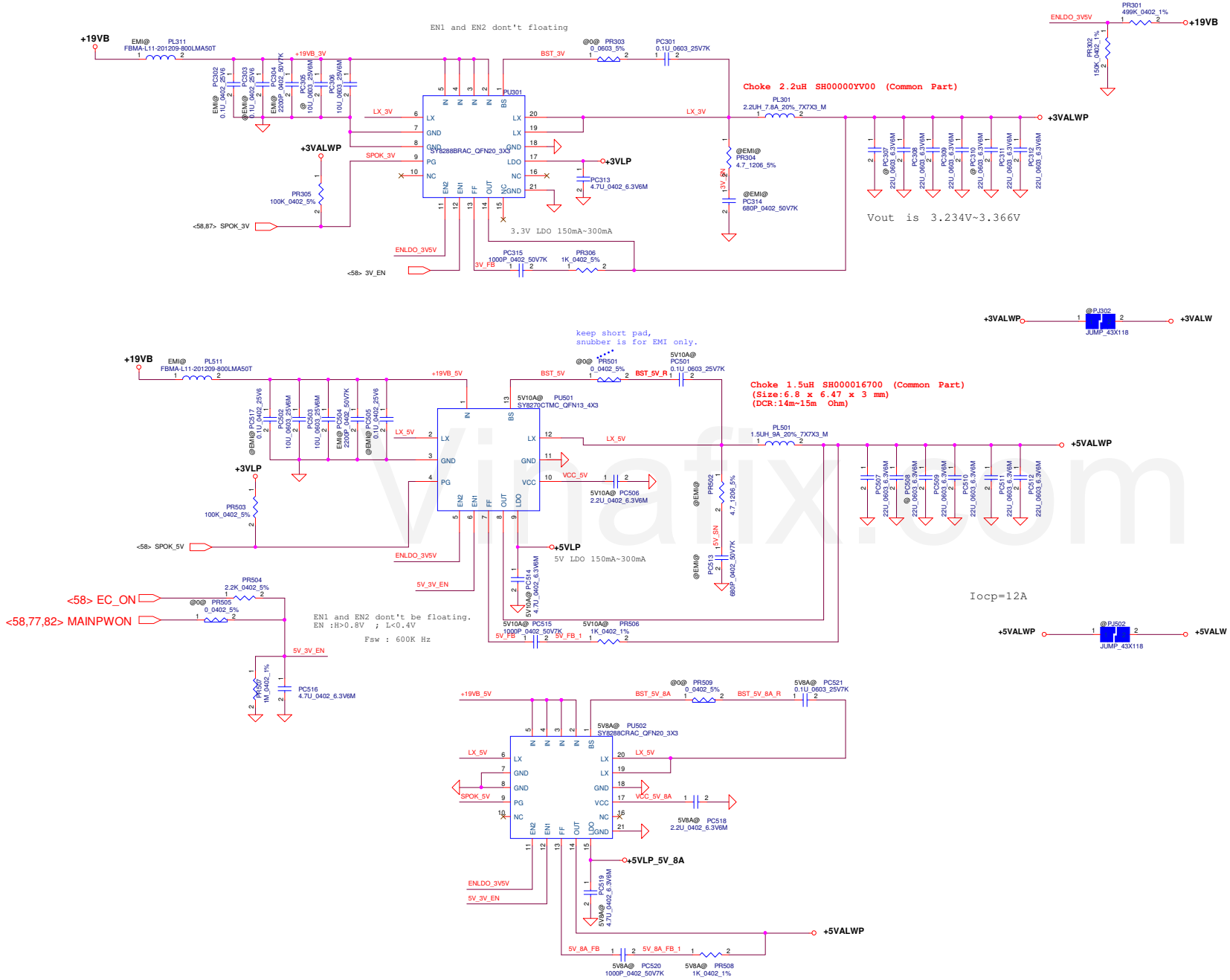
Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

Compal Electronics, Inc.

Title: **PWR_CHARGER**

Size | Document Number | Rev 1.0

Date: Monday, August 12, 2019 | Sheet 83 of 100



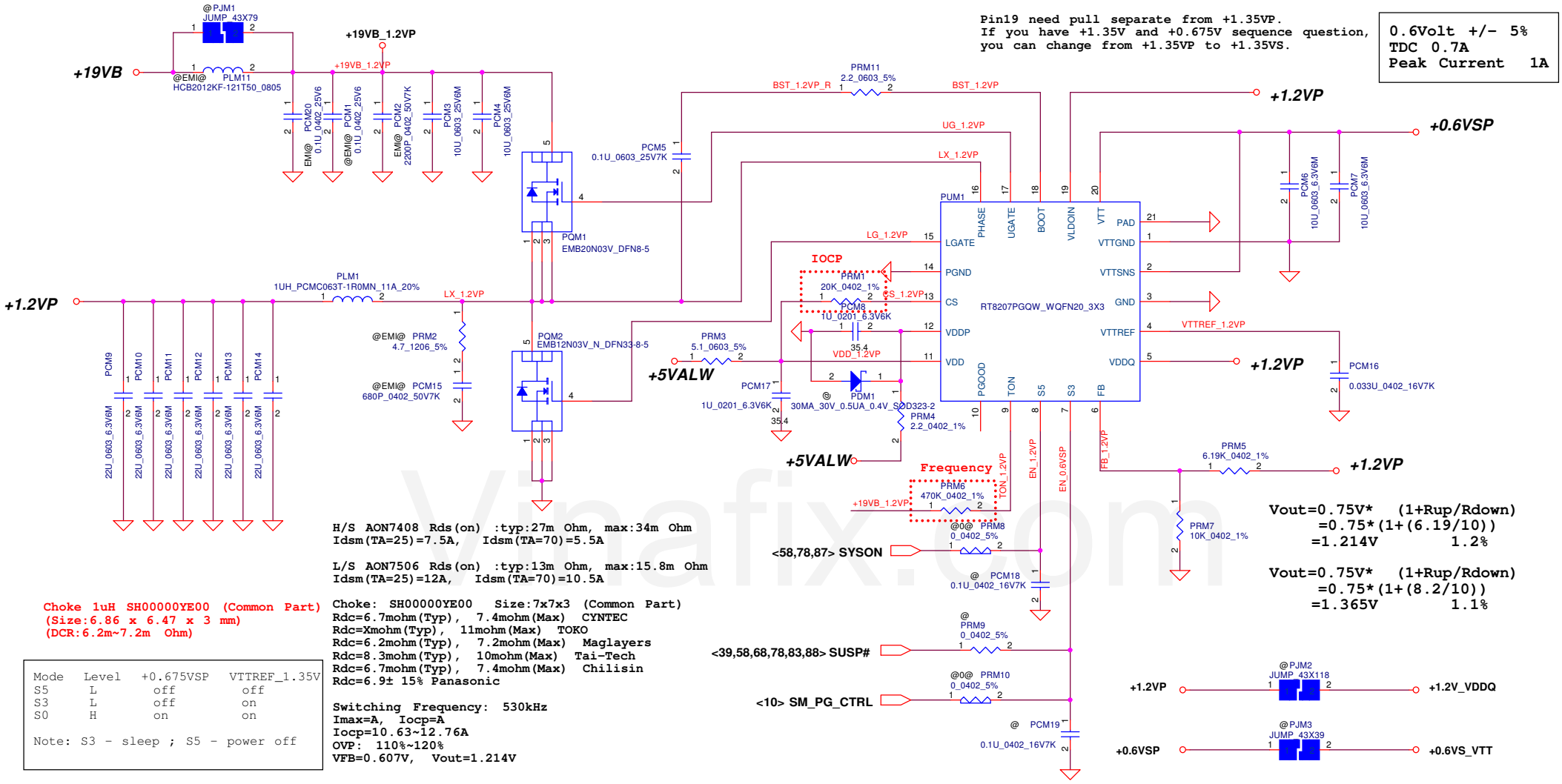
Security Classification	Compal Secret Data		
Issued Date	2017/11/15	Deciphered Date	2019/11/15

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size	Document Number	Rev
Custom	FH58F M/B LA-J251P	1.0

Date: Monday, August 12, 2019 Sheet 84 of 100



H/S AON7408 Rds(on) :typ:27m Ohm, max:34m Ohm
Idsm(TA=25)=7.5A, Idsm(TA=70)=5.5A

L/S AON7506 Rds(on) :typ:13m Ohm, max:15.8m Ohm
Idsm(TA=25)=12A, Idsm(TA=70)=10.5A

Choke: SH00000YE00 Size:7x7x3 (Common Part)
Rdc=6.7mohm(Typ), 7.4mohm(Max) CYNTEC
Rdc=Xmohm(Typ), 11mohm(Max) TOKO
Rdc=6.2mohm(Typ), 7.2mohm(Max) Maglayers
Rdc=8.3mohm(Typ), 10mohm(Max) Tai-Tech
Rdc=6.7mohm(Typ), 7.4mohm(Max) Chilisin
Rdc=6.9± 15% Panasonic

Switching Frequency: 530kHz
Imax=A, Iocp=A
Iocp=10.63~12.76A
OVP: 110%~120%
VFB=0.607V, Vout=1.214V

Choke 1uH SH00000YE00 (Common Part)
(Size:6.86 x 6.47 x 3 mm)
(DCR:6.2m~7.2m Ohm)

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

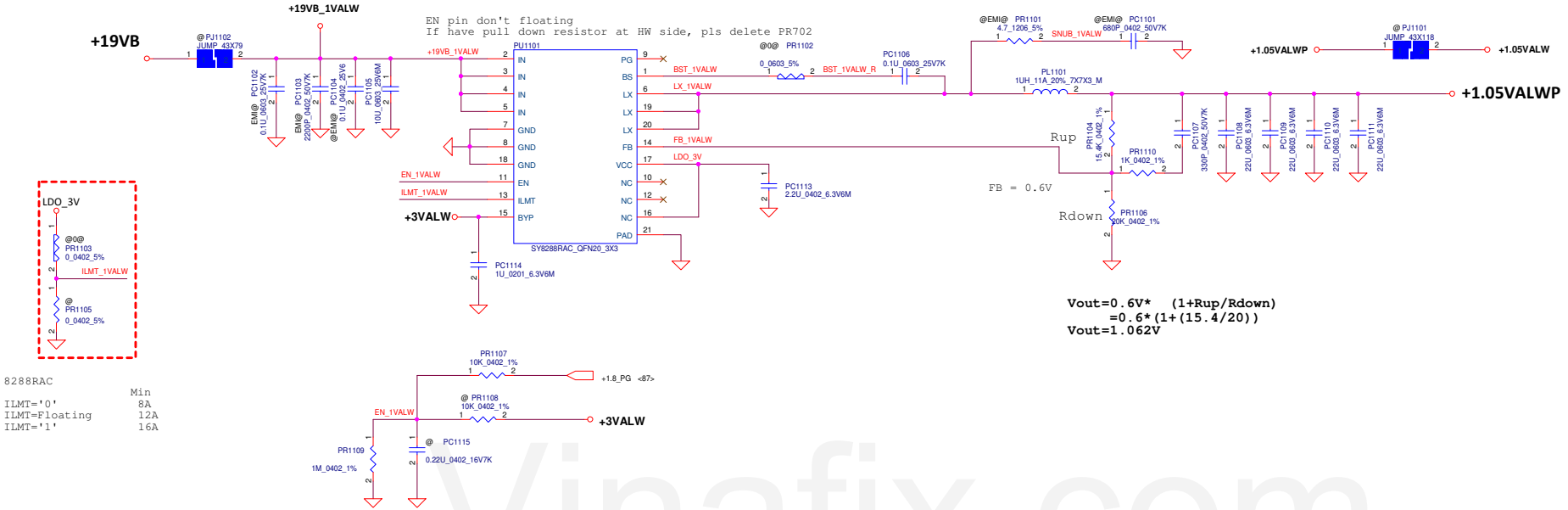
Compal Electronics, Inc.

Title: DDR4

Size: Custom | Document Number: FH58F M/B LA-J251P | Rev: 1.0

Date: Monday, August 12, 2019 | Sheet 85 of 100

Choke 1uH SH00000YE00 (Common Part)
(Size:6.86 x 6.47 x 3 mm)
(DCR:6.2m~7.2m Ohm)
Choke: SH00000YE00 Size:7x7x3 (Common Part)
Rdc=6.7mohm(Typ), 7.4mohm(Max) CYNTEC
Rdc=Xmohm(Typ), 11mohm(Max) TOKO
Rdc=6.2mohm(Typ), 7.2mohm(Max) Maglayers
Rdc=8.3mohm(Typ), 10mohm(Max) Tai-Tech
Rdc=6.7mohm(Typ), 7.4mohm(Max) Chilisin
Rdc=6.9± 15% Panasonic



8288RAC

	Min
ILMT='0'	8A
ILMT=Floating	12A
ILMT='1'	16A

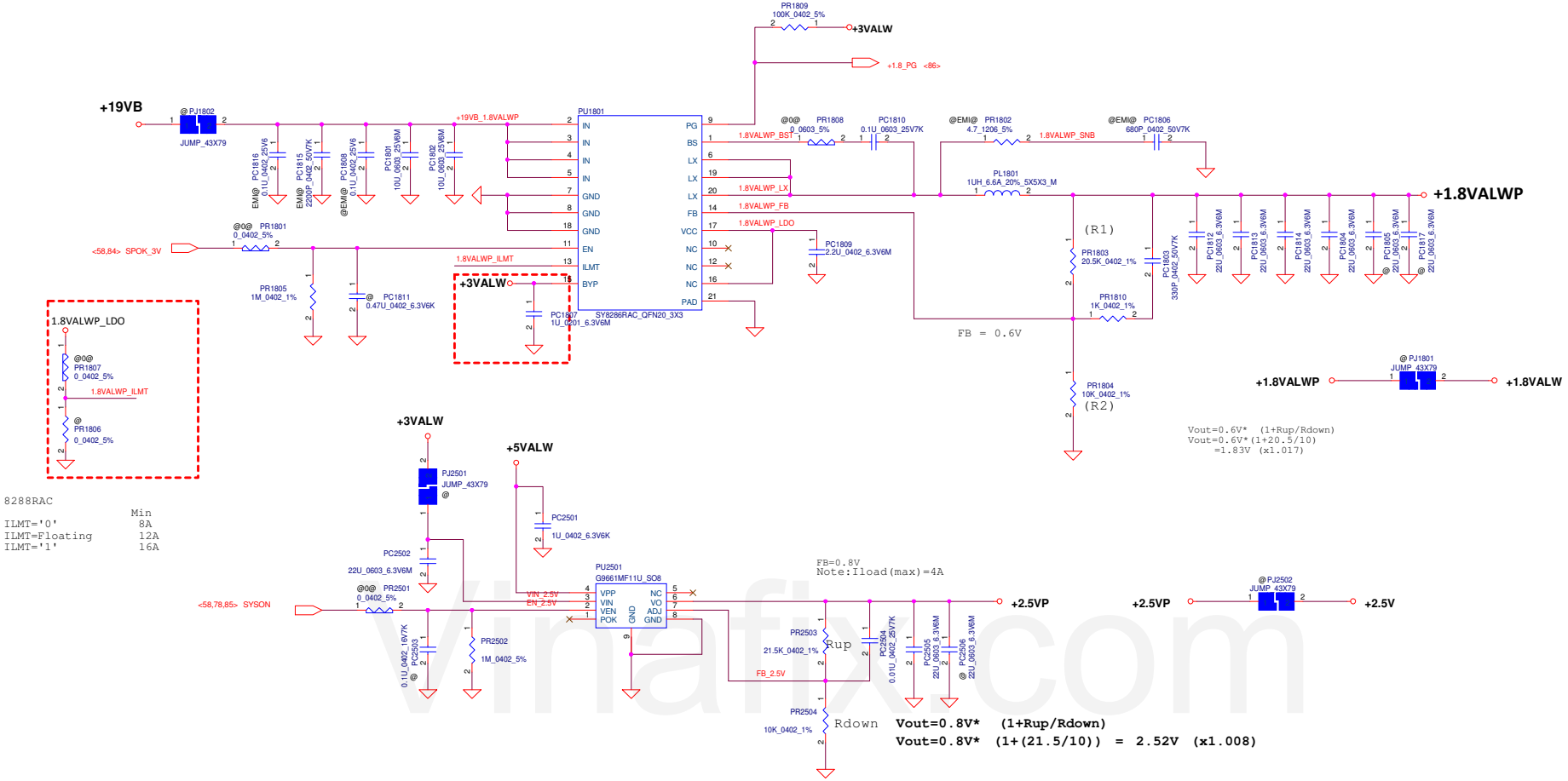
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

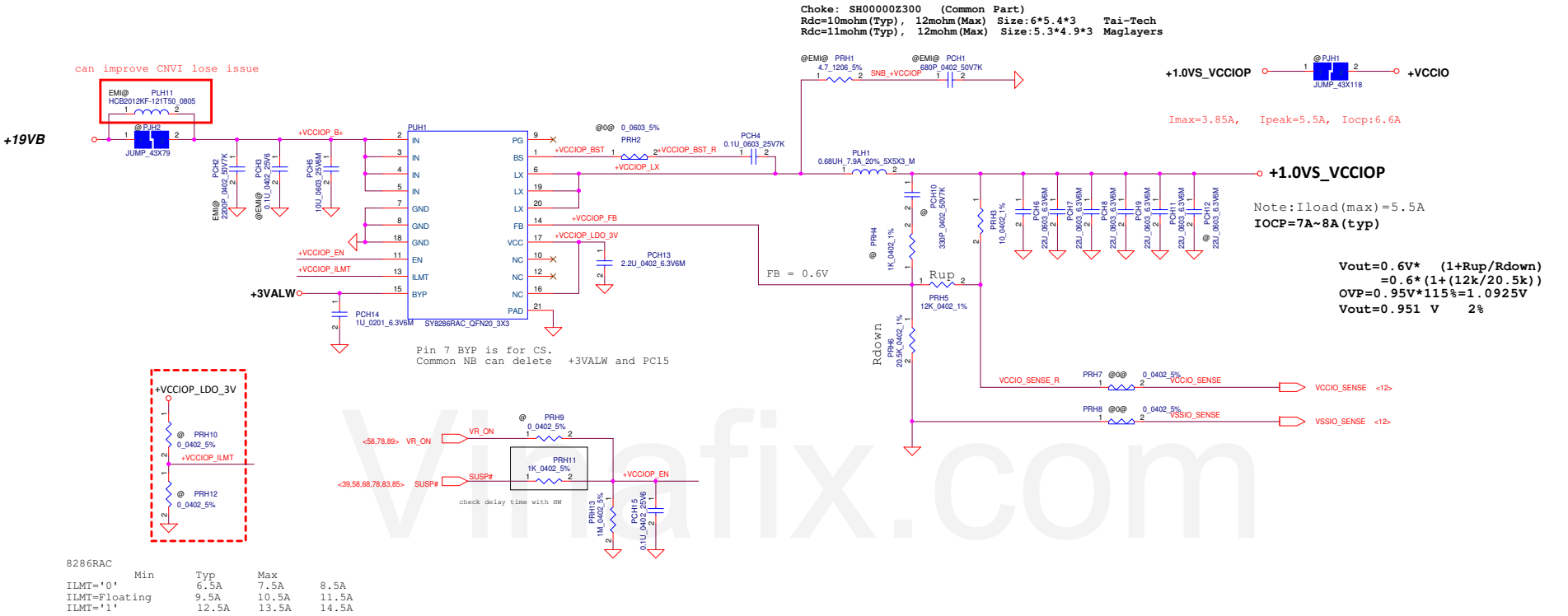
Title: 1V

Size	Document Number	Rev
C	FH58F M/B LA-J251P	1.0

Date: Monday, August 12, 2019 Sheet 86 of 100



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/11/23	Deciphered Date	2017/12/31
Title	1.5VS/2.5V		
Size	Document Number		Rev
	FH58F M/B LA-J251P		1.0
Date:	Monday, August 12, 2019	Sheet	87 of 100



8286RAC

	Min	Typ	Max	
ILMT='0'		6.5A	7.5A	8.5A
ILMT=Floating		9.5A	10.5A	11.5A
ILMT='1'		12.5A	13.5A	14.5A

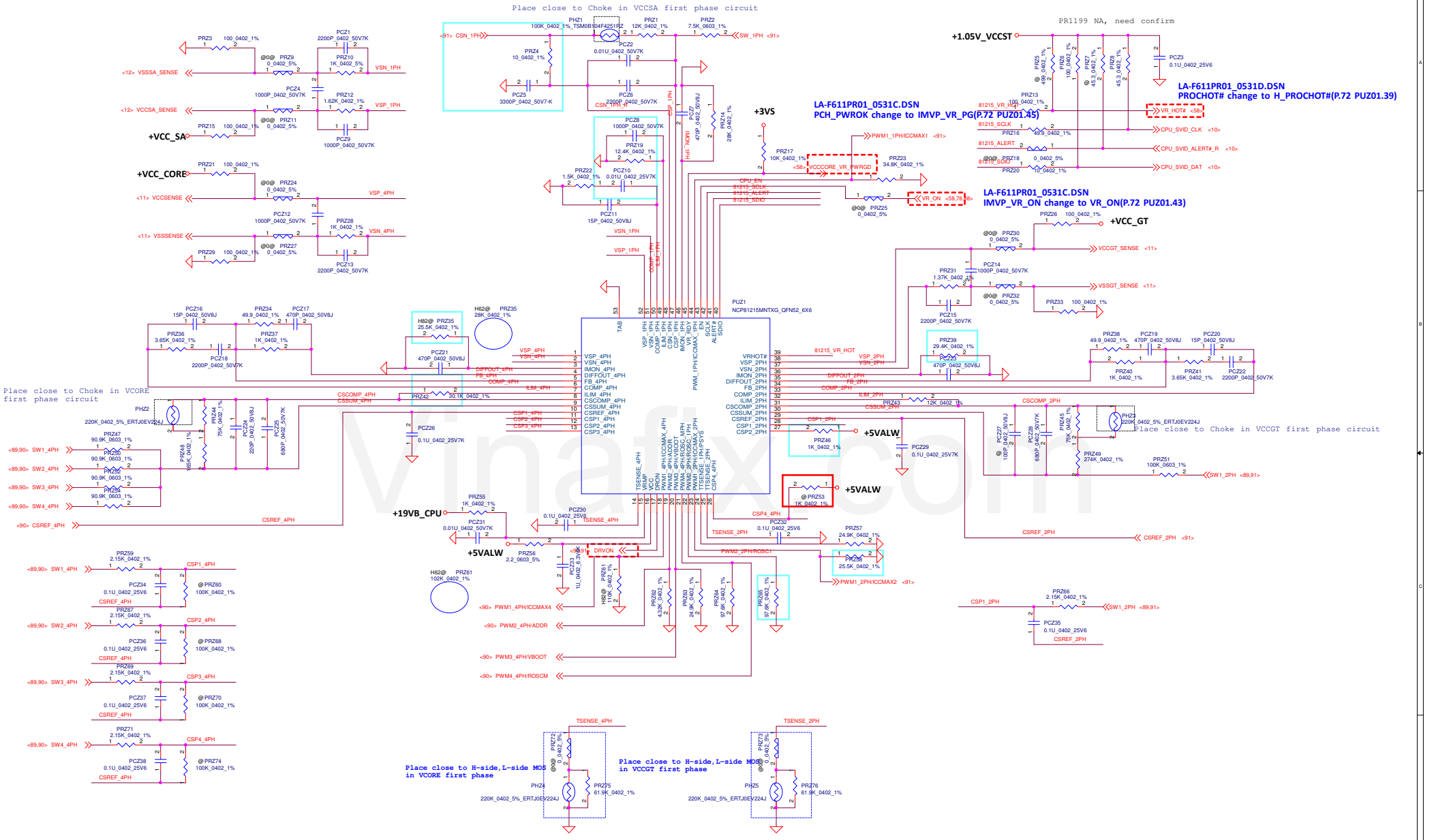
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: FH58F M/B LA-J251P

Size	Document Number	Rev
C	1.0VS_VCCIO	1.0

Date: Monday, August 12, 2019 Sheet 88 of 100



Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

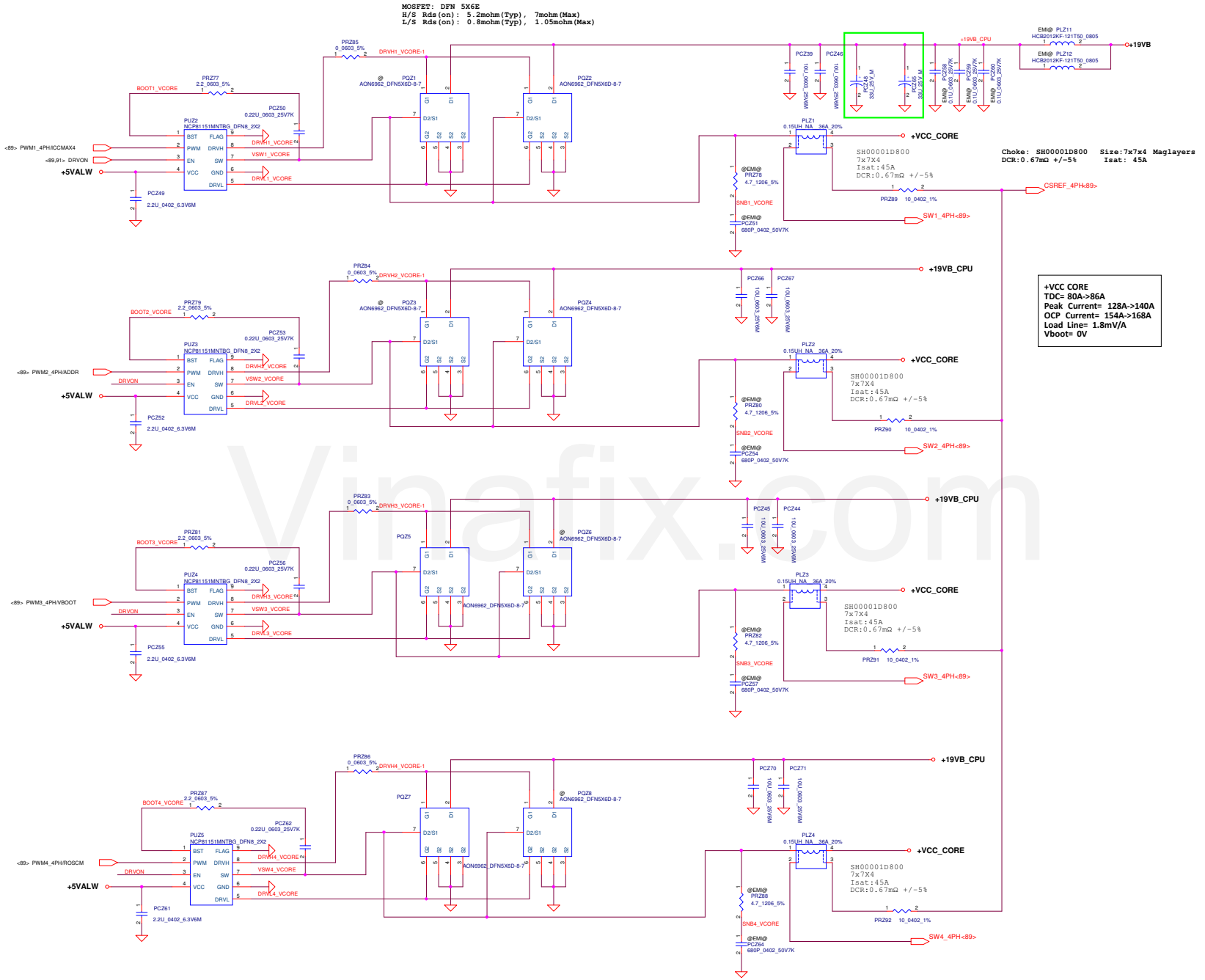
Compal Electronics, Inc.

Title: CPU IC

Size: Custom | Document Number: SKL_H 42 | Rev: 1.0

Date: Monday, August 12, 2019 | Sheet 89 of 100

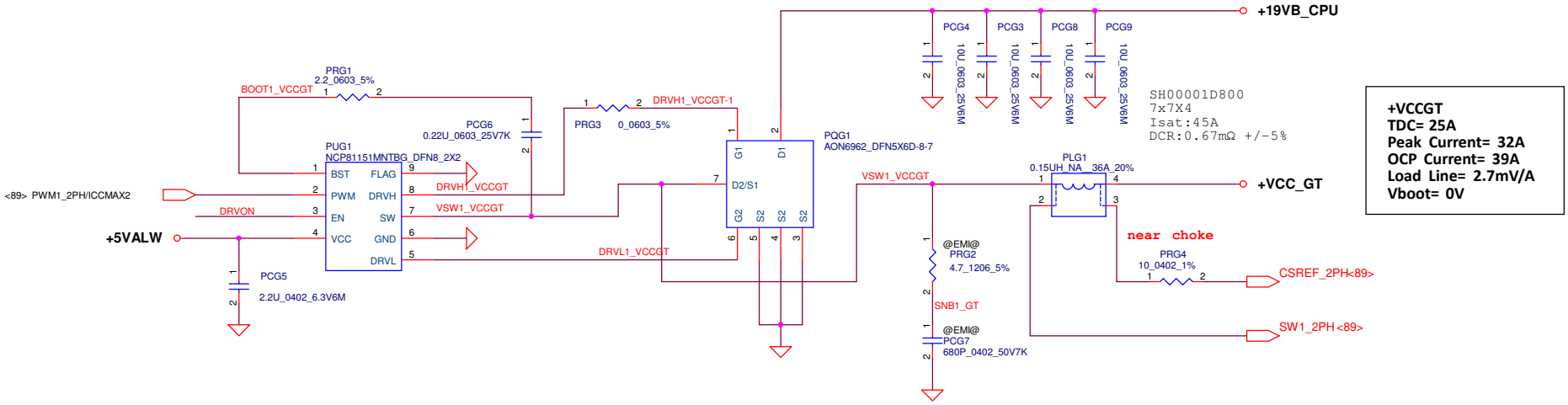
Main Func = CORE



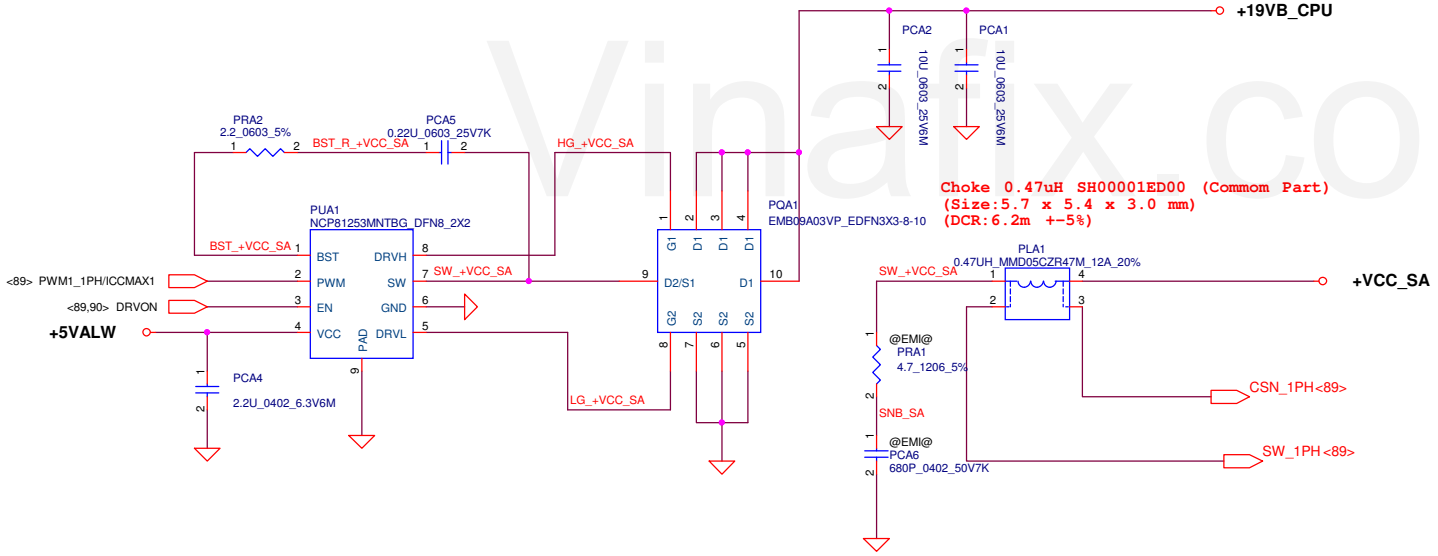
Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

Title	CPU_CORE		
Size	Document Number		Rev
Custom			1.0
Date:	Monday, August 12, 2019	Sheet	90 of 100

Main Func = VCCGT/+VCCSA



+VCCGT
TDC= 25A
Peak Current= 32A
OCP Current= 39A
Load Line= 2.7mV/A
Vboot= 0V



+VCCSA
TDC= 10A
Peak Current = 11A
OCP Current= 13A
Load Line= 10.3mV/A
Vboot= 1.05V

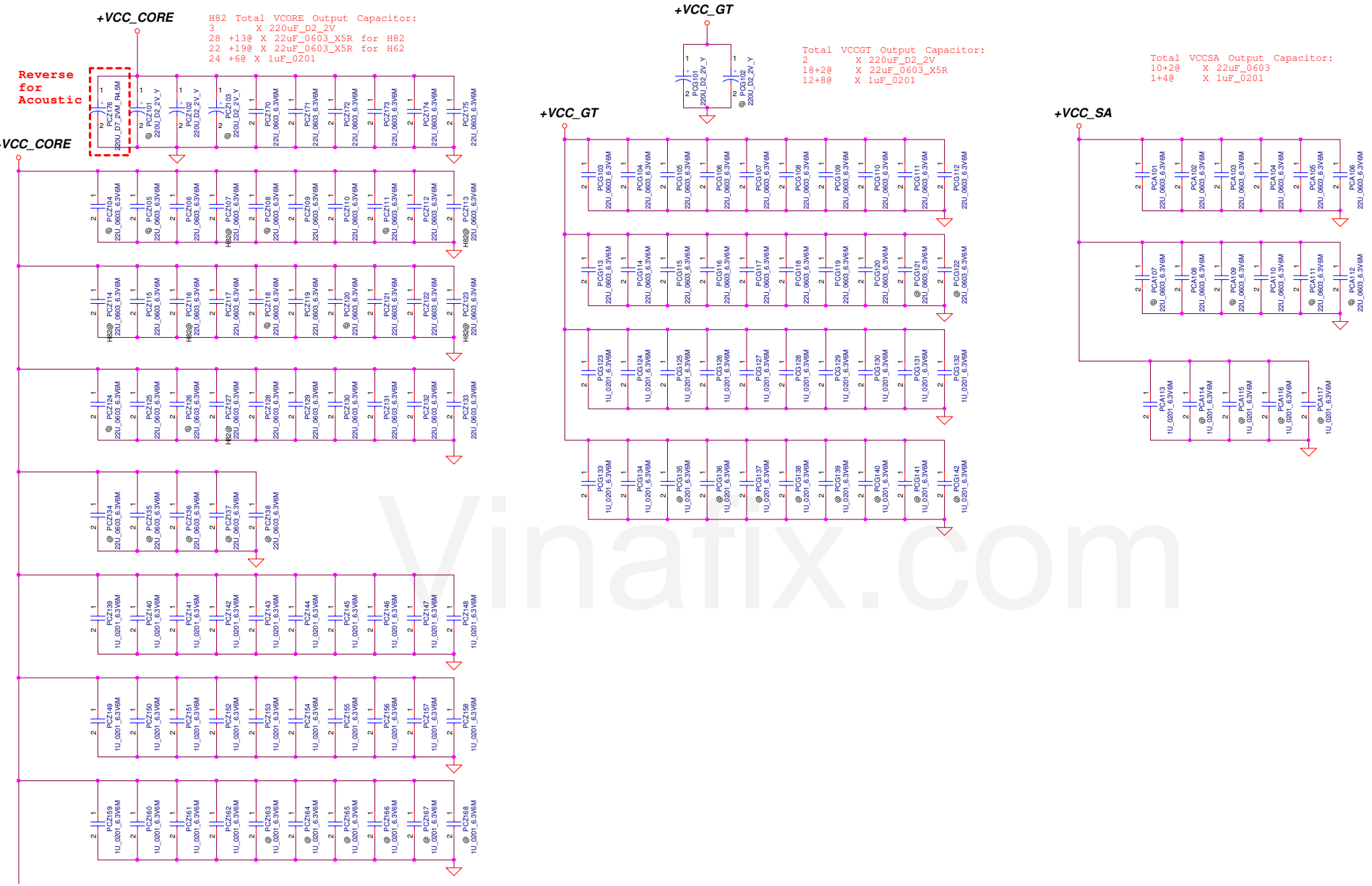
Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: +VCC_GT/+VCC_SA

Size | Document Number: FH58F M/B LA-J251P | Rev: 1.0

Date: Monday, August 12, 2019 | Sheet 91 of 100



Security Classification	Compal Secret Data		
Issued Date	NA	Deciphered Date	2014/07/04

Compal Electronics, Inc.

Title: FH58F M/B LA-J251P

Size	Document Number	Rev
Custom		1.0

Date: Monday, August 12, 2019 Sheet 92 of 100

Samesung VRAM
When,VRAM_VDD_CTL=High
Vboot=Vref*R2/(R1+R2+80)
=2*35.7K/(10K+35.7K+80)
=1.56V
When,VRAM_VDD_CTL=Low
Vboot=Vref*R2/(R1+R2+80)
=2*(35.7K//52.3K)/(10K+(35.7K//52.3K)+80)
=1.356V

Micron & Hynix VRAM
When,VRAM_VDD_CTL=High
Vboot=2*30.9K/(10K+30.9K+80)
=1.51V
When,VRAM_VDD_CTL=Low
Vboot=2*(30.9K//68.1K)/(10K+(30.9K//68.1K)+80)
=1.36V

MOSFET: DFN 5X6E
H/S Rds(on): 5.2mohm(Typ), 7mohm(Max)
L/S Rds(on): 0.8mohm(Typ), 1.05mohm(Max)

+1.35VSDGPU
TDC 14A
Peak Current 20A
OCP current 30A
fsw=400kHz

13X8X4
Isat:55A
DCR:1.3mΩ (+/-5%)

for cost 輸後再把30U 改 回 20

Rcost for 75.6A

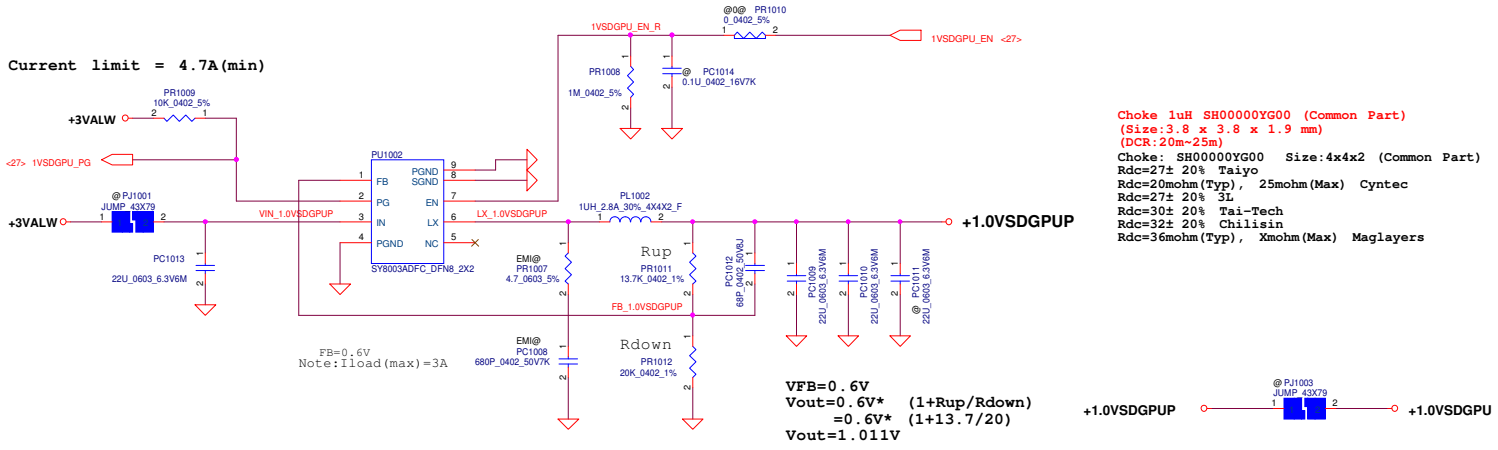
Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

Compal Electronics, Inc.

Title: PWR_+1.5VRAM

Size | Document Number: SKL_H 42 | Rev: 1.0

Date: Monday, August 12, 2019 | Sheet 93 of 100



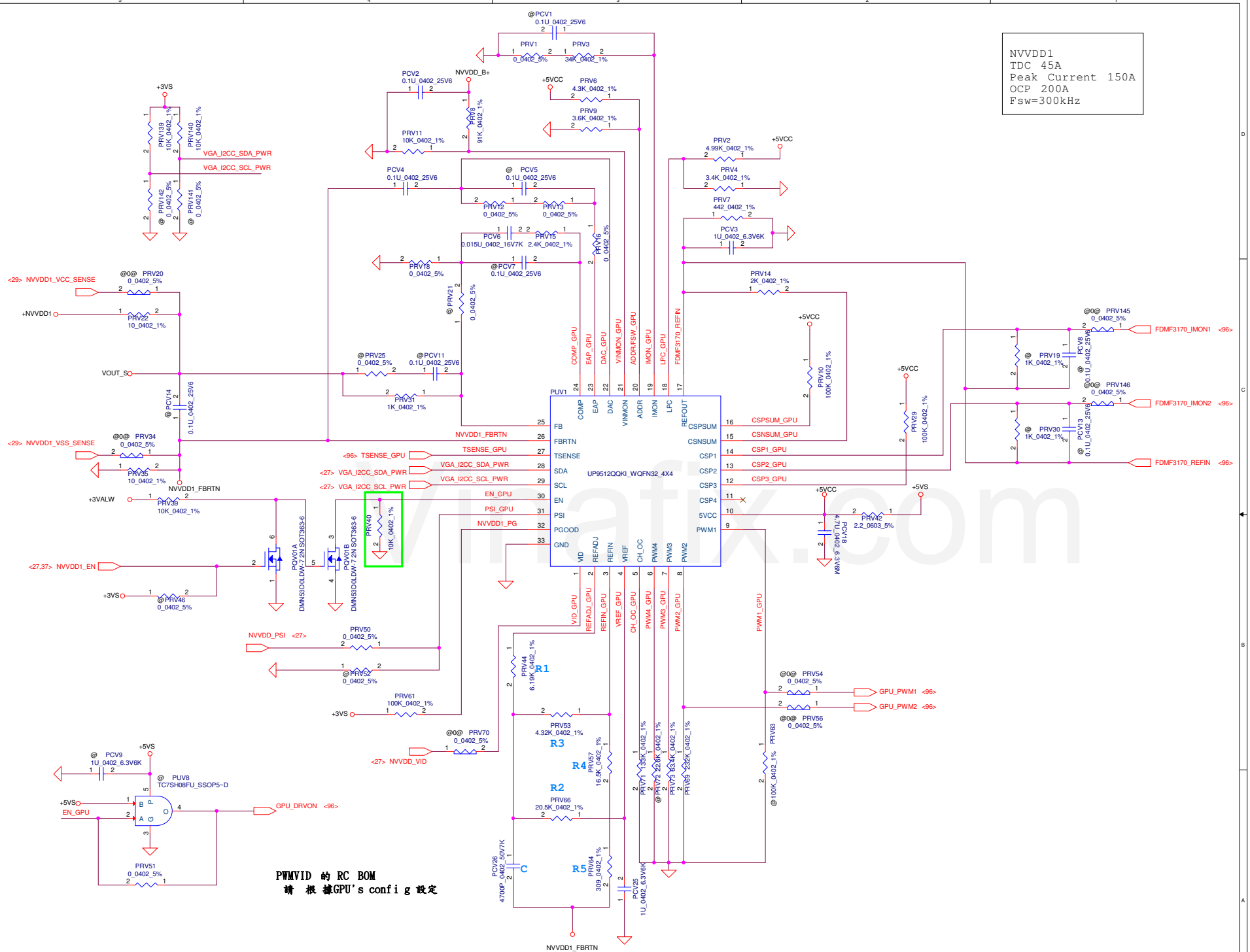
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: 1.05VSDGPU

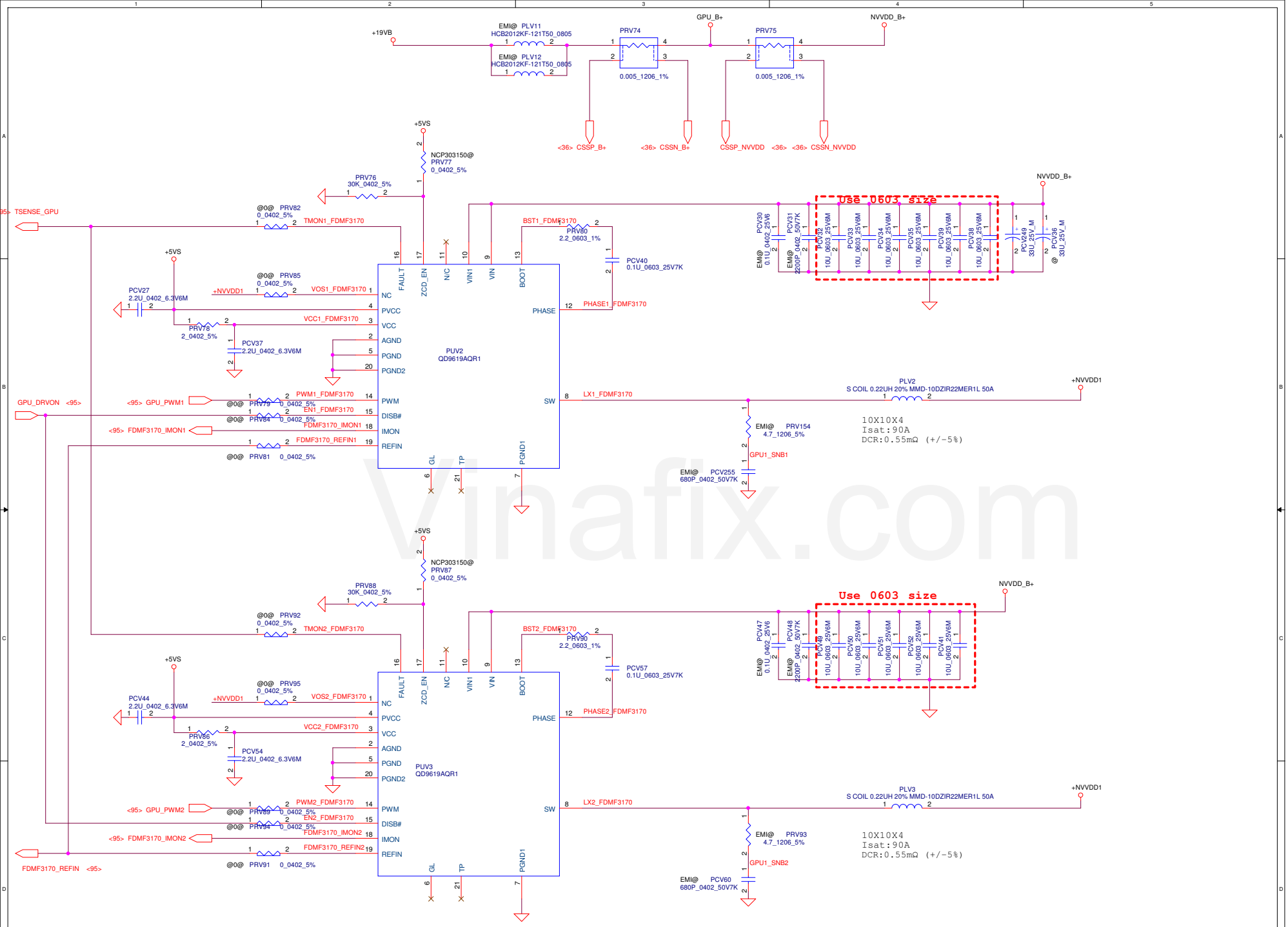
Size	Document Number	Rev
C	FH58F M/B LA-J251P	1.0

Date: Monday, August 12, 2019 Sheet 94 of 100



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title: PWR_VGA_UP9512P			
Size	Document Number: FH58F M/B LA-J251P		Rev: 1.0
Date: Monday, August 12, 2019		Sheet 95 of 100	

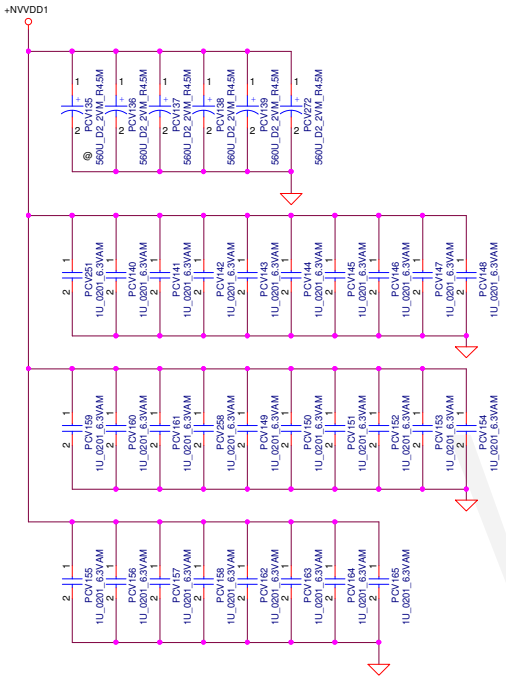


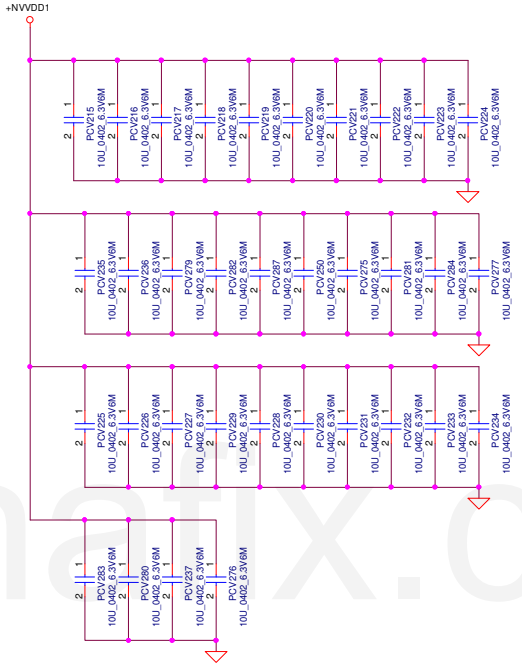
Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

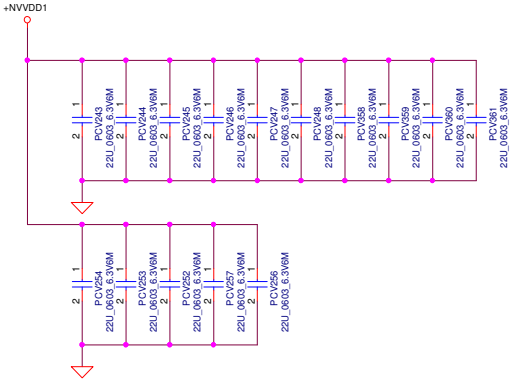
Compal Electronics, Inc.	
Title	PWR_+NVVDD1
Size	Document Number: FH58F M/B LA-J251P
Rev	1.0
Date: Monday, August 12, 2019	Sheet 96 of 100

N18P-G0
+NVVDD
560uF X 5
22uF_0603 X 15
10uF_0402X 34
1uF_0201 X 28

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4B-256 Package				
NVVDD		Varies	185 X 0.47uF (0201W X6S) 23 X 10uF (0603 X6S) 4 X 22uF (0805 X6S) 3 X 47uF (0805 X6S)	2 X 470uF (Poscap)
FBVDDQ (GPU side)[1]		1.25V 1.35V 1.5V 1.55V	48 X 0.47uF (0201 X6S) 5 X 10uF (0603 X6S)	7 X 10uF (0603 X6S) 9 X 22uF (0603 X6S)







Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR_VGA DECOUPLING

Size | Document Number: FH58F M/B LA-J251P | Rev: 1.0

Date: Monday, August 12, 2019 | Sheet 97 of 100

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 98 of 100	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.		
Title: N18E-GDDR6_D		
Size	Document Number: FH58F M/B LA-J251P	Rev: 1.0
Date: Monday, August 12, 2019	Sheet 99 of 100	

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
01	Design Update	For EA Turning and HW sequence	93, 94 95, 97 89, 92	change PR1009 from 100K_0402_5% (SD028100380) to 10K_0402_5% (SD028100280) change PG pull high from +3VS to +3VALW change PRW1 from 20K_0402_1% (SD034200280) to 1K_0402_1% (SD034100180) Change the PCW27 from pop to un-pop, and . PCW27.2 net name change from +1.35VSDGPU to Vsense_+1.35VS_VGAP. unpop PCV135 Change the PUV8, PCV9 from pop to un-pop. Add location PRV51 0_0402_5% (SD028000080), and pop. Change the PCW21, PCW22 From 4700P_0402_50V (SE074472K80) to 2200P_0402_50V(SE074222K80). Delete PL1111 (HCB2012KF-121T50_0805)	11/14	A
02	Design Update	solution change	83, 85 90, 91	Change the PQB2,PQM2 from AON7506 (SB000010A00) to EMB12N03V (SB00001HV00) update location PRG5 PRA3 to PUG1 PUA1 PLZ1,PLG1,PLZ2,PLZ3,PLZ4 change to common part P/N (SH00001EE00) pop PQZ2, PQZ4 unpop PQZ1, PQZ3	11/16	A
03	Design Update	0 ohm to R-short	83, 85 90, 91	Change PRM10, PRM8, PRV82, PRV85, PRV92, PRV95, PRV79, PRV81, PRV84, PRV89, PRV91, PRV94, PRV54, PRV56, PRV70, PRV145, PRV146, PRZ72, PRZ73, PRZ25, PRZ30, PRZ32, PRZ18, PRZ9, PRZ11, PRZ24, PRZ27,PRV20, PRV34	11/16	A
04	Design Update	For CPU transient	89, 92	change PRZ12 from 1.78K_0402_1%(SD00000WY80) to 1.62K_0402_1%(SD000003380) change PRZ14 from 31.6K_0402_1%(SD034316280) to 28K_0402_1%(SD034280280) change PCZ24 from 470P_0402_50V8J(SE071471J80) to 220P_0402_50V8J(SE082221J80) change PRZ51 from 84.5K_0603_1%(SD014845280) to 100K_0603_1%(SD014100380) PRZ61=110k ohm @H82, PRZ61=102k ohm @H62 PRZ35=25.5k ohm @H82, PRZ35=28k ohm @H62 unpop PCZ101, PCZ103, PCG102 pop PCZ176 un pop PCZ120, PCZ104, PCZ105, PCZ118, PCZ111, PCZ108, PCZ126, PCZ124 for H82 un pop PCZ120, PCZ104, CZ105, PCZ118, PCZ111, PCZ108, PCZ126, PCZ124, PCZ123, PCZ127, PCZ107, PCZ113, PCZ116, PCZ114 for H62	11/19	A
05	Design Update	solution change	84	Change the PL501 1.5uH to common part Change the PCZ47, PCZ48, PCZ65, PCV36, PCV249 from 33U_25V_NC_6.3X4.5 (SF000007200) to 33U_25V_M (SF000007700) Chnage the PRZ43 from 12.1K_0402_1% (SD034121280) to 12K_0402_1% (SD034120280)	12/3	A
06	Design Update	solution change	87	unpop PC1811 0.47U_0402_6.3V6K (SE124474K80)	12/12	B
07	Design Update	solution change	83, 97	pop PCV149~PCV158, PCV162~PCV165, PCV258 (1U_0201_6.3V6M) reserve PDB2 for dead battery	12/18	B
08	Design Update	solution change	87, 93, 94	Change PR1010, PRW9, PR1801, PR2501 from 0ohm to r-short	12/18	B
09	Design Update	For ESD request	82	Pop PC205 0.1U_0603_25V7K (SE042104K80) HS 鐵鋁皮鐵ESD 能量透過 HS小板及HS cable coupling到板造成	1/15	B
10	Design Update	For EMI request	93, 96	Pop PCW1, PCV48 2200P_0402_50V7K (SE074222K80) for EMI request Pop PCW2, PCV47 0.1U_0402_25V6 (SE00000G880) for EMI request	1/15	B

Compal Electronics, Inc.
Title: PIR
Size: Custom | Document Number: FH58F M/B LA-J251P | Rev: 1.0
Date: Monday, August 12, 2019 | Sheet 100 of 100

Version change list (P.I.R. List)

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	6	Chipset	11/14	Update CPU,PCH,GPU PN.		DVT	0.2
2	43,68,71,72	Source	11/14	Change material source.	1.Change CS95,CM3,CM20,CS5,CS111 to SGA00003700.	DVT	0.2
3	58	EC	11/14	Design change.	1.Add CB14 on EC_RST#.	DVT	0.2
4	27,37	GPU	11/14	Design change and fine tune sequence.	1.Remove RV397, pop RV335. 2.Reserve CV400, change RV106 to 100kohm. 3.Change RV105 to 10kohm, CV197 to 0.22uF, depop DV4. 4.Change RV22 to 200kohm. 5.Change UV45,UV48 to SA000070V00.	DVT	0.2
5	66	Sensor	11/15	Design change.	1.Remove R39,R40,C41,U6.	DVT	0.2
6	58	EC	11/16	Board ID.	1.Change RB3 to 12kohm.	DVT	0.2
7	43,56	Source	11/16	Change material source.	1.Change CS13 to SE00000X200,0603 size. 2.Change DS19 to SCA00004500. 3.Change LA4,LA5 to SM01000BW00. 4.Change UF2 to SA000067P00. 5.Change QV3,QV4 to SB00001GC00. 6.Change UH3 to SA00000OH00. 7.Change UC3 to SA00007WE00.	DVT	0.2
8	32	VRAM	11/19	For N17P-G0-K1 SKU.	1.Change UV4 related component BOM structure to VRAM4G@.	DVT	0.2
9			11/20	Design change.	1.Change RV338,RH94,RH96,RH99,RH101,RH102,RH103,RH105,RX8,RX9 to R-short.	DVT	0.2
10	67	HDD	11/20	Follow DVR1012,HDD CONN P11 pull-down.	1.Add RO25, remove T211.	DVT	0.2
11	10	ESD	11/21	For ESD request.	1.Add CC101,CC102,CC103, change CD10 to 33pF and pop.	DVT	0.2
12	27,51	Crystal	11/21	By Crystal EA result.	1.Add RL14, change CL21,CL22 to 18pF. 2.Change RV80 to 470ohm, CV1,CV2 to 18pF.	DVT	0.2
13	43	TYPEC	11/23	Update CONN symbol.	1.Change JTYPEC1 to DC23300RC00.	DVT	0.2
14	42,43,58	TYPEC	12/18	Follow 2018 Type-C spec.	1.Remove RS127, add US14. 2.Remove TYPEC_1P5A net from PCH. 3.Add TYPEC_1P5A_EC net from EC. 4.Add RS137.	DVT	0.3
15	36	GPU	12/18	OVRM issue.	1.Change RV399 power source to +3VLP. 2.Change RV345~RV348,RV370,RV371,RV372,RV374 power rail to +3V_OVRM. 3.Add QV16,RV400,OVRM_EN net to EC/PCH, reserve RH261.	DVT	0.3
16	58	EC	12/18	Update board ID.	1.Change RB3 to 15k.	DVT	0.3
17			12/27	Design change.	1.Change RA7,RQ1,RQ2,RQ3,RQ4,RQ8,RV352,RV353,RV356,RV358,RV362,RV364,RV365,RV382,RM53 to R-short.	PVT	1.0
18	63,77	ESD/EMI	01/03	For ESD/EMI request.	1.Reserve DK2,CK6,CK7 for ESD. 2.Add SPRING1~3 for EMI.	PVT	1.0
19	58	EC	01/03	Update board ID.	1.Change RB3 to 20k.	PVT	1.0
20	66	ESD	01/31	For ESD request.	1.Add C60.	PVT	1A

Compal Electronics, Inc.
Title: PIR-HW1
Size: Custom | Document Number: FH58F M/B LA-J251P | Rev: 1.0
Date: Monday, August 12, 2019 | Sheet 101 of 101